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A Silicon *p-i-n* Detector for a Hybrid CMOS Imaging System

Christopher G. Shea

A Thesis Submitted
In Partial Fulfillment
of the Requirements of the Degree of
Master of Science
in Microelectronic Engineering

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Technology (RIT). All simulations were performed in the Very Large Scale Integration (VLSI) Laboratory and all device fabrication was completed in the Semiconductor & Microsystems Fabrication Laboratory (SMFL), both at RIT. All photo-masks for the project were written in house at the SMFL, thanks to Mr. Thomas Grimsley.

Deposition of indium as the bump bond metal was performed at Jet Process Corporation (JPC) in North Haven, CT using the jet deposition process. Lift-off and flip-chip bonding were performed at Smart System Technology & Commercialization Center (STC) in Canandaigua, NY, as well as final packaging and wire-bonding.

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Abstract

A fully depleted silicon p-*i*-n image sensor for a very low noise hybrid CMOS imaging system was simulated, fabricated, and electrically characterized. The image sensor was then bonded to the foundry fabricated CMOS circuitry to create the imaging system. SILVACO Atlas was used to simulate the steady state electrical operation of the device as well as the optical response. Revisions were made to an existing mask set to allow the use of both contact and projection lithography in the fabrication process. Significant process improvements were introduced to eliminate needless complexity and reduce leakage current from the previously reported 1.5×10^{-6} A/cm^2 below the goal of 2.2×10^{-9} A/cm^2. Following fabrication of the image sensors, electrical testing was performed to verify diode quality from leakage and lifetime measurements. A lift-off process was developed for thick metal layers used in the bump-bond hybridization process. Daisy-chain test parts were created to characterize the mechanical and electrical connections formed in the hybridization process. Fabricated p-*i*-n photodiode arrays were diced and hybridized to read-out integrated circuits using a flip-chip bump bond process with indium interconnects. Testing of hybridized devices is currently ongoing.

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Chapter 1

Introduction

The 2009 Nobel Prize in Physics was awarded to Willard S. Boyle and George E. Smith from Bell Labs for their 1969 invention of the charge-coupled device (CCD), a solid state image sensor that has led to many scientific discoveries and consumer applications. Image sensor technology has evolved dramatically throughout the years, introducing new technologies such as active pixels, complimentary metal-oxide-semiconductor (CMOS) image sensors and more recently the hybrid detector [1-8].

An imaging system contains several key components, including a photodetector, read-out circuitry, and a collection of optical elements. The photodetector is a transducer designed to convert an optical signal into an electrical signal. The material must have desirable electrical properties that can be modified by an optical signal. Semiconductors are perfectly suited to this task due to the profound effect electromagnetic radiation has on the material. The read-out circuitry accesses many different elements of a large array and conditions the signal for output. The optical system is responsible for collecting the light in the desired field of view, and focusing this light onto the image sensor, or focal plane.

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Image sensors have become an invaluable tool to astronomical research enabling the discovery of new phenomena and the confirmation of models. Imaging systems operating in the harsh environments of outer space must be able to perform at cryogenic temperatures and withstand high energy radiation. This thesis continued the development of a fully depleted silicon p-*i*-n image sensor and hybridization process for a hybrid CMOS focal plane array enabling future NASA space missions.

1.1. A Review of Photodetectors

There are several types of semiconductor based photodetectors including photoconductors, photodiodes, charge-coupled devices, and phototransistors. The devices are classified by their structure and the principles upon which they operate. In a photoconductor a single piece of homogeneous semiconducting material is contacted by ohmic connections and the resistivity is modulated by the optical signal. Photodiodes consist of a metallurgical junction in a semiconducting material that is reverse biased to sweep out photo-generated carriers to the collection terminals. Charge-coupled devices are a special type of detector where an array of gated capacitors is incorporated to collect photogenerated carriers. These carriers are then transferred to the edge of the device and read out as the charge is converted to a voltage. The phototransistor is a device that uses

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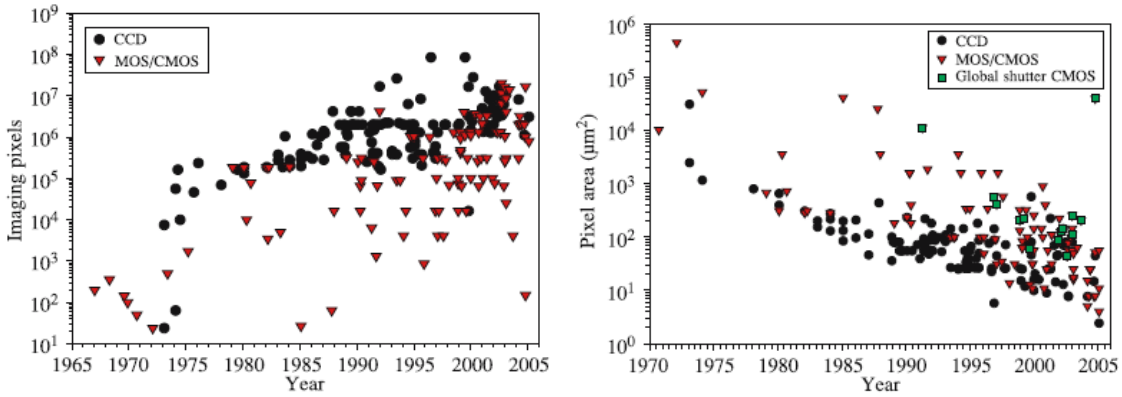
an optical signal to modulate gain of the transistor. Each device has advantages and disadvantages associated with the design and are suited to different applications.

A silicon p-*i*-n photodiode is similar to the ubiquitous p-n diode, except a nearly intrinsic region exists between the two highly doped terminals. In the reverse bias mode of operation, the entire intrinsic region is typically depleted providing a large volume for the photogeneration of carriers. One of the main advantages of the p-*i*-n photodiode is the thickness of the depleted intrinsic region can be tailored to optimize absorption at a desired wavelength. The absence of impurities in the depleted region and the use of high quality float zone silicon allow devices with extremely low leakage levels to be realized.

1.2. A Historical Perspective

Image sensors have developed very rapidly over the past five decades, helped enormously by the vast amount of research performed by the semiconductor industry. Using processes developed for integrated circuit manufacturing the image sensor industry has been able to shrink pixel size and increase total pixel counts at rates comparable to transistors in the IC industry. Luppino and Burke even created their own version of 'Moore's Law' stating pixel count and density would double every 2.5 years [2]. A graphical illustration of the trends can be seen in Fig. 1.1 a) and b) showing the pixel count and area for image sensors reported in IEEE publications [3].

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a) b)

Fig. 1.1 Data showing a) number of pixels and b) pixel area for imaging sensors reported in IEEE publications [3]

Like Moore's Law, this trend will eventually be faced by fundamental limitations restricting further growth. The number of pixels in a device is limited by the size of each pixel and the substrates used for manufacturing. Currently, most high grade scientific imagers are produced on 150 mm substrates, leaving the industry room for growth up to the current IC industry standard of 300 mm. The large areas required by the detectors however make defect densities a primary concern. The size of individual pixels is limited by the volume of detecting material required to produce a suitable signal for the sensing circuitry. The ability to prevent bleeding of a signal into adjacent pixels also limits the reduction of pixel area and becomes more difficult with increasing detector thickness.

1.3. Detector Materials

There are many different semiconducting materials that can be used as photodetectors. The structure of the material defines the fundamental properties of what

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types of radiation a material absorbs and how strongly it does so as shown by the absorption coefficient. An excellent illustration of the optical properties of various semiconductor materials shown in Fig. 1.2 is taken from Sze.

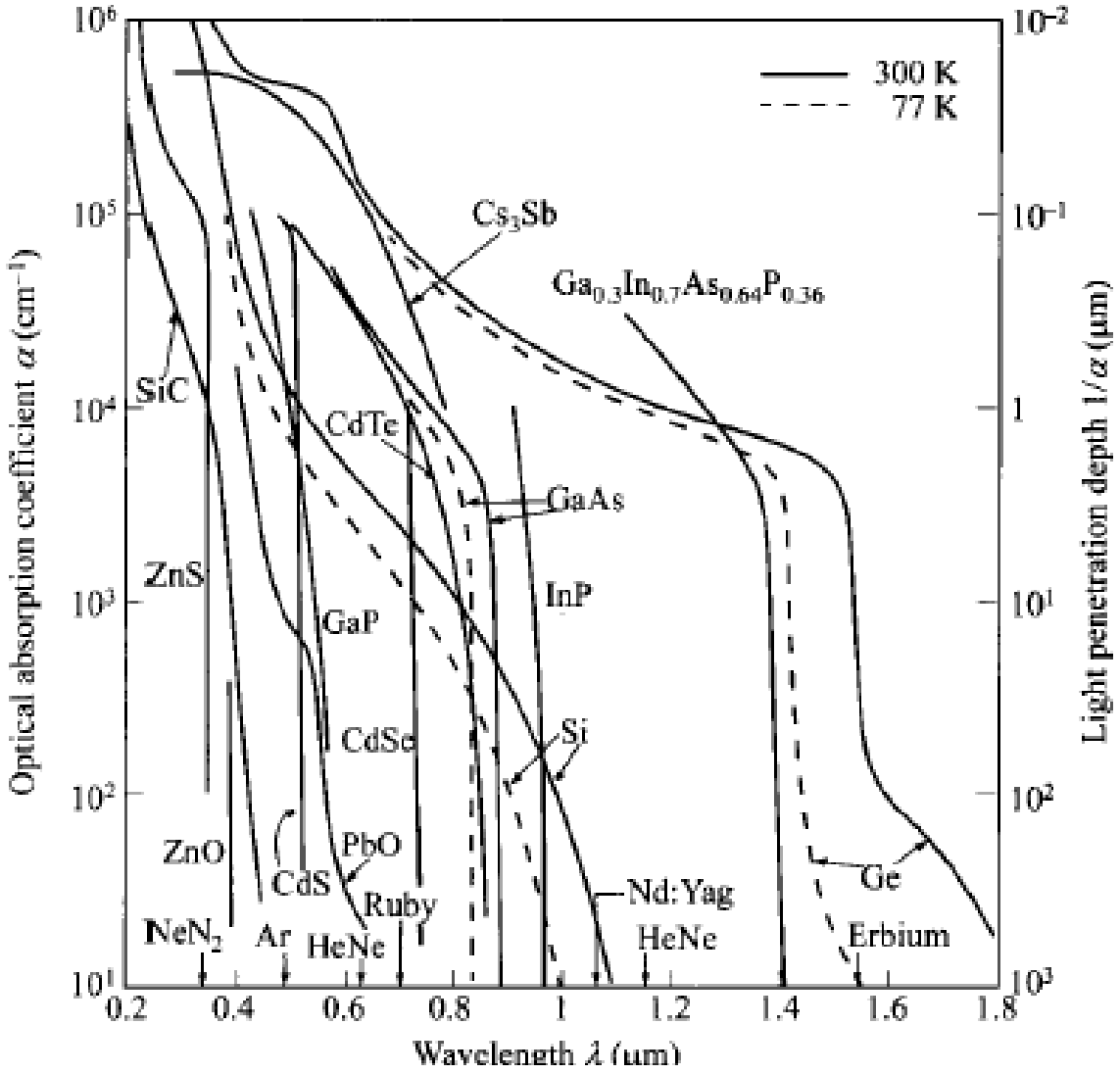


Fig. 1.2 Optical absorption coefficients for various semiconductor materials [4]

Silicon can be seen to absorb light at a reasonable rate (10^2 – 10^4 cm^{-1}) over a relatively wide range of photon wavelengths compared to other materials making, it an

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attractive material. Although germanium has an even higher absorption over a wider range of wavelengths, it has several drawbacks that limit its applications. The rarity of the material makes it considerably more expensive, and a smaller band gap creates much higher thermally generated noise. All work in this project was completed on ultra-high purity float zone silicon substrates. Float zone substrates are produced by passing an RF induction coil over a poly-Si rod, melting the material and inducing a single crystal growth. The absence of a crucible or any direct contact with melted Si, as found in traditional Czochralski grown substrates, reduces the introduction of carbon and oxygen impurities. The lower oxygen levels eliminate the need to form an oxygen depleted (denuded) zone resulting in consistent material properties throughout the thickness of the wafer.

1.4. Image Sensor Architectures

Image sensors can be classified based on the architecture at either the system level or the pixel level. The two types of system level architecture are monolithic and hybrid. A monolithically integrated image sensor contains both the active photodetector region and all circuitry necessary to convert the charge to a signal conditioned for output on a single substrate. In hybrid image detectors the active sensing region and readout circuitry are fabricated on separate substrates and the hybridization process makes the electrical

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connections between the two substrates. Hybrid detectors allow the substrate and fabrication processes for the image sensor and read out circuitry to be optimized separately, enabling ultra-low noise imaging systems that are highly sensitive and radiation hardened. The two types of pixel architecture are CCD and CMOS. The CCD is a more mature technology and the typical choice for most high end applications, although CMOS devices are steadily gaining market share.

1.4.1 CCD and CMOS Pixel Architectures

Charge-transfer devices were originally conceived as shift register devices [5], but their applications to image detection were readily apparent [6]. The main difference between the two architectures is the method of addressing the collected charge as shown in Fig. 1.3. In CCD's, overlapping gate structures serve to shift the charge to the edge of the array where it is read out, however in CMOS devices each pixel contains at least one transistor as an access device. Complex devices include additional transistors to amplify the signal and reduce noise. The use of CMOS processing also greatly eases process integration challenges of simultaneously fabricating logic circuitry in the periphery.

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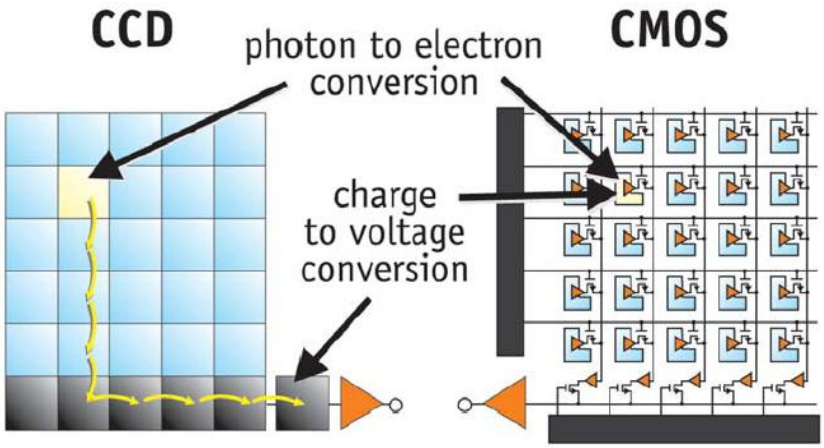


Fig. 1.3 Schematic representation of CCD and CMOS image sensors highlighting the differences of operation taken from [7]

Both architectures have their advantages and disadvantages. A summary of key aspects of the designs is provided in Table 1 [8]. Historically, CCD's are known for delivering a higher quality sensor although at a much higher price. CMOS sensors have benefited greatly from the advanced processing techniques developed by the memory and logic sectors making them extremely cost effective.

TABLE 1 SUMMARY COMPARISON OF CCD AND CMOS TECHNOLOGIES [8]

CCD Technology	CMOS Technology
Highly optimized for optical detection, special fabrication requirements	Benefits from advances in manufacture of high-volume digital products
Very high signal-to-noise	Noise typically higher
Low photoresponse nonuniformity (PRNU), low fixed-pattern noise (FPN)	High PRNU, high FPN, improved by gain and offset correction
Low dark current	Dark current typically higher
High power dissipation	Low power consumption
Complex driver electronics, no on-chip logic and digitization	Single power supply operation, digital output
Serial readout, no windowing capability	Random addressing capability

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Passive and Active CMOS Pixels

The type of pixel circuitry implemented in a CMOS sensor is an important aspect of system performance and can be used to categorize the device. The first designs were passive sensors that utilize a single transistor per pixel as an access device. Active sensors incorporate per-pixel amplification through the use of source-followers to greatly increase pixel performance [9]. Additional circuitry can further enhance device performance by reducing undesirable effects due to device variation and noise, however the additional transistors occupy precious real estate within the pixel [10]. The percentage of pixel area available for sensing incoming light is known as the fill factor. The two most prominent techniques used to mitigate the effects of reduced fill factors are discussed in the following sections.

1.4.2 System Architecture: Hybrid vs. Monolithic

The first image sensors were monolithically integrated CCD's based upon the charge transfer device conceived by Boyle and Smith. In a monolithic device, both the active sensing region and the read out circuitry are fabricated within the same substrate. This can require greater process complexity due to the vastly different doping requirements of the two regions. A top down micrograph of a typical monolithic CMOS image sensor is shown in Fig. 1.4 [11]. The sensor array is in the center and is

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surrounded by the logic circuitry used to select the rows and columns and condition the signal for output.

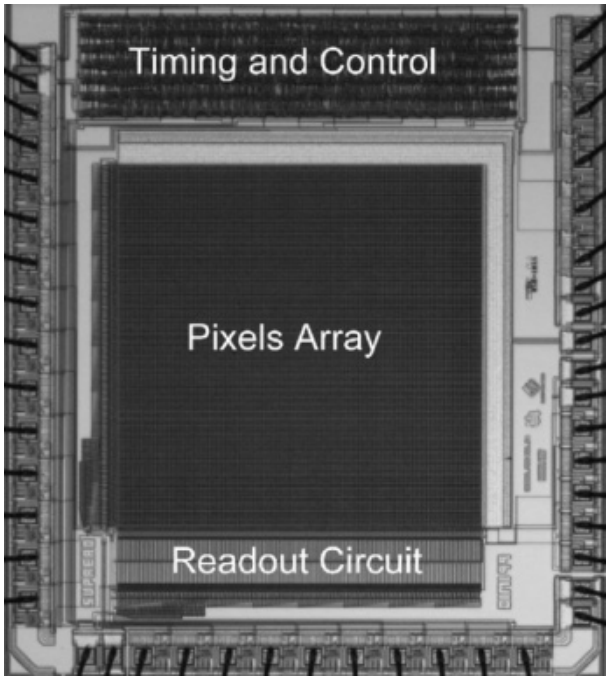


Fig. 1.4 Typical monolithic CMOS image sensor [11]

Front-side vs. Back-side Illumination

Topography and the use of opaque materials in the fabrication of image sensors leads to a loss signal before it reaches the photodetector due to absorption, reflection, and scattering. Transparent conductors such indium-tin-oxide (ITO) are often used to reduce the need for opaque metals, though imperfect and curved interfaces still cause some scattering of the light. This reduction of signal is enhanced even further in multi-transistor pixel designs with decreased fill factors, which are more common than older single transistor designs.

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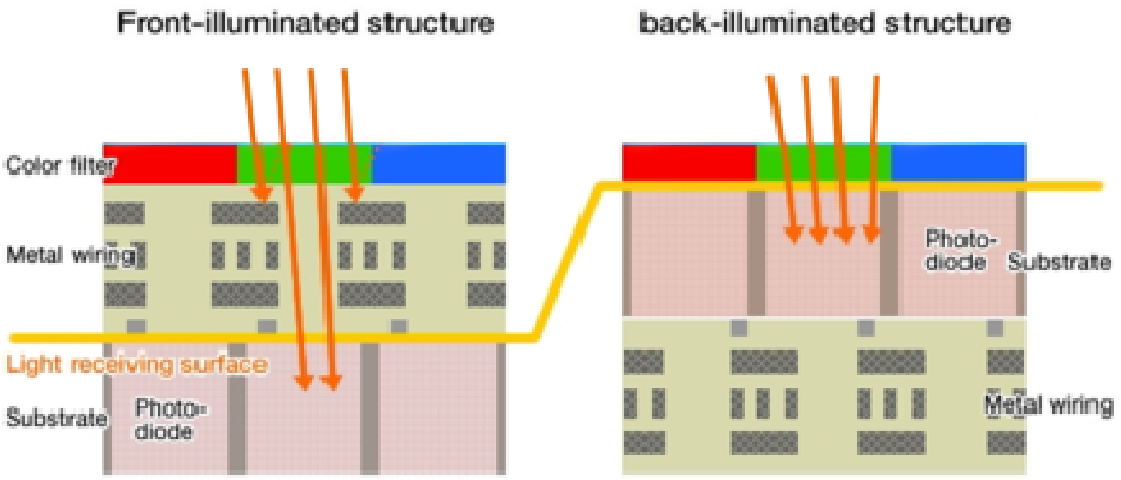


Fig. 1.5 Schematic representation of front-side illumination (FSI) vs back-side illumination (BSI) [12]

To eliminate virtually all possible sources of external light loss, one technique is to flip the substrate over after the processing of front-side is completed and illuminate the device from the back. This often requires additional processing, as most devices are fabricated in substrates too thick to allow light of sufficient intensities to penetrate into the depleted regions. The devices are can be thinned, taking special care to leave a high quality backside-surface to avoid the creation of defect states. Often specialty thinned and double side polished substrates are used for the creation of these devices. Anti-reflection layers are also used to almost completely eliminate all reflected light. A comparison of front-side illuminated (FSI) and back-side illuminated (BSI) structures is shown in Fig. 1.5.

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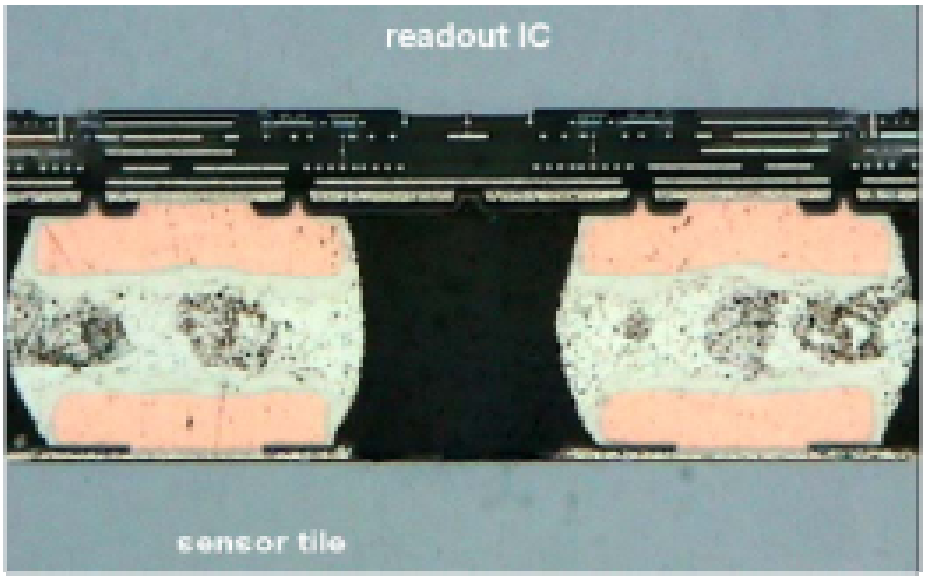


Fig. 1.6 Cross-section of hybrid imager used in ATLAS detector [13]

1.4.3 Hybrid Image Detectors

The development of advanced packaging techniques has enabled the creation of hybrid image detectors, where the sensor and readout circuit are fabricated on separate substrates and then connections are made between the two die. The large matrix of densely spaced interconnections between the substrates required for the pixel arrays makes traditional connections technologies such as wire-bonding and screen-printing incompatible. A lithographic pattern transfer combined with electroplating and lift-off processes have enabled large arrays of bumps to be formed with at a very fine pitch. A cross section of the hybrid sensor used in the ATLAS detector is shown in Fig. 1.6. Hybrid detectors are inherently back-side illuminated as the front-sides of the two chips are mated to each other. Wire-bond connections are made to the backside of the photo-

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diode to set the operating potential and the periphery of the read-out integrated circuit (ROIC) for communication.

Another large advantage of hybrid detectors is the ability use different substrates and fabrication sequences for the sensor and read out circuitry. The read-out circuitry requires high doping levels for radiation hardness, to prevent latch-up and maintain proper device operation. The sensor requires low doping levels to reduce leakage currents and increase the width of the space charge region.

1.5. APRA Imaging System

In 2006, the Rochester Imaging Detector Laboratory (RIDL) at the Rochester Institute of Technology (RIT) was awarded a grant from the National Aeronautic and Space Administration (NASA) for "A Very Low Noise CMOS Detector" under the Astronomy and Physics Research and Analysis (APRA) Program of the Science Mission Directorate [14]. The stated goal of the project from the grant proposal was "to design, fabricate, and measure the noise of a novel hybrid CMOS detector with ΣΔ (sigma-delta) pixel design at cryogenic temperatures." The initial plan called for the read out circuit to be fabricated through MOSIS, a low-cost prototyping and small-volume production service, and the detectors to be fabricated in the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at RIT.

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1.5.1 APRA Hybrid Imaging System

The APRA Hybrid imaging system was designed as a proof-of-concept device for astronomical purposes and was expected to meet the performance goals specified Table 2 [14]. A dark current of less than 1 e-/pixel/sec was desired at an operating temperature of 200 K from an 8-12 um pixel. To meet the performance goals, a hybrid architecture was designed with a silicon CMOS ROIC mated to a silicon p-*i*-n photodiode detector array using indium bump bonds.

TABLE 2 IMAGING SYSTEM PERFORMANCE GOALS [14]

Parameter	*Value*
Format	256x128
Pixel Size	8-12 μm
Read Noise	<1 e^- RMS
Dark Current (@200 K)	<0.1 e^-/s/pixel
QE[b]	>85%
Latent Image (after full well)	<1 e^-
Charge Rate Capacity	>10^8 e^-/s
Dynamic Range	>10^6
Operating Temperature	20 K – 300 K
Fill Factor	100%
Susceptibility to Radiation Damage	immeasureable[b]
Susceptibility to Radiation Transients	immeasureable
Maximum Frame Rate	1000 fps
Power (@30 fps)	<1 nW/pixel
Power (@0.1 fps)	<100 pW/pixel
Technology Readiness Level[c]	4

The ROIC design was modified to allow bump bond contacts and fabricated through a foundry service. The diodes were fabricated at the RIT SMFL and the hybridization process was developed in cooperation with the Smart System Technology

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& Commercialization Center (STC). A modest array size was chosen to reduce the negative impacts of poor reliability from immature processes on the proof-of-concept design. The pixel size was originally intended to be between 8-12 μm but was ultimately relaxed slightly to 15 μm due to lithographic constraints.

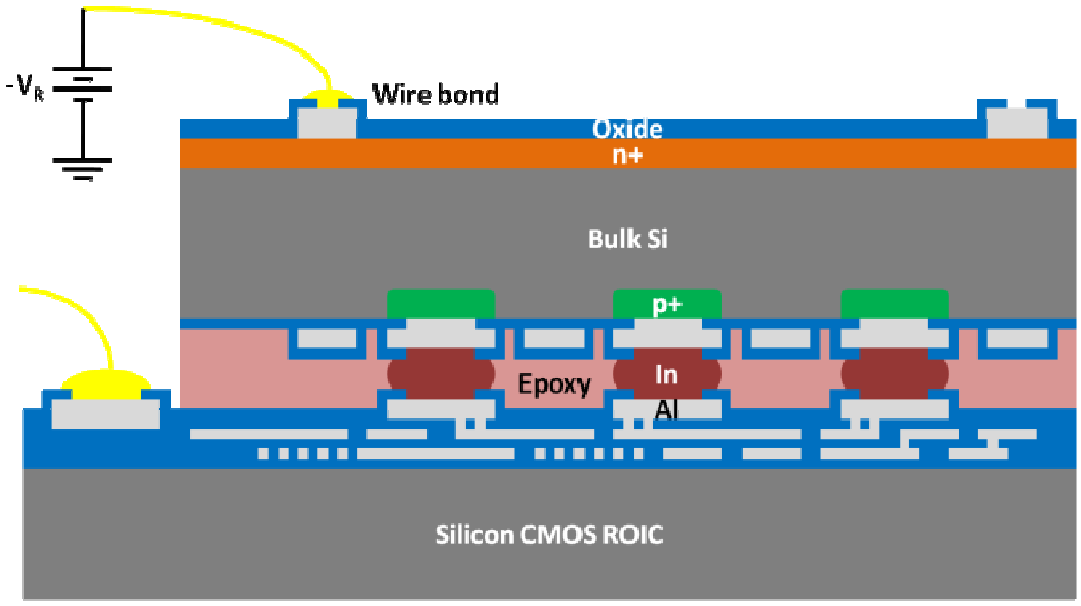


Fig. 1.8 Illustration of Hybridized Image Detector cross-section

Cross-section and top-down illustrations of the detector are shown in Fig. 1.8 and Fig. 1.9. Back-side illumination ensures a 100 % fill factor and the large depleted intrinsic region enables high quantum efficiencies throughout a wide range of wavelengths. The hybridization process uses techniques developed by the IC industry for flip chip packaging to create bump bond interconnects between the two chips. The gap is backfilled with epoxy to provide structural support and protection from environmental effects.

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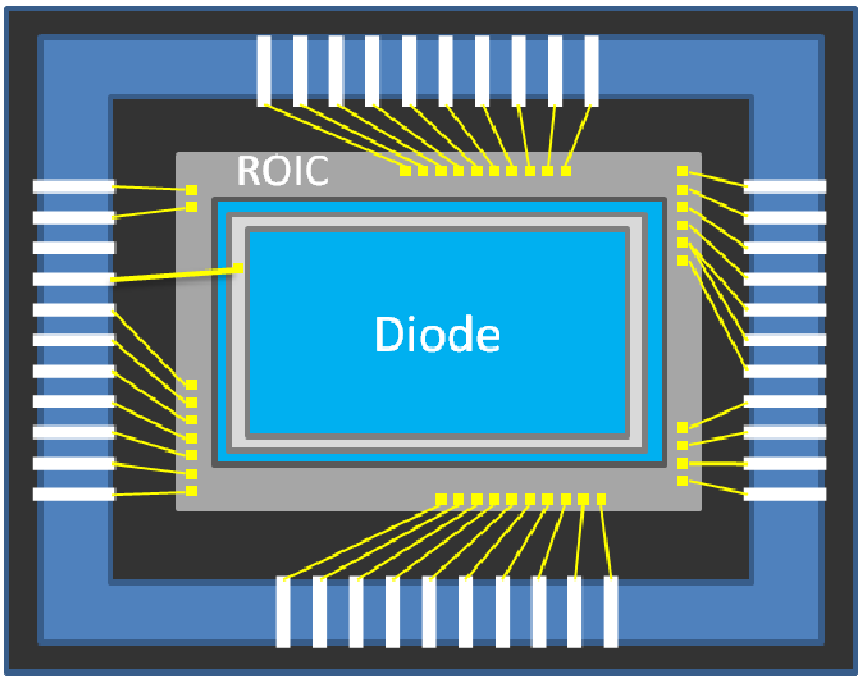


Fig. 1.9 Top Down Illustration of Hybridized Image Detector

1.5.2 MOSIS Read-out Integrated Circuit (ROIC)

The ROIC utilizes an oversampling sigma-delta (ΣΔ) analog-to-digital conversion technique to achieve an RMS read noise of < 1 e^-/pixel/sec. The circuits were designed by Dr. Zeljko Ignjatovic, an Assistant Professor of Electrical and Computer Engineering at the University of Rochester. The ROICs were manufactured at TSMC through the MOSIS foundry service using a 0.35 μm 2-poly 4-metal CMOS process. **Fig. 1.9** shows a top-down illustration of the ROIC and diode wire-bonded into the DIP package. An optical micrograph stitched together shows the full ROIC die in Fig. 1.10. The array of bump bond contacts can be seen as the shaded rectangle in the center of the die.

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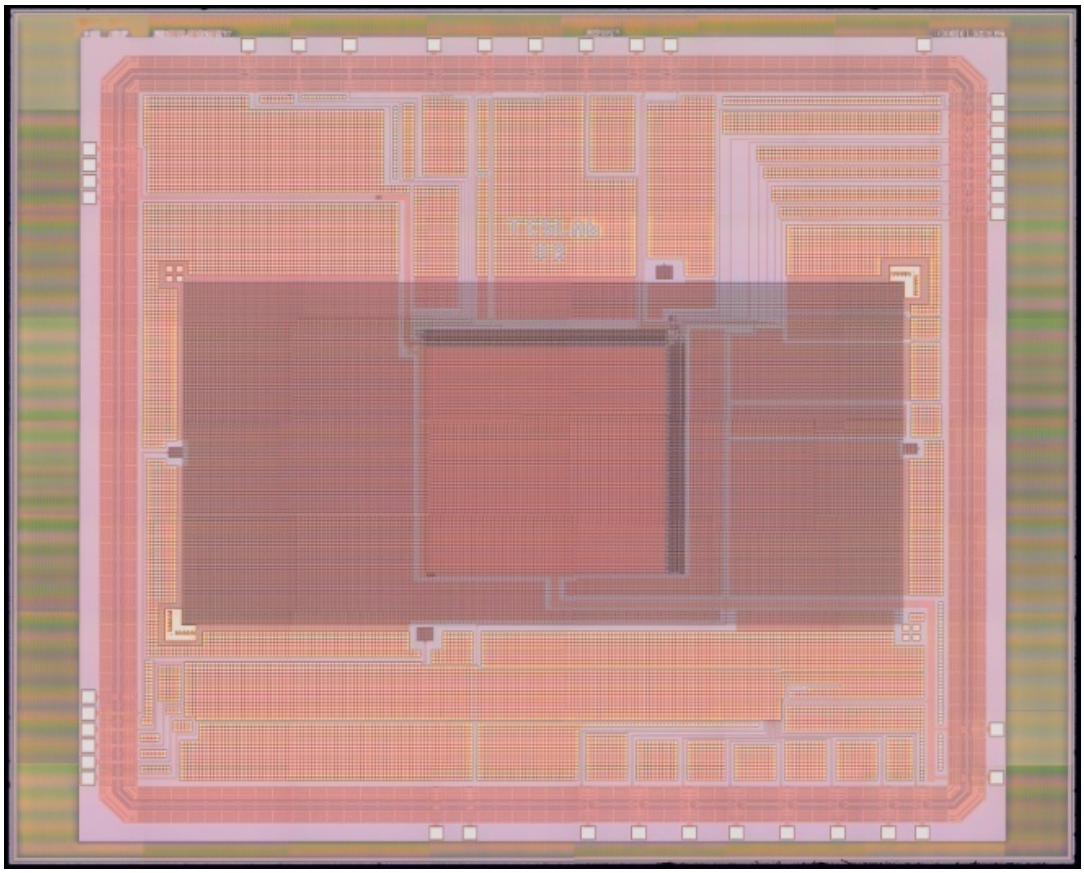


Fig. 1.10 Optical Micrograph of ROIC die

1.5.3 Silicon p-i-n Photodiode Array

The APRA imaging system consists of an array of p-*i*-n photodiodes at a pitch of 15 μm. The pixel is defined by an 11 μm p^+ region connected to a 9 μm aluminum pad through a 7 μm contact opening. The aluminum pad is made accessible by a 6 μm via through the passivation oxide. The pixel is also surrounded by a 1 μm aluminum border that forms a 2 μm grid throughout the array when the pixels are tiled. The layout for an individual pixel is shown in Fig. 1.11.

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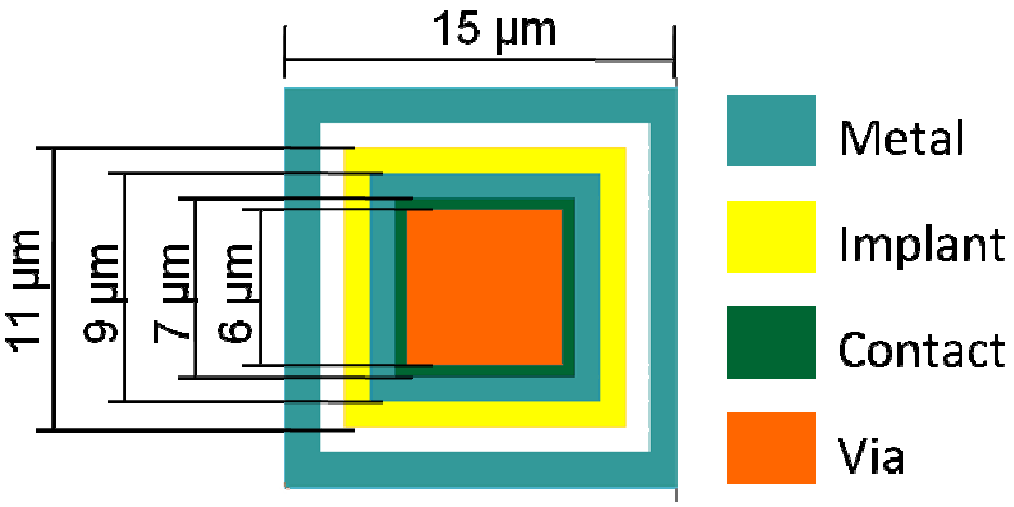


Fig. 1.11 Pixel Design and Layout

The pixel was repeated into a 128 x 256 element array surrounded by a bias ring that consisted of 6 modified pixel elements. Guard ring connections were located along the top and bottom of the array, and connections to the inter-pixel grid were placed at the midline on the left and right sides of the array. Alignment marks and verniers for the hybridization process were included within the 6 pixel guard ring border at the corners of the array. An image of the layout of the photodiode array is shown in Fig. 1.12.

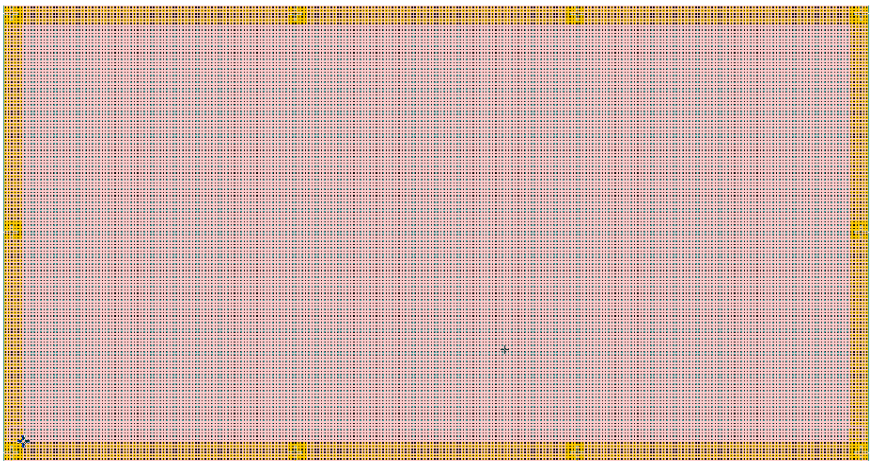


Fig. 1.12 Layout of 256x128 p-i-n photodiode array with guard ring

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A substrate thickness of 250 μm was selected to enhance efficiency in the longer wavelength (e.g. 1 μm) regime. The substrates were double-side polished ultra-high purity float-zone silicon substrates doped with phosphorous to a resistivity of 5000 Ω·cm. An operating bias of 50 V was designed to fully deplete the substrate at the chosen thickness. A single-layer anti-reflective coating was used to optimize the quantum efficiency for a selected wavelength range. The hybridization technique was a flip-chip process using indium bump-bonds as the interconnect metal.

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Chapter 2

p-i-n Photodiode Operation

The *p-n* junction, or diode, is the most basic, fundamental element of all solid state semiconductor devices. In use since 1906 in crystal radios, the theoretical framework behind the operation of the devices was unknown until 1939 when Russel Ohl discovered the role of impurities [15]. In its most simplistic form, the two-terminal device, also known as a rectifier, only allows current to pass in a single direction. The *p-i-n* diode consists of a *p-n* junction separated by a region so lightly doped that for most practical purposes is it assumed to be intrinsic. The intrinsic region most commonly denoted by the letter *i* though sometime the greek letters π or ν are used to denote the lightly doped region as either p or n-type. The static and dynamic characteristics of the device in the absence and presence of illumination will be discussed in the following chapter.

2.1. Junction Electrostatics

The junction electrostatics are discussed assuming a one sided abrupt junction for both of the p^+-n^- and n^+-n^- junctions under thermal equilibrium conditions. The fundamental equation describing the relationships between potential, electric field and

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charge is known as the Poisson equation. Derived from Gauss's Law, the partial-differential equation in its one-dimensional form is given in (2.1).

$$\frac{d^2\Psi_i}{dx^2} = -\frac{d\mathcal{E}}{dx} = -\frac{\rho}{\varepsilon_s} \tag{2.1}$$

where Ψ_i is the semiconductor potential, □ is the electric field, ρ is the volume charge density and ε_s is the permittivity of the material. The depletion approximation is used to simplify analysis by assuming a rectangular profile for the depleted charge. The total charge on each side of the junction is assumed to be opposite and equal and represented by (2.2)

$$N_A W_{Dp} = N_D W_{Dn} \tag{2.2}$$

where N_A and N_D are the doping densities and W_{Dp} and W_{Dn} are the depletion widths for the *p* and *n*-type sides of the junction respectively. The total built-in potential for both junctions can be determined by (2.3) where the intrinsic region is for all intents and purposes ignored.

$$\Psi_{bi} = \frac{kT}{q} ln\left(\frac{p_{p0}}{p_{n0}}\right) = \frac{kT}{q} ln\left(\frac{n_{p0}}{n_{n0}}\right) \tag{2.3}$$

where Ψ_{bi} is the built-in potential, *k* is the Boltzmann constant, *T* is the temperature in Kelvin, *q* is the electronic charge, and the carrier densities are the thermal equilibrium values represented in the traditional fashion. Integration of the Poisson equation, assuming complete ionization of impurities within the depletion, regions yields the

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electric field distribution, □(x). Further integration of the electric field yields the potential distribution, Ψ(x), of the junction. The width of the depletion region for a one-sided abrupt junction can be calculated by (2.4)

$$W_D = \sqrt{\frac{2\varepsilon_s}{qN}\left(\Psi_{bi} - V - \frac{2kT}{q}\right)} \tag{2.4}$$

The width of the depletion regions is modified by any applied bias, as well as a factor of *2kT/q* to account for the two minority-carrier distribution tails. The tails are caused by the diffusion of majority carriers into the depletion region causing a rounded corner in the assumed square charge profile.

2.1.1 Current-Voltage Characteristics

The current through an ideal diode is described by the Shockley equation, also known as the ideal diode law. The development of the ideal diode law, shown below in (2.5), is rather exhaustive and provided by many excellent textbooks so it will not be covered here. Interested readers are directed toward the development provided by Sze in "Physics of Semiconductor Devices" [4].

$$J = J_p + J_n = J_0\left[exp\left(\frac{qV}{\eta kT}\right) - 1\right] \tag{2.5}$$

where J is the total current density, J_p and J_n are hole and electron current densities respectively. J_o is the saturation current density, V is the applied voltage, and η is the

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ideality factor. The ideality factor provides insight into the dominant mechanism of current transport and varies between 1 for diffusion and 2 for recombination.

While the Shockley equation provided a breakthrough in the understanding of device operation, most practical devices do not exhibit ideal operation. Non-ideal effects contribute to deviations from the ideal operation, as shown in Fig. 2.1 [4]. Regions of forward operation are labeled as (a) generation-recombination region, (b) diffusion region, (c) high-injection region and (d) series-resistance effect. The reverse bias regions is labeled as (e) with junction breakdown occurring at a high reverse potential.

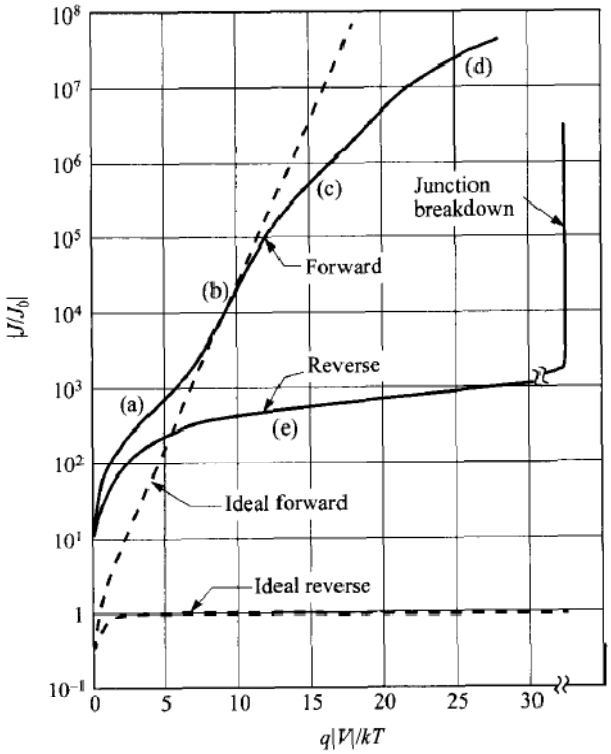


Fig. 2.1 Current-voltage characteristics of a practical Si diode showing ideal and experimental behavior in forward and reverse modes of operation [4]

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Forward Bias

The forward bias operation of a practical *p-i-n* diode is largely determined by recombination rate in the large intrinsic region. Thus, for good forward operation, long carrier lifetimes are desirable. A high quality junction is also needed to prevent defects from creating recombination centers in the vicinity of the junction. Due to the extremely low doping levels on the intrinsic side of the junction, high-injection effects start to occur at relatively low voltage levels. The ideality factor provides an insight into the dominant current mechanism.

Reverse Bias

In the absence of light, an ideal device would have an extremely small reverse bias current due only to the thermal generation of carriers within the depletion region. Leakage currents in practical devices are always larger than theoretically predicted due to mid-level traps in the vicinity of the metallurgical junction. These defects are typically due to the methods of dopant introduction used and the inability to completely heal all crystal imperfections in the annealing process. Metal-ion contamination can also be a major contributor to leakage currents, although the precautions taken in semiconductor fabrication are specifically designed to address contamination concerns. The net

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transition rate (U) in a semiconductor is the difference between the recombination rate and generation rate and is determined by (2.6) [4].

$$U = \frac{\sigma_n \sigma_p v_{th} N_t (np - n_i^2)}{\sigma_n \left(n + n_i e^{\left(\frac{E_t - E_i}{kT}\right)} \right) + \sigma_p \left(p + n_i e^{\left(\frac{E_t - E_i}{kT}\right)} \right)} \tag{2.6}$$

The numerator is the relative change in carrier concentrations compared to thermal equilibrium levels, σ_n and σ_p are the electron and hole capture cross sections respectively, v_{th} is the thermal velocity, and N_t is the density of bulk traps with corresponding energy levels E_t. A positive value corresponds to an excess of carriers resulting in recombination and a negative value indicates a deficit of carrier and leads to generation. Image sensors are typically operated in reverse bias with relatively large depletion regions so the defect levels in the substrate are an extremely important parameter.

As the energy of the trap level deviates from the mid-gap value its efficiency as a generation/recombination center falls of dramatically due to the exponential dependence, consequently only mid-gap traps are typically considered. Minority carrier lifetimes (τ) are defined as the inverse product of the capture cross section, thermal velocity, and bulk trap density for each of the carrier types. Substituting these values for lifetimes and using the above assumption (2.6) can be simplified to (2.7) [4].

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$$U = \frac{(np - n_i^2)}{\tau_p(n + n_i) + \tau_n(p + n_i)} \tag{2.7}$$

2.1.2 Minority Carrier Lifetime

Leakage currents are highly dependent upon minority carrier lifetimes, which are determined by initial doping concentration and the methods used to introduce additional dopants to create the desired profiles. The minority carrier lifetime (holes in n-type silicon) as a function of donor density is shown in Fig. 2.2 taken from [16]. Defects can be created during the doping process that form allowed energy levels within the band gap known as generation/recombination centers. Ion implantation has been shown to cause higher leakage levels than thermal doping due to lattice damage that is not fully healed during the activation anneal, however thermal doping can require additional process steps [16].

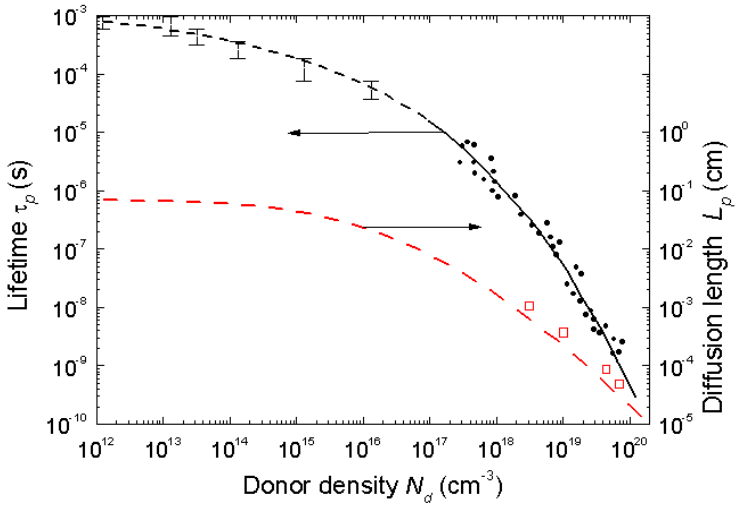


Fig. 2.2 Lifetime (τ_p) and Diffusion length (L_p) of Holes in n-type Si as a function of Donor density [17]

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There are several methods to electrically measure the lifetime of carriers in a p-*i*-n diode, although they all rely on similar principals [18, 19]. The diode is first forward biased to inject minority carriers across the junction into the base. In this condition the recombination of minority carriers in the quasi-neutral region is the primary contribution to total current flow through the device. The method by which the forward bias condition is removed leads to several techniques for measuring carrier lifetimes.

2.1.3 Open-Circuit Voltage Decay (OCVD) Method

In the open-circuit voltage decay (OCVD) method the voltage across the junction is monitored as a switch is opened removing the bias from the device [18]. Typical current and voltage transients in the device right before and after the switch is opened are shown in Fig. 2.3 (a). An initial drop in voltage is observed due to ohmic potential losses that vanish as the external current is removed. The remaining voltage across the diode is the junction voltage caused by the presence of excess carriers. As there is no current flow, the decay of this voltage is directly related to the recombination of these carriers and can be used to determine a carrier lifetime in the neutral bulk region. The lifetime can be shown to be related to the time-varying voltage by (2.8).

$$\tau = -\frac{kT/q}{dV(t)/dt} \tag{2.8}$$

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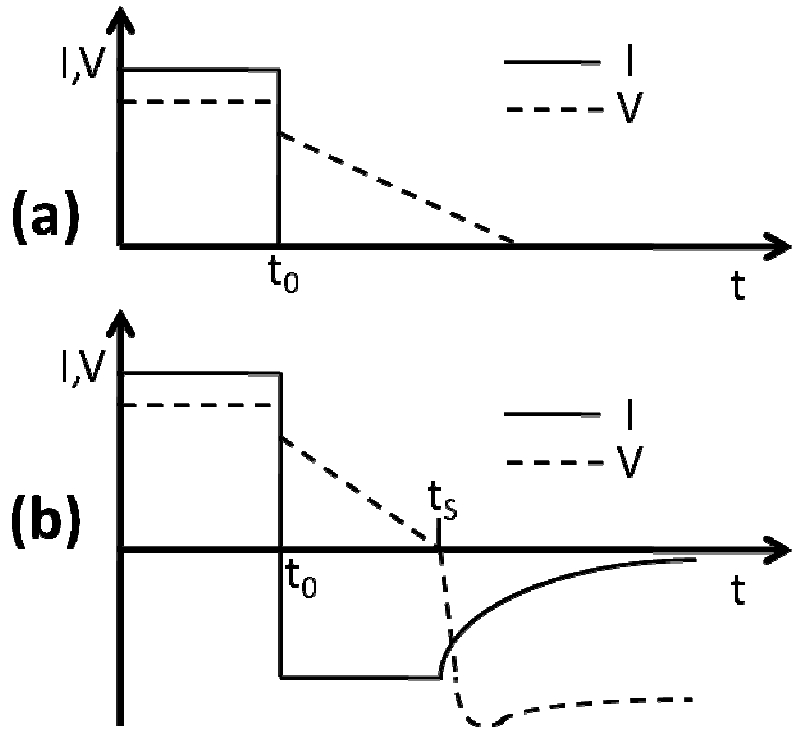


Fig. 2.3 Current and voltage transients observed in the methods used for carrier lifetime measurements: (a) OCVD; (b) Junction Recovery Method [18]

2.1.4 Reverse Recovery Method

In the reverse recovery method, the polarity of the voltage across the diode is switched from forward to reverse bias [20]. Excess carriers in the junction are removed by both recombination and a drift current caused by the electric field. Initially the device is still forward biased and the junction voltage is observed across the device as the ohmic losses are eliminated.

A reverse current begins to flow, as shown in Fig. 2.3 (b), and maintains a fairly constant magnitude as the junction voltage decays. This continues until the excess carriers at the edge of the space charge regions are approximately zero. This time,

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indicated as t_r, is known as the storage time for the device. At this point the reverse current decreases to its leakage level as the depletion region widens and the remaining excess carriers deep within the quasi-neutral region recombine. A charge storage analysis during the constant current phase results in (2.9). Recombination lifetimes (τ_R) can be determined from the slope of a best fit line on a plot of t_r versus $ln(1+ I_F/I_R)$.

$$t_r = \tau_R ln\left(1 + \frac{I_F}{I_R}\right) \tag{2.9}$$

The reverse recovery technique was one of the first methods available for electrically measuring lifetimes of carriers in devices. It was used widely in industry, however it can become inaccurate for small charge storage times or when the amount of charge stored in the device, when is has recovered, is significant. The OCVD method is much simpler, requiring only a single measurement to obtain carrier lifetimes, and the assumptions made during the derivation are less likely to be invalid in practical situations. For these reasons the OCVD method is a common test for solar cells created in the photovoltaic industry [18].

2.2. Absorption and Photogeneration

The first event that must occur in the photogeneration of carriers is the absorption of a photon by the silicon. Absorption is governed by several different mechanisms and

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the optical properties of the materials. These properties are determined by the complex refractive index of the material shown in (2.10)

(2.10)

where n is the real portion of the refractive index and k is the imaginary portion (also known as the extinction coefficient). Both parts of the refractive index are a function of the wavelength of the incident radiation. The complex refractive index as a function of wavelength for silicon is shown in Fig. 2.4.

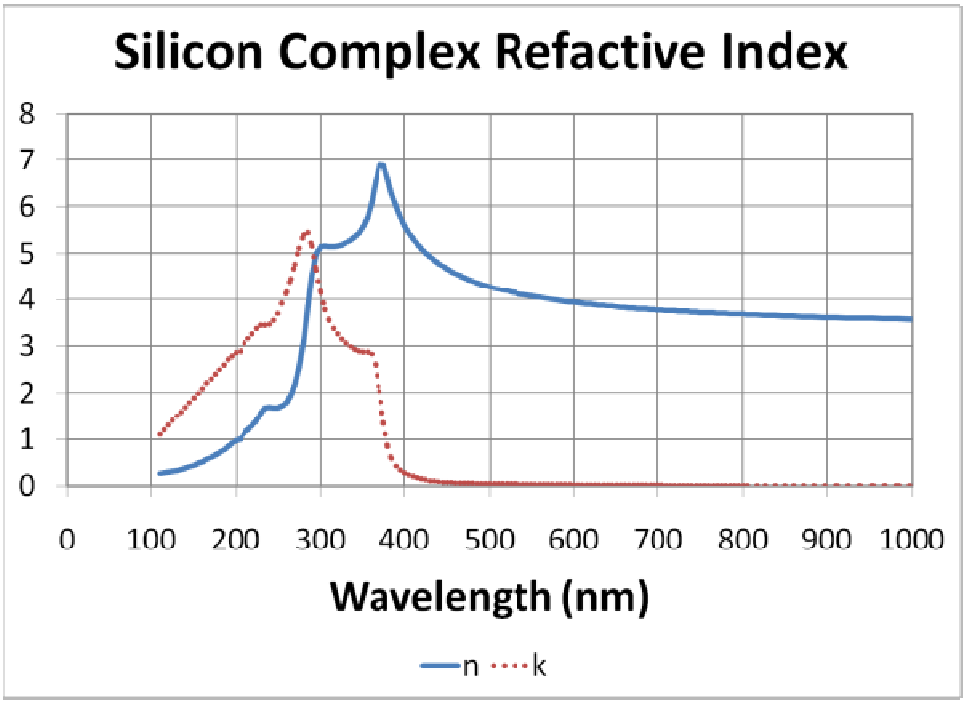


Fig. 2.4 Complex refractive index vs. wavelength for silicon

The Fresnel equations determine the amount of light that is either reflected or transmitted at the interface of two materials. It is dependent on the refractive index of the two materials forming the interface and the angle the incident radiation makes with the

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normal to the interface. The reflectance can depend on the polarization state of the light. For an angle of incidence nearly perpendicular through a transparent media, the equations simplify to (2.11) and (2.12).

(2.11)

(2.12)

The reflectance and transmittance at the silicon-interface have been calculated and are shown in Fig. 2.5 as a function of wavelength. It can be seen that there are significant reflection in the sub-400 nm region that limits the performance in the ultra violet (UV) region, but they decay to ~ 30% above 400 nm. The reflections at this interface will have a large affect on the device performance.

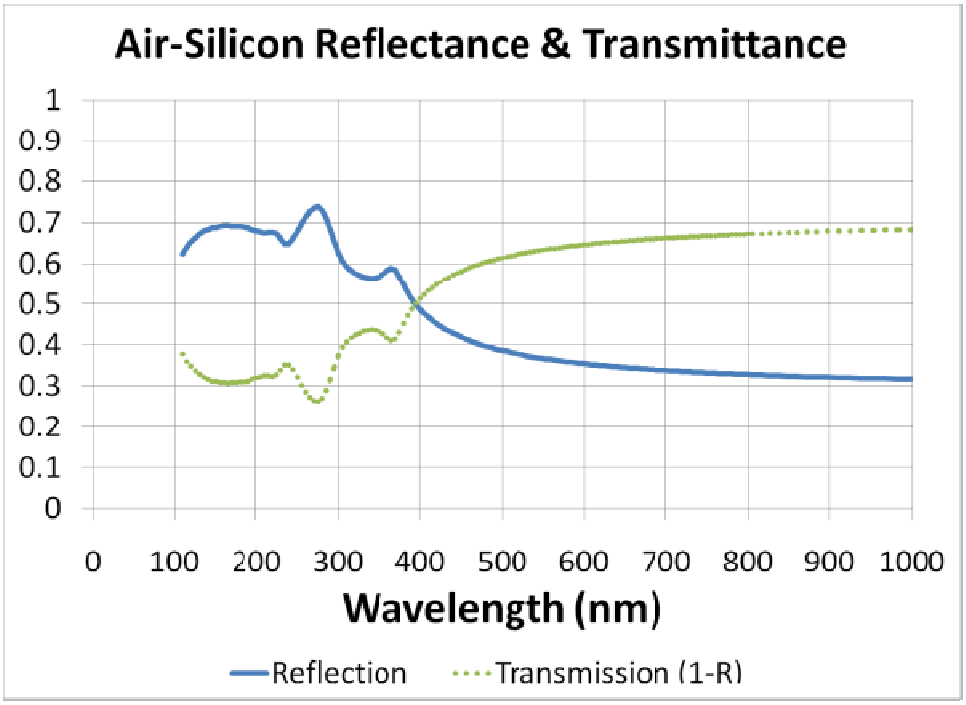


Fig. 2.5 Reflectance and Transmittance at the air-silicon interface

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Light that is transmitted at the interface must then be absorbed by the silicon. The absorption of light is determined by the absorption coefficient, α, as calculated by (2.13)

— (2.13)

where λ is the wavelength of the light. The intensity of the light is attenuated exponentially with distance in the silicon as shown by (2.14)

(2.14)

where I_0 is the incident intensity and x is the distance into the substrate. A characteristic penetration depth can be defined as the inverse of the absorption coefficient and is the depth at which 63.2% of the incoming radiation has been absorbed. A graph of the absorption coefficient and penetration depth as a function of wavelength for silicon is shown in Fig. 2.6.

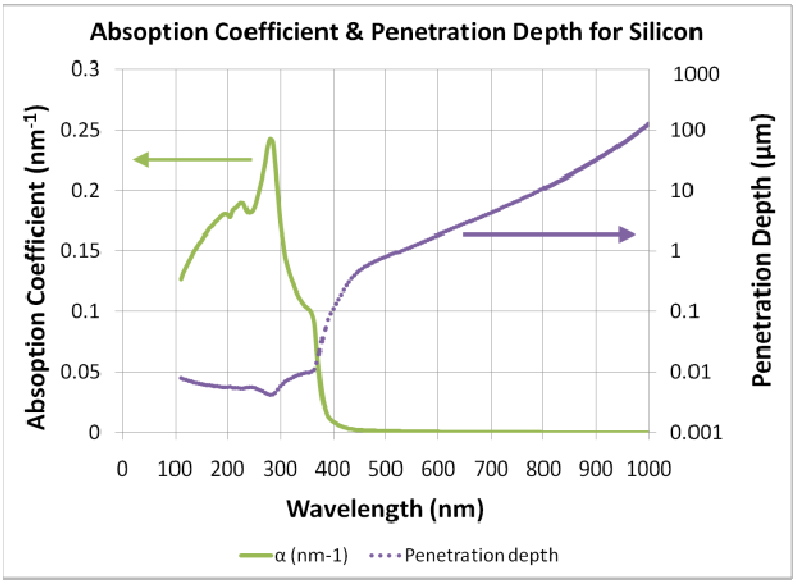


Fig. 2.6 Absorption coefficient and penetration depth vs. wavelength for silicon

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Carrier Generation

In order to generate carriers in a semiconducting material the absorbed photons must have sufficient energy to excite a carrier from the valence band to the conduction band; that is to say the energy must be greater than the band gap of the material. The generation of carriers is given by (2.15) and follows the same exponential decay as the absorption but is modified by the absorbed photon flux per unit area given in (2.16)

$$G_e(x) = \Phi_0 \alpha e^{-\alpha x} \tag{2.15}$$

$$\Phi_0 = \frac{P_{opt}(1-R)}{Ahv} \tag{2.16}$$

where P_{opt} is the incident optical power, R is the reflectivity, A is the area of the device and hv is the energy of the photon. P_{opt}/ hv can be recognized as the incident photon flux that is modified by $(1-R)$ to include only those photons that are not reflected.

2.3. Illuminated Operation

The main function of a photodiode is the efficient conversions of photons into electrons. Three events must occur to achieve the conversion of a signal from optical to electrical. A photon must be absorbed within the semiconducting material, charged carriers must be elevated to an excited state, and the charged carriers must be collected at the terminals of the device. The charge is then converted into a potential and read out by circuitry attached to the image sensor. During each of these steps there are opportunities for loss of signal and the incorporation of noise.

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2.3.1 Charge Collection

Once the carriers are generated they must be transported to the collection nodes before they recombine, giving rise to a current in the device. This current can be divided into two components, drift and diffusion. Carriers generated inside the depletion region will experience an immediate acceleration due to the electric field present, while those generated outside the depletion region must diffuse into the junction before they can be swept away. The total current density in a p-*i*-n diode is the sum of the individual components and is represented by (2.17)

$$J_{tot} = q\Phi_0\left[1 - \frac{e^{-\alpha W_D}}{1+\alpha L_p}\right] + \frac{qp_{no}D_p}{L_p} \tag{2.17}$$

where W_D is the depletion width, L_p is the minority carrier diffusion length, p_{no} is the equilibrium minority carrier concentration and D_p is the minority carrier diffusion constant [4]. The first term in (2.17) represents the carriers generated inside and within one diffusion length of the depletion region. A dependence on bias is not seen as it is assumed that all generated carriers are collected. The second term in Equation (8) is the dark current and is relatively insignificant in the presence of light. The minority carrier diffusion length is determined by (2.18)

$$L_p = \sqrt{D_p\tau_p} \tag{2.18}$$

where τ_p is the minority carrier lifetime.

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2.3.2 Quantum Efficiency

The quantum efficiency (QE) of a detector is a measure of the effectiveness at converting photons into electrons. The QE can be separated into internal QE and external QE, where internal QE is the ratio of absorbed photons to collected electrons. The external quantum efficiency is determined by taking the ratio of the collected carriers to the incident photon flux as shown in (2.19).

$$\eta = \frac{AJ_{tot}/q}{P_{opt}/h\nu} = (1-R)\left[1 - \frac{e^{-\alpha W_D}}{1+\alpha L_p}\right] \tag{2.19}$$

The external quantum efficiency is reduced due to both reflections at the silicon air interface and the generation of carriers outside the depletion region. To maximize the quantum efficiency it is desirable to have a large depletion region ($\alpha W_D \gg 1$) and a large diffusion length ($\alpha L_p \ll 1$).

2.3.3 Point Spread Function

Carriers generated in the device diffuse laterally as they are swept away by the electric field and collected at the terminals. The amount of lateral diffusion is determined by the diffusion rate and the amount of time the carrier has to diffuse. If the lateral diffusivity is large enough, or the transit time is too long, carriers generated in one pixel can be collected by an adjacent pixel. This is an extremely important effect for thick detectors, such as the one used in this project, as the transit time is considerably longer

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than for thin film detectors. The amount of lateral diffusion can be characterized by the point spread function (PSF), which also provides information about the minimum resolution of the device.

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Chapter 3

SILVACO Atlas TCAD Simulations

The physics based device simulation package Atlas from the technology computer-aided design (TCAD) software suite by SILVACO is used to simulate the electrical behavior of a defined structure. Numerical simulations are an extremely important tool to the modern day engineer. They allow new products to be developed faster and cheaper than traditional experimentation and prototyping methods. In the past century over a trillion dollars has been collectively invested into semiconductor research creating a vast pool of empirical data from which theoretical models have been created to describe virtually every aspect of device operation. In the early 1980's a group of researchers at Stanford developed a two-dimensional, two-carrier semiconductor simulation program known as PISCES-II [21]. This program became the basis for the S-PISCES module of Atlas, where the "S" implies it is specifically for silicon. The Luminous module is used to simulate the optoelectronic behavior of the device.

3.1. Numerical Poisson Solver Theory

The finite element method is a numerical technique for the discretization and solution of partial differential equations. The numerical simulation of the electrical behavior of semiconducting devices is accomplished by the application of the finite

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element method to a set of partial differential equations derived from Maxwell's Laws. The electrostatic potential is determined from Poisson's equation as a function of the space charge distribution. Carrier continuity and transport equations determine the concentration and motion of carriers within the devices as a result of generation/recombination and transport processes. In this specific application the simulation program is often referred to as a numerical Poisson solver.

3.1.1 Electrostatic Equations

The relationship between electrostatic potential and spatial charge distribution is described by the Poisson equation as

$$\nabla^2\varphi = -\frac{\rho}{\varepsilon_S} = \frac{q(n - p + N_A - N_D)}{\varepsilon_S} \tag{3.1}$$

where φ is the electrical potential, ρ is the space charge density, ε_S is the permittivity of the semiconductor, q is the electronic charge, n is the electron concentration, p is the hole concentration, N_A is the acceptor-like dopant density and N_D is the donor-like dopant density. The electric field is determined from the gradient of the potential.

$$E = -\nabla\varphi \tag{3.2}$$

3.1.2 Continuity Equations

To determine the space charge density the continuity equations relate the change in carrier concentrations over time due to generation/recombination events and low-level current injection.

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$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n + G_n - R_n \quad (3.3)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \cdot J_p + G_p - R_p \quad (3.4)$$

where J_n and J_p are the current densities, G_n and G_p are the generation rates, and R_n and *Rp* are the recombination rates for electrons and holes respectively, for each set of terms.

3.1.3 Drift-Diffusion Transport Equations

Carriers move about within the semiconductor due to two phenomena known as drift and diffusion. Drift is the movement of carriers in response to an electric field, or the desire of carriers to minimize their electric potential. Diffusion is the tendency of carriers to redistribute to achieve uniform concentrations or resist concentration gradients. The current density equations resulting from these processes are shown below

$$J_n = qn\mu_n E + qD_n \nabla n \quad (3.5)$$

$$J_p = qp\mu_p E - qD_p \nabla p \quad (3.6)$$

where μ_n and μ_p are the electron and hole mobility, and D_n and D_p are the electron and hole diffusion constants.

3.2. Atlas Simulation Organization

The code for an Atlas simulation follows an organizational structure outlined in Fig. 3.1. Specific excerpts of the code will be presented in this chapter for discussion as it relates to device operation and the validity of the results. A typically simulation file can be found in Appendix I.

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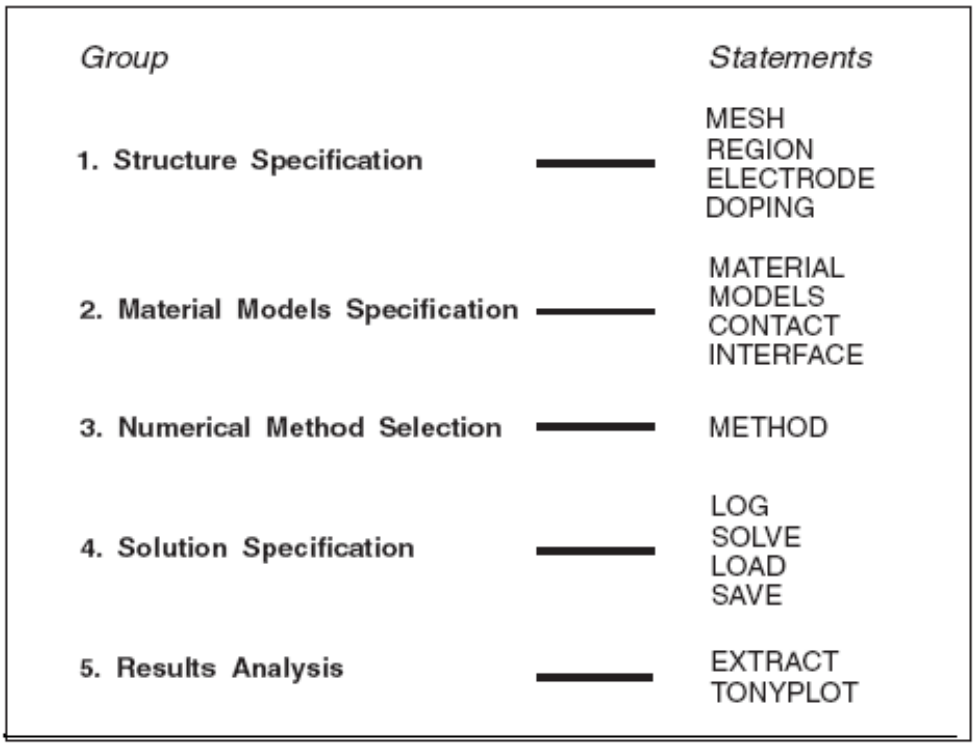


Fig. 3.1 Atlas Input Code Organizational Structure

First the structure of the device to be simulated is described by a grid of points known as a mesh. Regions within the mesh are specified as particular materials and electrodes and doping profiles are defined. Next the material properties are set for each region and the desired physical models are invoked. Contact characteristics for the terminals are specified, and any interface parameters such as surface generation rates, interface charge, or anti-reflective layers are defined. With the structure ready to be simulated, the numerical methods to be used for simulation are chosen. Finally the solution specification section allows the definition of the external stimulus applied during the simulation, and the location where results are saved. When a consistent solution has

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been reached parameters can be extracted or the structure can be plotted with overlaid distributions.

3.2.1 Device Structure Specification

The first set of commands in an Atlas simulation defines the size of the structure and spacing of the grid points. The '`loc`' and '`spacing`' commands specify lines in the x and y directions that intersect to form nodes, where the x-direction is horizontal and the y-direction is vertical. Locations can be positive or negative but must be in ascending order. The spacing can be uniform or non-uniform and Atlas will automatically grade the spacing from one location to the next. Nodes are also connected diagonally creating triangular domains. Abrupt changes in grid spacing and obtuse triangles are avoided as they can make convergence difficult and cause inaccurate results.

It is difficult to obtain the optimum mesh as there is an inherent trade-off between the resolution of grid points and the resulting accuracy of the simulation, and the computational efficiency of the simulation. Fine resolution is needed for areas with large doping gradients or electric fields but not in areas of uniform doping or constant fields. To avoid excessively large structures there is a 20000 node limit for a two-dimensional simulation.

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Fig. 3.2 Atlas example mesh definition code

The mesh definition for the simulations performed in this study are shown in Fig. 3.2. The structure was defined to have a variable width and thickness with constant node spacing in the x-direction and graded spacing in the y-direction. A fine resolution is specified at the light absorbing surface that gets coarser into the bulk of the device. The majority of the device thickness contains a rather coarse grid spacing of 5.0 microns before becoming fine again at the back surface. The thickness of the simulated device was typically set to 250 microns as determined by the substrate thickness, and the width was set to simulate the largest device possible within the available number of nodes.

A fair amount of time during the initial investigations centered around optimizing the vertical mesh spacing. Ensuring an adequate spacing of nodes at the light absorbing surface to accurately describe the absorption of short wavelength light was a particularly difficult problem and will be described further in Section 5.4 on Quantum Efficiency.

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Fig. 3.3 Atlas simulation code defining electrode name as positions and doping profiles

Once the mesh has been defined, areas within the mesh are specified as a region and material. For this simulation the entire structure was defined as a continuous region of silicon. Next electrodes are added to the structure and the doping contours are defined as shown in Fig. 3.3. The N+ contact was defined to cover the entire surface of the structure and five P+ electrodes are defined on the backside of the device to contact individual pixels. The electrodes are given arbitrary names and numbers as identifiers.

The substrate is defined to be uniformly doped with an n-type impurity to a concentration of $1x10^{-12}$ cm^{-3}. The species of the dopant is not important, and the concentration is set to match the substrate manufacturer specification. Both the N+ and P+ regions are specified with Gaussian doping profiles, although the N+ region is defined

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to have specific junction depth, and the P+ regions are defined with characteristic lengths that are related the standard deviation of the Gaussian. After the doping profiles have been defined a ‘regrid’ statement is included to increase the mesh resolution in the regions where doping concentration varies rapidly. The smoothing of the mesh in these areas helps to prevent the solutions creating large discontinuities between nodes.

3.2.2 Material Models

With the basic structure of the device defined, the materials properties and physical models to be used during the simulation are shown in Fig. 3.4. The only material properties of the silicon that were adjusted from default values are ‘TAUP0’ and ‘TAUN0,’ the minority carrier lifetimes. They were defined as 1 millisecond as specified by the substrate manufacturer and shown in literature for float-zone silicon [17], but were also varied in some simulations to see the effect they have on device performance.

Fig. 3.4 Atlas code defining material and interface properties and specifying numerical models

In the ‘models’ statement the temperature is defined as a variable because the device is designed to operate at low temperatures, so simulations were performed from

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room temperature to as low as 170K. The remaining terms in the '`models`' statement activate specific physical models as follows: '`srh`' Shockley-Reed-Hall (SRH) Recombination, '`auger`' Auger Recombination, '`cvt`' Lombardi CVT Model, '`fermi`' Fermi-Dirac statistics, '`bgn`' Band-Gap Narrowing.

Fermi-Dirac Statistics

Fermi-Dirac statistics are typically approximated by Boltzmann statistics in situations where the Fermi level is greater than a few *kT* away from the band edge. The approximation begins to fail at low temperatures and high doping concentrations. As both will be present in this work, Fermi statistics have been enabled for all simulations. The probability that an available electron energy state (ε) in a semiconductor is occupied by an electron is

$$f(\varepsilon) = \frac{1}{1 + exp^{\left(\frac{\varepsilon - E_F}{kT_L}\right)}} \tag{3.7}$$

where E_F is the Fermi level, k is Boltzmann's constant, and T_L is the lattice temperature. Evaluation of the Fermi-Dirac integral by Atlas is handled using a Rational Chebyshev approximation scheme [22].

Bandgap Narrowing

In heavily doped semiconductors the conduction and valence bands broaden slightly causing a narrowing of the bandgap. This primary effect of this phenomenon is

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to locally increase the effective intrinsic carrier concentrations and is modeled by Atlas using a spatially varying intrinsic concentration n_{ie} calculated as

$$n_{ie}^2 = n_i^2 exp^{\left(\frac{\Delta E_g}{kT}\right)} \tag{3.8}$$

where ΔE_g is the bandgap reduction calculated as

$$\Delta E_g = BGN.E\left[ln\frac{N}{BGN.N} + \sqrt{\left(ln\frac{N}{BGN.N}\right)^2 + BGN.C}\right] \tag{3.9}$$

where N is the dopant concentration and *BGN.E*, *BGN.N* and *BGN.C* are empirical values determined by Slotboom and de Graaf [23].

Once the amount of bandgap narrowing has been determined, the effect is introduced into the other models by adjusting the value of the bandgap used in their calculations accordingly. The primary motivation for the inclusion of this model was to account for any effects the heavy doping of the N+ surface may have on the absorption of light and photogeneration of carriers.

Shockley-Reed-Hall Recombination

The '`srh`' term invokes the Shockley-Reed-Hall Recombination statistics model shown in (3.10) to account for trap-assisted phonon transitions. The model uses the minority carrier lifetimes defined in the '`material`' statement to calculate the generation or recombination of carriers as

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$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUP0\left[n + n_{ie}e^{\left(\frac{ETRAP}{kT_L}\right)}\right] + TAUN0\left[p + n_{ie}e^{\left(\frac{-ETRAP}{kT_L}\right)}\right]} \quad (3.10)$$

where n_{ie} is the intrinsic carrier concentration, 'ETRAP' is the difference between the trap energy level and the intrinsic energy level, and T_L is the lattice temperature in degrees Kelvin. The default value of 'ETRAP' is 0 corresponding to the center of the band gap. This value was used for all simulations as the actual identity of contamination and defect states was not under investigation. The value for the lifetime combines the effects of the trap capture cross section, the thermal velocity, and trap density as

$$\tau_p = \frac{1}{\sigma_p \nu_{th} N_t} \quad (3.11)$$

An analogous statement can be written for electrons.

Lombardi CVT Model

Atlas contains many mobility models incorporating a variety of different phenomena appropriate for various situations. For the simulations presented here the Lombardi CVT Mobility models was used. Despite the fact that the model is intended for simulating the inversion layer of a MOSFET, it is the only model that includes the effects of doping concentrations, lattice temperature, and velocity saturation all in one model. It also includes effects due to transverse electric fields, although those won't be applicable to these simulations. The Lombardi model combines the effects of acoustic phonon

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scattering (μ_{AC}), surface roughness (μ_{sr}), and optical inter-valley phonon scattering (μ_b) using Matthiessen's rule as

— — — (3.12)

where μ_T is the total effective mobility. The additional effects of coulombic scattering are incorporated using the same reciprocal method akin to adding resistors in parallel.

3.2.3 Numerical Methods

To perform a simulation, Atlas uses an internal discretization procedure to convert one to six coupled, continuous non-linear partial differential equations (PDE) to a discrete non-linear algebraic system that is solved at each point in the mesh. Following an initial guess, an iterative procedure successively refines estimates of the solution until the changes are smaller than convergence criteria.

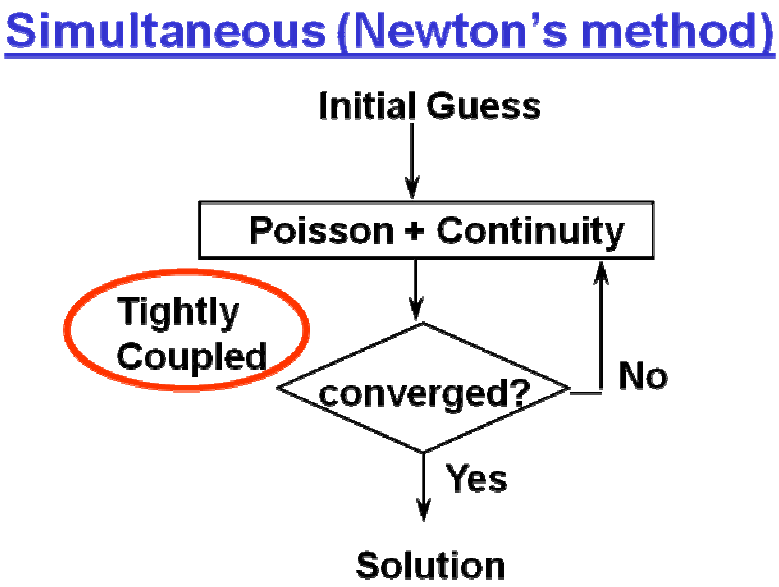


Fig. 3.5 Flow diagram for Newton method [24]

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The discretization process in Atlas is performed using the Box Integration Method that creates a polygon around each node within which the equations are integrated. The fluxes at the edges of a polygon are equated with sources and sinks within. The non-linear algebraic system is solved by Atlas using Newton's method, by evaluating a linearized version of the entire non-linear algebraic system. A block diagram of Newton's method is shown in Fig. 3.5. This makes the problem rather large and may take a while to solve, however the final solution can typically be reached in only a few iterations. This method requires computers with large amounts of processing power and memory.

Fig. 3.6 Atlas specification of solution method and parameters

Figure 3.6 shows the Atlas command that invokes the numerical models used to evaluate the solution. The '`trap`' command specifies that if the solution does not converge the magnitude of the bias step will be reduced. A factor of ½ is the default, although this term can also be adjusted. The '`clim.dd`' term specifies a cut-off value for carrier concentrations below which the convergence of equations is not required. This factor is included as the bulk of the material is very lightly doped to begin with, and is

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then depleted at reduced temperatures creating extremely low carrier concentrations in regions that are important to device operation.

3.2.4 Solutions Specification

The last section of code in an Atlas program specifies the external stimulus to be applied and the location where solution files are to be saved. A sample of the code used to define the solution conditions and specify output formats is shown in Fig. 3.7. The illumination sources for optical excitation are defined by the ‘beam’ statement. A location for the origination of the source is specified as well as the angle the incident beam makes with the surface of the structure.

Fig. 3.7 Atlas solution specification code sample

By default the illumination is monochromatic with uniform spatial intensity, although spectral sources and Gaussian intensity profiles can be specified. Atlas also

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contains spectral intensity profiles for both AM0 and AM1.5 illumination. The 'rays' command splits the uniform illumination into many different rays that can be applied individually to evaluate the spatial dependence of illumination. The '`front.refl`' and '`back.refl`' commands specify that reflections off the first surface and back surface should be included in the calculations. These reflections are not included in the default ray tracing performed by Atlas.

Simulations are finally performed when the program reaches the first '`solve`' statement. An initial solution is performed using the '`init`' command with no applied bias on any of the terminals. The initial guess for potential and carrier concentrations is made from the doping profiles. A file where extracted parameters are saved is specified using the '`log`' command. On subsequent '`solve`' statements the '`prev`' command is used to specify that the previous solution should be used as the initial guess for the following solution. This improves chances of convergence for small bias steps and prevents the program from performing a new solve init returning the device to zero applied bias. Once the device has reached the operating conditions the log file storing the I-V data is closed using the '`log off`' command and a new log file is opened.

In the final solve statement the optical beam is enabled using the '`b1=1`' command which specifies beam1 is to have an intensity of 1 W/cm^2. In the solve statement above

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the command '`scan.spot=1`' specifies that beam1 should be solve for each of the defined rays separately, much like scanning the beam across the surface of the wafer. The wavelength of the beam was also varied for uniform illumination much like the bias was incremented to determine spectral response.

3.3. Simulation Results

Simulations provide results in three different forms. Extract statements produce a single numerical result such as the junction depth or the photo-generation rate. Log files store the runtime output of a solve command including the potential and currents at all terminals and the result of any probe statements at every incremented step. When the solutions have been determined at operating conditions, the simulated structure can be visualized using Tony Plot to overlay contours of distributions including potential, electric field, current densities, and carrier concentrations.

3.3.1 Current Voltage Characteristics

The electrostatic solution for the device provides the current-voltage characteristics and an estimation of reverse bias leakage, or dark current. The thermal generation rate is largely determined by the minority carrier lifetime of the material. The minority carrier lifetime of $1x10^{-3}$ sec specified by the substrate manufacturer was implemented in Atlas. The current-voltage characteristics of the device are highly

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dependent on the starting substrate doping level and the methods of processing. Since the substrate conditions are fixed and the effects of processing are hard to predict, the un-illuminated results provide simulation baseline.

Forward Bias

The forward bias current density of the *p-i-n* diode was simulated from an applied bias of 0 to 1.5 Volts. A graph of the simulation results in Fig. 3.8 show the device did not exhibit the traditional diode behavior. Even with high minority carrier lifetimes, at low bias conditions recombination is the dominant current transport mechanism due to the extremely wide intrinsic region. As the device turns on further it enters a forward bias region with an ideality factor of nearly one. At even higher biases the injected carriers begin to overwhelm the background ion concentration ($N_D \sim 10^{12}$ cm^{-3}) of the intrinsic region and the ideality factor degrades rapidly due to high level injection and series resistance.

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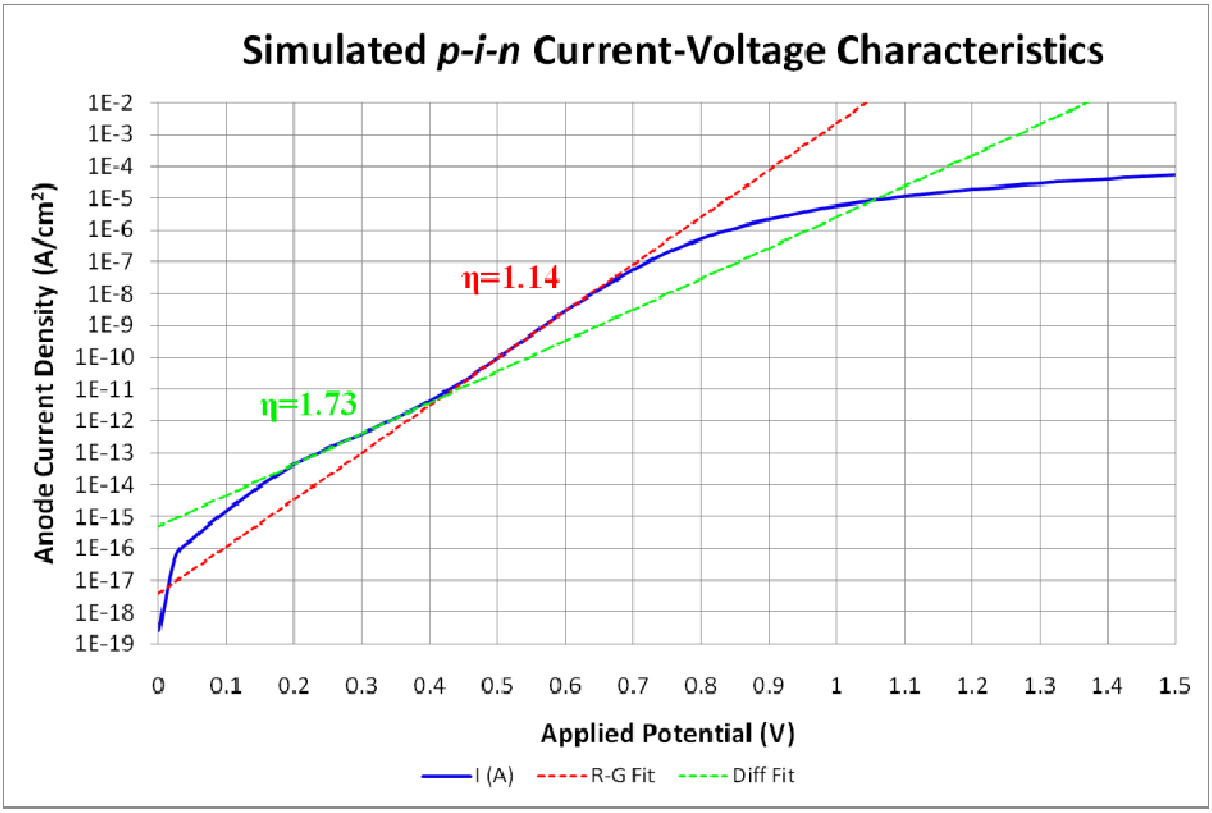


Fig. 3.8 Simulated *p-i-n* diode forward bias current density

Reverse Bias

The reverse bias leakage current presented another challenge for the simulation package. The results shown in Fig. 3.9 were generated for a structure of silicon with dimensions of 15 µm wide by 250 µm thick to represent a single pixel. Due to the very low doping levels, the resulting depletion width is hundreds of microns, and extends equally in all direction. The generation current is underestimated when attempting to simulate individual devices as the actual depleted region would create a hemisphere extending beyond the simulated structure.

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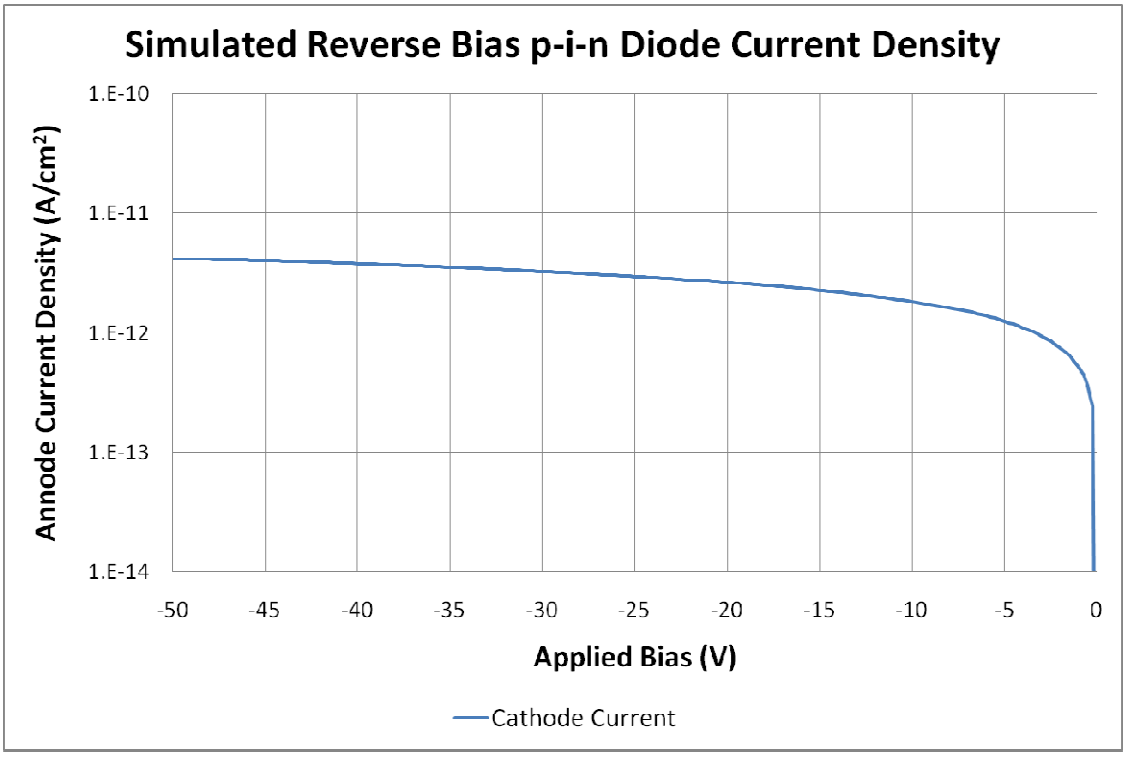


Fig. 3.9 Simulated *p-i-n* diode reverse bias leakage current vs. applied bias

The leakage current was also examined as a function of the minority carrier lifetime to confirm the expected relationship within the simulation and the choice of doping levels in the substrates. The results in Fig. 3.10 show that for a lifetime of 1 msec a current density of ~ $1x10^{-8}$ A/cm^2 can be expected. Although this seems rather large compared to the leakage goal, when scaled to low temperature the result is within an order of magnitude. As this lifetime represents the upper limit of lifetimes that can be realistically achieved in silicon, it shows that the goals set were realistic and can be attained with high quality manufacturing.

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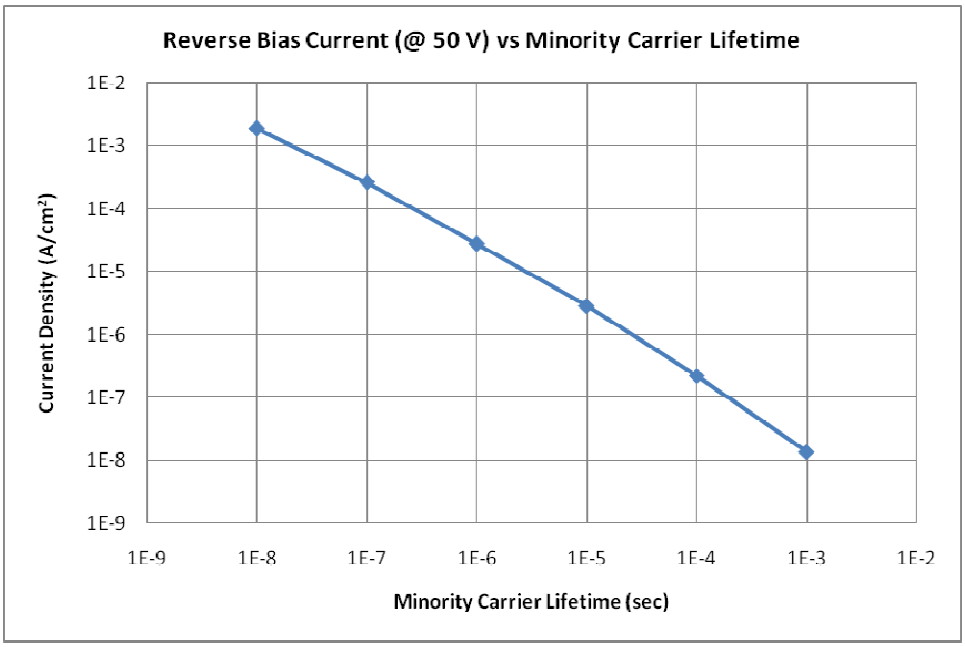


Fig. 3.10 Simulated reverse bias current density at 50 V vs. minority carrier lifetime

3.3.2 Quantum Efficiency

The quantum efficiency (QE) is a measure of the fraction of electrons extracted from a device per incident photon as a function of wavelength. It is an important metric used to quantify the performance of devices across different technologies. In this context QE can be separated into internal quantum efficiency (IQE), the ratio of collected carriers to absorbed photons, and external quantum efficiency (EQE), the ratio of collected carriers to incident photons. The IQE is only affected by losses within the device such as carrier recombination, or generation of carriers beyond a diffusion length away from the depletion region. EQE includes internal losses but also accounts for losses due to reflection and incomplete absorption. All further mentions of QE in this document will

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refer to external QE unless specified otherwise. Both are affected by many aspects of the device design such as the distribution of the electric field and the location where carriers are generated.

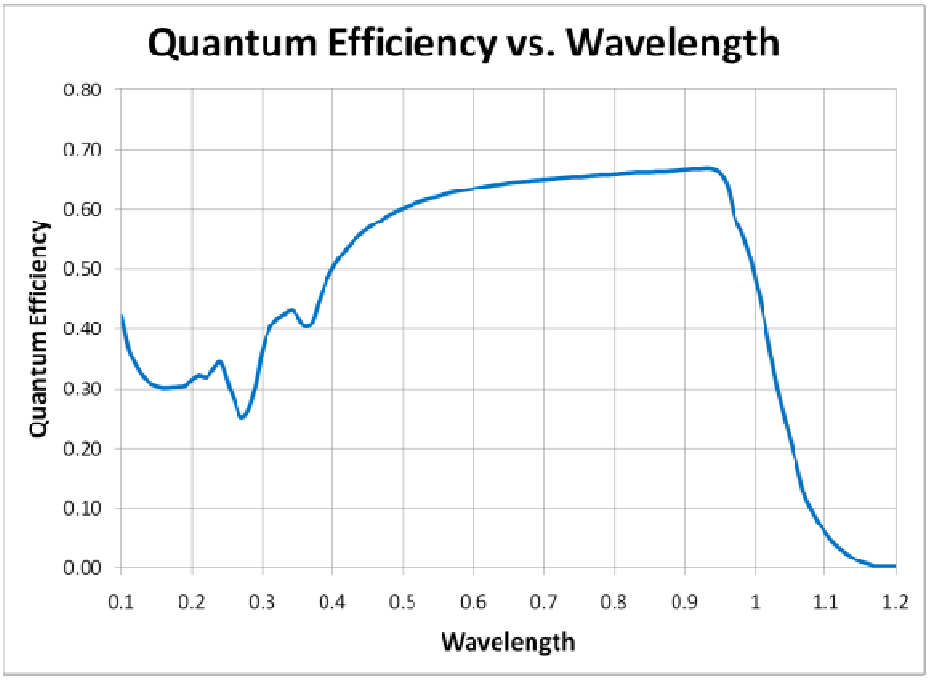


Fig. 3.11 Typical quantum efficiency curve from SILVACO Atlas

The biased device is illuminated with a uniform intensity monochromatic source as the wavelength is varied over the desired range (200 – 1200 nm). A typical quantum efficiency curve for a 250 μm thick silicon p-i-n diode operated at 2 kV/cm is shown in Fig. 3.11. In addition to providing a framework to characterize theoretical device performance, the simulations also provided an opportunity to optimize several process related parameters and explore the operating design space.

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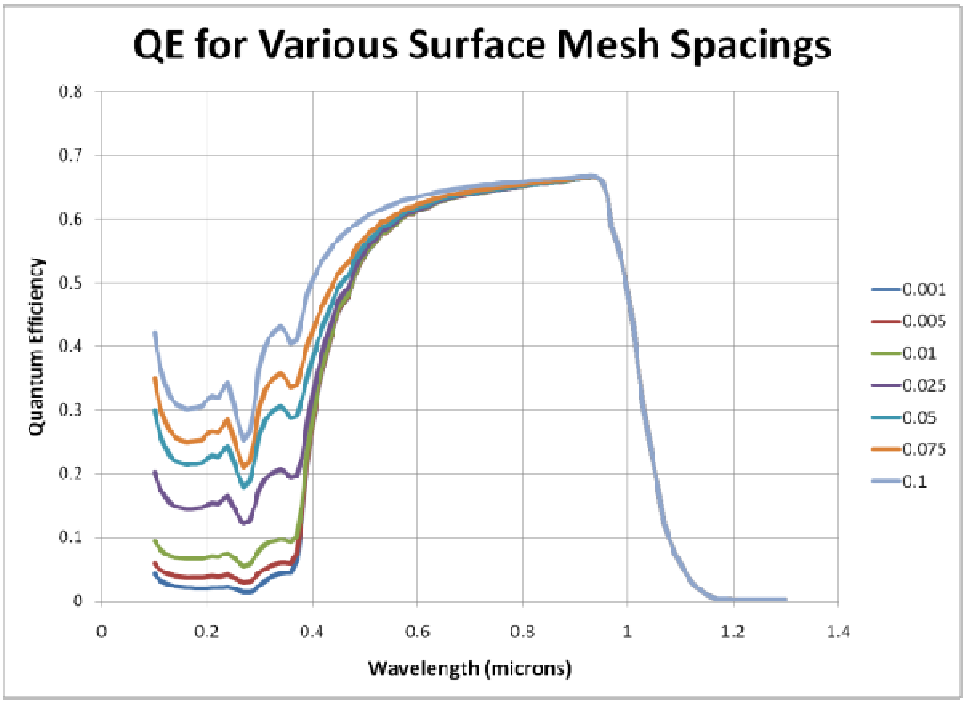


Fig. 3.12 QE curves for surface grid resolution from 0.001 to 0.1 μm

During the course of performing the simulations, a significant loss of signal for wavelengths less than 400 nm was observed. Recalling Fig. 2.6, this is where the absorption coefficient for silicon begins to increases rapidly reducing the penetration depth to about 10 nm. Further investigation found the resolution of the mesh at the surface of the device had a strong affect on the quantum efficiency in the short wavelength range. The simulated QE curves for surface grid resolutions ranging from 1 nm to 0.1 μm is shown in Fig. 3.12. The fine mesh spacing appears to overestimate recombination, reducing the amount of carriers that reach the depletion region. Unfortunately this effect was not noticed until after the completion of simulations.

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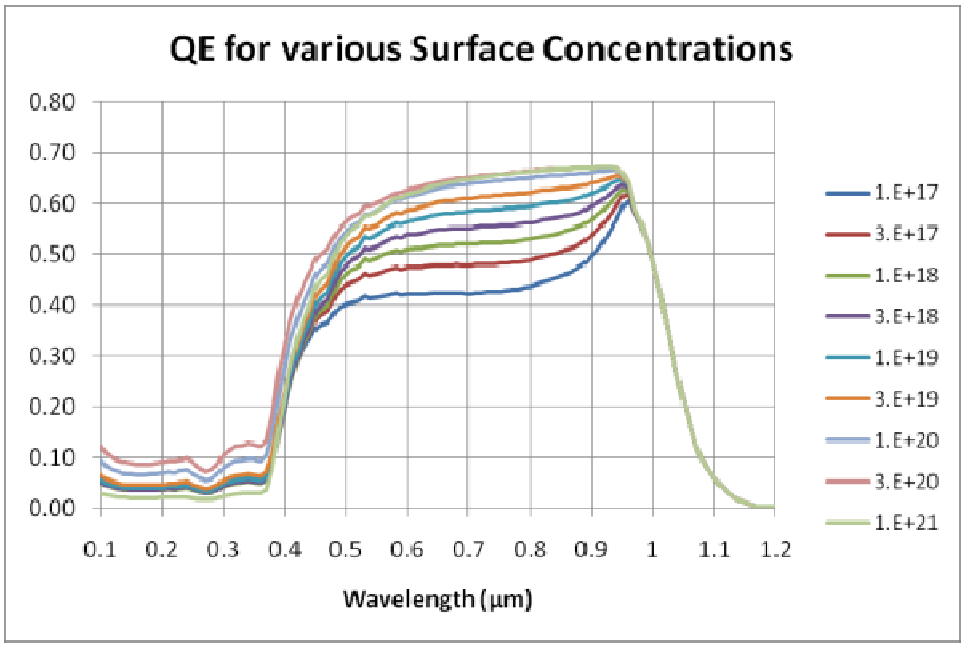


Fig. 3.13 Simulated QE curves for surface dopant concentrations ranging from $1x10^{17}$ $cm^{-3}$to $1x10^{21}$ cm^{-3}

The lack of a transparent conductive window on the light absorbing side of the detector placed an important constraint on the resistivity of the n^+ surface. The resistivity must be low enough that series resistance does not cause significant potential losses across the 1.9 x 3.8 mm detector. The peak surface concentration and homo-junction depth were varied to determine the optimum profile for device operation. The effect of varying the surface dopant concentration is shown in Fig. 3.13. Below a critical concentration of ~$1x10^{20}$ cm^{-3} the efficiency in the visible to near infra-red (NIR) range (500 – 900 nm) drops of significantly.

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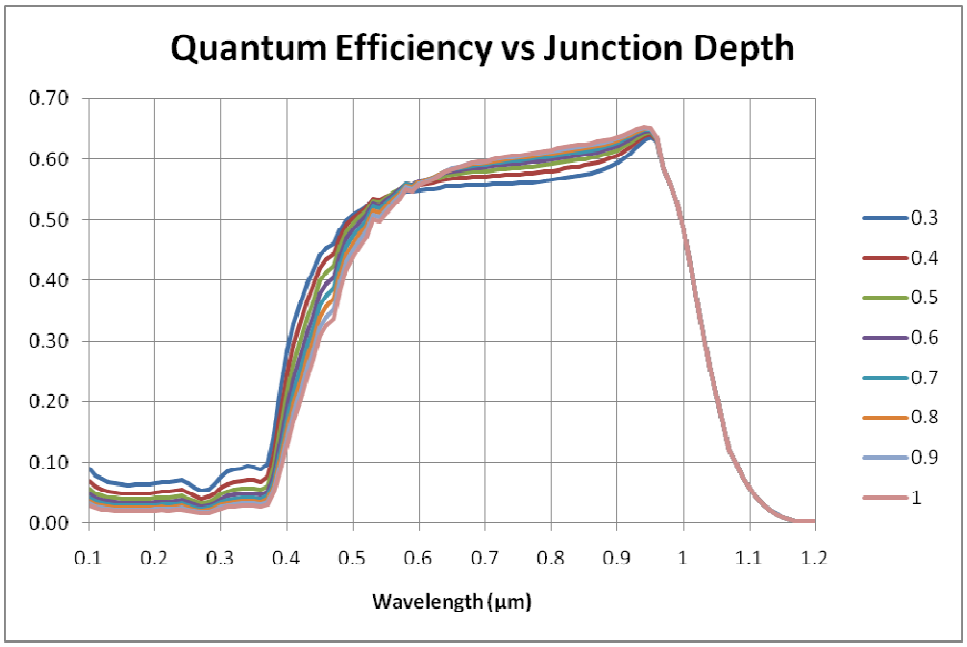


Fig. 3.14 Simulated QE curves for $n^+ - n^-$ homo-junction depths of 0.3 – 1.0 µm

Junction depth is an important parameter because it determines thickness of the un-depleted surface layer. Carriers generated in this surface layer must diffuse into the depleted region before they can be collected. For the devices under investigation in this work the intersection of the dopant profile with the background concentration is referred to as a homo-junction because the dopant on the light absorbing side is n-type, the same as in the substrate, so no metallurgical junction is formed. By specifying the junction depth the steepness of the Gaussian profile can be controlled. The junction depth was varied from 0.3 to 1.0 µm and the resulting QE curves can be seen in Fig. 3.14.

The junction depth did not have a significant effect on device performance throughout the entire spectrum. The small negative effect reducing the junction depth

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had at longer wavelengths is most likely due to the slight increase in resistance that would be caused by forcing the current flow through a shallower portion of the silicon. A positive effect can be seen at ~450 nm where the QE is increased by 10 %, although this does not translate to smaller wavelengths as was intended. The poor efficiency below 400 nm is most likely due to electron diffusion. The relative difference in electron concentration between the surface layer and the bulk silicon is ~8 orders of magnitude. The result is a significant tail to the profile created from the diffusion of electrons into the substrate region that increases the thickness of the un-depleted surface layer.

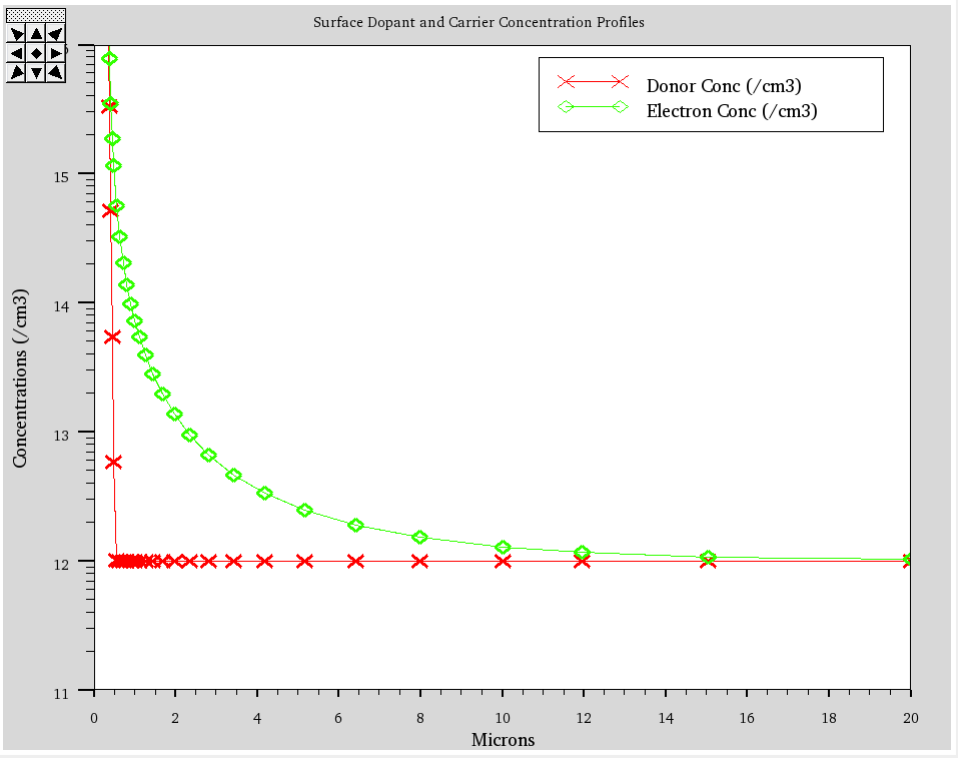


Fig. 3.15 Dopant and electron concentration profiles on *n*-type light absorbing side

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From the previous simulations it was determined that a surface concentration $N_{sur} \geq 5x10^{20}$ cm^{-3} was needed to prevent significant ohmic losses across the light absorbing surface. The junction depth was deemed to not be a critical parameter due to electron diffusion preventing a full depletion all the way to the metallurgical junction (see Fig. 3.15). This was advantageous as it allowed a relaxation of the thermal budget and for all implants to be done at RIT. The use of arsenic as an n-type dopant would have allowed for shallower junction depths to be created using ion implantation however it is unavailable in the RIT SMFL, therefore phosphorous served as the n-type dopant.

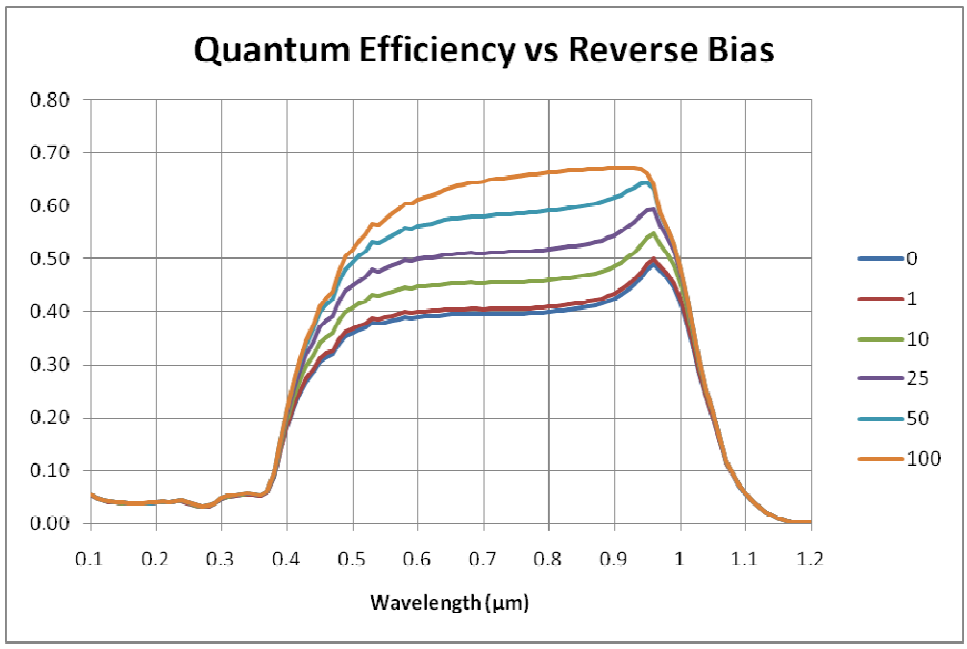


Fig. 3.16 Simulated QE curves for operating biases from 1 to 100 V

With the basic fabrication process parameters for the device determined, the detector operation was explored further by simulating the QE at various biases. Fig. 3.16

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shows QE curves for the detector biased at 1, 10, 25, 50, and 100 V. At low voltages the QE in the visible and NIR range is severely degraded. The QE reaches a maximum value at 100 V and simulations at higher voltage showed no addition improvements. The QE at wavelengths less than 400 nm are completely unaffected by the detector bias, again suggesting the carriers are being generated in a region that is not depleted.

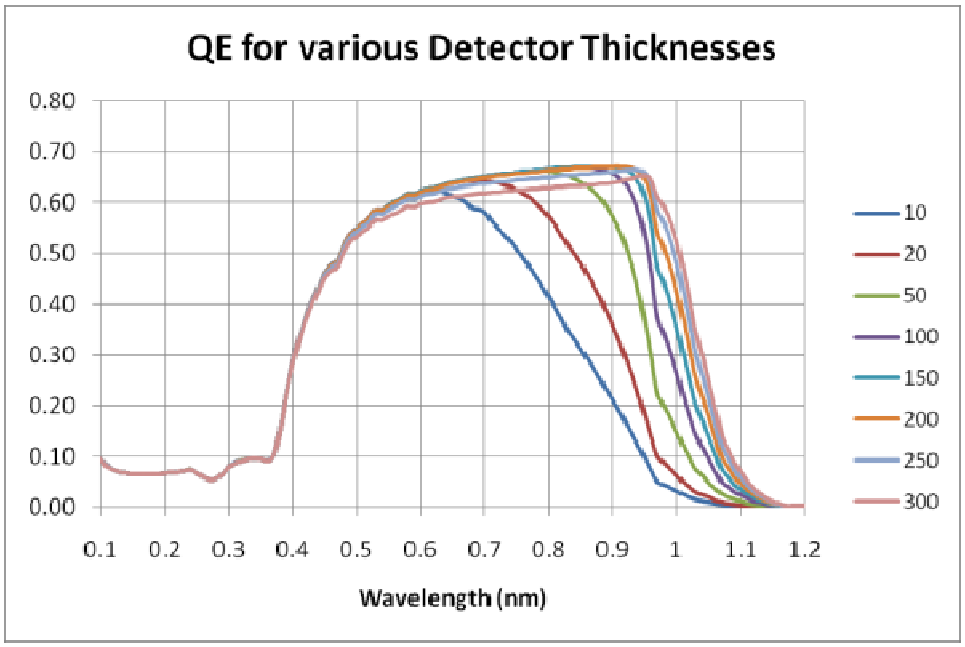


Fig. 3.17 QE curves for detector thicknesses from 10 to 300 μm

Although the thickness of the detector was determined by the substrates ordered for the project, the detector thickness was varied in simulations to demonstrate its effect on QE as shown in Fig. 3.17. The main effect increasing detector thickness has is to provide are greater volume of material for longer wavelength light to be absorbed within. At a thickness of 100 μm the efficiency has reached the maximum efficiency for all

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wavelengths less than 900 nm. Further increasing the thickness improves the 1 μm response until larger biases are required to maintain the efficiency.

3.3.3 Point Spread Function

To determine the PSF for a structure in the Atlas simulation program the uniform illumination is split into individual rays. A five pixel wide structure is solved for each of the rays individually and the current is plotted as a function of the position of the light source. A device 75 microns wide was defined in Atlas, the largest structure that could be simulated with adequate resolution due to the limit on the total number of grid points. The uniform monochromatic (600 nm) light was split into 150 rays and the current through each of the 5 pixels is plotted as a function or ray position in Fig. 3.18.

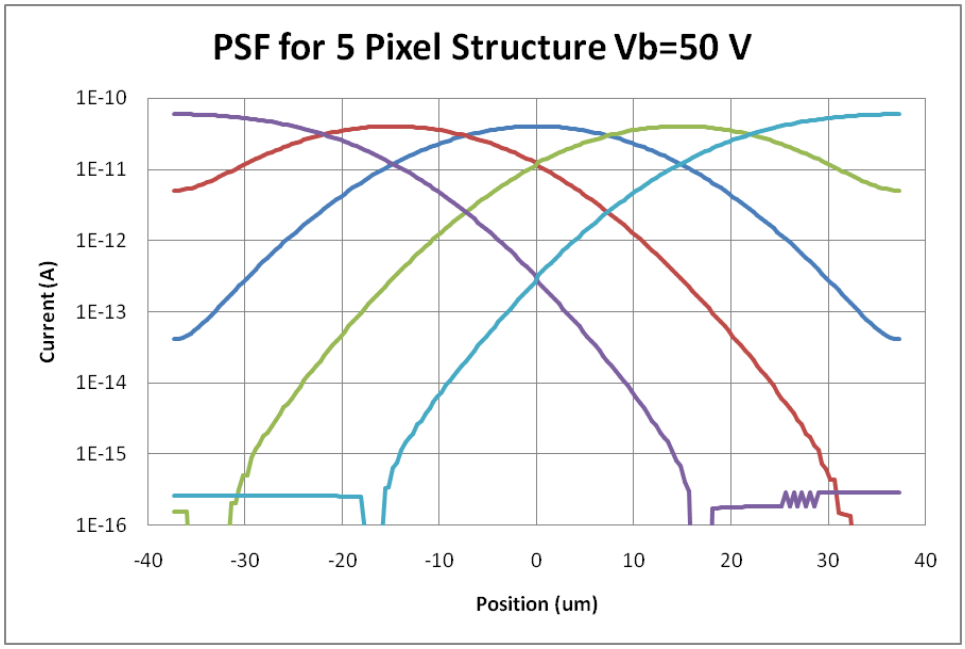


Fig. 3.18 Point spread function simulations showing current through pixels as a function of the source illumination position

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The curves can be seen to increase slightly towards the edge of the structure due to diffusion boundary conditions. The simulation software assumes the defined region of silicon is suspended in a vacuum and therefore does not allow any diffusion of carriers into or out of the lateral boundaries. The curve from each of the pixels is shifted to center the maximums in Fig. 3.19 showing this effect is only significant within a few microns of the boundary. This confirms the accuracy of the curve over the vast majority of the simulated region.

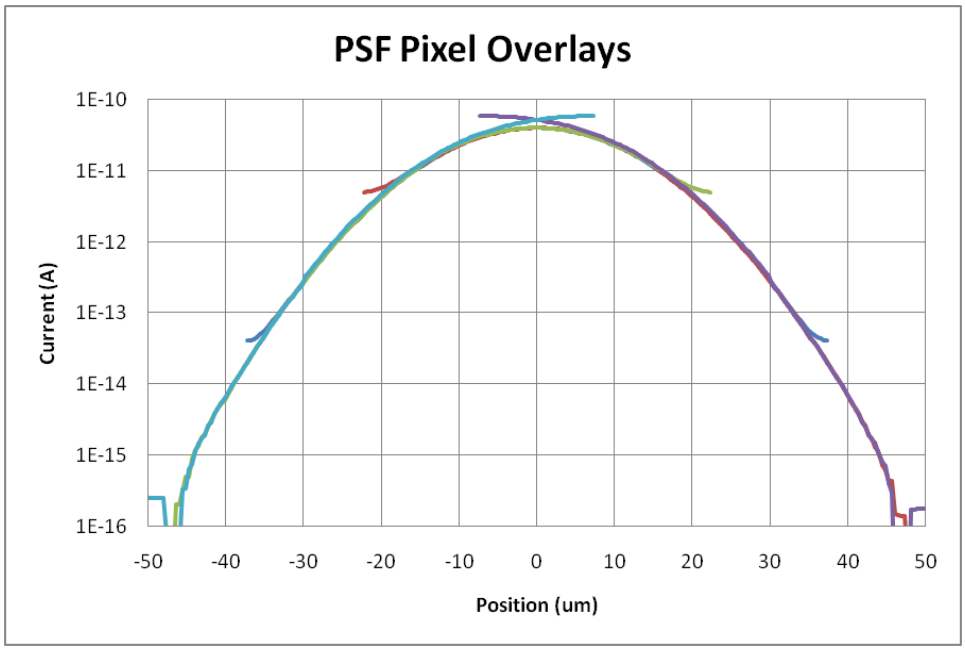


Fig. 3.19 Current through pixels overlaid with maximums centered

The point spread function was simulated as a function of the detector operating bias and the results are shown in Fig 3.20. At the designed operating bias, the full-width half-max (FWHM) of the PSF is significantly larger than the 15 µm pixel pitch. The

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consequence is an appreciable charge is expected to leak between adjacent pixels. This result is in line with literature that suggests over-depletion of the detector is required for best performance [25]. The 50 V used here is just enough to deplete the full thickness of the detector. For larger electric fields the FWHM of the PSF decreases rapidly.

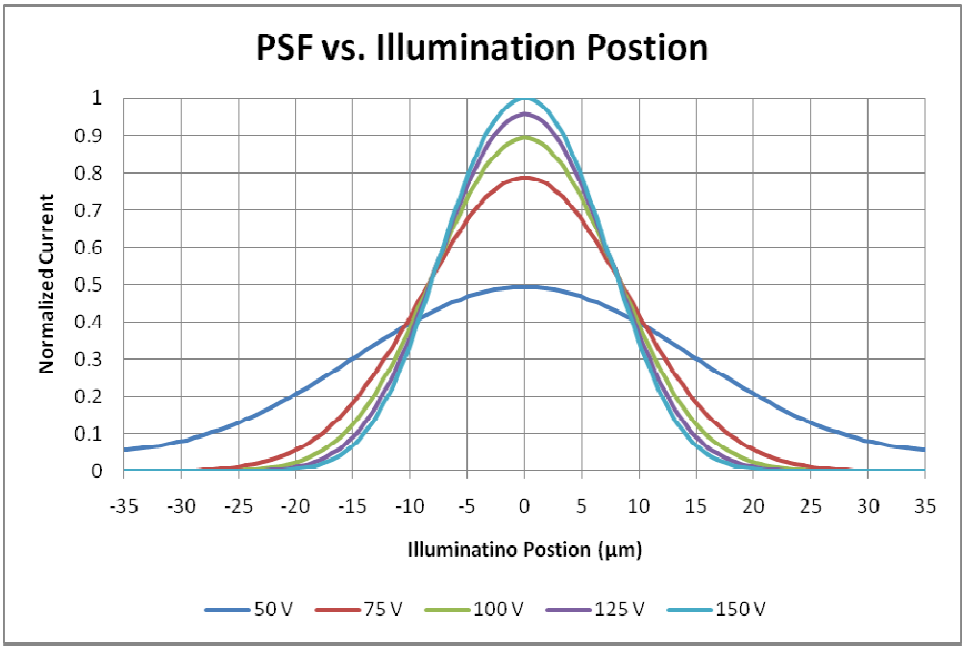


Fig. 3.20 Simulated current vs. illumination position for 50, 75, 100, 125 & 150 V

The amount of lateral diffusion is determined by temperature, electric field, and the depth at which the carriers are generated. Increasing either the electric field or generation depth reduces the transit time, which is the amount of time carriers have to diffuse. The location of carrier generation is determined by the wavelength and the optical properties of the material. Current versus illumination position curves were

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generated for wavelengths from 100 to 1200 nm at electric fields of 2 – 6 kV/cm. The FWHM of the curves were extracted and plotted as a surface graph shown in Fig. 3.21.

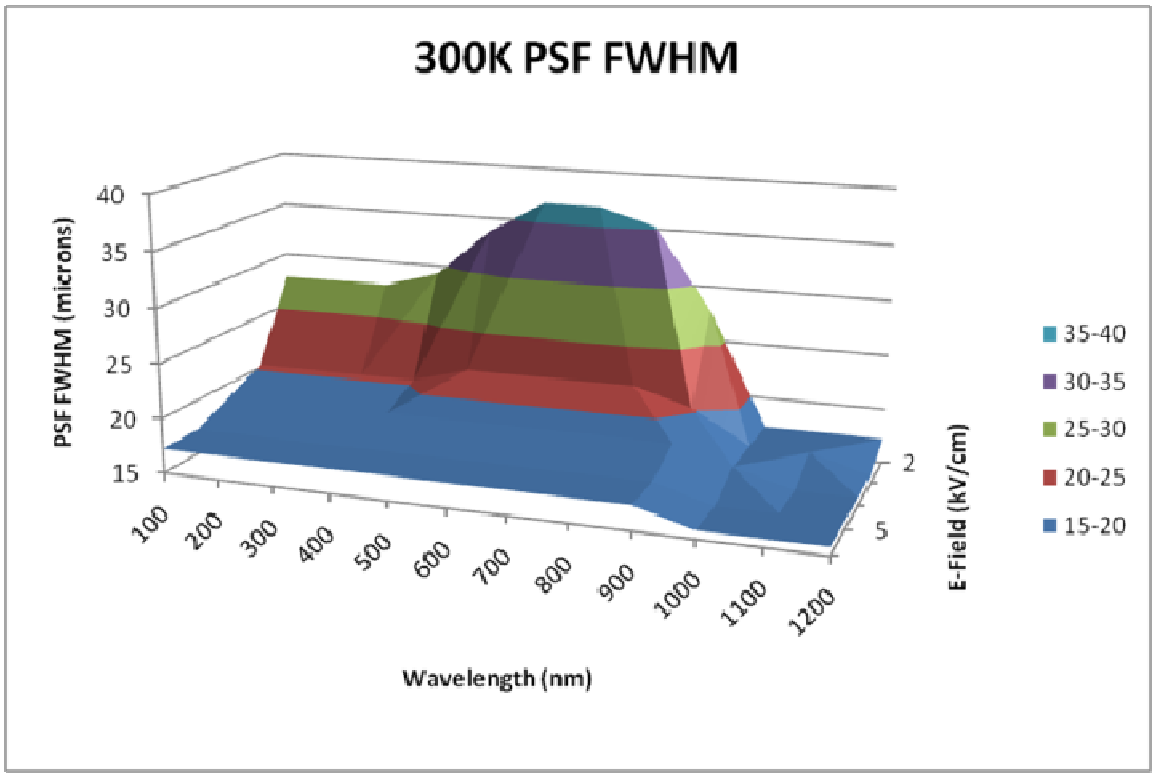


Fig. 3.21 FWHM of Simulated PSF for 100 – 1200 nm and 2 – 6 kV/cm at 300 K

The diffusivity and mobility are both influenced by the temperature of the device, and related by the Einstein relationship. As the temperature is decreased both the mobility and diffusivity increase though at different rates. Diffusivity is directly related to temperature; however the $T^{-3/2}$ dependence nested inside mobility dominates and causes the diffusivity to increase slightly at lower temperatures. The net result of reducing the temperature is an increase in carrier velocities compared to the relative diffusivity, resulting in decreased lateral diffusion.

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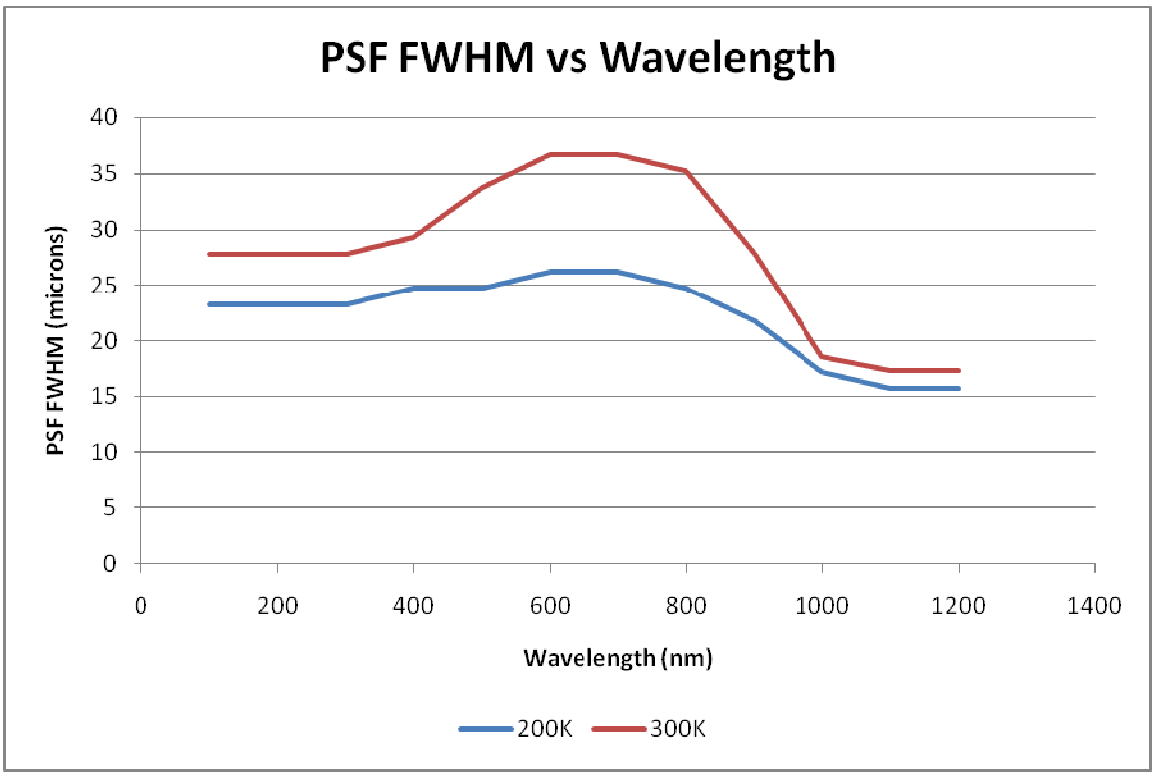


Fig. 3.22 Full width half max of point spread function vs. wavelength at 2 kV/cm for 200 K and 300 K

The effect of temperature is most prominent at lower electric fields and becomes nearly insignificant at fields greater than 4 kV/cm. The FWHM of the PSF is plotted as a function of wavelength at 200 K and 300 K in Fig. 3.22. At longer wavelengths carrier generation occurs throughout the thickness of the device, and again temperature has a subdued impact.

A greater understanding of effect wavelength has on the PSF can be attained by plotting the minority carrier concentration distributions within the device during steady state operation. The distributions are shown in Fig. 3.23 for various wavelengths at the designed operating bias with the point source illumination centered on the device. The

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lateral diffusion is most prominent in the 500 – 900 nm range of wavelengths, where most of the light is absorbed within the depletion region. At shorter wavelengths below 400 nm all of the carrier generation occurs within the first 100 nm of silicon, and carrier must diffuse into the depletion region reducing the concentration gradients by the time they arrive. At wavelengths greater than 900 nm the majority of carrier generation moves deeper within the device reducing the time carries have to diffuse laterally.

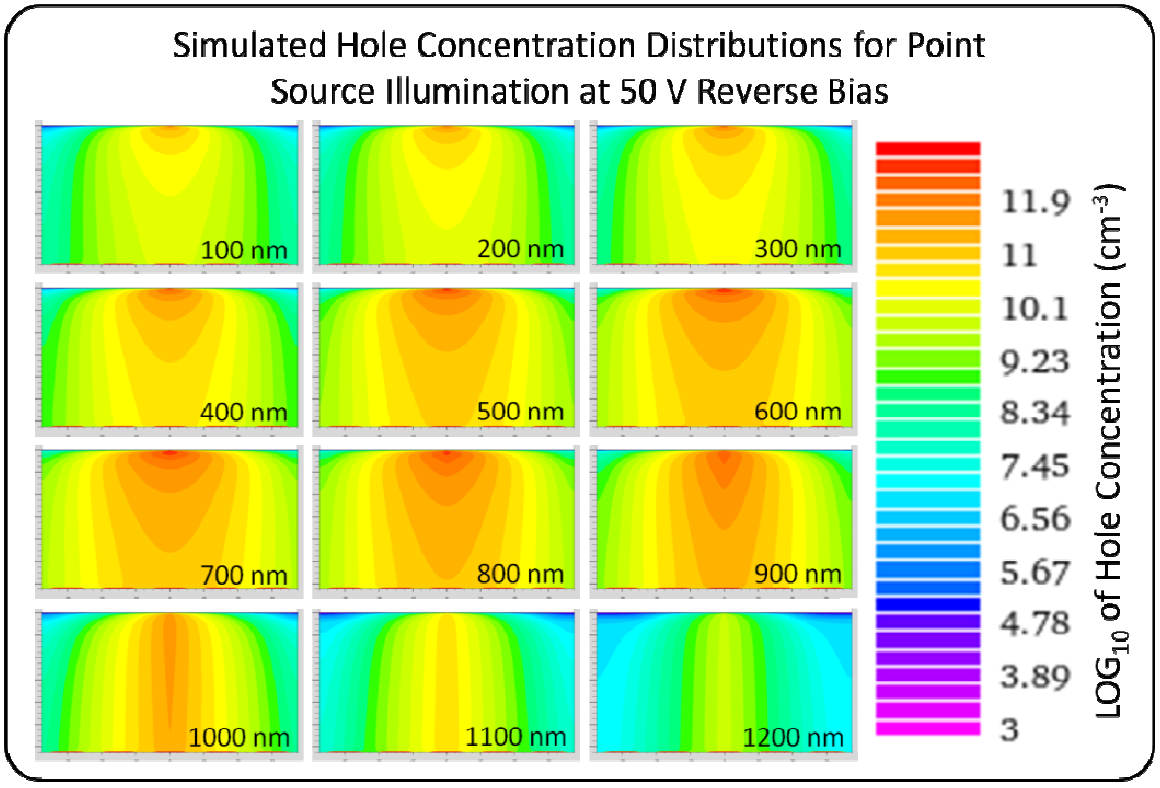


Fig. 3.23 Simulated hole concentration distributions for centered point source illumination at 50 V reverse bias and 300 K for various wavelengths in 5 pixel structure

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Chapter 4

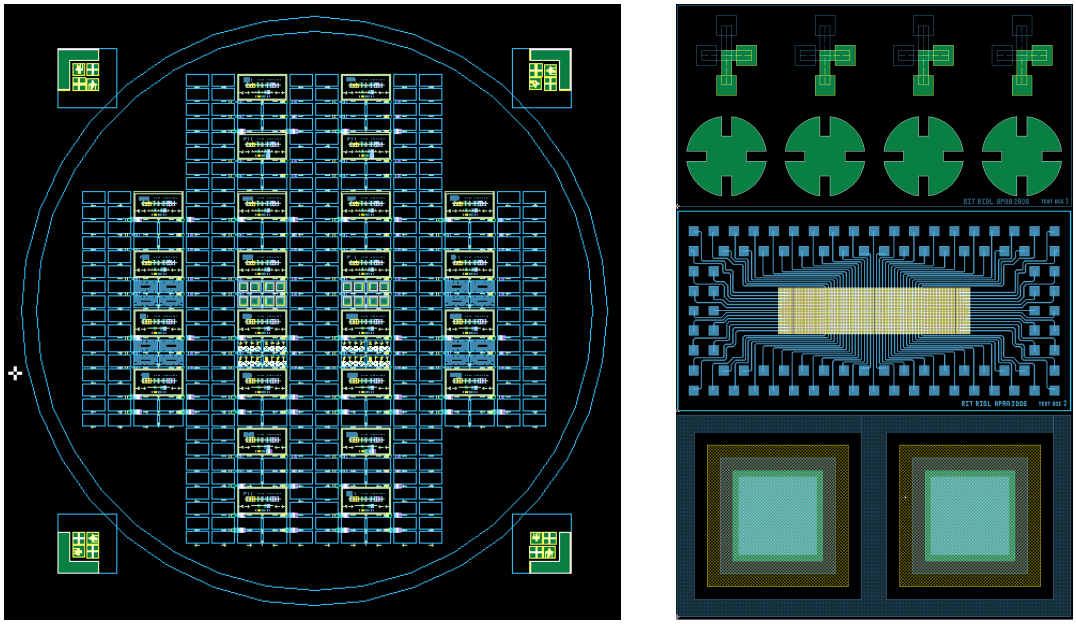
Layout and Fabrication

Wafers were fabricated in three process runs that subsequently incorporated the revised process flow, a new mask set, and finally the newly developed processes in each run. Electrical testing was performed to characterize device performance and evaluate process improvements. The first fabrication run used the existing contact mask set with the revised process flow to significantly reduce the number of process steps and related wafer handling in an attempt to limit the introduction of defects and contamination. The second process run incorporated a new mask set using both contact and projection lithography systems with the newly developed contact cut and dry aluminum etch processes. The final process run benefitted from lessons learned during the first two runs and included several process revisions.

4.1. Existing Layout

This thesis builds upon work performed by Kolb during the 2007-2008 academic year [26]. Devices were fabricated using a process by Kolb as part of the capstone project for her Bachelors degree. The layout for the previous work is shown in Fig. 4.1 with all levels of the contact mask set overlaid.

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(a) (b)

Fig. 4.1 CAD rendering of contact lithography mask layout of (a) entire wafer and (b) close-up of test structures

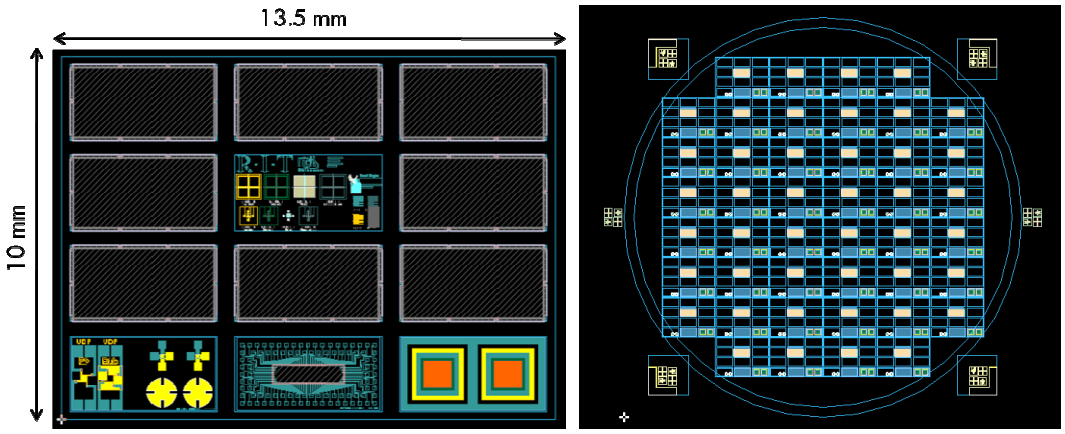
The process used contact alignment exclusively and relied upon manual alignment of the front and back layers. The test features in the mask set included cross-bridge Kelvin resistors, cloverleaf structures, an array with individually indexed pixels and two large test pixels.

4.2. Mask Design

The need for enhanced resolution and depth of focus on critical mask levels warranted the use of projection lithography and the need to create a new mask set. The lithography tool used was a GCA Automatic Wafer Stepper (AWS) with a g-line illumination source (436 nm) and a 5X reduction system yielding a minimum resolution of ~ 750 nm. A 10 mm x 13.5 mm die shown in Fig. 4.2 (a) was designed that

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incorporates 8 diode arrays, 3 test die, and a die that contains alignment marks and resolution features. This die has been arrayed to produce a contact mask shown in Fig. 4.2 (b). Alignment marks have been applied outside the four inch radius where the wafer is positioned to allow the alignment of one mask to another on the contact lithography system enabling the revised font-to-back side alignment process.



(a) (b)

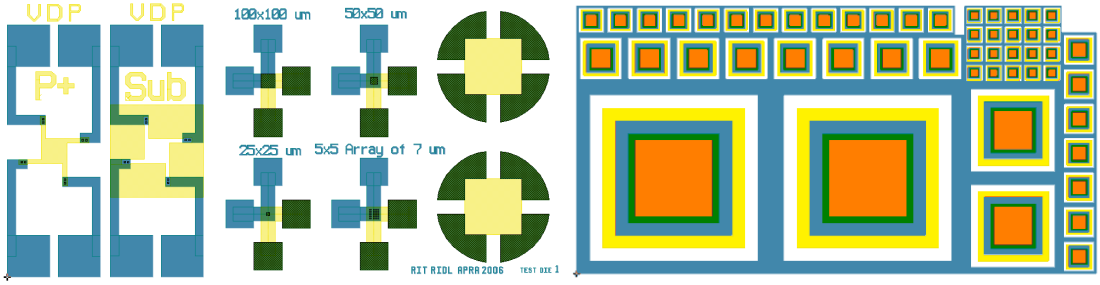
Fig. 4.2 CAD renderings of **(a)** projection die and **(b)** contact mask layout

4.2.1 Revised Test Die

Two of the test die were designed to provide additional process characterization. Additional Van der Pauw structures were included to measure the sheet resistance of the implanted layers through multiple structures. The relative percent of activated dopant can be determined from the conductivity. The cross-bridge Kelvin resistor structures were revised to vary the size and number of contacts between the metal layer and the implanted regions to determine the contact resistance. These test structures are shown in

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Fig. 4.3 (a). The pixels in the imaging array are too small to probe manually (15 μm), therefore enlarged versions were created of varying size to allow actual pixel performance to be extrapolated. The scaled pixels, shown in Fig. 4.3 (b) are 10, 15, 18, 25, 50 and 100 times the size of the device pixels. By including pixels of varying size, the area and perimeter contributions to leakage currents are able to be determined.



(a) (b)

Fig. 4.3 CAD renderings of **(a)** Process characterization test die and **(b)** Pixel characterization test die

4.3. Process Flow

A revised diode fabrication process was designed that dramatically reduced the number of steps and tools the wafers were subjected to. The number of process steps was cut nearly in half to ~ 35 steps and the use of low pressure chemical vapor deposition (LPCVD) and rapid thermal processing (RTP) systems have been eliminated. A thermal oxide grown in the initial steps of the process serves as a protective layer, substrate isolation, and anti-reflective layer. The method for front-to-back-side alignment used was altered to allow alignment to be performed on the contact alignment tool as opposed

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to the 'by hand' process under a microscope currently used. Figure 4.4 provides a summary of the key steps in the revised flow and a complete process flow in included in Appendix II.

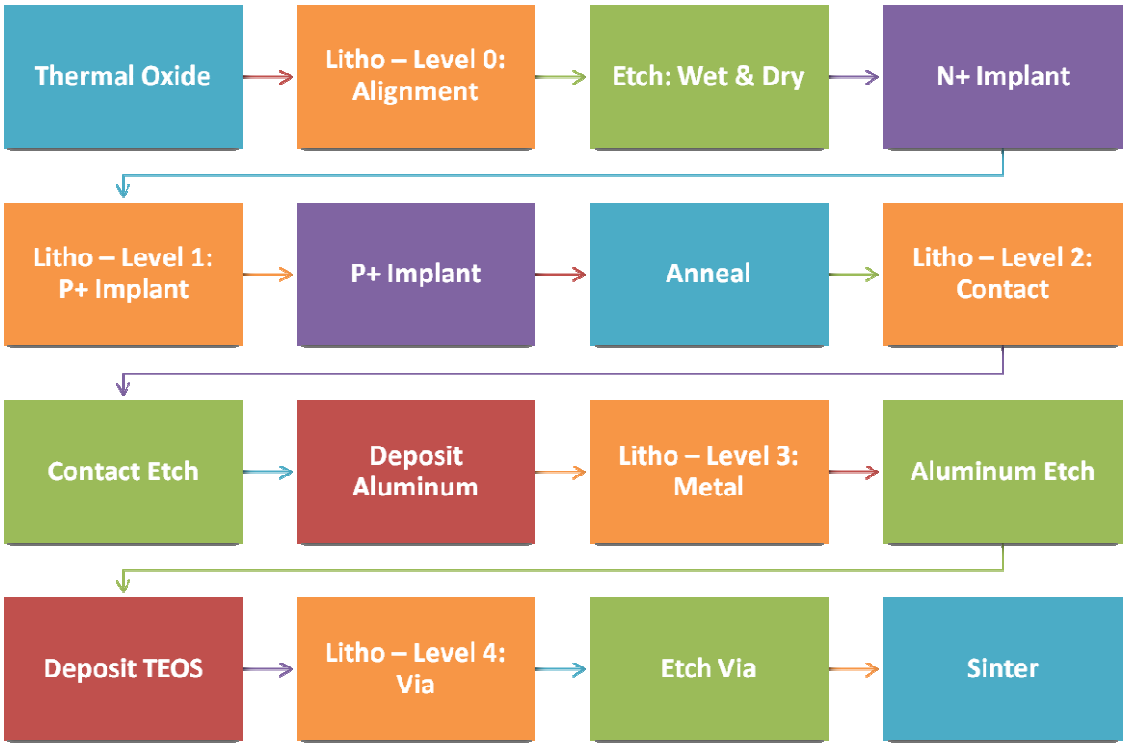


Fig. 4.4 Summary of key steps in revised process flow

First a thermal oxide was grown to serve as a protective layer against contamination as well as an anti-reflective layer. The first lithography step was used to define alignment features on both sides of the wafers. The features were then transferred into the oxide using a wet etch and into the substrates using a dry etch process. The light absorbing side of the wafers then received a blanket phosphorous implant to reduce the resistance of the surface layer to prevent ohmic losses and allow for a suitable contact to

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be made. The backside of the devices were patterned and implanted with boron to define the pixels. Next a thermal anneal was performed to activate the dopants and repair the implant damage. The contact lithography level was patterned onto each side of the wafer separately and then the oxide was removed using a wet etch with the opposing side of the wafer protected by a blanket layer of resist. Aluminum was sputtered onto both sides of the wafer and patterned with the metal layout. A TEOS passivation layer was deposited onto the backside of the wafer and vias were etched to open contacts for the bump bonds. Finally a sinter was performed to ensure a good contact between the aluminum and silicon substrate.

4.3.1 Front–to–Backside Alignment

The purpose of the first lithographic levels on both the front and back side of the wafer is to etch features into the silicon that can be used as alignment marks for all subsequent lithographic processes. Therefore the ability to ensure these two layers are aligned to each other is paramount to device performance. The process used to align these two layers has been revised from one which requires the manual alignment of the masks under a microscope to one where the contact lithography tool is utilized for all alignment events. The manual process requires significantly larger tolerances in the

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design as mis-alignment of less than 20 μm is difficult to achieve. The revised process can regularly achieve front-to-back side alignment within 5 or less microns.

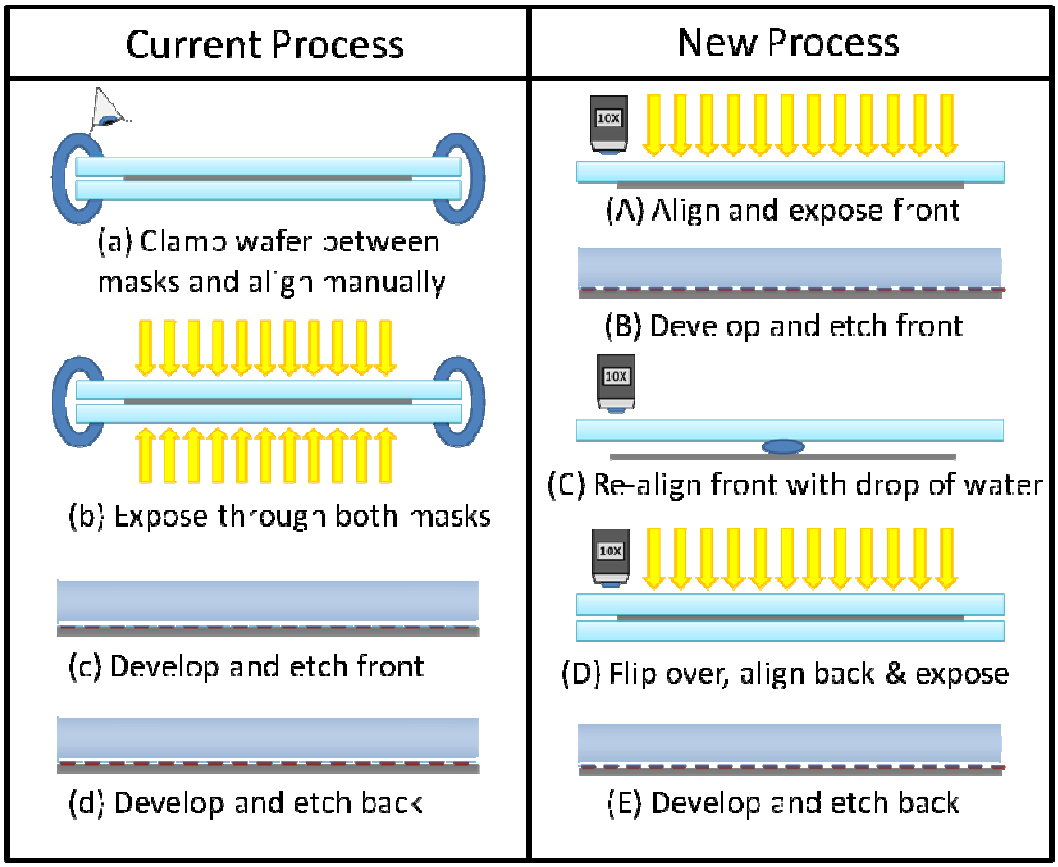
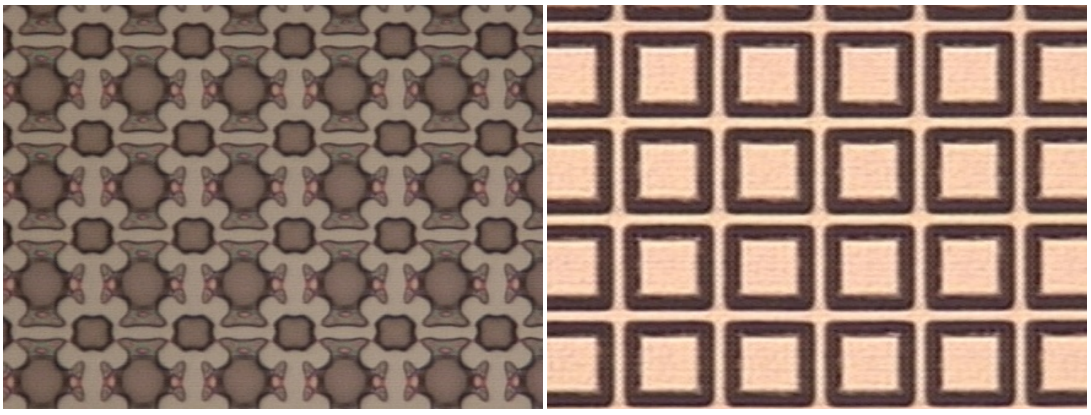


Fig. 4.5 Comparison of current and newly developed front-to-back side alignment process

A comparison of the current and new front-to-back side alignments processes are shown in Fig. 4.4. In the old process the wafer was clamped between the two masks and aligned manually underneath a microscope (Fig. 4.5 (a)). The wafer is then exposed through each mask (Fig. 4.5 (b)) and developed and etched on both sides (Fig. 4.5 (c) & (d)). A newly developed front-to-back side alignment process will allow the alignment of the masks to be performed on the contact alignment tool.

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First, the wafer is coated with resist on a single side, and the alignment marks are exposed into the wafer (Fig. 4.5 (A)). The wafer is then developed and the marks are etched into the wafer (Fig. 4.5 (B)). The wafer is loaded back onto the contact tool with a drop of water on the surface and the mask is aligned with the previously etched features (Fig. 4.5 (C)). The drop of water ensures that once the wafer has been aligned to the mask, they can be removed from the system without any movement between the two. They are placed back into the system, flipped over so the mask is in contact with the vacuum chuck and the back side of the wafer is ready for exposure. The second mask is loaded and the two are aligned to each other on the contact tool (Fig. 4.5 (D)). The back side is then exposed, developed and the alignment marks are etched into the wafer (Fig.4.5 (E)). Optical micrographs showing the improvement of the resist image from the metal lithography layer on the bump bond side of the device are shown in Fig 4.6.



(a) (b)

Fig. 4.6 Optical Micrographs of Metal layer pattern after **(a)** contact lithography **(b)** projection lithography

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4.3.2 Contact Cut Etch

During initial fabrication runs multiple failure mechanisms were observed during the contact cut etch process. A wet etch in 10:1 buffered oxide etch (BOE) was used and the process of record (POR) called for manual agitation. The method of agitation was defined as lifting the boat of wafers out of the bath and placing them back in.

Two defects were observed as a result of the etch process including an inability to fully clear a contact and a dramatically increased etch rate at the oxide-resist interface. An optical micrograph of the defect can be seen in Fig. 4.7 where the affected contacts exhibit a large colorful ring that is sometimes accompanied by brownish spots in the center. The colorful rings are due to a region of varying oxide thickness and the dark spots are thin regions of oxide most likely ~50 nm thick. It was initially believed that this was the result of an interaction between the two common problems of resist scumming and poor adhesion. Although poor adhesion was an issue at times, the main contributing factor was not discovered until much later while performing experiments for another process.

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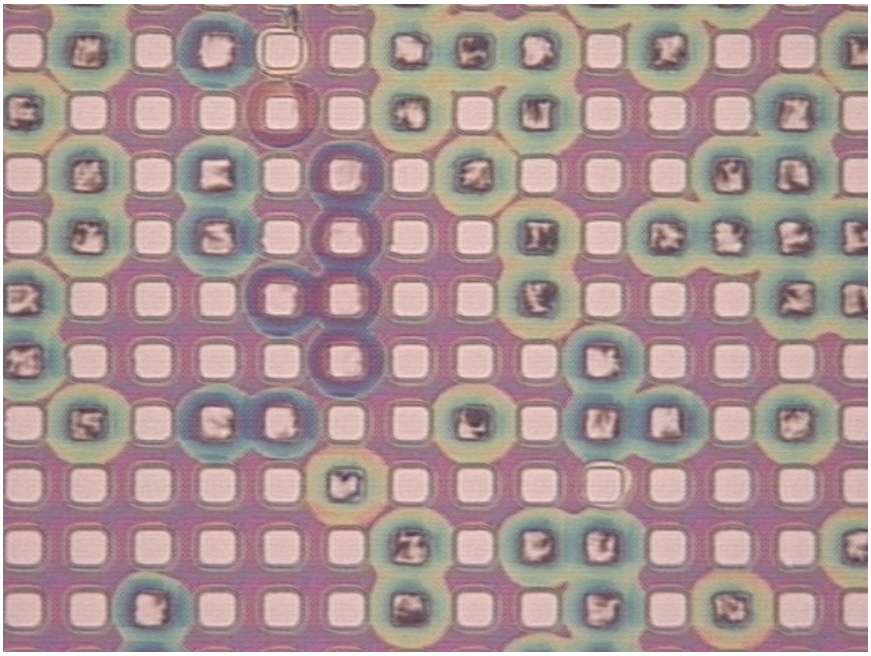


Fig. 4.7 An optical micrograph of the array after contact cut etch where the failure mechanism can be observed

During a wet process a fluid is drawn into a reservoir typically several microns square in size and one or two microns deep with relatively vertical sidewalls. As the fluid reacts with the underlying layer a cavity is formed below the film of resist. The development of the LOR layer used in during hybridization is a similar process, though with slightly thicker layers. It was discovered during the development of this process that if the surface of the wafer was dried after an initial exposure to the developer solution, rewetting the surface caused a very similar defect. An optical micrograph of the defect in the LOR layer can be seen in Fig.4.8.

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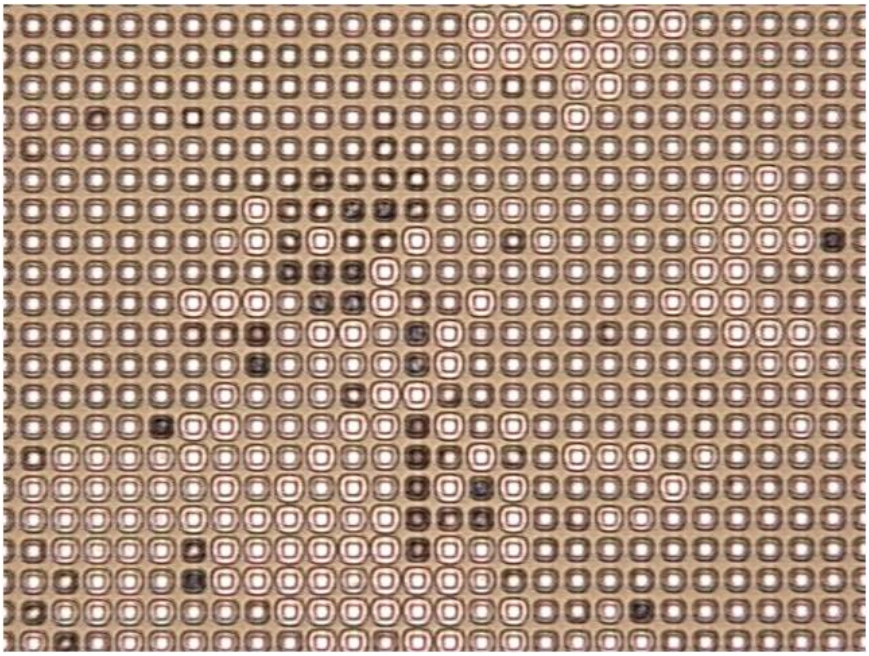


Fig. 4.8 Optical mirograph of features in LOR layer exhibiting blow-out and scumming

The proposed hypothesis for this mechanism is the formation of a cavity affects the ability of the fluid to flow into the feature. Any air trapped in the feature as the wafer is rewet prevents reaction at the bottom and enhances it at the interface. Combined with poor adhesion at the interface this can cause the feature to become severely blown-out and still not fully clear at the bottom.

4.3.3 Aluminum Dry Etch

The metal lithography level on the bump bond side of the wafer is a critical level as it contains the smallest features in the design. A 1 μm border of metal is defined around the outside of each pixel creating a 2 μm wide metal grid between adjacent pixels. The pattern transfer for this level was previously accomplished using a wet etching

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process, although significant undercutting led to the erosion of these lines as shown in Fig. 4.9.

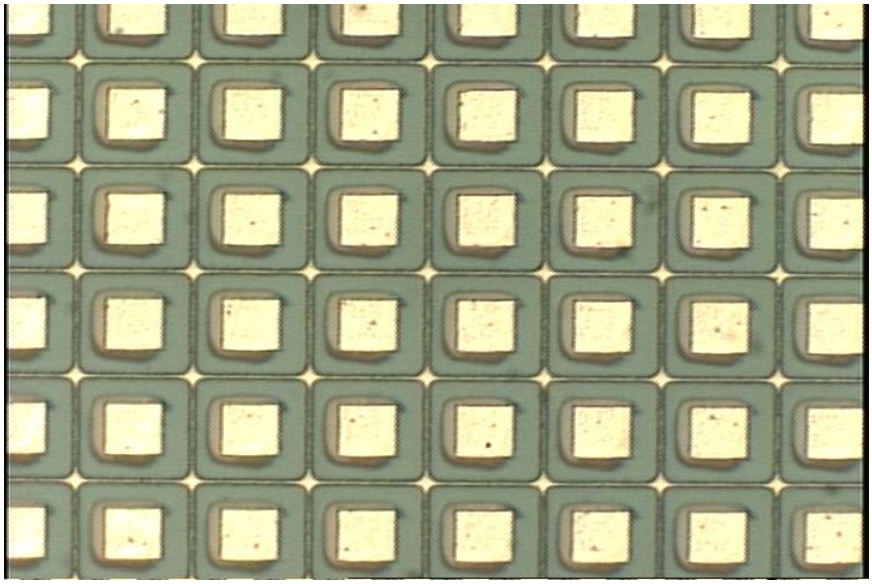


Fig. 4.9 Patterned aluminum layer on bump bond side of device showing thin grid lines due to undercutting during wet etch process

A dry aluminum etch process was developed based on a designed experiment performed a LAM 4600 Metal etcher at Xerox. This is the same model of chlorine dry etch tool available at the SMFL. The tool was designed to process 150 mm wafers and therefore carrier were required to process the 100 mm wafers used in this study. The carriers consist of a 150 mm wafer with a 105 mm circle recess in the center that serves as a pocket to contain the smaller wafer. Although necessary there are several drawbacks associated with the use of a carrier including reduced thermal conduction and capacitive coupling between the substrate and chuck. The recipe from the aforementioned study was used as a starting point for the aluminum dry etch process. An optical micrograph of

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resolution features from a test mask after the initial etch was performed is shown in Fig. 4.10.

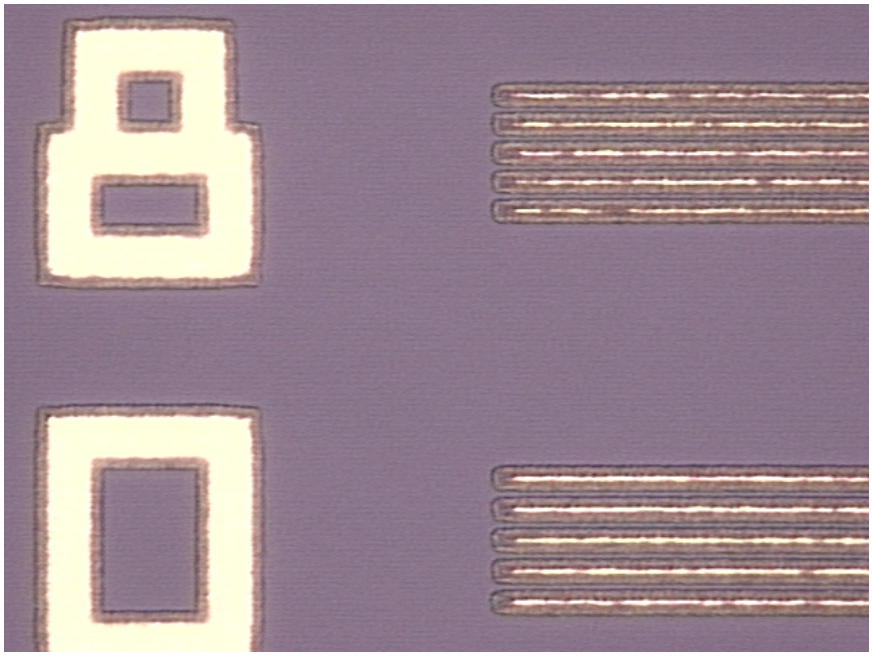


Fig. 4.10 Resolution features etched into aluminum layer using suggested recipe. Note significant undercut of resist features

A significant undercutting of resist features was observed in the initial test wafer, likely due to the introduction of the carrier wafer. The photoresist was also aggressively attacked during the etch and appeared to be shriveling under the intense heat. The inability to use the water passivation system also necessitated the immediate removal of the photoresist to prevent corrosion of the aluminum. Removing the photoresist with an oxygen plasma strip left residues behind so a solvent based process was used.

In order to reduce heat transfer into the wafer and make the etch process more anisotropic several recipe parameters were altered. The experiment found that RF power

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had the strongest effect on resist burning with minimal effect on etch rate due to the predominantly chemical nature of the etch and so was reduced significantly. The undercutting was believed to be a result of insufficient sidewall polymer deposition due to the increased temperature of the wafer. Reducing the power and thus heat transfer into the wafer should also help mitigate this problem, however the gas flows were also modified slightly to provide a more polymerizing mixture. A thinner aluminum layer was also used to reduce the total etch time prevent resist burning. The result of the optimized etch recipe can be seen in Fig. 4.11. A significant improvement over the wet process can be seen eliminating the risk of open circuits in the grid.

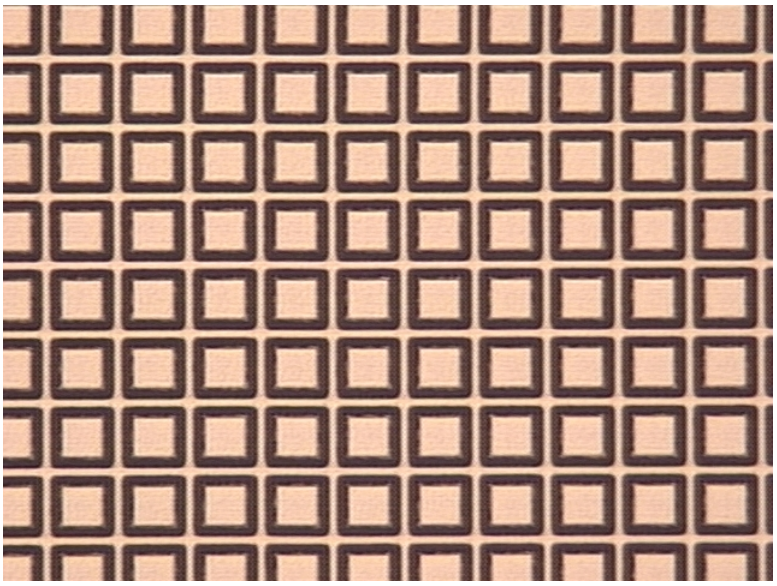


Fig. 4.11 Patterned aluminum pixel contacts dry etched with optimized recipe

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Chapter 5

Electrical Testing

Once the fabrication sequence was completed the test diodes structures were measured electrically to determine device performance and quality. The two aspects of device performance evaluated in depth were the on-state ideality factor and off-state leakage. Scaled versions of the diodes were measured to separate area and perimeter effects and extrapolate the performance down to an actual pixel. Carrier lifetimes were determined using the OCVD method and spectral and cryogenic testing was performed.

5.1. Previous Results

The current voltage characteristics of devices fabricated by Kolb are shown below in Fig. 5.1. In forward operation the different modes of current transport are not readily apparent and have rather indistinct transitions. The ideality factor increases rapidly within a couple hundred millivolts, and a large series resistance appears to prevent the device from delivering expected current density levels.

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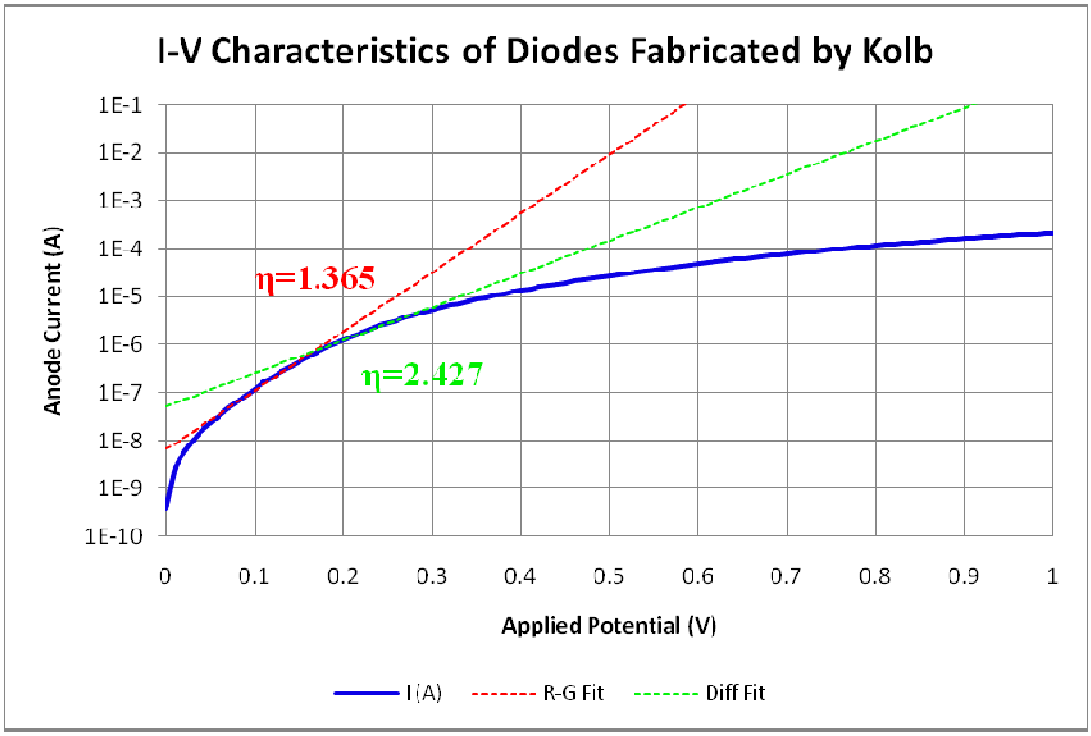


Fig. 5.1 Representative current-voltage characteristics of *p-i-n* diode fabricated by Kolb with ideality fits [26]

The reverse bias current voltage characteristics of several devices are shown in Fig. 5.2. Extremely high leakage current densities are observed as well as non-uniform device behavior. The minimum recorded leakage current of $2x10^{-6}$ A/cm^2 was almost three orders of magnitude higher than the stated goal. It is believed the use of the LPCVD system for deposition of passivation layers introduced contamination to the devices. The trap centers associated with the contamination resulted in severely degraded on and off-state performance.

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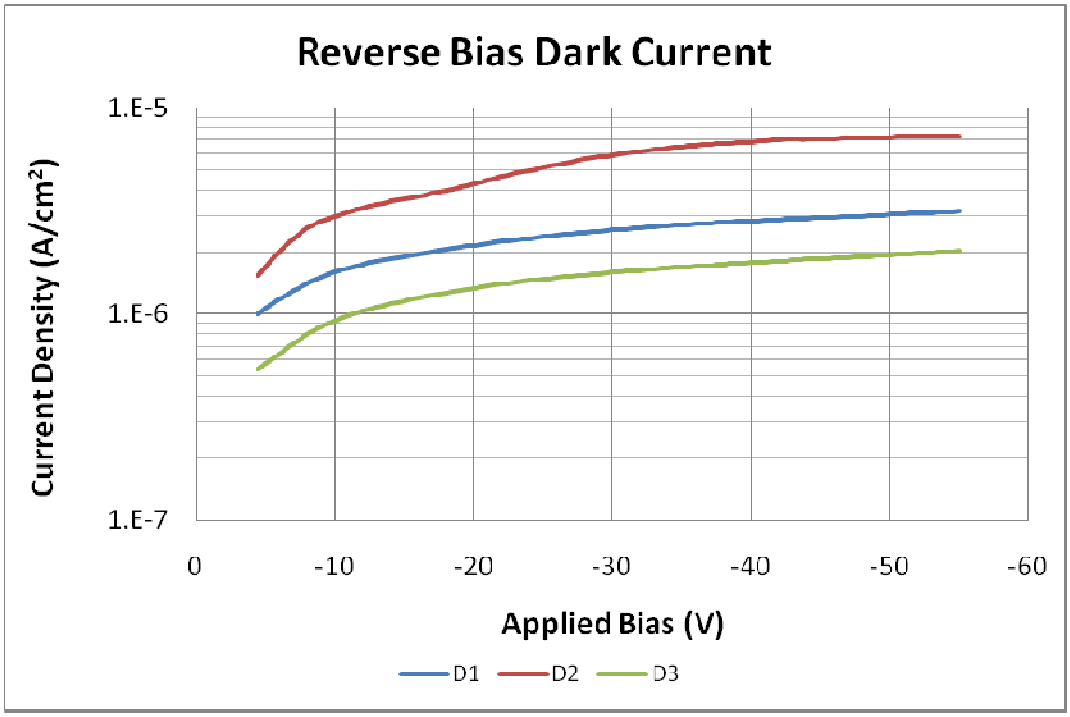


Fig. 5.2 Reverse bias leakage current densities for several devices fabricated by Kolb

5.2. Current-Voltage Characteristics

Electrical testing was performed in a shielded dark box on the 25X test diode structures to determine pixel performance. Current-voltage characteristics were obtained with high voltage resolution in the on-state, and high current resolution in the off state. The devices exhibited high quality diode behavior with low leakage levels. The currents levels at a reverse bias of 50 V were mapped across the wafers to evaluate the uniformity of the leakage currents. Measurements were also performed on a cryogenic testing station to observe the temperature dependence of device operation.

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5.2.1 On-State Ideality

A representative forward bias I-V characteristic is shown in Fig. 5.3 selected from one of the wafers sent for bonding. In the forward bias mode the device exhibited several distinct regions of operation. Similar to the simulation results in Chapter 3 an ideality factor of nearly 2 is extracted at lower biases, however a diffusion dominated regime with an ideality factor of ~1 is not observed. This is thought to be a soft transition into high-level injection, and series resistance dominating at higher current levels.

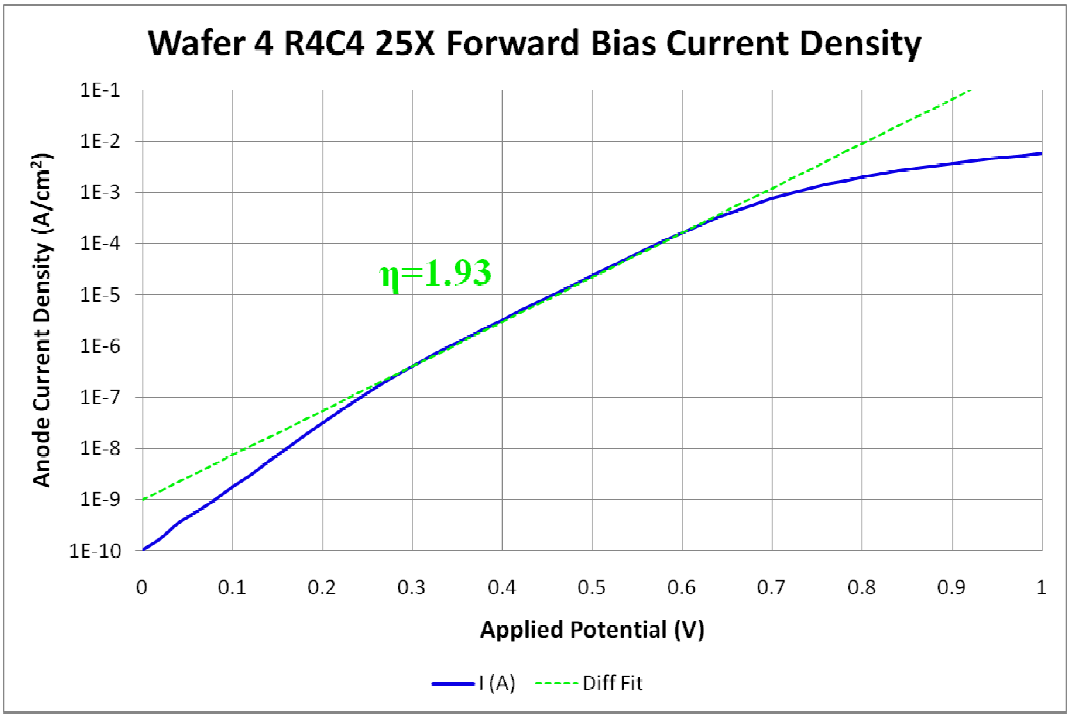


Fig. 5.3 Measured forward bias I-V characteristics of rev3 *p-i-n* diode with exponential fits and resulting ideality factors

Measurements were performed on a cryogenic testing station cooled with liquid nitrogen at temperatures ranging from 250 to 350 K. Unfortunately due to degraded insulation within the cryogenic probes leakage currents from the test set-up dominated

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over currents from the device at temperatures below 250 K. Thus although a clear dependence upon temperature is seen at the higher temperatures, no dependence is seen below 250 K. Despite this issue, the relationships observed at the upper temperature range were used to extrapolate device performance at lower current levels.

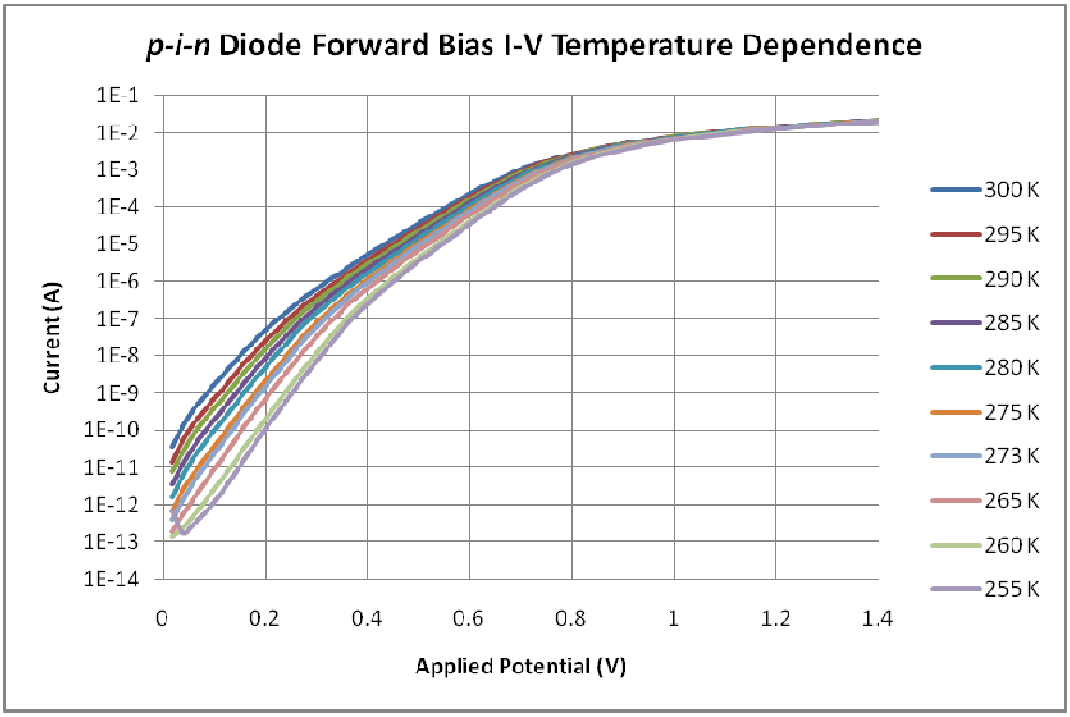


Fig. 5.4 Forward bias I-V characteristics of 25X p-*i*-n diode measured from 255 K to 300 K showing temperature dependence

The forward bias current-voltage characteristics for a 25X p-*i*-n diode are shown in Fig. 5.4 for the temperature range of 255 K to 300 K. A dependence on the temperature is seen for applied voltages below 800 mV, although when the device reaches the high-injection/series resistance limited regime temperature no longer has any influence. At the lower applied voltages reducing the temperature increases the ideality

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factor but reduces to total current flow. The increase in ideality factor could be due to the lifetime of the carriers increasing faster than the diffusion rate decreases.

5.2.2 Off-State Leakage

The off-state leakage current of test diodes was the primary metric used to determine the quality of the devices. The devices are intended to be used primarily in the reverse bias condition and the leakage current directly attributes to read noise in the final detector. Several sites were sampled from each wafer of the final two fabrication runs and the best wafers from each run were mapped to determine the uniformity and reliability of the process. An interior 25X scaled test diode was used to make all of the reverse bias measurements except for the spectral response.

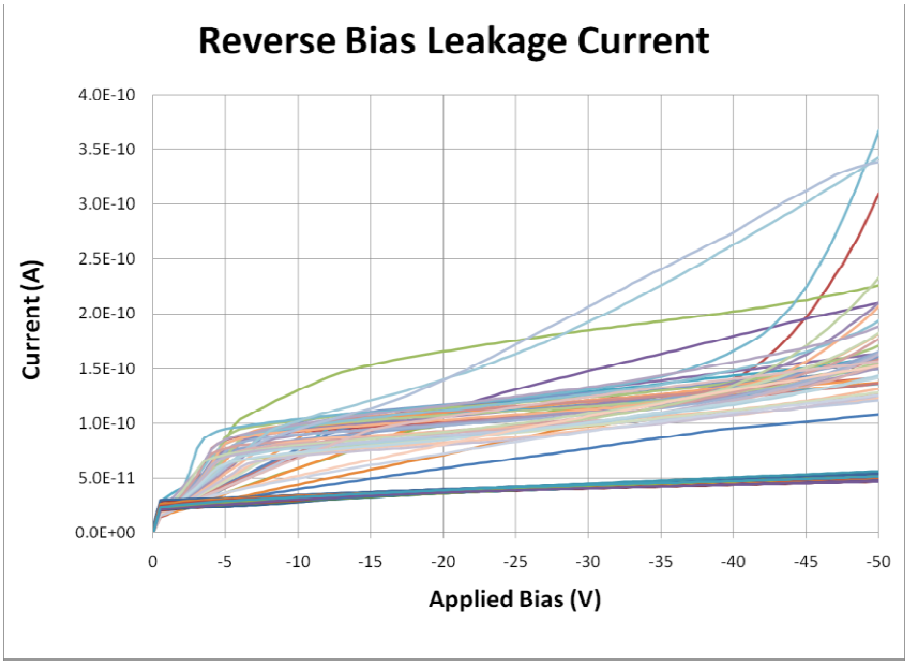


Fig. 5.5 Overlay of reverse bias leakage currents from best wafer of the final two processing runs

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An overlay of the leakage current measurements taken from the best wafer of the final two processing runs is shown in Fig. 5.5. Two distinct groups of devices are observed where the group with a larger average leakage and variation was measured on wafer 4 from the second process run and the tightly grouped measurements were made on wafer 1 from the third process run. The devices fabricated in the second process run allow a greater amount of current to flow before stabilizing and continue to show a greater dependence on the applied bias. Soft breakdown mechanisms are observed in several devices and a few other devices appear to simply be resistors with their current varying linearly with applied bias. The final process run significantly reduced both the average leakage currents as well as the variation.

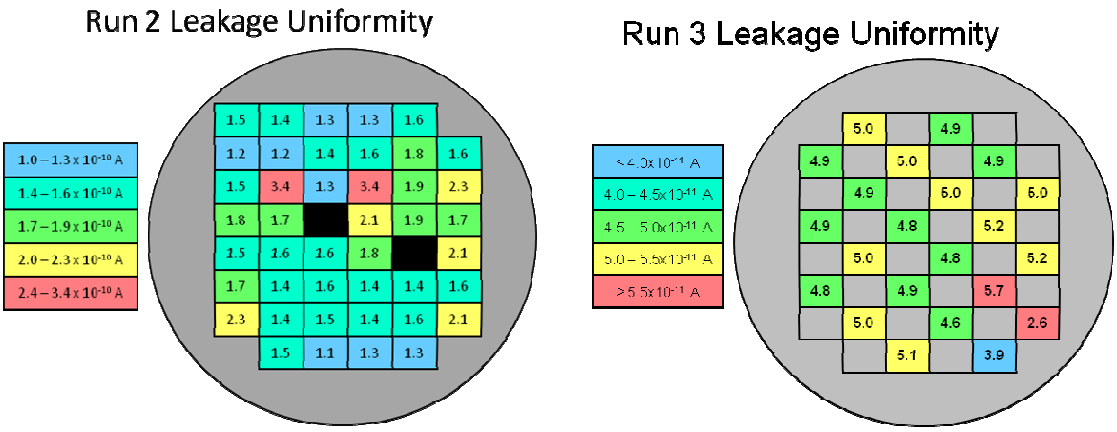


Fig. 5.6 Wafer map of leakage current uniformity for final two processing run.

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Wafer maps of the uniformity leakage currents for each of the final two processing runs, show in Fig. 5.6, were created by selecting the current at the designed operating bias of 50 V. No distinct patterns were observed in the yield of the devices.

Temperature Dependence

The reverse bias characteristics of a high quality device was measured at different operating temperatures using the same cryogenic testing station described earlier. Reverse bias measurements were made at temperatures from 260 to 350 K and are shown in Fig. 5.7. Temperature dependencies below 260 K were unable to be observed due to leakage paths in the test setup introducing too much noise. Leakage currents measured through the probes were at equivalent levels to those generated within from the devices.

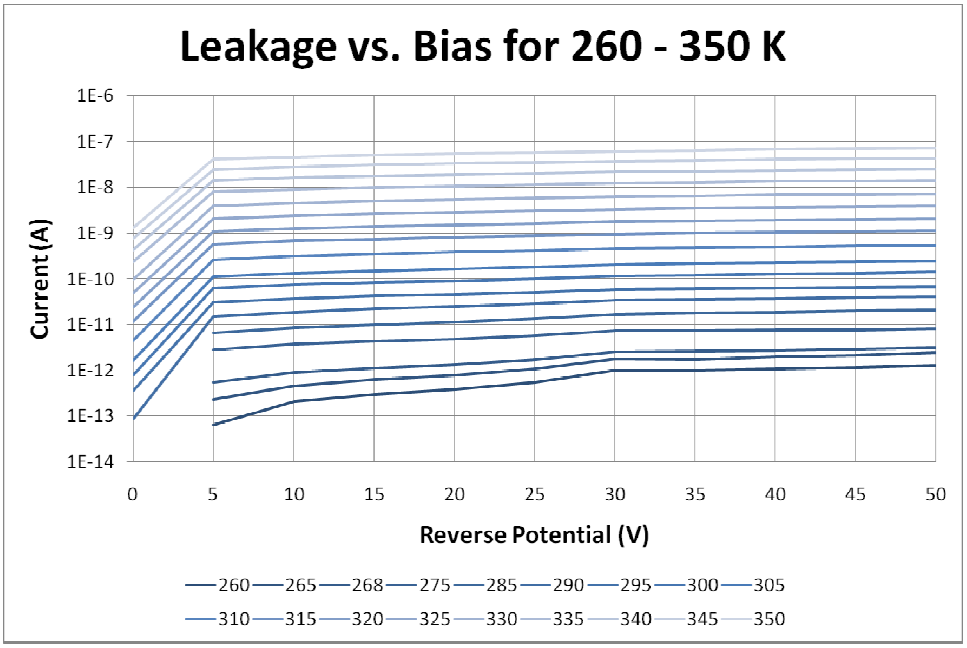


Fig. 5.7 Measure reverse bias leakage current vs. applied potential from 260 to 350 K

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The current level at a reverse bias of 50 V was plotted against the temperature the measurement was made at. The observed relationship differs slightly from theory in that an Arrhenius equation was difficult to match with the data. The best fit resulted from a linear extrapolation of the data on a semi-log plot. The extrapolation shown in Fig. 5.8 predicts an additional drop in leakage currents of three orders of magnitude at the designed operating temperature.

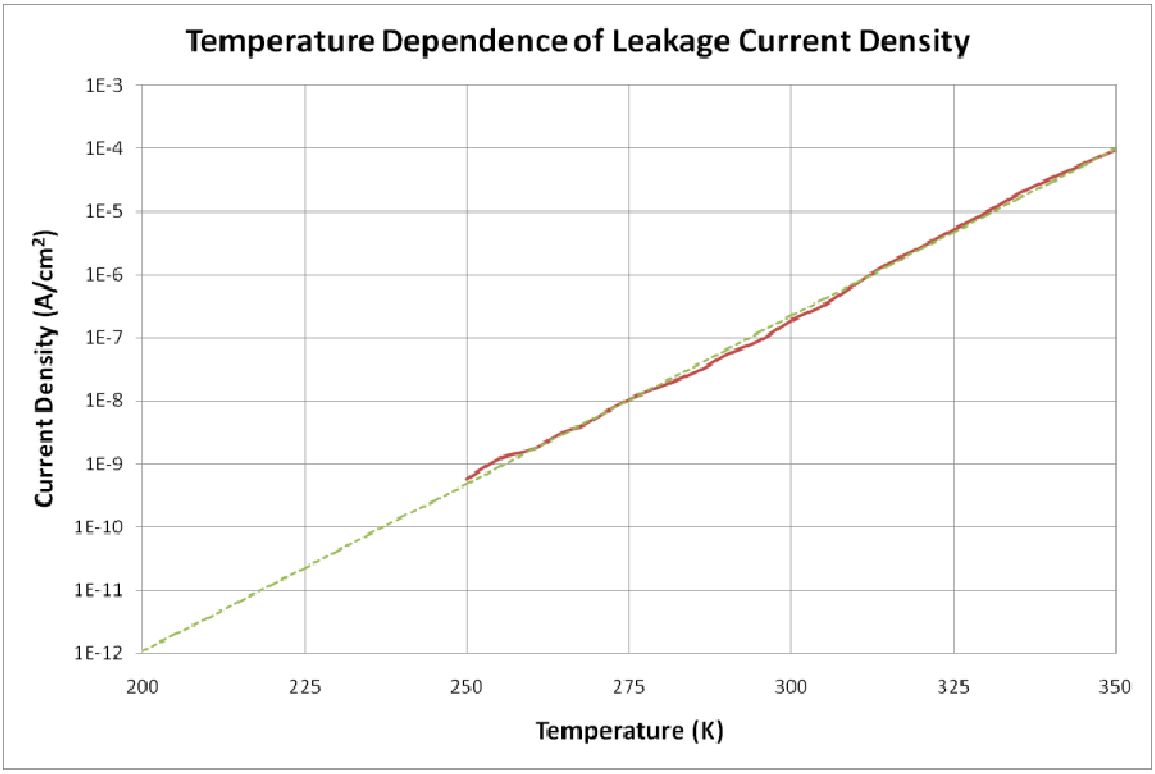


Fig. 5.8 Reverse bias leakage current density at 50 V from 250 to 350 K with exponential extrapolation down to 200 K

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TABLE 3 COMPARISON OF REVERSE BIAS LEAKAGE GOALS, SIMULATIONS AND EXPERIMENTAL RESULTS

	200K Goal	300K Goal	Previous Results	Simulated	Rev3	200K Extrap.	
	1	1.65×10^{4}	1.14×10^{7}	5.35×10^{5}	4.94×10^{5}	8.08	e/sec/pixel
Current	1.6×10^{-19}	2.64×10^{-15}	3.00×10^{-8}	8.57×10^{-14}	4.95×10^{-11}	8.09×10^{-15}	A/pixel
Current Density	1.32×10^{-13}	2.18×10^{-9}	1.51×10^{-6}	7.09×10^{-8}	6.55×10^{-8}	1.07×10^{-12}	A/cm^2
Side Length	11	11	1408	11	275	275	um

A summary of the previous results, simulated result and experimental results is shown in Table 3 along with a comparison to the goals of the project. The final fabrication sequence came extremely close to meeting the goals. At the designed operating temperature of 200 K it is expected to be a difference of sever electrons per second. The simulated results also demonstrated remarkable similarity to the experimental.

5.3. Junction Lifetime Measurements

Lifetime measurements were performed on fabricated devices using the open circuit voltage decay method. A high speed switch with high input impedance was used to create the open circuit condition. The switch was controlled by a function generator tied to an oscilloscope measuring the junction voltage. A resistor was placed in series with the device to provide a current limiting element. The lifetime is extrapolated by an exponential fit to the experimental data as shown in Fig. 5.9.

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The extracted lifetime for the data shown in Fig. 5.9 was about 1 microsecond. This is three orders of magnitude lower than the value specified by the substrate manufacturer although it must be remember this measurement is being made in direct vicinity of the junction. The excess charge creating the junction voltage decays at a faster rate due to high dopant concentrations and defects created during implant. A measurement of the lifetime within the bulk of the device would likely yield different results.

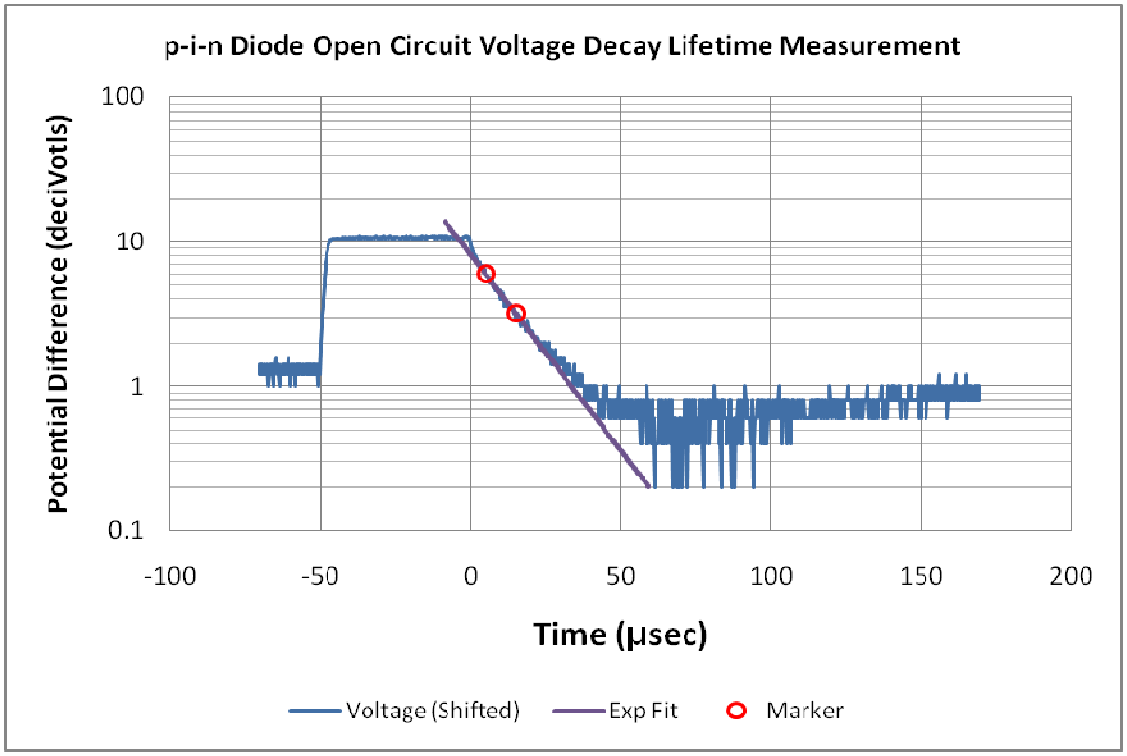


Fig. 5.9 Diode junction voltage decay with exponential fit

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5.4. Spectral Response Measurements

The quantum efficiency of fabricated devices was unable to be measured due to a lack of adequate testing equipment, although a similar type of test was able to be performed. The test setup used was designed for solar cell testing and thus allowed for the illumination of specific wavelengths and the ability to measure the current in the device but without an applied bias. The current was measured with the device in a short circuit configuration and the results are shown in Fig. 5.10. A general idea of the spectral response of the device can be observed although no explicit inferences into actual device performance can be made. The device does exhibit a good response all the way up to 1000 nm light.

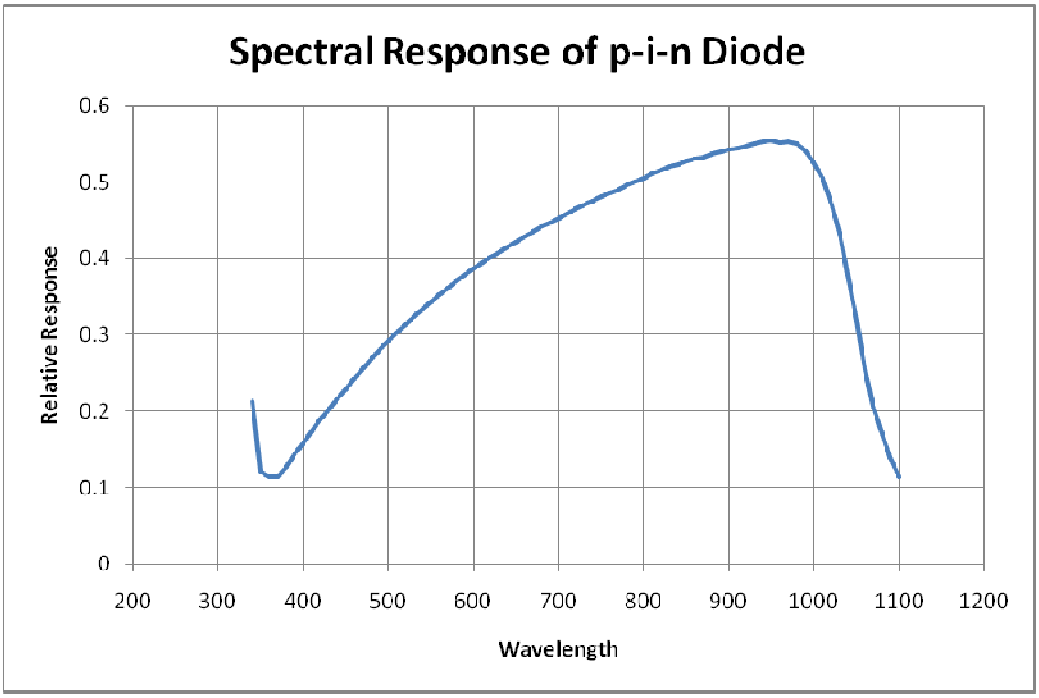


Fig. 5.10 Short circuit spectral response of *p-i-n* diode

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Chapter 6

Hybridization

The hybridization technique chosen for this project used a flip chip process with indium bump bonds. A summary of the process is depicted in Fig. 6.1. The wafers were coated with resist and patterned at RIT in the SMFL. The bump bond material was deposited at JPC and the flip chip bonding and packaging took place at STC. The selective deposition of bump bond material was accomplished through a lift-off process. An undercut resist profile is required to create a discontinuous layer for lift-off and several processes were evaluated including negative resists, image reversal, and multilayer stacks. Constraints imposed by the flip chip bonding process and the capillary forces needed for the epoxy under-fill required several microns of spacing between the bonded die. This spacing dictated the required height of the bump bonds, and the thickness of the resist layers needed for the lift-off process. Once coated with indium the lift-off was performed at STC using an N-Methyl-2-pyrrolidone (NMP) solvent stripper with ultrasonic agitation. The parts were then aligned and bonded using the Karl Seuss FC-150. The final step was to fill the space between the chips and bump bonds with an epoxy designed to provide both mechanical stability and protection from moisture and other environmental effects that can lead to corrosion and failure in an under-fill process.

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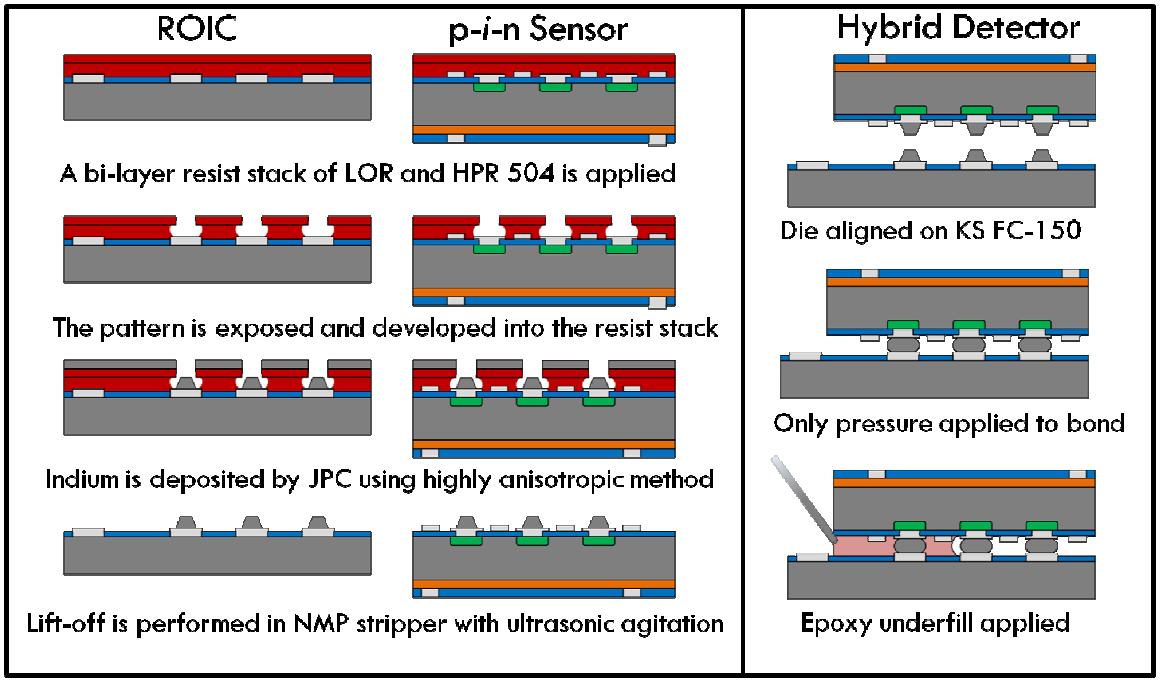


Fig. 6.1 Schematic representation of lift-off and flip chip bump bonding technique used for hybridization process

6.1. Lift-Off Process Development

Metal layers for flip chip bump bonding need to be quite thick relative to the typical thickness of thin films deposited in the semiconductor industry. The bonded die need to be separated by several (~ 3-5) microns after bonding to allow capillary forces to draw the epoxy in during the under-fill process. The bumps must be even taller than half the die spacing to account for leveling error in the bonding tool, variations in substrate thickness and compression of the bumps during bonding. For this project a bump height of 3 μm was targeted for both diode and ROIC die.

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A lift-off process relies upon the ability to create an undercut step height that causes a discontinuity in a deposited material. The discontinuity allows the deposited material to be removed in desired regions where the lift-off material remains. This is easily accomplished for thin layers (up to ~500 nm) and there are many standard materials and processes, however thicker layers present unique challenges. A standard rule of thumb in lift-off processing is that resist layers must be ~3-4 times thicker than the material being deposited. To achieve thick resist layers the materials must have a high viscosity and be spin applied at low speeds leading to uniformity issues. The thick layers also pose difficulties for the lithography processes where depth of focus becomes an issue. There is also a tradeoff between the profile of the undercut and the density or proximity of adjacent features

The method of deposition also plays a role in determining the lift-off process. Evaporation is a relatively anisotropic deposition process where the atoms mostly follow a line-of-sight path, although it would be difficult to achieve the desired thicknesses through thermal evaporation. Sputtering is a more isotropic deposition method due to the random collisions that occur in the plasma and requires a more pronounced undercut to ensure the creation of a discontinuity. For these reasons a proprietary process known as Jet Vapor Deposition (JVD) was selected for its high throughput and anisotropy.

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Jet Vapor Deposition is a deposition process invented by the Jet Process Corporation that “uses sonic jet nozzles, operating in chambers at ambient temperature (<100° C) and low vacuum (1-5 Torr), to deposit dense, adherent, high quality films at rates far higher than competitive techniques [JPC website].” The process creates a sonic jet of inert gas through a nozzle into which it evaporates the desired material. The material is carried as a vapor to the substrate in a collimated jet with a diameter of about ½”. The jet is then scanned across surface of the substrate by moving either the jet or the substrate. The size of the particles created in the JVD process is relatively large compared to sputtering, and thus their velocities are less affected by random collisions leading to highly anisotropic deposition.

6.1.1 Previous Development Work

A lift-off process was developed by Kolb that utilized a bi-layer resist stack consisting of FujiFilm HPR 504 on Microchem LOR-30A [26]. Microchem LOR is a polymethylglutarimide (PGMI) based ‘lift-off resist’ that acts as the sacrificial layer. The chemical does not contain a photoactive compound and therefore requires a second layer for pattern definition. The solubility of the LOR layer can be tailored by the soft-bake to help achieve the desired profile. Fujifilm HPR504 is the standard g-line photoresist used at RIT for projection lithography on 100 mm substrates.

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The LOR-30A was spin coated onto the substrates at 2000 rpm for 45 seconds to achieve a thickness of 4 μm and soft baked at 190 C for 60 sec. The HPR504 was then applied at 2500 rpm for 45 sec and soft-baked at 125 C for 60 sec. The resulting thickness of the total film stack was ~5 μm. A scanning electron micrograph of a bump bond opening is shown in Fig. 6.2.

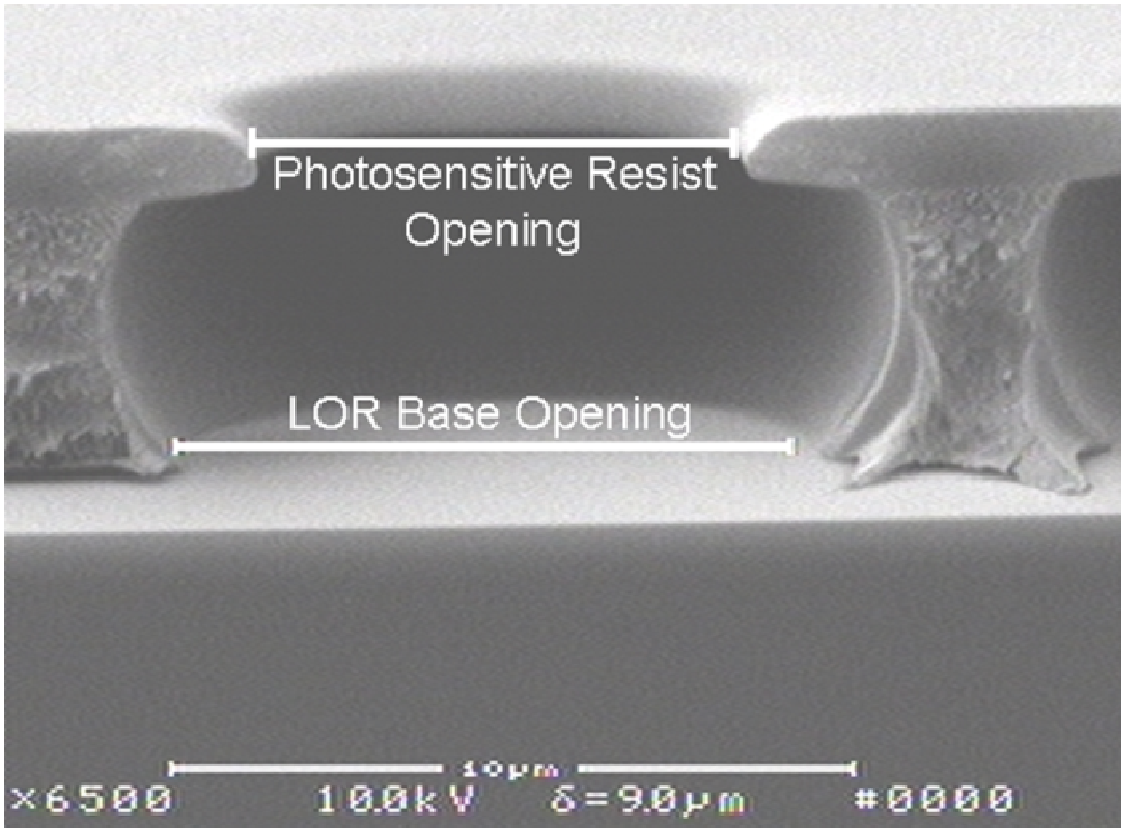
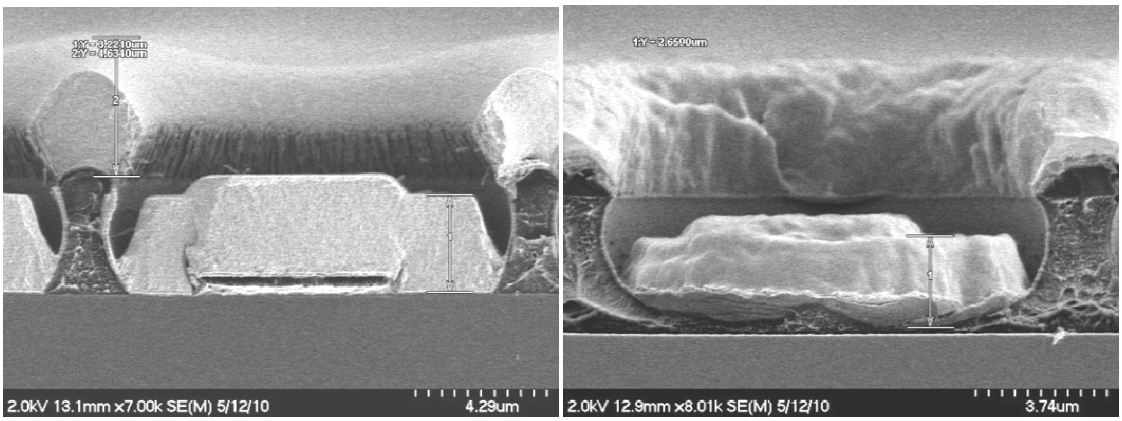


Fig. 6.2 Scanning electron micrograph of bump bond opening in bi-layer resist stack of HPR504 on LOR-30A [26]

The patterned samples were sent to the Jet Process Corporation (JPC)for deposition of the bump bond material. The initial investigation included an evaluation of both indium and gold-tin material systems. The gold-tin alloy provided very low

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resistances, oxidation resistance, and the ability to create a eutectic bond and relatively low temperatures, however the presence of gold near the detector poses a contamination concern. The gold-tin alloy also becomes relatively brittle at cryogenic temperatures, and concerns over low temperature operation and contamination led to the selection of indium and the bump bond material.



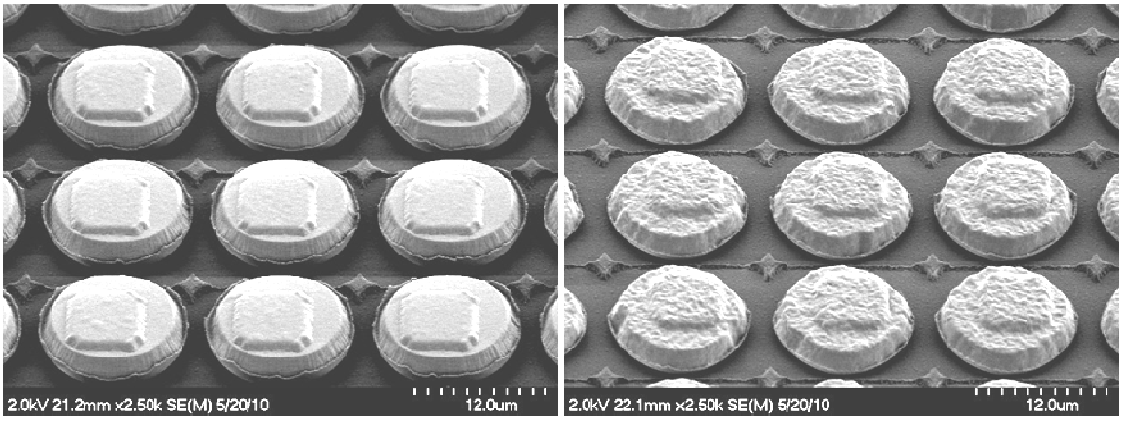
(a) (b)

Fig. 6.3 SEM cross-section of bump-bonds after deposition of **(a)** gold-tin **(b)** indium

After deposition, the samples were cleaved along the patterned regions and prepared for imaging. The cross-section SEMs taken through a bump bond are shown in Fig. 6.3 (a) for the gold-tin alloy and Fig. 6.3 (b) for indium. A discontinuous layer of material about three microns thick is achieved with both materials. The size of the features at about ten microns in width is larger than desired due to overdevelopment. The lack of an overhanging structure from the HPR504 is also readily apparent. The absence of this feature contributes to the larger bump size and allows deposition to occur on the

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foot of the profile. It is believed these structures were lost during either the pre-clean where the wafers are bombarded with Ar ions or during the subsequent deposition.



(a) (b)

Fig. 6.4 SEM of bump-bond array after lift-off (a) gold-tin(b) indium

The lift-off was successfully performed on several samples aided by the use of ultrasonic agitation. The top down SEMs taken of the bump-bond array are shown in Fig. 6.4 (a) for the gold-tin alloy and Fig. 6.4 (b) for indium. A cupping effect was observed on samples that did not receive the ultrasonic agitation. The work provided an excellent point for further development of the process.

6.1.2 Initial Investigation

Several different processes were initially investigated in an attempt to create an undercut profile that would be mechanically robust enough to withstand the deposition process. Lift-off resists have historically been negative resists as the dissolutions rate are reduced with exposure dose and the exponential decay of absorption readily allowed the

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creation of undercut profiles. The resolution limits and need for dangerous solvents as developers phased out their use however the same concept can be applied to positive resists with an image reversal process. The previous process by Kolb, *et al.* was reproduced for comparison, and a bi-layer process with a much thicker top layer was evaluated. SEMs of the resulting resist profiles can be seen in Figure 6.5

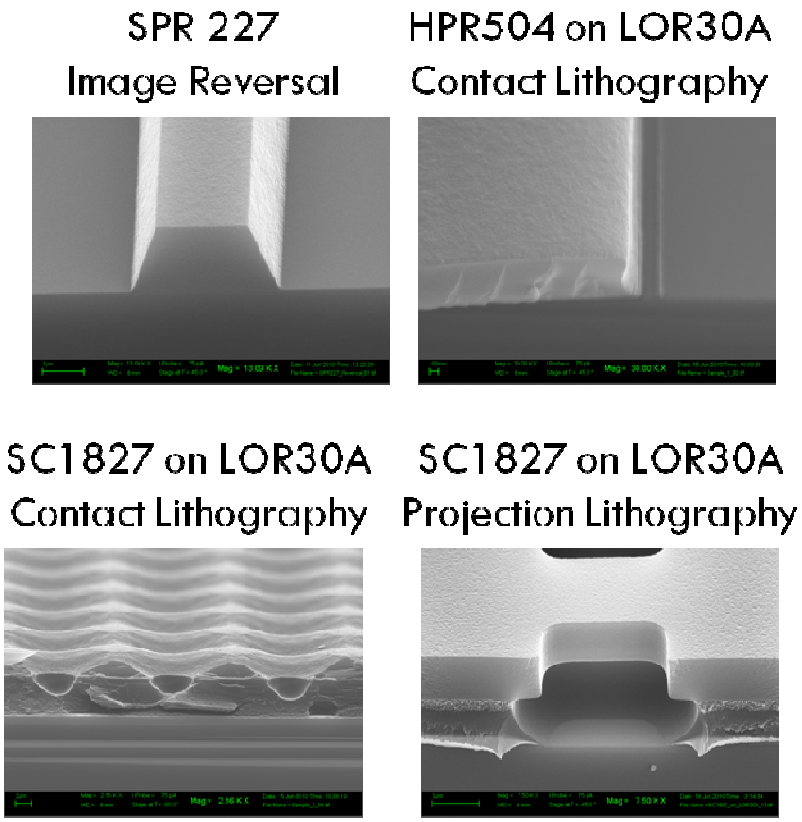


Fig. 6.5 SEM cross-section of resist profile after development for various processes

The image reversal technique involved the use of an ammonia bake and flood exposure process that proved difficult to recreate. The performance of the contact lithography system significantly affected the profile of standard process. The resolution

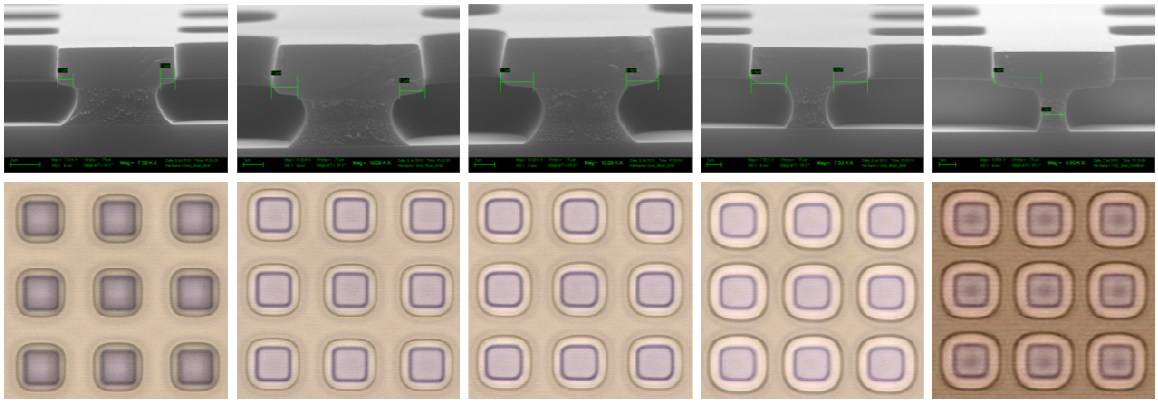
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of the system varied quite dramatically across the wafer, most likely due to variation in the gap between the wafer and reticle. In a new bi-layer process Shipley SC1827 photoresist was used to create a much thicker photoactive layer. This would require a large depth of focus and further drove the need to move to a projection system. The third SEM in Figure 6.5 shows the massive amount of diffraction introduced by the contact system. The profile from the SC1827 on LOR30A process using projection lithography was very promising and displayed all the desired features.

6.1.3 SC 1827 on LOR-30A Development

A simple two factor designed experiment was performed on the lift-off process varying the soft-bake and development time to optimize the resist profile. Several features were identified as key elements evaluated in the profile including the amount of overhang of the top layer beyond the base of the feature, the total undercut and the thickness loss of the top resist layer. The features were evaluated with both optical and scanning electron microscopes. The translucent nature of the materials allowed both layers to be observed with visible light and provided a clear indication of the amount of undercut. The samples were cleaved to allow the SEM to obtain a cross-section of the features. The results for a soft-bake temperature of 190° C at several different development times is shown in Fig. 6.6

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(a) (b) (c) (d) (e)

Fig. 6.6 SEM cross-section and correlating optical micrograph of bump-bond opening in bi-layer resist stack for 190 C soft bake and development times of **(a)** 120 sec **(b)** 135 sec **(c)** 150 sec **(d)** 165 sec and **(e)** 180 sec

A two stage soft bake was utilized based on a manufacturer recommendation with an initial temperature of 160° C and a final soft bake temperature of 190° C for 60 sec each. The temperature was found to not have a significant impact on the profile of the LOR layer. The most important factor affecting the profile of the LOR layer was the method of development. A puddle develop process with manual agitation was first used, however this resulted in an extremely slanted profile. This is most likely due to a transport limited mechanism slowing development at the bottom of the feature. The switch to a continuous spray-develop process created much more vertical profiles. The soft-bake temperature was then chosen at the higher end of the defined range to reduce develop times and chemical consumption. A develop time of 150 sec was chosen as the

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feature in Fig. 6.6 (c) was determined to have enough undercut to allow for process variations while maintaining the mechanical integrity of the overhang.

6.1.4 Indium Deposition

Samples were prepared with the new process of record and again sent to JPC for indium deposition. The samples were prepared for deposition in the same manner as the pervious samples. An argon ion pre-clean was followed by 100 nm of chrome and 1000 nm of gold. Three microns of indium was then deposited on the samples. Some samples were imaged as-deposited while other underwent the lift-off process with ultrasonic agitation before imaging. A SEM of the as deposited sample is shown in Fig. 6.7.

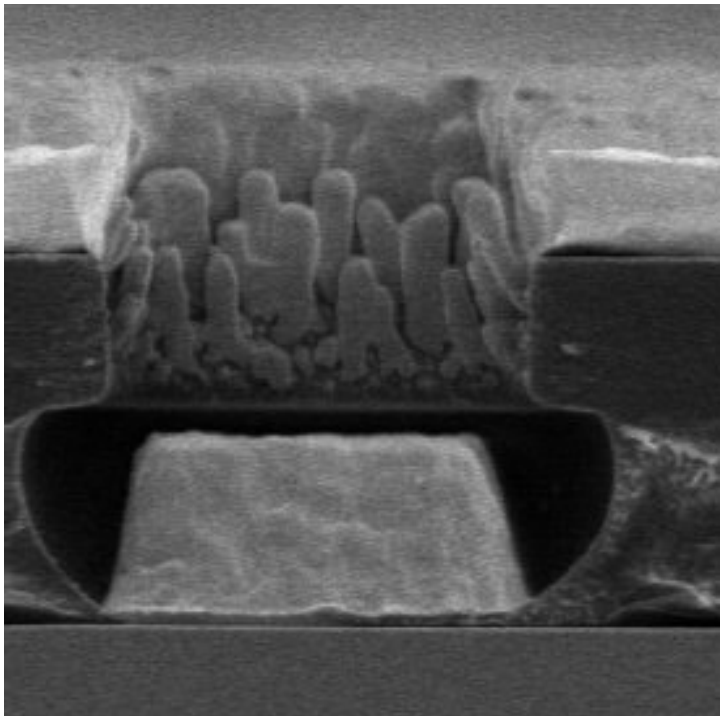


Fig. 6.7 SEM of new thick bi-layer LOR process after deposition of 3 μm of indium

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The results were exactly as desired, where a discontinuous indium layer was formed with a bump of the desired size and height. The slight angle to the resist profile caused deposition to occur on this surface creating stalagmite type features. This resulted in a shadowing effect during deposition giving the indium bump a slight taper. The unintended side effect is that it prevents the layers from connecting. This could also allow bumps of even greater heights to be created. The taper also helps to prevent shorting between adjacent bumps as they expand during compression.

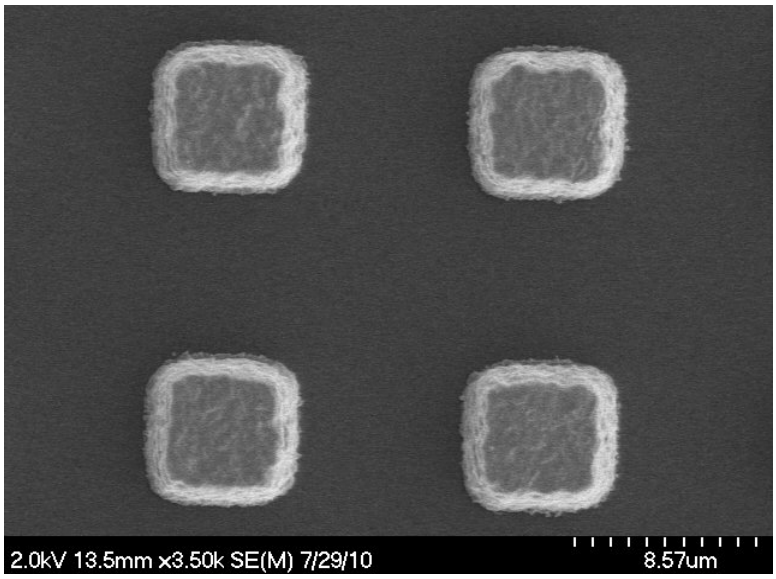


Fig. 6.8 SEM of several 3 μm tall indium bumps after lift-off of excess material

A top-down SEM of several indium bumps indium bumps is shown in Fig. 6.8. The bumps are six microns wide at the base narrowing to a width of about 4 microns at the top on 15 micron pitch. Although the samples appeared slightly under-developed due

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to the foot of the LOR profile extending all the way to the base of the bump, there were no adhesion issues observed during lift-off.

6.1.5 SC 1827 on Double-Coat LOR-30A

During the course of the project the need for a much thicker (~ 5 μm) indium layer on the detector side of the device arose. The driving factor for this need is discussed at length in Section 6.2. The obvious course of action was to increase the thickness of the sacrificial LOR layer in the bi-layer process. The spin coating was already being performed at the lowest recommended speed, so a second layer had to be applied. The second coating was applied at a much higher speed to achieve the best uniformity. Any irregularities in the initial coating are exaggerated by the second coating.

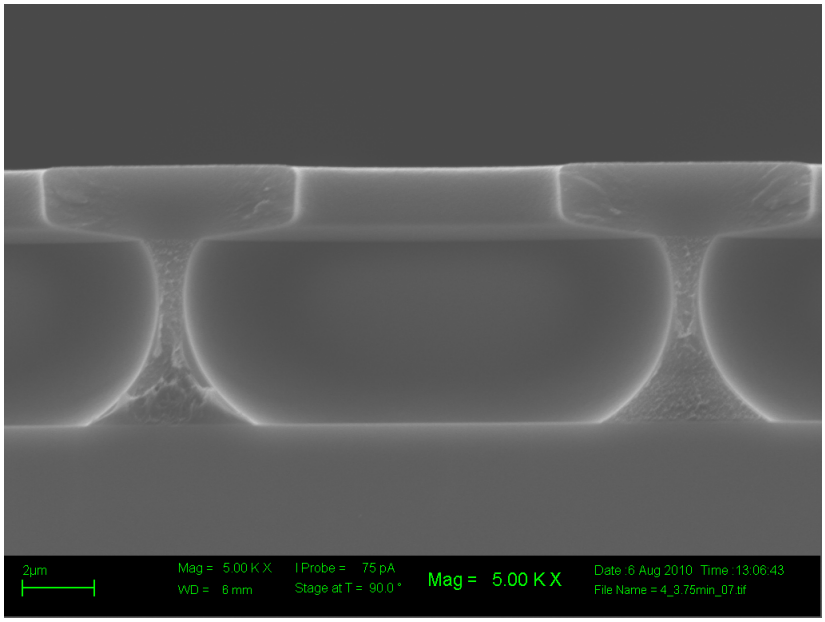


Fig. 6.9 SEM of bi-layer resist process with two LOR layers

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The standard two stage soft-bake process was performed after each layer was applied. The thicker sacrificial layer required the develop time be increased to 210 sec. The resulting profile shown in Fig. 6.9 has a 5.8 μm thick LOR layer with a sufficient overhang. It can be noted that the density of the features and the profile of the LOR layer impose a limit on the maximum allowable thickness of this layer. The neck of the feature must remain to prevent the resist layer from collapsing.

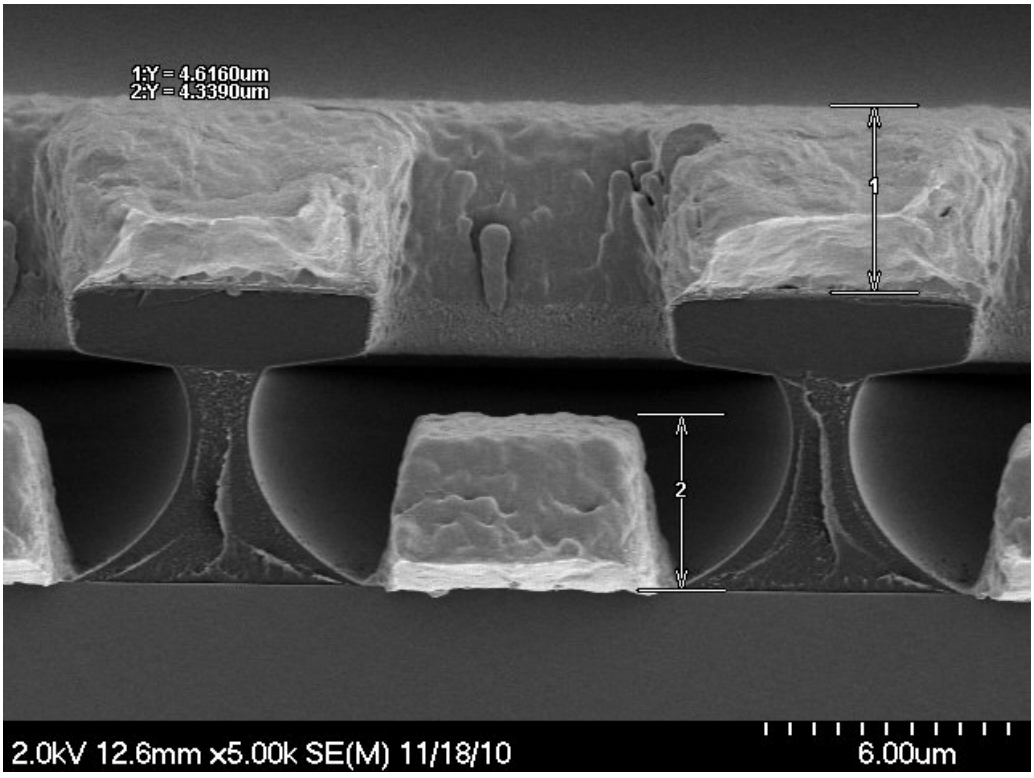


Fig. 6.10 SEM of thick bi-layer resist process after 4.6 μm of indium deposition

The samples prepared with the double LOR coat process were sent to JPC where 4.6 μm of indium was deposited. A cross-section SEM of the sample is shown in Fig. 6.10 through the bump bond array. The taller bump is clearly discontinuous from the

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rest of the film by several microns, a promising result. Although the resist sidewall is angled slightly outward in this sample, the feature opening still shrinks slightly as deposition proceeds. This results in a similar tapered profile to the bump, although at a steeper angle than before.

6.2. ROIC Passivation Cut

The read-out integrated circuits (ROIC) for the project were fabricated through the MOSIS service at TSMC using the 4-poly 2-metal process. Due to an oversight in the design, the ROICs were defined with passivation openings on the wire-bond pads, but not the bump bond pads. Since lithography already needed to be performed on the ROIC chips for bump bond metal deposition, a plasma etch was used to open the passivation layer above the bump bond pads before deposition. The locations that needed to be etched were the same as those needing the bump bond metal, so only a single photo-mask was required.

There were many challenges involved with transferring a pattern to a small irregularly shaped substrate. The small size made aligning a pattern to the die difficult and allows only a single point of observation. The irregular shape creates turbulence when spinning the substrate creating large edge beads in viscous coatings. To overcome these challenges several custom vacuum chucks were fabricated. The first was milled out

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of plastic with a recessed pocket designed to fit the ROIC die and a vacuum hold to be used for spin coating. The recessed pocket moved the turbulent air away from the edge of the die and significantly reduced the size of the edge beads. The second chuck was designed for the contact lithography tool in tandem with the photo-mask. Two recessed pockets were placed underneath each of the alignment microscopes to allow both to be utilized. A mask was designed with an array of 84x84 openings each 7 microns large at those same locations.

Although no specific details were given as to the thickness of composition of the passivation layer, it was stated to be an oxide, nitride, or oxynitride that was between 0.5 and 2 microns thick. The thickness was confirmed to be very nearly one micron through a profilometer measurement made at the wire-bond pad opening. The composition of the layer was investigated using both ellipsometry and energy dispersive x-ray spectroscopy and was determined to be an oxynitride. This was confirmed by attempting to etch a sample in hydrofluoric acid, which had no effect. A dry etch process was developed in a plasma etch system with fluorine based chemistry. A very low power was used to minimize the amount of resist degradation that occurred during the etch. A thick resist could not be used to due to the size of the edge beads when attempting to spin coat the sample.

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The samples were spin coated with HPR 504 at 8000 RPM for 45 sec and soft baked at 125 °C for 60 sec. They were aligned and exposed on the contact lithography tool with a dose of 160 mJ/cm^2. After a 300 sec etch in CF_4 at 10 mTorr the samples were imaged and one was cleaved and prepared for the SEM. An optical micrograph can showing etched bond pads adjacent to dummy bond pads that were not etched can be seen in Fig. 6.11

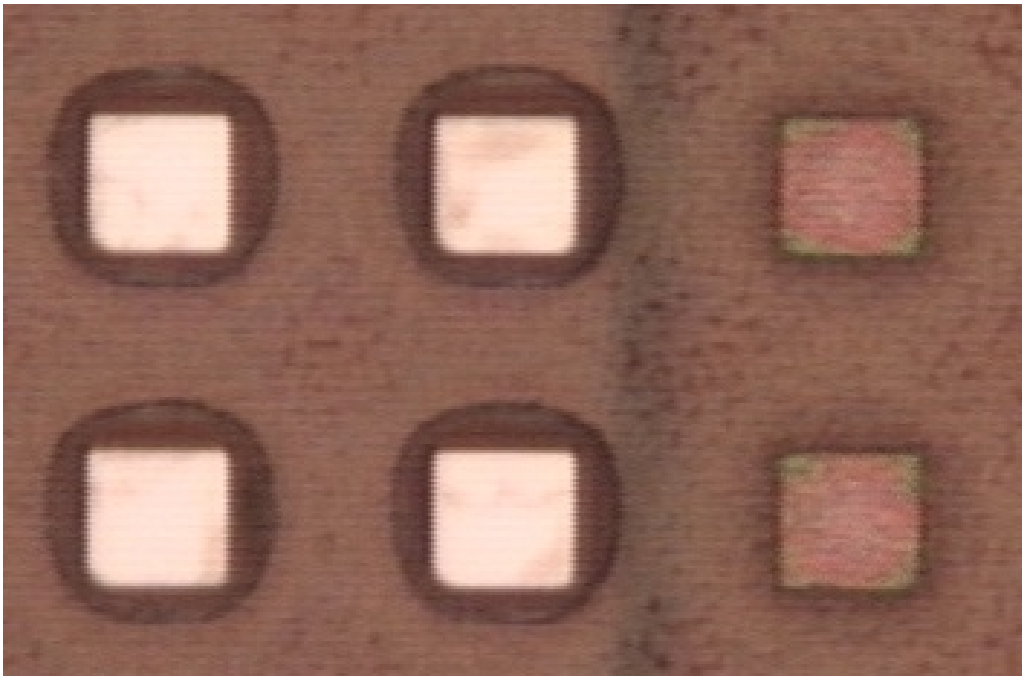


Fig. 6.11 Optical micrograph of etched and un-etched bump bond pads

The surface of the resist became very rough after the etch process, and although a significant thickness loss was not observed the size of the opening was much larger than designed. It was believed several process biases contributed to the enlargement of the feature. The presence of edge beads reduced the focus of the lithography process and the

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resulting diffraction enlarged the features slightly. During the plasma etch process the edges of the bond pads magnified the electric fields increasing the etch rates and further bloating the features size. An SEM cross-section though an etched bond pad is shown in Fig. 6.12. The features were sent out for indium deposition and although pictures are unavailable lift-off was successfully performed.

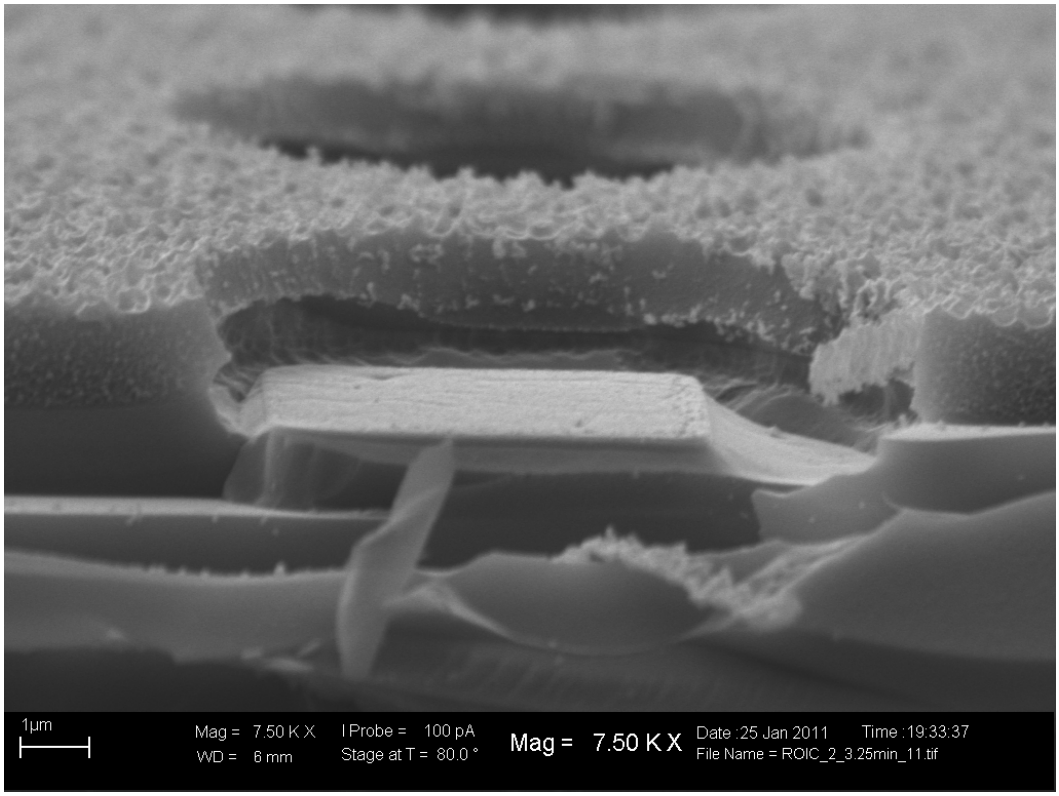


Fig. 6.12 SEM cross-section of ROIC die through etched bond pad

6.3. Bump-Bond Daisy Chain Test Parts

Test parts were created to evaluate the hybridization process and characterize the mechanical and electrical strength of the bonds. The electrical characteristics of the bump bonds were determined by connecting every other bump in the array and shifting

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the pattern by one bump on the opposing array in a ‘daisy-chain’ fashion. At the top and bottom of the array on the fake ROIC die connections are made to each column and connected together in a serpentine fashion. The connections also fan out to arrays of larger pads to be used for manual probing. On the left and right side of the array connections are made to individual bumps allowing any two bumps on the edges to be measured. A screen capture of the bump-bond daisy chain ROIC test part VLSI layout is shown in Fig. 6.13.

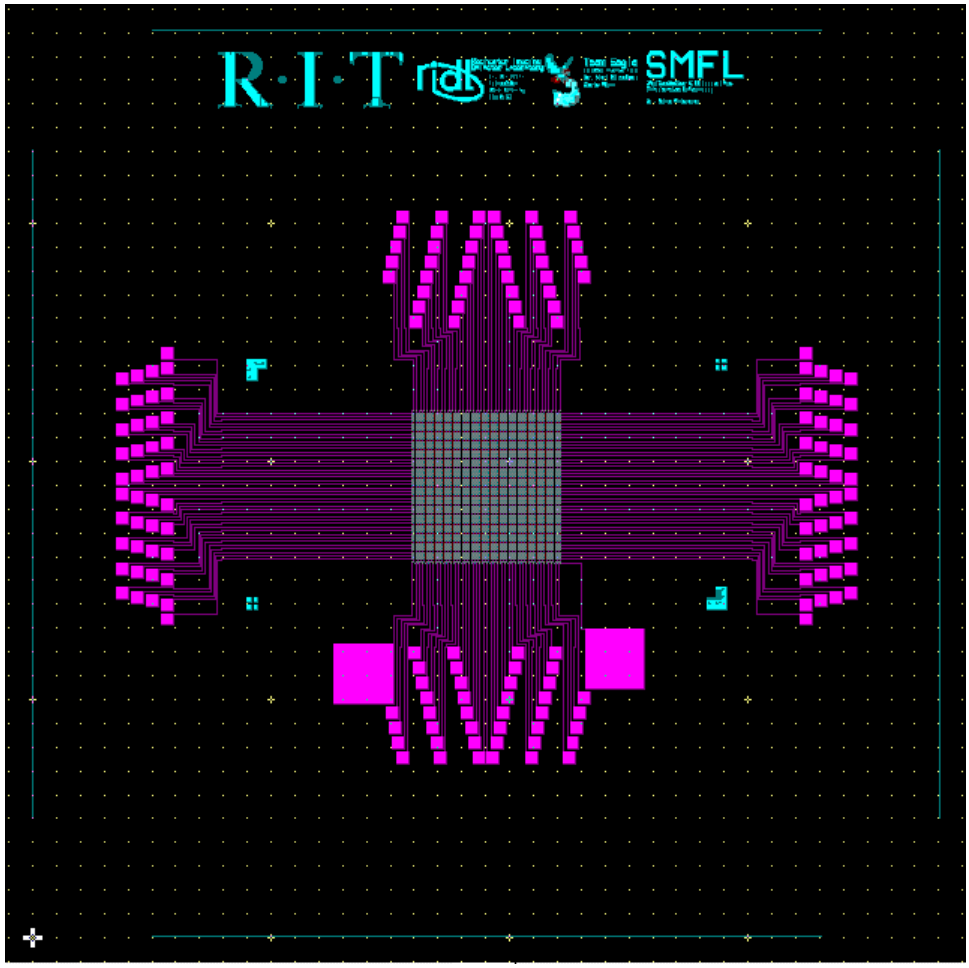


Fig. 6.13 Screen capture of bump-bond daisy chain ROIC test part VLSI layout

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A thermal oxide was grown first to electrically insulate the devices from the silicon substrates. An aluminum layer was deposited and patterned with the bump bond and probe connection layer. The test parts were coated with the same passivation layer from the diode fabrication process and patterned with the same contact cut opening design. The samples were wet etched in a pad etch solution and the resist stripped in a heated solvent bath. The ROIC test part wafer received the standard LOR process with a single coating of the LOR layer while the diode test part wafer received the thicker process with the two coatings of the LOR layer. The wafers were sent to JPC and the diode and ROIC parts were deposited with five and one microns of indium respectively. The intention was to mimic the real parts as closely as possible while still ensuring the greatest chance of success.

6.3.1 Physical Testing

The parts were sent to STC where the indium lift-off was performed with the ultra-sonic agitation. A protective coating was applied, the wafers were diced and individual samples were removed and prepared for bonding. A hydrogen peroxide etch was utilized directly before bonding to remove the native oxide. The parts were aligned and bonded in the Karl Seuss FC-150 using only applied pressure. Bonded parts were

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observed with infra-red imaging and a few samples were separated and imaged with an SEM. Electrical measurements were also made of bonded test parts.

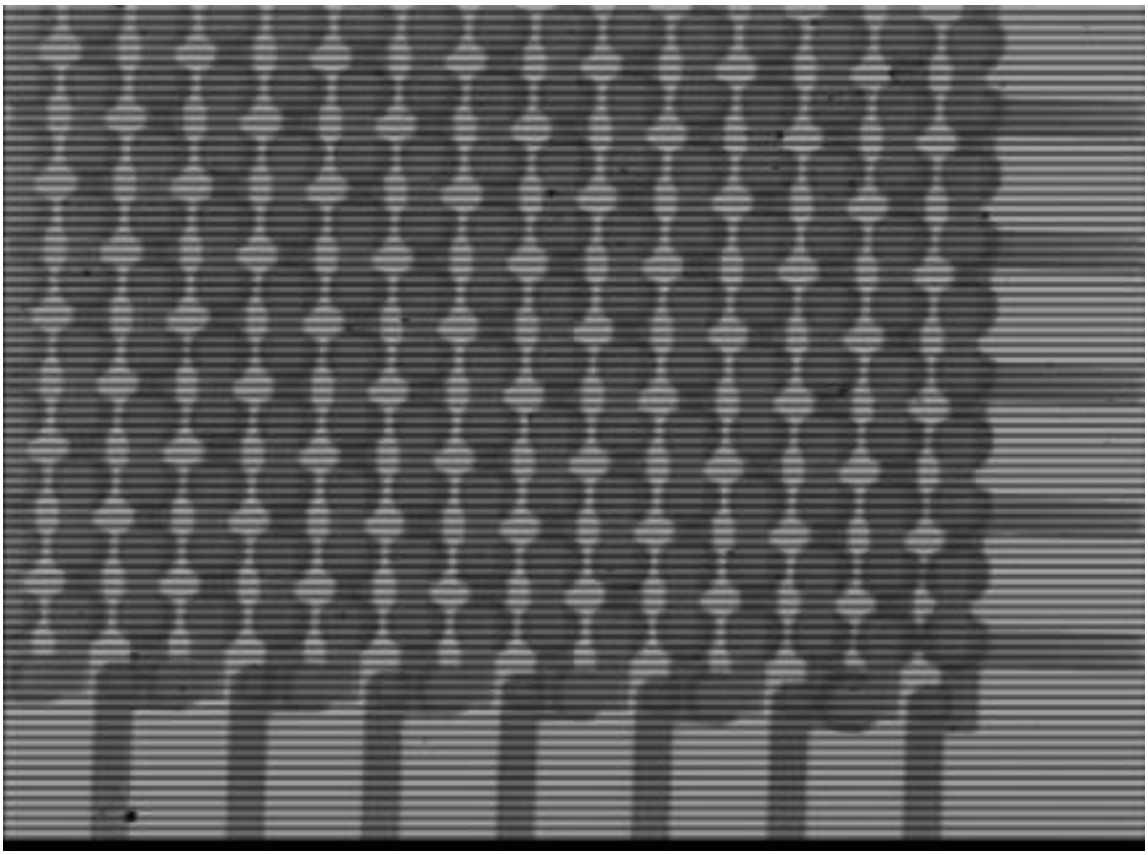


Fig. 6.14 Infra-red optical micrograph of the corner of the bump bond array

The infra-red image of the bump bonds in Fig. 6.14 shows good alignment of the parts and the connections between bumps and to probe pads. Some expansion of the bumps is visible due to the compression when forming the bond. No shorting of adjacent bumps is observed throughout the entire array. This indicates a good mechanical bond was formed between the bumps on the two die.

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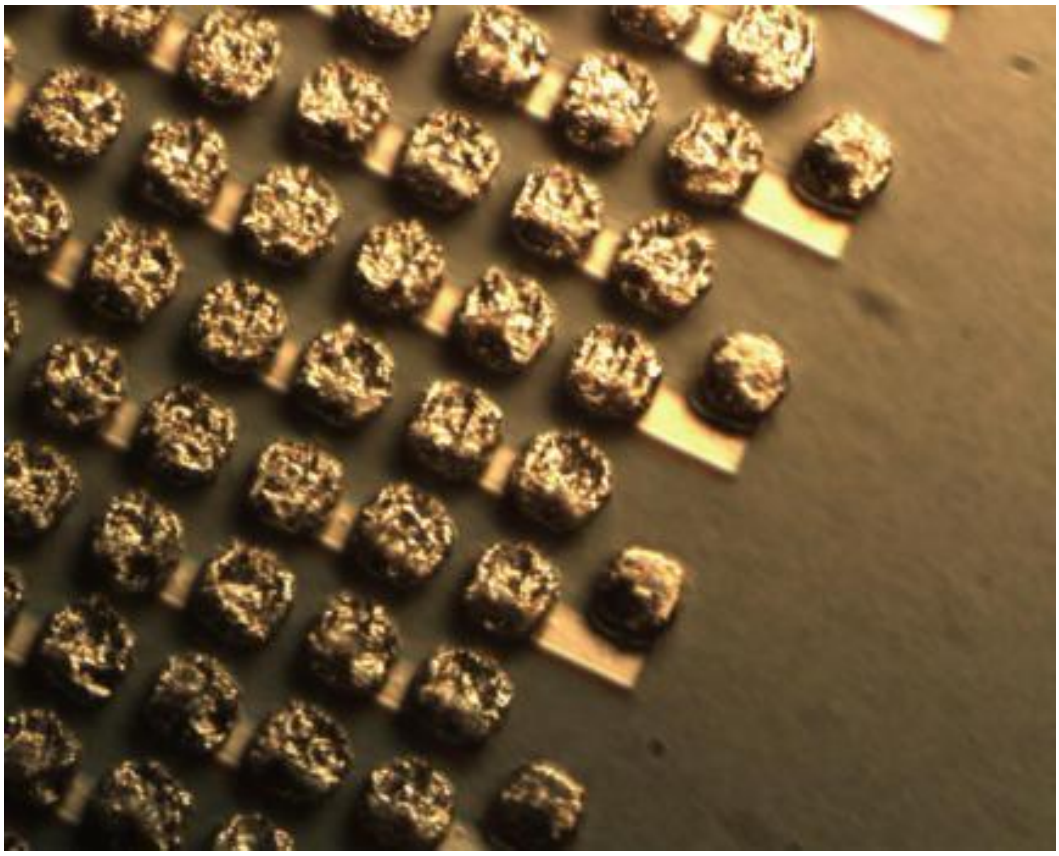


Fig. 6.15 Optical micrograph of 5 μm thick indium bumps after bonding and separation

An optical micrograph of the thicker five micron indium bumps after bonding and separation is shown in Fig. 6.15. A clear depression can be seen in the top of the features as the thicker indium bumps deformed significantly more than the thinner counterparts on the ROIC test die. An SEM image of one of the thinner bumps after bonding and separation is shown in Fig. 6.16.

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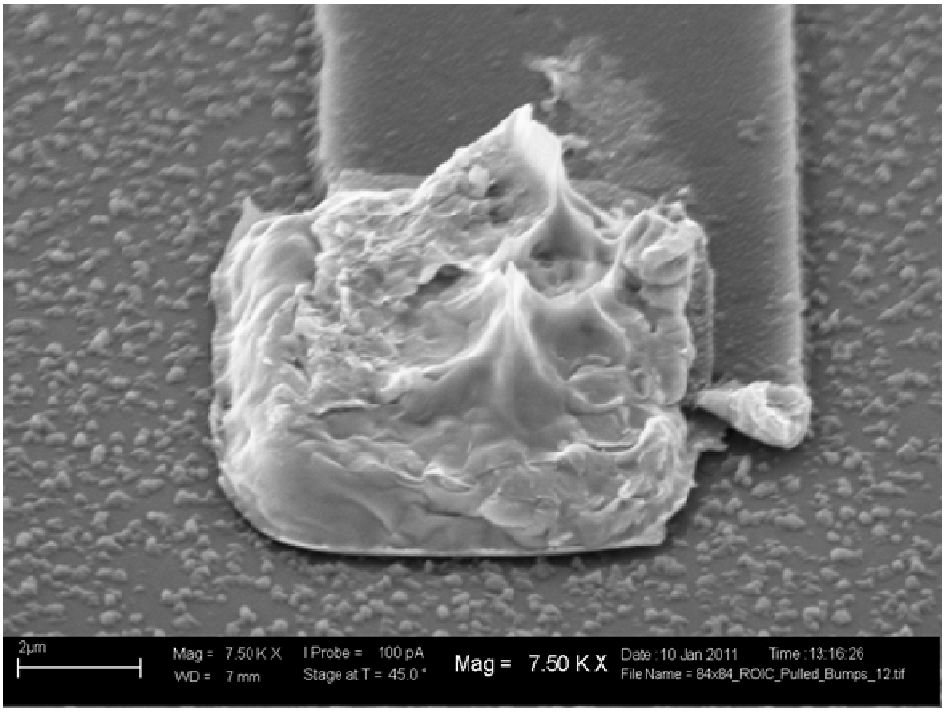


Fig. 6.16 SEM of 1 µm indium bump after bonding and separation

In Fig. 6.16 the indium bump is seen on the aluminum contact pad with pointed features rising out of it. These features are the classic result of the necking and eventual fracture of a piece of metal. The presence of these features indicates a good mechanical bond was formed between the two indium bumps.

6.3.2 Electrical Testing

The resistance of each of the 84 columns in the active array was measured to be about 20 MΩ as shown in Fig. 6.17. The actual resistances of each column varied slightly but all measurements were many orders of magnitude higher than expected. The results were similar for several tests parts and even when measuring smaller numbers of bumps using the side contacts.

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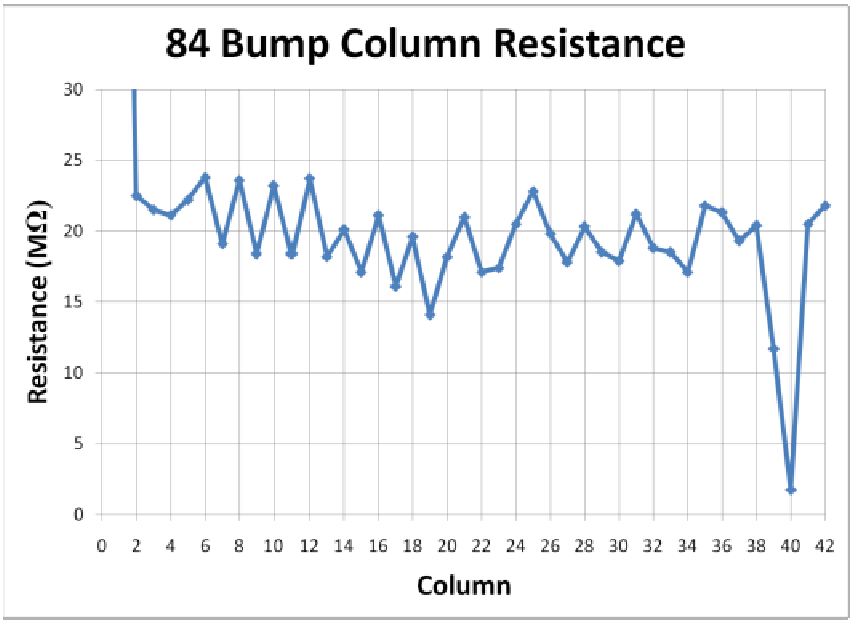


Fig. 6.17 Measured resistance of columns of 84 bump bonds

It was observed however than after the application of a small current through the bumps the current was dramatically reduced. For a pair of bumps the initial resistance of about 200 kΩ could be reduced to about 200 Ω. A current of at least 50 mA was needed to achieve the maximum reduction in resistance. This indicated a contact oxide was present that would breakdown after application of a current. Unfortunately this same type of contact healing through current drive is not available on the experimental devices. This is a major concern for the functionality of the device and an area that requires further development.

6.4. Final Hybridized Devices

Two fully processed *p-i-n* diode wafers patterned with the double layer LOR process were sent to JPC along with five patterned and etched ROIC die. The samples

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received five and one micron of indium deposition respectively, and were sent to STC for lift-off and bonding. The two diode wafers sent were the lowest measuring leakage currents from the final two processing runs for which the data was presented in Chapter 5. Unfortunately the wafer from the final run representing the best results to date was determined to be mis-aligned between the front and back.

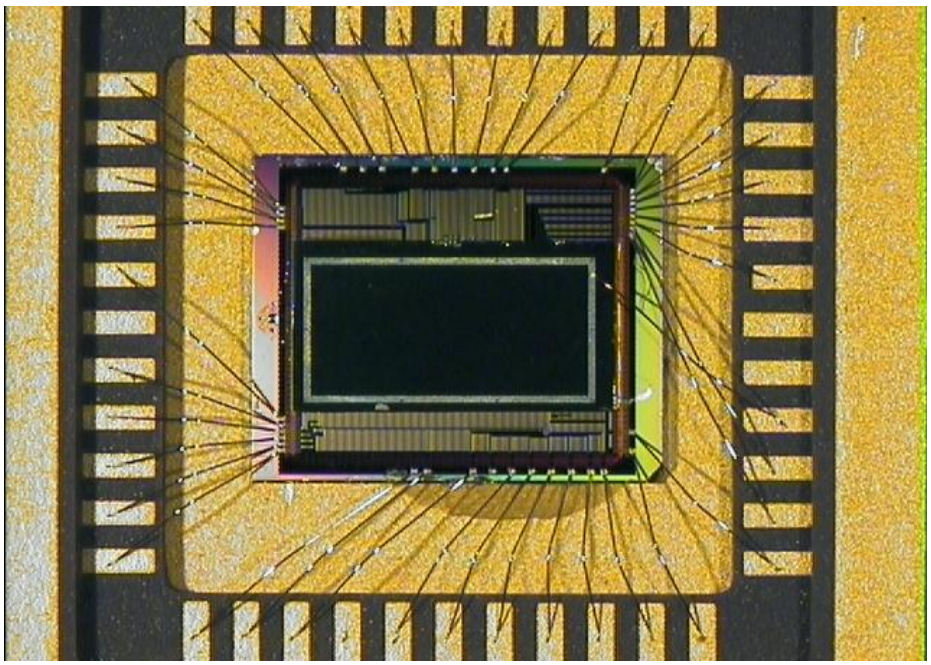


Fig. 6.18 Image of a hybrid *p-i-n* CMOS imaging system wire-bonded in DIP

The lift-off was successfully performed on four of the five etched ROIC die and they were bonded to diode arrays. The bonded die were then affixed to a dual in-line package (DIP) and wire-bonded. An image of the hybrid p-i-n CMOS imaging system ready for testing is shown in Fig. 6.18. Testing is currently ongoing at the Center for Detectors laboratory at RIT.

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Chapter 7

Final Remarks

In conclusion the project has been deemed largely successful, although there are still many areas that can be improved upon. The leakage measurement results achieving within an order of magnitude of the stated goals are a testament to the quality of devices that can be produced using the manufacturing processes offered at the SMFL. Despite the fact that an imaging system was produced at the completion of the project there were many stumbling blocks and unforeseen issues along the way that could provide beneficial learning opportunities for future projects.

Some of the lessons learned relating to the design of the diode include operating at higher over-depleted biases, incorporating a back side guard ring, and further optimization of passivation and anti-reflection coatings. The simulations performed for project showed in agreement with literature that over-depleted biasing conditions are critical for minimizing pixel cross talk in thick detectors. The incorporation of a guard ring structure on the backside of the devices would help to prevent the depletion region from reaching the edge of diced imagers mitigating surface leakages. The design of the ARC layer could also be further optimized using a nitride passivation layer to further reduce reflections across a broader range of wavelengths.

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The hybridization process was quite successful for a prototype device with bonded imagers being produced. The measured bump bond contact resistances were extremely large prohibiting device operation. A further analysis of the deposition pre-clean process is required to investigate possible interfacial layers. The use of under bump metallization layers electrochemically applied has also been shown to be a successful process alternative.

The oversight in ensuring opening in the passivation layer of the ROIC proved to be one of the most difficult challenges of the entire project to overcome. The development a process to pattern an etch individual die was critical to enabling the success of the project. The lesson from this challenge is the constant attention to detail required at every aspect of the project.

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Appendix I Typical Atlas Input File

```
######################################################################
#### Rocheseter Image Detector Laboratory & Team Strongarm
#### APRA Diode
#### Atlas Simulations
#### Reverse Bias Characteristics & Spectral Response
#### revision 5.9
#### 5 Pixel Structure: Wavelength Varied
#### Chris Shea
#### Friday, April 16, 2010
#### cgs4706@rit.edu
######################################################################
go atlas
#
setTh=250
set W=75
setVb=50
set T=300
set L=0.1
set Tau0=1e-3
set Ns=1e20
setXj=0.5
set rev=5.9
#
# SECTION 1: Mesh Specification
#
meshspace.mult=2.0
#
x.meshloc=-$W/2  spacing=0.25
x.meshloc=$W/2   spacing=0.25
#
y.meshloc=0.0     spacing=0.025
y.meshloc=1.0     spacing=0.05
y.meshloc=10.0    spacing=1.0
y.meshloc=20.0    spacing=2.5
y.meshloc=$Th-10  spacing=2.5
y.meshloc=$Th-2   spacing=0.05
y.meshloc=$Th     spacing=0.05
#
# SECTION 2: Structure Specification
#
regionnum=1 x.min=-$W/2 x.max=$W/2 y.min=0 y.max=$Th material=Silicon
#
elecnum=1 name=cathode top
elecnum=2 name=anode  x.min=-3.5  x.max=3.5   y.min=$Thy.max=$Th
elecnum=3 name=nwellx.min=-18.5 x.max=-11.5 y.min=$Thy.max=$Th
elecnum=4 name=pwellx.min=11.5  x.max=18.5  y.min=$Thy.max=$Th
elecnum=5 name=ndrainx.min=-33.5 x.max=-26.5 y.min=$Thy.max=$Th
elecnum=6 name=pdrainx.min=26.5  x.max=33.5  y.min=$Thy.max=$Th
#
#
doping uniform conc=1e12 n.type
dopinggaus peak=0.0 junction=$Xjconc=$Ns n.typedir=y
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=-3.5 x.max=3.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=-18.5 x.max=-11.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=11.5 x.max=18.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=-33.5 x.max=-26.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=26.5 x.max=33.5
regrid region=1 doping ratio=1.25 logarithm max.level=1 smooth.k=4
#
```


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```
# SECTION 3: Material Model Specification
#
material taup0=$Tau0 taun0=$Tau0
models temperature=$T srh auger cvtfermibgn
interface optical ar.index=1.45 ar.thick=0.1030 p1.x=0.0 p1.y=0.0 p2.x=0.0 p2.y=0.0
method newton trap clim.dd=1e-5
#
# SECTION 4: Optical source specification
#
beamnum=1     rays=150     x.origin=0     y.origin=-1.0     angle=90.0     wavelength=$L
front.reflambient.index=1.0
beamnum=2   x.origin=0   xmin=-0.25   xmax=0.25   y.origin=-1.0   angle=90.0   wavelength=$L
front.reflambient.index=1.0

#
# SECTION 5: Initial Solution & Reverse Bias IV
#
solveinitoutf=APRA_rev$'rev'_L$'L'_Tau$'Tau0'_T$'T'_W$'W'_init.str master
tonyplot
#
log outfile=APRA_IV_rev$'rev'_L$'L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log
probe name="Recombination rate" integrated srhx.min=0 x.max=15 y.min=0 y.max=250
solveprevvcathode=0.5 vstep=0.5 vfinal=$Vb/5 name=cathode
tonyplot
solveprevvcathode=$Vb/5 vstep=0.5 vfinal=$Vb name=cathode
log off
tonyplot    APRA_IV_rev$'rev'_L$'L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log
structoutf=APRA_rev$'rev'_L$'L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.str
tonyplot    APRA_rev$'rev'_L$'L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.str
measureu.total
#
# SECTION 6: Spectral Response
#
log outf=APRA_Spectral_rev$'rev'_Ns$'Ns'_Xj$'Xj'_Tau$'Tau0'_T$'T'_V$'Vb'.log master
solveprev b1=1 beam=1 lambda=0.1 wstep=0.01 wfinal=1.3
log off
tonyplot     APRA_Spectral_rev$'rev'_Ns$'Ns'_Xj$'Xj'_Tau$'Tau0'_T$'T'_V$'Vb'.log     -set
APRA_Spectral.set
quit

#
# SECTION 7: Spatial Response
#
log outf=APRA_Spatial_rev$'rev'_L$'L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log master
solveprev b1=1 scan.spot=1
log off
tonyplot APRA_Spatial_rev$'rev'_L$'L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log
quit
```


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Appendix II Process Flow

TABLE I. KEY FOR PROPOSED PROCESS FLOW

Thermal	Lithography	Wet Chemistry	Plasma Deposition & Etch	Implant	Measure

TABLE II. PROPOSED PROCESS FLOW

#	Step	Process Parameters	Process Details and Comments	Record	Wafers
1	Create Lot Notebook	Obtain a Cleanroom notebook, a previous notebook can be used Update and insert the file located in: \\kgcoe-file\morbo-eagle\RIDL	Tape into the notebook: •Process Flow (this document) •Important Lot Processing Information Sheet •Implant settings		All Device Wafers
2	Scribe	**Tool**: Diamond Tips Scribe Print out wafer box label and tape it on 4" polypropylene box	The bulk wafer can be found in XXXXXXXX box 5000 ohm-cm		All Device Wafers
3	Grow Oxide	**Tool**: Bruce Furnace **Tube:** 4 **Recipe:** ??? "1000 Å Oxide"	Do **Not** use dummy wafers	**Print Thermal History** **Include Profiles, N2, & O2**	All Device Wafers
4	Oxide Thickness Measurement	**Tool:**PrometrixSpectramap **Recipe**: ?	**Save**Spectramap data to disk and **copy** to Morbo	**M1** **C2** **Mean:** _____ _____ **Å** **Std. Dev:** _____ _____ **Å** **Min:** _____ _____ **Å** **Max:** _____ _____ **Å**	All Device Wafers
5	Coat BBS	**Tool:** CEE 100 Resist Spinner **Recipe:** 9 & 0 Do **Not** use SVG Track (backside resist splattering)	**Dehydration Bake:** 60 sec @ 150 ℃ **Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
6	Coat LAS	**Tool:** CEE 100 Resist Spinner **Recipe:** 9 & 0 Do **Not** use SVG Track (backside resist splattering)	**Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
7	LAS Litho Level I: Alignment	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** I **Mask:** Alignment	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
8	BBS Litho Level I: Alignment	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** I **Mask:** Alignment	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
9	Develop BBS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
10	Develop LAS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
11	Oxide Etch	**Tool:** Manual Wet Bench **Bath:** MOS Grade 5.2:1 HF:H20	**Thermal Oxide Etch Rate:** ~ 1200 Å/min **Time:** 1 min		
12	Silicon Etch	**Tool:** Drytek Quad **Recipe:** ???? **Chamber #1 -**Al Carrier **Power:** 50 W **Pressure:** 100 mT **SF_6:** 50 sccm **Chiller temperature:** 38℃ **Time:** 0:20 m:s	Make sure **chiller** temperature has been set to **38℃** Run a **clean&season** with Al **carrier wafer** Etch both sides of all wafers		
13	Resist Strip	**Tool**: Wet Bench **Solvent:** PRS2000 **Temp:** 90℃ **Time:** 10 min (each bath)			
14	Implant LAS Side	**Tool**: Varian 350D **Dose:2e15 cm^{-3}** **Energy:75 keV** **Species:** P_{31}	Target Peak Depth: 1074 Å		All Device Wafers

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15	Coat BBS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Dehydration Bake:** 60 sec @ 150 ℃ **Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Bake:** 60 sec @ 150 ℃ **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
16	BBS Litho Level II: P-Well	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** II **Mask:** P-Well	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
17	Develop BBS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
18	Implant LAS Side	**Tool**: Varian 350D **Dose:4e15 cm^{-3}** **Energy: 35 keV** **Species:** B_{11}	Target Peak Depth: 1455 Å		All Device Wafers
19	Resist Strip	**Tool**: Branson Asher **Recipe:** 4" Hard Ash			
20	APM Clean	**Tool:** Manual Processing Bench# 2 **SCA1:** 1:3:15 :: $NH_4OH:H_2O_2:H_2O$ **NH_4OH:** 300mL **H_2O_2:** 900mL **H_2O:** 4500mL **Time:** 10 min **Temp:** 75 ℃	Spike with **100 mL** of **H_20_2** if old	**Fill out log Sheet for chemicals added or changed.**	All Device Wafers
21	HPM Clean	**Tool:** Manual Processing Bench# 2 **SCA1:** 1:3:15 :: $HCl:H_2O_2:H_2O$ **HCL:** 300mL **H_2O_2:** 900mL **H_2O:** 4500mL **Time:** 10 min **Temp:** 75 ℃	Spike with **100 mL** of **H_20_2** if old		All Device Wafers
22	BBS Oxide Dep	**Tool**: AMat P5000 **Thickness:** 4000 Å of TEOS **Chamber:** A **Recipe**: A6-4000A TEOS LS	Deposit on the **Bump Bond Side** of the wafer Use TEOS Si Carrier wafer		All Device Wafers
23	Oxide Thickness Measurement	**Tool:**PrometrixSpectramap **Recipe**: ?	**Save**Spectramap data to disk and **copy** to Morbo	**M1** **C2** **Mean:** _____ _____ **Å** **Std. Dev:** _____ _____ **Å** **Min:** _____ _____ **Å** **Max:** _____ _____ **Å**	All Device Wafers
24	Anneal	**Tool**: Bruce Furnace **Tube:** 4 **Recipe #:** 444 "Shea RIDL Anneal"	Do **Not** use dummy wafers	**Print Thermal History** **Include Profiles, N2, & O2**	All Device Wafers
25	Oxide Thickness Measurement	**Tool:**PrometrixSpectramap **Recipe**: ?	**Save**Spectramap data to disk and **copy** to Morbo	**M1** **C2** **Mean:** _____ _____ **Å** **Std. Dev:** _____ _____ **Å** **Min:** _____ _____ **Å** **Max:** _____ _____ **Å**	All Device Wafers
26	Coat BBS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Dehydration Bake:** 60 sec @ 150 ℃ **Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Bake:** 60 sec @ 150 ℃ **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
27	Coat LAS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
28	LAS Litho Level III: Contact	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** III **Mask:** Contact	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
29	Develop LAS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
30	Oxide Etch	**Tool:** Manual Wet Bench **Bath:** MOS Grade 5.2:1 HF:H20	**Thermal Oxide Etch Rate:** ~ 1200 Å/min Annealed TEOS Etch Rate: ~ 2029 Å/min **Time:** 3:30 min		
31	Resist Strip	**Tool**: Wet Bench **Solvent:** PRS2000 **Temp:** 90℃ **Time:** 10 min (each bath)			

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32	Metal Deposition	**Tool**: CVC601 **Target:** #2 Aluminum	**Power:** 2000W **Ar Flow:** 20 sccms Argon **Pressure:** 5.0 mTorr **Presputter:** 300 seconds **Dep. Time:** 1000 sec	Record Base Pressure and Pump-down time.	All Device Wafers
33	Coat BBS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Dehydration Bake:** 60 sec @ 150 ℃ **Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Bake:** 60 sec @ 150 ℃ **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
34	BBS Litho Level III: Contact	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** III **Mask:** Contact	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
35	Develop BBS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ **150 C**		All Device Wafers
36	Oxide Etch	**Tool:** Manual Wet Bench **Bath:** MOS Grade 5.2:1 HF:H20	**Thermal Oxide Etch Rate:** ~ 1200 Å/min Annealed TEOS Etch Rate: ~ 2029 Å/min **Time:** 3:30 min		
37	Resist Strip	**Tool**: Wet Bench **Solvent:** PRS2000 **Temp:** 90℃ **Time:** 10 min (each bath)			
38	Metal Deposition	**Tool**: CVC601 **Target:** #2 Aluminum	**Power:** 2000W **Ar Flow:** 20 sccms Argon **Pressure:** 5.0 mTorr **Presputter:** 300 seconds **Dep. Time:** 1000 sec	Record Base Pressure and Pump-down time.	All Device Wafers
39	Coat BBS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Dehydration Bake:** 60 sec @ 150 ℃ **Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Bake:** 60 sec @ 150 ℃ **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
40	Coat LAS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
41	LAS Litho Level IV: Metal	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** IV **Mask:** Metal	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
42	BBS Litho Level IV: Metal	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** IV **Mask:** Metal	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
43	Develop BBS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
44	Develop LAS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
45	Aluminum Etch	**Tool:** LAM 4600 **Recipe:** ????	**Power:** ?? W **Pressure:** ???mT **Gas1:** ?? sccm **Time:** 0:?? m:s		
46	Aluminum Etch	**Tool:** LAM 4600 **Recipe:** ????	**Power:** ?? W **Pressure:** ???mT **Gas1:** ?? sccm **Time:** 0:?? m:s		
47	Resist Strip	**Tool**: Wet or Ash???			
48	BBS Oxide Dep	**Tool**: AMat P5000 **Thickness:** 4000 Å of TEOS **Chamber:** A **Recipe**: A6-4000A TEOS LS	Coat the **Bump Bond Side** of the wafer Use TEOS Si Carrier wafer		All Device Wafers
49	Coat BBS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Dehydration Bake:** 60 sec @ 150 ℃ **Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Bake:** 60 sec @ 150 ℃ **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers
50	Coat LAS	**Tool:** CEE 100 Resist Spinner **Recipe:** 0 Do **Not** use SVG Track (backside resist splattering)	**Spin Coat Microprime P20:** 15 sec @ 5000 RPM **Spin Coat HPR 504:** 3 sec @ 1000 RPM 60 sec @ 5000 RPM **Soft Bake:** 60 sec @ 105 ℃		All Device Wafers

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51	LAS Litho Level V: Passivation Cut	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** V **Mask:** Passivation Cut	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
52	BBS Litho Level V: Passivation Cut	**Tool:** Karl Seuss MA150 **Recipe**: adr **Level:** V **Mask:** Passivation Cut	**Dose:** 150 mJ/cm2 **Time:** Irradiance / Dose **Alignment Gap:** 20 µm **Hard Contact Delay:** 60 sec	Measure lamp **irradiance** to determine exposure **time** Irradiance: _____	All Device Wafers
53	Develop BBS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
54	Develop LAS	**Tool:** CEE 100 Developer **Recipe:** 0 Do **Not** use SVG Track	**Post Exposure Bake:** None **Hard Bake:** 60 sec @ 130 C		All Device Wafers
55	Oxide Etch	**Tool:** Manual Wet Bench **Bath:** MOS Grade 5.2:1 HF:H20	**Thermal Oxide Etch Rate:** ~ 1200 Å/min **Annealed TEOS Etch Rate:** ~ 2029 Å/min **Time:** ??? min		
56	Resist Strip	**Tool**: Wet Bench **Solvent:** PRS2000 **Temp:** 90℃ **Time:** 10 min (each bath)			
57	Sinter	**Tool**: Bruce Furnace Tube: 2 **Recipe**: 41 "425C H2/N2 30min"	Do **Not** use dummy wafers	**Print Thermal History** **Include Profiles, N2, & O2**	All Device Wafers
58	TEST	Electrical Test			All Device Wafers

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