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Back-Illuminated three-dimensionally integrated CMOS image sensors for scientific applications

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ABSTRACT

SOI-based active pixel image sensors have been built in both monolithic and vertically interconnected pixel technologies. The latter easily supports the inclusion of more complex pixel circuitry without compromising pixel fill factor. A wafer-scale back-illumination process is used to achieve 100% fill factor photodiodes. Results from 256 x 256 and 1024 x 1024 pixel arrays are presented, with discussion of dark current improvement in the differing technologies.

Keywords: SOI, active pixel imager, CCD, back-illumination, three-dimensional integration

1. INTRODUCTION

The CMOS support and pixel circuitry available with active pixel-based image sensors provide versatile capabilities to low-cost cameras such as random addressability, windowing, on-chip analog-to-digital-conversion, and noise filtering[1,2,3]. In harsh radiation environments such active pixel architectures have a further advantage since few to no charge packet transfers are required within the silicon detector; in contrast, charge coupled device-based imagers suffer from signal degradation during repetitive charge transfer through radiation-induced trap sites in silicon[4,5,6].

Fully depleted SOI CMOS offers several performance advantages for low-power digital circuits when compared to bulk CMOS, including: near-ideal sub threshold swing, reduced parasitic capacitances, and greater device packing densities[7]. In addition, because of its buried oxide device isolation, SOI-based technologies offer latch-up-free radiation tolerance and a physical amenability to three-dimensional circuit stacking. For imaging applications, Lincoln Laboratory has developed both monolithic[8] and three-dimensionally stacked[9] process technologies, and these fabrication methods includes steps that allow the image sensor to be operated with light directly incident on the photo detector without obscuration from pixel circuitry. Such back-illuminated operation not only permits the realization of 100% fill-factor pixels, but also recovers the blue response that is lost during front-illuminated operation. While other groups have reported back-illuminated CMOS pixel imagers[10,11], most of the technologies used employ epitaxial-silicon substrates with doping and layer thicknesses optimized to minimize latchup in bulk transistors. As seen in Figure 1, the implications for photo detectors fabricated in doped epitaxial silicon is that spectral sensitivity is limited since depletion regions are less than a few microns thick. In contrast, modern scientific CCDs can have depletion regions on the order of fifty to hundreds of microns to efficiently detect the full visible spectrum and x-rays[12,13].

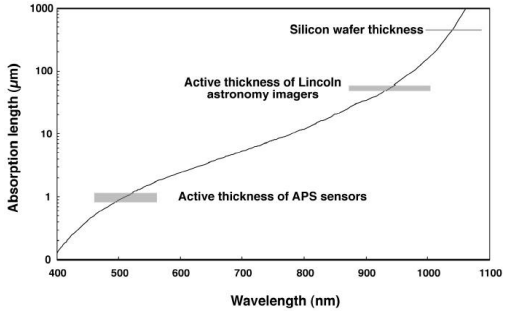

Figure 1: Plot of photon absorption depth into silicon as a function of wavelength. CMOS image sensors are typically fabricated using epi-layers only a few microns thick. Custom CCD-fabrication process technologies result in active photo-collection regions of 50-100 microns. Lincoln Laboratory's facility uses 150-mm diameter wafers that are approximately 675-microns thick.

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In this paper we describe results and progress with three active pixel sensors developed to explore new fabrication methods for future imagers. The first is an exploratory design built using a monolithic SOI-based image sensor technology. The second and third use a vertically interconnected (or three-dimensionally stacked) pixel architecture to bring greater functionality to the sensor without compromising on fill factor nor co-optimizing detector and transistor fabrication steps.

2. MONOLITHIC SOI-BASED ACTIVE PIXEL SENSOR

A single-wafer-based image sensor can be fabricated in silicon-on-insulator wafers by locating the photosensitive elements in the handle wafer. Figure 2 shows schematic illustrations of a back-illuminated charge coupled device and a single photodiode pixel.

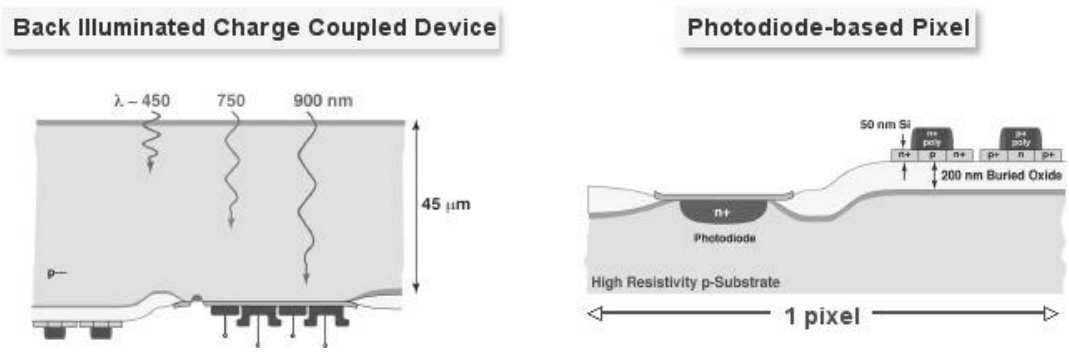

Figure 2: Schematic illustration of (left) back illuminated CCD adjacent to SOI devices and (right) single pixel implemented for an active pixel imager. The photosensitive elements are fabricated in the SOI handle wafer, which can be thinned for high-fill factor back illumination.

In both implementations the active CMOS transistors are built in the thin (~50nm) silicon islands. The handle wafer resistivity and photo detector device doping profiles can be tailored to suppress dark current and obtain the desired spectral response. Unlike a bulk, junction-isolated monolithic imager, the oxide isolation decouples the detectors from the CMOS circuitry and evades junction leakage. Several test CCD imagers were built using this first generation technology; a noteworthy demonstration included on-chip 3.3V control logic and analog-to-digital conversion[8].

While the process was optimized for low-voltage CCDs with integrated on-chip CMOS devices, an experimental active pixel test imager design was also included. It consists of a 256 × 256 array of pixels divided into sixteen 64 × 64 pixel blocks. Each 12-micron square pixel contains a photo detector, a source follower input transistor, row-selection transistors, and a reset transistor. The photo detector (diode or gate) is fabricated in the bulk high-resistivity handle wafer with all transistors fabricated in the thin SOI. The photogate pixels include a transfer gate to move charge from the integrating capacitor onto the sense node. All SOI transistors are fabricated as body-tied FDSOI n-MOS to minimize floating body effects, edge conduction, and (potentially) noise. The sensor employs a commonly used architecture in which a column parallel readout is multiplexed one row at a time and then one column at a time through a single on-chip amplifier/buffer[2]. This design includes circuitry for correlated-double-sampling (CDS) and on-chip fixed pattern noise (FPN) suppression within each column. Dark current, noise, and responsivity of the various pixel designs were measured using an electronics system adapted from a CCD test system[14].

Figure 3 displays a photomicrograph of a portion of the array (left) and an atomic force microscope image showing the bulk-photodetector and SOI-transistor regions within a single pixel (right). Several of the test pixel designs worked well and in certain cases the noise was sufficiently low to permit observation of X-rays from an Fe-55 source[14].

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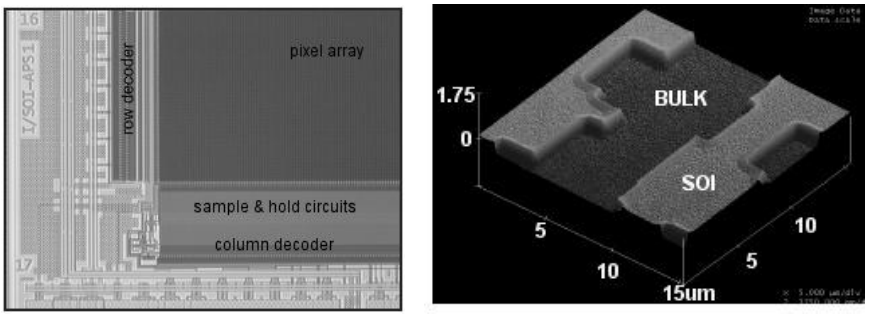

Figure 3: Photomicrograph detail of monolithic SOI-based active pixel imager (left) and atomic force microscope image from a single pixel (right). The bulk photosensitive regions are lower than the SOI transistor regions.

Two noteworthy issues were observed during testing. The first is best illustrated with the Figure 4 example dark image result captured from a CCD imager during alpha particle illumination. We observed that those CCD imagers that were closely surrounded by SOI circuits exhibited high dark current that increased from center to edge of the device. CCDs that had greater separation between the SOI-CMOS boundary and the imaging device did not exhibit this behavior. The source of the excess dark current, illustrated in Figure 4, is surface state generation arising from the buried oxide/handle wafer substrate interface. There are two solutions to this issue: the first is to include an additional boron implant positioned at the BOX/handle wafer interface to suppress surface state generation; the second is to include a n+ guard ring surrounding the CCD to intercept any perimeter dark current and stray photocurrent.

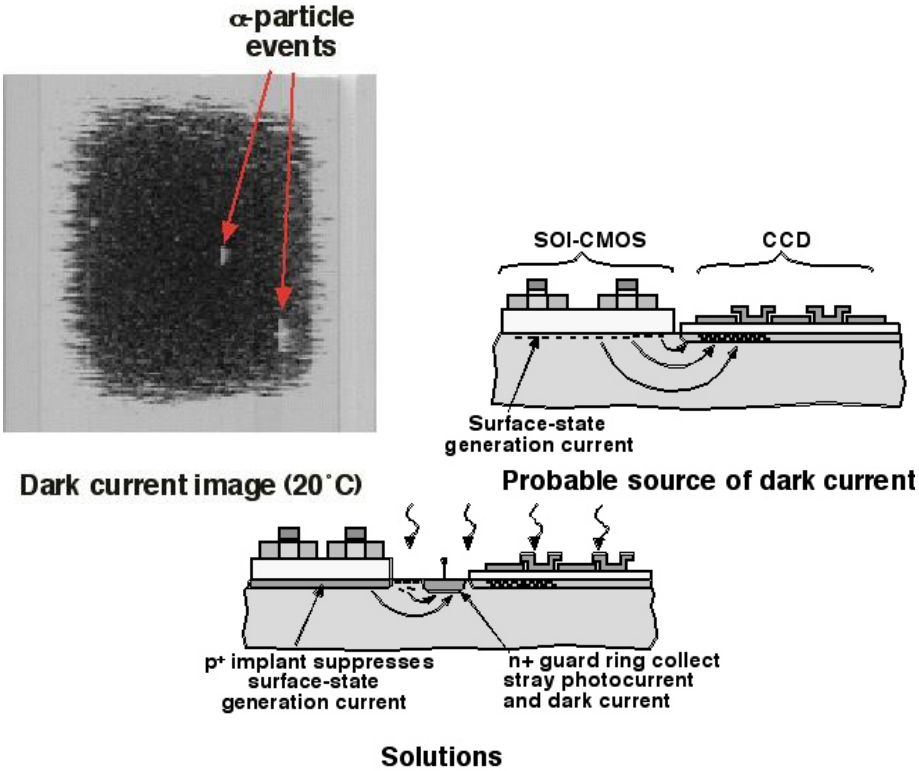

Figure 4: Example dark current image obtained from a CCD imager with nearby SOI circuitry. The perimeter source of dark current and potential solutions are also illustrated.

The second issue of note pertains to the impact of SOI transistor layout on pixel dark current. As shown in the Figure 5 pixel schematic, the pixel includes a reset transistor, with gate RSTG, connected in series with the photodiode. Any

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leakage through this reset transistor may be interpreted as pixel dark current. The scanning electron micrograph images of Figure 5 compare reset transistors in which the gate overhangs the SOI island (center) and in which the gate is enclosed on the SOI island (right).

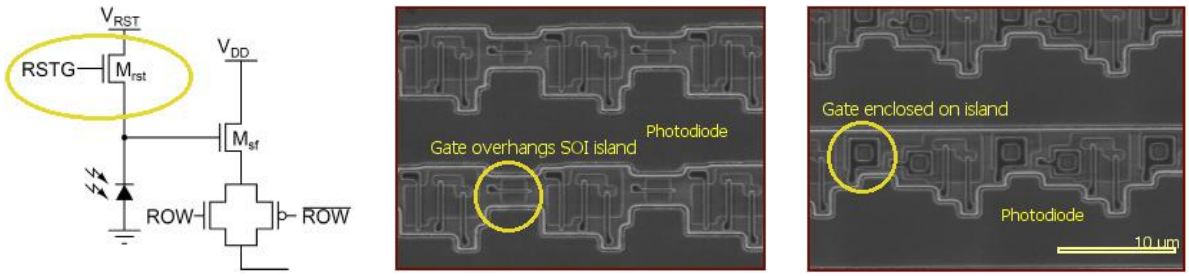

Figure 5: Pixel schematic illustrating reset transistor (left) and scanning electron micrograph images for pixels using conventional gate layouts (middle) and enclosed-gate layout (right).

In Figure 6 we compare measured dark current for these layouts. Pixels with the overhanging gate suffer from excess off-state current arising from locally lower transistor thresholds along the SOI island edge. Pixels with the enclosed gate do not have this extra conduction path. Enclosed gate layouts are commonly used in applications for radiation environments. Reset transistor leakage can be further reduced with a modified transistor threshold implant as well as an improved local implant to suppress SOI sidewall conduction.

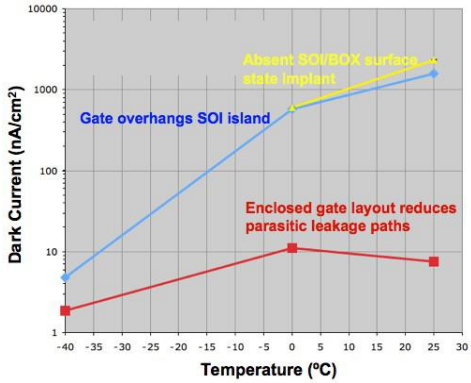

Figure 6: Comparison of measured dark current between pixels using reset transistors with gate overhanging the SOI island (circle) or enclosed within the island (square). The overhanging gate is vulnerable to SOI island edge conduction.

While a monolithic SOI-based imaging technology may have advantages for a CCD/CMOS application, the pixel-layout and co-optimized fabrication compromises may be overly restrictive for dense-pixel-pitch active pixel sensors. We next present a vertically interconnected approach that relieves some of these concerns and provides for even lower dark current photosensors.

3. BACK-ILLUMINATED 3-D CIRCUIT INTEGRATION TECHNOLOGY

3.1 Fabrication sequence

Lincoln Laboratory has developed a 150-mm wafer-scale process technology that enables the dense vertical interconnection of multiple circuit layers[9]. For image sensor applications the first circuit layer or tier is a silicon or compound semiconductor device and the second and subsequent tiers contain silicon-on-insulator (SOI)-based electronics. Up to three interconnected tiers have been demonstrated, including a laser radar focal plane based on Geiger-mode avalanche photodiodes, which can detect a single photon and produce a digital logic pulse directly from the detector[15].

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Each circuit layer of the 3-D stack is referred to as a "tier", as drawn in Figure 7. The photodiode tier (Tier-1) consisted of p+n diodes in high-resistivity (>3000 Ω-cm, n-type) float-zone silicon substrates. The diode's lateral doping profile is graded using implant masking and thermal annealing to minimize the surface contribution to dark current. A standard planar CMOS back-end sequence forms contact, plugs, and a metal layer. The second tier (Tier-2) is fabricated using our 0.35-µm FDSOI-CMOS process with 7.2-nm gate oxide, cobalt-silicide, and planar three-level-metal interconnect. After completion of individual circuit tier fabrication, Tier-2 is inverted over Tier-1, aligned and mated using a low-temperature oxide-oxide bonding process. A wet chemical etch removes the Tier-2 handle wafer down to the buried oxide. A multistep dry-etch process forms 2-µm square 3-D-vias between Tier-2 and Tier-1. The ~7.5µm via depth is filled with Ti/TiN liner deposited from a collimated bias-sputter source, tungsten (W) plugs are formed by CVD (475°C) to connect the two metal layers, and excess metal is removed by CMP. At this point additional tiers could be bonded and interconnected. To prepare the 3-D stack for illumination from the photodiode side, the detector tier silicon is thinned to approximately 50µm, coated with an antireflection layer, and then mounting onto a transparent support in a process sequence similar to that used to make back-illuminated CCDs[12]. Standard semiconductor equipment was used for all processing steps.

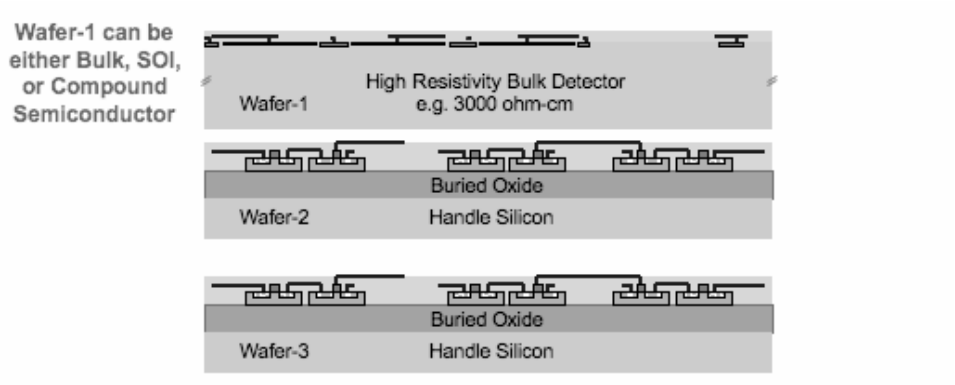

Figure 7: Illustration of three wafers to become vertically interconnected. Each circuit layer will become a "tier" of the three-dimensionally interconnected circuit.

As shown in Figure 8, the circuit tiers are vertically interconnected through an oxide-bonded interface, and the detector tier may be thinned for 100% fill factor, back-illuminated operation. For mechanical support, an optional transparent substrate may be present, and openings may be included in the substrate for soft X-ray penetration.

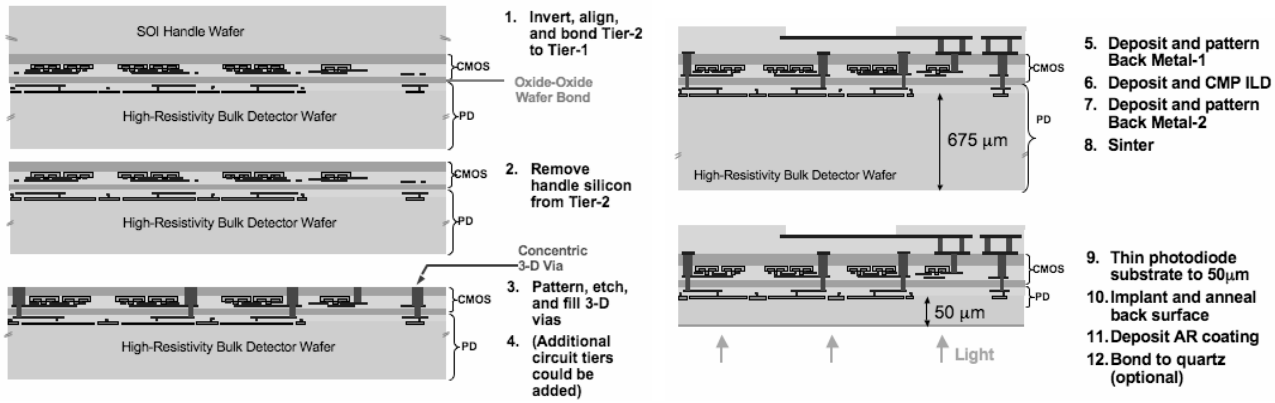

Figure 8: Summary of steps required to oxide bond and vertically interconnect

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We are working to continue scaling the 3-D via size to smaller dimensions[16]. The combination of small wafer-to-wafer alignment tolerance (+/- 0.50µm) and small 3D via size (1-2µm) permits aggressively small pixels which are 100% fill factor after back illumination. The use of high resistivity detector tier substrates, similar to those used for scientific-grade CCDs, provides much greater spectral sensitivity.

3.2 Example demonstration #1:1024 x 1024 array of 8 x 8 micron pixels

Earlier we demonstrated a back illuminated 1k x 1k CMOS visible imager[17] with 8µm x 8µm pixels. The final chip spans 8mm square, and 3-D (vertical) vias are located at every pixel, in addition to portions of the control circuitry. Transistor characteristics before and after 3-D fabrication are shown in Figure 9, for both p-channel (left) and n-channel (right) SOI transistors.

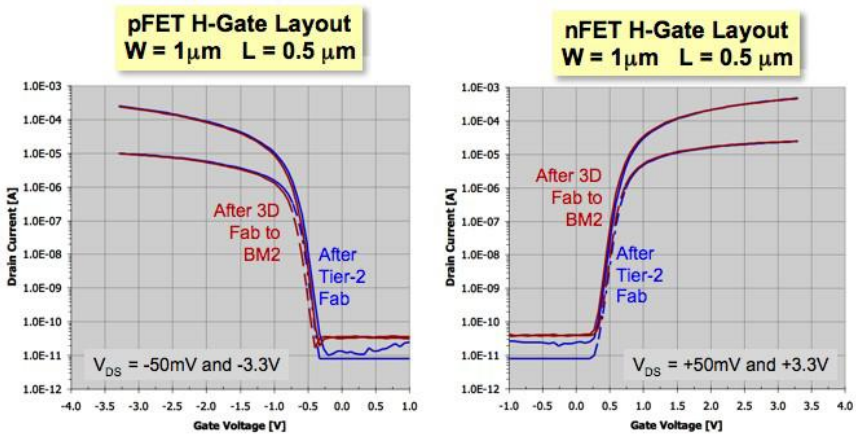

Figure 9: Comparison of p-channel (left) and n-channel (right) SOI transistor transfer characteristics measured before and after 3-D fabrication. No change in transistor behavior is observed due to the fabrication steps.

Despite the dense degree of vertical integration, the numerous level of metal interconnect and the physical complexity of the structure, the image sensor continued to functioned well after back illumination. Figure 10 shows example front illuminated (left) and back illuminated (right) images captured using the device, demonstrating that the back-illumination steps preserved the functionality of the sensor operation. Because of program schedules, only two devices were carried through packaging for back-illumination test. While both worked, full frame operation was limited because of a blockage in the row shift register addressing – a defect that is distinct from 3-D fabrication. A high assessment of 3-D via yield was deduced from pixel operability, which was measured on a few number of chips to be > 99.999%.

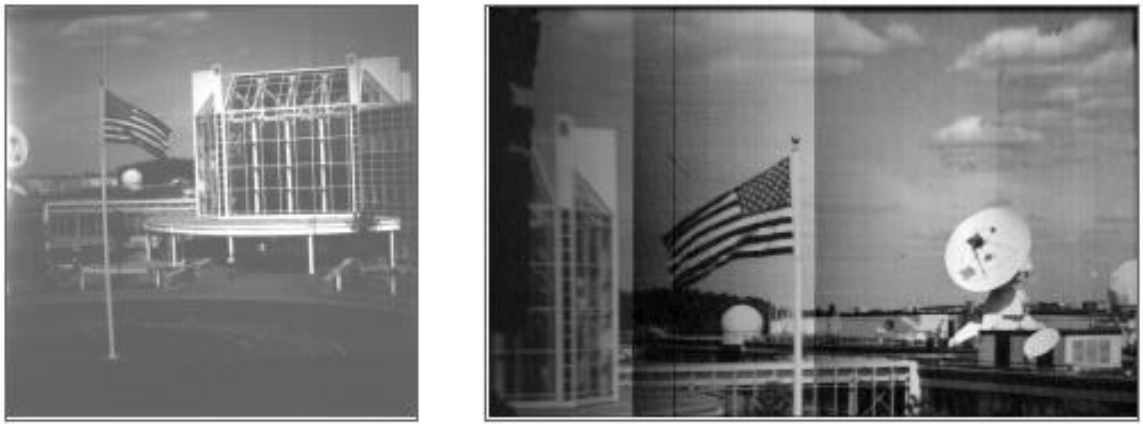

Figure 10: Example room temperature imagery from packaged (left) front illuminated and (b) back illuminated devices. Only

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For a test array of 8-micron square photodiodes without any readout circuitry, the room temperature dark current measured to be less than 200pA/cm^2. For the imager pixels, the room temperature dark current was measured to be 1-3nA/cm^2. The additional contribution to the imager pixel dark current arose from floating body and subthreshold leakage in the SOI transistors.

3.3 Example demonstration #2: 256 x 256 array of 24 x 24 micron pixels

With dense vertical integration of pixel detector to associated transistors comes the benefit that greater area in the pixel footprint can be devoted to readout circuitry than could be accomplished in a conventional monolithic architecture. We have recently begun testing of a second device, which takes advantage of the vertical connection to include a simple noise suppression circuit to reduce reset noise, which can be the dominant noise source under low illumination. The pixel schematic and timing are shown in Figure 11. This per-pixel 'clamp' CDS circuit is inspired by an earlier published design[18].

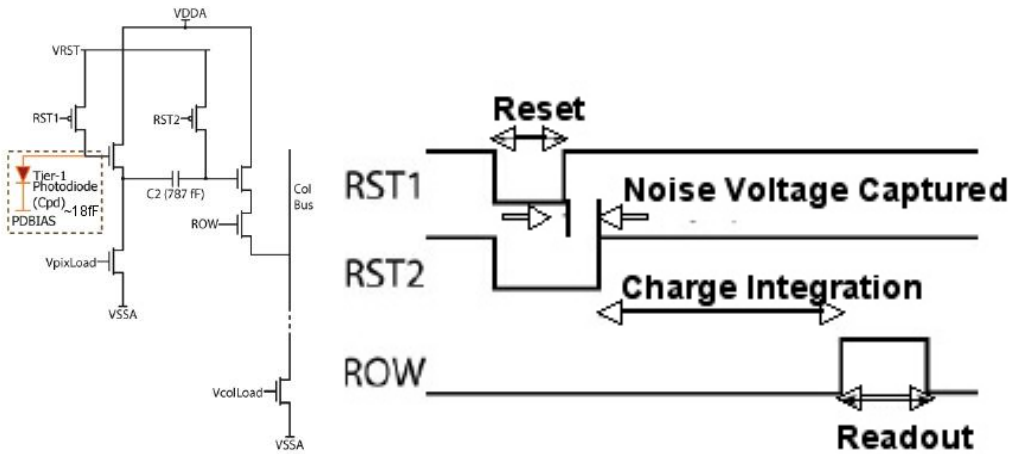

Figure 11: Pixel schematic (left) and timing diagram (right) implemented in 3-D integrated example #2. The pixel size is 24-micron square.

The pixel consists of two reset switches (MRST1 and MRST2), two source followers, a CDS capacitor (C2), and row selection transistors. Reset noise reduction is accomplished by transferring the large kT/Cpd reset noise from the MRST1 reset to the much larger coupling capacitance C2. The pixel is operated with a two-stage reset. In the first phase both MRST1 and MRST2 are held low (for p-MOS reset transistors). Integration begins when MRST1 is raised. The noise from MRST1 is transferred to C2, where it is subtracted by the capacitor. Since the initial reset noise is subtracted, the operation is a form of correlated double sampling, here occurring internal to the pixel. Finally MRST2 is raised, causing a smaller kT/C2 noise voltage to be sampled onto the capacitor.

The layout of the pixel in each of the two tiers is shown in Figure 12. We use p-MOS reset transistors to allow complete reset of the photo-diode node, thus avoiding image lag. SOI transistor layout was driven to minimize parasitic leakage mechanisms; thus H-gate geometries and body-ties were employed where possible. A generous 24-µm square was allotted to the pixel so that we could achieve a large in-pixel coupling capacitance (780fF). Much finer pixel sizes could be realized by using conventional (non-H-gate) transistor gate geometries, smaller coupling capacitance, or by elevating the coupling capacitance to an even higher third circuit tier. The diode tier layout is very simple, consisting only of implants, since there is no need for STI or LOCOS isolation.

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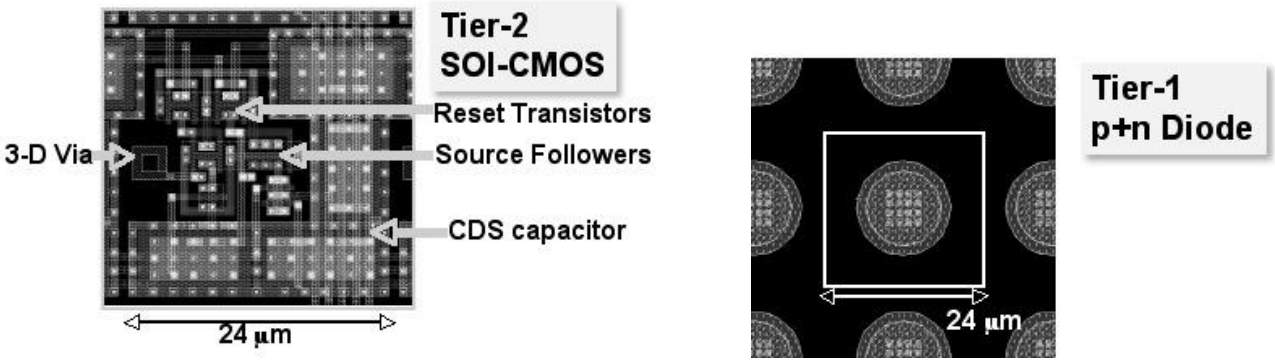

Figure 12: Pixel Layout in Tier-2 (left) and Tier-1 (right). The pixel circuit includes reset gates, CDS capacitor, and readout transistors.

The initial devices have completed fabrication through back illumination and packaging with good operation. Figure 13 shows example imagery obtained at room temperature under back illumination with no correction applied to the data. Early measurements of room temperature pixel dark current is <20 pA/cm^2. This low value is attributed in part to the relatively larger pixel size (24-micron square), the associated lower diode edge-to-area ratio, and the H-gate SOI reset transistor design. On the samples tested, pixel operability is high (>99.6%), dominated by column dropouts, not by 3-D via yield issues. Further measurements are in progress including quantum efficiency, responsivity, noise, and radiation testing.

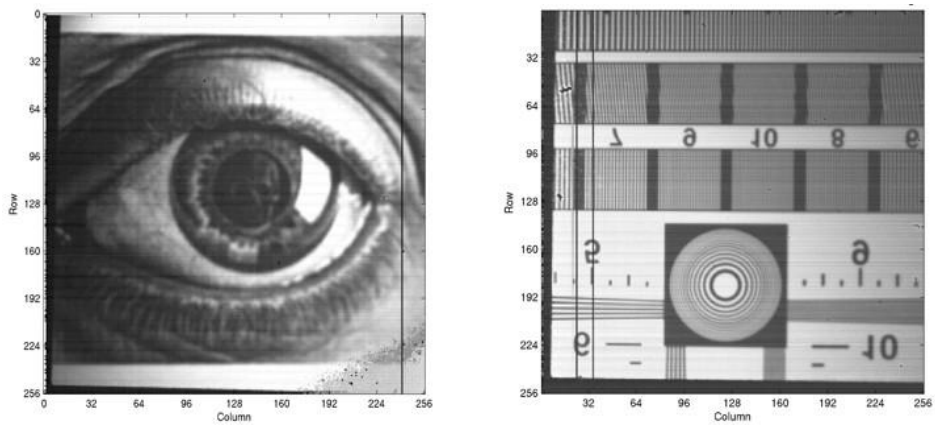

Figure 13: Two uncorrected example images captured at room temperature from the first packaged back-illuminated devices.

4. CONCLUSIONS

SOI-based technologies can support both monolithic and vertically interconnected active pixel image sensors. The inherent fabrication and device design tradeoffs inherent in a monolithic technology make 3-D technology particularly attractive for 100% fill factor, small-pixel-size active pixel imagers. Two 3-D interconnected, back-illuminated imager examples were presented, each showing good pixel operability after fabrication. Very low pixel dark currents can be obtained, especially with larger photodiode pixels sizes and SOI layout-managed techniques to minimize transistor leakage. These early results are encouraging for future demonstrations of scientific-grade active pixel imagers with broad spectral response.

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