

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

T-MOBILE US, INC., AT&T MOBILITY LLC, CELLCO PARTNERSHIP
D/B/A VERIZON WIRELESS, ERICSSON INC. AND
NOKIA OF AMERICA CORPORATION,

Petitioners,

v.

SMART RF INC.,

Patent Owner.

Case IPR2025-00691

U.S. Patent 10,958,296

PATENT OWNER'S PRELIMINARY RESPONSE

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I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Patent Owner Smart RF Inc. (“Patent Owner”) submits this Preliminary Response the Petition for *Inter Partes* Review (“Petition,” Paper 6) filed by T-Mobile US, Inc., AT&T Mobility LLC, Cellco Partnership d/b/a Verizon Wireless, Ericsson Inc., and Nokia of America Corporation (“Petitioners”) and challenging claims 1-10 of U.S. Patent No. 10,958,296 (the “’296 patent”) (Ex. 1001). The Board should not institute *inter partes* review because Petitioners have not met their burden of showing a reasonable likelihood of prevailing on any of its proposed grounds of unpatentability, each based on obviousness under 35 U.S.C. § 103(a) (pre-AIA).

The Petition suffers from many fundamental flaws, each of which warrants denial of institution. For example, to prevail under Grounds 1 and 2, Petitioners must show that World Intellectual Property Organization International Publication No. WO 2012/129768 to James Peroulas (“Peroulas”) discloses or suggests each element of independent claims 1 and 10. But as explained in detail below, Peroulas fails to disclose or suggest multiple elements of both of the claims. Similarly, under Grounds 3 and 4, Petitioners must show that U.S. Patent No. 6,999,523 to Harri Posti (“Posti”) discloses or suggest each element of independent claims 1 and 10, which Petitioners also fail to do, for many of the same reasons as with Peroulas.

To justify the institution of an *inter partes* review, a petitioner must establish that there is a “reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). For at least the reasons discussed in this preliminary response, Petitioners have not shown a reasonable likelihood of prevailing on any of the challenged claims.

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed in this preliminary response and expressly reserves the right to rebut any such arguments in its patent owner response if *inter partes* review is instituted. Additionally, Patent Owner is not limited to the arguments presented here in this preliminary response, but expressly reserves the right to raise further arguments, including claim construction arguments. Patent Owner also incorporates and makes reference to the arguments presented in Patent Owner’s Request for Discretionary Denial of Institution (Paper 10).

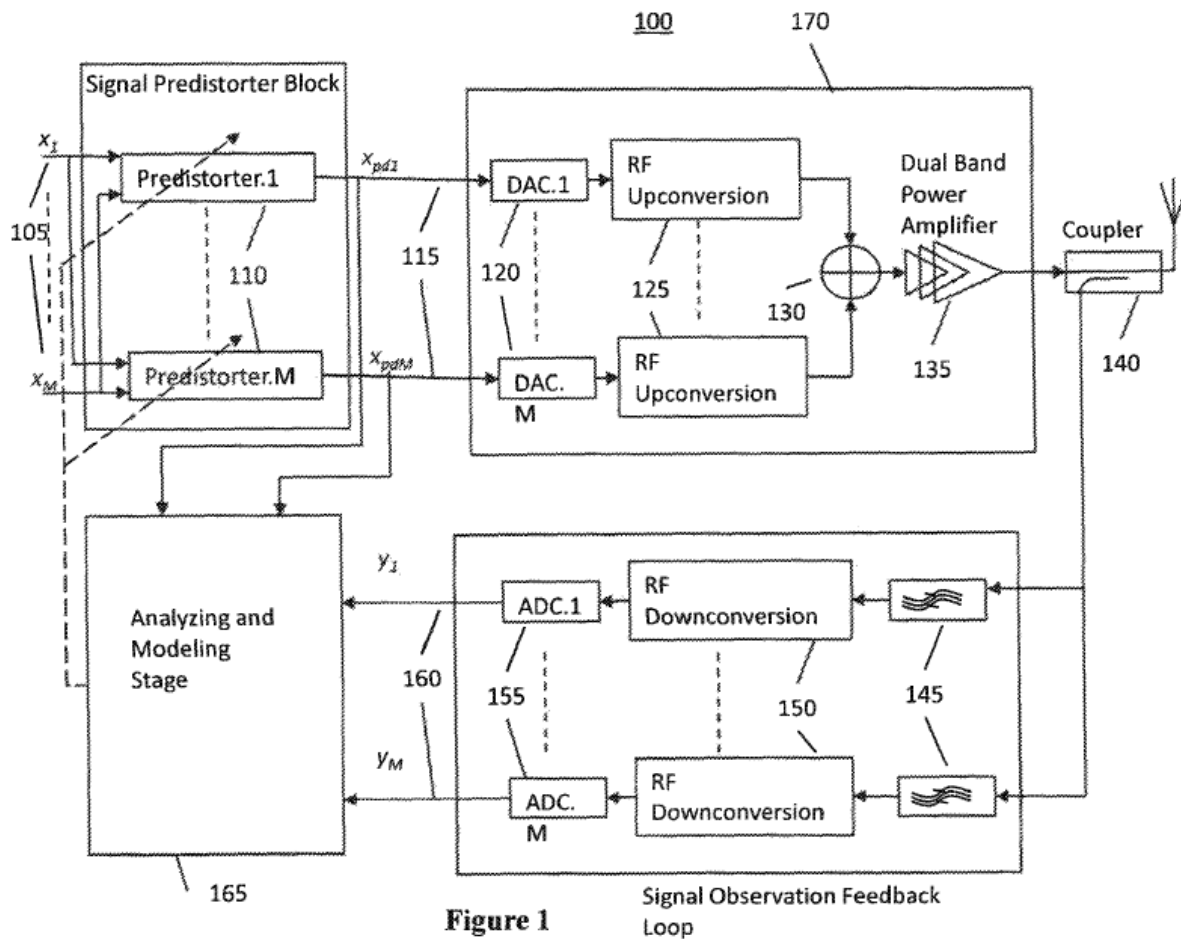
II. THE ’296 PATENT AND THE CHALLENGED CLAIMS

The ’296 patent issued from an application filed on May 1, 2017, and claims priority to an earlier application that was filed on October 14, 2011. Ex. 1001 at 1. The inventions disclosed and claimed in the ’296 patent relate generally to multi-band digital predistortion linearization, particularly as applied to radio frequency (RF) transmitters. *Id.* at 1:27-28; 1:32-41. The power amplifiers within such

transmitters consume the most power within the system, are inefficient, and function in a non-linear manner that introduces distortions that degrade signal quality. *Id.*

To address such problems, the '296 patent discloses and claims new and novel systems and methods that utilize a concurrent digital multi-band linearizer that predistorts the signals before they are amplified, effectively removing the resultant distortion from the amplifier. *Id.* at 2:35-41. The patent further discloses the use of a subsampling feedback loop in which the predistorted signals and the amplified signals are analyzed and modeled to better predict and compensate for signal distortions. *Id.* at 4:2-37.

Figure 1 of the '296 patent is a block diagram of one embodiment of the dual-band digital predistortion architecture.



This figure shows a transmitter 170 in which input signals x_1 and x_2 (105) are fed into pre-distorter blocks 110, which then outputs predistorted signals x_{pd1} and x_{pd2} (115). *Id.* at 3:51-57; 4:2. Those signals are combined and amplified by power amplifier 135. *Id.* at 3:56-57. A coupler 140 then captures a sample of the amplified signal, and ultimately the signal is processed such that the analyzing and modeling stage can receive output signals y_1 and y_2 (160) and process them along with the predistorted inputs x_1 and x_2 (105) within the feedback loop. *Id.* at 4:2-5. The processing model equations for that embodiment are:

$$x_{pd1}(n) = \sum_{m=0}^{M-1} \sum_{k=0}^{K-1} \sum_{j=0}^k c_{1,j,k,m} x_1(n-m) |x_1(n-m)|^{k-j} |x_2(n-m)|^j$$

$$x_{pd2}(n) = \sum_{m=0}^{M-1} \sum_{k=0}^{K-1} \sum_{j=0}^k c_{2,j,k,m} x_2(n-m) |x_2(n-m)|^{k-j} |x_1(n-m)|^j$$

Id. at 4:5-18.

Consistent with the foregoing, the '296 patent contains two independent claims as follows:

Claim 1	Limitations
1[pre]	A linearized transmitter comprising:
1[a]	a digital signal predistorter block including digital baseband signal predistorters effecting predistortion of concurrent input signals to output concurrent predistorted signals;
1[b]	a power amplifier block connected to amplify the predistorted signals; and
1[c]	an analyzing and modelling stage receiving first feedback signals taken from an output of the power amplifier, and second feedback signals taken concurrently from the concurrent predistorted signals and using the first feedback and the second feedback signals in the analyzing and modelling stage to model a nonlinearity in the power amplifier, wherein the digital baseband signal predistorters are updated by the analyzing and modelling stage.
Claim 10	Limitations
10[pre]	A method for linearizing a transmitter, said method comprising:

10[a]	effecting predistortion of concurrent input signals to output concurrent predistorted signals using a digital signal predistorter block including digital baseband signal predistorters;
10[b]	amplifying the predistorted signals using a power amplifier block;
10[c]	receiving in an analyzing and modelling stage first feedback signals taken from an output of the power amplifier, and second feedback signals taken concurrently from the concurrent predistorted signals; and
10[d]	using the first feedback and the second feedback signals in the analyzing and modeling stage to model a nonlinearity in the power amplifier, wherein the digital baseband signal predistorters are updated by the analyzing and modelling stage.

Id. at 6:2-18 and 7:1-17.

III. LEVEL OF ORDINARY SKILL

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioners' definition of a person of ordinary skill in the art, but it reserves the right to do so if trial is instituted.

IV. CLAIM CONSTRUCTION

Similarly, for the limited purpose of this Preliminary Response, Patent Owner does not contend that any claim terms need construction, and can be given their plain and ordinary meaning, but it reserves the right to do so if trial is instituted.

V. APPLICABLE LEGAL STANDARDS

The Board may only grant a petition for *inter partes* review where “the information presented in the petition ... shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioners bear the burden of showing that this statutory threshold has been met. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756 (Aug. 14, 2012) (“The Board ... may institute a trial where the petitioner establishes that the standards for instituting the requested trial are met”).

At a minimum, the reasonable-likelihood-of-prevailing standard “effectively requires the petitioner to present a prima facie case justifying a rejection of the claims in a patent.” 112 Cong. Rec. S1375 (daily ed. Mar. 8, 2011) (quoting Sen. Kyl). As explained by the Federal Circuit, “the expedited nature of IPRs bring[s] with it an obligation for petitioners to make their case in their petition to institute.” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). Moreover, the Board may not overlook flaws in the petition or reformulate its challenges to enhance their suitability. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (“[I]t’s the petitioner, not the Director, who gets to define the contours of the proceeding.”); *see also id.* (“[T]he petitioner is master of its complaint . . .”); *see also id.* at 1353 (forbidding the Board from “curat[ing]” the petition).

A. Obviousness

Section 103 of the Patent Act provides that “[a] patent may not be obtained ... if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries: the level of ordinary skill in the art must be established; the scope and content of the prior art must be determined; and any differences between the prior art and the claims at issue must be ascertained. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

1. Claims cannot be found obvious if an element is absent.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 15 at 15 (PTAB Jan. 9, 2013) (refusing to institute an *inter partes* review under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

2. *A petition must address the Graham factors.*

Obviousness is resolved on several factual determinations “including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art.” *See Graham*, 383 U.S. at 17-18. Petitions for *inter partes* reviews “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, IPR2014-00358, Paper 11 at 29-30 (PTAB July 23, 2014).

3. *A petition must provide articulated reasoning with rational underpinning to combine references.*

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, IPR2016-00197, Paper 7 at 7-11 (PTAB April 29, 2016) (faulting a

petition's obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

VI. GROUND 1 FAILS

For Ground 1, the Petitioners contend that Peroulas renders claims 1-7 and 10 obvious. Pet. at 22. As explained below, Peroulas fails to disclose a number of limitations of independent claims 1 and 10, and Petitioners provide no explanation about how it would have been obvious to modify Peroulas to add those missing limitations. Thus, the Board should deny institution as to Ground 1.

A. 1 [a] – Peroulas's MIMO pre-distortion module does not effect predistortion “of concurrent input signals to output concurrent predistorted signals.”

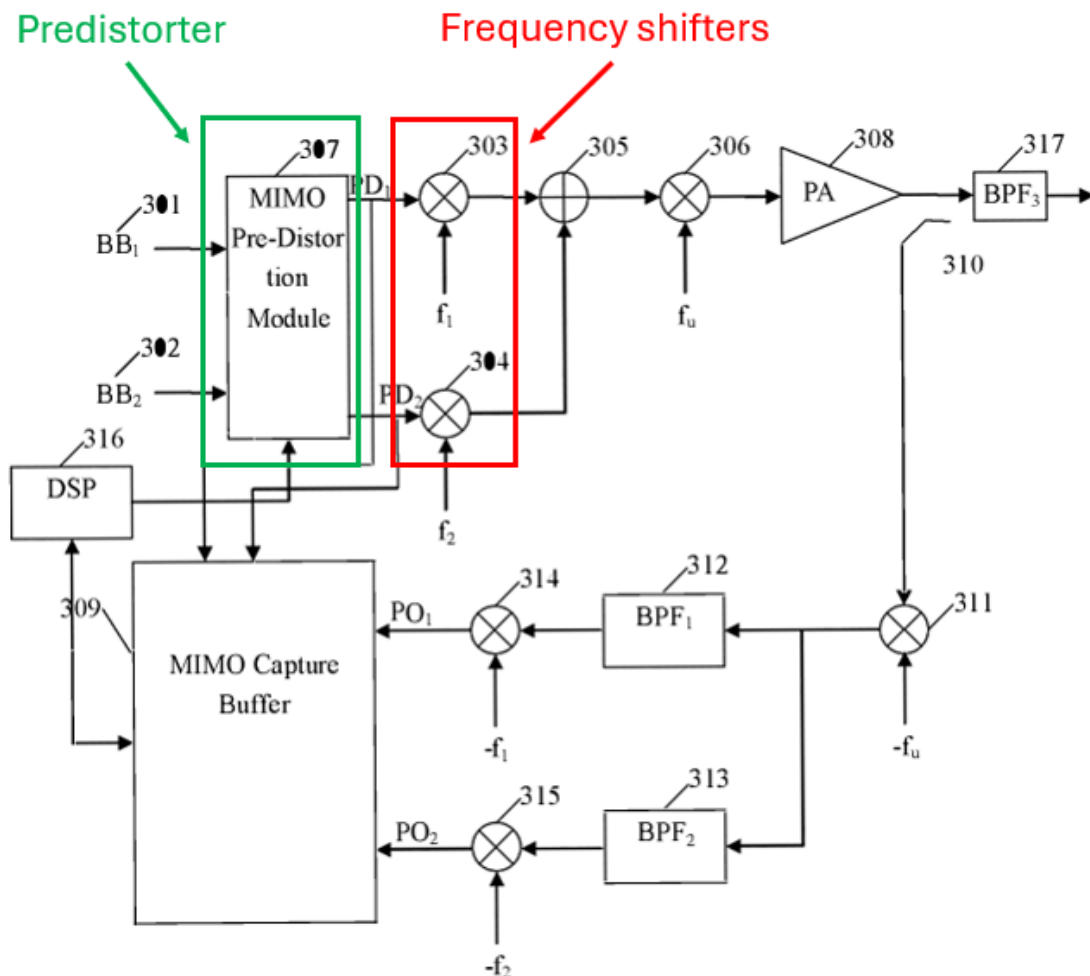
Petitioners failed to show that Peroulas renders element 1[a] obvious as to the requirements that two distinct predistorters effect predistortion “of *concurrent* input signals to output *concurrent* predistorted signals.” Ex. 1001 at 6:3-6. These requirements are essential to the inventions and Petitioners cannot show that Peroulas discloses or suggest that either the input signals or the output signals are concurrent. Indeed, claim 1 was amended to require that the predistorters “output concurrent predistorted signals.” Ex. 1002 at 173 (emphasis in original).

Peroulas does not specify or suggest that its MIMO predistortion module either receives concurrent input signals or produces concurrent output signals.

Instead, Peroulas merely states that:

Baseband signals BB1 301 and BB2 302 are sent into a multiple input multiple output (MIMO) pre-distortion module 307 to produce signals PD1 and PD2, and the MIMO pre-distortion module 307 processes baseband signals BB1 301 and BB2 302 with a MIMO predistortion function. Signals PD1 and PD2 are sent into frequency shifters 303 and 304 which shift the frequency of the signals PD1 and PD2 to f_1 and f_2 respectively. Then these shifted signals are combined by an adder 305. Wherein the MIMO predistortion function includes at least two predistortion functions, and each pre-distortion function has two inputs and one output. The number of the inputs for each pre-distortion function is equal to the number of the baseband signals input into the multiband digital pre-distorter, and the number of the predistortion functions is equal to the number of the baseband signals input into the multiband digital pre-distorter.

EX-1005, 22:26-23:9. But nothing in this disclosure suggests that either the input signals (BB1 301 and BB2 302) are concurrent. Frequency shifting signals does not mean the signals are concurrent. Moreover, the frequency shifters 303 and 304 are outside of the MIMO predistortion module 307, so they provide no indication as to whether BB1 or BB2 are concurrent.



EX-1005, Fig. 3 (annotated). In fact, neither Petitioners nor their expert make any attempt to explain separate frequency shifts outside of the predistorter evidence concurrent input signals to the predistorter.

Petitioners' claim that Equations 15 and 16 evidence concurrent input signals is also misplaced. Simply because the predistortion equations use BB_1 and BB_2 does not mean that BB_1 and BB_2 were received by the predistorter concurrently. Equations 15 and 16 take the sums of signals BB_1 and BB_2 at specific time

instances. But this does not speak to whether the predistortion module *concurrently* received BB1 and BB2.

Further, Peroulas expressly admits that it does not enable outputting concurrent predistorted signals.¹ Peroulas states

[T]he preferred embodiment assumes that the propagation delay through any one element in the chain is 0. This was done to simplify the description of the invention. **It should be clear to one skilled in the art that a real system will have a non-zero delay.** This delay can be measured and compensated by inserting an equivalent delay on the PD1 and PD2 signals **as they enter the MIMO capture buffer** 309.

EX-1005, 31:1-5 (emphasis added). In other words, Peroulas admits that a POSA would understand that its MIMO predistorter cannot concurrently output predistorted signals. And instead suggests using delays in the MIMO Capture Buffer to subsequently align such signals.

Thus, Petitioners have failed to show that Peroulas renders element 1[a] obvious for this additional reason.

B. 1[c] – Peroulas does not disclose “second feedback signals taken concurrently from the concurrent predistorted signals.”

¹ While Peroulas discusses an embodiment with no propagation delay, it does not inform a POSA how such an embodiment could be achieved. *See Raytheon Techs. Corp. v. GE*, 993 F.3d 1374, 1381 (Fed. Cir. 2021) (“In the absence of such other supporting evidence to enable a skilled artisan to make the claimed invention, a standalone § 103 reference must enable the portions of its disclosure being relied upon.”).

Element 1[c] provides for “an analyzing and modelling stage receiving first feedback signals taken from an output of the power amplifier, and second feedback signals taken concurrently from the concurrent predistorted signals and using the first feedback and the second feedback signals in the analyzing and modelling stage to model a nonlinearity in the power amplifier, wherein the digital baseband signal predistorters are updated by the analyzing and modelling stage.” Ex. 1001 at 6:9-18. The Petition alleges that “Fig. 3 depicts Peroulas’ predistorted signals PD1 and PD2 (second feedback signals) being concurrently provided to the MIMO Capture Buffer 309.” Pet. at 30. But Petitioner’s interpretation of Figure 3 contradicts the express disclosure of Peroulas. As discussed above, Peroulas unequivocally states that a POSA would understand that PD1 and PD2 are not taken concurrently by the MIMO Capture Buffer. EX-1005, 31:1-5.

The Petition attempts to cure this shortcoming by arguing that “a POSA would have been motivated to provide predistorted signals PD1 and PD2 to MIMO Capture Buffer 309 concurrently to not only avoid delays associated with serial processing, but to fulfill Peroulas’ disclosure that its predistorters are simultaneously updated” Pet. at 30. But this argument ignores the fact that Peroulas discloses a separate solution for the fact that PD1 and PD2 are not taken concurrently by the MIMO Capture Buffer. Specifically, Peroulas teaches using delays within the MIMO Capture Buffer to align PD1 and PD2. EX-1005, 31:4-5. Thus, Petitioners’ alleged

motivation is improper as Peroulas implements a separate solution to fulfill the simultaneous update requirement.

Thus, Petitioners have failed to show that Peroulas renders element 1[c] obvious.

C. 1[c] – Peroulas does not disclose “using the first feedback and the second feedback signals in the analyzing and modelling stage to model a nonlinearity in the power amplifier.”

Element 1[c] provides for “an analyzing and modelling stage receiving first feedback signals taken from an output of the power amplifier, and second feedback signals taken concurrently from the concurrent predistorted signals and using the first feedback and the second feedback signals in the analyzing and modelling stage to model a nonlinearity in the power amplifier, wherein the digital baseband signal predistorters are updated by the analyzing and modelling stage.” Ex. 1001 at 6:9-18. Accordingly, the analyzing and modeling stage must use the first and second feedback signals to model a nonlinearity in the power amplifier. Petitioners do not and cannot show this.

Petitioners allege that “Peroulas’ DSP Block 316 uses the outputs of the MIMO Capture buffer 309 and least squares minimization to obtain estimates” of the coefficient values of the predistortion function. Pet. at 29. But the Petition makes no effort to demonstrate how the DSP Block uses the first or second feedback signals. And the equations that the DSP Block allegedly uses solve for PD1(n) and

PD2(n). Petitioners have not and cannot show how solving for PD1(n) and PD2(n) constitute using PD1 and PD2.

Thus, Petitioners have failed to show that Peroulas renders element 1[c] obvious.

D. 10[a]– Peroulas’s does not disclose “effecting predistortion of concurrent input signals to output concurrent predistorted signals using a digital signal predistorter block including digital baseband signal predistorters.”

See limitation 1[a] above.

E. 10[c] – Peroulas does not disclose “second feedback signals taken concurrently from the concurrent predistorted signals.”

See limitation 1[c] above.

F. 10[d] – Peroulas does not disclose “using the first feedback and the second feedback signals in the analyzing and modeling stage to model a nonlinearity in the power amplifier.”

See limitation 1[c] above.

VII. GROUND 2 FAILS

For Ground 2, the Petitioners contend that dependent claims 8 and 9 are obvious in view of Peroulas in view of Cidronali. Pet. at 49. Those claims depend from independent claim 1, which Patent Owner shows is not obvious in view of Peroulas. *See* Section VI above. Further, Petitioners do not make new arguments about the elements of claim 1 for Ground 2, but instead that Cidronali provides additional disclosure as to additional elements of claims 8 and 9. Thus, for the same

reasons provided as to Ground 1, the Petition should also be dismissed as to Ground 2.

VIII. GROUND 3 FAILS

For Ground 3, the Petitioners contend that Posti renders claims 1-7 and 10 obvious. Pet. at 22. As explained below, Posit fails to disclose or suggest multiple limitations of independent claims 1 and 10. Thus, the Board should deny institution as to Ground 3.

G. 1[a] – Posti’s digital modulators do not effect predistortion “of concurrent input signals to output concurrent predistorted signals.”

Similar to Petitioners’ contentions about Peroulas under Ground 1, here Petitioners also fail to show that Posti renders element 1[a] obvious as to the requirements that two distinct predistorters effect predistortion “of concurrent input signals to output concurrent predistorted signals.” Ex. 1001 at 6:3-6. In addition to the plain language of the claim, the specification of the ’296 patent repeatedly discloses a concurrent transmitter, concurrent predistortion, and concurrent output signals. *See, e.g.*, Ex. 1001 at Abstract, 2:5-13, and 4:24-27. Further, claim 1 was amended to require that the predistorters “output concurrent predistorted signals.” Ex. 1002 at 173. These requirements are essential to the inventions and Petitioners cannot show that Posti discloses or suggests that either the input signals or the output signals are concurrent.

Posti does not specify or suggest that either the input signals or the output signals are concurrent. Petitioners rely singularly on Posti's Fig. 4 (as annotated by Petitioners), but that figure only shows that each digital modulator 106 receives one input (User 1 Data and User n Data) and each modulator outputs a signal to the combiner 110. *See* Pet. at 60-61 (citing Ex. 1009 at Fig. 4). Posti is silent about whether the input or output signals are concurrent, and Petitioners makes no argument that this would be obvious.

In fact, instead of showing "concurrent input signals," Posti's disclosure suggests that the input signals are sent at different times. In describing the embodiment of Fig. 4 (upon which Petitioners rely), Posti explains that "[i]n the case of the GSM standard the modulators 106 will perform Gaussian minimum shift keying (GMSK)." Ex. 1009 at 4:64-66. Posti also explains that "[t]he GSM standard is a time/frequency division multiple access system (F/TDMA) and accordingly signals will be transmitted by the base station to different mobile stations *in different time slots*." *Id.* at 1:30-34 (emphasis added). Thus, the two inputs to the digital modulators 106 (User 1 Data and User n Data) are not sent at the same time and are not concurrent.

Thus, Petitioners have failed to show that Peroulas renders element 1[a] obvious for this additional reason.

H. 1[c] – Posti does not disclose “second feedback signals taken concurrently from the concurrent predistorted signals.”

Element 1[c] provides for “an analyzing and modelling stage receiving first feedback signals taken from an output of the power amplifier, and second feedback signals taken concurrently from the concurrent predistorted signals and using the first feedback and the second feedback signals in the analyzing and modelling stage to model a nonlinearity in the power amplifier, wherein the digital baseband signal predistorters are updated by the analyzing and modelling stage.” Ex. 1001 at 6:9-18. The Petition alleges that “[s]o that the subtractors 202 can determine the difference signal between Posti’s first and second feedback signals, a POSA understood, as shown in Figs. 4 and 7, for example, that Posti’s second feedback signals are provided to the adaptive predistorter concurrently.” Pet. at 65. Petitioner’s assertions are wrong for multiple reasons.

First, Posti multiple independent subtracters that receive two inputs, one from the channeliser and one from the digital modulator. Ex. 1009 at 7:12-15 (“The predistortor 108a comprises n subtracters 202 each of which receives a respective one of the outputs from the digital modulators 106. Each subtracter also receives a input from the channeliser 140.”). Thus, each individual subtracter merely determines the difference between the predistorted signal and the corresponding power amplifier feedback, there is no need for the subtracter to be concurrent with the other subtracters.

Second, Figures 4 and 7 of Posti do not show concurrent signals. Figures 4 and 7 of Posti show delivering the modulated user data 1 through modulated user data n to the adaptive predistorter. But the fact that multiple signals are delivered to the adaptive predistorter has no bearing on whether such signals are concurrent. Showing two signals being delivered to the same module does not show concurrency because the figures do not indicate when each signal is present — they could be time-multiplexed or processed sequentially. This is particularly true here, as Posti contemplates a TDMA environment. *See* Ex. 1009 at 1:23-36; 9:36-43. Without explicit timing information, signal paths only show connectivity, not simultaneous activity. Notably, there is no reference to concurrent signals anywhere in Posti. In fact, Posti’s disclosure suggests that the input signals are received at different times and are thus not concurrent. *Id.* at 4:64-65.

I. 10[a] – Positi’s digital modulators do not effect predistortion “of concurrent input signals to output concurrent predistorted signals.”

See limitation 1[a] above.

J. 10[c] – Posti does not disclose “second feedback signals taken concurrently from the concurrent predistorted signals.”

See limitation 1[c] above.

IX. GROUND 4 FAILS

For Ground 2, the Petitioners contend that dependent claims 8 and 9 are obvious in view of Posti in view of Cidronali. Pet. at 84. Those claims depend from

independent claim 1, which Patent Owner shows is not obvious in view of Posti. *See* Section VIII above. Further, Petitioners do not make new arguments about the elements of claim 1 for Ground 3, but instead that Cidronali provides additional disclosure as to additional elements of claims 8 and 9. Thus, for the same reasons provided as to Ground 3, the Petition should also be dismissed as to Ground 4.

X. PATENT OWNER’S FINAL COMMENTS

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein and expressly reserves the right to rebut any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the Petition and reserves the right to rebut them later. Additionally, Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

XI. CONCLUSION

Petitioners have not met their burden of showing that either Peroulas or Posti disclose or suggest multiple elements of the independent claims. Consequently, Petitioners have not met their burden of showing a reasonable likelihood of prevailing. Patent Owner respectfully submits that the Board should deny institution.

Dated: July 16, 2025

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CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 4,264 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

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The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on July 16, 2025 to Lead and Back-up Counsel for Petitioners at the service address provided in Petitioner's Mandatory Notices:

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