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Paper No. ____

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMPHENOL CORPORATION,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD.,
Patent Owner.

Case No. IPR2025-00699

Patent No. 11,032,111

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq**

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EXHIBIT LIST

Exhibit	Description
1001	United States Patent No. 11,032,111 (“the ’111 Patent”)
1002	Prosecution History of United States Patent No. 11,032,111
1003	Declaration of Paul S. Min, Ph.D. (“Min”)
1004	Curriculum Vitae of Paul S. Min, Ph.D.
1005	United States Patent No. 9,882,706 (“Lugthart-706”)
1006	United States Patent Publication No. 2014/0281067 (“Das Sharma”)
1007	United States Patent No. 7,239,665 (“Mezer”)
1008	United States Patent No. 8,787,430 (“Raghavan”)
1009	United States Patent No. 9,806,812 (“Schmidt”)
1010	United States Patent No. 9,137,063 (“Zerbe-063”)
1011	United States Patent No. 7,308,058 (“Zerbe-058”)
1012	United States Patent No. 8,477,835 (“Zerbe-835”)
1013	United States Patent No. 9,152,257 (“McCall”)
1014	United States Patent No. 9,118,512 (“Gotman”)
1015	United States Patent No. 10,736,201 (“Burchardt”)
1016	United States Patent No. 7,664,171 (“Sun”)
1017	United States Patent No. 6,680,681 (“Hsu”)
1018	United States Patent Publication No. 2013/0223506 (“Kolze”)
1019	United States Patent Publication No. 2010/0232493 (“Thirumoorthy”)
1020	PCT Publication No. 2016/203205 (“Griffin”)
1021	United States Patent No. 9,495,245 (“Peddle”)
1022	United States Patent No. 5,854,921 (“Pickett”)
1023	United States Patent Publication No. 2004/0071203 (“Gorecki”)
1024	IEEE Std. 802.3-2015, “IEEE Standard for Ethernet: Section 5” (“802.3-2015, Section 5”)
1025	<i>Insertion loss</i> , Newton’s Telecom Dictionary (31st ed. 2018) (“Newton’s”)

Exhibit	Description
1026	<i>Insertion loss, package, loss, dissipation</i> , Oxford – A Dictionary of Electronics and Electrical Engineering (5th ed. 2018) (“Oxford”)
1027	IEEE Std. 802.3bs-2017 “IEEE Standard for Ethernet: Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation” (2017) (“802.3bs”).
1028	Optical Internetworking Forum Implementation Agreement, “Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps,” OIF-CEI-04.0 (Dec. 29, 2017) (“OIF-CEI-04.0”)
1029	United States Patent Publication No. 2015/0189092 (“Thapa”)
1030	United States Patent No. 9,088,336 (“Mani”)
1031	United States Patent No. 9,754,605 (“Chhetri”)
1032	Optical Internetworking Forum, “OIF Next Generation Interconnect Framework,” OIF-FD-Client-400G/1T-01.0 (2013) (“OIF-FD-Client-400G/1T-01.0”)
1033	Section 337 Statistics: Average Length of Investigations, available at https://www.usitc.gov/intellectual_property/337_statistics_average_length_investigations.htm (visited March 21, 2025).
1034	Federal Court Management Statistic-Profiles for the Eastern District of Texas, available at https://www.uscourts.gov/data-news/reports/statistical-reports/federal-court-management-statistics/federal-court-management-statistics-december-2024 (visited March 21, 2025).
1035	<i>In re Certain Active Electrical Cables and Components Thereof</i> , Inv. No. 337-TA-3814, Complaint (Mar. 13, 2025).
1036	<i>In re Certain Active Electrical Cables and Components Thereof</i> , Inv. No. 337-TA-3814, Amended Complaint (Mar. 18, 2025).
1037	<i>In re Certain Active Electrical Cables and Components Thereof</i> , Inv. No. 337-TA-3814, Amended Exhibit 36 to Amended Complaint (Mar. 18, 2025).
1038	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. Amphenol Corp.</i> , No. 2:25-cv-00296 (E.D. Tex. Mar. 13, 2025)

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1039	Dkt. 1-6, Exh. 6 To Complaint, <i>Credo Semiconductor Inc. et al. v. Amphenol Corp.</i> , No. 2:25-cv-00296 (E.D. Tex. Mar. 13, 2025)
1040	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. Molex, Inc.</i> , No. 1:25-cv-00316 (D. Del. Mar. 13, 2025)
1041	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. TE Connectivity PLC</i> , No. 2:25-cv-00297 (E.D. Tex. Mar. 13, 2025)
1042	Dkt. 1, Complaint, <i>Credo Semiconductor Inc. et al. v. Volex PLC</i> , No. 2:25-cv-00298 (E.D. Tex. Mar. 13, 2025)
1043	Boalick, Chief APJ, “Guidance on USPTO’s recission of ‘Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation’” (Mar. 24, 2025)

MANDATORY NOTICES

A. Real Party-In-Interest

Petitioner Amphenol Corporation is a real party-in-interest to this proceeding under 37 C.F.R. §42.8(b)(1).

B. Related Matters

A decision in this proceeding could affect or be affected by the following. The '111 Patent is currently asserted in actions listed in Section B.2, and infringement of the '111 Patent is alleged in the action in Section B.3.

1. United States Patent & Trademark Office

U.S. Patent No. 11,032,111 issued from application ser. no. 16/552,927 and claims priority to provisional application no. 62/723,701, filed on August 28, 2018. The '111 Patent has not been the subject of any post-grant review.

2. United States District Court

a. Eastern District of Texas

Credo Semiconductor Inc. et al. v. Amphenol Corp., No. 2:25-cv-00296 (E.D. Tex.), filed March 13, 2025 (“the Texas Litigation”).

Credo Semiconductor Inc. et al. v. TE Connectivity PLC, No. 2:25-cv-00297 (E.D. Tex.), filed March 13, 2025 (“the TE Connectivity Litigation”).

Credo Semiconductor Inc. et al. v. Volex PLC, No. 2:25-cv-00298 (E.D. Tex.), filed March 13, 2025 (“the Volex Litigation”).

b. District of Delaware

Credo Semiconductor Inc. et al. v. Molex, Inc., No. 1:25-cv-00316 (D. Del.),
filed March 13, 2025 (“the Molex Litigation”).

3. United States International Trade Commission

In re Certain Active Electrical Cables and Components Thereof, Inv. No.
337-TA-3814, complaint filed March 13, 2025.

C. Counsel and Service Information - §§42.8(b)(3) and (4)

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A power of attorney is submitted with the Petition. Counsel for Petitioners
consent to service of all documents via electronic mail.

Petitioner Amphenol Corporation requests *inter partes* review and cancellation of claims 1-19 (“Challenged Claims”) of U.S. Patent No. 11,032,111 (EX1001, “the ’111 Patent”).

I. INTRODUCTION

The ’111 Patent concerns communication methods, communication links, and transceivers that “pre-equalize” high data rate communication signals to mitigate distortion in a transmission channel. Pre-equalization is done by filtering a signal before transmitting it. Filter coefficients set the filter behavior. The filtering compensates for channel distortion.

The ’111 Patent claims storing filter coefficients for more than one channel, then picking a set of coefficients and using them in pre-equalization. It was well-known to store filter coefficients associated with a particular channel and use those coefficients for pre-equalization. **Ground 1** shows that Lugthart-706 in view of Das Sharma and Mezer renders obvious all claims of the ’111 Patent.

The Petition shows a reasonable likelihood that at least one ’111 Patent claim is unpatentable. Accordingly, Petitioner requests that the Board institute IPR and cancel the Challenged Claims.

II. STANDING CERTIFICATION

The ’111 Patent is available for IPR. Petitioner is neither barred nor estopped from requesting IPR of the ’111 Patent. 37 C.F.R. §42.104(a).

III. UNPATENTABILITY GROUNDS

The Challenged Claims are unpatentable as follows:

Ground	Reference(s)	Claims	Basis
1	Lugthart-706, Das Sharma, Mezer	1-19	§103

Post-AIA law applies because the '111 Patent's earliest effective-filing date is after March 16, 2013. The '111 Patent issued from an application filed August 27, 2019 (EX1001, code (22)) and purports to claim priority to a provisional application filed August 28, 2018 (*id.*, 1:8-12). The references are prior art to each Challenged Claim under post-AIA §102(a) even assuming an effective filing-date of the provisional application:

Reference	Published	Priority	Filing
Lugthart-706 (EX1005)	2018-01-30	2013-12-27	2016-12-28
Das Sharma (EX1006)	2014-09-18	None	2013-03-15
Mezer (EX1007)	2005-05-26	None	2003-11-24

IV. '111 PATENT¹

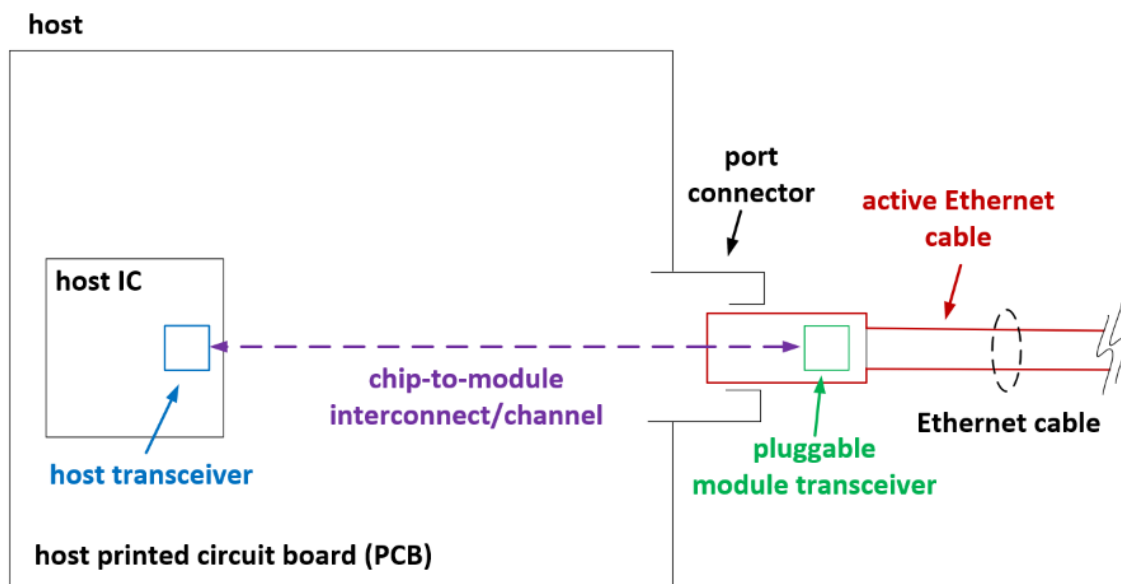
A. Background

The '111 Patent concerns high data-rate communication links connecting local area network ("LAN") nodes (*e.g.*, computers). EX1001, 1:19-35, 2:54-67,

¹ Unbolded italics indicate claim language herein. All other emphasis are added unless otherwise indicated.

Fig. 1 (links 110). The '111 Patent describes “chip-to-module” links and “pluggable modules” used in such links. EX1001, 11:26-31, claims 8, 11, 16.

A routing network often connects hosts—e.g., switches and routers—using active cables. EX1001, Fig. 1 (routing network 106, equipment items 108), 2:54-67; EX1003, Declaration of Paul S. Min, Ph.D. (“Min”), [0059]. A host typically has an integrated circuit (“IC”), comprising a transceiver, mounted on a printed circuit board (“PCB”). A host PCB electrically connects the host IC with a port connector compatible with an active cable’s “pluggable module.”



The pluggable module’s transceiver communicates with a transceiver (the “host transceiver”) within the host IC. Min, [0060]; EX1001, 5:10-23, claim 8; Lugthart-706, 10:17-22, 12:1-6, 15:5-10, FIG. 2A. Coupling the pluggable module to the port connector provides electrical connection and forms a channel between

the cable and the host IC. Min, [0059]; EX1001, claim 8, 5:10-23; Lugthart-706, 15:25-52. The port connector can electrically connect the host transceiver in different ways (*e.g.*, via copper traces of varying length on the PCB). EX1001, 4:52-64, 11:38-46, 12:1-36; Min, [0060]. The channel comprises the entire transmission medium between the host transceiver and the pluggable module transceiver. Min, [0060].

The channel between a host transceiver and a pluggable module transceiver was known as a “chip-to-module” (“C2M”) channel or link. Min, [0061]; EX1001, 5:24-30; EX1027 (“802.3bs”), §120E; EX1028 (“OIF-CEI-04.0”), 309, lines 3-5; EX1032, 15 (“Interconnect Applications... Chip-to-module” figure showing chip-to-module communication link for both copper and fiber optic interconnects, below), 17 (“3.4 Chip to module”), Fig. 8 (showing “Chip to Module Interconnect Application Space” annotated below); *see also* EX1011 (“Zerbe-058”), 1:26-28 (PCI Express could provide host’s electrical interconnect in C2M link).

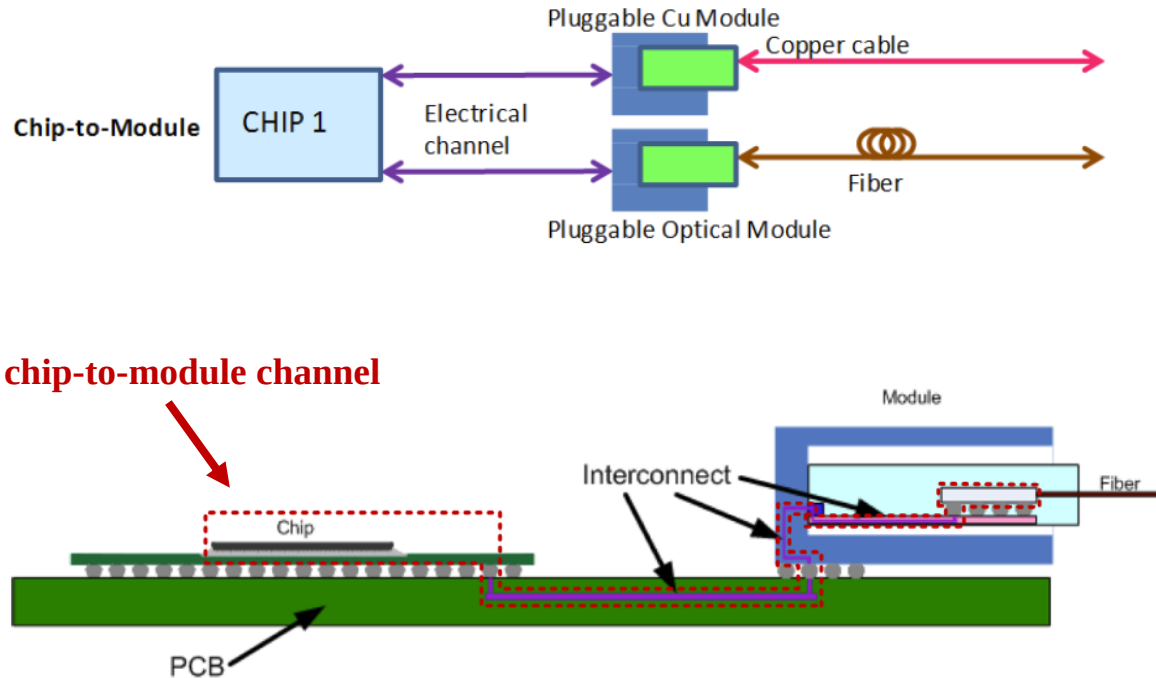


Figure 8 Chip to Module Interconnect Application Space

The C2M channel may distort signals transmitted between the pluggable module transceiver and the host transceiver “due to the physical channel’s introduction of noise, attenuation, and signal dispersion.” EX1001, 5:20-23; *see also* EX1008 (“Raghavan”), 2:24-34; Min, [0062]-[0063].

A common technique for mitigating this distortion was “pre-equalization”—also termed “pre-emphasis”—wherein a transmitter pre-distorts the signal in a manner that compensates for the anticipated channel-induced distortion. Raghavan, 2:39-41; EX1001, 6:40-43; Min, [0064]. Pre-equalization was implemented by filtering the signal before transmission. Min, [0064]; Lugthart-706, 9:38-51; EX1001, claim 8; OIF-CEI-04.0, 310, lines 8-11. These filters were configured by applying programmable coefficient values specifying the signal

modifications that would compensate distortion in the C2M channel. Min, [0064]; Lugthart-706, 22:13-17; EX1001, 7:43-59.

One known type of pre-equalization was “adaptive.” Min, [0065]; EX1001, 7:43-59; Mezer, 2:47-50; Das Sharma, [0079]-[0080]. **Adaptive** pre-equalization involved modifying the pre-equalization filter coefficients based on feedback from a receiver, e.g., transmitting a signal and measuring deviation (or “error”) from expected signal values received at the far end of the communication channel. Min, [0065]; Das Sharma, [0081]; EX1001, 7:43-59. From the measured deviation, the transmitter filter coefficient values are adjusted to improve distortion compensation. Min, [0065]; Das Sharma, [0081]; EX1001, 7:43-59. Adaptation can be repeated until the measured error becomes acceptably low. Min, [0065]; Das Sharma, [0081]; EX1001, 13:46-64.

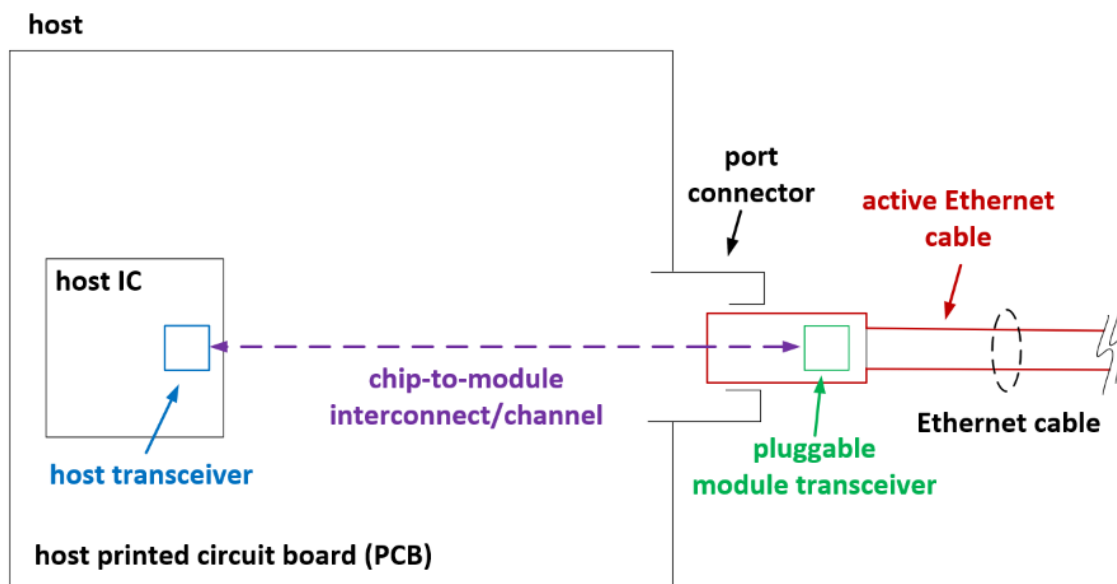
During adaptive training, the transmitter learns about the deviation between the known training signal and the received signal through a “backchannel” communication from the receiver, then implements pre-equalization using new coefficient values improve the distortion compensation. Min, [0066]; Das Sharma, [0078], [0081], Fig. 5; EX1001, 14:57-65.

B. Embodiments

The '111 Patent describes a serializer-deserializer (“SerDes”) architecture. EX1001, 1:39-40. In a SerDes architecture, used by Ethernet and other protocols,

data is converted between a serial and parallel data stream. Min, [0067];
Raghavan, 1:36-38; EX1024, 632; EX1001, 1:42-48. The '111 Patent purports to
implement “an efficient adaptation interface for transmitter pre-equalizers” for a
C2M link in a SerDes architecture. EX1001, 1:39-42.

POSAs knew that when designing a chip with embedded SerDes interfaces it
was necessary to incorporate mechanisms for adapting the SerDes in different
channel environments because it was not possible to know the exact environments
in which the chip would be used. Min, [0068]. The '111 patent calls this prior art
technique adaptive pre-equalization. Min, [0068].



The '111 Patent describes different channel models for different types of
devices that can receive a cable’s pluggable module. EX1001, 11:53-12:15.
Between the pluggable module transceiver and the host transceiver the channel

characteristics can vary widely (e.g., length of the channel, surrounding electronic components that may generate noises and interference), and different channel types distort the transmitted signal differently. Min, [0069]. Different default pre-equalization coefficients for the different channel models are stored in registers and are “expected to provide a good starting point for training/adaptation” of the transmit pre-equalizers. EX1001, 12:63-13:2, 13:22-24.

Storing various “channel models” including different “default [pre-equalization] coefficient values” for different channel types makes the adaptive pre-equalization process more efficient. EX1001, 12:16-58. When coupling a “pluggable module” (e.g., on a cable) to a host, the appropriate channel model can be selected. EX1001, 14:12-35. The selected channel model’s stored equalization coefficients provide initial values for the adaptive pre-equalization process. EX1001, 13:22-24. This well-known approach requires fewer training iterations because the initial values are well-suited to compensate for distortion in the type of channel to which the pluggable module has been connected. EX1001, 13:22-26; Min, [0072].

C. Challenged Claims

The ’111 Patent has 19 claims. Claims 1, 8, 11, and 16 are independent. Appendix A provides a claim list. Claim 1 is representative. It recites a communications method performed *in a transceiver* comprising three limitations:

- [1.a]: *selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;*
- [1.b]: *updating the initial pre-equalizer coefficient values during a training phase; and*
- [1.c]: *using the updated pre-equalizer coefficient values to convey a transmit data stream.*

Every Challenged Claim requires using a set of initial pre-equalization coefficients selected from among different sets of stored pre-equalization coefficients.

D. Prosecution History

The '111 Patent issued from application no. 16/552,927. The Examiner rejected all original independent claims as obvious over Kolze (EX1018) and Thirumoorthy (EX1019), but indicated that dependent application-claim 2—reciting “each of the multiple registers” storing initial pre-equalization coefficient values “corresponds to a different channel model”—contained allowable subject matter. EX1002, 88, 94, 212. Applicant substantively incorporated this limitation in each independent claim and the Office allowed the application.²

² Applicant rewrote original dependent claim 2 as an independent claim that issued as claim 1. EX1002, 77.

E. POSA

On August 28, 2018, a person having ordinary skill in the art (“POSA”) would have had a Bachelor of Science in electrical or computer engineering with at least three years of experience in digital communication system design. Min, [0050]-[0057]. A higher level of education may substitute for less experience. *Id.* A POSA’s level of skill would not have differed materially between August 28, 2018 and August 27, 2019. *Id.*

V. CLAIM INTERPRETATION

The Board construes claim terms using the civil action standard (35 U.S.C. §282(b)) consistent with the ordinary and customary meaning as understood by a POSA. 37 C.F.R. §42.100(b). The Board need only construe terms to the extent necessary to resolve disputes. *Nidec v. Zhongshan*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); 83 Fed. Reg. 51340, 51353. Because the prior art meets the claims under any reasonable interpretation the Board need not reach an exact outer construction for any term.

VI. GROUND 1: LUGTHART-DAS SHARMA-MEZER RENDERS OBVIOUS CLAIMS 1-19

A. Lugthart-706

Lugthart-706 discloses an “active cable” that “includes... first and second transceiver assemblies 105a, 105b positioned at either end of [] conductive lines

111.” Lugthart-706, 14:30-34, Fig. 2A (reproduced below). An active cable’s electronic components improve signal quality. Lugthart-706, 14:29-31.

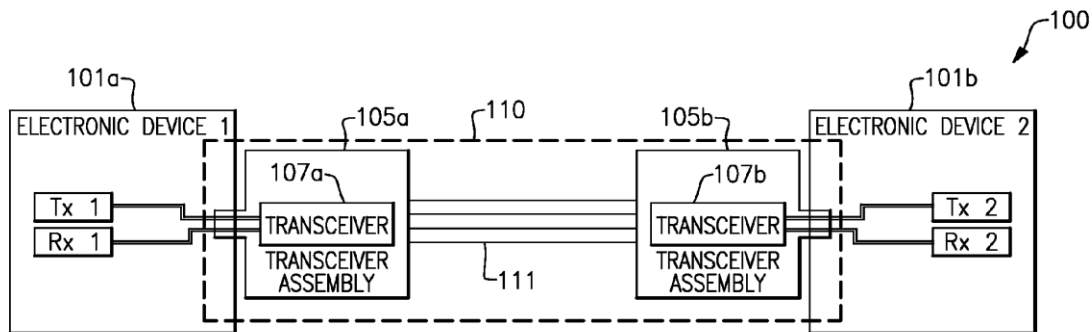
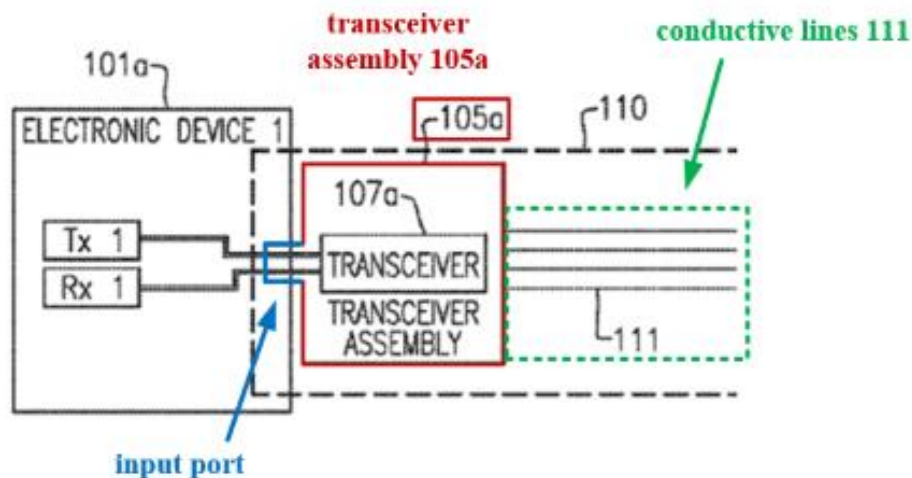


FIG.2A

The transceiver assemblies 105a, 105b include transceivers 107a, 107b, respectively. Lugthart-706, Fig. 2A, 14:47-53. Each transceiver assembly has a “host side” electrically connected to a host (termed an “electronic device”) and a “line side” electrically connected to one end of the cable’s conductive lines 111. Lugthart-706, 14:34-38, Fig. 2A (annotated detail below).

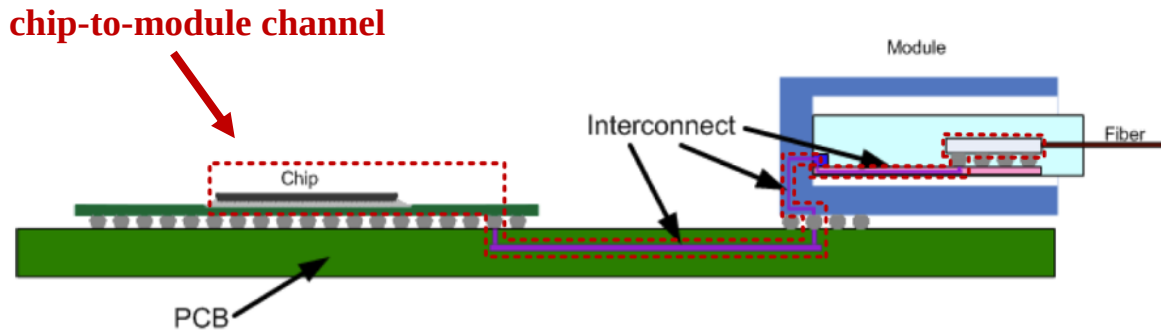


Lugthart-706, Fig. 2A (annotated detail)

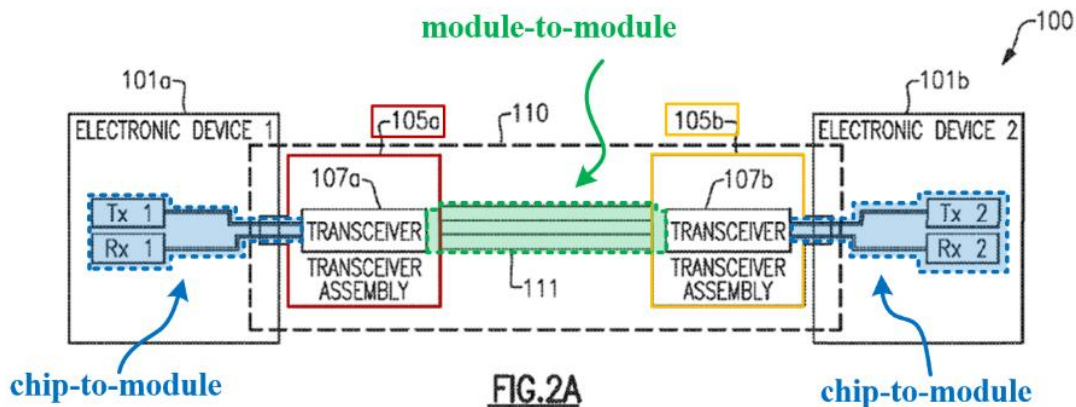
Each transceiver assembly's input port comprises a connector, such as an industry standard SFP or QSFP connector, that "is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable." Lugthart-706, 15:42-52, Fig. 2A; Min, [0082].

Lugthart-706 describes implementing transceivers 107a/107b on separate ICs. Lugthart-706, 15:31-36. Lugthart-706's transceivers 107a/107b provide signals "to one or more additional *transceivers... on the host side*," so that Lugthart-706 describes electronic device 101a having a host transceiver comprising an IC providing transmit (Tx 1) and receive (Rx 1) functionality. Lugthart-706, 8:61-9:1, 10:17-22; Min, [0083]. Electronic device 1's host transceiver transmits signals to, and receives signals from, pluggable module transceiver 107a. Electronic device 101b similarly has a chip comprising a host transceiver that transmits signal Tx 2 and receives signal Rx 2. Min, [0083].

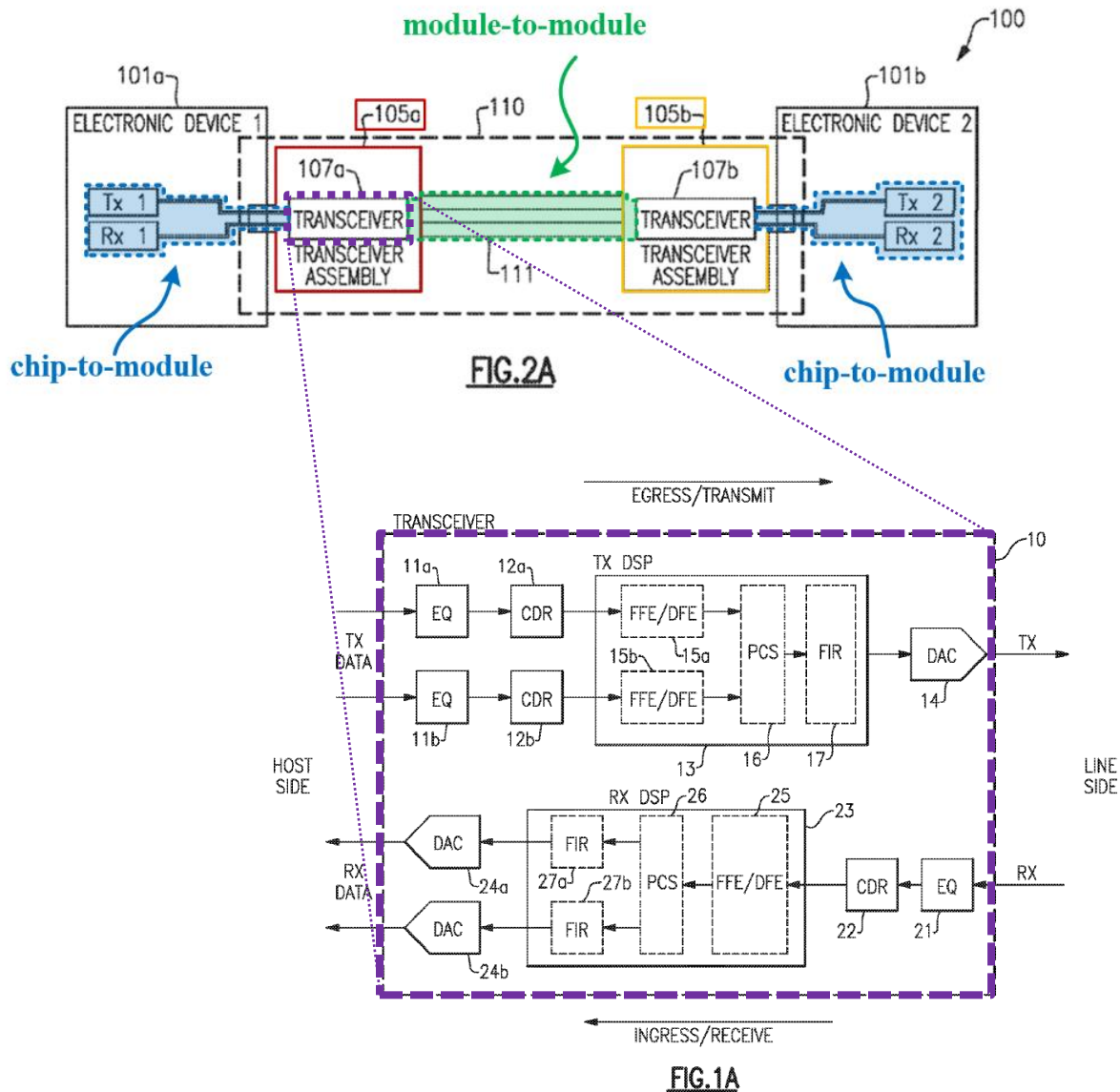
Lugthart-706's active cable comprises *three* communication links (depicted below): (1) a C2M channel between electronic device 101a's host IC and transceiver 107a; (2) another C2M channel for 101b to 107b; and (3) a module-to-module channel comprising transceiver 107a / conductors 111 / transceiver 107b. Min, [0083].



EX1032, Fig. 8



Lugthart-706's transceiver 107a/107b performs pre-equalization (which Lugthart-706 calls pre-emphasis) on signals transmitted *to the host IC* in the electronics device 101a/101b. Lugthart-706, 29:23-28. Figure 1A's transceiver 10 illustrates one embodiment of Figure 2A's pluggable module transceiver 107a/107b. Lugthart-706, 14:47-53; Min, [0084].



Lugthart-706 labels *communication paths* and *data signals* from the *host's* perspective: for a transceiver 10 the adjacent electronic device (host transceiver) *originates* the “EGRESS/TRANSMIT” path while it *terminates* the “INGRESS/RECEIVE” path. Thus, the “EGRESS/TRANSMIT” path carries data from electronic device 101a/101b (on the transceiver’s “host side”) and transmitted to conductive lines 111 (on the transceiver’s “line side”), whereas the

“INGRESS/RECEIVE” path carries data received from conductive lines 111 (on transceiver’s “line side”) and transmitted to electronic device 101a/101b (on the transceiver’s “host” side). Lugthart-706, Fig. 1A, 8:13-32, 8:50-60; Min, [0085].

A port connector couples the transceiver 10 (107a/107b) “host side” to the host transceiver on the electronic device 101a/101b. Lugthart-706, 15:42-52, Fig. 2A; Min, [0082]. The transceiver’s “line side” connects the cable’s conductive lines 111. Lugthart-706, Figs. 1A, 2A (showing lines 111), 8:13-32, 14:12-15 (“electronic devices 101a, 101b” are “referred to herein as host devices”); Min, [0085].

Transceiver 10’s “INGRESS/RECEIVE” path through DSP 23 performs digital signal processing on the ingress/receive signal before that signal is transmitted to the host (electronic device 101a/101b in Figure 2A). Lugthart-706, 8:26-32, 9:38-51, Fig. 1A; Min, [0086]. DSP 23 includes “finite impulse response (FIR) filter[s]” 27a/27b. Lugthart-706, 9:38-46.

DSP 23 uses these FIR filters for “adaptive and configurable signal conditioning features such as... **output pre-emphasis**” on the signal **transmitted to the host**. Lugthart-706, 9:52-55, 29:23-28. “Pre-emphasis” and “pre-equalization” were used interchangeably in the art. Min, [0086]; Raghavan, 2:39-41 (describing a “technique for combating ISI [inter-symbol interference]... known as ‘pre-emphasis’, or pre-equalization”); EX1009 (“Schmidt”), 7:54-55; EX1010 (“Zerbe-

063”), 3:24-27; EX1013 (“McCall”), 5:4-8. The pre-equalization compensates for anticipated channel distortion on a transmitted signal. Min, [0086]. This anticipated distortion is largely attributed to the limited bandwidth of the channel, wherein the relatively high frequency portion of signals is likely to be attenuated, and pre-equalization pre-distorts the signals by amplifying the higher frequency signal content. Min, [0086].

Lugthart-706 also describes signal conditioning for “output pre-emphasis” for FIR filter 17 in the egress/transmit path DSP 13, which that conditions signals transmitted to the line side. Lugthart-706, 29:23-28; Min, [0087]. Lugthart-706 configures FIR filters using “tap coefficients,” and the filters “perform emphasis on the signal to compensate for channel losses.” Lugthart-706, 22:13-16, 23:59-64; Min, [0087].

Lugthart-706 explains that the ingress/receive “DSP 23 can include componentry implementing similar functionality to the componentry in the egress path,” thereby indicating that—like FIR filter 17 in DSP 13—FIR filters 27a/27b in DSP 23 are also configured using “tap coefficients,” and also “perform emphasis on the signal to compensate for channel losses.” Lugthart-706, 23:21-23, 23:59-64; Min, [0087].

Lugthart-706 describes a “full speed training phase” during which data is transmitted over the communication channel and “parameters”—including

“operating parameters for the equalizers”—are “adjusted.” Lugthart-706, 48:64-49:19. POSAs understood that this describes adaptive equalization and adjusting equalization parameters for all of Lugthart-706’s equalizers, including for FIR filters 27a/27b of DSP 23 that pre-equalize signals transmitted to the host transceiver. Min, [0088]; Lugthart-706, 23:21-23, 23:59-64, 48:64-49:19.

B. Das Sharma

Das Sharma discloses *adaptive* pre-equalization to fine-tune pre-equalization coefficients. Das Sharma, [0075], [0080]; Min, [0089]. Das Sharma stores pre-equalization coefficients in registers on the transmitter side. Das Sharma, [0078], [0106]; Min, [0089]. Das Sharma uses these adaptive pre-equalization techniques for PCI Express applications, a widely practiced SerDes method and one of the protocols that Lugthart-706 explicitly supports. Das Sharma, [0038], [0069]; Lugthart-706, 16:33-36; Min, [0089].

More specifically, Das Sharma describes “a link training and equalization procedure” in which “a set of coefficients” is “applied to [the] transmission logic” of the transceiver. Das Sharma, [0066]. The set of coefficients is “applied to a finite impulse response (FIR) filter” in transmission logic of the transceiver to apply pre-emphasis before signal transmission. Das Sharma, [0079]; Min, [0090]. Das Sharma explains that “a lower bit error rate may be achieved in a channel of a

communications link... when an optimized set of coefficients are applied to” the transceiver’s “transmission logic.” Das Sharma, [0089].

Das Sharma stores “a set of default coefficients located within registers of the transmitter” that “may be applied to the transmission... logic.” Das Sharma, [0078], [0106]. Das Sharma refers to each register storing coefficient data as a “coefficient register table.” Das Sharma, [0078]. During operation, the default coefficients (also referred to as “pre-sets”) “are requested from the configuration registers” and applied to the transmitter’s pre-emphasis filter. Das Sharma, [0086]-[0088], [0136], [0155].

As discussed *supra* §IV.A, adaptive pre-equalization was a well-known process whereby (1) training signal(s) are transmitted to the receiver from the transmitter, (2) the receiver compares the received signal(s) to the known good training signal(s) and determines an error, (3) the equalization coefficients are adapted (i.e., modified), in the receiver or the transmitter, to reduce the error, (4) this continues iteratively until the received signal has an acceptable error such as, e.g., a target bit error rate (“BER”), and (5) the adapted coefficients are adopted for use in equalizing signals transmitted over the channel from the transmitter to the receiver. Min, [0092]; Das Sharma, [0081]; EX1016 (“Sun”), 1:62-2:40 (describing adaptive pre-equalization). In Das Sharma’s process, “Once the target

BER is achieved, no new coefficients are generated and applied to the transmission... logic[.]” Das Sharma, [0081].

Thus, Das Sharma teaches that pre-equalization coefficients may be optimized during a training process during which the settings of “a transmitter or receiver component” are “adjusted, optimized, etc.” to “achieve communication capability... with minimal data loss.” Das Sharma, [0075].

C. Mezer

Mezer discloses an equalization process that uses “a set of coefficients” that Mezer calls “equalizer characteristic[s].” Mezer, 3:64-4:7, 7:4-15 (“‘equalizer characteristic’ shall be understood to include a set of coefficients such as a set of filter coefficients”); Min, [0094]. “[V]arious types of channels may be tested in advance to determine suitable FFE [Feed-Forward Equalizer] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected.” Mezer, 6:53-57; *see also* 3:33-4:42 (describing the process for pre-computing the various sets of coefficients); Min, [0094]-[0095]. A POSA would have understood that Mezer teaches that different initial “set[s] of coefficients” can be “pre-computed” for different types of channels and those different sets of coefficients can be “stored in [a] storage unit.” Min, [0096]; Mezer, 4:4-15.

“Selection of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to virtually ***any communication channel*** that has an impulse response that varies with a physical characteristic,” including a C2M channel. Mezer, 6:62-7:3; Min, [0095]-[0097].

D. The Lugthart-Das Sharma-Mezer Combination

1. Reasons to Combine with a Reasonable Expectation of Success

a. Modifying Lugthart-706 to Use an Adaptive Pre-equalization Process With Coefficients Stored in Registers as Taught by Das Sharma

Lugthart-706 describes training phases. Lugthart-706, 47:55-60. During training, signals are transmitted over the communication channel and “parameters” are “adjusted,” including “operating parameters for the equalizers.” Lugthart-706, 48:65-49:12. POSAs understood that this describes adaptive equalization. Min, [0098]-[0101]. While Lugthart-706 is not explicit about which of the equalizers has its parameters “adjusted” during training, POSAs understood that Lugthart-706 describes adjusting the equalization parameters for any, or all, of Lugthart-706’s equalizers, including FIR filters 27a/27b of RX DSP 23 in Lugthart-706’s transceiver assembly that performs pre-equalization on signals transmitted to the host transceiver as discussed *supra* §VI.A. Lugthart-706, 23:21-23, 23:59-64, 48:65-49:12; Min, [0101].

To the extent Lugthart-706 is read to not expressly disclose using adaptive pre-equalization to adjust pre-equalization coefficients for FIR filters 27a/27b of RX DSP 23 in Lugthart-706's transceiver assembly, Das Sharma would have motivated a POSA to have implemented Lugthart-706 in that manner. Min, [0102]. Das Sharma teaches adaptive pre-equalization used in the same type of PCI Express protocol that Lugthart-706 describes. Das Sharma, [0038], [0069]; Lugthart-706, 16:33-36; Min, [0102]. Das Sharma stores an initial set of pre-equalization coefficients in registers of the transceiver on the transmitter side (Das Sharma, [0078], [0106]) and performs an adaptive pre-equalization process that optimizes the pre-equalization coefficients during a training process to "achieve communication... with minimal data loss." Das Sharma, [0075]; Min, [0102].

Lugthart-706 Figure 2A shows that Lugthart-706 specifically contemplates the using conductive lines 111 to connect transceiver assemblies 107a and 107b. A POSA would have known that Lugthart-706's cable assembly 110 in Figure 2A would be assembled during the manufacturing process. Min, [0103]. As such, the characteristics of the channel formed by conductive lines 111 connecting transceiver assemblies 107a and 107b would be largely determined during the manufacturing process, while surrounding factors such as the interference from other proximate conductors, transceiver electrical noise, or changes in cable

electrical conductivity from, e.g., temperature or humidity variations, would perturb the channel characteristics. Min, [0103].

POSAs knew that storing default pre-equalization parameter values determined during the manufacturing process was convenient and even essential for certain operating environments that made adaptation impractical. Min, [0104]. Storing default values also improves the cable assembly's boot-up speed as the pre-equalization adjusts incrementally from the default values, e.g., the training sequence, and need only account for deviations incurred during actual cable assembly use. *Id.*

If Lugthart-706 is not understood as describing an adaptive pre-equalization process, then POSAs had multiple reasons to modify Lugthart-706 to make Lugthart-706's pre-equalization process adaptive and to store the initial set of pre-equalization coefficients in a set of registers. Min, [0105].

First, Das Sharma expressly teaches the benefits of using an adaptive pre-equalization process that optimizes the pre-equalization coefficients to the particular channel, thereby achieving communication “with minimal data loss.” Das Sharma, [0075]; Min, [0106]. POSAs understood that an adaptive pre-equalization process, like Das Sharma's, enables optimizing coefficients for the current characteristics of a particular channel, thereby compensating for changes in the operating environment (*e.g.*, temperature) that may alter the channel

impairments (*e.g.*, distortion) affecting transmitted signals. Min, [0106]; EX1012 (“Zerbe-835”), 3:51-64 (pre-equalization coefficients “can be adapted periodically during system operation to account for changes in the system environment that may impact performance”). Das Sharma also expressly teaches storing initial pre-equalization coefficients in a set of registers. Das Sharma, [0078], [0106]; Min, [0106]. POSAs would have used Das Sharma’s teachings to make Lugthart-706’s pre-equalization process adaptive and to store an initial set of pre-equalization coefficients in a set of registers, which are specific memory locations that the processor(s) performing the pre-equalization can access quickly and conveniently. Min, [0107].

Second, adaptive pre-equalization’s benefits for improving data transmission performance were well-known. Das Sharma, [0075], [0089] (optimizing the initial pre-equalizer coefficients based on channel conditions yields “a lower bit error rate” and thus “***increase[d] data transmission performance*** within [the] communication system[.]”); Min, [0108]; Schmidt, 10:40-11:2; Zerbe-835, 5:34-39; EX1017 (“Hsu”), 2:20-28.

Similarly, on-chip registers were a well-known storage medium that POSAs understood were desirable for storing coefficients in a digital signal processor (DSP) because values can be retrieved from registers more quickly than from other types of storage, which may require the specific address locations for access (as

opposed to the names typically associated with the registers, to which the software programs can point), thereby increasing the speed and flexibility of DSP operations. Min, [0109]; EX1021 (“Peddle”), 5:13-22 (registers permit “parallel and... immediate[]” access and allow “data to be accessed, processed, and transferred more efficiently”); EX1022 (“Pickett”), 1:41-52, 2:8-34 (operations by a processor on data stored in “registers... within the microprocessor” requires fewer clock cycles than operations on data stored in off-chip memory like DRAM).

POSAs would have been motivated to store Mezer’s pre-computed sets of coefficients in a coefficient register table as taught by Das Sharma, to reduce the size, cost, and complexity of implementing Mezer’s “lookup table.” Hsu, 1:38-41 (the “size, cost and complexity” of storing equalizer coefficients in a “lookup table” in memory may be “unacceptable”), 2:46-49 (addressing these concerns by storing equalizer coefficients in a “register array”); Mezer, 5:13-18; Das Sharma, [0075], [0078], [0106]; Min, [0110].

These well-known benefits of an adaptive pre-equalization process and storing coefficients in registers would have motivated a POSA to make Lugthart-706’s pre-equalization process adaptive and to store an initial set of pre-equalization coefficients in registers. Min, [0111].

Third, making Lugthart-706’s pre-equalization process adaptive and storing an initial set of pre-equalization coefficients in a set of registers meets multiple

rationales that are indicative of obviousness. *KSR v. Teleflex*, 550 U.S. 398, 417-421 (2007). This combination is a “mere application of a known technique [adaptive pre-equalization using initial coefficients stored in registers as taught by Das Sharma] to a piece of prior art [Lugthart-706] ready for the improvement” because Lugthart-706’s system was ready for the improved error rate reduction achieved by Das Sharma’s adaptive pre-equalization. *Id.*, 417; Min, [0112]; *supra* §§VI.A-B.

This also combines known elements (Lugthart-706’s pluggable module transceiver that performs pre-equalization and Das Sharma’s adaptive pre-equalization that uses initial coefficients stored in registers) to perform their same known functions to yield predictable results. *KSR*, 550 U.S. at 417 (“When a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious.”) (cleaned up); *see also Intel v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-1381 (Fed. Cir. 2023) (“There is a motivation to combine when a known technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the prior art elements according to their established functions.”) (cleaned up); *Intel v. Qualcomm*, 21 F.4th 784, 799–800 (Fed. Cir. 2021) (applying “known-technique” rationale); Min, [0113].

b. Modifying Lugthart-Das Sharma to Use Different Coefficients for Different Channel Models as Taught by Mezer

To the extent Lugthart-706 and Das Sharma do not disclose storing different initial pre-equalization coefficient values for different channel models, that was taught by Mezer.

Mezer's equalization process uses "coefficients" that Mezer also calls "equalizer characteristics." *Supra* §VI.C; Mezer, 3:64-4:7, 7:11-15; Min, [0115]. Mezer teaches that "various types of channels may be tested in advance to determine suitable FFE [Feed-Forward **Equalizer**] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected." Mezer, 6:53-57; *see also id.* 3:33-4:42 (describing process for pre-computing the various sets of coefficients); Min, [0115]. POSAs understood that a "feed-forward equalizer" was a type of equalizer that, like pre-equalization, improved communication by compensating for channel distortion, and thus the "equalizer characteristics" (coefficients) in Mezer are analogous to coefficients used in an adaptive pre-equalization process. Min, [0115]; Raghavan, 17:4-14. Thus, Mezer teaches that different initial "set[s] of coefficients" can be "pre-computed" for different channel types and "stored in [a] storage unit." Mezer, 4:4-7; Min, [0115].

POSAs understood that Mezer's teachings were applicable to the pre-equalization process performed by Lugthart-706 (as modified by Das Sharma in the manner described *supra* §VI.D.1.a). Min, [0116]. Mezer teaches that "[s]election of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to virtually ***any communication channel*** that has an impulse response that varies with a physical characteristic" and is explicit that this includes Ethernet channels. Mezer, 6:62-7:3. POSAs understood that Lugthart-706's *chip-to-module communications link* between the pluggable module transceiver and the host transceiver (*supra* §VI.A) is a "communication channel that has an impulse response that varies with a physical characteristic" as described by Mezer, because Lugthart-706's C2M link distorts transmitted signals in ways that vary with the physical characteristics of the channel as discussed *supra* §VI.A. Min, [0116].

Mezer's equalizer is on the receiver side of the communication channel rather than the transmitter side as in Lugthart-706 and Das Sharma, so Mezer's equalization is not ***pre***-equalization as in Lugthart-706 and Das Sharma. Mezer, 5:25-28; Lugthart-706, 23:21-23, 23:59-64, 48:65-49:19; Das Sharma, [0078], [0081], FIG. 5; Min, [0117]. However, POSAs understood that the below-discussed benefits Mezer describes of storing different initial equalization coefficients for different channel types (improved efficiency and/or using less

hardware) apply equally to pre-equalization performed on the transmitter side. Min, [0117]; Mezer, 5:40-55. Indeed, applying the same type of “lookup table” approach for initial pre-equalizer coefficients on the transmitter side was known. Min, [0118]; EX1014 (“Gotman”), 12:34-55, 13:56-59 (“a measurement of a channel condition... may be used to index a lookup table and obtain... coefficient[s]” for a transmitter-side pre-equalizer); EX1015 (“Burchardt”), 10:13-52 (initial pre-equalizer coefficients “can be pre-determined and stored in a memory of the driving circuitry,” for example “in a look-up table”); Zerbe-835, 9:67-10:2 (“a simple mapping table, which can be realized through a table-lookup ROM, RAM, or through firmware, can provide the means to set TX equalizer coefficients”); Das Sharma, [0078], [0106].

Thus, POSAs understood that Mezer’s teachings apply directly to Lugthart-706’s pre-equalization process (as modified by Das Sharma as described *supra* §VI.D.1.a). Min, [0119].

POSAs had multiple reasons to modify the above-discussed combination of Lugthart-706 and Das Sharma to store, in Das Sharma’s registers, different pre-computed pre-equalization coefficients for different channel models. Min, [0120].

First, Mezer expressly teaches the benefits of using different pre-stored pre-computed pre-equalization coefficients for different channel types with different channel characteristics. Mezer, Abstract, 5:40-56; Min, [0121]. If the adaptive

equalizer does not customize the initial coefficients to the channel type, “convergence of the adaptive equalizer may be slower than desirable.” Mezer, 1:16-18; Min, [0121]. Mezer explains that its use of different pre-computed coefficients for different channel types can be used in an adaptive equalization process that uses “conventional principles” like in Lugthart-706 and Das Sharma, but “because of the relatively high degree of equalization provided by the pre-computed FFE block 48, the adaptive FFE 52 may **converge more rapidly**, and/or may **require less hardware** (e.g., fewer gates) than would be the case” if initial equalization coefficients were used that were not pre-computed for the specific channel type. Mezer, 5:40-55; *id.*, 2:21-23 (FFE means “feed forward **equalizer**”); Min, [0121].

Thus, Mezer expressly teaches that using different sets of stored coefficients for different channel types can advantageously provide a more efficient adaptive training process that “converges more rapidly” to coefficients that yield an acceptable error rate and/or can use less hardware. Mezer, 5:40-55; Min, [0122]. One exemplary Mezer channel characteristic is the length of a cable used in the channel, because different cable lengths can distort the signal transmitted through the channel differently. Mezer, 3:32-4:22; Min, [0123]. POSAs understood that Mezer’s techniques are applicable to other variable channel characteristics, such as different PCB trace lengths between the host transceiver and the pluggable module

connector. Min, [0123]; Mezer, 6:50-53 (“selection of one of a number of stored pre-computed equalizer characteristics may be performed on the basis of a channel characteristic other than cable length”), 6:62-7:3 (Mezer’s techniques “may be performed with respect to virtually any communication channel that has an impulse response that varies with a physical characteristic”).

Thus, POSAs understood that channel characteristics can vary widely, so that the designers of the chips with SerDes typically characterize multiple different channel models and store the corresponding pre-equalization parameters as potential initial values for the adaptation process. Min, [0124]-[0125]. Mezer’s express teachings would have motivated a POSA to modify Lugthart-706 and Das Sharma to store different pre-computed pre-equalization coefficients for different channel models as initial coefficients for use in the adaptive pre-equalization process used by Lugthart-706 as modified by Das Sharma. Min, [0126]. A POSA would have stored the pre-computed initial pre-equalization coefficients in a set of registers in the same way Das Sharma describes for storing initial pre-equalization coefficients. Das Sharma, [0078]; Min, [0126].

Second, it was well-known that using initial pre-equalization coefficients that accurately estimate the impact of the channel “shorten[s] the training time” for the pre-equalizer, leading to less costly down time for training. Min, [0127]; Mezer, 5:40-55 (the adaptive training process converges more rapidly); Sun,

10:30-33, 2:33-40 (“if the initial coefficient value of equalizer is estimated accurately enough, the equalizer will nearly enter into the convergence state before training”), 2:33-40 (describing a “pre-loading technique of equalizer coefficient[s], which first writes a group of initial coefficient value pre-calculated (estimated) into the coefficient register of equalizer before the equalizer starts training process”), 10:47-11:7 (“the effect of equalizer coefficient pre-load of the present invention is much better than the prior art.”); Gotman, 12:34-55, 13:56-59; Burchardt, 10:13-52; Zerbe-835, 9:67-10:3; Das Sharma, [0078], [0082], [0106]; Mezer, 6:27-42.

It was also well-known that active cable systems like Lugthart-706’s could be plugged into different types of electronic devices 101a/101b with different types of communication links between the pluggable module connector and the host transceiver (Lugthart-706 Fig. 2A) and that the C2M link between the pluggable module’s transceiver and the host device’s transceiver could vary for different electronic devices and distort the signal differently. *Supra* §VI.A; Lugthart-706, 6:22-45; Min, [0128].

Thus, a POSA would have understood that storing different initial equalization coefficients, for different types of electronic devices that might be used with the cable, would increase the likelihood of selecting, for a particular device, initial coefficients that accurately estimated the C2M channel’s impact on the signal, thus desirably yielding an efficient training process. Min, [0129].

Third, modifying the Lugthart-Das Sharma pluggable module transceiver discussed *supra* §VI.D.1.a to store different initial sets of pre-equalization coefficients for different channel models meets multiple rationales indicative of obviousness. *KSR*, 550 U.S. at 417-421. Modifying the Lugthart-Das Sharma pluggable module transceiver to use different pre-equalization coefficients for different C2M channel models is a “mere application of a known technique [using different initial coefficients for different channel types as taught by Mezer] to a piece of prior art [Lugthart-706 as modified by Das Sharma] ready for the improvement” because the Lugthart-Das Sharma pluggable module transceiver was ready for the improvement of a more efficient pre-equalization training process that results from having different initial coefficients for different channel types. *Id.*, 417; Min, [0130]; *supra* §VI.D.1.a.

This combination is also nothing more than combining known elements (Lugthart-706’s pluggable module transceiver that performs pre-equalization, Das Sharma’s adaptive pre-equalization that uses initial coefficients stored in registers, and Mezer’s different initial equalization coefficients for different channel types) to perform their same known functions to yield predictable results. *KSR*, 550 U.S. at 417; *PACT XPP*, 61 F.4th at 1380-81 (discussing known technique improving similar devices in same way); Min, [0131].

c. A POSA Would Have Had a Reasonable Expectation of Success in Making the Lugthart-Das Sharma-Mezer Combination

A POSA would have reasonably expected success in making Lugthart-706's pre-equalization process adaptive and storing an initial set of pre-equalization coefficients in a set of registers as taught by Das Sharma. Min, [0132]; *supra* §VI.D.1.a. Adaptive pre-equalization was well-known. *Supra* §VI.B; Das Sharma, [0081]; Sun, 1:62-2:40; Min, [0132]. Based on these teachings in the art, POSAs understood how to use training signals to perform adaptive pre-equalization and to update an initial set of pre-equalization coefficients. *Supra* §VI.B; Das Sharma, [0081]; Sun, 1:62-2:40; Min, [0132]. A POSA further knew how to store initial and updated pre-equalization coefficients in registers because Das Sharma taught this (Das Sharma, [0075]-[0078]) and registers were a well-known storage medium for storing data in a digital signal processor like Lugthart-706's RX DSP 23. *Supra* §VI.D.1.a; Peddle, 5:13-22; Pickett, 2:8-34; Min, [0132].

A POSA also would have reasonably expected success in further modifying Lugthart-706 and Das Sharma to store different initial pre-equalization coefficients for different channel types as taught by Mezer. Mezer, Abstract, 5:40-56; Min, [0133]. Mezer teaches that initial equalization coefficients for different channel types can be computed and stored in advance. Mezer, 3:34-4:22; Min, [0133].

At least two techniques were known for how the Lugthart-Das Sharma-Mezer transceiver would determine which set of initial coefficients to use when the cable is plugged into a new host device.

First, Mezer teaches that the pre-computed equalizer characteristics may be selected based on cable length or “**on the basis of a channel characteristic other than cable length.**” Mezer, 6:27-28, 6:50-57. “Selection of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to **virtually any communication channel** that has an impulse response that varies with a physical characteristic.” Mezer, 6:62-7:3. “[W]hen it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected.” Mezer, 6:50-57. Min, [0134].

Lugthart-706 teaches a “startup-phase” when its active cable is installed between two electronic devices. Lugthart-706, 47:65-48:7, Fig. 2A. In the start-up phase, a “basic channel test may be performed... to **determine the channel parameters** such as, for example, loss, noise, dispersion, non-linearity, etc.” Lugthart-706, 48:20-23. To the extent Lugthart-706 suggests that this “channel test” tests the channel between the host transceivers in the electronic devices 101a/101b, POSAs understood that pluggable module transceivers 107a/107b could have been easily adapted to each perform a channel test for the channel

shown in red below between the pluggable module transceiver and its respective host transceiver in the electronic device 101a/101b into which the pluggable module transceiver's assembly is releasably plugged. Min, [0135]; *supra* §VI.A (describing Lugthart-706). This would have been well-within the POSA's capabilities as it would have simply involved implementing Lugthart-706's known "basic channel test" capability in the pluggable module transceiver because Lugthart-706's host transceiver already had this "basic channel test" functionality. Lugthart-706, 48:20-23; Min, [0135].

POSAs understood that Lugthart-706's "basic channel test" that "***determine[s] the channel parameters***" like "loss, noise, dispersion, non-linearity, etc." was a desirable way to select among Mezer's different sets of initial pre-equalization coefficients for different channel types. Lugthart-706, 48:20-23; Mezer, 6:50-7:3; Min, [0136]. During Das Sharma's adaptive equalization process, equalization coefficients are adjusted to compensate for these types of "channel parameters" like loss and noise. Min, [0136]; Das Sharma, [0066], [0075]-[0077], [0087]-[0089]. POSAs understood that these same channel parameters used to adapt pre-equalization coefficients to yield suitably low error in the received signal were desirable parameters to use to select an initial set of pre-equalization coefficients that best compensates for the channel's impact on the signal to make the training process "converge more rapidly, and/or... require less

hardware.” Mezer, 5:40-55, 6:27-33, 6:50-57; Das Sharma, [0081] (describing generating new coefficient values during the adaptive equalization process based on a measured bit error rate for the channel); Min, [0137].

Second, an alternative way to select from among the sets of pre-computed pre-equalization coefficients in Lugthart-Das Sharma-Mezer was to send a known test signal using each set, determine which set produced a received signal that most closely matched the known test signal, and select the set of coefficients that produced that closest matching signal. Min, [0138]; Mezer, 6:53-57 (selecting set of coefficients when channel type is determined); Das Sharma, [0081] (iteratively cycling through multiple sets of coefficients during the adaptive equalization process and determining a bit error rate for each one). This was well-within the POSA’s capabilities. Min, [0138]. It simply involves the pluggable module transceiver sending a known test signal using each set of coefficients, the port transceiver determining which received test signal most closely matches the known test signal using the same error evaluation techniques known for use in adaptive equalization (Das Sharma, [0081]), selecting the register with the coefficients that yielded the test signal with lowest error, and the pluggable module transceiver using the set of coefficients selected by the port transceiver. Min, [0138].

Whether the pluggable module transceiver or the port transceiver selects the register with the best performing coefficients was a POSA's design choice, as backchannel communication between the transceivers meant either transceiver could make the selection. Min, [0139]; *KSR*, 550 U.S. at 421 (“When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.”).

It was well-known to use backchannel communication between transceivers on opposite ends of a communications channel to implement equalization. *E.g.*, EX1023 (“Gorecki”), [0070]; EX1024, 473 (802.3-215, Clause 72, “§72.6.10.2.3 Coefficient update field: The coefficient update field carries correction information from the local receiver to the link partner transmit equalizer.”); Min, [0140]. The receiving host transceiver could use a backchannel communication technique to provide error information on each test signal to the transmitting pluggable module transceiver, which could use that error information to select the register with the coefficients that produced the lowest error. Min, [0140]. Alternatively, the receiving port transceiver could evaluate the error data and select the register with the coefficients that produced the lowest error and communicate that selection to the pluggable module transceiver using backchannel communication. Min, [0140].

Thus, a POSA would have had a reasonable expectation of success in implementing Lugthart-706's active cable to perform adaptive pre-equalization, store in Das Sharma's registers different initial pre-equalization coefficients for different channel types as taught by Mezer, and select from among those different coefficients the set best suited to the channel in which the cable is installed because this involved simply using known techniques and was well within a POSA's skill. Min, [0141].

2. The Resulting Lugthart-Das Sharma-Mezer Combination

The result of modifying Lugthart-706 based on Das Sharma and Mezer in the manner explained *supra* §VI.D.1 is an active cable system like the one shown in Lugthart-706's Figure 2A with transceiver assemblies 105a/105b and conductive lines 111 between them. In the combination, receive path (RX) DSP 23 (Lugthart-706, Fig. 1A) of Lugthart-706's transceiver 107a/107b is modified to store different sets of initial pre-equalization coefficients for different channel types as taught by Mezer, in registers as taught by Das Sharma, and to use an adaptive pre-equalization process as taught by Das Sharma. *Supra* §VI.D.1; Min, [0142]; Das Sharma, [0078], [0106], [0155]; Mezer, 6:53-57. The initial set of coefficients is selected based on channel characteristics, or by using each set of coefficients to send a test signal and selecting the set that produces the best result, as discussed *supra* §VI.B. Min, [0142]. Updated coefficients generated during the adaptive

training process provide “tap coefficient” values for FIR filters 27a/27b in Lugthart-706’s modified RX DSP 23. *Supra* §§VI.A-C. Min, [0142]; Lugthart-706, 9:38-51, 22:12-16, 23:59-64, 29:23-28.

The above-described active cable system that results from modifying Lugthart-706 based on Das Sharma and Mezer is hereafter referred to as “Lugthart-Das Sharma-Mezer.”

E. Lugthart-Das Sharma-Mezer Meets All Challenged Claims

1. Claim 1

a. Preamble

1.PRE	A SerDes communications method that comprises, in a transceiver:
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If [1.PRE] is limiting, Lugthart-Das Sharma-Mezer meets it.

A “SerDes” communications method converts data between serial and parallel data streams. Min, [0144]; Raghavan, 1:36-38; EX1001, 1:42-48; *supra* §IV.B.

Lugthart-Das Sharma-Mezer’s active cable system provides a “high-speed communication link between first and second electronic devices[.]” Lugthart-706, 14:7-31. The cable includes conductive lines 111 extending between transceiver assemblies 105a/105b that include “transceivers 107a, 107b, respectively.” Lugthart-706, 14:31-34, 14:48-50, Fig. 2A. Lugthart-706’s transceivers “implement a serializer/deserializer (SerDes) function” converting between parallel

data paths on the host-side and a serial data path on the line side. Lugthart-706, 7:6-20; Min, [0145].

The transceiver in Lugthart-Das Sharma-Mezer's active cable system performs each step in claim 1 (*infra* §§VI.E.1.b-VI.E.1.d), and thus performs a *SerDes communications method* meeting [1.PRE]. Min, [0145].

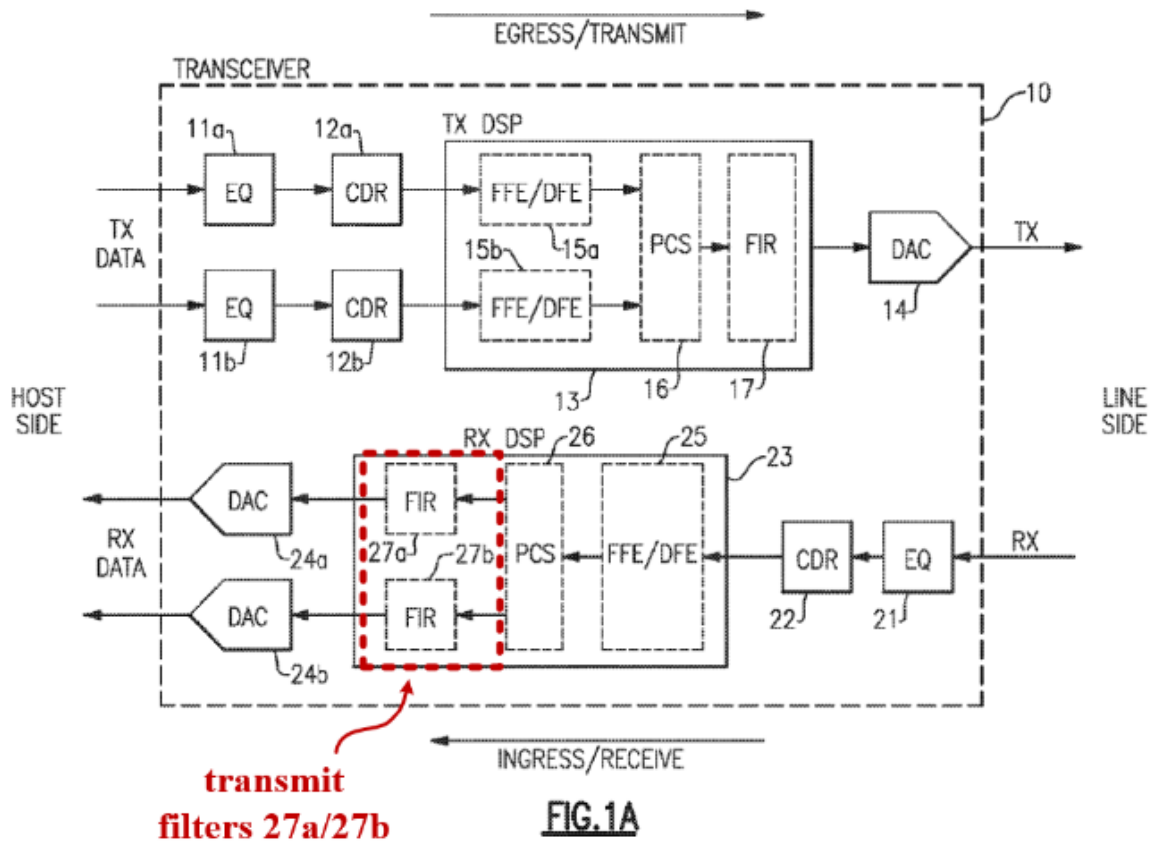
b. Limitation [1.a]

1.a	selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;
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Lugthart-Das Sharma-Mezer performs “*selecting one of multiple registers to specify initial pre-equalizer coefficient values.*” *Supra* §VI.D (describing the combination). Lugthart-Das Sharma-Mezer's transceiver provides “adaptive and configurable signal conditioning features such as... **output pre-emphasis.**” Lugthart-706, 29:23-28. POSAs understood that “pre-emphasis” and “pre-equalization” have the same meaning. Min, [0146]-[0148]; Raghavan, 2:39-41 (describing a “technique for combating ISI [intersymbol interference]... known as ‘pre-emphasis’, or pre-equalization”); Schmidt, 7:54-55; Zerbe-063, 3:24-27; McCall, 5:4-8.

Although *from the host's perspective* DSP 23 is on the “INGRESS/RECEIVE” path, Lugthart-Das Sharma-Mezer's DSP 23—including FIR filters 27a/27b—provides **pre-equalization** for the signal (“RX DATA”) that

transceiver 10 **transmits to** the host transceiver. Lugthart-706, Fig. 1A (annotated below), 9:38-51; Min, [0149].



Transmit filters 27a/27b condition the line side signal, which they provide to DACs 24a/24b for **transmission to the host side**. Lugthart-706, 23:3-13.

Lugthart-706 explicitly identifies “transmission line losses on the host side”

between the pluggable module transceiver and the host transceiver. Lugthart-706,

9:10-15; Min, [0150]. Lugthart-706 explains that FIR filter 17 in the

egress/transmit path “perform[s] emphasis on the signal to compensate for channel

losses” (Lugthart-706, 23:62-64) and notes that the “DSP 23 in the ingress path can

include componentry that is similar to the DSP 13 in the egress path.” *Id.*, 24:3-4;

see also id., 24:3-29 (explaining differences between DSP 23’s serial-to-parallel conversion and DSP 13’s parallel-to-serial conversion, but noting no difference in signal conditioning by the FIR filters); Min, [0150].

In Lugthart-706’s transceiver, equalizer 21 “compensate[s] for transmission line losses on the line side” in the ingress/receive data path (Lugthart-706, 9:10-12), and Lugthart-706’s pluggable module transceiver performs “**output pre-emphasis.**” Lugthart-706, 29:21-28; Min, [0151]. Thus, POSAs understood that Lugthart-706 describes FIR filters 27a/27b as performing “output pre-emphasis” to compensate for the transmission losses that Lugthart-706 describes on the host side between the pluggable module transceiver and the port transceiver. Lugthart, 29:21-28; Min, [0151].

To the extent Lugthart-706 is considered to not expressly disclose that FIR filters 27 in RX DSP 23 provide **pre**-equalization to compensate for transmission losses on the host side, that would have been a conventional and obvious way to implement what Lugthart-706 discloses. Min, [0152]. It was well-known that equalization can be performed on the transmitter side (i.e., pre-equalization) and/or on the receiver side and it was a design choice where to perform equalization. Das Sharma, [0085]; Mezer, 5:41-55; Hsu, 1:9-12, 2:1-7; Min, [0152]. A provider of an active cable like Lugthart-706’s had reasons to implement pre-equalization in the cable because this would ensure good cable performance irrespective of the

host device with which the cable is used. Min, [0152]; OIF-CEI-04.0, §16.2.2 (“16.2.2 Transmitter equalizer function: Both host and module Tx FIRs are likely to be required to meet... eye requirements... for high loss channels.”).

FIR filters 27a/27b use “**tap coefficients**” to control the output pre-emphasis functionality. Lugthart-706, 22:13-17, 23:21-23; Min, [0153]. In Lugthart-Das Sharma-Mezer, the transceiver’s pre-emphasis coefficients are adjusted during a training phase as taught by both Lugthart-706 (48:65-49:37) and Das Sharma ([0066], [0075]). *Supra* §VI.D (describing the combination); Min, [0153]. The set of coefficients adjusted during the training phase are applied to FIR filters 27a/27b in the RX DSP’s transceiver. *Supra* §VI.D (describing the combination); Min, [0153]; Das Sharma, [0079] (FIR filter uses adjusted coefficients).

Lugthart-Das Sharma-Mezer stores “a set of default coefficients located within registers” in the pluggable module transceiver as taught by Das Sharma, [0078], [0106]. *Supra* §VI.D (describing the combination). In Lugthart-Das Sharma-Mezer, “various types of channels may be tested in advance to determine suitable [pre-equalizer] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, **the suitable** [pre-equalizer] **characteristic for that type of channel may be selected**” as taught by Mezer. Min, [0153]-[0154]; Mezer, 6:53-57; *supra* §VI.D (describing the combination) and Mezer 3:33-4:42 (describing the process for pre-computing the

sets of coefficients), 4:24-26 (teaching “**selecting** one of the pre-computed equalizer characteristics” (i.e., sets of coefficients) “stored in the storage unit”), and 4:32-39 (describing a “**lookup table**” used “to select one of the pre-computed equalizer characteristics stored in the storage unit”). A POSA would have stored each coefficient set corresponding to a different channel model in a different register, so that on selecting the desired coefficient set they can be accessed by simply selecting the corresponding register. Min, [0154]. The pre-computed pre-equalizer coefficients stored in registers in Lugthart-Das Sharma-Mezer are *initial pre-equalizer coefficient values*. Min, [0154].

The ’111 Patent says that each *channel model* is provided based on assumptions of known or predicted link characteristics and that each channel model stores “default coefficient values” provided by the “the manufacturer of the pluggable module.” EX1001, 12:1-4, 12:54-13:8. That is precisely what the different sets of default coefficients for different channel types are in Lugthart-Das Sharma-Mezer. *Supra* §VI.D (describing the combination); Min, [0155]; Das Sharma, [0078] (describing default coefficients “provided by manufacturer”); Min, [0155]. Thus, the different sets of *equalizer coefficient values* stored in different registers in Lugthart-Das Sharma-Mezer for different channel types correspond to “*different channel model[s]*” in Limitation [1.a]. Min, [0155].

When the Lugthart-Das Sharma-Mezer active cable system is plugged into a host device, either (1) a channel test determines parameters of the channel between the cable's transceiver and the host's transceiver, or (2) a training signal is sent using each set of coefficients, and the best performing set is determined. *Supra* §VI.D (describing the combination); Lugthart-706, 48:20-22; Min, [0156]. The set of default coefficients that correspond to a channel having the parameters detected during the basic channel test, or the best performing set of coefficients, is *selected* and requested "from the configuration registers" (Das Sharma, [0155], Fig. 15) and then applied to the pre-emphasis FIR filters 27a/27b. *Supra* §VI.D (describing the combination); Min, [0156].

As discussed *supra* §VI.D (describing the combination), in Lugthart-Das Sharma-Mezer POSAs would have had a design choice for selecting the register with the desired initial coefficients can be made by the pluggable module transceiver or the host transceiver. Min, [0157]. Either option meets Limitation [1.a].

Accordingly, Lugthart-Das Sharma-Mezer's pluggable module transceiver or port transceiver meets [1.a]. Min, [0158].

c. Limitation [1.b]

1.b	updating the initial pre-equalizer coefficient values during a training phase; and
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Lugthart-706 teaches a “training phase” during which “operating parameters for the equalizers” are “adjusted.” Lugthart-706, 48:64-49:19, 49:20-34. Das Sharma also describes a “link ***training*** and equalization procedure” which is a training phase during which initial coefficients are “***adjusted.***” Das Sharma, [0066], [0075]; *see also* [0063] (it is “important to provide the capability to dynamically adjust the transmitter and receiver equalization settings”); Min, [0159]. “[O]nce the initial coefficients are computed...a new set of coefficients may be computed by ***adding a predefined constant or set of predefined constants to the computed set of coefficients***” at each iteration of the training phase. Das Sharma, [0124], [0136] (“multiple iterations may be performed to achieve the optimum link training and equalization transmitter...settings”). “[N]ew set[s] of coefficients” are “generated” and applied in an iterative fashion “until the target BER” (bit error rate) “is reached.” Das Sharma, [0081].

In Lugthart-Das Sharma-Mezer, *during a training phase*, as taught by Lugthart-706 and/or Das Sharma, the pluggable module transceiver 107a/107b that includes the registers storing different pre-equalizer coefficients *update[es] the initial pre-equalizer coefficients*, selected as discussed with Limitation [1.a], for

FIR filters 27a/27b to optimize those coefficients to reduce the error rate. See *supra* §VI.D (describing the combination); Min, [0160]; Das Sharma, [0063], [0066], [0075], [0081], [0124], [0136]; Lugthart-706, 9:38-51, 22:13-17, 23:21-23.

d. Limitation [1.c]

1.c	using the updated pre-equalizer coefficient values to convey a transmit data stream.
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Lugthart-Das Sharma-Mezer’s transceiver 107a/107b *us[es] the updated pre-equalizer coefficient values* generated during the training phase by applying them to transmit FIR filters 27a/27b in DSP 23 to process the “INGRESS/RECEIVE” data stream (*transmit data stream*) in Lugthart-706 Fig. 1A. *Supra* §VI.D (describing the combination); Min, [0161]. As explained *supra* §VI.A, Lugthart-706 names ***data streams*** from the adjacent host’s perspective, but this signal ***naming*** convention is irrelevant to filter 27a/27b’s ***function***, which is to condition signals ***for transmission*** over the C2M channel ***to the host transceiver***. Min, [0161].

FIR filters 27a/27b outputs are connected to DACs 24a/24b, respectively, that “include outputs that ***generate host side*** receive data (RX DATA)” which is a *transmit data stream* that is ***transmitted*** to the host device. Lugthart-706, 8:28-32; *supra* §VI.D (describing the combination); Min, [0161]. Thus, Lugthart-Das

Sharma-Mezer's pluggable module transceiver 107a/107b meets [1.c]. Min, [0161].

2. Claim 2

2	The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
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a. “C2M channel”

A “chip-to-module (C2M) channel” is a channel between a transceiver on a host IC and the transceiver on a pluggable module connected to a port on the device. *Supra* §§IV.A-IV.B; Min, [0162]-[0163]; EX1001, 5:24-30, 11:26-31 (describing the module side of a “C2M link” as implemented by a “**pluggable module**” such as a “**QSFP**” interface “that is inserted into a port in a host such as a switch or a router”); EX1032, 15 (“Interconnect Applications... Chip-to-module”), 17 (“3.4 Chip to module”), Fig. 8 (“Chip to Module Interconnect Application Space,” annotated below).

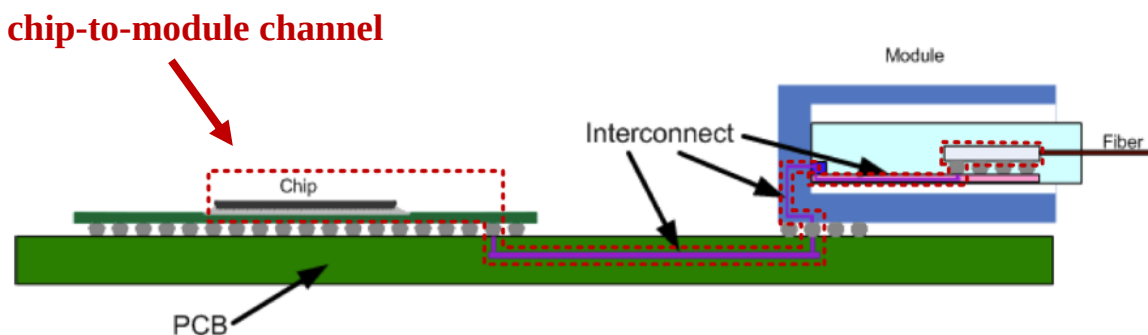


Figure 8 Chip to Module Interconnect Application Space

Lugthart-Das Sharma-Mezer meets claim 2 because Lugthart-706 teaches an active cable having a pluggable module that, when coupled to a host device, forms a *chip-to-module channel* between a host transceiver and the pluggable module transceiver. *Supra* §VI.D (describing the combination); Min, [0164]. Lugthart-Das Sharma-Mezer’s active cable system includes a “**QSFP** interface” which is a “**pluggable module**” and includes transceivers 107a/107b. Lugthart-706, 15:25-52 (active cable including transceivers 107a/107b in a host’s QSFP port-compatible connector), 50:34-59 (describing exemplary active cable comprising transceivers in QSFP interface), 51:64-52:5 (referring to QSFP interface as a “pluggable module”), FIG. 17A; Min, [0164].

Lugthart-706’s transceivers 107a/107b can send electrical signals to “one or more additional *transceivers... on the host side*” (host transceivers) in the electronic devices 101a/101b. Lugthart-706, 10:17-22; Min, [0165]. These signals can be sent “over **high loss PCB channels**” connecting the pluggable module transceivers 107a/107b and the host transceivers. Lugthart-706, 29:40-43; Min, [0165].

Lugthart-706 explains that “transceivers can be a monolithic device including analog and digital components **included in a single integrated circuit (IC)**, for example, or may instead include multiple integrated circuits.” Lugthart-706, 15:32-35. POSAs would have understood that Lugthart-706 described a host

transceiver in electronic device 101a/101b as comprising an IC, thus providing the “chip” for a C2M channel. Min, [0166]. Regardless, POSAs would have known that a conventional way to implement the host transceiver was with an IC mounted on the PCB in the host. Min, [0166]. Thus, in Lugthart-Das Sharma-Mezer, the “high loss PCB channel[]” that connects the host transceiver (an integrated circuit or “**chip**”) to the pluggable **module** transceiver 107a/107b is a “*chip-to-module (C2M) channel*.” Min, [0166]; Lugthart-706, 10:17-22, 15:25-52, 29:40-43, 50:34-59, 51:64-52:5.

To the extent “*chip-to-module (C2M) channel*” means a chip-to-module channel conforming to the 802.3-2015 Ethernet standard referenced throughout the ’111 Patent, Lugthart-Das Sharma-Mezer still meets claim 2 because Lugthart-706 describes, and conventional implementation supported, Ethernet communications over the PCB channel between the pluggable module transceiver 107a/107b and the host transceiver. Lugthart-706, 48:16-20; *see also id.* 16:24-26 (“conducting lines 111” can “reside on a PCB or other substrate”); Min, [0167].

b. “C2M channel insertion/package loss”

“*[I]nsertion loss*” refers to losses in signal strength from propagation through a channel, such as through the pluggable module’s port connection. Min, [0163], [0168]; EX1025 (“Newton’s”), 661; EX1026 (“Oxford”), 5. “*Package loss*” refers to loss attributed to the particular “integrated circuit package” or “PCB

layout” over which the signals travel. Min, [0168]; EX1001, 11:55-60; Oxford, 7 (“package” definition), 3 (definition of “dissipation (loss)”), 6 (“loss” definition refers to “dissipation”).

While Lugthart-706 does not expressly say that the “high loss PCB channels” on the host side have “*insertion loss*” and “*package loss*,” a POSA understood that this was so because it was well-known that there is *package loss* for signals exiting the pluggable module’s transceiver and entering the host device’s transceiver, as well as *insertion loss* as the signal propagates over the printed circuit board (PCB) between those transceivers. Min, [0169]; Lugthart-706, 29:21-37 (describing the use of signal conditioning features (*e.g.*, “output pre-emphasis”) to compensate for channel “insertion loss”), 15:25-42 (disclosing that the transceiver is “enclosed in a packaging” comprising “materials suitable for electronic and computer interfaces”).

Thus, POSAs understood that the host-side “loss” that Lugthart-706 describes compensating for using pre-equalization performed by the pluggable module transceiver includes both *insertion loss* and *packaging loss*. Min, [0170]; Lugthart-706, 29:21-43.

Thus, in Lugthart-Das Sharma-Mezer, the different chip-to-module channel models for which pre-equalizer coefficients are stored in registers include “*different channel models [] for chip-to-module (C2M) channels with different*

insertion loss and package loss characteristics” as in claim 2. Min, [0171]; *supra* §VI.D (describing the combination).

Alternatively, to the extent Lugthart-706 is considered to not expressly disclose compensating for insertion and package loss, a POSA would have had reasons for Lugthart-Das Sharma-Mezer’s pre-equalization to compensate for insertion and package loss, with a reasonable expectation of success, because these were well-known losses in a chip-to-module channel between an active cable’s transceiver and the host transceiver, which were routinely compensated for by the type of pre-equalization used in Lugthart-Das Sharma-Mezer. Min, [0172]; Lugthart-706, 15:25-42, 29:21-37; Kolze, [0060] (describing the use of equalization to compensate for different types of channel loss); Das Sharma, [0075] (same); *supra* §VI.D (describing the combination). Thus, an obvious implementation of Lugthart-Das Sharma-Mezer stores in its registers “*different channel models [] for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.*” Min, [0172]; *supra* §VI.D (describing the combination).

3. Claim 3

3	The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.
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Das Sharma describes pre-equalization “on a per *transmitter-receiver pair basis* to ensure interoperability” between the transmitter and the receiver in compensating for the channel’s distortion. Das Sharma, [0064]; Min, [0173]. It was well-known that receive equalization influenced the appropriate transmit equalization: “[i]deally, transmit and receive equalization work together to mitigate the degradation imposed by the channel, and thus allow increased data rates and/or reduced probability of communication errors.” Zerbe-835, 1:23-27; Min, [0174]. Thus, POSAs understood that when a particular host-side transceiver compensated for a particular distortion in a received signal, it was unnecessary for the pluggable module transceiver’s pre-equalization to compensate for that same distortion. Min, [0174].

Moreover, by avoiding pre-emphasis the transmitter could operate at lower power. Min, [0174]. Conversely, for a different host-side transceiver that was incapable of compensating for that same distortion in a received signal, it would be desirable for the cable-side transceiver’s pre-equalization to do so. Min, [0174]. POSAs also knew that transmitter pre-emphasis was desirable to compensate

channel distortion because it could mitigate noise enhancement wherein the receiver equalization boosts both received noise and signal. Min, [0174].

POSAs had reasons to implement the Lugthart-Das Sharma-Mezer combination so that *at least some of the different channel models presume different types of receiver equalization* to ensure interoperability between different transmitter-receiver pairs, to ensure that they each mitigate channel degradation as taught by Das Sharma and Zerbe-835. Das Sharma, [0064]; Zerbe-835, 1:23-27; Min, [0175].

A POSA would have had a reasonable expectation of success in implementing Lugthart-Das Sharma-Mezer in this manner because it required not using pre-equalization coefficients to compensate for some distortion that the host-side transceiver's equalization can compensate for. Min, [0176]. It was common practice for pluggable modules to be compatible with a range of hosts, such as prior generations or hosts with different performance levels. The proposed combination is an example of that, such that a POSA would have expected success. Min, [0176].

4. Claim 4

4	The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.
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Claim 4's antecedent is [1.a] *selecting one of multiple registers to specify initial pre-equalizer coefficient values...* (*supra* §VI.E.1.b), which recites a method performed *in a transceiver* (*supra* §VI.E.1.a ([1.PRE])). The '111 Patent describes testing each set of coefficients and selecting one that best performs best based on a performance characteristic such as “an error signal energy” or a “bit error rate.” EX1001, 2:4-5, 14:12-43, claims 5-6. The '111 specification's only description supporting claim 4's selection of the register with the best performing coefficients is Figure 8, steps 802-812, and 14:12-15:3. Min, [0177].

That disclosure describes actions by “training controller link or link controller” that receives test signals (steps 808 and 818) and selects the best performing register on a “**remote** transmitter” that transmitted the test signals. EX1001, 14:12-56; Min, [0178]. The “**remote** transmitter” is “instructed to use those preset coefficients” from a register selected in step 812 “as a starting point” and “programs the pre-equalizer with the preset coefficients from the selected register and transmits a training pattern and/or data.” EX1001, 14:38-43; Min, [0178].

Accordingly, claim 4 may be met by more than one transceiver, with at least one step (determining a performance characteristic for each register in claim 4) performed by a receive-side transceiver while another step (claim 1's conveying a transmit data stream) is performed by a transmit-side transceiver. Min, [0179]. *Baldwin Graphic Sys. v. Siebert*, 512 F.3d 1338, 1342-1343 (Fed. Cir. 2008). (“a transceiver” means one or more transceivers.) Thus, claim 1's method, as modified by claim 4, can be met by some steps performed by the pluggable module transceiver and others by the port transceiver in the above-discussed obvious implementation of Lugthart-Das Sharma-Mezer. Min, [0179].

As discussed *supra* §VI.D, in one obvious implementation of Lugthart-Das Sharma-Mezer, a selection is made from among the registers storing different sets of pre-computed pre-equalization coefficients by having the pluggable module transceiver send different instances of a test signal that were pre-equalized with the different set of coefficients, determining at the port transceiver which set of coefficients had the best performance characteristic (e.g., produced a signal with the smallest error), and then selecting (at either the pluggable module transceiver or the port transceiver) the set of coefficients that performed best. Min, [0180]; Mezer, 6:50-57 (describing determining a “channel type[]” to select between the different pre-computed channel models associated with different channel types);

Das Sharma, [0081] (describing testing multiple different sets of coefficients in an iterative fashion and determining a bit error rate for each).

That meets claim 4, and renders it obvious. Min, [0180].

5. Claim 5

5	The method of claim 4, wherein the performance characteristic is an error signal energy.
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Various performance characteristics were known for comparing a received signal to the known transmitted signal. Min, [0181]. Mezer “adapt[s]” equalizer coefficients “on the basis of *an error signal*” that “indicates deviation of the” received training signal “from a pre-determined ideal signal profile.” Mezer, 2:27-49 and 3:5-7; Min, [0181]. That meets the claimed “*error signal energy*.” Min, [0181]; EX1001, 14:29-30 (“measur[ing] error signals” represents “the difference between the equalized receive signals and an idealized receive signal”).

Furthermore, it was well-known in the art to use “*error signal energy*” as a performance characteristic for a control system. E.g., EX1029, [0160] (computing error signal energy); EX1030, 12:14-21, claims 2, 5, 14 (same); EX1031, 14:42-53 (same); Min, [0182]. Thus, an obvious implementation of Lugthart-Das Sharma-Mezer uses *error signal energy* as the performance characteristic to select among the registers storing different sets of pre-computed pre-equalization coefficients (*supra* §VI.D). Min, [0182].

6. Claim 6

6	The method of claim 4, wherein the performance characteristic is a bit error rate.
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Another known performance characteristic for comparing a received signal to a known transmitted signal was bit error rate. Min, [0183]. Das Sharma teaches the use of bit error rate and explains that it may be “the ratio of the number of bits incorrectly received (errors) and the total number of bits received.” Das Sharma, [0076]-[0077]. In another obvious implementation of Lugthart-Das Sharma-Mezer, the performance characteristic used to select from among the registers storing different sets of pre-computed pre-equalization coefficients (*supra* §VI.D) is *bit error rate* as taught by Das Sharma. Min, [0183].

7. Claim 7

7	The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.
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Lugthart-Das Sharma-Mezer implements a training phase, as taught by Lugthart-706 and/or Das Sharma, during which the pluggable module transceiver 107a/107b updates the pre-equalizer coefficient values for FIR filters 27a/27b from the selected register to optimize those coefficient values to reduce the error rate. *Supra* §§VI.E.1.c ([1.b]), VI.D (describing the combination); Min, [0184]; Das

Sharma, [0063], [0066], [0075], [0081], [0124], [0136]; Lugthart-706, 9:38-51, 22:13-17, 23:21-23.

POSAs had reasons to update the coefficient values in the selected register itself. Min, [0185]. It was known to store initial equalization coefficient values in a storage device and to then update those values directly in the storage medium during a training process. Gorecki, [0069] (the equalizer coefficients are “pre-programmed” and stored in a storage device “until re-programmed” to “be fine-tuned to enhance the system performance”); Min, [0185]. POSAs understood that using this technique in Lugthart-Das Sharma-Mezer would advantageously result in the coefficients in the selected register representing a particular chip-to-module channel being updated to reflect the channel more accurately given the adaptation that occurs during the training process. Min, [0185]. When Lugthart-Das Sharma-Mezer is implemented in this known (as taught by Gorecki) and obvious manner, the pluggable module transceiver *updat[es] the selected register with the updated pre-equalizer coefficient values* as required by claim 7. Min, [0185].

8. Claim 8

a. Preamble

8.PRE	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
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The '111 Patent uses “*chip-to-module communications link*” consistent with its known meaning, e.g., a communications link between a host IC and a pluggable module transceiver that can be plugged into a port on the host. *Supra* §VI.A; EX1032, 15 (“Interconnect Applications... Chip-to-module”), 17 (“3.4 Chip to module”), Fig. 8 (“Chip to Module Interconnect Application Space,” annotated below); Min, [0186].

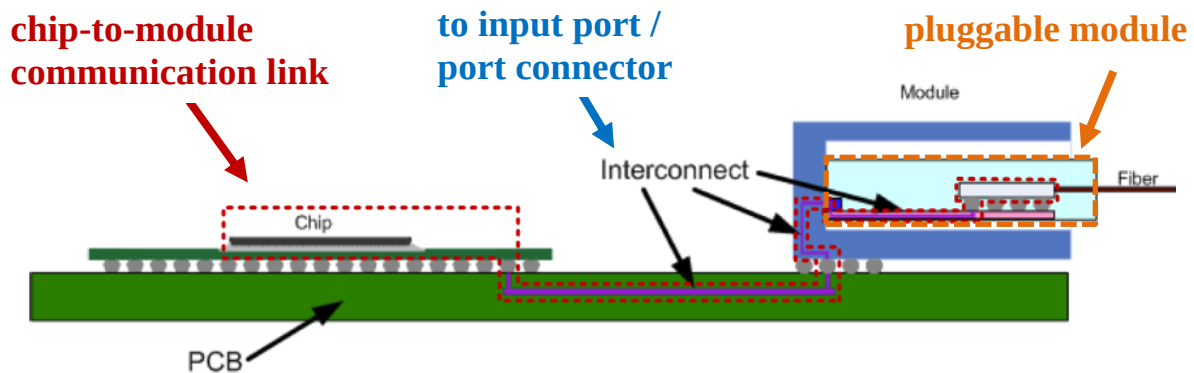
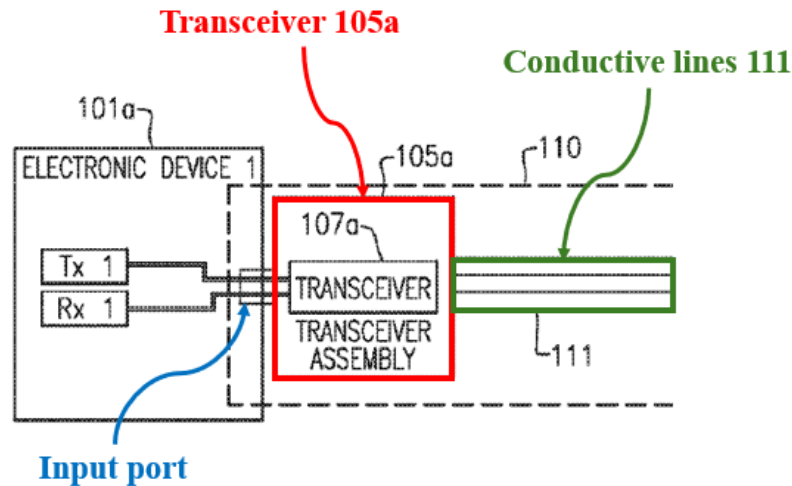


Figure 8 Chip to Module Interconnect Application Space

As discussed *supra* §VI.A, Lugthart-Das Sharma-Mezer’s communication link between a host transceiver in Lugthart-706’s electronic device 101a/101b and transceiver 107a/107b in the cable’s *pluggable module* (Lugthart-706’s modified

transceiver assembly 105a/105b), respectively, is a “*chip-to-module communications link*.” Min, [0187]; *cf. supra* §VI.E.2 (claim 2, “C2M channel”).



Transceiver assembly 105a is a *pluggable module* (red) with a port that is releasably coupled to an “input port” (blue) (i.e., *port connector*) on the first electronic device 101a. Min, [0188]; Lugthart-706, 14:31-38, 15:42-52 (describing an “input port” using existing standards, *e.g.*, SFP/QSFP), Fig. 2A (annotated detail above). The host device has a transceiver. Lugthart-706, 10:17-22 (transceiver 105a produces electrical signals that “can be provided to one or more additional **transceivers** electrically coupled to the transceiver... **on the host side**”); Min, [0188].

The host transceiver is a *port transceiver* because a port connector couples it to the pluggable module transceiver. EX1001, 1:50-51 (“a port connector couples a port transceiver to a pluggable module transceiver”); Min, [0189]. Transceiver

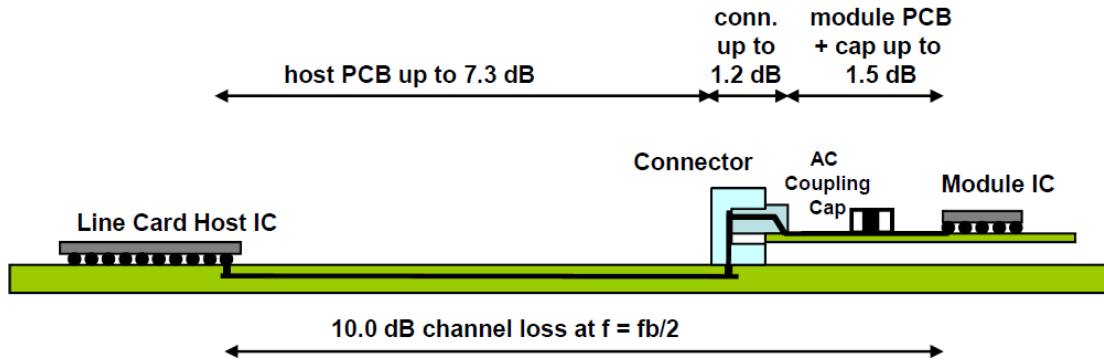
107a is a *pluggable module transceiver* because it is in transceiver assembly 105a, which is a *pluggable module* releasably pluggable into the host device port.

Lugthart-706, Fig. 2A, 4:10-30, 15:42-52, 52:1-5; Min, [0189].

Regardless, POSAs would have had reasons to implement Lugthart-Das Sharma-Mezer with a reasonable expectation of success so that it complied with the Ethernet standard because Lugthart-706 and Mezer each describe supporting Ethernet, and such standards-compliant implementation was conventional.

Lugthart-706, 48:16-20, 53:31-39; Mezer, 4:55-57, 6:62-7:3; Min, [0190]. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. Min, [0190]; 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 ("The chip-to-module interface is defined using a specification... that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0"); OIF-CEI-04.0, 334, Fig. 16-15 (below, showing a "Connector" receiving a pluggable module).

Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model



In OIF-CEI-04.0 Figure 16-15, the “Line Card Host IC” is the “*port transceiver*,” the “module IC” is the “*pluggable module transceiver*,” and the “Connector” is the “*port connector*,” meeting [8.PRE]. Min, [0191].

b. Limitation [8.a]

8.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
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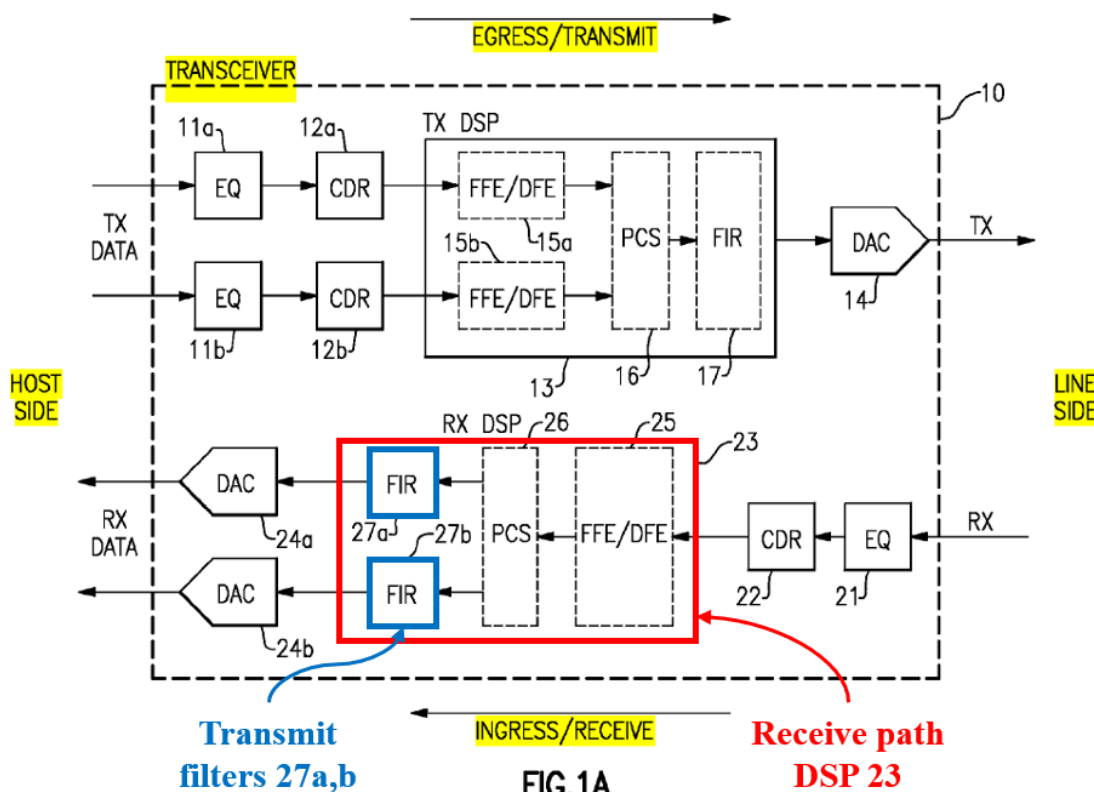
Lugthart-Das Sharma-Mezer meets [8.a] because it is an active cable system with Lugthart-706’s *pluggable module transceiver* 107a modified as discussed *supra* §VI.D. Transceiver 107a has a “host side” connected to electronic device 101a through the host’s port connector (discussed *supra* [8.PRE]) and a “line side” connected to the cable’s conductive lines 111. Min, [0192]; Lugthart-706, Fig. 1A, 8:13-32.

An “ingress/receive” data path represents data received from conductive lines 111 (“line side”) and transmitted to electronic device 101a (“host side”) after being processed by receive path RX DSP 23. Min, [0192]; Lugthart-706, Fig. 1A

(annotated below), 8:13-32, 8:56-9:9, 9:38-51, 10:17-22, 12:1-5, 15:42-47, Fig.

2A, 8:28-32 (receive path DSP 23's outputs are electrically coupled to DACs

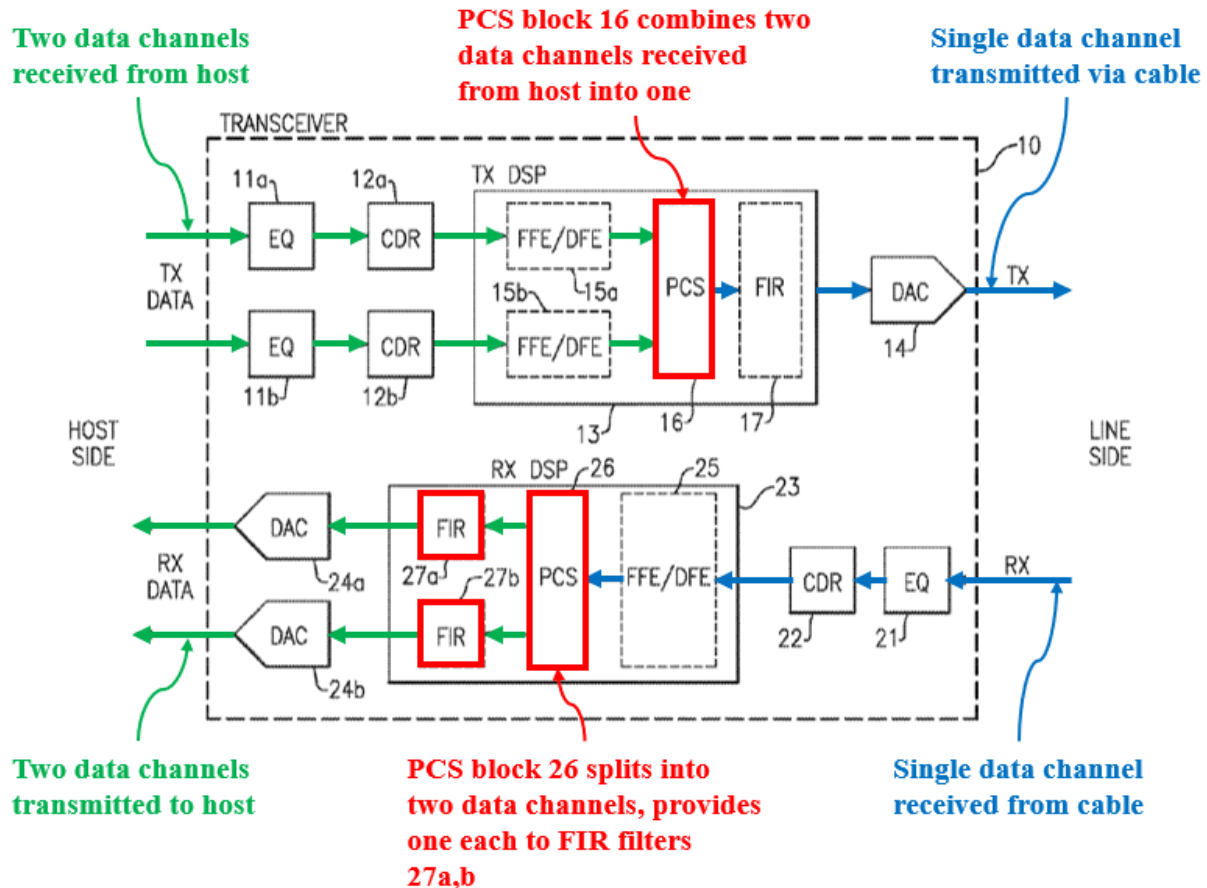
24a/24b which “include outputs that generate host side receive data (RX DATA).”)



Receive path DSP 23 includes FIR filters 27a/27b . Lugthart-706, Fig. 1A (transceiver 107a detail, annotated above), 9:38-51, Min, [0193]. FIR filters 27a/27b are *transmit filters* because they process data to be transmitted to the host transceiver, including providing pre-equalization. *Supra* §VI.E.1.b ([1.a]); Lugthart-706, 23:21-23, 23:62-64; Min, [0193]. The host transceiver is a “*port transceiver*” as discussed *supra* §VI.E.8.a ([8.PRE])). Min, [0193].

Lugthart-Das Sharma-Mezer's FIR filters 27a/27b *each pre-equalize[s] a corresponding serial symbol stream being transmitted to a port transceiver.*

Lugthart-706's transceivers "implement a serializer/deserializer (SerDes) function" converting between multiple signals on the host side and a single signal on the line side. Lugthart-706, 7:6-20; *id.*, Fig. 1A (annotated below), 24:17-20 (RX DSP 23's PCS block 26 "de-multiplex[es]" a single line-side signal into multiple signals transmitted to the host); Min, [0194].



POSAs understood that each signal transmitted to the host is a "serial symbol stream" as claimed. Min, [0195]. "Symbol" was a well-known term for a

portion of a waveform or a signal state that represents a unit of data. Lugthart-706, 31:39-46. Lugthart-706 notes that “intersymbol interference (ISI)” is “a form of signal distortion in which ***a symbol in a digital data stream interferes with subsequent symbols.***” Lugthart-706, 6:43-50. A symbol interfering with “subsequent symbols” transmitted over a data channel confirms that the symbols reside in a *serial symbol stream* are transmitted one after another. Min, [0195].

Thus, each of FIR filters 27a/27b “*pre-equalize[s] a corresponding serial symbol stream being transmitted to the port transceiver.*” Min, [0196].

c. Limitation [8.b]

8.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.
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Lugthart-Das Sharma-Mezer’s *pluggable module transceiver* (Lugthart-706’s modified transceiver 107a/107b) has *multiple registers each containing a set of initial coefficient values corresponding to a different channel model*. Min, [0197]; *supra* §§VI.E.1.b ([1.a]), VI.D (the combination uses Mezer’s teaching of different channel models with different initial coefficients and Das Sharma’s teaching to store coefficients in registers). As further discussed *supra* §§VI.D (explaining the combination) and VI.E.1.b ([1.a]), Lugthart-Das Sharma-Mezer modifies RX DSP 23 in Lugthart-706’s transceiver 107a/107b to have multiple

registers each storing a different set of coefficient values, and to select initial coefficient values for FIR filters 27a/27b (*transmit filters* per [8.a]) for use in an adaptive pre-equalization training process from among the registers. Min, [0197]; Das Sharma, [0078], [0193], Fig. 5; Lugthart-706, 9:38-51, 23:62-64.

POSAs would have implemented this functionality in the RX DSP 23 with a *controller*. Min, [0198]. Das Sharma teaches that the “coefficient register table” is used by a “coefficient algorithm module” that provides a set of initial coefficients to the transceiver’s transmission logic. Das Sharma, [0078], Fig. 5; Min, [0198]. Das Sharma Fig. 5 (annotated below) shows the coefficient algorithm module (red) and coefficient register table (blue). Das Sharma, [0078] (“coefficient algorithm module 520”); Min, [0198]. Das Sharm teaches that the coefficient algorithm module can be implemented by a microcontroller that includes the coefficient register table. Min, [0198]; Das Sharma, [0078], [0193] (Das Sharma’s “modules” can each be implemented via a “microcontroller” including “registers”).

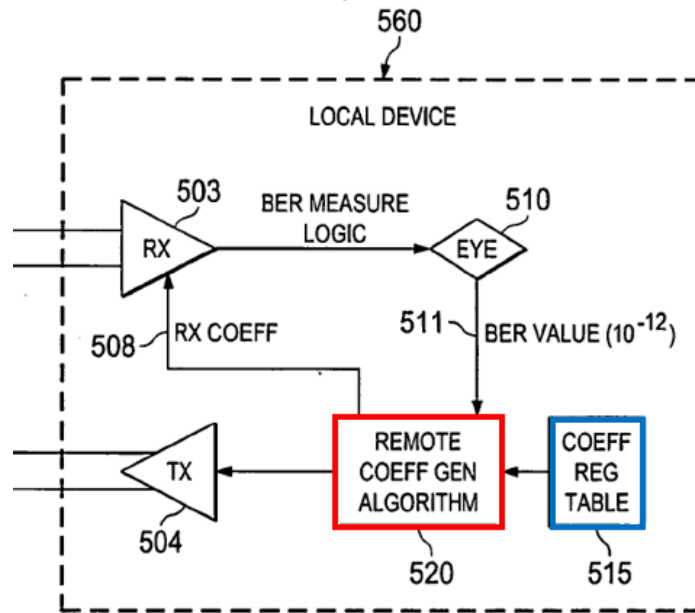


FIG. 5

Implementing Lugthart-Das Sharma-Mezer's pluggable module transceiver so that the RX DSP 23 functionality that stores initial coefficients in registers and selects an initial set is implemented by a controller including the registers would also have been a routine, conventional and obvious way to implement that functionality in RX DSP 23. Min, [0199]. It was common to implement functionality in a DSP via a controller and to include in the controller registers that store data used in implementing the controller's functionality to improve performance given that data can be quickly and efficiently accessed from a local register. Min, [0199]; Peddle, 5:13-22; Pickett, 2:8-34.

Accordingly, an obvious implementation of Lugthart-Das Sharma-Mezer meets [8.b]. Min, [0200].

9. Claims 9-10

Lugthart-Das Sharma-Mezer meets the additional limitations in claims 9 and 10 for the same reasons it meets the identical limitations in claims 2 and 3, respectively. *Supra* §§VI.E.2 (claim 2), VI.E.3 (claim 3); Min, [0201].

10. Claim 11

Lugthart-Das Sharma-Mezer meets Limitations [11.PRE] and [11.a] for the same reasons it meets the identical limitations [8.PRE] and [8.a], respectively. *Supra* §§VI.E.8.a ([8.PRE]), VI.E.8.b ([8.a]); Min, [0202].

a. Limitation [11.b]

11.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,
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Limitation [11.b]’s requirement of “*a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values*” is identical to a requirement in Limitation [8.b] and Lugthart-Das Sharma-Mezer meets that requirement in [11.b] for the same reasons. *Supra* §VI.E.8.c ([8.b]).

As discussed *supra* §VI.E.4 (claim 4), in one obvious implementation of Lugthart-Das Sharma-Mezer, a selection is made from among the registers storing different sets of pre-computed pre-equalization coefficients by having the pluggable module transceiver send an instance of a test signal pre-equalized with the set of coefficients stored in each register, and the port transceiver determine

which register's coefficients had the best performance characteristic (e.g., produced a signal with the smallest error). Min, [00204]. The port transceiver is a *port transceiver*. *Supra* §VI.E.8.a ([8.PRE]); Min, [0204]. Thus, the port transceiver determining a performance characteristic for each register meets “*each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic*” in [11.b]. Min, [0204].

b. Limitation [11.c]

11.c	the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.
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As discussed *supra* §VI.E.8.c ([8.b]), Lugthart-Das Sharma-Mezer's modified transceiver 107a/107b has a “*controller [that] us[es] one of the registers... to specify the initial coefficient values for the one or more transmit filters.*” Min, [0205]. The only additional requirement in limitation [11.c] is that the register is “*selected by the port transceiver.*”

As discussed *supra* §§VI.D (the combination), VI.E.4 (claim 4), and VI.E.10.a ([11.b]), one obvious implementation of Lugthart-Das Sharma-Mezer chooses the set of initial coefficients by having the pluggable module transceiver send an instance of a test signal pre-equalized with the coefficients in each register, determining at the *port (host) transceiver* which register's coefficients had the best performance characteristic and selecting the register with the best-performing

characteristics. Min, [0206]. In Lugthart-Das Sharma-Mezer, the *performance characteristic* is determined in the *port (host) transceiver* because that is where the test signal is received and can be best compared against a known error-free version of the test signal. *See supra* §§VI.E.5-6 (claims 5-6); Min, [0206].

In terms of which side (host/port or cable/pluggable module) of the link selects the register having the coefficients that produced the best performance characteristic, that was a matter of design choice. Min, [0207]. There were only two options and a POSA understood that either was a well-known design choice, making both obvious. Min, [0207]; *KSR*, 550 U.S. at 421. A POSA also understood that the *host/port transceiver* is the desirable design choice to make the selection because the *host/port transceiver* is the one that determines the performance characteristic for each register's coefficients and can simply select the best performing one and inform the pluggable module/pluggable module transceiver of that selection. Min, [0207]. This is analogous to Das Sharma's teaching that during its training phase, adapted equalization coefficients are determined by the receiving-side transceiver based on the received test signals and the adapted coefficients are then provided to transmitter-side transceiver. Das Sharma, [0078], [0193], FIG. 5; Min, [0207].

Thus, in the obvious implementation of Lugthart-Das Sharma-Mezer in which the *host/port transceiver* selects the register whose set of coefficients has the

best performance characteristics and sends that selection to the cable/pluggable module/transceiver, the *controller* in the pluggable module transceiver “*us[es] one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters*” as required by [11.c]. Min, [0208].

11. Claims 12-13

The additional limitations in claims 12 and 13 are identical to those in claims 5 and 6, respectively, and met by Lugthart-Das Sharma-Mezer for the same reasons. *Supra* §§VI.E.5-6 (claim 5-6); Min, [0209].

12. Claim 14

14	The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.
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Lugthart-Das Sharma-Mezer’s adaptive pre-equalization training process generates updated coefficients for FIR filters 27a/27b. *Supra* §VI.E.7 (claim 7); Min, [0210]. FIR filters 27a/27b are *transmit filters* *Supra* §VI.E.8.b (*transmit filters*). Min, [0210].

A conventional and obvious way to implement Lugthart-Das Sharma-Mezer’s training process was having the host “*port transceiver generate[] updates*” as required by claim 14. Min, [0211]; Das Sharma, [0078], [0193], FIG. 5. Either the host or module transceiver could generate filter coefficient updates;

POSAs understood that each was a possible design choice and therefore obvious. Min, [0211]; *KSR*, 550 U.S. at 421.

POSAs also understood that determining the equalization coefficient updates at the *host/port transceiver* was a desirable design choice because the *host/port transceiver* receives the test signals and can determine how they differ from known good signals, and thus how to adapt the equalization coefficients to reduce error. Min, [0211]. Additionally, Das Sharma specifically teaches that the channel's receive side (e.g., receiving training signals) determined updated equalization coefficients, which it transferred to the transmitter side. Das Sharma, [0078], [0193], FIG. 5; Min, [0211].

Lugthart-Das Sharma-Mezer implemented with the *host/port transceiver* determining updated coefficients during training—as suggested by Das Sharma and as was well-known in the art—renders obvious claim 14. Min, [0212].

13. Claim 15

Lugthart-Das Sharma-Mezer's adaptive pre-equalization stores *updated coefficient values* in one of the “multiple registers” in the cable's transceiver. *Supra* §VI.E.7 (claim 7); Min, [0213]. As discussed *supra* §VI.E.8.c ([8.b]), an obvious way to implement Lugthart-Das Sharma-Mezer's adaptive pre-equalization was via a **controller** in Lugthart-706's modified RX DSP 23. Min,

[0213]; Das Sharma, [0078], [0193]. Thus, Lugthart-Das Sharma-Mezer renders obvious claim 15. Min, [0213].

14. Claim 16

Lugthart-Das Sharma-Mezer meets [16.PRE] because its modified transceiver 107a/107b is a *pluggable module transceiver*. *Supra* §VI.E.8.a ([8.PRE]); Min, [0215]. Lugthart-Das Sharma-Mezer meets [16.a]-[16.b] for the same reasons it meets [8.a]-[8.b], respectively. *Supra* §§VI.E.8.b-c ([8.a]-[8.b]); Min, [0215].

15. Claims 17-19

The additional limitations in claims 17, 18, and 19 are substantively identical to those in Limitation [11.b], claim 5, and claim 6, respectively, and Lugthart-Das Sharma-Mezer meets them for the same reasons. *Supra* §§VI.E.10.a ([11.b]), VI.E.5 (claim 5), and VI.E.6 (claim 6); Min, [0216].

VII. NO BASIS FOR DISCRETIONARY DENIAL

A. Section 314(a) Denial is Unwarranted

The *General Plastic* analysis does not apply because the '111 Patent has not previously been challenged in IPR.

The *Fintiv*³ factors favor institution. Patent Owner (“PO”) filed a complaint in EDTX and the ITC on March 13, 2025. Petitioner expeditiously filed this

³ *Apple v. Fintiv*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential).

Petition within four weeks of the complaints. The ITC has not initiated a Section 337 Investigation—let alone set a trial date—and Petitioner has not even answered the EDTX complaint. ***If*** the ITC initiates an Investigation, FWD will likely issue ***before*** the ITC’s investigation concludes.

1. *Fintiv* factor one favors institution.

The complaints were filed four weeks ago and the ITC has not initiated an Investigation. If it does, Petitioner will seek automatic stay of the Texas Litigation under 28 U.S.C. §1659. *Fintiv* states that “an ***earlier*** ITC trial date ***may*** favor denial... ***if*** the ITC is going to decide the same or substantially similar issues to those presented in the petition. *Fintiv*, Paper 15, 8-9 (May 13, 2020) (informative); EX1043, 2 (“[T]he Board is less likely to deny institution under *Fintiv* where the ITC projected final determination date is ***after*** the Board's deadline to issue [FWD].”). There will be no “earlier ITC trial” here because FWD will likely issue before an ITC investigation—***if*** ordered—is completed. Because the Petition was expeditiously filed, neither the Texas Litigation nor an ITC Investigation—which has not even been instituted—is sufficiently developed to determine that the same or similar issues will be presented in those proceedings.

2. *Fintiv* factor two favors institution.

The ITC has not initiated an Investigation. If it does, the ITC’s average time to completion is over 18 months (EX1033), followed by a presidential review

period of 60 days. If the Texas Litigation is not stayed, the average time to trial in EDTX is 23 months (EX1034). Given the mandate to issue FWD within 18 months, an FWD will likely issue before final decision/trial in the ITC/district court proceedings, which favors institution. *Fintiv*, Paper 11, 9; EX1043, 2.

3. *Fintiv* factor three favors institution.

Petitioner filed “expeditiously”—only four weeks after PO’s ITC and district court complaints and before any response deadline for either. *Fintiv*, Paper 11, 11 (“If the evidence shows that the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted, this fact has weighed ***against*** exercising the authority to deny institution[.]”); *Mobileye Global v. Facet Tech.*, IPR2024-01110, Paper 16, 13 (Mar. 5, 2025); *Apple v. Alivecor*, IPR2021-00972, Paper 10, 12-13 (Dec. 8, 2021) (weighing factor three against denial where Petitioner filed IPR before response deadlines in ITC and district court).

4. *Fintiv* factor four favors institution.

This Petition challenges all claims. Although PO’s ITC complaint asserts all claims, at any ITC trial the asserted claims will likely be narrowed (EX1037, 1); PO identifies a single asserted claim in the Texas Litigation. EX1038, ¶31; EX1039, 2-11. The dependent claims challenged in the Petition raise numerous issues that will not overlap with either a hypothetical ITC proceeding or the Texas Litigation. This favors institution. *Fintiv*, Paper 11, at 12-13; *Volkswagen Group*

of Am. v. Arigna Tech., IPR2021-01531, Paper 7, 10 (Mar. 16, 2022); *3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12, at 34 (May 26, 2020).

Moreover, because Petitioner promptly filed this Petition, neither the Texas Litigation nor the ITC Investigation (which has not even been instituted) is sufficiently developed to determine whether, and to what extent, any issues will overlap, making factor four neutral at worst. *Cast Lighting v. Wangs Alliance*, PGR2021-00012, Paper 12, 34-35 (Jun. 7, 2021).

5. *Fintiv* factor five is neutral.

Despite Petitioner being an ITC “proposed Respondent” and Texas Litigation defendant, factor five is neutral because—given Petitioner’s expeditious filing—neither proceedings is developed sufficient to warrant denying institution. *Google v. Parus*, IPR2020-00846, Paper 9, 20-21 (Oct. 20, 2020) (factor five is neutral when it is speculative which tribunal will decide invalidity first).

6. *Fintiv* factor six favors institution.

Factor six favors institution because the Petition’s merits are strong.

Moreover, PO filed complaints against multiple potential parties in multiple venues. See EX1036 (ITC); EX1038 (Amphenol); EX1040 (Molex); EX1041 (TE Connectivity); EX1042 (Volex). The Board is the most efficient venue to resolve the ’111 Patent validity disputes and avoid piecemeal resolution in multiple proceedings. Since FWD will likely issue before validity determinations in any

parallel proceeding the Board’s decision will preclude needlessly duplicating efforts in those forums.

* * *

Factors 1-4 and 6 favor instituting IPR while factor 5 is neutral.

Discretionary denial under *Fintiv* and Section 314(a) is unwarranted.

B. Section 325(d) Denial is Unwarranted

1. Ground 1 fails *Advanced Bionics* step one.

The Office never considered or cited Lugthart-706, Das Sharma, or Mezer. EX1001, code (56). No record reference relies on Lugthart-Das Sharma-Mezer’s selecting one of multiple registers to specify initial pre-equalizer coefficient values, wherein each register’s data corresponds to a different channel model. EX1002, 87-94. The Examiner allowed the claims based on limitations related to “multiple registers [each] corresponding to a different channel model.” EX1002, 94 (indicating allowable subject matter in dependent claims, including the limitations referred to above), 77-79 (independent claims amended to include the indicated allowable subject matter). But as shown above, Lugthart-Das Sharma-Mezer meets this. *Supra* §VI.E.1.b ([1.a]).

Accordingly, the prior art presented in the Ground is not cumulative to prior art presented to the Office during prosecution. Thus, the Petition’s art and arguments were not previously considered, and the Petition fails *Advanced Bionics*

step one. *Advanced Bionics*, Paper 6, at 8-9; *PLR Worldwide Sales v. Flip Phone Games*, IPR2024-00209, Paper 9, 17 (May 10, 2024) (finding against discretionary denial because none of the grounds references were cited during prosecution).

2. Ground 1 fails *Advanced Bionics* step two.

Because the Petition fails *Advanced Bionics* step one there is no basis for reaching step 2. If the Board considers step two, then the Examiner materially erred by allowing claims at least because Lugthart-706-Das Sharma-Mezer meets [1.a], the limitation grounding the Examiner's reasons for allowance. *Supra* §§IV.D , VI.E.1.b ([1.a]).

VIII. CONCLUSION

The Board should institute review and cancel claims 1-19.

Respectfully submitted,
Amphenol Corporation

Dated: April 10, 2025

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APPENDIX A: U.S. PATENT NO. 11,032,111 CLAIM LIST

Ref	Limitation
1.PRE	A SerDes communications method that comprises, in a transceiver:
1.a	selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;
1.b	updating the initial pre-equalizer coefficient values during a training phase; and
1.c	using the updated pre-equalizer coefficient values to convey a transmit data stream.
2	The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
3	The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.
4	The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.
5	The method of claim 4, wherein the performance characteristic is an error signal energy.
6	The method of claim 4, wherein the performance characteristic is a bit error rate.
7	The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.

Ref	Limitation
8.PRE	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
8.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
8.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.
9	The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.
10	The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.
11.PRE	A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
11.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
11.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,
11.c	the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.

Ref	Limitation
12	The communications link of claim 11, wherein the performance characteristic is an error signal energy.
13	The communications link of claim 11, wherein the performance characteristic is a bit error rate.
14	The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.
15	The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.
16.PRE	A pluggable module transceiver including:
16.a	one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and
16.b	a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.
17	The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.
18	The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.
19	The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.

CERTIFICATE OF SERVICE UNDER 37 C.F.R. §42.6(e)(4)

I certify that on April 10, 2025, a copy of the foregoing document, including any exhibits or appendices filed therewith, is being served via *Overnight FedEx* at the following correspondence address of record for the patent:

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,972 words excluding a table of contents, a table of authorities, Mandatory Notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Date: April 10, 2025

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