

Exhibit C-2

Invalidity of U.S. Patent No. 11,032,111 (the “’111 Patent”) in View of U.S. Patent Publication No. 2017/0302431 (“Lugthart 431”)

Lugthart ’431 was filed on June 30, 2017, published October 19, 2017, and claims priority to U.S. Provisional Application No. 61/982,233, filed on April 21, 2014. Lugthart ’431 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the ’111 Patent is responsive to Complainant’s apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents’ claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents’ understanding of the proper scope of the Asserted Claims of the ’111 Patent.

All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant’s infringement and/or domestic industry contentions, and/or information obtained during discovery as the Investigation progresses.

To the extent Complainant alleges that Lugthart ’431 does not disclose any particular limitation of the Asserted Claims of the ’111 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’111 Patent to modify Lugthart ’431 and/or to combine the teachings of Lugthart ’431 with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the ’111 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the ’111 Patent that it contends is not fully disclosed by Lugthart ’431, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

1. Independent Claim 1

Claim 1	Lugthart '431
1[pre] A SerDes communications method that comprises, in a transceiver:	To the extent the preamble is limiting, Lugthart '431 discloses and/or renders obvious this preamble. “The communication system 100 of FIG. 2A illustrates an implementation of a high-speed communication link between first and second electronic devices 101 a, 101 b, which can also be referred to herein as host devices. In various implementations, the first and second electronic devices 101 a and 101 b can include one or more of a mobile computing device (e.g., a smart phone or a tablet), a personal computing device (e.g., a laptop, a desktop, a notebook), a workstation, a supercomputer, a peripheral device (e.g., a mouse, a keyboard, a joystick, a digital camera, a video camera, a webcam, a monitor, a display device, a speaker, a microphone, a printer, a scanner, a gaming system, an internet router, a hub, a network router, a port expansion device, an electronic switching device, a printed circuit board, a storage device (e.g., an external hard drive), an input/output interface device (e.g., read/write device, DVD player), a voice-over-IP device, etc.” Lugthart '431, ¶[0106] “FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105 a, 105 b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105 a includes a host side that is electrically connected to the first electronic device 101 a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105 b includes a host side that is electrically connected to the second electronic device 101 b and a line side that is electrically connected to a second end of the conductive lines 111.” Lugthart '431, ¶[0107]

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Claim 1	Lugthart '431
	“The first and second transceiver assemblies 105 a, 105 b can be implemented in a variety of ways. For example, the first and second transceiver assemblies include first and second transceivers 107 a, 107 b, respectively, which can be implemented using, for example, any of the embodiments of transceivers described earlier with respect to FIGS. 1A-1D.” Lugthart '431, ¶[0109]; <i>see also</i> FIGs. 1A-1D. “In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.” Lugthart '431, ¶[0058]

Claim 1	Lugthart '431
	FIG. 2A Lugthart '431, FIG. 2A “In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such

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	an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.” Lugthart '431, ¶[0067]. To the extent that this preamble is not disclosed, either explicitly or inherently, by Lugthart '431, this preamble is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this preamble as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[a] selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses a transceiver that provides “adaptive and configurable signal conditioning features such as... output pre-emphasis.” <i>See, e.g.</i>, Lugthart '431 ¶[0206]. Lugthart '431 teaches that “pre-emphasis” and “pre-equalization” have the same meaning. “Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).” Lugthart '431, ¶[0206] Although from the host’s perspective DSP 23 is on the “INGRESS/RECEIVE” path, Lugthart’s DSP 23—including FIR filters 27a/27b—provides pre-equalization for the signal (“RX DATA”) that transceiver 10 transmits to the host transceiver. Lugthart '431, ¶[0071], Fig. 1A (annotated below).

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	“The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12 a, 12 b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27 a, and a second FIR filter 27 b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15 a, a second FFE/DFE block 15 b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible.” Lugthart '431, ¶[0076]

Claim 1	Lugthart '431
	FIG. 1A transmit filters 27a/27b Lugthart '431, FIG. 1A (annotated) Transmit filters 27a/27b condition the line side signal, which they provide to DACs 24a/24b for transmission to the host side. <i>See id.</i> at ¶[00167]. Lugthart '431 explicitly identifies “transmission line losses on the host side” between the pluggable module transceiver and the host transceiver. <i>See id.</i> at ¶[0069]. Lugthart '431 explains that FIR filter 17 in the egress/transmit path “perform[s] emphasis on the

Claim 1	Lugthart '431
	signal to compensate for channel losses” (See <i>id.</i> at ¶[0172]) and notes that the “DSP 23 in the ingress path can include componentry that is similar to the DSP 13 in the egress path.” See <i>id.</i> at ¶[0173-0175]. In Lugthart '431's transceiver, equalizer 21 “compensate[s] for transmission line losses on the line side” in the ingress/receive data path (See <i>id.</i> at ¶[0069]), and Lugthart '431's pluggable module transceiver performs “output pre-emphasis.” See <i>id.</i> at ¶[0206]). Thus, Lugthart '431 describes FIR filters 27a/27b as performing “output pre-emphasis” to compensate for the transmission losses that Lugthart '431 describes on the host side between the pluggable module transceiver and the port transceiver. See <i>id.</i> at ¶[0206]. “The receive path equalizer 21 can be used to provide signal equalization to compensate for transmission line losses on the line side, and the first and second transmit path equalizers 11 a, 11 b can be used to provide signal equalization to compensate for transmission line losses on the host side. For example, in certain implementations, an equalizer can be used to compensate for high-frequency signal loss by boosting high frequency components of a signal relative to low frequency components of the signal, thereby improving signal fidelity. In certain configurations, an equalizer can also be used for balancing amplitude and/or frequency characteristics associated with non-inverted and inverted components of a differential signal. In one embodiment, the transmit path equalizers 11 a, 11 b and/or the receive path equalizer 21 are implemented as continuous-time linear equalizers (CTLEs).” Lugthart '431, ¶[0069] “In various implementations, the DSP 23 can also include one or more FIR filters and de-mapper to determine the signal components for the de-multiplexed data signal according to the desired modulation format. In some embodiments, the transceiver is configured to output the de-multiplexed signal as a differential signal encoded as NRZ format. However, any other suitable modulation format can be used in other implementations. The output of the DSP 23 is converted to an analog signal by the DACs 24 a, 24 b before being transmitted to the electronic device.” Lugthart '431, ¶[0167]

Claim 1	Lugthart '431
	“The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies.” Lugthart '431, ¶[0172] “The DSP 23 in the ingress path can include componentry that is similar to the DSP 13 in the egress path. However, because the data stream received from the line by the ingress path is already multiplexed and is transmitted over a different physical channel than the signals received on the egress path, the DSP 23 componentry in the ingress path can differ in certain ways from the DSP 13 componentry in the egress path. For instance, because the incoming data stream(s) is multiplexed, there may be a reduced number of instances of the FFE/DFE block 25 as compared to the DSP 13 componentry in the egress path. In the illustrated embodiment, the data is multiplexed to a single logical channel, and there is only one instance of the FFE/DFE block 25 in the ingress path.” Lugthart '431, ¶[0173] “Moreover, the PCS block 26 in the ingress path is configured to de-multiplex the incoming data channel(s), generally undoing the multiplexing function performed in the egress path. For instance, where NRZ and PAM-4 coding are used on the host and line side, respectively, the PCS block 26 maps the received PAM-4 signal to two or more NRZ data channels. To handle the de-multiplexed output of the PCS block 26, there may be multiple instances of the FIR filters 27 a-27 b and/or additional signal processing componentry—e.g., one corresponding to each data channel. In contrast to the FIR filters 27 a-

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Claim 1	Lugthart '431
	27 b of the DSP 23 that handle de-multiplexed data, the FIR filter 17 of the DSP 13 handles multiplexed data. Additional details of the transceiver 10 a can be similar to those described earlier.” Lugthart '431, ¶[0174-0175] “Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC).” Lugthart '431, ¶[0206] To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[b] updating the initial pre-equalizer coefficient values during a training phase; and	Lugthart '431 discloses and/or renders obvious this limitation. During a training phase, as taught by Lugthart '431 at the pluggable module transceiver 107a/107b that includes the registers storing different pre-equalizer coefficients update[es] the initial pre-equalizer coefficients, selected as discussed with claim limitation 1[a], for FIR filters 27a/27b to optimize those coefficients to reduce the error rate. <i>See, e.g.</i>, Lugthart '431 at ¶[0071], ¶[0161], ¶[0168]. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the

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Claim 1	Lugthart '431
	knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[c] using the updated pre-equalizer coefficient values to convey a transmit data stream.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431's transceiver 107a/107b us[es] the updated pre-equalizer coefficient values generated during the training phase by applying them to transmit FIR filters 27a/27b in DSP 23 to process the "INGRESS/RECEIVE" data stream (transmit data stream) in Lugthart '431 Fig. 1A. Lugthart '431 names data streams from the adjacent host's perspective, but this signal naming convention is irrelevant to filter 27a/27b's function, which is to condition signals for transmission over the C2M channel to the host transceiver. FIR filters 27a/27b outputs are connected to DACs 24a/24b, respectively, that "include outputs that generate host side receive data (RX DATA)" which is a transmit data stream that is transmitted to the host device. <i>See, e.g.,</i> Lugthart '431 at ¶[0065]. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1.1. Dependent Claim 2

Claim 2	Lugthart '431
2. The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	Lugthart '431 discloses and/or renders obvious this limitation. A “chip-to-module (C2M) channel” is a channel between a transceiver on a host IC and the transceiver on a pluggable module connected to a port on the device. See, e.g., '111 Patent at 5:24-30, 11:26-31 (describing the module side of a “C2M link” as implemented by a “pluggable module” such as a “QSFP” interface “that is inserted into a port in a host such as a switch or a router”); see <i>also</i> Optical Interworking Forum, “OIF Next Generation Interconnect Framework,” OIF-FD-Client-400G/1T-01.0 (2013), 15 (“Interconnect Applications... Chip-to-module”), 17 (“3.4 Chip to module”), Fig. 8 (“Chip to Module Interconnect Application Space,” annotated below). Figure 8 Chip to Module Interconnect Application Space Lugthart '431 teaches an active cable having a pluggable module that, when coupled to a host device, forms a chip-to-module channel between a host transceiver and the pluggable module transceiver. Lugthart '431 also teaches an active cable system includes a “QSFP interface” which is a “pluggable module” and includes transceivers 107a/107b. See, e.g., Lugthart '431 at ¶¶[0115-0116] (active cable including transceivers 107a/107b in a host’s QSFP port-compatible connector), ¶¶[0316-0318] (describing exemplary active cable comprising transceivers in QSFP interface), ¶¶[0323-0324] (referring to QSFP interface as a “pluggable module”), Fig. 17A.

Claim 2	Lugthart '431
	The transceivers 107a/107b of Lugthart '431 can send electrical signals to “one or more additional transceivers... on the host side” (host transceivers) in the electronic devices 101a/101b. <i>See, e.g.,</i> Lugthart '431 at ¶[0073]. These signals can be sent “over high loss PCB channels” connecting the pluggable module transceivers 107a/107b and the host transceivers. <i>See id.</i> at ¶[0205]. Lugthart '431 explains that “transceivers can be a monolithic device including analog and digital components included in a single integrated circuit (IC), for example, or may instead include multiple integrated circuits.” <i>See id.</i> at ¶[0115]. Lugthart '431 described a host transceiver in electronic device 101a/101b as comprising an IC, thus providing the “chip” for a C2M channel. Regardless, Lugthart '431 teaches that a conventional way to implement the host transceiver was with an IC mounted on the PCB in the host. Thus, in Lugthart '431 at the “high loss PCB channel[.]” that connects the host transceiver (an integrated circuit or “chip”) to the pluggable module transceiver 107a/107b is a “chip-to-module (C2M) channel.” <i>See id.</i> at ¶[0073], ¶[0115-0116], ¶[0205], ¶[0316-0318], ¶[0323-0324]. To the extent “chip-to-module (C2M) channel” means a chip-to-module channel conforming to the IEEE 802.3-2015 Ethernet standard referenced throughout the '111 Patent, Lugthart '431 still discloses claim 2 because Lugthart '431 describes, and conventional implementation supported, Ethernet communications over the PCB channel between the pluggable module transceiver 107a/107b and the host transceiver. <i>See id.</i> at ¶[0304]; <i>see also id.</i> ¶[0121] (“conducting lines 111” can “reside on a PCB or other substrate”). “[I]nsertion loss” refers to losses in signal strength from propagation through a channel, such as through the pluggable module’s port connection. “Package loss” refers to loss attributed to the particular “integrated circuit package” or “PCB layout” over which the signals travel. <i>See, e.g.,</i> '111 Patent at 11:55-60. While Lugthart '431 does not expressly say that the “high loss PCB channels” on the host side have “insertion loss” and “package loss,” Lugthart '431 teaches that this was so because it was well-known that there is package loss for signals exiting the pluggable module’s transceiver and entering the host device’s transceiver, as well as insertion loss as the signal propagates over the printed circuit board (PCB) between those transceivers. <i>See, e.g.,</i> Lugthart '431 at ¶[0204-0205] (describing the use of signal conditioning features (e.g., “output pre-emphasis”) to compensate for channel “insertion loss”), ¶[0115] (disclosing

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Claim 2	Lugthart '431
	that the transceiver is “enclosed in a packaging” comprising “materials suitable for electronic and computer interfaces”). Thus, Lugthart '431 teaches that the host-side “loss” that Lugthart '431 describes compensating for using pre-equalization performed by the pluggable module transceiver includes both insertion loss and packaging loss. <i>See, e.g.</i>, Lugthart '431 at ¶¶[0204-0205]. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1.2. Dependent Claim 3

Claim 3	Lugthart '431
3. The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1.3. Dependent Claim 4

Claim 4	Lugthart '431
4. The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1.4. Dependent Claim 5

Claim 5	Lugthart '431
5. The method of claim 4, wherein the performance characteristic is an error signal energy.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1.5. Dependent Claim 6

Claim 6	Lugthart '431
6. The method of claim 4, wherein the performance characteristic is a bit error rate.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

1.6. Dependent Claim 7

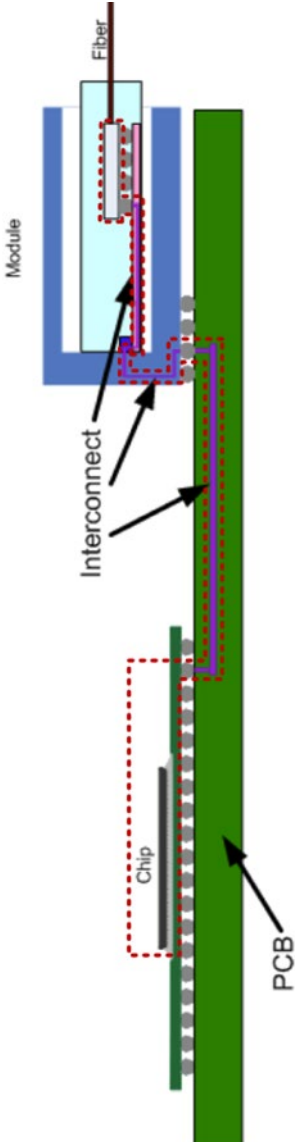
Claim 7	Lugthart '431
7. The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 teaches and implements a training phase, during which the pluggable module transceiver 107a/107b updates the pre-equalizer coefficient values for FIR filters 27a/27b from the selected register to optimize those coefficient values to reduce the error rate. <i>See, e.g.</i>, Lugthart '431 at ¶¶[0071], [0161], [0168]. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

2. Independent Claim 8

Claim 8	Lugthart '431
8[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	To the extent the preamble is limiting, Lugthart '431 discloses and/or renders obvious this preamble. “The communication system 100 of FIG. 2A illustrates an implementation of a high-speed communication link between first and second electronic devices 101 a, 101 b, which can also be referred to herein as host devices. In various implementations, the first and second electronic devices 101 a and 101 b can include one or more of a mobile computing device (e.g., a smart phone or a tablet), a personal computing device (e.g., a laptop, a desktop, a notebook), a workstation, a supercomputer, a peripheral device (e.g., a mouse, a keyboard, a joystick, a digital camera, a video camera, a webcam, a monitor, a display device, a speaker, a microphone, a printer, a scanner, a gaming system, an internet router, a hub, a network router, a port expansion device, an electronic switching device, a printed circuit board, a storage device (e.g., an external hard drive), an input/output interface device (e.g., read/write device, DVD player), a voice-over-IP device, etc.” Lugthart '431, ¶[0106] “FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105 a, 105 b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105 a includes a host side that is electrically connected to the first electronic device 101 a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105 b includes a host side that is electrically connected to the second electronic device 101 b and a line side that is electrically connected to a second end of the conductive lines 111.” Lugthart '431, ¶[0107]

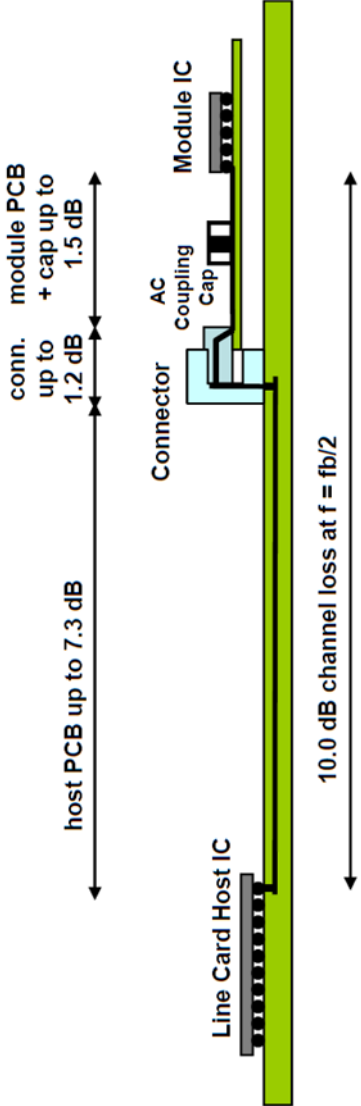
Claim 8	Lugthart '431
	“The first and second transceiver assemblies 105 a, 105 b can be implemented in a variety of ways. For example, the first and second transceiver assemblies include first and second transceivers 107 a, 107 b, respectively, which can be implemented using, for example, any of the embodiments of transceivers described earlier with respect to FIGS. 1A-1D.” Lugthart '431, ¶[0109]; <i>see also</i> FIGs. 1A-1D. “In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable.” Lugthart '431, ¶[0058]

Claim 8	Lugthart '431
	The diagram illustrates a transceiver system 100. It consists of two electronic devices, 101a and 101b, connected by a cable 111. Electronic device 101a contains a transmitter (Tx 1) and a receiver (Rx 1). Electronic device 101b contains a transmitter (Tx 2) and a receiver (Rx 2). The cable 111 has four signal paths: 105a (Tx 1 to Rx 2), 105b (Tx 2 to Rx 1), 107a (Tx 1 to Tx 2), and 107b (Tx 2 to Tx 1). The cable 111 is shown as a bundle of four lines. The signal paths are indicated by dashed lines with arrows. The label 100 points to the entire system. FIG. 2A Lugthart '431, FIG. 2A “In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such

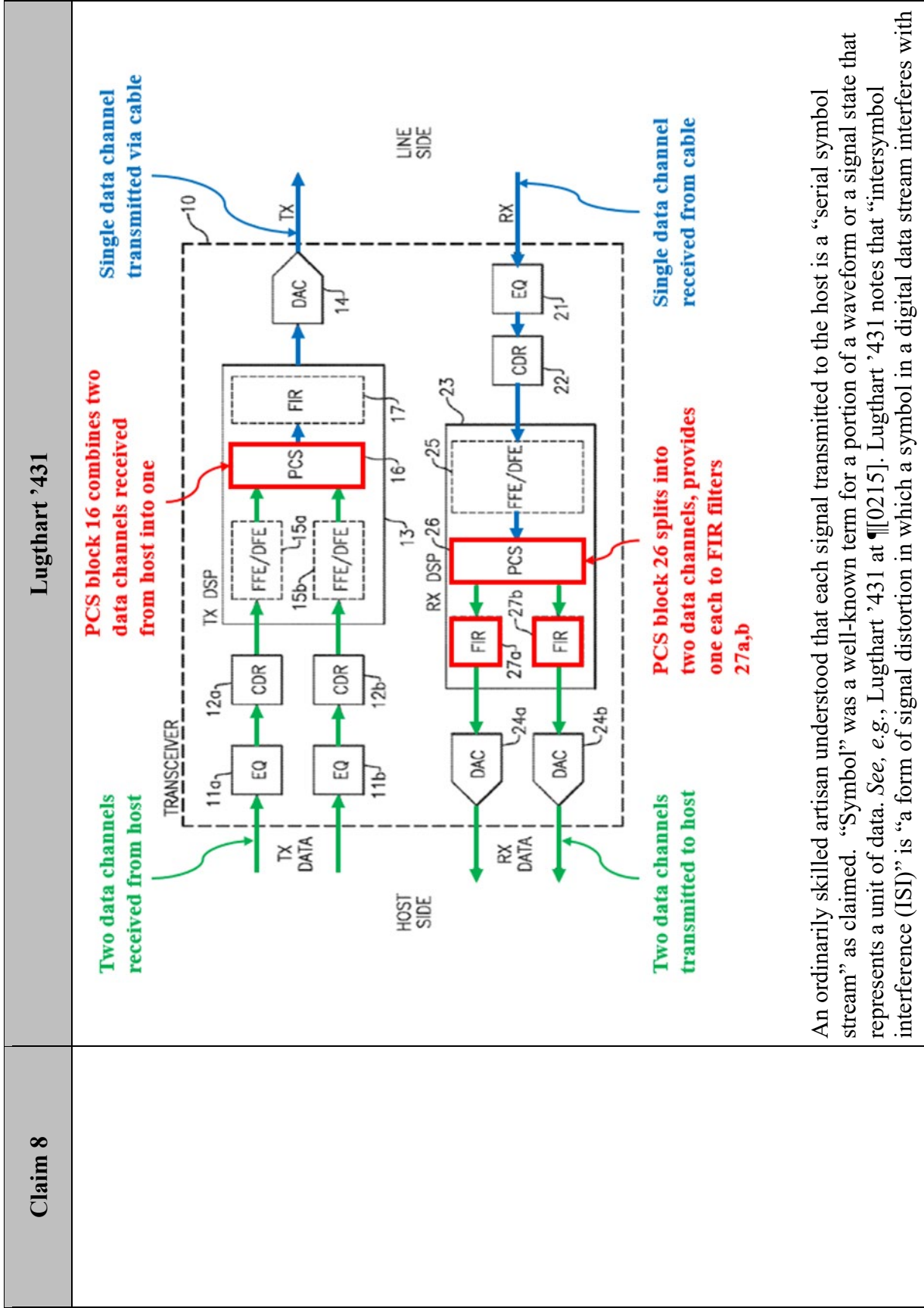
Claim 8	Lugthart '431
	an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side.” Lugthart '431, ¶[0067]. The '111 Patent uses “chip-to-module communications link” consistent with its known meaning, e.g., a communications link between a host IC and a pluggable module transceiver that can be plugged into a port on the host. Optical Internetworking Forum, “OIF Next Generation Interconnect Framework,” OIF-FD-Client-400G/1T-01.0 (2013), 15 (“Interconnect Applications... Chip-to-module”), 17 (“3.4 Chip to module”), Fig. 8 (“Chip to Module Interconnect Application Space,” annotated below).  Figure 8 Chip to Module Interconnect Application Space Lugthart '431's communication link between a host transceiver in Lugthart '431's electronic device 101a/101b and transceiver 107a/107b in the cable's pluggable module (Lugthart '431's modified transceiver assembly 105a/105b), respectively, is a “chip-to-module communications link.” See, e.g., claim 2 (“C2M channel”)

Claim 8	Lugthart '431
	The diagram illustrates a system architecture. On the left, a dashed box labeled 'ELECTRONIC DEVICE 1' contains two sub-components, 'Tx 1' and 'Rx 1'. A dashed line labeled '101a' points to this box. To the right of the electronic device is a 'TRANSCEIVER ASSEMBLY' box, which is part of a larger 'TRANSCIEVER' block labeled '105a'. A red arrow points from the label 'Transceiver 105a' to this block. Inside the transceiver assembly, a label '107a' points to a specific component. To the right of the transceiver assembly is a set of horizontal lines labeled '111', with a green arrow pointing to them from the label 'Conductive lines 111'. A dashed line labeled '110' is positioned between the transceiver assembly and the conductive lines. A blue arrow labeled 'Input port' points from the electronic device towards the transceiver assembly. Lugthart '431 FIG. 2A (annotated) “In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105 a and 105 b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101 a, 101 b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP).” Lugthart '431, ¶[0116]

Claim 8	Lugthart '431
	“In the illustrated configuration, the transmit path DAC 14 and the first and second receive path DACs 24 a, 24 b can be used to transmit signals generated by the transceiver 10 over transmission lines (which can include, for example, cables) to other circuitry, such as other transceivers and/or receivers. For example, the transmit path DAC 14 can be used to convert a digital output signal generated by the transmit path DSP 13 into an analog output signal, which can be provided to another transceiver electrically coupled to the transceiver 10 on the line side by a cable. Depending on the environment, the transmission line can include, for example, cables, printed circuit board (PCB) trace, backplane trace, and/or other electrical interconnect associated with the transmission line. Similarly, the first and second receive path DACs 24 a, 24 b can be used to convert digital output signals generated by the receive path DSP 23 into analog output signals that can be provided to one or more additional transceivers electrically coupled to the transceiver 10 on the host side via transmission lines.” Lugthart '431, ¶[0073] The host transceiver is a port transceiver because a port connector couples it to the pluggable module transceiver. <i>See, e.g.</i>, '111 Patent at 1:50-51 (“a port connector couples a port transceiver to a pluggable module transceiver”). Transceiver 107a is a pluggable module transceiver because it is in transceiver assembly 105a, which is a pluggable module releasably pluggable into the host device port. An ordinarily skilled artisan would have had reasons to implement as taught by Lugthart '431 with a reasonable expectation of success so that it complied with the Ethernet standard because Lugthart '431 describes supporting Ethernet, and such standards-compliant implementation was conventional. <i>See, e.g.</i>, Lugthart '431 at ¶[0304], ¶[0334-0335]. This obvious implementation would have met the Ethernet standard's description of a chip-to-module communication link comprising a port connector coupling a port transceiver to a pluggable module transceiver. <i>See, e.g.</i>, IEEE 802.3bs-2017, 323-330 (Annex 120C), 350-372 (Annex 120E), 350 (“The chip-to-module interface is defined using a specification... that is similar to that used for CEI-56G-VSR-PAM defined in OIF-CEI-04.0”); <i>see also</i> OIF-FD-Client-400G/1T-01.0 (2013) 334, Fig. 16-15 (below, showing a “Connector” receiving a pluggable module).

Claim 8	Lugthart '431
	Figure 16-15. CEI-56G-VSR-PAM4 Channel Reference Model  In OIF-CEI-04.0 Figure 16-15, the “Line Card Host IC” is the “port transceiver,” the “module IC” is the “pluggable module transceiver”, and the “Connector” is the “port connector”, meeting the preamble of claim 8. To the extent that this preamble is not disclosed, either explicitly or inherently, by Lugthart '431, this preamble is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this preamble as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses an active cable system with module transceiver 107a having a “host side” connected to electronic device 101a through the host’s port connector (discussed in claim 8[pre]) and a “line side” connected to the cable’s conductive lines 111. <i>See, e.g.</i>, Lugthart '431 at ¶[0065], Fig. 1A.

Claim 8	Lugthart '431
transmitted to the port transceiver; and	An “ingress/receive” data path represents data received from conductive lines 111 (“line side”) and transmitted to electronic device 101a (“host side”) after being processed by receive path RX DSP 23. <i>See, e.g.,</i> Lugthart '431 ¶¶0065], ¶¶067-0068], ¶0071], ¶0086], ¶0116], ¶0065] (receive path DSP 23’s outputs are electrically coupled to DACs 24a/24b which “include outputs that generate host side receive data (RX DATA)”, Fig. 1A (annotated below), Fig. 2A. Receive path DSP 23 includes FIR filters 27a/27b. <i>See, e.g.,</i> Lugthart '431 at ¶0071], Fig. 1A (transceiver 107a detail, annotated above). FIR filters 27a/27b are transmit filters because they process data to be transmitted to the host transceiver, including providing pre-equalization. <i>See, e.g.,</i> Lugthart '431 at ¶0168], ¶0172]. The host transceiver is a “port transceiver” as discussed supra §VI.E.8.a ([8][pre]). Lugthart '431’s FIR filters 27a/27b each pre-equalize[s] a corresponding serial symbol stream being transmitted to a port transceiver. Lugthart '431’s transceivers “implement a serializer/deserializer (SerDes) function” converting between multiple signals on the host side and a single signal on the line side. <i>See, e.g.,</i> Lugthart '431 at ¶0058]; <i>id.</i>, ¶0174] (RX DSP 23’s PCS block 26 “de-multiplex[es]” a single line-side signal into multiple signals transmitted to the host), Fig. 1A (annotated below).



Claim 8	Lugthart '431
	subsequent symbols.” See <i>id.</i> at ¶¶[0054-0055]. A symbol interfering with “subsequent symbols” transmitted over a data channel confirms that the symbols reside in a serial symbol stream are transmitted one after another. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[b] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses initial coefficient values for FIR filters 27a/27b (<i>i.e.</i>, transmit filters) for use in an adaptive pre-equalization training process from among the registers. See, e.g., Lugthart '431 at ¶¶[0071], [0172]. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to

Exhibit C-2

Claim 8	Lugthart '431
	modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

2.1. Dependent Claim 9

Claim 9	Lugthart '431
9. The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses for claim limitation 9 for the same reasons that Lugthart '431 discloses for claim 2. <i>See, e.g.</i>, claim 2. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

2.2. Dependent Claim 10

Claim 10	Lugthart '431
10. The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses for claim limitation 10 for the same reasons that Lugthart '431 discloses for claim 3. <i>See, e.g.</i>, claim 3. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

3. Independent Claim 11

Claim 11	Lugthart '431
11[pre] A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:	To the extent the preamble is limiting, Lugthart '431 discloses and/or renders obvious this preamble. Lugthart '431 discloses the preamble of claim 11 for the same reasons that Lugthart '431 discloses the preamble of claim 8. <i>See, e.g.,</i> claim 8[pre]. To the extent that this preamble is not disclosed, either explicitly or inherently, by Lugthart '431, this preamble is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this preamble as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses the claim limitation 11[a] for the same reasons that Lugthart '431 discloses for claim limitation 8[a]. <i>See, e.g.,</i> claim 8[a]. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[b] a controller having multiple registers, each of the multiple registers	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses the claim limitation 11[b] for the same reasons that Lugthart '431 discloses for claim limitation 8[b]. <i>See, e.g.,</i> claim 8[a].

Claim 11	Lugthart '431
containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,	To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
11[c] the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

3.1. Dependent Claim 12

Claim 12	Lugthart '431
12. The communications link of claim 11, wherein the performance characteristic is an error signal energy.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses for claim limitation 12 for the same reasons that Lugthart '431 discloses for claim 5. <i>See, e.g.</i>, claim 5. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

3.2. Dependent Claim 13

Claim 13	Lugthart '431
13. The communications link of claim 11, wherein the performance characteristic is a bit error rate.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses for claim limitation 13 for the same reasons that Lugthart '431 discloses for claim 6. <i>See, e.g.</i>, claim 3. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

3.3. Dependent Claim 14

Claim 14	Lugthart '431
14. The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

3.4. Dependent Claim 15

Claim 15	Lugthart '431
15. The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.	Lugthart '431 discloses and/or renders obvious this limitation. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

4. Independent Claim 16

Claim 16	Lugthart '431
16[pre] A pluggable module transceiver including:	To the extent the preamble is limiting, Lugthart '431 discloses and/or renders obvious this preamble. Lugthart '431 discloses the preamble of claim 16 for the same reasons that Lugthart '431 discloses the preamble of claim 8. <i>See, e.g.,</i> claim 8[pre]. To the extent that this preamble is not disclosed, either explicitly or inherently, by Lugthart '431, this preamble is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this preamble as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
16[a] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses the claim limitation 16[a] for the same reasons that Lugthart '431 discloses for claim limitation 8[a]. <i>See, e.g.,</i> claim 8[a]. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
16[b] a controller having multiple registers, each of the multiple registers	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses the claim limitation 16[b] for the same reasons that Lugthart '431 discloses for claim limitation 8[b]. <i>See, e.g.,</i> claim 8[b].

Claim 16	Lugthart '431
containing a set of initial coefficient values corresponding to a different channel model,	To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
16[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses the claim limitation 16[c] for the same reasons that Lugthart '431 discloses for claim limitation 8[c]. <i>See, e.g.</i>, claim 8[c]. To the extent that this claim limitation is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim limitation as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

4.1.1. Dependent Claim 17

Claim 17	Lugthart '431
17. The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses for claim 17 for the same reasons that Lugthart '431 discloses for claim limitation 11[b]. <i>See, e.g.</i>, claim limitation 11[b]. To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

4.2. Dependent Claim 18

Claim 18	Lugthart '431
18. The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses for claim 18 for the same reasons that Lugthart '431 discloses for claim 5. <i>See, e.g., claim 5.</i> To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

4.3. Dependent Claim 19

Claim 19	Lugthart '431
19. The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.	Lugthart '431 discloses and/or renders obvious this limitation. Lugthart '431 discloses for claim 19 for the same reasons that Lugthart '431 discloses for claim 6. <i>See, e.g., claim 6.</i> To the extent that this claim is not disclosed, either explicitly or inherently, by Lugthart '431, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '431 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.