

IEEE TRANSACTIONS ON MAGNETICS

A PUBLICATION OF THE IEEE MAGNETICS SOCIETY

JULY 2004

VOLUME 40

NUMBER 4

IEMGAQ

(ISSN 0018-9464)

PART II OF TWO PARTS



SELECTED PAPERS FROM THE NINTH JOINT MAGNETISM AND MAGNETIC MATERIALS-INTERNATIONAL
MAGNETICS CONFERENCE (MMM-INTERMAG)

Anaheim Marriott Hotel, Anaheim, California, January 5-9, 2004

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A PUBLICATION OF THE IEEE MAGNETICS SOCIETY

JULY 2004

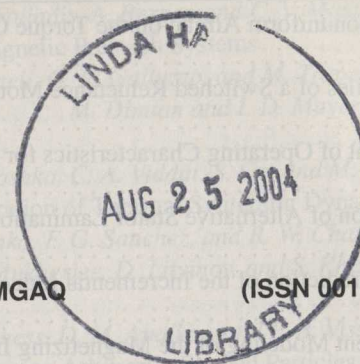
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70% TMR at Room Temperature for SDT Sandwich Junctions With CoFeB as Free and Reference Layers

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Abstract—Spin dependent tunneling (SDT) wafers were deposited using dc magnetron sputtering. SDT junctions were patterned and connected with one layer of metal lines using photolithography techniques. These junctions have a typical stack structure of $\text{Si}(100) - \text{Si}_3\text{N}_4 - \text{Ru} - \text{CoFeB} - \text{Al}_2\text{O}_3 - \text{CoFeB} - \text{Ru} - \text{FeCo} - \text{CrMnPt}$ with the antiferromagnet CrMnPt layers for pinning at the top. High-resolution transmission electron microscopy (HRTEM) reveals that the CoFeB has an amorphous structure and a smooth interface with the Al_2O_3 tunnel barrier. Although it is difficult to pin the amorphous CoFeB directly from the top, the use of a synthetic antiferromagnet (SAF) pinned layer structure allows sufficient rigidity of the reference CoFeB layer. The tunnel junctions were annealed at 250 °C for 1 h and tested for magneto-transport properties with tunnel magnetoresistive (TMR) values as high as 70.4% at room temperature, which is the highest value ever reported for such a sandwich structure. This TMR value translates to a spin polarization of 51% for CoFeB, which is likely to be higher at lower temperatures. These junctions also have a low coercivity (Hc) and a low parallel coupling field (Hcoupl). The combination of a high TMR, a low Hc, and a low Hcoupl is ideal for magnetic field sensor applications.

Index Terms—Amorphous CoFeB, magnetic sensor, magnetoresistance, MTJ, nanomagnetism, nanotechnology, spin-dependent tunneling (SDT).

I. INTRODUCTION

SPIN-DEPENDENT TUNNELING (SDT) materials have attracted extensive attention since 1995 when a sizable tunnel magnetoresistance (TMR) value of >10% was achieved at room temperature [1] which showed potential for new device applications. This TMR value compares with ~2% for the then-existing anisotropic magnetoresistive materials [2]. In general SDT materials have two key advantages over other magnetoresistive materials, one is a high field sensitivity, the other is orders-of-magnitude higher resistance which is easily attainable with small sizes [3], [4]. These superior properties make SDT materials especially attractive for low-field/low-power device applications [5], [6]. A high TMR value is desirable because it leads to greater signal level, lower power consumption, higher speed, and larger design margin for devices such as MRAM, read heads, and a variety of magnetic field sensors. TMR value is also the most important parameter in correlating experimental results with theoretical predictions.

New junction materials have been explored in dozens of laboratories around the world and ever increasing TMR values have been observed: 45% in 1999 [7], 59.5% in 2002 [8], through better material selection [9] and junction optimization. In this paper we report a 70.4% TMR value measured at room temperature for sandwich SDT structures, which is a new record high.

II. EXPERIMENT

SDT wafers were deposited using dc magnetron sputtering in a Shamrock system with a base pressure lower than 1.0×10^{-7} torr. A typical SDT wafer has a stack structure of $\text{Si}(100) - 200\text{Si}_3\text{N}_4 - 8\text{Ru} - 5\text{CoFeB} - 1.5\text{Al}_2\text{O}_3 - 5\text{CoFeB} - 0.9\text{Ru} - 5\text{FeCo} - 35\text{CrMnPt}$ (in nm) with the antiferromagnetic CrMnPt layers for pinning at the top. A $\text{Co}_{60}\text{Fe}_{20}\text{B}_{20}$ (at%) target and an $\text{Fe}_{60}\text{Co}_{40}$ target were used for the magnetic layer depositions. The Al_2O_3 barrier was formed by depositing a layer of metallic Al then oxidizing it in the plasma of Ar/ O_2 . A magnetic field of 50 Oe was applied during magnetic layer deposition to induce the easy axes and pinning direction. SDT junctions were patterned and connected with one layer of metal lines using photolithography techniques. Annealing was done in forming gas at a temperature of 250 °C for 1 h with a magnetic field applied. High-resolution TEM (HRTEM) analysis was done using a JEOL 2010F system with 200 keV energy. Magneto-transport data were taken using a computer controlled four-point-probe test station at room temperature.

III. RESULTS AND DISCUSSION

A. NiFeCo - Al_2O_3 - FeCo Junctions

A TMR value of 41.7% was previously reported for SDT junctions with a stack structure of $\text{Si}(100) - \text{Si}_3\text{N}_4 - \text{NiFeCo} - \text{Al}_2\text{O}_3 - \text{FeCo} - \text{CrMnPt}$ measured at room temperature after annealing at 250 °C for 1 h [10]. The highest TMR value we have obtained using this junction structure was 42.7% after barrier optimization.

B. CoFeB - Al_2O_3 - FeCo Junctions

In 2002 Kano *et al.* reported a TMR value of 59.5% using CoFeB as the free layer [8]. By changing the free layer from NiFeCo to CoFeB, we have increased the TMR value from 42.7% to 60.8%, with a SDT stack structure of $\text{Si}(100) - \text{Si}_3\text{N}_4 - \text{Ru} - \text{CoFeB} - \text{Al}_2\text{O}_3 - \text{FeCo} - \text{CrMnPt}$. The Ru buffer is necessary for efficiently conducting current due to the fact that CoFeB has a high resistivity. A representative TMR plot is shown in Fig. 1 for a pair of junctions in series. The benefit of using CoFeB is multifold: a higher TMR value,

Manuscript received October 9, 2003. This work was supported by the NSF under Grants DMI-9961165 and DMI-03-19974, ARMY under Grant DAAD17-01-C-0037, and MDA under Grant DTRA01-99-C-0110.

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Digital Object Identifier 10.1109/TMAG.2004.830219

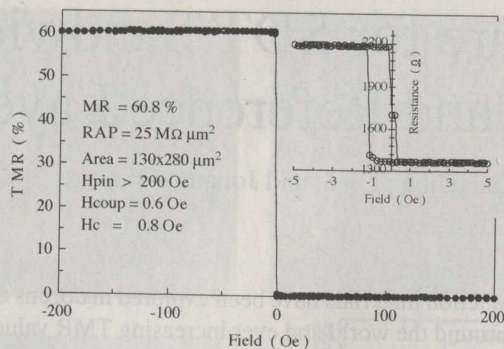


Fig. 1. TMR traces of a Si(100) - Si₃N₄ - Ru - CoFeB - Al₂O₃ - FeCo - CrMnPt SDT junction pair after 250 °C/1 h annealing. The inset shows a minor loop for the same junction pair with resistance in the vertical scale.

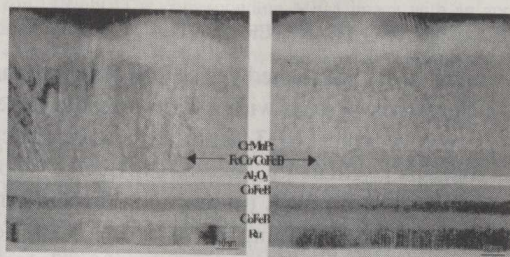


Fig. 2. Cross-section HRTEM images of a Si₃N₄ - CoFeB - Ta - CoFeB - Al₂O₃ - FeCo (left) [or CoFeB (right)] - CrMnPt SDT junctions.

a lower coercivity (H_c), and a lower coupling field (H_{coup}) for the free layer, which are all desirable for sensor applications.

C. CoFeB - Al₂O₃ - CoFeB Junctions

With such a large increase of TMR value by changing the free layer from NiFeCo to CoFeB, it is natural to replace both the free and pinned layers to CoFeB to further increase the TMR value. Such SDT junctions were fabricated with a stack structure of Si(100) - Si₃N₄ - Ru - CoFeB - Al₂O₃ - CoFeB - CrMnPt. However, magnetic pinning was not achieved to allow the TMR measurement for these junctions even after annealing. In comparison, a SDT stack structure of Si(100) - Si₃N₄ - Ru - CoFeB - Al₂O₃ - FeCo - CrMnPt referred in Fig. 1 has a pinning field >200 Oe as-deposited, which is further improved after annealing. Examination of the microstructure using HRTEM reveals that amorphous CoFeB does not support any crystalline grain growth of the CrMnPt layer, for which a correct crystal structure and large enough grains are needed to provide pinning to the CoFeB layer beneath it [11]. Details can be seen in the comparison of the two HRTEM images, shown in Fig. 2, for Si(100) - Si₃N₄ - Ru - CoFeB - Ta - CoFeB - Al₂O₃ - FeCo - CrMnPt (left) and Si(100) - Si₃N₄ - Ru - CoFeB - Ta - CoFeB - Al₂O₃ - CoFeB - CrMnPt (right). In Fig. 2 (left), continuous crystalline grain growth in vertical direction is observed throughout the FeCo-CrMnPt region, which is supported by the electron microdiffraction patterns (not shown here) from various spots in this region, and for which adequate pinning is obtained. In Fig. 2 (right), an amorphous CoFeB layer promote only amorphous-like CrMnPt growth, also supported by electron microdiffraction patterns, for which no pinning

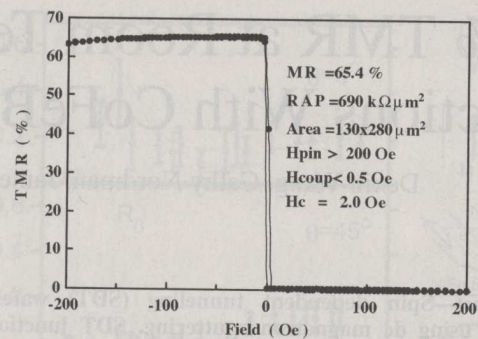


Fig. 3. TMR traces of a junction pair with a structure of Si(100) - Si₃N₄ - Ru - CoFeB - Ta - CoFeB - Al₂O₃ - CoFeB - Ru - FeCo - CrMnPt after 250 °C/1 h annealing. The inset shows the parameters of the junctions.

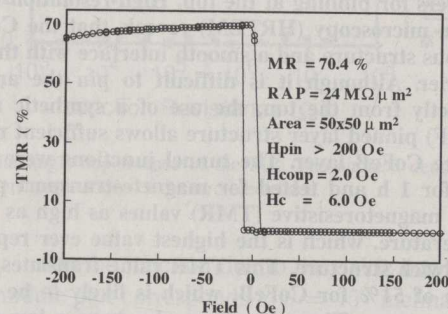


Fig. 4. TMR traces of a Si(100) - Si₃N₄ - Ru - CoFeB - Ta - CoFeB - Al₂O₃ - CoFeB - Ru - FeCo - CrMnPt SDT junction pair after 250 °C/1 h annealing. The inset shows the parameters of the junctions.

is observed. It is noted that the smooth barrier interfaces are similar for the two structures, as expected because only the top layers are different.

Synthetic antiferromagnet (SAF) sandwich structures of CoFeB-Ru-CoFeB and CoFeB-Ru-FeCo have been made and strong coupling has been observed. It appears that crystallinity is not required to have a strong indirect exchange coupling through Ru in a SAF structure, in contrast to the fact that crystallinity is required for the direct exchange coupling between a ferromagnetic layer and CrMnPt. A full SDT stack with a structure of Si(100) - Si₃N₄ - Ru - CoFeB - Ta - CoFeB - Al₂O₃ - CoFeB - Ru - FeCo - CrMnPt proves to be adequate to achieving sufficient pinning. A TMR plot is given in Fig. 3 for a pair of junctions connected back to back in series via the common free layer [10] with such a stacking structure. The TMR value is indeed improved to be 65.4%, comparing to 60.8% with CoFeB on only one side of the tunnel barrier.

Further optimization of the junctions leads to an even high TMR value of 70.4%, as shown in Fig. 4 for a pair of junctions with a slightly thicker tunnel barrier but otherwise identical nominal stack structure as shown in Fig. 3. This TMR value is the highest seen in the literature as well as presented at professional conferences to date.

The bias voltage dependence of the resistance for a pair of junctions is shown in Fig. 5 either when the two magnetizations are parallel or antiparallel. The bias voltage dependence of TMR is calculated from these data and plotted in Fig. 6. The TMR value becomes half of its maximum value at a voltage >1.2 V for the junction pair, which implies that the single

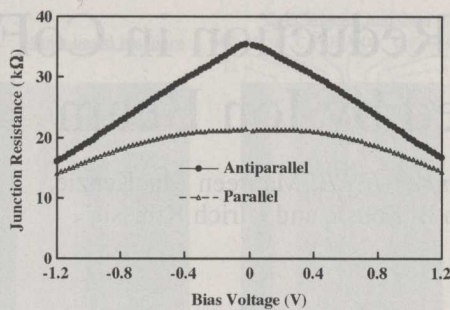


Fig. 5. Bias voltage dependence of the antiparallel and parallel resistances for a pair of junctions with a stack structure of Si(100) – Si₃N₄ – CoFeB – Ta – CoFeB – Al₂O₃ – CoFeB – Ru – FeCo – CrMnPt after 250 °C/1 h annealing.

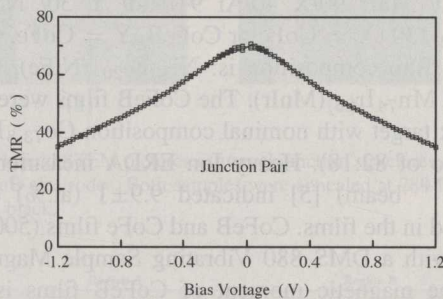


Fig. 6. Bias voltage dependence of the TMR values for a pair of junctions calculated using data from Fig. 5.

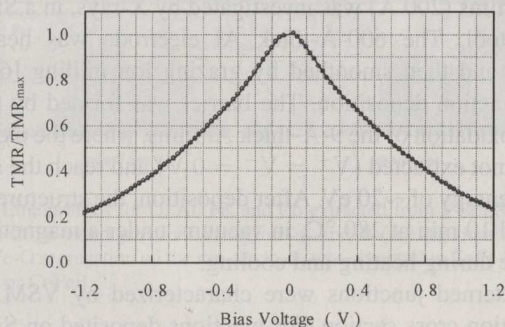


Fig. 7. Normalized bias voltage dependence of the TMR values for a single junction with a similar stack structure as shown in Fig. 5.

junction bias-voltage-at-half-maximum-TMR ($V_{1/2}$) > 0.6 V, which is among the highest observed. A high $V_{1/2}$ value represents a weaker bias voltage dependence, which is desirable for device applications.

Fig. 7 shows the bias dependence of the normalized TMR value for a single junction. The $V_{1/2}$ value is more accurately estimated to be 620 mV. Moreover, there is little asymmetry to the curve. For a practical junction, a high TMR value is a strong indication that a high quality of the tunnel barrier and its two interfaces is obtained. When this high TMR value is coupled with high symmetry of the bias dependence, it provides a necessary condition of having an optimized barrier and its two interfaces. If on the other hand a large asymmetry were observed, it would suggest that at least one of the two interfaces could be further optimized. Nevertheless, it is difficult to conclude that an ultimate optimization has been achieved.

D. Discussion

TMR is usually defined as the difference in the resistance values divided by the lower value. According to Julliere's model [12], this TMR can be expressed by:

$$TMR = \frac{2P_1P_2}{1 - P_1P_2} \quad (1)$$

where P_1 and P_2 are the spin polarizations at the two ferromagnetic interfaces with the tunnel barrier. It is reasonable to assume $P_1 = P_2$ for tunnel junctions with CoFeB at both interfaces. A TMR value of 70.4% at room temperature leads to a spin polarization of 51% from (1), comparing with a 50% for the best FeCo compositions. Even higher P value is expected for CoFeB at low temperatures for this easily produced magnetic material. Half-metallic magnetic materials such as Fe₃O₄ have a theoretical P value of 100%, though this is difficult to achieve at the interfaces in a practical junction [13]. Based on (1) there is no limit to the TMR value. However, (1) is an over simplified model; more realistic ones may yield practical limits. Nevertheless, experimentally realizing high TMR is of significance in verifying theories. Most importantly, a functioning junction with high TMR value means high signal level, high sensitivity, high speed, and lower power consumption for devices based on tunnel junctions.

ACKNOWLEDGMENT

The authors appreciate the assistance from Dr. Pohm, Dr. Tondra, Dr. Jander, Mr. Popple, Mr. Brownell, and Mr. Tran at NVE.

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