

Source-Sense Packages for HV MOSFETs

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Abstract

In traditional 3-pin High-Voltage (HV) power MOSFET (MOSFET) packages, the hard-switching transition speed is limited by the package source-inductance because the MOSFET drain current and gate current both share a path through the same package source inductance. The details of this mechanism are discussed and the resulting additional switching power loss caused by it is both measured and simulated.

Proposed innovative “Source-Sense” packages split the two currents into separate paths by adding separate source-pin for Kelvin-type driver connection to gate-source on the chip, thus completely eliminating all switching loss incurred by the source inductance for improved efficiency and lower die temperature.

Leadless SMD packages employing this method are explored for further addressing complications caused by package source inductance, such as common-mode noise and requirement for filtering.

Advanced package concepts are discussed for future optimization and thermal management, and versatility of these advanced concepts as well as existing leadless SMD packages with “Source-Sense” is examined.

Key words

Four Pin, Four-pin, High Voltage Switching, Kelvin, Sense Pin, Source Sense, Source-sense

I. Introduction

The transition time (di/dt) of HV MOSFETs has historically been determined by the performance of the Super Junction Silicon die; specifically the magnitudes of the input charges required to turn on (and off) the device; a combination of Q_{GS} and Q_{GD} . With the latest generation of Super Junction MOSFETs from Infineon, CoolMOS™ C7, the improvements to the input charges of the die have been so significant, that the transition speed of these devices is now limited by a different mechanism; the package parasitic source inductance.

Rather than developing new packages aiming for lower source-inductance, an innovative approach was chosen to completely eliminate the effect of package parasitic source inductance on switching loss – even in packages with relatively large values of source inductance.

In this paper the innovative “Source-Sense” approach is explored in great detail; from a thorough explanation of the loss mechanism to simulated A/B comparisons and real-life verification in physical test boards.

II. Source Inductance Loss Mechanism

In hard switching applications, such as the common boost PFC circuit operating in CCM mode, the MOSFET is switching a current (which can be considered constant during the transition time) sourced by an input inductor from the boost diode to its own channel. First the current will commute from the diode to the MOSFET channel, while the voltage across the diode (and therefore also the MOSFET) can be considered to remain constant (due to the forward current flowing through the diode). Since the MOSFET will see current through it and voltage across it at the same time, it will incur a power loss based on the current amplitude, the voltage potential and the rate of change of current. The commutation speed (di/dt) is governed by the transfer function of the MOSFET, which in turn is determined by the input charges as typically shown graphically in the MOSFET datasheet and exemplified in fig 1 (A) and (B). It is clear from these graphs that higher di/dt demands faster change of V_{GS} (dv_{GS}/dt), which can only be achieved by a higher current to

the MOSFET gate.

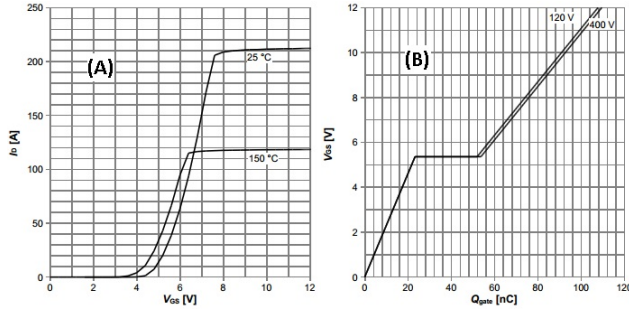


Figure 1: Datasheet examples for

(A): Transfer characteristics (B): Gate charge

The amplitude of current fed into its gate during current commutation thus directly influences the turn-on loss. To better understand how current is typically fed into the MOSFET gate during current commutation, an equivalent schematic is presented in fig. 2.

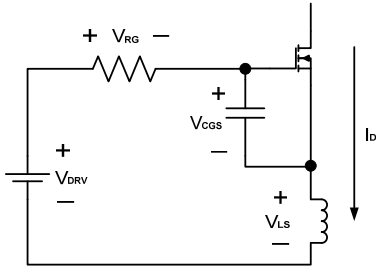


Figure 2: Typical gate current loop during commutation

An ideal driver supplies a constant voltage through a discrete gate resistor (in series with the driver output impedance and the internal gate resistance of the MOSFET) to the gate-source pins of a discrete MOSFET in a non-ideal package containing a parasitic source inductance. The current fed into the gate is determined by the chosen value of the gate resistor and the voltage across it V_{RG} , which can be found by applying KVL in the simplified circuit of fig. 2.

$$V_{RG} = V_{DRV} - V_{CGS} - V_{LS} \quad (1)$$

The driver voltage can be assumed to have a constant (DC) value of V_{DRV} and the voltage across the Silicon die gate-source capacitor V_{CGS} can also be approximated as a constant voltage (for simplicity of explanation) with an amplitude somewhere close to $V_{plateau}$.

The only unknown voltage in the mesh-analysis (apart from V_{RG}) is the voltage across the package parasitic source inductance, V_{LS} . This voltage can be found from the standard inductor equation given below in (2)

$$V_{LS} = L_S \cdot \frac{di}{dt} \quad (2)$$

Where L_S is the source inductance and di/dt is the commutation rate-of-change of the MOSFET drain-current.

If substituting (2) into (1), and solving for $V_{RG} > 0$, one can arrive at a 1st order theoretic maximum di/dt determined by L_S , where the current into the gate is $\sim 0A$ regardless of R_G :

$$V_{DRV} - V_{plateau} - L_S \cdot \frac{di}{dt} > 0 \Rightarrow \quad (3)$$

$$\frac{di}{dt} < \frac{V_{DRV} - V_{plateau}}{L_S} \quad)$$

To the extent that transfer characteristics and gate charge (for given driver voltage and gate resistance) determine a lower di/dt than the limit given in (3) for a given source-inductance, the switching loss is determined by the Silicon die performance. This has historically been the case. With the arrival of Silicon dies with very steep transfer characteristics and very little gate charge such as exemplified in fig. 1, the di/dt limit given in (3) can easily be exceeded by the Silicon – even for relatively low-inductance leadless SMD packages.

The switching loss in new generation HV power MOSFETs is thus a function of package parasitic source-inductance, as shall be shown in following example.

Consider a package with an intrinsic parasitic source inductance of 2nH. This is a conservative value considering the theoretic $\sim 8nH$ of a standard TO-247 3-pin and over 1.5nH for a typical HV leadless SMD package such as ThinPAK8x8. Driving the gate with a standard $V_{DRV}=12V$ and assuming a $V_{plateau}$ in the range of $\sim 5V$ during current commutation (fairly typical value), we arrive at

$$\frac{di}{dt} < \frac{12V - 5V}{2nH} \Rightarrow \frac{di}{dt} < 3.5 A/ns \quad (4)$$

In a simulation recreating these conditions at a quasi-arbitrarily chosen $\sim 5\Omega$ total gate resistance ($3.4\Omega R_{g,ext} + 0.5\Omega$ driver output impedance + $0.82\Omega R_{g,int}$), the I_d waveform looks as illustrated in fig. 3 (red):

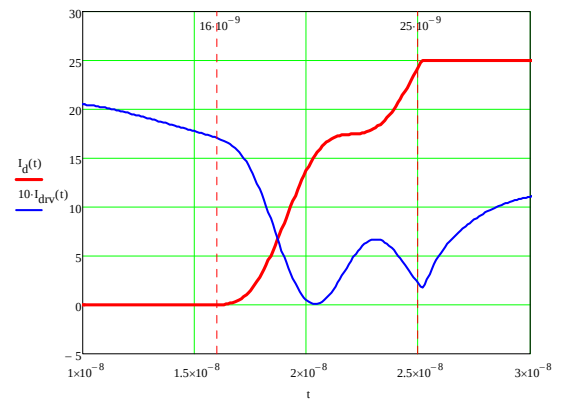


Figure 3: Simulated drain- (red) and (10x) gate currents (blue) during 25A turn-on commutation

The complex interaction between reactive elements (C_{GS} , L_S) causes a quasi-oscillatory behavior with an underlying

clear fundamental di/dt limit of around $25A/9ns$ or $\sim 2.8A/ns$ – and as predicted the gate current goes to 0 at max V_{LS} . Turn-on energy of $\sim 71\mu J$ is observed (from simulation).

III. Source-Sense concept and A/B simulation

A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.

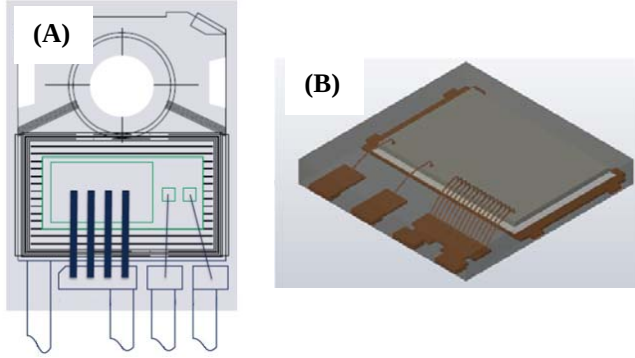


Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections

The principle is to provide a separate path for the drain-source current, such that voltage generated across the source inductance no longer appears in the KVL mesh of the gate current loop.

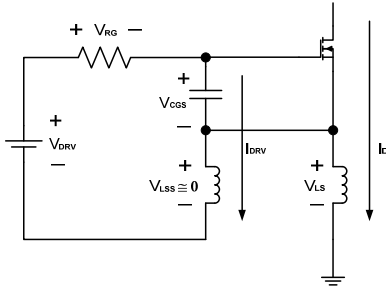


Figure 5: “Source-sense” loops during commutation

The implementation of the Source-Sense concept is illustrated above in fig. 3, where the KVL mesh analysis is radically different.

As was the case in fig. 2, V_{DRV} and V_{CGS} can both be approximated as constant. Since the drain current can no longer complete a loop through the source-sense connection, the di/dt will only cause a voltage drop across the “Power Source” package inductance; V_{LS} . Since V_{DRV} and V_{CGS} are both close to constant, V_{RG} will also be close to constant, and the current through the loop will therefore also be close to constant ($di/dt \sim 0$); causing V_{LSS} to be approximately 0 volts.

The limit on di/dt that was historically imposed on the drain-current by the package parasitic source inductance is thus completely averted, and therefore the loss associated with package parasitic source inductance is fundamentally eliminated.

Let us consider the same simulated scenario as above, but with “source-sense” implemented:

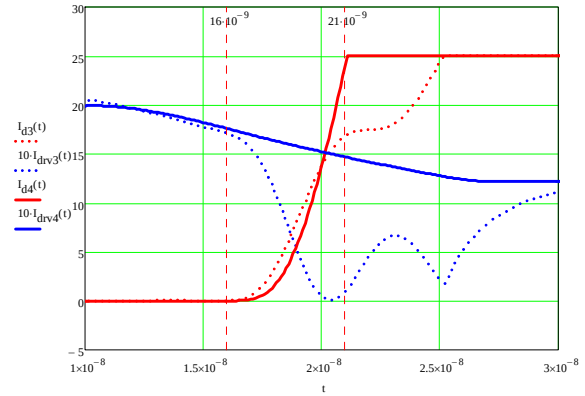


Figure 6: I_D (red) and I_{DRV} (blue) for 4-pin device

It is immediately clear that the di/dt achievable in this case is steeper than ‘allowed’ by source inductance. The gate current in the 4-pin case only reduces as V_{GS} rises (as would be expected) with no feedback contribution from L_S . The resulting di/dt of roughly $25A/5ns$ corresponds to $5A/ns$ or almost double that of the conventional 3-pin configuration.

Turn-on energy of $\sim 18\mu J$ is observed equating to a net energy savings of $53\mu J$ compared to previously observed value in 3-pin scenario in this example. If making some quick assumptions, this power savings equates to $\sim 2.6W$ in a typical $2.5kW$ PFC application (assuming $\sim 40\%$ operation near $25A$ peak for a sinusoidal wave-shape and a switching frequency of $100kHz$). Not only would the demands on the thermal management system become more relaxed, but a net efficiency increase on the order of 0.2% at low line ($\sim 1150W P_{OUT}$) would be a welcomed benefit onto itself – gained by nothing else but a package change; with no change to the silicon. The simulated energy loss cannot only be explained as a function of the drain-current di/dt , although the 1st order assumptions were based on full and constant voltage across drain-source at the time of current commutation. In a real physical circuit, the drain-voltage will be decreasing during the current commutation, since the di/dt will cause additional and significant voltage drops across the total commutation loop inductance. In a typical layout with sub-optimal total loop inductance, the effect can be seen as a smaller ‘blip’ on the V_{DS} curve in the 3-pin case, whereas the voltage will be naturally monotonically decreasing (since di/dt is monotonically increasing) in the 4-pin case.

The V_{DS} waveforms (excl. L_S) in the two cases look thus:

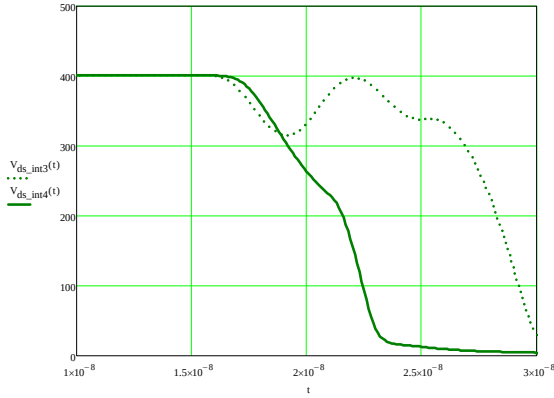


Figure 7: V_{DS} (excluding V_{LS}) for 4-pin vs. 3-pin (dash)

It is clear from the non-monotonically falling V_{DS} in the 3-pin configuration (dashed line in fig 6), that the di/dt is not monotonically increasing and that it is therefore limited by parasitic package source inductance rather than silicon performance. A check on V_{DS} is typically quite a bit more practical than measuring drain- or gate currents, and can provide easy hints on whether di/dt is source-inductance limited on a physical board.

Another good check is V_{RG} , which directly represents gate current; if this voltage shows non-monotonous behavior, then extra switching losses caused by parasitic source inductance in 3-pin configuration are evident.

IV. Physical verification

Simulations clearly confirmed the conclusion of sub-optimal di/dt and associated loss from the simple theoretic explanation (neglecting complex interaction of reactive elements) of the loss mechanism. The conceptualization of the 4-pin “source-sense” MOSFET device as a means of completely eliminating this loss mechanism afforded a theoretic relief, which was further proven in simulation and compared to the historical 3-pin package. A means of quickly and easily identifying the behavior in a physical board was offered by way of monitoring of V_{DS} .

A real test board was constructed in a way that a historical 3-pin package could be directly compared with a novel source-sense approach without any other changes than the package concept. I_D as well as V_{DS} was documented in both cases for direct A/B comparison in a scenario not too unlike the simulated one:

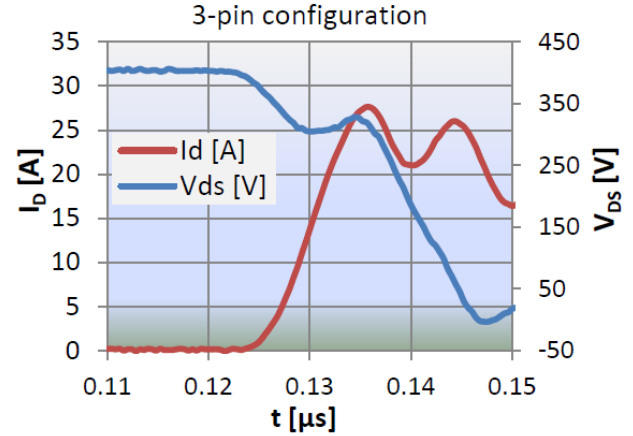


Figure 8: 45mOhm CoolMOS™ C7 switching $I_D=20A$ with $R_{G,ext}=10\Omega$ and $V_{DRV}=12V$ in 3-pin configuration

Of course the amplitude of initial voltage drop observed on the V_{DS} waveform is a function of total commutation loop inductance and the effective period of the oscillatory tendency is a function of complex interaction between reactive elements (primarily L_S and C_{GS}). In fig. 7 that is a measured waveform on a real test board, we can clearly observe such a V_{DS} wave shape, and conclude that switching speed in terms of di/dt is compromised by parasitic package source inductance.

We expect to see a direct efficiency improvement with higher di/dt and monotonically decreasing V_{DS} when changing to the 4-pin source-sense configuration.

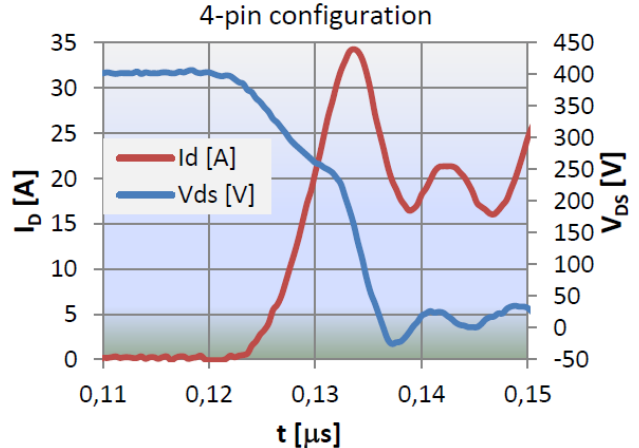


Figure 9: 45mOhm CoolMOS™ C7 switching $I_D=20A$ with $R_{G,ext}=10\Omega$ and $V_{DRV}=12V$ in 4-pin configuration

From fig. 8 a monotonically decreasing V_{DS} is observed as well as higher di/dt with a much shorter total transition time. The resulting effect on efficiency is a function of current magnitude (di/dt limiting for 3-pin devices is worse at higher current magnitudes), and we should therefore expect less difference at light loads and a much bigger efficiency gain at full load.

Efficiency at different load levels with both 3-pin and 4-pin devices was recorded:

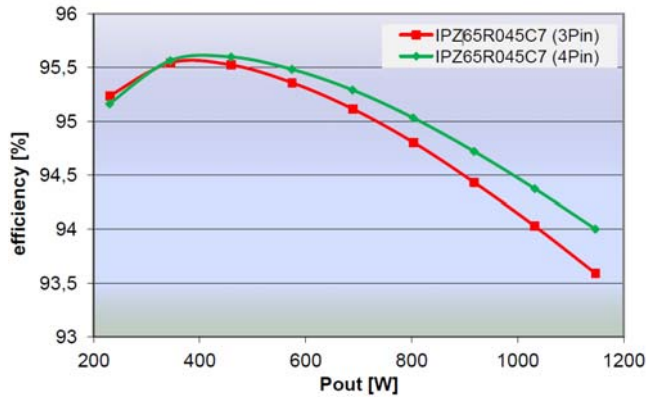


Figure 10: Efficiency comparison between a 4-pin and 3-pin device configuration for 90Vac input CCM PFC

One could quickly conclude from the measurements in fig. 9, that already from 50% load there is a real, tangible efficiency gain from faster switching transients, and at full load one can observe an efficiency increase on the order of 0.4%.

With an output power of 1150W, one can calculate the input power for 93.6% efficiency and subtract the calculated input power for 94% efficiency to arrive at a power dissipation difference in the switching MOSFET of ~5.2W!

Not only does this mean lower overall losses, but it can have a tangible impact on the requirement for heat sinking, and afford the designer some elements of freedom that cannot be otherwise obtained.

We can observe some differences between real measurements and simulation results. However, this is to be expected, since this hardware was implemented with a TO-247 device inserted only enough to still have the recommended 5mm of pin length from solder joint to package body. This means the effective source inductance is likely somewhat higher than the 2nH used in simulation. The use of different R_G can also be expected to have an impact, as can the difference between an ideal gate driver in case of the simulation and an existing physical one. Nevertheless there is still fairly good correlation between the theory, simulation and measurements, which all lead to the same conclusion: That with the most current generation of High Voltage silicon MOSFETs, a new benchmark is set in terms of achievable di/dt , which requires new thinking in both package design as well as circuit design.

V. Potential drawbacks

The fundamentally differentially driven V_{GS} requires some effort on the driver-side, which can no longer be ground referenced to the same common (GND) potential as the load and BUS capacitor. However, many solutions already exist in order to address very similar needs in a high-side MOSFET of a half- or full-bridge configuration. Practical

advice on how to easily deal with this approach using either isolated or non-isolated gate drivers is given in [1].

The Common Mode voltage spike incurred on the entire driver loop could be a concern, but also this topic is covered in said publication with pragmatic design strategies. Nevertheless it could be advantageous to limit this voltage spike, which calls for a lower source-inductance such as is offered in the ThinPAK8x8 leadless SMD package, which also employs the source-sense concept, and has potential for good cooling concepts as addressed in [5].

A high series package inductance – although not fundamentally limiting the di/dt beyond present HV Si chip capabilities – can also combine with other parasitic inductances around the current commutation loop to cause significant voltage drops during MOSFET turn-off. These parasitic voltage drops were previously prevented, or at least limited, by the feedback mechanism of the combined current branch in the 3-pin configuration discussed for turn-on transition in II. If unreasonably large total loop inductance exists, care must be taken to deal with the additional voltage stress across susceptible components in this loop (such as MOSFET and diode). For this reason it would be an advantage to lower the package source inductance by using a leadless SMD package rather than a leaded through-hole package if otherwise possible.

The arguments against a leadless SMD package at present are mostly based on thermal capabilities or lowest possible $R_{DS(on)}$, since the classic TO-247 can accommodate a physically larger Si chip. Advanced package concepts should combine excellent thermal capabilities – possibly double-sided cooling for added engineering freedom – with large die size accommodations and source-sense concept in a leadless SMD package affording a low total series inductance between drain and source for better total commutation loop inductance optimization.

VI. Conclusion

Since the introduction of the latest generation of high performance High Voltage Super Junction MOSFETs, the capabilities of the silicon chip in terms of handling fast current commutation transients far outpaces the fundamental di/dt limit set by a feedback mechanism caused by the ‘mixing’ of gate- and drain-currents in the package parasitic source inductance. The minimum possible losses during the turn-on current commutation phase in a hard-switching application was thus exemplified and theoretically shown to be limited by the source-inductance rather than silicon performance in both a traditional TO-247 package, but also in more low-inductance leadless SMD packages of today.

The introduction of the source-sense concept led to 4-pin packages, which were simulated against their 3-pin counterparts with an outcome similar as theorized.

A physical test board was used for A/B comparisons on the same silicon die operated under the same 90Vac input voltage CCM PFC conditions in both a 3-pin and 4-pin configuration. The results were as expected with significantly lowered switching losses at mid- to full load. Some difference compared with simulation was expected, since some parameters were slightly different, but the overall conclusion and expectation was in large agreement between 1st order theory (with some basic assumptions), simulation and measurements.

Some thoughts on potential drawbacks of the source-sense concept were offered with an expressed set of goals for a future advanced package.

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