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GaN and ZnO-based Materials and Devices

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Stephen Pearton
Editor

GaN and ZnO-based Materials and Devices

With 328 Figures

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Editor

Stephen Pearton

University of Florida
Materials Science and Engineering
100 Rhines Hall, 32611 Gainesville, USA
sppear@mse.ufl.edu

Series Editors:

Professor Robert Hull

University of Virginia
Dept. of Materials Science and Engineering
Thornton Hall
Charlottesville, VA 22903-2442, USA

Professor Chennupati Jagadish

Australian National University
Research School of Physics and Engineering
J4-22, Carver Building
Canberra ACT 0200, Australia

Professor Jürgen Parisi

Universität Oldenburg, Fachbereich Physik
Abt. Energie- und Halbleiterforschung
Carl-von-Ossietzky-Straße 9-11
26129 Oldenburg, Germany

Dr. Zhiming Wang

University of Arkansas
Department of Physics
835 W. Dickson St.
Fayetteville, AR 72701, USA

Professor R. M. Osgood, Jr.

Microelectronics Science Laboratory
Department of Electrical Engineering
Columbia University
Seeley W. Mudd Building
New York, NY 10027, USA

Springer Series in Materials Science ISSN 0933-033X

ISBN 978-3-642-23520-7

e-ISBN 978-3-642-23521-4

DOI 10.1007/978-3-642-23521-4

Springer Heidelberg Dordrecht London New York

Library of Congress Control Number: 2011945030

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Preface

The GaN materials system has applications in visible and UV light emitting devices and in high power, high temperature electronics. On the photonics side, the AlGaInN materials system, consisting of AlGaIn/GaN, InAlN/GaN, and InGaIn/GaN heterostructures and the GaN, AlN, and InN binaries, is widely used in blue/violet/white/UV light emitting diodes for stoplights and full color displays, blue and green lasers for use in high-density CD-ROM storage and high-resolution printers. The main applications for GaN-based high power microwave transistors are in phased array radar systems and wireless communication systems, while the low noise, radiation hard transistors can be used in high temperature sensors and spaceflight instrumentation. There have been many recent advances in this field, concerning sensors and nanostructure synthesis. Functional nanostructures are attracting much interest for use in sensing, energy harvesting and cell monitoring. In addition, there is a widespread interest in the use of ZnO in UV light emitters and flexible electronics. Flexible displays are attractive for portable devices such as smart phones, laptops, e-books, and wearable devices due to their lightweight, low power consumption, and being bendable. In defense applications, soldiers can use flexible display computers on the battlefield for communication and information access. Thin-film transistors (TFTs) are field effect transistors made by depositing thin films of amorphous Si, organics, or new inorganics based on ZnO for the semiconductor active layer. The channel region of a TFT is deposited onto a substrate such as glass, since the main market is in liquid crystal displays (LCDs). Since these types of substrates do not allow for high temperature processing, the TFT active region must be deposited at low temperature. Recently, indium zinc oxides (IZO) such as 90 wt% In_2O_3 –10 wt% ZnO and homogeneous $\text{In}_2\text{O}_3(\text{ZnO})_k$ ($k = 2, 3, 4, 5, 6, 7, 9, 11, 13, \text{ and } 15$) compounds have attracted significant attention as new candidates for transparent electrodes due to their good conductivity, high optical transparency, excellent surface smoothness, and low deposition temperature. One of the major challenges in the development of transparent thin-film transistors is to control the carrier concentration with high transparency in the active channel. For active channel materials, oxide semiconductors such as ZnO, $(\text{ZnO})_x(\text{SnO}_2)_{1-x}$, 90 wt% In_2O_3 –10 wt% ZnO, $\text{In}_2\text{O}_3(\text{ZnO})_2$, and InGaZnO_4 have been reported to

be as alternatives to α -Si:H in thin-film transistors. Recent results have shown that InZnO has high electron mobility even for room temperature deposition, allowing for use of cheap substrates such as glass for fabrication of TFTs with superior performance to a-Si(H)TFTs.

This book brings together experts in both the GaN and ZnO areas to provide the most up-to-date information on advances in these fields. The topics begin with growth of advanced III-Nitride structures, specifically non-polar growth and high Al content alloys, leading into devices such as green and UV LEDs, HEMT power devices, and sensors. Advances in nitride nanostructures and understanding of radiation defects in GaN are covered, followed by reviews of developments in synthesis and control of ZnO-based films and nanostructures. Finally, the use of amorphous, transparent conducting oxides for channels in TFTs on novel substrates is reviewed. The purpose of the book is to provide both a summary of the current state-of-the-art and directions for future research.

Gainesville, FL, USA
December 2011

S.J. Pearton

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Contributors

Pedro Barquinha CENIMAT-I3N, Departamento de Ciência dos Materiais, and CEMOP/UNINOVA, Faculdade de Ciências e Tecnologia, FCT, Universidade Nova de Lisboa, 2829-516, Caparica, Portugal

Xian-An (Andrew) Cao West Virginia University, Lane Department of Computer Science and Electrical Engineering, Morgantown, WV 26506-6070, USA, xacao@mail.wvu.edu

C.Y. Chang University of Florida, Department of Chemical Engineering, Gainesville, FL 32611, USA

K.H. Chen University of Florida, Department of Chemical Engineering, Gainesville, FL 32611, USA

Ruei-San Chen Graduate Institute of Applied Technology, National Taiwan University of Science and Technology, Taipei 106, Taiwan

Li-Chyong Chen Center for Condensed Matter Sciences, National Taiwan University, Taipei 106, Taiwan, chenkh@pub.iam.s.sinica.edu.tw

Victor Chen University of Florida, Department of Chemical Engineering, Gainesville, FL 32611, USA

H. Chen Department of Electrical and Computer Engineering, Rutgers University, 94 Brett Road, Piscataway, NJ 0885, USA

Leonid Chernyak Department of Physics, University of Central Florida, Orlando, FL 32816, USA, chernyak@physics.ucf.edu

T. Paul Chow Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180, USA, chowt@rpi.edu

B.H. Chu University of Florida, Department of Chemical Engineering, Gainesville, FL 32611, USA

Zinovy Dashevsky Department of Physics, University of Central Florida, Orlando, FL 32816, USA

Jeff Davis College of Physical and Mathematical Sciences, Australian National University, Canberra, ACT 0200, Australia

Alex Dobrinsky Sensor Electronic Technology, Inc., Columbia, SC 29209, USA, adobrinsky@s-et.com

Elena Flitsyan Department of Physics, University of Central Florida, Orlando, FL 32816, USA

Elvira Fortunato CENIMAT-13N, Departamento de Ciência dos Materiais, and CEMOP/UNINOVA, Faculdade de Ciências e Tecnologia, FCT, Universidade Nova de Lisboa, 2829-516, Caparica, Portugal, elvira-fortunato@fct.unl.pt

Abhijit Ganguly Center for Condensed Matter Sciences, National Taiwan University, Taipei 106, Taiwan

Remis Gaska Sensor Electronic Technology, Inc., Columbia, SC 29209, USA

Jung Han Department of Electrical Engineering, Yale University, 15 Prospect Street, BCT 517, New Haven, CT 06511, USA, jung.han@yale.edu

Kuei-Hsien Center for Condensed Matter Sciences, National Taiwan University, Taipei 106, Taiwan, Chen chenlc@ntu.edu.tw
and
Institute of Atomic and Molecular Sciences, Academia Sinica, Taipei 106, Taiwan

C. Jagadish College of Physical and Mathematical Sciences, Australian National University, Canberra, ACT 0200, Australia, Chennupati.Jagadish@anu.edu.au

Wayne Johnson Kopin Corporation, 125 North Drive, Westboro, MA 01581, USA, Wayne-Johnson@kopin.com

Hongxing Jiang Texas Tech University, Electrical and Computer Engineering Department, Lubbock, TX 79409-3102, USA, hx.jiang@ttu.edu

Jihyun Kim Department of Chemical and Biological Engineering, College of Engineering, Korea University, Anam-dong 5-1, Sungbuk-gu, Seoul 136-701, South Korea, hyunhyun7@korea.ac.kr

Z. Li Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180, USA

Jingyu Lin Texas Tech University, Electrical and Computer Engineering Department, Lubbock, TX 79409-3102, USA, jingyu.lin@ttu.edu

Yicheng Lu Department of Electrical and Computer Engineering, Rutgers University, 94 Brett Road, Piscataway, NJ 0885, USA, ylu@ece.rutgers.edu

Rodrigo Martins CENIMAT-I3N, Departamento de Ciência dos Materiais, and CEMOP/UNINOVA, Faculdade de Ciências e Tecnologia, FCT, Universidade Nova de Lisboa, 2829-516 Caparica, Portugal

Edwin Piner Texas State University, San Marcos, Department of Physics, 601 University Dr., San Marcos, TX 78666, USA, epiner@txstate.edu

B.N. Pantha Texas Tech University, Electrical and Computer Engineering Department, Lubbock, TX 79409-3102, USA

S.J. Pearton Department of Materials Science and Engineering, University of Florida, Gainesville, FL 32611, USA, spear@mse.ufl.edu

Alexander Polyakov Institute of Rare Metals, B. Tolmachevsky 5, 119017 Moscow, Russia, aypolyakov@gmail.com

Fan Ren University of Florida, Department of Chemical Engineering, Gainesville, FL 32611, USA, ren@che.ufl.edu

P.I. Reyes Department of Electrical and Computer Engineering, Rutgers University, 94 Brett Road, Piscataway, NJ 0885, USA

Max Shatalov Sensor Electronic Technology, Inc., Columbia, SC 29209, USA

Michael Shur Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180, USA, shurm@rpi.edu

Michael Snure Nanostructured Materials Research Laboratory, Department of Materials Science and Engineering, University of Utah, Salt Lake City, UT 84112, USA

Paul Slusser Nanostructured Materials Research Laboratory, Department of Materials Science and Engineering, University of Utah, Salt Lake City, UT 84112, USA

Qian Sun Department of Electrical Engineering, Yale University, 15 Prospect Street, BCT 517, New Haven, CT 06511 USA

Ashutosh Tiwari Nanostructured Materials Research Laboratory, Department of Materials Science & Engineering, University of Utah, Salt Lake City, UT 84112, USA, tiwari@eng.utah.edu

David Toledo Nanostructured Materials Research Laboratory, Dept. of Materials Science & Engineering, University of Utah, Salt Lake City, UT 84112 USA

J. Zhong Department of Electrical and Computer Engineering, Rutgers University, 94 Brett Road, Piscataway, NJ 0885, USA

Chapter 8

Recent Advances in High-Voltage GaN MOS-Gated Transistors for Power Electronics Applications

T. Paul Chow and Z. Li

Abstract The recent progress and present status of the development of high-voltage lateral power GaN field-effect transistors for power switching applications are reviewed and discussed. The basic device structures explored and the performance improvement in blocking voltage and specific on-resistance over the last few years are presented. The technical challenges and reliability issues that still need to be addressed are pointed out.

8.1 Introduction

Similar to SiC, GaN has many attractive material properties, such as high breakdown field, good bulk electron mobility, and thermal conductivity, which make it suitable for high-power switching as well as high-frequency amplifying electronic applications [1] (see Table 8.1). On the other hand, thin layers of GaN have been successfully heteroepitaxially grown, with suitable AlN/GaN buffer layers, on silicon, sapphire, and SiC substrates. In addition, GaN has demonstrated two-dimensional electron gas (2DEG) at heterojunction interfaces (AlGaIn/GaN, AlInN/GaN) that has very high electron mobilities ($\sim 2,000 \text{ cm}^2/(\text{V s})$). Furthermore, the fabrication processing steps for GaN devices have thermal budgets that are compatible with state-of-art silicon nanometer CMOS foundries and can exploit these infrastructures for cost-effective, large-scale GaN power device commercialization and manufacturing.

T. Paul Chow (✉) · Z. Li

Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute,
Troy, NY 12180, USA
e-mail: chowt@rpi.edu

S. Pearton (ed.), *GaN and ZnO-based Materials and Devices*,
Springer Series in Materials Science 156, DOI 10.1007/978-3-642-23521-4_8,
© Springer-Verlag Berlin Heidelberg 2012

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Table 8.1 Semiconductor properties

Material	E_g (eV)	Direct/ Indirect	n_i (cm^{-3})	ϵ_r	μ_n ($\text{cm}^2 / (\text{V s})$)	E_c ($\text{cm}^2 / (\text{V s})$)	v_{sat} (10^7 cm/s)	λ (W/cm – K)
Si	1.1	I	1.5×10^{10}	11.8	1,350	0.3	1.0	1.5
2H-Ga/n	3.39	D	1.9×10^{-10}	9.9	1,000 ^a 2,000 ^{**}	3.3 [*]	2.5	1.3
3C-GaN	3.27	D	8×10^{-9}	9.9	1,000	1 [*]	2.5	1.3
3C-SiC	2.2	I	6.9	9.6	900	1.2 [*]	2.0	4.5
4H-SiC	3.26	I	8.2×10^{-9}	10	720 ^a 650 ^c	2.0	2.0	4.5
6H-SiC	3.0	I	2.3×10^{-6}	9.7	370 ^a 50 ^c	2.4	2.0	4.5

Note: a – mobility along *a*-axis, c-mobility along *c*-axis, ^{*}Estimated value, ^{**}2DEG

A few years ago, discrete RF GaN power HEMTs on silicon substrates as well as high-voltage discrete power GaN Schottky diodes (600 V, 4–8 A) on sapphire substrates have been commercialized [2–4]. More recently, high-voltage (200 V, 12 A) GaN power transistors on silicon substrates are becoming commercially available [5, 6].

In this paper, we will present the recent advances in high-voltage GaN power transistors. These transistors can function both as discrete power switches or integrated with other logic or analog device elements to form power ICs.

8.2 Device Structures and Design

Most of the high-voltage GaN power transistors reported are lateral in structure because the GaN/AlGa_n epitaxial layers are grown on insulating or high-resistivity substrates. The schematic cross-sections of several high-voltage lateral GaN transistor structures are shown in Fig. 8.1a–d. Power GaN transistors are interesting in that they can either resemble that of lateral silicon power MOSFETs or AlGaAs/GaAs Schottky-gate HEMTs. Besides a MOS channel, lateral high-voltage GaN MOSFETs have a lightly doped drain region to support high-drain voltages and ion-implanted source/drain regions. By contrast, power AlGa_n/GaN HEMTs have Schottky-gate-controlled heterojunction 2DEG channel, a heterojunction drift region and alloyed source/drain contacts. In either type of transistors, the surface electric field must be suppressed so as to maximum the blocking voltage. The MOS Channel-HEMT (MOSC-HEMT, previously called hybrid MOS-HEMT [7]) combines the best features of the MOSFET and HEMT.

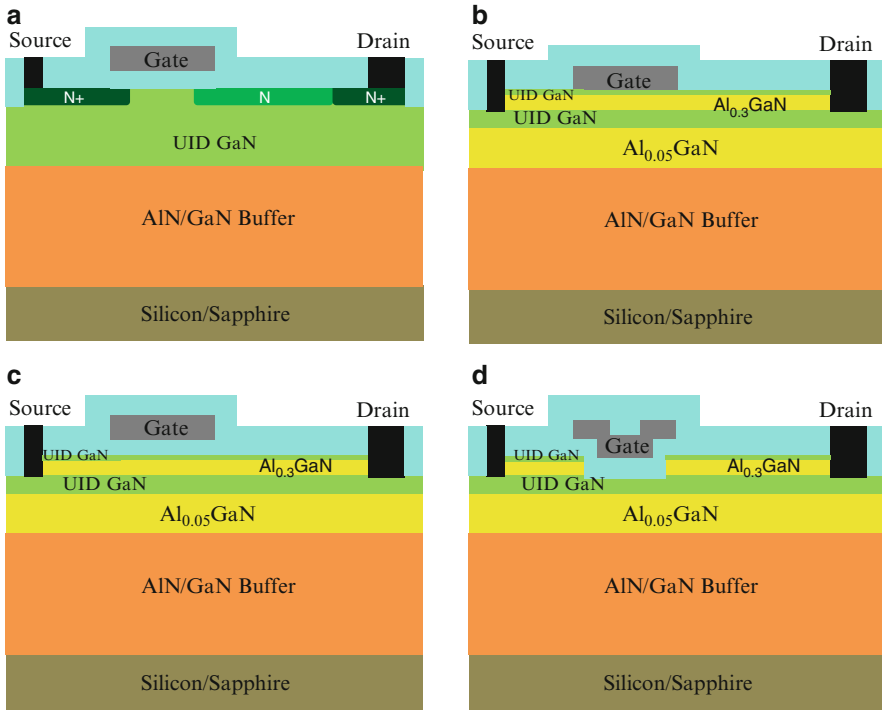


Fig. 8.1 Schematic cross-sections of high voltage lateral GaN: (a) MOSFET, (b) HEMT, (c) MOS-HEMT, and (d) MOS-channel HEMT (MOSC-HEMT)

8.3 Device Design

The REShaping of Surface Field (RESURF) principle [8] is employed to maximize the breakdown voltage (BV) of lateral high-voltage power devices since it can suppress the surface electric field and force the avalanche process to be initiated in the bulk junction region. The key design parameter is the space charge per unit area ($N_{\text{RESURF}} = \int N_{\text{epi}} dx$) in the drift region. Adoption of an optimum N_{RESURF} leads to inherent lateral and vertical electric field shaping due to non-planar, two- or three-dimensional depletion action originating from interactions of lateral and vertical pn or MIS junctions [9–11].

To determine the optimum RESURF charge density (N_{RESURF}), we use Gauss' Law to yield

$$\int \xi \times dA \approx \xi \times A = - \int \rho dV / \epsilon_s = -Q / \epsilon_s = -qN / \epsilon_s,$$

where ξ is the electric field in the depleted drift region, A the area, Q the total amount of space charges enclosed, and ϵ_s the semiconductor permittivity. Since

$N_{\text{RESURF}} = Q_{\text{RESURF}}/qA \approx \xi\epsilon_s/q$ and $\xi \approx 1.5 \times 10^5 \text{V/cm}$ in silicon, the optimum N_{RESURF} is about $10^{12}/\text{cm}^2$, but, for GaN and SiC, where the avalanche field is ten times higher, it is $10^{13}/\text{cm}^2$. Additional features, such as field plates, are needed to further reduce surface field crowding, either near the gate/source or drain side of the device. In addition, the RESURF action can be achieved in many ways (a) space charge can be introduced with in situ epi doping, ion implantation, or polarization charges, and (b) the substrates can be semiconductors (like Si or GaN), insulators (like sapphire), or semiconductor on insulator/semiconductor (SOI) structures (like silicon/oxide/silicon or GaN/AlN/silicon). Here, we are focusing on lateral GaN power devices on SOI substrates consisting of AlGaIn/GaN- or GaN-active epitaxial layers/AlN, GaN- or AlGaIn-insulating buffer layers on silicon substrates. Interestingly, the space charges in the AlGaIn/GaN case arise from polarization charges and with an aluminum mole fraction of about 22% and an AlGaIn/GaN layer thickness of 20 nm; these polarization charges are about $10^{13}/\text{cm}^2$ in concentration [12]. Consequently, such a structure can be called a “natural” RESURF structure, and, in the case of infinite number of parallel RESURF layers, a natural superjunction structure [13]. To illustrate the impact of balanced space charges in the drift region, we have simulated two structures, one with uncompensated positive charges at the AlGaIn/GaN interface and the other with balanced positive and negative charges on the two AlGaIn interfaces. The equipotential line profiles, shown in Fig. 8.2, clearly indicate field crowding at the gate corner in the former but much more uniform electric field in the latter [14].

While employment of the RESURF approach results in minimum drift region length for a given BV, it also leads to a minimum specific on-resistance ($R_{\text{on,sp}}$). In particular, using an one-dimensional pn junction breakdown theory, one deduce a $R_{\text{on,sp}} \propto (\text{BV})^{2.5}$ relationship for unipolar rectifiers or transistors and we almost always find this relationship to be applicable in vertical discrete devices. By contrast, lateral RESURF-type unipolar devices have a $R_{\text{on,sp}} \propto (\text{BV})^n$, where n is between 1.1 and 1.5, significantly smaller than that of vertical devices. In addition,

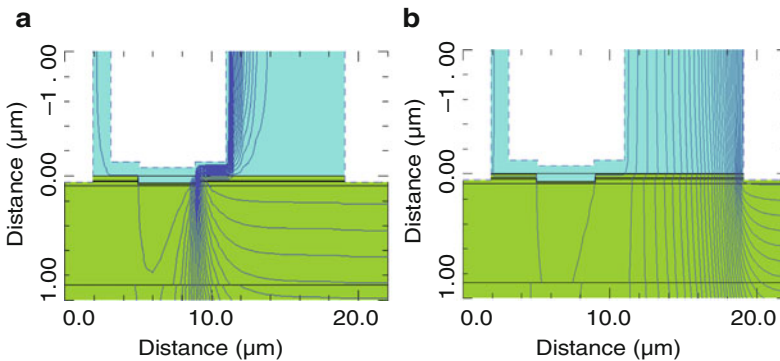


Fig. 8.2 Simulated equivalent potential line distribution for 1-zone RESURF MOSC-HEMT: (a) without GaN cap at V_{DS} of 40 V and (b) with GaN cap at V_{DS} of 646 V

for power FET structures, we also need to consider the on-resistance component (R_{ch}) contributed from the channel region and this resistance is directly related to the field-effect carrier mobility achievable from a particular FET process. The relative on-resistance contributions from the channel and drift regions are strongly dependent on the blocking or BV desired. In 600-V lateral silicon RESURF devices, the drift region resistance dominates. However, in lateral GaN RESURF devices of the same blocking voltage, the on-resistances from the MOS channel, relative to the resistance of the drift region, is becoming increasingly dependent on the channel length and field-effect mobility. Consequently, the choice of channel region design and technology in GaN power FETs plays a major role in ultimate device performance and proper channel scaling is necessary and critical with blocking voltages below 600 V. To illustrate these considerations, the specific on-resistance versus blocking voltage for GaN MOSFETs, using the set of device and material parameters assumed in Table 8.2, is shown in Fig. 8.3 [15]. Also, included for comparison is the one-dimensional bulk vertical GaN device performance projection.

For power MOSC-HEMTs, the channel resistance has become so dominant that scaling it to below submicron dimensions is necessary. We have performed a systematic channel scaling study and found that scaling the channel length to below 1 μm is needed to achieve specific on-resistance below 10 $\text{m}\Omega - \text{cm}^2$ [16], as shown in Fig. 8.4. It can also be noted that the $R_{\text{on,sp}}$ of the conventional HEMTs is less sensitive to the channel length because of a higher channel mobility, but it is more difficult to achieve a sufficiently large positive threshold voltage for enhancement mode operation.

Table 8.2 Device parameters for lateral GaN MOSFETs in calculating the breakdown voltage/on-resistance tradeoff

$L_G(\mu\text{m})$	$N_{\text{s,CH}}(\text{cm}^{-2})$	$\mu_{\text{CH}}(\text{cm}^2/(\text{V s}))$	$E_{\text{RES}}(\text{V}/\mu\text{m})$	$\Phi_{\text{RES}}(\text{cm}^{-2})$	$\mu_{\text{RES}}(\text{cm}^2/(\text{V s}))$
3	1×10^{13}	540	100	1×10^{13}	900

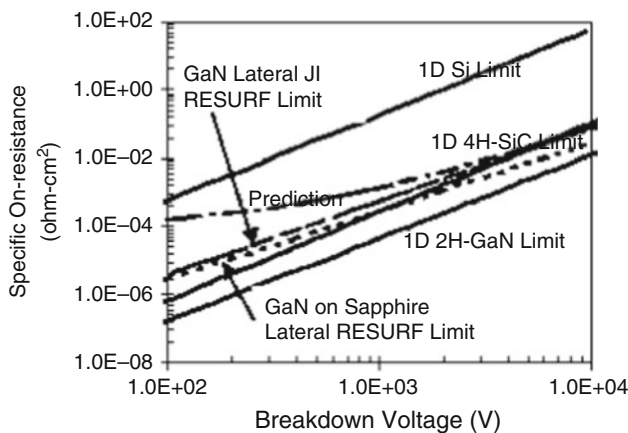


Fig. 8.3 Projections of the performance of GaN devices

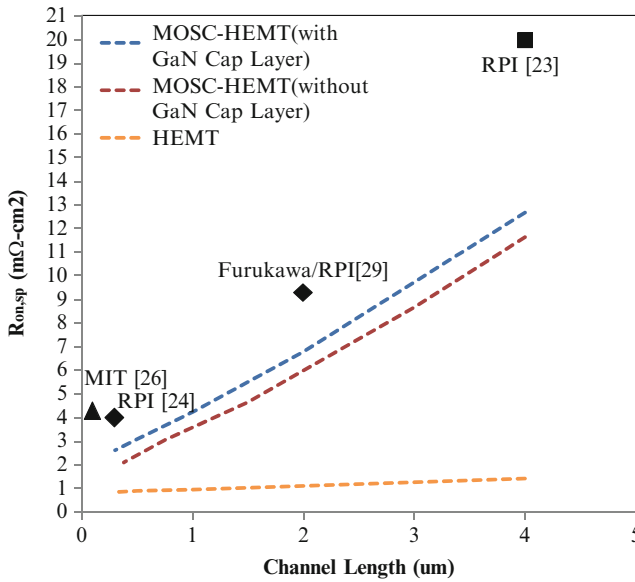


Fig. 8.4 $R_{on,sp}$ versus MOS channel length from experiments and simulations for HEMT and MOSC-HEMT without or with GaN cap layer

8.4 Experimental Results

The first high-voltage GaN power transistor is a MOS-HEMT on sapphire, with a $R_{on,sp}$ of $1.7 \text{ m}\Omega - \text{cm}^2$ and a BV of 1.3 kV [17]. Subsequently, there are many attempts to refine the device structures and process to improve its characteristics. The main structural variants include insertion of a better dielectric between the Schottky metal and AlGaIn layer, varying Al mole fraction in the AlGaIn layer, and better surface passivation layer. The device parameters optimized are: BV, off-state leakage current, gate leakage, and frequency-dependent current dispersion. However, most of the off-state leakage current reported are often excessive (usually, the BV was measured at 1 mA/mm) [18]. Recently, the situation has been improved, and, in one case, accomplished with an in situ grown surface SiN passivation layer [19]. The highest BV for a GaN HEMT reported is 10.4 kV, with a specific on-resistance of $186 \text{ m}\Omega - \text{cm}^2$ [20]. It is interesting to note that all the high-voltage commercial GaN power transistors so far base on the basic HEMT device structure approach, though mostly on silicon substrates [5, 6].

While most of the GaN transistors demonstrated utilized a heterojunction channel and Schottky (sometimes in conjunction with a dielectric) gate (see Table 8.3), we have focused on developing an enhancement mode MOS channel technology. Previously, we have successfully optimized the GaN/SiO₂ interface using a PECVD oxide followed with a high-temperature (1,000°C) nitrogen annealing. We first characterize the MOS capacitors and found the extracted interface state densities to

Table 8.3 Summary of GaN high-voltage transistors

Device	BV (V)	Ron, sp (mΩ × cm ²)/Imax(A)	Other features	Research group/company	References
HEMT	1,300	1.7	SiO ₂ /Si ₃ N ₄ as gate insulator L _{GD} = 20 μm	UCSB	N.Q. Zhang et al., IEDM (2001)
HEMT	8,300	186	L _{GD} = 125 μm, field plate	Panasonic	Y. Uemoto et al., IEDM (2007)
HEMT (GIT)	800	2.6	L _{GD} = 7.5, V _{th} = 1 V, p-AlGaIn/AlGaIn under gate	Panasonic	Y. Uemoto et al., TED (2007)
HEMT	1,800	7, 120 A	L _{GD} = 15 μm, Si substrate	Furukawa	N. Ikeda et al., ISPSD (2008)
HEMT	1,580	4	L _{GD} = 16 μm	Cornell	J. Shi et al., PSS(C) (2008)
HEMT	100	300 mA/mm	V _{th} = 0.75 V, Fluoride plasma treatment	HKUST	D. Song et al., EDL (2007)
HEMT	1,500	5.3	L _{GD} = 20 μm, Si substrate transfer	MIT	B. Lu et al., EDL (2010)
HEMT	2,200	18	L _{GD} = 20 μm, Si substrate removal	IEMC	P. Srivastava et al., EDL (2011)
HEMT	1,100	6.1	L _{GD} = 22 μm	U. of Sheffield/Powdec	A. Nakajima et al., EDL (2011)

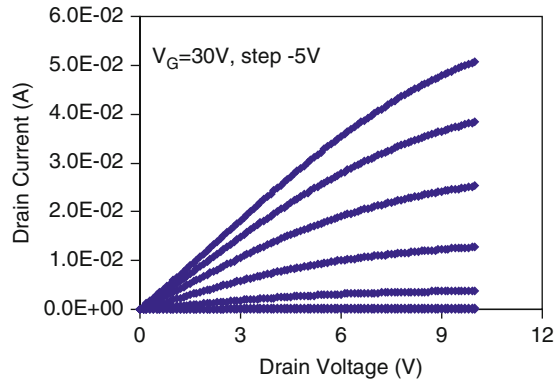
(continued)

Table 8.3 continued

Device	BV (V)	Ron, sp (mΩ × cm ²)/I _{max} (A)	Other features	Research group/company	References
HEMT	10,400	186	$L_{GD} = 125\text{ }\mu\text{m}$, thick poly-AlN passivation $V_{th} = 3\text{ V}$, implanted RESURF region	Panasonic	M. Yanagihara et al., PSS(A) (2009)
MOSFET	1,570	2.5 A	$V_{th} = 3\text{ V}$, implanted RESURF region	RPI	W. Huang et al., ISPSD (2008)
MOSFET	770 forward	80 mA/mm	$V_{th} = 5.1\text{ V}$ Monolithic	Rohm RPI	H. Otake et al., JJAP (2007)
MOSFET			Schottky pair, reverse blocking, $L_{GD} = 18\text{ }\mu\text{m}$		W. Huang et al., ISPSD (2007)
MOSFET	1,050 reverse 2,500	30	$L_{GD} = 30\text{ }\mu\text{m}$, field plates, lower temperature anneal	RPI	W. Huang et al., ISPSD (2008)
			$L_{GD} = 20\text{ }\mu\text{m}$, $V_{th} = 2\text{ V}$, higher temperature anneal		
			$L_{GD} = 16\text{ }\mu\text{m}$ $L_{GD} = 15\text{ }\mu\text{m}$, $V_{th} = 0.5\text{ V}$, Si substrate		
MOSFET	730	34	$L_{GD} = 16\text{ }\mu\text{m}$	RPI	W. Huang et al., ISPSD (2009)
MOS-HEMT	1,000	5	$L_{GD} = 15\text{ }\mu\text{m}$, $V_{th} = 0.5\text{ V}$, Si substrate	NEC	K. Ota et al., IEDM (2009)

MOS-HEMT	320	800 mA/mm	$L_{GD} = 5\text{ }\mu\text{m}$, $V_{th} = 3\text{ V}$, $L_{ch} = 0.8\text{ }\mu\text{m}$, GaN/AlN/GaN cap	Fujitsu	M. Kanamurua et al., EDL (2010)
MOS-HEMT	1,200	9	$L_{GD} = 5\text{ }\mu\text{m}$, $V_{th} = 0.64\text{ V}$, plasma treated gate	HRL	R. Chu et al., EDL (2011)
MOS-HEMT	640	3.8	$L_{GD} = 12\text{ }\mu\text{m}$, $V_{th} = 1\text{ V}$	Toshiba	M. Kuraguchi et al., PSS(c) 2007
MOS-HEMT		20	$L_{GD} = 20\text{ }\mu\text{m}$, $V_{th} = 2.5\text{ V}$	RPI	W. Huang et al., ISPSD (2008)
MOS-HEMT	1,300		$L_{GD} = 24\text{ }\mu\text{m}$, field plate	RPI	K. Tang et al=, ISPSD (2009)
MOS-HEMT	650	9.3, 100A	$L_{GD} = 15\text{ }\mu\text{m}$, $V_{th} = 2.7\text{ V}$, Si substrate	Furukawa/RPI	Kambayashi et. Al. and T.P Chow, SSE (2010)
MOS-HEMT	400	200 mA/mm	$L_{GD} = 6.5\text{ }\mu\text{m}$, $V_{th} = 5.2\text{ V}$, Si substrate	Sharp	T. Oka et al., EDL (2008)
MOS-HEMT	643	4.3	$L_{GD} = 18\text{ }\mu\text{m}$, $V_{th} = 2.9\text{ V}$, $L_{ch} = 0.1\text{ }\mu\text{m}$, Si substrate	MIT	B. Lu et al., EDL (2010)

Fig. 8.5 Output I - V characteristics of GaN MOSC-HEMT with 3- μm channel length and 20- μm RESURF length



be very low and approaching that in Si MOS [21]. Subsequently, we have, using this GaN MOS process, experimentally demonstrated a record high field-effect inversion electron mobility of $167 \text{ cm}^2/(\text{V s})$ in GaN MOSFETs with ion-implanted source/drain regions. In addition, since then, we have demonstrated several high-voltage enhancement-mode GaN lateral power MOS-gated FET structures (MOSFETs and MOSC-HEMTs) on sapphire substrates [7, 15, 22–25]. These prototype transistors have specific on-resistances up to more than $50\times$ better than the silicon counterparts at the same blocking voltage range (600–2.5 kV) and off-state leakage current density more than $100\times$ less than that in conventional HEMTs. The main advantages of the MOSC-HEMT is the low off-state leakage and low gate leakage current, often several orders of magnitude less than that of conventional HEMTs. On the other hand, the poorer channel mobility in the MOS channel requires the downscaling of the channel length, down to submicron dimensions, to minimize the dominance of the channel on-resistance [24, 26].

The output I - V characteristics of a 3- μm GaN MOSC-HEMT on sapphire substrate with specific on-resistance of $20 \text{ m}\Omega\text{-cm}^2$ are shown in Fig. 8.5 [23]. We have recently demonstrated a 0.3- μm channel GaN MOSC-HEMT on silicon substrate with specific on-resistance of $4 \text{ m}\Omega\text{-cm}^2$ and a BV over 350 V [24]. Hence, the on-state performance of the HEMT and MOSC-HEMT is now quite similar. In addition, we have found that under avalanche conditions, the MOSC-HEMT is survivable [24] when the drain current is limited but we have not found a report that a HEMT or MOS-HEMT has survived such an avalanche test.

8.5 Technical Challenges and Reliability

The key technical challenges for GaN power FET development and commercialization include current collapse, avalanche capabilities, device ruggedness, threshold voltage control, and long-term reliability.

Drain current collapse under ac frequencies is a well-known phenomenon and there are probably many causes. Minimization of surface electric field with field plates and reduced polarization charges are among the many ways to control it (see, for example, [24, 27]). We would like to point out that our GaN MOS-gated FETs do not exhibit, while MOSC-HEMTs do exhibit, the current collapse behavior commonly seen in AlGaIn/GaN HEMTs at room temperature. The temperature dependence of the current collapse behavior is also quite different, indicating the complexities of this degradation phenomenon [28]. Many ways have been suggested to control or increase the threshold voltage control in either MOS-HEMT or MOSC-HEMT (see, for example, [27]) but more efforts are needed to make it as controllable as that in state-of-art Si nanometer MOSFETs.

8.6 Summary

We have reviewed the recent advances of high-voltage lateral GaN power FETs. Its successful commercialization will impact many consumer and industrial power electronic applications, resulting in significant energy efficiency and conservation efforts.

Acknowledgement This work was supported by SRC (Task 1961.001) and the NSF ERC on Smart Lighting (Award #EEC-0812056).

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