
POWER ELECTRONICS HANDBOOK

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POWER ELECTRONICS HANDBOOK

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Preface

Introduction

The purpose of *Power Electronics Handbook* is to provide a reference that is both concise and useful for engineering students and practicing professionals. It is designed to cover a wide range of topics that make up the field of power electronics in a well-organized and highly informative manner. The Handbook is a careful blend of both traditional topics and new advancements. Special emphasis is placed on practical applications, thus, this Handbook is not a theoretical one, but an enlightening presentation of the usefulness of the rapidly growing field of power electronics. The presentation is tutorial in nature in order to enhance the value of the book to the reader and foster a clear understanding of the material.

The contributors to this Handbook span the globe, with fifty-four authors from twelve different countries, some of whom are the leading authorities in their areas of expertise. All were chosen because of their intimate knowledge of their subjects, and their contributions make this a comprehensive state-of-the-art guide to the expanding field of power electronics and its applications covering:

- the characteristics of modern power semiconductor devices, which are used as switches to perform the power conversions from ac-dc, dc-dc, dc-ac, and ac-ac;
- both the fundamental principles and in-depth study of the operation, analysis, and design of various power converters; and
- examples of recent applications of power electronics.

Power Electronics Backgrounds

The first electronics revolution began in 1948 with the invention of the silicon transistor at Bell Telephone Laboratories by Bardeen, Brattain, and Shockley. Most of today's advanced electronic technologies are traceable to that invention, and

modern microelectronics has evolved over the years from these silicon semiconductors. The second electronics revolution began with the development of a commercial thyristor by the General Electric Company in 1958. That was the beginning of a new era of *power electronics*. Since then, many different types of power semiconductor devices and conversion techniques have been introduced.

The demand for energy, particularly in electrical forms, is ever-increasing in order to improve the standard of living. *Power electronics* helps with the efficient use of electricity, thereby reducing power consumption. Semiconductor devices are used as switches for power conversion or processing, as are solid state electronics for efficient control of the amount of power and energy flow. Higher efficiency and lower losses are sought for devices for a range of applications, from microwave ovens to high-voltage dc transmission. New devices and power electronic systems are now evolving for even more effective control of power and energy.

Power electronics has already found an important place in modern technology and has revolutionized control of power and energy. As the voltage and current ratings and switching characteristics of power semiconductor devices keep improving, the range of applications continues to expand in areas such as lamp controls, power supplies to motion control, factory automation, transportation, energy storage, multi-megawatt industrial drives, and electric power transmission and distribution. The greater efficiency and tighter control features of power electronics are becoming attractive for applications in motion control by replacing the earlier electro-mechanical and electronic systems. Applications in power transmission include high-voltage dc (VHDC) converter stations, flexible ac transmission system (FACTS), and static-var compensators. In power distribution these include dc-to-ac conversion, dynamic filters, frequency conversion, and Custom Power System.

Almost all new electrical or electromechanical equipment, from household air conditioners and computer power supplies to industrial motor controls, contain power electronic circuits

and/or systems. In order to keep up, working engineers involved in control and conversion of power and energy into applications ranging from several hundred voltages at a fraction of an ampere for display devices to about 10,000 V at high-voltage dc transmission, should have a working knowledge of power electronics.

Organization

The Handbook starts with an introductory chapter and moves on to cover topics on power semiconductor devices, power converters, applications and peripheral issues. The book is organized into six areas, the first of which includes chapters on operation and characterizations of power semiconductor devices: power diode, thyristor, gate turn-off thyristor (GTO), power bipolar transistor (BJT), power MOSFET, insulated gate bipolar transistor, MOS controlled thyristor (MCT), and static induction devices.

The next topic area includes chapters covering various types of power converters, the principles of operation and the methods for the analysis and design of power converters. This also includes gate drive circuits and control methods for power converters. The next three chapters cover applications in power supplies, electronics ballasts, renewable energy sources, HVDC transmission, VAR compensation, and capacitor charging.

The following six chapters focus on the operation, theory and control methods of motor drives, and automotive systems. We then move on to two chapters on power quality issues and active filters, and two chapters on computer simulation, packaging and smart power systems.

Locating Your Topic

A table of contents is presented at the front of the book, and each chapter begins with its own table of contents. The reader should look over these tables of contents to become familiar with the structure, organization, and content of the book.

Audience

The Handbook is designed to provide both students and practicing engineers with answers to questions involving the wide spectrum of power electronics. The book can be used as a textbook for graduate students in electrical or systems engineering, or as a reference book for senior undergraduate students and for engineers who are interested and involved in operation, project management, design, and analysis of power electronics equipment and motor drives.

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35.1 Introduction

A continual endeavor in power electronics is to increase power density. This is achieved by shrinking component size, moving components closer and reducing component count. During the last two decades circuit frequencies increased sharply to shrink component dimensions. Improved thermal management and physical packaging materials brought components closer. And finally, increased integration of functions at the semiconductor and package levels reduced component count. This has been marked in the microelectronics world by “system on chip” (SOC) and “system on package” (SOP), all addressing higher densities and all applicable to power electronic systems.

The latter approach of “functional integration” has been ongoing for decades. Until the 1980s nearly all such integration was done at the packaging level melding control and power processing. The term “smart power” (within the context of power electronic conditioning) applied in the 1960s–1970s to the integration of computers and microprocessors into large rectifier and converter cabinets. With the advent of high-voltage-silicon integrated circuits more functionality was brought directly to the power semiconductors, and in the 1980s–1990s the term applied mostly to smart

power semiconductors. In the late 1990s there was a move back to hybrid integration following the trend to SOP. The term “Smart Power” has also been commercially associated with power management circuits.

From a designer’s perspective, “functional integration” exists in a *packaging continuum* with “smart power” as a subset, dependent on the definition in vogue. To take advantage of “functional integration” the designer, in reverse thinking, partitions or modularizes circuits and functions to achieve the most cost-effective approach that meets a set of required performance specifications. This chapter provides background information, framework and procedures to produce partitioning and functional integration.

35.2 Background

Circuits are typically designed with a pre-determined idea of what packaging technologies will be used. The technologies range from silicon integration of subcircuit functions to multiple boards in a rack. Partitioning a circuit packaged in one technology, such as all silicon, is straightforward. Partitioning a circuit in multiple technologies is much more difficult since higher performing technologies duplicate

aspects of lower technologies. The duplication geometrically increases parameter trade-offs and causes wasted packaging cost. Considerable literature exists about the technical characteristics of packaging materials and processes. (A table of characteristics is provided later.) Also, a study on the Status on Power Electronics Packaging (STATPEP) [1] identifies metrics to further evaluate the relative technical merits.

To optimize the use of multiple technologies in functional integration, a structured method should be used. A full-cost model for various technologies is used as a basis to produce a comparative cost diagram. The diagram allows intermixing of high and low performance technologies based on surface density, which is interpreted as circuit area and, hence, a partition. An example is given in Section 35.7 to demonstrate the method using a 2.2 kW motor drive module product.

The method is also applied to product modularization, i.e. system partitioning where a specific function is used across several products. A module can represent functional integration within a packaging technology or use multiple packaging technologies to create integrated power modules (IPMs) or power electronic building blocks (PEBBs). The importance of modularization is to increase product volume to lower cost. The cost model includes variations based on volume.

This partitioning approach matches user requirements to “Levels of Packaging” as defined in the “Framework for Power Electronics Packaging” [2] and provides optimum integration of packaging levels for a product. The Framework also identifies critical technical issues that need to be considered in

evaluating technical performance. This partitioning approach looks at electrical, magnetic, thermal and mechanical issues (multiple energy forms).

35.3 functional Integration

Figure 35.1 shows a 2.2 kW ac motor drive. Functional integration requires that the system be partitioned both electrically and physically. The systems integrator is usually an electrical designer and the first partitioning is usually electrical. The *electrical* partitions and distributed power losses are also shown in the figure. The physical partitioning, or packaging, involves different components with different functions ranging from fine-line control to high-current, high-loss power processing. Several partitions can be pursued. The Line-communications and Motor-control Blocks can use a signal-level packaging approach, such as all-silicon ASIC (application-specific integrated circuit), or discrete components on an epoxy-glass (FR-4) or insulated-metal substrates (IMS). If the Power Supply and Control Blocks are to be combined, an SMT approach cannot accommodate bulky storage components in the power supply. Hence, a through-hole approach is considered for part or both blocks. Regardless, such tradeoffs can be nearly endless. A structured method needs to be used to establish essential requirements and guide circuit and system partitioning. The method described here is based on characterizing and grouping the components, eval-

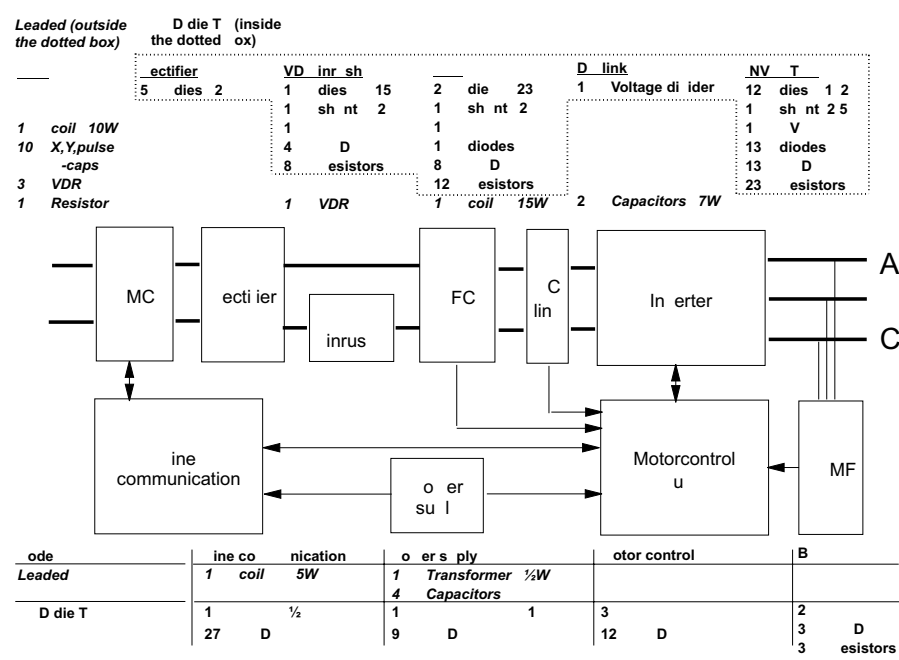


FIGURE 35.1 Block diagram of a 2.2 kW motor drive module. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

uating the cost and technical constraints, and then matching packaging technologies to the groupings. All this is set against a set of comprehensive user requirements.

35.3.1 Setting User Requirements

Effective systems design, including packaging, relies on accurate and comprehensive user requirements that are established through a formal structure. A brief review is presented here. The requirements are divided into five business taxonomies that can be considered comprehensive. These are: financial, environmental, legal, social and technical. The taxonomies are matrixed with three characteristics of requirements: assumed, articulated and unexpected. Assumed requirements are basic requirements for a product, process or service to be acceptable to all end users. Articulated requirements discern one user from another. The unexpected requirements are excitors that make the product, process or service unique and competitive.

Of the above, only technical, articulated, user requirements are used in this discussion.

The technical requirements are further categorized to reflect the electrophysical nature of packaging. The categories are: chemical, electrical, magnetic, mechanical and thermal. Relating the requirements to all relevant energy forms provides a comprehensive listing. The energy forms in this discussion are limited to electrical, magnetic, mechanical and thermal.

35.3.2 Steps To Partitioning

A first step to partitioning is the creation of a comprehensive categorized list of electrical, mechanical and thermal, technical user requirements. This is performed as mentioned above.

The second step is creation of a simple component characterization map that identifies dominant attributes of the components. The block diagram of a 2.2 kW motor drive is shown in Figure 35.1 and part of the characterization map is given in Table 35.1 The map is divided into metrics by energy

TABLE 35.1 Component characterization map

Functional Block	Function	Comp	Qty	Mechanical		Electrical			Thermal	
				Delivery Form	Size	Voltage	Current	Constraint	Loss	Max temp
						V			W/comp	°C
EMC	Filter	Y-cap	2	Leaded	13×5×10	300 ac		Low L to earth		
	Filter	X-cap	2	Leaded	26×10×18	300 ac		Low L to L1-L2		
	Choke	Inductor	1	Leaded	37×20	300 ac	11 rms		6	105
	Filter	X-cap	1	Leaded	17×6×12	300 ac		Low L to earth		
	Transient clamp	VDR	3	Leaded	φ21×5	300 ac		1 low L to L1-L2 2 low L to L-Earth		
	Filter	Y-cap	2	Leaded	18×9×15	300 ac		Low L to earth		
	Filter	Y-cap	2	Leaded	12×8×10 4×10	300 ac		Low L to earth		
Rectifier	Pulse	MKT	1	Leaded	31×18×28	300 ac		Close to DCP-DCN		
	Bridge	Diode	4	Die	3.5×2.5	600	11 rms		5	125
	Clamp	Diode	4	Die	3.5×2.5	600			< 1	125
	Switch	IGBT	1	Die	6×4.3	1,200	11 rms		15	125
	Cur. sense	Shunt	1	TF		11 rms			2	
	Controller	IC	1	Die		< 18			< 1	125
	Support	C R	4	SMD TF	0603— > B					
Inrush/VDE	Transient clamp	VDR	3	Leaded	21×5	300 ac		Low L DCN-PGND		
	Switch	MOS	1	Die	7.5×7.5	500	26 peak		16	125
	Freewheel	Diode	1	Die	3×4	500			7	125
	Cur. sense	Shunt	1	TF			11 rms		2	
	Controller	IC	1	Die			10 m		< 1	125
	Support	C R	8	SMD TF	0603— > B	< 70 V				
	Choke	L	1	Leaded		500	11 rms		15	130
DC-link.	DC-cap	E-lytics	2	Leaded	26×50	500	1.25 rms		3.5	75
	Voltage sense	R	2	TF						inner

form to categorize and record extreme operating values for each component. Not all blocks need to be completed or components included, only those that most impact the technology selection. For example, any 5 V, < 0.1 W resistor in the control circuit need not be listed since it is accommodated by nearly all technologies (e.g. as 0806, SMT, PTH, thick film, etc.). For each of the remaining components, all the mechanical package formats should be listed under the delivery form.

The third step is to strategically group components by delivery form taking into consideration limits on electrical and thermal operating points. This first-cut grouping brings a high level of packaging integration to the system and is a critical step. Similar components from all parts of the circuit become associated.

The fourth step uses the user requirements as constraints along with engineering experience to reassociate components into different groupings. Not all components are easily regrouped. The unassociated components become dominant factors during technology selection. As an example, the high-voltage components of a bootstrap gate-drive supply can be associated with the gate-drive circuit board or the high-voltage power inverter components. Interestingly, most unassociated components reside at the interfaces between functional blocks (as shown in Figure 35.1).

The fifth step is to map the groupings of components to the packaging technologies. This was partially performed in the previous step as engineering judgment guided the regrouping. Refinement of the selection comes when the unassociated components are incorporated. Steps four and five become iterative to provide optimum partition(s).

35.4 Assessing Partitioning Technologies

To better understand the correlation between electrical and physical circuits (partitioning and *packaging*), consider the morphology of a generic circuit. A circuit has three partitions: components, topologies and controls. Components are active or passive, such as ICs or heat sinks. Topologies are the positioning of the components to provide a function, such as a Buck converter or the thermal structure of silicon soldered on copper clad to ceramic. Controls provide a preferred set of rules for operation of those components, such as voltage regulation or a thermostatically controlled fan. Hence, a “circuit” design involves electrical and physical design. The physical design is packaging and can be defined as

“...the art (design) of arranging components to provide a function or characteristic

Note that *packaging* is a design function, whereas manufacturing embodies the processes to fabricate the designed arrangement. Although packaging and manufacturing are strongly interrelated, they are not synonymous.

The term “physical” should be further defined. “Electrical” identifies the form of energy being processed. Hence, “physical” represents other forms, such as mechanical, thermal, chemical, photonic, etc. The power electronics designer is mostly interested in electric, magnetic, mechanical and thermal. Discussion will be limited to these four energy forms.

An integrated design problem example relating the four energy forms of interest is as follows. A high-frequency magnetic core couples the radiated field into a copper conductor on a PWB and causes eddy current heating, increasing the skin-effect resistance. Higher resistance loss further increases conductor heating which increases the mechanical stresses between the conductor and PWB leading to early failure. Who would notice the problem first? The electrical designer through circuit loss measurements; the thermal designer through a thermograph of that specific spot, or the packaging engineer who first notices the conductors are lifting off the board and assumes the conductor adhesion is poor because of faulty chemistry?

35.4.1 Levels of Packaging

The levels of packaging divides a system, top-down, into lower and lower subassemblies with the boundary drawn between assembly and subassemblies as shown in Fig. 35.2.

1. the boundary conditions of electrical/mechanical/thermal performance characteristics within the level,
2. The electrical/mechanical/thermal interconnection between each level.

Each level is defined and numbered, bottom-up, in a micro-to-macro manner. Three traditional levels in electronic packaging [3] are also applicable to power packaging. Note that levels are not easily defined. Some packages may be categorized in either of two levels depending on the application.

Level-0: Component(s). This is the base level for a component that a designer can obtain and may be a passive, discrete semiconductor or integrated circuit, including a “smart power” circuit. The semiconductors and ICs are typically silicon (Si), though there is signifi-

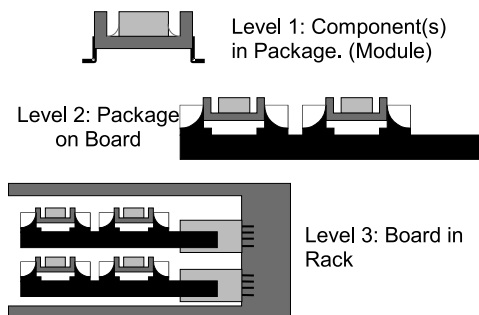


FIGURE 35.2 Levels of packaging.

cant development in SiC and GaAs for higher operating temperature and speed.

Level-1: Component(s) in Package. This is basic component packaging. Examples include mount-down and lead-attach of a component or semiconductor in a discrete package, or multiple components in a module. Traditional ‘chip and wire’ hybrid circuits mounted in a housing (often hermetic) are Level-1 packages. The package provides a ‘self contained environment’ that allows the components to be tested, transported and used at the next higher level of packaging while buffering electrical, mechanical and chemical discontinuities from the next level. This package becomes a subassembly to the next higher level.

Level-2: Package on Board. These boards carry mixed-technology components (capacitors, resistors, inductors and packaged discretes) that are usually coated and terminated with a connector. Examples are PCB, IMS (insulated metal substrate) and SMT boards. They differ from Level-1 in the lesser sophistication in fabrication. The board provides a functional partition and is a subassembly to the next packaging level.

Level-1.5 (half-level): Chip on Board (COB). This mounts ‘chip and wire’ semiconductors directly to a PCB or on IMS. A driver in packaging is to combine levels. An objective of the road map will be the development of a direction to combine levels.

Level-3: Board in Rack or Sub-Assembly Level. At this level the rack or case is considered. Each board or module is a subassembly connected to a rack backplane, motherboard or free-wired together. An example is the output modules in a multioutput power supply. The sub-module approach provides flexibility and fast assembly time.

Definition of levels can continue into Level-4: Rack in Cabinet and Level-5: Cabinet in Room or Multiple Cabinet Level. The technical issues and methods to partition the product applies to all these levels. Producers and suppliers have business thrusts that are aligned along one or more packaging levels. Note, that combining levels, as done with Levels 1 and 2, is of great advantage.

35.4.2 Technologies

The delivery form, i.e. mechanical support structure for integrating functions, divides the technologies. The simplest delivery form is a monomaterial approach, such as a silicon integrated circuit. Here, several functions are incorporated into the silicon. A thick-film hybrid uses ceramic-glass structures to create functions. A glass-epoxy board (FR-4) allows attachment of discrete components to “integrate functions.” Remember that the functions are not restricted to electrical, but may include magnetic, mechanical and thermal.

The delivery form is an important aspect since the size of mounted components greatly limits the choices in technologies. The greater the mass of the components, the more mechanically robust the technology needs to be. The technologies reviewed below belong to packaging Level-0 through Level-2 and, generally, sequentially range from fully imbedded components as in silicon ICs to modestly robust for surface mounted components, to very robust for clamped, screwed and axially leaded. The transition from plated through holes (PTH) to surface mount technology (SMT) occurs within FR-4 and partly explains the greater acceptance of this versatile technology.

Semiconductor Power Integrated Circuits. This is considerably different than the remaining packaging technologies in that it approaches a “monomaterial system.” Multiple functions can be produced in one material, usually silicon. This is expanded in the following section.

Thick-Film on Ceramic (TFC). Glass based pastes or inks are loaded with electrically conductive materials, such as copper, gold or silver, to form interconnects, loaded with resistive materials to form components, or used unloaded as dielectrics. The pastes are screen printed on ceramic and fired at $\sim 900^{\circ}\text{C}$. Vias are formed as holes in dielectric layers and discrete components are surface mounted with solder or adhesives. Only two types of air-fired thick film are considered here: multilayer thick film (TF-multilayer) for control circuitry and thick thick film (TTF) where silver is printed to form up to $160\mu\text{m}$ conductors for power.

Cu Plated on Ceramic (CuPC). Patterns are imaged or transferred to the surface of ceramic. Copper is then plated to a thickness $< 125\mu\text{m}$ (5 mils). Discrete components are attached or full thick-film processing is placed on the plated copper with screen-printed components imbedded or discrete components attached.

Glass-epoxy with surface mount pads (FR-4, SMT). A fiberglass mesh is impregnated with epoxy and metalized with copper. Interconnect patterns are etched into the foil. The patterned copper clad mesh can be laminated and vias formed by drilled and plated holes. Chip components are “surface mounted” with solder attachment or conductive polymer. Components can also be imbedded using loaded polymers similar to the TFC process, but with low temperature curing (SMT is “surface mount technology”).

Insulated Metal Substrate-polymer on Metal (IMS-PM). A polymer is used to isolate and attach a conductive interconnect to a metal plate which provides mechanical support. Vias can be placed between the interconnect and plate, and a layer of polymer and interconnect can be attached to the interconnect layer.

Insulated Metal Substrate-steel corded (IMS-PS). A high temperature glass ($\sim 900^{\circ}\text{C}$) coats a steel plate and a thick

film conductive cermet interconnect is applied upon the glass. The structure is similar to traditional thick film. Vias are processed as in multilayer thick-film.

Direct Bonded Copper (DBC). Copper foil is applied to ceramic, bonded at $\sim 1063^\circ\text{C}$, and a pattern is etched. Discrete components are surface mounted with solder or adhesive. There are no vias.

Glass-Epoxy with plated through holes (FR-4, PTH). Same as FR-4 above except leaded components are solder attached with leads placed through holes (PTH is “plated through holes”).

Molded Interconnect Device (MID). A high temperature plastic or polymer structure hosting electrical interconnects is fabricated by 1-shot, 2-shot or insert molding. The interconnections are formed by hot-stamping copper foil, imaging and metal plating the polymer, or insert-molding of structured metal. MID lends itself to high volume, 3D, net shape packaging and is extensively overlooked in the power electronics area (excluding automotive). Components can be surface mounted or through-hole with moderate to coarse line resolution. Only hot embossing is considered here.

Laminated Bus-Bar. A polymer, such as epoxy, glues together thick conductor bars while providing electrical isolation. The bars can be free-floating laminated interconnects or, if sufficiently thick, be the metal carrier. Vias between layers are metal posts or fasteners placed through drilled or stamped holes. These are used in high current systems and can accommodate very large components. These were not considered in this development.

35.4.3 Semiconductor Power Integrated Circuits

As noted in the introduction, the term “smart power” has been used for several decades to describe the imbedding of control into power processing systems. One approach integrates control and power into a monolithic circuit, such as silicon, and takes on two forms. One is the integration of analog and digital circuitry with discrete power devices. The second applies to high voltage ICs used for power monitoring and fault control. The term “smart power” has become synonymous with power integrated circuits (Power ICs) or application specific power ICs (Power ASICs). Motorola trademarked the term “SMARTpower” circa 1980.

A designer typically is a user of power ICs and seldom influences the chip design. Systems partitioning, as described throughout this chapter, is not directly applicable. However, once the chip is available, the designer is armed with a more functionally integrated component. A background to power ICs is given below to aid the designer in better understanding the technology. An excellent reference noting the beginning of high voltage ICs is an IEEE Press Book by B. J. Baliga [4].

TABLE 35.2 Examples of power ICs (smart power)

	Low Current	High Current
Low voltage	Power control Ics PWM controllers	Bipolar drivers Automotive actuators
High voltage	Bridge Gate drivers Gas-Display drivers	(limited application)

Power ICs can be divided into four groups resulting from a matrix of low and high voltage, and low and high current capabilities as identified in Table 35.2. The low-voltage, low-current ICs are readily available for the control and monitoring of power processing functions. These smart chips control power supplies, battery chargers, motor drives, etc., and are often referred to as “power controllers.” These chips are produced from standard IC processes and limited to the voltages of the process. Cost follows typical IC cost structures.

Low-voltage, low-current ICs can be further subdivided into ‘dedicated’ and ‘programmable’ chips. In the late 1990s and early 2000s, the incorporation of imbedded control expanded the definition of ‘power controllers’. Sophisticated control algorithms that were implemented in digital signal processors (DSPs) were incorporated into programmable power controllers. The role of the power electronics designer further changed to become adept at high performance programming.

Low-voltage, *high-current* power ICs again use standard IC processes for fabrication. The higher current requirement is met by creating effectively large device areas that maintain current densities consistent with process characteristics. In the 1970s and 1980s bipolar processing was dominant and large area devices were fabricated. Typically, processes were limited to 40 V and pushed to 60 V for actuator and transistor driver applications. As a side note, the most successful power MOSFET (metal-oxide semiconductor FET) driver in the 1980s used a commercially available digital “line driver” IC. Driver chips were later developed with FET processes that paralleled many low-power FET cells. Again, the required area was determined by the maximum current density of the allowed process.

Dedicated chips of the 1990s used power MOSFET technology to create driver and actuator chips. Applications of the low-voltage, high-current ICs fall mostly in the areas of power conditioning for photovoltaic systems, actuators for computer hard drives, actuators and motor drives for automotive and appliance applications, and driver applications in power semiconductors circuits.

Since most all IC technology was created for computer and telecommunications applications, creation of ‘higher voltage’ ICs for power was slow to develop. Lack of market size in power did not support substantial technology development, but rather incremental product development. However, high-voltage ICs were developed early on for the gas-tube display market (circa. 1980s). Other significant developments slowly

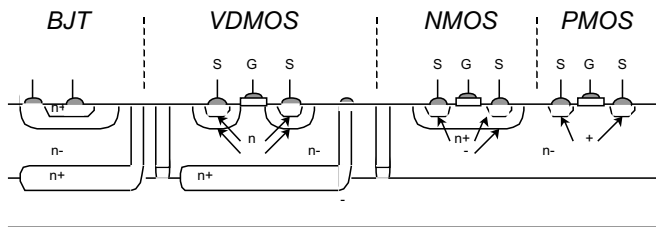


FIGURE 35.3 Junction isolation used to separate devices or circuits.

occurred, mostly in drivers for power-bridge circuits as used in motor drives and “application specific ICs.”

High-voltage ICs are processed with either dielectric isolation or junction isolation. In the 1980s dielectric isolation was used extensively by Dionics Incorporated for display drivers, which had ratings of several hundred volts. Dielectric isolation utilizes silicon dioxide wells. Devices, such as bipolar transistors, are fabricated in the wells, which serve as functional islands. The devices are then interconnected at the surface.

Limitation of the dielectric isolation process is the higher cost. However, dielectric isolation does provide for more reliable isolation with greater circuit flexibility. Both power rating and current capacity are low relative to junction isolation because of the planar nature of the structure and interconnects.

Junction isolation became the preferred method starting in mid 1990s with developments from General Electric and Harris companies followed by power ASICs from power semiconductor manufacturers. The isolation method used multiple levels of p-n junctions to form wells. A cross section of several basic technologies is shown in Fig. 35.3. Note the p-type sinkers connecting to the p-material of the substrate to provide cell isolation. There is also a combination of structures used to produce a BiCMOS process. The CMOS provides the control circuitry while the bipolar structures provide high current-density transistors for power processing.

Junction isolation has several limitations, most significant of which is possible “layer inversion.” Inversion occurs when the reference substrate, or portions thereof, become reverse biased. Relatively large currents can flow and biasing of four layer structures can cause latch-up. Manufacturers have paid significant attention to minimizing this problem. However, designers must always be cautious that a fault condition or capacitive current from a high-frequency transient does not induce an inversion.

35.5 Full-Cost Model 5

This is the one issue seldom discussed in the open literature, yet is the greatest driver to selection of circuit design approaches and determination of partitions. Unfortunately, a designer often limits cost estimation to only component cost, i.e. the bill of materials (BOM). The greatest cost is often not

the component, but the handling, mounting, and testing of a component. An excellent example is the selection of output filter capacitors in dc-dc supplies. The use of a multitude of smaller ceramic chip capacitors, which can be automatically surfaced mounted, is often less expensive than larger electrolytic through-hole-mounted capacitors, and provide much greater reliability over time. (This only applies to larger volume production.)

The use of cost is also dependent on the positioning product design within the company. A vertically structured design company with captive manufacturing has the advantage of increasing volume by modularizing their circuits to be used across several product lines. Regardless, the following procedure applies for both captive and out-sourced manufacturing.

When discussing cost it is necessary to define centers of cost for both product and business. The terms are defined as follows.

1. *Materials cost* represent direct costs of packaging, and include the minimum packaged component (e.g. silicon chip), component packaging materials (e.g. plastic housing on a TO-220) and packaging materials for manufacture (e.g. solder or adhesives for mount down). If the manufacturer can mount bare die, then these quantities are determined separately. If manufacturing is out-sourced, then the “pre-packaged” component cost accounts for the first two costs and the manufacturer (or assembler) determines the third cost. The variation in cost by volume must also be included. Volume dependency is greatest for custom products at low volume and lowest for standard high volume products. A typical volume cost factor is 20 decrease in cost per 10-fold increase in volume.
2. *Production cost* includes factors for wages and product volume, but is independent of material costs, (which is not often assumed when assessing overhead). Production cost can be characterized as a function of technology and quantity. To reflect this into a design tool, it is necessary to describe production cost as a function of simple information, such as the number of SMD and leaded components, and square inches of substrate board. Assessment is as follows for captive production:
 1. Determine the total wages, equipment and facility depreciation, and other facility overhead.
 2. Determine the number of production technologies in the facility, both in place and available with minimal extension.
 3. Determine technology costs by a ratio of the above two parameters.
 4. Add scaling factors for volume dependency.

In Fig. 35.4 relative production costs for various technologies (circa. 1999) are shown for fixed volume. Note that chip & wire is less expensive than

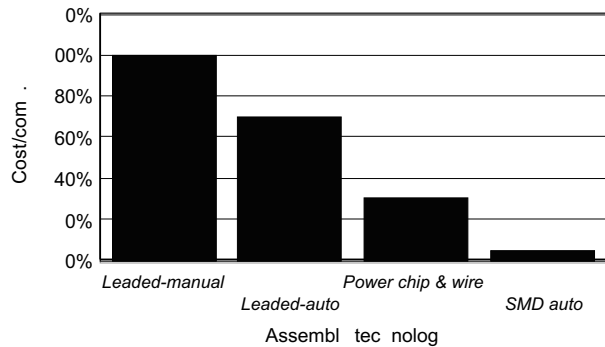


FIGURE 35.4 Relative production costs. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference*, New Orleans, LA, February 6–10 2000, ©2000, IEEE, New York.

handling a leaded component and is typical for captive facilities. Included scaling factors in your calculations to give a volume dependency for a highly automated production technology. Depreciation is for production equipment and buildings, whereas other overhead covers the significant cost involved in purchasing, management, production technology, etc.

3. *Partitioning cost* is incurred for each technology used. From the previous technology descriptions it appears straightforward to choose “this technology for these components” based on *technical* performance attributes. However, there is a drawback to this partitioning. Each partition adds one circuit to be handled through production with an additional interconnect and assembly process. This means additional incremental costs. Assembling subcircuits into a product is similar to assembling components on boards and is modeled as cost in wages modified by a different overhead factor. For chip & wire, costs for protecting (encapsulating) chips are included if necessary.

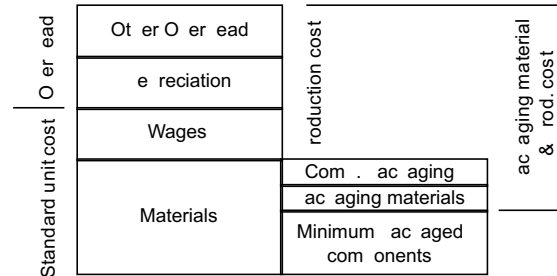


FIGURE 35.5 Full cost model for circuit partitioning. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference*, New Orleans, LA, February 6–10 2000, ©2000, IEEE, New York.

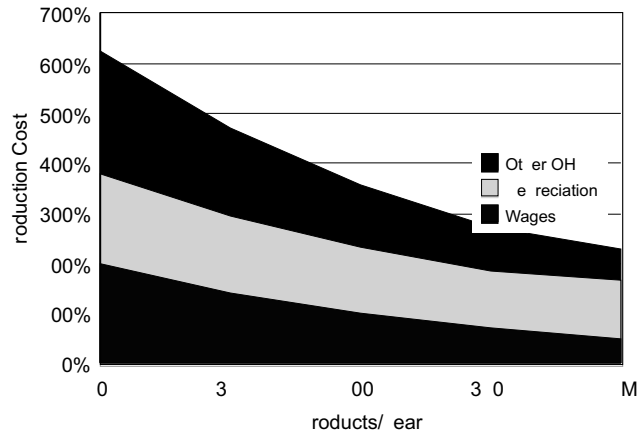


FIGURE 35.6 Cost variation due to volume. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference*, New Orleans, LA, February 6–10 2000, ©2000, IEEE, New York.

4. *Full cost* combines material costs and production costs as shown in Fig. 35.5. A minimum-packaged-component system is chosen to highlight the possibility of buying nonpackaged components, but the model is valid for any level of packaging. If there is not a captive circuit fabricator, then the cost is obtained through competitive quotes or experience with the manufacturer. A mixture of in-house and out-sourced costs can be included in the model.
5. *Product business cost*, i.e. returns on investment for development of one product, is an investment in future payback. The total cash flow from development until end of production determines the business costs for a product.
6. *Company business cost*, i.e. return on investment for cross products reflects the cost of suboptimization within one single product. The value of reusing the same packaging technologies, designs (diagrams) and even physical circuits (building blocks) across different products should be measured at the company level. The value of building blocks becomes obvious through savings in repetitive development costs and maintenance of function. Development and maintenance costs are saved since the function is only developed once and unilaterally maintained across all products.

The impact of volume on building block cost applied to three motor drive products is shown in Fig. 35.6. At low volumes the main savings are in development and maintenance costs, while at high volumes only savings in full cost matters. The overall conclusion is that, if a partition is necessary to meet requirements, then the partition must be guided by strategic choices in order to optimize cost on a company business level and relative cost diagrams should be used only for optimizing within partitions.

35.6 Partitioning Approach

There are several natural aids to partitioning. Rank ordering common packaging technologies by technical performance (for power processing) also orders most other attributes. As one moves down the list of technologies as described in Section 35.4.2, one finds, in general, increasing electrical performance in current-carrying capacity, decreasing performance in voltage isolation and operating frequency, lower thermal performance and density, less sophisticated processing, and lower cost for lower volumes (except for MID). These monotonic trends allow rich engineering judgment to effectively group components (step 4 in Section 35.3.1) for optimized partitioning. Important physical characteristics for relevant materials are given in Table 35.3 and Table 35.4.

Following a sequence of first matching the most challenging component grouping with the higher performance technology can minimize iterations of the last two steps in Section 35.3.1. The next challenging grouping is matched with the next technology of lower, but suitable performance and lowest

TABLE 35.3 Conductor/metal properties

Metal	Resistivity ($\mu\Omega\text{-cm}$)	Conductivity k (W/m-K)	TCE (ppm/ $^{\circ}\text{C}$)
Aluminum	4.3	240	23
Chromium	20	66	6.3
Copper	1.7	393	17
Gold	2.2	297	14.2
Invar	46	11	1.5
Kovar	50	17	5.3
Molybdenum	5.2	146	5
Nickel	6.8	92	13.3
Silicon		84	
Silver (30Ag)	5.6	130	5.6
Silver	1.6	418	19.7
Tin	11.5	63	
Tungsten	5.5	200	4.5
80 Au–20 Sn	16	57	15.9
95 Pb–5 Sn	19	63	29

TABLE 35.4 Insulator/substrate properties

Substrate	Rel. Perm ϵ_r	Conductivity k (W/m-K)	TCE (ppm/ $^{\circ}\text{C}$)
AlN	8.8	230	3.3
BeO	6.8	240	6.8
BN	6.5	600	3.7
Cu-Invar-Cu		100	3
Diamond (CVD)	3.5	400	2.3
Epoxy-Glass (x,y)	3.6	0.2	6
Polymide	3.5	0.2	50
SiC	42	270	3.7
Si ₃ N ₄	7	30	2.3
96 Al ₂ O ₃	9.4	26	6.6

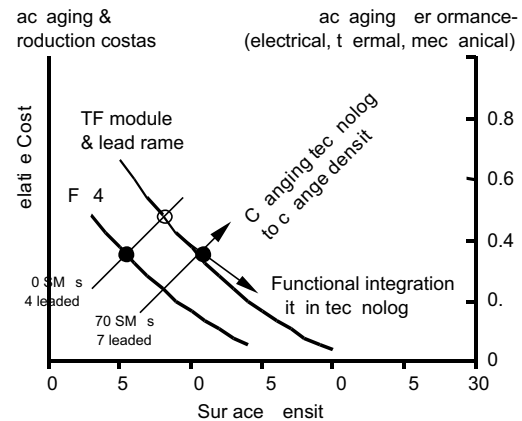


FIGURE 35.7 Cost variation within technologies. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

cost. Starting with the highest performance technology also allows much lower component groupings to be considered for inclusion at possibly no increased cost. For example, if ceramic thick film is used for chip and wire power die and current sense resistors, the inclusion of thick-film control circuits comes with little added real estate (cost).

The selection of technologies has been very misunderstood because a typical perspective is to look at “substrate area cost.” The famous “dollars per square inch” costing of technologies has been used. This is as limiting as using only a BOM for cost driven decisions. A better understanding is required and is aided by the graphical perspective in Fig. 35.7. It is recommended the curves be viewed right to left (as density decreases). The falling curves represent relative full-cost (Section 35.5) of each technology as area changes. The starting and ending points are the practical limits in the use of the technology at certain densities.

As an example, assume a given circuit is designed with only one technology, such as thick film (TF), and as dense as possible. As board area increases (becoming less dense), components can grow in size (0603 to 0805) with larger interconnect traces. The cost increases, following the curves up and to the left. A point is reached in area that a less costly technology may be suitable, such as SMT FR-4. This other technology would decrease cost for the same area. Hence, cost and density decrease, but performance also decreases. Within a range near maximum density, the higher performance TF technology with added area is still less costly. This is due to *packaging and production costs*, and is often overlooked by designers who look at ‘cost per square area of boards’ without looking at the full-cost model.

A more generalized set of curves is shown in Figure 35.8. This graph, in essence, is created for a specific production facility. The circuit designer, or design team, would follow the steps to partitioning, letting the costs of the technologies drive

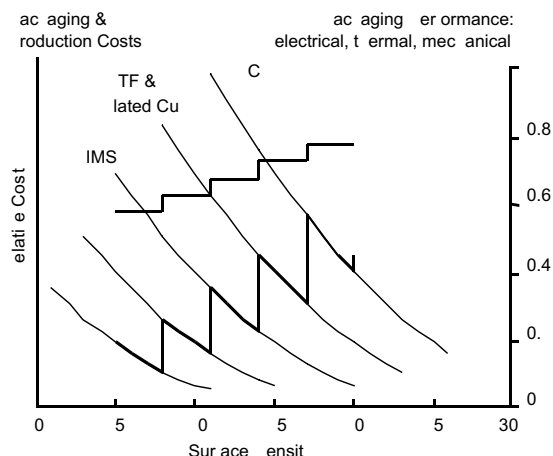


FIGURE 35.8 Generalized relationship of cost and technology. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

where partitions are best drawn. Remember that the overall circuit is composed of electric, magnetic, mechanical and thermal circuits.

35.7 Example 2.2k Motor Drive Design

A 2.2 kW motor drive, consisting of electronics, motor and pump encased in one housing, is used as an example product. The block diagram of the electronics is shown in Fig. 35.1. For an (planar) electrical-mesh circuit, the physical assembly pattern would closely follow the electrical schematic layout and one packaging technology, such as FR-4, could be used, though not efficiently. The design would then follow a single line up and to the left in Fig. 35.7. Using mixed packaging technologies provides multiple assembly levels and the assembly pattern more closely follows groupings of the physical delivery forms of the components. The steps outlined in Section 35.3.2 are followed to determine the proper partitioning of the system to meet performance requirements and provide maximum business profit. The steps are summarized as:

1. user requirements,
2. component characterization,
3. component grouping,
4. strategic partitioning with constraints,
5. optimizing within partitions.

35.7.1 User Requirements constraints

Many user requirements direct the system design as outlined in Section 35.3.1. However, several requirements place specific

constraints on the packaging of the 2.2 kW drive as noted below:

Mechanical: built-in stainless steel tube with diameter of 65 mm, and short as possible.

Thermal: cooling through tube with non-flow of water at 30°C.

Environment: potting complete electronics inside tube not allowed

Regulatory: UL, CE

Reliability: 1,000,000 quick start/stop
30,000 maximum gradient start/stop
40,000 h lifetime 10°C water

35.7.2 Component Characterization Map

A component characterization map is performed on all the components to identify dominant technical and physical attributes, and is illustrated for part of the circuit as in Table 35.1. In this component characterization map components are listed for each electrical functional block.

35.7.3 Component Grouping

An overview of possible groupings into packaging partitions is obtained by attaching main components and key attributes to the functional block diagram of Fig. 35.1.

35.7.4 Strategic Partitioning with Constraints

A major constraint is the limited space available (65 mm diameter). This makes it obvious that some miniaturization is very valuable, but what should be miniaturized? Packaging cannot miniaturize leaded components. These components require either through-hole PCB (FR-4, for soldering) or some form of lead frame (MID for welding). Power die are top candidates for miniaturization because the die can be grouped into a power module that is much smaller than discrete power components. Also, high power losses do not allow the same packaging technologies to be used as for leaded components.

The remaining nonpower die and associated components are prime candidates for modularization. Highest value is reached if a building block can be reused across different products. Therefore, as much control circuitry as possible should be integrated without violating the possibility for reuse in other products. For this product, the line communications bus and motor control circuitry would be excluded, but the control for VDE/inrush and PFC would be integrated together with the driver and all sense resistors. This integrates 82% of all power losses for easier cooling, integrates all power-component-dependent control circuitry, and enables product-independent maintenance and power die optimization.

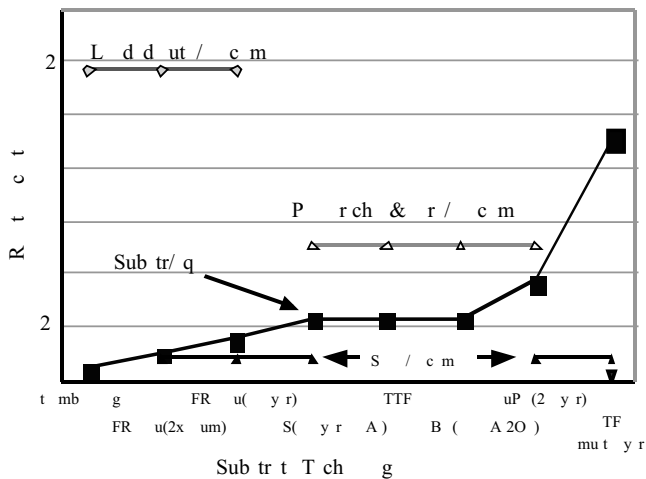


FIGURE 35.9 Substrate costs (1999). Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

At this stage there are usually new requirements added for cross-product reuse. This application requires 125°C baseplate temperature.

35.7.5 Optimization within Partitions

Optimization requires choosing optimum technologies to meet cost and performance requirements. In Figure 35.9 relative cost of various substrates is shown together with the cost of suitable production technologies. Note that the substrate cost is for equal substrate area but different performance. For example IMS requires more space for control circuitry than TF multilayer because IMS has only one conductor layer.

Figure 35.9 should be used together with Fig. 35.1, which shows that the module includes both power chip & wire (PC&W) and low power control circuitry (SMT). DBC, IMS, TTF and CuPC can accommodate the PC&W. FR4, IMS, TF multilayer and CuPC can accommodate fine line SMT. This should initially lead to the conclusion that DBC, IMS or TTF should be used for power, excluding CuPC due to cost; and FR4 for control, excluding the others due to cost.

Are all cost issues taken into account and all requirements met? Not necessarily. Packaging approaches influences component cost. Power sense resistors, which are typically in SMT form, can be integrated in TF multilayer at near-zero incremental cost. Also, less expensive integrated circuits can be chosen when the packaging approach allows active trimming of associated components. Besides cost, technical issues limit packaging choices for certain circuit partitions. Reliability and temperature requirement (125°C) rule out FR4.

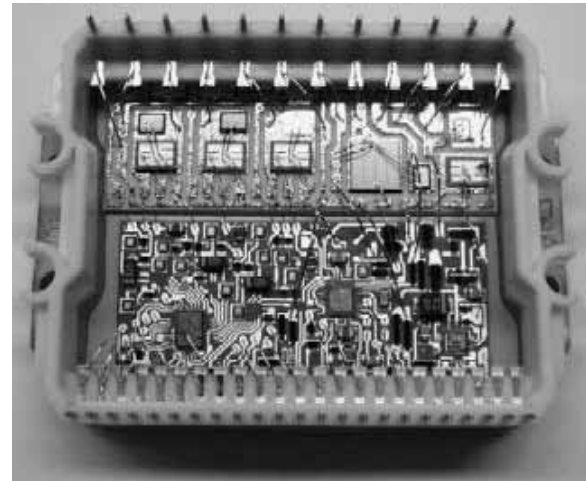


FIGURE 35.10 Final module combining several packaging approaches. Reprinted with permission, JB Jacobsen and DC Hopkins, Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10 2000*, ©2000, IEEE, New York.

There are fewer and fewer choices. If power die were available as known good die, then power and control could be combined on one substrate with IMS or CuPC. The IMS has drawbacks, such as lower power cycling capability due to a high TCE and is only a one-layer technology, which means more area and less noise immunity. CuPC has neither of these problems, but due to lack of known good power die was not chosen. Also, CuPC does not allow component integration at the cost indicated in Fig. 35.9. A two-substrate solution was needed.

Power DBC was chosen as the obvious highest performing technology among comparable low cost power substrates. The DBC is soldered onto a low cost copper base for thermal management and extends to form a mounting base for the control substrate.

Multilayer thick film was chosen for control circuitry despite the apparently high substrate cost. In the motor module, this substrate is the optimum cost choice because of high component integration, such as the three buried power current-sense resistors and many printed resistors for accurate active trimming of functions associated with the integrated circuits. Partitioning cost is minimized by combining interconnections of substrates with interconnection to I/O terminals in one technology heavy wire bonding. This has been possible by designing an MID interconnection component with terminals that are wire bondable on one end and solderable on the other. The resulting module is shown in Fig. 35.10.

Other components, both SMT and leaded, were not best accommodated in the module. Therefore, a two-layer FR4 is chosen as the lowest cost technology suitable for both delivery

forms and used for the module and components. Mechanical stability and cooling is achieved by using a patented structure of extruded aluminum profiles.

Using bare die, higher cost substrates and partitioning with different technologies allows the product to surpass cost targets. The partitioning in packaging Levels-1 and -2 address optimization of *product business cost* as defined in Section 35.5. Designing the module building block as a component for reuse across other products increases volume and reduces cost. More importantly, relative low volume products can benefit from the building block by faster development cycles, lower development cost, lower Level-3 packaging cost and lower maintenance cost. The building block value addresses optimization of *company business cost*.

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References

1. M. Meinhardt *et al.*, (1999) STATPEP-current status of power electronics packaging for power supplies – methodology, *Proc. 14th Annual Applied Power Electronics Conference and Exposition*, March 14–18, 1999, IEEE, New York, pp. 16–22.
2. D. C. Hopkins *et al.* (1998) A framework for developing power electronics packaging, *Proc. 14th Annual Power Electronics Conference and Exposition*, February 15–19, 1998, IEEE, New York, pp. 9–15.
3. R. R. Tummala and E. J. Rymaszewski (1989) *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York.
4. B. J. Baliga (ed.), (1988) *High Voltage Integrated Circuits*, IEEE Press, New York.
5. J. B. Jacobsen and D. C. Hopkins (2000) Optimally selecting packaging technologies and circuit partitions based on cost and performance, *Applied Power Electronics Conference, New Orleans, LA, February 6–10, 2000*, IEEE, New York.