Evaluation and Applications of 600V/650V Enhancement-Mode GaN Devices

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***Abstract*— This paper presents elaborate evaluation of 600V/650V enhancement mode gallium nitride (GaN) devices. The switching loss mechanism and the impact of package and driving circuit parameters are illustrated in detail. The hard-switching turn-on loss is dominant due to junction capacitor charge of the freewheeling switch. The turn-off loss is much smaller and it can be further improved by driving circuit parameters and packaging. The driving circuit taking consider of high dv/dt and di/dt immunity is discussed. A few design examples are shown to demonstrate the advantage of GaN and the impact of GaN on system design.**

Keywords—Enhancement-mode, depletion-mode, Gallium Nitride, cascode, switching loss, gate drive.

INTRODUCTION

Gallium Nitride devices are gathering momentum, with a number of recent market introductions for a wide range of applications such as point-of-load converters (POL), off-line switching power supplies, battery chargers and motor drives. GaN devices have a much lower gate charge and lower output capacitance than silicon MOSFETs and, therefore, are capable of operating at a switching frequency 10 times greater. This can significantly impact the power density, form factor and even the current design and manufacturing practices.

The 600V/650V GaN devices can be categorized into depletion-mode (normally-on), and enhancement-mode (normally-off) device. To easily apply a normally on GaN in circuit design, a low-voltage silicon MOSFET is used in series to drive the GaN, which is well known as cascode structure. Table I listed 3 different GaN devices with similar current ratings. The state of art Si MOSFET is also listed for comparison. The devices parameters clearly show that GaN devices have much smaller Q_g and C_{oss}, which indicates higher frequency operation capability. The characteristic of cascode GaN devices have been studied systematically in [1-3]. The analysis and experimental results shown in [1-2] indicates that turn-on switching loss is significant due to the charge of the free-wheeling switch while the turn-off switching loss is small and load current independent due to current source driving mechanism. The impact of packaging has been investigated in [4-6]. The use of two discrete devices means more interconnect parasitic inductance which may impact the switching speed and cause internal oscillation at large load current condition. A better packaging is required for cascode GaN to minimize interconnect parasitic inductance in order to eliminate GaN gate oscillation and reduce the switching loss. Another concern with cascode GaN device is the dynamic voltage distribution during turn-off and turn-on transition, which has been analyzed in [3]. It quite often occurs that the junction capacitor charge of the high-voltage GaN is higher than that of the low-voltage Si MOSFET in the cascode GaN devices. A series of consequences may occur when the charge of the GaN and Si MOSFET are mismatched. The Si MOSFET may reach avalanche at the turn-off transition, which would cause additional loss and reliability concerns. The GaN switch cannot achieve zero-voltage turn-on even when the external waveform of the cascode GaN looks like ZVS. The mismatch charge can be compensated by adding extra capacitor without sacrificing switching loss.

TABLE I DEVICES PARAMETERS COMPARISON

	Cascode GaN	E-mode GaN		Si MOSFET
	Device A	Device B	Device C	
V_{DS_max} (V)	600	600	650	600
I_{DS} (A)	17	10	15	13
R_{on}(Ω)	0.15	0.154	0.11	0.15
Q_g(nC)	9	4	3.3	39
C_{oss_tr} (pF)	105	34	72	220
Max V_{GS}(V)	±18	-10~4.5	±10	±20
V_{TH}(V)	2.1	1.2	1.6	3
Recommended V_{GS} (V)	8	3	7	10

The 600V/650V enhancement-mode (e-mode) GaN devices came to the market recently [7-8]. The devices parameter listed in the datasheet are slightly better than that of cascode GaN devices with similar voltage and current ratings. The static and dynamic behavior of the e-mode GaN device from GaN Systems Inc. has been investigated in [9]. However, the impact of the driving circuit parameters on the switching loss has not been studied in depth. One of the most critical features of e-mode GaN devices is the small margin of gate voltage. The gate breakdown voltage is low and the desired fully turn-on voltage is quite close to the maximum value. The gate drive design consideration of e-mode GaN devices has been studied in [10]. The key of safely driving an e-mode GaN device is to optimize the gate drive loop by minimizing the loop inductance and selecting the proper external gate resistors for turn-on and turn-off loop separately.

This paper shows more detailed switching loss analysis considering the driving circuit parameters and packaging

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influence. The comparisons between e-mode GaN and cascode GaN under similar switching condition are also presented. The gate drive design considerations for e-mode GaN, especially for high side devices are shown in section III. The different switching characteristic of e-mode GaN and cascode GaN indicates different applications which can be more beneficial. A few design examples are shown to demonstrate the advantage of e-mode GaN devices and the impact on system design.

SWITCHING LOSS ANALYSIS OF ENHANCEMENT-MODE GAN SWITCHES

Understand the switching characteristics of GaN switches, is essential to use GaN devices in circuit design correctly and efficiently. In this section, the switching loss analysis under hard-switching and soft-switching condition is presented based on a double-pulse-test circuit which can be easily extended to a half bridge configured topology, such as a buck converter. The impact of the driving circuit parameters and package parasitic inductor on switching loss is also discussed.

Switching loss mechanism

In hard-switching converters, the overlap of voltage and current across the drain and source of the device leads to significant power losses during switching events. To better illustrate the switching characteristics of high-voltage e-mode GaN switches, typical switching waveforms of the active switch in a double-pulse test circuit are shown in Fig.1. During the turn-on transition, a large current overshoot is induced by the junction capacitor charge of the free-wheeling switch. The integral of voltage and current during the turn-on transition generates significant power dissipation, which is in the magnitude of tens of uJ. However, the turn-on switching loss is much lower than the Si MOSFET, which has the same breakdown voltage and same on-resistance.

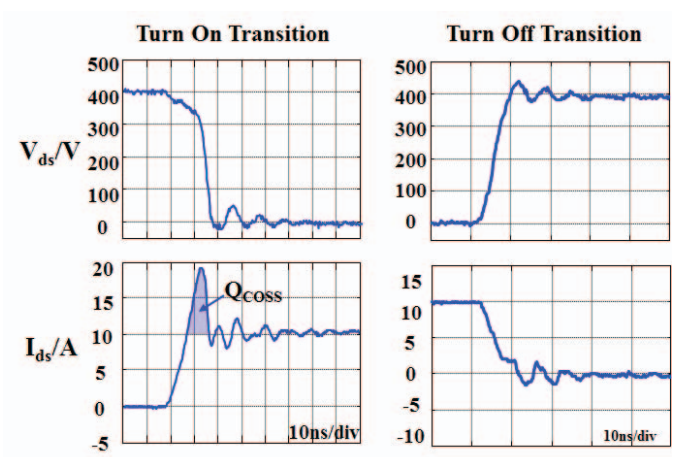

Fig. 1 Typical transition waveforms of an e-mode GaN device

On the other hand, the cross time of the drain-source voltage and current during the turn-off transition is quite short and the transition is more smooth compared with turn-on transition. The channel of GaN can be easily pitched off since the GaN device has relatively high transconductance. The majority of the drain-source current measured from terminals actually is used to charge the junction capacitors voltage to the steady-state value and this part of stored energy is either dissipated during the hard-switching turn-on transition or recycled to the source during the soft-switching turn-on transition. The real energy dissipation during turn-off transition is small and it is typically less than few uJ.

The absolute switching energy of the 600V/650V e-mode GaN devices is less meaningful since it is highly related to the packaging and PCB layout parasitic inductance and the driving circuit parameters which will be illustrated in the following parts.

Packaging impact on switching loss

The switching speed of GaN devices is much faster than comparable Si MOSFET which makes the packaging even more critical to achieve lower loss and less ringing during switching transition. The impact of the packaging parasitics on cascode GaN devices has been investigated in [4-5]. The common source inductance and inter-connected inductance are detrimental to switching loss and gate reliability.

TO220 and DFN packages are typically used for high voltage e-mode GaN devices. Fig. 2 shows the package-related parasitic inductance and the value is listed in Table II which are extracted by FEA simulation in Ansoft Q3D. With Kelvin connection, the DFN package is able to decouple the power loop and driving loop, and therefore it can minimize the common source inductance. Moreover, the inductance of DFN package is much smaller than TO220 package which also helps to reduce the loss and ringing issue.

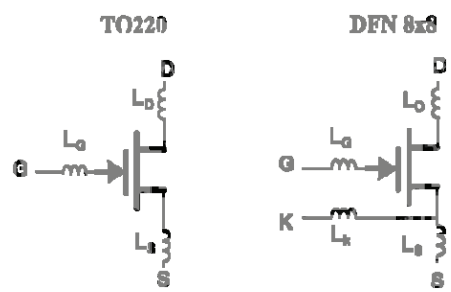

Fig. 2 Packaging related parasitic inductance

TABLE II. PACKAGE-RELATED PARASITIC INDUCTANCE VALUES

	L_G	L_D	L_S	L_K
TO220	3.6nH	2.3nH	3.9nH	N/A
DFN 8x8	2.4nH	1.3nH	0.9nH	1.3nH

The key experimental waveforms with two different packages are shown in Fig. 3. For the turn-on transition, the voltage and current slew rate of DFN package is much larger than that of TO220 package due to smaller common source inductance and loop inductance. As a result, the turn-on energy of DFN package is much smaller than TO220 package as shown in Fig.5. For the turn-off transition, a severe ringing occurred in TO220 package. The false turn-on is observed at high current turn-off condition as shown in Fig. 4, and therefore, the turn-off energy of TO220 package increases dramatically with turn-off current.

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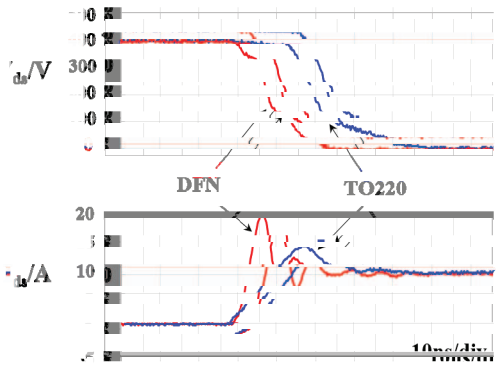

Fig. 3 Turn-on transition of different packages

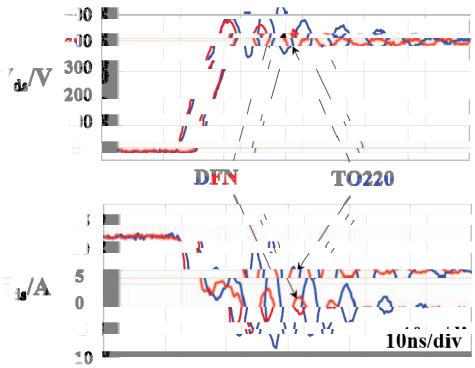

Fig. 4 Turn-off transition of different packages

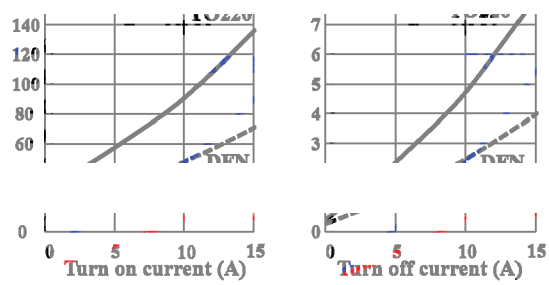

Fig. 5 Switching energy of different packages

Gate resistance impact on switching loss

The gate resistance plays an important role in the e-mode GaN device switching loss, especially in the turn-off loss. The gate resistance limits the gate discharging current and therefore slow down the drain-source voltage and current transition as shown in Fig. 6. The experimental waveforms are based on a DFN packaged e-mode GaN device. As a result, the turn-off energy reduces significantly with 0 Ω gate resistance as shown in Fig. 7. A small gate resistance may cause false turn-on issue in TO220 package and therefore it is necessary to put a relatively large R_G to slow down the transition.

It should be mentioned that the external gate resistor is less effective in a cascode GaN since the GaN actually is controlled by internal Si MOSFET. It is possible to insert a resistor inside the cascode package to control the switching speed of GaN.

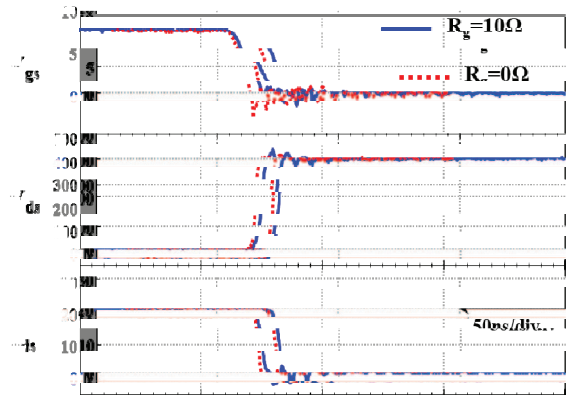

Fig. 6 Turn-off transition with different gate resistance

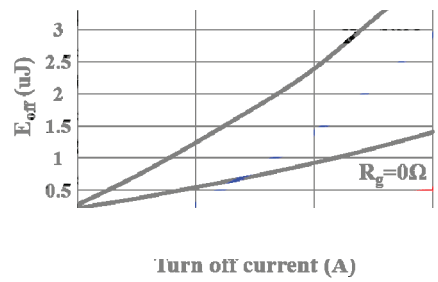

Fig. 7 Turn-off energy with different gate resistance

Comparison with cascode GaN switches

We have built similar test circuits to measure the switching energy of different GaN devices listed in Table I. Device A is a cascode GaN and the other two are e-mode GaN devices. The power loop and driving circuit parameters are optimized in all test conditions in order to get the minimal loss. The turn-on and turn-off switching loss is shown in Fig. 8 and Fig. 9, respectively. It is noticed that the turn-on loss of cascode GaN is higher than that of e-mode GaN, and it is due to the reverse recovery charge of the body diode of the low voltage Si MOSFET inside the cascode GaN device.

On the other hand, the cascode GaN has a smaller turn-off loss at higher-current conditions due to the intrinsic current-source driving mechanism [1-2]. The cascode structure minimizes the miller effect during the turn-off transition; therefore the loss is not sensitive to the turn-off current.

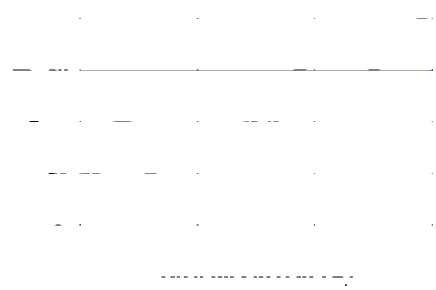

Fig. 8 Turn-on energy comparison

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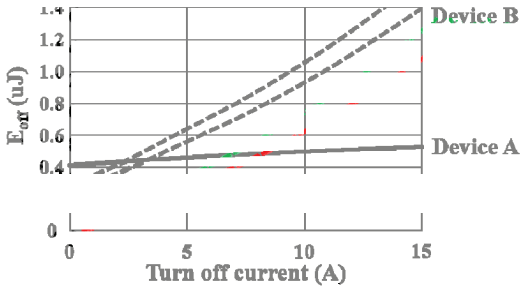

Fig. 9 Turn-off energy comparison

In general, the turn-on switching loss is much higher than turn-off switching loss for both cascode GaN and e-mode GaN devices. Zero-voltage turn-on is desired to fully exploit the advantage of the GaN devices.

Comaprison of hard-switching and soft-switching with enhancement-mode GaN switches

A 500kHz buck converter with 400V to 200V conversion ratio is built to evaluate the e-mode GaN device under hard-switching and soft-switching condition. Fig. 10 shows the efficiency comparison. The efficiency of soft-switching is much higher than that of hard-switching and the difference grows bigger at light load condition. Fig. 11 shows the loss breakdown with 100W output. The chart clearly shows that the turn-on loss is the dominant part under hard-switching and it is completely removed with ZVS. The conduction loss slightly increases with soft-switching due to the circulating energy used to achieve ZVS.

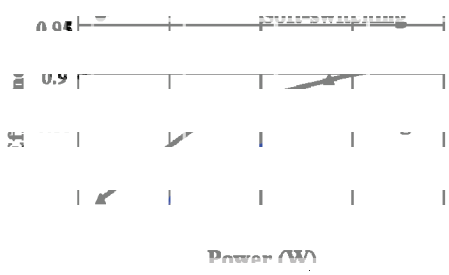

Fig. 10 Efficiency comparison of hard-switching and soft-switching

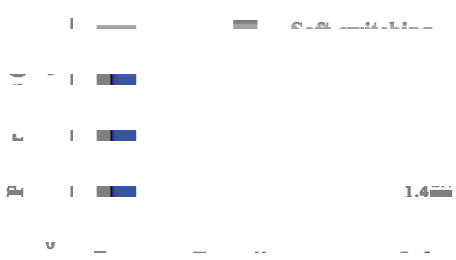

Fig. 11 Loss breakdown at Po=100W

GATE DRIVE DEISGN FOR E-MODE GAN DEVICES

The switching speed of GaN devices in terms of dv/dt and di/dt, is 3-5 times higher than that of Si MOSFETs [11]. The gate drive circuit should be carefully designed to avoid the issues brought by high di/dt and dv/dt.

di/dt immunity

When the GaN switch is turned off, the falling di/dt slope induces negative voltage on the common source inductance. The common source inductance consists of the inductance in the device package and the parasitic inductance of the PCB trace. This negative voltage will induce an opposing voltage across the gate-source of the GaN, which is intended to turn on the device as shown in Fig. 12.

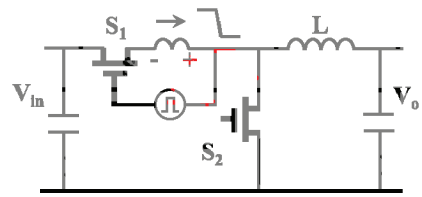

Fig. 12 di/dt impact on the gate drive circuit

The best way to improve the di/dt immunity is to minimize common source inductance by improving packaging and the PCB layout. Separating the gate and power loops with a Kelvin connection is helpful to reduce common source inductance. The internal source inductance of the GaN device also should be minimized. The PCB layout should also decouple the power loop and driving loop to avoid creating any common source inductance.

dv/dt immunity

The dv/dt related driving issue is more complicated and difficult than the di/dt problem. In most cases, a level shifter or isolator are used for the high side driver. Parasitic capacitance of this part is a high-frequency noise path for the common-mode current generated by the switch node dv/dt. For a positive dv/dt event, the high-voltage slew rate across the capacitor C_{IO} generates the common-mode current which flows in the loops, as shown in Fig. 13. This common-mode current causes ground bounce on the PWM input side and can cause changes in the logic state. For a negative dv/dt event, the common-mode current flows clockwise and can also deteriorate the PWM signal.

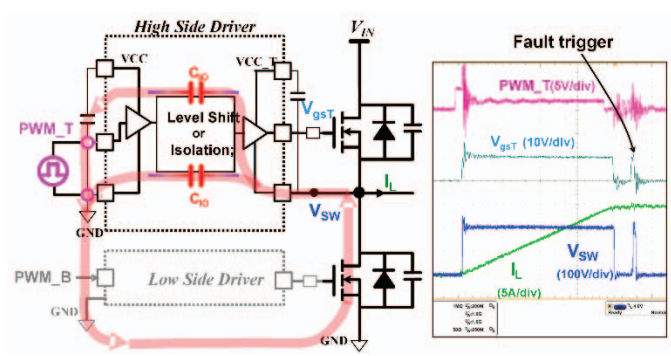

Fig. 13 dv/dt impact on the gate drive circuit

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Generally speaking, a bootstrap IC, optocoupler, driving transformer, and digital isolator are typical candidates for the high side driver. Among these four candidates, the digital isolator has the lowest parasitic capacitance and smallest propagation delay. These features make it suitable for GaN application. The bootstrap power supply is preferred for the high side digital isolator and high speed driver since the junction capacitor of the bootstrap diode is relatively small and the size is also very small which allows to put the decoupling capacitor as close to the dv/dt noise source ground as possible to minimize the common-mode current loop. To further improve the dv/dt immunity, a negative bias circuit and RC filter can be added at the input PWM terminal.

The PCB layout also plays an important role in improving the dv/dt immunity for the high side driver. Avoiding PCB layout overlap between the ground and the high side can effectively reduce the parasitic capacitance. The experimental waveforms resulting from the improved driving circuit and PCB layout are shown in Fig. 14. The voltage ringing on the PWM signal is minimized, and the dv/dt immunity is over 120V/ns.

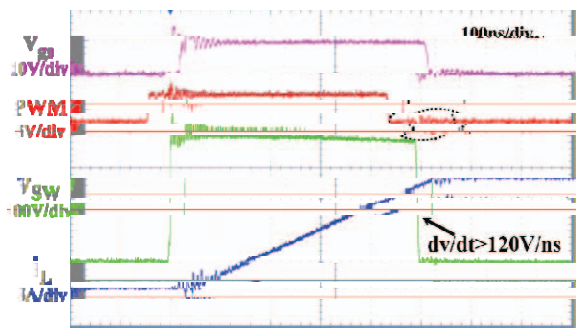

Fig. 14 dv/dt impact on the gate drive circuit

APPLICATIONS OF E-MODE GAN DEVICES

Based on the loss analysis in section II, soft-switching is desired for e-mode GaN in order to operate at very high frequency. Compared with cascode GaN, e-mode GaN devices prefer small turn-off current applications as indicated in Fig. 9. One advantage of e-mode GaN over cascode GaN at soft-switching condition is the smaller junction capacitor charge which requires less circulating energy. We take a low power adapter and a 1kW LLC converter as examples to show the impact of GaN devices on system design.

65W High density apdater

The adapter is strongly driven by efficiency and power density for all forms of portable electronics. The state-of-the-art product only operates at relatively low frequencies (<150 kHz), with efficiency up to 91.5%. The power density is low and typically it is around 9-11 W/in^3. Flyback converters are the dominant topology for low-power adapter application due to their simplicity and low cost. The traditional flyback transformer is hand-made, which is an intensive, labor-involved manufacturing process. The manufacturing cost is a concern, and the parameter variation is another circuit design issue.

The e-mode GaN devices show great potential in this application. The switching frequency can be easily pushed to MHz with active clamp circuit. By adding an active clamp circuit, the voltage stress is low, the leakage energy can be recycled, and more importantly, both main switch and clamp switch can achieve ZVS with proper design. All the passive components can be shrunk significantly by increasing frequency to 10 times of current practice. The PCB winding-based transformer is feasible due to its capacity for fewer turns and a smaller core size. The leakage inductance and parasitic capacitance of the transformer can be well-controlled by PCB manufacturers. Moreover, shielding can be easily integrated in the PCB winding to reduce the CM noise [12].

Fig. 15 shows the prototype of a MHz active clamp flyback converter. The power density excluding the case is over 40W/in^3, which is at least two times higher than the state-of-the-art product. The measured full-load efficiency over a wide input range is 1-2% higher than the state-of-the-art product.

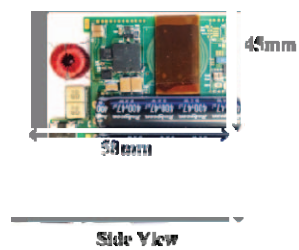

Fig. 15 Prototype of 65W MHz active clamp flyback converter

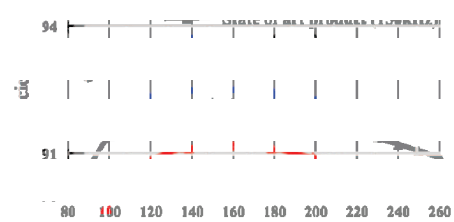

Fig. 16 Efficiency comparison of MHz prototype and state-of-the-art product

High density LLC converter

LLC resonant converter is widely used in consumer electronics due to its capability of ZVS and small turn-off current of the primary switch. E-mode GaN devices are very suitable for LLC converter due to its smaller junction capacitor charge. A 1kW 400V to 12V LLC resonant converter is built to demonstrate the advantage of the GaN device and its impact on system design. The switching frequency is 1MHz and the primary switch is 650V e-mode GaN device.

Instead of a traditional single-core structure with litz wire winding, the proposed design has eight transformers integrated into four cores and PCB winding. The turns ratio of each transformer is only 2:1, and the primary winding is in series and the secondary winding output is in parallel as shown in Fig. 17 [13]. The matrix transformer distributes the high output current and reduces the ac resistance of the windings. The flux cancellation method can be used to reduce core size and loss. Synchronous rectifier and output capacitors are integrated into

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the secondary windings to eliminate termination related losses and to reduce leakage inductance as well. All transformer windings can be implemented in a 4-layer PCB board. The 1MHz 1kW LLC converter prototype is shown in Fig. 18.

The prototype efficiency is shown in Fig. 19. The peak efficiency of the converter with proposed system structure is 97% and the power density can achieve 700W/in^3, which is 5-10 times higher than state-of-the-art industry practice. More importantly, the system design eliminates intensive labor process and it is easier for automatic manufacturing.

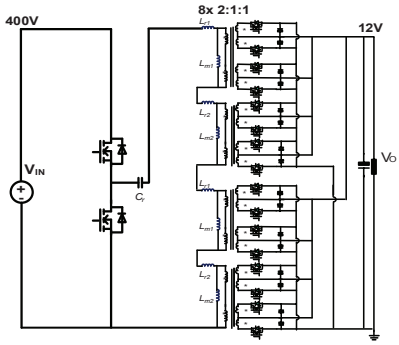

Fig. 17 LLC converter with matrix transformer structure

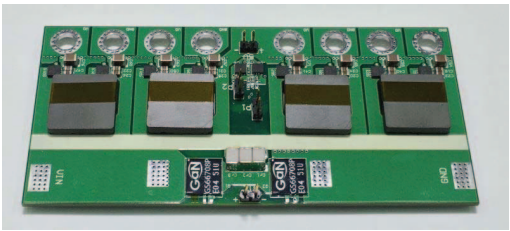

Fig. 18 Prototype of 1MHz 1kW 400V/12V LLC converter

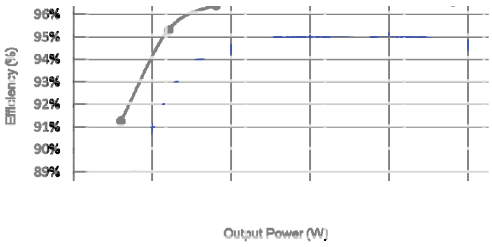

Fig. 19 Efficiency of the prototype

CONCLUSION

This paper presents the loss analysis and driving circuit design for 600V/650V e-mode GaN devices. The loss mechanism and the impact of package and driving circuit parameters are illustrated in detail. The comparison between e-mode GaN and cascode GaN shows that e-mode GaN has smaller turn-on loss due to no reverse recovery charge while cascode GaN has smaller turn-off loss due to structure advantage. Soft-switching is desired to fully exploit the advantage of e-mode GaN devices. The designs of the low power adapter using active clamp flyback converter and the 1kW LLC resonant converter demonstrate the efficiency and density improvement, and more importantly, the system level impact with GaN devices.

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