

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

IPR2024-00975
U.S. Patent 9,899,481

PETITION FOR *INTER PARTES* REVIEW

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TABLE OF EXHIBITS

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Ex-1001	U.S. Patent No. 9,899,481 (“the ’481 patent”)
Ex-1002	Prosecution History of the ’481 Patent (“Prosecution History”)
Ex-1003	Expert Declaration of Dr. Michael Lebby (“Lebby”)
Ex-1004	Curriculum Vitae of Dr. Michael Lebby
Ex-1005	U.S. Patent Application Publication No. 2014/0110760 (“Nega”)
Ex-1006	U.S. Patent Application Publication No. 2014/0175454 (“Roberts”)
Ex-1007	U.S. Patent Application Publication No. 2014/0225124 (“Otremba124”)
Ex-1008	U.S. Patent Application Publication No. 2014/0084433 (“Otremba433”)
Ex-1009	U.S. Patent No. 7,880,280 (“Otremba280”)
Ex-1010	U.S. Patent No. 10,930,524 (“Liu”)
Ex-1011	U.S. Provisional Patent Application No. 62/196,629 (“Provisional”)
Ex-1012	<i>Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.</i> , No. 3:24-cv-01553-SK, Dkt. No. 1, Complaint (N.D. Cal. Mar. 13, 2024)
Ex-1013	Anders Lind, <i>Source-Sense Packages for HV MOSFETs</i> , 46th International Symposium on Microelectronics (2013) (“Lind”)
Ex-1014	U.S. Patent No. 9,589,869 (“McKnight”)
Ex-1015	U.S. Patent Application Publication No. 2014/0097528 (“Otremba528”)

Exhibit	Description
Ex-1016	ThinPAK 8x8 New High Voltage SMD-Package (Apr. 2010) (“ThinPAK 8x8 Brochure”)
Ex-1017	Recommendations for Printed Circuit Board Assembly of Infineon VDSO Packages (ThinPAK) (July 2010) (“ThinPAK Recommendations”)
Ex-1018	U.S. Patent No. 9,099,441 (“Otremba441”)
Ex-1019	<i>Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.</i> , No. 3:24-cv-01553-SK, Dkt. No. 28, Order Granting Administrative Motion to Continue Initial Case Management Conference and Associated Deadlines (N.D. Cal. May 2, 2024)
Ex-1020	U.S. Patent No. 9,230,880 (“Otremba880”)
Ex-1021	U.S. Patent No. 8,691,631 (“Otremba631”)
Ex-1022	Excerpts of Stephen Pearton, <i>GaN and ZnO-based Materials and Devices</i> , Springer Series in Materials Science (2012) (“Pearton”)
Ex-1023	Excerpts of Muhammad H. Rashid, <i>Power Electronics Handbook</i> , Academic Press Series in Engineering (2001) (“Rashid”)
Ex-1024	Xiucheng Huang et al., <i>Evaluation and Applications of 600V/650V Enhancement-Mode GaN Devices</i> , IEEE Explore (2015) (“Huang”)

I. PRELIMINARY STATEMENT

Petitioner requests review of U.S. Patent 9,899,481 and cancellation of claims 1-17.

The '481 patent, filed in 2016, claims a lateral compound semiconductor device—a device with multiple base elements, like gallium nitride (GaN) as opposed to silicon (Si) alone—in a particular packaging layout. Compound semiconductors were well known, and packaging a compound device in known designs, using conventional components was obvious. Lebbby, [053]-[055]

II. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa. Lebbby, [056]-[058].

III. STATEMENT OF RELIEF REQUESTED

Petitioner requests review of claims 1-17 under the following:

Exhibit	Prior Art
Ex-1005	U.S. Patent Application Publication No. 2014/0110760 (“Nega”) (published April 24, 2014; prior art under AIA §102(a)(2)).

Exhibit	Prior Art
Ex-1006	U.S. Patent Application Publication No. 2014/0175454 (“Roberts”) (published June 26, 2014; prior art under AIA §102(a)(2)).
Ex-1007	U.S. Patent Application Publication No. 2014/0225124 (“Otremba124”) (published August 14, 2014; prior art under AIA §102(a)(1)).
Ex-1008	U.S. Patent Application Publication No. 2014/0084433 (“Otremba433”) (published March 27, 2014; prior art under AIA §102(a)(1)).
Ex-1009	U.S. Patent No. 7,880,280 (“Otremba280”) (issued February 1, 2011; prior art under AIA §102(a)(1)).
Ex-1010	U.S. Patent No. 10,930,524 (“Liu”) (provisional (Ex-1011) filed July 24, 2015 (“Provisional”); prior art under AIA §102(a)(2) (Section VII.A.2)).
Ex-1021	U.S. Patent No. 8,691,631 (“Otremba631”) (Published April 8, 2014, prior art under AIA 102(a)(1)).

Grounds		Challenged Claims	Basis	Prior Art
Nega Grounds	1A	1-3, 5, 6, 10, 11, 16	§103	Nega in view of Roberts
	1B	4, 9, 17	§103	Nega in view of Roberts and Otremba124
	1C	4, 7, 8, 17	§103	Nega in view of Roberts and Otremba433
	1D	7, 8	§103	Nega in view of Roberts, Otremba433, and Otremba280
	1E	12, 13	§ 103	Nega in view of Roberts and Otremba631
	1F	14, 15	§ 103	Nega in view of Roberts and Otremba280
Liu Grounds	2A	1, 2, 4-6	§103	Liu
	2B	3, 17	§103	Liu in view of Roberts
	2C	4, 9	§103	Liu in view of Otremba433
	2D	4, 9	§103	Liu in view of Otremba124
	2E	7, 8	§103	Liu in view of Otremba433 and Otremba280
	2F	17	§103	Liu in view of Roberts and Otremba433

IV. CLAIM CONSTRUCTION

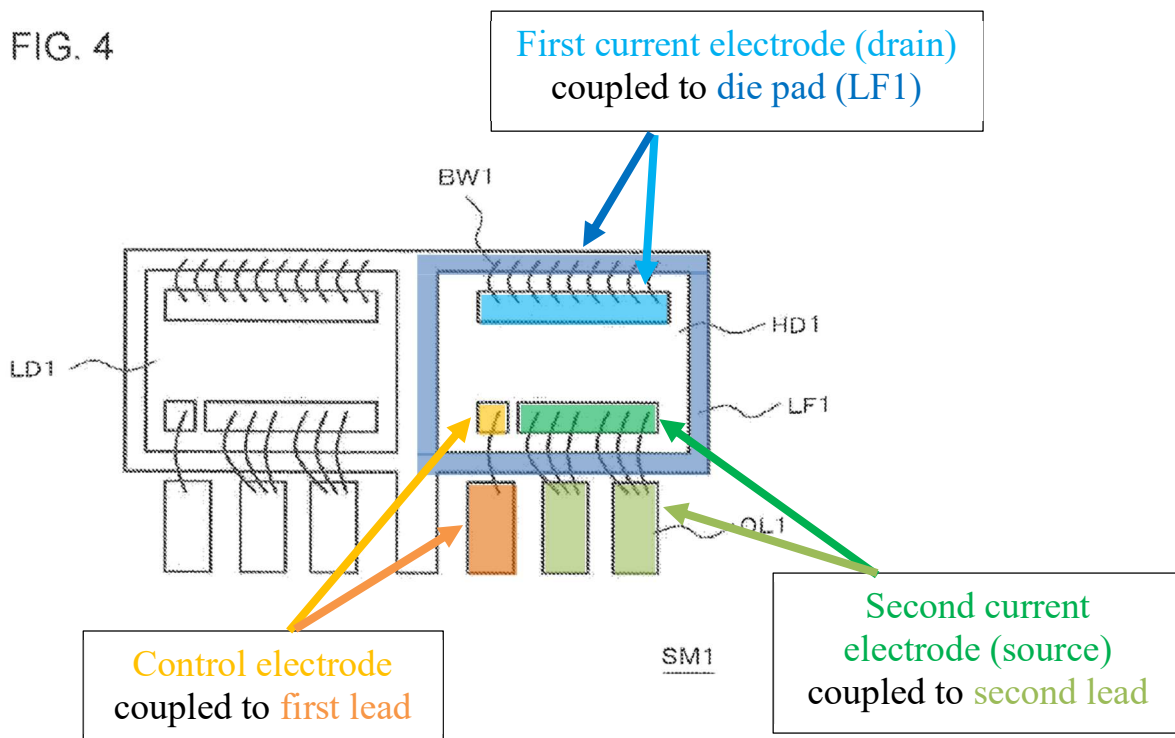
The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). For the purposes of this IPR, the plain meaning of each term can be applied. Lebbby, [059]-[064].

V. NEGA GROUNDS 1A-1F (CLAIMS 1-17)

A. Overview of the Combinations

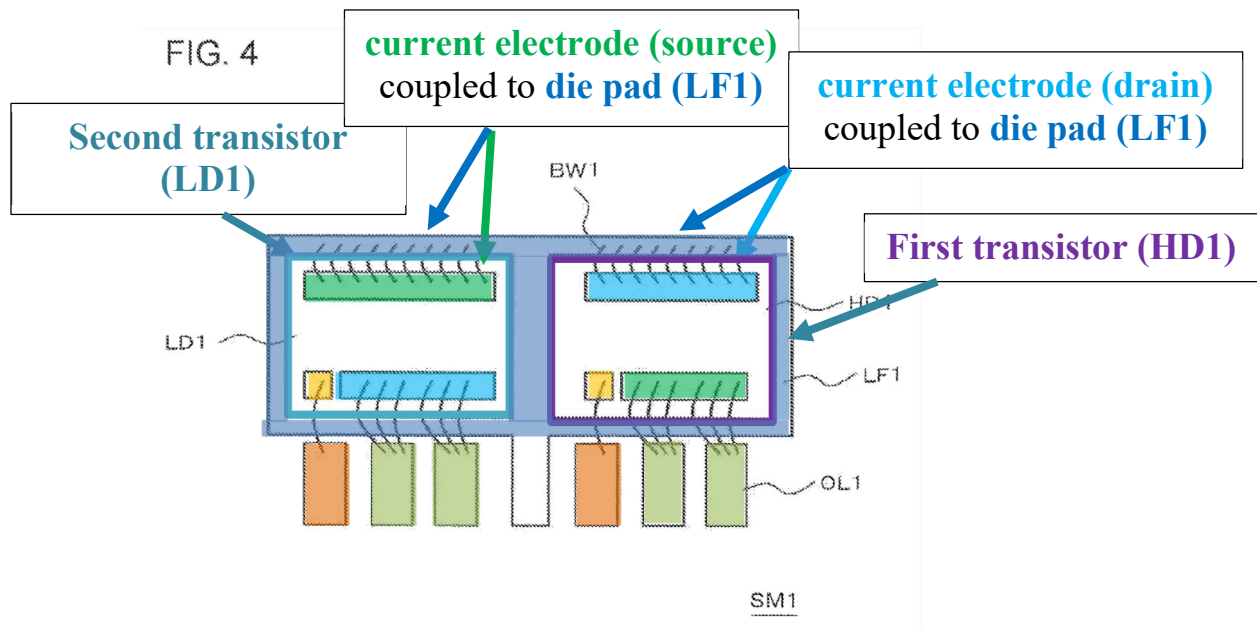
Nega discloses claims 1, 2-3, 5-6, 10, 11, 16 except a source sensing lead and standard electrical characteristics. Nega discloses “transistor HT1” where “one of the **source electrode SE1** and the **drain electrode DE1** is connected to the **lead frame LF1**, and the other thereof is connected to the **outer lead OL1**. The gate **electrode GE1** is connected to the **outer lead OL1**.” Nega, [0094]-[0095].

FIG. 4



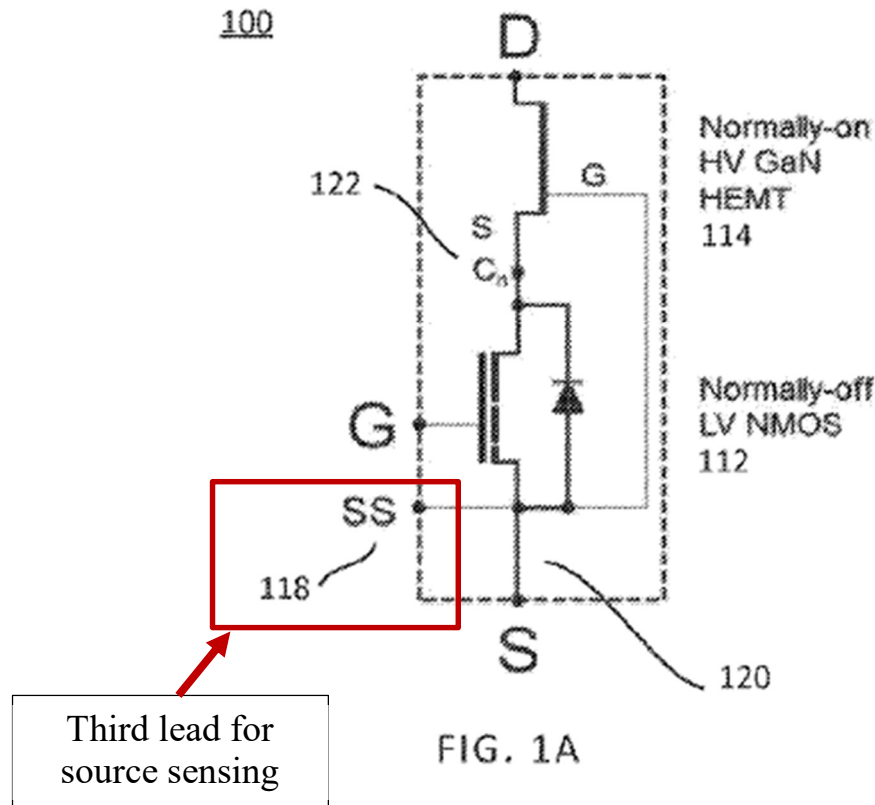
Id., Fig. 4 (annotated).

In conjunction with Nega’s second transistor (claim 10):



Nega, Fig. 4 (annotated).

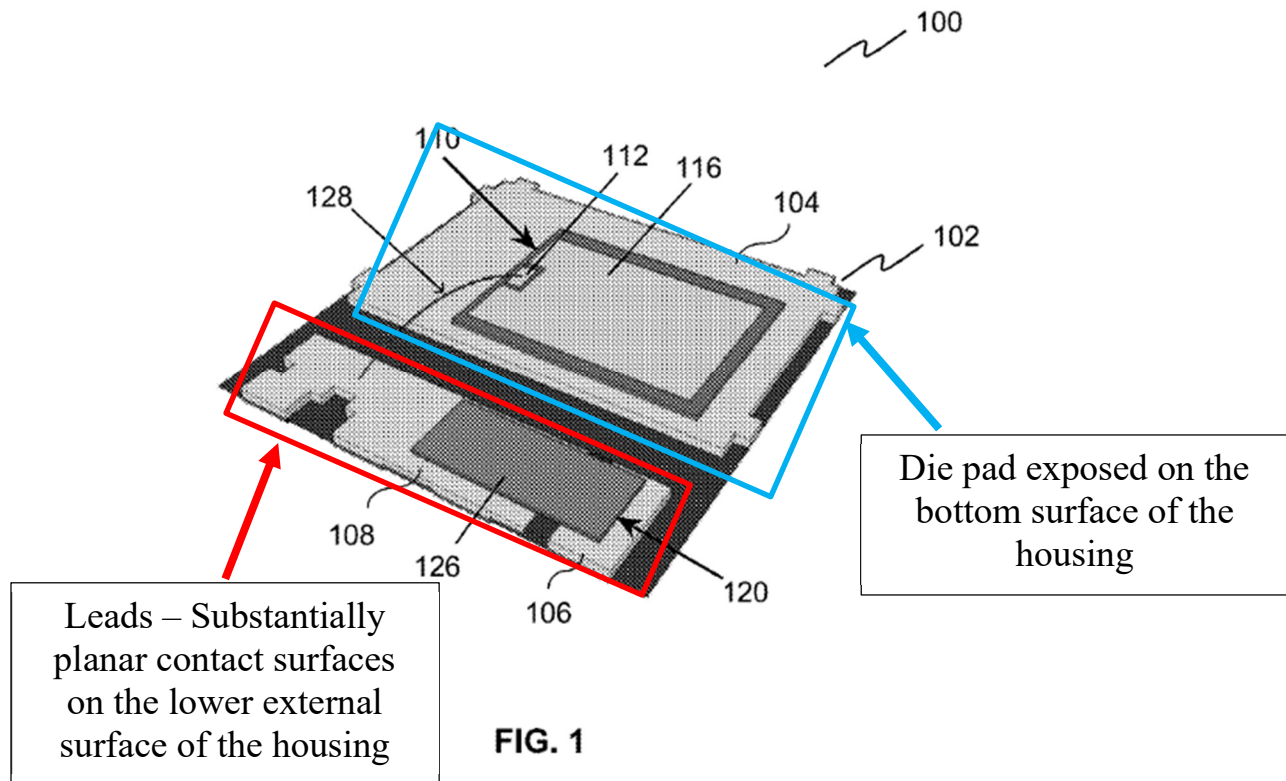
Roberts discloses a source sensing lead (claims 1, 10) and blocking voltages and switching speeds (claims 3, 17). Roberts discloses “a ‘Kelvin Source Sense’ or Kelvin connection SS ... provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive $L \, di/dt$ noise generated by the high current fluctuations of the source sense connection S.” Roberts, [0056], Fig. 1A.



Id., Fig. 1A (annotated).

Roberts also discloses that high-voltage-application transistor characteristics, “e.g., 600/650V” in “normally-on (depletion mode) transistors,” were known (*id.*, [0006], [0012]), and that GaN transistors “provide <20 ns switching time and more than 30 A current switching capability” (*id.*, [0008]).

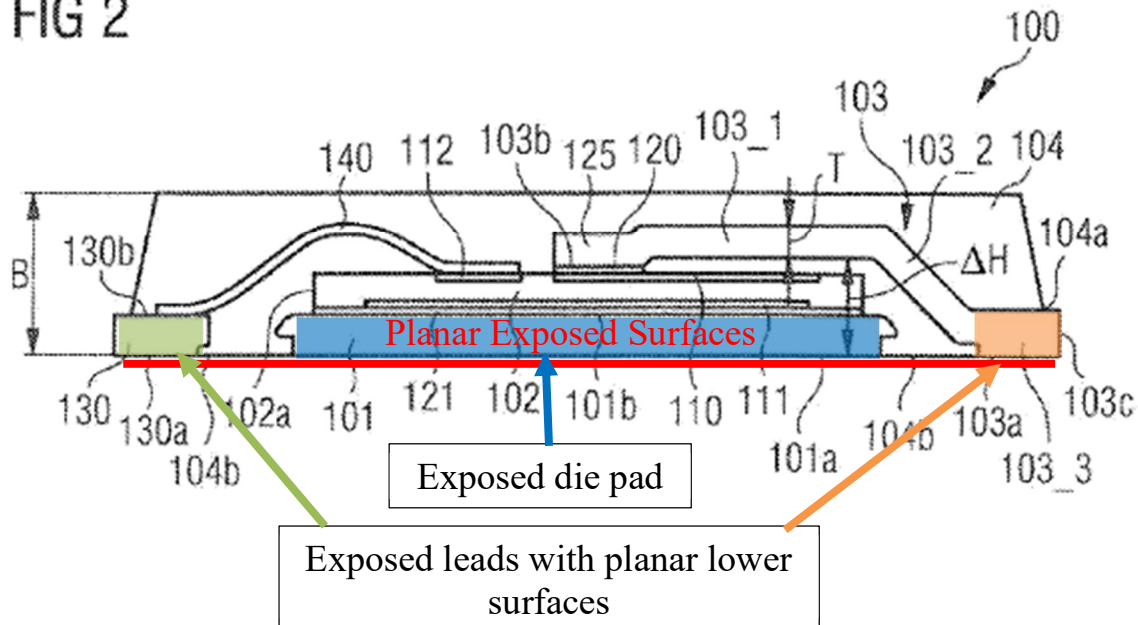
Otremba124 discloses a ThinPAK8x8 packaging, including planar exposed leads and an exposed die pad (claims 4, 9, 17) in design. Otremba124, [0041].



Id., Fig. 1 (annotated).

Otremba433 discloses planar exposed leads, an exposed die pad (claims 4, 17), and connecting components using contact clips (claims 7, 8). Otremba433 discloses “external contact area[s]” 103a and 130a that are “coplanar with a reference plane defined by a bottom surface 101a of the carrier 101” (die pad) that is “exposed at the bottom of the package.” Otremba433, [0037], [0039].

FIG 2

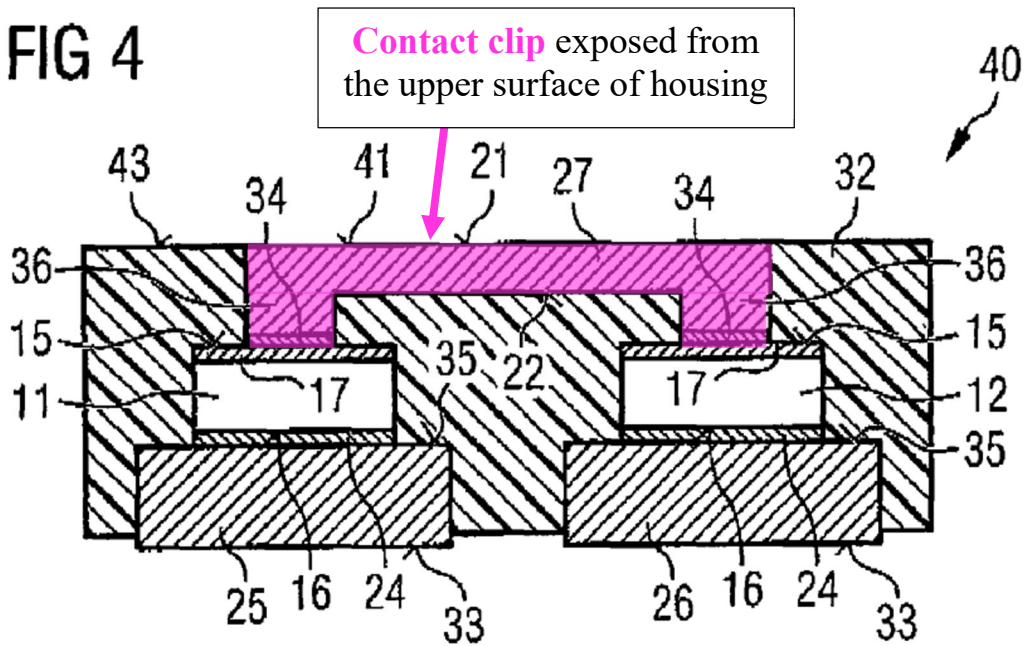


Id., Fig. 2 (annotated).

Otremba433 discloses coupling components with a “conventional contact clip” instead of bond wires. *Id.*, [0072].

Otremba280 discloses using exposed contact clips to couple components (claims 7, 8). Otremba280, 8:33-41, Fig. 4.

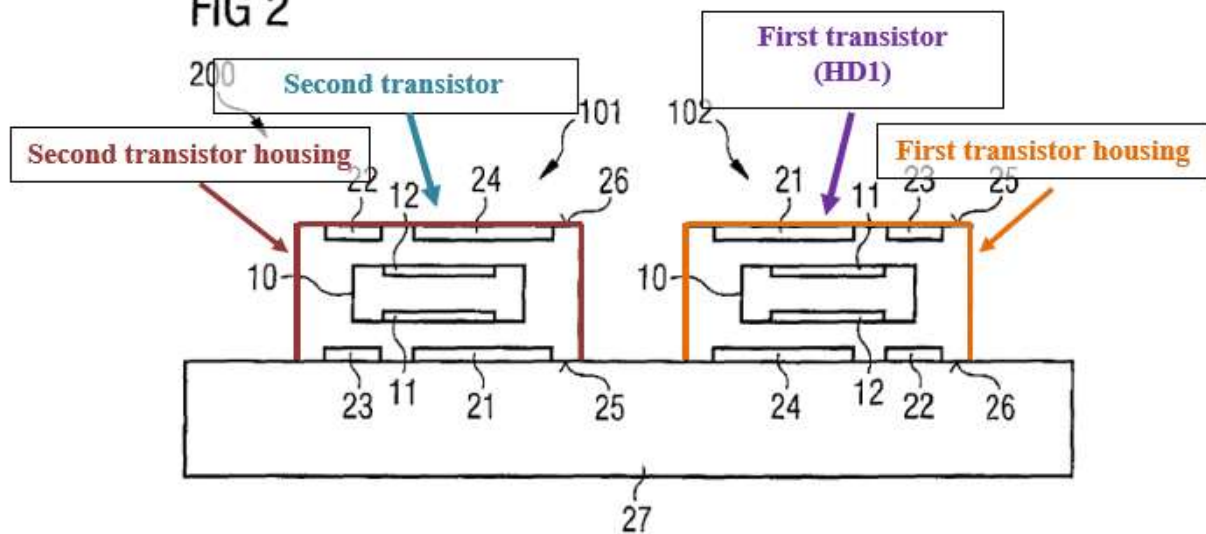
FIG 4



Id., Fig. 4 (annotated).

Otremba631 discloses packaging two transistors with separate housings and mounting surfaces coupled to a board (claims 12 and 13). Otremba631, 4:64-67.

FIG 2



Id., Fig. 2 (annotated).

All references are analogous because they are in the same field of endeavor as the '481 patent—packaging semiconductor electronic components. *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). Lebbby, [065]-[077], [080]-[092].

B. Ground 1A: Nega in View of Roberts Renders Obvious Claims 1-3, 5, 6, 10, 11, and 16

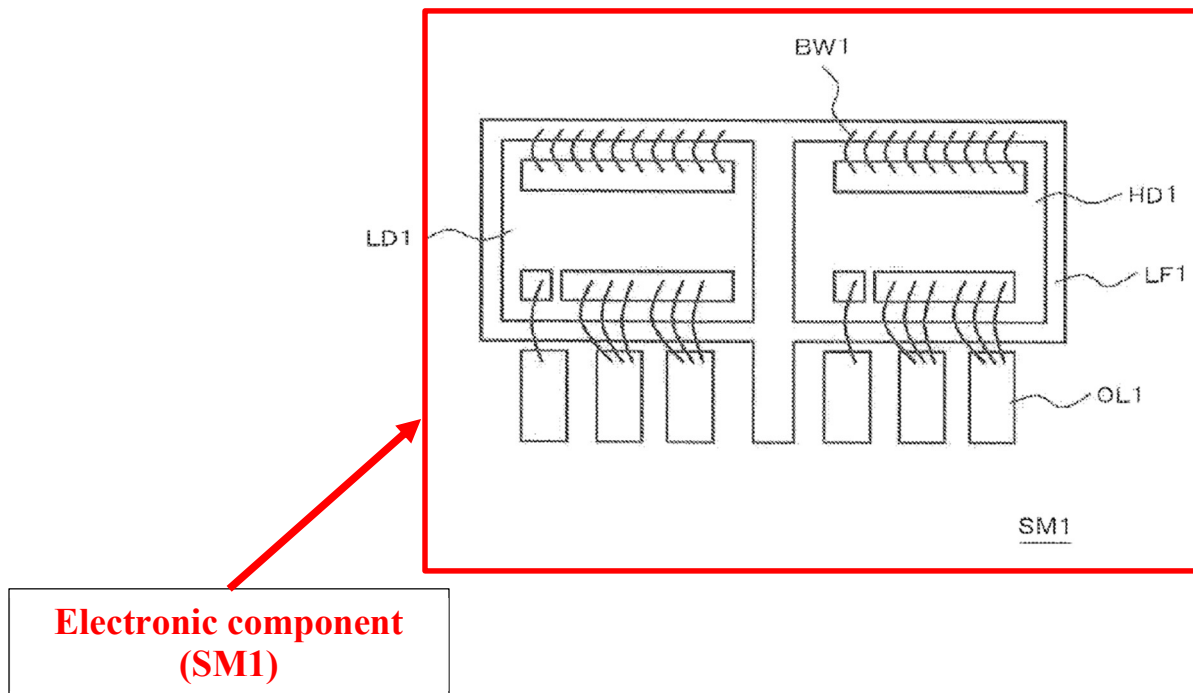
1. Claim 1

a. [1pre]: An electronic component, comprising:

Nega discloses [1pre] because Nega discloses a “semiconductor device SM1.”

Nega, [0090], [0018]. Lebbby, [093]-[094].

FIG. 4

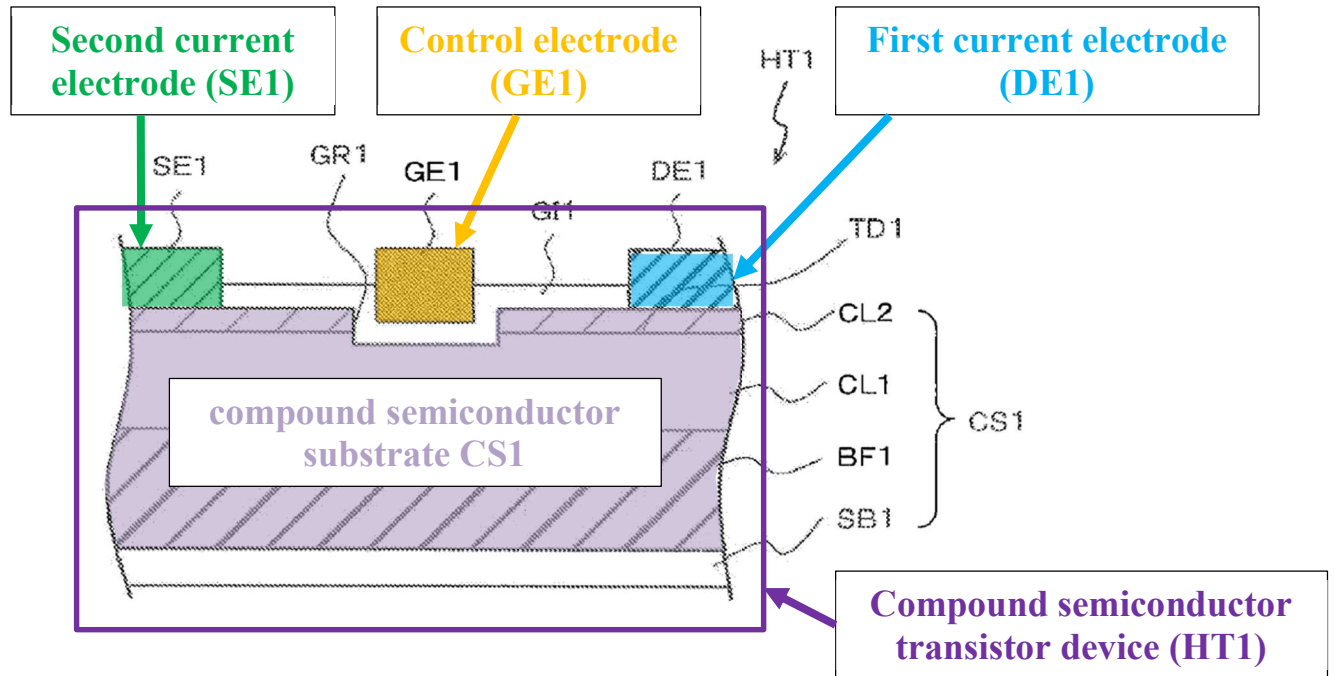


Id., Fig. 4 (annotated).

- b. [1a]: a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;

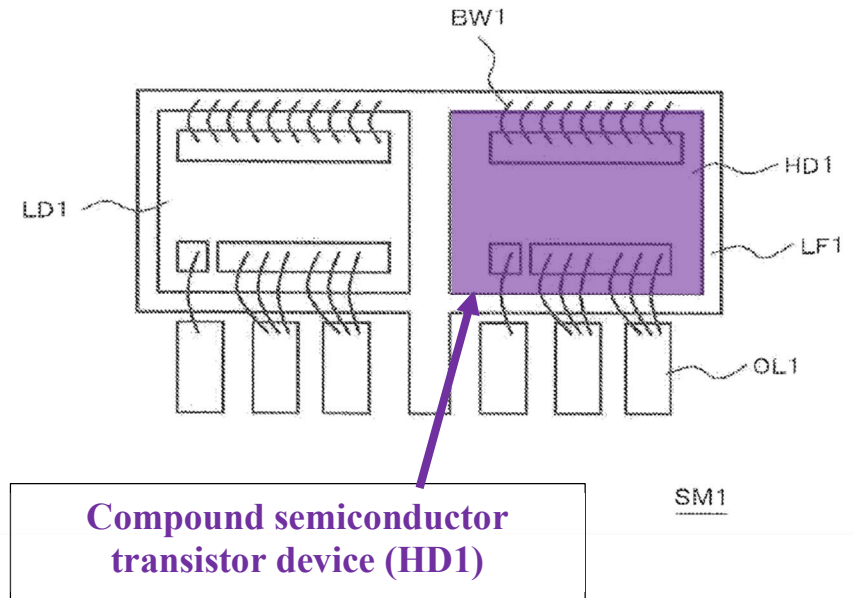
Nega discloses [1a] because it discloses **transistor HT1 (compound semiconductor transistor)** (*id.*, [0046]) with a **drain electrode DE1 (first current electrode)** (*id.*, [0058]), a **source electrode SE1 (second current electrode)** (*id.*), and a **gate electrode GE1 (control electrode)** (*id.*, [0056]). Nega's HT1 transistor is a compound semiconductor transistor device because "HT1 is formed in the **compound semiconductor substrate CS1** having the two-dimensional electron gas layer TD1" (*id.*, [0034]), including a "compound semiconductor layer CL1 [that] is, ... a GaN layer" (*id.*, [0049]) and a "compound semiconductor layer CL2 [that] is ... an AlGaIn layer" (*id.*, [0050]). Lebbly, [095]-[096].

FIG. 2



Id., Fig. 2 (annotated).

FIG. 4

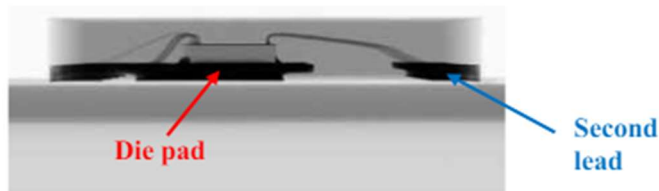


Id., Fig. 4 (annotated).

c. [1b] a die pad; and

Nega discloses [1b] because it discloses lead frame LF1 (die pad).

A die pad is a common component of transistor devices generally comprising a conductive material that supports the die of the semiconductor device and is part of a lead frame. It is also commonly referred to as a die-attach pad, or generically as a lead frame (with the die pad as a specific part). Lebby, [096]. Infineon's infringement allegations are consistent with a lead frame and a die pad being similar and often interchangeable, mapping a lead frame as the die pad:



Side-view X-ray photograph of INN650DA190A along the direction of the arrow marked "side view" in the plan-view X-ray photograph above (annotations added)

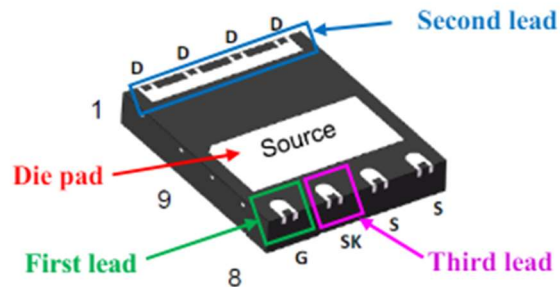
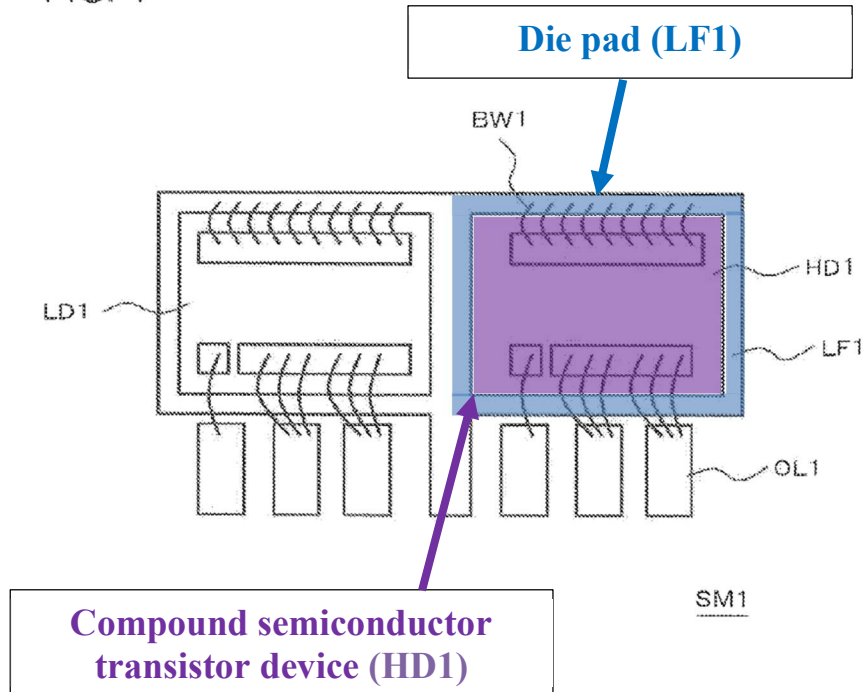


Exhibit D, INN650DA190A Datasheet, at 1 (annotations added)

Ex-1012, 19-20 (identifying frame supporting the transistor device as “die pad”).

Nega’s lead frame LF1 supports active device HD1/HT1 (Nega, [0095]) and constitutes a die pad under Infineon’s interpretation. *Id.*, [0091]-[0095]. Lebby, [097]-[099].

FIG. 4



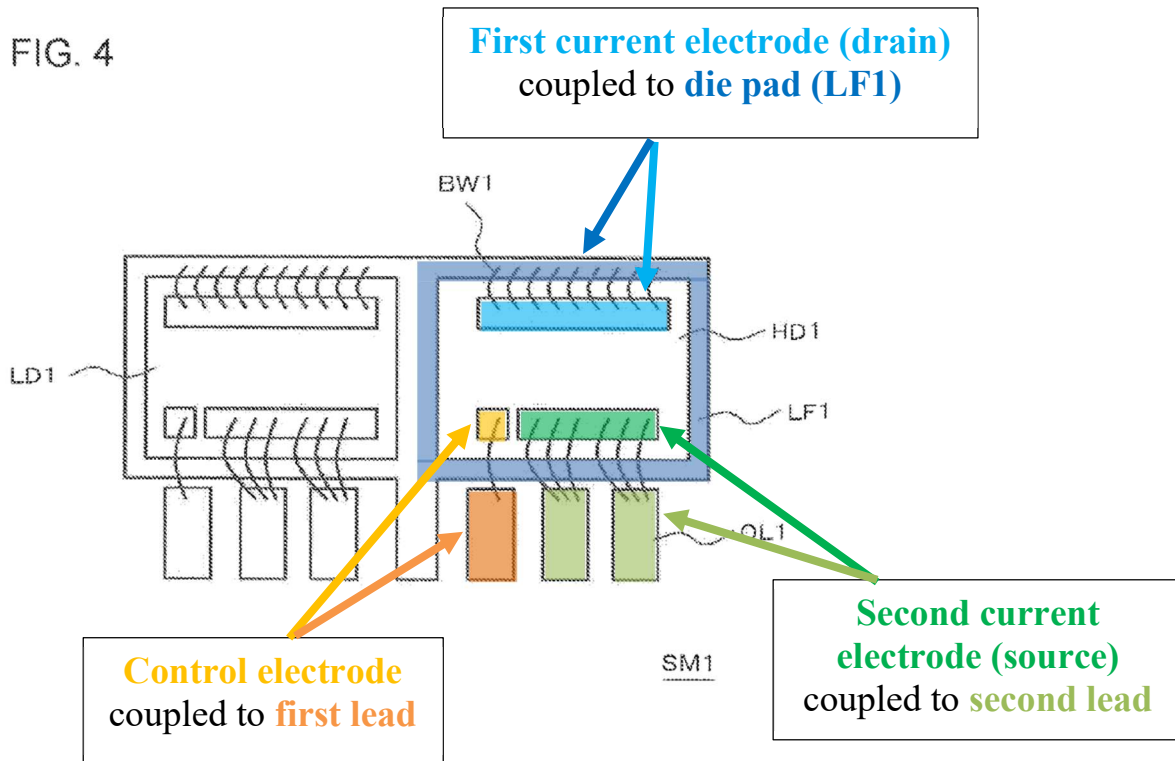
Id., Fig. 4 (annotated).

- d. [1c] a first lead, a second lead and a third lead,
- [1d] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,
- [1e] wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,

[1c]-[1e] recite three leads and couplings. Nega's HT1 compound semiconductor transistor device has all but the third lead providing source sensing functionality—but Roberts discloses a third lead for source sensing functionality, as was known in the art.

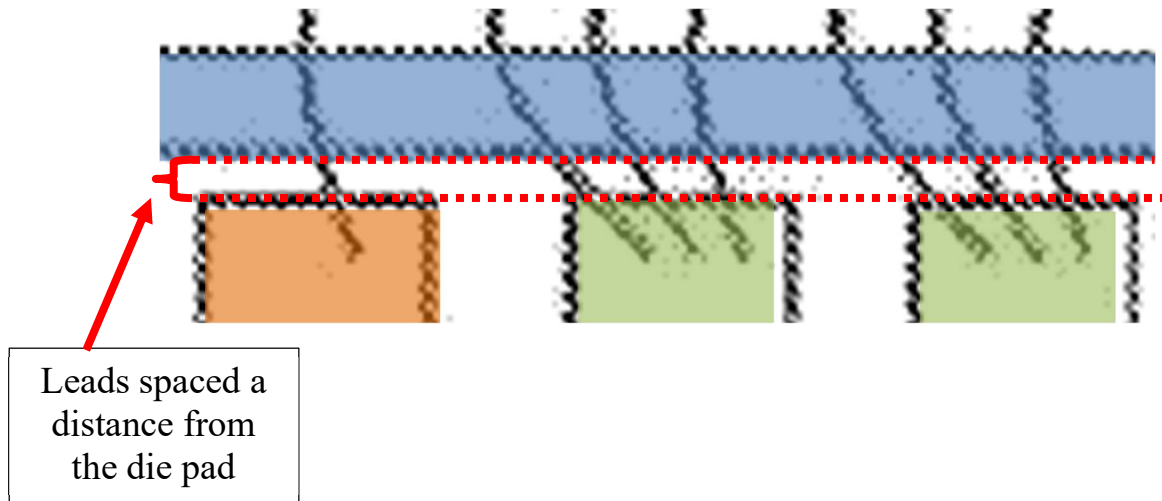
As explained for [1a], Nega's HT1 includes a drain electrode **DE1 (first current electrode)** (*id.*, [0058]), a **source electrode SE1 (second current electrode)** (*id.*), and a **gate electrode GE1 (control electrode)** (*id.*, [0056]). "In the transistor HT1 constituting the high-side switching device HD1, one of the **source electrode SE1** and the **drain electrode DE1** is connected to the **lead frame LF1**, and the other thereof is connected to the **outer lead OL1**. In addition, the gate **electrode GE1** is connected to the **outer lead OL1**." *Id.*, [0095]. And Nega's "connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed ... using ... a bonding wire BW1." *Id.*, [0094].

FIG. 4



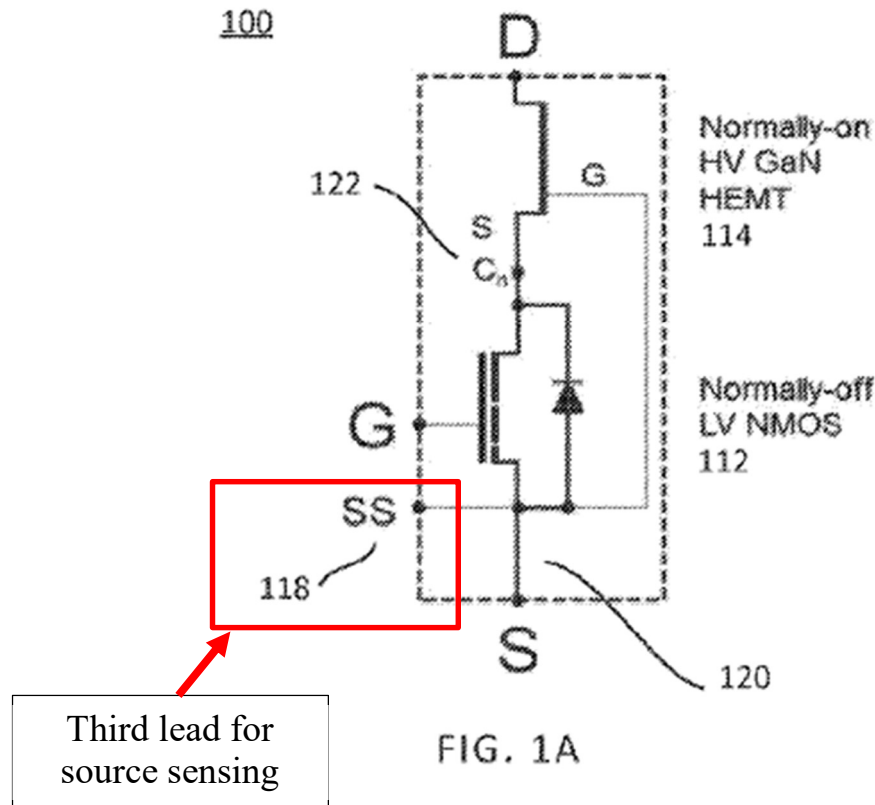
Id., Fig. 4 (annotated).

Nega's first and second leads (OL1) are spaced a distance from the die pad (LF1) because they are aligned separate from but adjacent to LF1, with a space separating them. *Id.*



Id. (excerpted, zoomed, annotated).

Nega does not expressly disclose a source sensing third lead, but Roberts does, as was common. Roberts explains that in a “high voltage (HV) normally-on, depletion mode, GaN FET, which may comprise a GaN HEMT”—a compound semiconductor transistor device—“a ‘Kelvin Source Sense’ or Kelvin connection SS is provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive $L \, di/dt$ noise generated by the high current fluctuations of the source [sense] connection S.” Roberts, [0055]-[0056], Fig. 1A. Lebbby, [100]-[0104].

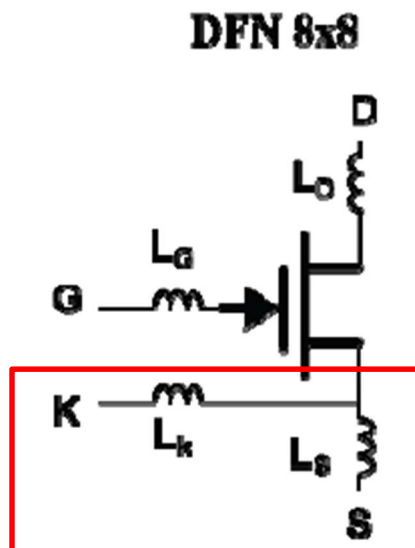


Id., Fig. 1A (annotated).

As Roberts recognizes, transients can be so high as to “result in unwanted switching,” so, as Roberts expressly teaches and suggests “it is desirable to provide a driver circuit that provides monitoring and control of noise and transients” by using a Kelvin Source Sense connection. *Id.*, [0056]-[0057]. This benefit of using a Kelvin Source Sense connection was well known, as evidenced by Lind and Huang.

Lind explains that “implementing a Source Sense connection allows measuring and monitoring at a close to constant di/dt , without any noise”—the

benefit expressly recognized by Roberts. Lebbby, [0104] (quoting Lind, 3); Roberts, [0056]. Huang explains that in GaN devices with high switching speeds, “common source inductance and inter-connected inductance are detrimental to switching loss and gate reliability,” and thus, using a package with a Kelvin (source sensing) connection “decouple[s] the power loop and driving loop” to “minimize the common source inductance.” Huang, 2.



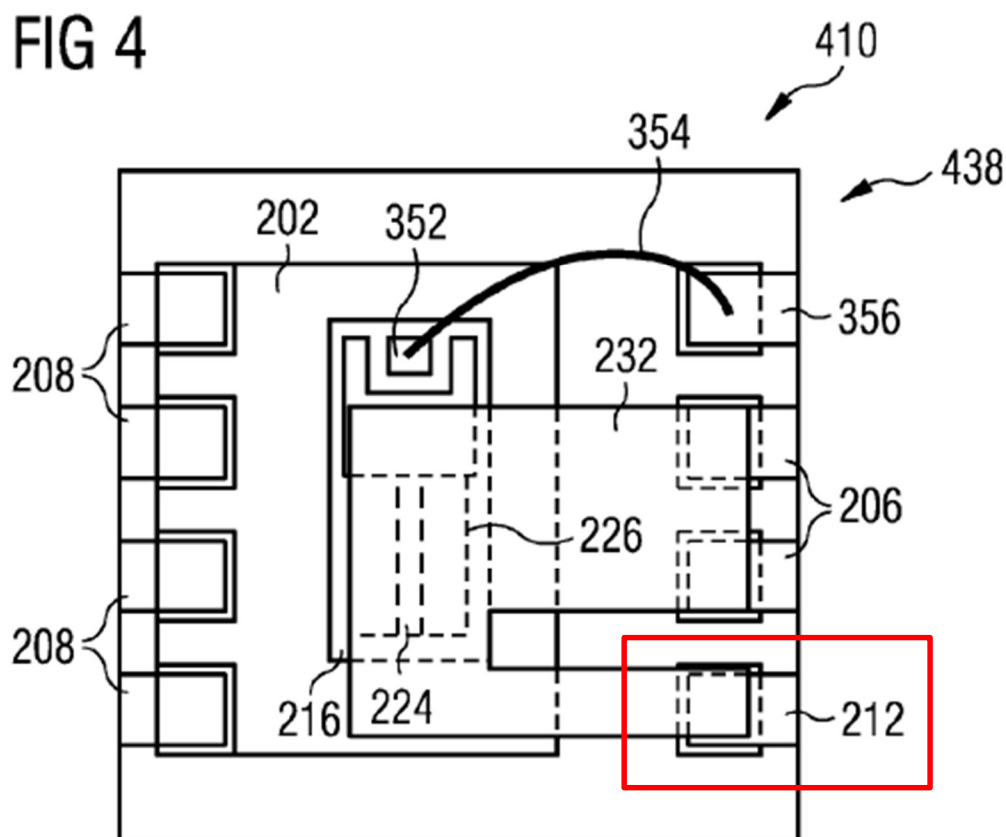
Huang, Fig. 2 (annotated).

In Roberts, a Kelvin Source Sense connection SS is provided by “separate Kelvin connection(s)” (Roberts, [0095]), which would be routinely implemented in Nega’s device by adding an additional external connection or contact pad connected to the transistor, for source sensing functionality, as evidenced by Huang, McKnight,

and Otremba528. Lebbby, [0103]-[0105]. Huang shows a separate Kelvin lead implemented in a DFN8x8 package. Huang, 2, Fig. 2.

McKnight, like Roberts, expressly discloses that in lateral GaN transistor devices, the package includes “an additional external contact pad, e.g.[,] a source sense (Kelvin) connection.” Lebbby, [0105]-[0109] (quoting, McKnight, 12:20-27).

Otremba528 expressly recognizes that a “source-sensing lead may be connected to a source contact to measure and/or monitor the potential of the source contact” (Otremba528, [0002])—the same purpose as Robert’s Kelvin Source Sense connection. Lebbby, [0106].

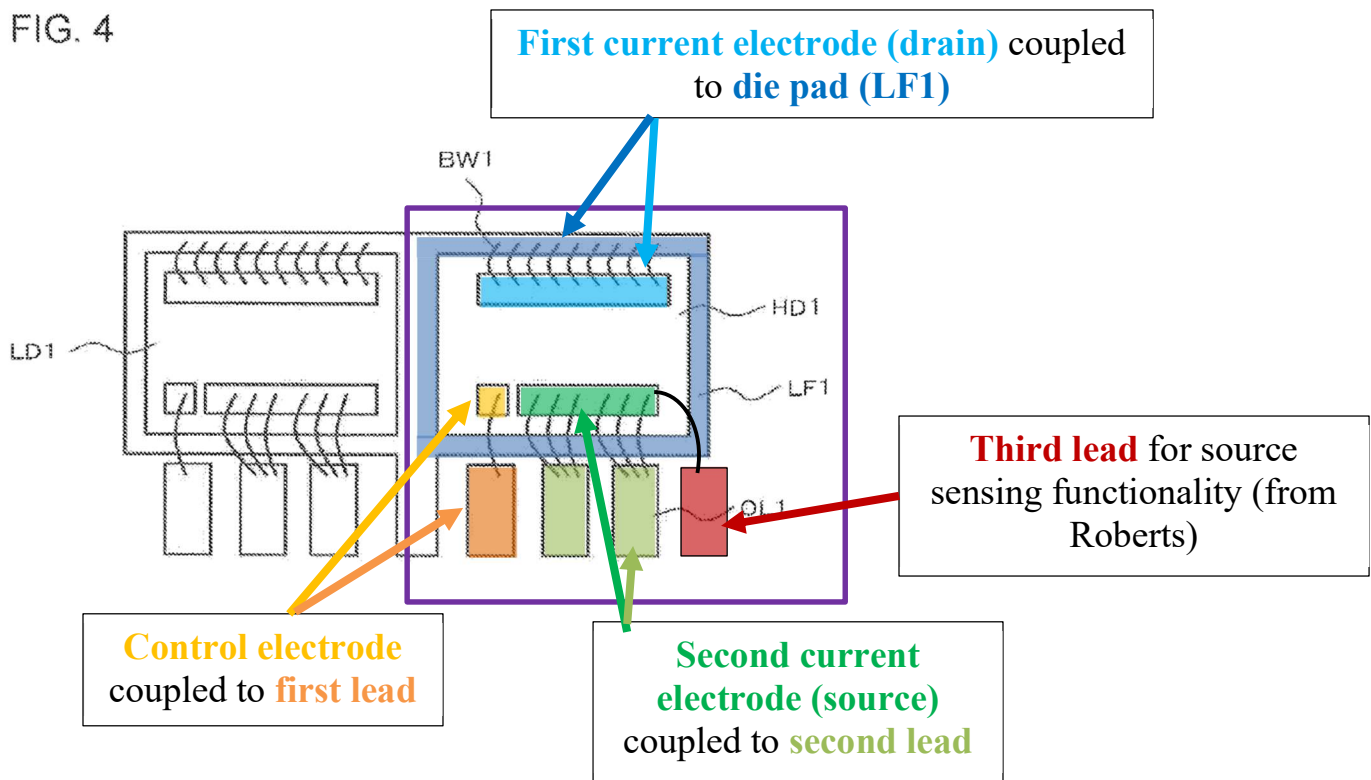


Id., Fig. 4 (annotated).

A POSITA would have been motivated to implement Robert's source sensing connection as a third lead in Nega's device and would have expected success because source sensing functionality had known benefits, and implementing source sensing functionality as a separate lead was known in the art—combining prior art elements according to known techniques to a known device ready for improvement to yield predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2001); Lebbby, [0110]-[0111].

Nega-Roberts teaches the following configuration, with the control electrode coupled to the first lead (Nega), the first current electrode coupled to the die pad (Nega), the second current electrode coupled to the second lead (Nega), and the third lead coupled to the compound semiconductor transistor device and providing a source sensing functionality (Roberts).

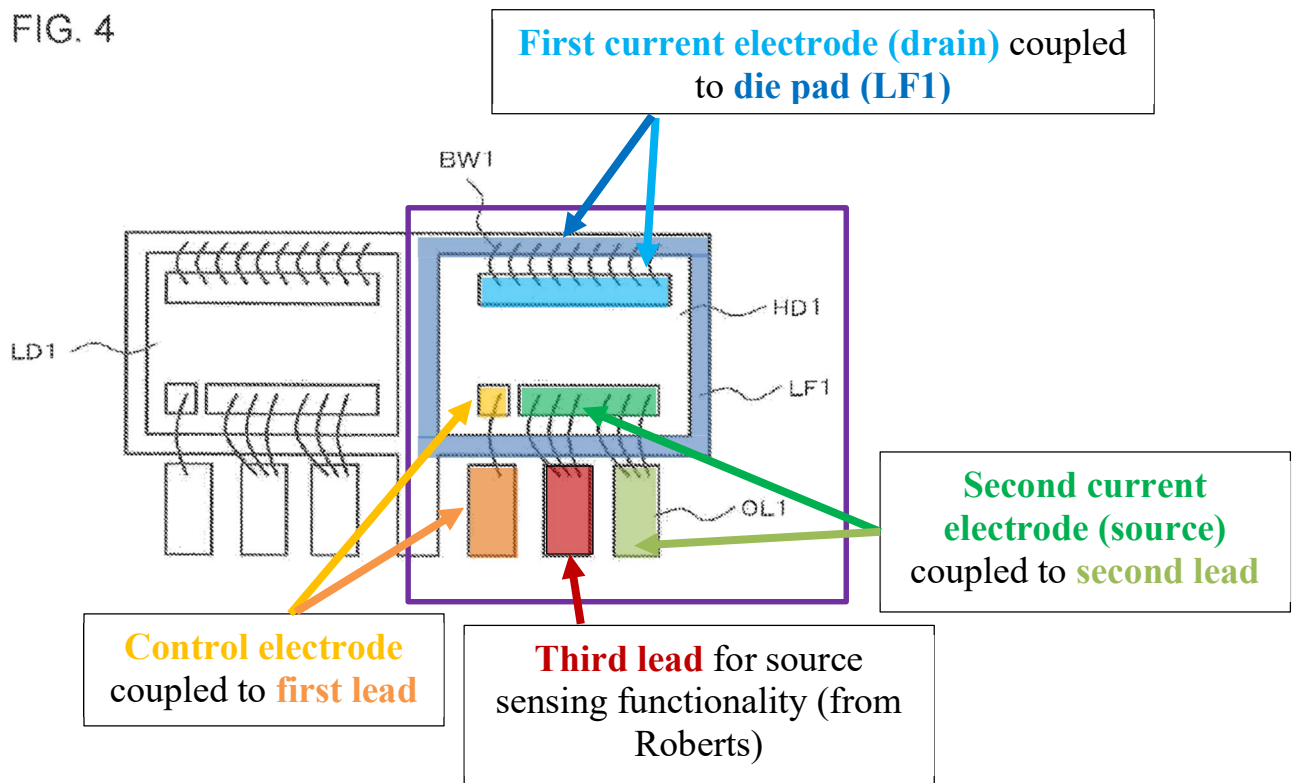
FIG. 4



Lebby, [0112]-[0114] (modifying Nega, Fig. 4 to add Roberts’s source sensing third lead).

Alternatively, Nega already discloses two leads connected to the source electrode. As Dr. Lebby explains, a POSITA would have understood that one of “these leads would readily be modified to serve as a lead for source sensing functionality, as taught by Roberts” because it was “known to interchange leads in packaging structures based on the application” (Lebby, [0110]); for example, Nega discloses interchanging the source and drain leads (Nega, [0095])). A POSITA would have understood that leads would simply be repurposed as a design choice within the skill of a POSITA with a reasonable expectation of success. Lebby, [0115].

FIG. 4



Nega, Fig. 4 (annotated).

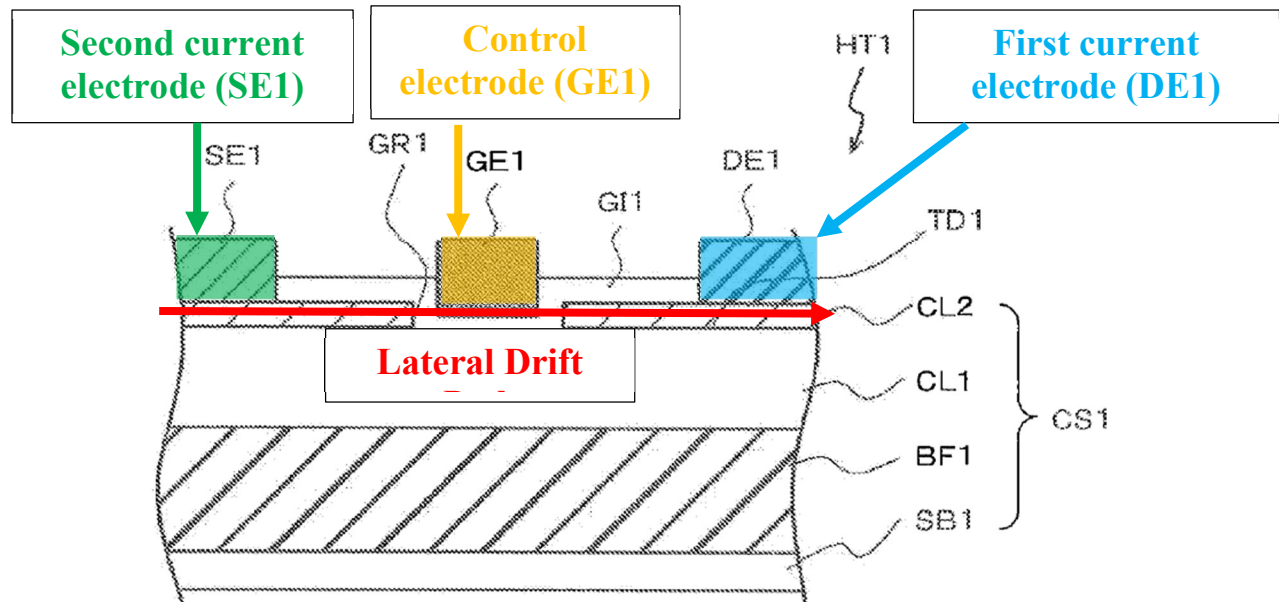
- e. [1f] wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad,

Nega discloses [1f] because HT1 is arranged laterally—gate, source, and drain side by side on the same lateral plane in a lateral drift path—and either of its source or drain is coupled to the lead frame LF1 (die pad).

The '481 patent explains that “lateral” means “run[ning] generally parallel to the lateral extent of a semiconductor material or semiconductor carrier” (Ex-1001, 3:14-18) and describes a device that “has a lateral drift path” (*id.*, 4:37-38). Nega’s

source, drain, and gate are spread laterally in a lateral drift path, instead of vertically stacked.

FIG. 2



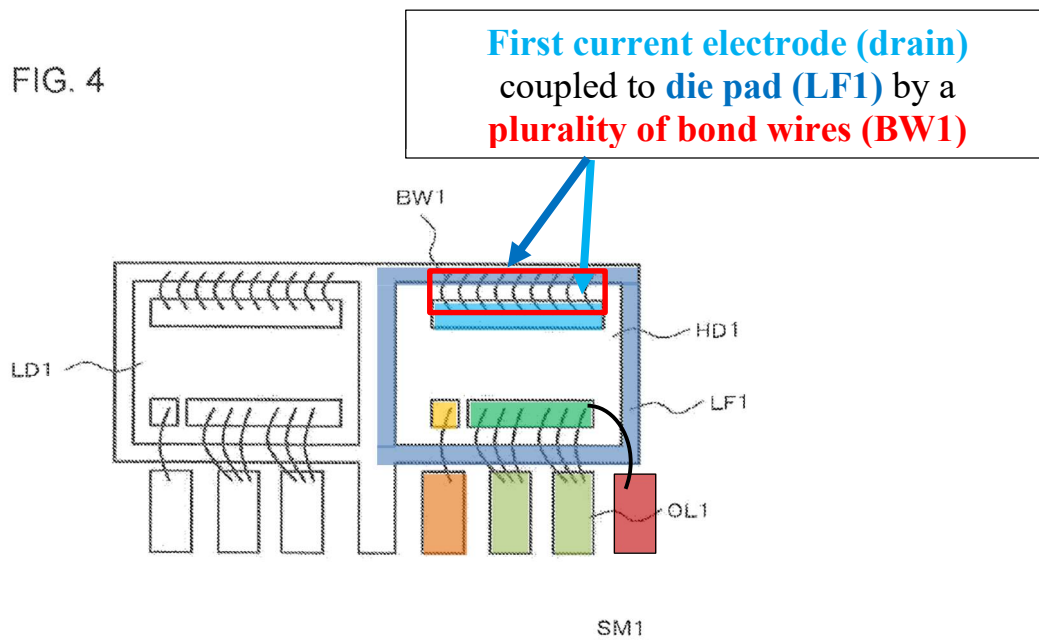
Nega, Fig. 2 (annotated).

Nega's source or drain is coupled to lead frame LF1 (die pad): "The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed ... using ... a bonding wire BW1." *Id.*, [0094]; Lebby, [0116]-[0118].

- f. [1g] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

Nega discloses [1g] because, as explained for [1f], the drain electrode (first current electrode) is coupled to lead frame LF1 (die pad) by a plurality of bond wires.

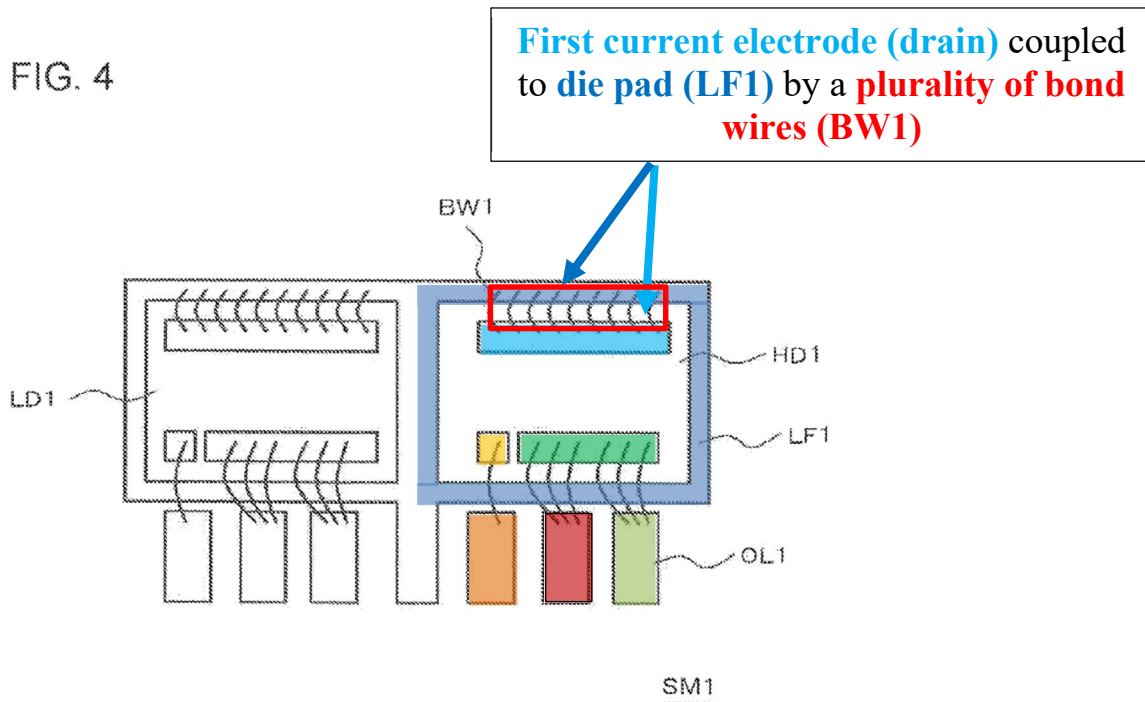
As explained for [1e]-[1f], Nega’s **drain electrode DE1 (first current electrode)** is coupled to the **lead frame LF1 (die pad)** by a plurality of bond wires. Nega states, “The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed ... using ... a bonding wire BW1.” *Id.*, [0094]. Nega’s drain is connected to lead frame LF1 by a **plurality of bond wires**—nine shown. *Id.*, Fig. 4; Lebby, [0119]-[0123].



Id. (annotated and modified).

Alternatively, repurposing one of Nega’s source leads as a source sensing lead:

FIG. 4

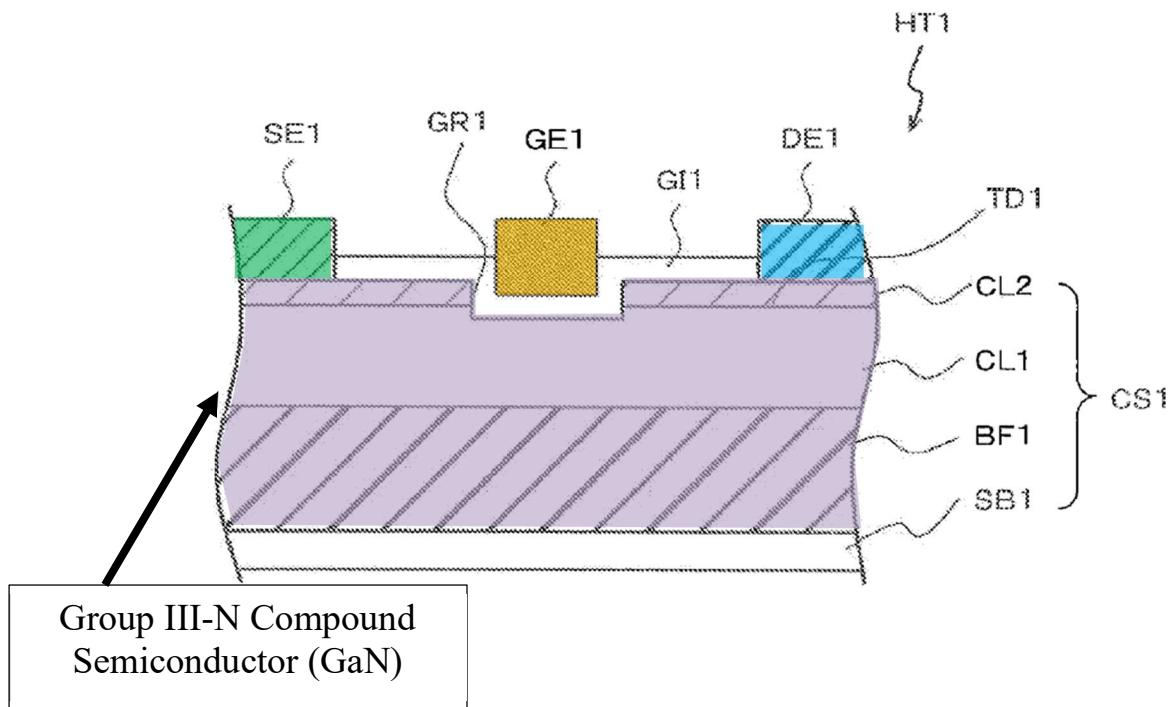


Id. (annotated).

2. **Claim 2 - The electronic component of claim 1, wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device.**

Nega discloses claim 2. The '481 patent explains that "Group III-N semiconductor devices" include "gallium nitride (GaN)" devices. Ex-1001, 1:21-25. Nega discloses a Group III-N device because it discloses that its transistor device HT1 includes "**compound semiconductor substrate CS1**" (Nega, [0034]), including a "compound semiconductor layer CL1 [that] is ... a GaN layer" (*id.*, [0049]) and a "compound semiconductor layer CL2 [that] is ... an AlGaN layer" (*id.*, [0050]). Lebbby, [0124].

FIG. 2



Id., Fig. 2 (annotated).

3. **Claim 3 - The electronic component of claim 1, wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.**

Nega in view of Roberts renders claim 3 obvious. A POSITA would have understood that Nega's compound semiconductor device would have achieved a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, which were common for high-voltage compound semiconductor power conversion transistors, as explained expressly by Roberts.

Claim 3 requires a transistor for high-voltage applications. The '481 patent explains that a transistor device's blocking voltage capability is its capability to block a voltage when the transistor is off—the maximum voltage that can be applied to a transistor while preserving operation. Ex-1001, 3:41-50; Lebby, [0125]-[0126]. Blocking voltage is also referred to as breakdown voltage. Lebby, [0126].

Roberts discloses that high-voltage (e.g., high blocking voltage capability) transistors were common in the art. Roberts explains that high-voltage transistor devices, “e.g., 600/650V” in “normally-on (depletion mode) transistors,” were well known. Roberts, [0006], [0012].

Although Nega does not expressly disclose switching frequency capability, Roberts discloses that switching frequency capabilities of at least 100 kHz were common for compound semiconductor devices (like Nega). Roberts, explains that GaN transistors “provide <20 ns switching time and more than 30 A current switching capability.” *Id.*, [0008]. The corresponding switching frequency is determined by: $\text{Hz} = 1/(\text{ns}/(1 \times 10^9))$. Applying this routine formula, switching time of 20 ns corresponds to 50 MHz—much greater than 100 kHz. Lebby, [0127]-[0128].

A POSITA would have understood that a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz were standard, routine, and readily-achievable characteristics for high-voltage compound

semiconductor transistors (like Nega). Lebby, [0129]. Higher blocking voltage capability and faster switching frequencies were some of the very benefits boasted by compound semiconductor devices generally, as opposed to traditional Si-based devices. As Dr. Lebby explains “GaN devices specifically were known for their high-frequency amplifying electronic applications and were suitable for high-power switching.” *Id.* (citing Ex-1024, 2 (“The switching speed of GaN devices is much faster than comparable Si.”)). Because Nega discloses compound semiconductor transistor devices but is silent on the corresponding switching time or frequency, a POSITA would have been motivated to look to references disclosing expected switching frequencies for compound semiconductor devices, like Roberts.

Here, as in *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1374 (Fed. Cir. 2019), a POSITA would have looked to references like Roberts “to better understand or interpret” the achievable characteristics of Nega’s device, including the switching frequency. Lebby, [0130]; *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1371 (Fed. Cir. 2018) (a motivation to combine may be based on “the background knowledge, creativity, and common sense of the person of ordinary skill” (quoting *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013))). Because these characteristics were common, well known, and readily achievable in compound semiconductor transistor devices, a POSITA would have had a reasonable expectation that Nega’s compound semiconductor transistor device would operate

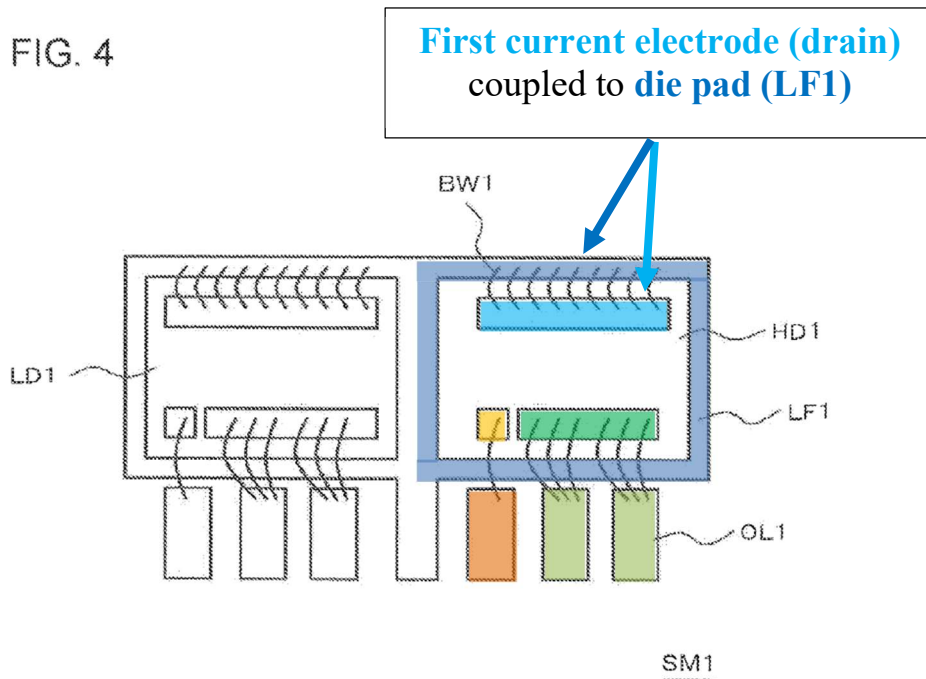
with a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz. Lebby, [0130].

4. Claim 5 – The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad.

Claim 5 directly contradicts the requirement in claim 1 that the compound semiconductor device is a lateral transistor (not a vertical transistor). Applicant expressly disclaimed vertical transistors during prosecution. Ex-1002, 31-32 (Sept. 19, 2017, Response to Office Action, amending claim 1 to recite a “**lateral transistor device**” to overcome a rejection over “Otremba ‘284[, which] teaches a **vertical** transistor” (emphases in original)).

To the extent claim 5 is interpreted as requiring a **lateral transistor** (consistent with claim 1) where the drain of the device is coupled to the die pad, Nega discloses it as explained for [1e]. Nega, [0095]; Lebby, [0131]-[0132].

FIG. 4



Id., Fig. 4 (annotated).

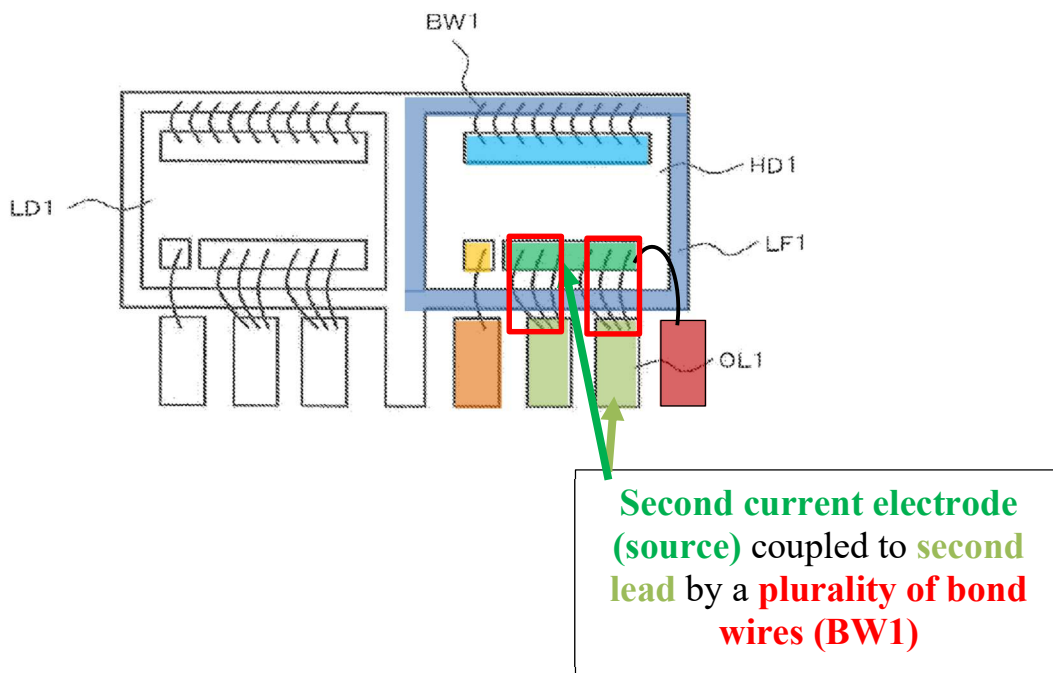
5. **Claim 6 - The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.**

Nega discloses claim 6 because its source electrode (second current electrode) is coupled to second lead OL1 by a plurality of bond wires BW1.

As explained for [1e], Nega's Figure 4 shows that, "[i]n the transistor HT1 constituting the high-side switching device HD1, one of the **source electrode SE1** and the **drain electrode DE1** is connected to the **lead frame LF1**, and the other thereof is connected to the **outer lead OL1**. In addition, the gate **electrode GE1** is connected to the **outer lead OL1**." *Id.*, [0095]. And Nega's "connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed ... using ... a

bonding wire BW1.” *Id.*, [0094]. Figure 4 shows a plurality of bond wires connecting the **source electrode SE1** to **outer lead OL1**—three bond wires for each lead. Lebbby, [0133]-[0135].

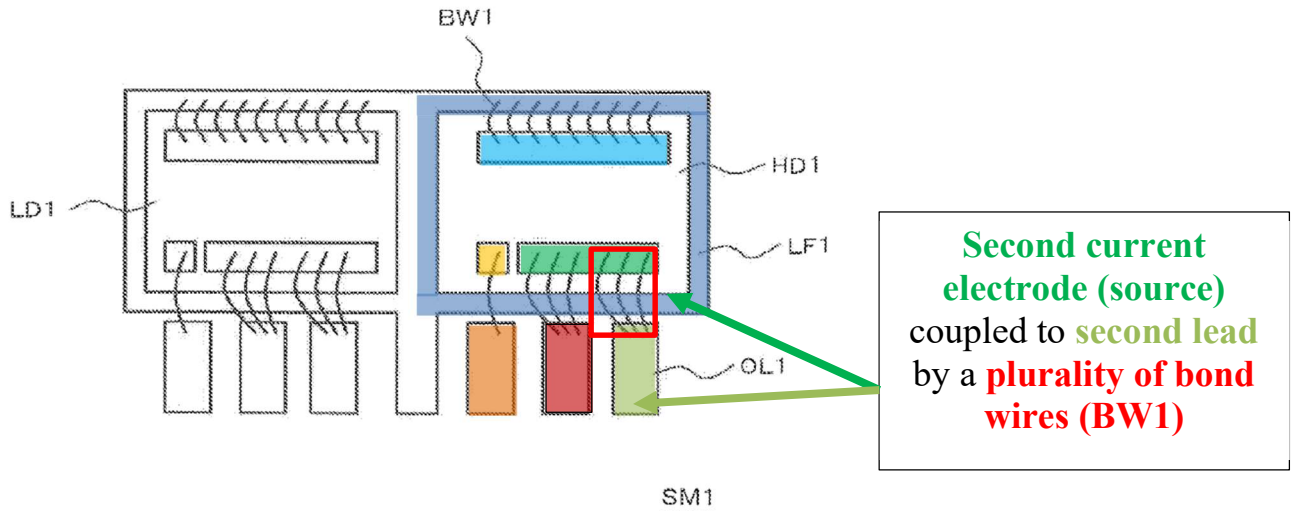
FIG. 4



Id., Fig. 4 (annotated, modified).

Alternatively, repurposing one of Nega’s source leads as a source sensing lead:

FIG. 4

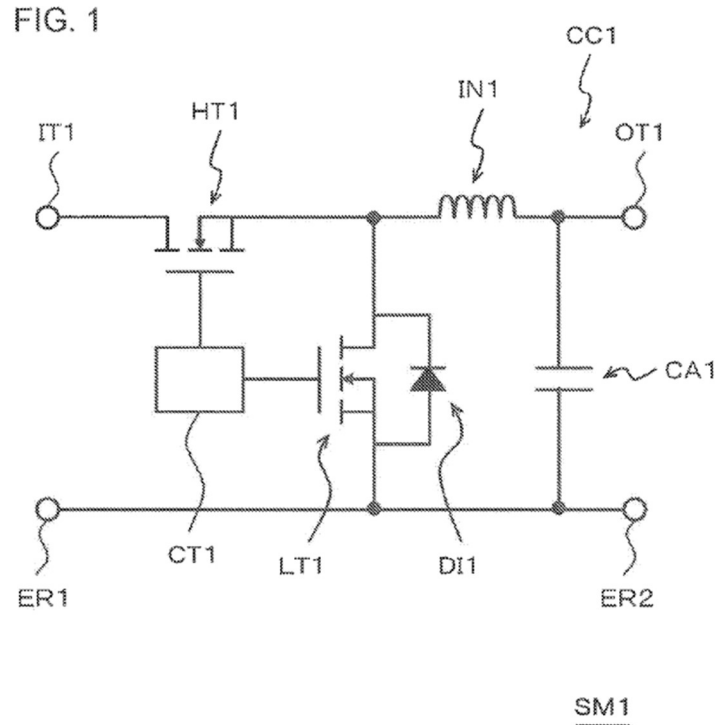


Id. (annotated).

6. Claim 10

a. [10p] A switch circuit, comprising:

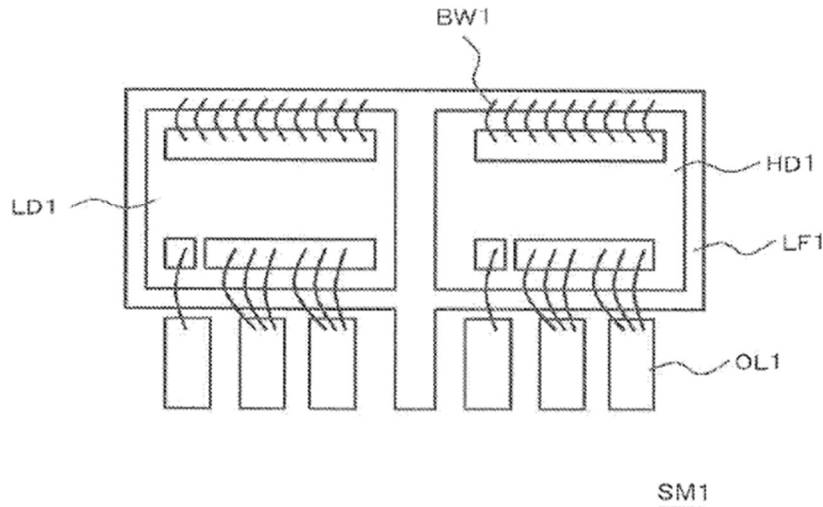
Nega discloses [10p] because it discloses a high-side switching device HT1 and a low-side switching device LT1 collectively comprising circuit CC1 (switch circuit) implemented in semiconductor device SM1. Nega, [0030]-[0034], [0037].



Nega, Fig. 1.

Nega explains that circuit CC1 is implemented in semiconductor device SM1, which includes a “high-side switching device HD1 constituted by the transistor HT1 and a low-side switching device LD1 constituted by the transistor LT1.” Nega, [0090]-[0091]; Lebby, [0136]-[0138].

FIG. 4



Nega, Fig. 4.

- b. [10a] a first transistor device comprising a compound semiconductor, a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead, and a third lead, the first lead the second lead and the third lead being spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the transistor device and provide a source sensing functionality, and

Element [10a] is identical to elements [1a]-[1e]. Nega-Roberts discloses [10a] as explained for [1a]-[1e]. Lebbby, [0139].

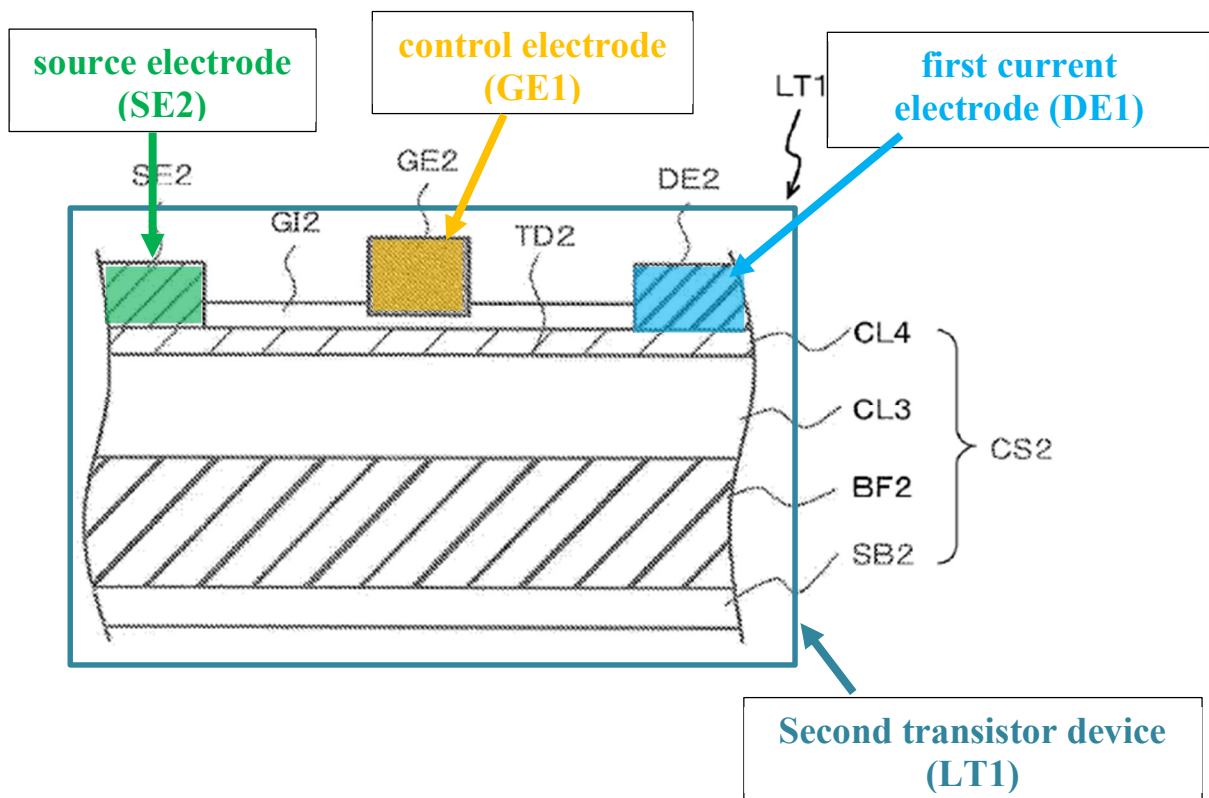
- c. [10b] a second transistor device,

Nega discloses a second transistor device (LT1/LD1).

Nega's transistor LT1 "is formed in a compound semiconductor substrate," Nega, [0073], or is a "silicon device," Nega, [0074]. LT1 is a separate semiconductor chip from HT1—a separate device. Nega, [0093]. LD1 is a low-side switching device constituted by the transistor LT1. Nega, [0091], [0093].

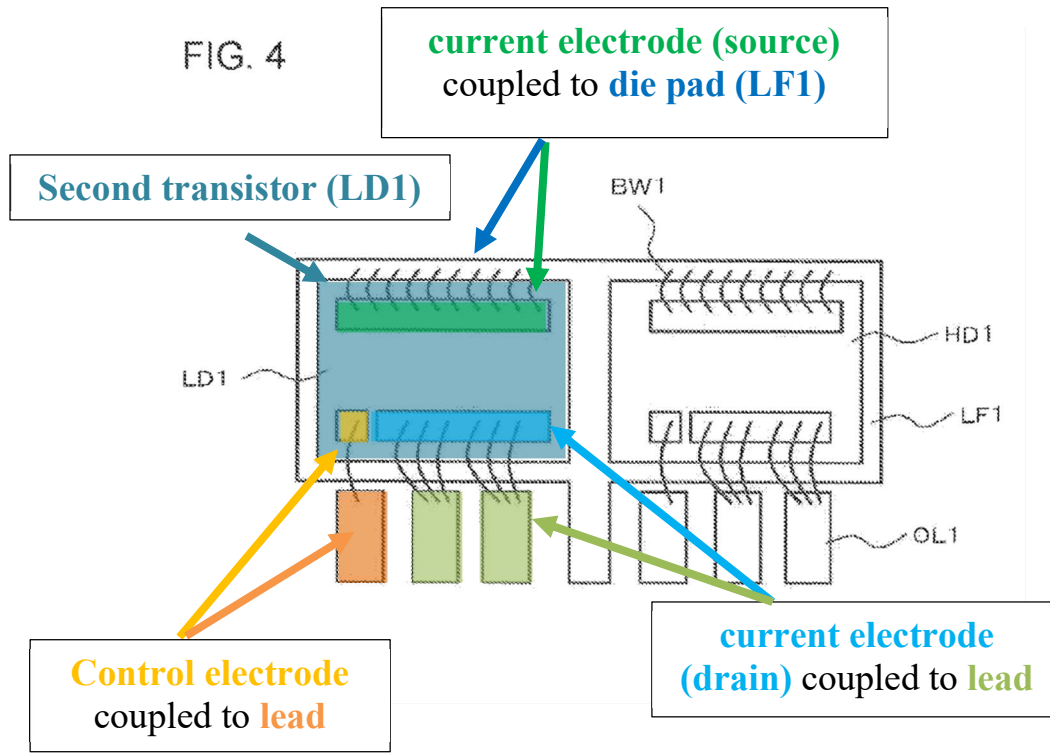
Nega's second transistor device LT1 has a **drain electrode DE2** (Nega, [0080]), a **source electrode SE2** (Nega, [0080]), and a **gate electrode GE2** (Nega, [0079], [0081]). Lebby, [0140]-[0143].

FIG. 3



Nega, Fig. 3 (annotated).

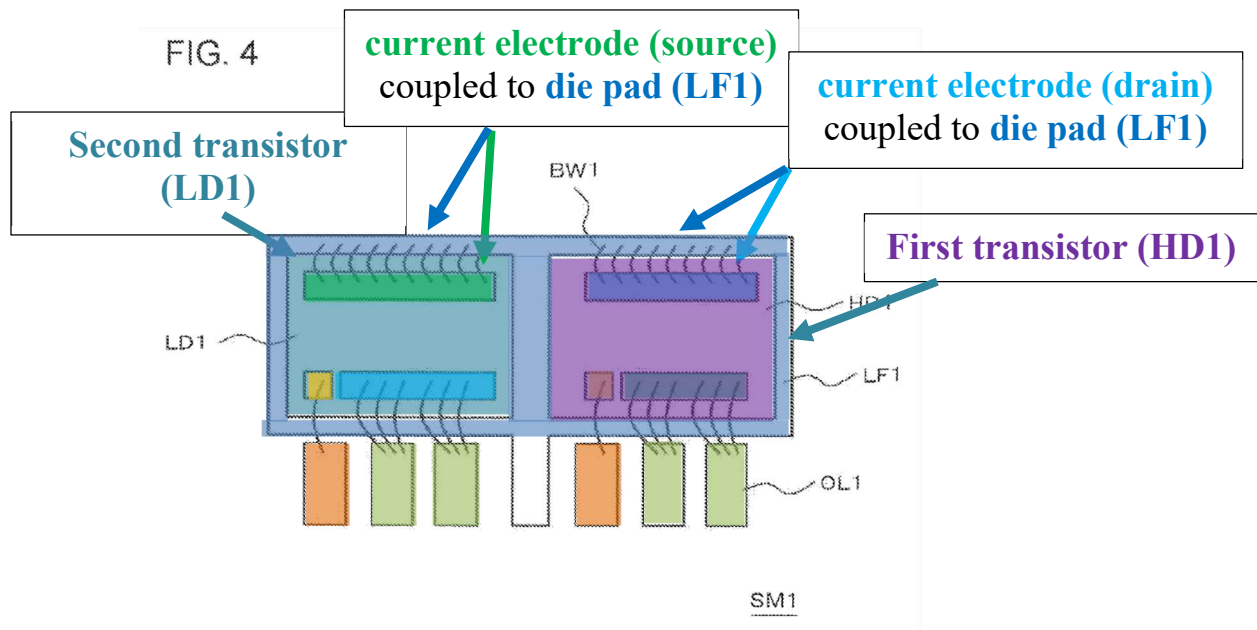
Nega's second transistor device LD1 is on the die pad LF1.



Nega, Fig. 4 (annotated).

- d. [10c] wherein the first transistor device has a current path coupled serially or antiseri-ally with a current path of the second transistor device,

Nega's first transistor device (HD1) has a serially connected current path with its second transistor device (LD1) because, as explained for [10a] and [10b], the drain electrode of Nega's first transistor device (HD1) is coupled to the die pad and the source of Nega's second transistor device (LD1) is connected to the die pad—serially connected. Nega, [0095].



Nega, Fig. 4 (annotated).

Nega discloses that “[i]n the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1,” and “[i]n the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1.” Nega, [0095]. A POSITA would have understood that Figure 4 discloses a serial connection because the drain electrodes of Nega’s first transistor device (HD1) is coupled to the die pad and the source of Nega’s second transistor device (LD1) is connected to the die pad. Lebbby, [0144]-[0145].

- e. **[10d] wherein the first transistor device is a lateral transistor device and a drain or a source of the first transistor device is coupled to the die pad,**

Element [10d] is identical to element [1e]. Nega-Roberts discloses [10d] as explained for [1e]. Lebby, [0146].

- f. **[10e] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.**

Element [10e] is identical to element [1f]. Nega-Roberts discloses [10e] as explained for [1f]. Lebby, [0147].

- 7. **Claim 11 - The switch circuit of claim 10, wherein a drain of the first transistor device and a source of the second transistor device are coupled to a common die pad.**

Nega discloses claim 11.

As explained for element [10c], Nega discloses the drain of the first transistor device and the source of the second transistor device are coupled to the common die pad. A POSITA would have understood that this is the serial connection. Lebby, [0148].



Nega, Fig. 4 (annotated).

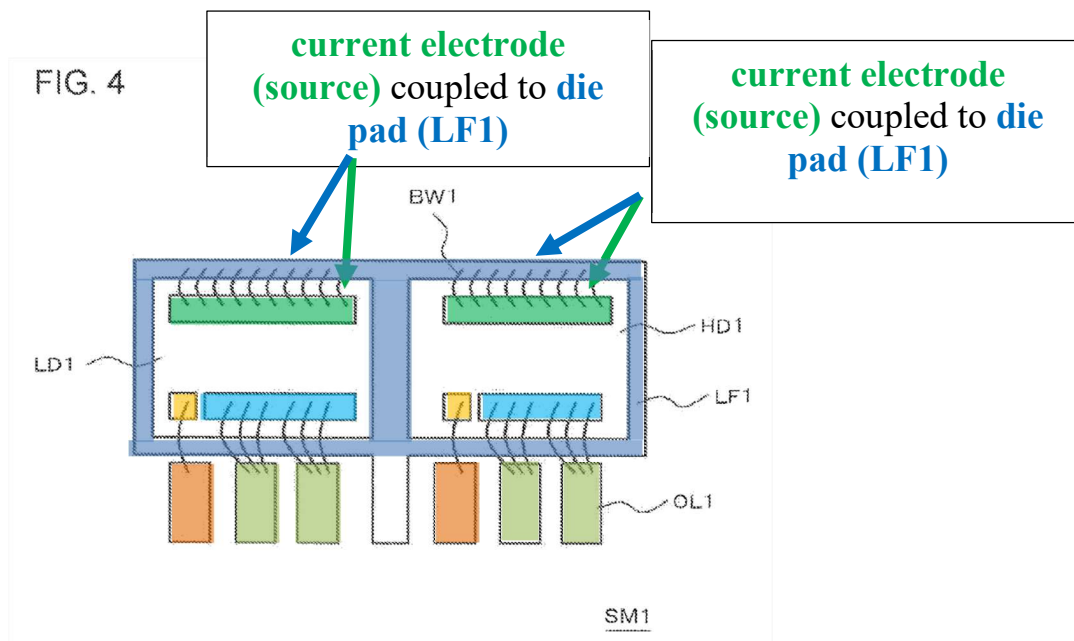
8. Claim 16 – The switch circuit of claim 10, wherein a source of the first transistor device is coupled to a source of the second transistor device.

Nega discloses claim 16 because Nega discloses that the source electrodes for its first transistor devices HD1 and second transistor device LD1 are connected.

Nega, [0095].

The source of Nega's first transistor device SE1 and the source of Nega's second transistor device SE2 are coupled via the outer lead LF1. Nega discloses that "[i]n the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1," and "[i]n the transistor LT1 constituting the low-side switching device LD1, one of the source

electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1.” Nega, [0095]. Lebby, [0149]-[0150]. The ’481 patent discloses that “when an element is referred to as being ‘connected’ or ‘coupled’ to another element, it can be directly connected or coupled to the other element or intervening elements may be present.” ’481 patent, 3:34-37.



Nega, Fig. 4 (annotated).

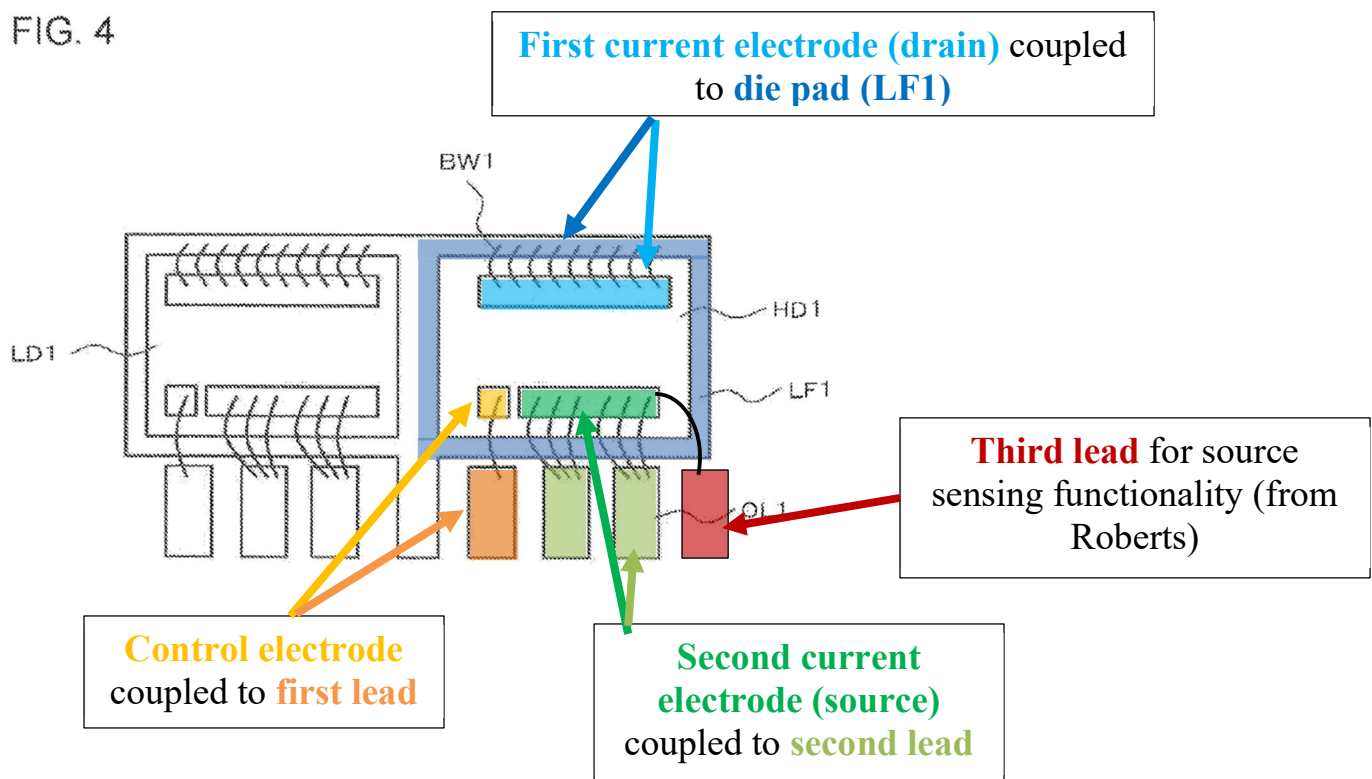
**C. Ground 1B: Nega in View of Roberts and Otremba¹²⁴
Renders Obvious Claims 4, 9, and 17**

1. **Claim 4 - The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.**

Nega in view of Roberts and Otremba¹²⁴ renders claim 4 obvious.

As explained for [1c]-[1e], Nega discloses first and second leads, and Nega-Roberts renders obvious the third lead. Lebbby, [0151]-[0153].

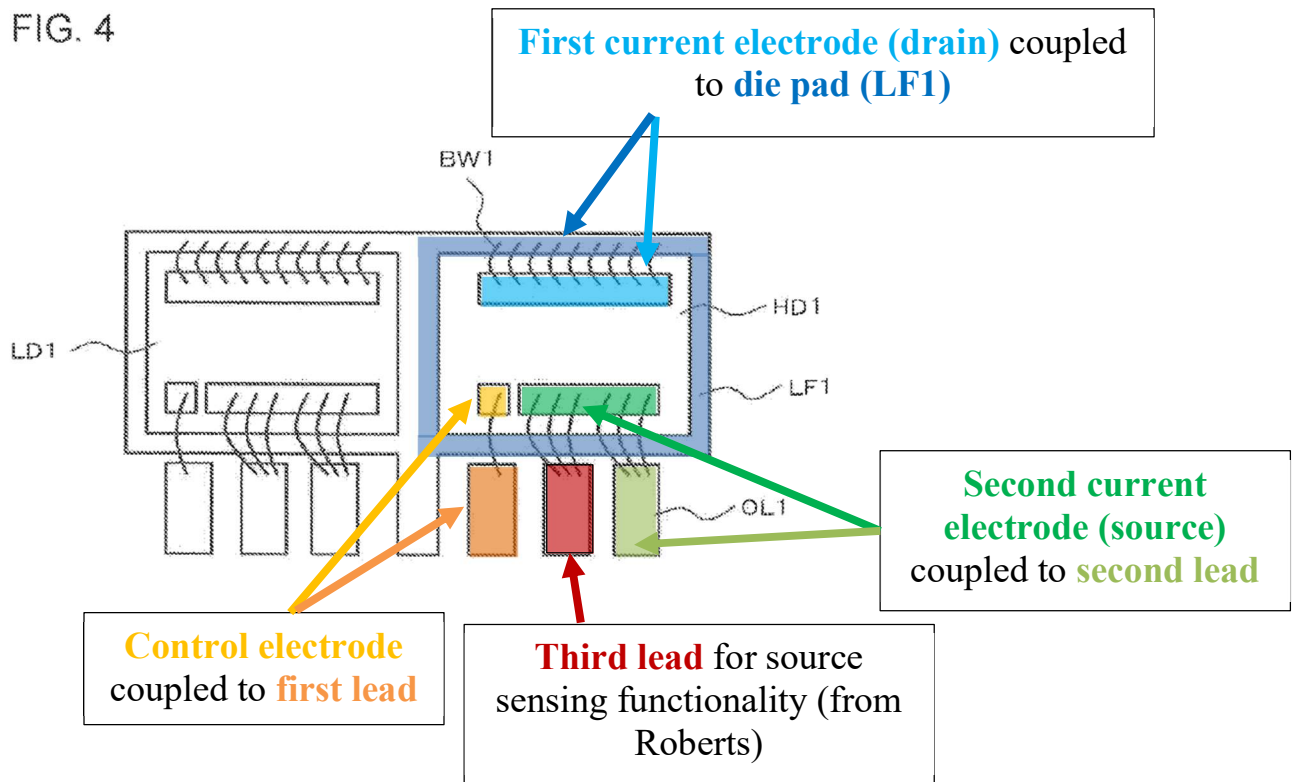
FIG. 4



Id., Fig. 4 (annotated and modified).

Alternatively, repurposing one of Nega's source leads as a source sensing lead:

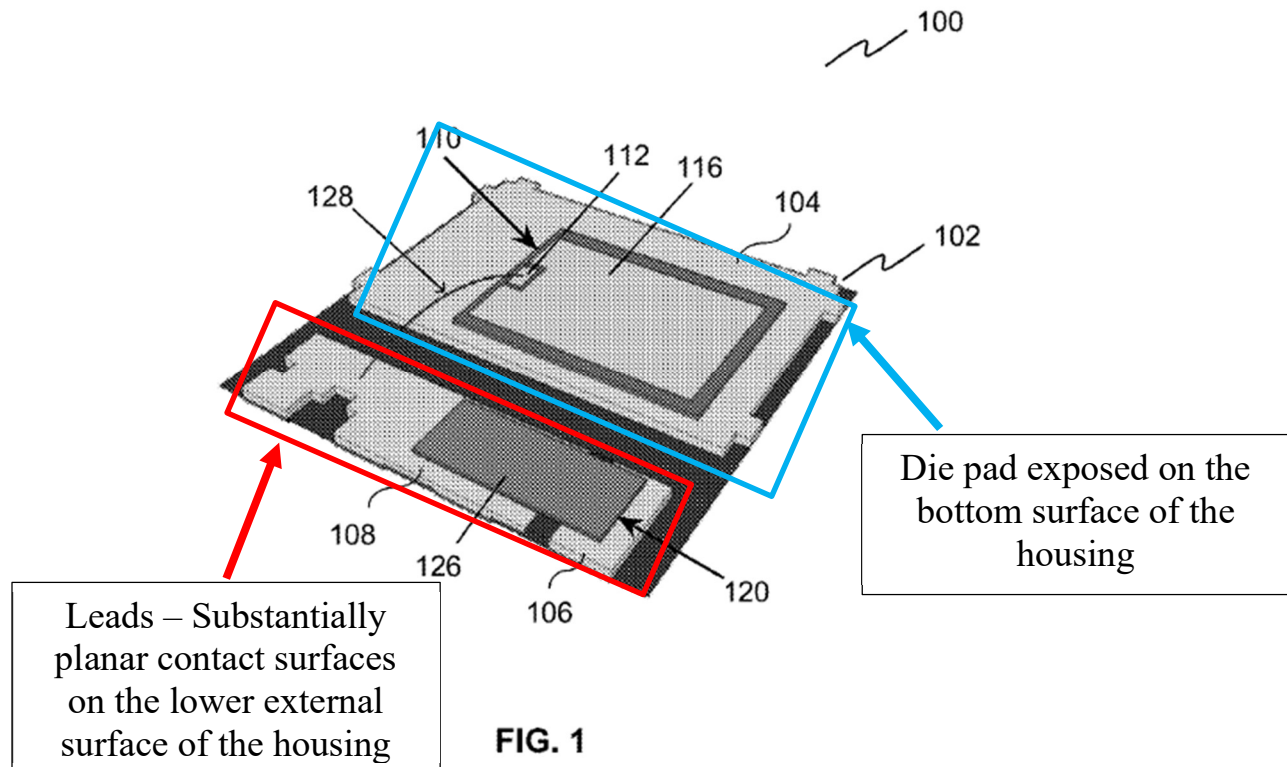
FIG. 4



Id. (annotated).

Nega's transistor is contained within a housing—"the package of TO220." *Id.*, [0063]. Nega, however, does not expressly disclose that its leads and die pad are exposed on the lower surface forming planar contacts—commonly referred to as a leadless package design when coplanar with the lower surface of the housing. Lebbly, [0154]. But this configuration was known in the art, as at least suggested by Otremba124.

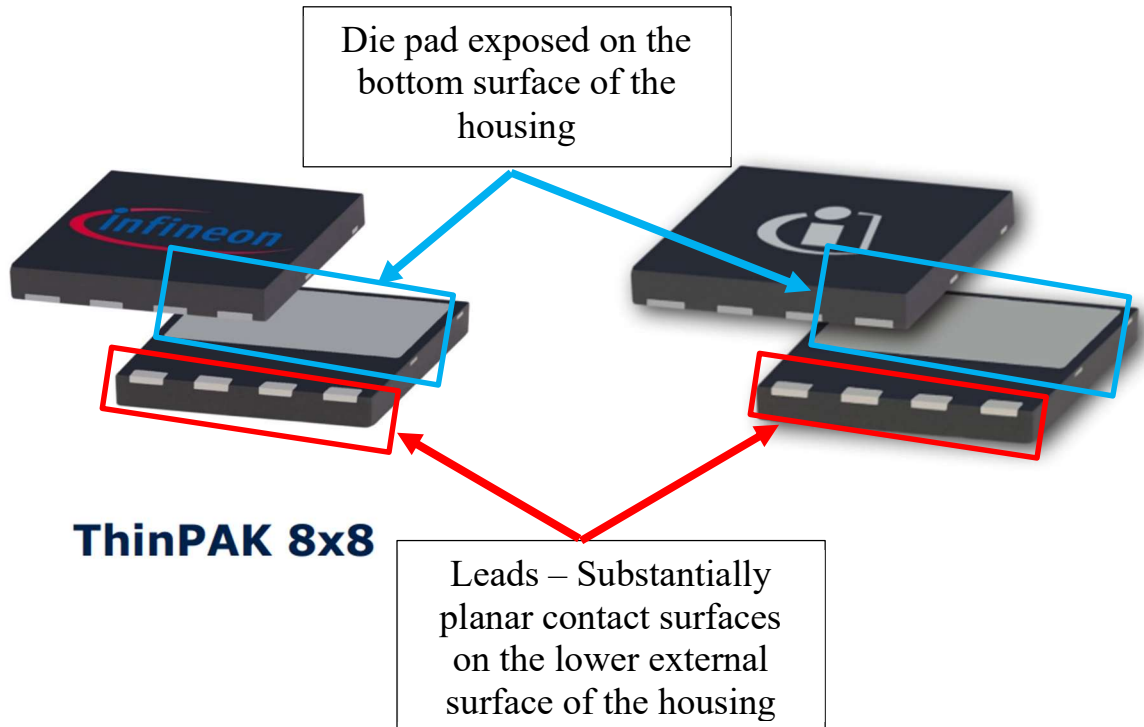
Otremba124 discloses a power transistor including a GaN HEMT “packaged in a[n] 8x8 ThinPAK.” Otremba124, [0041]. Figure 1 shows the ThinPAK8x8 package outline with flat source leads 108 and 106 on the bottom of the package.



Id., Fig. 1 (annotated).

ThinPAK8x8 was a well-known leadless package design, as evidenced by ThinPAK8x8 Brochure and ThinPAK Recommendations, which confirm that ThinPAK8x8 packaging included leads and a die pad exposed on the lower surface and forming planar contacts (a leadless design). Lebby, [0155]-[0156]; ThinPAK8x8

Brochure, 1, 5, 6; ThinPAK Recommendations 1, 4 (“Visible are the 4 small Source/Gate-Pads ... and the big exposed drain pad.”).



ThinPAK8x8 Brochure, 1, 31; ThinPAK Recommendations, 1 (annotated).

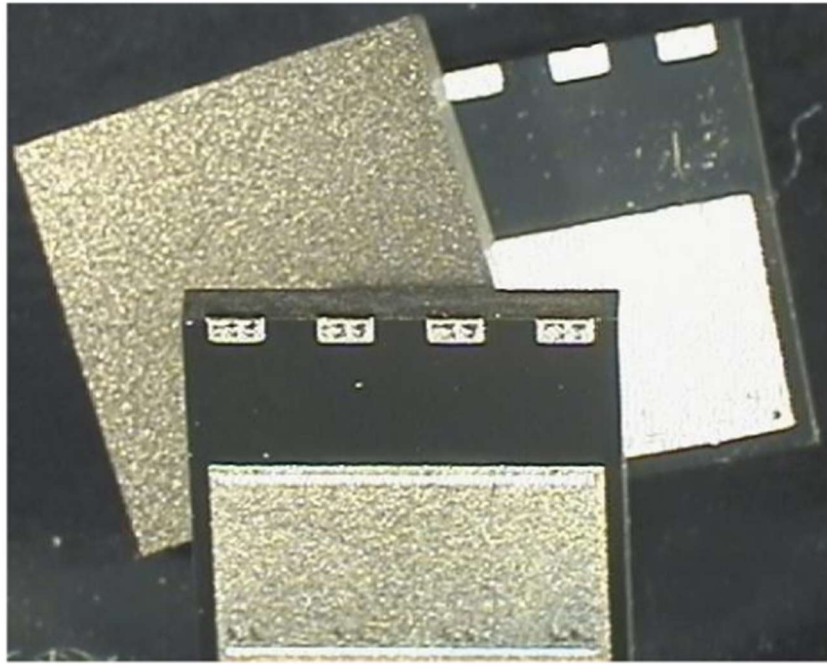


Figure 1: Top and bottom view of VDSO4-4 (ThinPAK 8x8)

ThinPAK Recommendations, 4 (Fig. 1) (annotated).

A POSITA would have been motivated and found it obvious to package Nega's HT1 (HD1) in Otremba124's ThinPAK8x8 package with an exposed die pad and planar lead contacts on the lower surface. As Dr. Lebby explains, "ThinPAK8x8 was boasted as an improvement on other leaded packaging designs, saving space on the printed circuit board (PCB) with a footprint of 64mm² (as opposed to 150mm² for competitive devices)." Lebby, [0157] (citing ThinPAK8x8 Brochure, 3). Dr. Lebby explains that "because ThinPAK8x8 was leadless, it showed faster performance and switching speeds than through-hole and other conventional packages (like the TO220), enabling improved performance, switching behavior, ease of use, EMI (electromagnetic interference), reliability, and higher power

density.” *Id.* Nega recognizes that it implements a standardized TO220 package (a leaded package) as an exemplary package design and would have realized the known benefits ThinPAK8x8 offered as improvements to a device ready for such improvement. Lind shows ThinPAK8x8 with source sensing connections as an alternative to a similar leaded package as would have been obvious to a POSITA (Lebby, [0157]-[0159]):

III. Source-Sense concept and A/B simulation

A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.

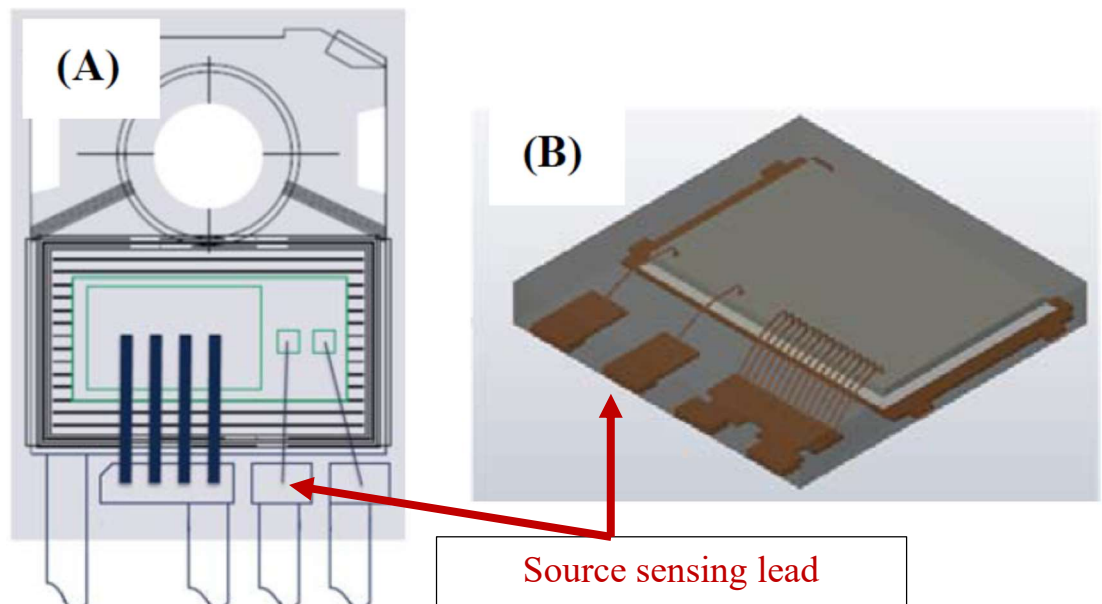


Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections

Lind, 3 (Fig. 4) (annotated).

Packaging Nega-Roberts as a ThinPAK8x8, disclosed by Otremba124, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416. Additional package formats, including leadless, exposed-die packages, were also known as taught by Otremba124 and would have been at least considered suitable options for packaging Nega's compound semiconductor transistor device HT1 (HD1). *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021); *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197-98 (Fed. Cir. 2014). And additional, similar packaging types were known, including those with source sensing leads, like a DFN8x8 package. Lebbby, [0159] (citing Huang, 2, Fig. 2).

2. Claim 9 - The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline.

Claim 9 is of similar scope to claim 4, but claims the ThinPAK8x8 design expressly. Nega in view of Roberts and Otremba124 (expressly disclosing ThinPAK8x8 packaging at [0041]) renders claim 9 obvious as explained for claim 4. Lebbby, [0160].

3. Claim 17

Claim 17 is substantially similar to claims 3 and 4, as incorporating the limitations of claim 1. Nega-Roberts teaches the entirety of claims 1 and 3.

Otremba124 discloses the additional limitation of claim 4. Nega-Roberts-Otremba124 renders obvious claim 17. Leby, [0161].

a. [17p] An electronic component, comprising:

[17p] is identical to [1p]. Nega discloses [17p] as explained for [1p]. Leby, [0162].

b. [17a] a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and

Nega in view of Roberts renders obvious [17a].

As explained for [1a] and claim 2, Nega discloses a Group III nitride-based transistor device.

As explained for claim 3, Nega-Roberts teaches a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

As explained for [1a], Nega discloses a first current electrode, a second current electrode, and a control electrode.

As explained for [1e], Nega-Roberts teaches the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current

electrode is coupled to a second lead, and a third lead is coupled to the transistor device and provides a source sensing functionality. Lebbby, [0163]-[0167].

c. [17b] a housing,

[17b], like claim 4, requires a housing. Nega-Roberts-Otremba124 discloses a housing as explained for claim 4. Lebbby, [0168].

d. [17c] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

[17c] is identical to [1d]. Nega-Roberts teaches [17c] as explained for [1d]. Lebbby, [0169].

e. [17d] wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces,

[17d] is identical to claim 4. Nega-Roberts-Otremba124 teaches [17d] as explained for claim 4. Lebbby, [0170].

f. [17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad,

[17e] is similar to [1f] but claims a Group III nitride-based transistor device rather than a general compound semiconductor device.

As explained for [17a] and claim 2, Nega discloses a Group III nitride-based transistor device.

Nega-Roberts teaches the remainder of [17e] as explained for [1f]. Lebby, [0171]-[0173].

- g. [17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.**

[17f] is identical to [1g]. Nega discloses [17f] as explained for [1g]. Lebby, [0174].

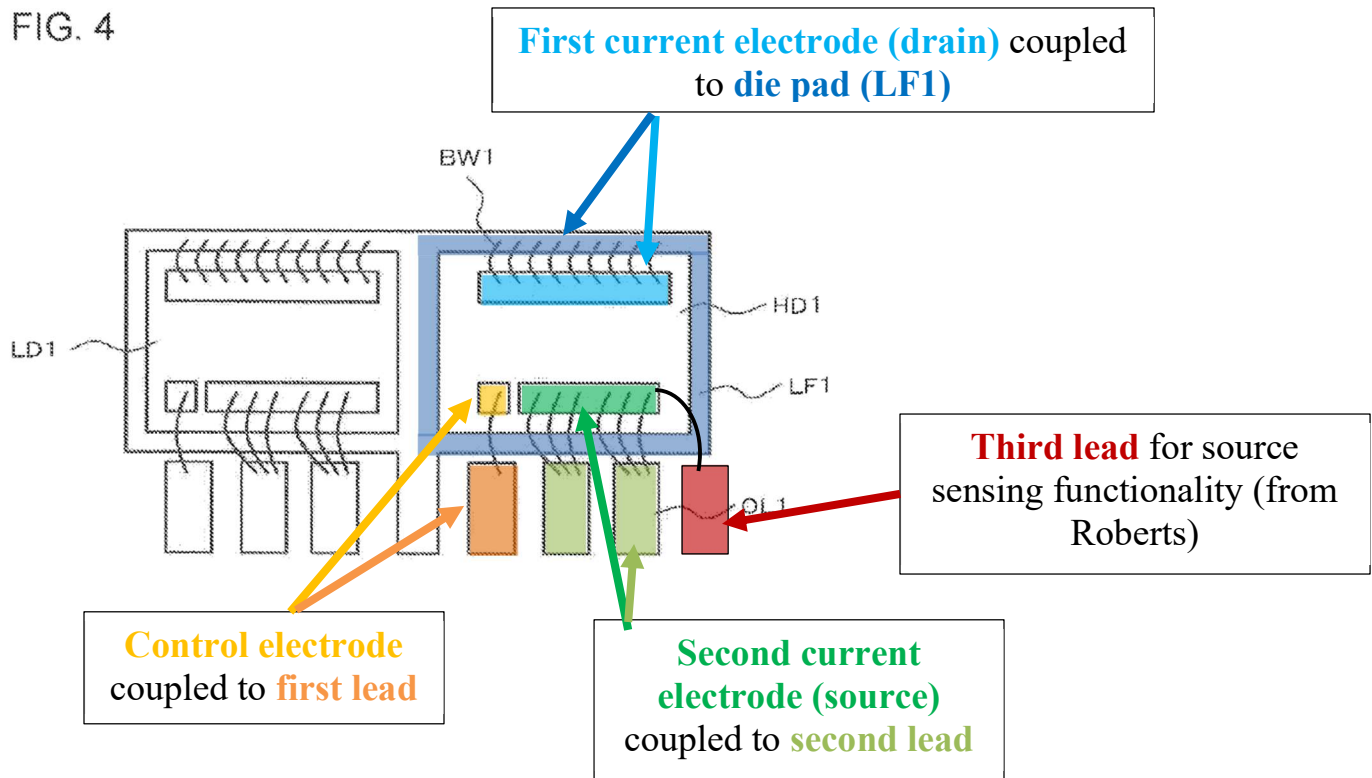
D. Grounds 1C and 1D: Nega in View of Roberts and Otremba433 Renders Obvious Claims 4, 7, 8, and 17 (1C); Nega in View of Roberts, Otremba433, and Otremba280 Renders Obvious Claims 7 and 8

1. Claim 4

Nega in view of Roberts and Otremba433 renders claim 4 obvious.

As explained for [1c]-[1e], Nega discloses first and second leads and Nega-Roberts renders obvious the third lead.

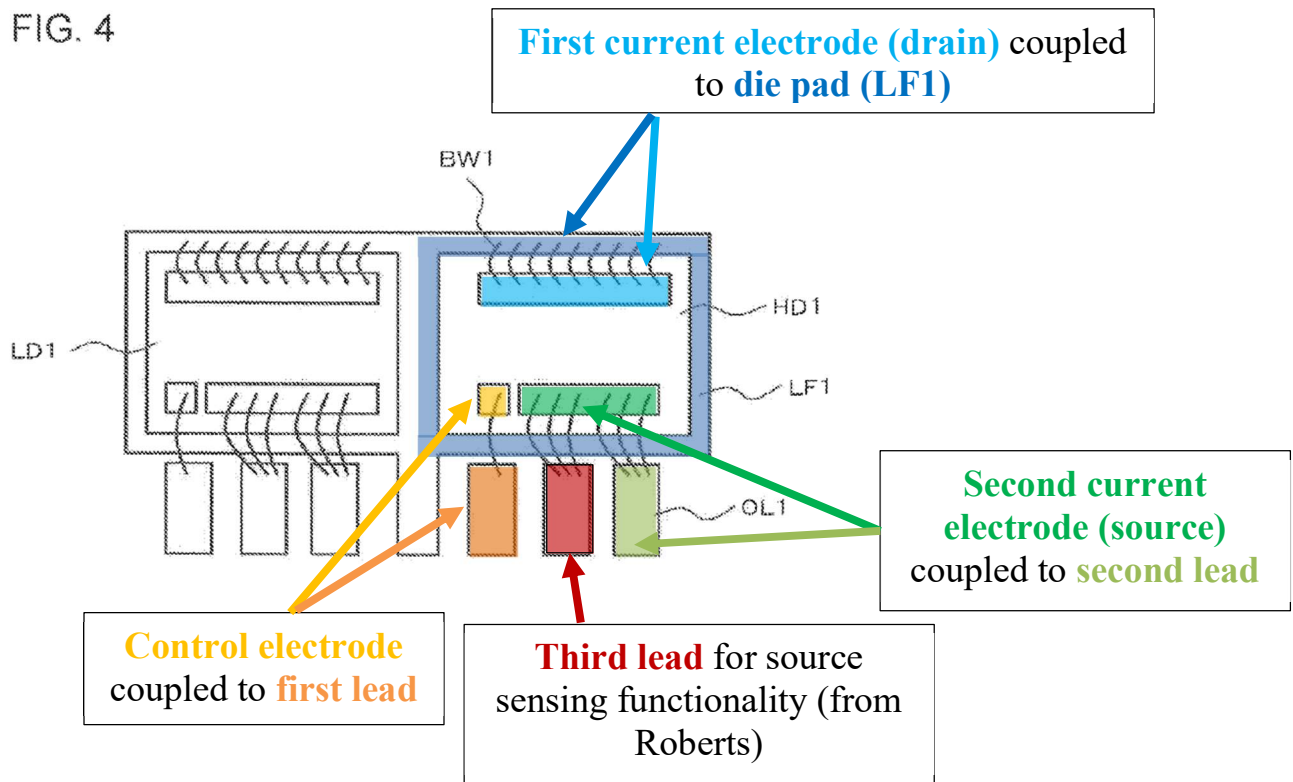
FIG. 4



Nega, Fig. 4 (annotated, modified).

Alternatively, repurposing one of Nega's source leads as a source sensing lead:

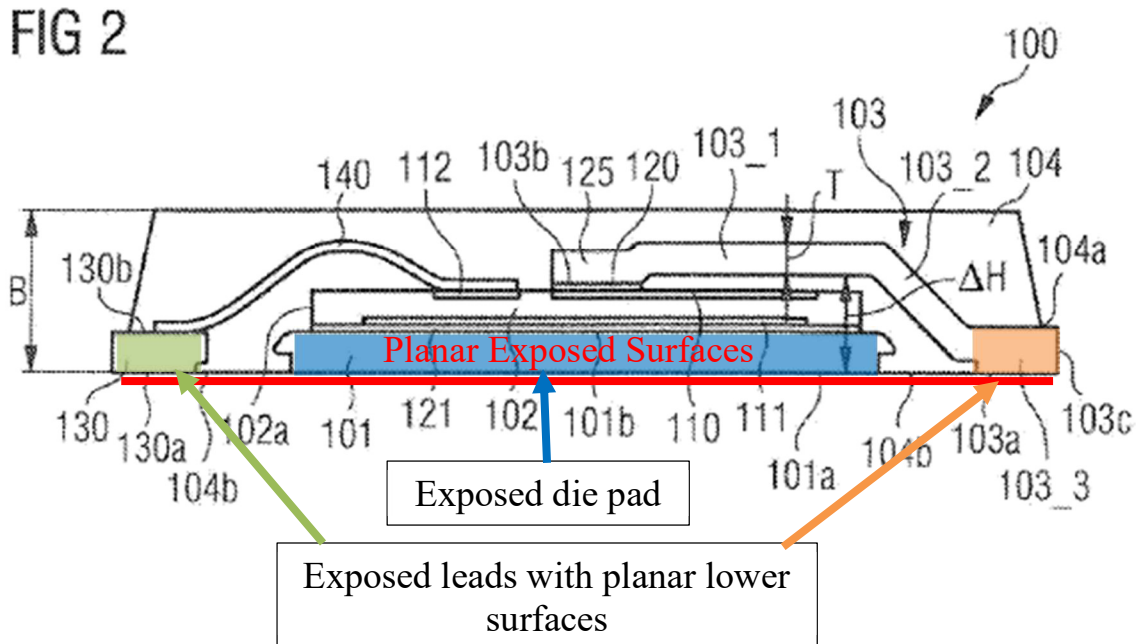
FIG. 4



Id., Fig. 4 (annotated).

As explained for claim 4, Ground 1B, Nega does not expressly disclose that its leads and die pad are exposed on the lower surface forming planar contacts. But this configuration was well known, as at least suggested by Otremba433. Otremba433 discloses a “leadless package” with contacts and die pad exposed on the bottom of the devices (Otremba433, [0037]), explaining that “semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104.” *Id.*, [0027]. Otremba433’s contacts

130 and 103 (leads) have “external contact area[s]” 103a and 130a that are “coplanar with a reference plane defined by a bottom surface 101a of the carrier 101” (die pad) that is “exposed at the bottom of the package.” *Id.*, [0037] (discussing lead 103/103a and carrier 101/101a), [0039] (discussing lead 130/130a); Otremba280, 4:17-29 (“The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a surface mountable or leadless type electronic component.”).



Otremba433, Fig. 2 (annotated).

As explained for claim 4, Ground 1B, a POSITA would have understood Nega's device to be readily implemented in a leadless package (like Otremba433) and would have realized the known benefits of leadless package designs. Packaging

Nega-Roberts as a leadless package, disclosed by Otremba433, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416.

As explained for claim 4, Ground 1B, leadless, exposed-die packages, were known, as taught by Otremba433, and would have been at least suitable options for packaging Nega's device. *Intel*, 21 F.4th at 800; *PAR Pharm.*, 773 F.3d at 1197-98. Otremba433 recognizes that leaded and leadless packages were both possible for packaging semiconductor devices. Otremba433, [0025]; Huang, 2; Lebby, [0175]-[0180].

2. Claim 7 - The electronic component of claim 4, wherein the first current electrode is coupled to the die pad by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

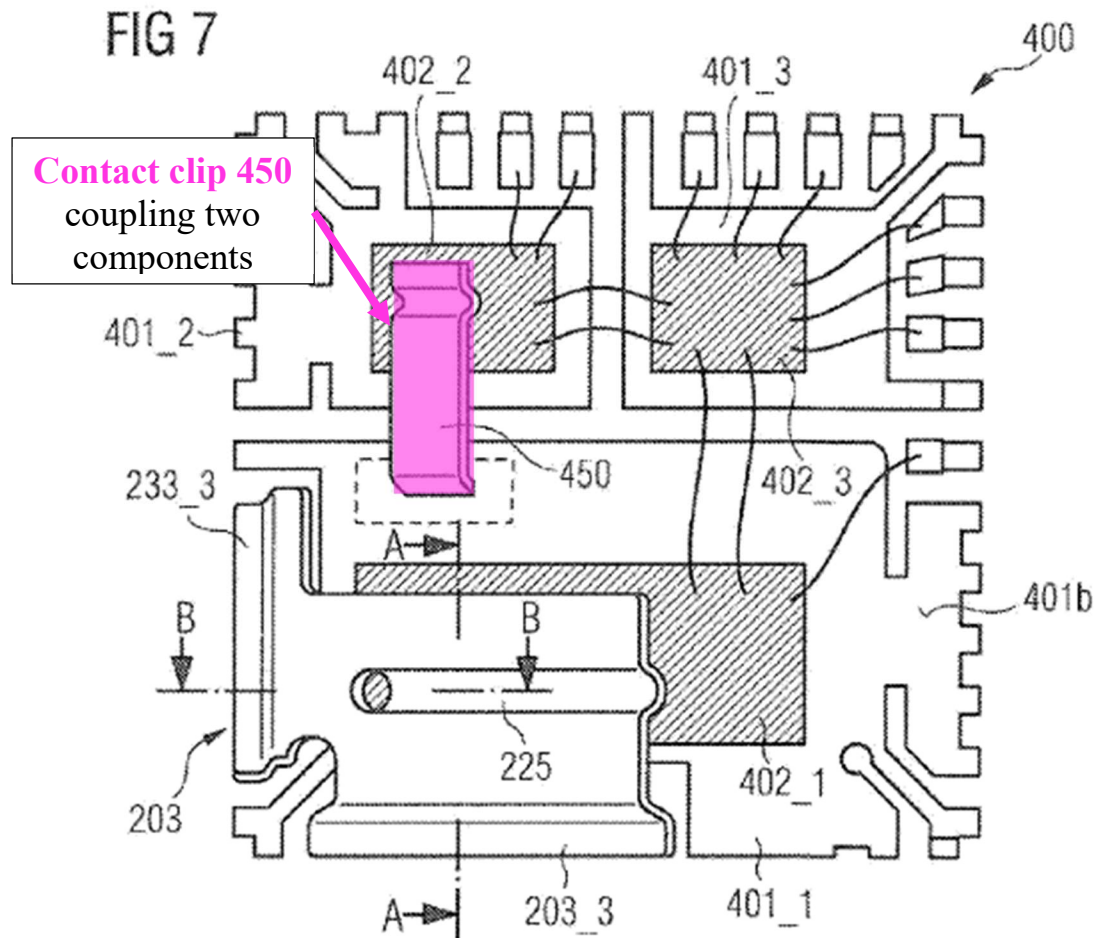
Claim 7 depends from claim 4, but requires a contact clip exposed from the housing forming the connection between the drain electrode (first current electrode) and the die pad (as opposed to bond wires, as allowed for claims 1 and 4).

Nega-Roberts discloses coupling the drain electrode (first current electrode) to the die pad, as explained for [1f]-[1g] but using a plurality of bond wires rather than a contact clip. Bond wires and contact clips were well-known alternatives largely interchangeable but each boasting certain advantages over the other. A POSITA would have understood that contact clips would have been a suitable option

when implementing the Nega-Roberts packaged compound semiconductor transistor device, particularly in devices where there is a desire to reduce parasitic-inductance caused by bond wires. Exposed contact clips provided enhanced thermal performance. Lebbby, [0181]-[0182].

For Ground 1C, Otremba433 discloses coupling components using conventional contact clips. Otremba433 explains: “The source electrode of the high side power semiconductor chip 402_2 is connected to the first carrier 401_1 by a contact clip 4[50]. The contact clip 4[50] may be a conventional contact clip which bridges a level difference.”¹ Otremba433, [0072].

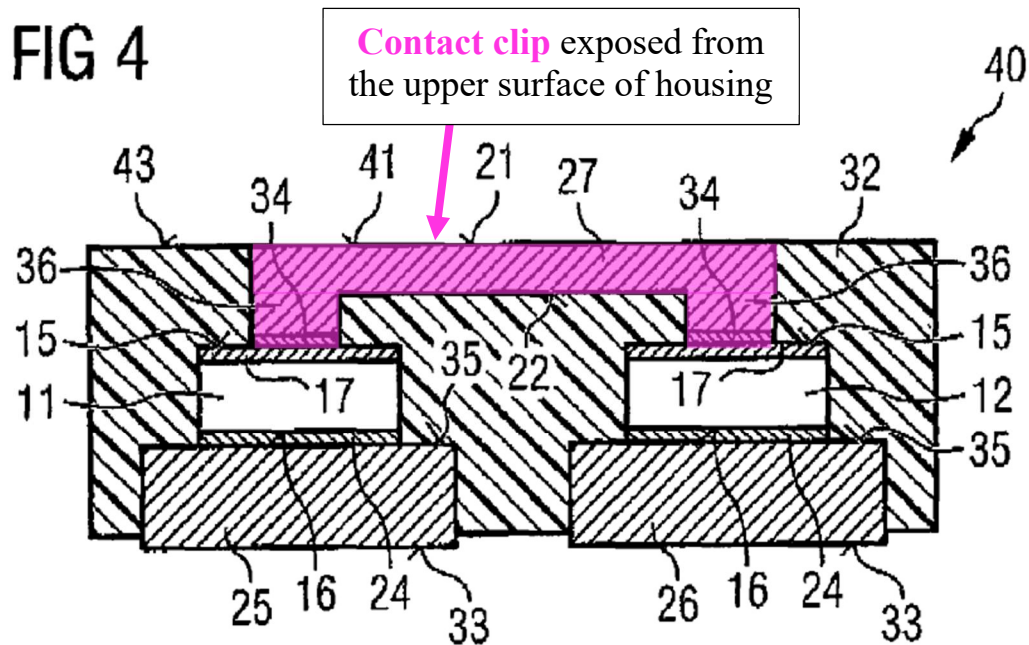
¹ Otremba433 mistakenly refers to contact clip 450 as contact clip 405. Figure 7 has no 405, and the contact clip is correctly referenced a 450 in [0072].



Id., Fig. 7 (annotated).

A POSITA would have understood the known thermal benefits of exposing contact clips from the upper surface of the device housing (like “provid[ing] a shorter path of thermal resistance” between the device “and the environment around the electronic component” (Otremba280, 8:45-57)), and would have readily understood how to implement exposed contact clips, as was known in the art (as explained for Ground 1D, Otremba280), within the Nega-Roberts-Otremba433 device. Lebbby, [0183]-[0184].

For Ground 1D, like Otremba433, Otremba280 discloses using contact clips to couple components. Otremba280's electronic component includes a "contact clip 14 [that] is exposed from the plastic encapsulation compound 32 [(housing)]." *Id.*, 8:33-41, Fig. 4.



Id., Fig. 4 (annotated).

Otremba280 teaches and suggests exposing contact clips from the housing because the "exposed area 41 of the contact clip 14 provides a shorter path of thermal resistance" with "the environment around the electronic component 40." *Id.*, 8:45-48. By exposing the clip, the "thermal performance of the electronic component 40 may be increased due to an improvement in the efficiency of thermal dissipation from the electronic component 40." *Id.*, 8:48-51. To realize thermal benefits, a

POSITA would have been motivated to expose Otremba433's contact clip in Nega-Roberts (Ground 1C) and/or implement Otremba280's exposed contact clip in Nega-Roberts-Otremba433 (Ground 1D) to couple Nega's drain electrode (first current electrode) and LF1 (die pad). Lebbby, [0185]-[0186].

For Grounds 1C and 1D, a POSITA would have been motivated to use a contact clip, as taught by either Otremba433 or Otremba280, to couple Nega-Roberts's first current electrode to the die pad in place of Nega's bond wires to (1) improve current carrying capability; (2) allow for better current spreading to avoid hot spots; (3) reducing on resistance; (4) reducing parasitic induction; and (5) simplifying assembly and manufacturing. Dr. Lebbby explains each of these in detail, summarized below:

First, contact clips have better current carrying capability than bond wires because of their larger surface area connections as opposed to narrow gauge bond wires. Lebbby, [0187]-[0188].

Second, contact clips provide better current spreading across the clip as opposed to narrow gauge bond wires that can cause hotspots from current crowding. Lebbby, [0189].

Third, contact clips reduce device on-resistance ($R_{DS(on)}$) because the contribution of R_{pkg} is lower than bond wire resistance, which usually must be

accounted for in the overall figure, especially when aiming for a total device $RDS(on) \leq 25 \text{ m}\Omega$. Lebbby, [0190].

Fourth, contact clips reduce parasitic inductance because bond wires behave as parasitic inductors that can negatively impact device switching. Contact clips inherently have lower parasitic inductance, enabling higher device switching. Otremba880, from the same time period, explains that “[a]n electronic device comprising a semiconductor chip may exhibit a parasitic source- or emitter-inductance and a parasitic drain- or collector-inductance,” and “[r]educing a parasitic inductance may improve an efficiency of the electronic device.” Otremba880, 1:11-18. To resolve parasitic impendence, a POSITA would have understood using contact clips to connect components—not bond wires that can incur parasitic inductance. Lebbby, [0191].

Fifth, contact clips are simple to handle in assembly and packaging for back-end manufacturing because they can be easily loaded into automatic tools for high yielding, high volume assembly, which lowers costs. Lebbby, [0192].

Bond wires and contact clips were known alternative coupling components. Otremba441 discloses that commonly known coupling structures within transistor devices include any of “a clip, a ribbon, a wire, a plate, or a conductor track,” so long as the resistance is below a certain threshold. Otremba441, 2:59-65, 6:34-43; Otremba124, [0027], [0057]. A POSITA would have understood that bond wires and

contact clips were ubiquitous coupling means, each suited to different design preferences and needs, and at least constituting suitable options. *Intel*, 21 F.4th at 800; *PAR Pharm.*, 773 F.3d at 1197-98; *Lebby*, [0193].

3. Claim 8 - The electronic component of claim 4, wherein the second current electrode is coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

As explained for claim 7, implementing an exposed contact clip to couple components in Nega-Roberts would have been obvious. Coupling Nega's second current electrode to the second lead with Otremba433's (Ground 1C) and/or Otremba280's (Ground 1D) contact clip would have been obvious for the same reason coupling Nega's first current electrode to the die pad would have been obvious, as explained for claim 7. *Lebby*, [0194].

4. Claim 17

a. [17p]

Nega discloses [17p] as explained for [1p]. *Lebby*, [0195]-[0196].

b. [17a]

Nega in view of Roberts renders obvious [17a].

As explained for [1a] and claim 2, Nega discloses a Group III nitride-based transistor device.

As explained for claim 3, Nega-Roberts teaches a blocking voltage capability of at least 100 kHz, a first current electrode, a second current electrode, and a control electrode.

As explained for [1a], Nega discloses a first current electrode, a second current electrode, and a control electrode.

As explained for [1e], Nega-Roberts teaches the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead, and a third lead is coupled to the transistor device and provides a source sensing functionality. Lebbby, [0197]-[0201].

c. [17b]

Nega-Roberts-Otremba433 discloses a housing as explained for claim 4. Lebbby, [0202].

d. [17c]

Nega-Roberts teaches [17c] as explained for [1d]. Lebbby, [0203].

e. [17d]

[Nega-Roberts-Otremba124 teaches [17d] as explained for claim 4. Lebbby, [0204].

f. [17e]

As explained for [17a] and claim 2, Nega discloses a Group III nitride-based transistor device.

Nega-Roberts teaches the remainder of [17e] as explained for [1f]. Lebby, [0205]-[0207].

g. [17f]

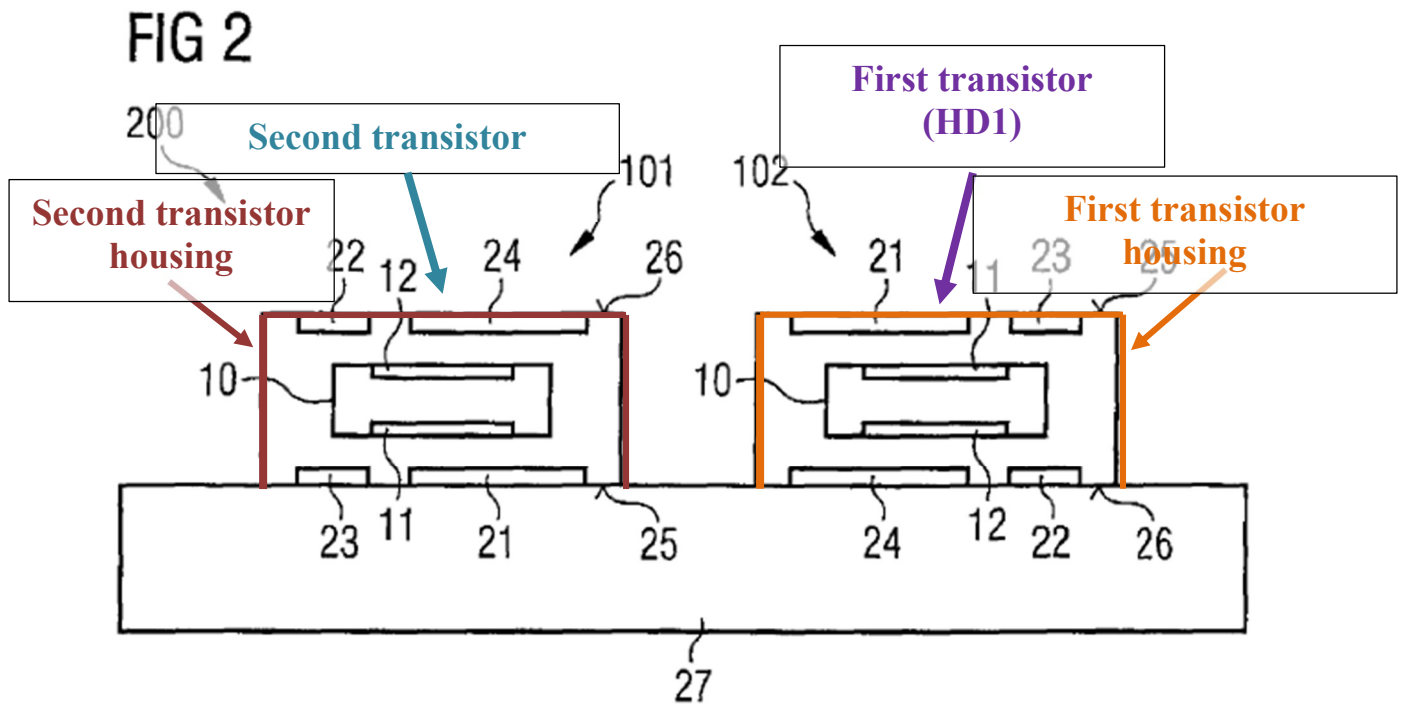
Nega discloses [17f] as explained for [1g]. Lebby, [0208].

E. Ground 1E: Nega in view of Roberts and Otremba631 Renders Claims 12 and 13 Obvious

- 1. Claim 12 - The switch circuit of claim 10, wherein the first transistor device is housed in a package comprising a first die pad coupled to a drain of the first transistor device and the second transistor device is housed in a package comprising a second die pad coupled to a source of the second transistor device.**

Claim 12 differs from claim 1 by requiring two separately packaged transistors. As explained for claim 10, Nega-Roberts discloses a single package containing two transistors. Otremba631 discloses separately packaging each transistor.

Otremba631 discloses packaging two transistors in separate housings and mounting surfaces coupled to a common circuit board. Otremba631, Fig. 2. Otremba631's "first device 101 is mounted on the circuit board 27 with its first mounting surface 25 facing the circuit board 27. The second device 102 is mounted on the circuit board 27 with its second mounting surface 26 facing the circuit board 27." Otremba631, 4:64-67.



Otremba631, Fig. 2 (annotated).

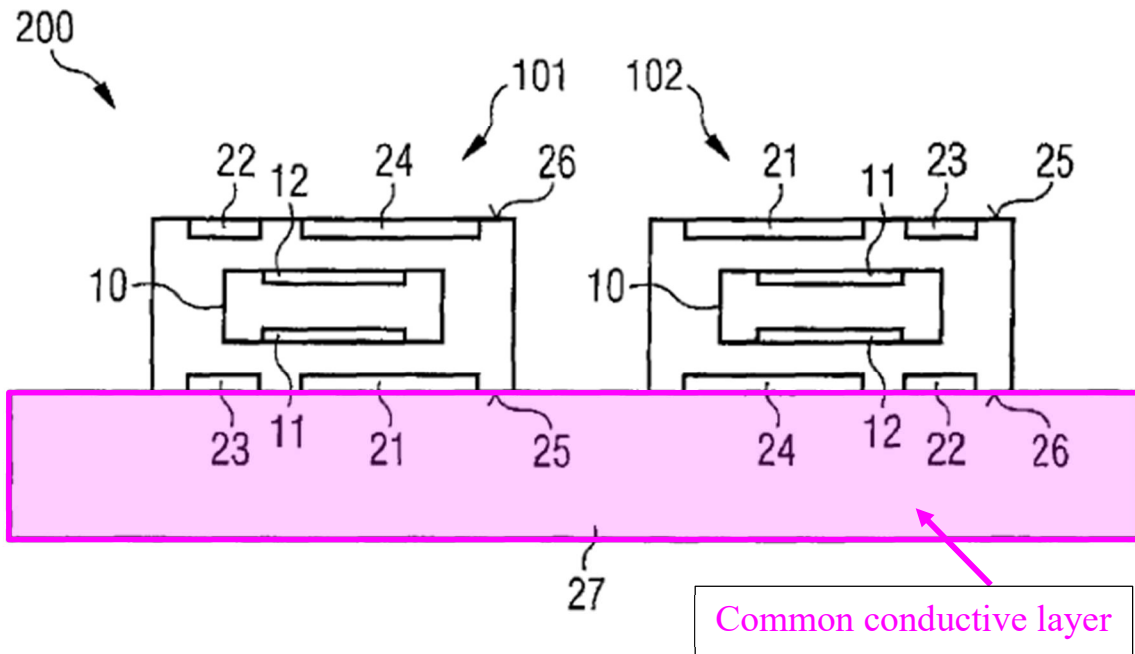
A POSITA would have been motivated to house each of Nega’s transistors separately, connected to a common circuit board, like in Otremba631 because packaging two transistors in a single package and packaging each transistor separately were known alternatives of one another—each achieving the same result, a dual-transistor switch circuit. Lebby, [0209]-[0212]. As Dr. Lebby explains, “[e]ach alternative was suited to different design preferences and application needs,” both at least constituting suitable options for achieving the desired switch circuit. *Id.*, [0211] (explaining the thermal benefits of housing two transistors separately); *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021); *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014)).

A POSITA would have had an expectation of success implementing Nega-Roberts's device as separately packaged transistors because it would have been a simple substitution of one known packaging configuration for another—with the electronic characteristics of the overall circuit maintained—applying only conventional manufacturing processes and techniques. Leiby, [0213].

2. Claim 13 – The switch circuit of claim 12, wherein the first die pad and the second die pad are mounted on a common conductive layer.

As explained for claim 12, Otremba631 discloses two transistor devices mounted on a common conductive layer, **circuit board 27**. Otremba631, 4:64-67, Fig. 2. Otremba631's "first device 101 is mounted on the circuit board 27 with its first mounting surface 25 facing the circuit board 27. The second device 102 is mounted on the circuit board 27 with its second mounting surface 26 facing the circuit board 27." Otremba631, 4:64-67.

FIG 2



Otremba631, Fig. 2 (annotated).

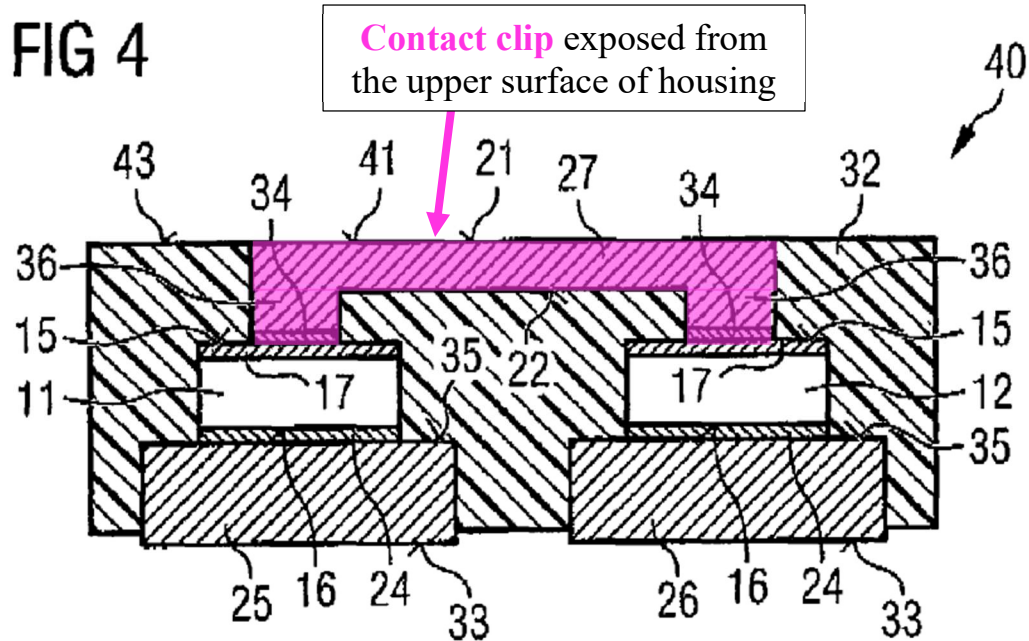
A POSITA would have been motivated to house Nega's transistors separately and connect them to a common board, as disclosed in Otremba631 as explained for claim 12. Lebbby, [0214]-[0215].

F. Ground 1F: Nega in view of Roberts and Otremba280 Renders Claims 14 and 15 Obvious

- 1. Claim 14 – The switch circuit of claim 10, wherein a first contact clip is coupled to one of a source and a drain of the first transistor device and a second contact clip is coupled to the other one of a source and a drain of the second transistor device, wherein the first contact clip and the second contact clip are at least partially uncovered.**

As explained for Ground 1A [10c], Nega’s first transistor device and second transistor devices are coupled serially. Nega teaches coupling the components using bond wires, but Otremba280 teaches that contact clips were commonly known alternatives and exposing the contact clips provided known benefits.

Otremba280 discloses using contact clips to couple components, stating that its device includes “a contact clip 14 [that] is exposed from the plastic encapsulation compound 32 [(housing)].” Otremba280, 8:33-41, Fig. 4.



Otremba280, Fig. 4 (annotated).

As explained for claim 7, Grounds 1B and 1D, a POSITA would have been motivated to use a contact clip, as taught by Otremba280, to couple Nega-Roberts's transistor devices.

Using an exposed contact clip was taught by Otremba280, which discloses exposing the contact clip from the housing because the “exposed area 41 of the contact clip 14 provides a shorter path of thermal resistance” with “the environment around the electronic component 40.” Otremba280, 8:45-51. To realize thermal benefits, a POSITA would have been motivated to implement Otremba280's exposed contact clip in Nega-Roberts to couple Nega's first transistor device's drain

electrode (first current electrode) and LF1 (die pad) and Nega's second transistor device's source electrode and LF1. Lebbby, [0216]-[0219].

2. Claim 15 – The switch circuit of claim 14, wherein the first contact clip and the second contact clip are coupled to a common heat dissipation member.

Otremba280 also discloses claim 15 because Otremba280 disclose a heatsink coupled to the contact clip.

Otremba280 discloses that “[a]n additional heat sink or cooling element may be positioned on the upper surface 42 of the electronic component 40. In an embodiment, an additional heat sink may be positioned directly on the exposed regions 41 of the contact clip 14. The additional heat sink may be in electrical connection with the contact clip 14 if the contact clip 14 is connected to ground potential.” Otremba280, 8:51-57. A POSITA would have understood that Otremba280's use of a heat sink is the same as what is disclosed by the '481 patent because both disclosures relate to placing a heat sink on the exposed region of the clip. The '481 patent states that “The exposed region of the contact clip may be used as cooling surface on to which an additional heat dissipation device such as a heat sink may be mounted.” Ex-1001, 6:66-7:2.

A POSITA would have been motivated to include Otremba280's heat sink in Nega-Roberts switch circuit because Otremba280 expressly teaches and suggests improving the efficiency of thermal dissipation from the electronic component.

Otremba280, 8:48-51. By adding a heat sink, the “thermal performance of the electronic component 40 may be increased due to an improvement in the efficiency of thermal dissipation from the electronic component 40.” Otremba280, 8:47-51. To realize the thermal benefits, a POSITA would have been motivated to implement Otremba280’s heat sink in Nega-Roberts. A POSTA would have understood adding heat sinks to a contact clip was a routine way to dissipate thermal energy from an electronic component. Lebbby, [0220]-[0222].

A POSITA would have had an expectation of success in implementing Otremba280’s heat sinks onto its contact clip and Nega-Robert’s switch circuit because it would have been a simple addition of a known component and would have needed to apply only conventional techniques. Lebbby, [0223].

VI. LIU GROUNDS 2A-2F (CLAIMS 1-9 AND 17)

A. Liu Is Prior Art Based On Its Provisional Application

Liu claims priority to U.S. Provisional Application No. 62/196,629 (“Provisional”), filed July 24, 2015. Because the subject matter of Liu Petitioner relies on is supported by the Provisional, Liu was effectively filed under 35 U.S.C. §102(d)(2) “as of the filing date of the earliest such application that describes the subject matter”—July 24, 2015. *Penumbra, Inc. v. RapidPulse, Inc.*, IPR2021-01466, Paper 34, 29-35 (PTAB Mar. 10, 2023) (precedential). Although not required under *Penumbra*, a representative claim of Liu is supported by the Provisional. *Id.*;

Dynamic Drinkware, LLC v. Nat’l Graphics, Inc., 800 F.3d 1375 (Fed. Cir. 2015); Lebbby, [0224]-[0225].

1. Cited Disclosures of Liu Are Supported in the Provisional

Liu and its Provisional are nearly identical. Every figure of Liu appears in the Provisional, and all Liu’s cited disclosures are identical or nearly identical to its Provisional.² Petitioner additionally cites both Liu and the Provisional throughout. Lebbby, [0226]-[0227].

Relied-Upon Liu Subject Matter	Provisional Support
8:11-26: “A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with	[00042]: “A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance

² The Figures of both Liu and its Provisional have only minor variations in numbers (e.g., 42I in Liu Figure 11 corresponds to 42 in Provisional Figure 11, 42I in Liu Figure 12 corresponds to 56 in Provisional Figure 12, and 90 in Liu Figure 12 corresponds to 133 in Provisional Figure 12).

an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.”	with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact 54B formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.”
8:27-44: “Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of	[00043]: “Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact 54B of semiconductor

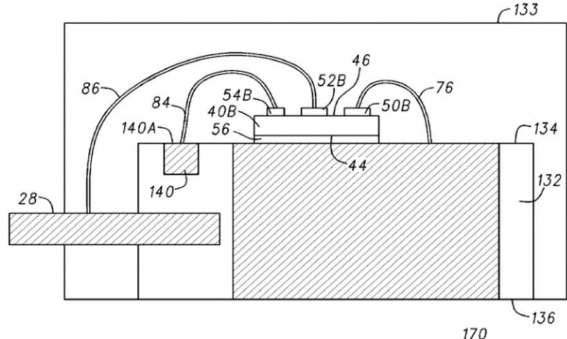
semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment[,], drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.”	device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment[,], drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.”
3:55-58: “[S]emiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride.”	[00021]: “[S]emiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride.”

4:60-5:3: “FIG. 4 is a perspective view of a semiconductor component 100 in accordance with another embodiment of the present invention. Semiconductor component 100 is similar to semiconductor component 10 except that bond wires 76 have been replaced by an electrically conductive clip 102, bond wires 78 have been replaced by an electrically conductive clip 104, and bond wires 88 have been replaced by an electrically conductive clip 106. It should be noted that mounting semiconductor chips 40 and 60 to device receiving areas 18 and 20, respectively, have been described with reference to FIGS. 1 and 2.”	[00027]: “FIG. 4 is a perspective view of a semiconductor component 100 in accordance with another embodiment of the present invention. Semiconductor component 100 is similar to semiconductor component 10 except that bond wires 76 have been replaced by an electrically conductive clip 102, bond wires 78 have been replaced by an electrically conductive clip 104, and bond wires 88 have been replaced by an electrically conductive clip 106. It should be noted that mounting semiconductor chips 40 and 60 to device receiving areas 18 and 20, respectively, have been described with reference to FIGs. 1 and 2.”
7:33-38: “As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40A and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 106, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example[,] mold compound 90.”	[00038]: “As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40A and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 106, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example[,] a mold compound.”

2. Liu Claim 1 Is Supported in the Provisional

The Provisional supports Liu's claim 1:

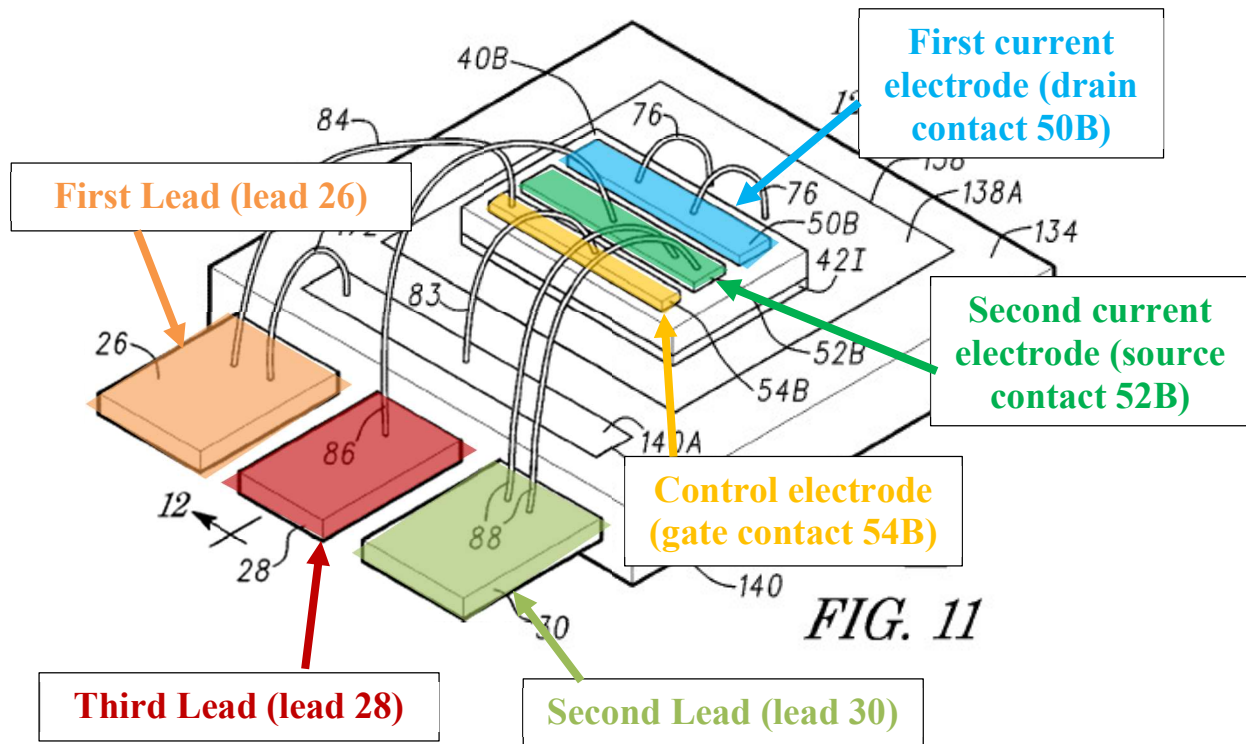
Liu Claim 1	Provisional Support
"1. A semiconductor component comprising:"	Claim 1: "A semiconductor component having at least first and second terminals, comprising:"
"a molded support structure having a top surface and a bottom surface, the molded support structure including:"	[00020]: "a molded device support structure 12 having a top surface 14 and a bottom surface 16."
"a device receiving structure embedded in a first portion of the molded support structure, the device receiving structure extending from the top surface into the molded support structure;"	[00020]: "Molded support structure 12 includes a device receiving area 18 ... and a bond pad 22 at top surface 14 and a contact 24 at bottom surface 16." [00020]: "Device receiving areas 18 and 20 may be referred to as device receiving structures." Fig. 12: FIG. 12

“a first bond pad embedded in a second portion of the molded support structure;”	[00020]: “[M]olded support structure 12 includes ... a bond pad 22 at top surface 14”
“a first leadframe lead extending from a third portion of the molded support structure, the first leadframe lead vertically positioned between the first bond pad and the bottom surface;” “a second leadframe lead extending from a fourth portion of the molded support structure, the second leadframe lead vertically positioned between the first bond pad and the bottom surface;”	[00020]: “Leadframe leads 26, 28, and 30 protrude from a side or an edge of molded device support structure 12.” Fig. 12:  FIG. 12
“a semiconductor device bonded to the device receiving structure, the semiconductor device having a control electrode, a first current carrying electrode, and a second current carrying electrode;”	Claim 1: “a first semiconductor device mounted to the first receiving structure, the first semiconductor device having a control terminal and first and second current carrying terminals and configured from a III-N semiconductor material;”
“a first electrical interconnect coupling the first leadframe lead to the first current carrying electrode of the semiconductor device;”	Claim 1: “a first electrical interconnect coupled between the control terminal of the first semiconductor device and a first lead of the plurality of leads;”

“a second electrical interconnect coupling the second leadframe lead to the control electrode of the semiconductor device;”	Claim 1: “a second electrical interconnect coupled between the first current carrying terminal of the first semiconductor device and a second lead of the plurality of leads; and”
“a third electrical interconnect coupling the second current carrying electrode to the device receiving structure;”	Claim 1: “a third electrical interconnect coupled between the second current carrying terminal of the first semiconductor device and one of the first device receiving structure or the first interconnect structure.”
“a fourth electrical interconnect coupling a third leadframe lead to the first current carrying electrode of the semiconductor device; and”	Claim 4: “The semiconductor component of claim 1, further including a fourth electrical interconnect coupled between the first current carrying terminal of the first semiconductor device and a third lead of the plurality of leads.”
“a protection material over the semiconductor device, the first electrical interconnect, and the second electrical interconnect, and over at least a portion of the molded support structure.”	[00028]: “[D]evice receiving areas 18 and 20, semiconductor chips 40 and 60, ... and portions of molded support structure 12 may be encapsulated in a protection material”

B. Overview of the Combinations

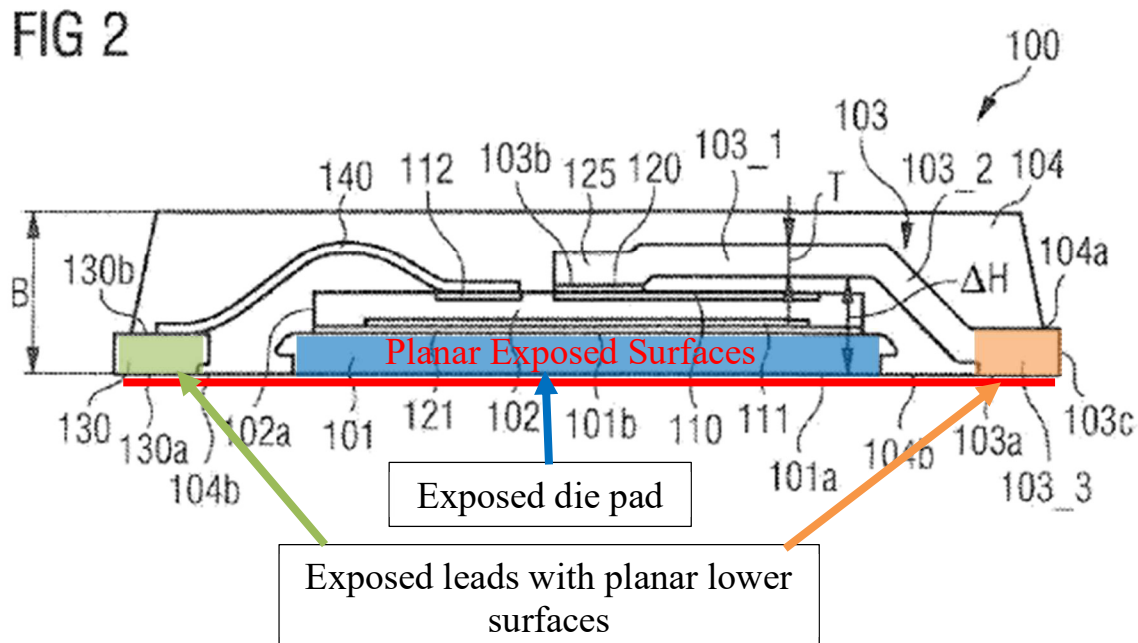
Liu discloses claims 1, 2, and 4-6. Liu discloses a semiconductor device with **gate contact 54B (control electrode)** coupled to a leadframe **lead 26 (first lead)**, **drain contact 50B (first current electrode)** coupled to the **device receiving area 138 (die pad)**, and **source contact 52B (second current electrode)** coupled to the leadframe **lead 30 (second lead)**. Liu, 8:27-40; Provisional, [00043]. Liu discloses **lead 28 (third lead)** connected to “source contact 52B of semiconductor device 40B” that “is a Kelvin leadframe lead or a Kelvin lead.” *Id.*



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

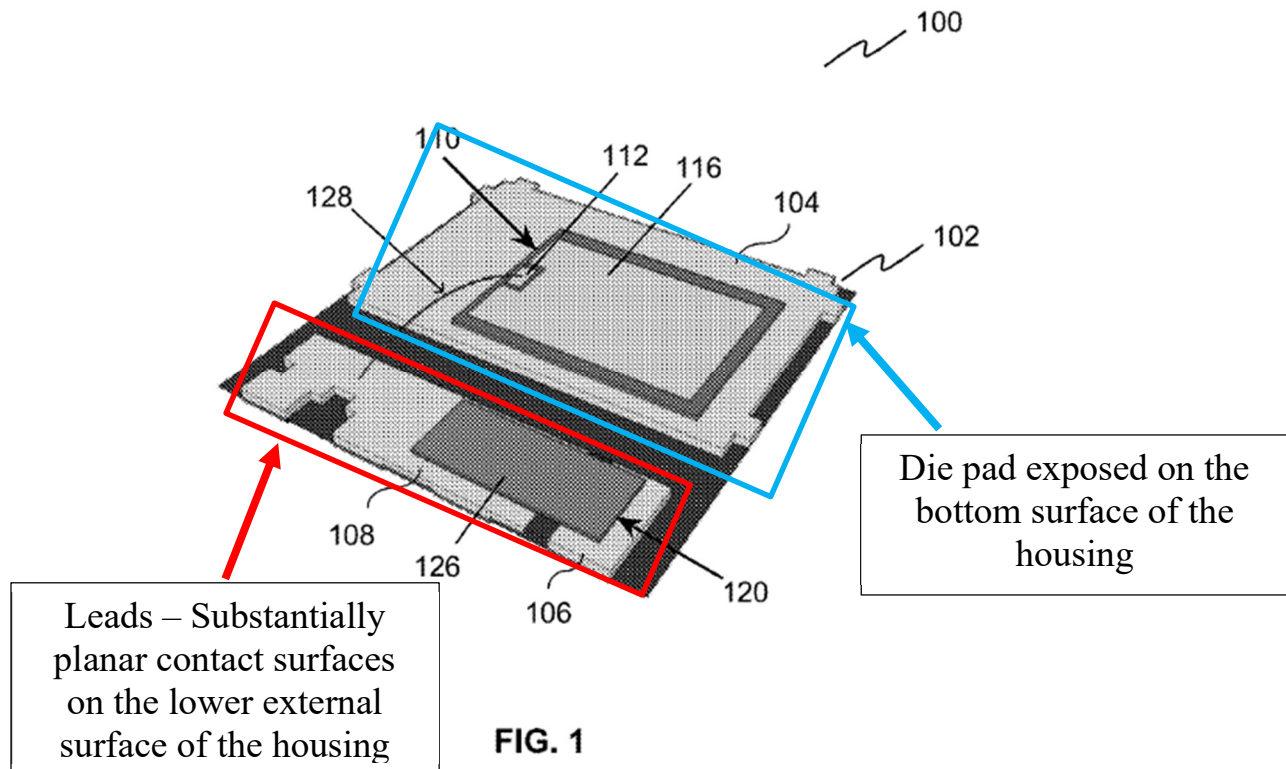
Roberts discloses customary high-voltage device blocking voltages and switching speeds (claims 3 and 17), explained for Ground 1.

Otremba433 discloses planar exposed leads and an exposed die pad (claims 4, 9, and 17), and contact clip couplings, explained for Ground 1. Otremba433, [0037], [0039].



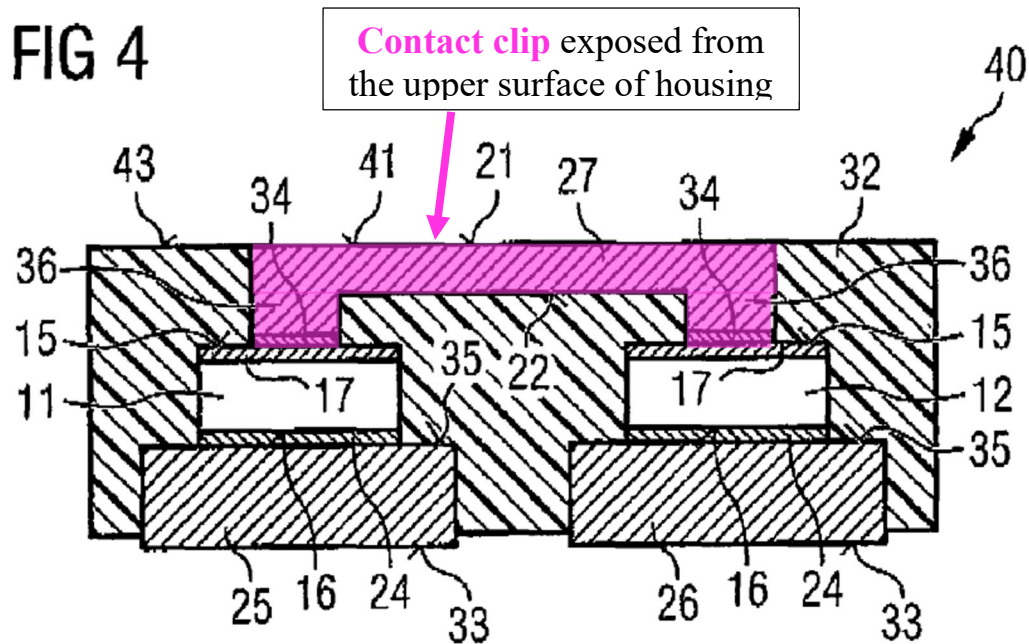
Id., Fig. 2 (annotated).

Otremba124 discloses a ThinPAK8x8, including planar exposed leads and an exposed die pad (claims 4, 9, 17), explained for Ground 1. Otremba124, [0041].



Id., Fig. 1 (annotated).

Otremba280 discloses using exposed contact clips to couple components (claims 7, 8), explained for Ground 1. Otremba280, 8:33-41, Fig. 4.



Id., Fig. 4 (annotated).

All references are analogous because they are in the same field of endeavor as the '481 patent—packaging designs for semiconductor electronic components. *In re Bigio*, 381 F.3d at 1325; Lebby [078]-[079], [0228]-[0234].

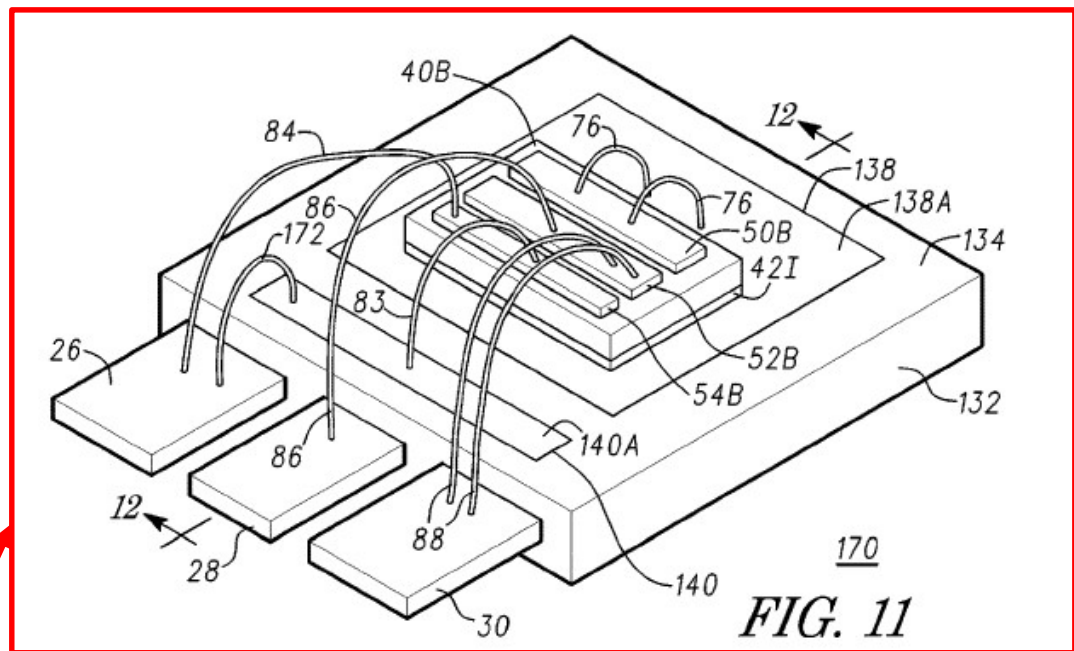
C. Ground 2A: Liu Renders Obvious Claims 1, 2, 4-6

1. Claim 1

a. [1pre]

Liu discloses [1pre] because it discloses a “semiconductor component 170.”

Liu, 8:1-3, Fig. 11; Provisional, [00041], Fig. 11; Lebby, [0235].



Electronic component (component 170)

Liu, Fig. 11 (annotated); Provisional, Fig. 11.

b. [1a]

Liu discloses [1a] because Liu's semiconductor component 170 includes a “**semiconductor chip 40B** [that] is a compound semiconductor chip.” Liu, 8:16-25, Fig. 11; Provisional, [0042], Fig. 11. Semiconductor chip 40B includes a **drain contact 50B (first current electrode)**, a **source contact 52B (second current**

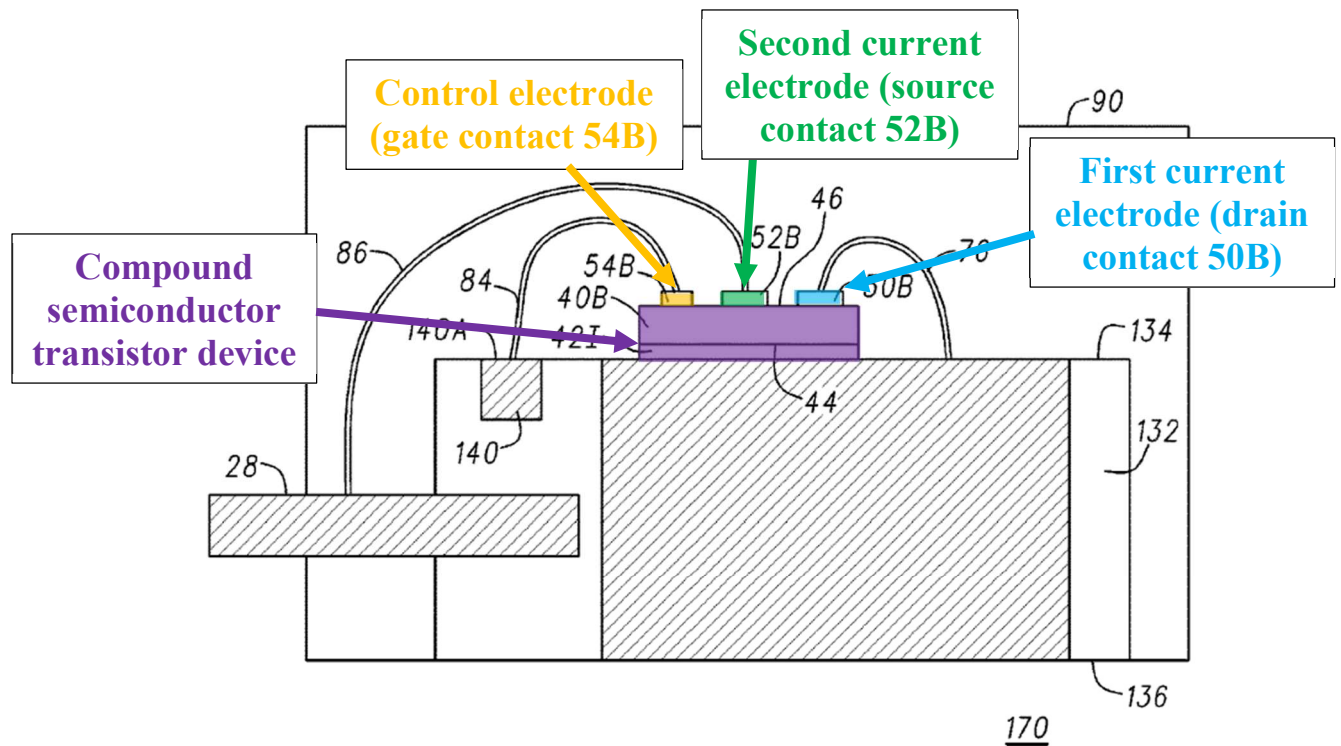


FIG. 12

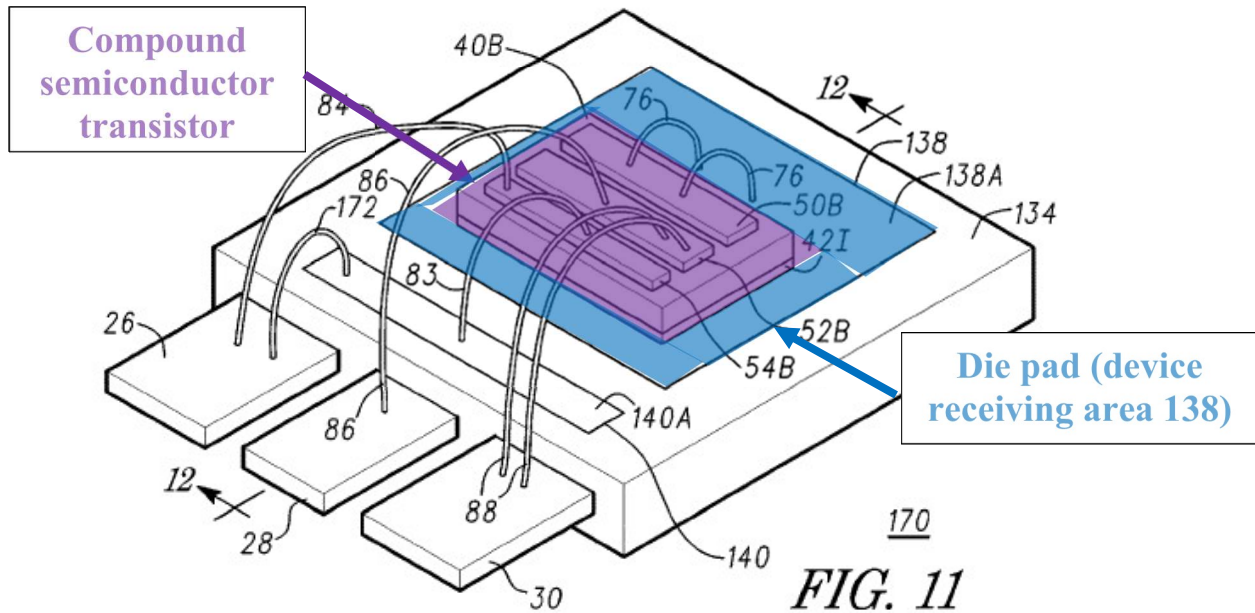
Liu, Fig. 12 (annotated); Provisional, Fig. 12.

c. [1b]

Liu discloses [1b] because it discloses a “device receiving area 138.” Liu, 5:42-45; Provisional, [00031].

As explained for Ground 1A, [1b], a die pad is a common component of a transistor device that serves as a mounting area for a chip. Lebbly, [0238]. Liu’s device receiving area 138 is comprised of surface 138A. Liu, 8:11-14; Provisional, [00042]. Surface 138A uses a die attach material 421. *Id.* **Device receiving area 138**, which includes surface 138A and die attach material 421, supports

semiconductor chip 40B mounted thereon, and is the die pad. Liu, 8:11-16; Provisional, [00042]; Lebby, [0237]-[0238].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

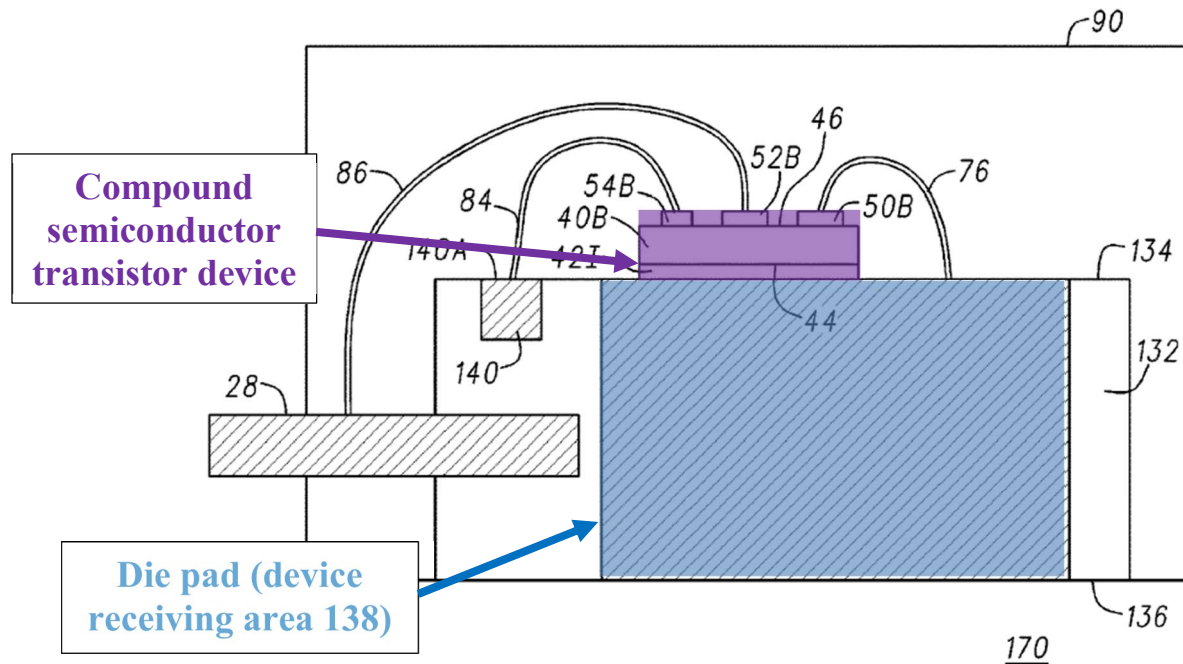


FIG. 12

Liu, Fig. 12 (annotated); Provisional, Fig. 12.

d. [1c]

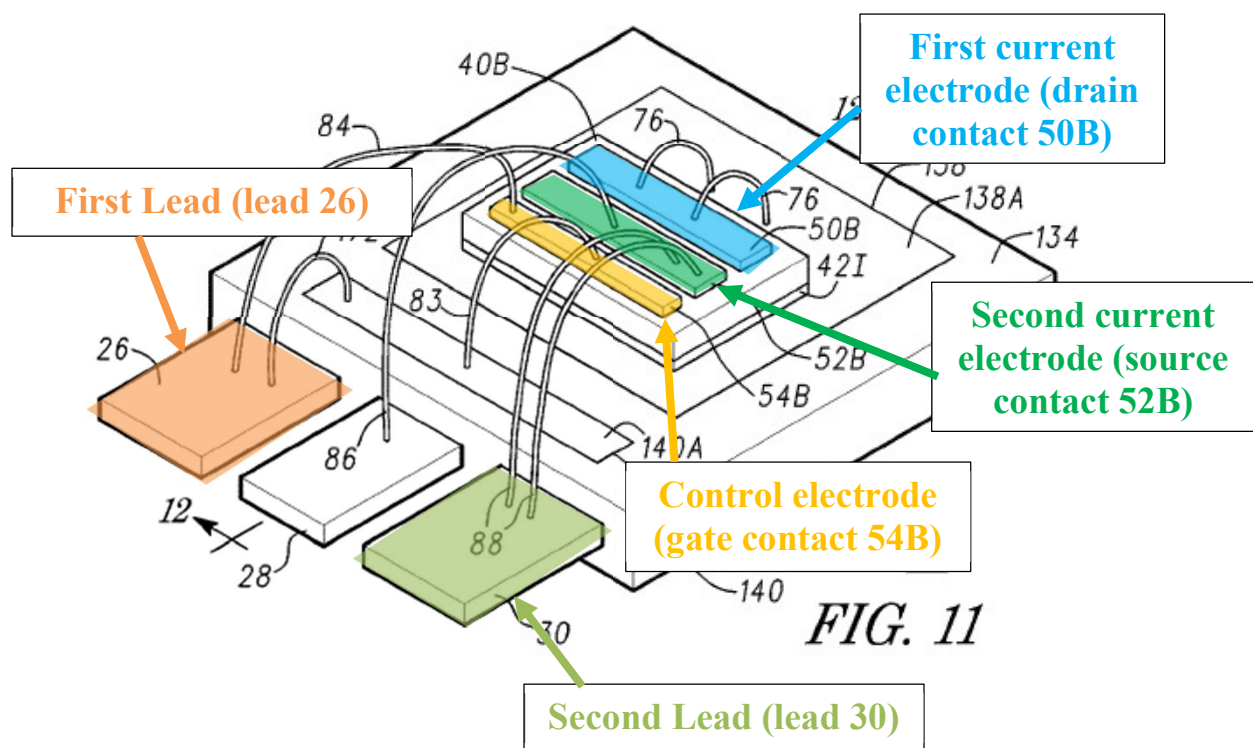
[1d]

[1e]

As explained for Ground 1A, [1c]-[1e] collectively recite three leads and the various connections of components within the device.

As explained for [1a], Liu's semiconductor device includes a **drain contact 50B (first current electrode)**, a **source contact 52B (second current electrode)**, and a **gate contact 54B (control electrode)**. Liu, 8:16-25; Provisional, [00042]. Liu discloses leadframe leads coupled to the various electrodes of its semiconductor

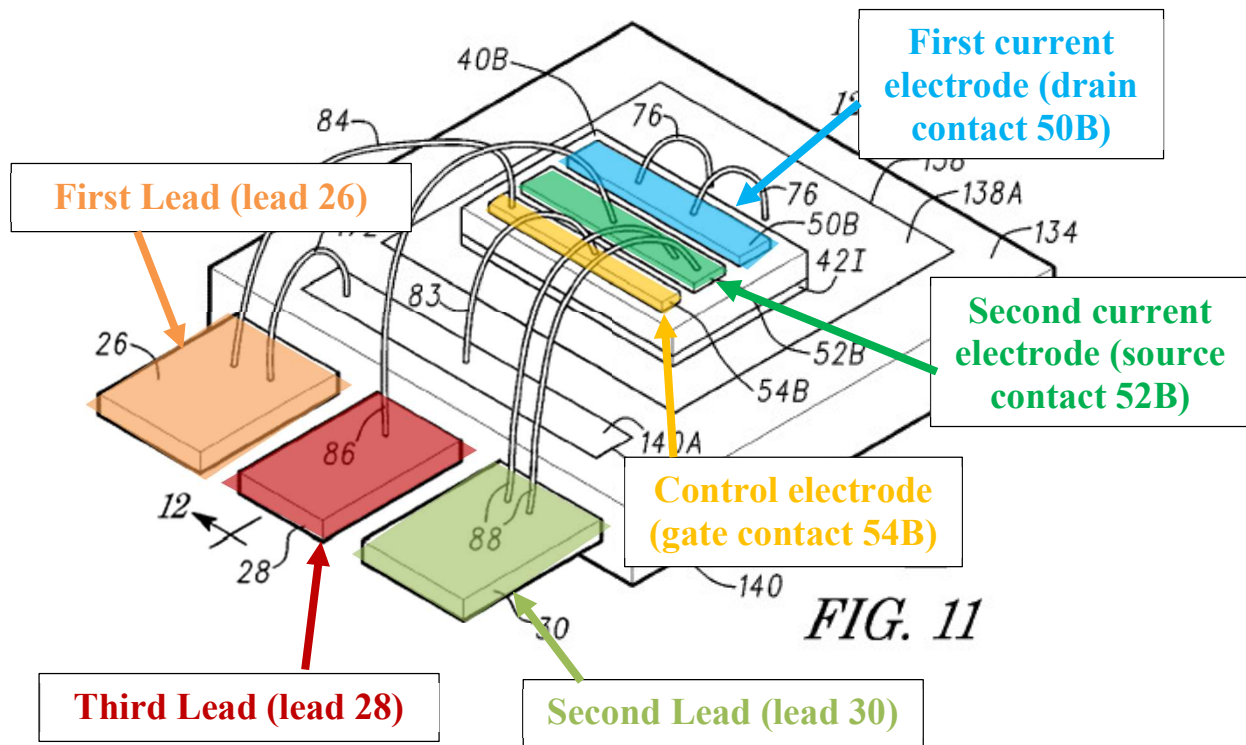
chip. Liu's **gate contact 54B (control electrode)** is coupled to a leadframe **lead 26 (first lead)**, Liu's **drain contact 50B (first current electrode)** is coupled to the **device receiving area 138 (die pad)**, and Liu's **source contact 52B (second current electrode)** is coupled to the leadframe **lead 30 (second lead)**. Liu, 8:27-40; Provisional, [00043].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

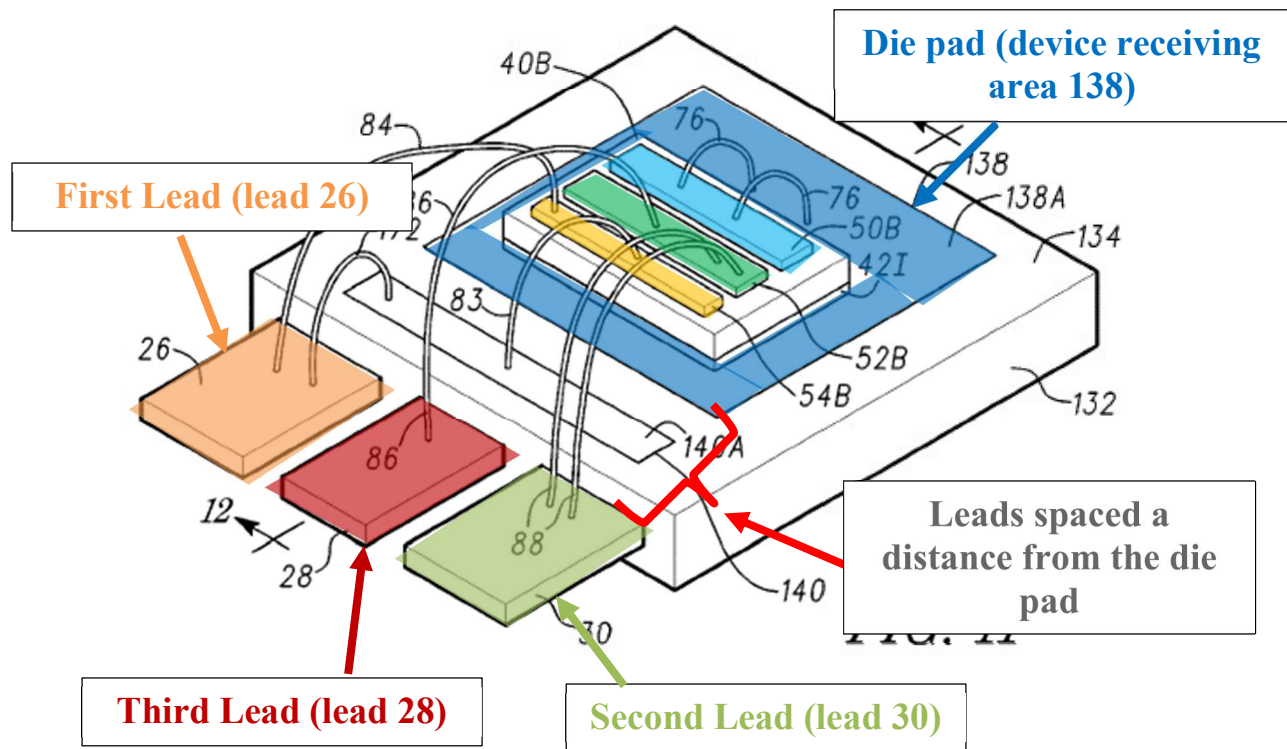
Liu's leadframe **lead 28 (third lead)** is connected to "source contact 52B of semiconductor device 40B" (coupled to the compound semiconductor transistor device). Liu, 8:27-33; Provisional, [00043]. Liu's leadframe **lead 28** "is a Kelvin leadframe lead or a Kelvin lead." Liu, 8:36-40; Provisional, [00043]. A POSITA

would have understood that a Kelvin leadframe provides monitoring and sensing to provide accurate measurements of resistance and voltage, and therefore has a source sensing functionality. Lebbby, [0241]; Ground 1A, [1c]-[1e].

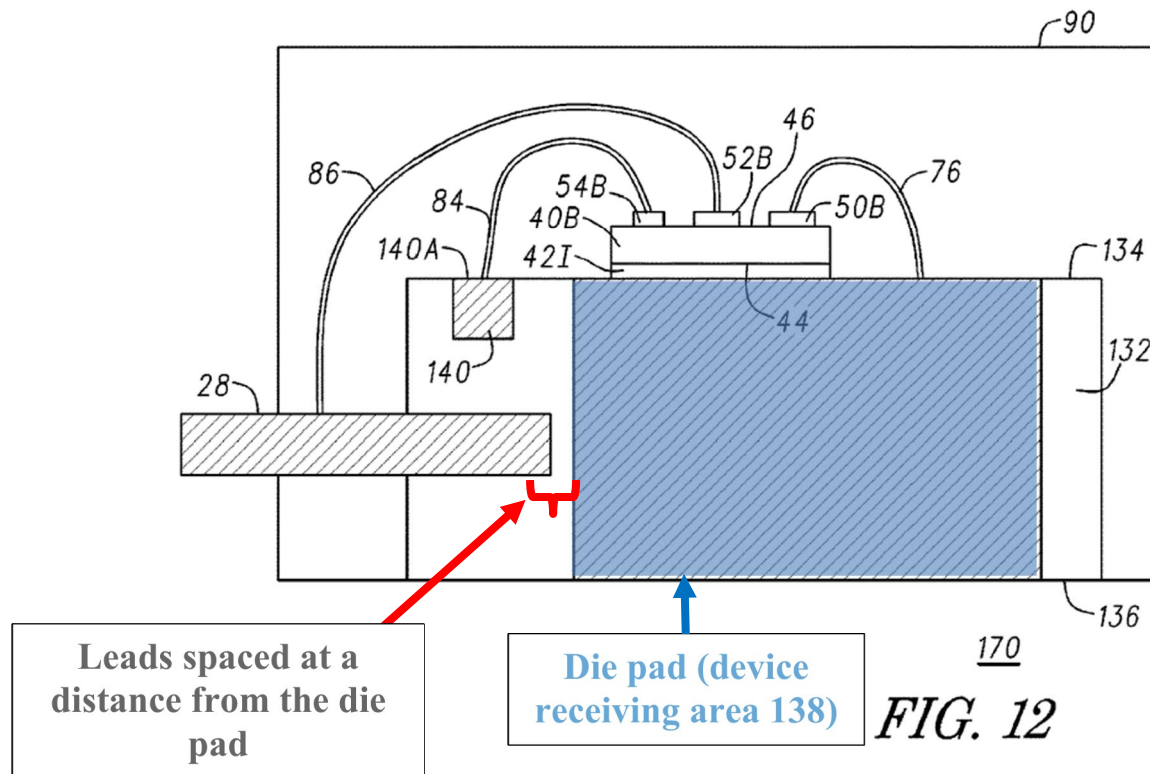


Liu, Fig. 11 (annotated); Provisional, Fig. 11.

Figures 11 and 12 show leadframe leads 26, 28, and 30 positioned a distance from Liu's device receiving area 138 (die pad). Liu, Fig. 11-12; Provisional, Fig. 11-12; Lebbby, [0239]-[0242].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

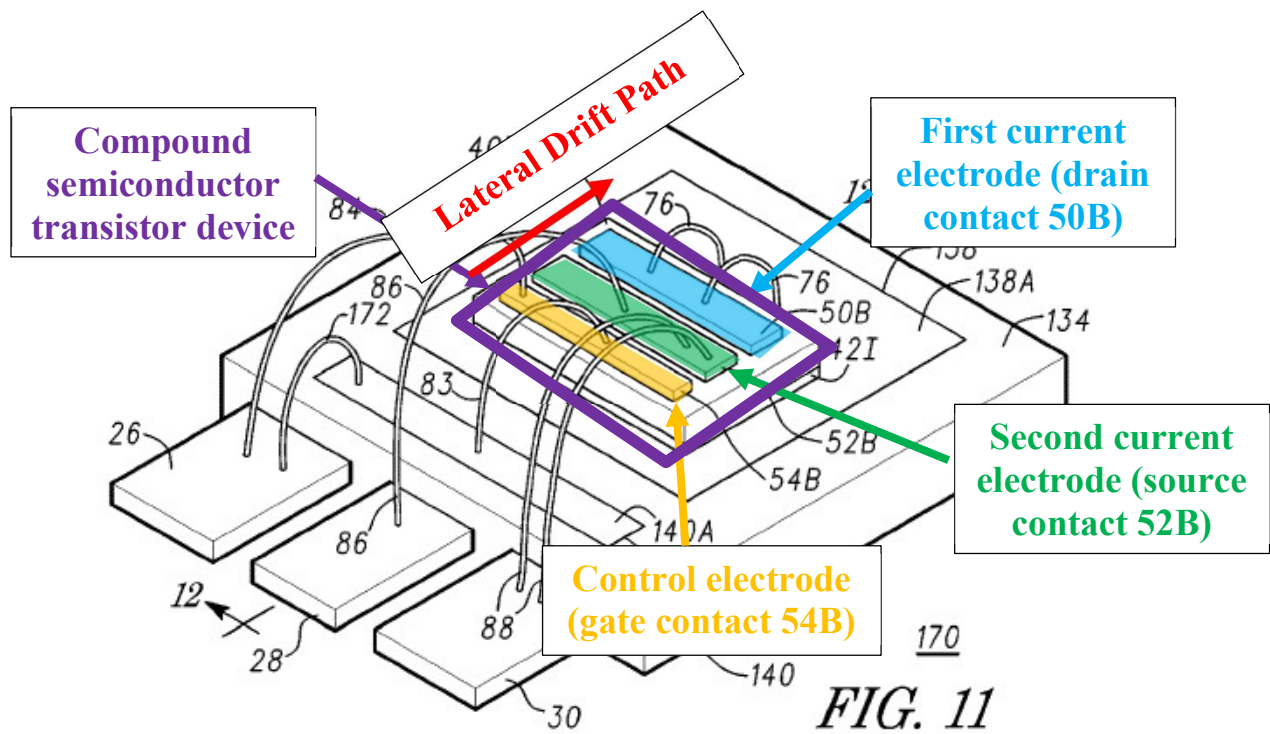


Liu, Fig. 12 (annotated); Provisional, Fig. 12.

e. [1f]

Liu discloses [1f] because Liu's semiconductor component 170 is arranged laterally, and the drain is coupled to the device receiving area 138 (die pad).

Liu's source, drain, and gate are spread laterally across the semiconductor material creating a lateral drift path, as opposed to a vertical configuration:



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

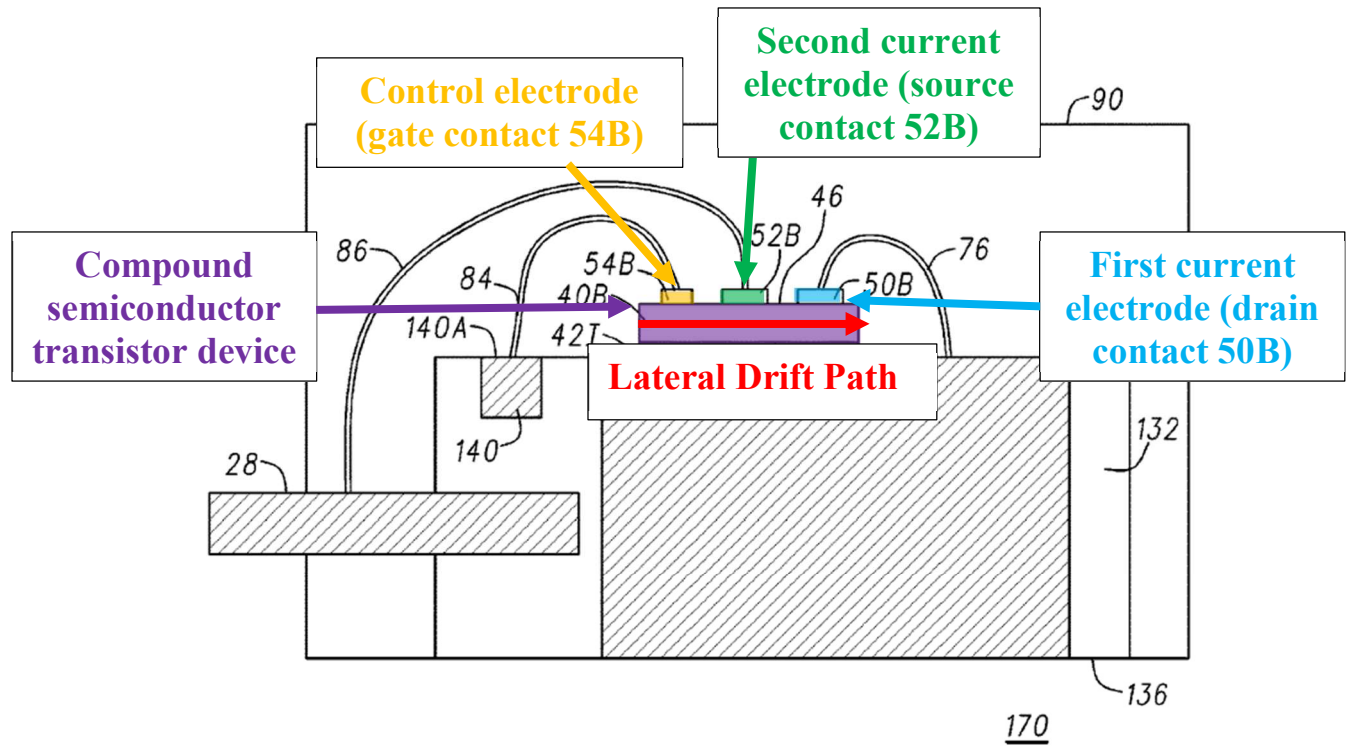
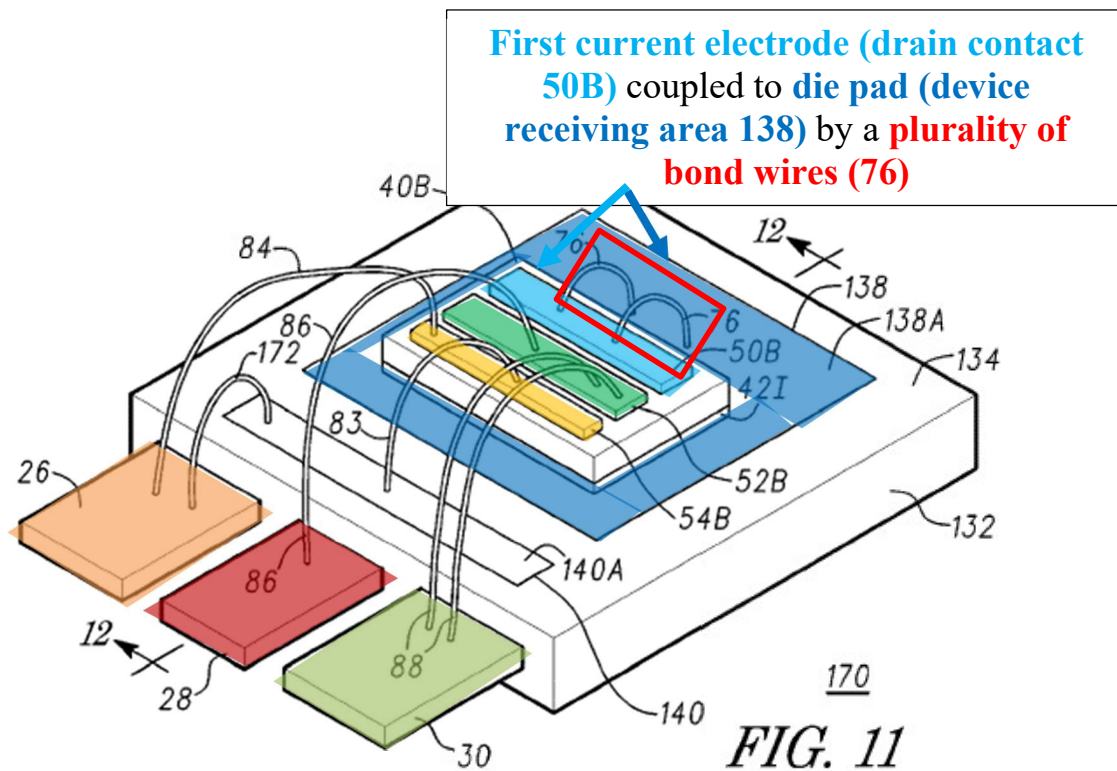


FIG. 12

Liu, Fig. 12 (annotated); Provisional, Fig. 12.

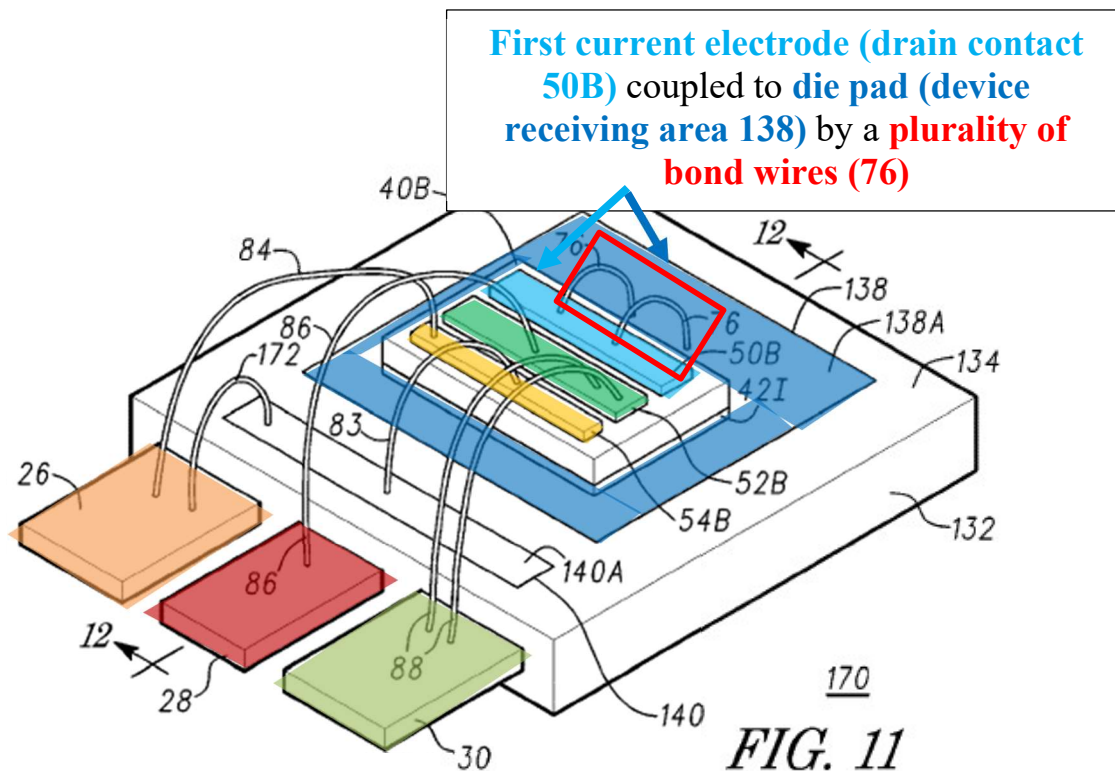
As explained for [1c]-[1e], Liu's drain is coupled to the receiving area 138 (die pad) via bond wires. Liu, 8:27-33; Provisional, [00043]; Lebby, [0243]-[0246].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

f. [1g]

Liu discloses [1g] because, as explained for [1e]-[1f], Liu's drain contact 50B (first current electrode) is coupled to its device receiving area 138 (die pad) by bond wires. Liu, 8:27-33; Provisional, [00043]; Lebby, [0247]-[0249].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

2. Claim 2

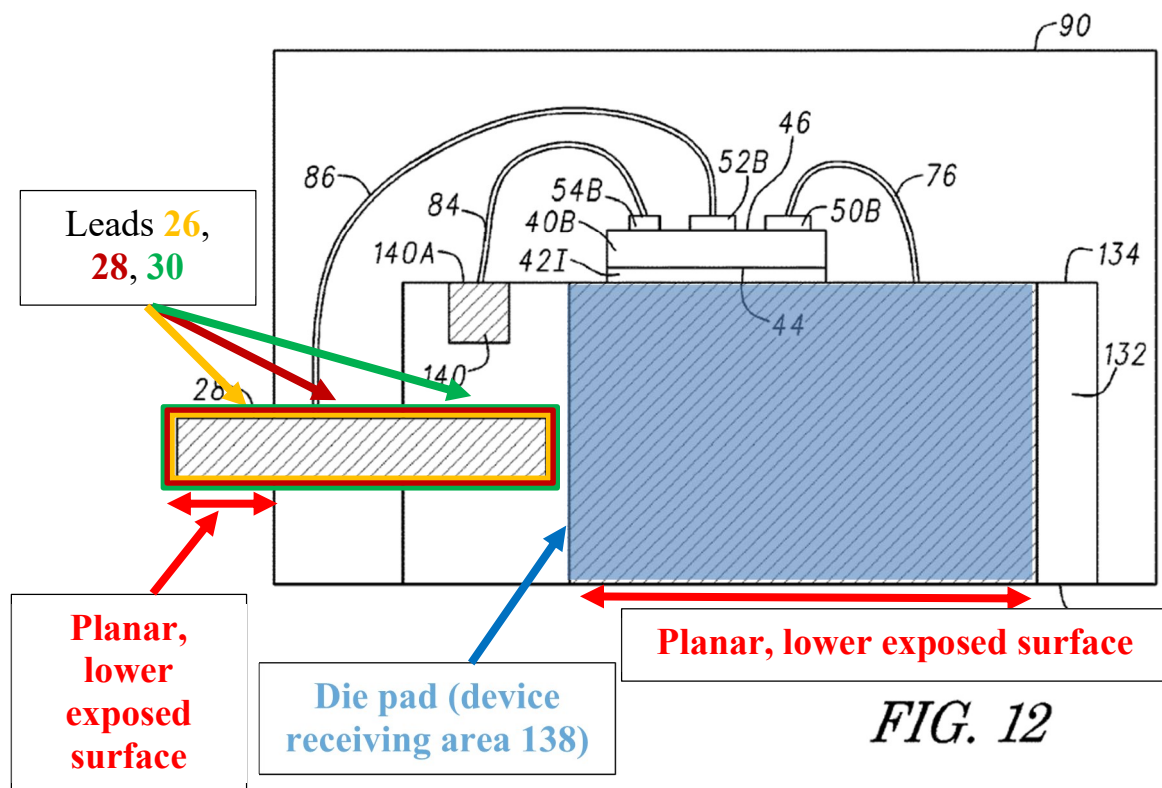
Liu discloses claim 2 because Liu's "semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride." Liu, 3:55-58; Provisional, [0021]; Lebby, [0250].

3. Claim 4

Liu discloses claim 4 because Liu's leads and die pad are exposed from its housing with substantially planar lower surfaces.

Liu discloses a housing—a mold compound 90 that encapsulates the device receiving area—semiconductor chip, and bond wires. Liu, 7:33-38; Provisional, [00038].

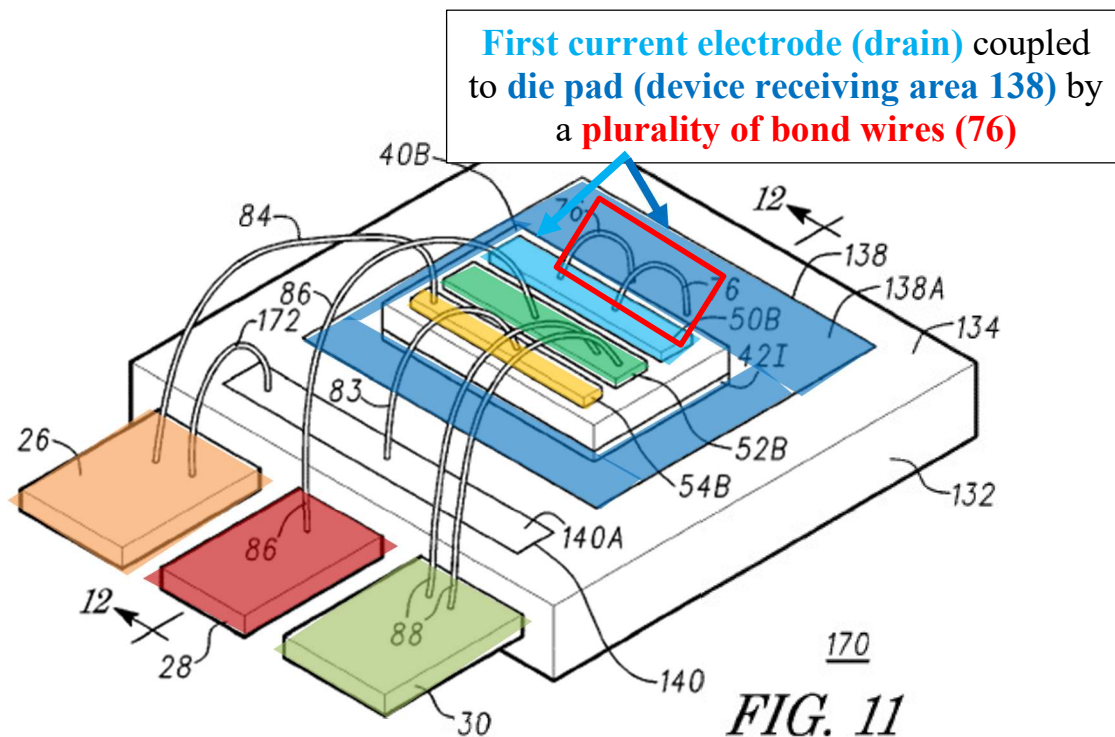
As explained for [1b]-[1e], Liu discloses three leads and a die pad. Figure 12 shows the lower surfaces of Liu's leads and die pad exposed from housing 90 with planer surfaces. Liu's device receiving area 138 (die pad) and leadframe leads 26, 28, and 30 have substantially planar lower contact surfaces. Lebbly, [0251]-[0253].



Liu, Fig. 12 (annotated); Provisional, Fig. 12.

4. Claim 5

To the extent claim 5 is interpreted as requiring a **lateral transistor** with the drain coupled to the die pad, Liu discloses it as explained for [1e]-[1g]. Liu's **drain contact 50B (first current electrode)** is coupled to the **device receiving area 138 (die pad)**. Liu, 8:27-33; Provisional, [00043]. Lebby, [0254].

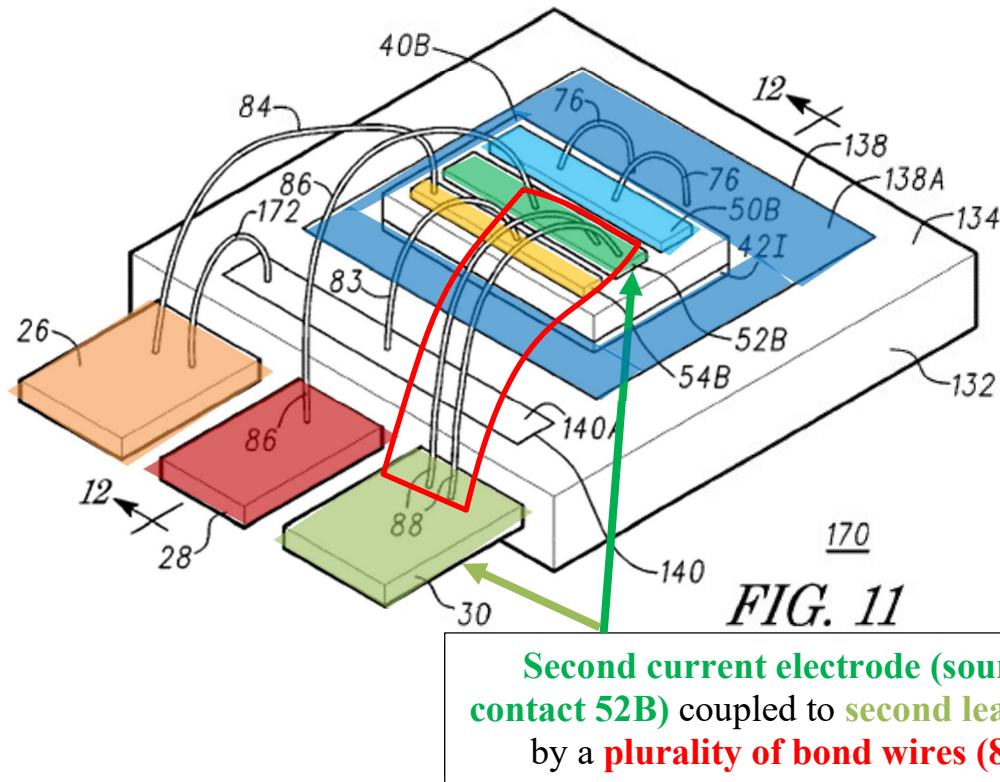


Liu, Fig. 11 (annotated); Provisional, Fig. 11.

5. Claim 6

Liu discloses claim 6 because, as explained for [1e], Liu's “**source contact** **52B** of semiconductor device 40B is electrically connected to leadframe lead 28

through a bond wire 86 and to **leadframe lead 30** through **bond wires 88.**” Liu, 8:27-33; Provisional, [00043]. Lebby, [0255]-[0258].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

D. Ground 2B: Liu in View of Roberts Renders Obvious Claims 3, 17

1. Claim 3

Liu in view of Roberts renders claim 3 obvious. A POSITA would have understood Liu’s compound semiconductor device would have achieved at least 400V and a switching frequency capability of at least 100 kHz, which were common for compound semiconductor power conversion transistors designed for high-voltage applications, as disclosed by Roberts.

Although Liu does not expressly disclose its device's voltage blocking and switching speed, as explained for claim 3, Ground 1A, Roberts explains that these characteristics were common. Roberts, [0006], [0008], [0012].

As explained for claim 3, Ground 1A, a POSITA would have understood that a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz were standard, routine, and readily-achievable characteristics for compound semiconductor transistors designed for high-voltage applications (like Liu) and were the very benefits of compound semiconductor devices. Lebbby, [0259]-[0262].

Because Liu expressly discloses compound semiconductor transistor devices but is silent on corresponding switching time or frequency, a POSITA would have been motivated to look to references that disclose expected switching time or frequencies for other compound semiconductor devices to better understand or interpret the achievable characteristics of Liu's device, including high-voltage application GaN transistor devices like in Roberts. Because these characteristics were well known, a POSITA would have had a reasonable expectation of success in operating Liu's compound semiconductor transistor device with a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz. Lebbby, [0259]-[0262].

2. Claim 17

a. [17p]

Liu discloses [17p] as explained for [1p]. Lebby, [0263].

b. [17a]

As explained for [1a] and claim 2, Liu discloses a Group III nitride-based transistor device.

As explained for claim 3, Liu-Roberts teaches a blocking voltage capability of at least 100 kHz.

As explained for [1a], Liu discloses a first current electrode, a second current electrode, and a control electrode.

As explained for [1e], Liu's control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead, and a third lead is coupled to the transistor device and provides a source sensing functionality. Lebby, [0264]-[0268].

c. [17b]

Liu discloses a housing as explained for claim 4. Lebby, [0269].

d. [17c]

Liu teaches [17c] as explained for [1d]. Lebby, [0270].

e. [17d]

Liu teaches [17d] as explained for claim 4. Lebby, [0271].

f. [17e]

As explained for [17a] and claim 2, Liu discloses a Group III nitride-based transistor device.

Liu teaches the remainder of [17e] as explained for [1f]. Lebbby, [0272]-[0274].

g. [17f]

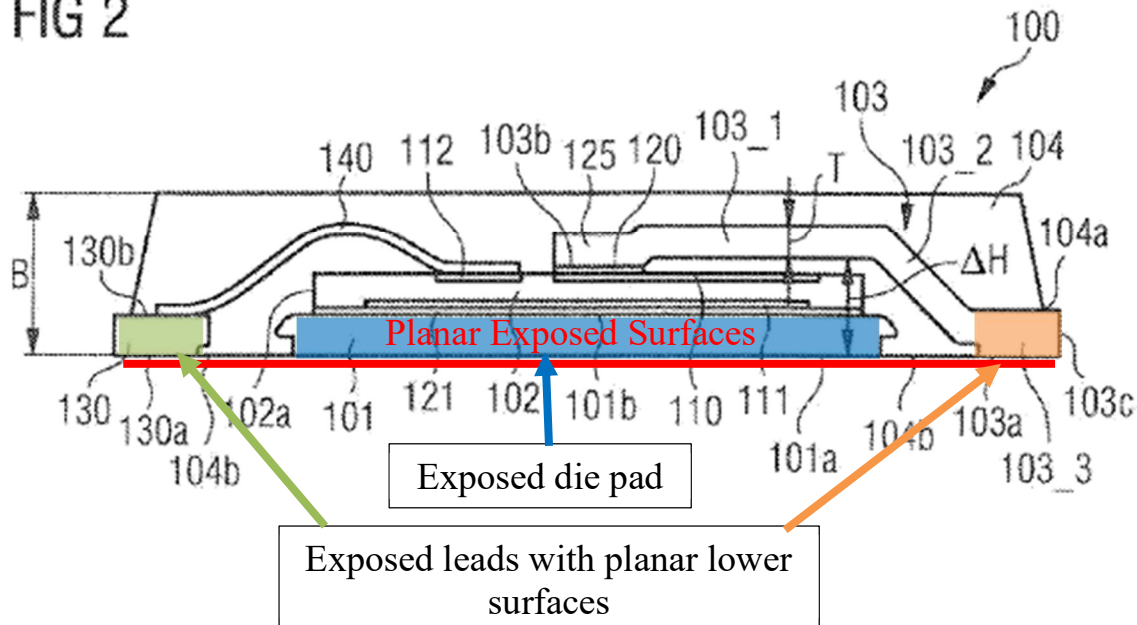
Liu discloses [17f] as explained for [1g]. Lebbby, [0275].

E. Grounds 2C and 2D: Liu in View of Otremba433 (Ground 2C) and Liu in View of Otremba124 (Ground 2D) Render Claims 4, 9 Obvious

1. Claim 4

For Ground 2C, as explained for claim 4, Ground 1C, Otremba433 discloses a “leadless package” with contacts and a die pad exposed on the bottom of the devices (Otremba433, [0037], [0039]), as was commonly known (Otremba280, 4:17-29).

FIG 2

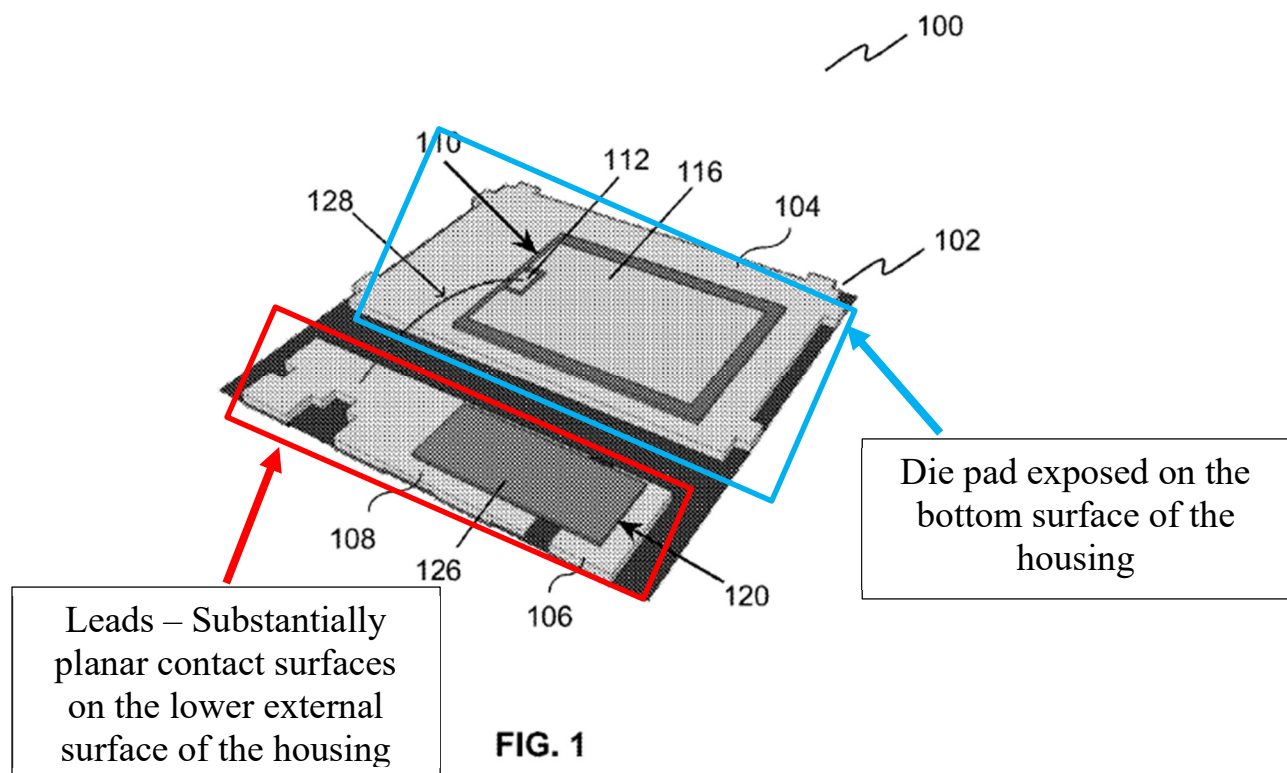


Otremba433, Fig. 2 (annotated).

A POSITA would have understood Liu's device would be readily implemented in the leadless package of Otremba433 because package designs were easily modifiable to meet the needs of a particular use. Liu implements a leaded package, but a POSITA would have realized the known benefits of leadless package designs. Leadless package designs saved space on the printed circuit board and showed faster performance and switching speeds than through-hole and other conventional packages, enabling improved performance, switching behavior, ease of use, EMI, reliability, and higher power density. Leiby, [0276]-[0279]. A POSITA would have understood the known benefits a leadless package as improvement to Liu's device ready for such improvement—combining prior art elements using

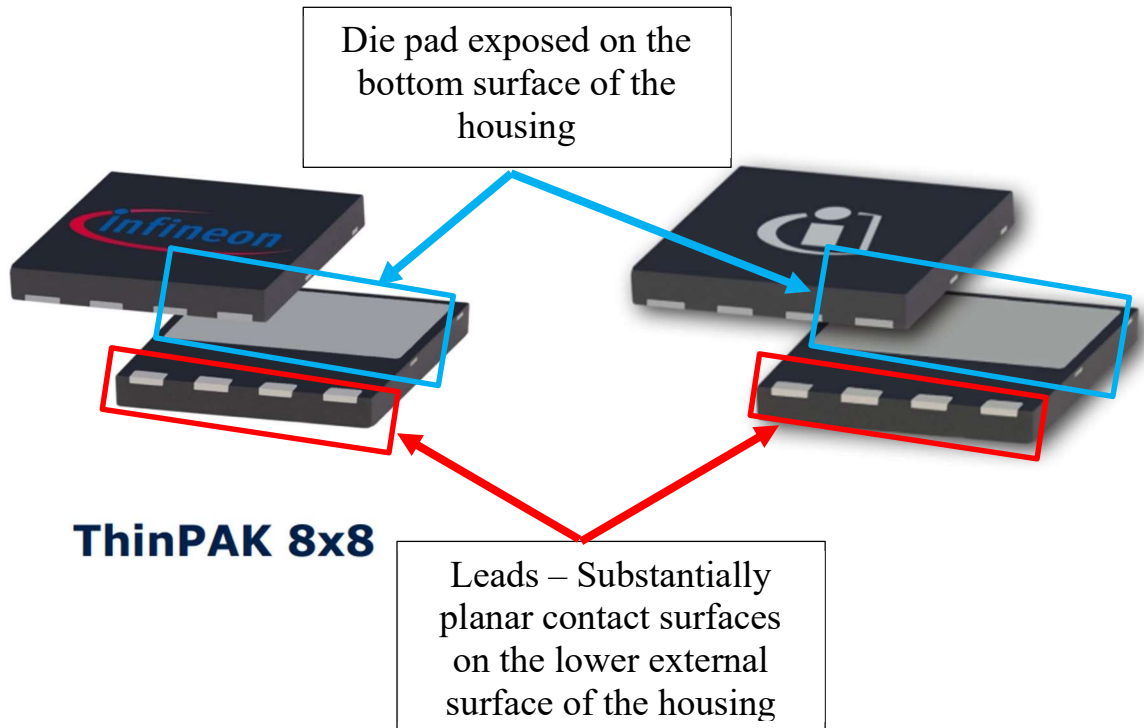
known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416. And leadless packaging types were known, including those with source sensing leads, like a DFN8x8 package. Lebbby, [0278]-[0279] (citing Huang, 2, Fig. 2).

For Ground 2D, as explained for claim 4, Ground 1B, Otremba124 discloses a power transistor including a GaN HEMT “packaged in a[n] 8x8 ThinPAK” with flat source leads 108 and 106 on the bottom of the package. Otremba124, [0041].



Id., Fig. 1 (annotated).

As explained for claim 4, Ground 1B, ThinPAK8x8 was a well-known leadless package design and included leads and a die pad exposed on the lower surface and forming planar contacts (a leadless design). Leebby, [0280]-[0281]; ThinPAK8x8 Brochure, 1, 5, 6; ThinPAK Recommendations 1, 4.



ThinPAK8x8 Brochure, 1, 31; ThinPAK Recommendations, 1 (annotated).

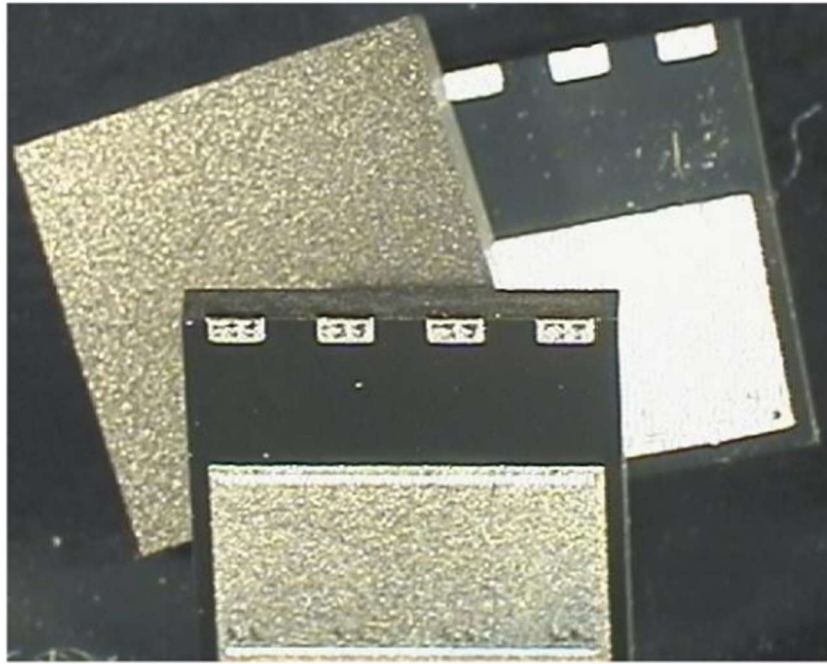


Figure 1: Top and bottom view of VDSO4 (ThinPAK 8x8)

ThinPAK Recommendations, 4 (Fig. 1) (annotated).

A POSITA would have been motivated to package Liu's semiconductor device in the Otremba124's ThinPAK8x8 package with an exposed die pad and planar lead contacts on the lower surface because, as explained for claim 4, Ground 1B, ThinPAK8x8 was boasted as an improvement over leaded packaging designs, saving space on the printed circuit board (PCB), and having faster performance and switching speeds enabling improved performance, switching behavior, ease of use, EMI, reliability, and higher power density. ThinPAK8x8 Brochure, 3.

Because Liu implements a leaded package design, a POSITA would have realized the benefits ThinPAK8x8 offered as improvements Liu's device. Lind even

shows ThinPAK8x8 with source sensing connections as an alternative to a leaded package.

III. Source-Sense concept and A/B simulation

A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.

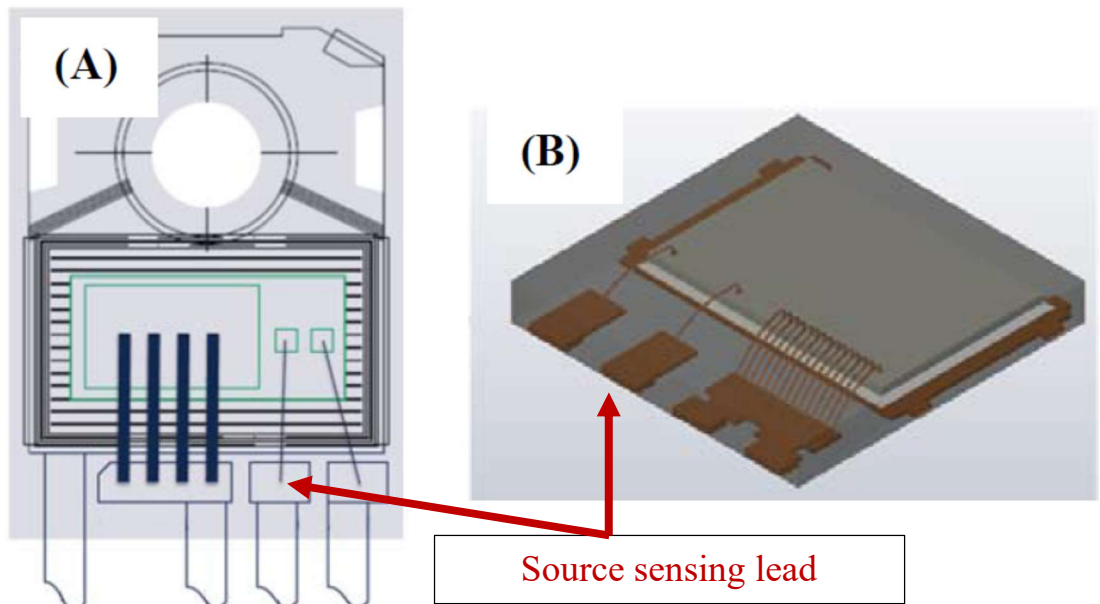


Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections

Lind, 3 (Fig. 4) (annotated).

Packaging Liu as Otremba124's ThinPAK8x8 would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416.

Additional package formats, including leadless, exposed-die packages were known, as taught by Otremba433 and Otremba400, and would have been at least

considered suitable options for packaging Liu's device. *Intel*, 21 F.4th at 800; *PAR Pharm.*, 773 F.3d at 1197-98. Otremba433 recognizes that leaded and leadless packages were suitable alternatives. Otremba433, [0025]; Lebby, [0282]-[0284]. And leadless packaging types including those with source sensing leads, like a DFN8x8 package, were known. Lebby, [0284] (citing Huang, 2, Fig. 2).

2. Claim 9

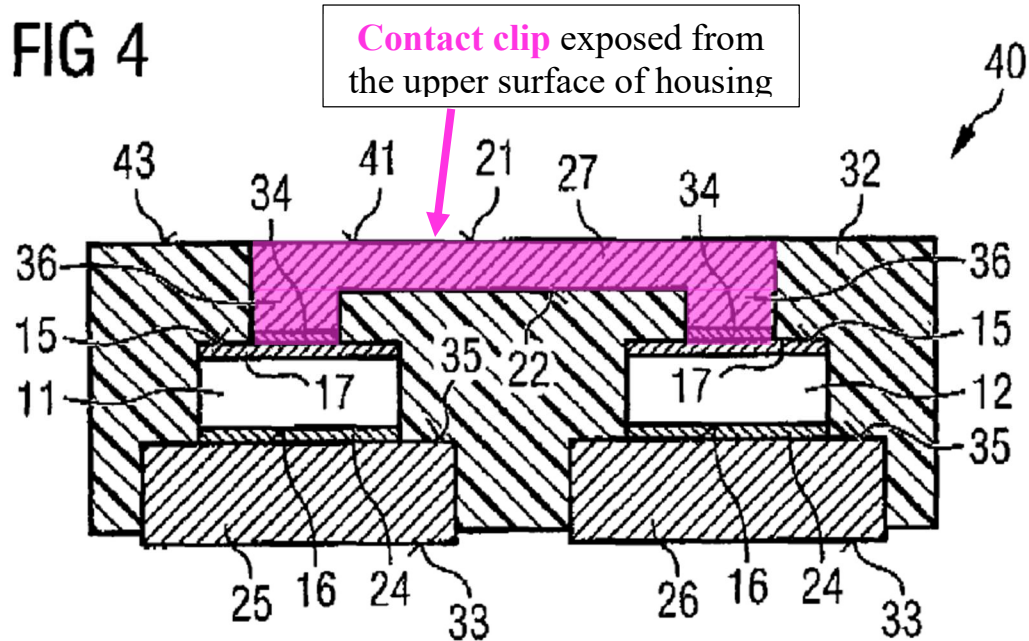
For Ground 2C, Liu in view of Otremba433, which expressly discloses a leadless package outline, such as the ThinPAK8x8 package outline (*id.*, [0025], [0037]), renders claim 9 obvious for the same reasons explained for claim 4. Lebby, [0285]-[0286].

For Ground 2D, Liu in view of Otremba124, which expressly discloses ThinPAK8x8 packaging (Otremba124, [0041]), renders claim 9 obvious as explained for claim 4. Lebby, [0287].

F. Ground 2E: Liu in View of Otremba433 and Otremba280 Renders Claims 7, 8 Obvious

1. Claim 7

As explained for claim 6, Liu discloses replacing bond wires with a contact clip. As explained for claim 7, Ground 1C-1D, Otremba280 discloses using exposed contact clips. Otremba280, 8:33-41, Fig. 4.



Id., Fig. 4 (annotated).

Otremba280 expressly discloses exposing the contact clip because the “exposed area 41 of the contact clip 14 provides a shorter path of thermal resistance” with “the environment around the electronic component 40” to realize “improvement in the efficiency of thermal dissipation from the electronic component 40.” *Id.*, 8:45-51.

As explained for claim 1, Grounds 1C-1D, to realize thermal benefits, and as Dr. Lebby explains, a POSITA would have been motivated to implement Otremba280’s exposed contact clip to (1) improve current carrying capability; (2) allow for better current spreading to avoid hot spots; (3) reducing on resistance; and (4) reducing parasitic induction. Lebby, [0288]-[0296]. Bond wires and contact clips

were known alternatives for coupling components, each suited to different design preferences and needs, both constituting suitable options. *Intel*, 21 F.4th at 800; *PAR Pharm.*, 773 F.3d at 1197-98.

2. Claim 8

As explained for claim 7, coupling Liu's components with an exposed contact clip would have been obvious. Coupling Liu's second current electrode to the second lead with Otremba280's exposed contact clip would have been obvious for the same reason. Lebbby, [0297].

G. Ground 2F: Liu in View of Roberts and Otremba433 Renders Obvious Claim 17

1. Claim 17

a. [17p]

Liu discloses [17p] as explained for [1p]. Lebbby, [0298].

b. [17a]

Liu in view of Roberts renders obvious [17a].

As explained for [1a] and claim 2, Liu discloses a Group III nitride-based transistor device.

As explained for claim 3, Liu-Roberts teaches a blocking voltage capability of at least 100 kHz.

As explained for [1a], Liu discloses a first current electrode, a second current electrode, and a control electrode.

As explained for [1e], Liu teaches the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead, and a third lead is coupled to the transistor device and provides a source sensing functionality. Leebby, [0299]-[0303].

c. [17b]

Liu discloses a housing as explained for claim 4. Leebby, [0304].

d. [17c]

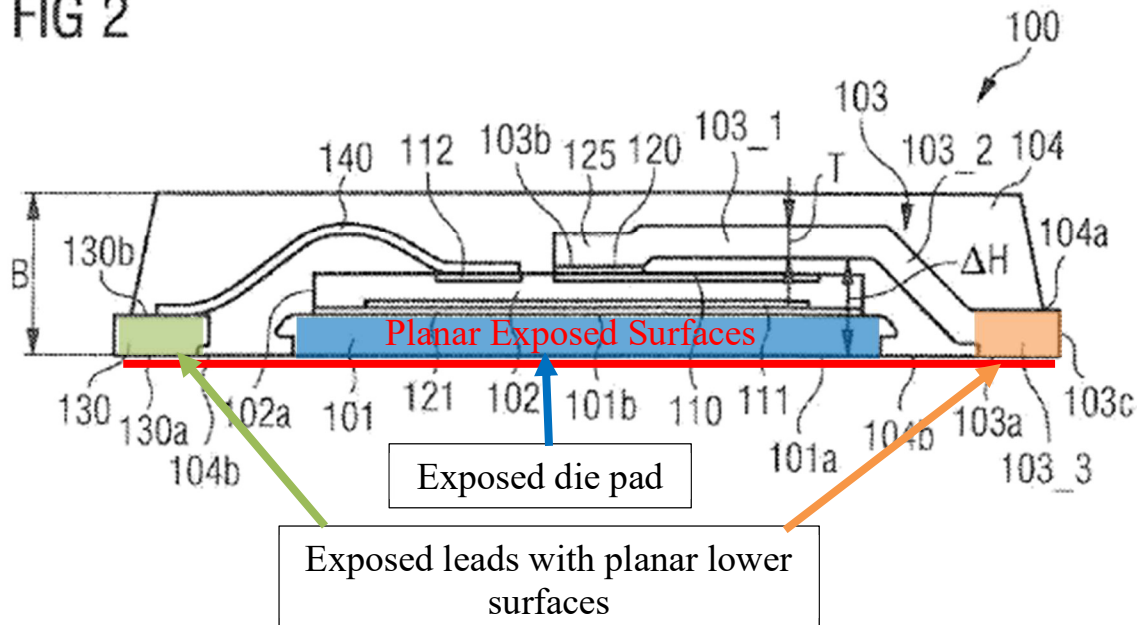
Liu teaches [17c] as explained for [1d]. Leebby, [0305].

e. [17d]

Liu teaches [17d] as explained for claim 4.

As explained for Ground 2C, Otremba433 discloses a “leadless package” with contacts and die pad exposed on the bottom of the devices. Otremba433, [0037]. Otremba433’s contacts 130 and 103 (leads) have “external contact area[s]” 103a and 130a that are “coplanar with a reference plane defined by a bottom surface 101a of the carrier 101” (die pad) that is “exposed at the bottom of the package.” *Id.*, [0037] (discussing lead 103/103a and carrier 101/101a), [0039] (discussing lead 130/130a).

FIG 2



Id., Fig. 2 (annotated).

A POSITA would have understood Liu's device would be readily implemented in the leadless package of Otremba433 and would have been motivated to do so as explained for Ground 2C, claim 4. Lebbby, [0306]-[0308].

f. [17e]

As explained for [17a] and claim 2, Liu discloses a Group III nitride-based transistor device.

Liu teaches the remainder of [17e] as explained for [1f]. Lebbby, [0309]-[0311].

g. [17f]

Liu discloses [17f] as explained for [1g]. Lebbby, [0312].

VII. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *Fintiv* Denial Is Improper

The *Fintiv* factors weigh strongly in favor of institution because the district court case has minimal investment from the Court or Parties. No discovery or claim construction has occurred. No trial date is set. Defendants have not responded to the Complaint (response due June 25, 2024), and an initial case management conference is not scheduled until July 22, 2024 (Ex-1019).

B. 35 U.S.C. §325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, 17-18 (PTAB Dec. 15, 2017) and *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, 8-11 (PTAB Feb. 13, 2020) (precedential) favor institution.

Advanced Bionics, step 1 (*BD* factors (a), (b), (d)) favor institution because none of the cited references were before the Office during prosecution. Ex-1002; Ex-1001, Cover.

Advanced Bionics, step 2, (*BD* factors (c), (e), (f)) favor institution because the cited references are not cumulative of those before the Office during prosecution—they disclose 1) “the first transistor device is a lateral transistor device and a drain or a source of the first transistor device is coupled to the die pad” (which applicants argued was not presented in the examined art (Ex-1002, 31-32)), and 2)

“the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip” (which the Examiner identified in the reasons for allowance (*id.*, 12-14)).

VIII. MANDATORY NOTICES

A. Real Parties-in-Interest

The real parties-in-interest are Innoscience America, Inc.; Innoscience (Zhuhai) Technology Company, Ltd.; and Innoscience (Suzhou) Technology Holding Company, Ltd.

B. Related Matters

To the best of Petitioner’s knowledge, the ’481 patent is involved in:

Name	Number	Court	Filed
<i>Infineon Techs. Austria AG v. Innoscience (Suzhou) Tech. Co., Ltd. et al.</i>	3:24-cv-01553	N.D. Cal.	March 13, 2024

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Petitioner consents to electronic service at the following email address:

Innoscence-Infineon-IPR@finnegan.com.

IX. STANDING

The '481 patent is available for IPR. Petitioner is not barred or estopped.

X. CONCLUSION

Petitioner requests institution and cancellation of challenged claim.

Dated: June 14, 2024

/Lionel M. Lavenue/

Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CLAIM APPENDIX

1. **[1p]** An electronic component, comprising:
 - [1a]** a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;
 - [1b]** a die pad; and
 - [1c]** a first lead, a second lead and a third lead,
 - [1d]** wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,
 - [1e]** wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,
 - [1f]** wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad,
 - [1g]** wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.
2. The electronic component of claim 1, wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device.

3. The electronic component of claim 1, wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.
4. The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.
5. The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad.
6. The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.
7. The electronic component of claim 4, wherein the first current electrode is coupled to the die pad by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.
8. The electronic component of claim 4, wherein the second current electrode is coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.
9. The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline.

10. **[10p]** A switch circuit, comprising:

[10a] a first transistor device comprising a compound semiconductor, a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead, and a third lead, the first lead, the second lead and the third lead being spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the transistor device and provides a source sensing functionality, and

[10b] a second transistor device,

[10c] wherein the first transistor device has a current path coupled serially or antiserially with a current path of the second transistor device,

[10d] wherein the first transistor device is a lateral transistor device and a drain or a source of the first transistor device is coupled to the die pad,

[10e] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

11. The switch circuit of claim 10, wherein a drain of the first transistor device and a source of the second transistor device are coupled to a common die pad.
12. The switch circuit of claim 10, wherein the first transistor device is housed in a package comprising a first die pad coupled to a drain of the first transistor

device and the second transistor device is housed in a package comprising a second die pad coupled to a source of the second transistor device.

13. The switch circuit of claim 12, wherein the first die pad and the second die pad are mounted on a common conductive layer.
14. The switch circuit of claim 10, wherein a first contact clip is coupled to one of a source and a drain of the first transistor device and a second contact clip is coupled to the other one of a source and a drain of the second transistor device, wherein the first contact clip and the second contact clip are at least partially uncovered.
15. The switch circuit of claim 14, wherein the first contact clip and the second contact clip are coupled to a common heat dissipation member.
16. The switch circuit of claim 10, wherein a source of the first transistor device is coupled to a source of the second transistor device.
17. **[17p]** An electronic component, comprising:

 [17a] a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is

coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and

[17b] a housing,

[17c] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

[17d] wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces,

[17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad,

[17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

37 C.F.R. § 42.24(D) CERTIFICATION

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), Petitioner certifies that this Petition complies with the requirements of 37 C.F.R. § 42.24. Excluding parts of this Petition exempted under § 42.24(a), this Petition contains 13,990 words, as measured by the word-processing system used to prepare this paper.

Dated: June 14, 2024

By: Lionel M. Lavenue/
Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent 9,899,481, the Power of Attorney, and Exhibits 1001 through 1024, were served on June 14, 2024, by Priority Mail Express on the correspondence address of record indicated in the Patent Office's Patent Center website for the '481 patent:

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Date: June 14, 2024

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