

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

IPR2024-00975
Patent 9,899,481 B2

Before JO-ANNE M. KOKOSKI, CHRISTOPHER M. KAISER, and
DANIEL KAZHDAN, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. *Background and Summary*

Innoscence America, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting *inter partes* review of claims 1–17 (“the challenged claims”) of U.S. Patent No. 9,899,481 B2 (Ex. 1001, “the ’481 patent”). Infineon Technologies Austria AG (“Patent Owner”) filed a Preliminary Response (Paper 6, “Prelim. Resp.”).

We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). *Inter partes* review may not be instituted unless “the information presented in the petition filed under [35 U.S.C.] section 311 and any response filed under [35 U.S.C.] section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). “When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a) (2023).

For the reasons set forth below, upon considering the briefing and the evidence of record, we determine that the information presented in the Petition does not establish a reasonable likelihood that Petitioner will prevail with respect to any of the challenged claims. Accordingly, we do not institute *inter partes* review.

B. *Real Parties-in-Interest*

Petitioner identifies Innoscence America, Inc.; Innoscence (Zhuhai) Technology Company, Ltd.; and Innoscence (Suzhou) Technology Holding Company, Ltd. as the real parties-in-interest. Pet. 113. Patent Owner

identifies Infineon Technologies Austria AG as the real party-in-interest.
Paper 4, 1.

C. Related Matters

The parties identify the following related court proceeding: *Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Co.*, Case No. 4:24-cv-01553 (N.D. Cal.). Pet. 113; Paper 4, 1.

D. The '481 Patent

The '481 patent is titled “Electronic Component and Switch Circuit” and issued on February 20, 2018. Ex. 1001, codes (45), (54).

According to the '481 patent, “[a]n electronic component may include one or more semiconductor devices in a package,” which “includes internal electrical connections from the semiconductor device to a substrate or a leadframe which includes outer contacts.” *Id.* at 1:6–10. At the time of the '481 patent, most “transistors used in power electronic applications [were] typically . . . fabricated with silicon (Si) semiconductor materials,” but “compound semiconductor devices such as silicon carbide (SiC) power devices and Group III-N semiconductor devices, such as gallium nitride (GaN) devices” were starting to “be[] considered.” *Id.* at 1:17–25. The more recent SiC and GaN devices were, at the time, “emerging as attractive candidates to carry large currents, support high voltages and to provide very low on-resistance and fast switching times,” with some of these characteristics “result[ing] in additional challenges for package development.” *Id.* at 1:25–29. For example, the '481 patent describes “high switching speeds” as causing “a voltage drop across a parasitic source inductance which is sufficiently high to counteract the driving voltage which may result in increased energy loss.” *Id.* at 5:39–43. The '481 patent seeks

to solve this problem by implementing “source sense functionality . . . to exclude the parasitic source inductance from the driver circuit.” *Id.* at 5:50–53. It accomplishes this by including a “separate connection to the source” in the form of a connection “separate from the connection between the source pad . . . and the die pad.” *Id.* at 5:43–49.

E. Illustrative Claim

Petitioner challenges claims 1–17 of the ’481 patent. Claims 1, 10, and 17 are independent. Claim 1 is illustrative; it is reproduced below.

1. An electronic component, comprising:
 - a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;
 - a die pad; and
 - a first lead, a second lead and a third lead,wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,
wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,
wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad,
wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

Ex. 1001, 15:50–16:2.

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 3, 10–111):

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1–3, 5, 6, 10, 11, 16	103	Nega, ² Roberts ³
4, 9, 17	103	Nega, Roberts, Otremba124 ⁴
4, 7, 8, 17	103	Nega, Roberts, Otremba433 ⁵
7, 8	103	Nega, Roberts, Otremba433, Otremba280 ⁶
12, 13	103	Nega, Roberts, Otremba631
14, 15	103	Nega, Roberts, Otremba280
1, 2, 4–6	103	Liu ⁷
3, 17	103	Liu, Roberts
4, 9	103	Liu, Otremba433
4, 9	103	Liu, Otremba124
7, 8	103	Liu, Otremba433, Otremba280
17	103	Liu, Roberts, Otremba433

In support of its unpatentability arguments, Petitioner relies on the declaration of Michael Lebby, Ph.D. (Ex. 1003).

¹ Amendments to 35 U.S.C. § 103 enacted by the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”) took effect in March 2013. The ’481 patent issued from an application filed in January 2016. *See* Ex. 1001, code (22). Therefore, we apply the post-AIA version of § 103.

² US 2014/0110760 A1, published Apr. 24, 2014 (Ex. 1005).

³ US 2014/0175454 A1, published June 26, 2014 (Ex. 1006).

⁴ US 2014/0225124 A1, published Aug. 14, 2014 (Ex. 1007).

⁵ US 2014/0084433 A1, published Mar. 27, 2014 (Ex. 1008).

⁶ US 7,880,280 B2, issued Feb. 1, 2011 (Ex. 1009).

⁷ US 10,930,524 B2, issued Feb. 23, 2021 (Ex. 1010).

II. ANALYSIS

A. *Legal Standards*

In *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 (1966), the Supreme Court set out a framework for assessing obviousness under 35 U.S.C. § 103 that requires consideration of four factors: (1) the “level of ordinary skill in the pertinent art,” (2) the “scope and content of the prior art,” (3) the “differences between the prior art and the claims at issue,” and (4) if in evidence, “secondary considerations” of non-obviousness, such as “commercial success, long-felt but unsolved needs, failure of others, etc.” *Id.* at 17–18. “While the sequence of these questions might be reordered in any particular case,” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 407 (2007), the U.S. Court of Appeals for the Federal Circuit has repeatedly emphasized that “it is error to reach a conclusion of obviousness until all those factors are considered,” *WBIP, LLC v. Kohler Co.*, 829 F.3d 1317, 1328 (Fed. Cir. 2016). Because Patent Owner does not address objective evidence of non-obviousness, we focus solely on the first three *Graham* factors.

B. *Level of Ordinary Skill in the Art*

The level of ordinary skill in the pertinent art at the time of the invention is a factor in how we construe patent claims. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc). It is also one of the factors we consider when determining whether a patent claim is obvious over the prior art. *See Graham*, 383 U.S. at 17–18.

Factors pertinent to a determination of the level of ordinary skill in the art include “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity

with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). “Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case.” *Id.*

Petitioner contends that one of ordinary skill in the art “would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design.” Pet. 1. Petitioner also asserts that “[a]dditional education could substitute for professional experience and vice versa.” *Id.* On the present record, Patent Owner does not dispute this proposed level of skill. Prelim. Resp. 1–78. Neither party explains why the outcome of this case would be affected by the adoption of any of the proffered definitions of a person of ordinary skill in the art.

For purposes of this Decision, we adopt Petitioner’s assessment of the level of ordinary skill in the art, as it appears consistent with the ’481 patent and the asserted prior art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

We apply the same claim construction standard used in the federal courts—in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips*. *See* 37 C.F.R. § 42.100(b). Under the *Phillips* standard, the “words of a claim ‘are generally given their ordinary and

customary meaning,” which “is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1312–13.

On the present record, neither party proposes any claim terms for construction. Pet. 3; Prelim. Resp. 1–78. As discussed below, we are able to determine whether to institute review without resolving the construction of any claim terms. Accordingly, we need not and do not construe any terms expressly. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Asserted Obviousness Based on Nega

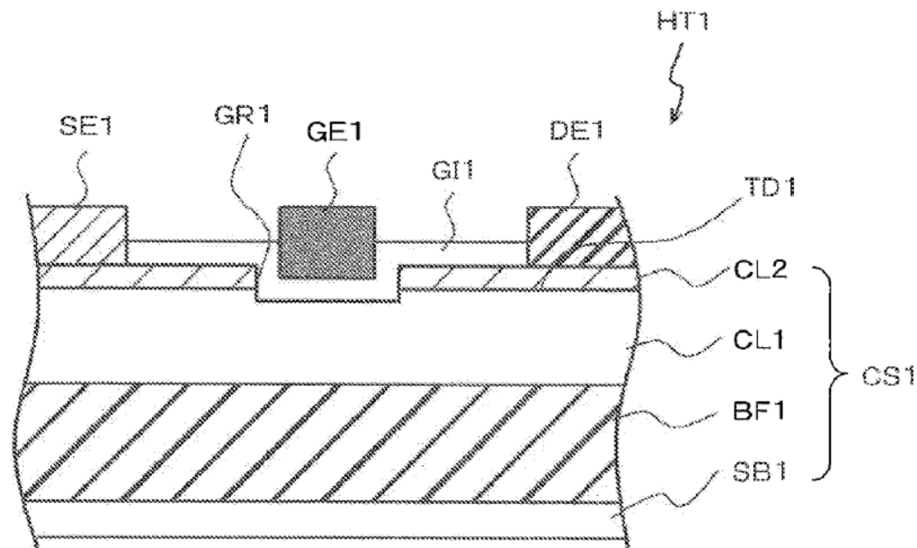
Petitioner argues that claims 1–3, 5, 6, 10, 11, and 16 would have been obvious over the combination of Nega and Roberts; that claims 4, 9, and 17 would have been obvious over the combination of Nega, Roberts, and Otremba124; that claims 4, 7, 8, and 17 would have been obvious over the combination of Nega, Roberts, and Otremba433; that claims 7 and 8 would have been obvious over the combination of Nega, Roberts, Otremba433, and Otremba280; that claims 12 and 13 would have been obvious over the combination of Nega, Roberts, and Otremba631; and that claims 14 and 15 would have been obvious over the combination of Nega, Roberts, and Otremba280. Pet. 3, 10–82. Patent Owner disagrees. Prelim. Resp. 23–55. Based on the current record, we are not persuaded that

Petitioner has established a reasonable likelihood of prevailing on these asserted obviousness grounds with respect to any claim.

1. *Overview of Nega*

Nega is a U.S. patent application titled “Semiconductor Device.” Ex. 1005, code (54). It “relates to a semiconductor device, and relates to, for example, a technique applicable to a semiconductor device having a DC/DC converter circuit.” *Id.* ¶ 3. Figure 2 of Nega is reproduced below.

FIG. 2



Id. at Fig. 2. Figure 2 “is a cross-sectional view illustrating a configuration of a high-side transistor.” *Id.* ¶ 16. In Figure 2, “the transistor HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1.” *Id.* ¶ 46. “The transistor HT1 has a recess gate structure” in which “[a]t least a portion of the gate electrode GE1 is located within the gate recess GR1.” *Id.* ¶ 51. “The transistor HT1 includes a gate insulating film GI1 provided on the compound semiconductor layer CL2.” *Id.* ¶ 53.

2. *Analysis of Claim 1*

a) *Disputed Limitation: “Wherein the Compound Semiconductor Transistor Device is a Lateral Transistor Device”*

Claim 1 recites “wherein the compound semiconductor transistor device is a lateral transistor device.” Ex. 1001, 15:64–65. Petitioner contends that Nega teaches or suggests this limitation. Pet. 24–25. Patent Owner disagrees. Prelim. Resp. 45–54.

Petitioner notes that “[t]he ’481 patent explains that ‘lateral’ means ‘run[ning] generally parallel to the lateral extent of a semiconductor material or semiconductor carrier’” and that “[t]he ’481 patent . . . describes a device that ‘has a lateral drift path.’” Pet. 24 (quoting Ex. 1001, 3:14–18, 4:37–38). Patent Owner directs us to a statement in the prosecution history that “[a] lateral transistor is a transistor in which current flows across ‘in the direction parallel to’ the device surface,” as opposed to “a vertical transistor,” in which “[c]urrent ‘flows in the direction normal to’ the device surface.” Prelim. Resp. 8 (quoting Ex. 1002, 33–34). Thus, the parties generally agree that a lateral transistor is a transistor in which current flows in a direction parallel to the surface of the transistor.

Petitioner argues that Nega teaches or suggests a transistor in which current flows parallel to the surface because Nega’s source, gate, and drain electrodes “are spread laterally in a lateral drift path, instead of vertically stacked.” Pet. 24–25 (citing Ex. 1005, Fig. 2). Patent Owner argues to the contrary that the placement of source, gate, and drain electrodes in the same lateral plane, rather than in a vertical stack, does not necessarily indicate that the current flow within the transistor is parallel to the surface. Prelim. Resp. 47–48 (citing Ex. 2002, 7–8, Figs. 1.7a, 1.7c). According to Patent Owner, transistors with electrodes in the same horizontal plane can have

either lateral or vertical current flow. *Id.* Thus, Patent Owner argues, the lateral placement of the source, gate, and drain electrodes in Nega does not mean that Nega teaches or suggests a lateral transistor.

On the present record, we agree with Patent Owner that Petitioner has not shown sufficiently that Nega teaches a transistor in which current flows in a direction parallel to the surface, rather than in a direction normal to the surface. Transistors with current flow in either direction can have electrodes located on a common horizontal plane, with the direction of the current flow depending on the configuration of doped semiconductor regions located below the electrodes. Ex. 2002, Figs. 1.7a, 1.7c. Because Petitioner relies on the location of Nega's electrodes, rather than on any particular configuration of doped semiconductor regions in Nega, Petitioner does not show sufficiently that Nega teaches a lateral transistor.

b) Conclusion Regarding Claim 1

Based on the current record, we determine that Petitioner has not shown that there is a reasonable likelihood that Petitioner will prevail in demonstrating that claim 1 is unpatentable as obvious in view of the combination of Nega and Roberts.

3. Claims 10 and 17

Petitioner argues that independent claim 10 would have been obvious over the combination of Nega and Roberts; and that independent claim 17 would have been obvious over the combination of Nega, Roberts, and Otremba124 and the combination of Nega, Roberts, and Otremba433. Pet. 34–40, 49–52, 62–64. Claims 10 and 17 include a limitation similar to the “lateral transistor” limitation of claim 1, with both of these limitations requiring that a particular recited transistor be a lateral transistor. Ex. 1001,

16:49–50, 18:11–12. As with claim 1, Petitioner relies on Nega to teach or suggest these “lateral transistor” limitations. Pet. 40, 51–52, 63–64. As discussed above with respect to claim 1, however, Petitioner has not shown sufficiently that Nega teaches or suggests a lateral transistor. Accordingly, Petitioner has not shown that there is a reasonable likelihood that Petitioner will prevail in demonstrating that claims 10 and 17 are unpatentable as obvious on any of the asserted grounds that challenge those claims.

4. Claims 2–9 and 11–16

Petitioner argues that claims 2, 3, 5, 6, 11, and 16 would have been obvious over the combination of Nega and Roberts; that claims 4 and 9 would have been obvious over the combination of Nega, Roberts, and Otremba124; that claims 4, 7, and 8 would have been obvious over the combination of Nega, Roberts, and Otremba433; that claims 7 and 8 would have been obvious over the combination of Nega, Roberts, Otremba433, and Otremba280; that claims 12 and 13 would have been obvious over the combination of Nega, Roberts, and Otremba631; and that claims 14 and 15 would have been obvious over the combination of Nega, Roberts, and Otremba280. Pet. 3, 27–34, 40–49, 52–62, 64–82. Claims 2–9 “incorporate by reference all the limitations of” claim 1, and claims 11–16 incorporate the limitations of claim 10, because each of these claims depends from claim 1 or claim 10, respectively. 35 U.S.C. § 112(d) (2023); Ex. 1001, 16:3–32, 16:54–17:10. Petitioner relies on its arguments with respect to claims 1 and 10 in arguing that claims 2–9 and 11–16 would have been obvious. Pet. 3, 27–34, 40–49, 52–62, 64–82. In particular, Petitioner relies on the portions of its arguments for claims 1 and 10 that argue that Nega teaches or suggests a lateral transistor. *Id.* As discussed above, however, Petitioner has not

shown sufficiently that Nega teaches or suggests every limitation of claims 1 or 10. Accordingly, Petitioner has not shown that there is a reasonable likelihood that Petitioner will prevail in demonstrating that any of claims 2–9 and 11–16 is unpatentable as obvious on any Nega-based asserted ground that challenges those claims.

E. Asserted Obviousness Based on Liu

Petitioner argues that claims 1, 2, and 4–6 would have been obvious over Liu; that claims 3 and 17 would have been obvious over the combination of Liu and Roberts; that claims 4 and 9 would have been obvious over the combination of Liu and Otremba433; that claims 4 and 9 would have been obvious over the combination of Liu and Otremba124; that claims 7 and 8 would have been obvious over the combination of Liu, Otremba433, and Otremba280; and that claim 17 would have been obvious over the combination of Liu, Roberts, and Otremba433. Pet. 3, 82–111. Patent Owner disagrees. Prelim. Resp. 55–78.

1. Overview of Liu

Liu is a U.S. patent titled “Semiconductor Component and Method of Manufacture.” Ex. 1010, code (54). It “relates, in general, to electronics and, more particularly, to semiconductor structures thereof, and methods of forming semiconductor devices.” *Id.* at 1:18–20. Figure 11 of Liu is reproduced below.



Id. at Fig. 11. Figure 11 “is a perspective view of a semiconductor component in a cascode configuration.” *Id.* at 2:18–19. In Figure 11, “semiconductor chip 40B is bonded to surface 138A of device receiving area 138.” *Id.* at 8:11–12. Semiconductor chip 40B has “[d]rain contact 50B,” “source contact 52B,” and “gate contact” 54B. *Id.* at 8:27–33.

2. Analysis of Claim 1

a) *Disputed Limitation: “Wherein the Compound Semiconductor Transistor Device is a Lateral Transistor Device”*

Claim 1 recites “wherein the compound semiconductor transistor device is a lateral transistor device.” Ex. 1001, 15:64–65. Petitioner contends that Liu teaches or suggests this limitation. Pet. 91–93. Patent Owner disagrees. Prelim. Resp. 55–77.

As discussed above with respect to the Nega grounds, the parties generally agree that a lateral transistor is a transistor in which current flows in a direction parallel to the surface of the transistor. Petitioner argues that

Liu teaches or suggests a transistor in which current flows parallel to the surface because Liu's source, gate, and drain electrodes "are spread laterally across the semiconductor material creating a lateral drift path, as opposed to a vertical configuration." Pet. 91–93 (citing Ex. 1010, Figs. 11–12; Ex. 1011, Figs. 11–12). Patent Owner argues to the contrary that the placement of source, gate, and drain electrodes in the same lateral plane, rather than in a vertical stack, does not necessarily indicate that the current flow within the transistor is parallel to the surface. Prelim. Resp. 63–65 (citing Ex. 2002, 7–8, Figs. 1.7a, 1.7c; Ex. 2003, 1937, Fig. 3(a)). According to Patent Owner, transistors with electrodes in the same horizontal plane can have either lateral or vertical current flow. *Id.* Thus, Patent Owner argues, the lateral placement of the source, gate, and drain electrodes in Liu does not mean that Liu teaches or suggests a lateral transistor.

On the present record, we agree with Patent Owner that Petitioner has not shown sufficiently that Liu teaches a transistor in which current flows in a direction parallel to the surface, rather than in a direction normal to the surface. Transistors with current flow in either direction can have electrodes located on a common horizontal plane, with the direction of the current flow depending on the configuration of doped semiconductor regions located below the electrodes. Ex. 2002, Figs. 1.7a, 1.7c. Because Petitioner relies on the location of Liu's electrodes, rather than on any particular

configuration of doped semiconductor regions in Liu, Petitioner does not show sufficiently that Liu teaches a lateral transistor.⁸

b) Conclusion Regarding Claim 1

Based on the current record, we determine that Petitioner has not shown that there is a reasonable likelihood that Petitioner will prevail in demonstrating that claim 1 is unpatentable as obvious in view of Liu.

3. Claims 2–9

Petitioner argues that claims 2 and 4–6 would have been obvious over Liu; that claim 3 would have been obvious over the combination of Liu and Roberts; that claims 4 and 9 would have been obvious over the combination of Liu and Otremba433; that claims 4 and 9 would have been obvious over the combination of Liu and Otremba124; and that claims 7 and 8 would have been obvious over the combination of Liu, Otremba433, and Otremba280.

⁸ Moreover, we note that Petitioner’s conjectured current flow in Liu is horizontally from the gate electrode, across the source electrode, toward the drain electrode. Pet. 92–93 (replicating figures 11 and 12 from Liu with Petitioner’s annotations). At least on the present record, this seems to be contrary to the operation of transistor devices. Rather than current flowing from the gate electrode to the drain electrode, in a metal oxide semiconductor field effect transistor, “[v]oltage applied to the gate controls the current flow between underlying semiconductor regions by either creating or eliminating a conducting channel.” Ex. 2001, 63; *see also* Ex. 2002, Figs. 1a–1c (depicting current flow from source to drain across gate). Thus, it seems on the present record that Liu’s device is more likely to be constructed similarly to the HV DMOSFET of Exhibit 2003, in which the source electrode is placed horizontally between the gate and drain electrodes, and in which the current flow is primarily downward from the source electrode to the buried N⁺ layer that is connected to the drain electrode, rather than parallel to the surface of the transistor. Ex. 2003, 1937, Fig. 3(a). For this additional reason, we are not persuaded that Petitioner sufficiently shows that Liu teaches or suggests a lateral transistor.

Pet. 3, 95–99, 101–109. Claims 2–9 “incorporate by reference all the limitations of” claim 1, because each of these claims depends from claim 1. 35 U.S.C. § 112(d) (2023); Ex. 1001, 16:3–32. Petitioner relies on its arguments with respect to claim 1 in arguing that claims 2–9 would have been obvious. Pet. 3, 95–99, 101–109. In particular, Petitioner relies on the portions of its arguments for claim 1 that argue that Liu teaches or suggests a lateral transistor. *Id.* As discussed above, however, Petitioner has not shown sufficiently that Liu teaches or suggests the recited lateral transistor. Accordingly, Petitioner has not shown that there is a reasonable likelihood that Petitioner will prevail in demonstrating that any of claims 2–9 is unpatentable as obvious on any Liu-based asserted ground that challenges those claims.

4. *Claim 17*

Petitioner argues that claim 17 would have been obvious over the combination of Liu and Roberts and that claim 17 would have been obvious over the combination of Liu, Roberts, and Otremba433. Pet. 100–101, 109–111. Claim 17 recites a limitation similar to the “lateral transistor” limitation of claim 1, requiring that a recited transistor be a lateral transistor. Ex. 1001, 18:11–12. As with claim 1, Petitioner relies on Liu to teach or suggest this “lateral transistor” limitation. Pet. 40, 51–52, 63–64. As discussed above with respect to claim 1, however, Petitioner has not shown sufficiently that Liu teaches or suggests a lateral transistor. Accordingly, Petitioner has not shown that there is a reasonable likelihood that Petitioner will prevail in demonstrating that claim 17 is unpatentable as obvious on any of the asserted grounds that challenge that claim.

III. CONCLUSION

For the reasons set forth above, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing with respect to any challenged claim of the '481 patent. Accordingly, we do not institute *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314, the Petition is denied, and no *inter partes* review is instituted.

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