

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

IPR2024-00975
U.S. Patent 9,899,481

PETITIONER'S REQUEST FOR REHEARING

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Pursuant to 37 C.F.R. § 42.71(d), Petitioner Innoscience America, Inc. (“Innoscience”) respectfully requests that the Patent Trial and Appeal Board (“Board”) reconsider its decision denying institution of *inter partes* review (“IPR”) of U.S. Patent No. 9,899,481 (“the ’481 patent”) due to an exceptional situation, where Patent Owner misrepresented the patent, its prosecution history, *and* the prior art, which caused the Board to erroneously deny institution.

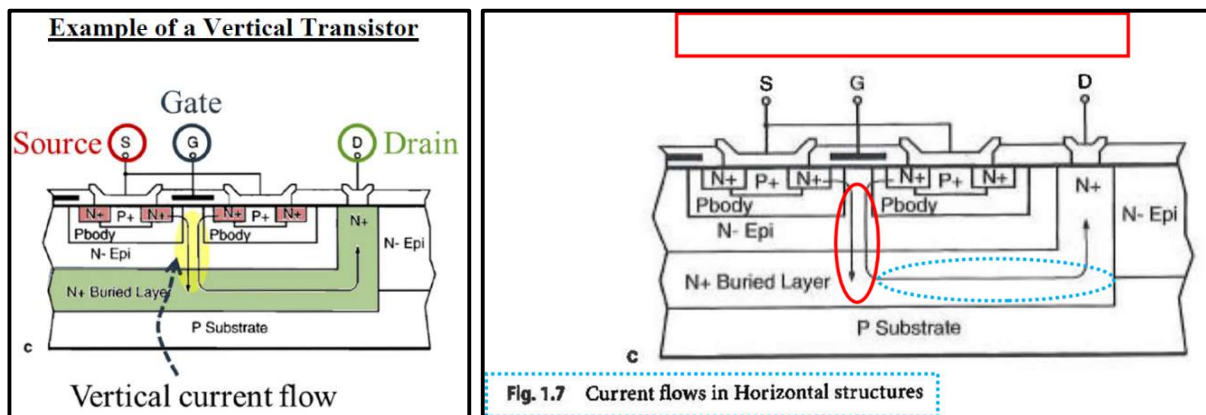
I. INFINEON MISREPRESENTED AND DOCTORED EVIDENCE

The Board based its decision denying institution on whether Petitioner’s prior-art combinations rendered obvious the “lateral transistor” limitation in claim 1 of the ’481 patent. Whether a transistor is defined as “lateral” or “vertical” depends on the location of the electrodes. Ex. 1001, 5:54-6:7. Indeed, when applying for its patent, Patent Owner Infineon Technologies Austria AG (“Infineon”) ***disclaimed “vertical” transistors by partially defining them based on the electrode locations.*** See Ex. 1002, pp. 31-32. But when addressing this prosecution history in these IPR proceedings, Infineon ***clipped its admissions about electrode placement*** and argued that only current flow can dictate whether a transistor is defined as “lateral” or “vertical.” Paper 6, pp. 8-10, 21-23, 47-48.

After this about face, Infineon then ***doctored prior-art evidence.*** In particular, it argued that Petitioner’s prior-art designs were distinguishable because they were not lateral transistor designs. Infineon presented a state-of-the-art reference

(“Murari”) disclosing a transistor structure with mixed current flows (i.e., parallel and perpendicular) similar to the transistor structure described in Petitioner's prior art. Infineon argued that Murari's disclosures undermined Petitioner's obviousness case—*but Infineon doctored the most material figure in Murari in arguing this.*

In particular, Figure 1.7c of Murari is captioned “Current flows in Horizontal Structures.” Ex. 2002 at Fig 1.7c. Infineon *removed this caption* and *replaced it with the following made up caption: “Example of a Vertical Transistor.”* Moreover, Infineon annotated the transistor structure shown in Figure 1.7c to suggest that the figure only discloses **perpendicular current** flow and not **parallel current flow**:



Paper 6, at 8-10; Ex. 2002, Figure 1.7c (annotated). The image on the left was presented by Infineon, and the image on the right is the actual image from Murari, with the exception of the blue/red annotations that Petitioner presents now to show the doctoring. The blue annotations illustrate what was hidden by Infineon, and the red annotations show Infineon's misrepresentations. At bottom, Infineon tried to

rewrite a transistor reference to suggest that the presence of vertical current flow makes a transistor a vertical transistor, and that Petitioner's prior-art designs are not lateral transistors because they have vertical current flows.

When the record is viewed accurately, however, and not through the lens of the doctored evidence, it becomes clear that the lateral transistor in claim 1 can have both lateral and vertical current flows—as Murari and Petitioner's obviousness combinations show. Moreover, as Infineon's clipped prosecution history admissions prove, whether a transistor is defined as lateral or vertical depends largely on electrode placement. It is clear from the decision denying institution that Infineon's misrepresentations, omissions, and doctored evidence caused the Board to misapprehend the record. In fact, the Board relied on these very misrepresentations in its analysis. Paper 7 at 10, 15. But for Infineon's egregious conduct, the Board would have instituted. Rehearing should be granted to correct the Board's errors.

II. LEGAL BASIS: MISAPPREHENSION BY MISREPRESENTATION

A party may request rehearing not to institute a trial. 37 C.F.R. § 42.71(d). A request for rehearing “must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply.” 37 C.F.R. § 42.71(d).

III. INFINEON'S MISREPRESENTATIONS AND OMISSIONS CAUSED THE BOARD TO MISAPPREHEND THE RECORD

A. Infineon Mischaracterized the '481 Patent—Electrode Location Helps Define Whether a Transistor Is Vertical or Lateral

Infineon argued that the lateral transistors are defined solely by current flow direction and not by electrode location. Paper 6, pp. 47-48. This contradicts the '481 patent. The patent *explicitly states* that the “lateral” and “vertical” transistors are defined by the location of the electrodes. Ex. 1001, 5:54-6:7. In fact, the only enabling descriptions of “lateral” and “vertical” transistors in the '481 patent limit the structures to specific electrode placements. The patent states that, in a lateral device, the electrodes “**are arranged on the upper surface [] of the compound semiconductor transistor device []**.” Ex. 1001, 5:54-63 (emphasis added); *see also id.*, 4:37-42; 9:2-7. And, for vertical devices, “one of the current electrodes is arranged on [the] lower surface of the body of the compound semiconductor transistor device and the other current electrode and control electrode are arranged on the opposing surface.” Ex. 1001, 5:63-6:7.

Infineon knew electrode location mattered when defining transistor types. During prosecution of the patent, Infineon expressly disclaimed “vertical” transistors *by distinguishing electrode location designs in the cited prior art*. *See* Ex. 1002, pp. 31-32. For example, Infineon argued during prosecution that a prior-art reference

failed to teach a lateral transistor and instead taught a vertical transistor because the transistor had “current electrodes on opposing surfaces.” Ex. 1002, p. 32.

When addressing the “lateral” and “vertical” transistor issue in its Preliminary Response, Infineon clipped the prosecution disclaimer admissions it made on electrode location and instead presented cherrypicked prosecution statements on transistor current flow. Paper 6, pp. 8-10, 21-23, 47-48. There can be no question that Infineon's prosecution disclaimer on electrode location should have impacted how the lateral transistor term was construed. But because Infineon shielded the Board from this disclaimer, the Board did not properly address it. The prosecution history confirms that the transistors must have specific plane electrode placements. To help correct the record, Petitioner compares in the table below certain Infineon statements with what the evidence actually shows:

Infineon's Representation	Contradictory Citation
“A lateral transistor cannot be identified by the placement of the transistor's electrodes.” Infineon POPR (Paper 6, pp. 47-48)	<i>“In a lateral device, the ... electrode[s] are arranged on the upper surface</i> 32 of the compound semiconductor transistor device 21.” The '481 patent (Ex. 1001, 5:56-60)
“[A]ll the electrodes being ‘arranged laterally’ on one side of the substrate does not . . . mean a transistor is a lateral transistor,” and “[i]ndeed, vertical transistors were known in which all the electrodes were ‘arranged laterally’ on one side of the substrate.” Infineon POPR (Paper 6, pp. 46-48, 62)	“[A] vertical device . . . in which case one of the current electrodes is <i>arranged on lower surface of the body</i> of the compound semiconductor transistor and the other current electrode and control electrode <i>are arranged on the opposing surface</i> of the compound semiconductor transistor device.”

	The '481 patent (Ex. 1001, 5:65-6:6)
"The Applicant [Infineon] argued that Otremba '284 and Otremba '313 disclosed vertical transistor devices, not a lateral transistor device, as required by the amended claims." Infineon POPR (Paper 6, p. 22)	"However, Otremba '284 fails to teach at least the feature of a lateral transistor device as recited in amended claim 1. Otremba '284 teaches a vertical transistor which <i>includes current electrodes on opposing surfaces.</i> " Prosecution History (Ex. 1002, p. 32)

The Board relied on Infineon's prosecution arguments—*which omitted the electrode location disclaimer*—to incorrectly conclude that the transistors were not tethered to specific electrode placements. Paper 7, pp. 10-11, 14-15. Instead, the Board erroneously based its construction entirely on the current flow in the transistor. Paper 7, pp. 10-11. Rehearing is necessary to correct this error.

B. Infineon Mischaracterized the '481 Patent's Disclosures on Current Flow

Infineon argued in this IPR proceeding that current flow described in the '481 patent flows *exclusively* parallel to the surface in "lateral" transistors and *exclusively* perpendicular to the surface in "vertical" transistors. Paper 6, pp. 8-10. The patent, however, expressly states that "lateral" "should be understood to mean a direction or extent that runs *generally parallel* to the lateral extent of a semiconductor material," and that "vertical" should be "understood to mean a direction that runs *generally perpendicular* to these surfaces or sides." Ex. 1001, 3:13-25 (emphasis added). In other words, lateral drift path has a current that flows generally, but not

exclusively, parallel to the surface; and vertical drift path has a current that flows generally, but not exclusively, perpendicular to the surface.

In its Preliminary Response, Infineon not only omitted “generally” from its description of current flow—it implicitly added an exclusive qualifier. Paper 6, pp. 8-10, 21-23. Infineon pointed to prosecution history to argue that “lateral” transistors and “vertical” transistors are mutually exclusive. Paper 6, pp. 8-10, 21-23 (referencing Ex. 1002, pp. 32-33). That is, the current in “lateral” transistors can only flow parallel to the surface, and the current in “vertical” transistors can only flow perpendicular to the surface. *Id.* The Board incorrectly adopted this construction. Paper 7, pp. 10-11, 14-15. The construction is incorrect because the current in both lateral or vertical transistors may be mixed, meaning that the current in each type of transistor can flow parallel **and** perpendicular. *See generally* Paper 6; *see also infra* Section III.C. More specifically, in “lateral” transistors, with all the electrodes arranged on a common surface, the current *generally* flows parallel to the surface (despite possible perpendicular flow), and in “vertical” transistors, with the electrodes arranged on opposite surfaces, the current *generally* flows perpendicular (despite possible parallel flow).

The Board, relying on Infineon's arguments that implicitly inject an “exclusive” qualifier into the flow direction analysis, incorrectly concluded that “a lateral transistor is a transistor in which current flows in a direction parallel to the

surface of the transistor,” only. Paper 7, pp. 10, 14-15. Infineon's position tainted the Board's understanding of prior art transistors, with both lateral and vertical current flows (i.e., applying exclusive lateral and vertical flows). *See infra* Section III.C. The Board strictly applied this construction, without considering the proper “generally” current flow construction, or devices with *both* parallel and perpendicular current flows. Paper 7, pp. 10, 14-15. Because this conclusion contradicts the '481 patent, it should be reconsidered.

C. Infineon's Mischaracterized Prior Art References

1. Infineon's Material Misrepresentations of the POPR Prior Art

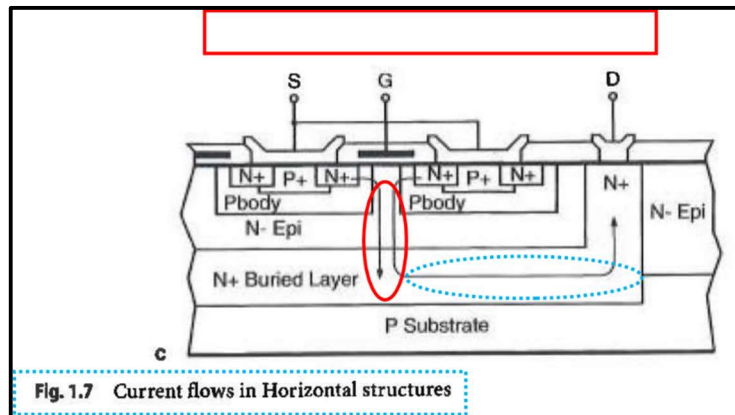
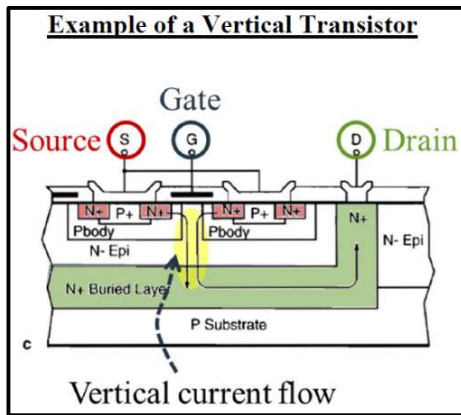
Infineon also misrepresented the prior art to the Board. Infineon identified Murari and Baliga as prior art transistors, concluding—without supporting expert opinions—that these devices were examples of transistors with electrodes arranged laterally on a common horizontal plane but that they nevertheless were vertical transistors solely because of *some* perpendicular current flow. Paper 6, pp. 8-10, 46-48, 62. Infineon's position was inconsistent with the art and a misrepresentation.

Infineon mischaracterized these references by concealing inconsistent teachings in them and even altered the evidence. Murari and Baliga **do not teach vertical transistors** with electrodes arranged laterally on one side of the substrate (as understood within the context of the '481 patent). These two references **instead**

teach *lateral transistors* with electrodes arranged laterally on one side and current flowing *generally* parallel to that surface.

Regarding the altered evidence, Infineon relied on Murari's Figure 1.7c as allegedly teaching a vertical transistor with electrodes arranged laterally on the same surface and with current flowing vertically. Paper 6, pp. 8-10 (citing Ex. 2002, 7-8). Infineon, however, omitted words and teachings from the reference ***that show the Murari transistor was actually a lateral transistor***. Even though Figure 1.7c expressly defines its transistor as a "horizontal" transistor (i.e., a "lateral" transistor), Infineon argued that the transistor in Figure 1.7c was a vertical transistor because "when a voltage is applied at the gate, the current flows vertically between the source region and the drain region, normal to the surface of the device." *Id.*

Contrary to Infineon's argument that the Figure 1.7c shows a *vertical* transistor because it had perpendicular current flow, the current in Figure 1.7c's transistor ***actually*** flows in *both* directions. Even more, the current *generally* flows ***laterally***, but Infineon masked this issue by doctoring the figure to: (1) **remove the actual Fig. 1.7c caption** ("Current flows in Horizontal structures") and **replace it with an erroneous and misleading caption** ("Example of a Vertical Transistor"); and (2) annotate only the **perpendicular current** flow while omitting annotations for the **parallel flow**:



(Left) Paper 6, pp. 8-10 (Infineon's annotations of Figure 1.7c of Ex. 2002, 7-8);
(Right) Figure 1.7c of Ex. 2002, 7-8 (annotated).

Indeed, when properly annotated (below), the Murari Fig. 1.7c transistor satisfies the '481 patent criteria for a “**lateral**” transistor—electrodes arranged on a common planar surface, and current *generally* flowing parallel to the surface.

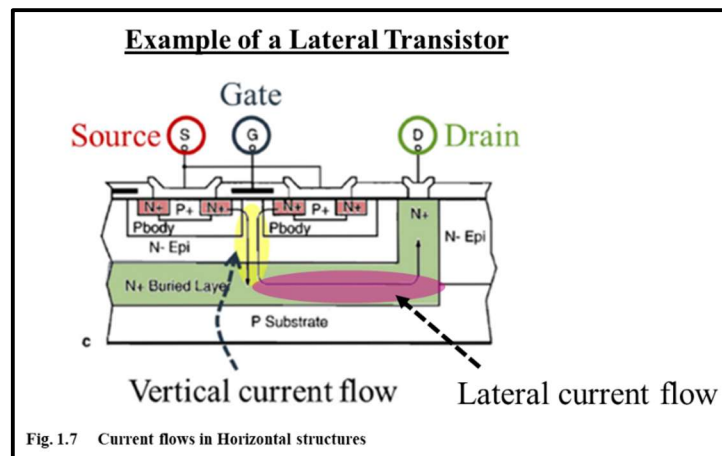


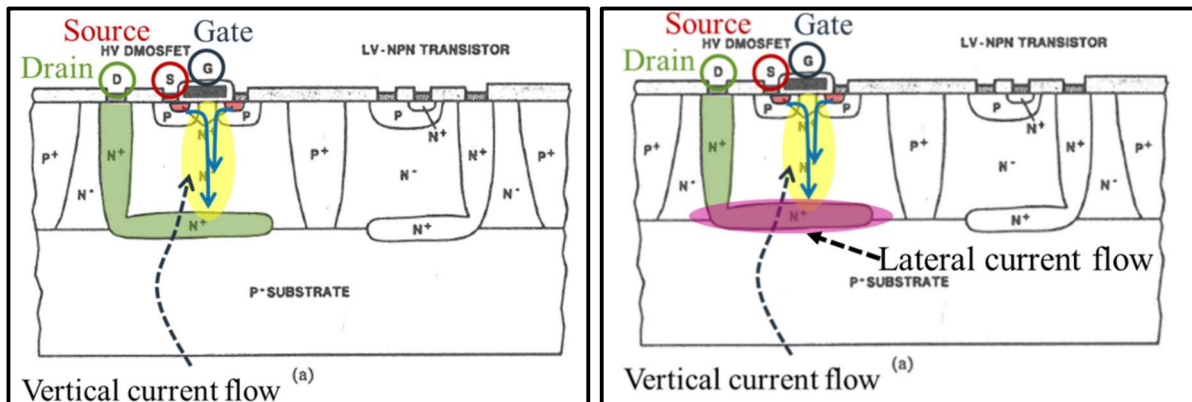
Figure 1.7c of Ex. 2002, 7-8 (annotated). By doctoring Figure 1.7c, Infineon presented a false and misleading position to the Board, which provoked the Board to erroneously deny institution (as described below).

The parentheticals Infineon added to Figure 1.7c also omitted context showing that the transistor was a lateral transistor. Paper 6, pp. 8-10. Infineon quoted Murari's description of Figure 1.7c as follows: "current flow is vertical in the power device structure"—removing the lateral current flow context (and giving the false impression of an exclusive flow). *Id.* Infineon omitted the lateral current flow context from the full quote: "**[i]n mixed horizontal/vertical structures** the current flow is vertical in the power device structure **but the current is brought to the surface through buried layers and sinkers.**" Ex. 2002, pp. 7-8 (emphasis added). Of note, Murari also confirms that vertical transistors have current primarily flowing perpendicular to the surface with the electrodes located on opposite ends of the substrate. Ex. 2002, pp. 6-7 (describing Figure 1.6, "[i]n a vertical structure the current flows through the device from the top to the bottom.").

The Board, in relying on Infineon's materially doctored version of Figure 1.7c, incorrectly concluded that Nega and Liu did not necessarily teach the claimed "lateral" transistors as stated in the Petition. Paper 7, pp. 10-11, 14-15. The Board reached this conclusion because it relied on Infineon's false positions. Specifically, by focusing exclusively on the perpendicular current flow in Figure 1.7c, the Board determined that transistors with electrodes on the same surface—like Figure 1.7c, Nega, and Liu—were not necessarily "lateral" transistors. *Id.* (finding that "transistors with electrodes in the same horizontal plane" can be either lateral or

vertical transistors with respective parallel or perpendicular current flows). The Board further concluded that the “lateral placement of the source, gate, and drain electrodes” arranged along the same horizontal plane (like Nega and Liu) does not necessarily teach or suggest a lateral transistor. *Id.* The Board’s understanding was contradicted by the patent itself because the only definite and enabling description of “lateral” transistors (i.e., current generally flowing parallel) have all the electrodes located on a common horizontal plane.

Second, like Murari, Infineon likewise omitted teachings from the Baliga reference that were inconsistent with its conclusion. Paper 6, pp. 8-10 (citing Ex. 2003, 1937). For Figure 3(a) of Baliga, Infineon again omitted (left) the parallel current flows (annotated on right):

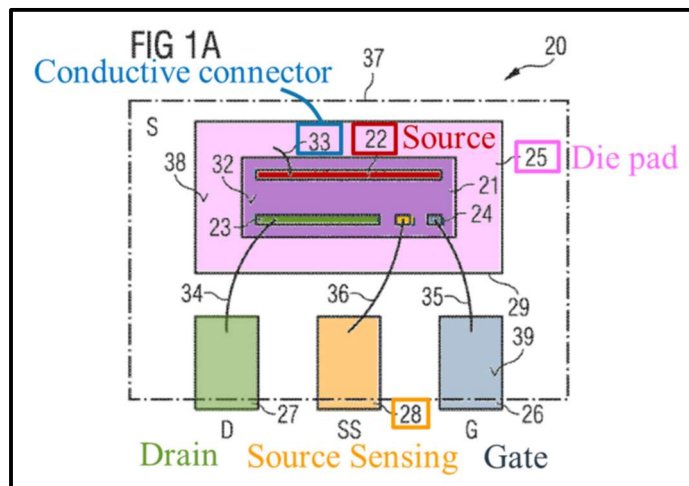


2. Infineon's Material Misrepresentations of the Petition Prior Art

As for prior art cited in the Petition, one ground in the Petition relied on the prior art reference Liu transistor as teaching the claimed “lateral” transistor element.

Paper 1, pp. 91-94. Infineon argued that the Liu transistor did not disclose a “lateral” transistor. Paper 6, pp. 60-66. Specifically, Infineon argued that even though all the electrodes were arranged on the same surface in Liu, because the gate electrode placement was not adjacent to the source and drain electrodes it was a “vertical,” not “lateral” transistor. Paper 6, pp. 60-66. The '481 patent, however, specifically discloses transistors with this electrode placement and defines them as “lateral” transistors. *See* Ex. 1001, 5:54-63.

The '481 patent does not require that a lateral transistor gate be located between the source and drain, because as noted above for the electrode placements (*see supra* Section III.A), the patent only requires that the electrodes be located on the same planar surface for lateral transistors. *See* Ex. 1001, 5:54-63. Indeed, Infineon even identified an exemplary embodiment of a lateral transistor from the '481 patent *without* the gate located between the source and drain (yet still on the same plane). Paper 6, p. 20 (referencing Fig. 1A of the patent and acknowledging that the patent “states that ‘[t]he compound semiconductor transistor device 21 is a lateral device.’”). The **gate 26** in Figure 1A of the patent is located adjacent to both sources, **source 22** and **source 28**, but *not* between **the drain 27** and a source:



See Paper 6, p. 20; see also Ex. 1001, 5:1-6.

For this additional reason, Infineon further misrepresented the teachings of the asserted prior-art combination. These misrepresentations tainted the Board’s understanding of the Petition’s prior art references and whether those references taught the claimed “lateral” and “vertical” transistors, which the Board ultimately incorrectly concluded that they did not. Paper 7, pp. 10-11, 14-15. The Board’s misunderstanding, however, is contradicted by the correct reading of the patent and the evidence, and the denial of institution should be reconsidered.

D. The Petition Identifies Prior Art Lateral Transistors Meeting the Challenged Claim Language as Written, and as Applied by the Applicant

The Petition's obviousness combinations based on Nega and Liu, especially when viewed in context with the disclosures in the '481 patent specification and Infineon's prosecution history admissions, teach each element of the challenged '481 patent claims. *See e.g.*, Paper 1, pp. 10-52. Nega and Liu both describe lateral

transistors with electrodes arranged laterally on a common horizontal plane with the current flowing generally laterally to the plane. *See id.*, pp. 24-25, 91-94. The '481 patent's lateral compound semiconductor device components and particular packaging layout were well known, and packaging a compound device in known designs, using conventional components was obvious.

Through this Request, Petitioner seeks reconsideration of the merits of the Petition unencumbered by Infineon's misrepresentations and the Decision's erroneous reliance on them. Given that the only deficiencies the Board identified in its Decision were rooted in Infineon's incorrect arguments and faulty evidence, reconsideration of the decision not to institute is warranted. And cancellation of all challenged claims is proper.

IV. CONCLUSION: REHEARING IS WARRANTED IN VIEW OF THE BOARD'S MISAPPREHENSION OF KEY PATENT TERMS

But for the misrepresentations and omissions by Infineon to the Board, the Board would have instituted the Petition. Because Infineon caused the Board to misapprehend the patent, the prosecution history, and the prior art, rehearing is necessary. Petitioner respectfully requests that the Board grant this request for rehearing and institute *inter partes* review.

Dated: January 10, 2025

/Lionel M. Lavenue/

Lionel M. Lavenue, Lead Counsel
Reg. No. 46,859

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on January 10, 2025, a copy of **PETITIONER'S REQUEST FOR REHEARING** was served upon the below-listed counsel by electronic mail:

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