

***ATTACHMENTS CONTAIN CONFIDENTIAL BUSINESS INFORMATION
SUBJECT TO PROTECTIVE ORDER***

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before the Honorable Bryan F. Moore
Administrative Law Judge**

In the Matter of

**CERTAIN SEMICONDUCTOR DEVICES,
AND PRODUCTS CONTAINING THE
SAME**

Inv. No. 337-TA-1414

RESPONDENTS' INVALIDITY CONTENTIONS

Respondents Innoscience (Suzhou) Technology Holding Company Ltd., Innoscience (Suzhou) Semiconductor Co., Ltd., Innoscience (Zhuhai) Technology Company, Ltd., and Innoscience America, Inc. (collectively "Innoscience" or "Respondents") provide these Invalidity Contentions to Complainants Infineon Technologies Americas Corporation and Infineon Technologies Austria AG ("Infineon" or "Complainants") in response to Infineon's Interrogatory Nos. 13-14. 19 C.F.R. §§ 210.27 and 210.29, Order Nos. 2 and 7.

I. PRELIMINARY STATEMENT AND RESERVATION OF RIGHTS

In its Complaint, Infineon alleges that Respondents infringe claims 1, 2-4, 6, 9 and 17 of U.S. Patent No. 9,899,481 ("the '481 patent"); claims 1, 2, 8-10, and 13-15¹ of U.S. Patent No. 8,686,562 ("the '562 patent"); claims 1, 2-4, 8, and 9 of U.S. Patent No. 9,070,755 ("the '755 patent"); and claims 1, 2, and 10 of U.S. Patent No. 8,264,003 ("the '003 patent") (collectively the "asserted claims" and "Asserted Patents"). Infineon also alleges that a technical domestic industry exists for each of the Asserted Patents.

¹ Complainants further identify claims 11 and 16 of the '562 patent for domestic industry.

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Respondents contend that each claim asserted by Infineon or relied on for domestic industry is invalid under at least 35 U.S.C. §§ 102, 103, and/or 112. Respondents expressly reserve the right to amend, correct, and/or supplement these Invalidity Contentions in accordance with Commission Rules and the Ground Rules and Procedural Schedule governing this Investigation. This includes, for example, the obligation under 19 C.F.R. § 210.27(c) to address any additional information that is located or otherwise becomes available.

These Invalidity Contentions are based, *inter alia*, on Infineon's apparent theories set out in the Complaint. Respondents reserve all rights to disclose new or supplemental invalidity contentions, including to address any changed theories of infringement and/or technical domestic industry and any newly discovered evidence obtained through continued discovery, both formal and informal.

Respondents do not provide any invalidity contentions directed to claims Infineon has not asserted for purposes of infringement or technical domestic industry. To the extent Infineon may be permitted to assert additional claims in the future, Respondents reserve all rights to disclose new or supplemental invalidity contentions regarding such claims.

Because the Administrative Law Judge has not yet construed any of the claims in this litigation, Respondents reserve the right to supplement these Invalidity Contentions after receiving any claim construction ruling.

Further, these Invalidity Contentions reflect Respondents' knowledge, investigation, and discovery as of the date of service. Respondents reserve the right to supplement these Invalidity Contentions as appropriate and for any permissible reason. For example, Respondents reserve the right to supplement these Invalidity Contentions if they become aware of additional prior art, become aware of additional features of the prior art references cited below, or become aware of

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any other relevant information gained through discovery, including non-party discovery, or otherwise. Respondents also reserve the right to modify or supplement their contentions based on any claim construction ruling.

II. INVALIDITY BASED ON ANTICIPATION AND OBVIOUSNESS (35 U.S.C. §§ 102 AND 103)

Respondents contend that all asserted claims of the Asserted Patents and all claims relied on for domestic industry are invalid because they are anticipated and/or rendered obvious under 35 U.S.C. §§ 102 and 103. To the extent Infineon contends that the limitations of these claims are not disclosed in the prior art identified as anticipatory, Respondents reserve the right to assert obviousness based on the identified references and/or to identify other references that would have rendered obvious the allegedly missing limitation. Further, the obviousness positions provided below and in the accompanying claim charts under 35 U.S.C. § 103 are exemplary only and are not intended to be exhaustive. To the extent that Infineon challenges the disclosure of any of these references with respect to particular limitations of the claims, Respondents reserve the right to supplement these Invalidity Contentions to assert additional or different bases for obviousness. Respondents reserve the right to use any combination of the references set forth in these contentions to render the claims obvious.

In the exemplary invalidity claim charts accompanying these Invalidity Contentions, Respondents identify specific portions of certain prior art references that disclose elements of the asserted claims and claims relied on for domestic industry. These specific portions and references, however, are not exhaustive. They are merely exemplary as to the teachings of particular prior art reference and how those teachings relate to certain elements of the asserted claims and claims relied on for domestic industry. For example, while Respondents have identified at least one citation per claim element for each prior art reference, each disclosure of that same element in that

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prior art reference is not necessarily identified. In addition, where Respondents identify an exemplary figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure as well as any text relating to the figure in the specification and prosecution history in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well.

It also should be recognized that a person of ordinary skill in the art would have generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would have relied upon other information, including other publications and general scientific or engineering knowledge.

Respondents therefore reserve the right to rely upon other unidentified or uncited portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions, as well as additional evidence that the prior art discloses a claim limitation or the alleged invention as a whole. Respondents also reserve the right to rely upon any portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including to establish the state of the art and to establish a basis for modifying or combining certain features in the prior art. Respondents also reserve the right to rely upon any admissions or characterizations relevant to invalidity of the Asserted Patents, their prosecution histories, the prosecution histories of any foreign counterparts, admissions made in this Investigation, in any post-grant challenges at the United States Patent & Trademark Office, or otherwise. Respondents also reserve the right to rely upon any documentary or testimonial

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evidence of the existence of any systems that embodied or practiced the disclosures found in the accompanying invalidity charts, for example as discussed in the prior art references cited herein, as such systems may qualify as prior art under 35 U.S.C. § 102.

A. Identification of Prior Art and Documents Relating to Invalidity

Respondents identify the following prior art that anticipates or renders obvious at least one of the asserted claims or claims relied on for domestic industry of the '562 patent, '755 patent, and '003 patent under at least pre-AIA 35 U.S.C. § 102(a), (b), (e), (f), and/or (g) or 35 U.S.C. § 103(a). Respondents identify the following prior art that anticipates or renders obvious at least one of the asserted claims or claims relied on for domestic industry of the '481 patent under 35 U.S.C § 102(a) and/or (g) or 35 U.S.C. § 103.

Based on their investigation to date, Respondents have provided in the list below the prior art presently known to Respondents that they contend anticipates and/or renders obvious the asserted claims and claims relied on for domestic industry under at least Infineon's actual and/or apparent application of those claims. The prior art identified in these contentions discloses the elements of the asserted claims and claims relied on for domestic industry either explicitly or inherently.

Prior-art patents or publications included in these contentions may be related (such as a divisional, continuation, continuation-in-part, parent, or child) to earlier or later-filed patents or publications, may have counterparts filed in other jurisdictions, or may incorporate (or be incorporated by) other patents or publications by reference. The listed patents or publications are intended to be representative of these other patents or publications to the extent they exist. Respondents accordingly reserve the right to modify, amend, or supplement these contentions with these related patents or publications, as well as other prior art references, upon further

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investigation. Additionally, any reference in these Invalidity Contentions, including the appendices thereto, to a specific subsection or subsections of 35 U.S.C. § 102, is merely exemplary, and Respondents expressly reserve the right to rely on additional or other sections of 35 U.S.C. § 102, as appropriate. If Infineon asserts that one or more of these references or systems fails to disclose one or more elements of a claim, Respondents reserve the right to also use those references to invalidate the claim under 35 U.S.C. § 103.

Exemplary invalidity claim charts for the Asserted Patents are attached as Appendices A-1 through A-5 ('481 patent), B-1 through B-4 ('562 patent), C-1 through C-3 ('755 patent), D-1 through D-4 ('003 patent). These charts, however, are merely examples. The claimed features are similarly described and suggested in other places (including in the documents cited during prosecution of each Asserted Patent, or the documents cited during prosecution of each prior art patent or patent application), and also were present when prior-art systems practicing the described prior art were used before the application that ultimately led to the Asserted Patents. Thus, where patents or other printed materials are disclosed, Respondents reserve the right to also rely on those materials as descriptions of systems, devices, or methods referenced therein, publicly used, and/or on sale or known in the United States. Further, Respondents reserve the right to rely on other evidence of the prior art beyond merely the exemplary references cited in Appendices A-1 through A-5, B-1 through B-4, C-1 through C-3, D-1 through D-4. For the references cited in these Appendices, each listed document or item became prior art at least as early as the dates given therein.

Below, Respondents identify prior art and other documents potentially relevant to the validity of the Asserted Patents that are presently known to the Respondents, as further explained in the attached Appendices:

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Table 1: Prior Art Patents and Patent Applications

Country	Patent/ Application Publication No.	Date of Issue/ Publication	Bates Range
US	US20140110760A1	2014-04-24	Innoscence 1414-00007194 - Innoscence 1414-00007215
US	US20140175454A1	2014-06-26	Innoscence 1414-00007223 - Innoscience 1414- 00007240
US	US20140225124A1	2014-08-14	Innoscence 1414-00007241 - Innoscience 1414- 00007254
US	US20140084433A1	2014-03-27	Innoscence 1414-00007167 - Innoscience 1414- 00007179
US	US62/196,629	2019-08-29	Innoscence 1414-00013460 - Innoscience 1414- 00013529
US	US5523599A	1996-06-04	Innoscence 1414-00002932 - Innoscience 1414- 00002961
US	US7417257B2	2008-08-26	Innoscence 1414-00002978 - Innoscience 1414- 00002984
US	US20060091498A1	2006-05-04	Innoscence 1414-00002985 - Innoscience 1414- 00003000
US	US20090315075A1	2009-12-24	Innoscence 1414-00003096 - Innoscience 1414- 00003107
US	US20130009165A1	2013-01-10	Innoscence 1414-00003161 - Innoscience 1414- 00003174

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Country	Patent/ Application Publication No.	Date of Issue/ Publication	Bates Range
US	US20040178443A1	2004-09-16	Innoscence 1414-00012374 - Innoscience 1414- 00012383
US	US20120280280A1	2012-11-08	Innoscence 1414-00012514 - Innoscience 1414- 00012531
US	US5943601A	1999-08-24	Innoscence 1414-00003742 - Innoscience 1414- 00003753
US	US7777252B2	2010-08-17	Innoscence 1414-00003905 - Innoscience 1414- 00003921
US	US20100052066A1	2010-03-04	Innoscence 1414-00004344 - Innoscience 1414- 00004375
US	US20080023726A1	2008-01-31	Innoscence 1414-00004284 - Innoscience 1414- 00004297
US	US6249056B1	2001-06-19	Innoscence 1414-00003766 - Innoscience 1414- 00003774
US	US20050051800A1	2005-03-10	Innoscence 1414-00006160 - Innoscience 1414- 00006170
US	US20040041169A1	2004-03-04	Innoscence 1414-00006118 - Innoscience 1414- 00006124
US	US20060255403A1	2006-11-16	Innoscence 1414-00003040 - Innoscience 1414- 00003079
KR	KR20070041134A	2007-04-18	Innoscence 1414-00004519 - Innoscience 1414- 00004526; Innoscience 1414-

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Country	Patent/ Application Publication No.	Date of Issue/ Publication	Bates Range
			00181330 - Innoscience 1414-00181339 ²
US	US6160280A	2000-12-12	Innoscience 1414-00005663 - Innoscience 1414- 00005676
US	US7408399B2	2008-08-05	Innoscience 1414-00005843 - Innoscience 1414- 00005848
US	US 2006/0113593A1	2006-06-016197	Innoscience1414-00006197 – Innoscience1414-00006237
US	US20060175633A1	2006-08-10	Innoscience 1414-00006249 - Innoscience 1414- 00006256
US	US10930524B2	2021-02-23	Innoscience1414-00006838 - Innoscience1414-00006852
US	US7880280B2	2011-02-01	Innoscience 1414-00006891 - Innoscience 1414-00006900
US	US9589869B2	2017-03-07	Innoscience 1414-00006981 - Innoscience 1414-00007001
US	US20140097528A1	2014-04-10	Innoscience 1414-00007180 - Innoscience 1414- 00007193
US	US6483135B1	2002-11-19	Innoscience 1414-00005677 - Innoscience 1414- 00005703
US	US5910670	1999-06-08	Innoscience1414-00002972- Innoscience1414-00002977

² Translation Certification at Innoscience 1414-00181340.

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Country	Patent/ Application Publication No.	Date of Issue/ Publication	Bates Range
US	US20110073912	2011-03-31	Innoscience1414-00015307- Innoscience1414-00015318
US	US20100171150	2010-07-08	Innoscience1414-00015265- Innoscience1414-00015286
US	US20120146097	2012-06-14	Innoscience1414-00015319- Innoscience1414-00015347
US	US20090278236	2009-11-12	Innoscience1414-00015245- Innoscience1414-00015264
US	US20100193842	2010-08-05	Innoscience1414-00015287- Innoscience1414-00015306
US	US20110121389	2011-05-26	Innoscience1414-00003117- Innoscience1414-00003127
US	US20050127438	2005-06-16	Innoscience1414-00171366- Innoscience1414-00171375
US	US20070164321A1	2007-07-19	Innoscience 1414-00014701 - Innoscience 1414- 00014715
US	US20090250816A1	2009-10-08	Innoscience 1414-00176331 - Innoscience 1414- 00176340
US	US7335590B2	2008-02-26	Innoscience 1414-00176341 - Innoscience 1414- 00176371
US	US6607976B2	2003-08-19	Innoscience 1414-00176372 - Innoscience 1414- 00176381
US	US6844258B1	2005-01-18	Innoscience 1414-00003826 - Innoscience 1414- 00003836

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Country	Patent/ Application Publication No.	Date of Issue/ Publication	Bates Range
US	US4980752A	1990-12-25	Innoscence 1414-00014650 - Innoscience 1414- 00014656
US	US5635763A	1997-06-03	Innoscence 1414-00014657 - Innoscience 1414- 00014674
US	US6646352B2	2003-11-11	Innoscence 1414-00014683 - Innoscience 1414- 00014700
US	US7161194B2	2007-01-09	Innoscence 1414-00005810 - Innoscience 1414- 00005828
US	US7800131	2010-09-21	Innoscence 1414-00005870 - Innoscience 1414- 00005902
US	US7548112	2009-06-16	Innoscence 1414-00005864 - Innoscience 1414- 00005869
WO	WO2005070009A2	2005-08-04	Innoscence 1414-00014271 - Innoscience 1414- 00014296
US	US20050051796A1	2005-03-10	Innoscence 1414-00006146 - Innoscience 1414- 00006159
US	US60/649,393	2006-08-10	Innoscence 1414-00006792 - Innoscience 1414- 00006797

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Table 2: Non-Patent Publications

Citation	Bates Range
Fukuta et al., <i>GaAs Microwave Power FET</i> , IEEE Transactions on Electron Devices, Vol. ED-23, No. 4 (April 1976)	Innoscience 1414-00177496 - Innoscience 1414-00177502; Innoscience 1414-00177514
S. Mil 'Shtein et al., Heterostructure transistor with tunable gate bias, <i>Microelectronics Journal</i> , Vol. 36, Is. 3-6, 301-303 (Apr 19, 2005), https://doi.org/10.1016/j.meio.2005.02.049	Innoscience 1414-00014297 - Innoscience 1414-00014299
Lind, Anders. "Source-Sense Packages for HV MOSFETs." 46th International Symposium on Microelectronics (2013).	Innoscience 1414-00007466 - Innoscience 1414-00007471
Huang, Xiucheng, et al. "Evaluation and Applications of 600V/650V Enhancement-Mode GaN Devices." IEEE Explore (2015).	Innoscience 1414-00007460 - Innoscience 1414-00007465
ThinPAK 8x8 New High Voltage SMD-Package (Apr. 2010).	Innoscience 1414-00007539 - Innoscience 1414-00007572
Recommendations for Printed Circuit Board Assembly of Infineon VDSO Packages (ThinPAK) (July 2010).	Innoscience 1414-00007573 - Innoscience 1414-00007599
Kanamura et al., <i>High power and high gain AlGaIn/GaN MIS-HEMTs with high-k dielectric layer</i> , Phys. Stat. Sol., 5, No. 6, 2037–2040 (2008)	Innoscience 1414-00170802 - Innoscience 1414-00170805
Okino et al., <i>Drain Current DLTS of AlGaIn–GaN MIS-HEMTs</i> , IEEE Electron Device Letters, Vol. 25, No. 8 (2004)	Innoscience 1414-00015744 - Innoscience 1414-00015746; Innoscience 1414-00177510
Imada et al., <i>Enhancement-Mode GaN MIS-HEMTs for Power Supplies</i> , The 2010 International Power Electronics Conference (2010)	Innoscience 1414-00015733 - Innoscience 1414-00015739; Innoscience 1414-00177512

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Citation	Bates Range
Excerpts from Rudiger Quay, Gallium Nitride Electronics (2008)	Innoscence 1414-00170919 - Innoscence 1414-00170944
Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , <i>Proceedings of the IEEE</i> , Vo. 90, No. 6 (2002)	Innoscence 1414-00007967 - Innoscence 1414-00007976; Innoscence 1414-00177508
Wu et al., <i>Very-High Power Density AlGaIn/GaN HEMTs</i> , <i>IEEE Transactions on Electronic Devices</i> , Vol. 48, No. 3 (2001)	Innoscence 1414-00010157 - Innoscence 1414-00010161; Innoscence 1414-00177522
S.H. Lee et al., <i>700V Lateral DMOS with New Source Fingertip Design</i> , <i>Proceedings of the 20th International Symposium on Power Semiconductor Devices & IC's</i> (2008)	Innoscence 1414-00010338- Innoscence 1414-00010341; Innoscence 1414-00177504
Excerpts from Umesh K. Mishra et al., <i>Semiconductor Device Physics and Design</i> (2008)	Innoscence 1414-00171080 - Innoscence 1414-00171155
R. P. Jindal, <i>Noise Associated with Distributed Resistance of MOSFET Gate Structures in Integrated Circuits</i> , <i>IEEE Transactions on Electron Devices</i> , Vol. ED-31, No. 10 (October 1984)	Innoscence 1414-00171171- Innoscence 1414-00171175
Evangelos F. Tsakas et al., <i>Noise Associated with Interdigitated Gate Structures in RF Submicron MOSFETs</i> , <i>IEEE Transactions on Electron Devices</i> , Vol. 47, No. 9 (September 2000)	Innoscence 1414-00171176 - Innoscence 1414-00171181
A. Blicher et al., <i>Encyclopedia of Physical Science and Technology</i> , Vol. 5, p. 831-849 (Robert A. Meyers, 3d. ed. 2003)	Innoscence 1414-00171304- Innoscence 1414-00171327
Shreepad Karmalkar, <i>A New Equivalent MOSFET Representation of a HEMT to Analytically Model Non-Linear Charge Control for Simulation of HEMT Devices and Circuits</i> , <i>IEEE Transactions on Electron Devices</i> , Vol. 44, No. 5 (May 1997)	Innoscence 1414-00171423 - Innoscence 1414-00171429

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Citation	Bates Range
Sonu Daryanani, <i>GaN Power HEMT > 650 V: A Parametric Analysis and Comparison to SiC MOSFET</i> , Power Electronics News (Jun. 23, 2022), https://www.powerelectronicsnews.com/gan-power-hemt-650-v-a-parametric-analysis-and-comparison-to-sic-mosfet/	Innoscience 1414-00171360 - Innoscience 1414-00171365
Enrico Bottaro et al., <i>Circuit Models of Power MOSFETs Leading the Way of GaN HEMT Modelling—A Review</i> , Energies 2022, 15, 2415 (May 7, 2022)	Innoscience 1414-00171376 - Innoscience 1414-00171407
Utkarsh Jadli, <i>Modeling Power GaN-HEMTs Using Standard MOSFET Equations and Parameters in SPICE</i> , Electronics 2021, 10, 130 (January 9, 2021)	Innoscience 1414-00171408 - Innoscience 1414-00171422
Pearnton et al., <i>Gallium Nitride Processing for Electronics, Sensors and Spintronics</i> , Springer, 10.1007/1-84628-359-0. (2006)	Innoscience 1414-00009126 - Innoscience 1414-00009508
Adachi, <i>Properties of Group-IV, III–V and II–VI Semiconductors</i> , John Wiley & Sons, Ltd, 10.1002/0470090340 (2005)	Innoscience 1414-00174101 - Innoscience 1414-00174130
Mishra et al., <i>Semiconductor Device Physics and Design</i> , Springer (2007)	Innoscience 1414-00007977 - Innoscience 1414-00008559
Wu et al., <i>Very-High Power Density AlGaIn/GaN HEMTs</i> , IEEE Transactions on Electronic Devices, Vol. 48, No. 3, March 2001	Innoscience 1414-00010157 - Innoscience 1414-00010161
Quay, <i>Gallium Nitride Electronics</i> , Springer, 10.1007/978-3-540-71892-5. (2008)	Innoscience 1414-00009509 - Innoscience 1414-00010000
Mishra et al., <i>AlGaIn/GaN HEMTs—An Overview of Device Operation and Applications</i> , Proceedings of the IEEE, Vol. 90, No. 6, June 2002	Innoscience 1414-00007967 - Innoscience 1414-00007976
Neaman, <i>Semiconductor Physics and Devices</i> , 3 rd edition (2002)	Innoscience 1414-00008560 - Innoscience 1414-00009125
Voss, <i>Thermally Stable Ohmic and Schottky Contacts to GaN</i> , University of Florida, 2008	Innoscience 1414-00010001 -

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Citation	Bates Range
	Innoscence 1414-00010144
Krämer, <i>Fabrication and characterization of metal-semiconductor contacts for application in Al_xGa_{1-x}N/GaN HEMTs</i> , (Oct. 31, 2000)	Innoscence 1414-00007816 - Innoscence 1414-00007966
Kuzmick et al., <i>Technology and Performance of InAlN/AlN/GaN HEMTs With Gate Insulation and Current Collapse Suppression Using ZrO₂ or HfO₂</i> , IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 55, No. 3, Mar. 2008	Innoscence 1414-00015098 - Innoscence 1414-00015102
Wu et al., <i>Aluminum, magnesium, and gold contacts to contamination free n-GaN surfaces</i> , Journal of Applied Physics, Vol. 89, No. 1, Jan. 1, 2001	Innoscence 1414-00010152 - Innoscence 1414-00010156
Foresi et al., <i>Metal contacts to gallium nitride</i> , Appl. Phys. Lett., Vol. 62, No. 22, May. 31, 1993	Innoscence 1414-00007813 - Innoscence 1414-00007815
Kayali et al., <i>GaAs MMIC Reliability Assurance Guideline for Space Applications</i> , JPL Publication 96-25, Dec. 15, 1996	Innoscence 1414-00014756 - Innoscence 1414-00014976
Bauccio, Michael, <i>Refractory metals</i> , ASM metals reference book, ASM International, American Society for Metals, ISBN 978-0-87170-478-8, (1993)	Innoscence 1414-00171605 - Innoscence 1414-00171615
Preuss, <i>Finer Copper Wires Make for Faster Integrated Circuits</i> , Berkeley Lab, https://www2.lbl.gov/Science-Articles/Archive/integrated-circuits-copper.html , Apr. 5, 1999	Innoscence 1414-00015103 - Innoscence 1414-00015105
Cockeram, <i>The Diffusion Bonding of Silicon Carbide and Boron Carbide Using Refractory Metals</i> , USDOE Contract No. DE-ACI 1-98 PN38206, Nov. 22, 1999	Innoscence 1414-00014745 - Innoscence 1414-00014755
Kim, <i>Atomic Layer Deposition of Metal and Nitride Thin films: Current Research Efforts and Applications for Semiconductor Device Processing</i> , RC22737 (W0303-012), Mar. 5, 2003	Innoscence 1414-00014977 - Innoscence 1414-00015097
Excerpts from Rooy, E.L., <i>Introduction to Aluminum and Aluminum Alloys</i> , Metals Handbook, 10 th Edition, Volume 2 Properties and Selection: Nonferrous Alloys and Special-Purpose Materials, ASM International, ISBN 978-0-87170-378-1, (October 1990)	Innoscence 1414-00176769 - Innoscence 1414-00176782

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Citation	Bates Range
Pierson, Hugh O., <i>The Refractory Nitrides</i> , Handbook of Refractory Carbides and Nitrides, Properties, Characteristics, Processing and Applications, ISBN 978-0-8155-1392-6, (1996)	Innoscence 1414-00176783 - Innoscence 1414-00177142

Table 3: Prior Art Systems

Citation	Bates Range
Transphorm's TPH3006LD transistor device	TGAN_00000001; TGAN_00000178 – TGAN_00000185; Innoscience 1414-00014177– Innoscience 1414-00014178; Innoscience 1414-00014179; Innoscience 1414-00014213 – Innoscience 1414-0001
Transphorm's TPH3002LD transistor device	TGAN_00000003; TGAN_00000146 – TGAN_00000153; Innoscience 1414-00014177– Innoscience 1414-00014178; Innoscience 1414-00014179; Innoscience 1414-00014213 – Innoscience 1414-00014215
Panasonic's PGA26E19 Device	Innoscence 1414-00181341 – Innoscience 1414-00181368; Innoscience 1414-00181369 – Innoscience 1414-00181383; Innoscience 1414-00007738 – Innoscience 1414-00007740

For the avoidance of doubt, Respondents reserve their rights to cite and rely on additional prior art identified herein as appropriate. To the extent they constitute prior art, Respondents also reserve the right to rely upon (1) foreign counterparts of the U.S. Patents identified in these Invalidity Contentions, (2) U.S. counterparts of foreign patents and foreign patent applications identified in these Invalidity Contentions, and (3) U.S. and foreign patents and patent applications corresponding to articles and publications identified in these Invalidity Contentions.

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B. The Level of Ordinary Skill in the Art

A person of ordinary skill in the art with respect to the Asserted Patents would have possessed at least a four-year degree in electrical engineering, chemical engineering, physics, or material science or a closely related field and at least two years of experience in semiconductor device design or fabrication, including the processing of semiconductor materials, analysis of device operation, or the development of new device topologies. Additional education could substitute for professional experience and vice versa.

C. Anticipation Under 35 U.S.C. § 102 and Obviousness Under 35 U.S.C. §103

As noted above, Respondents contend that, at least under Infineon's actual and/or apparent application of the claims, the prior art below independently anticipates the asserted claims and claims relied on for domestic industry under 35 U.S.C. § 102, as set forth in the appendices attached hereto. Where patents or other printed materials are disclosed, Respondents reserve the right to also rely on those materials as descriptions of systems, devices, or methods referenced therein, publicly used, and/or on sale or known in the United States. If Infineon asserts that any of this prior art fails to disclose one or more elements of a claim, Respondents reserve the right to also use those references to invalidate the claim under 35 U.S.C. § 103.

Much of the art identified in these contentions reflects common knowledge and the state of the art prior to the filing or the asserted priority date of each Asserted Patents. As such, the obviousness combinations in these contentions are intended to be exemplary. There are many possible combinations of the disclosed prior art, and the inclusion of certain exemplary combinations does not exclude other combinations. For example, where a particular contention calls for combining references, multiple other references can be combined.

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Citations to particular excerpts from the prior art are likewise exemplary and not exhaustive of the evidentiary support for the invalidity of the Asserted Patents contained in and/or concerning a particular piece of prior art. Respondents may rely on uncited portions of the prior art references, other documents or operational systems, the “Background of the Invention” and other relevant portions of the Asserted Patents, the prosecution histories of the Asserted Patents (including all cited references and all foreign counterparts), and forthcoming fact and expert testimony to provide context to aid in understanding the prior art reference and/or the cited portions of the references. Where Respondents cite to a particular figure in a reference, the citation encompasses the caption and description of the figure and any text relating to or discussing the figure. Likewise, where Respondents cite text referring to a figure, the citation includes the figure as well.

Further, Respondents incorporate by reference all current and future filings in the *inter partes* reviews challenging the validity of the Asserted Patents. See *Innoscence America, Inc. v. Infineon Techs. Austria AG*, IPR2024-00975; *Innoscence America, Inc. v. Infineon Techs. Americas Corp.*, IPR2025-00175, IPR2025-00010, IPR2025-00094.

In light of the statements and reservation of rights set forth in these Invalidity Contentions, the Respondents specifically identify at least the following grounds (and similar permutations based on the references listed below) that render the asserted claims of the Asserted Patents invalid under 35 U.S.C. §§ 102 and 103.

1. '481 Patent

**Table 3: Exemplary Anticipatory and Combinations
for the Asserted Claims of the '481 Patent**

Appendix	Prior Art References
A-1	Invalidity Chart Based on U.S. Patent No. 10,930,524 (“ <i>Liu</i> ”)

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Appendix	Prior Art References
A-2	Invalidity Chart Based on U.S. Patent Application Publication No. 2014/0110760 (“ <i>Nega</i> ”)
A-3	Invalidity Chart Based on Transphorm’s TPH3006LD transistor device (“ <i>Transphorm TPH3006LD Device</i> ”)
A-4	Invalidity Chart Based on Transphorm’s TPH3002LD transistor device (“ <i>Transphorm TPH3002LD Device</i> ”)
A-5	Invalidity Chart Based on Panasonic’s PGA26E19 device (“ <i>Panasonic PGA26E19 Device</i> ”)

Exemplary invalidity claim charts in Appendices A-1 through A-5 illustrate the following invalidity grounds for the ’481 patent:

- Obviousness based on Liu in combination with the knowledge of a skilled artisan (claims 1, 2, 4, and 6);
- Obviousness based on Liu in combination with U.S. Patent Application Publication No. 2014/0175454 (“Roberts”) (claims 3 and 17);
- Obviousness based on Liu in combination with U.S. Patent Application Publication No. 2014/0084433 (“Otremba433”) (claims 4 and 9);
- Obviousness based on Liu in combination with U.S. Patent Application Publication No. 2014/0225124 (“Otremba124”) (claims 4 and 9);
- Obviousness based on Liu in combination with Roberts and Otremba433 (claim 17);
- Obviousness based on Nega in combination with Roberts (claims 1-3 and 6);
- Obviousness based on Nega in combination with Roberts and Otremba124 (claims 4, 9, and 17);
- Obviousness based on Nega in combination with Roberts and Otremba433 (claims 4 and 17)
- Obviousness based on Transphorm TPH3006LD Device in combination with the knowledge of a skilled artisan (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Transphorm TPH3006LD Device in combination with Liu (claims 1, 2-4, 6, 9, and 17);

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- Obviousness based on Transphorm TPH3006LD Device in combination with Nega (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Transphorm TPH3006LD Device in combination with Roberts (claims 3 and 17);
- Obviousness based on Transphorm TPH3006LD Device in combination with Liu and Roberts (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Transphorm TPH3006LD Device in combination with Nega and Roberts (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on TPH3002LD in combination with the knowledge of a skilled artisan (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on TPH3002LD in combination with Liu (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on TPH3002LD in combination with Nega (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on TPH3002LD in combination with Roberts (claims 3 and 17);
- Obviousness based on Transphorm TPH3002LD Device in combination with Liu and Roberts (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Transphorm TPH3002LD Device in combination with Nega and Roberts (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Panasonic PGA26E19 Device in combination with the knowledge of a skilled artisan (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Panasonic PGA26E19 Device in combination with Liu (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Panasonic PGA26E19 Device in combination with Nega (claims 1, 2-4, 6, 9, and 17); and
- Obviousness based on Panasonic PGA26E19 Device in combination with Roberts (claims 3, 17).
- Obviousness based on Panasonic PGA26E19 Device in combination with Liu and Roberts (claims 1, 2-4, 6, 9, and 17);
- Obviousness based on Panasonic PGA26E19 Device in combination with Nega and Roberts (claims 1, 2-4, 6, 9, and 17);

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2. '562 Patent

**Table 4: Exemplary Anticipatory and Combinations
for the Asserted Claims of the '562 Patent**

Appendix	Prior Art References
B-1	Invalidity Chart Based on Korean Patent Application Publication No. 10-2007-0041134 (“Jung”)
B-2	Invalidity Chart Based on U.S. Patent No. 5,943,601 (“Usui”)
B-3	Invalidity Chart Based on U.S. Patent Publication No. 2010/0052066 (“Yu”)
B-4	Invalidity Chart Based on U.S. Patent No. 6,249,056 (“Kwon”)

Exemplary invalidity claim charts in Appendices B-1 through B-4 illustrate the following invalidity grounds for the '562 Patent:

- Anticipation based on Usui (claims 1 and 2);
- Obviousness based on Usui in combination with the knowledge of a skilled artisan (claims 1 and 2);
- Obviousness based on Usui in combination with Yu (claims 8 and 13);
- Obviousness based on Usui in combination with Yu and Adesida (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Usui in combination with Adesida (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Usui in combination with Yu and Sugimoto (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Usui in combination with Sugimoto (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Yu (claims 1, 2, 8, and 13);
- Obviousness based on Yu in combination with Usui (claims 1, 2, 8, and 13);

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- Obviousness based on Yu in combination with Adesida (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Yu in combination with Usui and Adesida (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Yu in combination with Sugimoto (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Yu in combination with Usui and Sugimoto (claims 9, 10, 11, 14, 15, and 16);
- Obviousness based on Kwon in combination with Usui (claims 1 and 2);
- Obviousness based on Kwon in combination with Usui and Yu (claims 8 and 13);
- Obviousness based on Kwon in combination with Usui and Adesida (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Kwon in combination with Usui and Sugimoto (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Kwon in combination with Yu (claims 1, 2, 8, and 13);
- Obviousness based on Kwon in combination with Yu and Adesida (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Kwon in combination with Yu and Sugimoto (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Jung in combination with Usui (claims 1 and 2);
- Obviousness based on Jung in combination with Usui and Yu (claims 8 and 13);
- Obviousness based on Jung in combination with Usui and Adesida (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Jung in combination with Usui and Sugimoto (claims 8, 9, 10, 11, 13, 14, 15, and 16);
- Obviousness based on Jung in combination with Yu (claims 1, 2, 8, and 13);
- Obviousness based on Jung in combination with Yu and Adesida (claims 8, 9, 10, 11, 13, 14, 15, and 16); and

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- Obviousness based on Jung in combination with Yu and Sugimoto (claims 8, 9, 10, 11, 13, 14, 15, and 16).

3. '755 Patent

**Table 5: Exemplary Anticipatory and Combinations
for the Asserted Claims of the '755 Patent**

Appendix	Prior Art References
C-1	Invalidity Chart Based on U.S. Patent No. 5,523,599 (“Fujishima599”)
C-2	Invalidity Chart Based on U.S. Patent Publication No. 2006/0255403 (“Asano”)
C-3	Invalidity Chart Based on “GaAs Microwave Power FET” authored by Masumi Fukuta, Katsuhiko Suyama, Hidetake Suzuki, and Hajime Ishikawa (“Fukuta”)

Exemplary invalidity claim charts in Appendices C-1 through C-3 illustrate the following invalidity grounds for the '755 patent:

- Anticipation based on *Fujishima599* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with the knowledge of a skilled artisan (claims 1-4, 8-9); and
- Obviousness based on *Fujishima599* in combination with *Sriram* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Beach* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Park* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Hossain* (claims 1-4, 8-9);

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- Obviousness based on *Fujishima599* in combination with *Sriram* and *Beach* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Sriram* and *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Sriram* and *Park* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Sriram* and *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Sriram* and *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Beach* and *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Beach* and *Park* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Beach* and *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Beach* and *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Zhang* and *Park* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Zhang* and *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Zhang* and *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Park* and *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Park* and *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fujishima599* in combination with *Sato* and *Hossain* (claims 1-4, 8-9);
- Anticipation based on *Fukuta* (claims 1, 4, 9);

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- Obviousness based on *Fukuta* in combination with the knowledge of a skilled artisan (claims 1-4, 8-9); and
- Obviousness based on *Fukuta* in combination with *Sriram* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Beach* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Park* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Sriram* and *Beach* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Sriram* and *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Sriram* and *Park* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Sriram* and *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Sriram* and *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Beach* and *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Beach* and *Park* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Beach* and *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Beach* and *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Zhang* and *Park* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Zhang* and *Sato* (claims 1-4, 8-9);

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- Obviousness based on *Fukuta* in combination with *Zhang* and *Hossain* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Park* and *Sato* (claims 1-4, 8-9);
- Obviousness based on *Fukuta* in combination with *Park* and *Hossain* (claims 1-4, 8-9); and
- Obviousness based on *Fukuta* in combination with *Sato* and *Hossain* (claims 1-4, 8-9);
- Anticipation based on *Asano* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with the knowledge of a skilled artisan (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Sriram* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Beach* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Park* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Sriram* and *Beach* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Sriram* and *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Sriram* and *Park* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Beach* and *Zhang* (claims 1-4, 8-9);
- Obviousness based on *Asano* in combination with *Beach* and *Park* (claims 1-4, 8-9); and
- Obviousness based on *Asano* in combination with *Zhang* and *Park* (claims 1-4, 8-9).

4. '003 Patent

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**Table 6: Exemplary Anticipatory and Combinations
for the Asserted Claims of the '003 Patent**

Appendix	Prior Art References
D-1	Invalidity based on U.S. Patent Application Publication No. 2005/0051800 (“Mishra”)
D-2	Invalidity based on U.S. Patent Application Publication No. 6,160,280 (“Bonn”)
D-3	Invalidity based on S. Mil 'Shtein et al., Heterostructure transistor with tunable gate bias, Microelectronics Journal, Vol. 36, Is. 3-6, 301-303 (Apr 19, 2005), https://doi.org/10.1016/j.meio.2005.02.049 (“Mil’Shtein”)
D-4	Invalidity based on U.S. Patent Publication No. 2006/0175633 (“Kinzer633”)

Exemplary invalidity claim charts in Appendices D-1 through D-4 illustrate the following invalidity grounds for the '003 patent:

- Obviousness based on Mishra in combination with Ren (claims 1, 2, and 10);
- Obviousness based on Bonn in combination with Mizuta (claim 1);
- Obviousness based on Bonn in combination with Mishra (claim 1);
- Obviousness based on Bonn in combination with Ren and Mishra (claims 1, 2, and 10);
- Obviousness based on Mil’Shtein alone (claim 1);
- Obviousness based on Mil’Shtein and Bonn (claim 1);
- Obviousness based on Mil’Shtein in combination with Mishra and/or Ren (claims 1, 2, and 10); and
- Obviousness based on Mil’Shtein in combination with Bonn and further in view of Mishra and/or Ren (claims 1, 2, and 10)
- Anticipation based on Kinzer633 (claims 1-2, 10)
- Obviousness based on Kinzer633 alone (claim 1);

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- Obviousness based on Kinzer633 and Bonn (claims 1-2, 10);
- Obviousness based on Kinzer633 in combination with Mishra and/or Ren (claims 1, 2, and 10); and
- Obviousness based on Kinzer633 in combination with Bonn and further in view of Mishra and/or Ren (claims 1, 2, and 10).

D. Secondary Considerations

Infineon bears the burden of producing evidence and argument to establish any purported secondary considerations of non-obviousness. *See, e.g., ZUP, LLC v. Nach Mfg., Inc.*, 896 F.3d 1365, 1373 (Fed. Cir. 2018) (“[A] patentee bears the burden of production with respect to evidence of secondary considerations of nonobviousness.”). Respondents are aware that Infineon has produced documents that they allege may support secondary considerations of non-obviousness. *See* Infineon’s Response to Interrogatory No. 7 (identifying documents that “may be responsive”). However, to date, Infineon has not put forth any arguments or contentions to establish any purported secondary considerations of non-obviousness nor has Infineon provided an explanation whether, much less how, the identified documents may relate to any argument of secondary considerations. Accordingly, Respondents reserve all rights to address and rebut any such contentions from Infineon (including by proffering arguments and evidence not identified in these Invalidity Contentions) if and when Infineon satisfies its burden.

III. INVALIDITY UNDER 35 U.S.C. § 112

Respondents identify below the grounds upon which certain asserted claims of the Asserted Patents are invalid under 35 U.S.C. § 112, paragraphs (a), (b), and (d) and Pre-AIA 35 U.S.C. § 112, paragraphs one, two, and three.

Section 112 requires that a patent specification “contain a written description . . . of the manner and process of making and using [the invention] in such full, clear, concise and exact terms

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as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same.” 35 U.S.C. § 112 ¶(a); *see also* Pre-AIA 35 U.S.C. § 112. A patent’s written description “must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). The disclosure must “convey to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Id.* The level of detail required to satisfy the written description requirement varies depending on the nature and scope of the claims and on the complexity and predictability of the relevant technology, but a “mere wish or plan” for obtaining the alleged invention does not satisfy the written description requirement. *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1344 (Fed. Cir. 2013). Put another way, “a description that merely renders the invention obvious does not satisfy the requirement.” *Ariad*, 598 F.3d at 1351. Instead, “all the limitations must appear in the specification.” *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997). Respondents contend that, at least under Infineon’s actual and/or apparent application of the claims, the Asserted Patents do not include a sufficient written description supporting at least the claims identified below.

Section 112 likewise requires that the specification “enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the” alleged invention. 35 U.S.C. § 112 ¶(a) ; *see also* Pre-AIA 35 U.S.C. § 112. A claim is not enabled if, “at the effective filing date of the patent, one of ordinary skill in the art could not practice their full scope without undue experimentation.” *Wyeth and Cordis Corp. v. Abbott Labs.*, 720 F.3d 1380, 1384 (Fed. Cir. 2013). “This important doctrine prevents both inadequate disclosure of an invention and overbroad claiming that might otherwise attempt to cover more than was actually invented.” *MagSil Corp. v.*

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Hitachi Global Storage Techs., Inc., 687 F.3d 1377, 1381 (Fed. Cir. 2012). Respondents contend that, at least under Infineon’s actual and/or apparent application of the claims, the specifications of the Asserted Patents do not enable any person skilled in the relevant art to make and use the alleged inventions of at least the claims identified below without undue experimentation.

Section 112 further requires the specification to “conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.” 35 U.S.C. § 112 ¶(b); *see also* Pre-AIA 35 U.S.C. § 112. According to the Supreme Court, this provision requires the “claims, viewed in light of the specification and the prosecution history, [to] inform those skilled in the art about the scope of the invention with reasonable certainty.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). Respondents contend that, at least under Infineon’s apparent application of the claims, at least the claims identified below of the Asserted Patents fail to distinctly claim the alleged invention and thus are indefinite.

Each dependent claim that depends from any of the claims identified below of the Asserted Patents is also invalid under § 112 for similar reasons, as “[a] claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers” and thus must also satisfy paragraphs one and two for each limitation of the claim to which it refers. 35 U.S.C. § 112 ¶(d); *see also* Pre-AIA 35 U.S.C. § 112. Further, paragraph (d) also requires that a dependent claim “specify a further limitation of the subject matter claimed” beyond the claim to which it refers. 35 U.S.C. § 112 ¶(d); *see also* Pre-AIA 35 U.S.C. § 112. Respondents contend that, at least under Infineon’s apparent application of the claims, at least the dependent claims identified below of the Asserted Patents fail specify a further limitation beyond the claim to which they refer.

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Respondents' contentions that these claims are invalid under § 112 do not constitute, and should not be interpreted as, admissions regarding the scope of those claims, or that any of those claims are not anticipated or rendered obvious by any prior art.

Respondents' investigation of grounds of invalidity under § 112 is ongoing, and Respondents reserve the right to supplement these Invalidity Contentions.

A. '481 Patent

1. "lateral transistor" (claims 1, 17)

Independent claims 1 and 17 recite a "lateral transistor," which considered in view of Infineon's *inter partes* review proceeding preliminary response, now part of the intrinsic record,³ lacks written description support, is not enabled, and is indefinite. Infineon's inconsistent distinctions for a "lateral transistor" are arbitrary, decoupled from the specification, and fail to inform a person of ordinary skill in the art the scope of the respective transistors.

The '481 patent describes "lateral" and "vertical"⁴ transistors based on (1) the general flow of electrical current within the device, and (2) the electrode placement for each device. For

³ See *R2 Sol'ns LLC v. Databricks, Inc.*, No. 4:23-cv-01147, ECF No. 71 (E.D. Tex. Dec. 10, 2024) (patent owner response in an *inter partes* review proceeding creates prosecution disclaimer).

⁴ To the extent that a "lateral transistor" is understood within the full context of the independent and dependent claims, then a "lateral transistor" further lacks written description support, is not enabled, and is indefinite in view of dependent claim 5. Dependent claim 5 recites a "vertical transistor." Infineon, however, as applicant disclaimed "vertical transistor," arguing in an office action response that "Otremba '284 fails to teach at least the feature of a lateral transistor device" because "Otremba '284 teaches a vertical transistor which includes current electrodes on opposing surfaces," but "Otremba '284 does not teach a lateral transistor device." See Respondents Responsive Claim Construction Brief, Ex. 13, pp. 32-33. First, the full scope of this disclaimer underscores that the scope of the claimed transistors lack written description support, are not enabled, and are indefinite in view of Infineon's *inter partes* review position that the claimed transistors "cannot be identified by the placement of the transistor's electrodes." *Innoscence America, Inc. v. Infineon Technologies Austria AG*, IPR2024-00975, Paper 6, pp. 22-23, 47-48. Second, to the extent that Infineon defines the scope of a "lateral transistor" device by distinguishing it from a "vertical transistor" device, then these terms lack written description

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instance, the electric current drift path for “lateral transistors” “runs generally parallel to the lateral extent of a semiconductor material,” and “generally perpendicular to those surfaces” for a “vertical transistor.” The ’481 patent, 3:13-25. And the “[i]n a lateral device, the . . . electrode[s] are arranged on the upper surface [] of the compound semiconductor,” while in a “vertical device . . . one of the current electrodes is arranged on [the] lower surface of the body of the compound semiconductor and the other current electrode and control electrode are arranged on the opposing surface of the compound semiconductor transistor device.” The ’481 patent, 5:56-6:6. Infineon, as applicant, even distinguished the claimed “lateral transistor” from “vertical transistor” prior art based on the current flow *and* location of electrodes. *See* Respondents Responsive Claim Construction Brief, Ex. 13, pp. 32-33 (“Otremba ’284 fails to teach at least the feature of a lateral transistor device” because “Otremba ’284 teaches a vertical transistor which includes current electrodes on opposing surfaces,” but “Otremba ’284 does not teach a lateral transistor device.”).

As such, a transistor with both parallel (i.e., lateral) and perpendicular (i.e., vertical) current flow requires a definition that also includes the placement of its electrodes—e.g., a transistor with current flowing equally both vertically and laterally is a “lateral transistor” when the electrodes are arranged on the same surface and is a “vertical transistor” when the electrodes are arranged on opposite surfaces.

Infineon, however, now contradicts the ’481 patent specification *and* its own statements made during earlier prosecution, arguing that the transistors are not defined by the placement of electrodes, but rather, defined solely based on the current flow. *Innoscience America, Inc. v.*

support, are not enabled, and are indefinite in view of Infineon disclaiming a “vertical transistor” for claim 1, while still claiming a “vertical transistor” in claim 5 (dependent of claim 1). Infineon’s distinctions from a “lateral transistor” and “vertical transistor” are arbitrary, decoupled from the specification, and fail to inform a person of ordinary skill in the art the scope of the respective transistors.

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Infineon Technologies Austria AG, IPR2024-00975, Paper 6, pp. 22-23, 47-48. For instance, in an *inter partes* review proceeding for the '481 patent, Infineon argues that the claimed “lateral transistor” “cannot be identified by the placement of the transistor’s electrodes,” but rather a “lateral transistor” is a “transistor in which current flows across the base in the direction parallel to’ the device surface in contrast to vertical transistor ‘in which current across the base flows in the direction normal to the surface.’” *Id.*

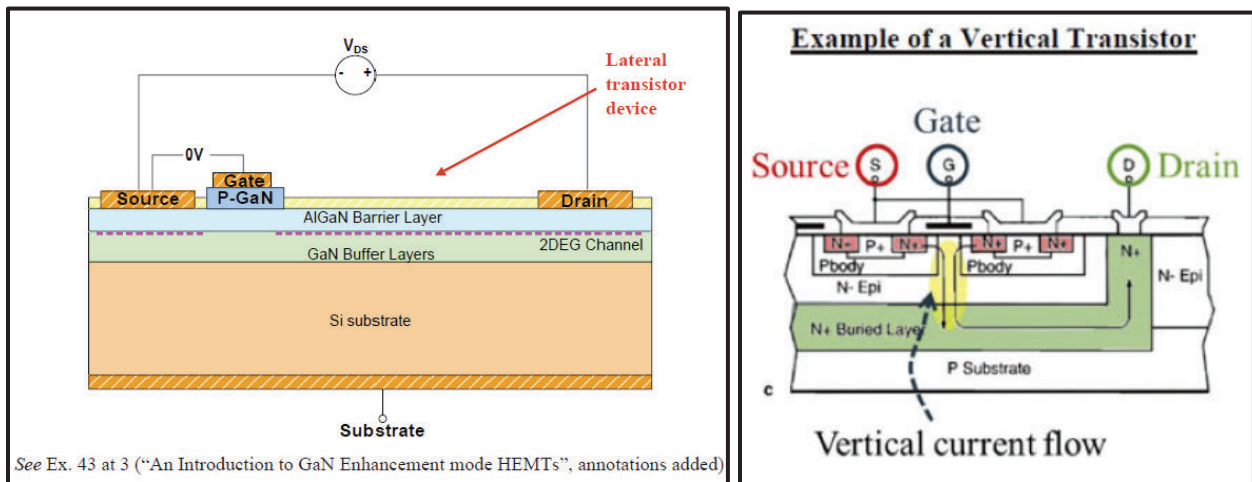
Infineon’s *inter partes* review statement is now part of the intrinsic record for understanding the scope of the '481 patent claims. *See R2 Sol’ns LLC v. Databricks, Inc.*, No. 4:23-cv-01147, ECF No. 71 (E.D. Tex. Dec. 10, 2024) (patent owner response in an *inter partes* review proceeding creates prosecution disclaimer). Further yet, Infineon is further judicially estopped from arguing otherwise (including reverting back to defining the transistors as requiring both current flow and electrode placement) as the Board adopted Infineon’s revised position in denying institution of the *inter partes* review. As such, this term must now be viewed in light of that updated intrinsic record, and the scope of “lateral transistor” *as construed without* the placement of electrodes lacks written description support, is not enabled, and is indefinite—the example above, a transistor with equal parts of parallel and perpendicular current flow, underscores how Infineon’s recent construction of defining transistors solely on current flow fails under § 112.

First, Infineon’s application of “lateral transistor” and defining it solely based on the current flow lacks written description support. As discussed above, the specification defines transistors based on both (1) current flow, and (2) the placement of electrodes. Thus, Infineon’s application of the term is directly at odds with the specification and lacks support.

Second, Infineon’s application of “lateral transistor” lacks enablement as a person of ordinary skill in the art would be unable, based solely on the direction of current flow, to

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distinguish a “lateral” transistor with current flowing both parallel and perpendicular, from a “vertical” transistor with current likewise flowing both parallel and perpendicular. For instance, without tethering the transistors to electrode placements, Infineon arbitrarily determines below that its own GS-065-11-1-L transistor (wherein the current flows both vertically and laterally), is a “lateral transistor” (left), but that a transistor (wherein the current flows both vertically and laterally) disclosed in the Murari prior art reference (contrary to its own disclosure) is a “vertical transistor” (right):



See (left) Complaint, Ex. 33C, p. 18; (right) Complainants’ Opening Claim Construction Brief, p. 5 (right). Thus, Infineon’s application of the term fails to enable a person of ordinary skill in the art to determine the scope of the claimed “lateral transistor.”

Third, Infineon’s application of “lateral transistor” is also indefinite. Infineon’s application of a “lateral transistor” fails to distinguish transistors with current flowing both parallel and perpendicular to the device surface. To a person of ordinary skill it would be unclear what types of transistors with perpendicular current flow amount to a “lateral transistor,” and vice versa, what types of transistors with parallel current flow amount to a “vertical transistor.” Thus, under

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Infinion's apparent application of "lateral transistor," this limitation is indefinite because a person of ordinary skill art cannot ascertain its meaning.

B. '562 Patent

1. "said refractory metal nitride . . . having a thickness greater than that of a bottommost layer of said plurality of metal layers" (claims 1, 13)

Independent claims 1 and 13 recite "said refractory metal nitride . . . having a thickness greater than that of a bottommost layer of said plurality of metal layers." The '562 patent's application of this phrase, however, lacks written description support, is not enabled, and is indefinite.

The '562 specification does not describe the means for measuring the thickness and consequently does not provide support for "refractory metal nitride . . . having a thickness greater than that of a bottommost layer of said plurality of metal layers." Specifically, the '562 specification (1) does not describe the means for measuring a layer thickness, and (2) does not describe a bottommost layer. Accordingly, this phrase is not sufficiently described in the '562 patent. Similarly, the '562 patent does not inform a person of ordinary skill how to practice the claimed limitation without undue experimentation to, for instance, measure the respective claim element layer thicknesses. Thus, the '562 patent likewise does not enable this claim limitation.

The application of "said refractory metal nitride . . . having a thickness greater than that of a bottommost layer of said plurality of metal layers" in the '562 patent is also indefinite. To a person of ordinary skill, it would be unclear what thickness of the respective layers should be measured. Thus, this limitation is indefinite because a person of ordinary skill art cannot ascertain its meaning.

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CERTIFICATE OF SERVICE

I, Damon Isaac Anderson, hereby certify that on January 24, 2025, copies of the foregoing were served upon the following as indicated:

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