

INNOSCIENCE'S INITIAL INVALIDITY CONTENTIONS

US 9,899,481 B2

APPENDIX A-1

In the Matter of:
CERTAIN SEMICONDUCTOR DEVICES, AND PRODUCTS
CONTAINING THE SAME

Investigation No. 337-TA-1414

APPENDIX A-1
INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 9,899,481 B2¹
LIU

U.S. Patent No. 10,930,524 (“*Liu*”) (Innoscence1414-00006838 - Innoscence1414-00006852) claims priority to Provisional application No. 62/196,629 (“*Liu Provisional*”) (Innoscence1414-00013460 - Innoscence1414-00013529) filed on July 24, 2015 and qualifies as prior art to U.S. Patent No. 9,899,481 (the ’481 Patent) at least under 35 U.S.C. § 102(a)(2).²

The following list identifies one or more references cited in certain grounds for invalidity of claims 1-4, 6, 9, and 17 of the ’481 Patent based on *Liu*:

- U.S. Patent Application Publication No. 2014/0175454 (“Roberts”) (Innoscence1414-00007223 - Innoscence1414-0007240) published on June 26, 2014, making it prior art at least under 35 U.S.C. § 102(a)(2).
- U.S. Patent Application Publication No. 2014/0084433 (“Otremba433”) (Innoscence1414-00007167 - Innoscence1414-00007179) published March 27, 2014, making it prior art under at least 35 U.S.C. §102(a)(1).
- U.S. Patent Application Publication No. 2014/0225124 (“Otremba124”) (Innoscence1414-00007241 - Innoscence1414-00007254) published August 14, 2014, making it prior art under at least 35 U.S.C. §102(a)(1).
- U.S. Patent No. 7,880,280 (“Otremba280”) (Innoscence1414-00006891 - Innoscence1414-00006900) issued February 1, 2011 is prior art under at least 35 U.S.C. §102(a)(1).

¹ The claim chart below is meant to illustrate how the identified reference invalidates the asserted claim. By not discussing other portions of the reference below, Respondents do not waive their right to rely on other portions of the reference; instead, Respondents expressly reserve their right to rely on other portions of the reference. These contentions are not an admission by Respondents that any accused products, including any past, current, or future version of these products, are covered by or infringe Complainant’s asserted claim, particularly once the claim is construed by the ALJ, do not constitute an admission by Respondents as to the proper construction of any asserted claim, citations may be based on Complainants’ apparent construction of the claim. These contentions are not an admission by Respondents as to the proper scope of any asserted claim or the proper construction of any asserted claim. Respondents reserve the right to modify, amend, or supplement these contentions as additional information becomes available.

² All statutory citations refer to AIA law.

As illustrated below, one or more claims of the '481 Patent are invalid as expressly and/or inherently anticipated by *Liu*, including asserted claims 1-4, 6, 9, and 17. Additionally, to the extent that *Liu* is found not to anticipate, expressly or inherently, claim 1 of the '481 Patent, it is invalid as obvious in view of *Liu* alone or in combination with other prior art references, including, but not limited to, the prior art discussed below, the prior art identified in the Respondents' Invalidity Contentions, and the prior art described in additional claim charts attached as Appendices A-1 through A-5. Exemplary invalidity grounds based on the *Liu* reference include the following, although these examples are by no means limiting:

- Obviousness based on *Liu* in combination with the knowledge of a skilled artisan (claims 1, 2, 4, and 6);
- Obviousness based on *Liu* in combination with Roberts (claims 3 and 17);
- Obviousness based on *Liu* in combination with Otremba433 (claims 4 and 9);
- Obviousness based on *Liu* in combination with Otremba124 (claims 4 and 9);
- Obviousness based on *Liu* in combination with Roberts and Otremba433 (claim 17).

The citations included in the table below are exemplary only and are not intended to be limiting or exhaustive. Respondents reserve the right to cite additional disclosures and evidence in support of their positions as the Investigation develops further.

Additionally, Respondents may be basing the arguments below on claim interpretations suggested in Complainant's infringement and domestic industry claim charts provided with the Complaint, as best as they can be deciphered. By applying the prior art in this way, Respondents do not concede their agreement with Complainant's positions, nor do these Invalidity Contentions constitute any admission regarding claim scope. Nor are Respondents asserting any claim construction positions through these charts. Moreover, preambles generally are not limiting, and nothing in these contentions should be deemed an admission that the preamble in the asserted claims is limiting.

As these proceedings further develop, Respondents intend to amend or supplement these exemplary disclosures and any related contentions as appropriate, and in a manner consistent with all applicable rules governing this Investigation. In particular, Respondents reserve the right to rely on (1) uncited portions of the identified prior art; (2) other prior art not identified herein; (3) references that show the state of the art (irrespective of whether such references themselves qualify as prior art to the asserted patents); (4) factual testimony from the named inventors or authors of the prior art references; and/or (5) expert testimony, to provide context to or aid in understanding the prior art and the state of the art at the time of the alleged inventions.

Descriptions of Exemplary Obviousness Combinations Based on *Liu*

All references are analogous because a POSITA would have understood that they are in the same field of endeavor as the '481 patent—packaging semiconductor electronic components. *Liu*, Abstract, 8:27-40, Figs. 11-12; Roberts, [0006], [0008], [0012], [0056]; Otremba124, [0041], Fig. 1; Otremba433, [0037], [0039], [0072], Fig. 2; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). Because a POSITA would have understood that they are all directed to the same type of packaging semiconductor electronic components and problems associated with those devices, a person of ordinary skill in the art would have further appreciated that *Liu* and the additional references cited below come from the same field of endeavor and provide disclosures that relate to one another.

The combination of *Liu* with one or more of the additional references would involve one or more of: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; use of a known technique to improve similar devices in the same way; applying a known technique to the device ready for improvement to yield predictable results; obvious trying given a finite number of identified, predictable solutions, and a reasonable expectation of success; known work in one field of endeavor that prompts variations for use in the same field based on design incentives or market forces; and a teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at claims 1-4, 6, 9, and 17.

For example, a POSITA would have understood *Liu*'s compound semiconductor device would have achieved at least 400V and a switching frequency capability of at least 100 kHz, which were common for compound semiconductor power conversion transistors designed for high voltage applications, as disclosed by Roberts. *See also* Huang (Innoscence1414-00007460 – Innoscence1414-00007465). Although *Liu* does not expressly disclose its device's voltage locking and switching speed, as explained for claim 3, Ground 1A, Roberts explains that these characteristics were common. Roberts, [0006], [0008], [0012]. A POSITA would have understood that a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz were standard, routine, and readily-achievable characteristics for compound semiconductor transistors designed for high-voltage applications (like *Liu*) and were the very benefits of compound semiconductor devices. Because *Liu* expressly discloses compound semiconductor transistor devices but is silent on corresponding switching time or frequency, a POSITA would have been motivated to look to references that disclose expected switching time or frequencies for other compound semiconductor devices to better understand or interpret the achievable characteristics of *Liu*'s device, including high-voltage application GaN transistor devices like in Roberts. Because these characteristics were well known, a POSITA would have had a reasonable expectation of success in operating *Liu*'s compound semiconductor transistor device with a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

Additionally, Otremba433 discloses a “leadless package” with contacts and a die pad exposed on the bottom of the devices (Otremba433, [0037], [0039]), as was commonly known (Otremba280, 4:17-29). A POSITA would have understood *Liu*'s device would be readily

implemented in the leadless package of Otremba433 because package designs were easily modifiable to meet the needs of a particular use. *Liu* implements a leaded package, but a POSITA would have realized the known benefits of leadless package designs. Leadless package designs saved space on the printed circuit board and showed faster performance and switching speeds than through-hole and other conventional packages, enabling improved performance, switching behavior, ease of use, EMI, reliability, and higher power density. A POSITA would have understood the known benefits a leadless package as improvement to *Liu*'s device ready for such improvement—combining prior art elements using known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416. And leadless packaging types were known, including those with source sensing leads, like a DFN8x8 package.

A POSITA would have been motivated to package *Liu*'s semiconductor device in the Otremba124's ThinPAK8x8 package with an exposed die pad and planar lead contacts on the lower surface because, as explained for claim 4, ThinPAK8x8 was boasted as an improvement over leaded packaging designs, saving space on the printed circuit board (PCB), and having faster performance and switching speeds enabling improved performance, switching behavior, ease of use, EMI, reliability, and higher power density. ThinPAK 8x8 New High Voltage SMD-Package ("ThinPAK8x8 Brochure") (Innoscience1414-00007539 - Innoscience1414-00007572), 3. Because *Liu* implements a leaded package design, a POSITA would have realized the benefits ThinPAK8x8 offered as improvements over *Liu*'s device. Lind even shows ThinPAK8x8 with source sensing connections as an alternative to a leaded package. Lind (Innoscience1414-00007466 - Innoscience1414-00007471). Packaging *Liu* as Otremba124's ThinPAK8x8 would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416. Additional package formats, including leadless, exposed-die packages were known, as taught by Otremba433 and Otremba400, and would have been at least considered suitable options for packaging *Liu*'s device. *Intel*, 21 F.4th at 800; *PAR Pharm.*, 773 F.3d at 1197-98. Otremba433 recognizes that leaded and leadless packages were suitable alternatives. Otremba433, [0025]. Additionally, ThinPAK8x8 was a well known leadless package design and included leads and a die pad exposed on the lower surface and forming planar contacts (i.e., a leadless design). ThinPAK8x8 Brochure, 1, 5, 6; Recommendations for Printed Circuit Board Assembly of Infineon VDSO Packages (ThinPAK) ("ThinPAK Recommendations") (Innoscience1414-00007573 - Innoscience1414-00007599), 1, 4.

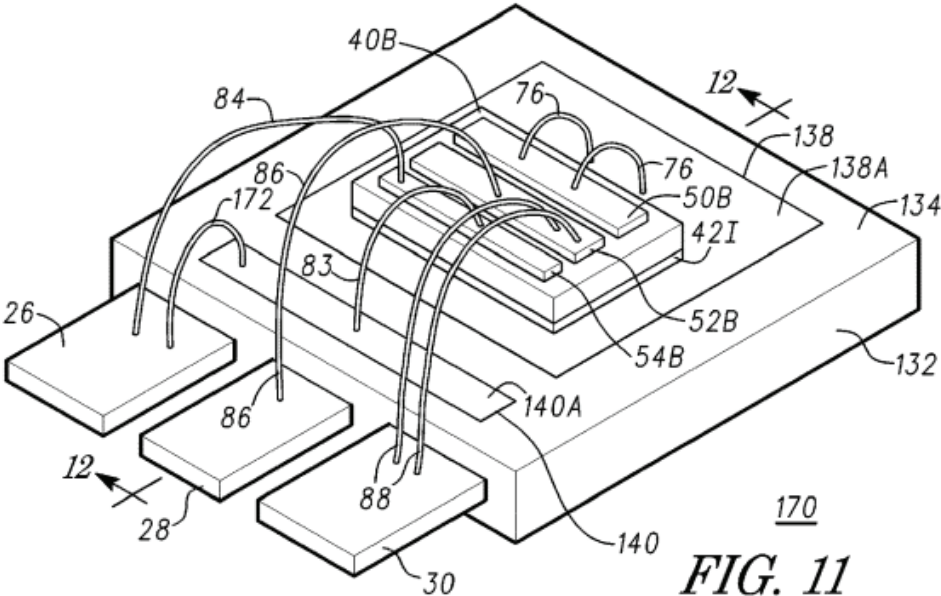
***Liu*'s Priority Date Based on Its Provisional Application**

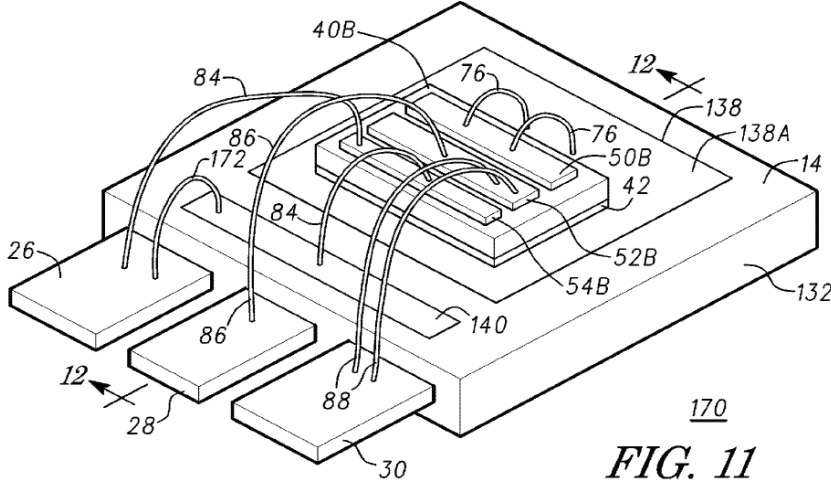
Liu claims priority to *Liu Provisional*, filed July 24, 2015. Because the subject matter of *Liu* Respondents rely on is supported by the Provisional, *Liu* was effectively filed under 35 U.S.C. §102(d)(2) "as of the filing date of the earliest such application that describes the subject matter"—July 24, 2015. A representative claim of *Liu* is supported by *Liu Provisional*. *Dynamic Drinkware, LLC v. Nat'l*

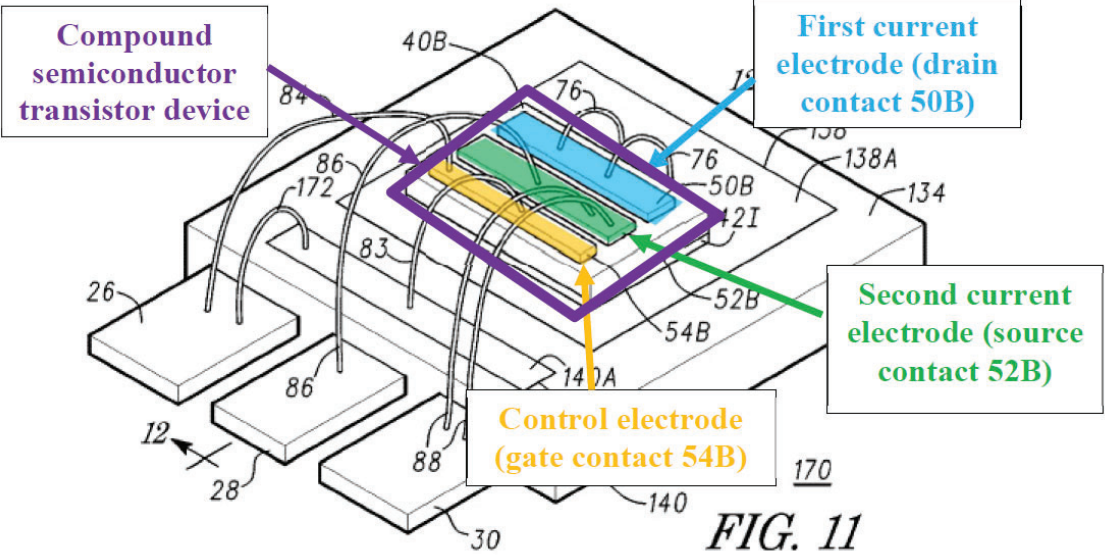
Graphics, Inc., 800 F.3d 1375 (Fed. Cir. 2015); *see also Innoscience America, Inc. v. Infineon Technologies Austria AG*, IPR2024-00975, Paper 1 (June 14, 2024) (Innoscience1414-00013776-Innoscience1414-00013910).

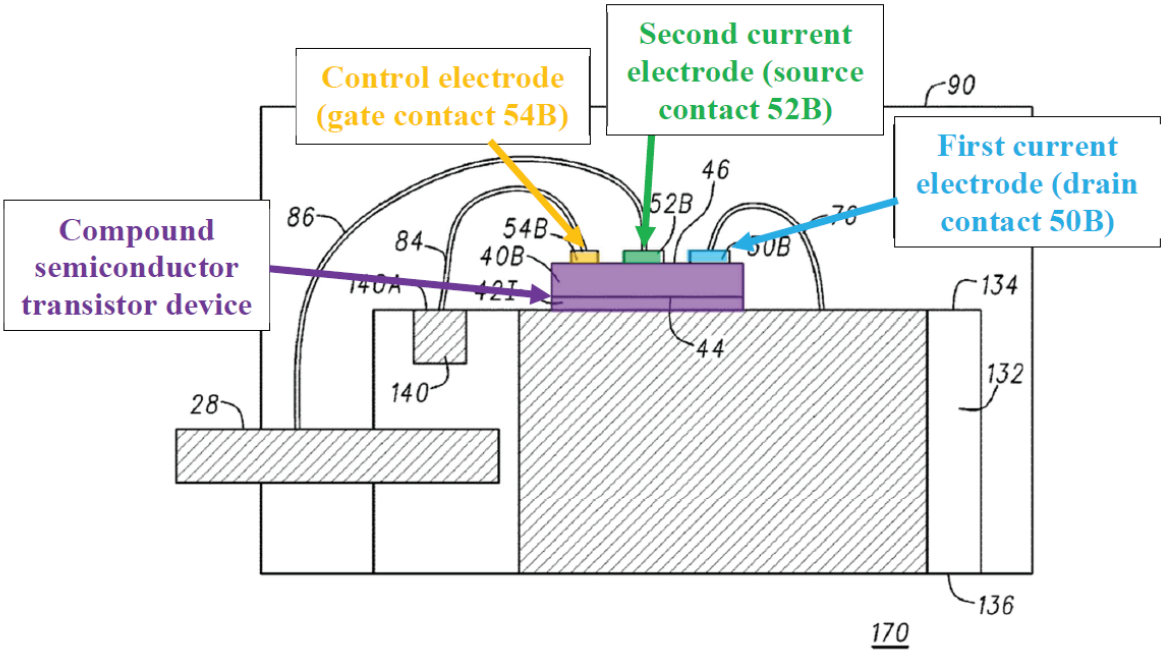
Liu and *Liu Provisional* are nearly identical. Every figure of *Liu* appears in *Liu Provisional*, and all *Liu*'s cited disclosures are identical or nearly identical to *Liu Provisional*. The Figures of both *Liu* and its Provisional have only minor variations in numbers (e.g., 42I in *Liu* Figure 11 corresponds to 42 in Provisional Figure 11, 42I in *Liu* Figure 12 corresponds to 56 in Provisional Figure 12, and 90 in *Liu* Figure 12 corresponds to 133 in Provisional Figure 12).

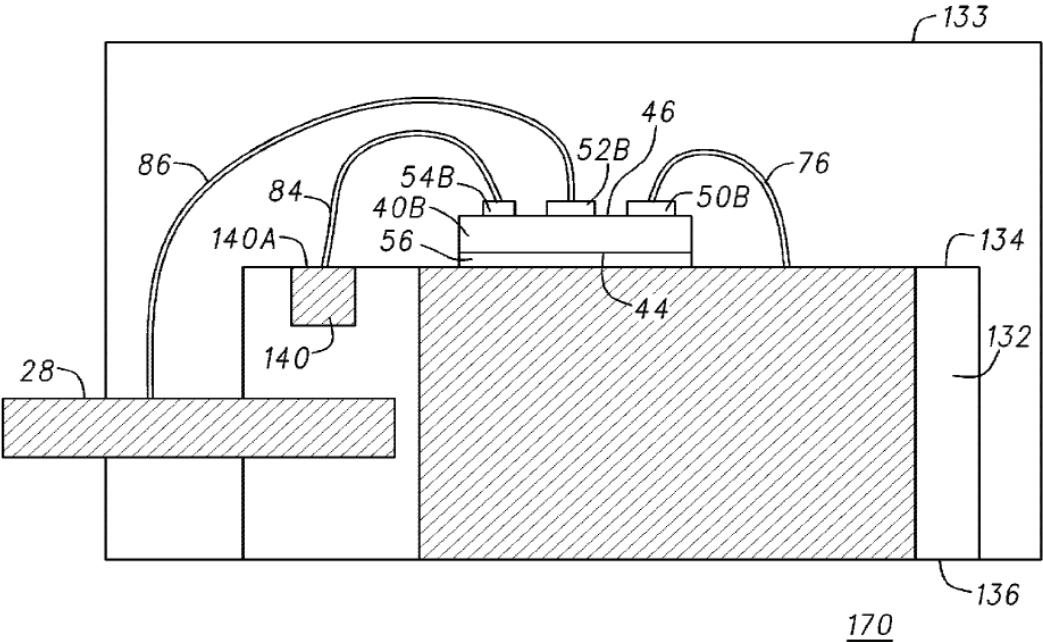
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>[1p] An electronic component, comprising:</p>	<p>To the extent the preamble is limiting, <i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious an electronic component.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 8:1-10</p> <p style="padding-left: 40px;">FIG. 11 is a perspective view of a semiconductor component 170 in accordance with another embodiment of the present invention. FIG. 12 is a cross-sectional view of semiconductor component 170 taken along section line 12-12 of FIG. 11. FIGS. 11 and 12 are described together. What is shown in FIGS. 11 and 12 are a molded device support structure 132 that includes device receiving area 138 and bond pad 140, and leadframe leads 26, 28, and 30. Molded device support structure 132 has been described with reference to FIGS. 6 and 7.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:56-59; 4:60-5:7; 5:14-30; 5:36-64; 6:47-7:8; 7:14-32; 7:39-62; 8:49-9:10</p> <p><i>Liu</i> discloses the following at Fig. 11</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 11</p> <p><i>Liu Provisional</i> discloses the following at [00041]</p> <p>FIG. 11 is a perspective view of a semiconductor component 170 in accordance with another embodiment of the present invention. FIG. 12 is a crosssectional view of semiconductor component 170 taken along section line 12-12 of FIG. 11. FIGs. 11 and 12 are described together. What is shown in FIGs. 11 and 12 are a molded device support structure 132 that includes device receiving area 138 and bond pad 140, and leadframe leads 26, 28, and 30. Molded device support structure 132 has been described with reference to FIGs. 6 and 7.</p> <p><i>See also Liu Provisional</i>, [00020], [00026]- [00027], [00029], [00031], [00035], [00037], [00039], [00044]</p>

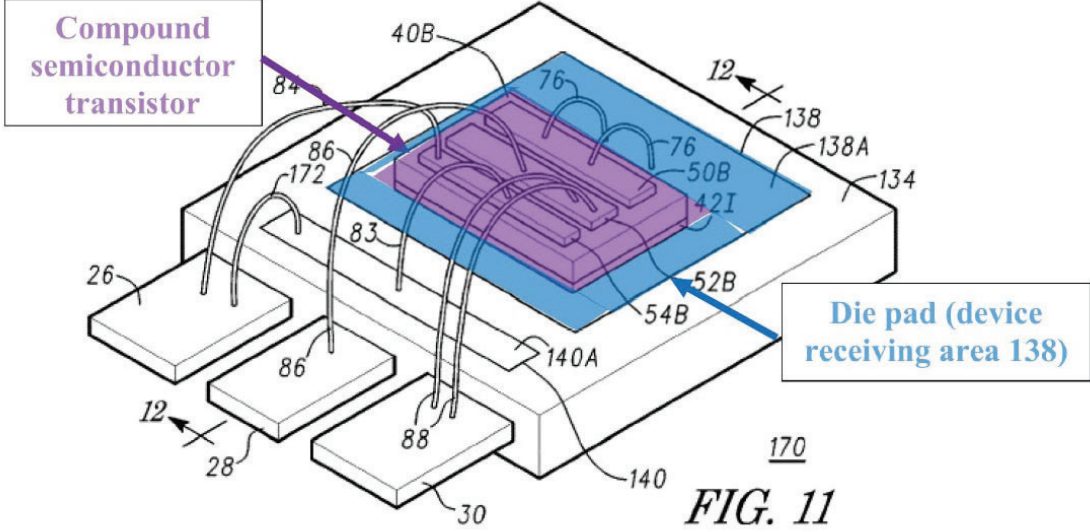
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p><i>Liu Provisional</i> discloses the following at Fig. 11</p>  <p style="text-align: center;">FIG. 11</p>
<p>[1a] a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;</p>	<p><i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 8:11-25</p> <p style="padding-left: 40px;">A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor</p>

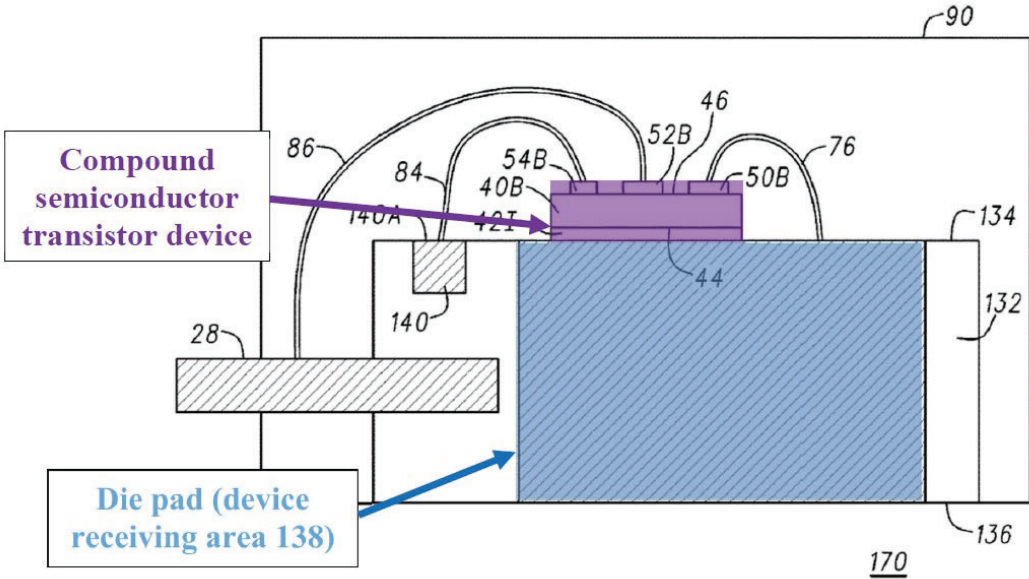
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>See also Liu</i>, 3:30-4:51; 5:65-6:41; 6:47-7:8; 7:14-32; 7:39-62; 8:27-9:10</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>  <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p> <p><i>Liu Provisional</i> discloses the following at [00042]</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact S4B</p>

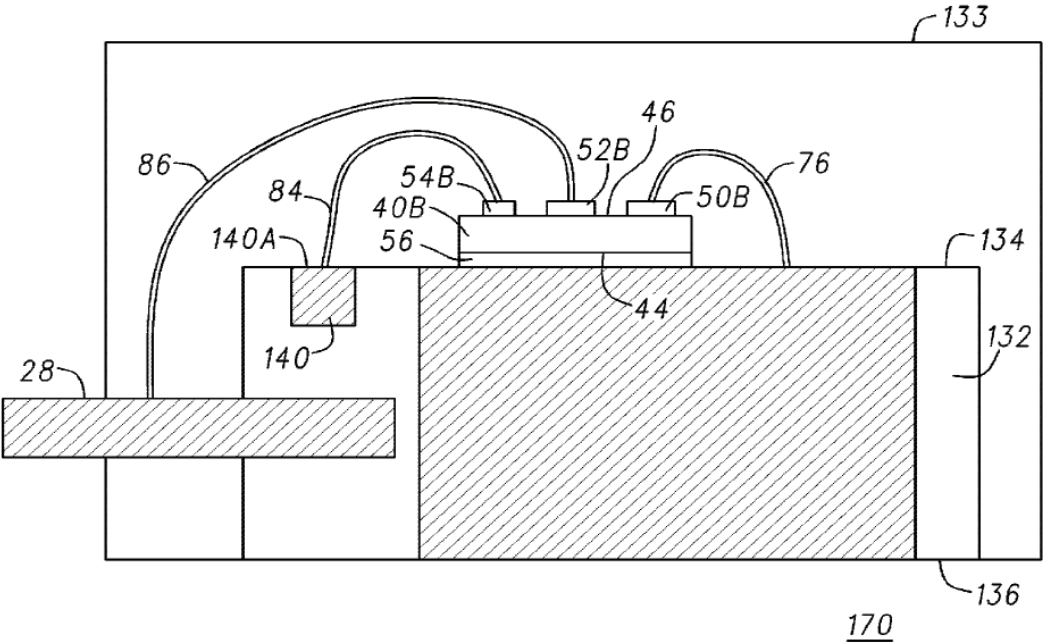
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p>
<p>[1b] a die pad; and</p>	<p><i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious a die pad.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 5:34-64</p> <p>FIG. 6 is a perspective view of a semiconductor component 130 in accordance with another embodiment of the present invention. FIG. 7 is a cross-sectional view of semiconductor component 130 taken along section line 7-7 of FIG. 6. FIGS. 6 and 7 are described together. What is shown in FIGS. 6 and 7 are a molded device support structure 132 having a top surface 134 and</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>a bottom surface 136. Molded support structure 132 includes a device receiving area 138, a bond pad 140 at top surface 134, and a contact 143 at bottom surface 136. In accordance with an embodiment, bond pads 138 and 140 are coplanar with surface 134. Leadframe leads 26, 28, and 30 protrude from a side or an edge of molded device support structure 132. Device receiving area 138 may be referred to as a device receiving structure. Molded support structure 132 may be formed by placing an electrically conductive strip in a mold having a mold cavity and injecting a mold compound into the mold cavity. The electrically conductive strip may include a pad or plate 138 having a contact region 140, wherein pad or plate 138 serves as a device receiving area, and a plurality of leadframe leads such as, for example, leadframe leads 26, 28, and 30. After injecting the mold compound into the cavities, the electrically conductive strip may be singulated into a plurality of molded support structures 132. Suitable materials for the electrically conductive strips include copper, aluminum, or the like. As mentioned, molded support structure 132 is illustrated and described as a single element; however, it may be a portion singulated from a leadframe strip encapsulated in a mold compound.</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>See also Liu</i>, at 2:62-3:29; 3:30-4:51; 4:60-5:33</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

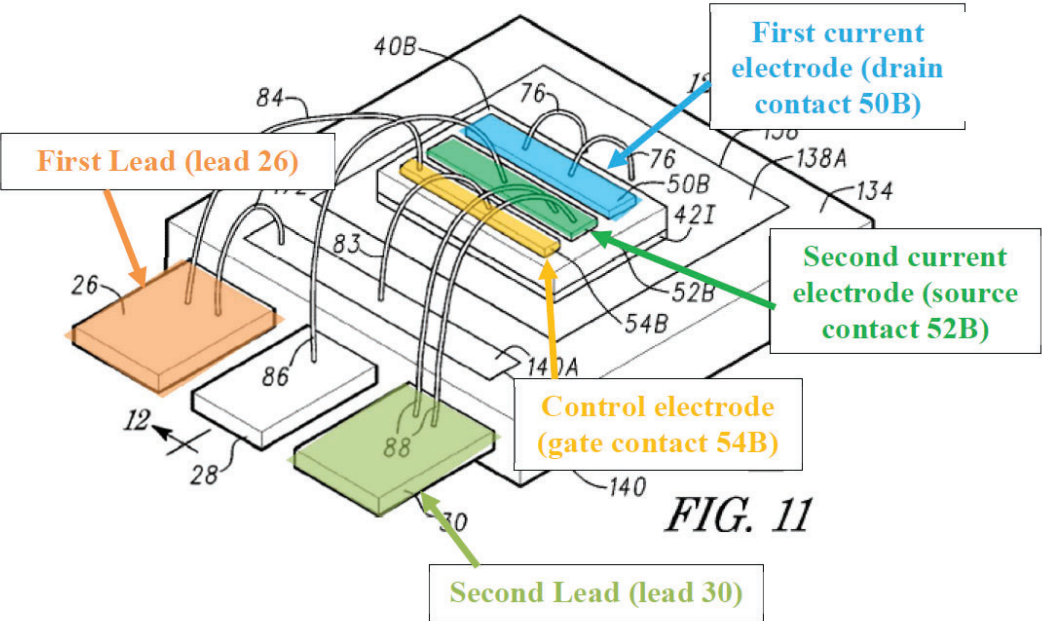
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>Compound semiconductor transistor</p> <p>Die pad (device receiving area 138)</p> <p>FIG. 11</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

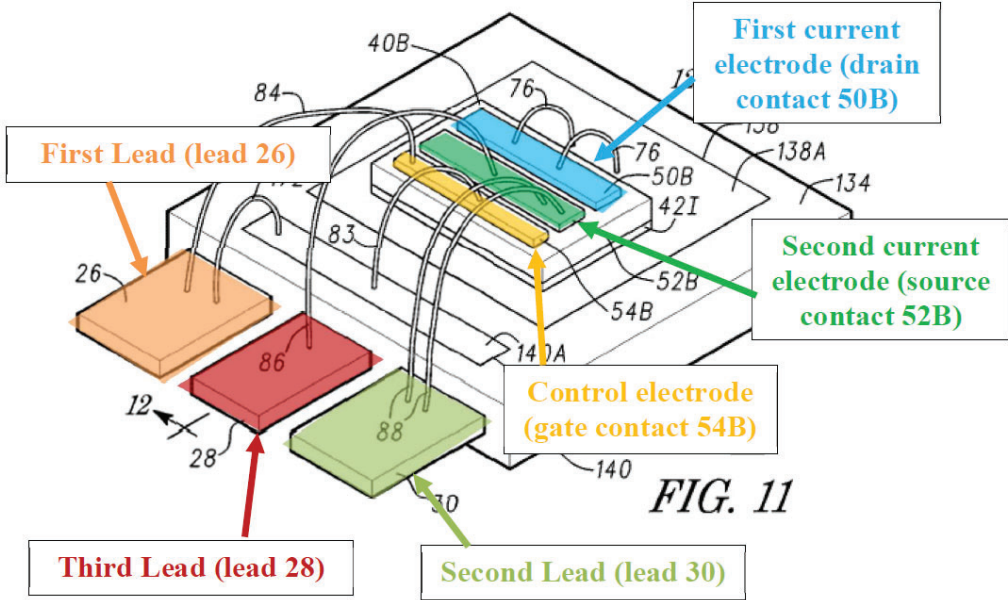
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p> <p><i>Liu Provisional</i> discloses the following at [00031]</p> <p>FIG. 6 is a perspective view of a semiconductor component 130 in accordance with another embodiment of the present invention. FIG. 7 is a crosssectional view of semiconductor component 130 taken along section line 7-7 of FIG. 6. FIGS. 6 and 7 are described together. What is shown in FIGS. 6 and 7 are a molded device support structure 132 having a top surface 134 and a bottom surface 136. Molded support structure 132 includes a device receiving area 138, a bond pad 140 at top surface 134, and a contact 142 at bottom surface 136. In accordance with an embodiment, bond pads 138 and 140 are coplanar with surface 134. Leadframe leads 26, 28, and 30 protrude from a side or an edge of molded device support structure 132. Device receiving area 138 may be referred to as a device receiving structure. Molded support structure 132 may be formed by placing an electrically conductive strip in a mold having a mold cavity and injecting a mold compound into the mold cavity. The</p>

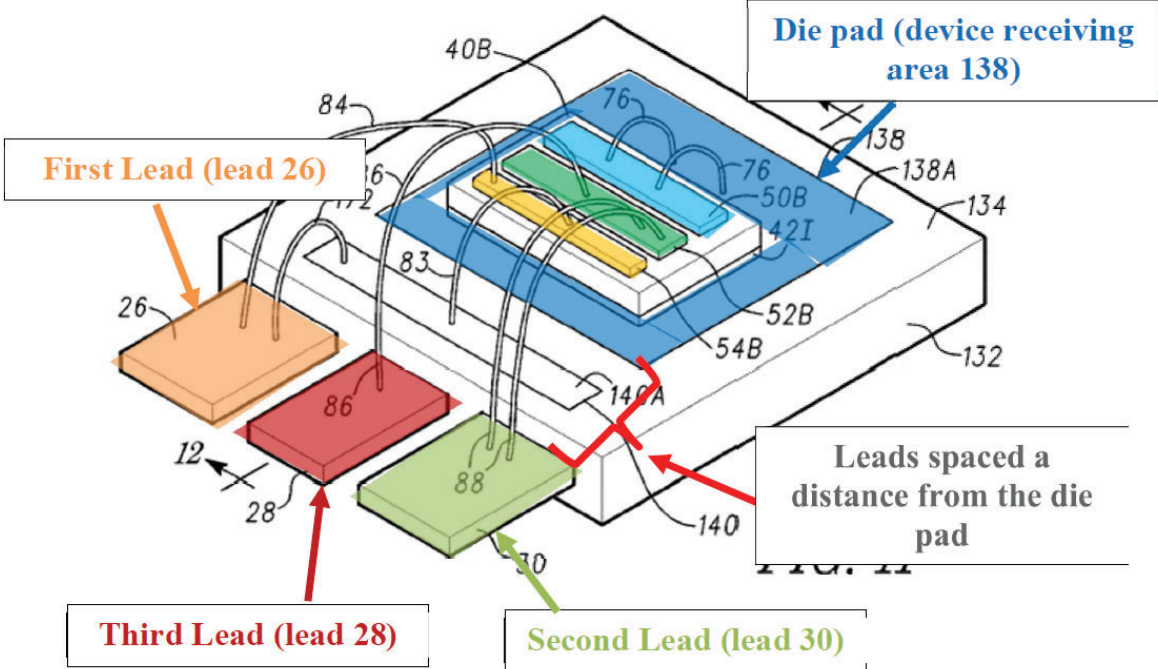
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>electrically conductive strip may include a pad or plate 138 having a contact region 140, wherein pad or plate 138 serves as a device receiving area, and a plurality of leadframe leads such as, for example, leadframe leads 26, 28, and 30. After injecting the mold compound into the cavities, the electrically conductive strip may be singulated into a plurality of molded support structures 132. Suitable materials for the electrically conductive strips include copper, aluminum, or the like. As mentioned, molded support structure 132 is illustrated and described as a single element; however, it may be a portion singulated from a leadframe strip encapsulated in a mold compound.</p> <p><i>Liu Provisional</i> discloses the following at [00042]</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact S4B formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>See also Liu Provisional</i>, [00021]- [00022]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

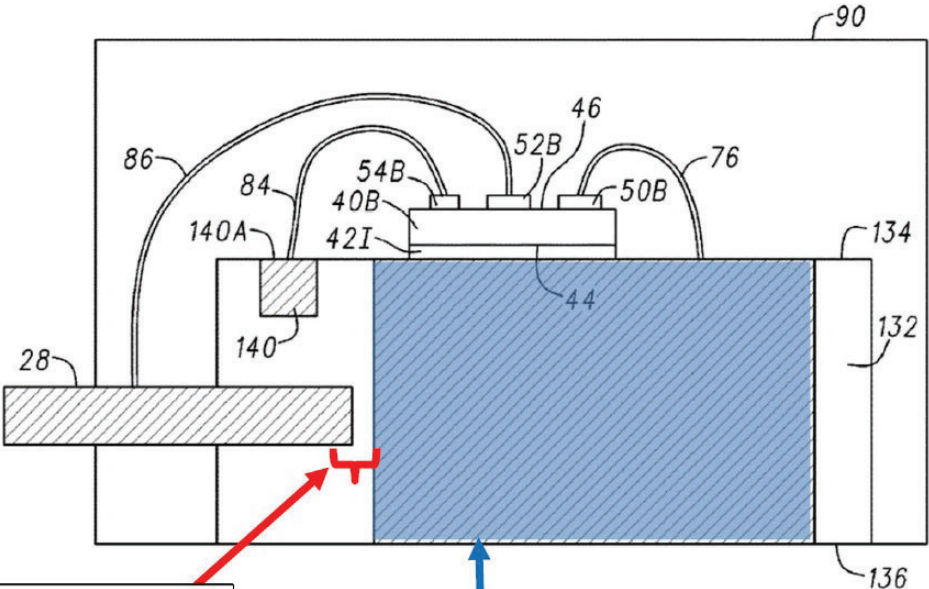
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p>
<p>[1c] a first lead, a second lead and a third lead,</p>	<p><i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious a first lead, a second lead and a third lead.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p style="padding-left: 40px;">A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:20-52; 4:56-59; 5:36-64; 6:20-41; 6:47-7:8; 8:1-10; 8:49-9:10</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

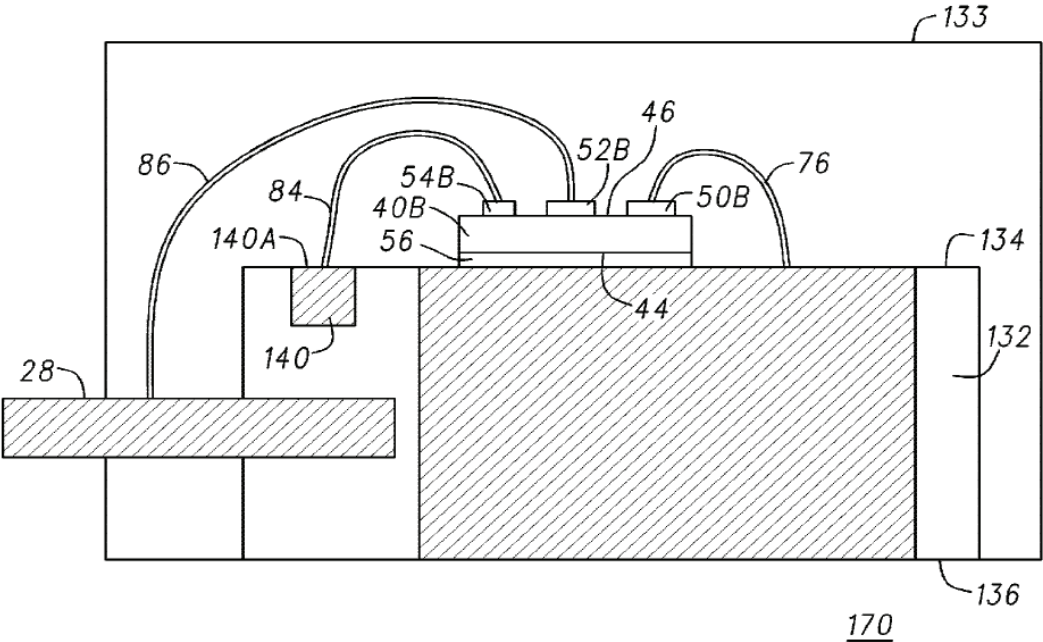
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>Second Lead (lead 30)</p> <p>FIG. 11</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>FIG. 11</p>

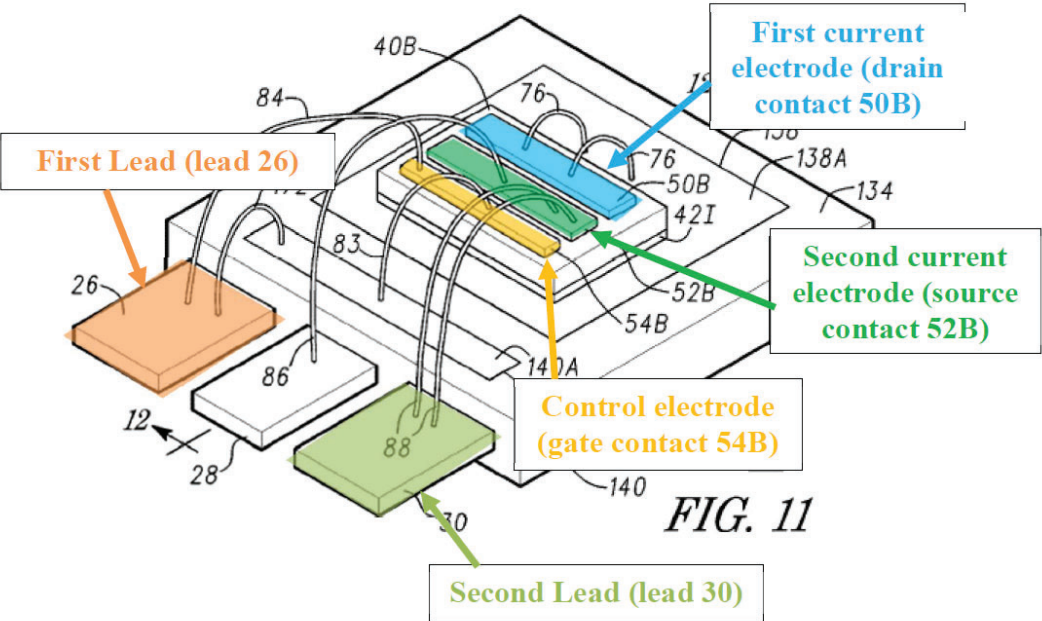
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>Die pad (device receiving area 138)</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p>Leads spaced a distance from the die pad</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

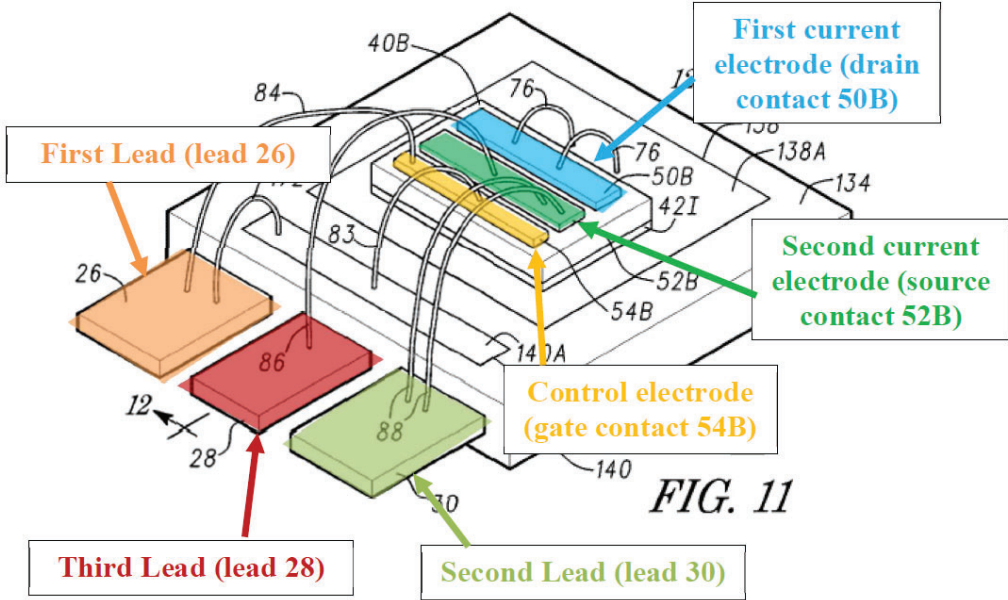
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p data-bbox="525 852 913 990">Leads spaced at a distance from the die pad</p> <p data-bbox="987 852 1323 966">Die pad (device receiving area 138)</p> <p data-bbox="1333 909 1501 966">FIG. 12</p> <p data-bbox="489 1052 1129 1088"><i>Liu Provisional</i> discloses the following at [00042]</p> <p data-bbox="583 1123 1883 1409">A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact 54B</p>

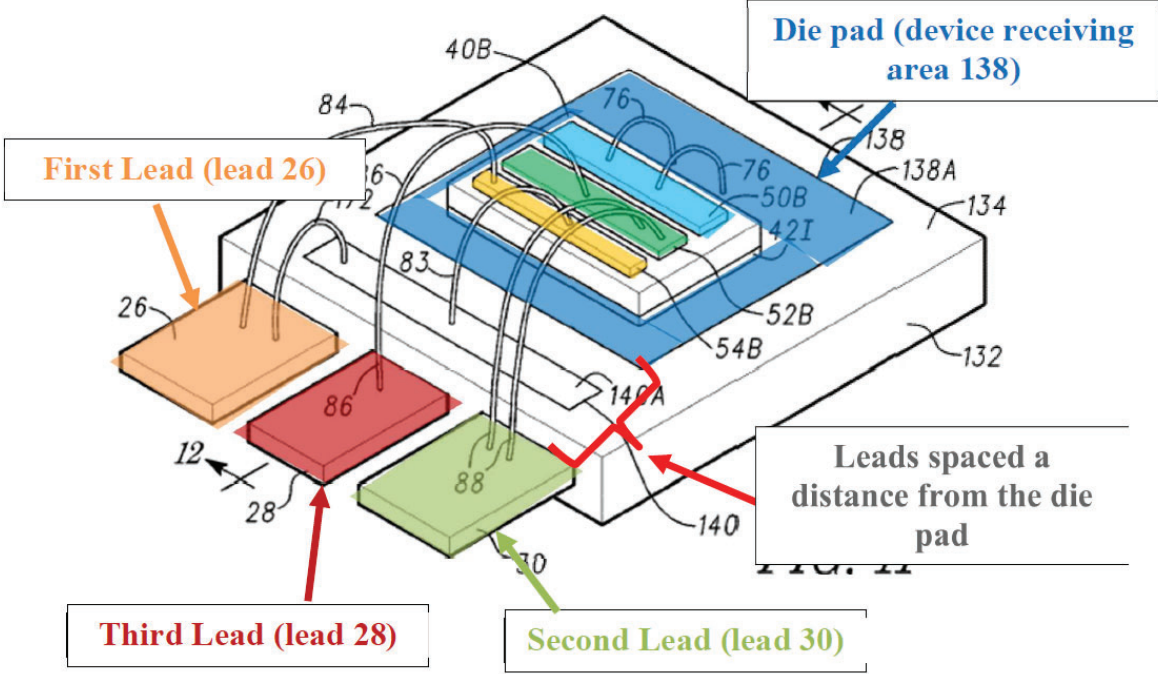
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00020], [00023]-[00024], [00026], [00031], [00033], [00035], [00041], [00044]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

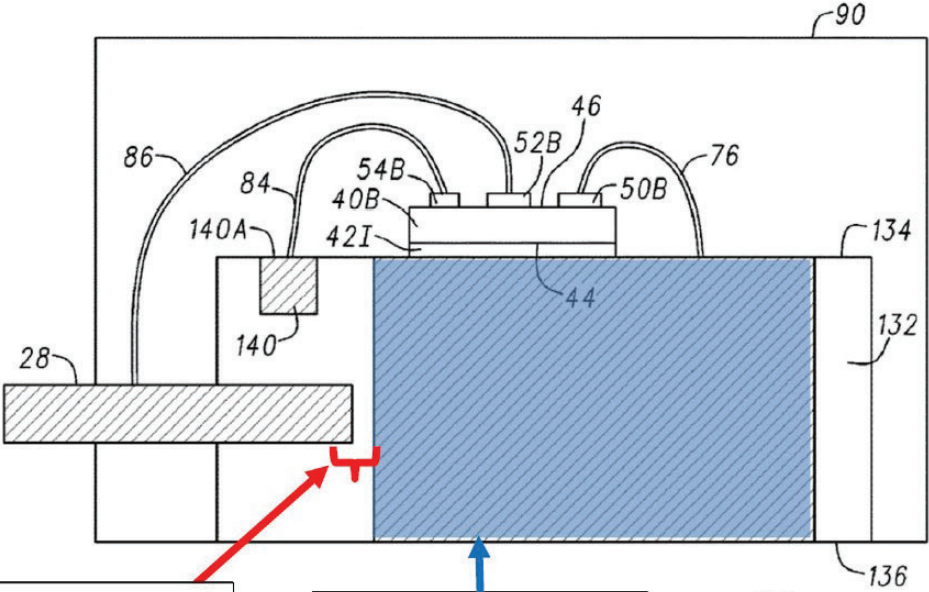
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p>
<p>[1d] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,</p>	<p><i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p style="padding-left: 40px;">A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:20-52; 4:56-59; 5:36-64; 6:20-41; 6:47-7:8; 8:1-10; 8:49-10</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

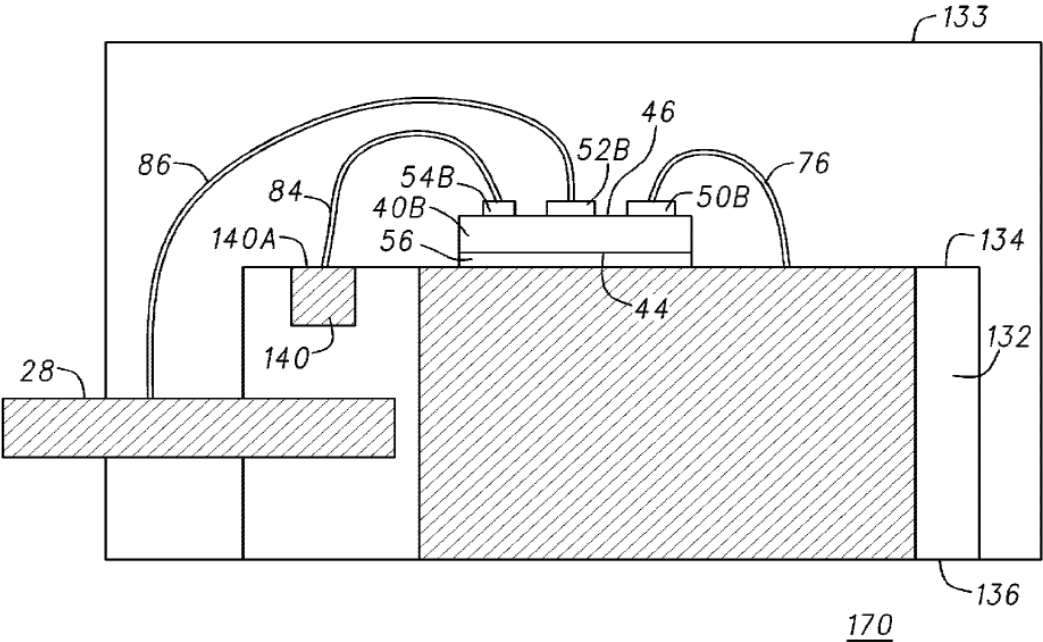
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>Second Lead (lead 30)</p> <p>FIG. 11</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>FIG. 11</p>

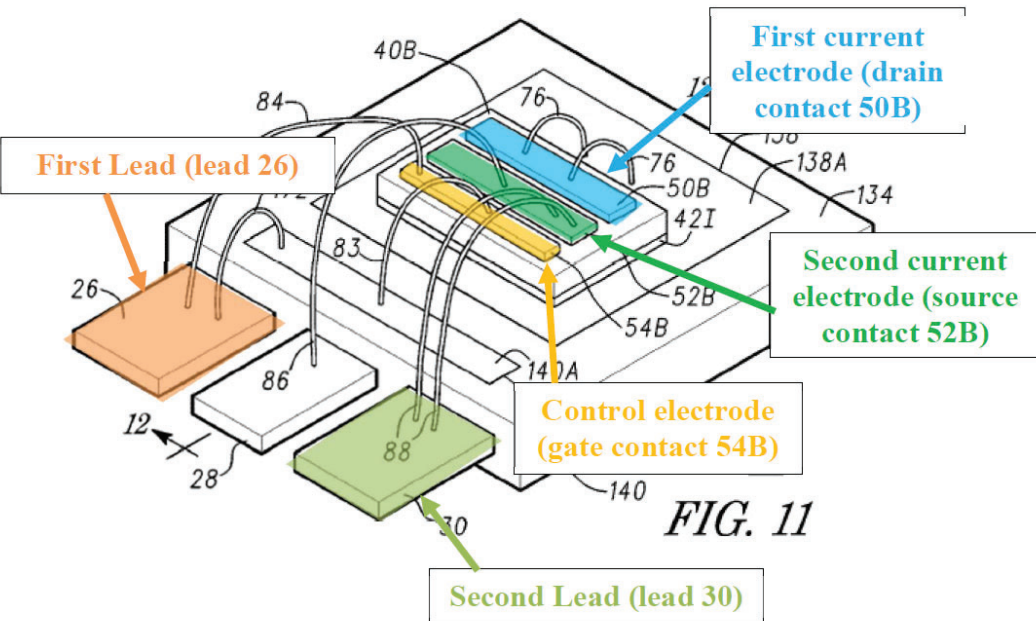
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p>Die pad (device receiving area 138)</p> <p>Leads spaced a distance from the die pad</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

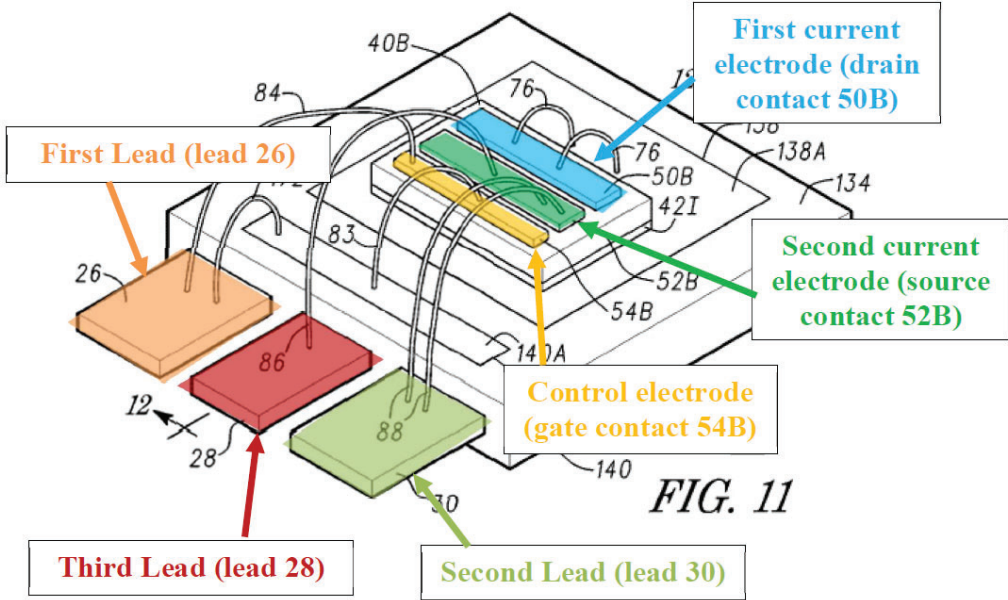
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p data-bbox="522 849 911 992">Leads spaced at a distance from the die pad</p> <p data-bbox="989 857 1320 963">Die pad (device receiving area 138)</p> <p data-bbox="1331 911 1503 963">FIG. 12</p> <p data-bbox="489 1052 1129 1089"><i>Liu Provisional</i> discloses the following at [00042]</p> <p data-bbox="583 1122 1883 1409">A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact 54B</p>

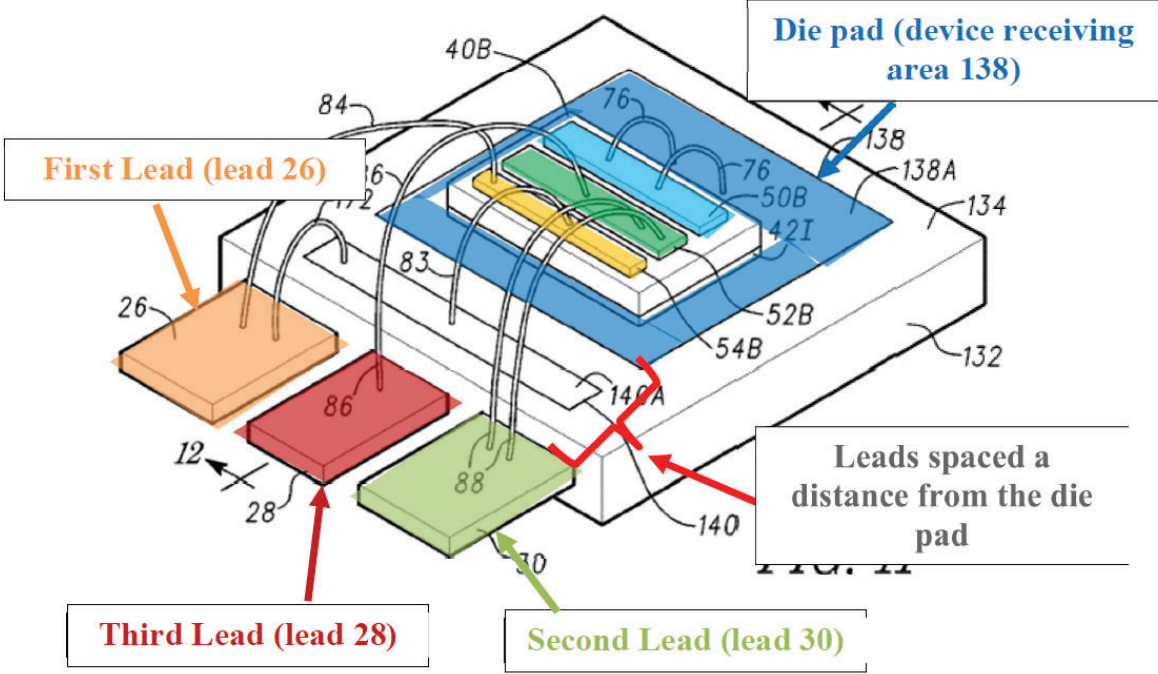
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00020], [00023]-[00024], [00026], [00031], [00033], [00035], [00041], [00044]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p>
<p>[1e] wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality.</p>	<p><i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality.</p> <p>For example,</p>

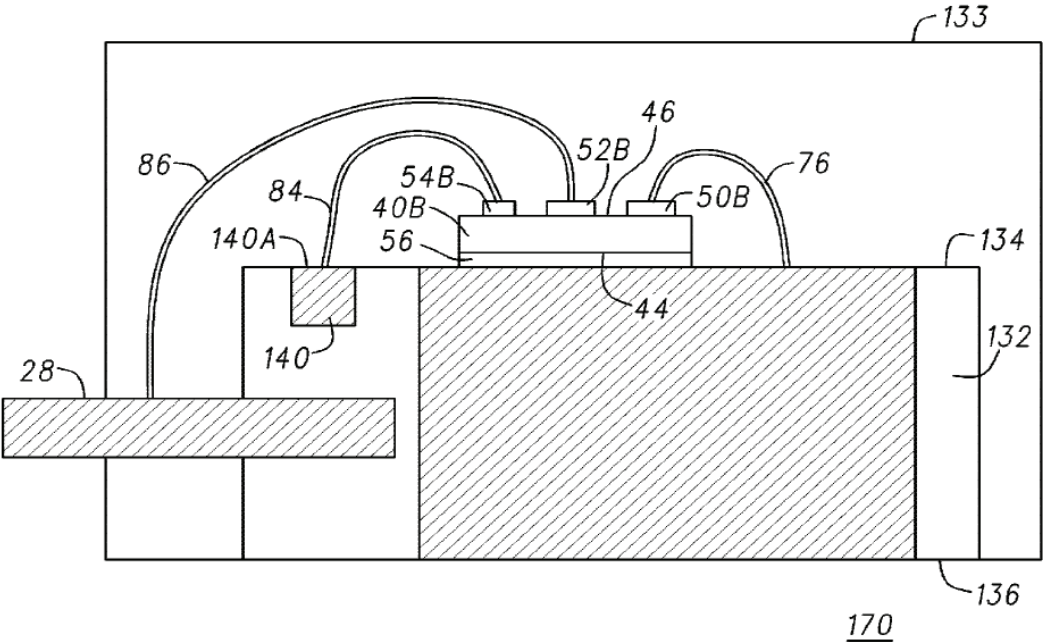
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,</p>	<p><i>Liu</i> discloses the following at 8:11-26</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:20-52; 4:56-59; 5:36-64; 6:20-41; 6:47-7:8; 8:1-10; 8:49-9:10</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>  <p>FIG. 11</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p>FIG. 11</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p>Die pad (device receiving area 138)</p> <p>Leads spaced a distance from the die pad</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

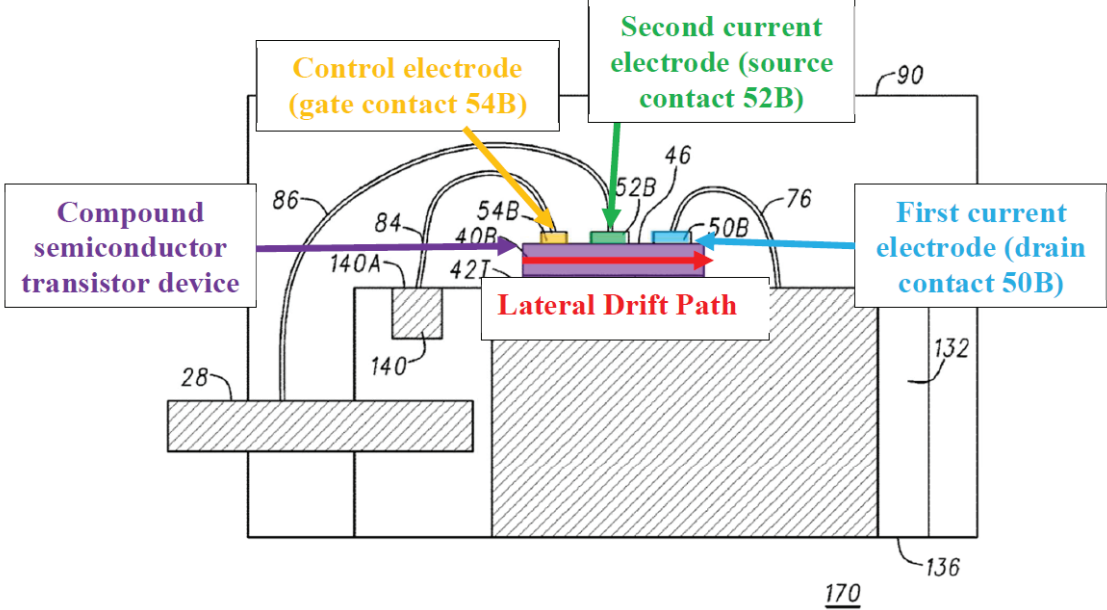
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00020], [00023]-[00024], [00026], [00031], [00033], [00035], [00041], [00044]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

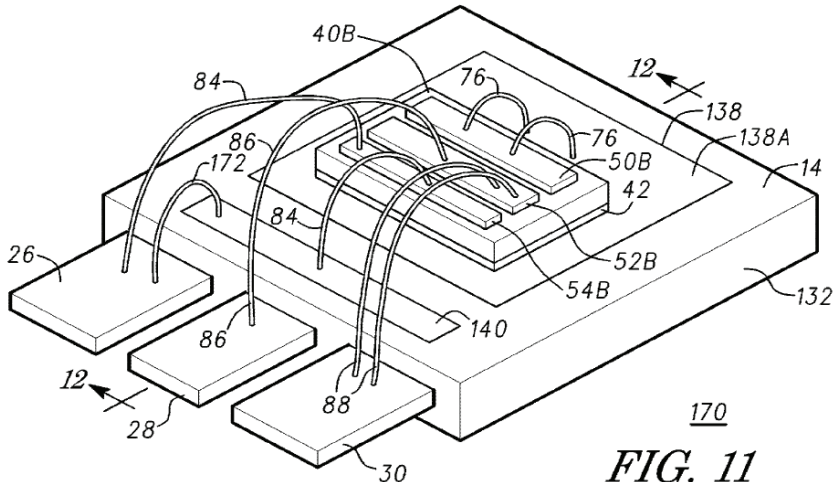
Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p>
<p>[1f] wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound</p>	<p><i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad,</p> <p>For example,</p> <p><i>Liu</i> discloses that the compound semiconductor transistor device is a lateral transistor because the device is arranged laterally with the electrodes on the same lateral plane in a lateral drift path with the current generally</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
semiconductor transistor device is coupled to the die pad,	<p>flowing parallel to the surface. The '481 patent explains that “lateral” means “run[ning] generally parallel to the lateral extent of a semiconductor material or semiconductor carrier” ('481 patent, 3:14-18) and describes a device that “has a lateral drift path” ('481 patent, 4:37-38). Smart Power ICs (Innoscience 1414-00012740 – Innoscience 1414-00012823) defines a horizontal (i.e. lateral) transistor as a structure where “current enters and leaves the chip through the upper surface of the chip.” At 7.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.</p> <p>Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 3:30-4:41; 5:65-6:41; 6:47-7:8; 7:15-32</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Compound semiconductor transistor device</p> <p>Lateral Drift Path</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>FIG. 11</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<div data-bbox="525 292 1780 1153"> <p>First current electrode (drain contact 50B) coupled to die pad (device receiving area 138) by a plurality of bond wires (76)</p> <p>FIG. 11</p> </div> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus,</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00021]-[00023], [00032]-[00033], [00035], [00037], [00039], [00042]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>  <p>FIG. 11</p> <p><i>Liu Provisional</i> discloses the following at Fig. 12</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
wires or a contact clip.	<p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 4:20-41; 4:60-5:7; 5:14-30; 6:20-41; 6:47-7:8; 7:39-62; 8:49-9:10</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

Claim 1	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00023], [00027], [00029], [00033], [00035], [00039]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

Claim 2	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
semiconductor transistor device and a Group III-nitride transistor device.	<p><i>Liu</i> discloses the following at 3:30-61</p> <p>A semiconductor chip 40 is bonded to surface 18A of device receiving area 18 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. More particularly, surface 44 of semiconductor chip 40 is bonded to surface 18A of device receiving area 18 through electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40 is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40 includes a field effect semiconductor device having a drain contact 50 formed on or from a portion of surface 46, a source contact 52 formed on or from another portion of surface 46, and gate contacts 54 and 55 formed on or from other portions of surface 46. It should be noted that the semiconductor device is not limited to being a field effect transistor. For example, the semiconductor device may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. In accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 40, semiconductor chip 40 may be referred to as a semiconductor device. In addition, die attach material 42 is not limited to being an electrically conductive material but may be an electrically insulating material or a thermally conductive material. By way of example, semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride. A III-nitride semiconductor material may be referred to as a III-N semiconductor material, a III-nitride based semiconductor material, a III-N based semiconductor material, or the like.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:52-59; 4:60-5:7; 5:14-30; 6:20-41; 6:47-7:8; 7:14-33; 7:39-62; 8:27-9:10</p> <p><i>Liu Provisional</i> discloses the following at [00021]</p> <p>A semiconductor chip 40 is bonded to surface 18A of device receiving area 18 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. More particularly, surface 44 of semiconductor chip 40 is bonded to surface 18A of device receiving area 18 through electrically insulating die attach material 42.</p>

Claim 2	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>In accordance with an embodiment, semiconductor chip 40 is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40 includes a field effect semiconductor device having a drain contact 50 formed on or from a portion of surface 46, a source contact 52 formed on or from another portion of surface 46, and gate contacts 54 and 55 formed on or from other portions of surface 46. It should be noted that semiconductor device 48 is not limited to being a field effect transistor. For example, semiconductor device 48 may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. In accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 40, semiconductor chip 40 may be referred to as a semiconductor device. In addition, die attach material 42 is not limited to being an electrically conductive material but may be an electrically insulating material or a thermally conductive material. By way of example, semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride. A III-nitride semiconductor material may be referred to as a III-N semiconductor material, a III-nitride based semiconductor material, a III-N based semiconductor material, or the like.</p> <p><i>See also Liu Provisional</i>, [00020]-[00021], [00025], [00027], [00029], [00033], [00035], [00037], [00039], [00043]</p>
Claim 3	Exemplary Disclosure based on <i>LIU</i> and Related Combinations
[3p] The electronic component of claim 1,	<i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious the electronic component according to claim 1. <i>See supra</i> claim 1.
[3a] wherein the compound semiconductor transistor device has a blocking voltage capability	<p><i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.</p> <p>For example,</p>

Claim 3	Exemplary Disclosure based on <i>LIU</i> and Related Combinations
<p>of at least 400V and a switching frequency capability of at least 100 kHz.</p>	<p>A person of ordinary skill would have understood that the compound semiconductor transistor device disclosed in <i>Liu</i> would have achieved at least 400V and a switching frequency capability of at least 100kHz, which were common for compound semiconductor power conversion transistors designed for high-voltage applications. <i>See</i> Huang at 114, describing the switching speeds of GaN devices.</p> <p>Huang discloses the following at 114</p> <p>The switching speed of GaN devices is much faster than comparable Si MOSFET which makes the packaging even more critical to achieve lower loss and less ringing during switching transition. The impact of the packaging parasitics on cascode GaN devices has been investigated in [4-5]. The common source inductance and inter-connected inductance are detrimental to switching loss and gate reliability. TO220 and DFN packages are typically used for high voltage e-mode GaN devices. Fig. 2 shows the package-related parasitic inductance and the value is listed in Table II which are extracted by FEA simulation in Ansoft Q3D. With Kelvin connection, the DFN package is able to decouple the power loop and driving loop, and therefore it can minimize the common source inductance. Moreover, the inductance of DFN package is much smaller than TO220 package which also helps to reduce the loss and ringing issue.</p> <div data-bbox="619 868 1123 1193" data-label="Diagram"> </div> <p>Fig. 2 Packaging related parasitic inductance</p>

Claim 3	Exemplary Disclosure based on <i>LIU</i> and Related Combinations															
	<p>TABLE II. PACKAGE-RELATED PARASITIC INDUCTANCE VALUES</p> <table><tr><td></td><td>L_G</td><td>L_D</td><td>L_S</td><td>L_K</td></tr><tr><td>TO220</td><td>3.6nH</td><td>2.3nH</td><td>3.9nH</td><td>N/A</td></tr><tr><td>DFN 8x8</td><td>2.4nH</td><td>1.3nH</td><td>0.9nH</td><td>1.3nH</td></tr></table> <p>The key experimental waveforms with two different packages are shown in Fig. 3. For the turn-on transition, the voltage and current slew rate of DFN package is much larger than that of TO220 package due to smaller common source inductance and loop inductance. As a result, the turn-on energy of DFN package is much smaller than TO220 package as shown in Fig.5. For the turn-off transition, a severe ringing occurred in TO220 package. The false turn-on is observed at high current turn-off condition as shown in Fig. 4, and therefore, the turn-off energy of TO220 package increases dramatically with turn-off current.</p> <p>In addition, Roberts discloses a compound semiconductor transistor device with a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.</p> <p>Roberts discloses the following at [0006]</p> <p>GaN power transistors for power conversion circuits for high voltage (HV) applications, e.g. 600/650V, are typically normally-on (depletion mode) transistors. These transistors are usually driven by a series connected, discrete, power MOSFET device, i.e. in a cascode configuration, to provide normally-off operation (see FIG. 1). Conventionally, the hybrid cascode arrangement is provided with a separate, high power, high speed driver circuit, having a separate isolated power supply.</p> <p>Roberts discloses the following at [0008]</p> <p>The GaN transistor may be required, for example, to provide <20 ns switching time and more than 30 A current switching capability. Any significant series inductance at the MOSFET source or at the common node will provide unwanted $L di/dt$ transients which can be as large as the threshold voltage of the devices, thus causing unwanted switching. It will be appreciated that in operation of an electronic power switching system that is capable of switching, for example, 30 Amps at 1000V, i.e.</p>		L_G	L_D	L_S	L_K	TO220	3.6nH	2.3nH	3.9nH	N/A	DFN 8x8	2.4nH	1.3nH	0.9nH	1.3nH
	L_G	L_D	L_S	L_K												
TO220	3.6nH	2.3nH	3.9nH	N/A												
DFN 8x8	2.4nH	1.3nH	0.9nH	1.3nH												

Claim 3	Exemplary Disclosure based on <i>LIU</i> and Related Combinations
	<p>30,000 Watts, safe operation may be compromised by any unwanted switching caused by transients or noise that exceeds the threshold voltage of the device.</p> <p>Roberts discloses the following at [0012] GaN transistors that can switch, for example, 24 A (1200 V) and 47 A (650 V) may have die sizes as small as 2×2 mm Calculations show these die, when packaged, can have a thermal resistance of greater than 2° C./W. For example, it is estimated that, for an on-resistance of 80 mΩ, the ohmic power dissipation would be 32 Watts if the device were required to sink 20 Amps The thermal resistance in total for the combination of the device, package and heat sink could exceed 5° C./W, so that the temperature increase from the GaN device dissipation alone could exceed 150° C. The additional heat dissipation of the MOSFET, assuming a 20 mΩ device is used, would be 8 Watts. With the total structure dissipating 40 Watts, the temperature within the package could exceed the safe operating limits of the MOSFET, typically 175° C., if there is insufficient heat dissipation.</p> <p><i>See also</i> Roberts, [0003]-[0004], [0010], [0056]</p>

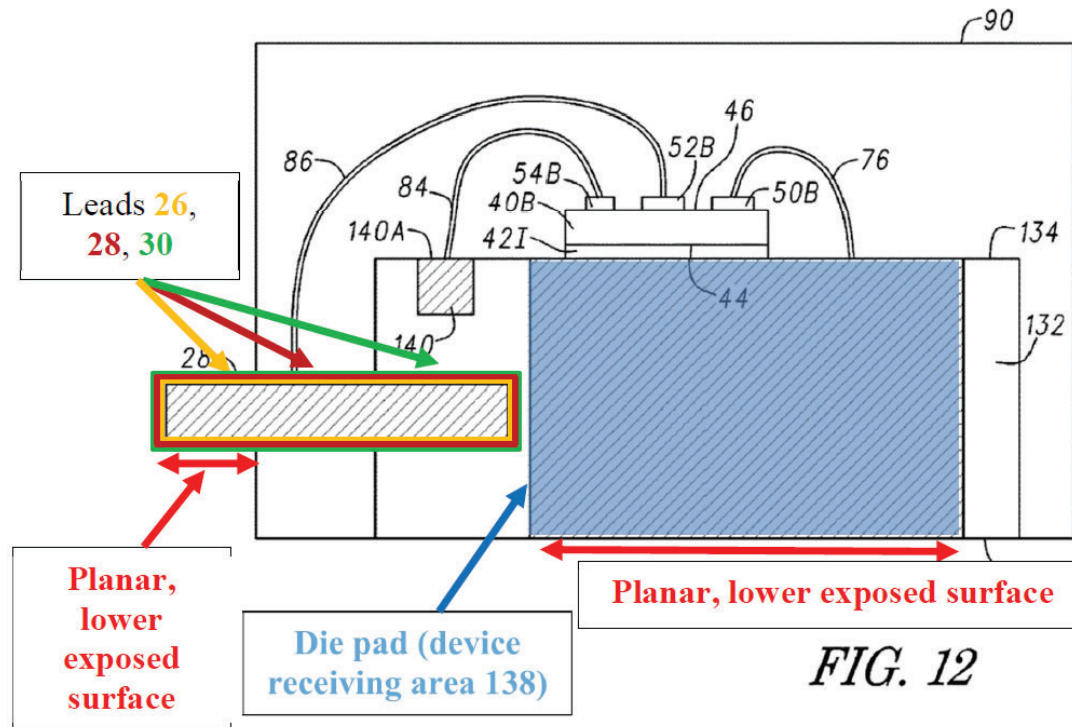
Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
[4p] The electronic component of claim 1,	<i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious the electronic component according to claim 1. <i>See supra</i> claim 1.
[4a] further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing	<p><i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 7:14-38</p>

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>and provide substantially planar contact surfaces.</p>	<p>FIG. 9 is a perspective view of a semiconductor component 150 in accordance with another embodiment of the present invention. Semiconductor component 150 is similar to semiconductor component 100 described with reference to FIG. 4 except the semiconductor device is identified by reference character 40A, i.e., the letter A has been appended to reference character 40, because drain contact 50 has been replaced by a drain contact 50A which extends over a portion of an active area of III-N semiconductor device 40A and source contact 52 have been replaced by a source contact 52A which extends over another portion of the active area of III-N semiconductor device 40A. It should be noted that mounting semiconductor chips to device receiving areas has been described with reference to FIGS. 1 and 2. Thus, semiconductor component 150 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40A.</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to</p>

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.</p> <p>Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu, 2:62-3:29; 4:42-51; 5:8-13; 5:31-64; 6:42-46; 7:9-13; 7:63-67</i></p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 4

Exemplary Disclosure based on *Liu* and Related Combinations



Liu Provisional discloses the following at [00038]

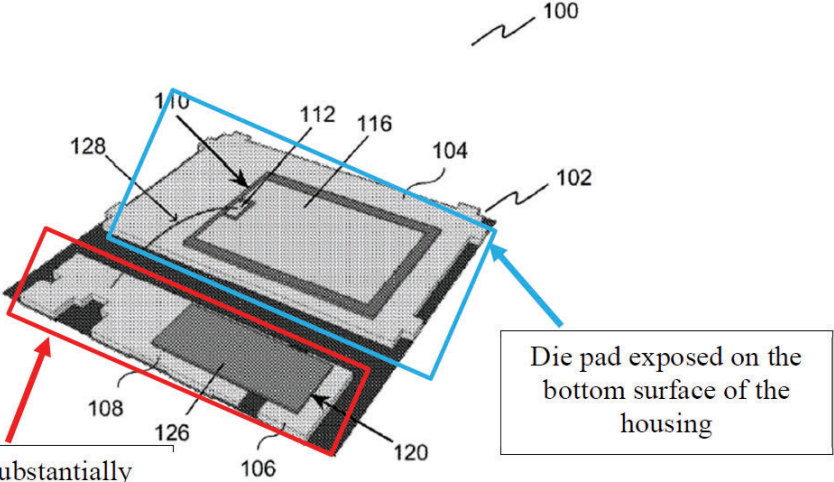
As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40A and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 106, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example a mold compound.

See also *Liu Provisional*, [00020], [00024], [00028], [00030]-[00031], [00034], [00036], [00040]

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p><i>Liu Provisional</i> discloses the following at Fig. 12</p> <p style="text-align: center;">FIG. 12</p> <p>Otremba433 discloses the following at [0027]</p> <p>FIG. 1 illustrates a top view of an exemplary semiconductor device 100 in accordance with one embodiment. The semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104. FIG. 2 schematically illustrates a cross-sectional view of the semiconductor device 100 shown in FIG. 1 along section line A-A.</p>

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Otremba433 discloses the following at [0037]</p> <p>The encapsulation body 104 of the semiconductor device 100 may embed the carrier 101 and the semiconductor chip 102 at side and top faces. The terminal portion 103_3 of the contact clip 103 forms an external terminal of the semiconductor device 100 and, therefore, protrudes out of the encapsulation body 104. By way of example, as illustrated in FIGS. 1 and 2, the semiconductor device may have a leadless package. In this and other cases the terminal portion 103_3 of the contact clip 103 may have an external contact area 103 a exposed at the encapsulation body 104, e.g., at the bottom of the package. The external contact area 103 a may be coplanar with a reference plane defined by a bottom surface 101 a of the carrier 101. The bottom surface 101 a of the carrier 101 may also be exposed at the bottom of the package. Further, a bottom surface portion 104 b of the encapsulation body 104 may be coplanar with the reference plane defined by the bottom surface 101 a of the carrier 101. In this case, the bottom surface 101 a of the carrier, the bottom surface portion 104 b of the encapsulation body 104 and the external contact area 103 a of the terminal portion 103 may all be arranged substantially level with each other. They may form the bottom of the package.</p> <p>Otremba433 discloses the following at [0039]</p> <p>The lead post 130 may form another external terminal of the semiconductor device 100. A bottom surface 130 a of the lead post 130 may be exposed at the bottom surface of the package of the semiconductor device 100 in order to e.g., provide for another SMT external contact area of the package.</p> <p>Otremba433 discloses the following at [0025]</p> <p>A contact clip is provided to electrically connect an electrode of the semiconductor chip to an external terminal of the semiconductor device. The contact clip may be an integral part having a bond portion bonded to the first electrode and having a terminal portion forming an external terminal of the semiconductor device. By way of example, the external terminal of the semiconductor device may</p>

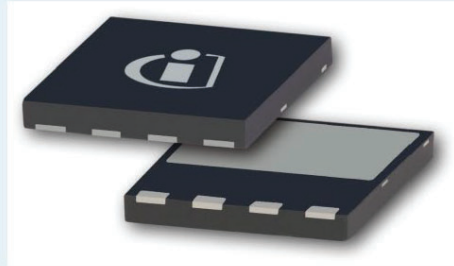
Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>between the first load electrodes 17 of two semiconductor devices 11, 12 and the upper surface 35 of a lead 23 of a leadframe 13. In this embodiment, the leadframe 13 is positioned within the electronic component at a level below the first side of the semiconductor devices 11, 12. The upper surface of the lead 23 may lie generally coplanar with the second side 16 of the semiconductor devices 11, 12. The contact clip 14 may have a general form and height adapted to accommodate the thickness of the semiconductor devices 11, 12. Typically, the device carrier portion 19 and the leads 20 of the leadframe 13 are stamped or etched from a metal sheet so that the upper side 35 of the device carrier portion 19 and the upper side 35 of the leads 20 are generally coplanar with one another. The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a surface mountable or leadless type electronic component. Alternatively, the outer portions of the leads may be bent in a general direction away from the first side of the two semiconductor devices to provide pins by which the electronic component 10 may be mounted on a redistribution board such as a printed circuit board.</p> <p>Otremba124 discloses the following at [0041]</p> <p>In an example, the power transistor arrangement 100 with a flipped SFET and a wire bonded GaN HEMT may be packaged in a 8x8 ThinPAK, wherein the GaN HEMT 110 may be a high voltage (e.g. larger than 200V) HEMT switch and the SFET 120 may be a low voltage (e.g. smaller than 200V) power MOSFET. The GaN HEMT 110 is a normally on device, and is transformed to a normally off transistor with introducing of the low-voltage SFET 120. Such a GaN-SFET arrangement 100 may correspond to the cascade circuit 500 of FIG. 5.</p> <p>Otremba124 discloses the following at Fig. 1 (annotated)</p>

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p data-bbox="562 724 856 854">Leads – Substantially planar contact surfaces on the lower external surface of the housing</p> <p data-bbox="898 821 982 854">FIG. 1</p> <p data-bbox="1192 602 1507 716">Die pad exposed on the bottom surface of the housing</p> <p data-bbox="489 927 1129 959">ThinPak8x8 Brochure discloses the following at 1</p>

Claim 4

Exemplary Disclosure based on *Liu* and Related Combinations

ThinPAK 8x8



**New High Voltage
SMD-Package**

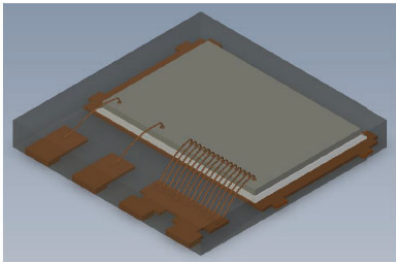
**April 2010
Version 1.0**

Page 1 of 34



INNOSCIENCE EXHIBIT 1016

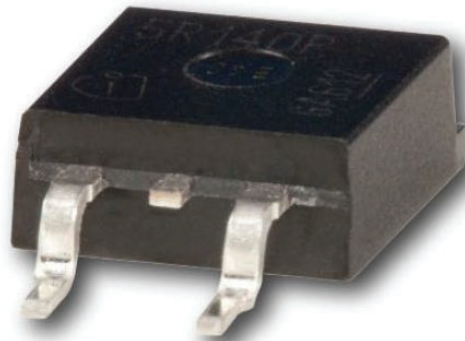
ThinPAK8x8 Brochure discloses the following at 5

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<div data-bbox="562 313 1696 418"> <div data-bbox="594 375 999 418">Package specification</div> <div data-bbox="1556 354 1661 402">  </div> </div> <ul data-bbox="594 456 1520 943" style="list-style-type: none"> ■ SMD package - leadless ■ Height: 1 mm package height ■ Footprint smaller than D2PAK (8 x 8 mm²) ■ Rdson -> similar to D²PAK / TO220 ■ Creepage distance: 2.7 mm ■ Low Parasitics (package inductivity, package resistance) ■ Double sided cooling (optional) ■ Soldering: wave and reflow ■ Green mold compound <div data-bbox="1220 824 1612 1084">  </div> <div data-bbox="594 1133 659 1154"> <p>April 2010</p> </div> <div data-bbox="604 1162 741 1192"> <p>Page 5 of 34</p> </div> <div data-bbox="1623 1133 1667 1154"> <p>Page 5</p> </div> <p data-bbox="489 1252 1146 1284">ThinPAK8x8 Brochure discloses the following at 6</p>

Claim 4

Exemplary Disclosure based on *Liu* and Related Combinations

ThinPAK 8x8 versus D²PAK



10 x 15 x 4.4 mm³



8 x 8 x 1 mm³

60 % footprint reduction - 80% height reduction - 90% Volume reduction

April 2010

Page 6

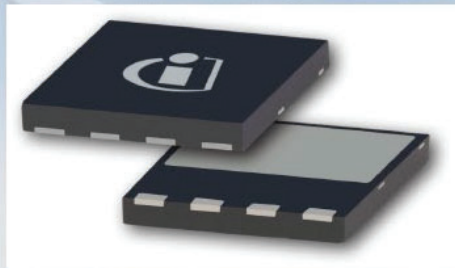
Page 6 of 34

See also ThinPAK8x8, 3, 21, 31, 33

ThinPAK Recommendations discloses the following at 1



**Recommendations
for Printed Circuit Board Assembly of In-
fineon VDSO Packages (ThinPAK)**



Application Note

Infineon VDSO Packages (ThinPAK)

July 2010

Published by Infineon Technologies AG
<http://www.infineon.com/coolmos>

Page 1 of 27

INNOSCIENCE EXHIBIT 1017

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	ThinPAK Recommendations discloses the following at 4



1. Package Description

The PG-VDSON (Plastic Green High Voltage Small Single Outline Package) is a near chip-scale plastic encapsulated package with a copper leadframe and pads at the bottom of the package to provide electrical and thermal contact to the printed circuit board.

The PG-VDSON (alias ThinPAK) is a leadless package consuming smaller area for high voltage applications compared to e.g. packages like D²PAK

Characteristics

- Small package outline 8x8 mm²
- Low profile 1 mm
- Exposed drain pad for optimized heat transfer to the PCB
- Pads with Pb-free solder plating (electroplated Sn)

Figure 1 shows a photo of PG-VDSON-4 packages (alias ThinPAK 8x8). Visible are the 4 small Source/Gate-Pads, which show exposed copper at the package side wall (due to package singulation) and the big exposed drain pad which is fully surrounded by mold compound.

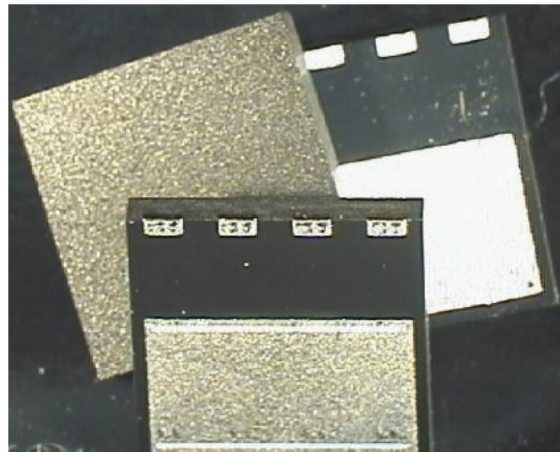
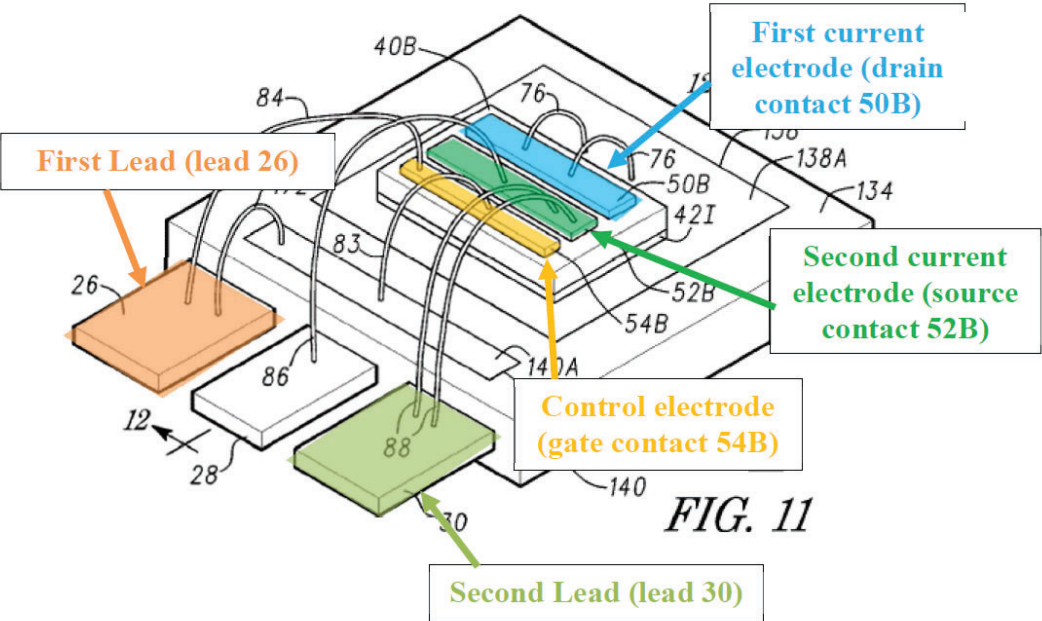
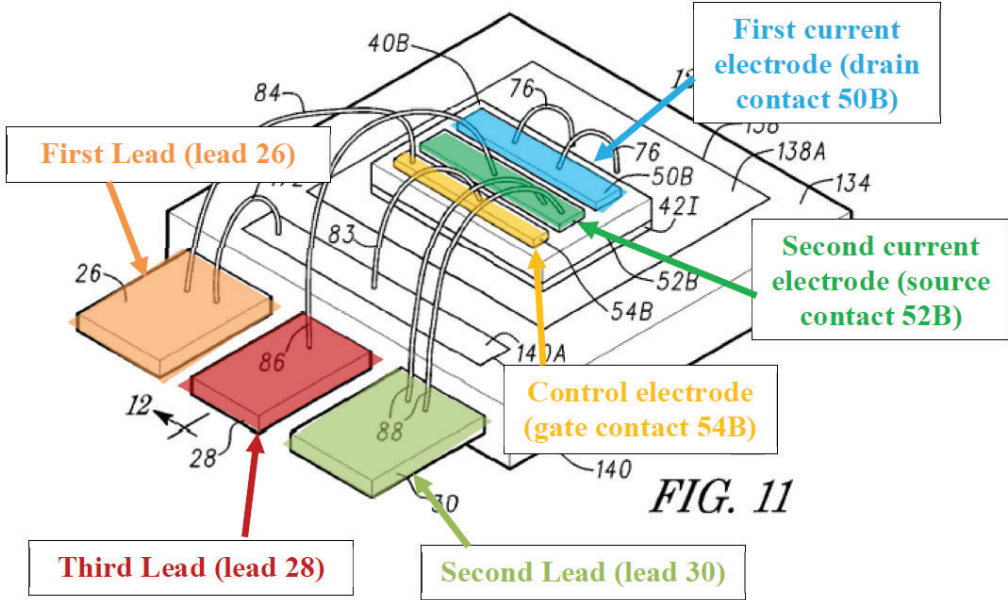


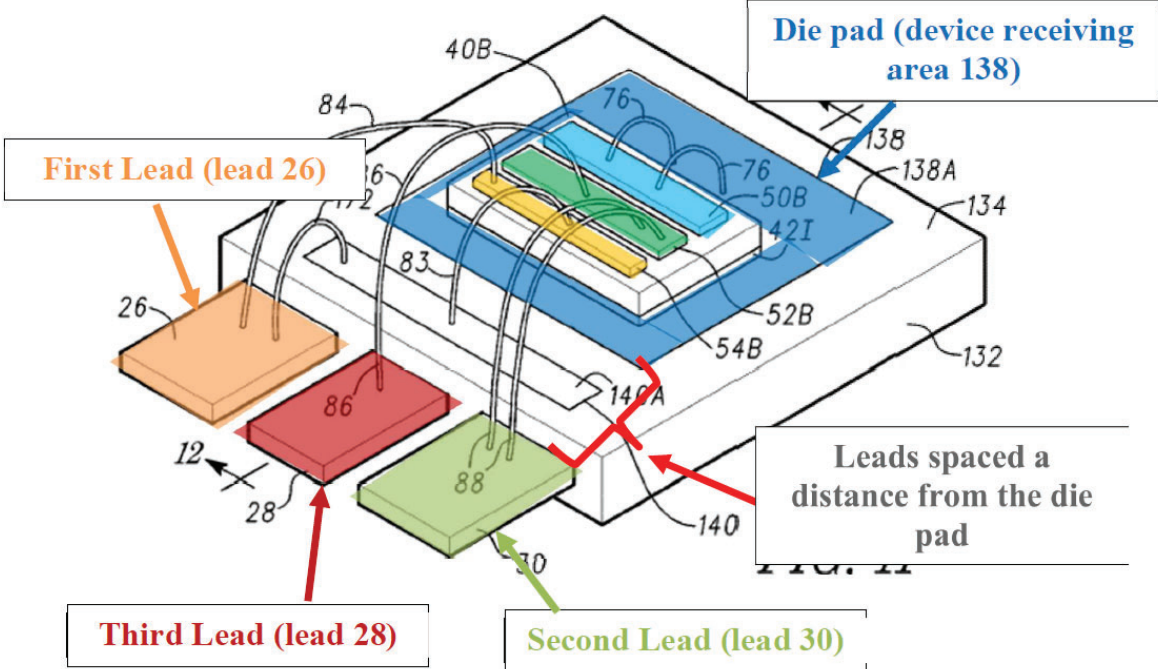
Figure 1: Top and bottom view of VDSON-4 (ThinPAK 8x8)

Claim 4	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Lind discloses the following at 3</p> <p>III. Source-Sense concept and A/B simulation</p> <p>A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.</p> <div data-bbox="558 456 1283 862"> </div> <p>Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections</p> <p>The principle is to provide a separate path for the drain-source current, such that voltage generated across the source inductance no longer appears in the KVL mesh of the gate current loop.</p>
thi	
Claim 6	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>[6p] The electronic component of claim 1,</p>	<p><i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious the electronic component according to claim 1. <i>See supra</i> claim 1.</p>

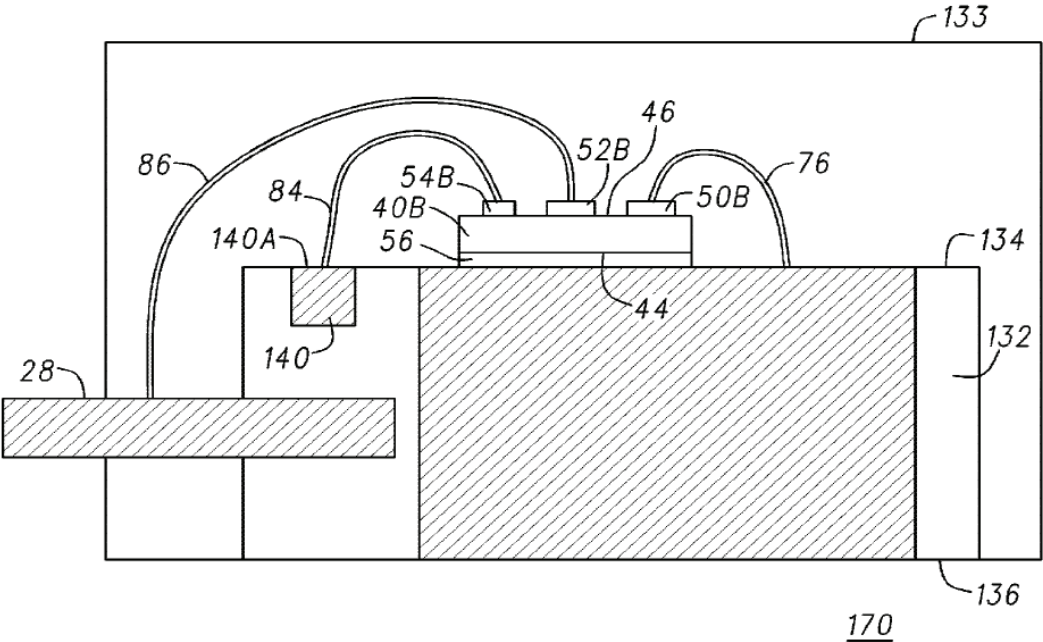
Claim 6	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>[6a] wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.</p>	<p><i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p style="padding-left: 40px;">A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p style="padding-left: 40px;">Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-</p>

Claim 6	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>FIG. 11</p>

Claim 6	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p>FIG. 11</p>

Claim 6	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>Die pad (device receiving area 138)</p> <p>First Lead (lead 26)</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p>Leads spaced a distance from the die pad</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 6	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00023], [00027], [00029], [00033], [00035], [00039], [00044]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

Claim 6	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p>

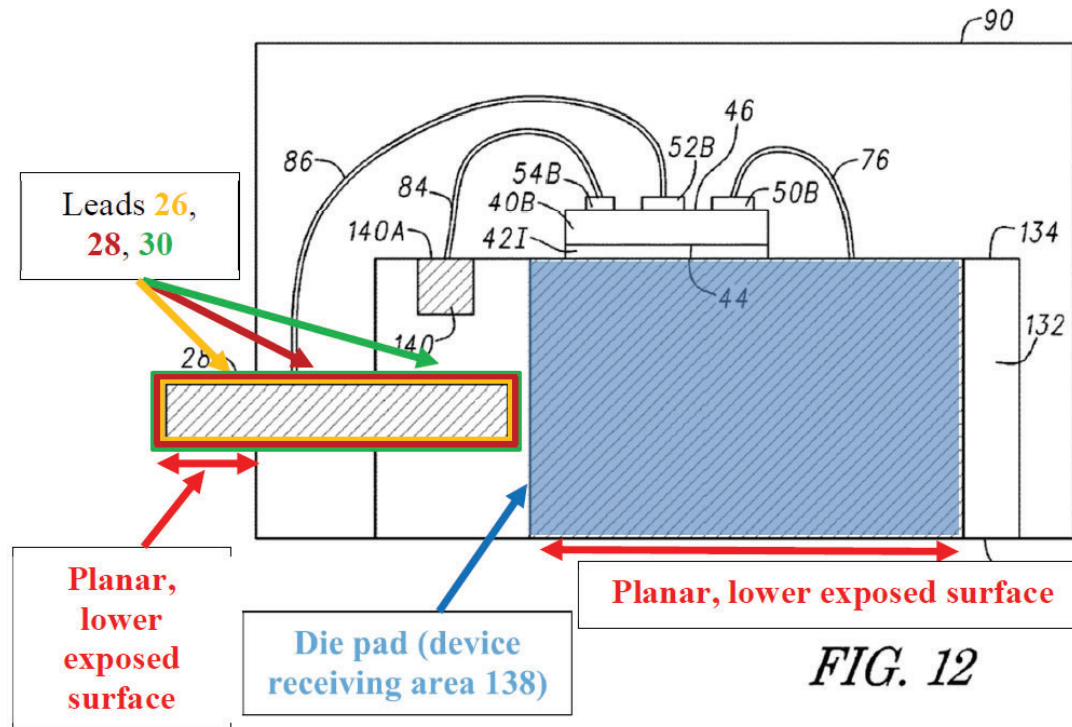
Claim 9	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
[9p] The electronic component of claim 1,	<i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious the electronic component according to claim 1. <i>See supra</i> claim 1.
[9a] wherein the electronic	<i>Liu</i> alone or in combination with other references discloses and/or renders obvious wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8×8 package outline.

Claim 9	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>component conforms to a TO leadless package outline or a ThinPAK8×8 package outline.</p>	<p>For example</p> <p><i>Liu</i> discloses the following at 7:14-38</p> <p>FIG. 9 is a perspective view of a semiconductor component 150 in accordance with another embodiment of the present invention. Semiconductor component 150 is similar to semiconductor component 100 described with reference to FIG. 4 except the semiconductor device is identified by reference character 40A, i.e., the letter A has been appended to reference character 40, because drain contact 50 has been replaced by a drain contact 50A which extends over a portion of an active area of III-N semiconductor device 40A and source contact 52 have been replaced by a source contact 52A which extends over another portion of the active area of III-N semiconductor device 40A. It should be noted that mounting semiconductor chips to device receiving areas has been described with reference to FIGS. 1 and 2. Thus, semiconductor component 150 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40A.</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p>

Claim 9	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.</p> <p>Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

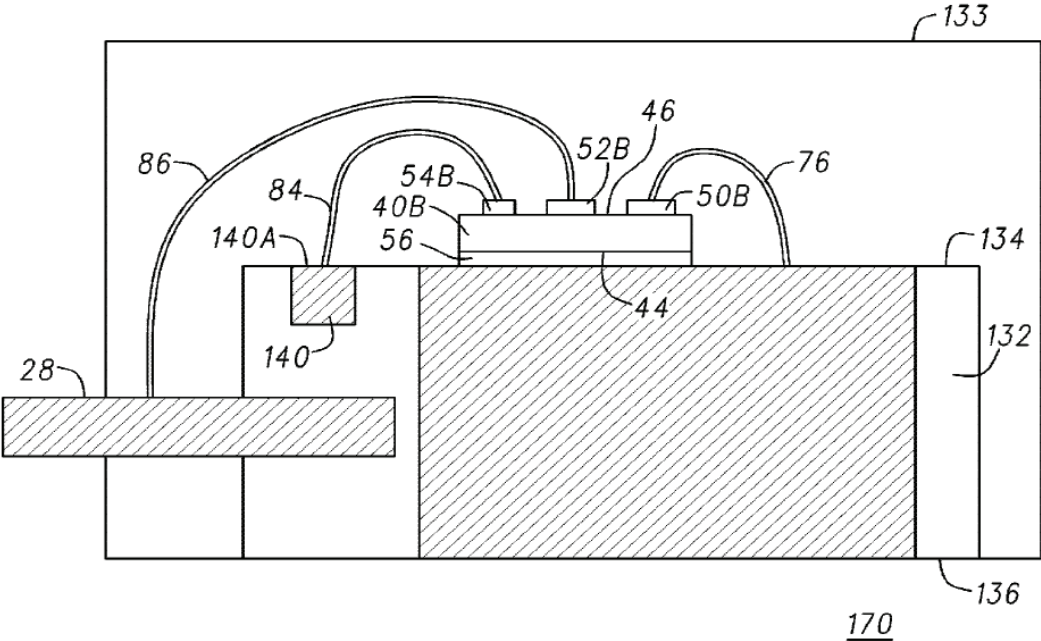
Claim 9

Exemplary Disclosure based on *Liu* and Related Combinations



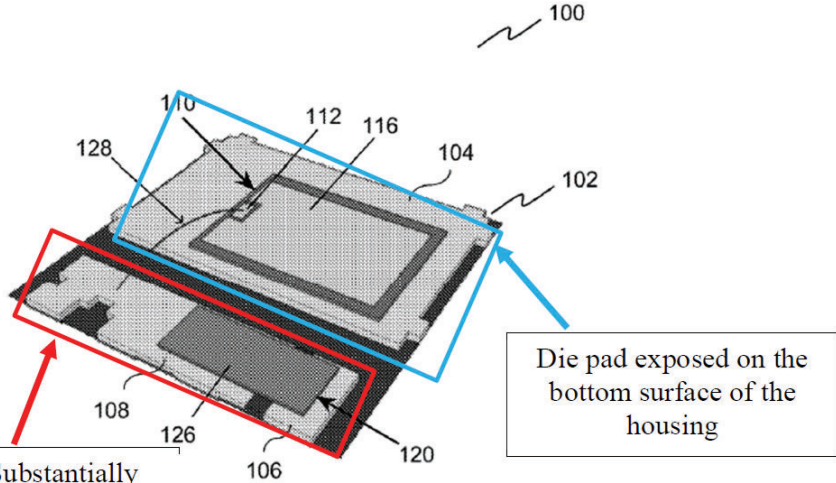
Liu Provisional discloses the following at [00037]

FIG. 9 is a perspective view of a semiconductor component 150 in accordance with another embodiment of the present invention. Semiconductor component 150 is similar to semiconductor component 100 described with reference to FIG. 4 except the semiconductor device is identified by reference character 40A, i.e., the letter A has been appended to reference character 40, because drain contact 50 has been replaced by a drain contact 50A which extends over a portion of an active area of III-N of semiconductor device 40A and source contact 52 has been replaced by a source contact 52A which extends over another portion of the active area of III -N of semiconductor device 40A. It should be noted that mounting semiconductor chips to device receiving areas has been described with

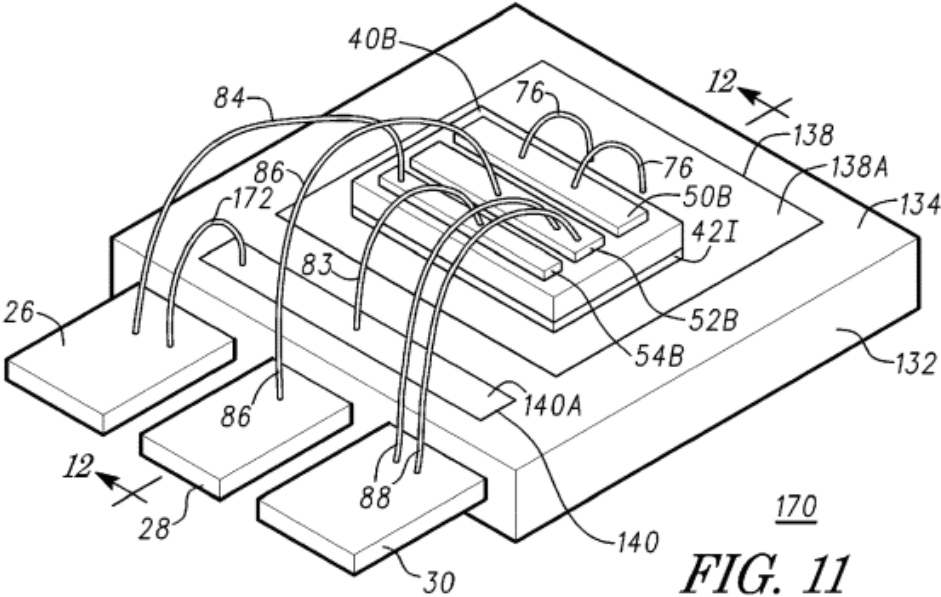
Claim 9	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>reference to FIGs. 1 and 2. Thus, semiconductor component 150 includes a III-N cascade switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40A.</p> <p><i>Liu Provisional</i> discloses the following at Fig. 12</p>  <p style="text-align: center;">FIG. 12</p> <p>Otremba433 discloses the following at [0037]</p> <p>The encapsulation body 104 of the semiconductor device 100 may embed the carrier 101 and the semiconductor chip 102 at side and top faces. The terminal portion 103_3 of the contact</p>

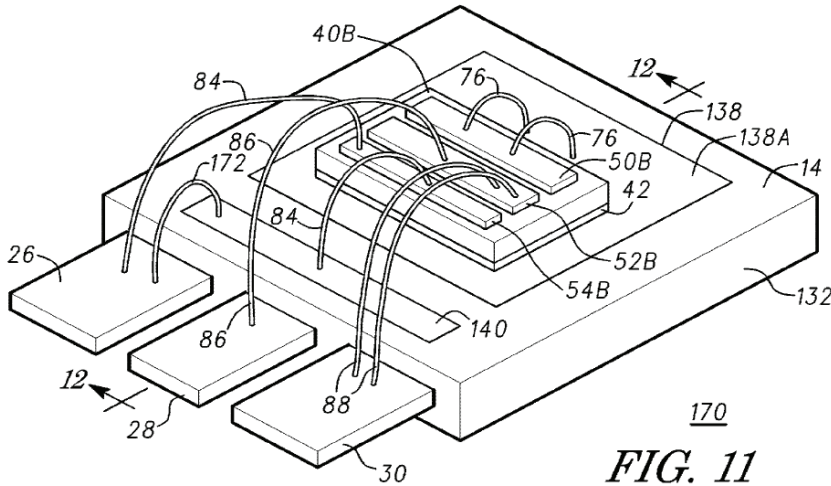
Claim 9	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>clip 103 forms an external terminal of the semiconductor device 100 and, therefore, protrudes out of the encapsulation body 104. By way of example, as illustrated in FIGS. 1 and 2, the semiconductor device may have a leadless package. In this and other cases the terminal portion 103_3 of the contact clip 103 may have an external contact area 103 a exposed at the encapsulation body 104, e.g., at the bottom of the package. The external contact area 103 a may be coplanar with a reference plane defined by a bottom surface 101 a of the carrier 101. The bottom surface 101 a of the carrier 101 may also be exposed at the bottom of the package. Further, a bottom surface portion 104 b of the encapsulation body 104 may be coplanar with the reference plane defined by the bottom surface 101 a of the carrier 101. In this case, the bottom surface 101 a of the carrier, the bottom surface portion 104 b of the encapsulation body 104 and the external contact area 103 a of the terminal portion 103 may all be arranged substantially level with each other. They may form the bottom of the package.</p> <p>Otremba433 discloses the following at [0039]</p> <p>The lead post 130 may form another external terminal of the semiconductor device 100. A bottom surface 130 a of the lead post 130 may be exposed at the bottom surface of the package of the semiconductor device 100 in order to e.g., provide for another SMT external contact area of the package.</p> <p>Otremba433 discloses the following at [0025]</p> <p>A contact clip is provided to electrically connect an electrode of the semiconductor chip to an external terminal of the semiconductor device. The contact clip may be an integral part having a bond portion bonded to the first electrode and having a terminal portion forming an external terminal of the semiconductor device. By way of example, the external terminal of the semiconductor device may comprise an external contact area exposed at the encapsulation body of a leadless package. The external terminal of the semiconductor device may also be a lead of a leaded package.</p> <p>Otremba433 discloses the following at Fig. 2 (annotated)</p>

Claim 9	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>portion 19 and the upper side 35 of the leads 20 are generally coplanar with one another. The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a Surface mountable or leadless type electronic component. Alternatively, the outer portions of the leads may be bent in a general direction away from the first side of the two semiconductor devices to provide pins by which the electronic component 10 may be mounted on a redistribution board such as a printed circuit board.</p> <p>Otremba124 discloses the following at [0041]</p> <p>In an example, the power transistor arrangement 100 with a flipped SFET and a wire bonded GaN HEMT may be packaged in a 8x8 ThinPAK, wherein the GaN HEMT 110 may be a high voltage (e.g. larger than 200V) HEMT switch and the SFET 120 may be a low voltage (e.g. smaller than 200V) power MOSFET. The GaN HEMT 110 is a normally on device, and is transformed to a normally off transistor with introducing of the low-voltage SFET 120. Such a GaN-SFET arrangement 100 may correspond to the cascade circuit 500 of FIG. 5.</p> <p>Otremba124 discloses the following at Fig. 1 (annotated)</p>

Claim 9	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>FIG. 1</p> <p>Leads – Substantially planar contact surfaces on the lower external surface of the housing</p> <p>Die pad exposed on the bottom surface of the housing</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>[17p] An electronic component, comprising:</p>	<p>To the extent the preamble is limiting, <i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious an electronic component. <i>See supra</i> claim 1.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 8:1-10</p> <p>FIG. 11 is a perspective view of a semiconductor component 170 in accordance with another embodiment of the present invention. FIG. 12 is a cross-sectional view of semiconductor component 170 taken along section line 12-12 of FIG. 11. FIGS. 11 and 12 are described together. What is shown in FIGS. 11 and 12 are a molded device support structure 132 that includes device</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>receiving area 138 and bond pad 140, and leadframe leads 26, 28, and 30. Molded device support structure 132 has been described with reference to FIGS. 6 and 7.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:56-59; 4:60-5:7; 5:14-30; 5:36-64; 6:47-7:8; 7:14-32; 7:39-62; 8:49-9:10</p> <p><i>Liu</i> discloses the following at Fig. 11</p>  <p><i>FIG. 11</i></p> <p><i>Liu Provisional</i> discloses the following at [00041]</p> <p>FIG. 11 is a perspective view of a semiconductor component 170 in accordance with another embodiment of the present invention. FIG. 12 is a crosssectional view of semiconductor component 170 taken along section line 12-12 of FIG. 11. FIGs. 11 and 12 are described together. What is shown</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>in FIGs. 11 and 12 are a molded device support structure 132 that includes device receiving area 138 and bond pad 140, and leadframe leads 26, 28, and 30. Molded device support structure 132 has been described with reference to FIGs. 6 and 7.</p> <p><i>See also Liu Provisional</i>, [00020], [00026]- [00027], [00029], [00031], [00035], [00037], [00039], [00044]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>  <p style="text-align: center;">FIG. 11</p>
<p>[17a] a Group III nitride-based transistor device having a blocking voltage capability</p>	<p><i>Liu</i> alone or in combination with other references discloses and/or renders obvious a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second</p>

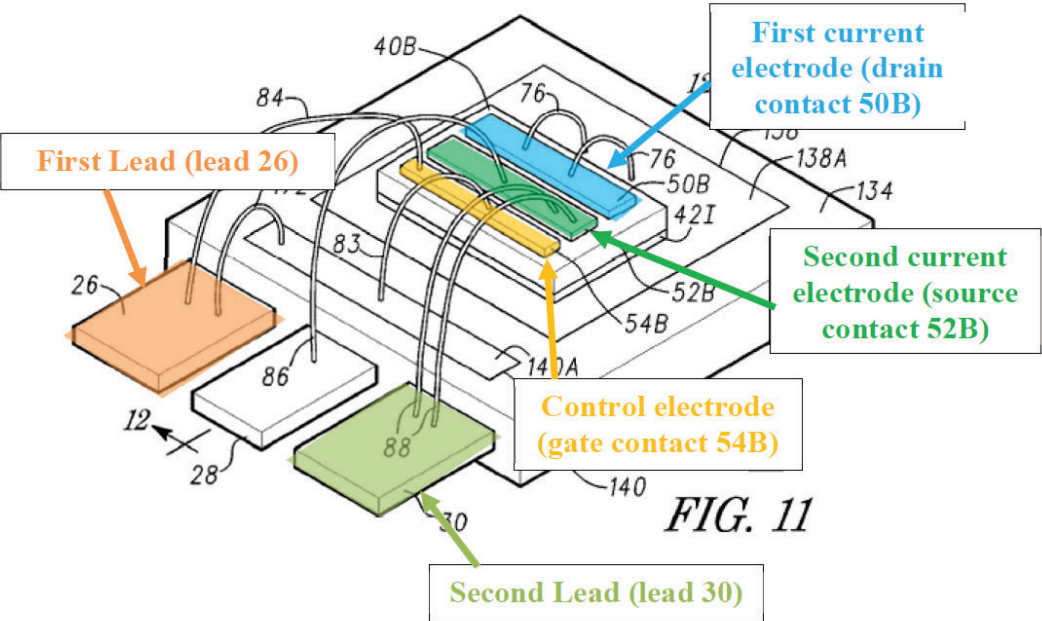
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
<p>of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and</p>	<p>current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality. <i>See supra</i> claims 1-3.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 3:30-61</p> <p style="padding-left: 40px;">A semiconductor chip 40 is bonded to surface 18A of device receiving area 18 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. More particularly, surface 44 of semiconductor chip 40 is bonded to surface 18A of device receiving area 18 through electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40 is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40 includes a field effect semiconductor device having a drain contact 50 formed on or from a portion of surface 46, a source contact 52 formed on or from another portion of surface 46, and gate contacts 54 and 55 formed on or from other portions of surface 46. It should be noted that the semiconductor device is not limited to being a field effect transistor. For example, the semiconductor device may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. In accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 40, semiconductor chip 40 may be referred to as a semiconductor device. In addition, die attach material 42 is not limited to being an electrically conductive material but may be an electrically insulating material or a thermally conductive material. By way of example, semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride. A III-nitride semiconductor material may be referred to as a III-N semiconductor material, a III-nitride based semiconductor material, a III-N based semiconductor material, or the like.</p> <p><i>Liu</i> discloses the following at 5:34-64</p> <p style="padding-left: 40px;">FIG. 6 is a perspective view of a semiconductor component 130 in accordance with another embodiment of the present invention. FIG. 7 is a cross-sectional view of semiconductor component 130 taken along section line 7-7 of FIG. 6. FIGS. 6 and 7 are described together. What is</p>

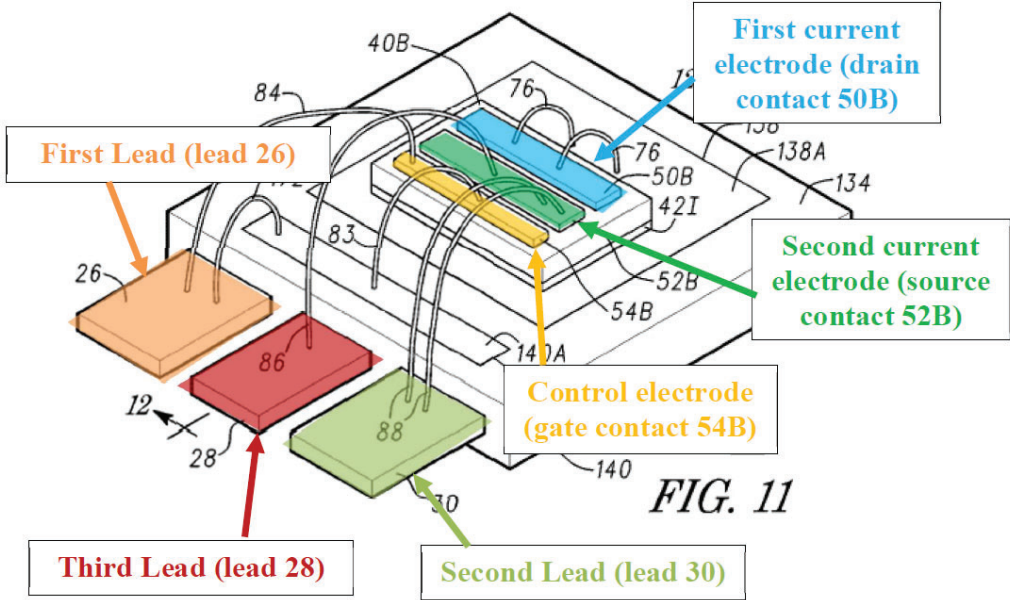
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>shown in FIGS. 6 and 7 are a molded device support structure 132 having a top surface 134 and a bottom surface 136. Molded support structure 132 includes a device receiving area 138, a bond pad 140 at top surface 134, and a contact 143 at bottom surface 136. In accordance with an embodiment, bond pads 138 and 140 are coplanar with surface 134. Leadframe leads 26, 28, and 30 protrude from a side or an edge of molded device support structure 132. Device receiving area 138 may be referred to as a device receiving structure. Molded support structure 132 may be formed by placing an electrically conductive strip in a mold having a mold cavity and injecting a mold compound into the mold cavity. The electrically conductive strip may include a pad or plate 138 having a contact region 140, wherein pad or plate 138 serves as a device receiving area, and a plurality of leadframe leads such as, for example, leadframe leads 26, 28, and 30. After injecting the mold compound into the cavities, the electrically conductive strip may be singulated into a plurality of molded support structures 132. Suitable materials for the electrically conductive strips include copper, aluminum, or the like. As mentioned, molded support structure 132 is illustrated and described as a single element; however, it may be a portion singulated from a leadframe strip encapsulated in a mold compound.</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

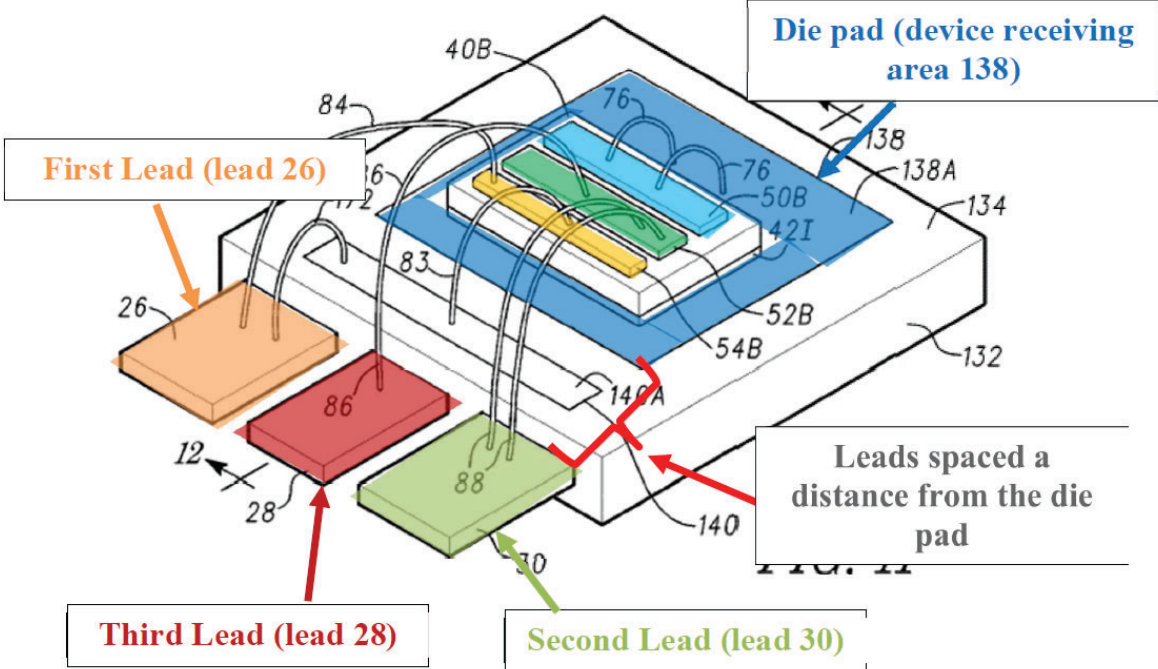
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<div data-bbox="499 289 1596 841"> <p style="text-align: center;">FIG. 11</p> </div> <p><i>Liu</i> discloses the following at 7:39-62</p> <p>FIG. 10 is a perspective view of a semiconductor component 160 in accordance with another embodiment of the present invention. Semiconductor component 160 is similar to semiconductor component 120 described with reference to FIG. 5 except that drain contact 50 has been replaced by a drain contact 50B which extends over a portion of an active area of III-N semiconductor device 40B, source contact 52 has been replaced by a source contact 52B which extends over another portion of the active area of III-N semiconductor device 40B, and gate contacts 54 and 55 have been replaced by a gate contact 54B which extends over another portion of the active area of III-N semiconductor device 40B, bond wire 80 has been replaced by bond wires 80B, and bond wire 82 is not present in the embodiment of FIG. 10. A reference character B has been appended to reference character 40 to distinguish a semiconductor chip having bond pads over active areas from a semiconductor chip without bond pads over active areas. It should be noted that mounting semiconductor chips to device receiving areas has been described with reference to FIGS. 1 and 2.</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Thus, semiconductor component 160 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically grounded and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>Liu</i> discloses the following at 8:49-9:10</p> <p>FIG. 13 is a perspective view of a semiconductor component 180 in accordance with another embodiment of the present invention. Semiconductor component 180 is similar to semiconductor component 139 except that semiconductor chip 40 of FIG. 8 has been replaced by a semiconductor chip 40B (shown in FIG. 11); semiconductor component 180 includes a bond pad 141 shown and described with reference to FIG. 8; bond wire 85 of semiconductor component 139 is replaced by a bond wire 172; and a bond wire 84 connects gate contact 54B to bond pad 140. Thus, drain contact 50B is electrically connected to bond pad 141 by bond wires 76, source contact 52B is electrically connected to lead 30 by bond wires 88 and to lead 28 by bond wire 86, and gate contact 54B is electrically connected to bond pad 140 by a bond wire 84 and to lead 26 by a bond wire 84. Bond wire 142 connects leadframe lead 30 with surface 138A of device receiving area 138. Bond wires 142 and 88 and leadframe lead 30 electrically connect source electrode 52B, hence the source of semiconductor device 40B, to the substrate of the semiconductor material of semiconductor device 40B. Thus, semiconductor component 180 includes a III-N cascode switch in which the substrate of the III-N semiconductor device is connected to its source and bond pads are formed over active regions of semiconductor device 40B. The source of the III-N semiconductor device can be connected to a potential such as, for example ground. Connecting the source of the III-N semiconductor device also connects the substrate of the III-N semiconductor device to ground in accordance with this embodiment.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact 54B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.</p> <p>Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu, 2:62-4:59; 4:60-5:33; 5:36-6:41; 6:20-41; 6:47-7:8; 7:14-32; 7:39-62; 8:1-10</i></p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

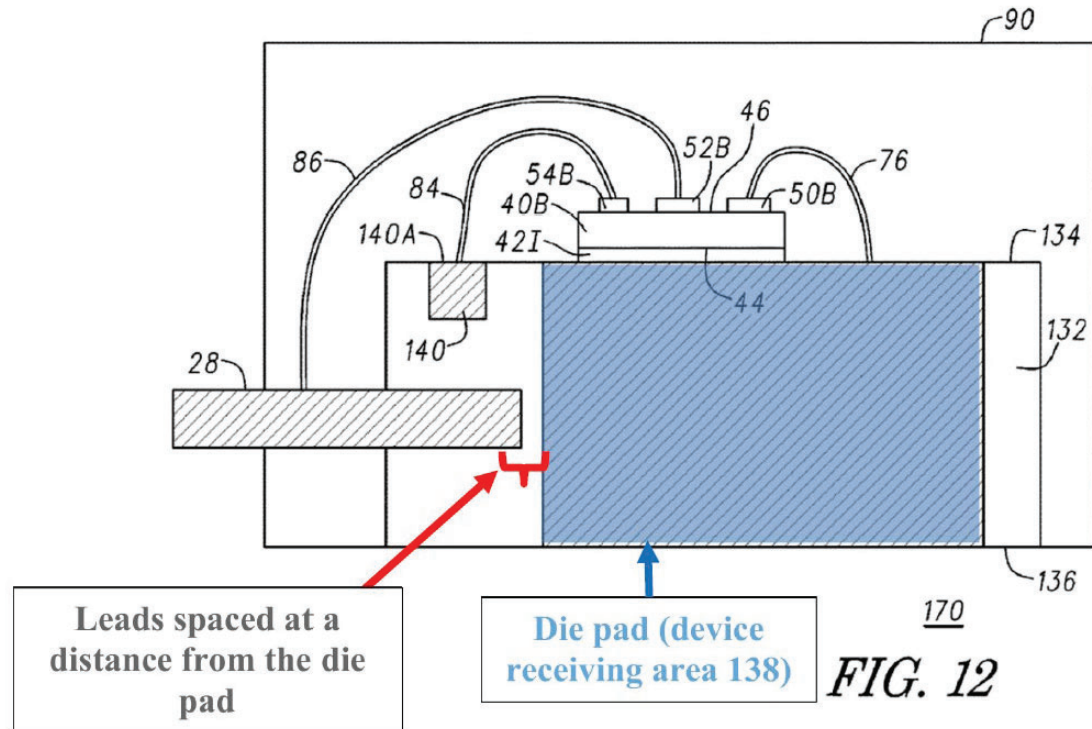
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>Second Lead (lead 30)</p> <p>FIG. 11</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p>FIG. 11</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>Die pad (device receiving area 138)</p> <p>Leads spaced a distance from the die pad</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations



Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00020]-[00027], [00029], [00031]-[00033], [00035], [00037], [00039], [00041], [00043], [00044]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations

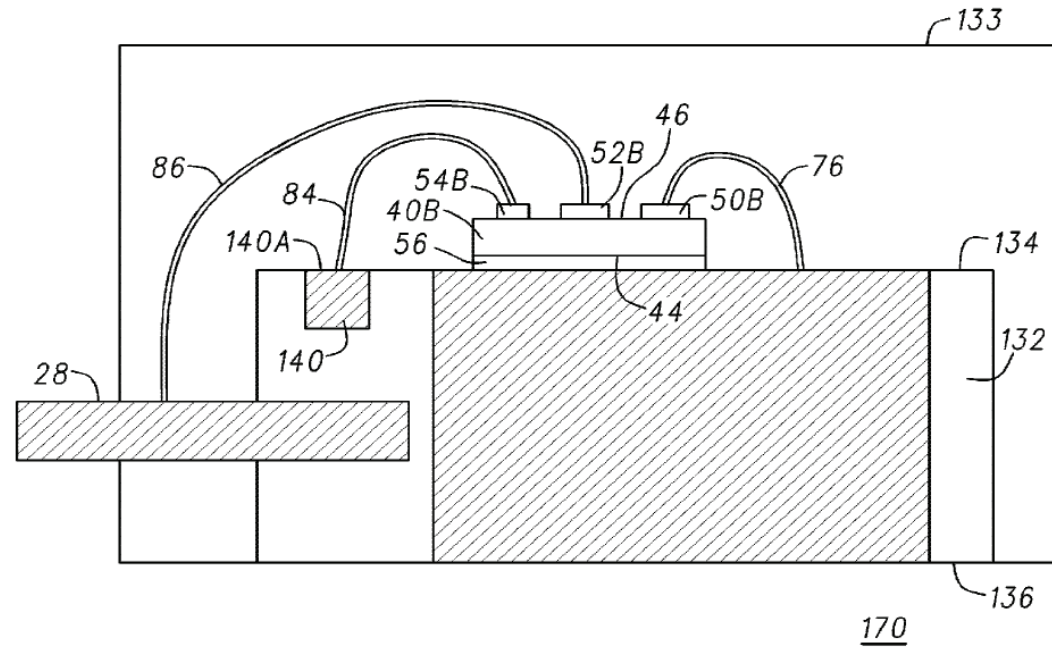


FIG. 12

A person of ordinary skill would have understood that the compound semiconductor transistor device disclosed in *Liu* would have achieved at least 400V and a switching frequency capability of at least 100kHz, which were common for compound semiconductor power conversion transistors designed for high-voltage applications. *See* Huang at 114, describing the switching speeds of GaN devices.

Huang discloses the following at 114

The switching speed of GaN devices is much faster than comparable Si MOSFET which makes the packaging even more critical to achieve lower loss and less ringing during switching transition. The impact of the packaging parasitics on cascode GaN devices has been investigated in [4-5]. The

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations

common source inductance and inter-connected inductance are detrimental to switching loss and gate reliability. TO220 and DFN packages are typically used for high voltage e-mode GaN devices. Fig. 2 shows the package-related parasitic inductance and the value is listed in Table II which are extracted by FEA simulation in Ansoft Q3D. With Kelvin connection, the DFN package is able to decouple the power loop and driving loop, and therefore it can minimize the common source inductance. Moreover, the inductance of DFN package is much smaller than TO220 package which also helps to reduce the loss and ringing issue.

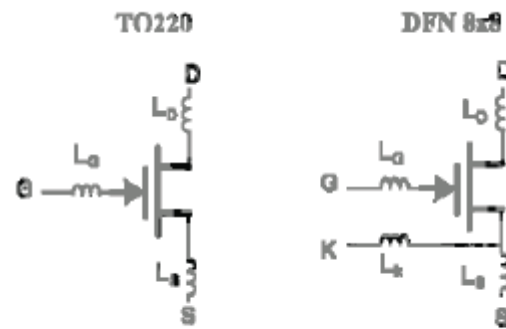


Fig. 2 Packaging related parasitic inductance

TABLE II. PACKAGE-RELATED PARASITIC INDUCTANCE VALUES

	L_G	L_D	L_S	L_K
TO220	3.6nH	2.3nH	3.9nH	N/A
DFN 8x8	2.4nH	1.3nH	0.9nH	1.3nH

The key experimental waveforms with two different packages are shown in Fig. 3. For the turn-on transition, the voltage and current slew rate of DFN package is much larger than that of TO220 package due to smaller common source inductance and loop inductance. As a result, the turn-on energy of DFN package is much smaller than TO220 package as shown in Fig.5. For the turn-off

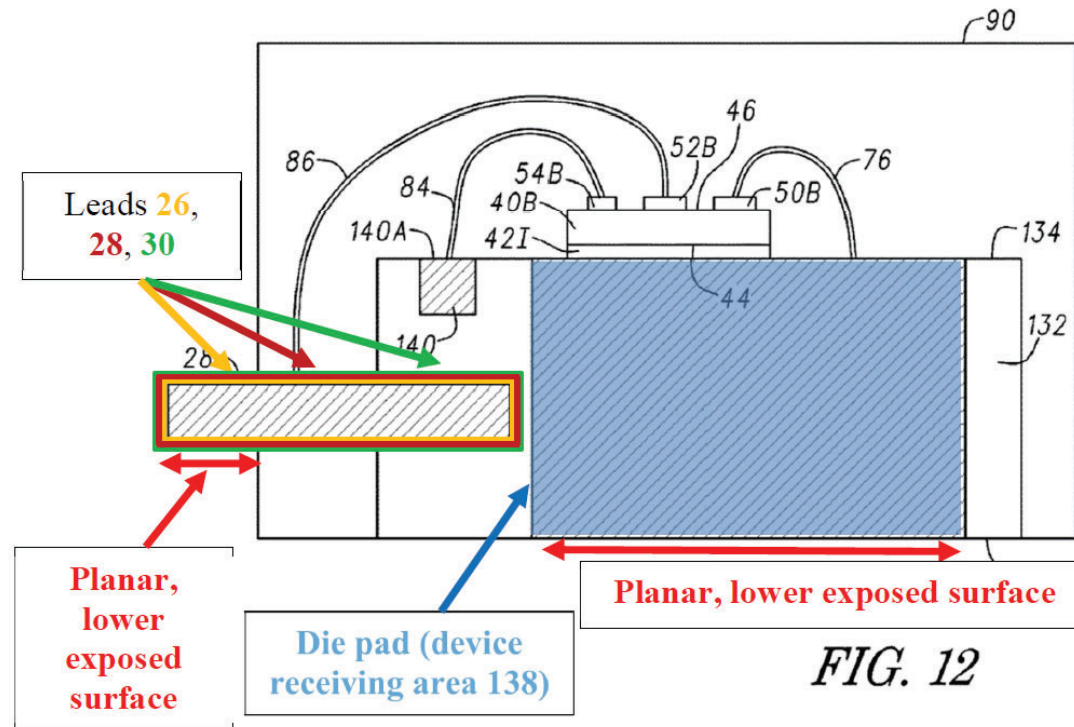
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>transition, a severe ringing occurred in TO220 package. The false turn-on is observed at high current turn-off condition as shown in Fig. 4, and therefore, the turn-off energy of TO220 package increases dramatically with turn-off current.</p> <p>In addition, Roberts discloses a compound semiconductor transistor device with a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.</p> <p>Roberts discloses the following at [0006] GaN power transistors for power conversion circuits for high voltage (HV) applications, e.g. 600/650V, are typically normally-on (depletion mode) transistors. These transistors are usually driven by a series connected, discrete, power MOSFET device, i.e. in a cascode configuration, to provide normally-off operation (see FIG. 1). Conventionally, the hybrid cascode arrangement is provided with a separate, high power, high speed driver circuit, having a separate isolated power supply.</p> <p>Roberts discloses the following at [0008] The GaN transistor may be required, for example, to provide <20 ns switching time and more than 30 A current switching capability. Any significant series inductance at the MOSFET source or at the common node will provide unwanted $L di/dt$ transients which can be as large as the threshold voltage of the devices, thus causing unwanted switching. It will be appreciated that in operation of an electronic power switching system that is capable of switching, for example, 30 Amps at 1000V, i.e. 30,000 Watts, safe operation may be compromised by any unwanted switching caused by transients or noise that exceeds the threshold voltage of the device.</p> <p>Roberts discloses the following at [0012] GaN transistors that can switch, for example, 24 A (1200 V) and 47 A (650 V) may have die sizes as small as 2×2 mm. Calculations show these die, when packaged, can have a thermal resistance of greater than 2° C./W. For example, it is estimated that, for an on-resistance of 80 mΩ, the ohmic power dissipation would be 32 Watts if the device were required to sink 20 Amps. The thermal resistance in total for the combination of the device, package and heat sink could exceed 5° C./W, so that the temperature increase from the GaN device dissipation alone could exceed 150° C. The additional heat dissipation of the MOSFET, assuming a 20 mΩ device is used, would be 8 Watts.</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>With the total structure dissipating 40 Watts, the temperature within the package could exceed the safe operating limits of the MOSFET, typically 175° C., if there is insufficient heat dissipation.</p> <p><i>See also</i> Roberts, [0003]-[0004], [0010], [0056]</p>
<p>[17b] a housing,</p>	<p><i>Liu</i> alone or in combination with one or more references discloses and/or renders obvious a housing. <i>See supra</i> claim 4.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 7:14-38</p> <p>FIG. 9 is a perspective view of a semiconductor component 150 in accordance with another embodiment of the present invention. Semiconductor component 150 is similar to semiconductor component 100 described with reference to FIG. 4 except the semiconductor device is identified by reference character 40A, i.e., the letter A has been appended to reference character 40, because drain contact 50 has been replaced by a drain contact 50A which extends over a portion of an active area of III-N semiconductor device 40A and source contact 52 have been replaced by a source contact 52A which extends over another portion of the active area of III-N semiconductor device 40A. It should be noted that mounting semiconductor chips to device receiving areas has been described with reference to FIGS. 1 and 2. Thus, semiconductor component 150 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40A.</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.</p> <p>Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:42-51; 5:8-13; 5:31-64; 6:42-46; 7:9-13; 7:63-67</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations

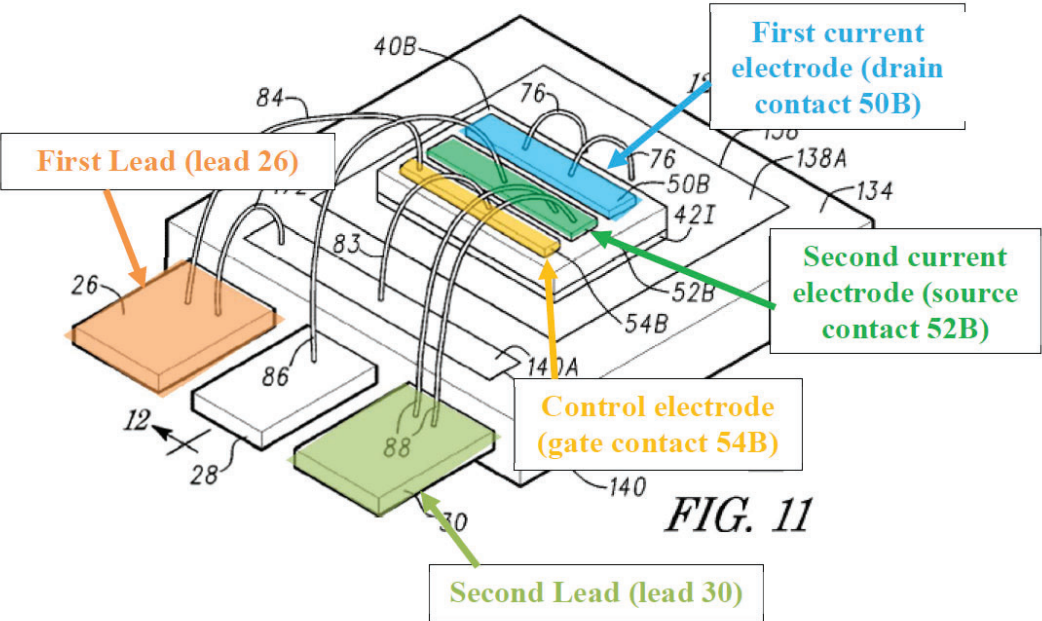


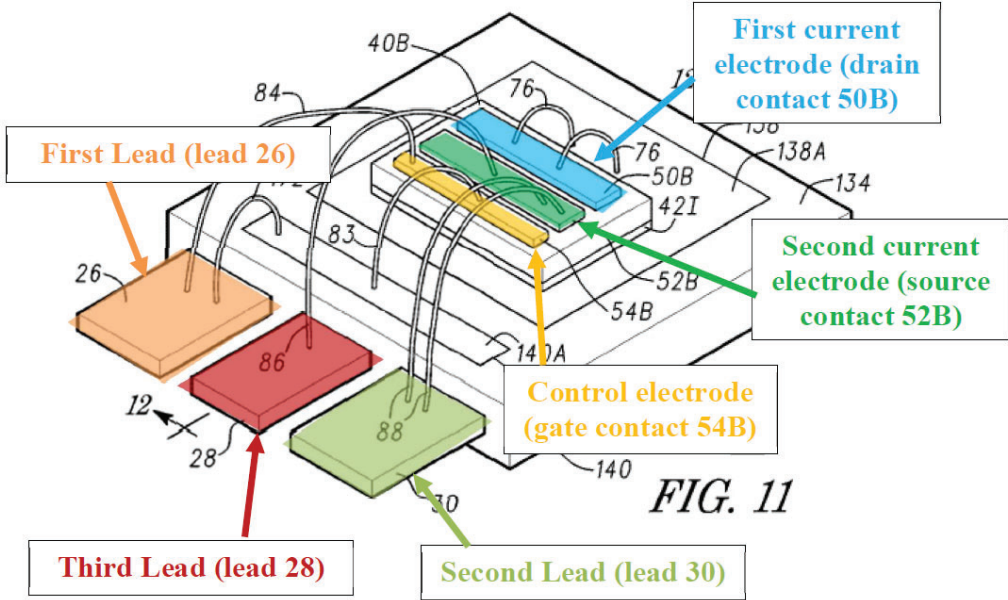
Liu Provisional discloses the following at [00038]

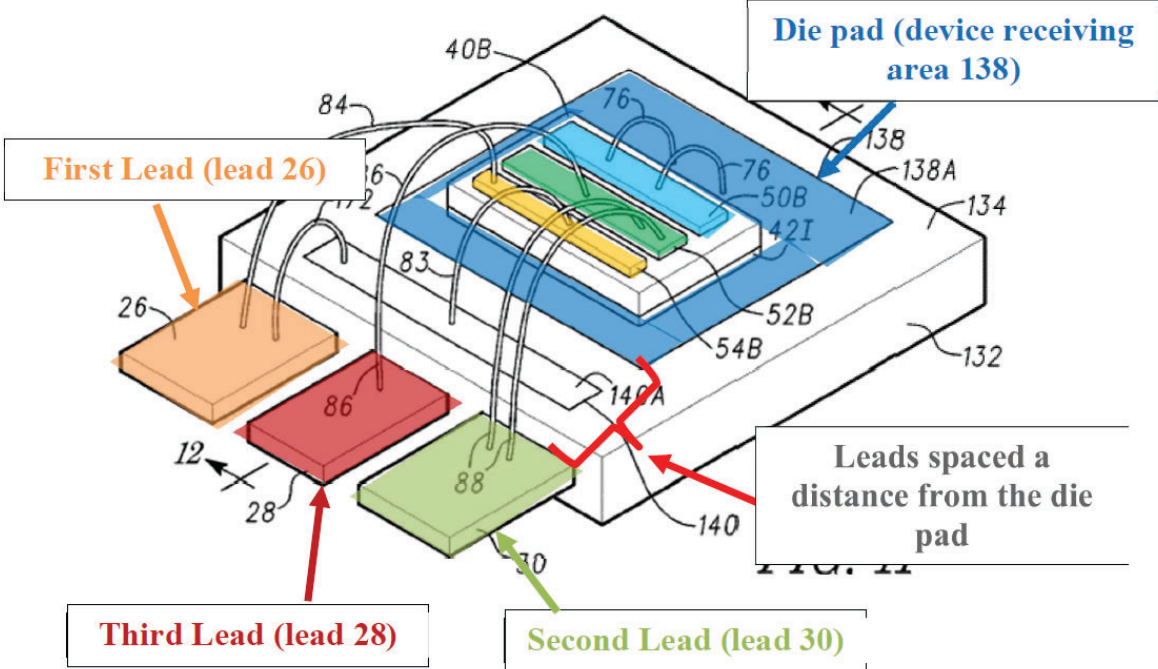
As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40A and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 106, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example a mold compound. See also *Liu Provisional*, [00020], [00024], [00028], [00030]-[00031], [00034], [00036], [00040]

Liu Provisional discloses the following at Fig. 12

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 2:62-3:29; 4:20-52; 4:56-59; 5:36-64; 6:20-41; 6:47-7:8; 8:1-10; 8:49-10</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

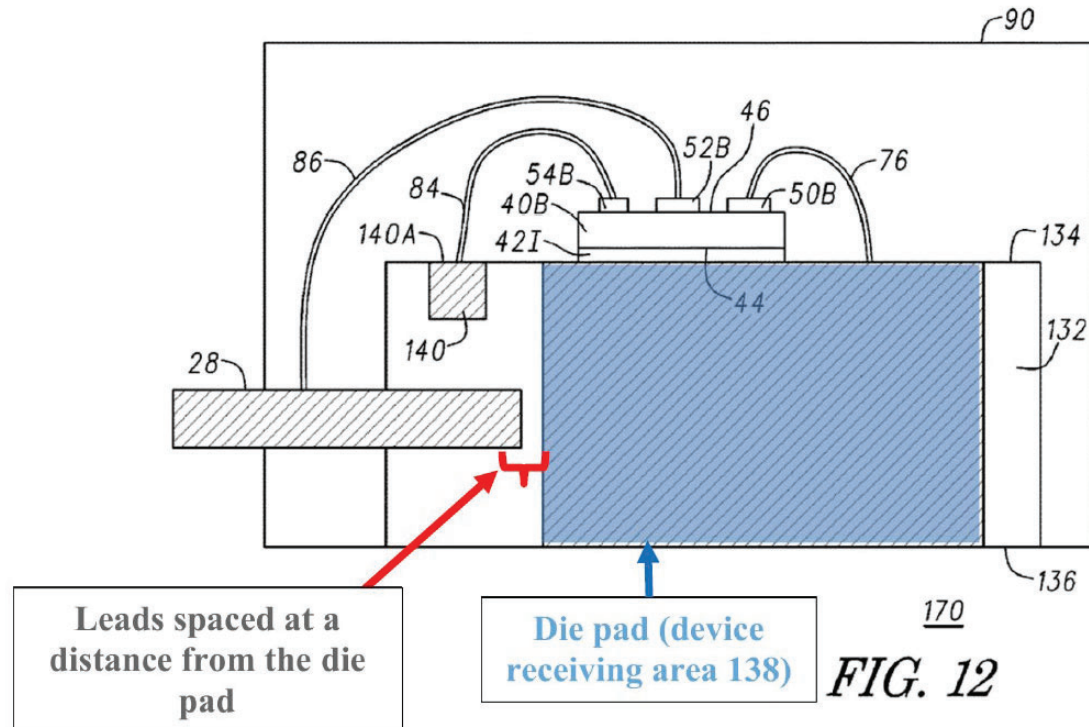
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>Second Lead (lead 30)</p> <p>FIG. 11</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>FIG. 11</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p>First Lead (lead 26)</p> <p>Die pad (device receiving area 138)</p> <p>Leads spaced a distance from the die pad</p> <p>Third Lead (lead 28)</p> <p>Second Lead (lead 30)</p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 17

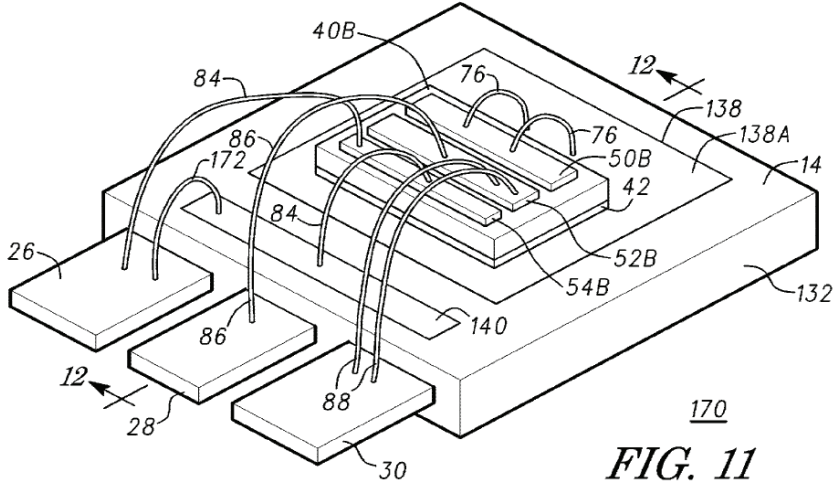
Exemplary Disclosure based on *Liu* and Related Combinations

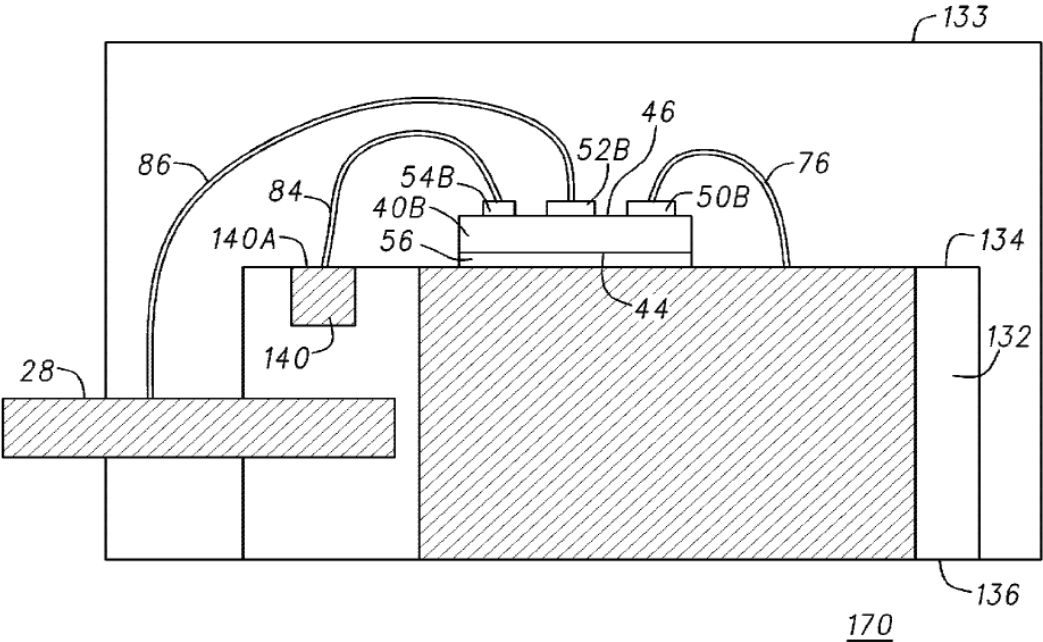


Liu Provisional discloses the following at [00042]

A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact 54B

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00020], [00023]-[00024], [00026], [00031], [00033], [00035], [00041], [00044]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

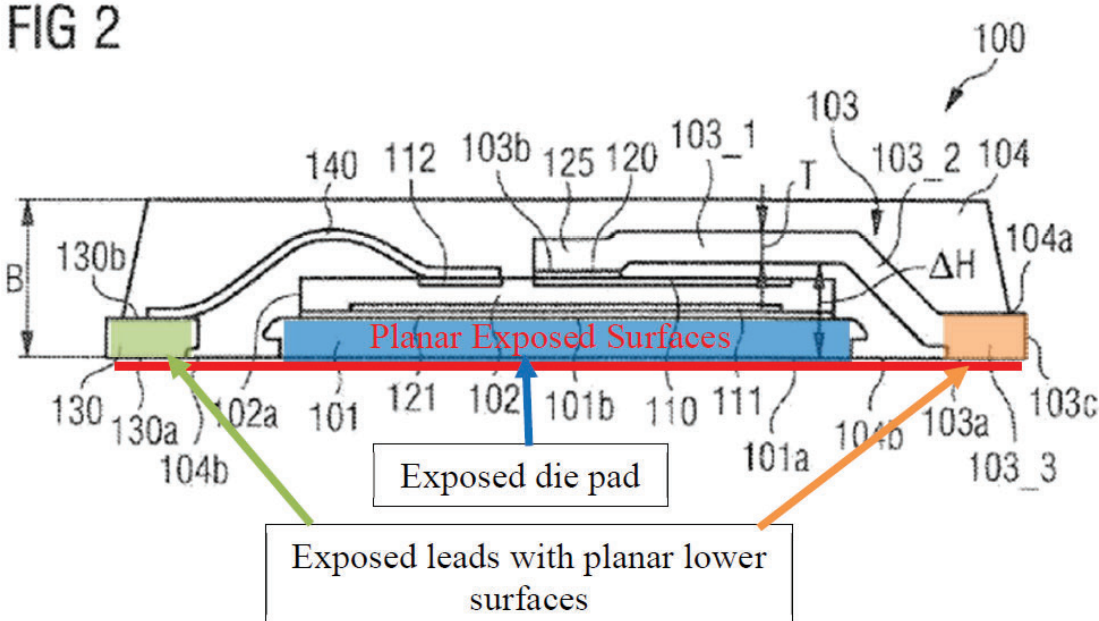
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 11</p> <p><i>Liu Provisional</i> discloses the following at Fig. 12</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p>
<p>[17d] wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and</p>	<p><i>Liu</i> alone or in combination with other references discloses or renders obvious wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces. <i>See supra</i> claim 4.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 7:14-38</p>

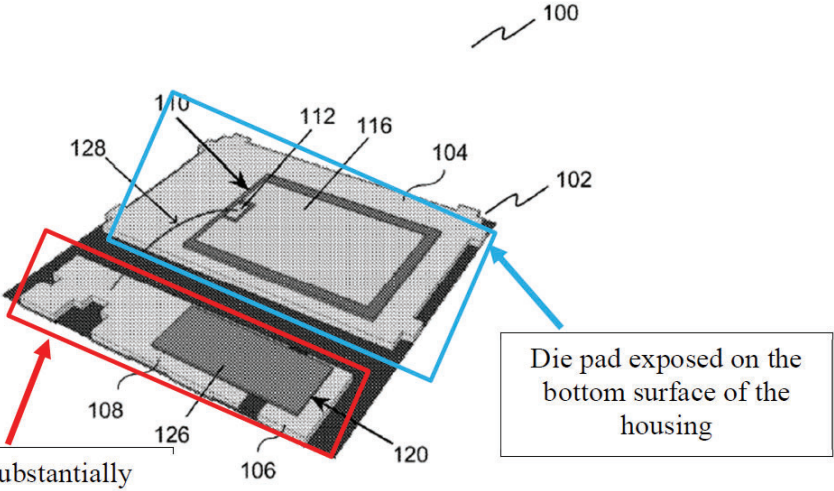
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
provide substantially planar contact surfaces,	<p>FIG. 9 is a perspective view of a semiconductor component 150 in accordance with another embodiment of the present invention. Semiconductor component 150 is similar to semiconductor component 100 described with reference to FIG. 4 except the semiconductor device is identified by reference character 40A, i.e., the letter A has been appended to reference character 40, because drain contact 50 has been replaced by a drain contact 50A which extends over a portion of an active area of III-N semiconductor device 40A and source contact 52 have been replaced by a source contact 52A which extends over another portion of the active area of III-N semiconductor device 40A. It should be noted that mounting semiconductor chips to device receiving areas has been described with reference to FIGS. 1 and 2. Thus, semiconductor component 150 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40A.</p> <p><i>Liu</i> discloses the following at 8:11-26</p> <p>A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10.</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.</p> <p>Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu, 2:62-3:29; 4:42-51; 5:8-13; 5:31-64; 6:42-46; 7:9-13; 7:63-67</i></p> <p><i>Liu</i> discloses the following at Fig. 12 (annotated)</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>comprise an external contact area exposed at the encapsulation body of a leadless package. The external terminal of the semiconductor device may also be a lead of a leaded package.</p> <p>Otremba433 discloses the following at [0027]</p> <p>FIG. 1 illustrates a top view of an exemplary semiconductor device 100 in accordance with one embodiment. The semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104. FIG. 2 schematically illustrates a cross-sectional view of the semiconductor device 100 shown in FIG. 1 along section line A-A.</p> <p>Otremba433 discloses the following at [0037]</p> <p>The encapsulation body 104 of the semiconductor device 100 may embed the carrier 101 and the semiconductor chip 102 at side and top faces. The terminal portion 103_3 of the contact clip 103 forms an external terminal of the semiconductor device 100 and, therefore, protrudes out of the encapsulation body 104. By way of example, as illustrated in FIGS. 1 and 2, the semiconductor device may have a leadless package. In this and other cases the terminal portion 103_3 of the contact clip 103 may have an external contact area 103 a exposed at the encapsulation body 104, e.g., at the bottom of the package. The external contact area 103 a may be coplanar with a reference plane defined by a bottom surface 101 a of the carrier 101. The bottom surface 101 a of the carrier 101 may also be exposed at the bottom of the package. Further, a bottom surface portion 104 b of the encapsulation body 104 may be coplanar with the reference plane defined by the bottom surface 101 a of the carrier 101. In this case, the bottom surface 101 a of the carrier, the bottom surface portion 104 b of the encapsulation body 104 and the external contact area 103 a of the terminal portion 103 may all be arranged substantially level with each other. They may form the bottom of the package.</p> <p>Otremba433 discloses the following at [0039]</p> <p>The lead post 130 may form another external terminal of the semiconductor device 100. A bottom surface 130 a of the lead post 130 may be exposed at the bottom surface of the package of</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>the semiconductor device 100 in order to e.g., provide for another SMT external contact area of the package.</p> <p>See also Otremba433, [0040], [0042]</p> <p>Otremba433 discloses the following at Fig. 2 (annotated)</p> <p>FIG 2</p>  <p>Otremba280 discloses the following at 4:1-29</p> <p>The electronic component 10 comprises two semiconductor devices 11, 12 whose first load electrodes 17 (sources) are electrically connected to one another and to a lead 23 of the leadframe 13 by a single</p>

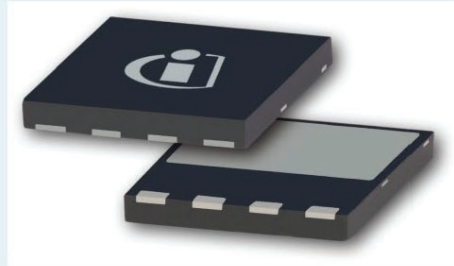
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>electrically conductive element in the form of a contact clip 14. The contact clip 14 may be provided in the form of a metal strip having the lateral size and shape and vertical form adapted to extend between the first load electrodes 17 of two semiconductor devices 11, 12 and the upper surface 35 of a lead 23 of a leadframe 13. In this embodiment, the leadframe 13 is positioned within the electronic component at a level below the first side of the semiconductor devices 11, 12. The upper surface of the lead 23 may lie generally coplanar with the second side 16 of the semiconductor devices 11, 12. The contact clip 14 may have a general form and height adapted to accommodate the thickness of the semiconductor devices 11, 12. Typically, the device carrier portion 19 and the leads 20 of the leadframe 13 are stamped or etched from a metal sheet so that the upper side 35 of the device carrier portion 19 and the upper side 35 of the leads 20 are generally coplanar with one another. The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a surface mountable or leadless type electronic component. Alternatively, the outer portions of the leads may be bent in a general direction away from the first side of the two semiconductor devices to provide pins by which the electronic component 10 may be mounted on a redistribution board such as a printed circuit board.</p> <p>Otremba124 discloses the following at [0041]</p> <p>In an example, the power transistor arrangement 100 with a flipped SFET and a wire bonded GaN HEMT may be packaged in a 8x8 ThinPAK, wherein the GaN HEMT 110 may be a high voltage (e.g. larger than 200V) HEMT switch and the SFET 120 may be a low voltage (e.g. smaller than 200V) power MOSFET. The GaN HEMT 110 is a normally on device, and is transformed to a normally off transistor with introducing of the low-voltage SFET 120. Such a GaN-SFET arrangement 100 may correspond to the cascade circuit 500 of FIG. 5.</p> <p>Otremba124 discloses the following at Fig. 1 (annotated)</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p data-bbox="898 820 976 852">FIG. 1</p> <p data-bbox="562 722 840 852">Leads – Substantially planar contact surfaces on the lower external surface of the housing</p> <p data-bbox="1207 609 1501 706">Die pad exposed on the bottom surface of the housing</p> <p data-bbox="493 917 1123 950">ThinPak8x8 Brochure discloses the following at 1</p>

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations

ThinPAK 8x8



**New High Voltage
SMD-Package**

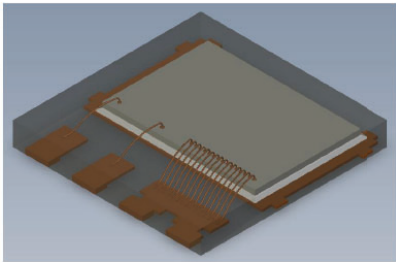
**April 2010
Version 1.0**

Page 1 of 34



INNOSCIENCE EXHIBIT 1016

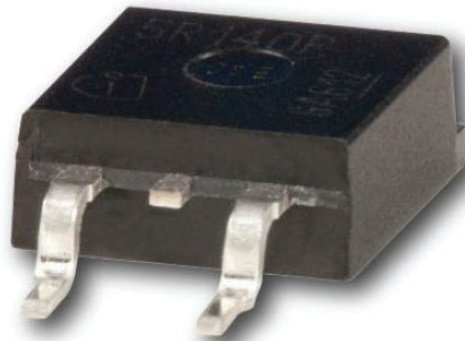
ThinPAK8x8 Brochure discloses the following at 5

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<div data-bbox="562 313 1696 418"> <div data-bbox="594 375 999 418">Package specification</div> <div data-bbox="1556 354 1667 402">  </div> </div> <ul data-bbox="594 456 1520 943" style="list-style-type: none"> ■ SMD package - leadless ■ Height: 1 mm package height ■ Footprint smaller than D2PAK (8 x 8 mm²) ■ Rdson -> similar to D²PAK / TO220 ■ Creepage distance: 2.7 mm ■ Low Parasitics (package inductivity, package resistance) ■ Double sided cooling (optional) ■ Soldering: wave and reflow ■ Green mold compound <div data-bbox="1220 824 1612 1084">  </div> <div data-bbox="594 1133 659 1154"> <p>April 2010</p> </div> <div data-bbox="604 1162 743 1192"> <p>Page 5 of 34</p> </div> <div data-bbox="1623 1133 1667 1154"> <p>Page 5</p> </div> <p data-bbox="489 1252 1146 1284">ThinPAK8x8 Brochure discloses the following at 6</p>

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations

ThinPAK 8x8 versus D²PAK



10 x 15 x 4.4 mm³



8 x 8 x 1 mm³

60 % footprint reduction - 80% height reduction - 90% Volume reduction

April 2010

Page 6

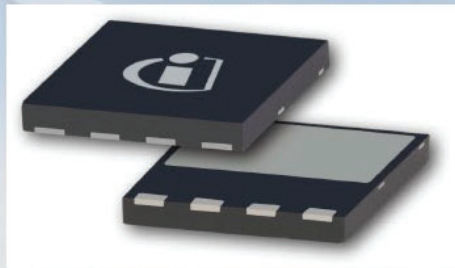
Page 6 of 34

See also ThinPAK8x8, 3, 21, 31, 33

ThinPAK Recommendations discloses the following at 1



**Recommendations
for Printed Circuit Board Assembly of In-
fineon VDSO Packages (ThinPAK)**



Application Note

Infineon VDSO Packages (ThinPAK)

July 2010

Published by Infineon Technologies AG
<http://www.infineon.com/coolmos>

Page 1 of 27

INNOSCIENCE EXHIBIT 1017

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	ThinPAK Recommendations discloses the following at 4



1. Package Description

The PG-VDSON (Plastic Green High Voltage Small Single Outline Package) is a near chip-scale plastic encapsulated package with a copper leadframe and pads at the bottom of the package to provide electrical and thermal contact to the printed circuit board.

The PG-VDSON (alias ThinPAK) is a leadless package consuming smaller area for high voltage applications compared to e.g. packages like D²PAK

Characteristics

- Small package outline 8x8 mm²
- Low profile 1 mm
- Exposed drain pad for optimized heat transfer to the PCB
- Pads with Pb-free solder plating (electroplated Sn)

Figure 1 shows a photo of PG-VDSON-4 packages (alias ThinPAK 8x8). Visible are the 4 small Source/Gate-Pads, which show exposed copper at the package side wall (due to package singulation) and the big exposed drain pad which is fully surrounded by mold compound.

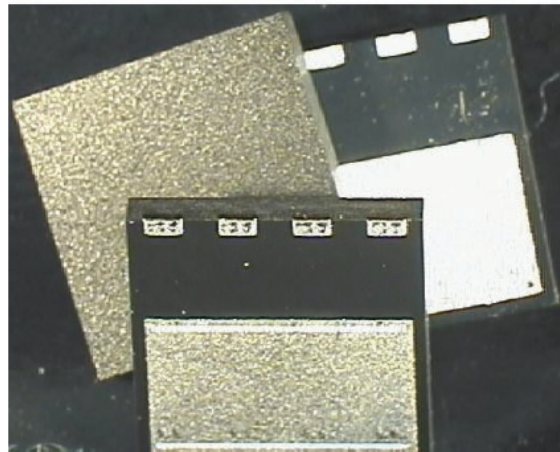
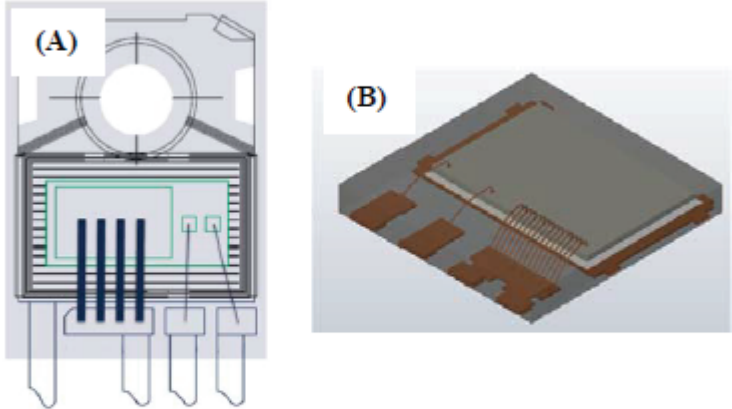


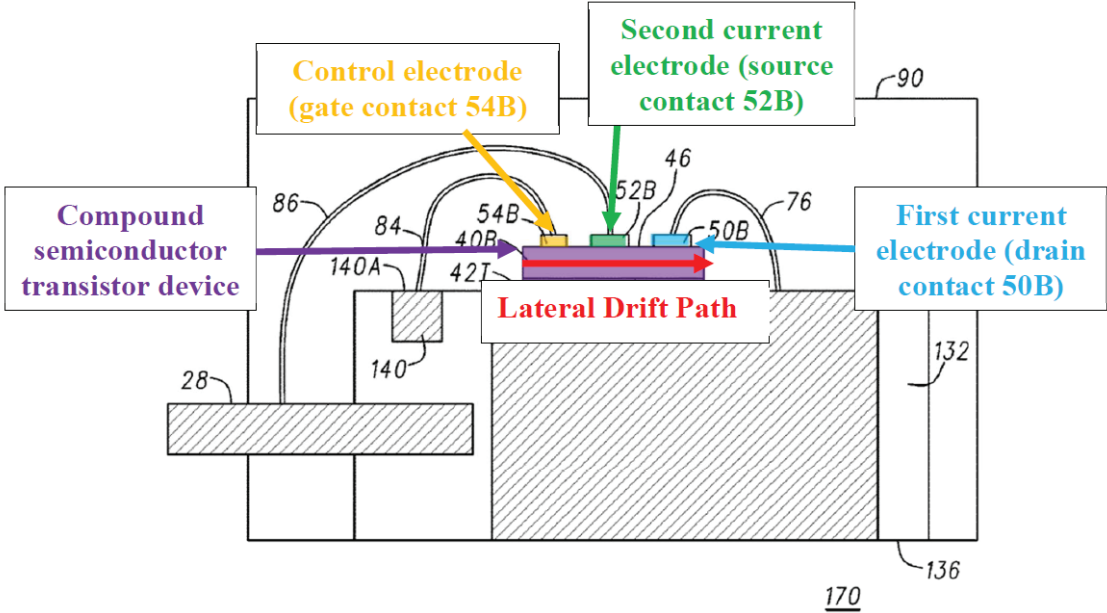
Figure 1: Top and bottom view of VDSON-4 (ThinPAK 8x8)

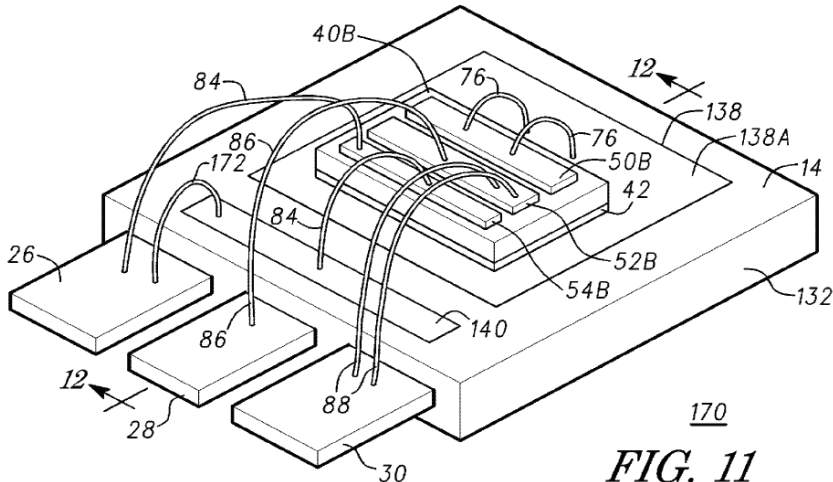
Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Lind discloses the following at 3</p> <p>III. Source-Sense concept and A/B simulation</p> <p>A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.</p> <div data-bbox="556 456 1283 862">  </div> <p>Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections</p> <p>The principle is to provide a separate path for the drain-source current, such that voltage generated across the source inductance no longer appears in the KVL mesh of the gate current loop.</p>
<p>[17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based</p>	<p><i>Liu</i> alone or in combination with other references renders obvious wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad. <i>See supra</i> claims 1-2.</p> <p>For example,</p> <p><i>Liu</i> discloses that the compound semiconductor transistor device is a lateral transistor because the device is arranged laterally with the electrodes on the same lateral plane in a lateral drift path with the current generally flowing parallel to the surface. The '481 patent explains that “lateral” means “run[ning] generally parallel to</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
transistor device is coupled to the die pad,	<p>the lateral extent of a semiconductor material or semiconductor carrier” (’481 patent, 3:14-18) and describes a device that “has a lateral drift path” (’481 patent, 4:37-38). Smart Power ICs (Innoscience 1414-00012740 – Innoscience 1414-00012823) defines a horizontal (i.e. lateral) transistor as a structure where “current enters and leaves the chip through the upper surface of the chip.” At 7.</p> <p><i>Liu</i> discloses the following at 3:30-61</p> <p>A semiconductor chip 40 is bonded to surface 18A of device receiving area 18 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. More particularly, surface 44 of semiconductor chip 40 is bonded to surface 18A of device receiving area 18 through electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40 is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40 includes a field effect semiconductor device having a drain contact 50 formed on or from a portion of surface 46, a source contact 52 formed on or from another portion of surface 46, and gate contacts 54 and 55 formed on or from other portions of surface 46. It should be noted that the semiconductor device is not limited to being a field effect transistor. For example, the semiconductor device may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. In accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 40, semiconductor chip 40 may be referred to as a semiconductor device. In addition, die attach material 42 is not limited to being an electrically conductive material but may be an electrically insulating material or a thermally conductive material. By way of example, semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride. A III-nitride semiconductor material may be referred to as a III-N semiconductor material, a III-nitride based semiconductor material, a III-N based semiconductor material, or the like.</p> <p><i>Liu</i> discloses the following at 8:27-48</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172.</p> <p>Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu, 5:65-6:41; 6:47-7:8; 7:15-32</i></p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Compound semiconductor transistor device</p> <p>Lateral Drift Path</p> <p>First current electrode (drain contact 50B)</p> <p>Second current electrode (source contact 52B)</p> <p>Control electrode (gate contact 54B)</p> <p>FIG. 11</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	 <p style="text-align: center;">FIG. 12</p> <p><i>Liu Provisional</i> discloses the following at [00043]</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus,</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00022]-[00023], [00032]-[00033], [00035], [00037], [00039], [00042]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>  <p>FIG. 11</p> <p><i>Liu Provisional</i> discloses the following at Fig. 12</p>

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations

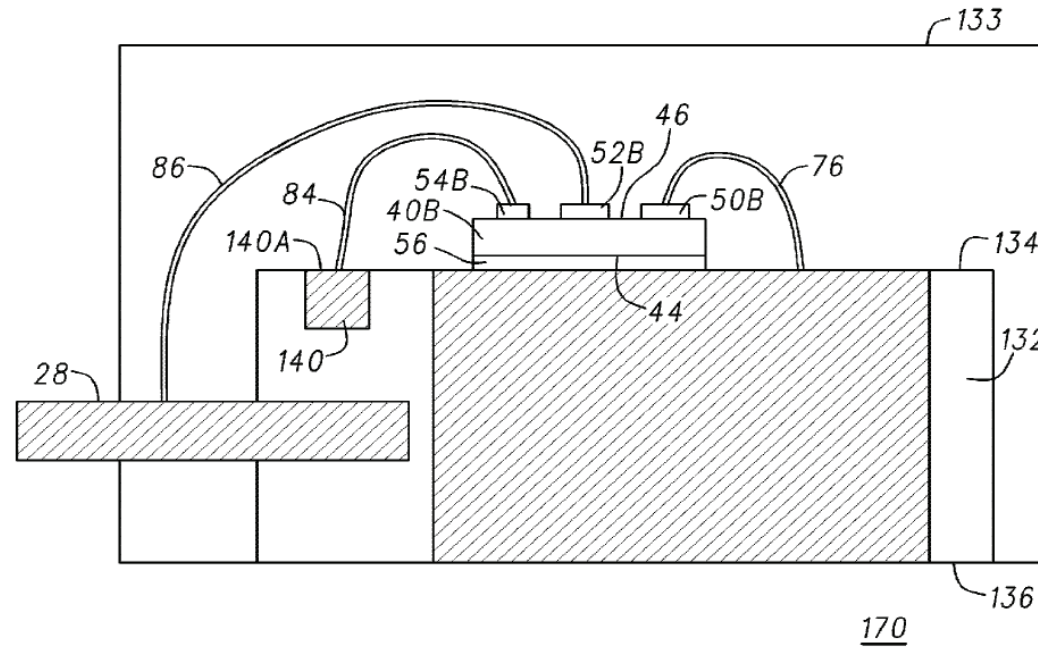


FIG. 12

Liu Provisional discloses the following at [00021]

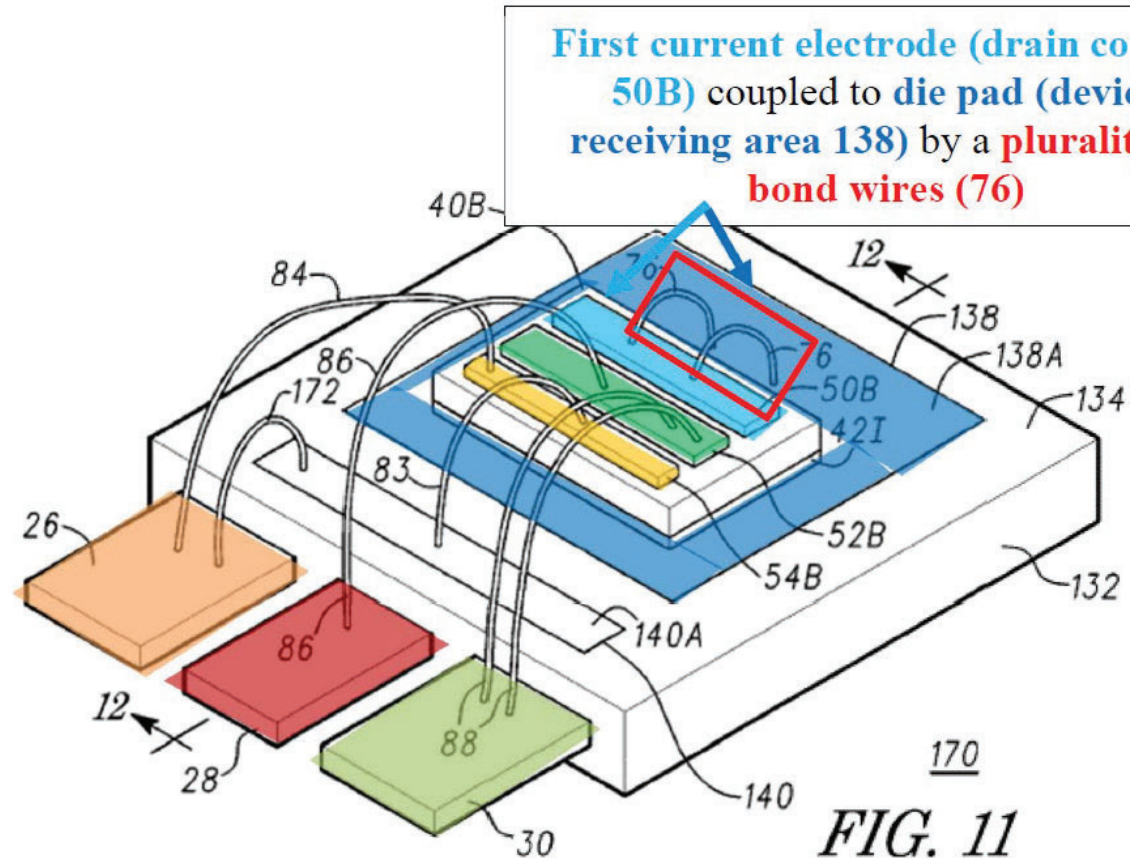
A semiconductor chip 40 is bonded to surface 18A of device receiving area 18 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. More particularly, surface 44 of semiconductor chip 40 is bonded to surface 18A of device receiving area 18 through electrically insulating die attach material 42. In accordance with an embodiment, semiconductor chip 40 is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40 includes a field effect semiconductor device having a drain contact 50 formed on or from a portion of surface 46, a source contact 52 formed on or from another portion of surface 46, and gate contacts 54 and 55

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>formed on or from other portions of surface 46. It should be noted that semiconductor device 48 is not limited to being a field effect transistor. For example, semiconductor device 48 may be an insulated gate bipolar transistor, a bipolar transistor, a junction field effect transistor, a diode, or the like. In accordance with embodiments in which a discrete semiconductor device such as for example, a field effect transistor, is formed from semiconductor chip 40, semiconductor chip 40 may be referred to as a semiconductor device. In addition, die attach material 42 is not limited to being an electrically conductive material but may be an electrically insulating material or a thermally conductive material. By way of example, semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride. A III-nitride semiconductor material may be referred to as a III-N semiconductor material, a III-nitride based semiconductor material, a III-N based semiconductor material, or the like.</p>
<p>[17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.</p>	<p><i>Liu</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip. <i>See supra</i> claim 1.</p> <p>For example,</p> <p><i>Liu</i> discloses the following at 8:27-48</p> <p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III-N cascode switch in which the substrate of the III-</p>

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu</i>, 4:20-41; 4:60-5:7; 5:14-30; 6:20-41; 6:47-7:8; 7:39-62; 8:49-9:10</p> <p><i>Liu</i> discloses the following at Fig. 11 (annotated)</p>

Claim 17

Exemplary Disclosure based on *Liu* and Related Combinations



Liu Provisional discloses the following at [00043]

Claim 17	Exemplary Disclosure based on <i>Liu</i> and Related Combinations
	<p>Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact S4B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172. Thus, semiconductor component 170 includes a III -N cascade switch in which the substrate of the III -N semiconductor material is electrically floating and bond pads are formed over active regions of semiconductor device 40B.</p> <p><i>See also Liu Provisional</i>, [00023], [00027], [00029], [00033], [00035], [00039]</p> <p><i>Liu Provisional</i> discloses the following at Fig. 11</p>

