

INNOSCIENCE'S INITIAL INVALIDITY CONTENTIONS

US 9,899,481 B2

APPENDIX A-2

***In the Matter of:
CERTAIN SEMICONDUCTOR DEVICES, AND PRODUCTS
CONTAINING THE SAME***

Investigation No. 337-TA-1414

APPENDIX A-2
INVALIDITY CLAIM CHART FOR U.S. PATENT NO. 9,899,481 B2¹
NEGA

U.S. Patent Application Publication No. 2014/0110760 (“*Nega*”) (Innoscence 1414-00007194 - Innoscence 1414-00007215) published on April 24, 2014, qualifies as prior art to U.S. Patent No. 9,899,481 (the ’481 Patent) at least under 35 U.S.C. §§ 102(a)(2).²

The following list identifies one or more references cited in certain grounds for invalidity of claim 1-4, 6, 9 and 17 of the ’481 Patent based on *Nega*:

- U.S. Patent Application Publication No. 2014/0175454 (“Roberts”) (Innoscence 1414-00007223 - Innoscence 1414-0007240) published on June 26, 2014 making it prior art at least under 35 U.S.C. § 102(a)(2).
- U.S. Patent Application Publication No. 2014/0084433 (“Otremba433”) (Innoscence 1414-00007167 - Innoscence 1414-00007179) published March 27, 2014 making it prior art under at least 35 U.S.C. § 102(a)(1).
- U.S. Patent Application Publication No. 2014/0225124 (“Otremba124”) (Innoscence 1414-00007241 - Innoscence 1414-00007254) published August 14, 2014 making it prior art under at least 35 U.S.C. § 102(a)(1).

As illustrated below, one or more claims of the ’481 Patent are invalid as expressly and/or inherently anticipated by *Nega*, including asserted claims 1-4, 6, 9, and 17. Additionally, to the extent that *Nega* is found not to anticipate, expressly or inherently, claim 1 of the ’481 Patent, it is invalid as obvious in view of *Nega* alone or in combination with other prior art references, including, but not limited

¹ The claim chart below is meant to illustrate how the identified reference identified above invalidates the asserted claims. By not discussing other portions of the reference in the chart below, Respondents do not waive their right to rely on other portions of the reference; instead, Respondents expressly reserve their right to rely on other portions of the reference. These contentions are not an admission by Respondents that any accused products, including any past, or current, or future version of these products, are covered by or infringe Complainant’s’ asserted claim, particularly once the claim is construed by the ALJ, and do not constitute an admission by Respondents as to the proper construction of any asserted claim, and citations may be based on Complainant’s’ apparent construction of the claim. These contentions are not an admission by Respondents as to the proper scope of any asserted claim or the proper construction of any asserted claim. Respondents reserve the right to modify, amend, or supplement these contentions as additional information becomes available.

² All statutory citations refer to AIA law.

to, the prior art discussed below, the prior art identified in the Respondents' Invalidity Contentions, and the prior art described in additional claim charts attached as Appendices A-1 through A-5. Exemplary invalidity grounds based on the *Nega* reference include the following, although these examples are by no means limiting:

- Obviousness based on *Nega* in combination with Roberts (claims 1-3 and 6);
- Obviousness based on *Nega* in combination with Roberts and Otremba124 (claims 4, 9, and 17);
- Obviousness based on *Nega* in combination with Roberts and Otremba433 (claims 4 and 17)

The citations included in the table below are exemplary only and are not intended to be limiting or exhaustive. Respondents reserve the right to cite additional disclosures and evidence in support of their positions as the Investigation develops further.

Additionally, Respondents may be basing the arguments below on claim interpretations suggested in Complainant's infringement and domestic industry claim charts provided with the Complaint, as best as they can be deciphered. By applying the prior art in this way, Respondents do not concede their agreement with Complainant's positions, nor do these Invalidity Contentions constitute any admission regarding claim scope. Nor are Respondents asserting any claim construction positions through these charts. Moreover, preambles generally are not limiting, and nothing in these contentions should be deemed an admission that the preamble in the asserted claims is limiting.

As these proceedings further develop, Respondents intend to amend or supplement these exemplary disclosures and any related contentions as appropriate, and in a manner consistent with all applicable rules governing this Investigation. In particular, Respondents reserve the right to rely on (1) uncited portions of the identified prior art; (2) other prior art not identified herein; (3) references that show the state of the art (irrespective of whether such references themselves qualify as prior art to the asserted patents); (4) factual testimony from the named inventors or authors of the prior art references; and/or (5) expert testimony, to provide context to or aid in understanding the prior art and the state of the art at the time of the alleged inventions.

Descriptions of Exemplary Obviousness Combinations Based on *Nega*

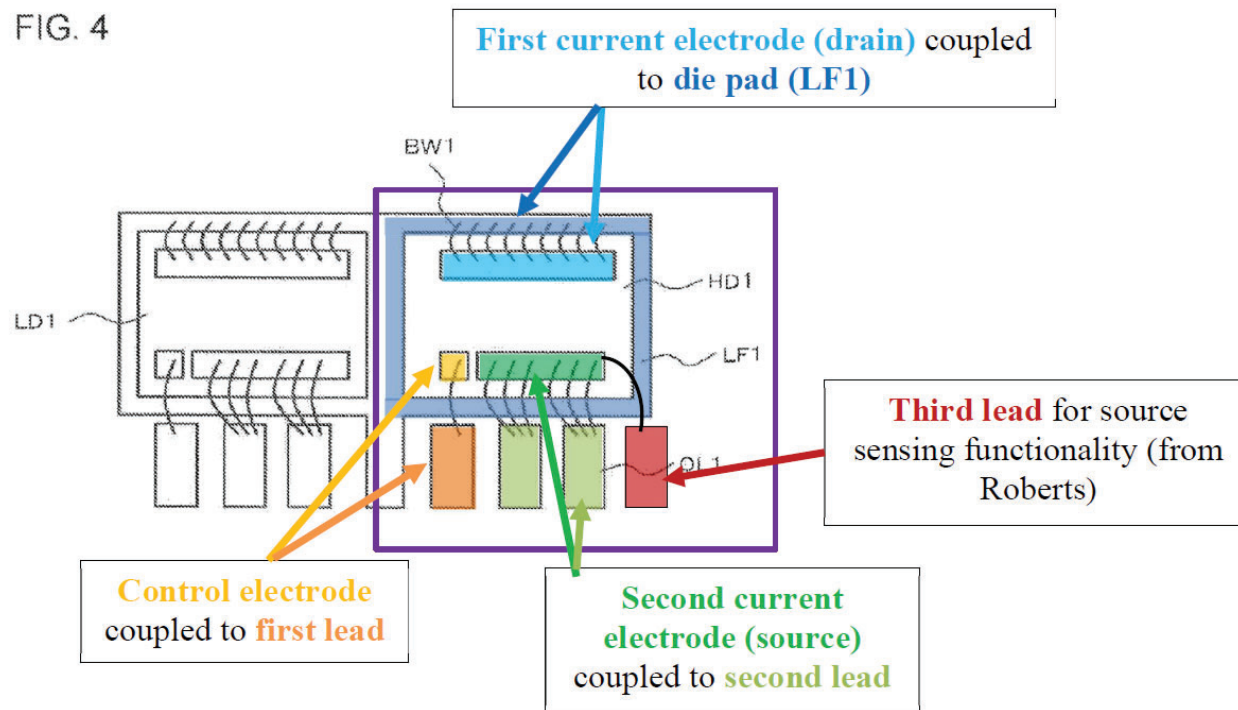
All references are analogous because a POSITA would have understood that they are in the same field of endeavor as the '481 patent—packaging semiconductor electronic components. *Nega*, [0094]-[0095], Fig. 4; Roberts, [0006], [0008], [0012], [0056]; Otremba124, [0041], Fig. 1; Otremba433, [0037], [0039], [0072], Fig. 2; *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004). Because a POSITA would have understood that they are all directed to the same type of packaging semiconductor electronic components, a person of ordinary skill

in the art would have appreciated that *Nega* and the additional references cited below come from the same field of endeavor and provide disclosures that relate to one another.

The combination of *Nega* with one or more of the additional references would involve one or more of: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to obtain predictable results; use of a known technique to improve similar devices in the same way; applying a known technique to the device ready for improvement to yield predictable results; obvious trying given a finite number of identified, predictable solutions, and a reasonable expectation of success; known work in one field of endeavor that prompts variations for use in the same field based on design incentives or market forces; and a teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at claims 1-4, 6, 9, and 17.

For example, in Roberts, a Kelvin Source Sense connection SS is provided by “separate Kelvin connection(s)” (Roberts, [0095]), which would be routinely implemented in *Nega*’s device by adding an additional external connection or contact pad connected to the transistor, for source sensing functionality, as seen in Huang and McKnight. Huang (Innoscence 1414-00007460 - Innoscience 1414-00007465); McKnight (Innoscence 1414-00006981 - Innoscience 1414-00007001). Roberts expressly discloses that in lateral GaN transistor devices, the package includes an additional external contact pad, e.g.,] a source sense (Kelvin) connection. Further Otremba528 recognizes that a “source-sensing lead may be connected to a source contact to measure and/or monitor the potential source contact,” which is the same purpose as Robert’s Kelvin source sense connection. Otremba528 (Innoscence 1414-00007180 - Innoscience 1414-00007193). A POSITA would have understood that a source sensing leading would be connected to a source contact to measure and/or monitor the potential of the source contact. A POSITA would have been motivated to implement Robert’s source sensing connection as a third lead in *Nega*’s device and would have expected success because source sensing functionality had known benefits, and implementing source sensing functionality as a separate lead was known in the art—combining prior art elements according to known techniques to a known device ready for improvement to yield predicable results. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2001). *Nega*-Roberts teach the following configuration, with the control electrode coupled to the first lead (*Nega*), the first current electrode coupled to the die pad (*Nega*), the second current electrode coupled to the second lead (*Nega*), and the third lead coupled to the compound semiconductor transistor device and providing a source sensing functionality (Roberts).

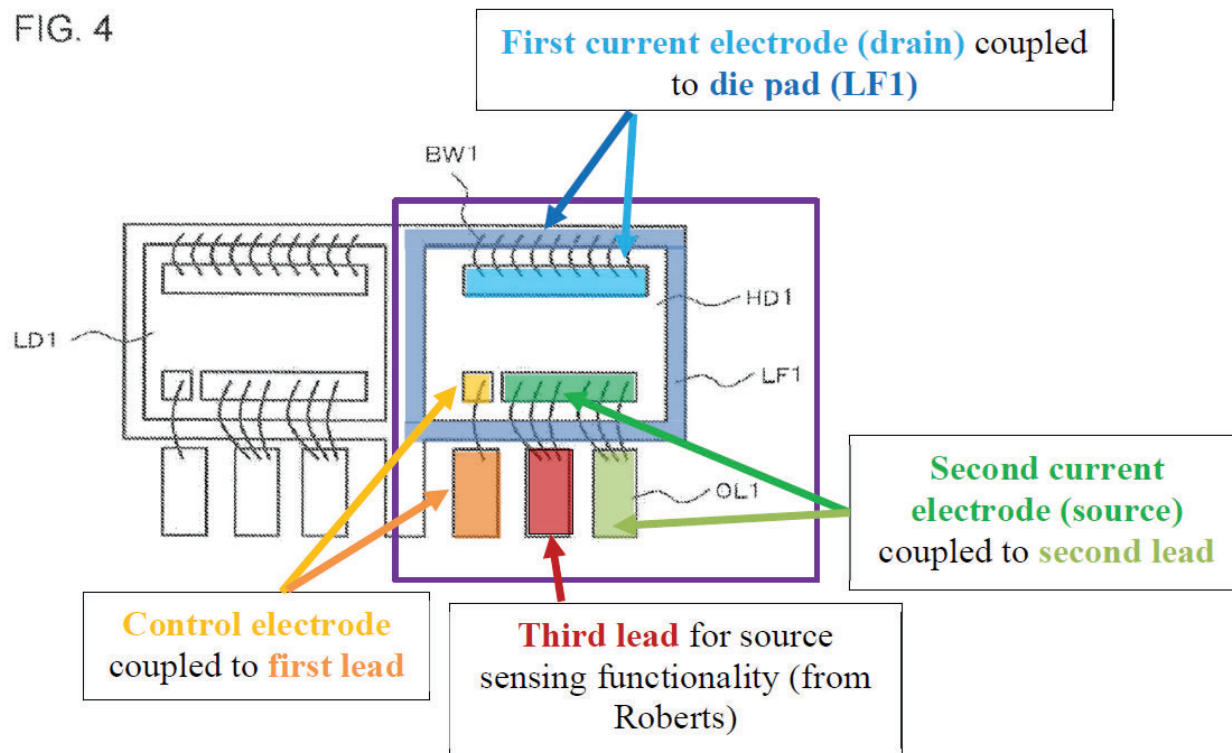
FIG. 4



Nega, Fig. 4 modified to add Roberts' source sensing third lead.

Additionally, a POSITA would have understood that one of “these leads would readily be modified to serve as a lead for source sensing functionality, as taught by Roberts” because it was “known to interchange leads in packaging structures based on the application”; for example, *Nega* discloses interchanging the source and drain leads (*Nega*, [0095])). A POSITA would have understood that leads would simply be repurposed as a design choice within the skill of a POSITA with a reasonable expectation of success.

FIG. 4



Nega, Fig. 4 (annotated).

A POSITA also would have understood that *Nega*'s compound semiconductor device would have achieved a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, which were common for high-voltage compound semiconductor power conversion transistors, as explained expressly by Roberts. The '481 patent explains that a transistor device's blocking voltage capability is its capability to block a voltage when the transistor is off—the maximum voltage that can be applied to a transistor while preserving operation. '481 patent, 3:41-50. Blocking voltage is also referred to as breakdown voltage. Roberts discloses that high-voltage (e.g., high blocking voltage capability) transistors were common in the art. Roberts explains that high-voltage transistor devices, "e.g., 600/650V" in "normally-on (depletion mode) transistors," were well known. Roberts, [0006], [0012]. A POSITA would have understood that a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz were standard, routine, and readily-achievable characteristics for high-voltage compound semiconductor transistors (like *Nega*). Higher

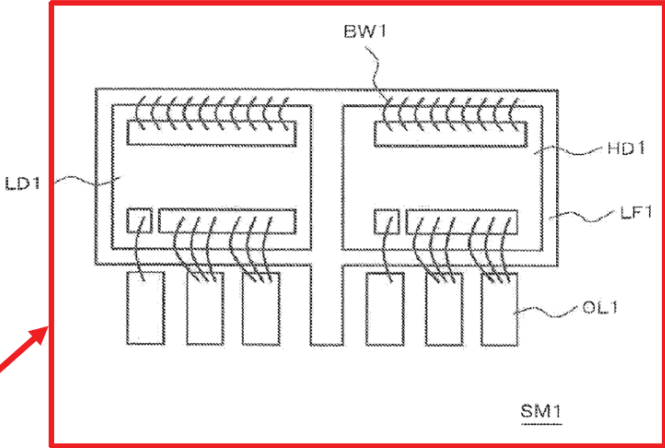
blocking voltage capability and faster switching frequencies were some of the very benefits boasted by compound semiconductor devices generally, as opposed to traditional Si-based devices. Because *Nega* discloses compound semiconductor transistor devices but is silent on the corresponding switching time or frequency, a POSITA would have been motivated to look to references disclosing expected switching frequencies for compound semiconductor devices, like Roberts. Here, as in *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1374 (Fed. Cir. 2019), a POSITA would have looked to references like Roberts “to better understand or interpret” the achievable characteristics of *Nega*’s device, including the switching frequency. *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1371 (Fed. Cir. 2018) (a motivation to combine may be based on “the background knowledge, creativity, and common sense of the person of ordinary skill” (quoting *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354 (Fed. Cir. 2013))). Because these characteristics were common, well known, and readily achievable in compound semiconductor transistor devices, a POSITA would have had a reasonable expectation that *Nega*’s compound semiconductor transistor device would operate with a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

A POSITA would have been motivated and found it obvious to package *Nega*’s HT1 (HD1) in Otremba124’s ThinPAK8x8 package with an exposed die pad and planar lead contacts on the lower surface. ThinPAK8x8 was boasted as an improvement on other leaded packaging designs, saving space on the printed circuit board (PCB) with a footprint of 64mm² (as opposed to 150mm² for competitive devices). ThinPAK 8x8 New High Voltage SMD-Package (“ThinPAK8x8 Brochure”) (Innoscience1414-00007539 - Innoscience1414-00007572), 3. A POSITA would have understood that because ThinPAK8x8 was leadless, it showed faster performance and switching speeds than through-hole and other conventional packages (like the TO220), enabling improved performance, switching behavior, ease of use, EMI (electromagnetic interference), reliability, and higher power density. *Nega* recognizes that it implements a standardized TO220 package (a leaded package) as an exemplary package design and would have realized the known benefits ThinPAK8x8 offered as improvements to a device ready for such improvement. ThinPAK8x8 with source sensing connections as an alternative to a similar leaded package as would have been obvious to a POSITA. Packaging *Nega*-Roberts as a ThinPAK8x8, disclosed by Otremba124, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416. Additional package formats, including leadless, exposed-die packages, were also known as taught by Otremba124 and would have been at least considered suitable options for packaging *Nega*’s compound semiconductor transistor device HT1 (HD1). *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021); *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197-98 (Fed. Cir. 2014). And additional, similar packaging types were known, including those with source sensing leads, like a DFN8x8 package.

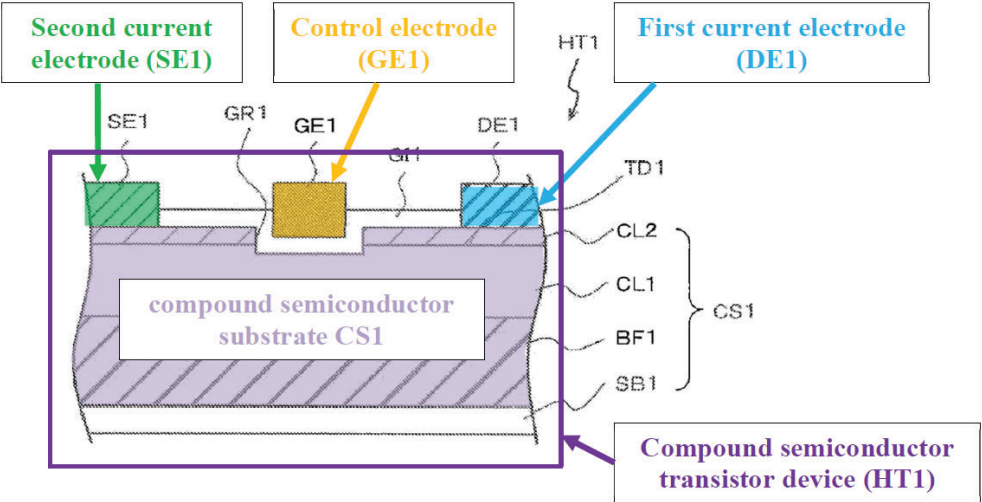
For example, a POSITA would have understood *Nega*’s device to be readily implemented in a leadless package (like Otremba433) and would have realized the known benefits of leadless package designs. Packaging *Nega*-Roberts as a leadless package, disclosed by Otremba433, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results. *KSR*, 550 U.S. at 416. Leadless, exposed-die packages, were known, as taught by Otremba433, and would

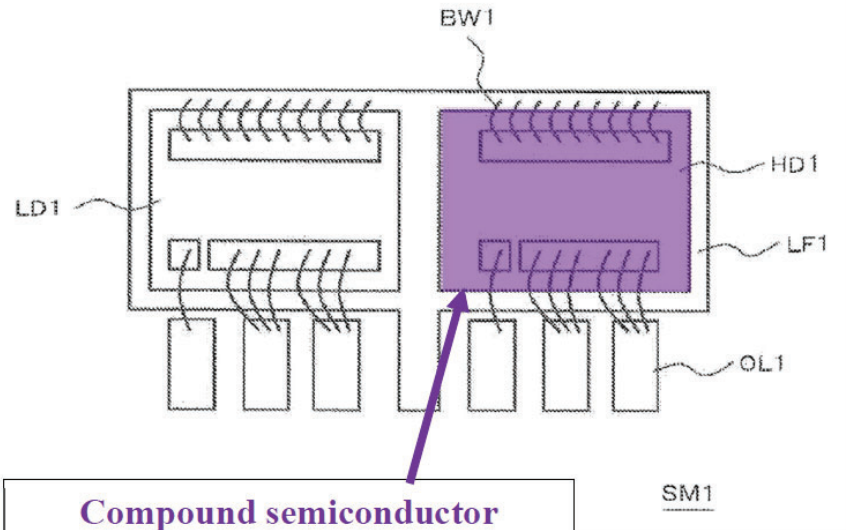
have been at least suitable options for packaging *Nega*'s device. *Intel*, 21 F.4th at 800; *PAR Pharm.*, 773 F.3d at 1197-98. Otremba433 recognizes that leaded and leadless packages were both possible for packaging semiconductor devices. Otremba433, [0025].

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[1p] An electronic component, comprising:	To the extent the preamble is limiting, <i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious an electronic component. For example, <i>Nega</i> discloses the following at [0018] FIG. 4 is a plan view illustrating an example of the semiconductor device according to the first embodiment. <i>Nega</i> discloses the following at [0090] FIG. 4 is a plan view illustrating an example of the semiconductor device SM1 according to the present embodiment. <i>Nega</i> discloses the following at Fig. 4 (annotated)

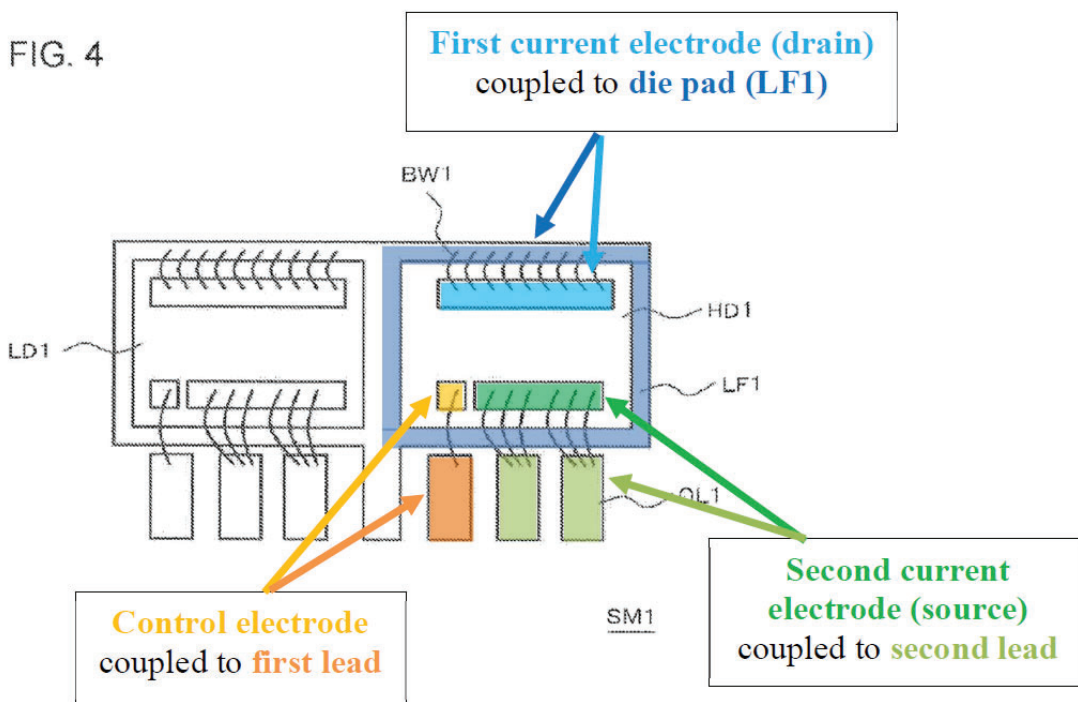
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4  Electronic component (SM1)
[1a] a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode. For example, <i>Nega</i> discloses the following at [0034] According to such a configuration, the transistor HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1, thereby allowing a switching device having a lower loss than a silicon device to be realized. For this reason, it is possible to achieve an improvement in the power source efficiency of the DC/DC converter circuit. In addition, the transistor HT1 connected to the input terminal is configured to be a normally-off type, thereby

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	allowing flow of a through-current into a circuit in a state where power is not completely supplied to the DC/DC converter circuit to be suppressed, without newly providing a protection circuit. Therefore, it is possible to suppress complication of a circuit. <i>Nega</i> discloses the following at [0046] As shown in FIG. 2, the transistor HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1. In addition, the transistor HT1 is a normally-off type transistor. <i>Nega</i> discloses the following at [0049] The compound semiconductor layer CL1 is provided on the buffer layer BF1. The compound semiconductor layer CL1 is, for example, a GaN layer. The thickness of the compound semiconductor layer CL1 is, for example, 1 μm. <i>Nega</i> discloses the following at [0050] The compound semiconductor layer CL2 is provided on the compound semiconductor layer CL1. As the compound semiconductor layer CL2, a layer having a hetero interface being formed with respect to the compound semiconductor layer CL1 is selected. Thereby, the two-dimensional electron gas layer TD1 serving as a channel region of the transistor HT1 is formed on the interface between the compound semiconductor layer CL1 and the compound semiconductor layer CL2. In the present embodiment, the compound semiconductor layer CL2 is, for example, an AlGa_{0.15}N layer, and particularly preferably an Al_{0.15}Ga_{0.85}N layer. The thickness of the compound semiconductor layer CL2 is, for example, 10 nm. <i>Nega</i> discloses the following at [0056] The transistor HT1 includes the gate electrode GE1 provided on the gate insulating film GI1. The gate electrode GE1 is formed at a position overlapping the gate recess GR1 when seen in a plan view. The gate electrode GE1 is, for example, a laminated structure in which Ni and Au are laminated in order.

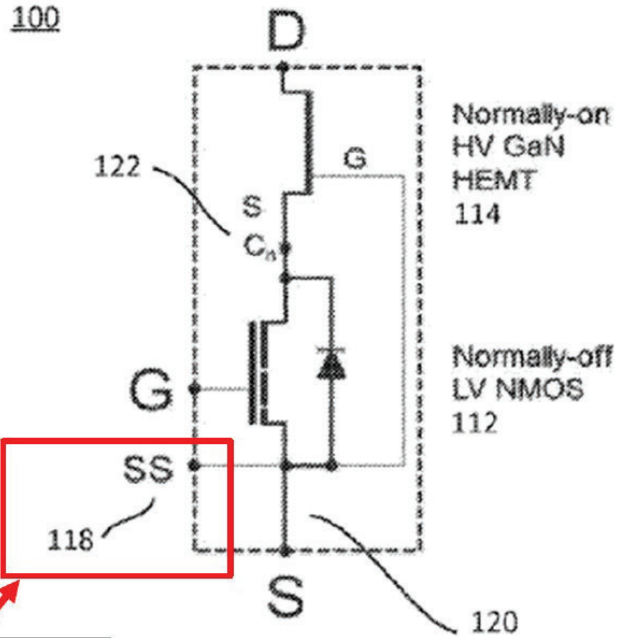
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	<i>Nega</i> discloses the following at [0058] The transistor HT1 includes the source electrode SE1 and the drain electrode DE1. The source electrode SE1 and the drain electrode DE1 is provided on the compound semiconductor layer CL2 so as to come into contact with the compound semiconductor layer CL2. In the present embodiment, the source electrode SE1 and the drain electrode DE1 are provided in the opening formed in the gate insulating film GI1, and thus the source electrode SE1 and the drain electrode DE1 come into contact with the compound semiconductor layer CL2. <i>Nega</i> discloses the following at Fig. 2 (annotated) FIG. 2  <i>Nega</i> discloses the following at Fig. 4 (annotated)

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4  The diagram shows a compound semiconductor transistor device (HD1) with a central die pad (BW1). To the left is a low-side switching device (LD1) and to the right is a high-side switching device (HD1). Both devices have a lead frame (LF1) and an outer lead (OL1). A source material (SM1) is indicated at the bottom right. A purple box highlights the die pad (BW1) with the text 'Compound semiconductor transistor device (HD1)'.
[1b] a die pad; and	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious a die pad. For example, <i>Nega</i> discloses the following at [0095] In the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1. In the transistor LT1 constituting the low-side switching device LD1, one of the source electrode

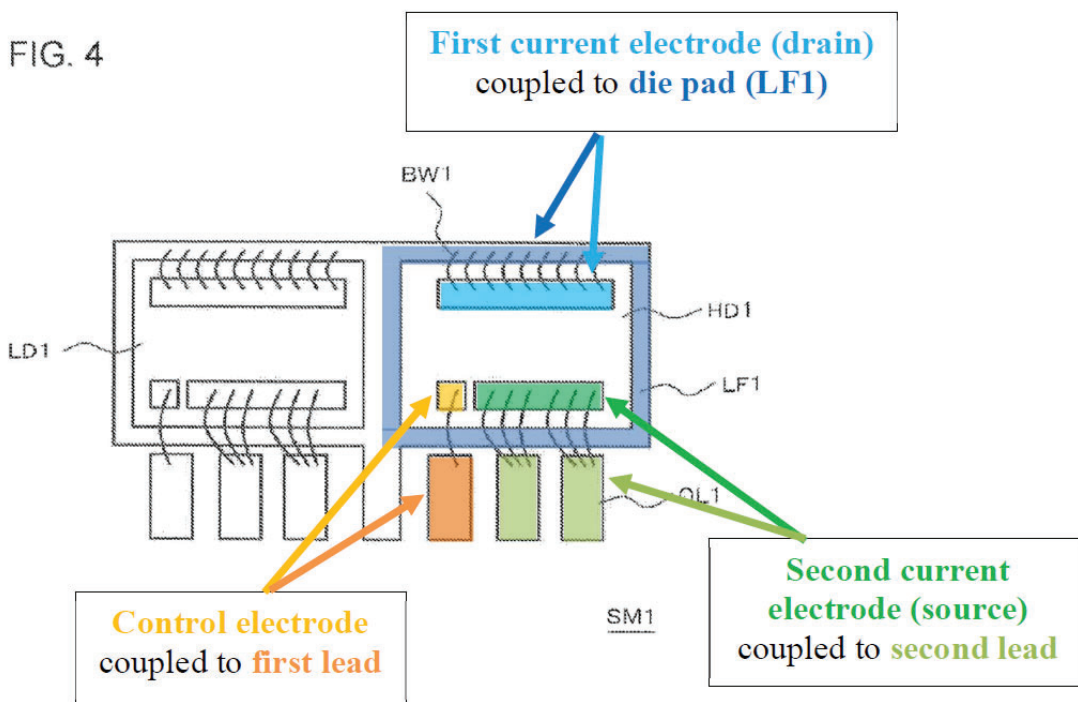
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[1c] a first lead, a second lead and a third lead,	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious a first lead, a second lead and a third lead. For example, <i>Nega</i> discloses the following at [0056] The transistor HT1 includes the gate electrode GE1 provided on the gate insulating film GI1. The gate electrode GE1 is formed at a position overlapping the gate recess GR1 when seen in a plan view. The gate electrode GE1 is, for example, a laminated structure in which Ni and Au are laminated in order. <i>Nega</i> discloses the following at [0057] The gate recess GR1 and the gate electrode GE1 are provided so as to be located between the source electrode SE1 and the drain electrode DE1. <i>Nega</i> discloses the following at [0058] The transistor HT1 includes the source electrode SE1 and the drain electrode DE1. The source electrode SE1 and the drain electrode DE1 is provided on the compound semiconductor layer CL2 so as to come into contact with the compound semiconductor layer CL2. In the present embodiment, the source electrode SE1 and the drain electrode DE1 are provided in the opening formed in the gate insulating film GI1, and thus the source electrode SE1 and the drain electrode DE1 come into contact with the compound semiconductor layer CL2. <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at [0095]

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	In the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1. In the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE2 is connected to the outer lead OL1. <i>Nega</i> discloses the following at Fig. 4 (annotated) FIG. 4  The diagram illustrates a power MOSFET package. It features a lead frame (LF1) with a die pad. A high-side switching device (HD1) is mounted on the die pad, with its drain electrode (DE1) connected to the die pad. A low-side switching device (LD1) is mounted on the lead frame, with its source electrode (SE2) connected to the lead frame. The gate electrodes (GE1, GE2) are connected to an outer lead (OL1). A bond wire (BW1) connects the drain of HD1 to the source of LD1. The package is mounted on a substrate (SM1). Annotations highlight: 1. 'First current electrode (drain) coupled to die pad (LF1)' pointing to the drain of HD1. 2. 'Control electrode coupled to first lead' pointing to the gate of LD1. 3. 'Second current electrode (source) coupled to second lead' pointing to the source of LD1.

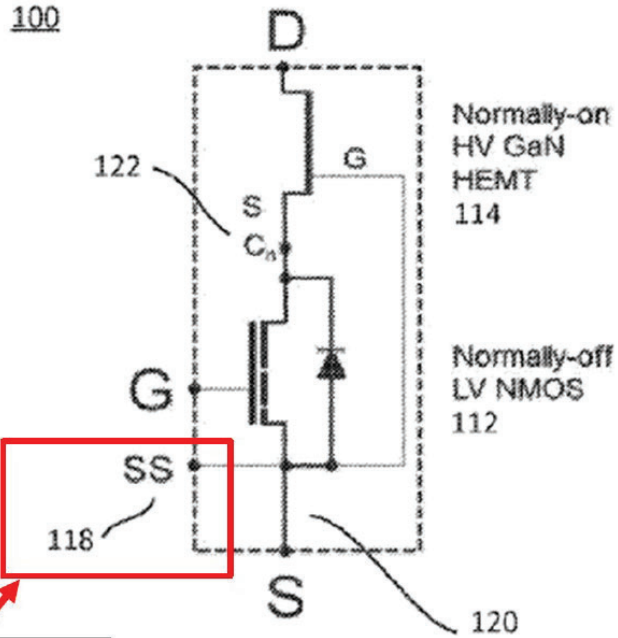
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Roberts discloses the following at [0055] A circuit 100 comprising a hybrid cascode arrangement of a normally-on depletion mode GaN FET power transistor 114 and a normally-off driver FET 112 is shown schematically in FIG. 1A. The equivalent circuit 102 is shown as a single high voltage transistor in FIG. 1B. In embodiments of the invention described herein, the power transistor comprises a high voltage (HV) normally-on, depletion mode, GaN FET, which may comprise a GaN HEMT (High electron mobility transistor) and the driver FET comprises a normally-off low voltage (LV) NMOS (N-channel) MOSFET. Roberts discloses the following at [0056] The arrangement shown in FIGS. 1A and 1B may be viewed as a very high power microwave integrated hybrid device. As mentioned above, the GaN power transistor may, for example, be required to provide less than 20 nS switching time and more than 30 A current switching capability. In conventional arrangements using a discrete, single N channel driver FET, such as shown in FIG. 1A, a “Kelvin Source Sense” or Kelvin connection SS is provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive $L \, di/dt$ noise generated by the high current fluctuations of the source connection S. Roberts discloses the following at [0057] Any significant series inductance at the MOSFET source (S) 120 or at the common node (Cn) 122 will provide unwanted $L \, di/dt$ transients. Such transients can potentially be as large as the threshold voltage of devices—typically plus 2 V for the MOSFET and minus 3 V for a GaN HEMT or minus 7 V for a GaN MISFET, which would result in unwanted switching. Additionally, series resistance in the source connection 120 results in debiasing which produces an apparent increase of the on-resistance. Thus, it is desirable to provide a driver circuit that provides monitoring and control of noise and transients. Preferably the driver circuit comprises a CMOS driver circuit and the driver MOSFET is integrated with the CMOS driver circuit.

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Roberts discloses the following at [0095] Thus systems according to the embodiments provide one or more of reduced series inductance and resistance; low thermal resistance; separate Kelvin connection(s); effective thermal management. Roberts discloses the following at Fig. 1A (annotated)  FIG. 1A

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[1d] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad. For example, <i>Nega</i> discloses the following at [0056] The transistor HT1 includes the gate electrode GE1 provided on the gate insulating film GI1. The gate electrode GE1 is formed at a position overlapping the gate recess GR1 when seen in a plan view. The gate electrode GE1 is, for example, a laminated structure in which Ni and Au are laminated in order. <i>Nega</i> discloses the following at [0057] The gate recess GR1 and the gate electrode GE1 are provided so as to be located between the source electrode SE1 and the drain electrode DE1. <i>Nega</i> discloses the following at [0058] The transistor HT1 includes the source electrode SE1 and the drain electrode DE1. The source electrode SE1 and the drain electrode DE1 is provided on the compound semiconductor layer CL2 so as to come into contact with the compound semiconductor layer CL2. In the present embodiment, the source electrode SE1 and the drain electrode DE1 are provided in the opening formed in the gate insulating film GI1, and thus the source electrode SE1 and the drain electrode DE1 come into contact with the compound semiconductor layer CL2. <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at [0095]

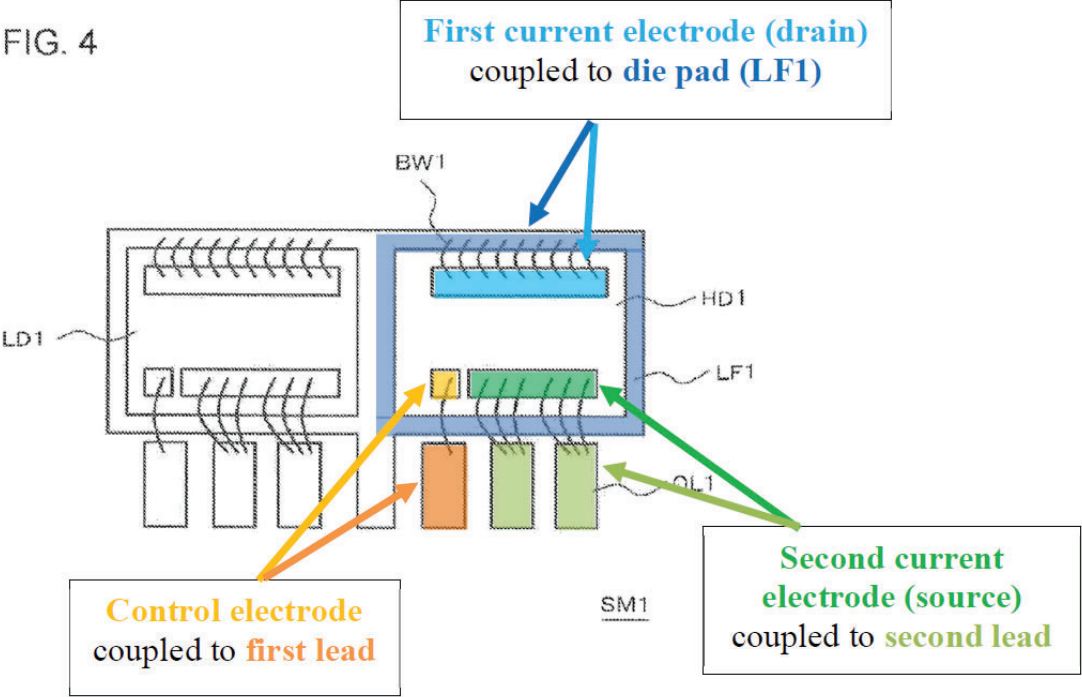
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	In the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1. In the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE2 is connected to the outer lead OL1. <i>Nega</i> discloses the following at Fig. 4 (annotated) FIG. 4  The diagram illustrates a power MOSFET package. It features a high-side switching device (HD1) and a low-side switching device (LD1). The high-side device (HD1) has a drain electrode (DE1) connected to a die pad (LF1) and a source electrode (SE1) connected to an outer lead (OL1). The low-side device (LD1) has a drain electrode (DE2) connected to a die pad (LF1) and a source electrode (SE2) connected to an outer lead (OL1). The gate electrodes (GE1, GE2) are connected to the outer lead (OL1). A bond wire (BW1) connects the die pad (LF1) to the outer lead (OL1). A control electrode (CE) is coupled to the first lead (LF1). A second current electrode (SE) is coupled to the second lead (OL1). The package is mounted on a substrate (SM1).

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Roberts discloses the following at [0055] A circuit 100 comprising a hybrid cascode arrangement of a normally-on depletion mode GaN FET power transistor 114 and a normally-off driver FET 112 is shown schematically in FIG. 1A. The equivalent circuit 102 is shown as a single high voltage transistor in FIG. 1B. In embodiments of the invention described herein, the power transistor comprises a high voltage (HV) normally-on, depletion mode, GaN FET, which may comprise a GaN HEMT (High electron mobility transistor) and the driver FET comprises a normally-off low voltage (LV) NMOS (N-channel) MOSFET. Roberts discloses the following at [0056] The arrangement shown in FIGS. 1A and 1B may be viewed as a very high power microwave integrated hybrid device. As mentioned above, the GaN power transistor may, for example, be required to provide less than 20 nS switching time and more than 30 A current switching capability. In conventional arrangements using a discrete, single N channel driver FET, such as shown in FIG. 1A, a “Kelvin Source Sense” or Kelvin connection SS is provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive $L \, di/dt$ noise generated by the high current fluctuations of the source connection S. Roberts discloses the following at [0057] Any significant series inductance at the MOSFET source (S) 120 or at the common node (Cn) 122 will provide unwanted $L \, di/dt$ transients. Such transients can potentially be as large as the threshold voltage of devices—typically plus 2 V for the MOSFET and minus 3 V for a GaN HEMT or minus 7 V for a GaN MISFET, which would result in unwanted switching. Additionally, series resistance in the source connection 120 results in debiasing which produces an apparent increase of the on-resistance. Thus, it is desirable to provide a driver circuit that provides monitoring and control of noise and transients. Preferably the driver circuit comprises a CMOS driver circuit and the driver MOSFET is integrated with the CMOS driver circuit.

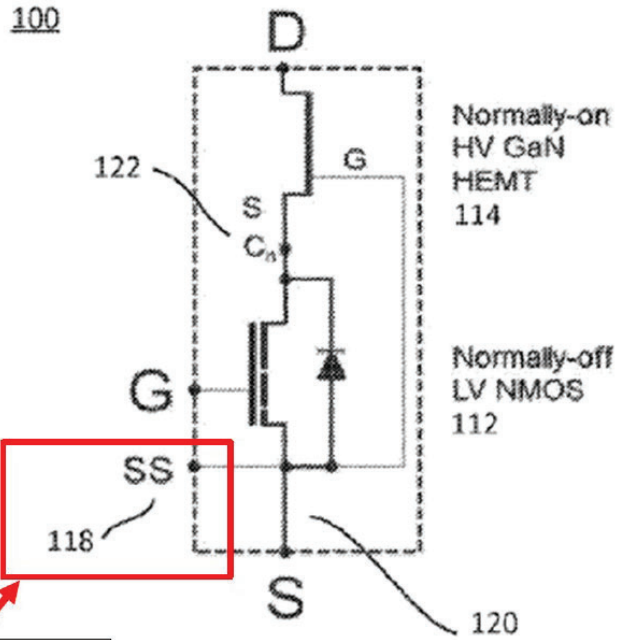
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Roberts discloses the following at [0095] Thus systems according to the embodiments provide one or more of reduced series inductance and resistance; low thermal resistance; separate Kelvin connection(s); effective thermal management. Roberts discloses the following at Fig. 1A (annotated)  FIG. 1A

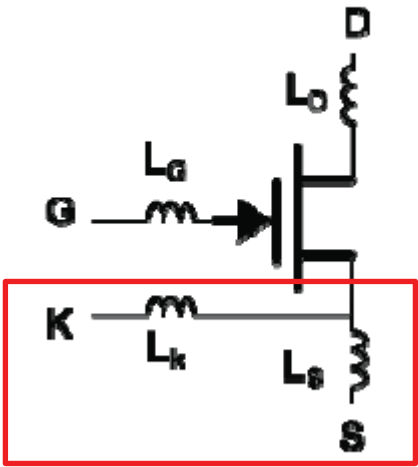
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[1e] wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality. For example, <i>Nega</i> discloses the following at [0056] The transistor HT1 includes the gate electrode GE1 provided on the gate insulating film GI1. The gate electrode GE1 is formed at a position overlapping the gate recess GR1 when seen in a plan view. The gate electrode GE1 is, for example, a laminated structure in which Ni and Au are laminated in order. <i>Nega</i> discloses the following at [0057] The gate recess GR1 and the gate electrode GE1 are provided so as to be located between the source electrode SE1 and the drain electrode DE1. <i>Nega</i> discloses the following at [0058] The transistor HT1 includes the source electrode SE1 and the drain electrode DE1. The source electrode SE1 and the drain electrode DE1 is provided on the compound semiconductor layer CL2 so as to come into contact with the compound semiconductor layer CL2. In the present embodiment, the source electrode SE1 and the drain electrode DE1 are provided in the opening formed in the gate insulating film GI1, and thus the source electrode SE1 and the drain electrode DE1 come into contact with the compound semiconductor layer CL2. <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1.

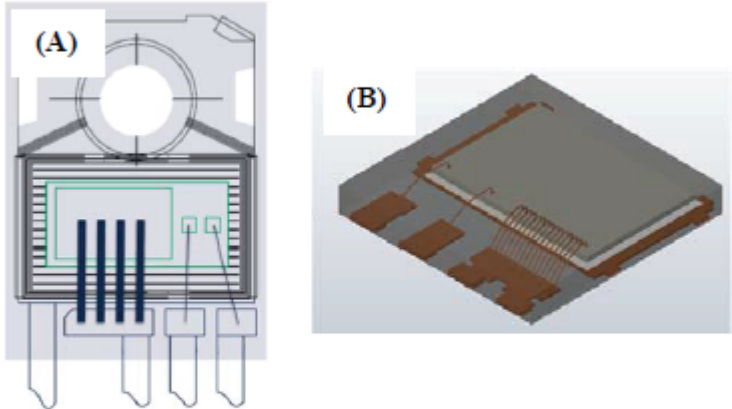
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	<i>Nega</i> discloses the following at [0095] In the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1. In the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE2 is connected to the outer lead OL1. <i>Nega</i> discloses the following at Fig. 4 (annotated)

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4  Roberts discloses the following at [0055] A circuit 100 comprising a hybrid cascode arrangement of a normally-on depletion mode GaN FET power transistor 114 and a normally-off driver FET 112 is shown schematically in FIG. 1A. The equivalent circuit 102 is shown as a single high voltage transistor in FIG. 1B. In embodiments of the invention described herein, the power transistor comprises a high voltage (HV) normally-on, depletion mode, GaN FET, which may comprise a GaN HEMT (High electron mobility transistor) and the driver FET comprises a normally-off low voltage (LV) NMOS (N-channel) MOSFET.

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Roberts discloses the following at [0056] The arrangement shown in FIGS. 1A and 1B may be viewed as a very high power microwave integrated hybrid device. As mentioned above, the GaN power transistor may, for example, be required to provide less than 20 nS switching time and more than 30 A current switching capability. In conventional arrangements using a discrete, single N channel driver FET, such as shown in FIG. 1A, a “Kelvin Source Sense” or Kelvin connection SS is provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive L di/dt noise generated by the high current fluctuations of the source connection S. Roberts discloses the following at [0057] Any significant series inductance at the MOSFET source (S) 120 or at the common node (Cn) 122 will provide unwanted L di/dt transients. Such transients can potentially be as large as the threshold voltage of devices—typically plus 2 V for the MOSFET and minus 3 V for a GaN HEMT or minus 7 V for a GaN MISFET, which would result in unwanted switching. Additionally, series resistance in the source connection 120 results in debiasing which produces an apparent increase of the on-resistance. Thus, it is desirable to provide a driver circuit that provides monitoring and control of noise and transients. Preferably the driver circuit comprises a CMOS driver circuit and the driver MOSFET is integrated with the CMOS driver circuit. Roberts discloses the following at [0095] Thus systems according to the embodiments provide one or more of reduced series inductance and resistance; low thermal resistance; separate Kelvin connection(s); effective thermal management. Roberts discloses the following at Fig. 1A (annotated)

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	 FIG. 1A Huang discloses the following at 2, Fig. 2 (annotated):

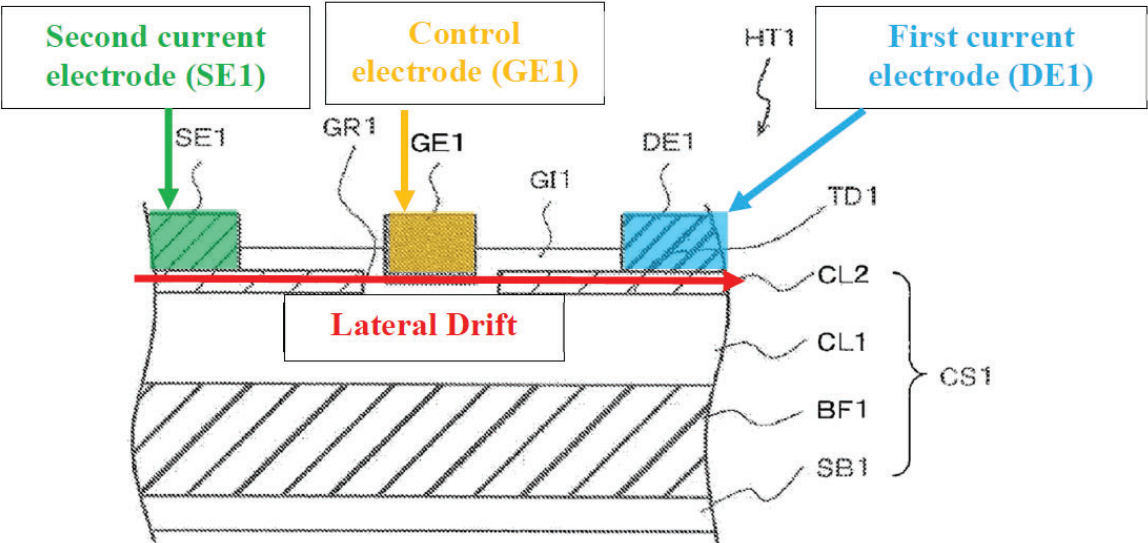
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	DFN 8x8  Lind discloses the following at 3

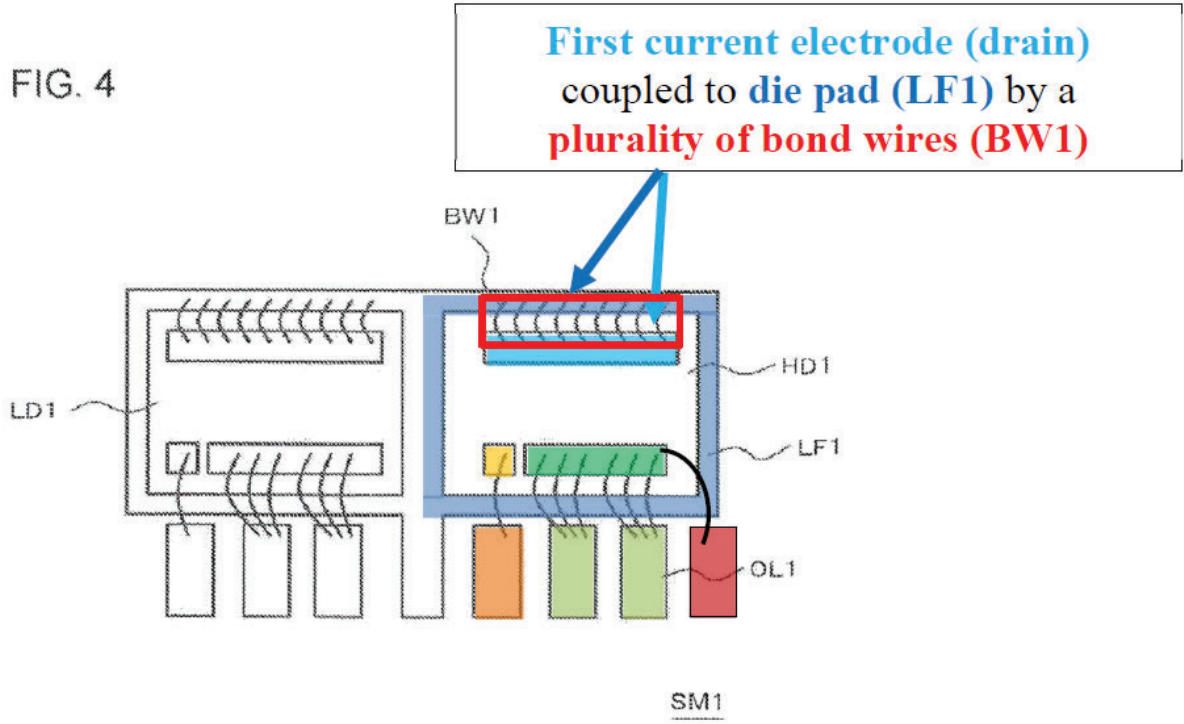
Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	III. Source-Sense concept and A/B simulation A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.  Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections The principle is to provide a separate path for the drain-source current, such that voltage generated across the source inductance no longer appears in the KVL mesh of the gate current loop. McKnight discloses the following at 12:20-27: For example, the packaging assemblies of the embodiments described herein may be adapted for GaN dies comprising lateral GaN devices with alternative layouts. Pack ages with other external contact arrangements, e.g. comprising single or multiple external pads for each of the Source, drain and gate connections may be provided. Option ally, the package includes an additional external contact pad, e.g. a source sense (Kelvin) connection.

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Otremba528 discloses the following at [0002]: Chip contact regions, such as source and/or drain contacts are each normally supplied with voltage through connecting elements, such as electrically conductive wires, electrically conductive leads or clips. Furthermore, a source-sensing lead may be connected to a source contact to measure and/or monitor the potential of the source contact. Source-sensing leads may be connected to the source contact through additional redistribution elements, such as through an electrically conductive wire. The electrically conductive wire may be connected to a source contact, e.g. by wire bonding. These multiple contacting mechanisms may lead to additional packaging costs, which in particular may be attributed to the need for extra source-sensing leads. Otremba528 discloses the following at Fig 4 (annotated):

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG 4
[1f] wherein the compound semiconductor transistor device is a lateral transistor device and a drain	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad. For example,

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
or a source of the compound semiconductor transistor device is coupled to the die pad,	<i>Nega</i> discloses that the compound semiconductor transistor device is a lateral transistor because the device is arranged laterally with the electrodes on the same lateral plane in a lateral drift path with the current generally flowing parallel to the surface. The '481 patent explains that “lateral” means “run[ning] generally parallel to the lateral extent of a semiconductor material or semiconductor carrier” ('481 patent, 3:14-18) and describes a device that “has a lateral drift path” ('481 patent, 4:37-38). Smart Power ICs (Innoscience 1414-00012740 – Innoscience 1414-00012823) defines a horizontal (i.e. lateral) transistor as a structure where “current enters and leaves the chip through the upper surface of the chip.” At 7. <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at Fig. 2

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 2 
[1g] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip. For example, <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at Fig. 4 (annotated and modified)

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4  First current electrode (drain) coupled to die pad (LF1) by a plurality of bond wires (BW1) <i>Nega</i> discloses the following at Fig. 4 (annotated)

Claim 1	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4 First current electrode (drain) coupled to die pad (LF1) by a plurality of bond wires (BW1) Labels in diagram: LD1, BW1, HD1, LF1, OL1, SM1

Claim 2	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[2p] The electronic component of claim 1,	<i>Nega</i> alone or in combination with one or more references discloses the electronic component according to claim 1. <i>See supra</i> claim 1.
[2a] wherein the compound semiconductor transistor device is one of a SiC transistor device, a	<i>Nega</i> alone or in combination with one or more references discloses wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device. For example,

Claim 2	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
III-V compound semiconductor transistor device and a Group III-nitride transistor device.	<i>Nega</i> discloses the following at [0049] The compound semiconductor layer CL1 is provided on the buffer layer BF1. The compound semiconductor layer CL1 is, for example, a GaN layer. The thickness of the compound semiconductor layer CL1 is, for example, 1 μm. <i>Nega</i> discloses the following at [0050] The compound semiconductor layer CL2 is provided on the compound semiconductor layer CL1. As the compound semiconductor layer CL2, a layer having a hetero interface being formed with respect to the compound semiconductor layer CL1 is selected. Thereby, the two-dimensional electron gas layer TD1 serving as a channel region of the transistor HT1 is formed on the interface between the compound semiconductor layer CL1 and the compound semiconductor layer CL2. In the present embodiment, the compound semiconductor layer CL2 is, for example, an AlGa_N layer, and particularly preferably an Al_{0.15}Ga_{0.85}N layer. The thickness of the compound semiconductor layer CL2 is, for example, 10 nm. <i>Nega</i> discloses the following at Fig. 2 (annotated)

Claim 2	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 2 Group III-N Compound Semiconductor (GaN)

Claim 3	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[3p] The electronic component of claim 1,	<i>Nega</i> alone or in combination with one or more references discloses the electronic component according to claim 1. <i>See supra</i> claim 1.
[3a] wherein the compound semiconductor	<i>Nega</i> alone or in combination with one or more references discloses or renders obvious wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

Claim 3	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.	For example, Roberts discloses the following at [0006] GaN power transistors for power conversion circuits for high voltage (HV) applications, e.g. 600/650V, are typically normally-on (depletion mode) transistors. These transistors are usually driven by a series connected, discrete, power MOSFET device, i.e. in a cascode configuration, to provide normally-off operation (see FIG. 1). Conventionally, the hybrid cascode arrangement is provided with a separate, high power, high speed driver circuit, having a separate isolated power supply. Roberts discloses the following at [0008] The GaN transistor may be required, for example, to provide <20 ns switching time and more than 30 A current switching capability. Any significant series inductance at the MOSFET source or at the common node will provide unwanted L di/dt transients which can be as large as the threshold voltage of the devices, thus causing unwanted switching. It will be appreciated that in operation of an electronic power switching system that is capable of switching, for example, 30 Amps at 1000V, i.e. 30,000 Watts, safe operation may be compromised by any unwanted switching caused by transients or noise that exceeds the threshold voltage of the device. Roberts discloses the following at [0012] GaN transistors that can switch, for example, 24 A (1200 V) and 47 A (650 V) may have die sizes as small as 2×2 mm. Calculations show these die, when packaged, can have a thermal resistance of greater than 2° C./W. For example, it is estimated that, for an on-resistance of 80 mΩ, the ohmic power dissipation would be 32 Watts if the device were required to sink 20 Amps. The thermal resistance in total for the combination of the device, package and heat sink could exceed 5° C./W, so that the temperature increase from the GaN device dissipation alone could exceed 150° C. The additional heat dissipation of the MOSFET, assuming a 20 mΩ device is used, would be 8 Watts. With the total structure dissipating 40 Watts, the temperature within the package could exceed the safe operating limits of the MOSFET, typically 175° C., if there is insufficient heat dissipation.

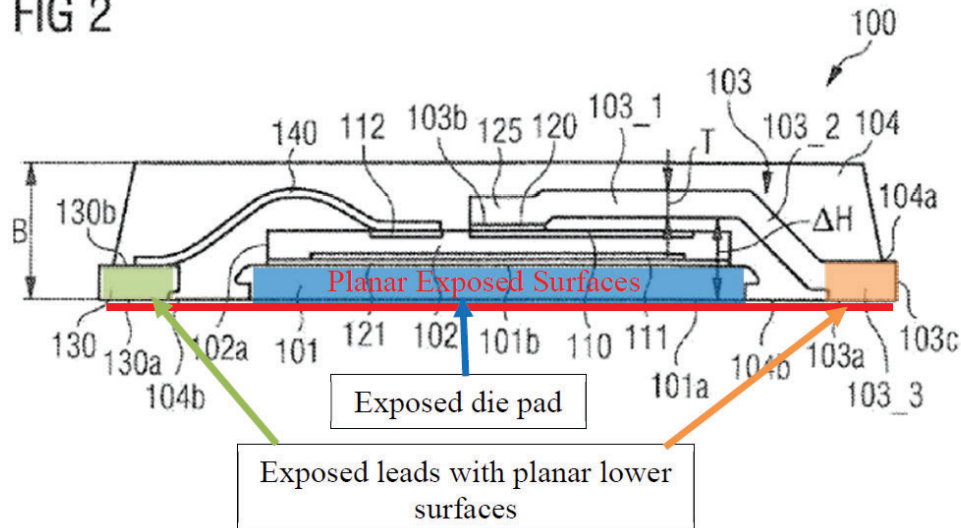
Claim 4	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[4p] The electronic component of claim 1,	<i>Nega</i> alone or in combination with one or more references discloses the electronic component according to claim 1. <i>See supra</i> claim 1.
[4a] further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.	<i>Nega</i> alone or in combination with one or more references discloses or renders obvious comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces. Otremba433 discloses the following at [0027] FIG. 1 illustrates a top view of an exemplary semiconductor device 100 in accordance with one embodiment. The semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104. FIG. 2 schematically illustrates a cross-sectional view of the semiconductor device 100 shown in FIG. 1 along section line A-A. Otremba433 discloses the following at [0037] The encapsulation body 104 of the semiconductor device 100 may embed the carrier 101 and the semiconductor chip 102 at side and top faces. The terminal portion 103_3 of the contact clip 103 forms an external terminal of the semiconductor device 100 and, therefore, protrudes out of the encapsulation body 104. By way of example, as illustrated in FIGS. 1 and 2, the semiconductor device may have a leadless package. In this and other cases the terminal portion 103_3 of the contact clip 103 may have an external contact area 103 a exposed at the encapsulation body 104, e.g., at the bottom of the package. The external contact area 103 a may be coplanar with a reference plane defined by a bottom surface 101 a of the carrier 101. The bottom surface 101 a of the carrier 101 may also be exposed at the bottom of the package. Further, a bottom surface portion 104 b of the encapsulation body 104 may be coplanar with the reference plane defined by the bottom surface 101 a of the carrier 101. In this case, the bottom surface 101 a of the carrier, the bottom surface portion 104 b of the encapsulation body 104 and the external contact area 103 a of the terminal portion 103 may all be arranged substantially level with each other. They may form the bottom of the package.

Claim 4	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Otremba433 discloses the following at [0039] The lead post 130 may form another external terminal of the semiconductor device 100. A bottom surface 130 a of the lead post 130 may be exposed at the bottom surface of the package of the semiconductor device 100 in order to e.g., provide for another SMT external contact area of the package. Otremba433 discloses the following at [0025] A contact clip is provided to electrically connect an electrode of the semiconductor chip to an external terminal of the semiconductor device. The contact clip may be an integral part having a bond portion bonded to the first electrode and having a terminal portion forming an external terminal of the semiconductor device. By way of example, the external terminal of the semiconductor device may comprise an external contact area exposed at the encapsulation body of a leadless package. The external terminal of the semiconductor device may also be a lead of a leaded package. Otremba433 discloses the following at Fig. 2 (annotated)

Claim 4

Exemplary Disclosure based on *Nega* and Related Combinations

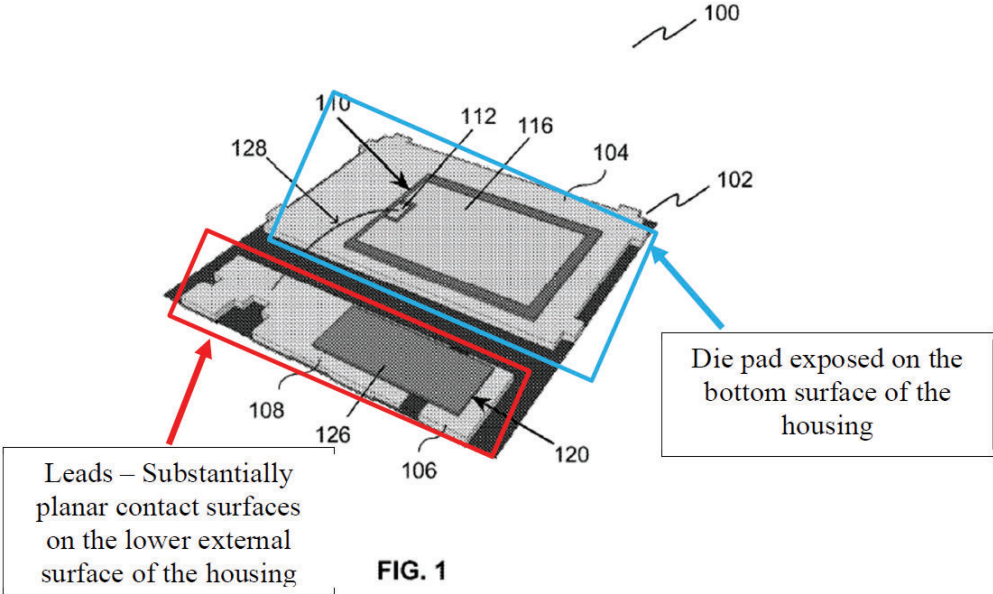
FIG 2



Otremba280 discloses the following at 4:1-29

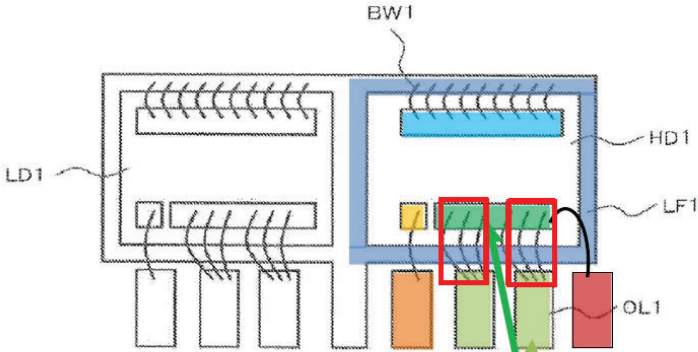
The electronic component 10 comprises two semiconductor devices 11, 12 whose first load electrodes 17 (sources) are electrically connected to one another and to a lead 23 of the leadframe 13 by a single electrically conductive element in the form of a contact clip 14. The contact clip 14 may be provided in the form of a metal strip having the lateral size and shape and vertical form adapted to extend between the first load electrodes 17 of two semiconductor devices 11, 12 and the upper surface 35 of a lead 23 of a leadframe 13. In this embodiment, the leadframe 13 is positioned within the electronic component at a level below the first side of the semiconductor devices 11, 12. The upper surface of the lead 23 may lie generally coplanar with the second side 16 of the semiconductor devices 11, 12. The contact clip 14 may have a general form and height adapted to accommodate the thickness of the semiconductor devices 11, 12. Typically, the device carrier portion 19 and the leads 20 of the leadframe 13 are stamped or etched from a metal sheet so that the upper side 35 of the device carrier

Claim 4	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	portion 19 and the upper side 35 of the leads 20 are generally coplanar with one another. The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a Surface mountable or leadless type electronic component. Alternatively, the outer portions of the leads may be bent in a general direction away from the first side of the two semiconductor devices to provide pins by which the electronic component 10 may be mounted on a redistribution board such as a printed circuit board. Otremba124 discloses the following at [0041] In an example, the power transistor arrangement 100 with a flipped SFET and a wire bonded GaN HEMT may be packaged in a 8x8 ThinPAK, wherein the GaN HEMT 110 may be a high voltage (e.g. larger than 200V) HEMT switch and the SFET 120 may be a low voltage (e.g. smaller than 200V) power MOSFET. The GaN HEMT 110 is a normally on device, and is transformed to a normally off transistor with introducing of the low-voltage SFET 120. Such a GaN-SFET arrangement 100 may correspond to the cascade circuit 500 of FIG. 5. Otremba124 discloses the following at Fig. 1 (annotated)

Claim 4	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	 FIG. 1

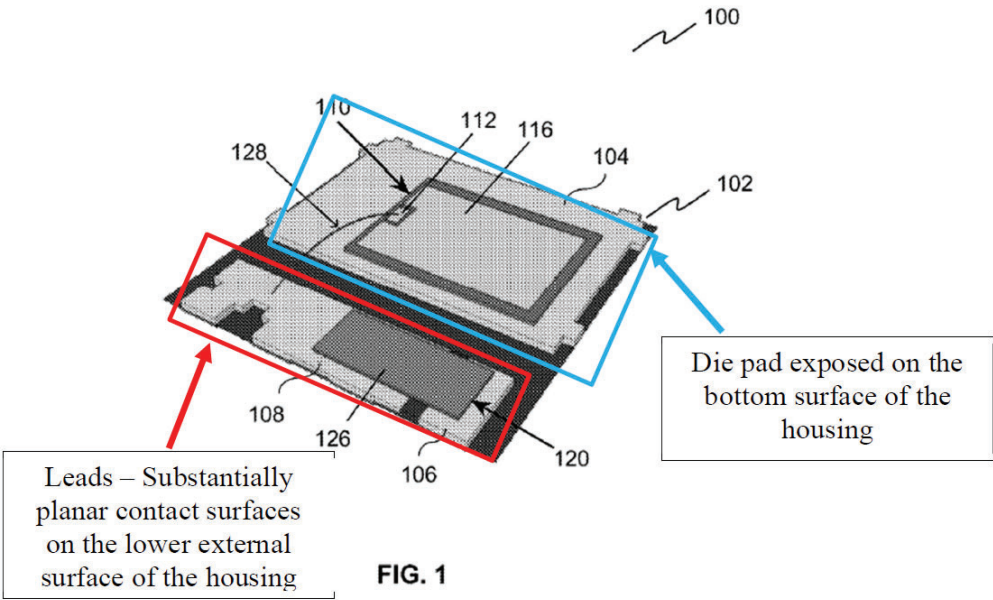
Claim 6	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[6p] The electronic component of claim 1,	<i>Nega</i> alone or in combination with one or more references discloses the electronic component according to claim 1. <i>See supra</i> claim 1.
[6a] wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.	<i>Nega</i> alone or in combination with one or more references discloses or renders obvious wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip. For example, <i>Nega</i> discloses the following at [0094]

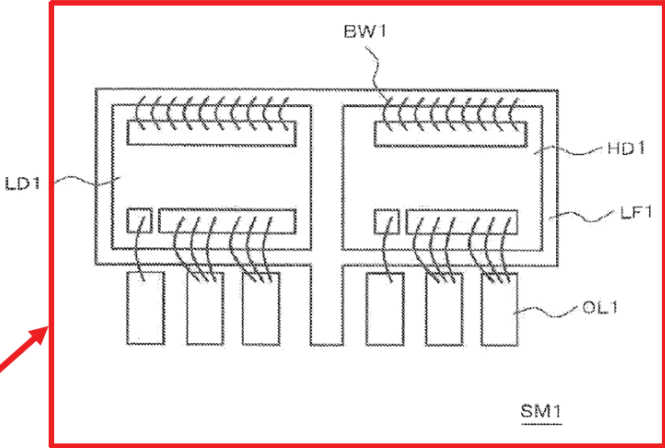
Claim 6	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at [0095] In the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1. In the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE2 is connected to the outer lead OL1. <i>Nega</i> discloses the following at Fig. 4 (annotated and modified)

Claim 6	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4  Second current electrode (source) coupled to second lead by a plurality of bond wires (BW1) <i>Nega</i> discloses the following at Fig. 4 (annotated)

Claim 6	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4 Second current electrode (source) coupled to second lead by a plurality of bond wires (BW1)

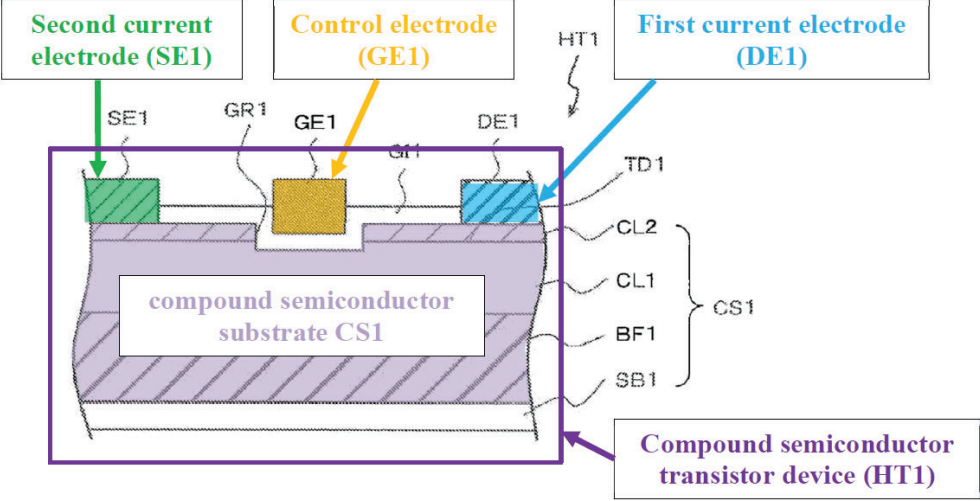
Claim 9	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[9p] The electronic component of claim 1,	<i>Nega</i> alone or in combination with one or more references discloses the electronic component according to claim 1. <i>See supra</i> claim 1.
[9a] wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8×8 package outline.	<i>Nega</i> alone or in combination with other references discloses or renders obvious wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8×8 package outline. Otremba124 discloses the following at [0041] In an example, the power transistor arrangement 100 with a flipped SFET and a wire bonded GaN HEMT may be packaged in a 8x8 ThinPAK, wherein the GaN HEMT 110 may be a high voltage (e.g. larger than 200V) HEMT switch and the SFET 120 may be a low voltage (e.g. smaller than 200V)

Claim 9	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	power MOSFET. The GaN HEMT 110 is a normally on device, and is transformed to a normally off transistor with introducing of the low-voltage SFET 120. Such a GaN-SFET arrangement 100 may correspond to the cascade circuit 500 of FIG. 5. Otremba124 discloses the following at Fig. 1 (annotated)  FIG. 1 Leads – Substantially planar contact surfaces on the lower external surface of the housing Die pad exposed on the bottom surface of the housing
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[17p] An electronic component, comprising:	To the extent the preamble is limiting, <i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious an electronic component. <i>See supra</i> claim 1. For example,

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	<i>Nega</i> discloses the following at [0018] FIG. 4 is a plan view illustrating an example of the semiconductor device according to the first embodiment. <i>Nega</i> discloses the following at [0090] FIG. 4 is a plan view illustrating an example of the semiconductor device SM1 according to the present embodiment. <i>Nega</i> discloses the following at Fig. 4 (annotated) FIG. 4  Electronic component (SM1)

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
[17a] a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and	<i>Nega</i> alone or in combination with one or more references discloses and/or renders obvious a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality. <i>See supra</i> claims 1-3. For example, <i>Nega</i> discloses the following at [0034] According to such a configuration, the transistor HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1, thereby allowing a switching device having a lower loss than a silicon device to be realized. For this reason, it is possible to achieve an improvement in the power source efficiency of the DC/DC converter circuit. In addition, the transistor HT1 connected to the input terminal is configured to be a normally-off type, thereby allowing flow of a through-current into a circuit in a state where power is not completely supplied to the DC/DC converter circuit to be suppressed, without newly providing a protection circuit. Therefore, it is possible to suppress complication of a circuit. <i>Nega</i> discloses the following at [0046] As shown in FIG. 2, the transistor HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1. In addition, the transistor HT1 is a normally-off type transistor. <i>Nega</i> discloses the following at [0049] The compound semiconductor layer CL1 is provided on the buffer layer BF1. The compound semiconductor layer CL1 is, for example, a GaN layer. The thickness of the compound semiconductor layer CL1 is, for example, 1 μm.

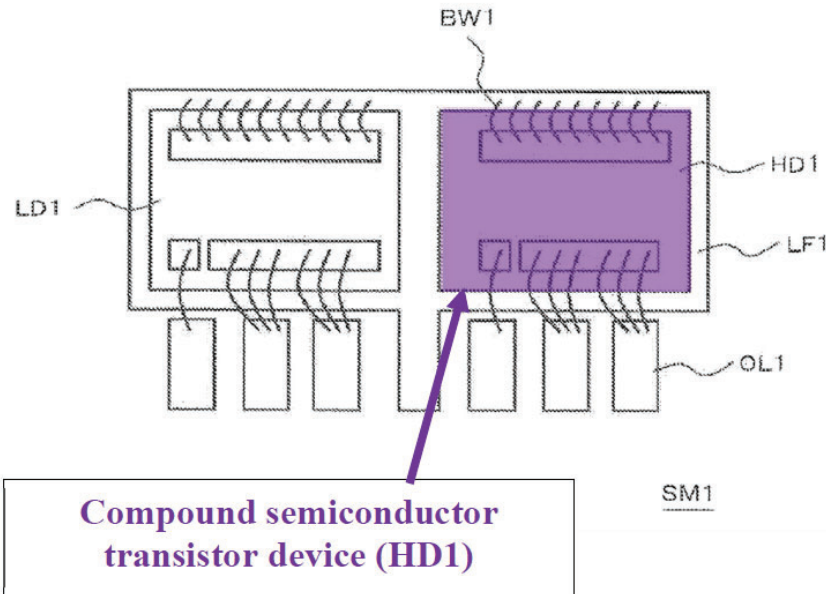
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	<i>Nega</i> discloses the following at [0050] The compound semiconductor layer CL2 is provided on the compound semiconductor layer CL1. As the compound semiconductor layer CL2, a layer having a hetero interface being formed with respect to the compound semiconductor layer CL1 is selected. Thereby, the two-dimensional electron gas layer TD1 serving as a channel region of the transistor HT1 is formed on the interface between the compound semiconductor layer CL1 and the compound semiconductor layer CL2. In the present embodiment, the compound semiconductor layer CL2 is, for example, an AlGa_N layer, and particularly preferably an Al_{0.15}Ga_{0.85}N layer. The thickness of the compound semiconductor layer CL2 is, for example, 10 nm. <i>Nega</i> discloses the following at [0056] The transistor HT1 includes the gate electrode GE1 provided on the gate insulating film GI1. The gate electrode GE1 is formed at a position overlapping the gate recess GR1 when seen in a plan view. The gate electrode GE1 is, for example, a laminated structure in which Ni and Au are laminated in order. <i>Nega</i> discloses the following at [0058] The transistor HT1 includes the source electrode SE1 and the drain electrode DE1. The source electrode SE1 and the drain electrode DE1 is provided on the compound semiconductor layer CL2 so as to come into contact with the compound semiconductor layer CL2. In the present embodiment, the source electrode SE1 and the drain electrode DE1 are provided in the opening formed in the gate insulating film GI1, and thus the source electrode SE1 and the drain electrode DE1 come into contact with the compound semiconductor layer CL2. <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at Fig. 2 (annotated)

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 2  <i>Nega</i> discloses the following at Fig. 4 (annotated)

Claim 17

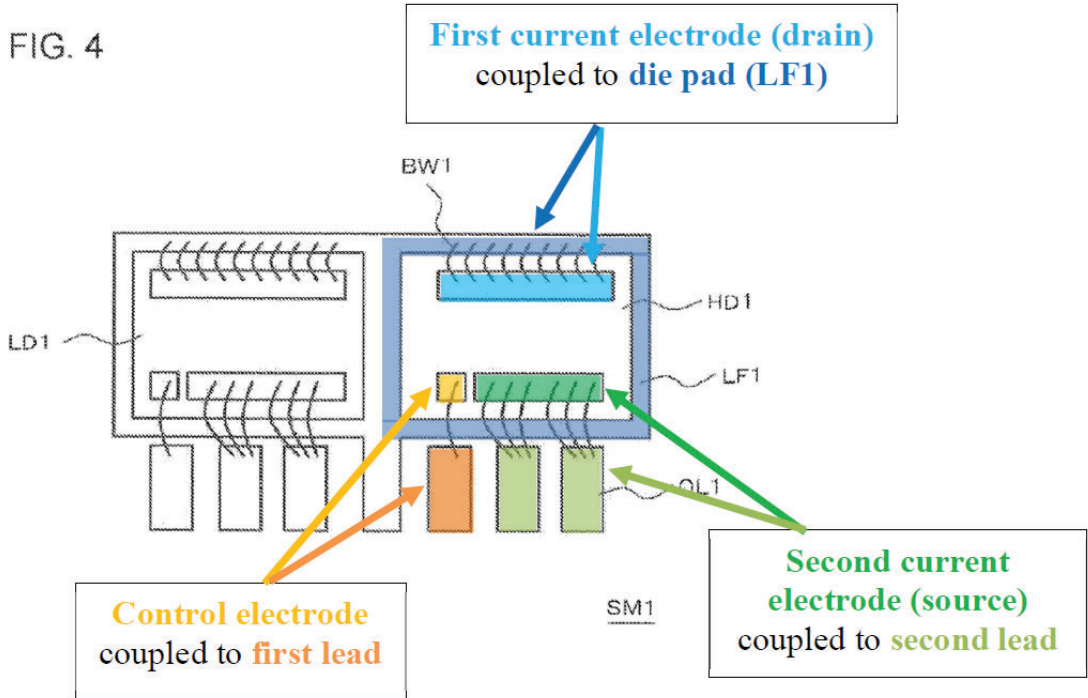
Exemplary Disclosure based on *Nega* and Related Combinations

FIG. 4



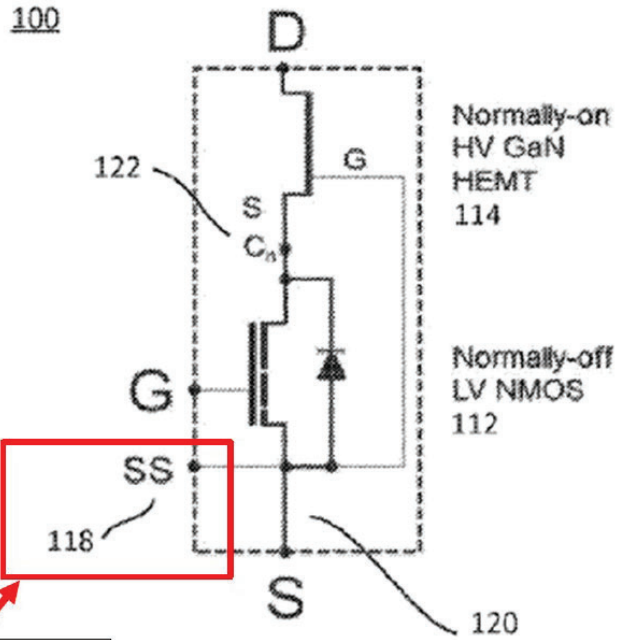
Nega discloses the following at [0095]

In the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1. In the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE2 is connected to the outer lead OL1.

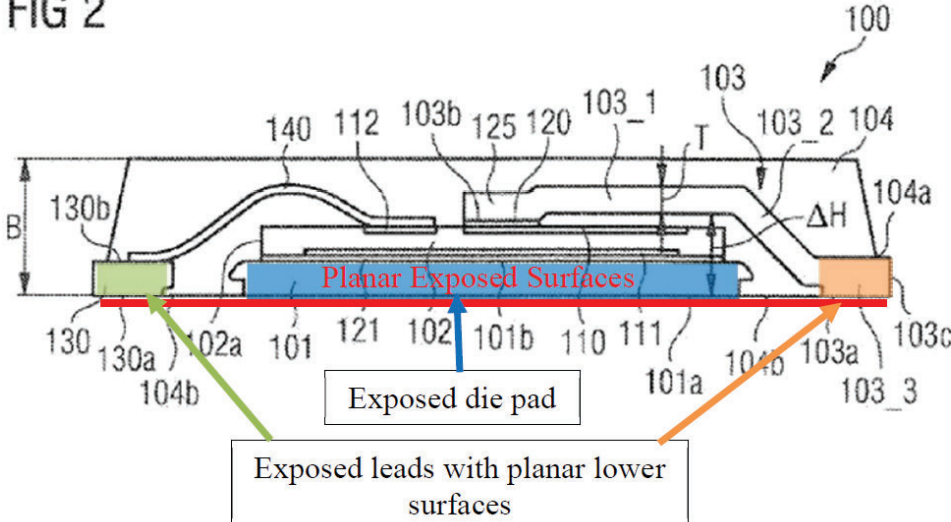
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	<i>Nega</i> discloses the following at Fig. 4 (annotated) FIG. 4  The diagram shows a cross-sectional view of a GaN power transistor. It includes a substrate (SM1) with a buffer layer (BL1). A gate stack (GW1) is formed on the substrate. A drain electrode (blue) is coupled to a die pad (LF1). A source electrode (green) is coupled to a second lead. A control electrode (orange) is coupled to a first lead. The structure also includes a drain region (LD1) and a drain contact (HD1). First current electrode (drain) coupled to die pad (LF1) Control electrode coupled to first lead Second current electrode (source) coupled to second lead Roberts discloses the following at [0006] GaN power transistors for power conversion circuits for high voltage (HV) applications, e.g. 600/650V, are typically normally-on (depletion mode) transistors. These transistors are usually driven by a series connected, discrete, power MOSFET device, i.e. in a cascode configuration, to provide normally-off operation (see FIG. 1). Conventionally, the hybrid cascode arrangement is provided with a separate, high power, high speed driver circuit, having a separate isolated power supply.

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Roberts discloses the following at [0008] The GaN transistor may be required, for example, to provide <20 ns switching time and more than 30 A current switching capability. Any significant series inductance at the MOSFET source or at the common node will provide unwanted $L di/dt$ transients which can be as large as the threshold voltage of the devices, thus causing unwanted switching. It will be appreciated that in operation of an electronic power switching system that is capable of switching, for example, 30 Amps at 1000V, i.e. 30,000 Watts, safe operation may be compromised by any unwanted switching caused by transients or noise that exceeds the threshold voltage of the device. Roberts discloses the following at [0012] GaN transistors that can switch, for example, 24 A (1200 V) and 47 A (650 V) may have die sizes as small as 2×2 mm Calculations show these die, when packaged, can have a thermal resistance of greater than 2° C./W. For example, it is estimated that, for an on-resistance of 80 mΩ, the ohmic power dissipation would be 32 Watts if the device were required to sink 20 Amps The thermal resistance in total for the combination of the device, package and heat sink could exceed 5° C./W, so that the temperature increase from the GaN device dissipation alone could exceed 150° C. The additional heat dissipation of the MOSFET, assuming a 20 mΩ device is used, would be 8 Watts. With the total structure dissipating 40 Watts, the temperature within the package could exceed the safe operating limits of the MOSFET, typically 175° C., if there is insufficient heat dissipation Roberts discloses the following at [0055] A circuit 100 comprising a hybrid cascode arrangement of a normally-on depletion mode GaN FET power transistor 114 and a normally-off driver FET 112 is shown schematically in FIG. 1A. The equivalent circuit 102 is shown as a single high voltage transistor in FIG. 1B. In embodiments of the invention described herein, the power transistor comprises a high voltage (HV) normally-on, depletion mode, GaN FET, which may comprise a GaN HEMT (High electron mobility transistor) and the driver FET comprises a normally-off low voltage (LV) NMOS (N-channel) MOSFET. Roberts discloses the following at [0056]

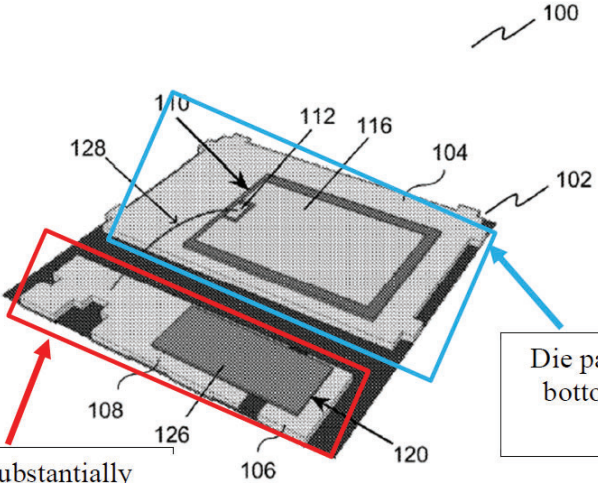
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	The arrangement shown in FIGS. 1A and 1B may be viewed as a very high power microwave integrated hybrid device. As mentioned above, the GaN power transistor may, for example, be required to provide less than 20 nS switching time and more than 30 A current switching capability. In conventional arrangements using a discrete, single N channel driver FET, such as shown in FIG. 1A, a “Kelvin Source Sense” or Kelvin connection SS is provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive L di/dt noise generated by the high current fluctuations of the source connection S. Roberts discloses the following at [0057] Any significant series inductance at the MOSFET source (S) 120 or at the common node (Cn) 122 will provide unwanted L di/dt transients. Such transients can potentially be as large as the threshold voltage of devices—typically plus 2 V for the MOSFET and minus 3 V for a GaN HEMT or minus 7 V for a GaN MISFET, which would result in unwanted switching. Additionally, series resistance in the source connection 120 results in debiasing which produces an apparent increase of the on-resistance. Thus, it is desirable to provide a driver circuit that provides monitoring and control of noise and transients. Preferably the driver circuit comprises a CMOS driver circuit and the driver MOSFET is integrated with the CMOS driver circuit. Roberts discloses the following at [0095] Thus systems according to the embodiments provide one or more of reduced series inductance and resistance; low thermal resistance; separate Kelvin connection(s); effective thermal management. Roberts discloses the following at Fig. 1A (annotated)

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	 FIG. 1A
[17b] a housing,	<i>Nega</i> alone or in combination with one or more references discloses or renders obvious a housing. <i>See supra</i> claim 4. For example, Otremba433 discloses the following at [0027]

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 1 illustrates a top view of an exemplary semiconductor device 100 in accordance with one embodiment. The semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104. FIG. 2 schematically illustrates a cross-sectional view of the semiconductor device 100 shown in FIG. 1 along section line A-A. Otremba433 discloses the following at [0037] The encapsulation body 104 of the semiconductor device 100 may embed the carrier 101 and the semiconductor chip 102 at side and top faces. The terminal portion 103_3 of the contact clip 103 forms an external terminal of the semiconductor device 100 and, therefore, protrudes out of the encapsulation body 104. By way of example, as illustrated in FIGS. 1 and 2, the semiconductor device may have a leadless package. In this and other cases the terminal portion 103_3 of the contact clip 103 may have an external contact area 103 a exposed at the encapsulation body 104, e.g., at the bottom of the package. The external contact area 103 a may be coplanar with a reference plane defined by a bottom surface 101 a of the carrier 101. The bottom surface 101 a of the carrier 101 may also be exposed at the bottom of the package. Further, a bottom surface portion 104 b of the encapsulation body 104 may be coplanar with the reference plane defined by the bottom surface 101 a of the carrier 101. In this case, the bottom surface 101 a of the carrier, the bottom surface portion 104 b of the encapsulation body 104 and the external contact area 103 a of the terminal portion 103 may all be arranged substantially level with each other. They may form the bottom of the package. Otremba433 discloses the following at [0039] The lead post 130 may form another external terminal of the semiconductor device 100. A bottom surface 130 a of the lead post 130 may be exposed at the bottom surface of the package of the semiconductor device 100 in order to e.g., provide for another SMT external contact area of the package. Otremba433 discloses the following at [0025]

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	A contact clip is provided to electrically connect an electrode of the semiconductor chip to an external terminal of the semiconductor device. The contact clip may be an integral part having a bond portion bonded to the first electrode and having a terminal portion forming an external terminal of the semiconductor device. By way of example, the external terminal of the semiconductor device may comprise an external contact area exposed at the encapsulation body of a leadless package. The external terminal of the semiconductor device may also be a lead of a leaded package. Otremba433 discloses the following at Fig. 2 (annotated) FIG 2  Otremba280 discloses the following at 4:1-29 The electronic component 10 comprises two semiconductor devices 11, 12 whose first load electrodes 17 (sources) are electrically connected to one another and to a lead 23 of the leadframe 13 by a single electrically conductive element in the form of a contact clip 14. The contact clip 14 may be provided in the form of a metal strip having the lateral size and shape and vertical form adapted to extend

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	between the first load electrodes 17 of two semiconductor devices 11, 12 and the upper surface 35 of a lead 23 of a leadframe 13. In this embodiment, the leadframe 13 is positioned within the electronic component at a level below the first side of the semiconductor devices 11, 12. The upper surface of the lead 23 may lie generally coplanar with the second side 16 of the semiconductor devices 11, 12. The contact clip 14 may have a general form and height adapted to accommodate the thickness of the semiconductor devices 11, 12. Typically, the device carrier portion 19 and the leads 20 of the leadframe 13 are stamped or etched from a metal sheet so that the upper side 35 of the device carrier portion 19 and the upper side 35 of the leads 20 are generally coplanar with one another. The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a surface mountable or leadless type electronic component. Alternatively, the outer portions of the leads may be bent in a general direction away from the first side of the two semiconductor devices to provide pins by which the electronic component 10 may be mounted on a redistribution board such as a printed circuit board. Otremba124 discloses the following at [0041] In an example, the power transistor arrangement 100 with a flipped SFET and a wire bonded GaN HEMT may be packaged in a 8x8 ThinPAK, wherein the GaN HEMT 110 may be a high voltage (e.g. larger than 200V) HEMT switch and the SFET 120 may be a low voltage (e.g. smaller than 200V) power MOSFET. The GaN HEMT 110 is a normally on device, and is transformed to a normally off transistor with introducing of the low-voltage SFET 120. Such a GaN-SFET arrangement 100 may correspond to the cascade circuit 500 of FIG. 5. Otremba124 discloses the following at Fig. 1 (annotated)

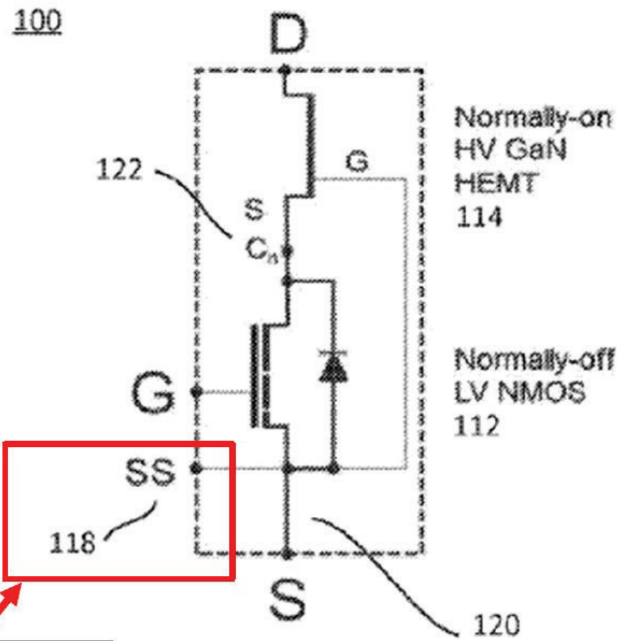
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	 Leads – Substantially planar contact surfaces on the lower external surface of the housing Die pad exposed on the bottom surface of the housing FIG. 1
[17c] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,	<i>Nega</i> alone or in combination with other references discloses or renders obvious wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad. <i>See supra</i> claim 1. For example, <i>Nega</i> discloses the following at [0056] The transistor HT1 includes the gate electrode GE1 provided on the gate insulating film GI1. The gate electrode GE1 is formed at a position overlapping the gate recess GR1 when seen in a plan view. The gate electrode GE1 is, for example, a laminated structure in which Ni and Au are laminated in order. <i>Nega</i> discloses the following at [0057]

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	The gate recess GR1 and the gate electrode GE1 are provided so as to be located between the source electrode SE1 and the drain electrode DE1. <i>Nega</i> discloses the following at [0058] The transistor HT1 includes the source electrode SE1 and the drain electrode DE1. The source electrode SE1 and the drain electrode DE1 is provided on the compound semiconductor layer CL2 so as to come into contact with the compound semiconductor layer CL2. In the present embodiment, the source electrode SE1 and the drain electrode DE1 are provided in the opening formed in the gate insulating film GI1, and thus the source electrode SE1 and the drain electrode DE1 come into contact with the compound semiconductor layer CL2. <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at [0095] In the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1. In the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE2 is connected to the outer lead OL1. <i>Nega</i> discloses the following at Fig. 4 (annotated)

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Roberts discloses the following at [0056] The arrangement shown in FIGS. 1A and 1B may be viewed as a very high power microwave integrated hybrid device. As mentioned above, the GaN power transistor may, for example, be required to provide less than 20 nS switching time and more than 30 A current switching capability. In conventional arrangements using a discrete, single N channel driver FET, such as shown in FIG. 1A, a “Kelvin Source Sense” or Kelvin connection SS is provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive L di/dt noise generated by the high current fluctuations of the source connection S. Roberts discloses the following at [0057] Any significant series inductance at the MOSFET source (S) 120 or at the common node (Cn) 122 will provide unwanted L di/dt transients. Such transients can potentially be as large as the threshold voltage of devices—typically plus 2 V for the MOSFET and minus 3 V for a GaN HEMT or minus 7 V for a GaN MISFET, which would result in unwanted switching. Additionally, series resistance in the source connection 120 results in debiasing which produces an apparent increase of the on-resistance. Thus, it is desirable to provide a driver circuit that provides monitoring and control of noise and transients. Preferably the driver circuit comprises a CMOS driver circuit and the driver MOSFET is integrated with the CMOS driver circuit. Roberts discloses the following at [0095] Thus systems according to the embodiments provide one or more of reduced series inductance and resistance; low thermal resistance; separate Kelvin connection(s); effective thermal management. Roberts discloses the following at Fig. 1A (annotated)

Claim 17

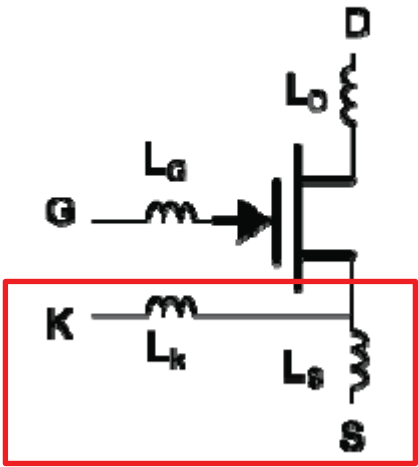
Exemplary Disclosure based on *Nega* and Related Combinations

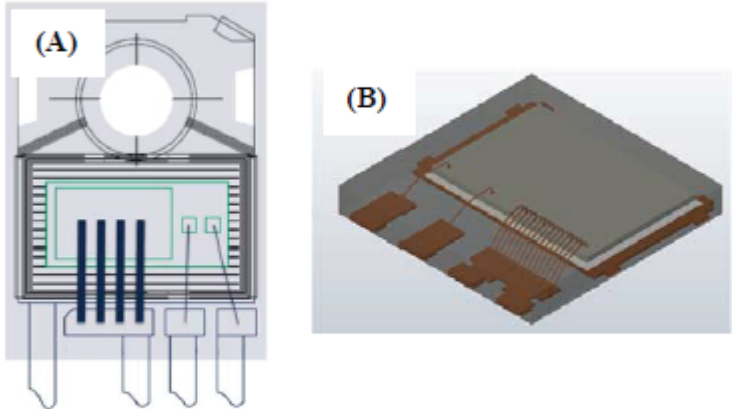


Third lead for
source sensing

FIG. 1A

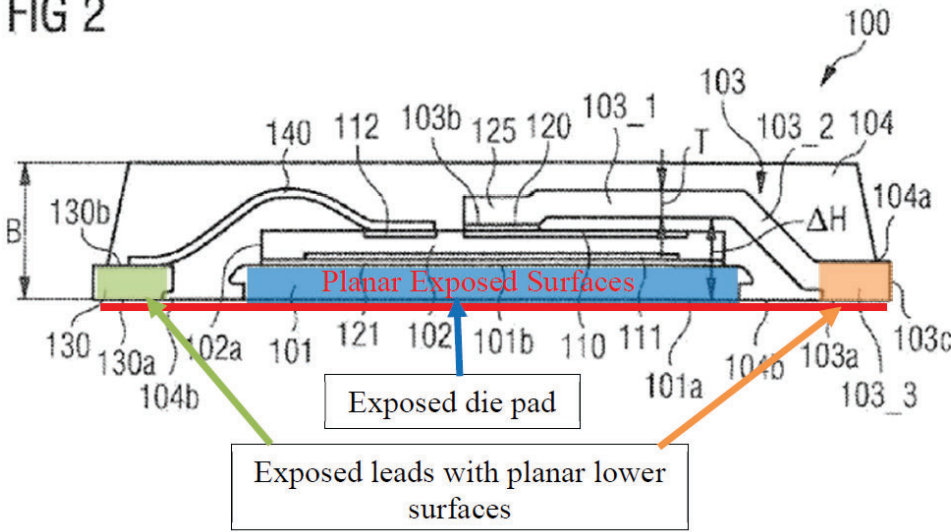
Huang discloses the following at 2, Fig. 2 (annotated):

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	DFN 8x8  Lind discloses the following at 3

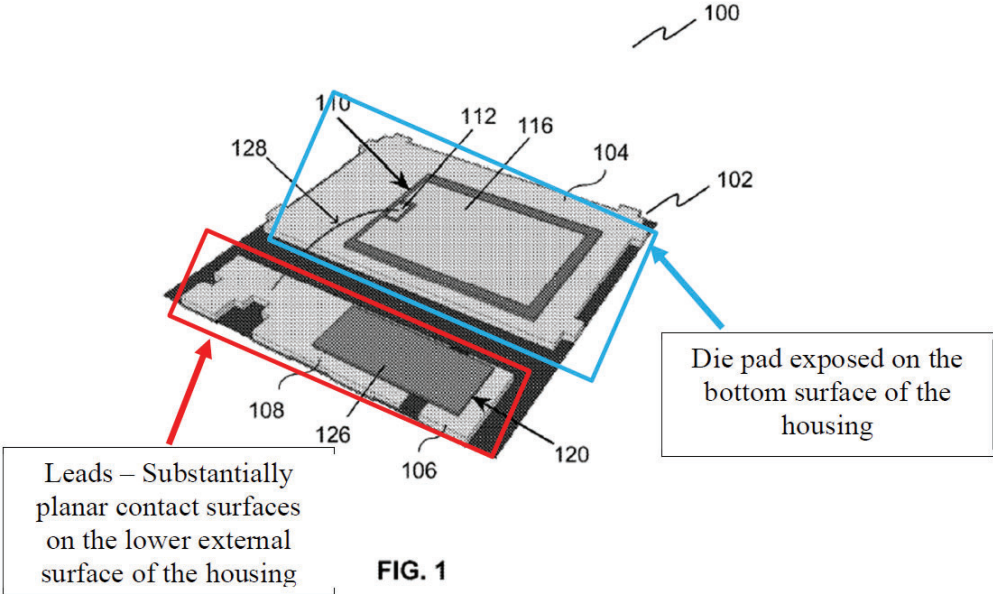
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	III. Source-Sense concept and A/B simulation A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.  Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections The principle is to provide a separate path for the drain-source current, such that voltage generated across the source inductance no longer appears in the KVL mesh of the gate current loop. McKnight discloses the following at 12:20-27: For example, the packaging assemblies of the embodiments described herein may be adapted for GaN dies comprising lateral GaN devices with alternative layouts. Pack ages with other external contact arrangements, e.g. comprising single or multiple external pads for each of the Source, drain and gate connections may be provided. Option ally, the package includes an additional external contact pad, e.g. a source sense (Kelvin) connection.

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Otremba528 discloses the following at [0002]: Chip contact regions, such as source and/or drain contacts are each normally supplied with voltage through connecting elements, such as electrically conductive wires, electrically conductive leads or clips. Furthermore, a source-sensing lead may be connected to a source contact to measure and/or monitor the potential of the source contact. Source-sensing leads may be connected to the source contact through additional redistribution elements, such as through an electrically conductive wire. The electrically conductive wire may be connected to a source contact, e.g. by wire bonding. These multiple contacting mechanisms may lead to additional packaging costs, which in particular may be attributed to the need for extra source-sensing leads. Otremba528 discloses the following at Fig 4 (annotated):

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
housing and provide substantially planar contact surfaces,	Otremba433 discloses the following at [0027] FIG. 1 illustrates a top view of an exemplary semiconductor device 100 in accordance with one embodiment. The semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104. FIG. 2 schematically illustrates a cross-sectional view of the semiconductor device 100 shown in FIG. 1 along section line A-A. Otremba433 discloses the following at [0037] The encapsulation body 104 of the semiconductor device 100 may embed the carrier 101 and the semiconductor chip 102 at side and top faces. The terminal portion 103_3 of the contact clip 103 forms an external terminal of the semiconductor device 100 and, therefore, protrudes out of the encapsulation body 104. By way of example, as illustrated in FIGS. 1 and 2, the semiconductor device may have a leadless package. In this and other cases the terminal portion 103_3 of the contact clip 103 may have an external contact area 103 a exposed at the encapsulation body 104, e.g., at the bottom of the package. The external contact area 103 a may be coplanar with a reference plane defined by a bottom surface 101 a of the carrier 101. The bottom surface 101 a of the carrier 101 may also be exposed at the bottom of the package. Further, a bottom surface portion 104 b of the encapsulation body 104 may be coplanar with the reference plane defined by the bottom surface 101 a of the carrier 101. In this case, the bottom surface 101 a of the carrier, the bottom surface portion 104 b of the encapsulation body 104 and the external contact area 103 a of the terminal portion 103 may all be arranged substantially level with each other. They may form the bottom of the package. Otremba433 discloses the following at [0039] The lead post 130 may form another external terminal of the semiconductor device 100. A bottom surface 130 a of the lead post 130 may be exposed at the bottom surface of the package of the semiconductor device 100 in order to e.g., provide for another SMT external contact area of the package.

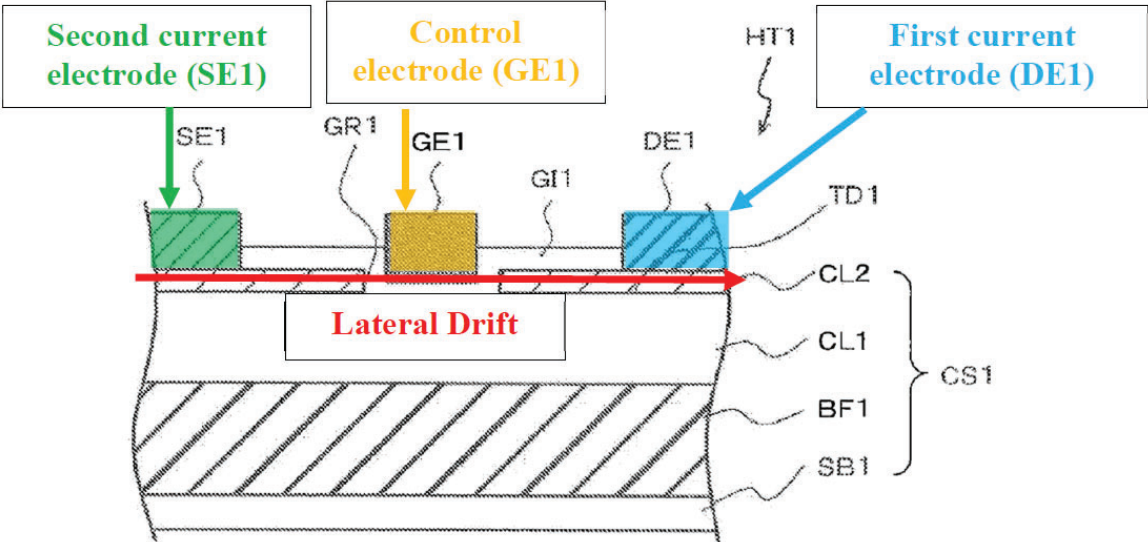
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Otremba433 discloses the following at [0025] A contact clip is provided to electrically connect an electrode of the semiconductor chip to an external terminal of the semiconductor device. The contact clip may be an integral part having a bond portion bonded to the first electrode and having a terminal portion forming an external terminal of the semiconductor device. By way of example, the external terminal of the semiconductor device may comprise an external contact area exposed at the encapsulation body of a leadless package. The external terminal of the semiconductor device may also be a lead of a leaded package. Otremba433 discloses the following at Fig. 2 (annotated) FIG 2  Otremba280 discloses the following at 4:1-29

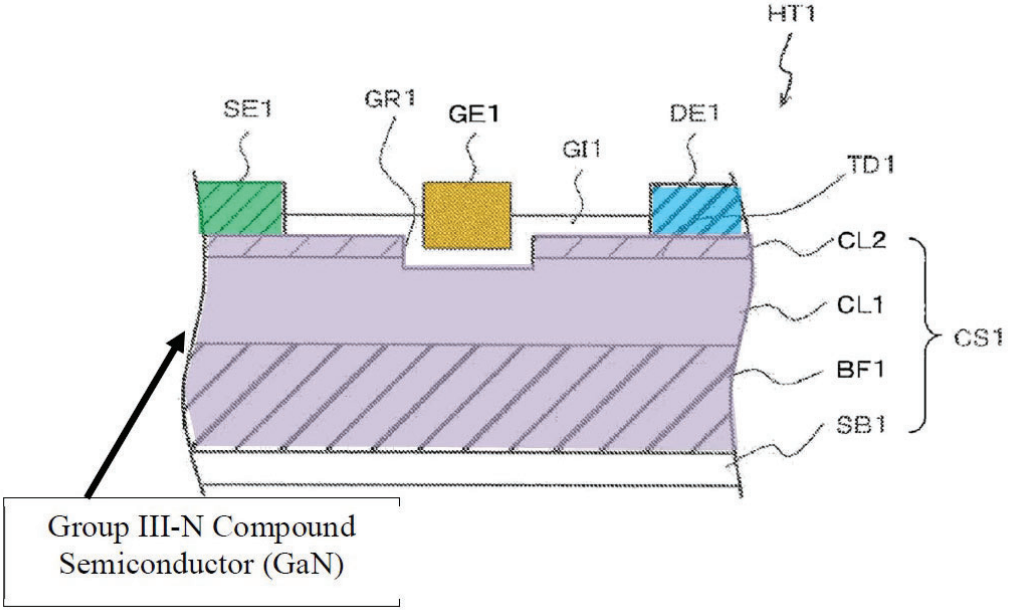
Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	The electronic component 10 comprises two semiconductor devices 11, 12 whose first load electrodes 17 (sources) are electrically connected to one another and to a lead 23 of the leadframe 13 by a single electrically conductive element in the form of a contact clip 14. The contact clip 14 may be provided in the form of a metal strip having the lateral size and shape and vertical form adapted to extend between the first load electrodes 17 of two semiconductor devices 11, 12 and the upper surface 35 of a lead 23 of a leadframe 13. In this embodiment, the leadframe 13 is positioned within the electronic component at a level below the first side of the semiconductor devices 11, 12. The upper surface of the lead 23 may lie generally coplanar with the second side 16 of the semiconductor devices 11, 12. The contact clip 14 may have a general form and height adapted to accommodate the thickness of the semiconductor devices 11, 12. Typically, the device carrier portion 19 and the leads 20 of the leadframe 13 are stamped or etched from a metal sheet so that the upper side 35 of the device carrier portion 19 and the upper side 35 of the leads 20 are generally coplanar with one another. The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a surface mountable or leadless type electronic component. Alternatively, the outer portions of the leads may be bent in a general direction away from the first side of the two semiconductor devices to provide pins by which the electronic component 10 may be mounted on a redistribution board such as a printed circuit board. Otremba124 discloses the following at [0041] In an example, the power transistor arrangement 100 with a flipped SFET and a wire bonded GaN HEMT may be packaged in a 8x8 ThinPAK, wherein the GaN HEMT 110 may be a high voltage (e.g. larger than 200V) HEMT switch and the SFET 120 may be a low voltage (e.g. smaller than 200V) power MOSFET. The GaN HEMT 110 is a normally on device, and is transformed to a normally off transistor with introducing of the low-voltage SFET 120. Such a GaN-SFET arrangement 100 may correspond to the cascade circuit 500 of FIG. 5. Otremba124 discloses the following at Fig. 1 (annotated)

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	 FIG. 1
[17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad,	<i>Nega</i> alone or in combination with other references renders obvious wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad. <i>See supra</i> claims 1-2. For example, <i>Nega</i> discloses that the compound semiconductor transistor device is a lateral transistor because the device is arranged laterally with the electrodes on the same lateral plane in a lateral drift path with the current generally flowing parallel to the surface. The '481 patent explains that “lateral” means “run[ning] generally parallel to the lateral extent of a semiconductor material or semiconductor carrier” ('481 patent, 3:14-18) and describes a device that “has a lateral drift path” ('481 patent, 4:37-38). Smart Power ICs (Innoscience 1414-00012740 –

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	Innoscience 1414-00012823) defines a horizontal (i.e. lateral) transistor as a structure where “current enters and leaves the chip through the upper surface of the chip.” At 7. <i>Nega</i> discloses the following at [0034] According to such a configuration, the transistor HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1, thereby allowing a switching device having a lower loss than a silicon device to be realized. For this reason, it is possible to achieve an improvement in the power source efficiency of the DC/DC converter circuit. In addition, the transistor HT1 connected to the input terminal is configured to be a normally-off type, thereby allowing flow of a through-current into a circuit in a state where power is not completely supplied to the DC/DC converter circuit to be suppressed, without newly providing a protection circuit. Therefore, it is possible to suppress complication of a circuit. <i>Nega</i> discloses the following at [0046] As shown in FIG. 2, the transistor HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1. In addition, the transistor HT1 is a normally-off type transistor. <i>Nega</i> discloses the following at [0049] The compound semiconductor layer CL1 is provided on the buffer layer BF1. The compound semiconductor layer CL1 is, for example, a GaN layer. The thickness of the compound semiconductor layer CL1 is, for example, 1 μm. <i>Nega</i> discloses the following at [0050] The compound semiconductor layer CL2 is provided on the compound semiconductor layer CL1. As the compound semiconductor layer CL2, a layer having a hetero interface being formed with respect to the compound semiconductor layer CL1 is selected. Thereby, the two-dimensional electron gas layer TD1 serving as a channel region of the transistor HT1 is formed

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	on the interface between the compound semiconductor layer CL1 and the compound semiconductor layer CL2. In the present embodiment, the compound semiconductor layer CL2 is, for example, an AlGa_N layer, and particularly preferably an Al_{0.15}Ga_{0.85}N layer. The thickness of the compound semiconductor layer CL2 is, for example, 10 nm. <i>Nega</i> discloses the following at [0094] The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at Fig. 2

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	FIG. 2  The diagram illustrates a cross-sectional view of a device. At the top, three electrodes are shown: a green 'Second current electrode (SE1)' on the left, a yellow 'Control electrode (GE1)' in the center, and a blue 'First current electrode (DE1)' on the right. A red arrow labeled 'Lateral Drift' points from the SE1 towards the DE1. The device is built on a substrate with several layers: a top layer (GI1) containing the electrodes, a middle layer (CL2) with a red arrow indicating lateral drift, and a bottom layer (CL1) which is part of a stack (CS1) including BF1 and SB1. A heat source (HT1) is indicated by a wavy arrow pointing towards the DE1. A gate region (GR1) is located between the SE1 and GE1. A top dielectric layer (TD1) is shown above the DE1. <i>Nega</i> discloses the following at Fig. 2 (annotated)

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	FIG. 2  Group III-N Compound Semiconductor (GaN)
[17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.	<i>Nega</i>, alone or in combination with one or more references, discloses and/or renders obvious wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip. <i>See supra</i> claim 1. For example, <i>Nega</i> discloses the following at [0094]

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	The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1. <i>Nega</i> discloses the following at Fig. 4 (annotated and modified) FIG. 4 The diagram illustrates a semiconductor package assembly. A central die pad (LF1) is shown with a first current electrode (drain) connected to it by a plurality of bond wires (BW1). The assembly includes a lead frame (LF1) and an outer lead (OL1). A bonding wire (BW1) is shown connecting the die pad (LF1) to the outer lead (OL1). A callout box highlights the connection of the first current electrode (drain) to the die pad (LF1) by a plurality of bond wires (BW1). Other components labeled include LD1, HD1, and SM1. <i>Nega</i> discloses the following at Fig. 4 (annotated)

Claim 17	Exemplary Disclosure based on <i>Nega</i> and Related Combinations
	FIG. 4 First current electrode (drain) coupled to die pad (LF1) by a plurality of bond wires (BW1) 