UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOSCIENCE AMERICA, INC.,
Petitioner,

v.

INFINEON TECHNOLOGIES AUSTRIA AG,
Patent Owner.

IPR2024-00975
U.S. Patent 9,899,481

DECLARATION OF MICHAEL LEBBY, PH.D.

Infineon Exhibit 2019
Innoscience v. Infineon
IPR2025-00721

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3. Claim 3 - The electronic component of claim 1, wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz. 70

4. Claim 5 - The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad. 73

5. Claim 6 - The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip. 75

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2. Claim 9 - The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline. 93

3. Claim 17 94

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3. Claim 4 - The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces. 146

4. Claim 5 - The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad. 147

5. Claim 6 – The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip. 148

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1. Claim 3 - The electronic component of claim 1, wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400 V and a switching frequency capability of at least 100 kHz. 150

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1. Claim 4 - The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces. 155

2. Claim 9 - The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline. 162

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1. Claim 7 – The electronic component of claim 4, wherein the first current electrode is coupled to the die pad by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing. 163

2. Claim 8 - The electronic component of claim 4, wherein the second current electrode is coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing. 167

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I. INTRODUCTION

[01] I have been retained by Innoscience America, Inc. as an independent expert for the above-identified *inter partes* review proceeding involving U.S. Patent No. 9,899,481 ("the '481 patent").

[02] I am over 21 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein.

[03] Although I am being compensated for my time in connection with this proceeding at my standard hourly consulting rate and reimbursed for reasonable out-of-pocket expenses, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

[04] I have been asked to provide my opinion whether the claims of the '481 patent would have been obvious to a person of ordinary skill in the art at the time of the earliest claimed priority date of the '481 patent. In performing my analysis, I have been asked to assume that the priority date is January 18, 2016. My opinions are set forth below.

[05] Throughout this declaration, I refer to specific pages, figures, and/or line numbers of various exhibits. These citations are illustrative and are not intended to suggest that they are the only support for the propositions for which they are cited.

II. SUMMARY OF OPINIONS

[06] This declaration analyses claims 1-17 of the ’481 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for my opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

[07] Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of January 18, 2016), it is my opinion that claims 1-17 of the ’481 patent would have been obvious based on the asserted grounds discussed below.

III. QUALIFICATIONS AND BACKGROUND

[08] I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Ex-1004.

[09] I am competent to write this Declaration.

[010] I received a Bachelor of Engineering degree in Electrical and Electronic Engineering in 1984 from the University of Bradford, UK. I also received a Ph.D. in Semiconductor Physics in 1987 from the University of Bradford, UK. My Ph.D. thesis involved the design and fabrication of both optoelectronic and electronic compound semiconductor devices, as well as their

characterization. In 2004, I was awarded a Doctor of Engineering degree (a higher doctorate degree) from the University of Bradford for my technical contributions to the field.

[011] As described in this Section, and further detailed in my curriculum vitae (Ex-1004), over the course of my 40-year career in electronics and optoelectronics, I have worked in nearly every aspect of the electronic and optoelectronics business, ranging from epitaxial wafer growth (compound semiconductors), electrical and optoelectronic device design, using modeling and simulation, electrical and optoelectronic device and component fabrication, testing, and qualification, to the implementation of devices into packages, both hermetic and non-hermetic, as well as analysis of package materials such as plastics (including plastic housings such as resin-packaged lead frame housings), optical plastics, metallic-based packages, semiconductor-based packages, and ceramic-based packages. I have also designed and fabricated field effect transistors, including III-nitride transistors. I have also worked in commercially based industrial research-and-development laboratories to bring new electronic, optoelectronic- and photonic-based technologies from the research proof-of-concept phase through prototyping and qualified manufacturing for volume release.

[012] I have been both an entrepreneur (e.g., Ignis Optics Inc, One Chip Photonics, Lightwave Logic Inc.), as well as an intrapreneur (e.g., Motorola, Intel, TE Connectivity (previously Tyco Electronics), AT&T Bell Labs), creating innovative new programs, both as venture backed start-ups as well as corporate funded divisions. I have built these entities to develop electronic, optoelectronics, and photonics technology from the laboratory and fabrication clean room to production factories.

[013] My career started in the late 1970s at the Ministry of Defense in the UK where I spent time at their R&D facility in Malvern (RSRE – Royal Signals and Radar Establishment). I worked on electronic and optoelectronic semiconductor device design, fabrication, and characterization, and especially materials using III-V compound semiconductors. These devices included electronic transistors, optical waveguides, and optoelectronic device operation. My research work in semiconductor device design then took me to AT&T Bell Laboratories in 1985, where I pursued research in novel opto-device designs using III-V semiconductor material systems that included FETs, bipolar transistors, optical waveguides, optics, LEDs, laser diodes, and photodetectors. The devices researched became in part the subject of my PhD thesis that was granted in 1987.

[014] I moved to Motorola in 1989 to further develop my electronic, optoelectronic, semiconductor engineering and development skills, and I became a

Research and Development Manager in Motorola, until I left the company in 1998. During my time at Motorola, I worked on many photonic, electronic, and optical technology projects that included optical lenses, display, imaging, camera, fiber-optic optical interconnects, electronic circuits (both analog and digital), displays, LEDs, and laser devices, as well as the packaging and reliability of mobile product prototypes. At that time, I worked on miniature displays and miniature optics using a number of technologies such as LEDs, lasers, LCDs, lenses, and organic LEDs which were aimed towards (at the time) pagers, mobile phones, micro-imagers/displays, holograms, and advanced prototypes of futuristic communications hardware. I also worked in miniature color displays in which LEDs could be utilized, and the associated drive and processing electronics for them.

[015] In aiming for miniature full color displays and associated optics, the early 1990s, there was only red wavelength Phosphide (GaAsP and/or InGaAlP) and AlGaAs based LED technology that was advanced in technology and performance. Green wavelength Gallium Phosphide based LEDs had low emission output, and blue wavelength emission LEDs were only available using pure Silicon Carbide on Silicon Carbide substrate wafers, with very low emission output. I worked closely with Motorola's mobile divisions on new and novel display prototypes for mobile phones etc., and optics to research and develop how best to

innovate with full color red, green, and blue displays and associated electronics. A number of alternative technologies were evaluated, such as LCD (Liquid Crystal Displays), OLED (organic LEDs), and Gallium Nitride and Indium Gallium Nitride materials grown onto Sapphire. I also explored the electronic circuits that were needed to drive, operate, and signal these types of optoelectronic displays.

[016] The compound semiconductors used in the early 1990s at Motorola corporate research, for which I was a Research and Development Manager, included the Group III-V materials system, Group IV material system, Group VI material system, and Group III-N material system. A number of these materials included: GaAs, InP, GaN, GaP, InGaAlP, and silicon, amongst other materials, all of which were intended to be designed into various light emitting sources, detectors, and electronics in their associated optical package platforms that included optics and lens design.

[017] I was one of Motorola's most prolific inventors, having over 150 issued utility patents as an inventor or a co-inventor by the late 1990s. Many of the photonics, electronics, and optical prototypes with which I was involved were subject to reliability and stress testing that included humidity, temperature, optical, mechanical, and electrical evaluation. These consumer products all were driven using standard electronic ICs and electronic signaling.

[018] I filed my first GaN patent, which taught techniques using GaN and InGaN LEDs, in 1996, shortly after the invention of high performance GaN/InGaN blue LEDs by Nichia in the early 1990s. My work at Motorola addressed, in part, the big issue at the time in the mid-1990s: full color display and display electronics composed of red, green and blue LEDs that could be utilized in mobile products as well as other applications. As part of this work, I was engaged in how to optically package these technologies that allowed for electrical, optical, and thermal high performance. Examples of patents on which I am a co-inventor include, for example, U.S. Patent No. 5,538,919, as well as U.S. Patent No. 5,818,404, U.S. Patent No. 5,739,800, and U.S. Patent No. 5,838,703. My additional patents, including during my time at Motorola, are listed in my curriculum vitae (Ex-1004).

[019] Another of my inventions was directed to a new semiconductor laser that had the potential to be manufactured in high volume. This device was called a VCSEL (vertical cavity surface emitting laser), and the invention was to optimize the performance using an oxide process. It is now the basis for the highest volume semiconductor laser today (with its recent implementation as a structured light sensor in facial recognition systems utilized in modern day smart mobile phones).

[020] Between 1998 and 1999, I worked as the Director of Technology/ BD (Fiber Optics) for Tyco Electronics (previously AMP). I joined Tyco Electronics as a member of the Global Optoelectronics Division's management team. I was

responsible for growing the optoelectronics and optical business through external interactions that included mergers, acquisitions, strategic alliances, and technical strategic planning. Much of that work was laser- and LED-based, with associated optics, and included designing and characterizing laser- and LED-based optical packages and modules for customer qualification specifications.

[021] In 1999, I left Tyco and started employment at Intel. At Intel, I was involved heavily in photonic technology, especially technology that supported silicon photonic device platforms. As a culmination of this work, I was one of Intel's founders of its silicon photonics division in the year 2000, and worked to set up a fabrication facility in South San Jose. The work involved integrating silicon FET electronics with optoelectronics and optics onto the same silicon semiconductor wafer. I was also part of Intel Capital's optical investment team, and participated in over 30 photonics investments into photonics, optics, and optoelectronics. Focus included optical devices, packaging and modules. Technologies investigated included lasers, LEDs, optics, and optical displays.

[022] At the end of 2000, I left Intel and raised venture capital funding for a company called Ignis Optics Inc. The main goal of the company was to design and manufacture, in high volume, very high-performance optoelectronic devices. For my work at Ignis Optics, I worked on different semiconductor devices like diodes and photodetectors. My work at Ignis Optics is further described in my patents,

such as U.S. Patent Nos. 6,999,644; 6,663,296; and 6,795,461, which generally relate to semiconductor devices, optoelectronics, and device fabrication and design. I am also an inventor or co-inventor on other patents that generally relate to semiconductors devices and their fabrication such as U.S. Patent Nos. 5,045,908; 5,125,054; 5,959,315; 5,228,101; 5,313,545; 5,337,391; 5,361,317; 5,369,529; 5,416,870; 5,428,704; 5,521,992; 5,545,359; 5,539,200; 6,064,780; 5,543,958; 5,486,946; 5,625,734; 5,739,800; and 5,905,750; as well as EP0633607A1; EP0635741A2; and JPH0756062A.

[023] In 2005, I took up employment for a trade association, based in Washington, D.C., called IEEE Optoelectronics Industry Development Association (OIDA). As head of this trade association, and with photonics and optics manufacturers that included fiber optics, display, cameras, sensing, defense, aerospace, LED lighting, and automotive vendors as members, I was responsible, in part, for industry-based technology roadmaps; and I implemented common industry roadmap methodologies with common features such as "Red Brick Walls" and transferred them into optoelectronics roadmaps for the industry in which LEDs, fiber-optics, optics, fiber, cameras, optical sensors, displays, and their associated packaging, were featured. OIDA roadmaps featured purple brick walls, to show differentiation from the semiconductor industry.

[024] In 2010, I became the General Manager and CTO of Translucent, Inc., a high-tech start-up company which developed and manufactured silicon and rare earth oxide based epitaxial semiconductor wafers. One of the key drivers at Translucent was to develop a new and novel platform for the growth of GaN and InGaN onto silicon for low-cost LED, RF FET, and power FET manufacturing on larger format substrate wafers (e.g., 200mm), in order to achieve economies of scale and lower chip costs. Translucent pioneered the deposition of single crystal rare earth oxides such as Erbium Oxide (ErOx), Gadolinium Oxide (GdOx), Neodymium Oxide (NdOx), etc., that, when grown, single crystal layers of GaN and III-N materials such as InGaN, InGaAlN, InGaAlNAs, AlN etc., could be grown on top of them. This allows a lattice-matched (strained or otherwise), and monolithic-based, wafer template to be manufactured for both FET and LED fabrication. While at Translucent, I researched various epitaxial semiconductor layer structures that utilized rare earth oxide technology in order to improve the performance of III-N, GaN based FETs and LEDs. Other material growth work at Translucent focused on the growth of Silicon Germanium (SiGe) compounds with rare earth oxides, and various crystal orientation wafer substrates. I patented a number of electronic FET device designs using rare earth oxides while employed at Translucent.

[025] I am currently Chief Executive Officer (CEO) and Chief Technology Officer (CTO) of GenusTechnik Inc. GenusTechnik Inc., is my consulting company, through which I engage in my expert witness work.

[026] I also presently hold the position of CEO of Lightwave Logic Inc. (LWLG), where I also serve as a Director on the Board of Directors. Lightwave Logic develops electro-optical polymer modulators for the fiber optic communications industry.

[027] Throughout my career, I have also had an active role in a number of technical professional organizations, including, among others, IEEE Components, Packaging, and Manufacturing Technology (CPMT), IEEE Electronic Components and Technology Conferences (ECTC); IEEE TC-10 (Technical Committee on Optoelectronics), and IEEE Optoelectronics Industry Development Association (OIDA). Through these organizations, I have consistently been a part of committees, events, and workshops relating to semiconductor, optoelectronics, electronics, and packaging technology.

[028] I also serve as a Technical Expert/Consultant for the European Commission. In my work at the European Commission, I review and advise on general electronics, semiconductors, photonics, optoelectronics, imaging, sensing, display, and related ICT (Information and communications technology) technology.

[029] My work has also led to over 225 USPTO utility patents in semiconductors, electronics, optics, and optoelectronics, including a number of patents relating to optics for LEDs and laser technology. I am the author of more than 60 publications.

[030] A current copy of my curriculum vitae, Ex-1004provides further information concerning my experience and qualifications and includes: a list of my patents, a list of the publications I have authored, and a list of the matters on which I have served as an expert witness.

IV. MATERIALS CONSIDERED

[031] In forming my opinions, I read and considered the ’481 patent and its prosecution history, the exhibits listed in the Exhibit List filed with the petition for inter partes review of the ’481 patent, as well as any other materials referenced herein. I have reviewed the following at least the following documents:

Exhibit	Description
Ex-1001	U.S. Patent No. 9,899,481 (“the ’481 patent”)
Ex-1002	Prosecution History of the ’481 Patent (“Prosecution History”)
Ex-1005	U.S. Patent Application Publication No. 2014/0110760 (“Nega”)
Ex-1006	U.S. Patent Application Publication No. 2014/0175454 (“Roberts”)
Ex-1007	U.S. Patent Application Publication No. 2014/0225124 (“Otremba124”)

Ex-1008	U.S. Patent Application Publication No. 2014/0084433 ("Otremba433")
Ex-1009	U.S. Patent No. 7,880,280 ("Otremba280")
Ex-1010	U.S. Patent No. 10,930,524 ("Liu")
Ex-1011	U.S. Provisional Patent Application No. 62/196,629 ("Provisional")
Ex-1012	*Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.*, No. 3:24-cv-01553-SK, Dkt. No. 1, Complaint (N.D. Cal. Mar. 13, 2024)
Ex-1013	Anders Lind, *Source-Sense Packages for HV MOSFETs*, 46th International Symposium on Microelectronics (2013) ("Lind")
Ex-1014	U.S. Patent No. 9,589,869 ("McKnight")
Ex-1015	U.S. Patent Application Publication No. 2014/0097528 ("Otremba528")
Ex-1016	ThinPAK 8x8 New High Voltage SMD-Package (Apr. 2010) ("ThinPAK 8x8 Brochure")
Ex-1017	Recommendations for Printed Circuit Board Assembly of Infineon VDSON Packages (ThinPAK) (July 2010) ("ThinPAK Recommendations")
Ex-1018	U.S. Patent No. 9,099,441 ("Otremba441")
Ex-1019	*Infineon Technologies Austria AG v. Innoscience (Suzhou) Technology Company, Ltd. et al.*, No. 3:24-cv-01553-SK, Dkt. No. 28, Order Granting Administrative Motion to Continue Initial Case Management Conference and Associated Deadlines (N.D. Cal. May 2, 2024)
Ex-1020	U.S. Patent No. 9,230,880 ("Otremba880")
Ex-1021	U.S. Patent No. 8,691,631 ("Otremba631")

Ex-1022	Excerpts of Stephen Pearton, *GaN and ZnO-based Materials and Devices*, Springer Series in Materials Science (2012) ("Pearton")
Ex-1023	Excerpts of Muhammad H. Rashid, *Power Electronics Handbook*, Academic Press Series in Engineering (2001) ("Rashid")
Ex-1024	Xiucheng Huang et al., *Evaluation and Applications of 600V/650V Enhancement-Mode GaN Devices*, IEEE Explore (2015) ("Huang")

[032] I reserve the right to supplement and amend any of my opinions in this declaration based on documents, testimony, and other information that becomes available to me after the date of this declaration.

V. LEGAL STANDARDS

[033] I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

[034] I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can "anticipate" a claim. Second, I have been informed that the prior art can render a claim "obvious" to a person of ordinary skill in the art. I understand that a claim

is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

[035] I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

[036] I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-17 of the ’481 patent from the perspective of a person of ordinary skill in the art at the ’481 patent’s earliest claimed priority date in 2016, as described in more detail below.

[037] I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

[038] For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill in the Art

[039] I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with

which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

[040] I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Anticipation

[041] I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

C. Obviousness

[042] I have been informed that obviousness under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

[043] I have been informed that a proper obviousness analysis includes the following:

a. Determining the scope and content of the prior art;

b. Ascertaining the differences between the prior art and the claims at issue;

c. Resolving the level of ordinary skill in the pertinent art; and

d. Considering evidence of secondary indicia of non-obviousness (if available).

[044] I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the challenged claims is January 18, 2016. My opinions would not change if I assumed a later date of invention.

[045] I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

[046] I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

[047] In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;

e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a "reasonable expectation of success"—but not "absolute predictability" of success—in achieving the claimed invention by combining prior art references.

[048] I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been

informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

[049] I have been informed that the law permits the application of "common sense" in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

[050] I have been informed that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine references. But I also understand that the "teaching, suggestion, or motivation" test can be a useful guide in establishing a rationale for combining

elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

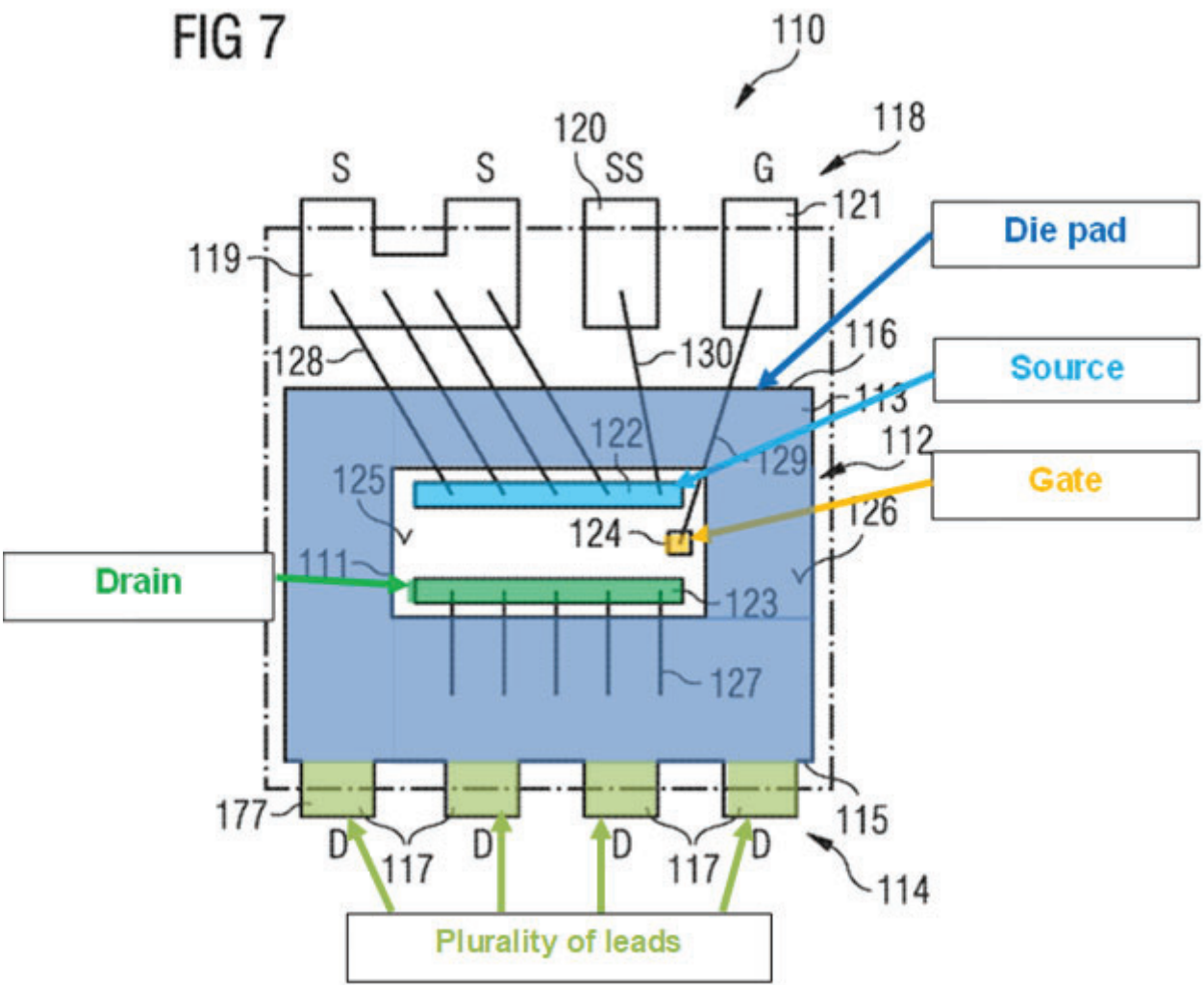
[051] I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the ’481 patent.

[052] I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. OVERVIEW OF THE ’481 PATENT

[053] The application that issued as the ’481 patent was filed on January 18, 2016. ’481 patent, Cover. The patent issued on February 20, 2018, with 17 claims, 3 of which are independent. ’481 patent, Cover, 15:50-18:16.

[054] The ’481 patent is directed to packaging a lateral compound semiconductor transistor device and coupling the transistor device to packaging leads in several different configurations using different coupling mechanisms. The lateral compound semiconductor transistor device includes a **die pad**, a **source**, a **gate**, and a **drain**. A **plurality of leads** extend from the **die pad**.



Ex-1001, Fig. 7 (annotated).

[055] The **drain** is electrically coupled to the **die pad** by a plurality of bond wires or a contact clip. The compound semiconductor transistor device conforms to a JEDEC package outline, a TO leadless (TOLL) package outline, or a ThinPak 8x8 package outline. Ex-1001, 6:29-34.

VII. LEVEL OF ORDINARY SKILL

[056] In rendering the opinions set forth in this declaration, I have been asked to consider the ’481 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as “one skilled in the art,” “skilled artisan,” “POSITA,” “POSA” or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

[057] Taking the factors described in the Legal Standards – Level of Ordinary Skill in the Art section into consideration, it is my opinion that a person of ordinary skill in the art with respect to the ’481 patent would have possessed at least a four-year degree in electrical engineering or a closely related field, and at least two years of experience in semiconductor device design. Additional education could substitute for professional experience and vice versa.

[058] Based on my educational background and experience, I was at least a person of ordinary skill in the art at the earliest priority date of the ’481 patent.

VIII. CLAIM CONSTRUCTION

[059] I am not an attorney. However, I have been informed by counsel of certain legal standards that apply with respect to claim construction and indefiniteness, and have used those standards, described below in formulating my opinions.

[060] I have been instructed that the "intrinsic record" includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent's prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office ("Patent Office") concerning the patent (Ex. 1002). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term's plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent's written description, the patent's prosecution history, or both.

[061] I understand that claim interpretation may also be informed by "extrinsic evidence" (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises,

and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the relevant time period.

[062] I am also informed by counsel that the applicant of the ’481 patent can act as their own lexicographer, to set forth a definition of a claim term in the specification. The definition provided by the applicant can differ from the claim term’s plain and ordinary meaning. I have also been informed by counsel that when a patent claim uses the term “comprises” as a transitional statement after the preamble, there is a presumption that the claim is open-ended and not limited to the recited elements.

[063] I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the ’481 patent, other than as identified below.

[064] Based on my review of these materials and my personal knowledge and experience, I have considered the plain and ordinary meaning of each term of the ’481 patent as it would have been understood by one skilled in the art at the earliest claimed priority date of the ’481 patent of January 18, 2016. I apply the plain and ordinary meaning of each claim term throughout this declaration, other than as identified below.

IX. THE PRIOR ART

[065] In forming my opinions, I found the following prior art relevant when considering whether the claims of the ’481 patent would have been obvious to a person of ordinary skill in the art:

- Ex. 1005, U.S. Patent Publication No. 2014/0110760 to Nega (“Nega”);
- Ex. 1006, U.S. Patent Publication No. 2012/0175454 to Roberts (“Roberts”);
- Ex. 1007, U.S. Patent Application Publication No. 2014/0225124 (“Otremba124”)
- Ex. 1008, U.S. Patent Application Publication No. 2014/0084433 to Otremba (“Otremba433”)
- Ex. 1009, U.S. Patent No. 7,880,280 to Otremba (“Otremba280”)
- Ex. 1010, U.S. Patent No. 10,930,524 to Liu (“Liu”)
- Ex. 1021, U.S. Patent No. 8,691,631 (“Otremba631”)

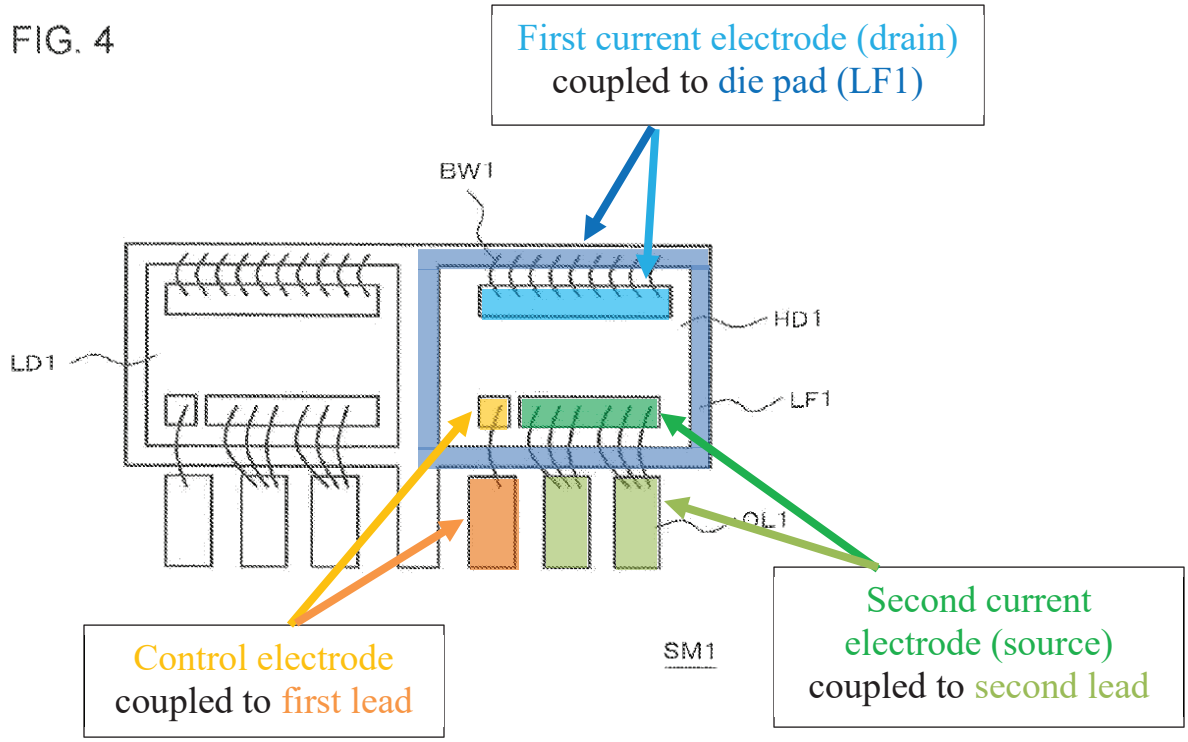
[066] In my opinion, these references disclose information that was not disclosed in the prior art the Examiner considered during prosecution. *Prosecution History*; ’481 patent, Cover. Based on my review, Nega, Roberts, Otremba124, Otremba433, Otremba280, Otremba631, and Liu are not cumulative of the prior art considered during prosecution because Nega, Roberts, Otremba124, Otremba433, Otremba280, Otremba631, and Liu teach the claim feature the patent applicant argued was not disclosed by the prior art. Additionally, Nega, Roberts,

Otremba124, Otremba433, Otremba280, Otremba631, and Liu are not cumulative from what the Examiner considered.

A. Nega (US 2014/0110760)

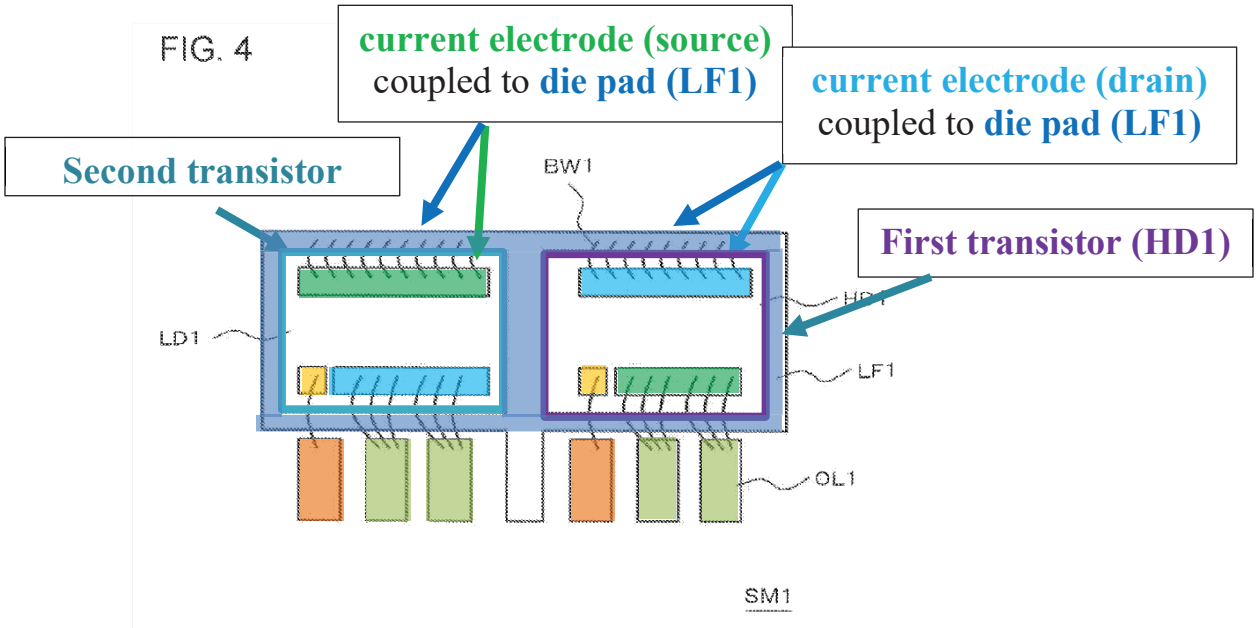
[067] Nega is a U.S. patent application publication that published April 24, 2014. Nega, Cover. The corresponding application had been filed on October 22, 2013. Nega, Cover.

[068] Like the '481 patent, Nega discloses a transistor with a source electrode and drain electrode connected to a lead frame and a gate electrode connected to an outer lead. Nega, [0095]. Nega discloses that each electrode is connected to the lead frame or outer lead by a bond wire. Nega, [0094].



Nega, Fig. 4 (annotated).

[069] Nega also discloses a second transistor.

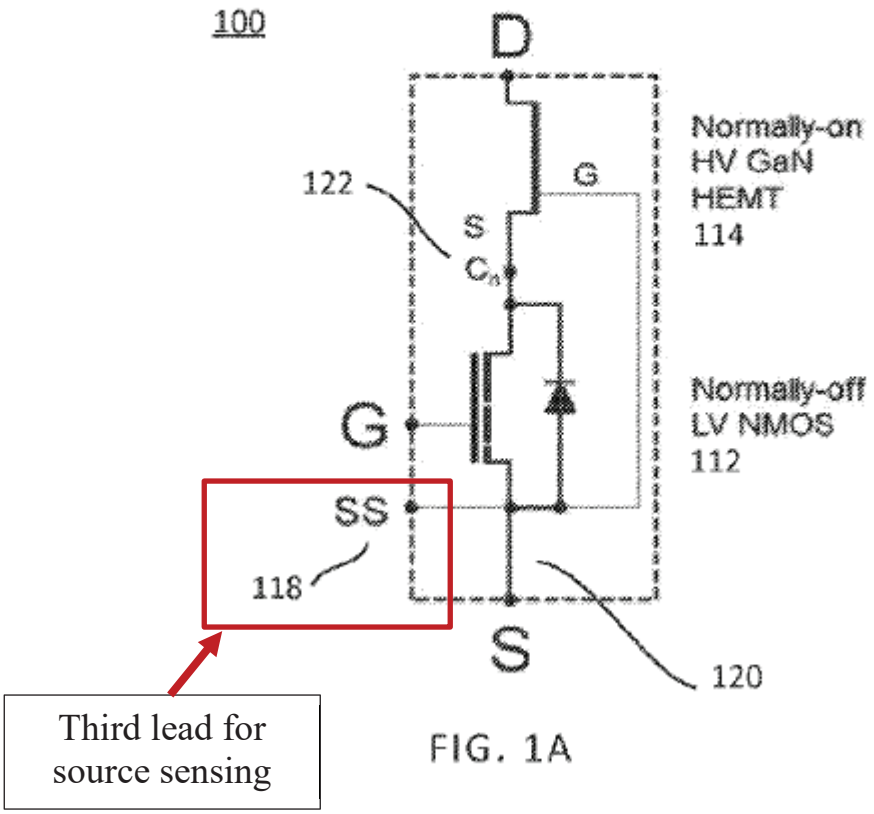


Nega, Fig. 4 (annotated).

B. Roberts (US 2014/0175454)

[070] Roberts is a U.S. patent application publication that published June 26, 2014. Roberts, Cover. The corresponding application had been filed on December 13, 2013. Roberts, Cover.

[071] Roberts discloses a transistor device intended for high-voltage applications. Roberts, [0006], [0012]. Roberts further discloses a Kelvin Source Sense or Kelvin "provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive L di/dt noise generated by the high current fluctuations of the source sense connection S." Roberts, [0056].

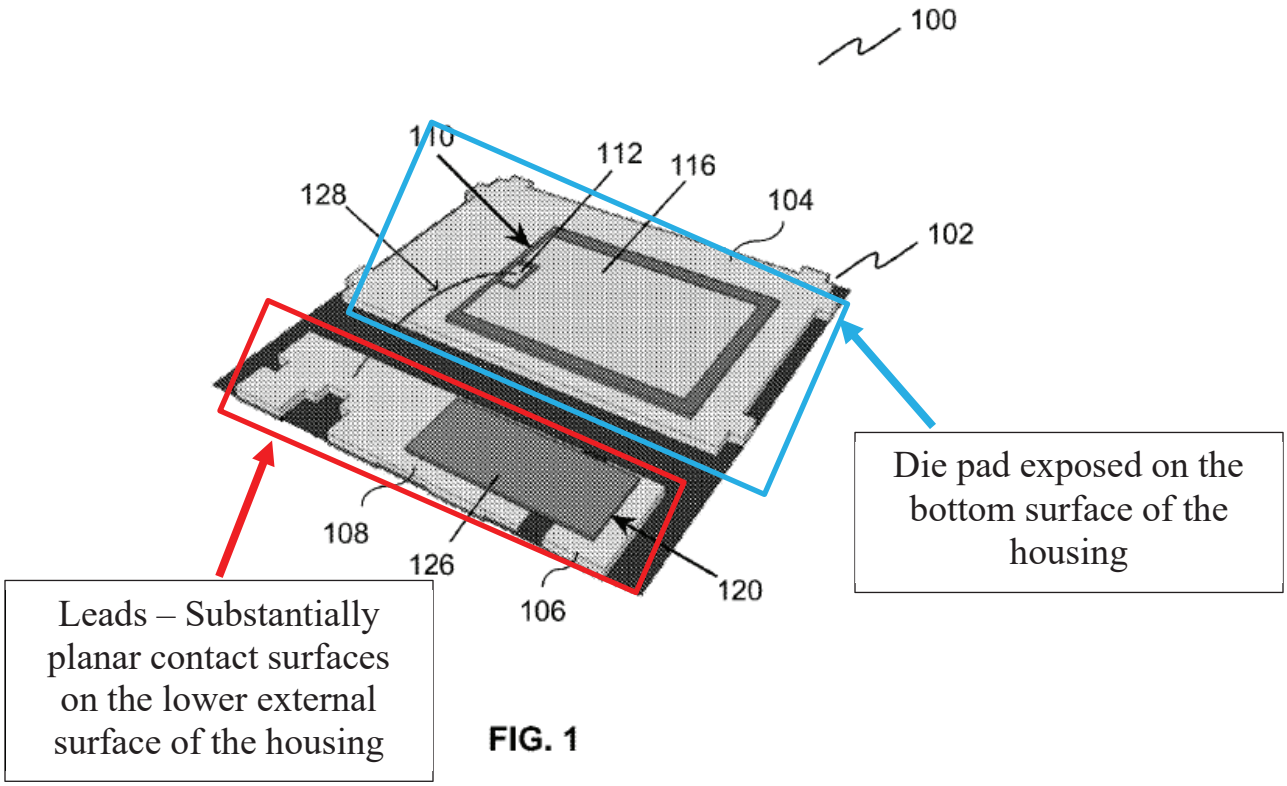


Roberts, Fig. 1A (annotated).

C. Otremba124 (US 9,263,440)

[072] Otremba124 is a U.S. patent that issued February 16, 2016. Otremba124, Cover. The corresponding application was published on August 14, 20214 and had been filed on February 11, 2013. Otremba124, Cover.

[073] Otremba124 discloses a ThinPak8x8 package outline with flat source leads on the bottom of the package. Otremba124, [0041]. Otremba124 also discloses planar exposed leads and an exposed die pad. Otremba124, [0041].

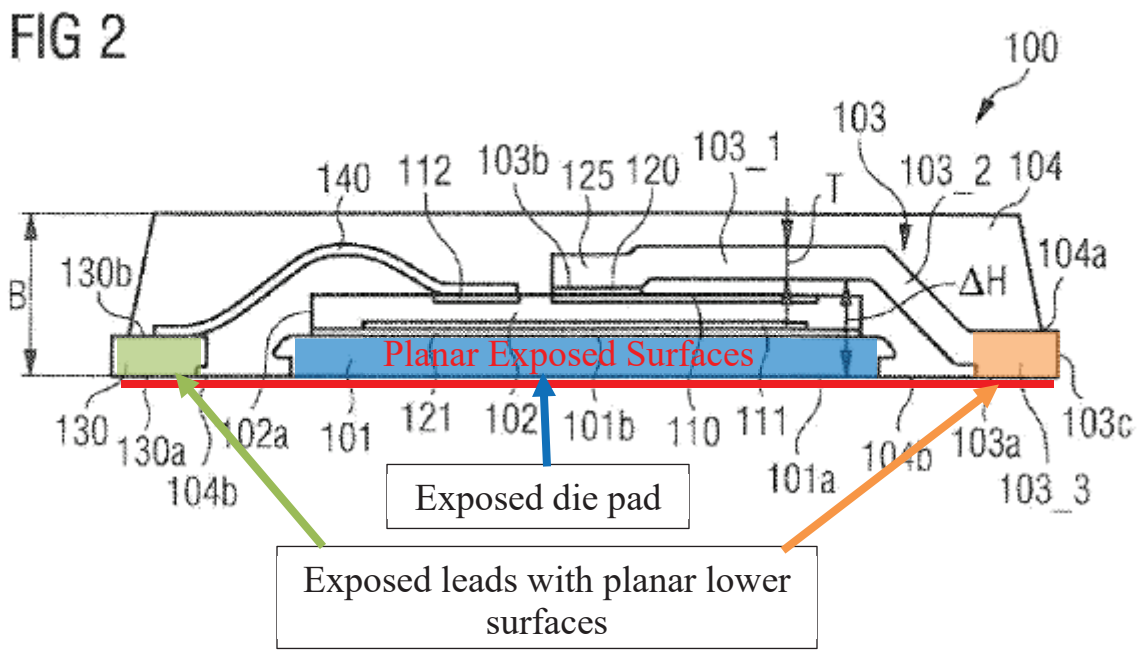


Otremba124, Fig. 1 (annotated).

D. Otremba433 (US 2014/0084433)

[074] Otremba433 is a U.S. patent application that published March 27, 2914. Otremba433, Cover. The corresponding application was filed on September 25, 2012. Otremba433, Cover.

[075] Otremba433 discloses planar exposed leads and an exposed die pad. Otremba433, [0037], [0039]. Otremba433 also discloses the use of contact clips. Otremba433, [0037], [0039].

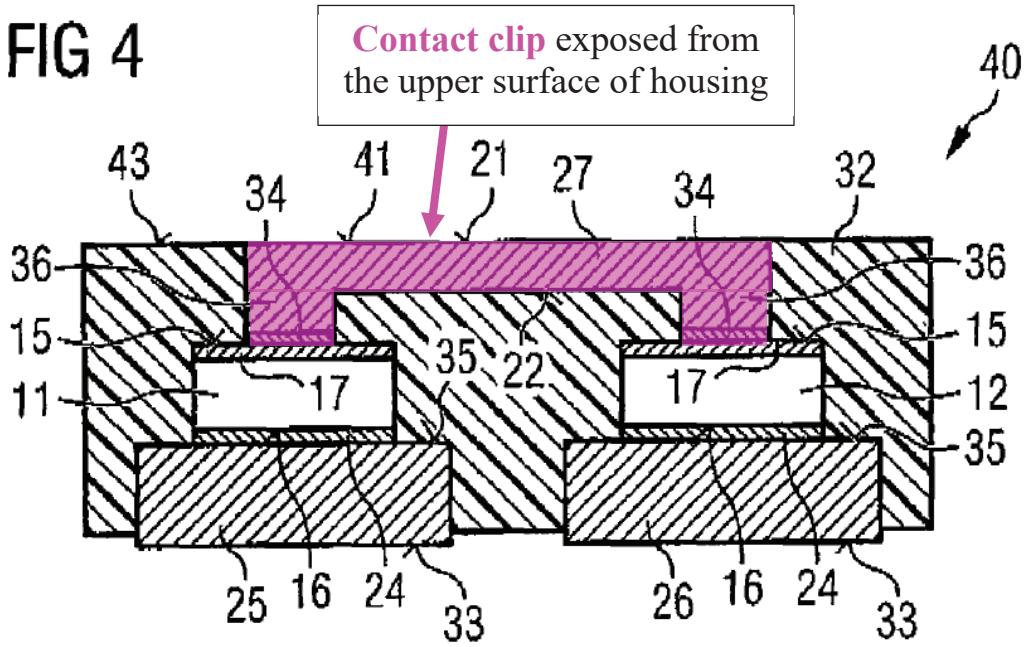


Otremba433, Fig. 2 (annotated).

E. Otremba280 (US 7,880,280)

[076] Otremba280 is a U.S. patent that issued on February 1, 2011. Otremba280, Cover. The corresponding application was published on August 21, 2008 and had been filed on February 16, 2007. Otremba280, Cover.

[077] Otremba280 discloses using exposed contact clips to couple components within a packaged device.

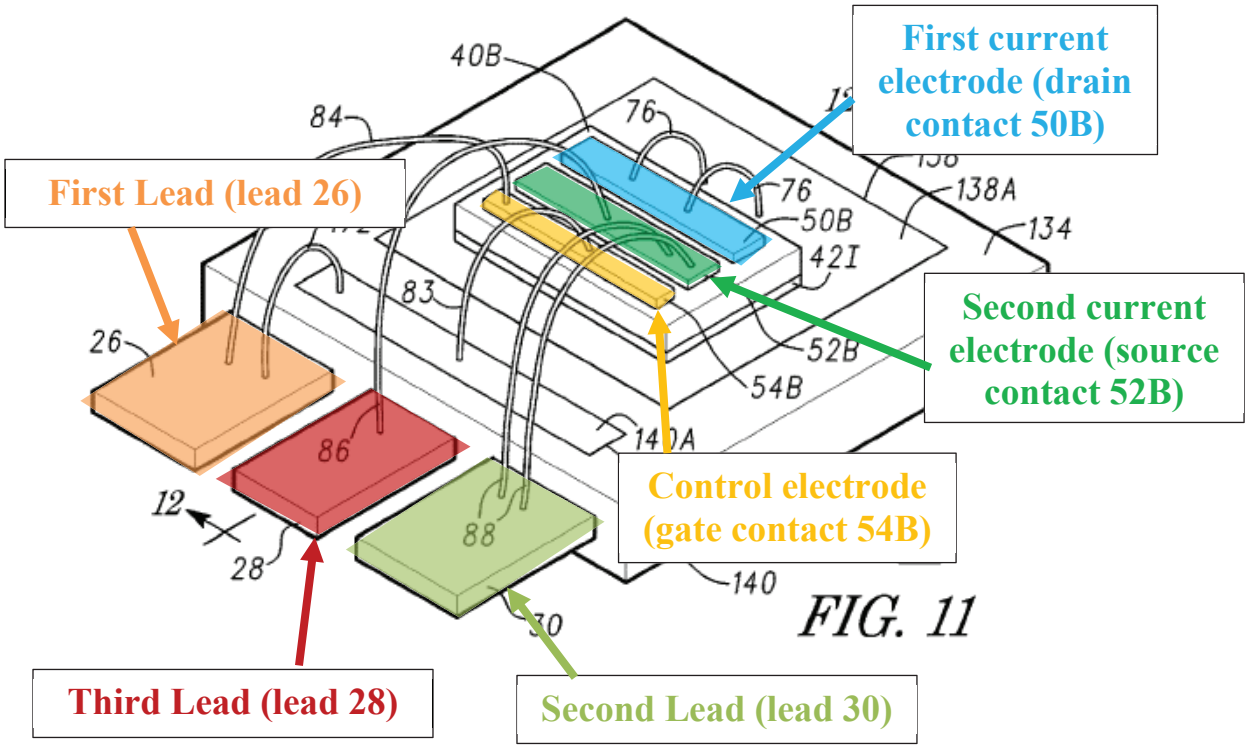


Otremba280, Fig. 4 (annotated).

F. Liu (US 10,930,524)

[078] Liu is a U.S. patent that issued on February 23, 2021. Liu, Cover. The corresponding provisional application was filed on July 24, 2015.

[079] Liu discloses a semiconductor device with leads coupled to various electrodes of a semiconductor chip. Liu, 8:27-33; Provisional, [00043].

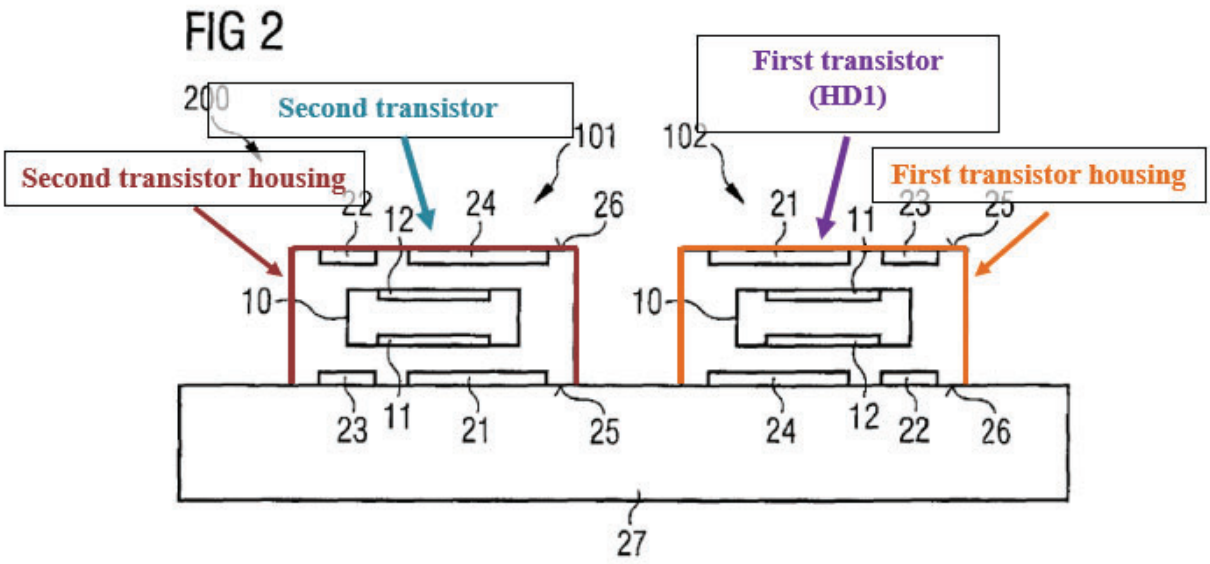


Liu, Fig. 11 (annotated); Provisional, Fig. 11.

G. Otremba631 (US 8,691,631)

[080] Otremba631 is a U.S. patent that issued on April 8, 2014. Otremba631, Cover. The corresponding application was published on July 12, 2012 and had been filed on March 20, 2012. Otremba631, Cover.

[081] Otremba631 discloses packaging two transistors in separate housings and mounting surfaces coupled to a common circuit board. Otremba631, Fig. 2.



Otremba631, Fig. 2 (annotated).

X. GROUNDS OF UNPATENTABILITY

[082] Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my opinion that claims 1-17 of the ’481 patent would have been obvious to one of ordinary skill in the art.

[083] In particular, it is my opinion that claims 1-17 of the ’481 patent would have been obvious to one of ordinary skill in the art, based on the grounds shown below:

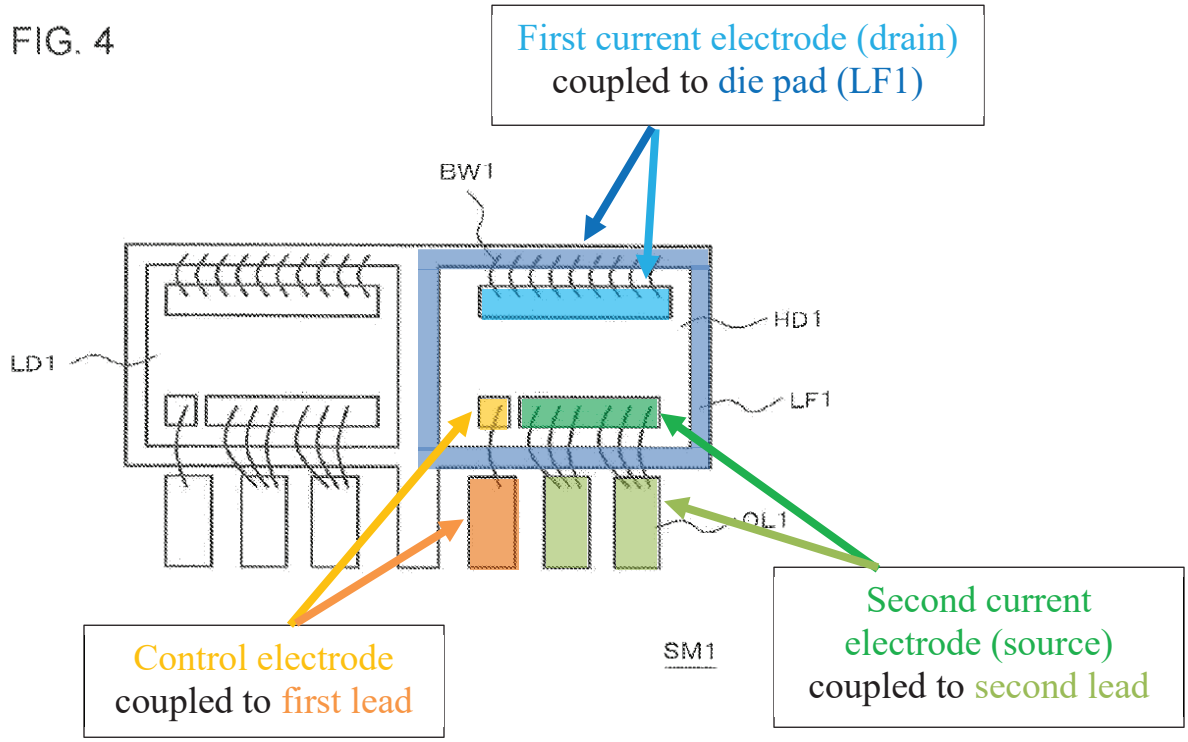
Grounds		Challenged Claims	Basis	Prior Art
Nega Grounds	**1A**	**1**-3, 5, 6, **10**, 11, and 16	§103	Nega in view of Roberts
	1B	4, 9, and **17**	§103	Nega in view of Roberts and Otremba124
	1C	4, 7, 8, and **17**	§103	Nega in view of Roberts and Otremba433
	1D	7 and 8	§103	Nega in view of Roberts, Otremba433, and Otremba280
	1E	12 and 13	§ 103	Nega in view of Roberts and Otremba631
	1F	14 and 15	§ 103	Nega in view of Roberts and Otremba280
Liu Grounds	**2A**	**1**, 2, and 4-6	§103	Liu
	2B	3 and **17**	§103	Liu in view of Roberts
	2C	4 and 9	§103	Liu in view of Otremba433
	2D	4 and 9	§103	Liu in view of Otremba124
	2E	7 and 8	§103	Liu in view of Otremba433 and Otremba280
	2F	**17**	§103	Liu in view of Roberts and Otremba433

XI. NEGA GROUNDS 1A-1F (CLAIMS 1-17)

[084] Claims 1-17 of the ’481 patent are unpatentable in view of the prior art. In particular, a person of ordinary skill would have found Nega in combination with Roberts, Otremba124, Otremba433, Otremba280, and/or Otremba631 renders all the challenged claims obvious.

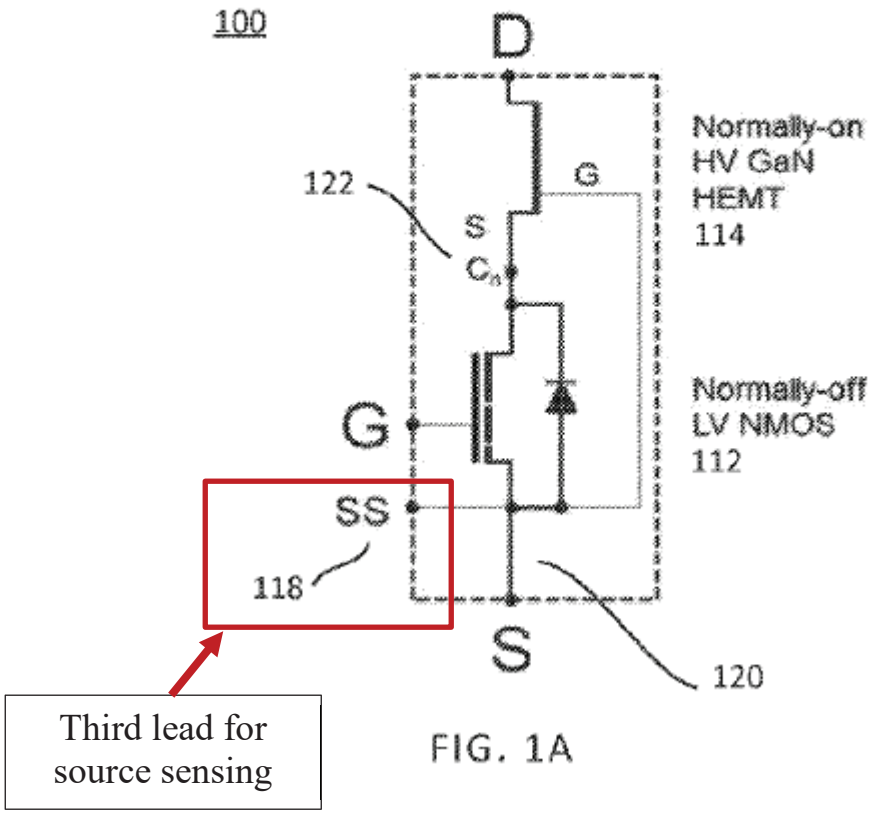
A. Overview of the Combinations

[085] **Nega** discloses all of claims 1, 2, 5, and 6 except a source sensing lead, which was obvious to include in Nega's device (as detailed below). Nega discloses "transistor HT1" where "one of the **source electrode SE1** and the **drain electrode DE1** is connected to the **lead frame LF1**, and the other thereof is connected to the **outer lead OL1**. In addition, the gate **electrode GE1** is connected to the **outer lead OL1**." Nega, [0095]. And Nega's "connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1." Nega, [0094].



Nega, Fig. 4 (annotated).

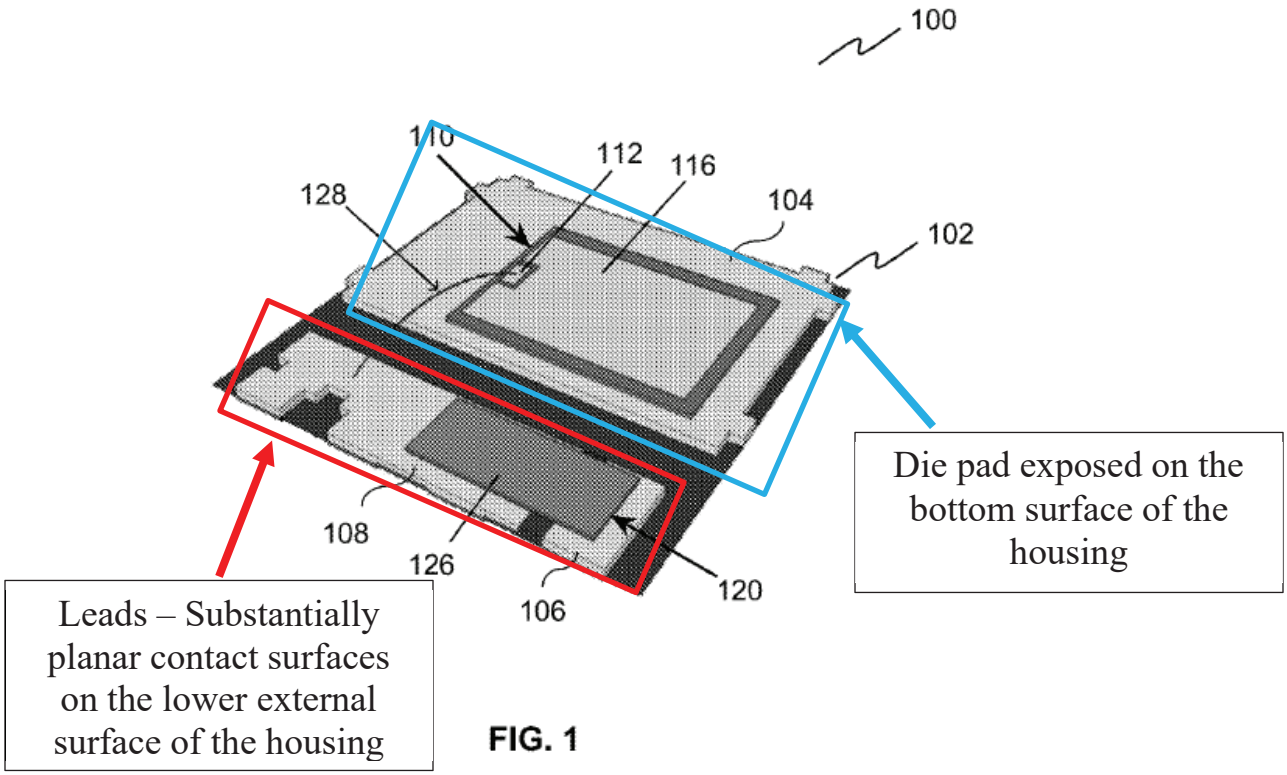
[086] **Roberts** discloses a source sensing lead (claim 1) and customary high voltage device blocking voltages and switching speeds (claims 3 and 17). Roberts discloses "a 'Kelvin Source Sense' or Kelvin connection SS … provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive L di/dt noise generated by the high current fluctuations of the source sense connection S." Roberts, [0056], Fig. 1A.



Roberts, Fig. 1A (annotated).

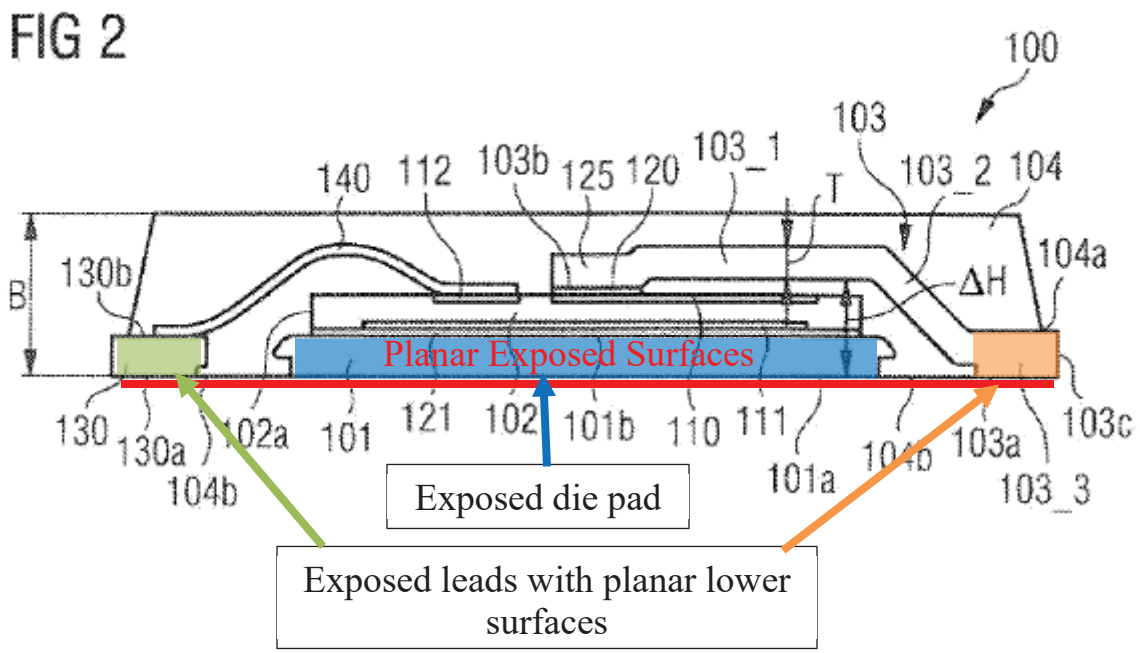
Roberts also discloses that transistor devices intended for high-voltage applications, "e.g.[,] 600/650V" in "normally-on (depletion mode) transistors," were well known at the time (Roberts, [0006], [0012]), and that GaN transistors "provide <20 ns switching time and more than 30 A current switching capability" (equating to more than 1kHz switching speed) (Roberts, [0008]).

[087] **<u>Otremba124</u>** discloses specific packaging requirements, like planar exposed leads and an exposed die pad (claims 4 and 17) in a ThinPAK8x8 design (claim 9). Otremba124 discloses a power transistor including a GaN high-electron-mobility-transistor (HEMT) "packaged in a[n] 8x8 ThinPAK." Otremba124, [0041]. Figure 1 shows the ThinPAK8x8 package outline with flat source leads 108 and 106 on the bottom of the package.



Otremba124, Fig. 1 (annotated).

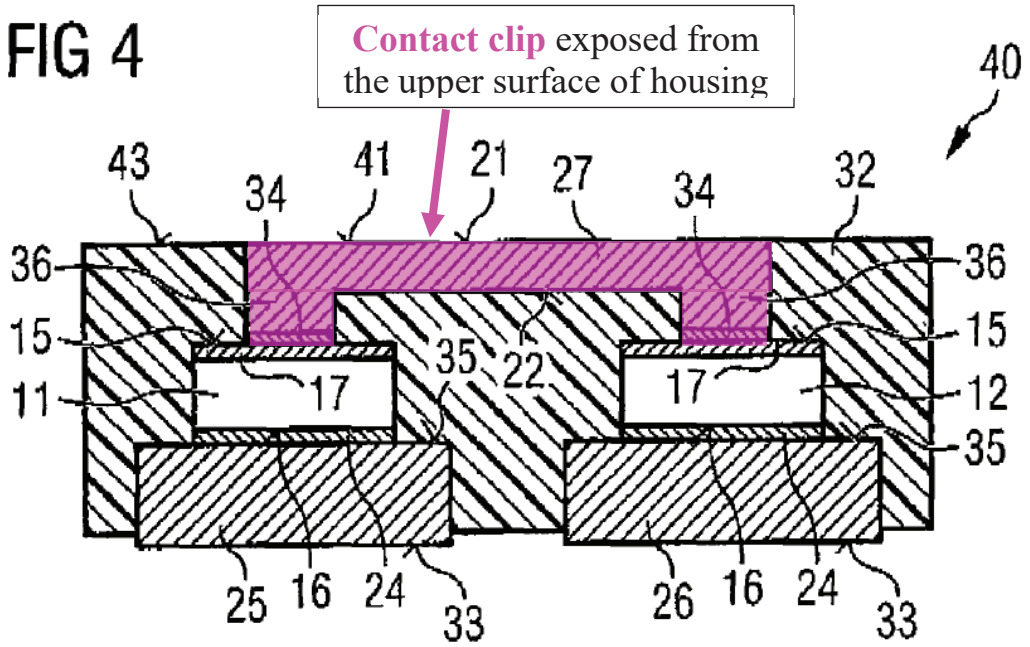
[088] **<u>Otremba433</u>** discloses planar exposed leads and an exposed die pad (claims 4 and 17) and connecting components using contact clips instead of bond wires (claims 7 and 8). Otremba433 discloses "external contact area[s]" 103a and 130a that are "coplanar with a reference plane defined by a bottom surface 101a of the carrier 101" (die pad) that is "exposed at the bottom of the package." Otremba433, [0037], [0039].



Otremba433, Fig. 2 (annotated).

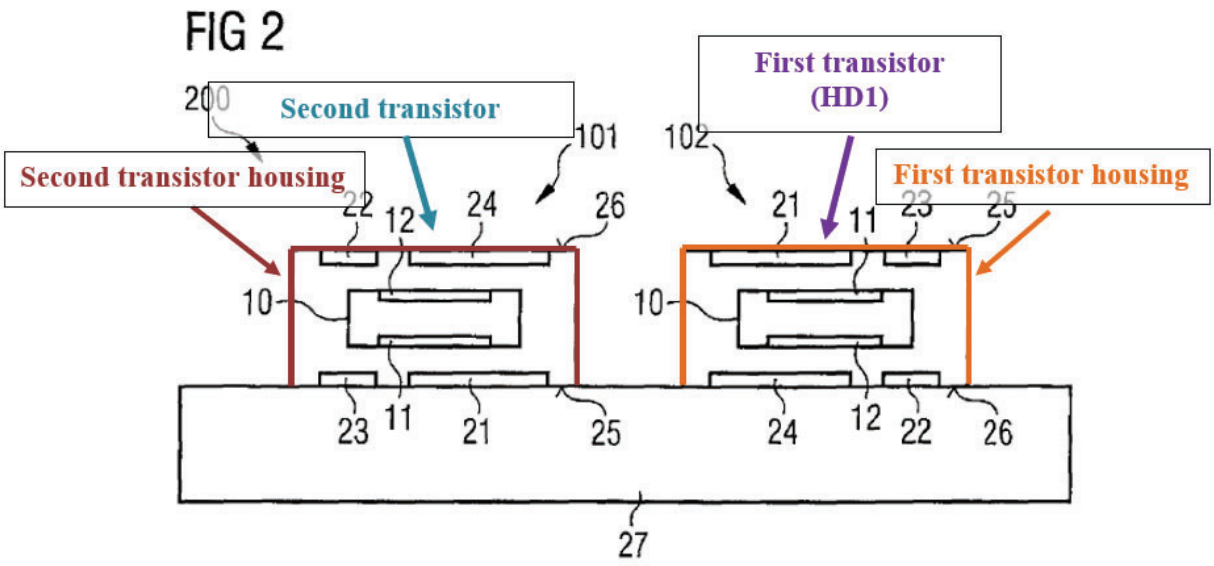
[089] Otremba433 also discloses coupling components with a "conventional contact clip" instead of bond wires. Otremba433, [0072].

[090] **<u>Otremba280</u>** discloses using exposed contact clips to couple components within a packaged device, rather than bond wires (claims 7 and 8). Otremba280's electronic component includes a "contact clip 14 [that] is exposed from the plastic encapsulation compound 32 [(housing)]." Otremba280, 8:33-41, Fig. 4.



Otremba280, Fig. 4 (annotated).

[091] **<u>Otremba631</u>** discloses a device with two mounting surfaces. Otremba631, Abstract. Otremba631 discloses packaging two transistors in separate housings and mounting surfaces coupled to a common circuit board. Otremba631, Fig, 2. Otremba631 states, "The first device 101 is mounted on the circuit board 27 with its first mounting surface 25 facing the circuit board 27. The second device 102 is mounted on the circuit board 27 with its second mounting surface 26 facing the circuit board 27." Otremba631, 4:64-67.



Otremba631, Fig. 2 (annotated).

[092] All references are analogous at least because they are in the same field of endeavor as the ’481 patent—packaging designs for semiconductor electronic components. *In re Bigio*, 381 F.3d 1320, 1325 (Fed. Cir. 2004).

B. Ground 1A: Nega in View of Roberts Renders Obvious Claims 1-3, 5, 6, 10, 11, and 16

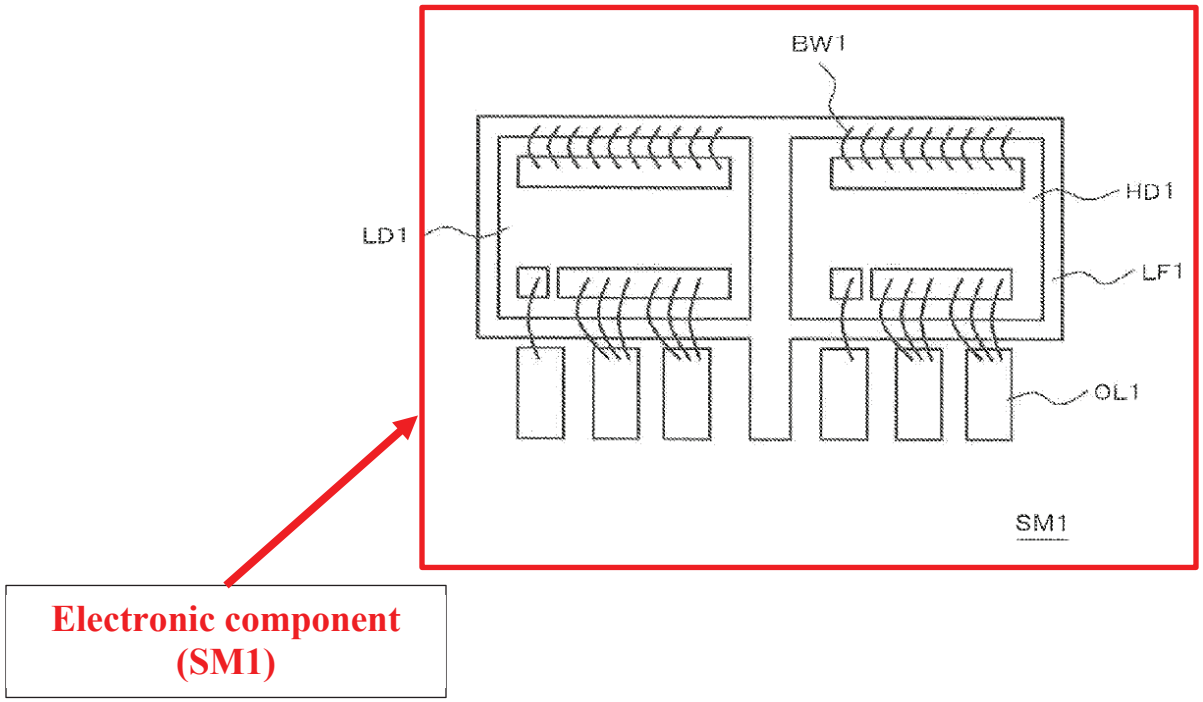
1. Claim 1

[093] In my opinion, Nega in combination with Roberts renders claim 1 obvious.

a. [1pre]: An electronic component, comprising:

[094] Nega discloses an electronic device described as a “semiconductor device SM1.” Nega, [0090], [0018].

FIG. 4



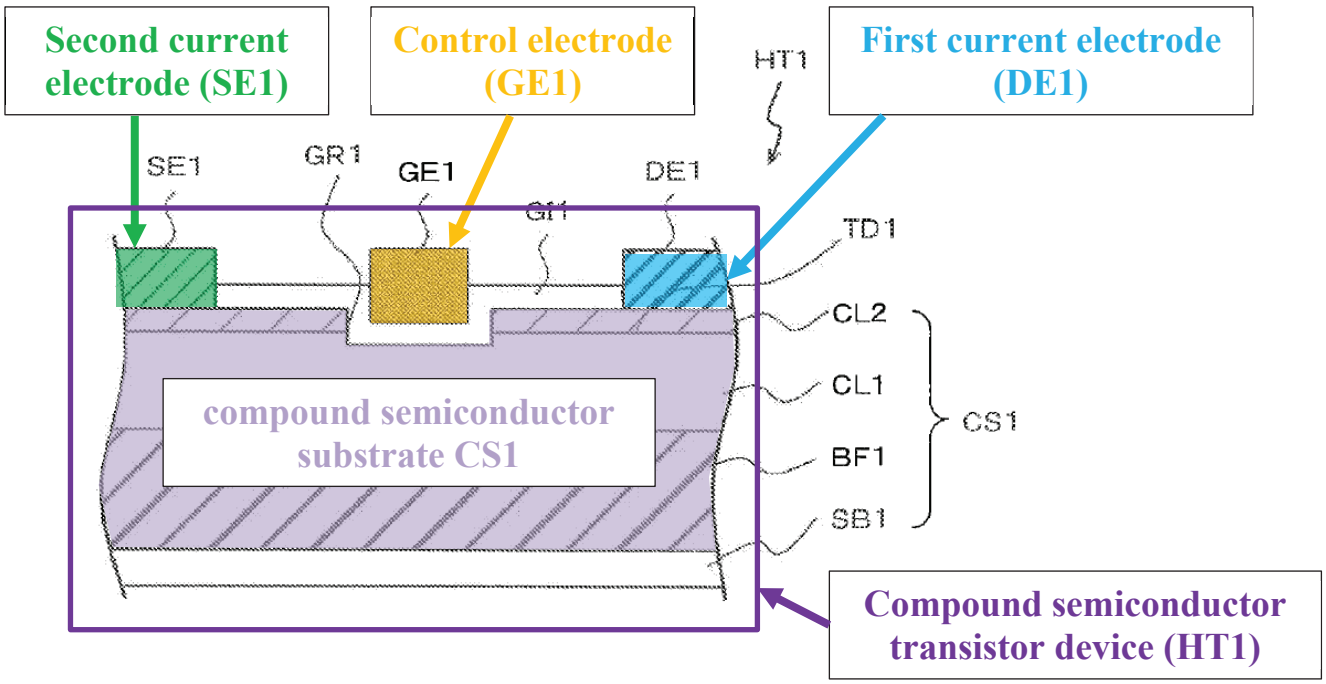
Nega, Fig. 4 (annotated).

b. [1a]: a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode;

[095] Nega discloses [1a]. Specifically, Nega discloses transistor HT1 (compound semiconductor transistor) (Nega, [0046]) with a drain electrode DE1 (first current electrode) (Nega, [0058]), a source electrode SE1 (second current electrode) (Nega), and gate electrode GE1 (control electrode) (Nega, [0056]). Nega explains that its HT1 transistor is a compound semiconductor transistor device because "HT1 is formed in the compound semiconductor substrate CS1 having the two-dimensional electron gas layer TD1" (Nega, [0034]), including a "compound

semiconductor layer CL1 [that] is, for example, a GaN layer" (Nega, [0049]) and a "compound semiconductor layer CL2 [that] is, for example, an AlGaN layer" (Nega, [0050]).

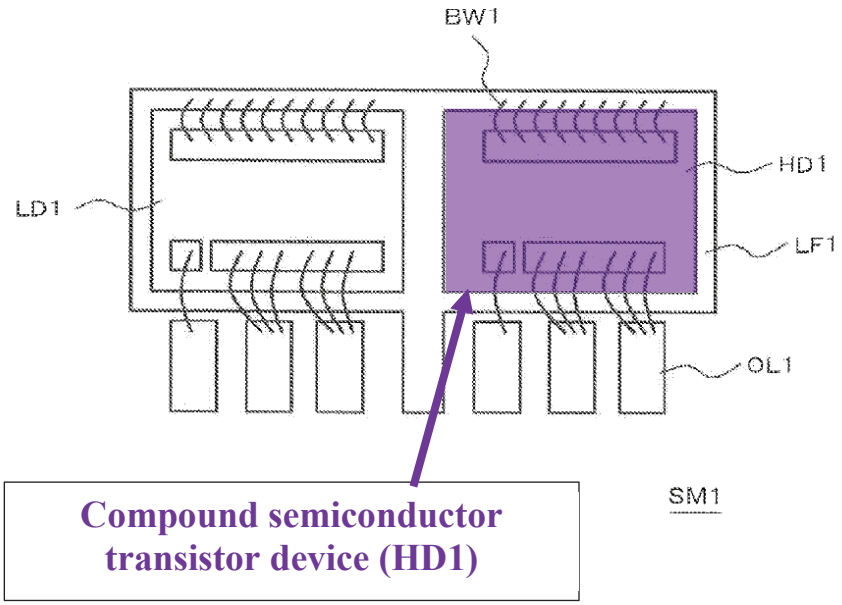
FIG. 2



Nega, Fig. 2 (annotated).

[096] HD1 in Figure 4 constitutes HT1. Nega, [0091], [0093].

FIG. 4



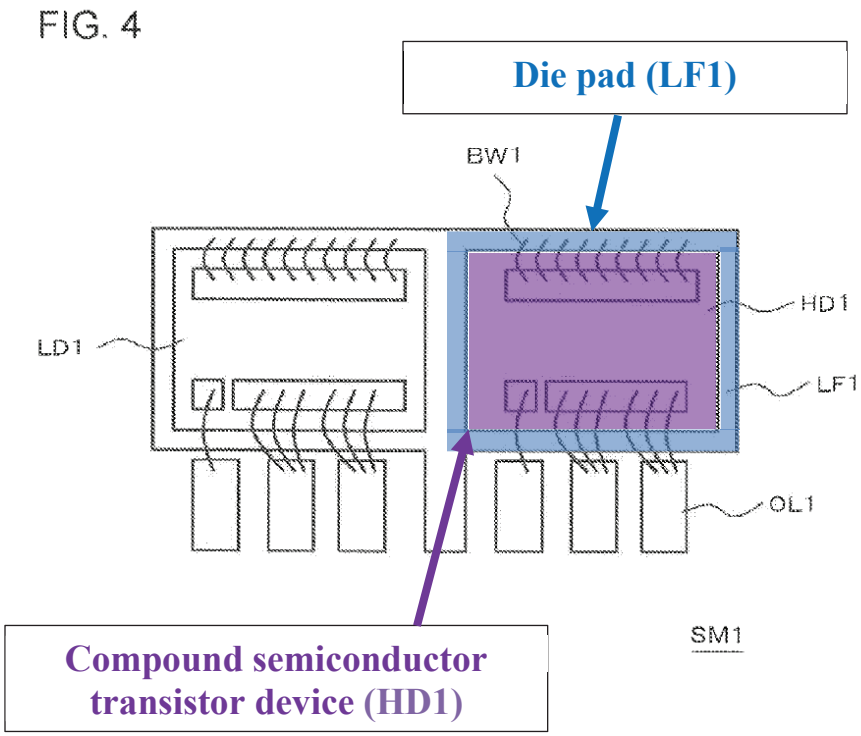
Nega, Fig. 4 (annotated).

c. [1b] a die pad; and

[097] Nega discloses [1b] because it discloses lead frame LF1 (die pad).

[098] A die pad is a common component of transistor devices generally comprising a conductive material that supports the die of the semiconductor device and is part of a lead frame. It is also commonly referred to as a die-attach pad, or generically as a lead frame (of which the die pad is a specific part).

[099] Nega's lead frame LF1 supports the active device (HD1 or compound semiconductor transistor device HT1 (Nega, [0095] ("HT1 constituting the high-side switching device HD1")) that is mounted thereon, and constitutes a die pad under Infineon's interpretation. Nega, [0091]-[0094].



Nega, Fig. 4 (annotated).

d. [1c] a first lead, a second lead and a third lead,

[1d] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

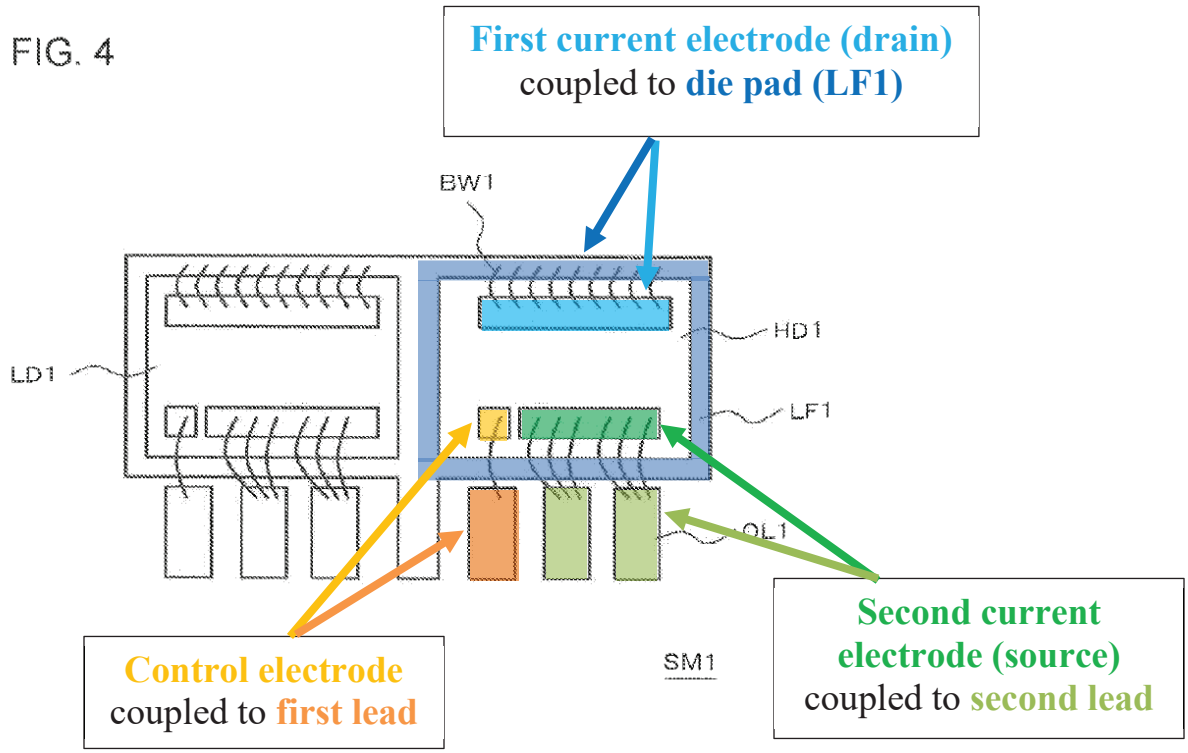
[1e] wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,

[0100] [1c]-[1e] collectively recite three leads, and various connections of components within the device to the die pad and the leads.

[0101] Nega's HT1 compound semiconductor transistor device discloses all but the third lead providing source sensing functionality—and Roberts

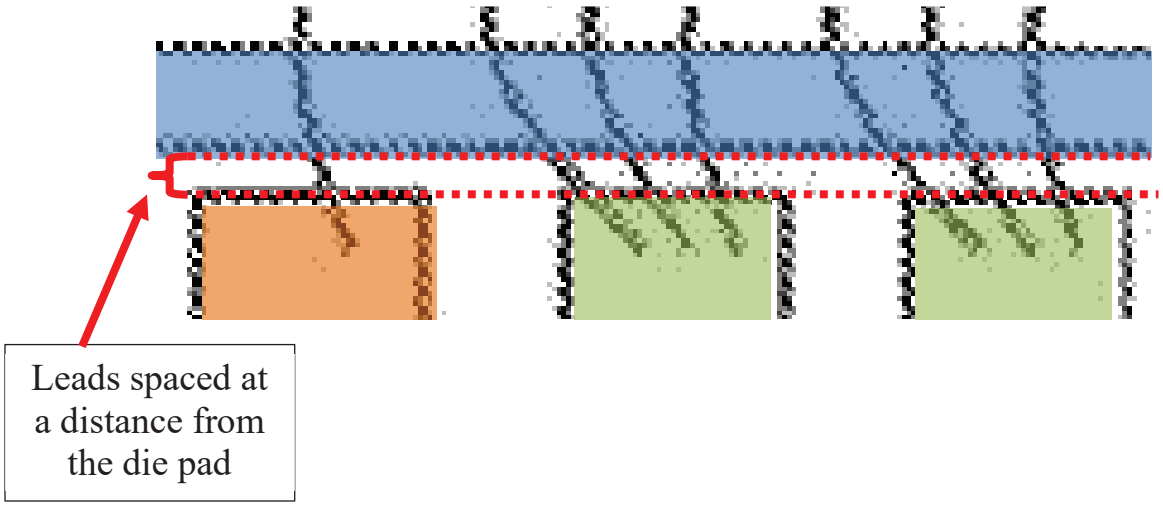
discloses implementing a third lead for source sensing functionality, as was commonly known in the art.

[0102] As explained for [1a], Nega's HT1 includes a drain electrode **DE1 (first current electrode)** (Nega, [0058]), a **source electrode SE1 (second current electrode)** (Nega), and **gate electrode GE1 (control electrode)** (Nega, [0056]). Nega's Figure 4, shows its HT1 (designated HD1, Nega, [0091], [0095], Fig. 4) with its electrodes coupled to various leads OL1 and LF1 (Nega, [0094]-[0095]). Nega explains: "In the transistor HT1 constituting the high-side switching device HD1, one of the **source electrode SE1** and the **drain electrode DE1** is connected to the **lead frame LF1**, and the other thereof is connected to the **outer lead OL1**. In addition, the gate **electrode GE1** is connected to the **outer lead OL1**." Nega, [0095]. And Nega's "connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1." Nega, [0094].



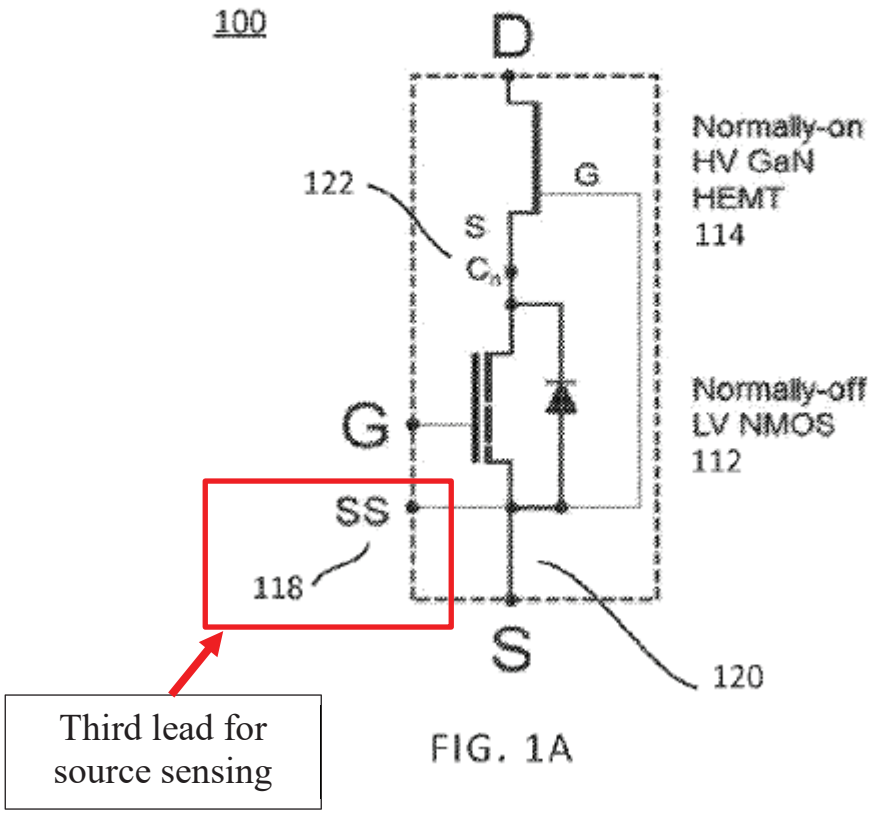
Nega, Fig. 4 (annotated).

[0103] Nega's first and second leads (OL1) are spaced a distance from the die pad (LF1) because, as shown in Figure 4, they are aligned separate from but adjacent to LF1, with a space separating OL1 and LF1 (white space below). Nega



Nega (excerpted, zoomed).

[0104] Nega does not expressly disclose using a source sensing third lead, but Roberts does, consistent with the common knowledge of a POSITA at the time. Roberts explains that in a "high voltage (HV) normally-on, depletion mode, GaN FET, which may comprise a GaN HEMT" (a compound semiconductor device like that of Nega), "a 'Kelvin Source Sense' or Kelvin connection SS is provided to enable an external driver device to more cleanly drive the intrinsic source, free of inductive L di/dt noise generated by the high current fluctuations of the source [sense] connection S." Roberts, [0055]-[0056], Fig. 1A.

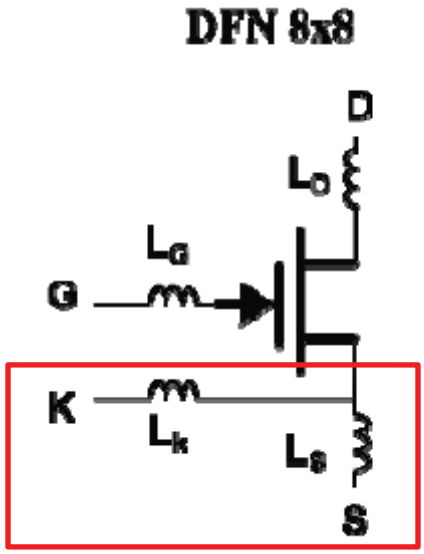


Roberts, Fig. 1A (annotated).

[0105] As recognized by Roberts, transients can be so high as to "result in unwanted switching," so, as Roberts expressly teaches, suggests, and motivates, "it is desirable to provide a driver circuit that provides monitoring and control of noise and transients" by using a Kelvin Source Sense connection. Roberts, [0056]-[0057]. This benefit of using a Kelvin Source Sense connection was well-known in the art at the time, as evidenced by Lind and Huang.

[0106] Lind explains that implementing a Source Sense connection allows for measurement and monitoring at a close to constant di/dt, without any noise—the benefit expressly recognized by Roberts. Ex-1013, 3; Roberts, [0056].

[0107] Huang explains that in GaN devices with high switching speeds, "common source inductance and inter-connected inductance are detrimental to switching loss and gate reliability," and thus, using a package with a Kelvin (source sensing) connection "decouple[s] the power loop and driving loop" to "minimize the common source inductance." Ex-1024, 2. Further, Huang describes that "[t]he switching speed of GaN devices is much faster than comparable Si MOSFET which makes the packaging even more critical to achieve lower loss and less ringing during switching transition." Ex-1024, 2.



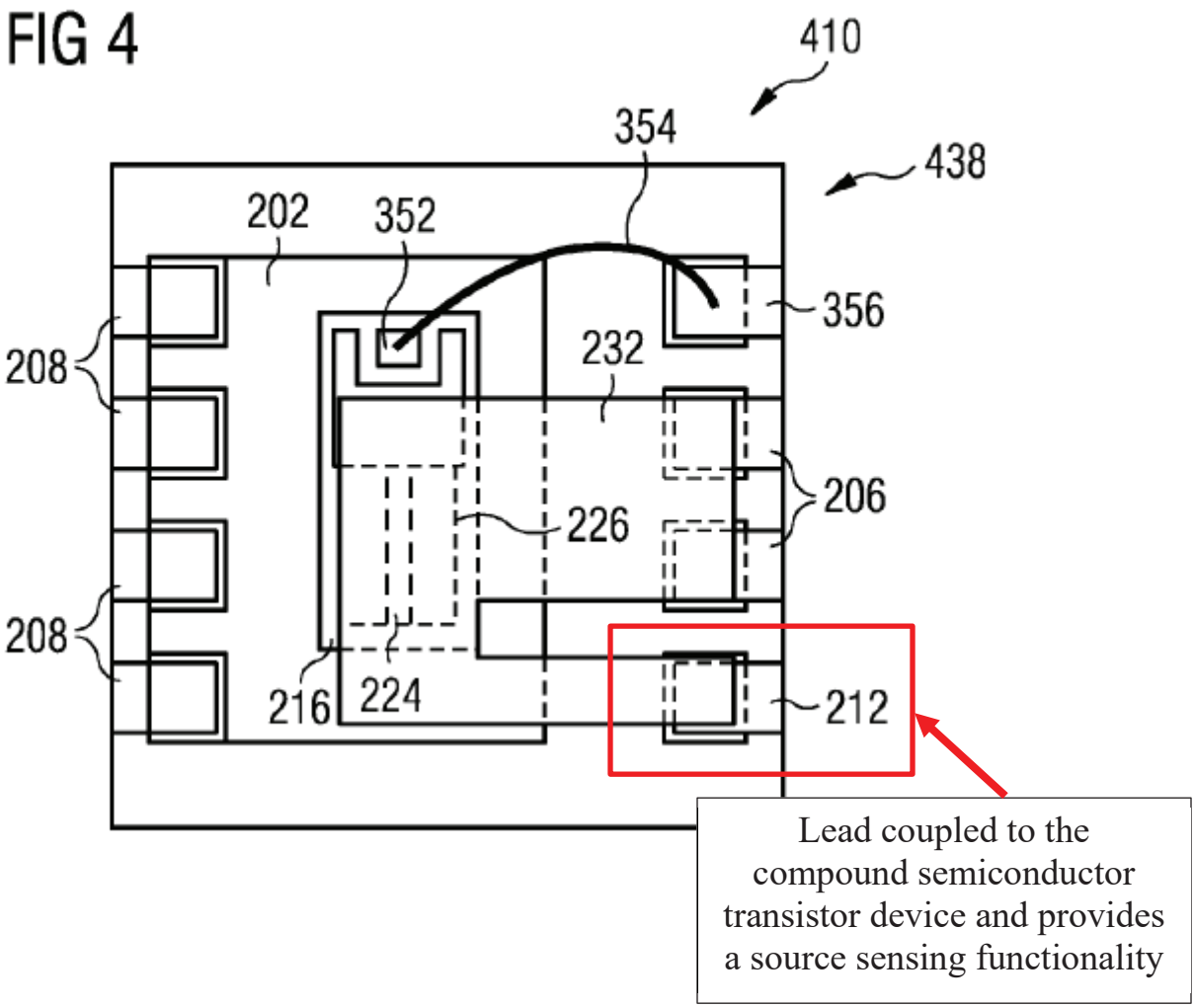
Ex-1024, Fig. 2 (annotated).

[0108] In Roberts, a Kelvin Source Sense connection SS is provided by "separate Kelvin connection(s)" (Roberts, [0095]), which could be routinely implemented in Nega's device by simply adding an additional external connection or contact pad connected to the transistor, for source sensing functionality, as further evidenced by Huang, McKnight, and Otremba528. Huang shows a separate Kelvin lead implemented in a DFN8x8 package. Ex-1024, 2, Fig. 2. Huang also explains that "[w]ith Kelvin connection, the DFN package is able to decouple the power loop and driving loop, and therefore it can minimize the common source inductance". Ex-1024, 2. A POSITA would have known that a DFN8x8 package is a type of leadless package. Further, Huang states that "DFN packages are typically used for high voltage e-mode GaN devices" such as the device disclosed by Nega. Ex-1024, at 2. And a POSITA would have been motivated to implement a Kelvin lead in Nega's device because implementing a lead in GaN packaging was known at the time.

[0109] McKnight, like Roberts, expressly discloses that in lateral GaN transistor devices, the package includes "an additional external contact pad, e.g.[,] a source sense (Kelvin) connection." McKnight, 12:20-27.

[0110] Otremba528 expressly recognizes, in its background section, that a "source-sensing lead may be connected to a source contact to measure and/or monitor the potential of the source contact" (Otremba528, [0002])—the same

purpose as the Kelvin Source Sense connection in Roberts added as a separate lead as shown below in Figure 4 from Otremba528.



Otremba528, Fig. 4 (annotated).

[0111] In my opinion, a POSITA would, therefore, have been motivated to implement Robert's source sensing connection as a separate connection, lead, or contact pad (third lead) in Nega's device, and would have expected success in doing so because source sensing functionality had known

benefits and implementing source sensing functionality as a separate lead was known in the art. The combination is no more than combining prior art elements according to known techniques to a known device ready for improvement to yield predicable results.

[0112] In addition, Roberts also discloses packaging compound semiconductor transistor devices. Roberts discloses "a system . . . comprising an assembly of a GaN die comprising a normally-on GaN HEMT, a CMOS die comprising an integrated driver MOSFET, another CMOS die comprising an interface circuit and packaging elements. Roberts, [0051]. Element 622 in Figure 7, shown below, represents these packaging elements.

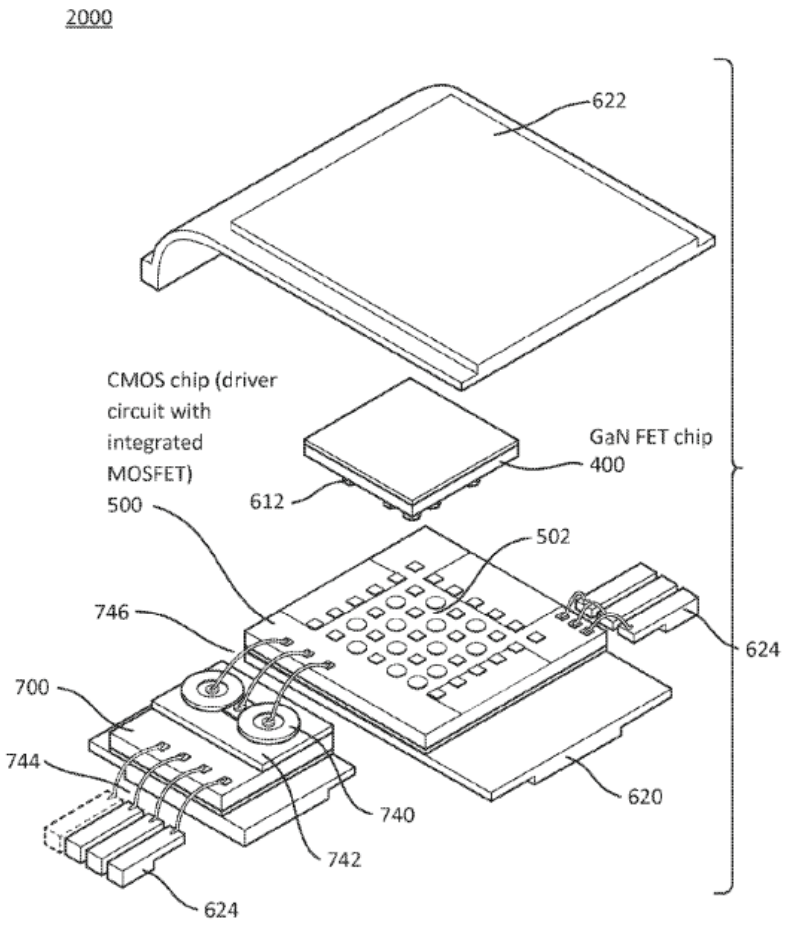


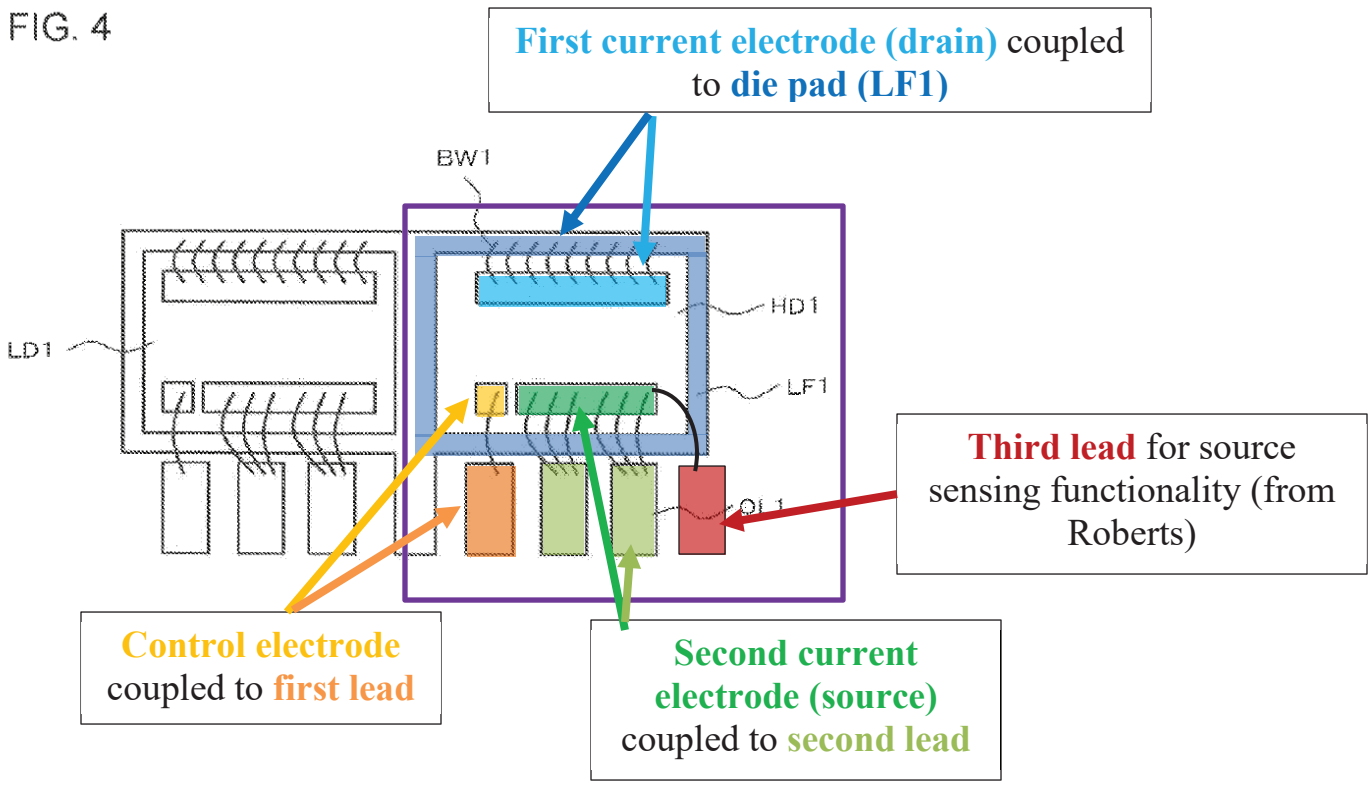
FIG. 7

Roberts, Figure 7.

[0113] Therefore, it would have been obvious to a POSITA to implement Robert's source sensing connection in Nega's device because both references disclose packaging for compound semiconductor transistor devices.

[0114] As combined, Nega-Roberts teaches and suggests the following configuration, with the control electrode coupled to the first lead (Nega), the first current electrode coupled to the die pad (Nega), the second current electrode

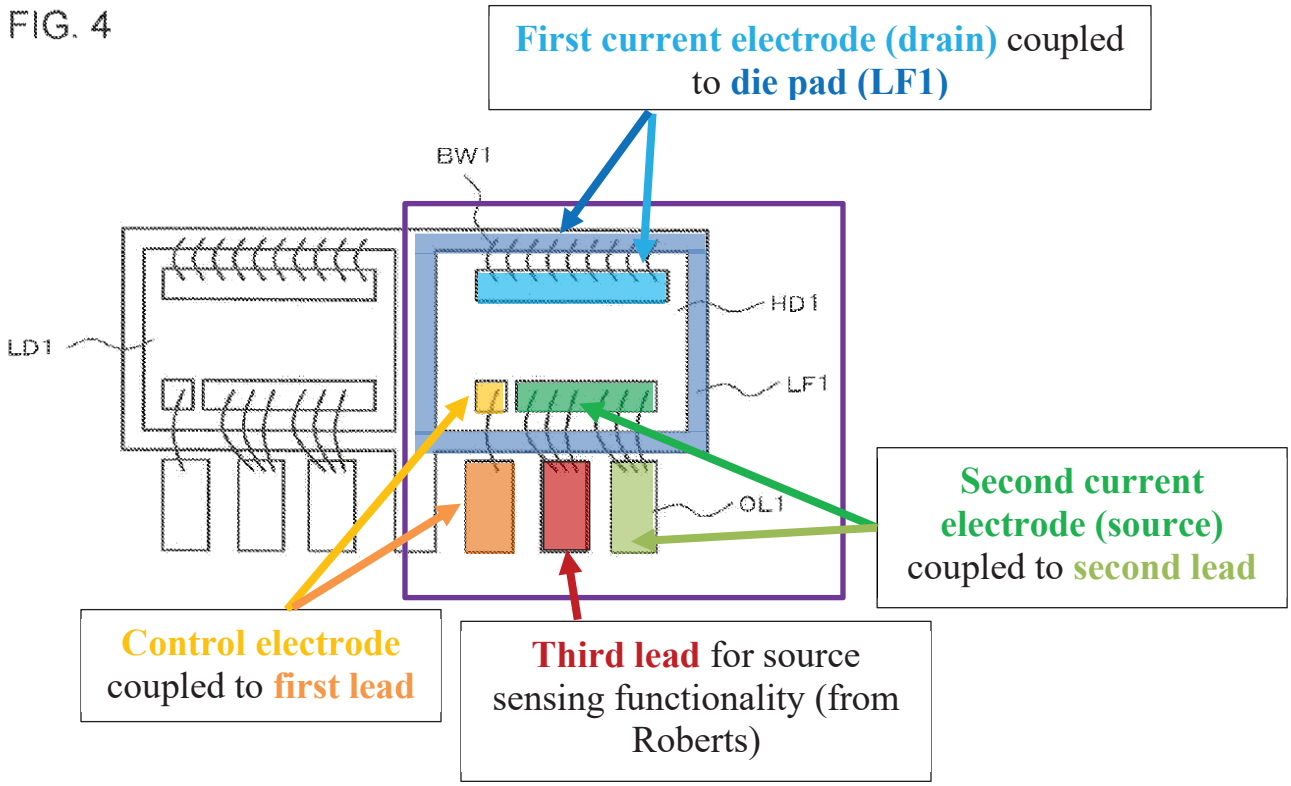
coupled to the second lead (Nega), and the third lead coupled to the compound semiconductor transistor device and providing a source sensing functionality (Roberts).



Nega, Fig. 4 (annotated and modified by Roberts to add source sensing third lead).

[0115] Alternatively, Nega already discloses two leads connected to the source electrode. In my opinion, a POSITA would have understood that one of these lead structures, already shown coupled to the source electrode, would readily be modified to serve as a lead for source sensing functionality, as taught by Roberts, because altering lead connections within a device was commonplace requiring only ordinary skill. It was known at the time to use leads in packaging

structures to meet the needs of a particular application (for example, interchanging the source and drain leads, as Nega teaches (Nega, [0095])). In my opinion, a POSITA would therefore have understood that leads could simply be repurposed as a design choice within the skill of a POSITA, and with a reasonable expectation of success.



Nega, Fig. 4 (annotated).

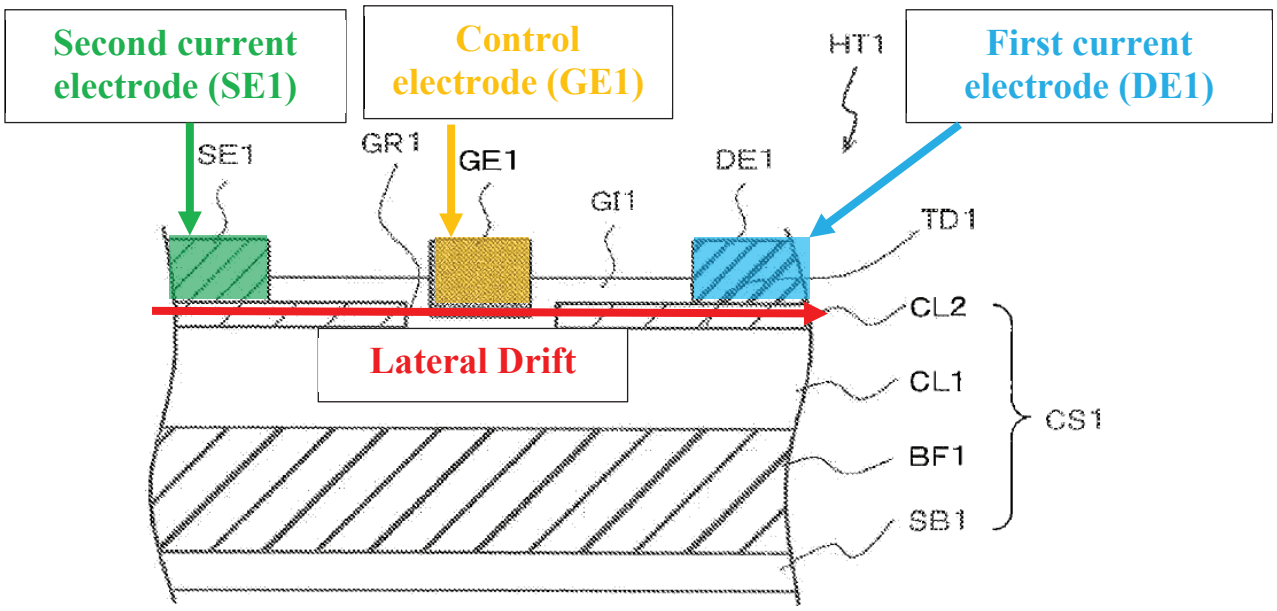
e. **[1f] wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a**

source of the compound semiconductor transistor device is coupled to the die pad,

[0116] Nega discloses [1f] because its transistor device HT1 is arranged laterally, with the gate, source, and drain side-by-side on the same lateral plane in a lateral drift path, and either of its source or drain is coupled to the lead frame LF1 (die pad).

[0117] The ’481 patent explains that “lateral” means “run[ning] generally parallel to the lateral extent of a semiconductor material or semiconductor carrier” (Ex-1001, 3:14-18) and describes a device that “has a lateral drift path” (Ex-1001, 4:37-38). Nega’s source, drain, and gate are spread laterally across the semiconductor material and thus create a lateral drift path, as opposed to being stacked on top of one another in a vertical configuration.

FIG. 2



Nega, Fig. 2 (annotated).

[0118] As explained for [1b], Nega's lead frame LF1 is the claimed die pad. Nega discloses that one of its source or drain is coupled to lead frame LF1 (die pad). Nega states: "The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1." Nega, [0094].

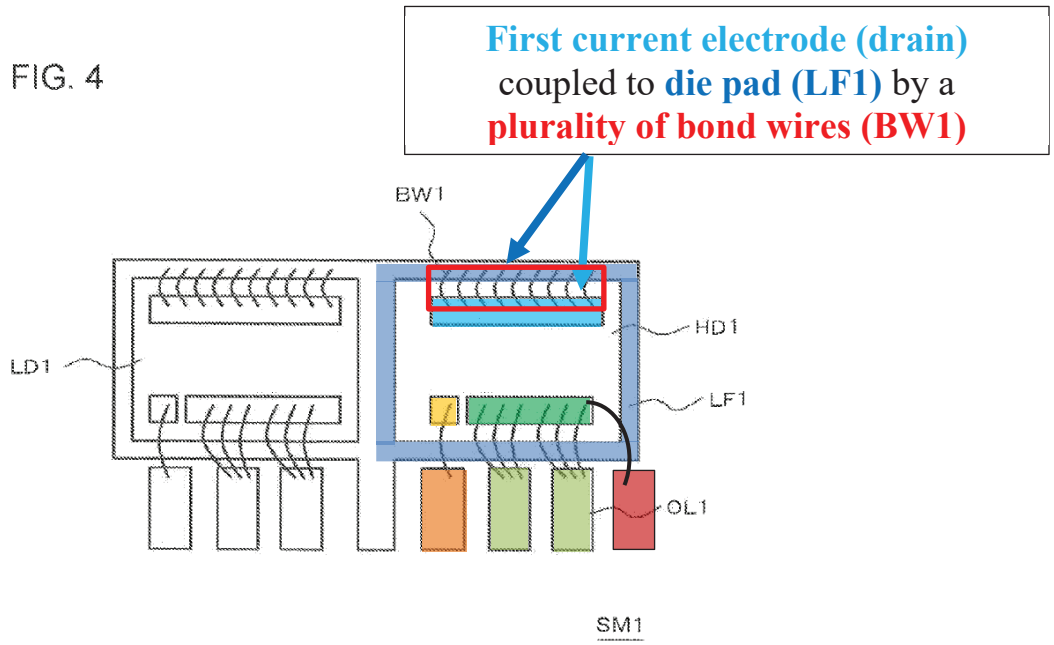
f. [1g] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

[0119] Nega discloses [1g] because, as explained for [1f], the drain electrode (first current electrode) is coupled to lead frame LF1 (die pad) by a plurality of bond wires.

[0120] As explained for [1a], Nega discloses a drain electrode (first current electrode).

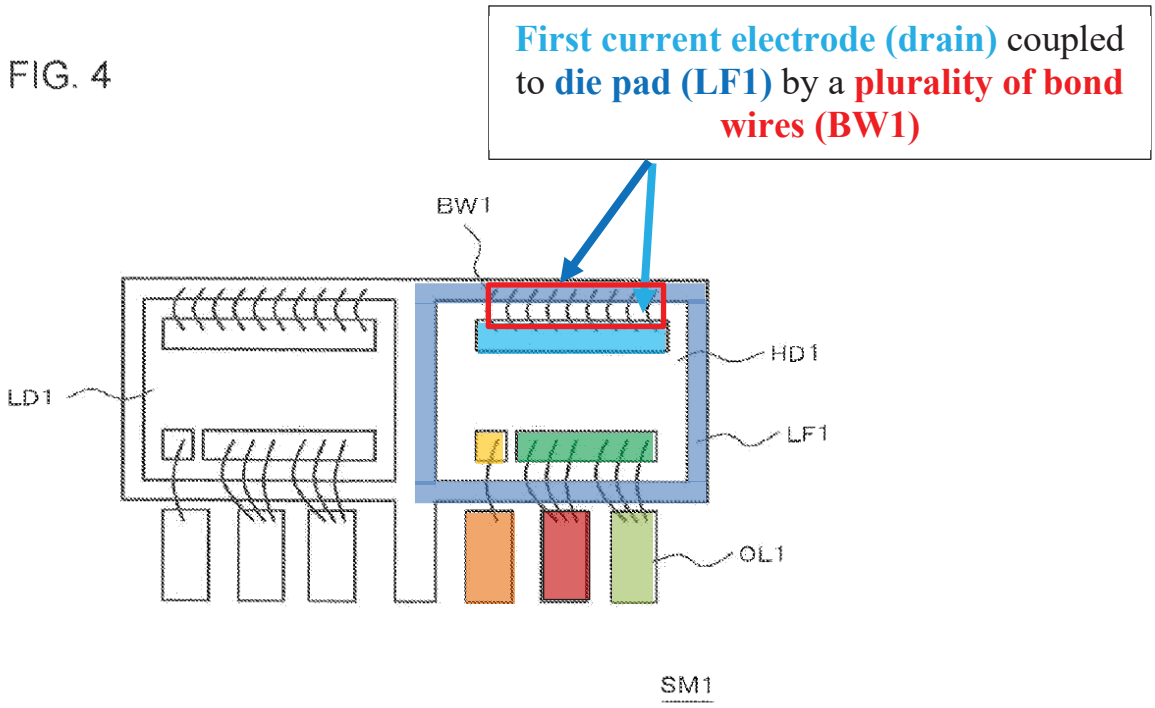
[0121] As explained for [1b], Nega discloses a lead frame LF1 (die pad).

[0122] As explained for [1e]-[1f], Nega's drain electrode DE1 (first current electrode) is coupled to the lead frame LF1 (die pad) by a plurality of bond wires. Nega states: "The connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1." Nega, [0094]. As depicted in Figure 4, Nega's drain is connected to lead frame LF1 by a **plurality of bond wires**—nine shown. Nega, Fig. 4.



Nega (annotated and modified).

[0123] Alternatively, repurposing one of Nega's source leads as a source sensing lead:

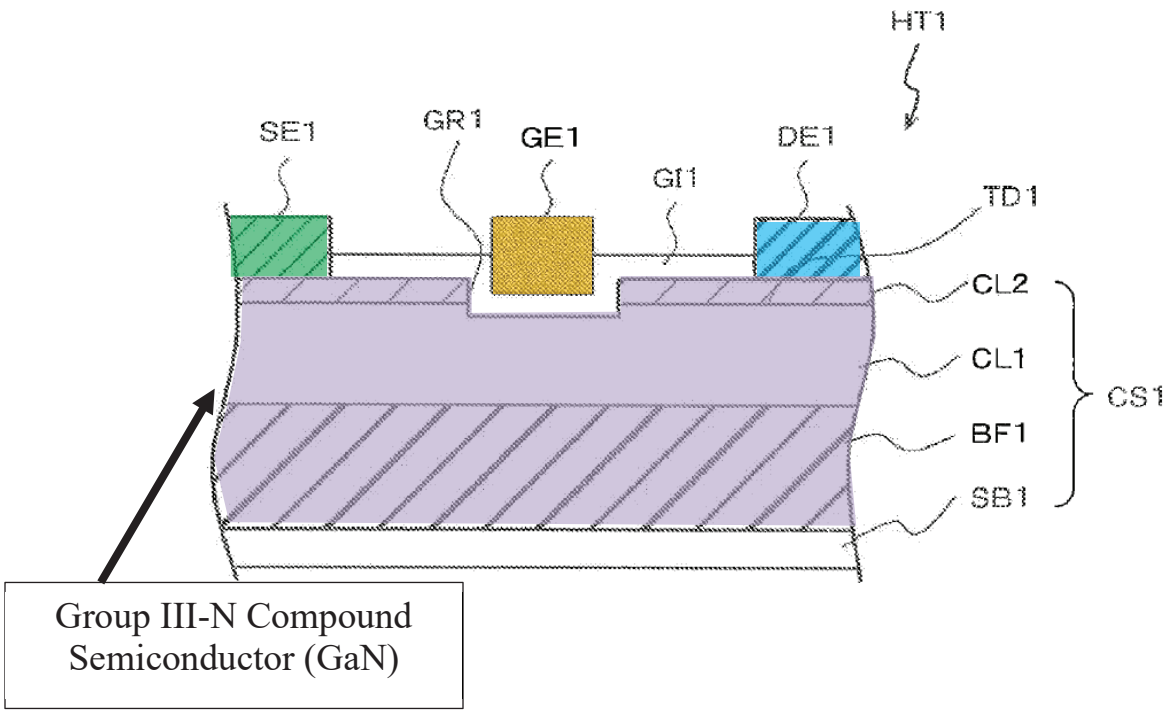


Nega (annotated).

2. Claim 2 - The electronic component of claim 1, wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device.

[0124] Nega discloses claim 2. The ’481 patent explains that “Group III-N semiconductor devices” include “gallium nitride (GaN)” devices. Ex-1001, 1:21-25. The ’481 patent also discloses that the “compound semiconductor transistor device . . . is [a] silicon carbide-based compound semiconductor transistor device.” Ex-1001, 6:3-6. Nega discloses a Group III-N device because it discloses that its transistor device HT1 includes “**compound semiconductor substrate CS1**” (Nega, [0034]), including a “compound semiconductor layer CL1 [that] is, for example, a GaN layer” (Nega, [0049]) and a “compound semiconductor layer CL2 [that] is, for example, an AlGaN layer” (Nega, [0050]).

FIG. 2



Nega, Fig. 2 (annotated).

3. Claim 3 - The electronic component of claim 1, wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

[0125] Nega in view of Roberts renders claim 3 obvious. Claim 3 requires the device to have a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz. It is my opinion that a POSITA would have understood that Nega's compound semiconductor device would have achieved these characteristics, which were common for compound semiconductor

power conversion transistors designed for high voltage applications, as explained expressly by Roberts.

[0126] The ’481 patent explains that a transistor device’s blocking voltage capability is its capability to block a voltage when the transistor is off. Ex-1001, 3:41-50. For high voltage applications, like those in claim 3, the device would block at least 400V or even higher, up to 1200V. Ex-1001. In other words, it is the maximum voltage that can be applied to a transistor while preserving intended operation. Blocking voltage capability is also commonly referred to as the breakdown voltage because it is the maximum voltage that can be applied before the operation of the transistor breaks down. Claim 3, therefore, is simply reciting a transistor intended for use in a high voltage application.

[0127] Roberts includes a “Background Art” section that notes that high voltage (e.g., high blocking voltage capability) transistors were common in the art. Roberts explains that transistor devices intended for high voltage applications, “e.g.[,] 600/650V” in “normally-on (depletion mode) transistors,” were well known at the time. Roberts, [0006], [0012].

[0128] Although Nega does not expressly disclose its device’s switching frequency capability, switching frequency capabilities of at least 100 kHz were common in the art, particularly for compound semiconductor devices (like Nega), as Roberts discloses. Roberts, in its “Background Art” section,

explains that GaN transistors "provide <20 ns switching time and more than 30 A current switching capability." Roberts, [0008]. From a switching time in nanoseconds, the corresponding switching frequency is determined by the following formula: Hz = 1/(ns/(1*10^9). Applying this routine formula, a switching time of 20 ns corresponds to 50 MHz—much greater than 100 kHz.

[0129] A POSITA would have understood that a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz were standard, routine, and readily-achievable characteristics for compound semiconductor transistors designed for high voltage applications (like Nega) at the time of the '481 patent. Indeed, higher blocking voltage capability and faster switching frequencies were some of the very benefits boasted by compound semiconductor devices generally, as opposed to traditional Si-based devices. GaN devices specifically were known for their high-frequency amplifying electronic applications and were suitable for high-power switching. Ex-1022, at 20 ("GaN has many attractive material properties, such as high break-down field, good bulk electron mobility, and thermal conductivity, which make it suitable for high-power switching as well as high-frequency amplifying electronic applications."); Ex-1024, 2 ("The switching speed of GaN devices is much faster than comparable Si MOSFET which makes the packaging even more critical to achieve lower loss and less ringing during switching transition.").

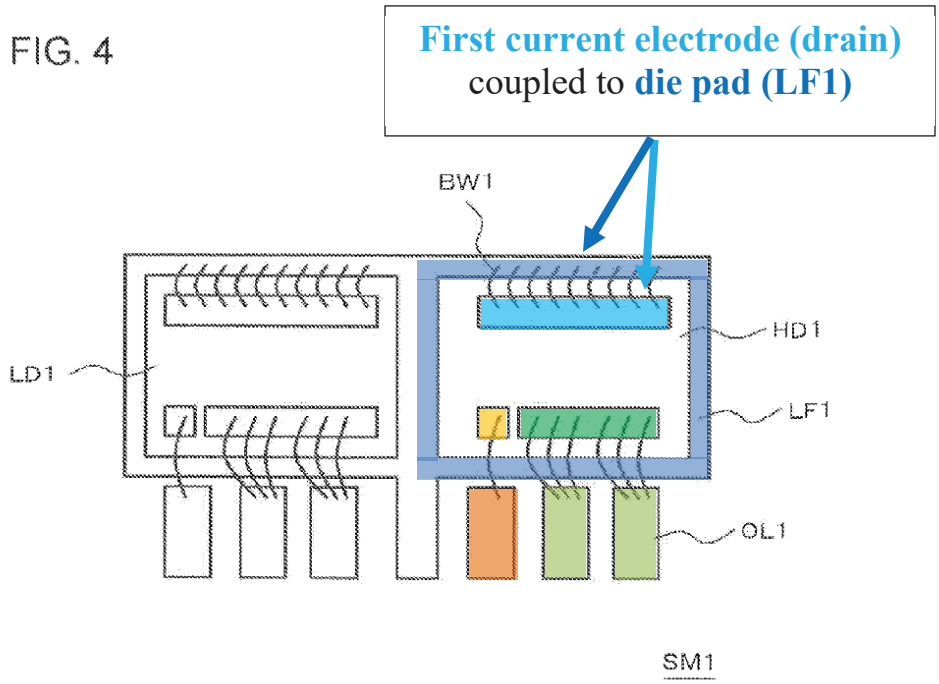
[0130] Because Nega expressly discloses compound semiconductor transistor devices, but is silent on the corresponding switching time or frequency, it is my opinion that a POSITA would have been motivated to look to references that disclose expected switching time or frequencies for other compound semiconductor devices, including high voltage application GaN transistor devices like in Roberts. In my opinion, a POSITA would have looked to references like Roberts "to better understand or interpret" the achievable characteristics of Nega's compound semiconductor transistor device, including the switching time and frequency. And, because these characteristics were common, well-known, and readily achievable in compound semiconductor transistor devices at the time, it is my opinion that a POSITA would have had a reasonable expectation of success in operating Nega's compound semiconductor transistor device with a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz.

4. Claim 5 - The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad.

[0131] Claim 5 directly contradicts the requirement in claim 1 that the compound semiconductor device is a lateral transistor (not a vertical transistor). I understand that the applicant expressly disclaimed claim scope comprising vertical

transistors during prosecution. *E.g.*, Ex-1002, 31-32 (Sept. 19, 2017, Response to Office Action, amending claim 1 to recite a "**lateral transistor device**" to overcome a rejection over "Otremba '284[, which] teaches a **vertical** transistor" (emphases in original)).

[0132] To the extent claim 5 is interpreted as requiring a **lateral transistor** (consistent with claim 1) where the drain of the device is coupled to the die pad, Nega discloses it for the reasons explained for [1e]. Nega explains that "[i]n the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the **drain electrode DE1** is connected to the **lead frame LF1**, and the other thereof is connected to the outer lead OL1. In addition, the gate electrode GE1 is connected to the outer lead OL1." Nega, [0095].



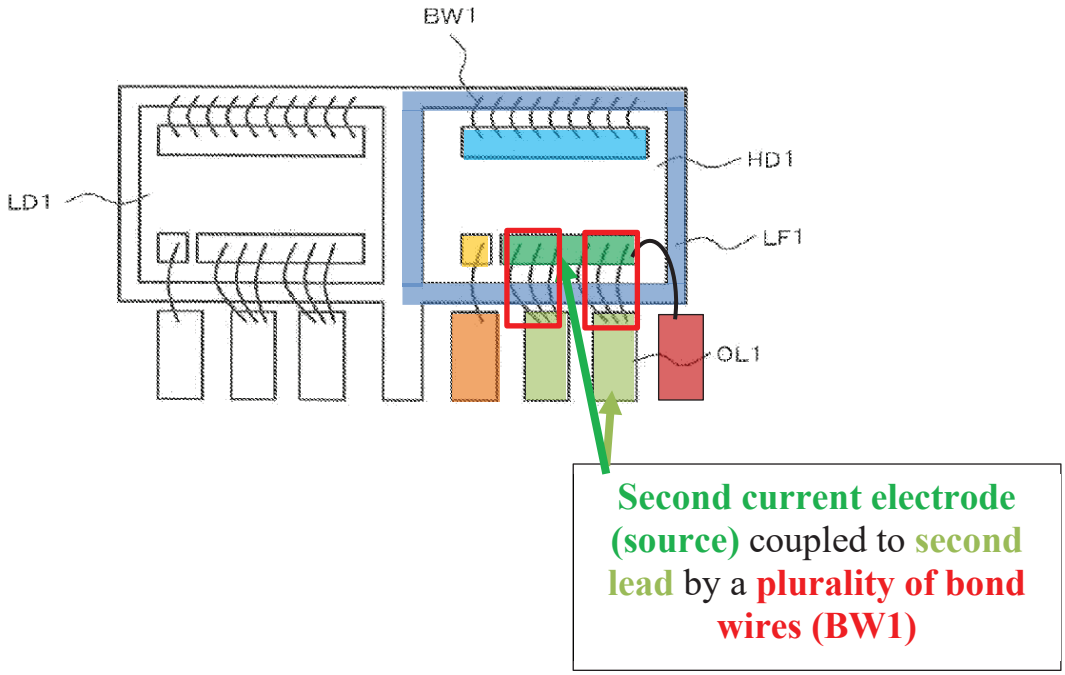
Nega, Fig. 4 (annotated).

5. Claim 6 - The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.

[0133] Nega discloses claim 6 because its source electrode (second current electrode) is coupled to second lead OL1 by a plurality of bond wires BW1.

[0134] As explained for [1e], Nega's Figure 4 shows that, "[i]n the transistor HT1 constituting the high-side switching device HD1, one of the **source electrode SE1** and the **drain electrode DE1** is connected to the **lead frame LF1**, and the other thereof is connected to the **outer lead OL1**. In addition, the gate **electrode GE1** is connected to the **outer lead OL1**." Nega, [0095]. And Nega's "connection of each electrode to the lead frame LF1 or an outer lead OL1 is performed as follows using, for example, a bonding wire BW1." Nega, [0094]. Figure 4 shows a plurality of bond wires connecting the **source electrode SE1** to **outer lead OL1**—three bond wires for each lead.

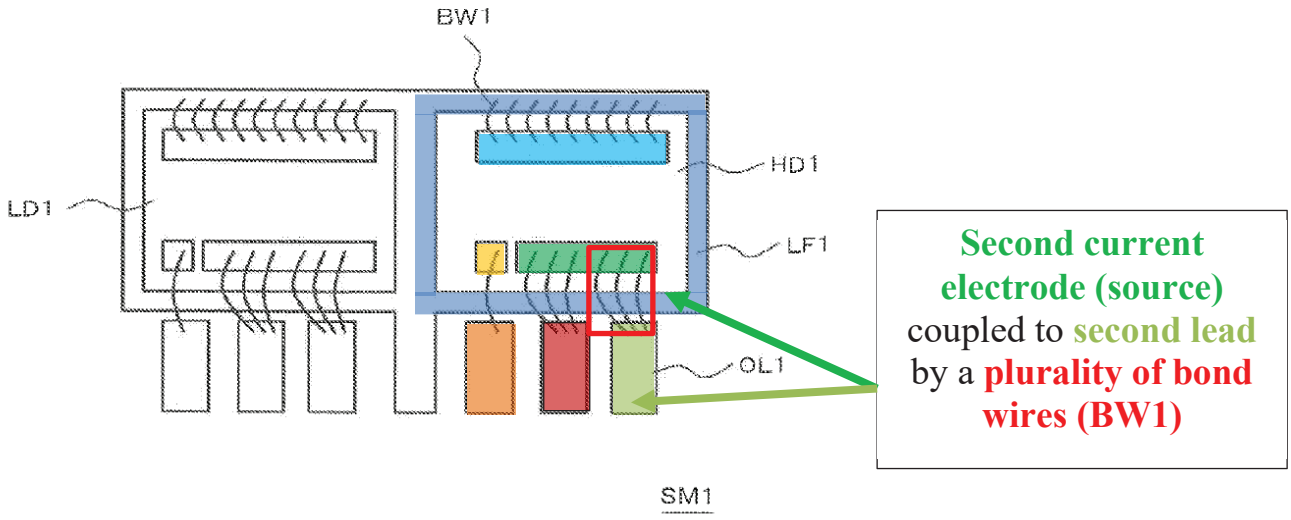
FIG. 4



Nega, Fig. 4 (annotated and modified).

[0135] Alternatively, repurposing one of Nega's source leads as a source sensing lead:

FIG. 4

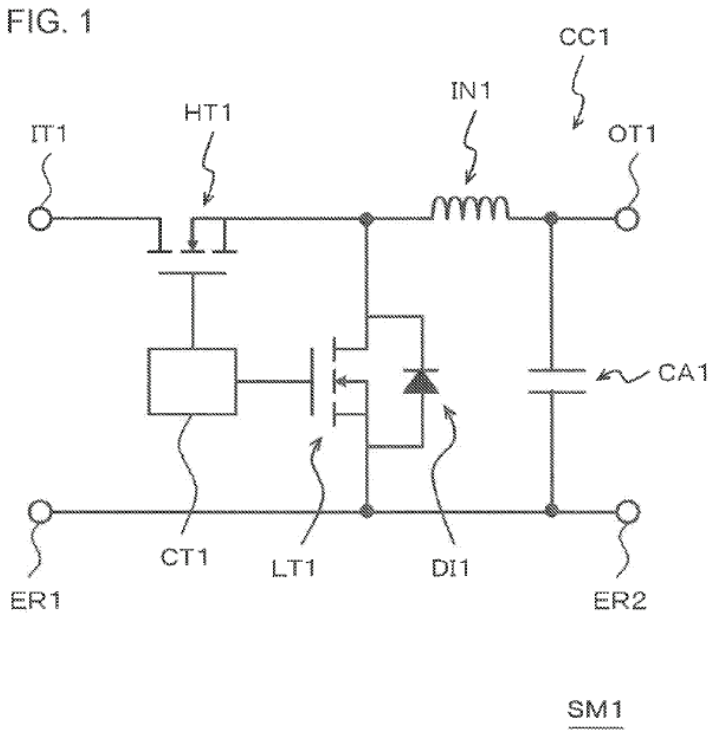


Nega (annotated).

6. Claim 10

a. [10p] A switch circuit, comprising:

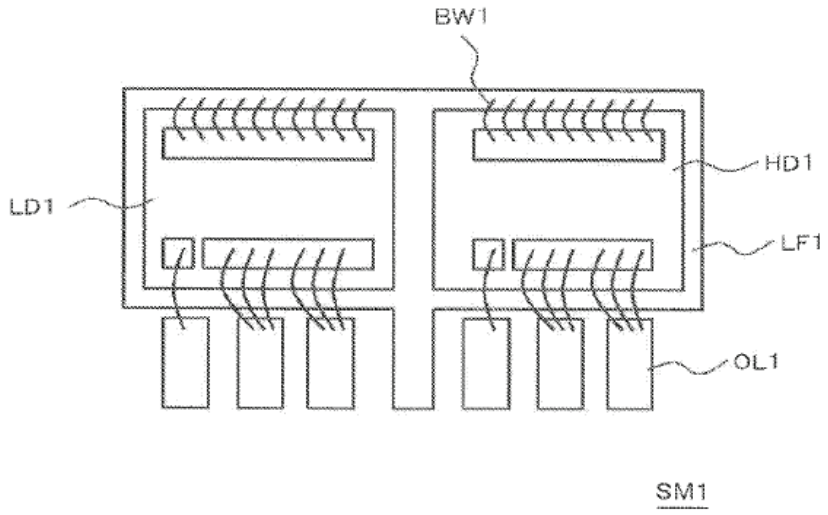
[0136] Nega discloses [10p] because it discloses a high-side switching device HT1 and a low-side switching device LT1 collectively comprising circuit CC1 (switch circuit) implemented in semiconductor device SM1. Nega, [0030]-[0034], [0037].



[0137] Nega, Fig. 1 (showing switch circuit CC1 implemented in device SM1).

[0138] Nega explains that circuit CC1 is implemented in semiconductor device SM1, which includes a "high-side switching device HD1 constituted by the transistor HT1 and a low-side switching device LD1 constituted by the transistor LT1." Nega, [0090]-[0091].

FIG. 4



Nega, Fig. 4.

b. [10a] a first transistor device comprising a compound semiconductor, a first current electrode, a second current electrode and a control electrode, a die pad, a first lead, a second lead, and a third lead, the first lead the second lead and the third lead being spaced at a distance from the die pad, wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the transistor device and provide a source sensing functionality, and

[0139] Element [10a] is identical to elements [1a]-[1e]. Nega-Roberts discloses [10a] for the reasons explained for [1a]-[1e].

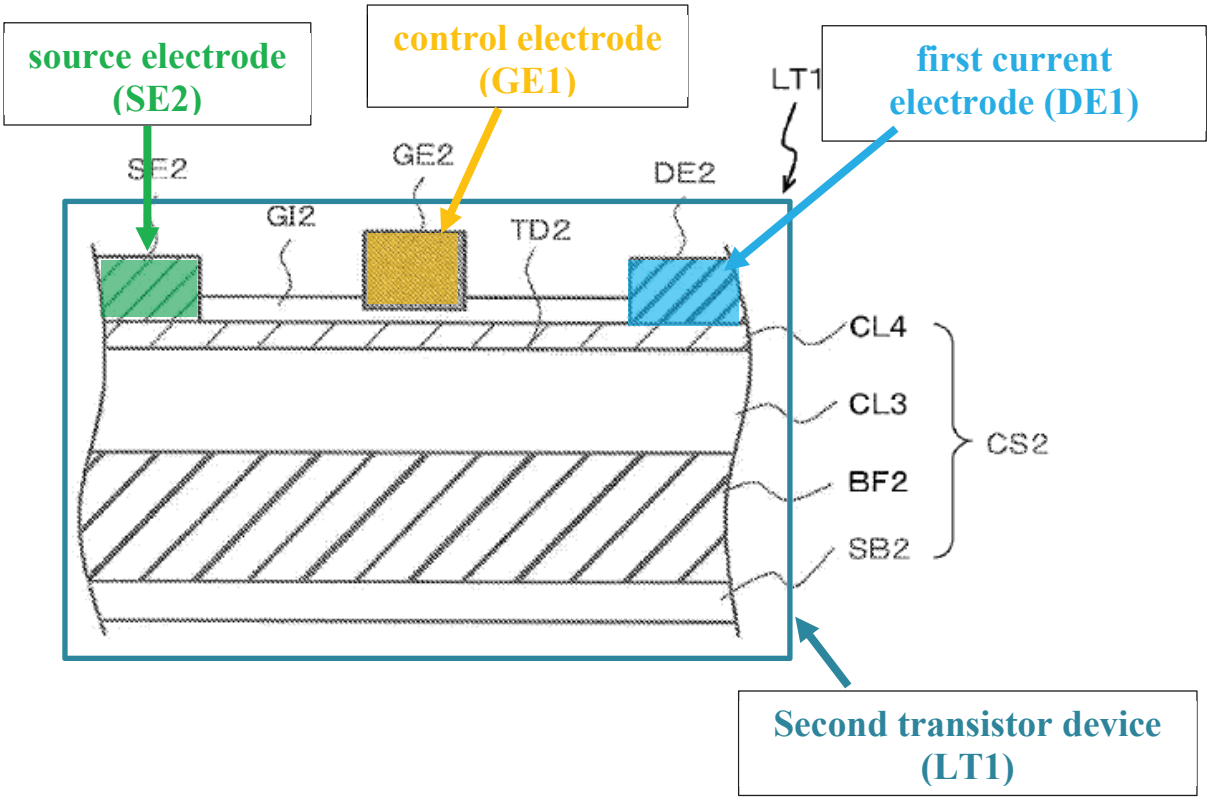
c. [10b] a second transistor device,

[0140] Nega discloses a second transistor device (LT1/LD1).

[0141] Nega discloses that transistor LT1 "is formed in a compound semiconductor substrate," Nega, [0073], or is a "silicon device," Nega, [0074]. LT1 is a separate semiconductor chip from HT1—thus a separate device. Nega, [0093]. Further, LD1 is a low-side switching device constituted by the transistor LT1. Nega, [0091], [0093].

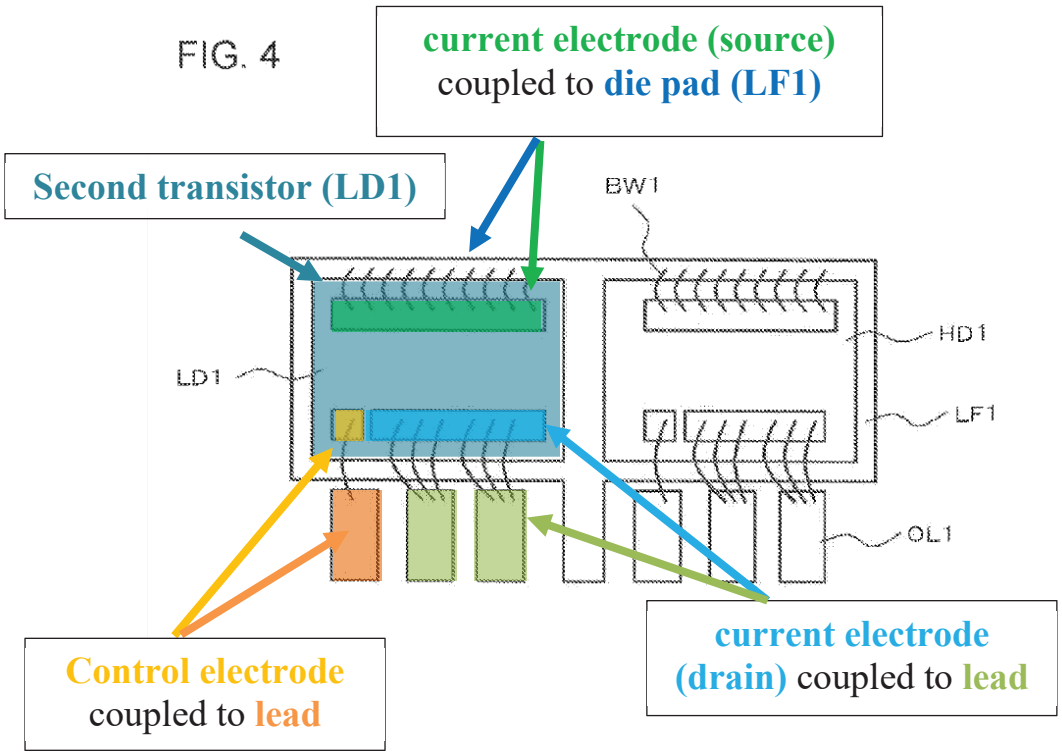
[0142] As shown below in Figure 3, Nega's second transistor device LT1 has a **drain electrode DE2** (Nega, [0080]), **a source electrode SE2** (Nega, [0080]), and a **gate electrode GE2** (Nega, [0079], [0081]).

FIG. 3



Nega, Fig. 3 (annotated).

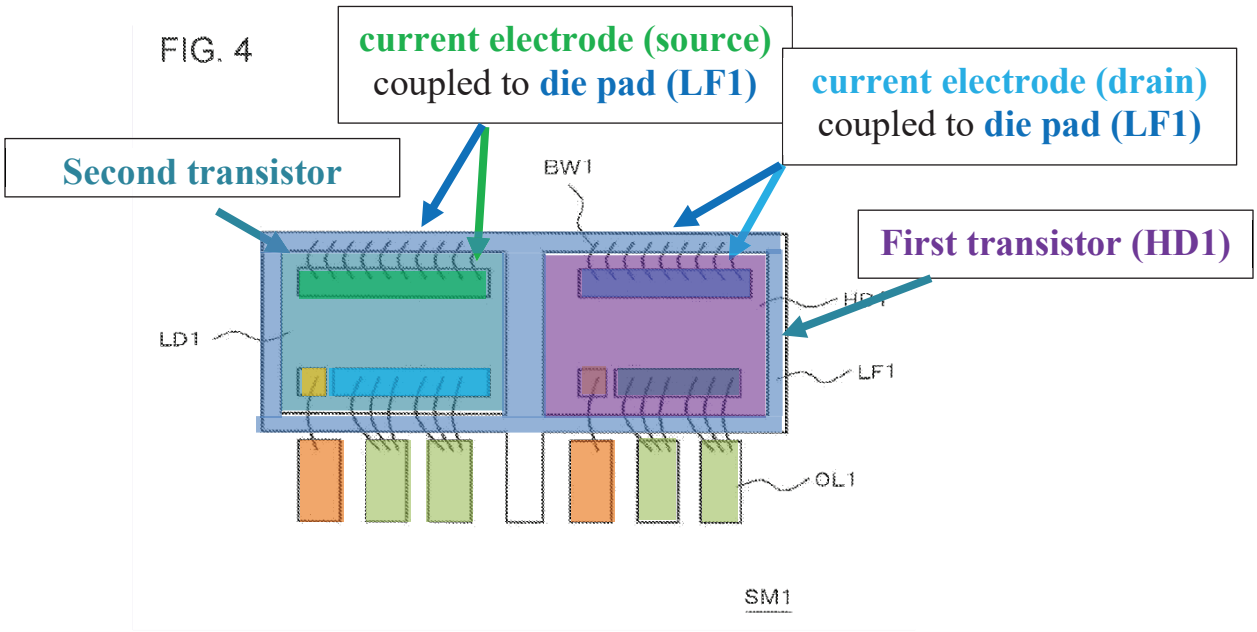
[0143] HD1 in Nega's Figure 4 constitutes HT1, Nega's first transistor device. Nega, [0091], [0093]. Annotated Figure 4 below further shows the second transistor device LD1 on the die pad LF1.



Nega, Fig. 4 (annotated).

d. [10c] wherein the first transistor device has a current path coupled serially or antiserially with a current path of the second transistor device,

[0144] Nega's first transistor device (HD1) has a serially connected current path with its second transistor device (LD1) because, as discussed in [10a] and [10b] and shown below in annotated Figure 4, the drain electrodes of Nega's first transistor device (HD1) is coupled to the die pad and the source of Nega's second transistor device (LD1) is connected to the die pad, thus serially connected. Nega, [0095].



Nega, Fig. 4 (annotated).

[0145] Nega discloses that "[i]n the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1," and "[i]n the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1." Nega, [0095]. In my opinion, a POSITA would have understood that Figure 4 discloses a serial connection because the drain electrodes of Nega's first transistor device (HD1) is coupled to the die pad and the source of Nega's second transistor device (LD1) is connected to the die pad.

e. [10d] wherein the first transistor device is a lateral transistor device and a drain or a source of the first transistor device is coupled to the die pad,

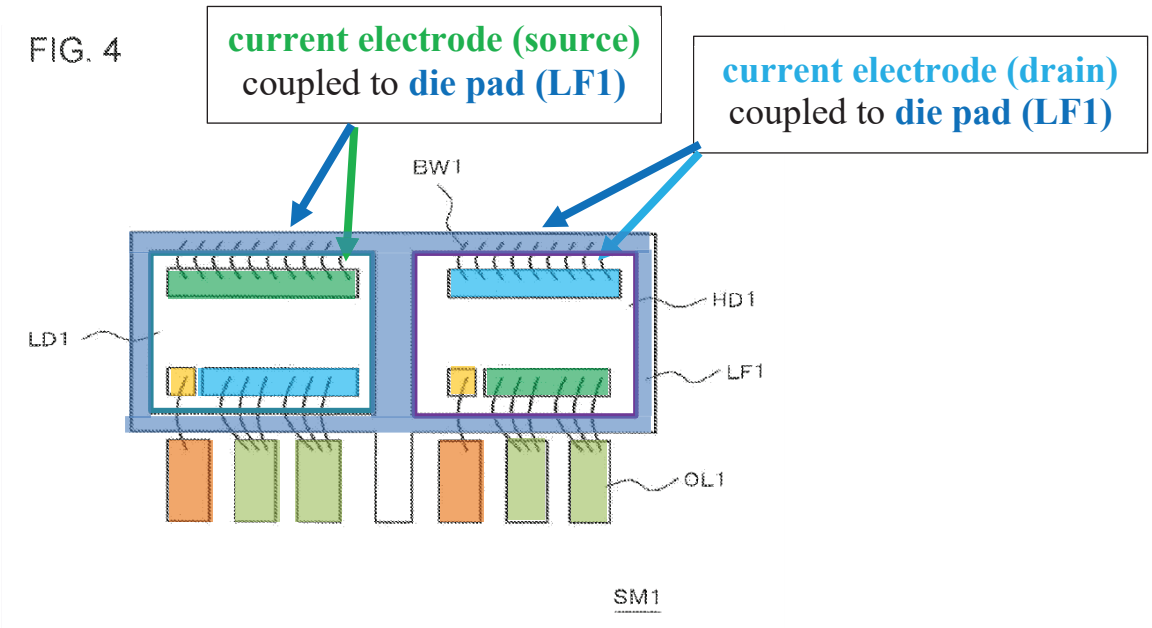
[0146] Element [10d] is identical to element [1e]. Nega-Roberts discloses [10d] for the reasons explained for [1e].

f. [10e] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

[0147] Element [10e] is identical to element [1f]. Nega-Roberts discloses [10e] for the reasons explained for [1f].

7. Claim 11 - The switch circuit of claim 10, wherein a drain of the first transistor device and a source of the second transistor device are coupled to a common die pad.

[0148] Nega discloses claim 11. As explained for element [10c], Nega discloses the drain of the first transistor device and the source of the second transistor device are coupled to the common die pad. In my opinion, a POSITA would have understood that this is the serially connection. This is also demonstrated in annotated Figure 4 below.



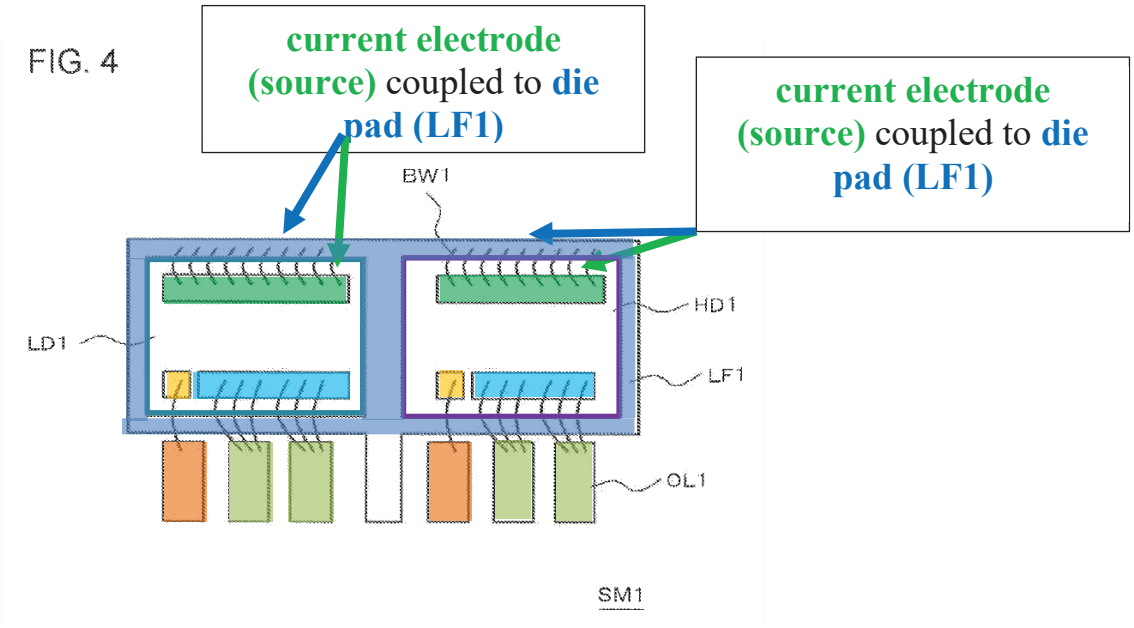
Nega, Fig. 4 (annotated).

8. Claim 16 – The switch circuit of claim 10, wherein a source of the first transistor device is coupled to a source of the second transistor device.

[0149] Nega discloses claim 16 because Nega discloses that the source electrodes for its first transistor devices HD1 and second transistor device LD1 are connected. Nega, [0095].

[0150] Nega discloses that "[i]n the transistor HT1 constituting the high-side switching device HD1, one of the source electrode SE1 and the drain electrode DE1 is connected to the lead frame LF1, and the other thereof is connected to the outer lead OL1," and "[i]n the transistor LT1 constituting the low-side switching device LD1, one of the source electrode SE2 and the drain electrode DE2 is connected to the lead frame LF1, and the other thereof is connected to the

outer lead OL1." Nega, [0095]. The '481 patent discloses that "when an element is referred to as being 'connected' or 'coupled' to another element, it can be directly connected or coupled to the other element or intervening elements may be present." '481 patent, 3:34-37. Thus, the source of Nega's first transistor device SE1 and the source of Nega's second transistor device SE2 are coupled through the mutual connection to the outer lead LF1.



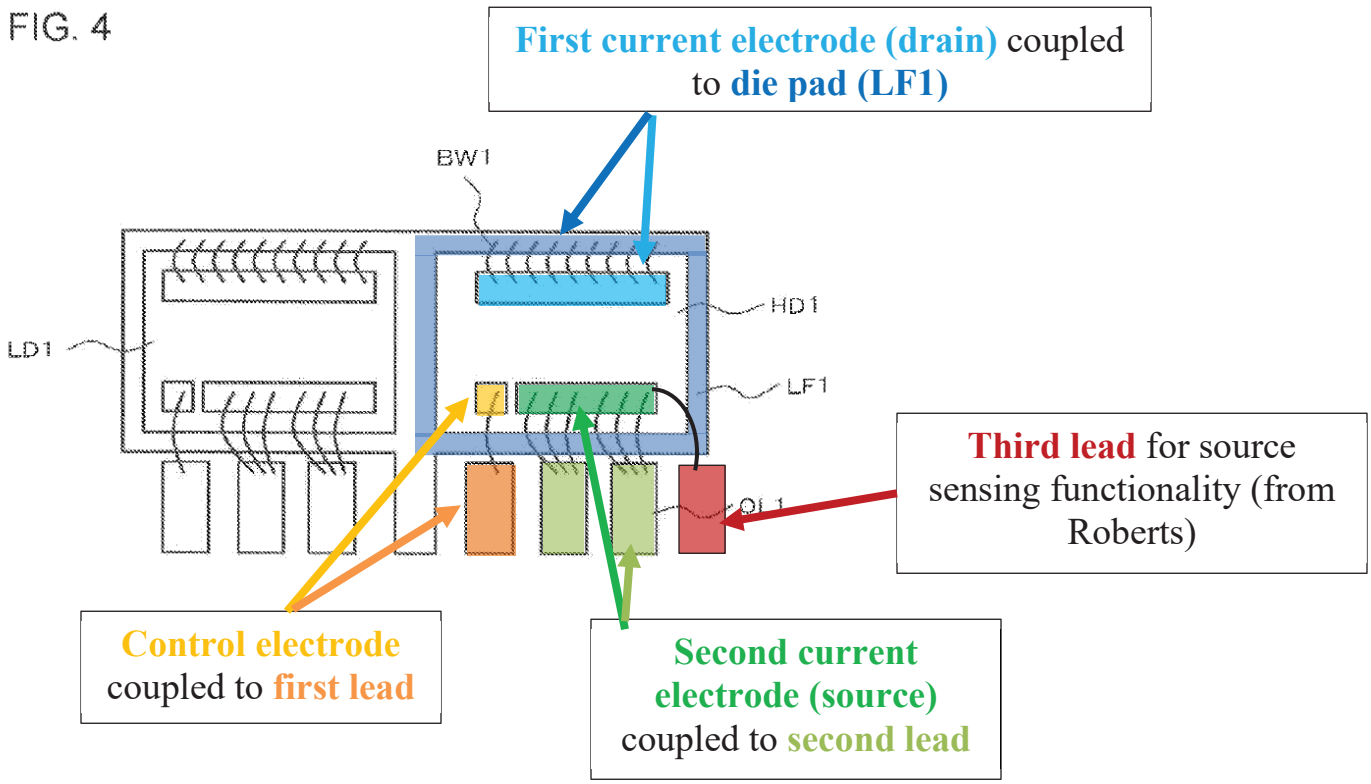
Nega, Fig. 4 (annotated).

C. Ground 1B: Nega in View of Roberts and Otremba124 Renders Obvious Claims 4, 9, and 17

1. Claim 4 - The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.

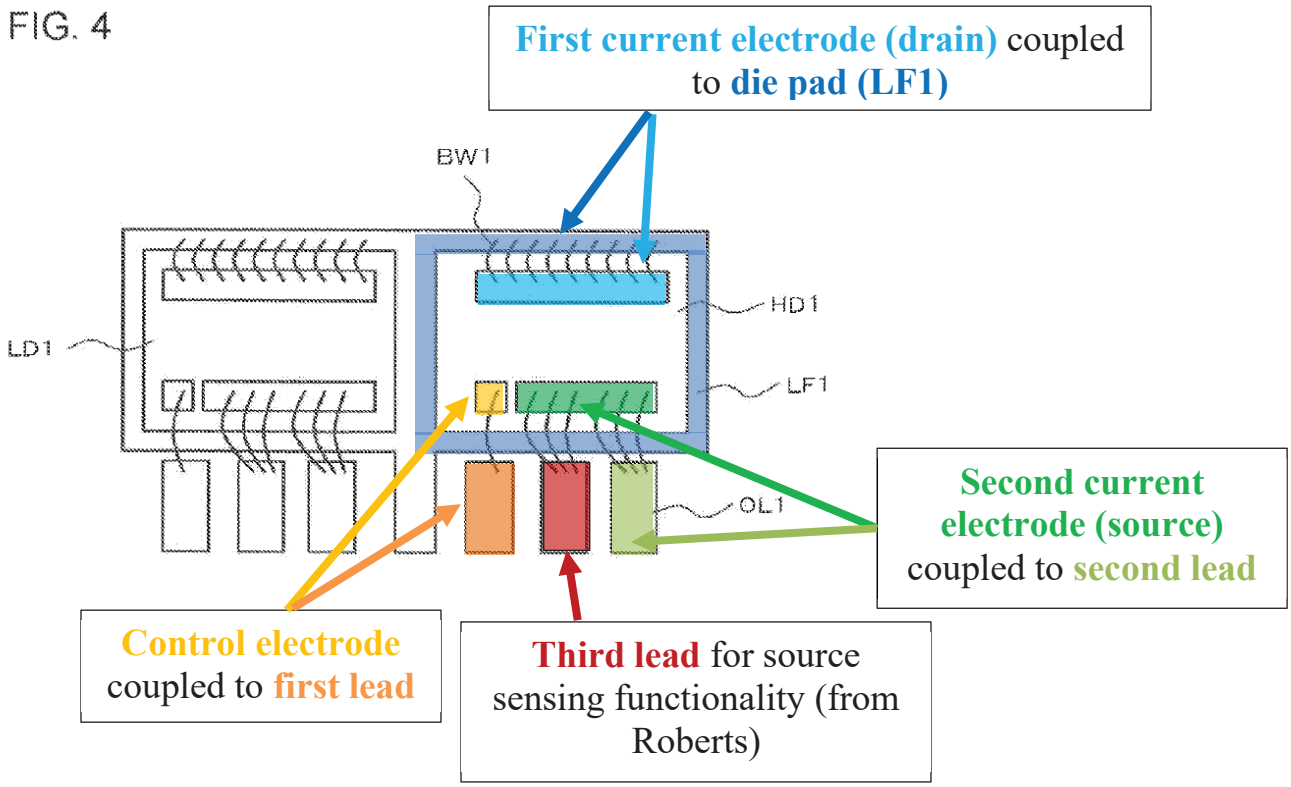
[0151] Nega in view of Roberts and Otremba124 renders claim 4 obvious.

[0152] As explained for [1c]-[1e], Nega discloses first and second leads, and Nega-Roberts renders obvious the third lead.



Nega, Fig. 4 (annotated and modified).

[0153] Alternatively, repurposing one of Nega's source leads as a source sensing lead:

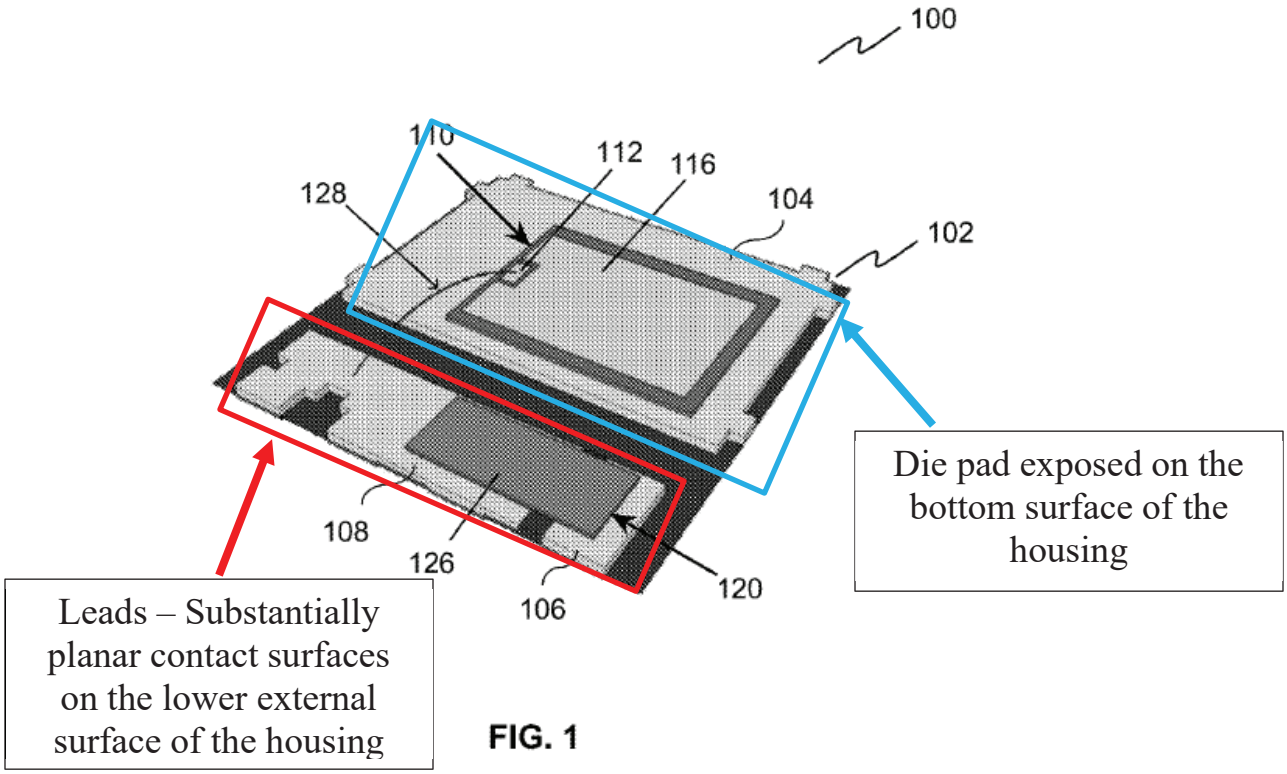


Nega (annotated).

[0154] Nega discloses that the transistor is contained within a housing, for example "the package of TO220." Nega, [0063]. Nega, however, does not expressly disclose that its leads and die pad are exposed on the lower surface forming planar contacts. But this configuration was well known in the art, as at least suggested by Otremba124.

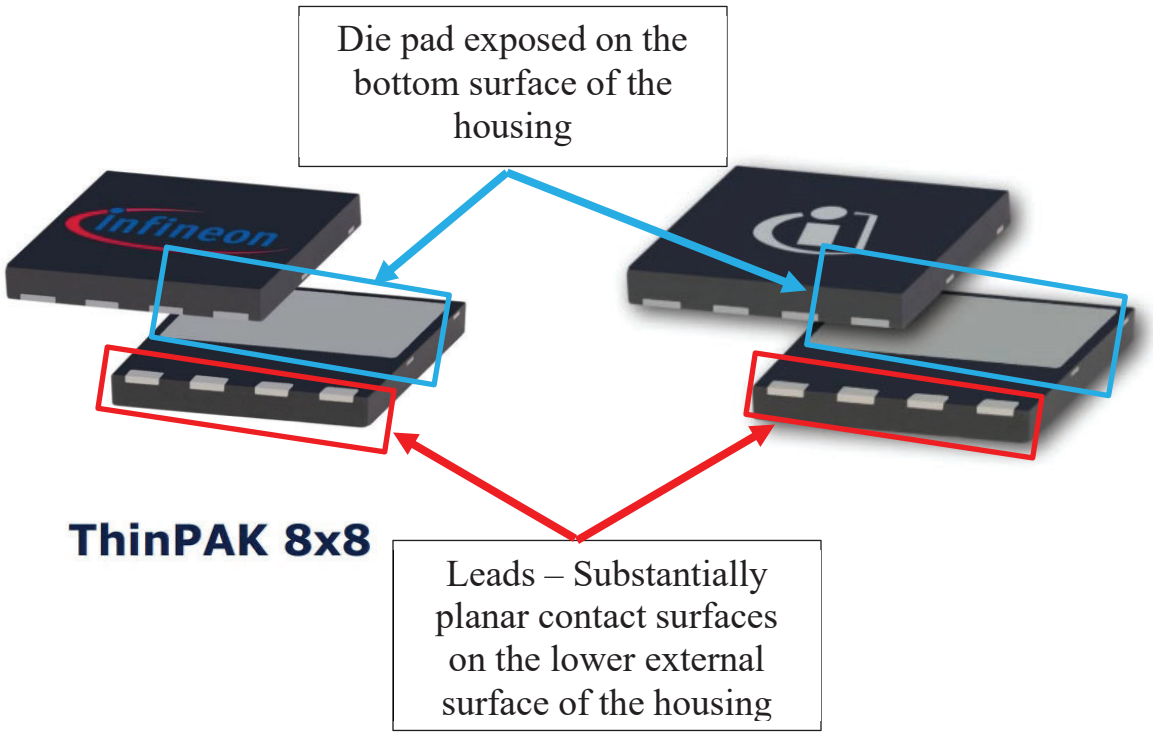
[0155] Otremba124 discloses a power transistor including a GaN HEMT "packaged in a[n] 8x8 ThinPAK." Otremba124, [0041]. Figure 1 shows the

ThinPAK8x8 package outline with flat source leads 108 and 106 on the bottom of the package.



Otremba124, Fig. 1 (annotated).

[0156] ThinPAK8x8 was a well-known leadless package design at the time, as evidenced by ThinPAK8x8 Brochure and ThinPAK Recommendations, which confirms that ThinPAK8x8 packaging included leads and a die pad exposed on the lower surface and forming planar contacts (a leadless design). Ex-1016, 1, 5, 6; Ex-1017, 1, 4 ("Visible are the 4 small Source/Gate-Pads … and the big exposed drain pad ….").



Ex-1016, 1, 31; Ex-1017, 1 (annotated).

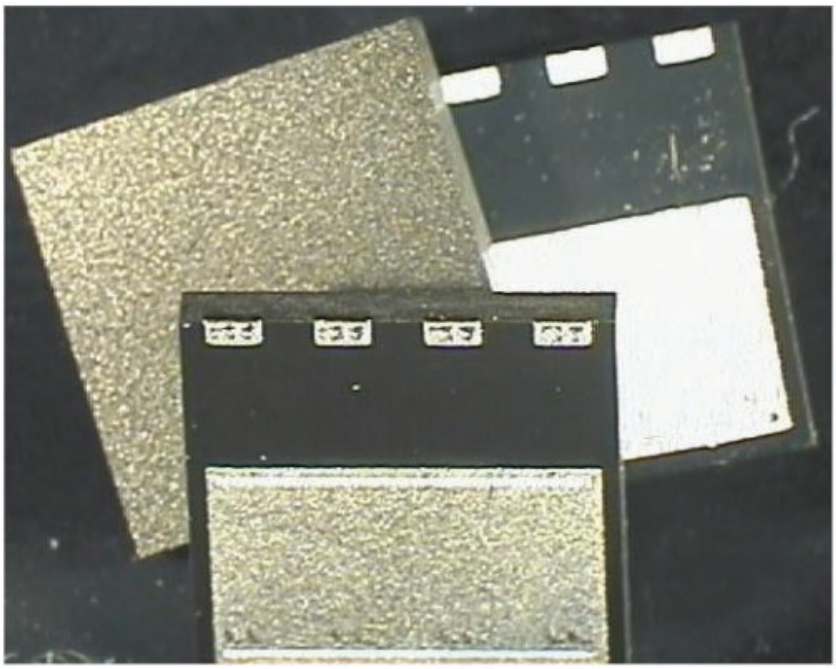


Figure 1: Top and bottom view of VDSON-4 (ThinPAK 8x8)

Ex-1017, 4 (Fig. 1) (annotated).

[0157] In my opinion, a POSITA would have been motivated to package Nega's HT1 (HD1) in the ThinPAK8x8 package design of Otremba124 with an exposed die pad and planar lead contacts on the lower surface. ThinPAK8x8 was boasted as an improvement on other leaded packaging designs, saving space on the printed circuit board (PCB) with a footprint of 64mm^2 (as opposed to 150mm^2 for competitive devices at the time). Ex-1016, 3. Likewise, because ThinPAK8x8 was leadless, it showed faster performance and switching speeds than through-hole and other conventional packages (like the TO220), thus enabling improved performance, switching behavior, ease-of-use, EMI (electromagnetic interference), reliability, and higher power density. Ex-1016, 3. These package features also led to lower parasitics because a faster performing package leads to lower parasitics. Nega recognizes that it implements a standardized TO220 package (a leaded package), as an exemplary package design, and would have realized the known benefits ThinPAK8x8 offered as improvements to a device ready for such improvement. Indeed, Lind shows ThinPAK8x8 with source sensing connections as an alternative to a similar leaded package, TO-247-4P, as, in my opinion, would be obvious to a POSITA:

III. Source-Sense concept and A/B simulation

A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.

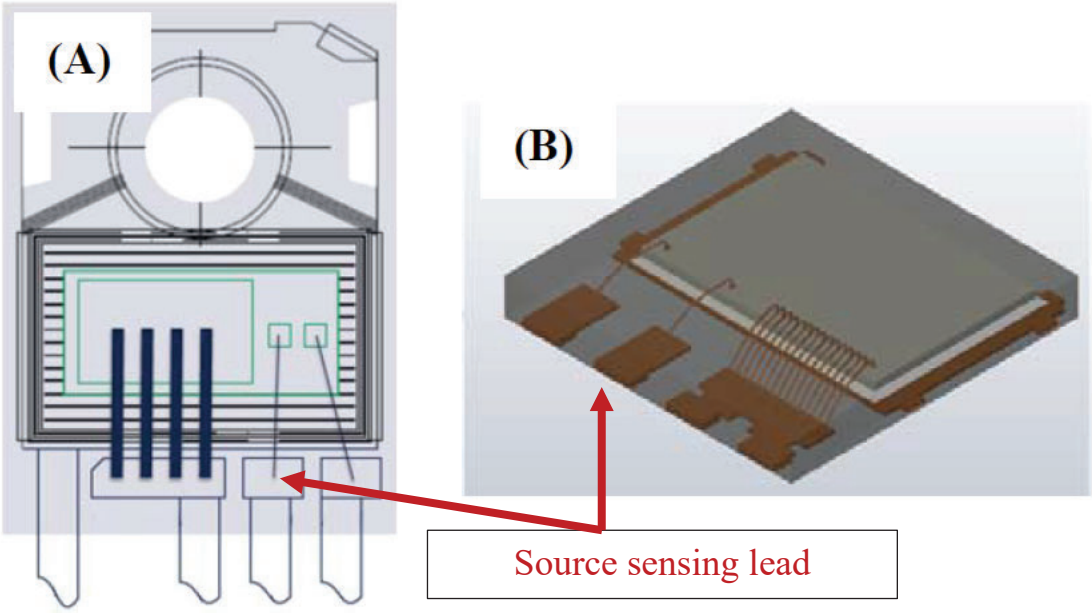


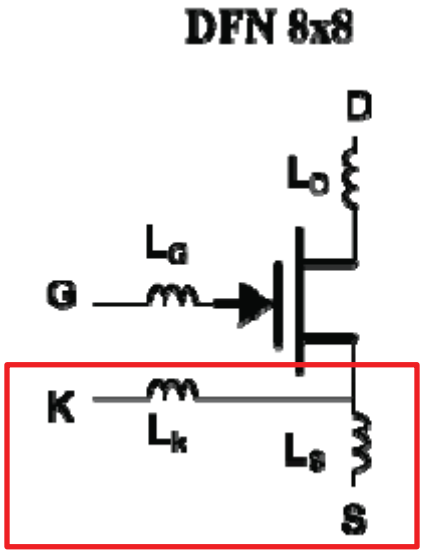
Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections

Ex-1013, 3 (Fig. 4) (annotated).

[0158] Thus, packaging Nega-Roberts as a ThinPAK8x8, disclosed by Otremba124, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results.

[0159] Moreover, additional package formats, including leadless, exposed-die packages, were also known and in use at the time as taught by Otremba433 and would have been at least considered suitable options for packaging Nega's compound semiconductor transistor device HT1 (HD1). And

additional, similar packaging types were known, including those with source sending leads, like a DFN8x8 package. Ex-1024, 2 (showing a DFN package with a Kelvin connection). A POSITA would also have been motivated to combine Huang's DFN8x8 package, which is "typically used for high voltage e-mode GaN devices[,]" with Nega's compound semiconductor transistor device. Ex-1024.



Ex-1024, Fig. 2 (annotated).

2. Claim 9 - The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline.

[0160] Claim 9 is of similar scope to claim 4, except claiming the ThinPAK8x8 design expressly. Nega in view of Roberts and Otremba124 (expressly disclosing ThinPAK8x8 packaging at [0041]) renders claim 9 obvious for the reasons explained for claim 4.

3. Claim 17

[0161] Claim 17 is substantially similar to claims 3 and 4, as incorporating the limitations of claim 1. Nega-Roberts teaches the entirety of claims 1 and 3. Otremba124 discloses the additional limitation of claim 4. Thus Nega-Roberts-Otremba124 renders obvious claim 17.

a. [17p] An electronic component, comprising:

[0162] [17p] is identical to [1p]. Nega discloses [17p] for the reasons explained for [1p].

b. [17a] a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality;

[0163] Nega in view of Roberts renders obvious [17a].

[0164] As explained for [1a] and claim 2, Nega discloses a Group III nitride-based transistor device.

[0165] As explained for claim 3, Nega-Roberts teaches a blocking voltage capability of at least 100 kHz, a first current electrode, a second current electrode, and a control electrode.

[0166] As explained for [1a], Nega discloses a first current electrode, a second current electrode, and a control electrode.

[0167] As explained for [1e], Nega-Roberts teaches the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead, and a third lead is coupled to the transistor device and provides a source sensing functionality.

c. [17b] a housing,

[0168] [17b], like Claim 4, requires a housing. Nega-Roberts-Otremba124 discloses a housing for the reasons explained for claim 4.

d. [17c] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

[0169] [17c] is identical to [1d]. Nega-Roberts teaches [17c] for the reasons explained for [1d].

e. [17d] wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces,

[0170] [17d] is identical to claim 4. Nega-Roberts-Otremba124 teaches [17d] for the reasons explained for claim 4.

f. [17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a

source of the Group III nitride-based transistor device is coupled to the die pad,

[0171] [17e] is similar to [1f] except that it requires a Group III nitride-based transistor device rather than a general compound semiconductor device.

[0172] As explained for [17a] and claim 2, Nega discloses a Group III nitride-based transistor device.

[0173] Nega-Roberts teaches the remainder of [17e] for the reasons explained for [1f].

g. [17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

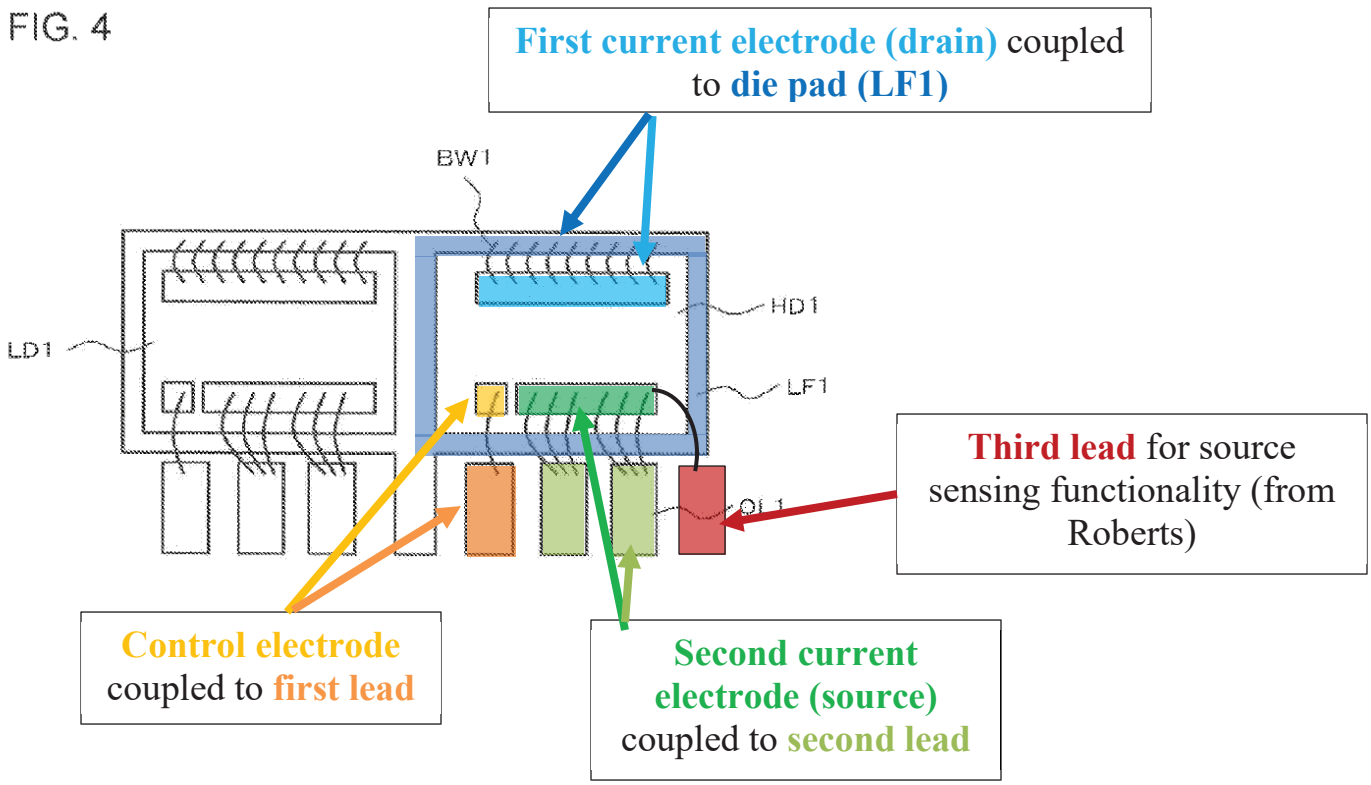
[0174] [17f] is identical to [1g]. Nega discloses [17f] for the reasons explained for [1g].

D. Grounds 1C and 1D: Nega in View of Roberts and Otremba433 Renders Obvious Claims 4, 7, 8, and 17 (1C); Nega in View of Roberts, Otremba433, and Otremba280 Renders Obvious Claims 7 and 8

1. Claim 4 - The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.

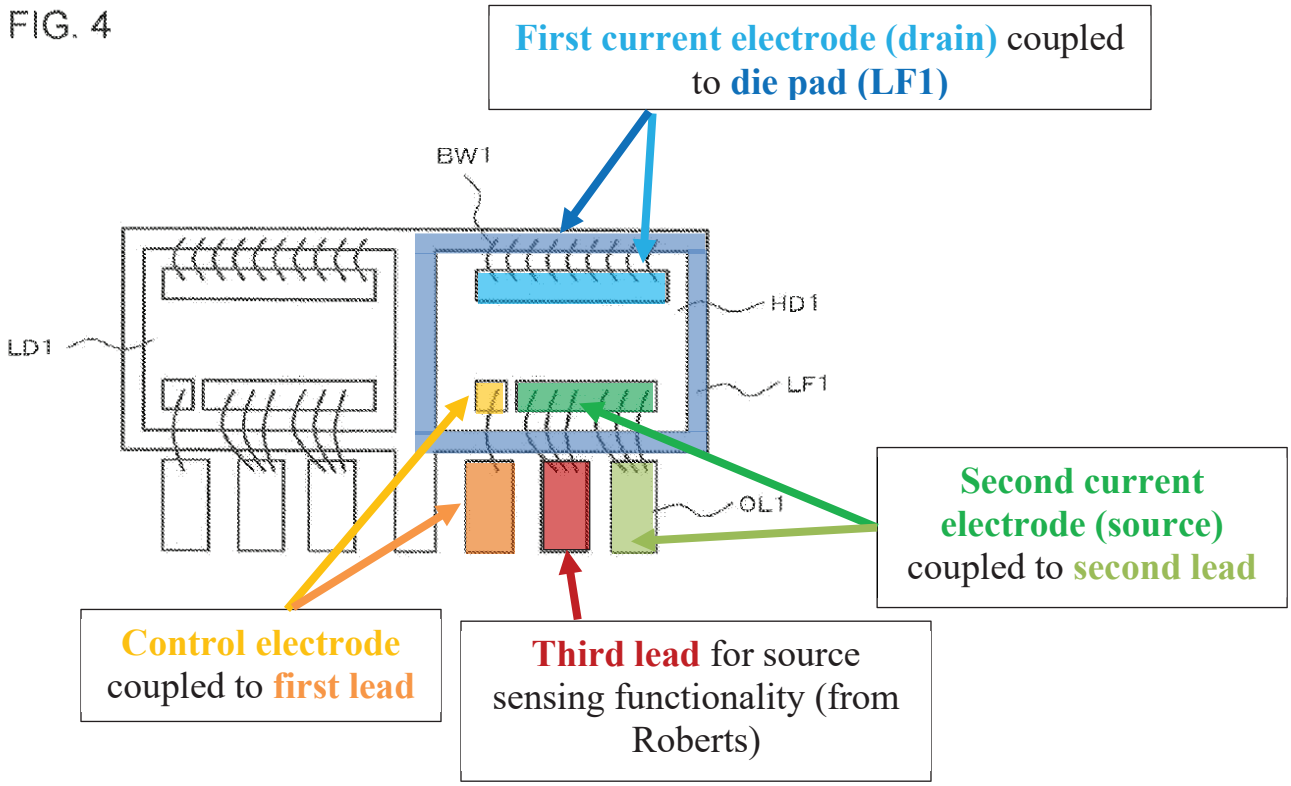
[0175] Nega in view of Roberts and Otremba433 renders claim 4 obvious.

[0176] As explained for [1c]-[1e], Nega discloses first and second leads and Nega-Roberts renders obvious the third lead.



Nega, Fig. 4 (annotated and modified).

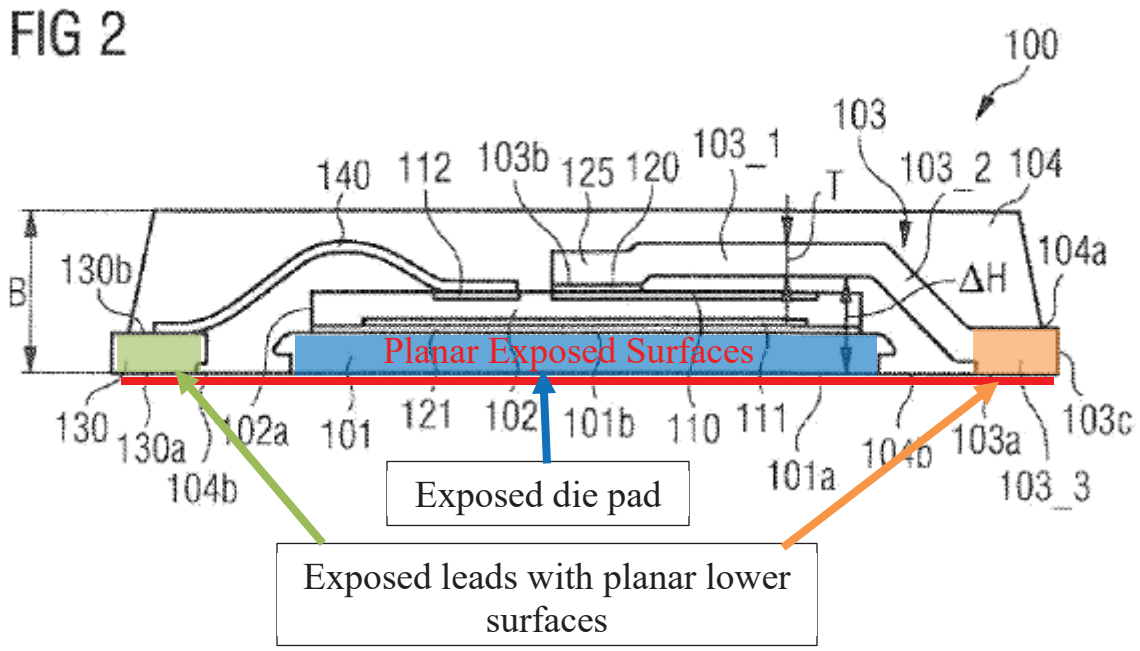
[0177] Alternatively, repurposing one of Nega's source leads as a source sensing lead:



Nega, Fig. 4 (annotated).

[0178] Further, Nega discloses that the transistor is contained within a housing, for example "the package of TO220." Nega, [0063]. Nega, however, does not expressly disclose that its leads and die pad are exposed on the lower surface forming planar contacts. But this configuration was well known in the art, as at least suggested by Otremba433. Otremba433 discloses a "leadless package" with contacts and die pad exposed on the bottom of the devices (Otremba433, [0037]), explaining that "semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104." Otremba433, [0027]. Otremba433's contacts 130 and 103 (leads) have "external

contact area[s]" 103a and 130a that are "coplanar with a reference plane defined by a bottom surface 101a of the carrier 101" (die pad) that is "exposed at the bottom of the package." Otremba433, [0037] (discussing lead 103/103a and carrier 101/101a), [0039] (discussing lead 130/130a); *see also* Otremba280, 4:17-29 ("The lower surface 33 of the device carrier portion 19 and the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a surface mountable or leadless type electronic component.").

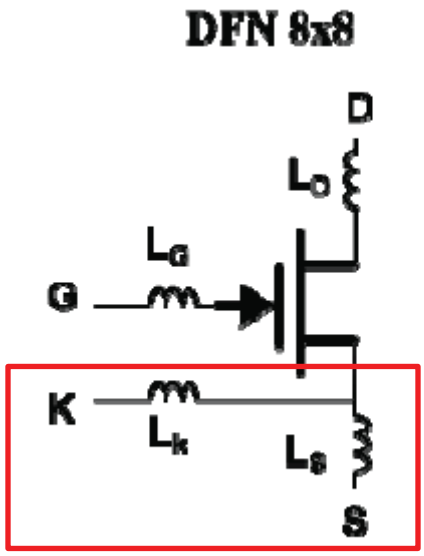


Otremba433, Fig. 2 (annotated).

[0179] A POSITA would have understood that Nega's device would be readily implemented in the leadless package of Otremba433 because package

designs were easily modifiable to meet the needs of a particular use. Nega recognizes that it implements a standardized TO220 package (a leaded package), as an exemplary package design, and would have realized the known benefits of leadless package designs as explained for claim 4 in Ground 1B. Thus, packaging Nega-Roberts as a leadless package, disclosed by Otremba433, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results.

[0180] Moreover, as explained for claim 4, additional package formats, including leadless, exposed-die packages, were also known and in use at the time, as taught by Otremba433, and would have been at least considered suitable options for packaging Nega's compound semiconductor transistor device HT1 (HD1). In fact, Otremba433 recognizes that leaded and leadless packages were both possible for packaging semiconductor devices. Otremba433, [0025]. And Huang shows another type of leadless package, a DFN8x8 package, with a source sensing lead. Ex-1024, 2, Fig. 2. This type of package is "typically used for high voltage e-mode GaN devices." Ex-1024, 2.



Ex-1024, Fig. 2 (annotated).

2. Claim 7 - The electronic component of claim 4, wherein the first current electrode is coupled to the die pad by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

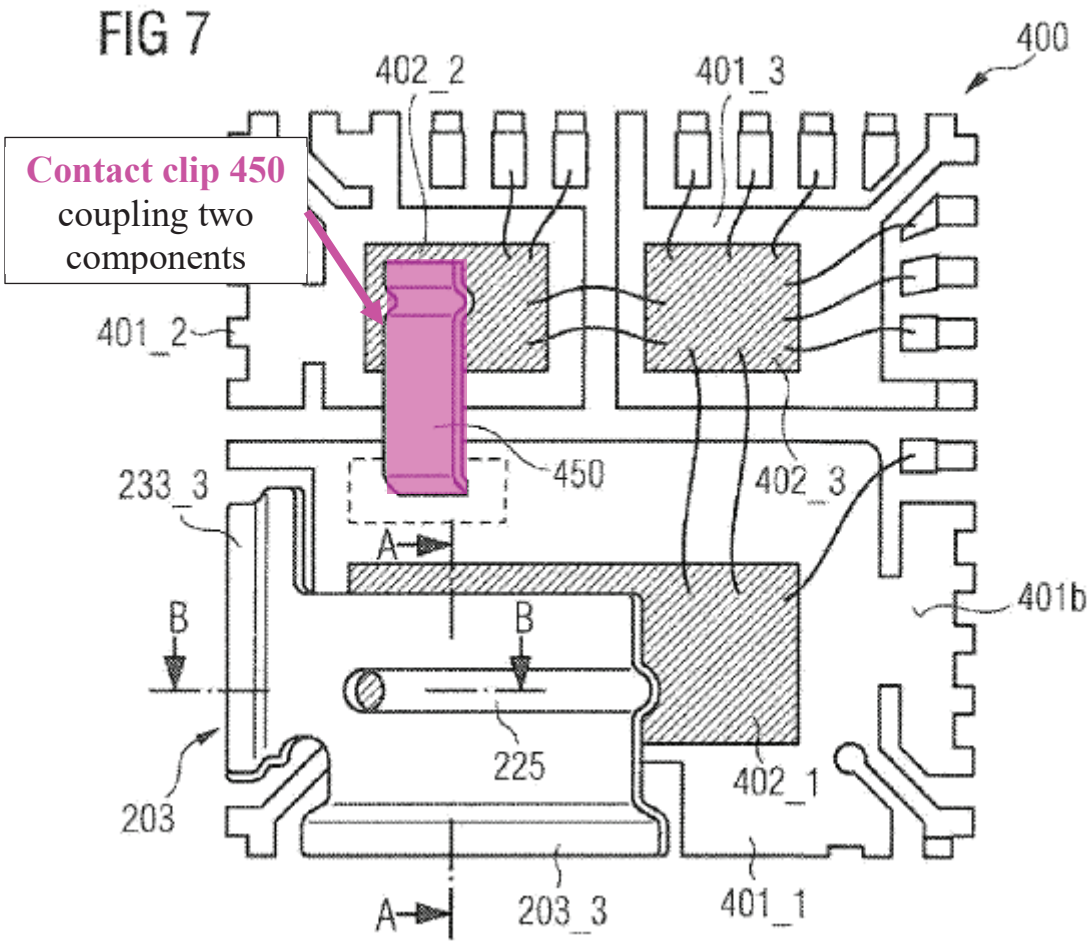
[0181] Claim 7 depends from claim 4, but additionally requires a contact clip exposed from the housing forming the connection between the drain electrode (first current electrode) and the die pad (as opposed to bond wires, as allowed for claims 1 and 4).

[0182] Nega-Roberts discloses coupling the drain electrode (first current electrode) to the die pad, as explained for [1f]-[1g] but does so using a plurality of bond wires rather than a contact clip. Bond wires and contact clips were well-known alternatives to one another at the relevant time, largely interchangeable but each boasting certain advantages over the other. A POSITA

would have understood that contact clips, as opposed to bond wires, would have been a suitable option when implementing the Nega-Roberts packaged compound semiconductor transistor device, particularly in devices where there is a desire to reduce parasitic-inductance caused by bond wires. And exposed contact clips provided enhanced thermal performance.

[0183] **For Ground 1C**, Otremba433 discloses coupling components of devices using conventional contact clips. Otremba433 explains: "The source electrode of the high side power semiconductor chip 402_2 is connected to the first carrier 401_1 by a contact clip 4[50]. The contact clip 4[50] may be a conventional contact clip which bridges a level difference …."[1] Otremba433, [0072].

[1] Otremba433 mistakenly refers to contact clip 450 as contact clip 405. Figure 7 has no numeral 405, and the contact clip is numeral 450, correctly referenced later in [0072].

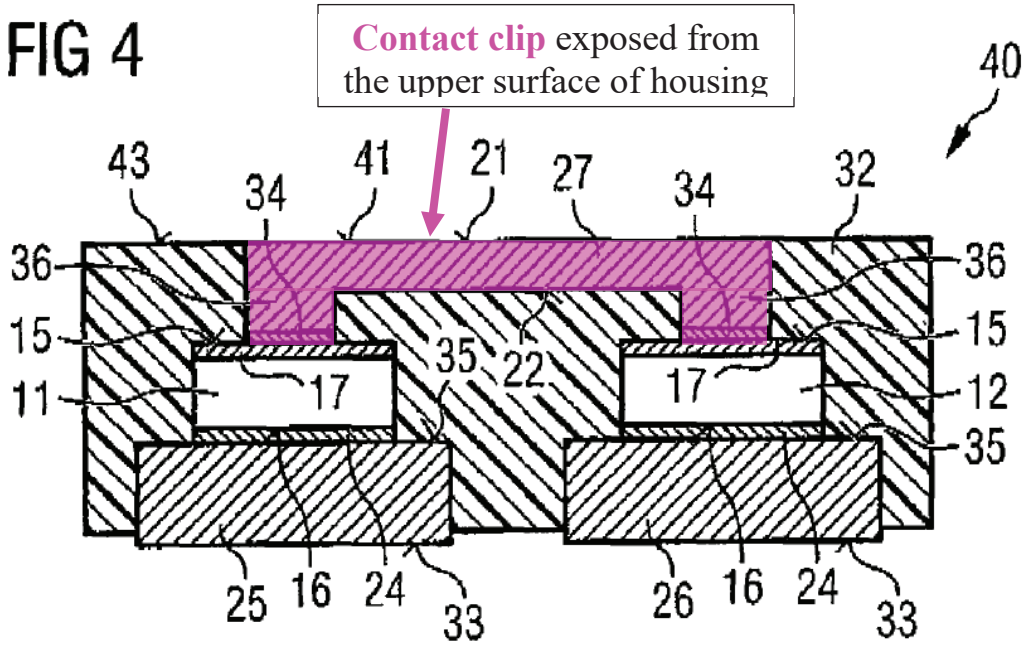


Otremba433, Fig. 7 (annotated).

[0184] A POSITA would have understood the known thermal benefits of exposing the contact clips from the upper surface of the device housing (like "provid[ing] a shorter path of thermal resistance" between the device "and the environment around the electronic component" (Otremba280, 8:45-57)), and would have readily understood how to implement exposed contact clips, as was

known in the art (as explained for Ground 1D and Otremba280), within the Nega-Roberts-Otremba433 device.

[0185] **For Ground 1D**, like Otremba433, Otremba280 discloses using contact clips to couple components within a device. Otremba280 states that its electronic component includes a "contact clip 14 [that] is exposed from the plastic encapsulation compound 32 [(housing)]." Otremba280, 8:33-41, Fig. 4.



Otremba280, Fig. 4 (annotated).

[0186] Otremba280 expressly teaches suggests and motivates exposing the contact clip from the housing because the "exposed area 41 of the contact clip 14 provides a shorter path of thermal resistance" with "the environment around the electronic component 40." Otremba280, 8:45-48. By exposing the clip, the

"thermal performance of the electronic component 40 may be increased due to an improvement in the efficiency of thermal dissipation from the electronic component 40." Otremba280, 8:48-51. To realize the thermal benefits, a POSITA would have been motivated to implement Otremba443's contact clip in Nega-Roberts as an exposed contact clip (Ground 1C) and/or to implement Otremba280's exposed contact clip in Nega-Roberts-Otremba433 (Ground 1D) to couple Nega's drain electrode (first current electrode) and LF1 (die pad).

[0187] For Grounds 1C and 1D, a POSITA would have been motivated to use a contact clip, as taught by either Otremba433 or Otremba280, to couple Nega-Roberts's first current electrode to the die pad in place of Nega's bond wires to (1) improve current carrying capability; (2) allow for better current spreading to avoid hot spots; (3) reducing on resistance; (4) reducing parasitic induction; and (5) simplifying assembly and manufacturing.

[0188] **First,** contact clips have better current carrying capability than bond wires because of their larger surface area connections, thicker metal, stronger construction, and higher integrity for assembly and manufacturing as opposed to narrow gauge bond wires which can be considered fragile.

[0189] **Second,** contact clips provide better current spreading across the clip as opposed to narrow gauge bond wires that can cause hotspots from current crowding. The thicker metal helps the current to become more uniform

within the clip. Current hot spots are caused by current crowding which is when current is forced to go into a narrow area. Current crowding is a well-known reliability and lifetime issue for narrow gauge bond wires.

[0190] **Third,** contact clips reduce device on-resistance (RDS(on)) because the contribution of Rpkg is lower than bond wire resistance, which usually must be accounted for in the overall figure, especially when aiming for a total device RDS(on) ≤ 25 mΩ. RDS(on) is lower as the metal contact clips are thicker and are capable to carry more current, as well as having the physical dimensions through larger area and thickness to mitigate current hot spots and current crowding.

[0191] **Fourth**, contact clips reduce parasitic inductance because bond wires behave as parasitic inductors that can negatively impact device switching. Contact clips inherently have lower parasitic inductance, enabling higher device switching. Otremba880, from the same time period, explains that "[a]n electronic device comprising a semiconductor chip may exhibit a parasitic source- or emitter-inductance and a parasitic drain- or collector-inductance," and "[r]educing a parasitic inductance may improve an efficiency of the electronic device." Otremba880, 1:11-18. To resolve the issue of parasitic impendence, a POSITA would have understood using contact clips to connect components of the device—not bond wires that can incur parasitic inductance.

[0192] **Fifth,** contact clips are simple to handle in assembly and packaging for back-end manufacturing. Contract clips can be easily loaded into automatic tools for high yielding, high volume assembly, which keeps costs under control.

[0193] At the very least, bond wires and contact clips were known alternatives for coupling components of a compound semiconductor transistor device. Otremba441 discloses that commonly-known coupling structures within transistor devices include any of "a clip, a ribbon, a wire, a plate, or a conductor track," so long as the resistance is below a certain threshold. Otremba441, 2:59-65, 6:34-43; *see also* Otremba124, 3:48-60, 7:49-55. A POSITA would have understood that bond wires and contact clips were ubiquitous coupling means, each suited to different design preferences and needs, and at least both constituting suitable options.

3. Claim 8 - The electronic component of claim 4, wherein the second current electrode is coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

[0194] As explained for claim 7, implementing an exposed contact clip to couple components in Nega-Roberts would have been obvious. Coupling Nega's second current electrode to the second lead with Otremba433's (Ground 1C) and/or Otremba280's (Ground 1D) contact clip would have been obvious for the same

reason coupling Nega's first current electrode to the die pad would have been obvious, as explained for claim 7.

4. Claim 17

[0195] Claim 17 is substantially similar to claims 3 and 4, as incorporating the limitations of claim 1. Nega-Roberts teaches the entirety of claims 1 and 3. Otremba124 discloses the additional limitation of claim 4. Thus Nega-Roberts-Otremba124 renders obvious claim 17.

a. [17p] An electronic component, comprising:

[0196] [17p] is identical to [1p]. Nega discloses [17p] for the reasons explained for [1p].

b. [17a] a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and

[0197] Nega in view of Roberts renders obvious [17a].

[0198] As explained for [1a] and claim 2, Nega discloses a Group III nitride-based transistor device.

[0199] As explained for claim 3, Nega-Roberts teaches a blocking voltage capability of at least 100 kHz, a first current electrode, a second current electrode, and a control electrode.

[0200] As explained for [1a], Nega discloses a first current electrode, a second current electrode, and a control electrode.

[0201] As explained for [1e], Nega-Roberts teaches the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead, and a third lead is coupled to the transistor device and provides a source sensing functionality.

c. [17b] a housing,

[0202] [17b], like claim 4, requires a housing. Nega-Roberts-Otremba433 discloses a housing for the reasons explained for claim 4.

d. [17c] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

[0203] [17c] is identical to [1d]. Nega-Roberts teaches [17c] for the reasons explained for [1d].

e. [17d] wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces,

[0204] [17d] is identical to claim 4. Nega-Roberts-Otremba124 teaches [17d] for the reasons explained for claim 4.

f. [17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad,

[0205] [17e] is similar to [1f] except that it requires a Group III nitride-based transistor device rather than a general compound semiconductor device.

[0206] As explained for [17a] and claim 2, Nega discloses a Group III nitride-based transistor device.

[0207] Nega-Roberts teaches the remainder of [17e] for the reasons explained for [1f].

g. [17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

[0208] [17f] is identical to [1g]. Nega discloses [17f] for the reasons explained for [1g].

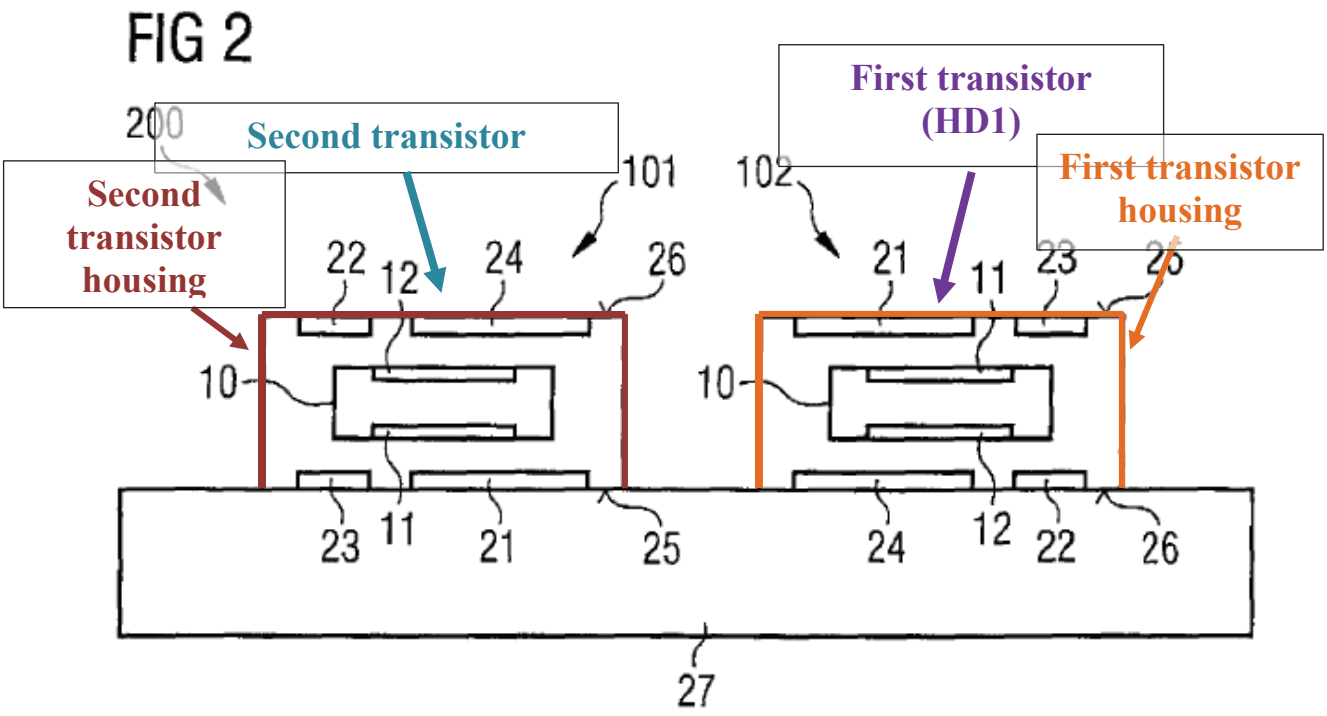
E. Ground 1E: Nega in view of Roberts and Otremba631 Renders Claims 12 and 13 Obvious

1. Claim 12 - The switch circuit of claim 10, wherein the first transistor device is housed in a package comprising a first die pad coupled to a drain of the first transistor device and the second transistor device is housed in a package comprising a second die pad coupled to a source of the second transistor device.

[0209] Claim 12 differs from claim 1 because it requires two separate packages, each containing a single transistor, coupled to a common board. As explained for claim 10, Nega-Roberts discloses a single package containing two

transistors, but it would have been obvious or at least a suitable alternative to separately package each transistor and couple both to a common board, as disclosed by Otremba631.

[0210] Otremba631 discloses packaging two transistors in separate housings and mounting surfaces coupled to a common circuit board. Otremba631, Fig. 2. Otremba631 states, "The first device 101 is mounted on the circuit board 27 with its first mounting surface 25 facing the circuit board 27. The second device 102 is mounted on the circuit board 27 with its second mounting surface 26 facing the circuit board 27." Otremba631, 4:64-67.



Otremba631, Fig. 2 (annotated).

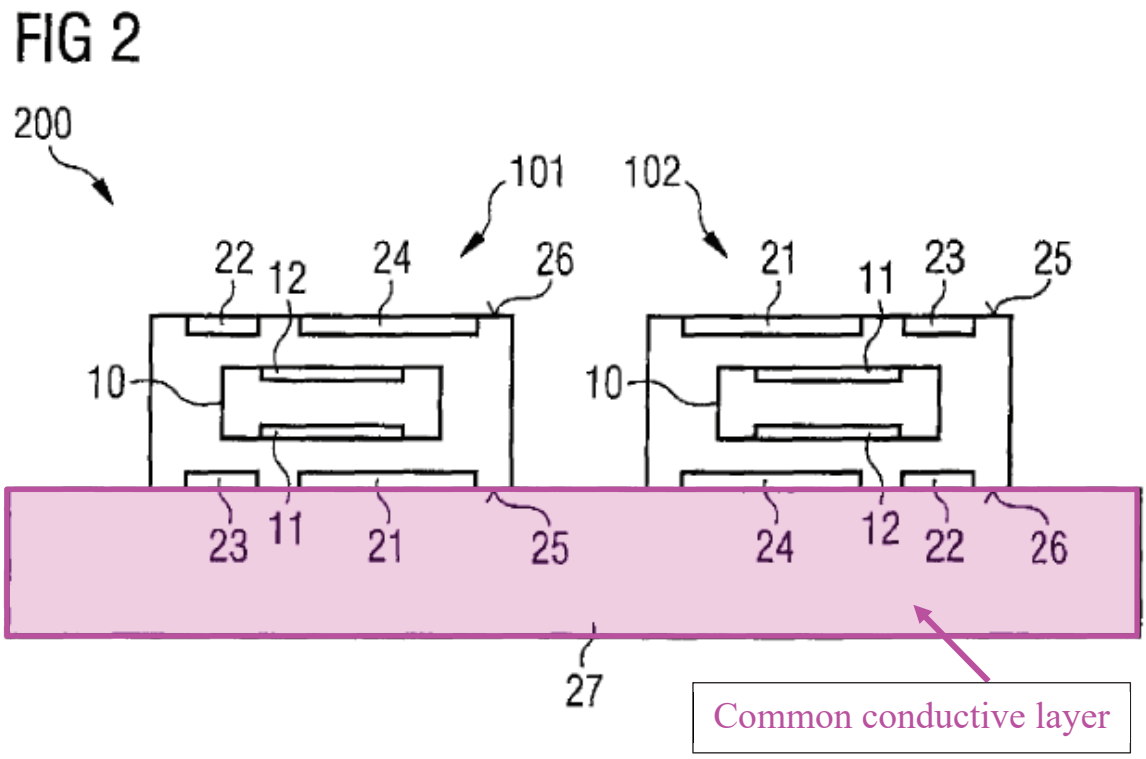
[0211] A POSITA would have been motivated to house each of Nega's transistors separately and connect them to a common circuit board, as disclosed in Otremba631 because packaging two transistors in a single package and packaging each transistor separately were known alternatives of one another—each achieving the same result, a dual-transistor switch circuit. Each alternative was suited to different design preferences and application needs, both at least constituting suitable options for achieving the desired switch circuit. Ex-1023, 19-21 (describing mounting discretely packaged components to a board like a "PCB, IMS (insulated metal substrate) and SMT boards," the benefit of discrete components being to "provide[] a 'self contained environment' that allows the components to be tested, transported and used at the next higher level of packaging [(e.g., mounted to a board)] while buffering electrical, mechanical and chemical discontinuities form the next level.").

[0212] In addition, a POSITA would have been motivated to house Nega's two transistors separately when considering thermal conditions of the packaging. Two separate transistor packages create a lower thermal impedance than a single package. A POSITA would also have recognized that two separate packages would last longer and be more reliable than a single package and provide a more efficient cost/yield advantage.

[0213] Further, a POSITA would have had an expectation of success implementing Otremba631's separately packaged transistors to implement a switch circuit because it would have been a simple swap of one known packaging configuration for another—with the electronic characteristics of the overall circuit maintained—applying only conventional manufacturing processes and techniques with no undue experimentation. And combining Otremba631's separately packaged transistors with Nega's switch circuit would have provided better thermal considerations, as described above.

2. Claim 13 – The switch circuit of claim 12, wherein the first die pad and the second die pad are mounted on a common conductive layer.

[0214] As explained for claim 12, Otremba631 discloses two transistor devices mounted on a common conductive layer, circuit board 27. Otremba631, 4:64-67, Fig 2. Otremba631 states, "the first device 101 is mounted on the circuit board 27 with its first mounting surface 25 facing the circuit board 27. The second device 102 is mounted on the circuit board 27 with its second mounting surface 26 facing the circuit board 27." Otremba631, 4:64-67.



Otremba631, Fig. 2 (annotated).

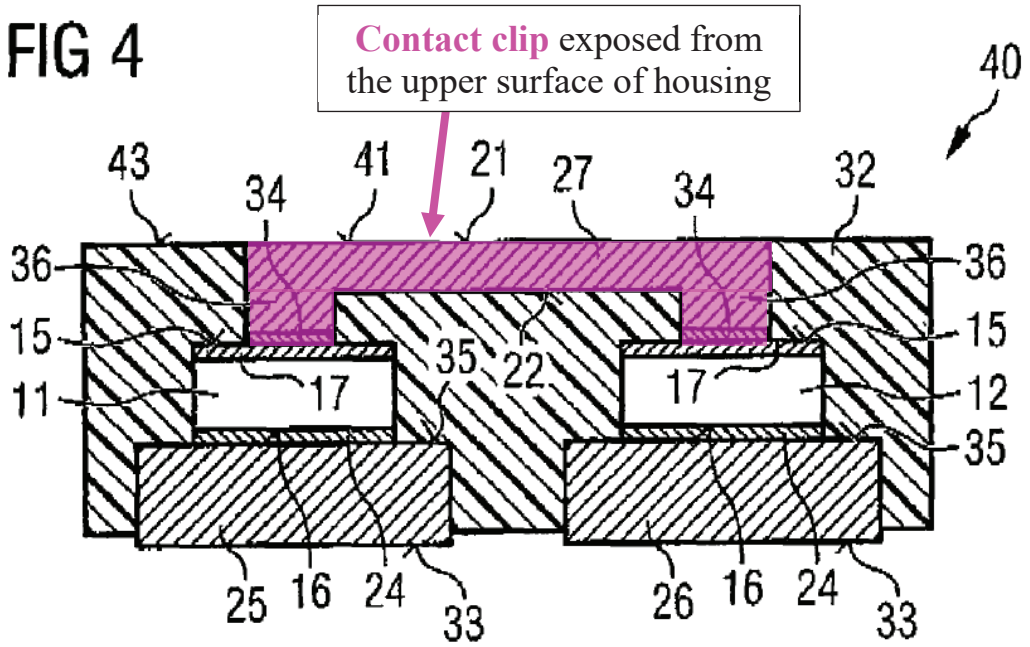
[0215] A POSITA would have been motivated to house each of Nega's transistors separately and connect them to a common circuit board, as disclosed in Otremba631 for the reasons explained for claim 12.

F. Ground 1F: Nega in view of Roberts and Otremba280 Claims 14 and 15 Obvious

1. Claim 14 – The switch circuit of claim 10, wherein a first contact clip is coupled to one of a source and a drain of the first transistor device and a second contact clip is coupled to the other one of a source and a drain of the second transistor device, wherein the first contact clip and the second contact clip are at least partially uncovered.

[0216] As explained for Ground 1A [10c], Nega's first transistor device and the second transistor devices are coupled to create a serial or antiserial current path. Nega teaches coupling the components using bond wires, but contact clips were commonly known alternatives, and exposing the contact clips provided known benefits, both of which are expressly disclosed by Otremba280.

[0217] Otremba280 discloses using contact clips to couple components within a device, including transistor devices. Otremba280 states that its electronic component includes "a contact clip 14 [that] is exposed from the plastic encapsulation compound 32 [(housing)]." Otremba280, 8:33-41; Fig. 4.



Otremba280, Fig. 4 (annotated).

[0218] Otremba280 expressly teaches suggests and motivates exposing the contact clip from the housing because the "exposed area 41 of the contact clip 14 provides a shorter path of thermal resistance" with "the environment around the electronic component 40." Otremba280, 8:45-47. By exposing the clip, the "thermal performance of the electronic component 40 may be increased due to an improvement in the efficiency of thermal dissipation from the electronic component 40." Otremba280, 8:47-51. To realize the thermal benefits, a POSITA would have been motivated to implement Otremba280's exposed contact clip in Nega-Roberts to couple, for example, Nega's first transistor device's drain

electrode (first current electrode) and LF1 (die pad) and Nega's second transistor device's source electrode and LF1.

[0219] A POSITA would have been motivated to use a contact clip, as taught by Otremba280, to couple Nega-Roberts's transistor devices for the same reasons explained in Ground 1D above.

2. Claim 15 – The switch circuit of claim 14, wherein the first contact clip and the second contact clip are coupled to a common heat dissipation member.

[0220] Otrembra280 also discloses claim 15 because Otremba280 disclose a heatsink coupled to the contact clip.

[0221] Otremba280 discloses that "[a]n additional heat sink or cooling element may be positioned on the upper surface 42 of the electronic component 40. In an embodiment, an additional heat sink may be positioned directly on the exposed regions 41 of the contact clip 14. The additional heat sink may be in electrical connection with the contact clip 14 if the contact clip 14 is connected to ground potential." Otremba280, 8:51-57. A POSITA would have understood that Otremba280's use a of a heat sink is the same as what is disclosed by the '481 patent because both disclosures relate to placing a heat sink on the exposed region of the clip. For example, the '481 patent states that "The exposed region of the contacts clip may be used as cooling surface on to which an additional heat dissipation device such as a heat sink may be mounted." '481 patent, 6:66-7:2.

[0222] A POSITA would have been motivated to include Otremba280's heat sink in Nega-Roberts switch circuit because Otremba280 expressly teaches and motivates improving the efficiency of thermal dissipation from the electronic component. *See* Otremba280, 8:48-51. By adding a heat sink, the "thermal performance of the electronic component 40 may be increased due to an improvement in the efficiency of thermal dissipation from the electronic component 40." Otremba280, 8:47-51. To realize the thermal benefits, a POSITA would have been motivated to implement Otremba280's heat sink in Nega-Roberts. A POSTA would have known that adding heat sinks to a contact clip was a commonly-known way to dissipate thermal energy from an electronic component.

[0223] Further, a POSITA would have had an expectation of success in implementing Otremba280's heat sinks onto its contact clip and Nega-Robert's switch circuit because it would have been a simple addition of a known component and would have needed to apply only conventional manufacturing processes and techniques to implement.

XII. LIU GROUNDS 2A-2F (CLAIMS 1-9 AND 17)

A. Liu Is Prior Art Because Its Provisional Application Was Filed Before the Priority Date of the '481 Patent

[0224] Liu was issued on February 23, 2021, claiming priority to U.S. Provisional Application No. 62/196,629 ("Provisional"), filed July 24, 2015—before the earliest possible priority date of the '481 patent. Because the subject matter of Liu Petitioners rely on is fully supported by its provisional application, Liu is considered to have been effectively filed under 35 U.S.C. 102(d)(2) "as of the filing date of the earliest such application that describes the subject matter"—July 24, 2015.

[0225] The subject matter of Liu Petitioners rely on is fully supported in the Provisional, as shown by the parallel citations to both Liu and its Provisional. Further, a representative claim of Liu is fully supported by the Provisional.

1. Petitioners' Cited Disclosures of Liu Are Supported in the Provisional

[0226] Liu and its Provisional are nearly identical. Every figure of Liu, including the cited figures, are identically included in Liu. And all cited disclosures of Liu are identical or nearly identical to those in its Provisional. I have cited to

both Liu and the Provisional throughout the Petition, and a complete mapping to specification citations is included here.[2]

Relied Upon Liu Subject Matter	Provisional Support
8:11-26: "A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421, wherein die attach material 421 is an electrically insulating die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically insulating die attach material 421. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip 40B includes a field effect semiconductor	**[00042]:** "A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 42, wherein die attach material 42 is an electrically and thermally conductive die attach material. Thus, surface 44 is bonded to surface 138A of device receiving area 138 through an electrically and thermally conductive die attach material 42. In accordance with an embodiment, semiconductor chip 40B is a compound semiconductor chip having opposing major surfaces 44 and 46, wherein semiconductor chip

[2] Because the Figures are identical in Liu and its Provisional, with only minor variations in numbers (e.g., 42I in Liu Figure 11 corresponds to 42 in Provisional Figure 11, 42I in Liu Figure 12 corresponds to 56 in Provisional Figure 12, and 90 in Liu Figure 12 corresponds to 133 in Provisional Figure 12 , they are omitted from this chart.

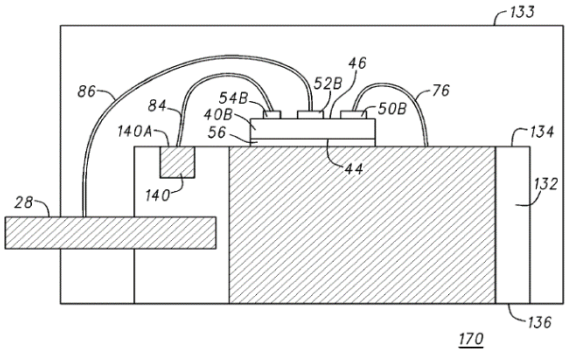
device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact MB formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10."	40B includes a field effect semiconductor device having a drain contact 50B formed on a portion of an active area of semiconductor device 40B, a source contact 52B formed on another portion of the active area of semiconductor device 40B, and a gate contact 54B formed on another portion of the active area of semiconductor device 40B. Semiconductor device 40B has been described with reference to FIG. 10."
8:27-48: "Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact MB of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically	**[00043]:** "Drain contact 50B of semiconductor device 40B is electrically connected to device receiving area 138 through bond wires 76, source contact 52B of semiconductor device 40B is electrically connected to leadframe lead 28 through a bond wire 86 and to leadframe lead 30 through bond wires 88, gate contact 54B of semiconductor device 40B is electrically connected to leadframe lead 26 through bond wire 84. Bond pad 140 is electrically connected to leadframe lead 26 through

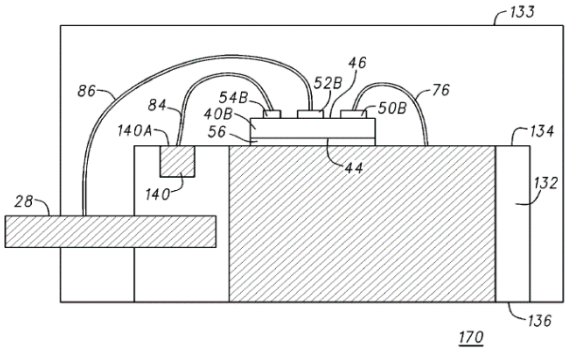
connected to leadframe lead 26 through a bond wire 172 and to gate contact MB through bond wire 83. In accordance with the embodiment of FIGS. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172."	a bond wire 172. In accordance with the embodiment of FIGs. 11 and 12, leadframe lead 26 is a gate leadframe lead or a gate lead, leadframe lead 28 is a Kelvin leadframe lead or a Kelvin lead, and leadframe lead 30 is a source leadframe lead or a source lead. Bond wires may be referred to as wirebonds. It should be noted that in accordance with this embodiment drain contact 50B of semiconductor device 40B is electrically connected to surface 138A of device receiving area 138 by bond wire 172."
3:55-58: "[S]emiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride."	**[00021]:** "[S]emiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride semiconductor chip 40 comprises aluminum nitride."
4:60-5:3: "FIG. 4 is a perspective view of a semiconductor component 100 in accordance with another embodiment of the present invention.	**[00027]**: "FIG. 4 is a perspective view of a semiconductor component 100 in accordance with another embodiment of the present invention.

Semiconductor component 100 is similar to semiconductor component 10 except that bond wires 76 have been replaced by an electrically conductive clip 102, bond wires 78 have been replaced by an electrically conductive clip 104, and bond wires 88 have been replaced by an electrically conductive clip 106. It should be noted that mounting semiconductor chips 40 and 60 to device receiving areas 18 and 20, respectively, have been described with reference to FIGS. 1 and 2."	Semiconductor component 100 is similar to semiconductor component 10 except that bond wires 76 have been replaced by an electrically conductive clip 102, bond wires 78 have been replaced by an electrically conductive clip 104, and bond wires 88 have been replaced by an electrically conductive clip 106. It should be noted that mounting semiconductor chips 40 and 60 to device receiving areas 18 and 20, respectively, have been described with reference to FIGs. 1 and 2."
7:33-38: "As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40A and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 16, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example mold compound 90."	**[00038]**: "As those skilled in the art are aware, device receiving areas 18 and 20, semiconductor chips 40A and 60, and bond wires 80, 82, 84, 86, and 88, clips 102, 104, and 106, and portions of molded support structure 12 are typically encapsulated in a protection material such as, for example a mold compound."

2. Claim 1 of Liu Is Supported in the Provisional

[0227] The Provisional supports Liu's claim 1:

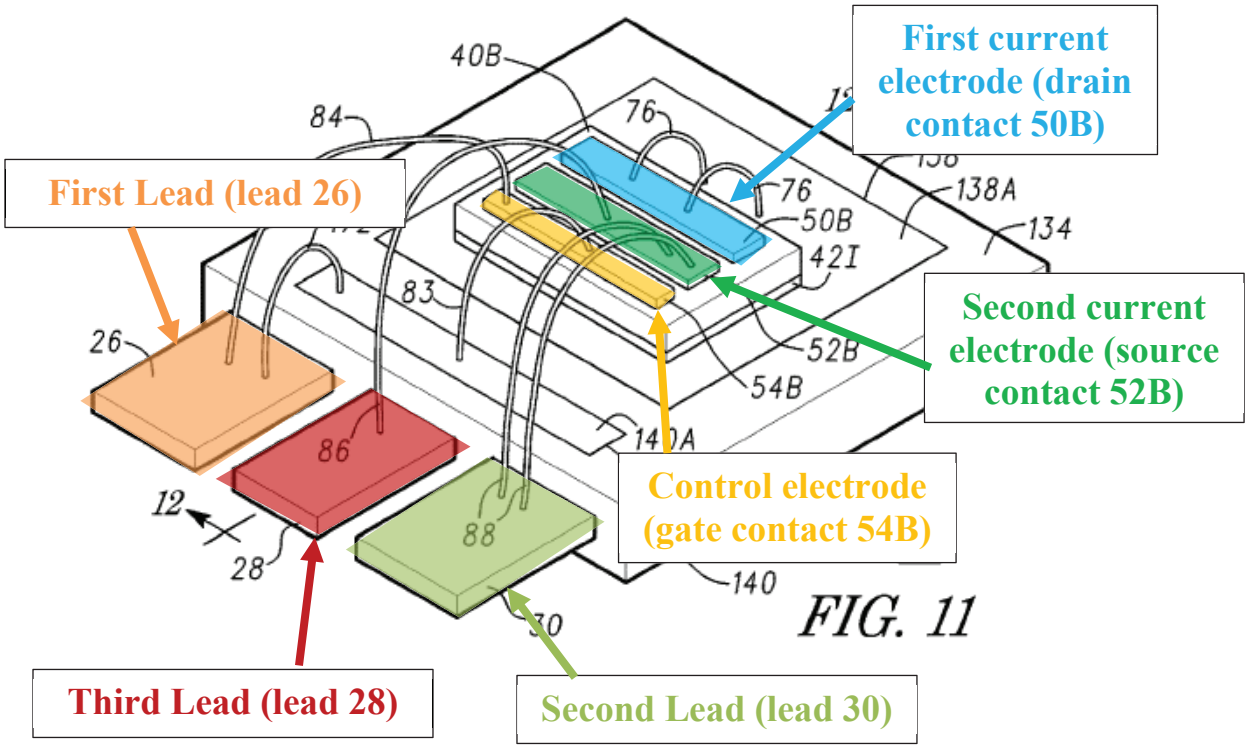
Liu Claim 1	Provisional Support
"1. A semiconductor component comprising:"	**Claim 1:** "A semiconductor component having at least first and second terminals, comprising:"
"a molded support structure having a top surface and a bottom surface, the molded support structure including:"	**[00020]:** "a molded device support structure 12 having a top surface 14 and a bottom surface 16."
"a device receiving structure embedded in a first portion of the molded support structure, the device receiving structure extending from the top surface into the molded support structure;"	**[00020]:** "Molded support structure 12 includes a device receiving area 18…and a bond pad 22 at top surface 14 and a contact at bottom surface 16." **[00020]:** "Device receiving areas 18 and 20 may be referred to as device receiving structures." **Fig. 12:**  *FIG. 12*

"a first bond pad embedded in a second portion of the molded support structure;"	**[00020]:** "molded support structure 12 includes… a bond pad 22 at top surface 14."
"a first leadframe lead extending from a third portion of the molded support structure, the first leadframe lead vertically positioned between the first bond pad and the bottom surface;" "a second leadframe lead extending from a fourth portion of the molded support structure, the second leadframe lead vertically positioned between the first bond pad and the bottom surface;"	**[00020]:** "Leadframe leads 26, 28, and 40 protrude from a side or an edge of molded device support structure 12." **Fig. 12:**  *FIG. 12*
"a semiconductor device bonded to the device receiving structure, the semiconductor device having a control electrode, a first current carrying electrode, and a second current carrying electrode;"	**Claim 1: "**a first semiconductor device mounted to the first receiving structure, the first semiconductor device having a control terminal and first and second current carrying terminals and configured from III-N semiconductor material;"
"a first electrical interconnect coupling the first leadframe lead to the first current carrying electrode of the semiconductor device;"	**Claim 1:** "a first electrical interconnect coupled between the control terminal of the first semiconductor device and a first lead of the plurality of leads;"

"a second electrical interconnect coupling the second leadframe lead to the control electrode of the semiconductor device;"	**Claim 1:** "a second electrical interconnect coupled between the first current carrying terminal of the first semiconductor device and a second lead of the plurality of leads; and"
"a third electrical interconnect coupling the second current carrying electrode to the device receiving structure;"	**Claim 1:** "a third electrical interconnect coupled between the second carrying terminal of the first semiconductor device and one of the first device receiving structure or the first interconnect structure."
"a fourth electrical interconnect coupling a third leadframe lead to the first current carrying electrode of the semiconductor device; and"	**Claim 4:** "The semiconductor component of claim 1, further including a fourth electrical interconnect coupled between the first carrying terminal of the first semiconductor device and a third lead of the plurality of leads."
"a protection material over the semiconductor device, the first electrical interconnect, and the second electrical interconnect, and over at least a portion of the molded support structure."	**[00028]:** "…device receiving areas 18 and 20, semiconductor chips 40 and 60, … and portions of molded support structure 12 may be encapsulated in a protection material…"

B. Overview of the Combinations

[0228] **Liu** discloses all of claims 1-6. Liu discloses a semiconductor device with leads coupled to the various electrodes of its semiconductor chip and a device receiving area (die pad). Liu's **gate contact 54B (control electrode)** is coupled to a leadframe **lead 26 (first lead)**, Liu's **drain contact 50B (first current electrode)** is coupled to the **device receiving area 138 (die pad)**, and Liu's **source contact 52B (second current electrode)** is coupled to the leadframe **lead 30 (second lead)**. Liu, 8:27-33; Provisional, [00043]. Liu also discloses **lead 28 (third lead)** connected to "source contact 52B of semiconductor device 40B" that "is a Kelvin leadframe lead or a Kelvin lead." Liu, 8:27-40; Provisional, [00043].

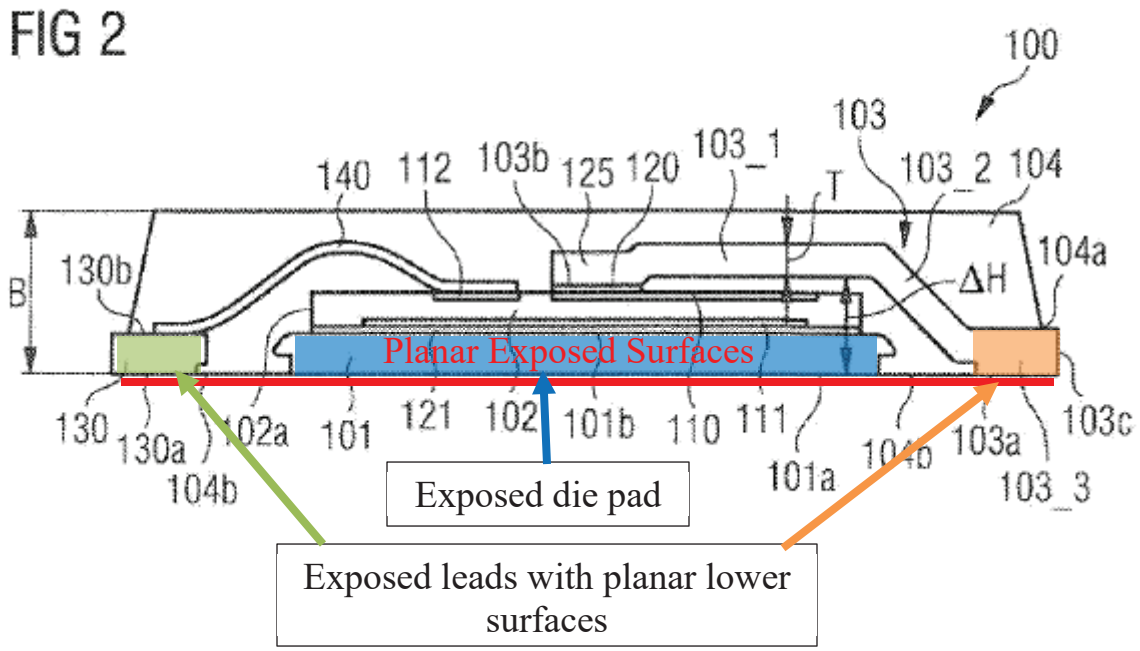


Liu, Fig. 11 (annotated); Provisional, Fig. 11.

[0229] **<u>Roberts</u>** discloses customary high voltage device blocking voltages and switching speeds (claims 3 and 17). Roberts discloses that transistor devices intended for high voltage applications, "e.g.[,] 600/650V" in "normally-on (depletion mode) transistors" were well known at the time (Roberts, [0006], [0012]), and that GaN transistors "provide <20 ns switching time and more than 30 A current switching capability" (equating to more than 1kHz switching speed) (Roberts, [0008]).

[0230] **<u>Otremba433</u>** discloses planar exposed leads and an exposed die pad (claims 4, 9, and 17). Otremba433 discloses "external contact area[s]" 103a

and 130a that are "coplanar with a reference plane defined by a bottom surface 101a of the carrier 101" (die pad) that is "exposed at the bottom of the package." Otremba433, [0037], [0039].

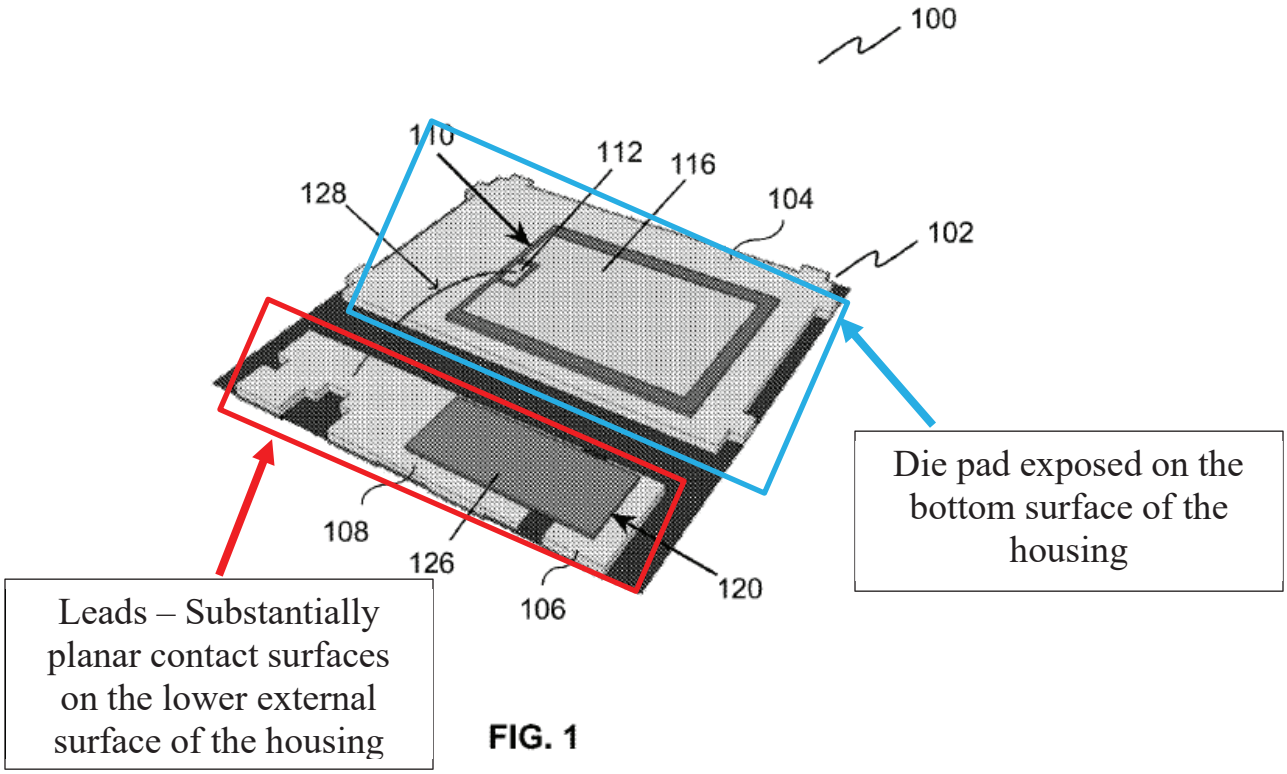


Otremba433, Fig. 2 (annotated).

[0231] Otremba433 also discloses coupling components with a "conventional contact clip" instead of bond wires. Otremba433, [0072].

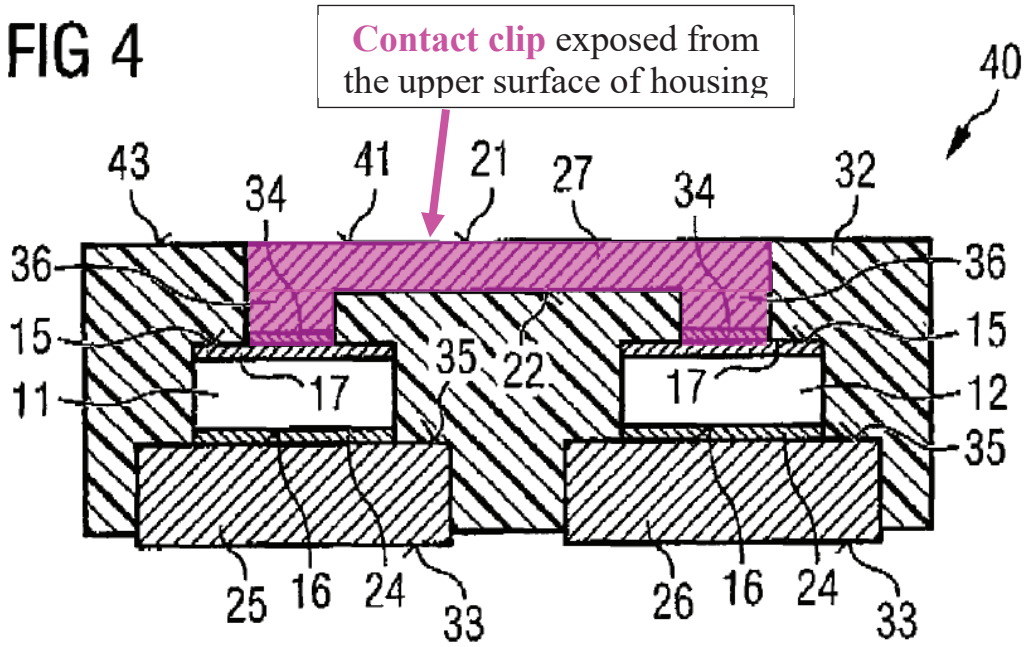
[0232] **<u>Otremba124</u>** discloses specific packaging requirements, like planar exposed leads and an exposed die pad (claims 4 and 17) in a ThinPAK8x8 design (claim 9). Otremba124 discloses a power transistor including a GaN HEMT "packaged in a[n] 8x8 ThinPAK." Otremba124, [0041]. Figure 1 shows the

ThinPAK8x8 package outline with flat source leads 108 and 106 on the bottom of the package.



Otremba124, Fig. 1 (annotated).

[0233] **<u>Otremba280</u>** discloses using exposed contact clips to couple components within a packaged device, rather than bond wires (claims 7 and 8). Otremba280's electronic component includes a "contact clip 14 [that] is exposed from the plastic encapsulation compound 32 [(housing)]." Otremba280, 8:33-41, Fig. 4.



Otremba280, Fig. 4 (annotated).

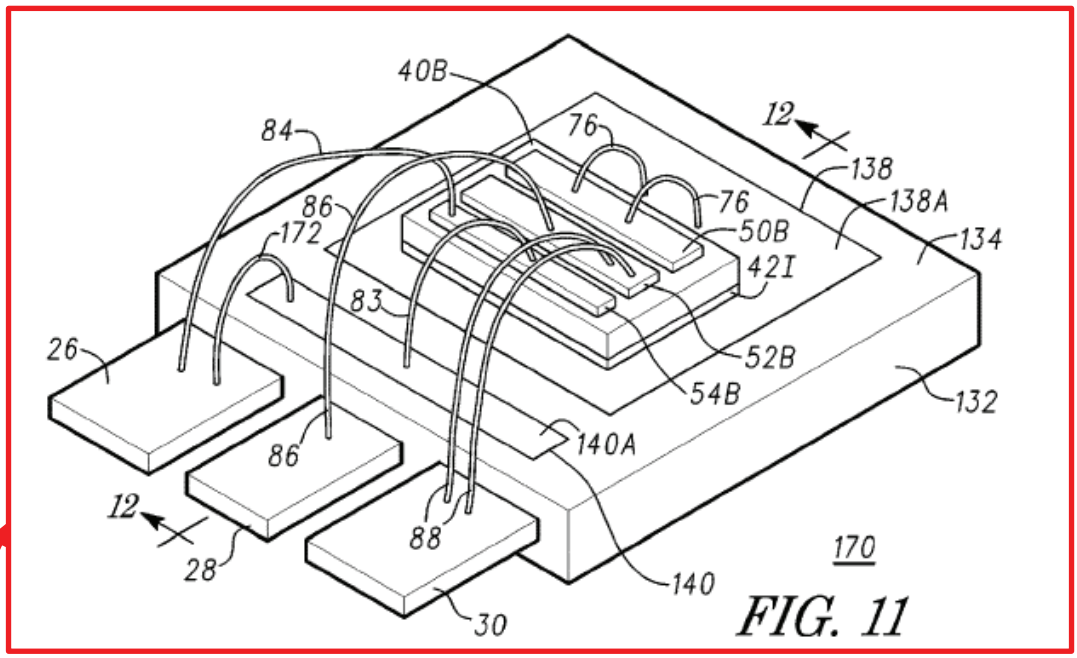
[0234] All references are analogous at least because they are in the same field of endeavor as the ’481 patent—packaging designs for semiconductor electronic components.

C. Ground 2A: Liu Renders Obvious Claims 1, 2, and 4-6

1. Claim 1

a. [1pre] An electronic component, comprising:

[0235] To the extent limiting, Liu discloses [1pre] because it discloses a “semiconductor component 170.” Liu, 8:1-3, Fig. 11; Provisional, [00041], Fig. 11.



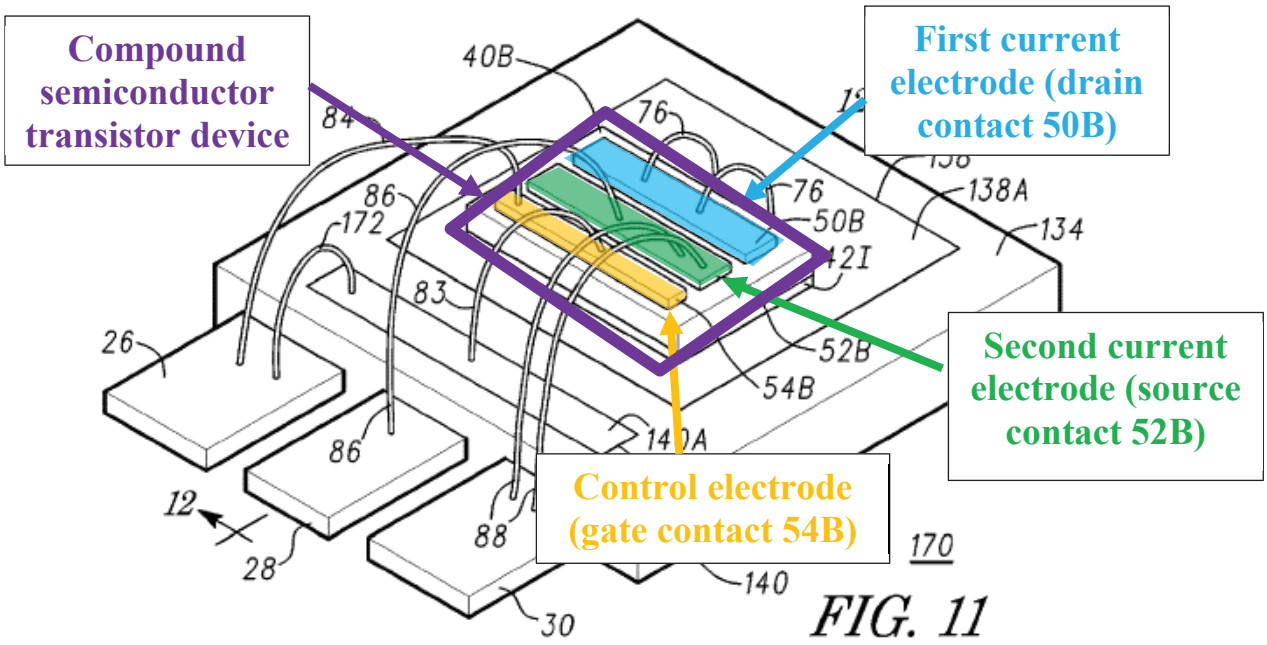
Electronic component (component 170)

Liu, Fig. 11 (annotated); Provisional Fig. 11.

b. [1a] a compound semiconductor transistor device comprising a first current electrode, a second current electrode and a control electrode,

[0236] Liu discloses [1a] because Liu's semiconductor component 170 includes a "**semiconductor chip 40B** [that] is a compound semiconductor chip." Liu, 8:16-25; Provisional, [0042]. Liu's semiconductor chip 40B includes a **drain contact 50B (first current electrode)**, a **source contact 52B (second current**

electrode), and a **gate contact 54B (control electrode)**.[3] Liu, 8:16-25; Provisional, [00042].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

[3] Gate contact 54B is referred to as gate contact MB in the specification describing Figure 11. Figure 11 has no MB, and 54B is described as the gate contact with reference to Figures 10 and 13 (Liu, 7:39-62, 8:49-63). A POSITA would therefore have understood that MB is a typo, and the gate contact of Figure 11 and corresponding description is 54B.

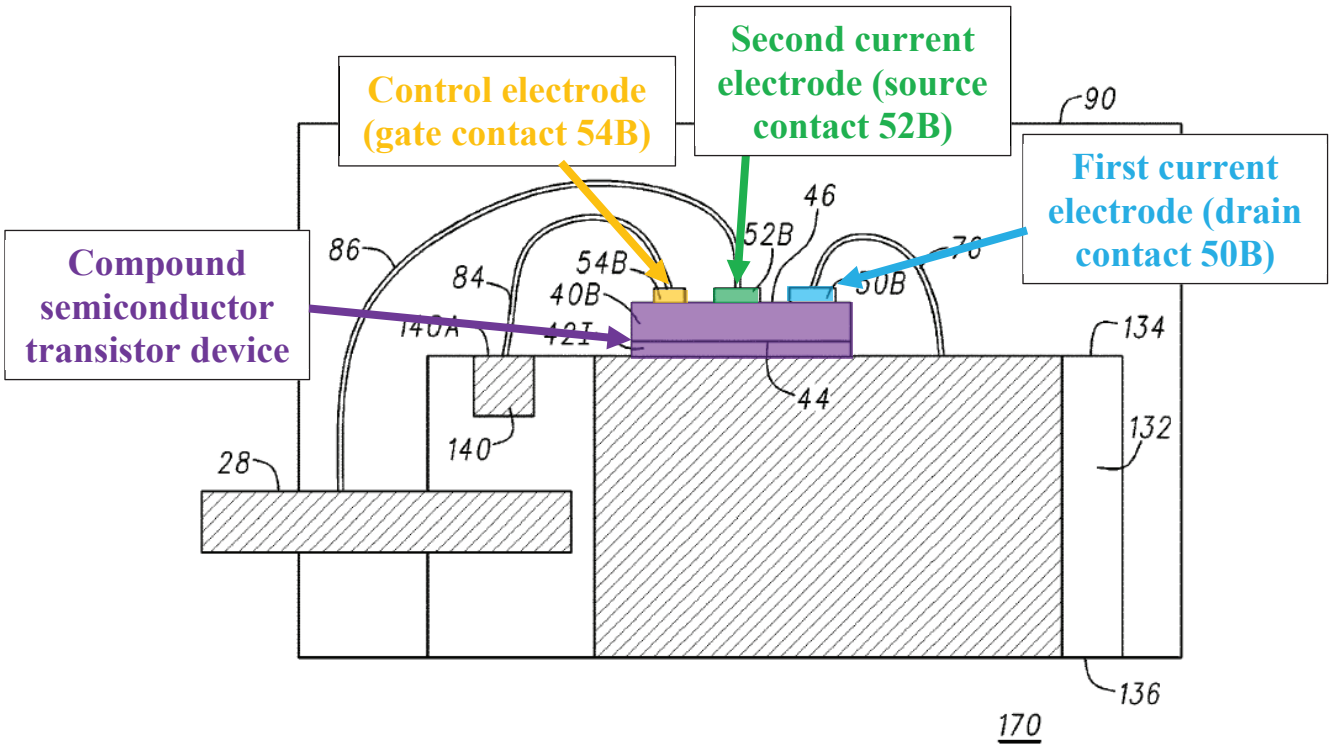


FIG. 12

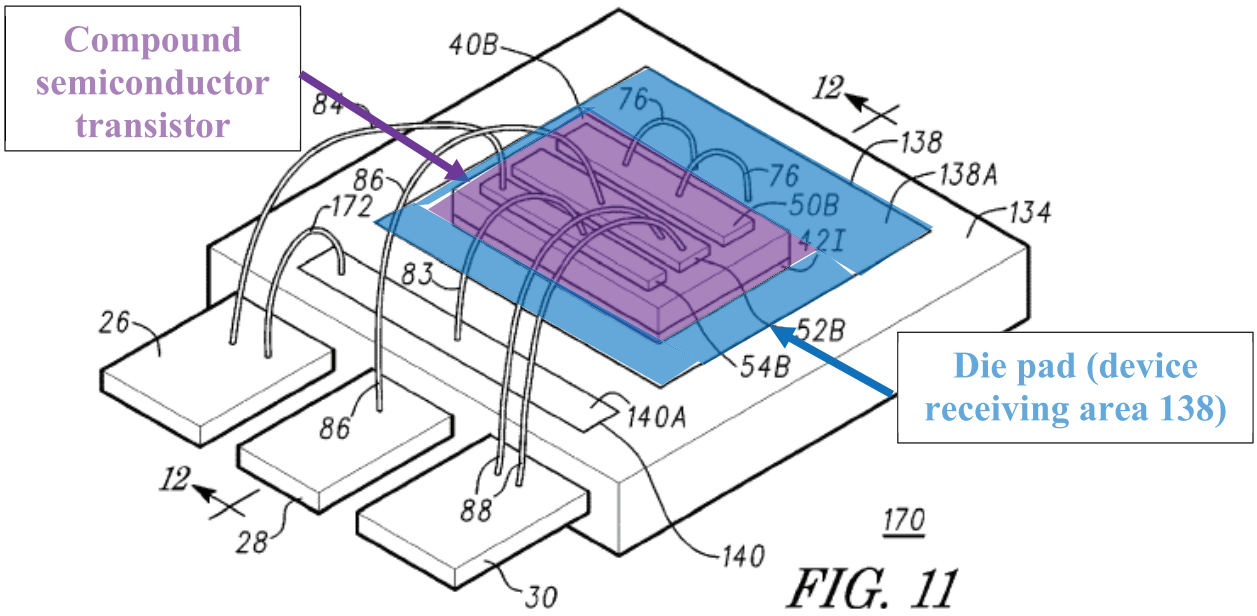
Liu, Fig. 12 (annotated); Provisional, Fig. 12.

c. [1b] a die pad; and

[0237] Liu discloses [1b] because it discloses a "device receiving area 138." Liu, 5:42-45; Provisional, [00031].

[0238] As explained for Ground 1A, element [1b], a die pad is a common component of a transistor device that serves as a mounting area for a chip. Liu's device receiving area 138 is comprised of surface 138A. Liu, 8:11-14; Provisional, [00042]. Surface 138A uses a die attach material 42I. Liu, 8:11-14; Provisional, [00042]. The **device receiving area 138**, which includes surface 138A and die attach material 42I, supports the semiconductor chip 40B mounted thereon,

and constitutes the claimed die pad. Liu, 8:11-16 ("A semiconductor chip 40B is bonded to surface 138A of device receiving area 138 using a die attach material 421 …."); Provisional, [00042].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

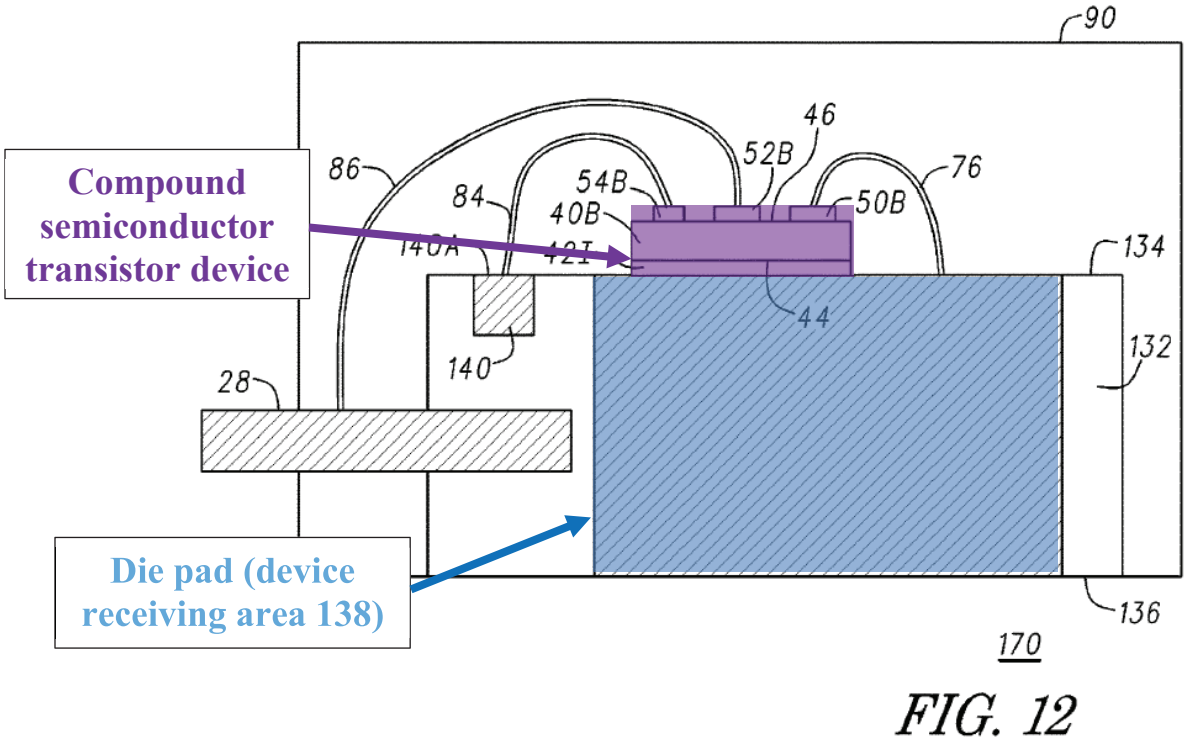


FIG. 12

Liu, Fig. 12 (annotated); Provisional, Fig. 12.

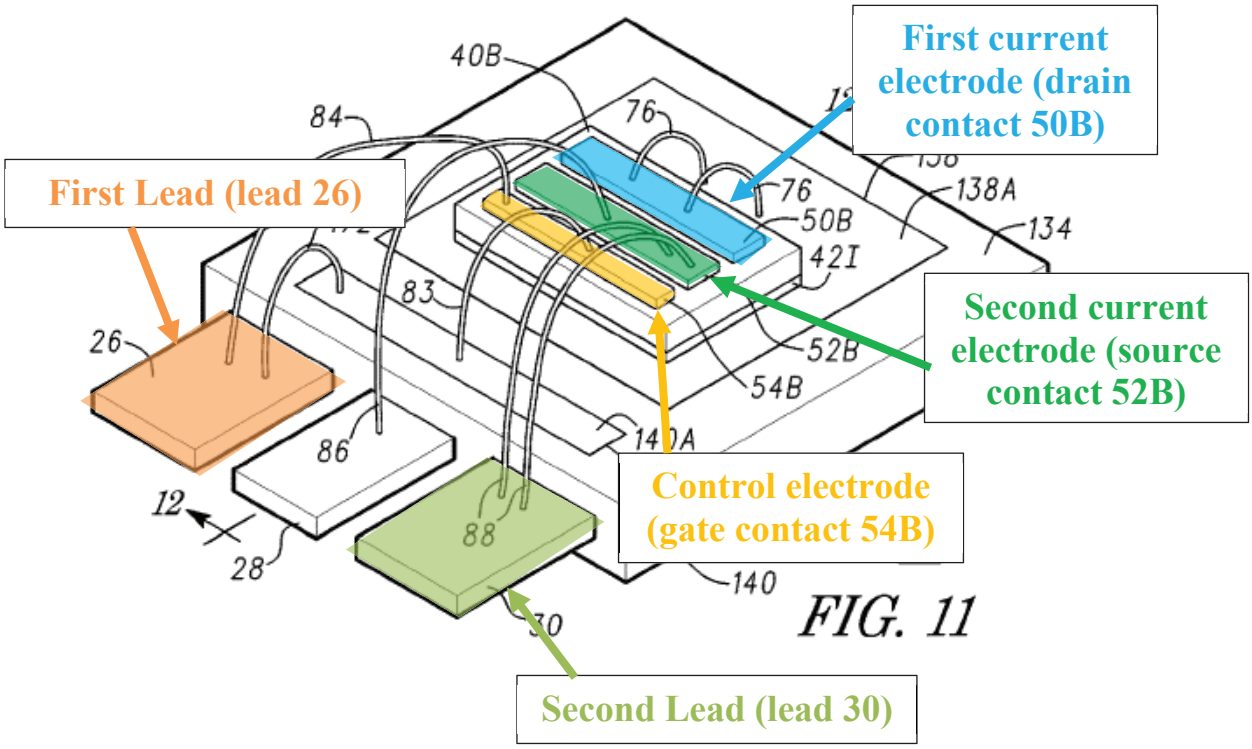
d. [1c] a first lead, a second lead and a third lead,

[1d] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

[1e] wherein the control electrode is coupled to the first lead, the first current electrode is coupled to the die pad, the second current electrode is coupled to the second lead and the third lead is coupled to the compound semiconductor transistor device and provides a source sensing functionality,

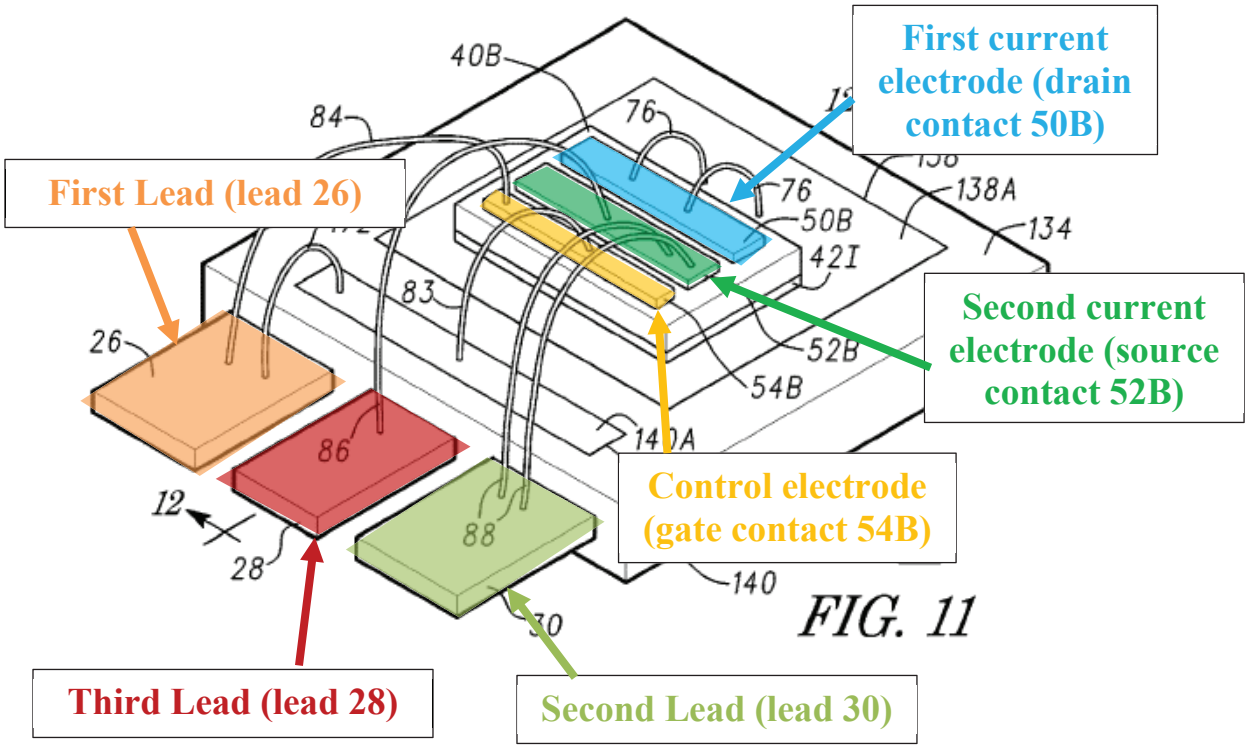
[0239] As explained for Ground 1A, [1c]-[1e] collectively recite three leads, and the various connections of components within the device.

[0240] As explained above for element [1a], Liu's semiconductor device includes a **drain contact 50B (first current electrode)**, a **source contact 52B (second current electrode)**, and a **gate contact 54B (control electrode)**. Liu, 8:16-25; Provisional, [00042]. Liu discloses leadframe leads coupled to the various electrodes of its semiconductor chip—lead 26 coupled to the gate control electrode (control electrode coupled to the first lead), lead 28 coupled to the transistor device (third lead to provide source sensing functionality), and lead 30 coupled to the source contact (second current electrode coupled to the second lead). Liu, 8:27-40; Provisional, [0043]. Liu's drain contact 50B (first current electrode) is coupled to the device receiving area 138. Liu, 8:27-33; Provisional, [00043]. As Figure 11 shows, Liu's **gate contact 54B (control electrode)** is coupled to a leadframe **lead 26 (first lead)**, Liu's **drain contact 50B (first current electrode)** is coupled to the **device receiving area 138 (die pad)**, and Liu's **source contact 52B (second current electrode)** is coupled to the leadframe **lead 30 (second lead)**. Liu, 8:27-33; Provisional, [00043].



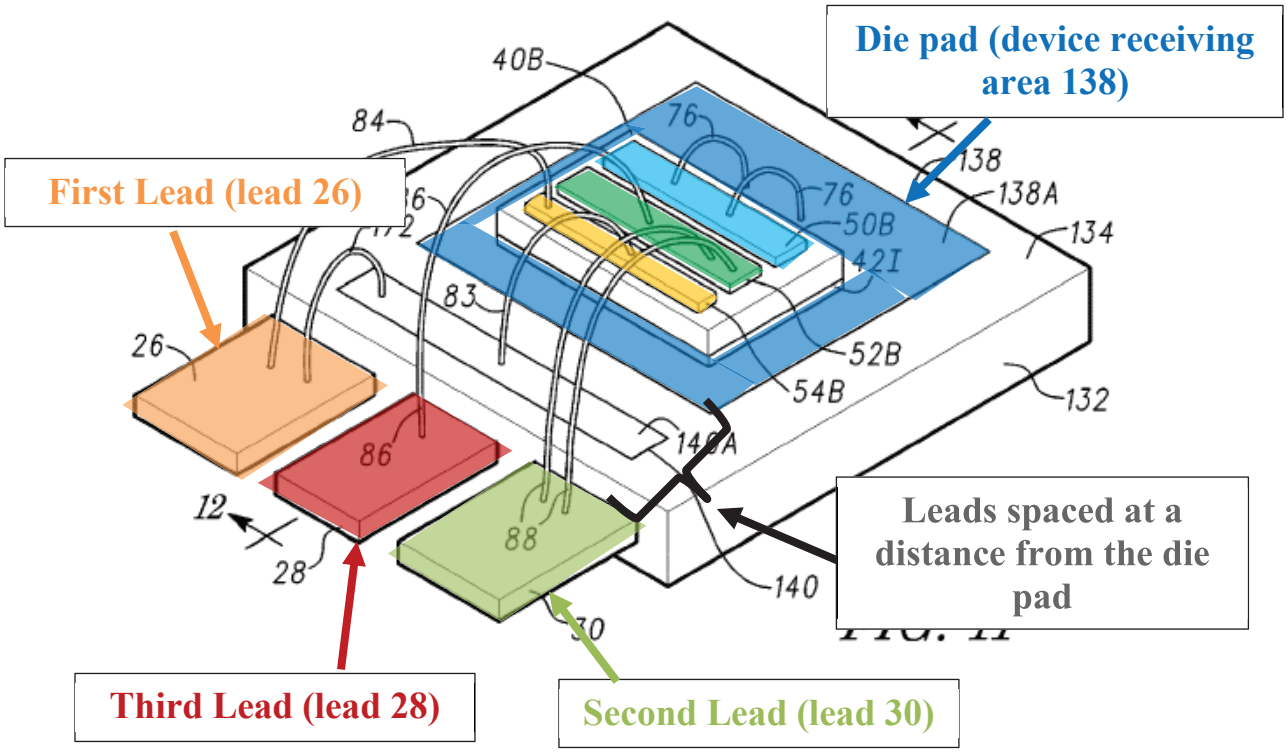
Liu, Fig. 11 (annotated); Provisional, Fig. 11.

[0241] Liu further discloses that leadframe **lead 28 (third lead)** is connected to "source contact 52B of semiconductor device 40B" (coupled to the compound semiconductor transistor device). Liu, 8:27-33; Provisional, [00043]. Liu's leadframe **lead 28** "is a Kelvin leadframe lead or a Kelvin lead." Liu, 8:27-33; Provisional, [00043]. A POSITA would have understood that a Kelvin leadframe provides monitoring and sensing to provide accurate measurements of resistance and voltage, and therefore, has a source sensing functionality. Ground 1A, [1c]-[1e] (explaining source sensing leads).

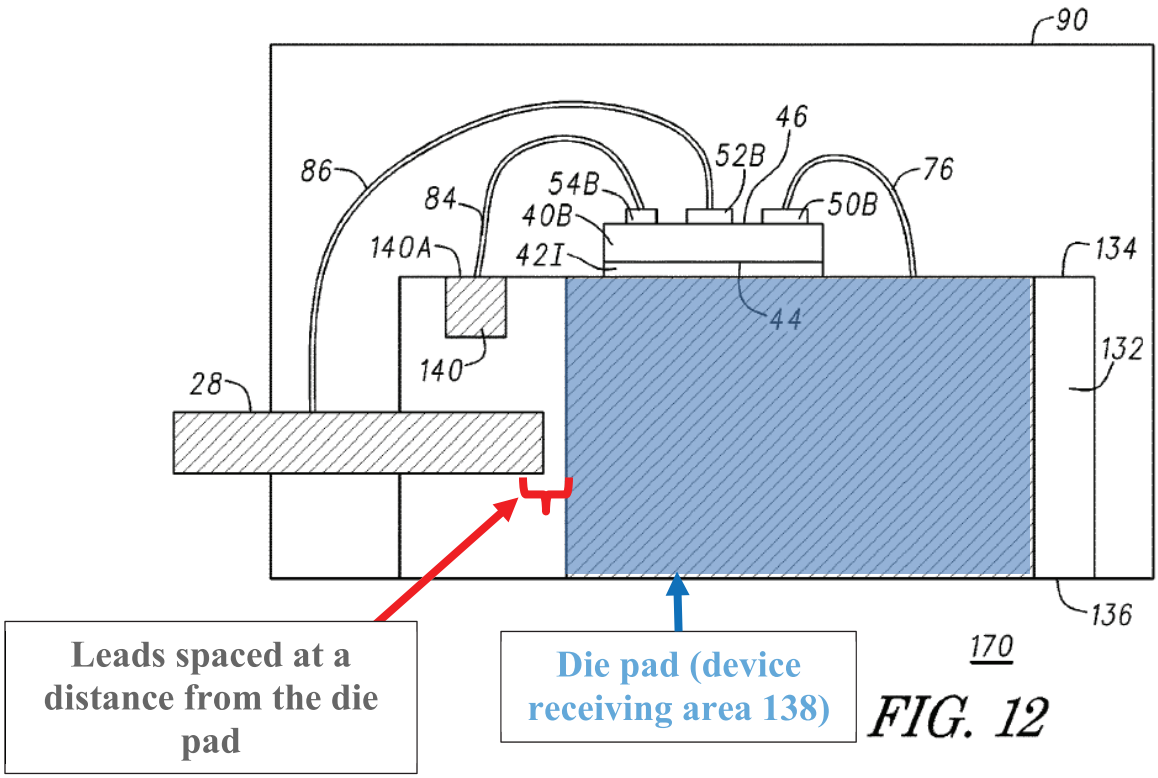


Liu, Fig. 11 (annotated); Provisional, Fig. 11.

[0242] Liu's leads are spaced a distance from the die pad 31.Liu, Fig. 11; Provisional, Fig. 11. Figures 11 and 12 show leadframe leads 26, 28, and 30 positioned a distance from Liu's device receiving area 138 (die pad).



Liu, Fig. 11 (annotated); Provisional, Fig. 11.



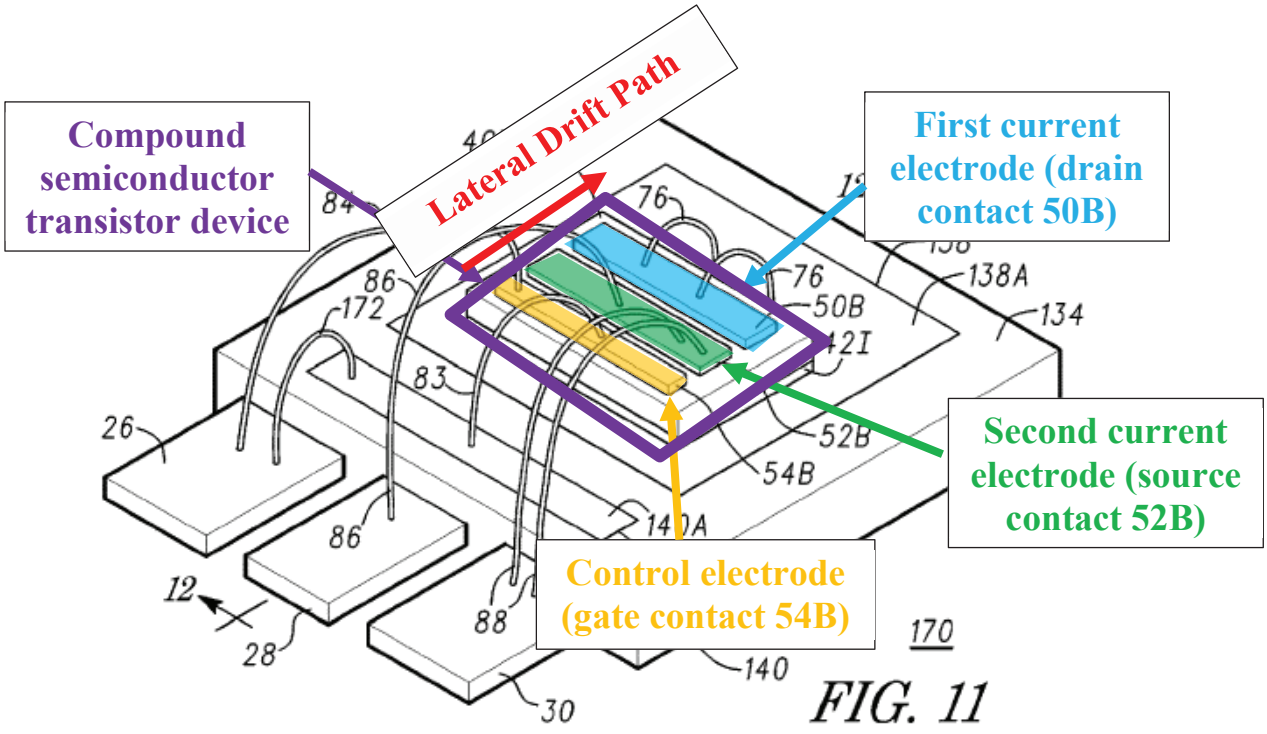
Liu, Fig. 12 (annotated); Provisional, Fig. 12.

e. [1f] wherein the compound semiconductor transistor device is a lateral transistor device and a drain or a source of the compound semiconductor transistor device is coupled to the die pad,

[0243] Liu discloses [1f] because Liu's semiconductor component 170 is arranged laterally, with the gate, source, and drain side-by-side on the same lateral plane, and the drain is coupled to the device receiving area 138 (die pad).

[0244] As explained above for Ground 1A, element [1f], the '481 patent explains that "lateral" means "run[ning] generally parallel to the lateral extent of a semiconductor material or semiconductor carrier" (Ex-1001, 3:14-18) and describes a device that "has a lateral drift path" (Ex-1001, 4:36-37). Liu's

source, drain, and gate are spread laterally across the semiconductor material and thus create a lateral drift path, as opposed to being stacked on top of one another in a vertical configuration.



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

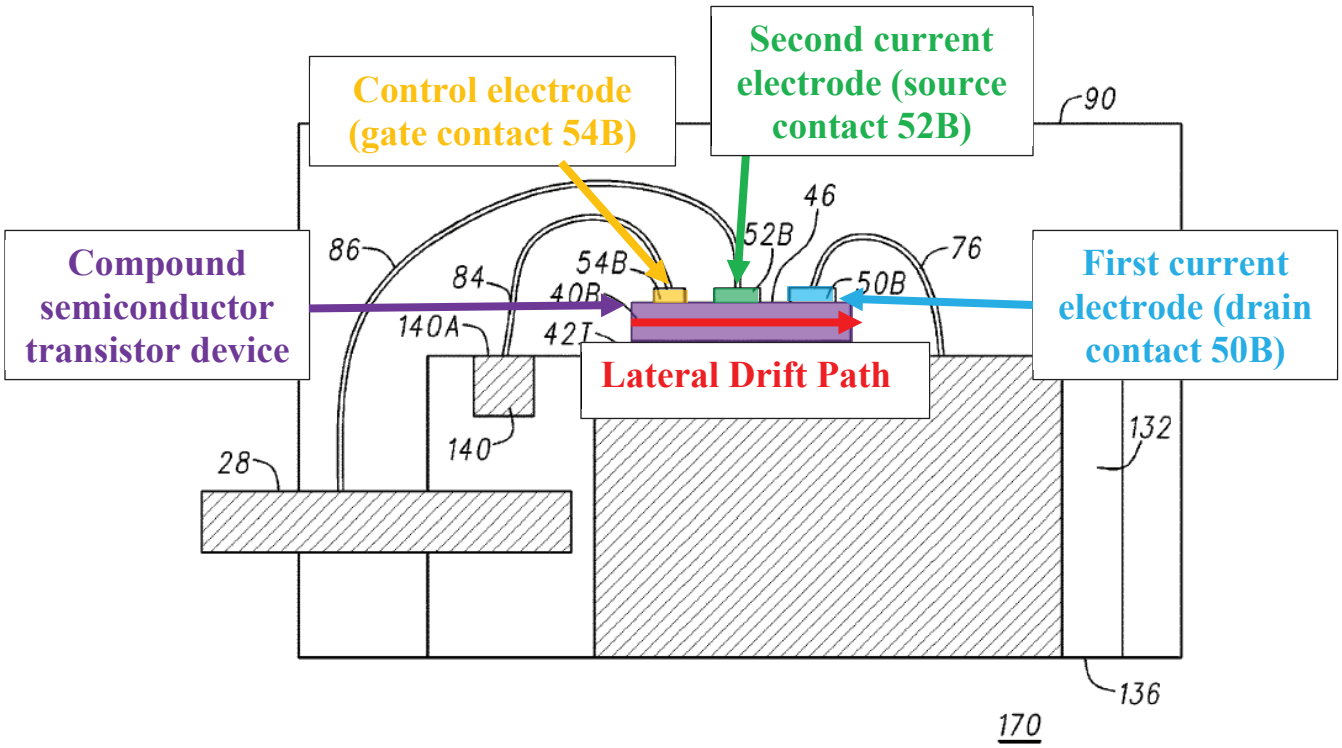


FIG. 12

Liu, Fig. 12 (annotated); Provisional, Fig. 12.

[0245] As explained for [1b], Liu's receiving area 138 is a die pad.

[0246] As explained for [1c]-[1e], Liu's drain is coupled to the receiving area 138 (die pad). Liu states, "**Drain contact 50B** of semiconductor device 40B is electrically connected to **device receiving area 138** through **bond wires 76** …." Liu, 8:27-33; Provisional, [00043].

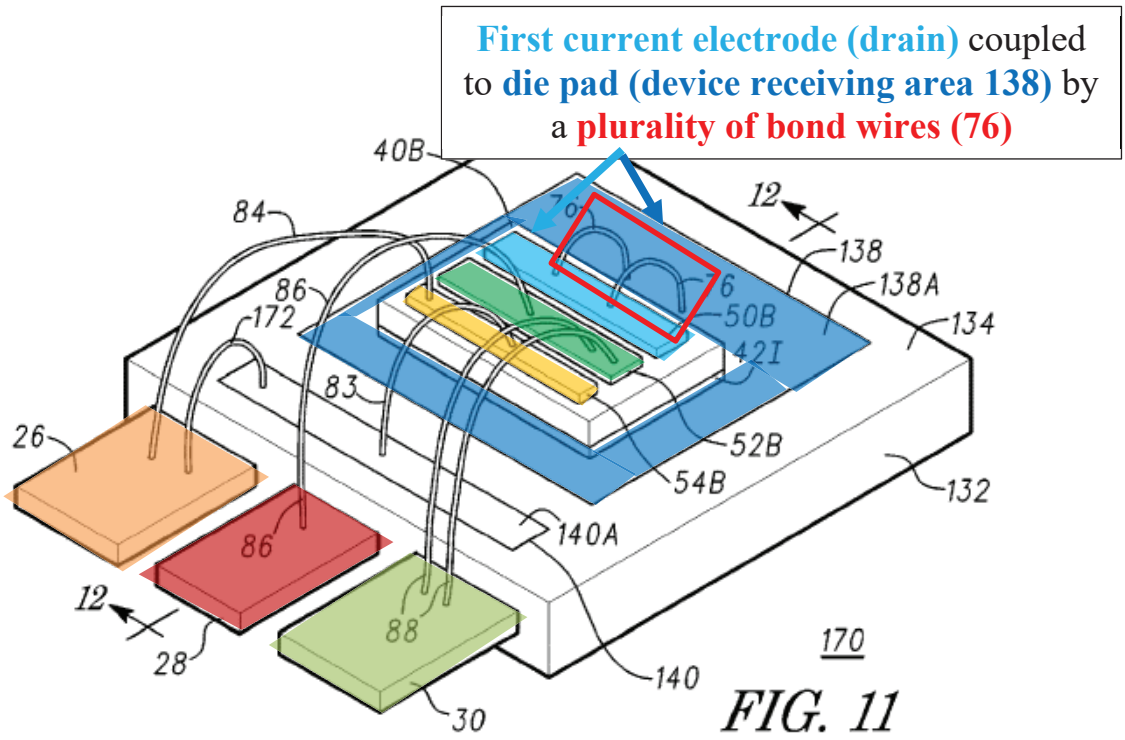


FIG. 11

Liu, Fig. 11 (annotated); Provisional, Fig. 11.

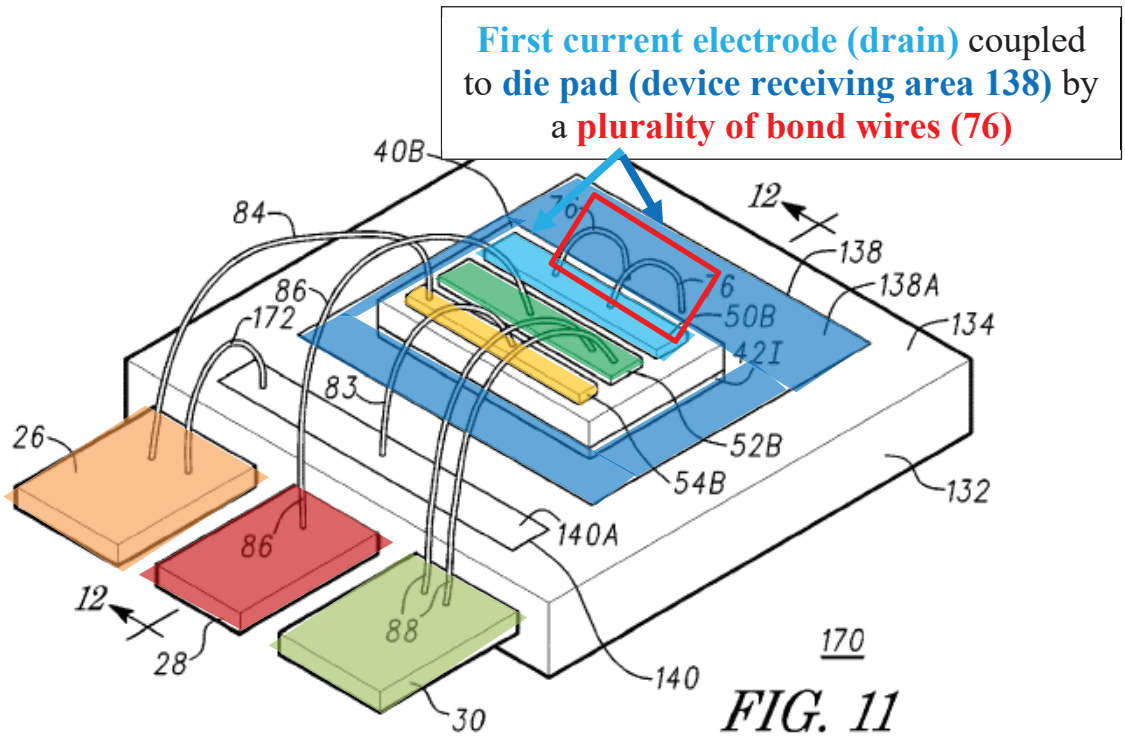
f. [1g] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

[0247] Liu discloses [1g] because, as explained for [1f], Liu's drain contact (first current electrode) is coupled to the die pad by two bond wires. Liu, 8:27-33, Fig. 11; Provisional, [00043], Fig. 11.

[0248] As explained for [1a], Liu discloses a drain contact 50B (first current electrode). Liu, 8:16-25; Provisional, [00042].

As explained for [1b], Liu discloses a device receiving area (die pad). Liu, 5:42-45; Provisional, [00031].

[0249] As explained for [1e]-[1f], Liu's drain contact 50B (first current electrode) is coupled to its device receiving area 138 (die pad) by bond wires. Liu states, "**Drain contact 50B** of semiconductor device 40B is electrically connected to **device receiving area 138** through **bond wires 76**," depicted as two (a plurality of) bond wires. Liu, 8:27-33; Provisional, [00043].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

2. Claim 2 - The electronic component of claim 1, wherein the compound semiconductor transistor device is one of a SiC transistor device, a III-V compound semiconductor transistor device and a Group III-nitride transistor device.

[0250] Liu discloses claim 2 because Liu's "semiconductor chip 40 is a III-nitride semiconductor chip, i.e., the substrate material of III-nitride

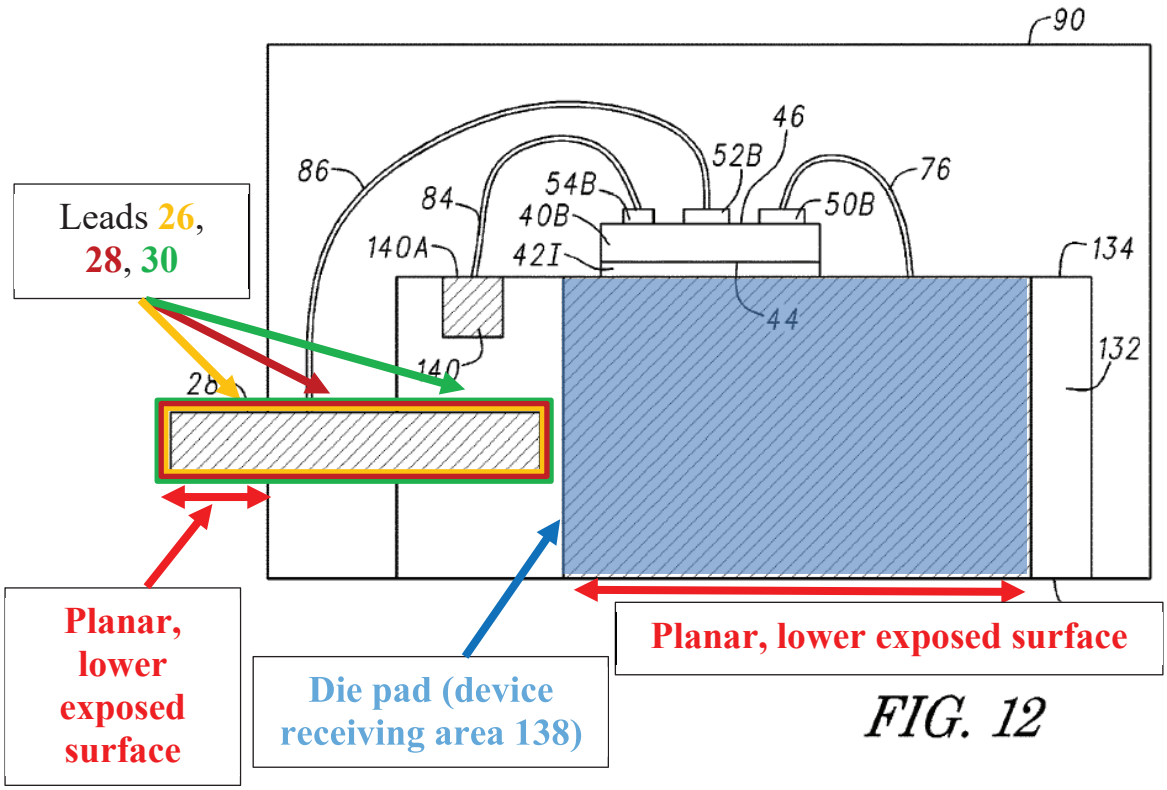
semiconductor chip 40 comprises aluminum nitride." Liu, 3:55-58; Provisional, [0021].

3. Claim 4 - The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.

[0251] Liu discloses claim 4 because its leads and die pad are exposed from its housing with substantially planar lower surfaces.

[0252] Liu discloses a housing because Liu discloses a mold compound 90 that encapsulates the device receiving area, semiconductor chip, and bond wires. Liu, 7:33-38; Provisional, [00038].

[0253] As explained for [1b]-[1e], Liu discloses three leads and a die pad. Figure 12 shows the lower surfaces of Liu's leads and die pad exposed from housing 90 with planer surfaces. Liu's device receiving area 138 (die pad) and leadframe leads 26, 28, and 30 are substantially flat (planar) contact surfaces.



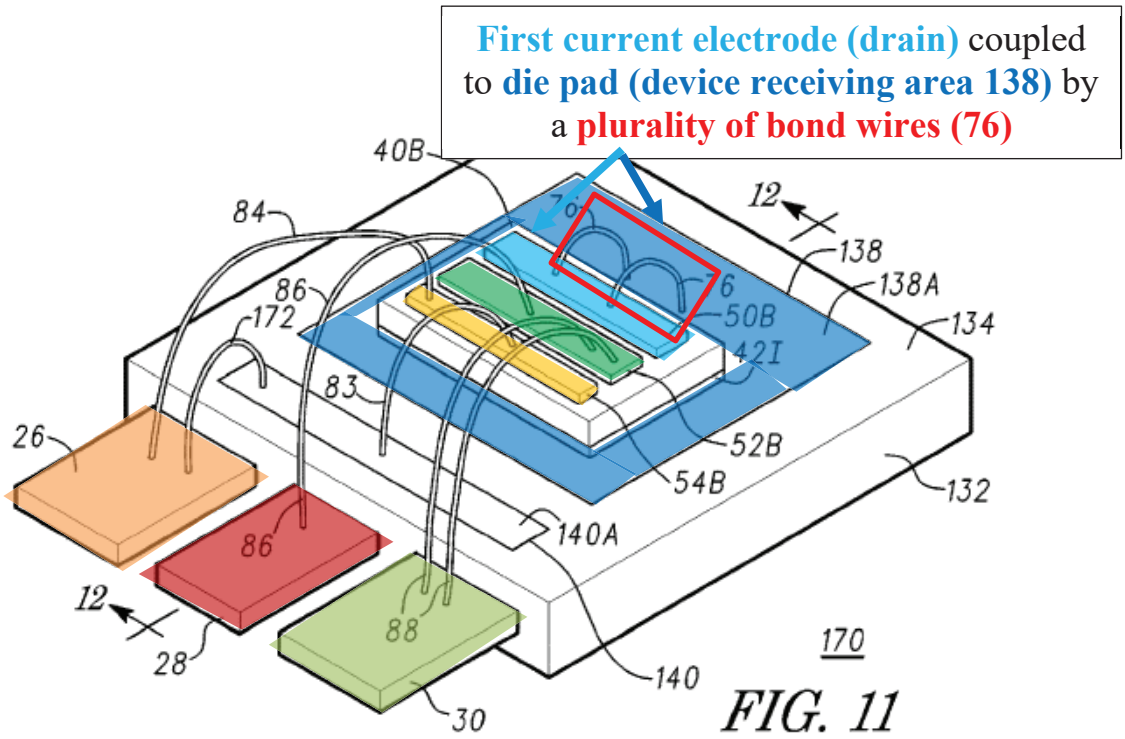
Liu, Fig. 12 (annotated); Provisional, Fig. 12[4].

4. Claim 5 - The electronic component of claim 1, wherein the compound semiconductor device is a vertical transistor device and a drain of the compound semiconductor transistor device is coupled to the die pad.

[0254] To the extent claim 5 is interpreted as requiring a **lateral transistor** (consistent with claim 1, *see* Ground 1A) where the drain of the device is coupled to the die pad, Liu discloses it for the reasons explained for [1e]-[1g].

[4] In the Provisional, the mold compound is number 133 of Figure 12.

Liu's **drain contact 50B (first current electrode)** is coupled to the **device receiving area 138 (die pad)**. Liu, 8:27-33; Provisional, [00043].



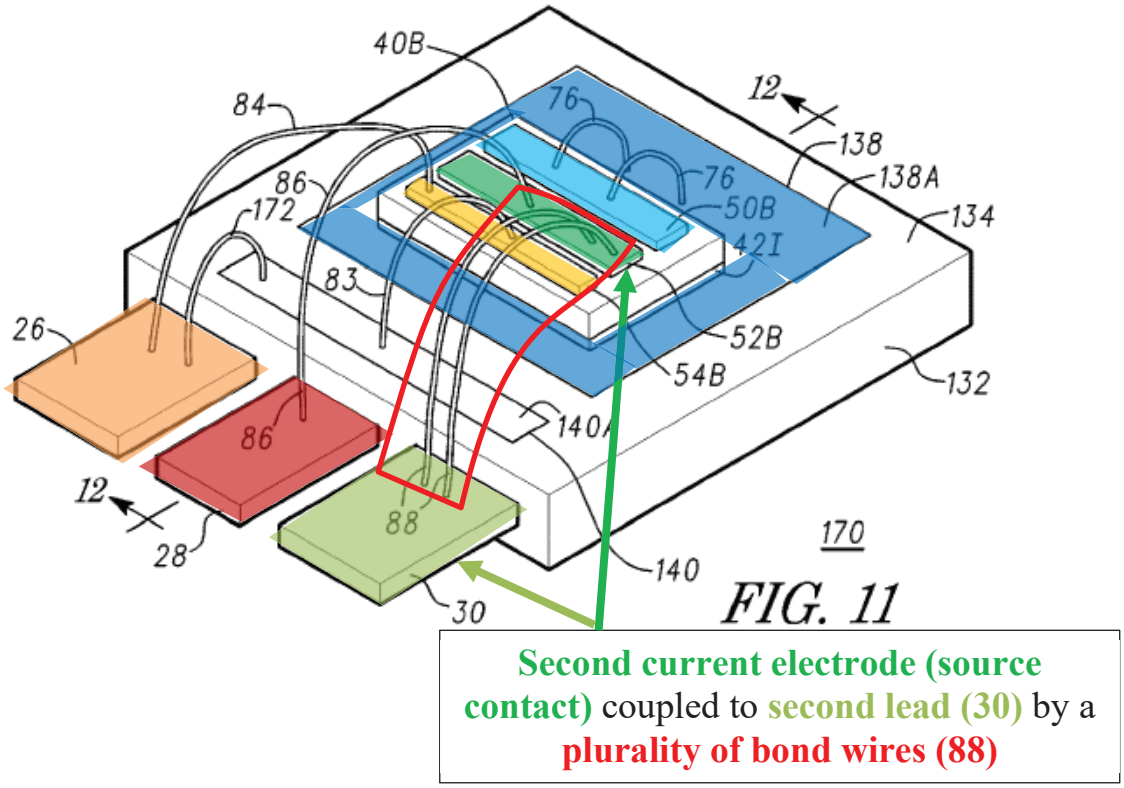
Liu, Fig. 11 (annotated); Provisional, Fig. 11.

5. Claim 6 – The electronic component of claim 1, wherein the second current electrode is coupled to the second lead by a plurality of bond wires or a contact clip.

[0255] Liu discloses claim 6 because Liu's source contact 52B (second current electrode) is coupled to the leadframe lead 30 (second lead) by bond wires 88. Liu, 8:27-33; Provisional, [00043].

[0256] As explained for [1e], Liu's Fig. 11 shows "**source contact 52B** of semiconductor device 40B is electrically connected to leadframe lead 28

through a bond wire 86 and to **leadframe lead 30** through **bond wires 88**." Liu, 8:27-33; Provisional, [00043].



Liu, Fig. 11 (annotated); Provisional, Fig. 11.

[0257] Liu also discloses its source (second current electrode) is coupled to the second lead by a contact clip. Liu discloses that bond wires 88 are "replaced by an electrically conductive clip 106" (contact clip). Liu, 4:62-67; Provisional, [00027].

[0258] A POSITA would have been motivated and found it obvious to use Liu's conductive clip 106 to couple Liu's source contact 52B to leadframe lead 30, in place of bond wires 88, for the reasons explained for Ground 1, claim 7. As I

explained above, the same benefits of a contact clip would be realized in Liu, and at very least a contact clip was a suitable option expressly suggested by Liu.

D. Ground 2B: Liu in View of Roberts Renders Obvious Claims 3 and 17

1. Claim 3 - The electronic component of claim 1, wherein the compound semiconductor transistor device has a blocking voltage capability of at least 400 V and a switching frequency capability of at least 100 kHz.

[0259] Liu in view of Roberts renders claim 3 as obvious. As explained for Ground 1A, claim 3 requires the device to have a blocking voltage capacity of at least 400V and a switching frequency capability of at least 100 kHz. A POSITA would have understood that Liu's compound semiconductor device would have achieved these characteristics, which were common for compound semiconductor power conversion transistors designed for high voltage applications, as explained expressly by Roberts.

[0260] Roberts includes a "Background Art" section that notes that high voltage (e.g., high blocking voltage capability) transistors were common in the art. Roberts explains that transistor devices intended for high voltage applications, "e.g., 600/650V" in "normally-on (depletion mode) transistors" were well known at the time. Roberts, [0006], [0012].

[0261] Although Liu does not expressly disclose its device's switching frequency capability, switching frequency capabilities of at least 100kHz were

common in the art, particularly for compound semiconductor devices (like Liu), as Roberts discloses. Roberts, in its "Background Art" section, explains that GaN transistors "provide <20ns switching time and more than 30A current switching capability." Roberts, [0008]. From a switching time in nanoseconds, the corresponding switching frequency is determined by the following formula: Hz = 1/(ns/(1*10^9). Applying this routine formula, a switching time of 20ns corresponds to 50MHz—much greater than 100kHz.

[0262] A POSITA would have understood that a blocking voltage capability of at least 400 V and a switching frequency capability of at least 100 kHz were standard, routine, and readily-achievable characteristics for compound semiconductor transistors designed for high voltage applications (like Liu) at the time of the '481 patent. Indeed, higher blocking voltage capability and faster switching frequencies were some of the very benefits boasted by compound semiconductor devices generally, as opposed to traditional Si-based devices. Ex. 1022, at 20. Because Liu expressly discloses compound semiconductor transistor devices, but is silent on the corresponding switching time or frequency, a POSITA would have been motivated to look to references that disclose expected switching time or frequencies for other compound semiconductor devices, including high voltage application GaN transistor devices like in Roberts. A POSITA would have looked to references like Roberts "to better understand or interpret" the achievable

characteristics of Liu's compound semiconductor transistor device, including the switching time and frequency. As noted by Huang, "[t]he switching speed of GaN devices is much faster than comparable Si MOSFET which makes the packaging even more critical to achieve lower loss and less ringing during switching transition." Ex-1024, 2. Further, "DFN packages are typically used for high voltage e-mode GaN devices[,]" such as the device disclosed in Liu. Ex-1024, 2. And, because these characteristics were common, well-known, and readily achievable in compound semiconductor transistor devices at the time, a POSITA would have had a reasonable expectation of success in operating Liu's compound semiconductor transistor device with a blocking voltage capability of at least 400 V and a switching frequency capability of at least 100 kHz.

2. Claim 17

a. [17p] An electronic component, comprising:

[0263] [17p] is identical to [1p]. Liu discloses [17p] for the reasons explained for [1p].

b. [17a] a Group III nitride-based transistor device having a blocking voltage capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead

is coupled to the Group III nitride-based transistor device and provides a source sensing functionality,

[0264] Liu in view of Roberts and Roberts renders obvious [17a].

[0265] As explained for [1a] and claim 2, Liu discloses a Group III nitride-based transistor device.

[0266] As explained for claim 3, Liu-Roberts teaches a blocking voltage capability of at least 100 kHz,.

[0267] As explained for [1a], Liu discloses a first current electrode, a second current electrode and a control electrode.

[0268] As explained for [1e], Liu teaches the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead is coupled to the transistor device and provides a source sensing functionality.

c. [17b] a housing,

[0269] Claim 4, like [17b], requires a housing. Liu discloses a housing for the reasons explained for claim 4.

d. [17c] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

[0270] [17c] is identical to [1d]. Liu teaches [17c] for the reasons explained for [1d].

e. [17d] wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are

exposed from the housing and provide substantially planar contact surfaces,

[0271] [17d] is identical to claim 4. Liu teaches [17d] for the reasons explained for claim 4.

f. [17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad,

[0272] [17e] is similar to [1f] except that it requires a Group III nitride-based transistor device rather than a general compound semiconductor device.

[0273] As explained for [17a] and claim 2, Liu discloses a Group III nitride-based transistor device.

[0274] Liu teaches the remainder of [17e] for the reasons explained for [1f].

g. [17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

[0275] [17f] is identical to [1g]. Liu discloses [17f] for the reasons explained for [1g].

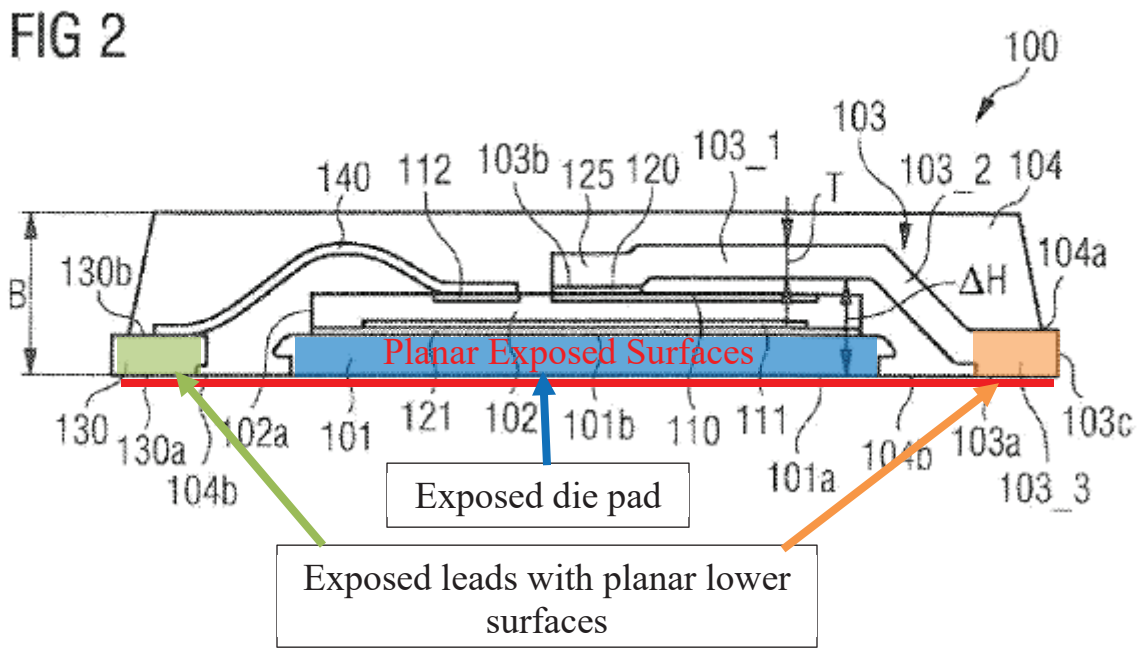
E. Grounds 2C and 2D: Liu in View of Otremba433 (Ground 2C) and Liu in View of Otremba400 (Ground 2D) Render Claims 4 and 9 Obvious

1. Claim 4 - The electronic component of claim 1, further comprising a housing, wherein lower surfaces of the die pad, the first lead, the second lead and the third lead are exposed from the housing and provide substantially planar contact surfaces.

[0276] To the extent claim 4 is interpreted as requiring a leadless package— a package that has the lower surfaces of leads and die pads exposed in a coplanar configuration along the bottom of the housing—Otremba433 (Ground 2C) and Otremba400 (Ground 2D) disclose it.

[0277] **For Ground 2C,** Otremba433 discloses a "leadless package" with contacts and a die pad exposed on the bottom of the devices, Otremba433, [0037]. Otremba433 explains that "semiconductor device 100 may be a package comprising a carrier 101, a semiconductor chip 102, a contact clip 103 and an encapsulation body 104." Otremba433, [0027]. Otremba433's contacts 130 and 103 (leads) have "external contact area[s]" 103a and 130a that are "coplanar with a reference plane defined by a bottom surface 101a of the carrier 101" (die pad) that is "exposed at the bottom of the package." Otremba433, [0037] (discussing lead 103/103a and carrier 101/101a), [0039] (discussing lead 130/130a); *see also* Otremba280, 4:17-29 ("The lower surface 33 of the device carrier portion 19 and

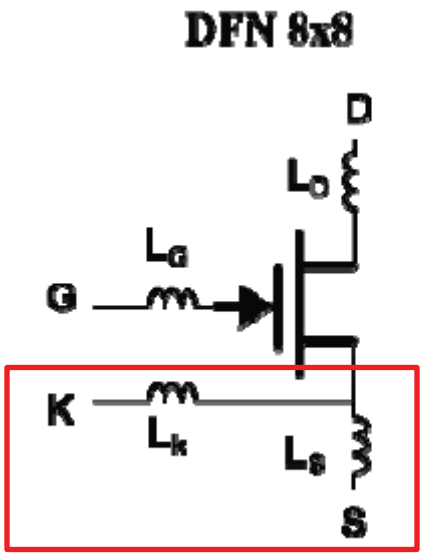
the lower surface 33 of the leads 20 may be generally coplanar with one another so as to provide a surface mountable or leadless type electronic component.”).



Otremba433, Fig. 2 (annotated).

[0278] In my opinion, a POSITA would have understood that Liu’s device would be readily implemented in the leadless package of Otremba433 because package designs were easily modifiable to meet the needs of a particular use. Liu recognizes that it implements a package with leadframe leads as an exemplary package design. It is my opinion that a POSITA would have realized the known benefits of leadless package designs. For example, leadless package designs saved space on the printed circuit board and showed faster performance and switching speeds than through-hole and other conventional packages, thus

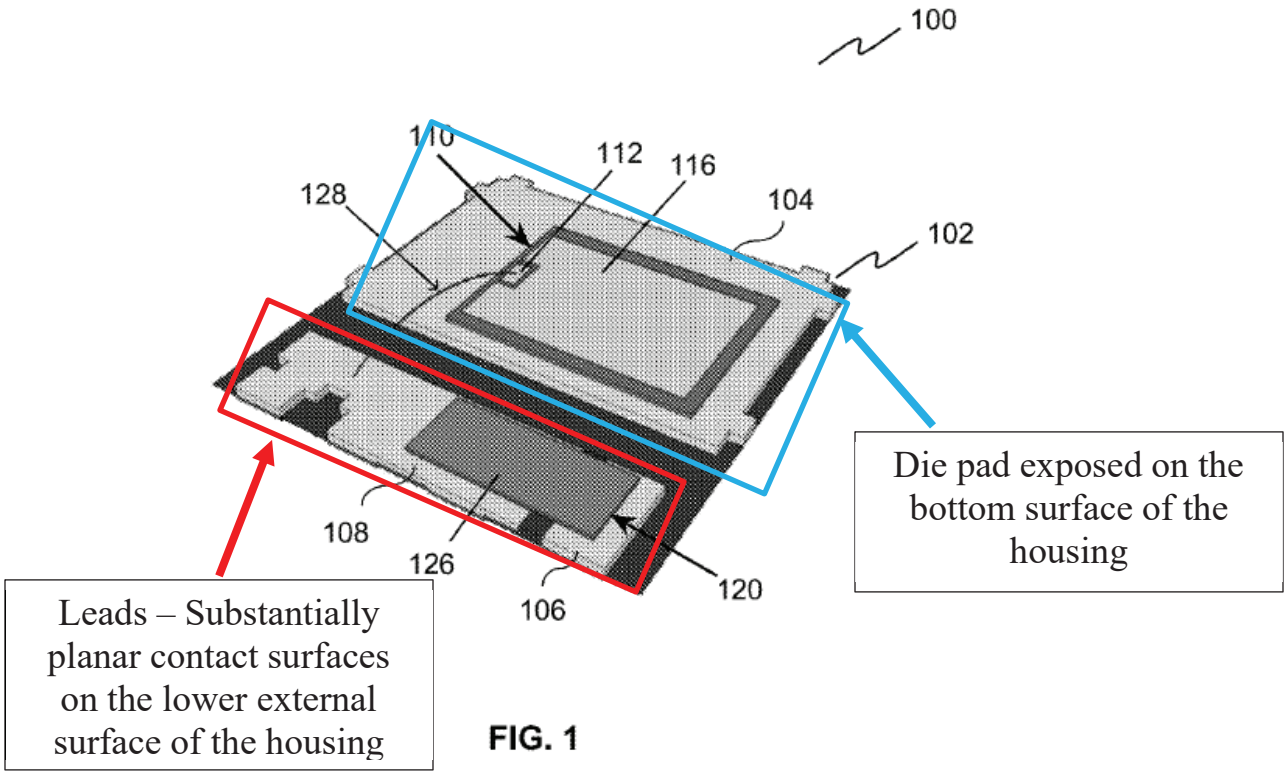
enabling improved performance, switching behavior, ease of use, EMI, reliability, and higher power density. Liu recognizes that it implements a leaded package as an exemplary package design, and would have realized the known benefits a leadless package offered as improvements to a device ready for such improvement. And leadless packaging types were known, including those with source sensing leads, like a DFN8x8 package. Ex-1024, 2, Fig. 2. Further, DFN packages were "typically used for high voltage e-mode GaN devices. Ex-1024, 2.



Ex-1024, Fig. 2 (annotated).

[0279] Thus, packaging Liu as a leadless package, disclosed by Otremba433, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results.

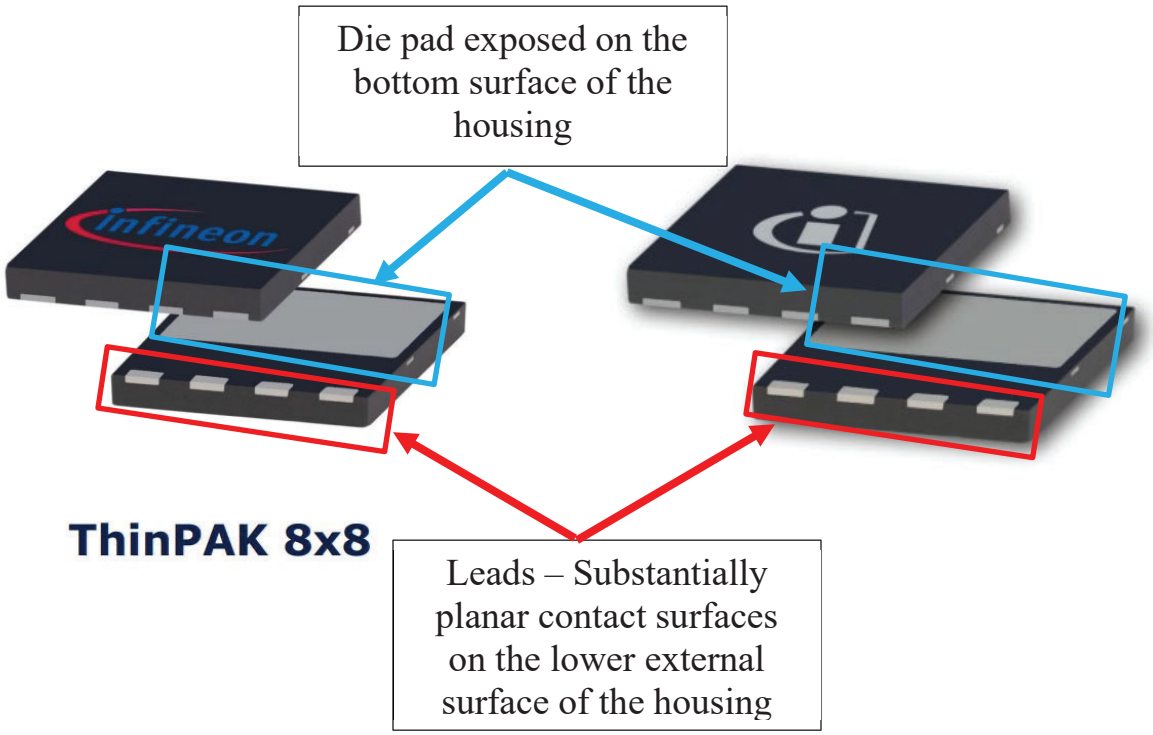
[0280] **For Ground 2D**, Otremba124 discloses a power transistor including a GaN HEMT "packaged in a[n] 8x8 ThinPAK." Otremba124, [0041]. Figure 1 shows the ThinPAK8x8 package outline with flat source leads 108 and 106 on the bottom of the package.



Otremba124, Fig. 1 (annotated).

[0281] ThinPAK8x8 was a well-known leadless package design at the time, as evidenced by ThinPAK8x8 Brochure and ThinPAK Recommendations, which confirms that ThinPAK8x8 packaging included leads and die pad exposed on the lower surface and forming planar contacts (a leadless design). Ex-1016, 1, 5,

6; Ex-1017, 1, 4 ("Visible are the 4 small Source/Gate-Pads … and the big exposed drain pad ….").



Ex-1016, 1, 31; Ex-1017, 1 (annotated).

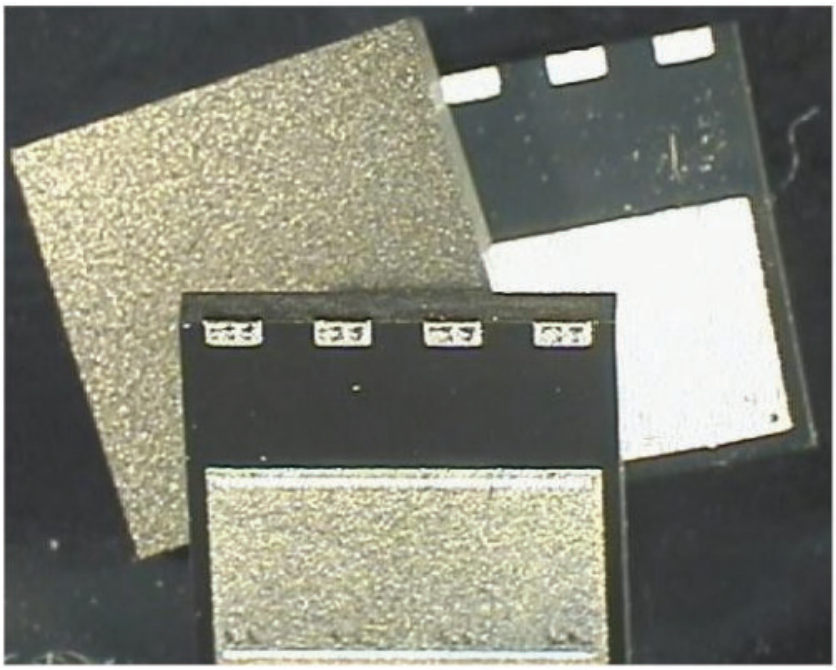


Figure 1: Top and bottom view of VDSON-4 (ThinPAK 8x8)

Ex-1017, 4 (Fig. 1) (annotated).

[0282] In my opinion, a POSITA would have been motivated to package Liu's semiconductor device in the ThinPAK8x8 package design of Otremba124 with an exposed die pad and planar lead contacts on the lower surface. ThinPAK8x8 was boasted as an improvement on other leaded packaging designs, saving space on the printed circuit board (PCB) with a footprint of 64mm^2 (as opposed to 150mm^2 for competitive devices at the time). Ex-1016, 3. Likewise, because ThinPAK8x8 was leadless, it showed faster performance and switching speeds than through-hole and other conventional packages (like the TO220), thus enabling improved performance, switching behavior, ease of use, EMI, reliability, and higher power density. Ex-1016, 3. Liu recognizes that it implements a leaded

package, as an exemplary package design, and would have realized the known benefits ThinPAK8x8 offered as improvements to a device ready for such improvement. Indeed, Lind shows ThinPAK8x8 with source sensing connections as an alternative to a similar leaded package, TO-247-4P, as would be obvious to a POSITA:

III. Source-Sense concept and A/B simulation

A novel concept has been introduced to fundamentally eliminate the loss mechanism described in II.

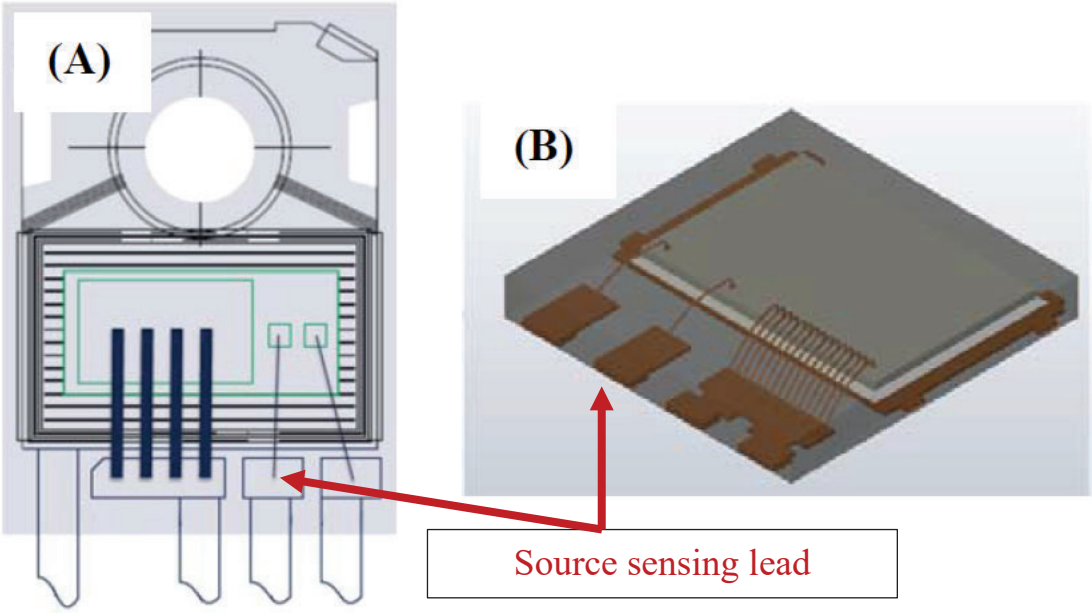


Figure 4 (A): TO-247-4P and (B) ThinPAK8x8 with Source-sense connections

Ex-1013, 3 (Fig. 4) (annotated).

[0283] Thus, packaging Liu as a ThinPAK8x8, disclosed by Otremba124, would have been no more than combining prior art elements using known techniques to a device ready for improvement to yield predictable results.

[0284] Additional package formats, including leadless, exposed-die packages were also known and in use at the time, as taught by Otremba433 and Otremba400, and would have been at least considered suitable options for packaging Liu's compound semiconductor component 170. In fact, Otremba433 recognizes that leaded and leadless packages were both possible for packaging semiconductor devices. Otremba433, [0025]. And leadless packaging types including those with source sensing leads, like a DFN8x8 package, were known. Ex-1024, 2, Fig. 2. Further, DFN packages were "typically used for high voltage e-mode GaN devices. Ex-1024, 2.

2. Claim 9 - The electronic component of claim 1, wherein the electronic component conforms to a TO leadless package outline or a ThinPAK8x8 package outline.

[0285] Claim 9 is of similar scope to claim 4, except claiming the ThinPAK8x8 leadless ***outline*** expressly.

[0286] **For Ground 2C**, Liu in view of Otremba433, which expressly discloses a leadless package outline, such as the ThinPAK8x8 package outline (Otremba433, [0025], [0037]), renders claim 9 obvious for the same reasons explained for claim 4.

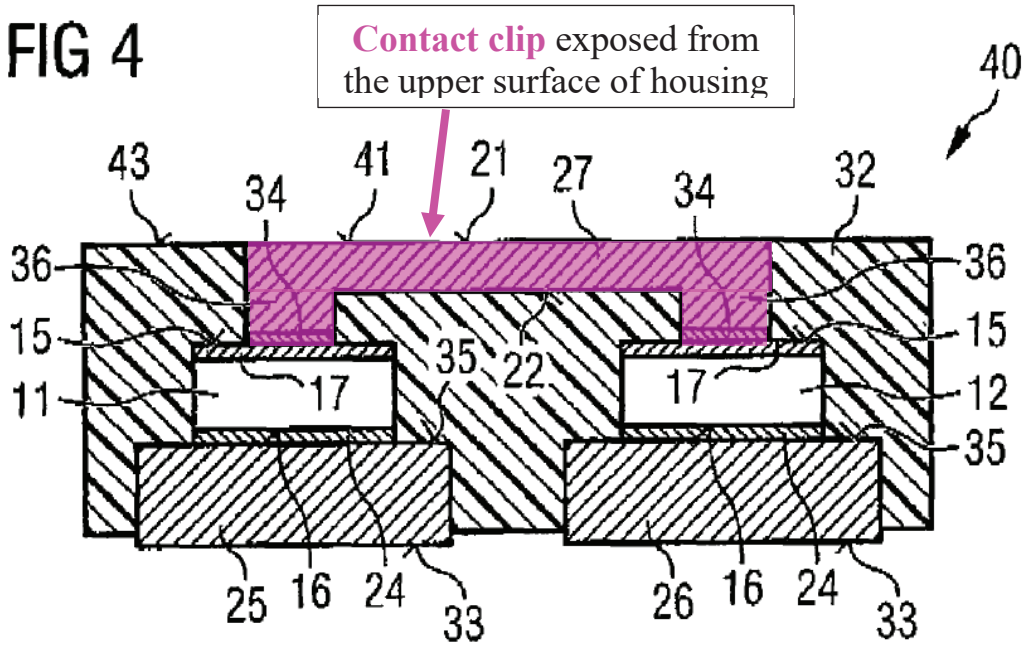
[0287] **For Ground 2D**, Liu in view of Otremba124, which expressly discloses ThinPAK8x8 packaging (Otremba124, [0041]) renders claim 9 obvious for the reasons explained for claim 4.

F. Ground 2E: Liu in View of Otremba433 and Otremba280 Renders Obvious Claims 7 and 8

1. Claim 7 – The electronic component of claim 4, wherein the first current electrode is coupled to the die pad by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

[0288] Liu in view of Otremba433 renders claim 4 obvious.

[0289] As explained for claim 6, Liu discloses replacing bond wires with a contact clip, but Liu does not expressly disclose that the contact clip is exposed from the housing. Otremba280 discloses using exposed contact clips to couple components within a device. Otremba280 states that its electronic component includes a "contact clip 14 [that] is exposed from the plastic encapsulation compound 32 [(housing)]." Otremba280, 8:33-41, Fig. 4.



Otremba280, Fig. 4 (annotated).

[0290] Otremba280 expressly teaches, suggests, and motivates exposing the contact clip from the housing because the "exposed area 41 of the contact clip 14 provides a shorter path of thermal resistance" with "the environment around the electronic component 40." Otremba280, 8:45-48. By exposing the clip, the "thermal performance of the electronic component 40 may be increased due to an improvement in the efficiency of thermal dissipation from the electronic component 40." Otremba280, 8:48-51. To realize the thermal benefits, a POSITA would have been motivated to implement Otremba280's exposed contact clip to couple Liu's drain electrode (first current electrode) and device receiving area (die pad), as I explain for Ground 1C and 1D, claim 7 to (1)

improve current carrying capability; (2) allow for better current spreading to avoid hot spots; (3) reducing on resistance; (4) reducing parasitic induction; and (5) ; and (5) simplifying assembly and manufacturing.

[0291] **First,** contact clips have better current carrying capability than bond wires because of their larger surface area connections, thicker metal, stronger construction, and higher integrity for assembly and manufacturing as opposed to narrow gauge bond wires which can be considered fragile.

[0292] **Second,** contact clips provide better current spreading across the clip as opposed to narrow gauge bond wires that can cause hotspots from current crowding. The thicker metal helps the current to become more uniform within the clip. Current hot spots are caused by current crowding which is when current is forced to go into a narrow area. Current crowding is a well-known reliability and lifetime issue for narrow gauge bond wires.

[0293] **Third,** contact clips reduce device on-resistance (RDS(on)) because the contribution of Rpkg is lower than bond wire resistance, which usually must be accounted for in the overall figure, especially when aiming for a total device RDS(on) ≤ 25 mΩ. RDS(on) is lower as the metal contact clips are thicker and are capable to carry more current, as well as having the physical dimensions through larger area and thickness to mitigate current hot spots and current crowding.

[0294] **Fourth**, contact clips reduce parasitic inductance because bond wires behave as parasitic inductors that can negatively impact device switching. Contact clips inherently have lower parasitic inductance, enabling higher device switching. Otremba880, from the same time period, explains that "[a]n electronic device comprising a semiconductor chip may exhibit a parasitic source- or emitter-inductance and a parasitic drain- or collector-inductance," and "[r]educing a parasitic inductance may improve an efficiency of the electronic device." Otremba880, 1:11-18. To resolve the issue of parasitic impendence, a POSITA would have understood using contact clips to connect components of the device—not bond wires that can incur parasitic inductance.

[0295] **Fifth,** contact clips are simple to handle in assembly and packaging for back-end manufacturing. Contract clips can be easily loaded into automatic tools for high yielding, high volume assembly, which keeps costs under control.

[0296] At the very least, bond wires and contact clips were known alternatives for coupling components of a compound semiconductor transistor device. Otremba441 discloses that commonly-known coupling structures within transistor devices include any of "a clip, a ribbon, a wire, a plate, or a conductor track," so long as the resistance is below a certain threshold. Otremba441, 2:59-65, 6:34-43; *see also* Otremba124, 3:48-60, 7:49-55. A POSITA would have

understood that bond wires and contact clips were ubiquitous coupling means, each suited to different design preferences and needs, and at least both constituting suitable options.

2. Claim 8 - The electronic component of claim 4, wherein the second current electrode is coupled to the second lead by a contact clip and a portion of the contact clip is exposed from the upper surface of the housing.

[0297] As explained for claim 7, implementing an exposed contact clip to couple components in Liu would have been obvious. Coupling Liu's second current electrode to the second lead with Otremba280's exposed contact clip would have been obvious for the same reason coupling Liu's first current electrode to the die pad would have been obvious, as explained for claim 7.

G. Ground 2F: Liu in View of Roberts and Otremba433 Renders Obvious Clam 17

1. Claim 17

a. [17p] An electronic component, comprising:

[0298] [17p] is identical to [1p]. Liu discloses [17p] for the reasons explained for [1p].

b. [17a] a Group III nitride-based transistor device having a blocking voltage capability of at least 400V and a switching frequency capability of at least 100 kHz, a first current electrode, a second current electrode and a control electrode, wherein the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead and a third lead

is coupled to the Group III nitride-based transistor device and provides a source sensing functionality; and

[0299] Liu in view of Roberts renders obvious [17a].

[0300] As explained for [1a] and claim 2, Liu discloses a Group III nitride-based transistor device.

[0301] As explained for claim 3, Liu-Roberts teaches a blocking voltage capability of at least 100 kHz.

[0302] As explained for [1a], Liu discloses a first current electrode, a second current electrode, and a control electrode.

[0303] As explained for [1e], Liu teaches the control electrode is coupled to a first lead, the first current electrode is coupled to a die pad, the second current electrode is coupled to a second lead, and a third lead is coupled to the transistor device and provides a source sensing functionality.

c. [17b] a housing,

[0304] [17b], like claim 4, requires a housing. Liu discloses a housing for the reasons explained for claim 4.

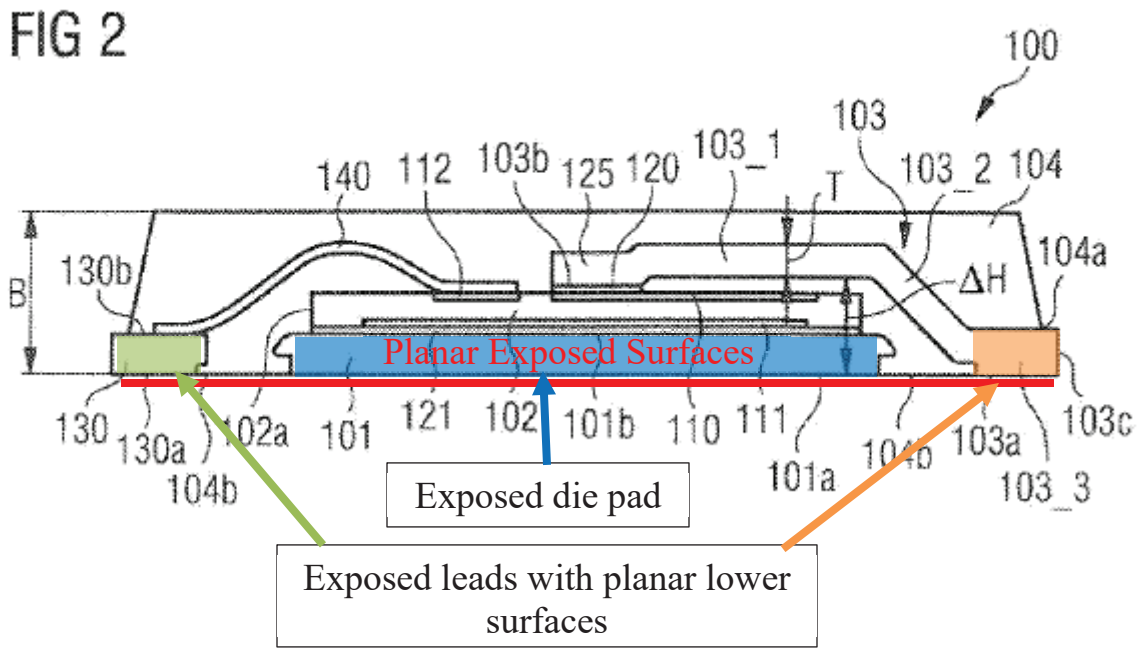
d. [17c] wherein the first lead, the second lead and the third lead are spaced at a distance from the die pad,

[0305] [17c] is identical to [1d]. Liu teaches [17c] for the reasons explained for [1d].

e. [17d] wherein lower surfaces of the die pad, of the first lead, of the second lead and of the third lead are exposed from the housing and provide substantially planar contact surfaces,

[0306] [17d] is identical to claim 4. Liu teaches [17d] for the reasons explained for claim 4.

[0307] Additionally, as explained for Ground 2C, Otremba433 discloses a "leadless package" with contacts and die pad exposed on the bottom of the devices. Otremba433, [0037]. Otremba433's contacts 130 and 103 (leads) have "external contact area[s]" 103a and 130a that are "coplanar with a reference plane defined by a bottom surface 101a of the carrier 101" (die pad) that is "exposed at the bottom of the package." Otremba433, [0037] (discussing lead 103/103a and carrier 101/101a), [0039] (discussing lead 130/130a).



Otremba433, Fig. 2 (annotated).

[0308] It is my opinion that a POSITA would have understood that Liu's device would be readily implemented in the leadless package of Otremba433 and would have been motivated to do so for the reasons explained for Ground 2C, claim 4.

f. [17e] wherein the Group III nitride-based transistor device is a lateral transistor device and a drain or a source of the Group III nitride-based transistor device is coupled to the die pad,

[0309] [17e] is similar to [1f] except that it requires a Group III nitride-based transistor device rather than a general compound semiconductor device.

[0310] As explained for [17a] and claim 2, Liu discloses a Group III nitride-based transistor device.

[0311] Liu further teaches the remainder of [17e] for the reasons explained for [1f].

g. [17f] wherein the first current electrode is coupled to the die pad by a plurality of bond wires or a contact clip.

[0312] [17f] is identical to [1g]. Liu discloses [17f] for the reasons explained for [1g].

XIII. CONCLUSION

[0313] For the reasons set forth above, in my opinion, a person of ordinary skill in the art would have found claims 1-17 of the ’481 patent obvious.

[0314] In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: June 13, 2024 By:_____

Michael Lebby, Ph.D.