

A Platform-Based MPEG-4 Advanced Video Coding (AVC) Decoder with Block Level Pipelining

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Abstract

We present a baseline MPEG-4 AVC (Advanced Video Coding) decoder based on an optimized platform-based design methodology. With this methodology, we jointly optimize the software and hardware design of the decoder. Overall decoding throughput is increased by synchronizing the software and the dedicated co-processors. The synchronization is achieved at macroblock-level pipelining. In addition, we optimize the decoder software by enhancing the frame buffer management, boundary padding, and content aware inverse transform. To speed up motion compensation and inverse transform, which are the most computationally intensive modules, two dedicated acceleration modules are realized. For comparison, the proposed prototype decoder and MPEG-4 AVC reference decoder are evaluated on an ARM platform, which is one of most popular portable devices. Our experiments show that the throughput of the MPEG-4 reference decoder can be improved by 6 to 7 times. On an ARM966 board, the optimized software without hardware acceleration can achieve a decoding rate up to 5 frames per second (fps) for QCIF video sequences. With the dedicated accelerators, the overall throughput is increased by about 30% to reach 6.6 fps on the average and is up to 10.3 fps for slow motion video sequences.

1. Introduction

Multimedia services over mobile network are becoming important with the pervasive presence of the Internet and wireless devices. For this kind of application, MPEG-4 Advanced Video Coding [7] provides better image quality due to its significant improvement on the coding efficiency as compared to that of MPEG-4 visual simple profile. Since some of the AVC modules consume considerable power, it is challenging to realize real-time AVC encoder and decoder. Several AVC codec [8][9] are optimized for general purpose processors that have sufficient computation power, large memory, special instruction sets, and wide buses to facilitate the speedup of AVC modules. But the performance of the optimized AVC modules is seriously constrained by the low computation power and small memory for mobile devices to achieve the least service requirement of QCIF 7.5 fps. To address such constraints with limited resource, we adopt platform based design method to increase overall throughput.

The design methodology using existing platforms for a multimedia system on a single chip has been widely adopted as in [2]-[6]. The design in [6] is optimized for TI C62x DSP and the design in [5] is for ARM7 TDMI processor. There are other designs [2-4] that adopt a physical ASIC design methodology with maximum performance but longer design cycle. On the other hand, the former case of using existing platform has more flexibility on implementation and algorithm level verification but lacks high performance and cost effectiveness. Thus, there is a tradeoff between the efficiency and the design cycle. To address the problems of extended design cycle and less performance in the case of general purpose processor, we propose an optimized platform-based architecture with macroblock (MB) level pipelining to implement a baseline MPEG-4 AVC decoder. On this platform, a general-purpose processor controls the decoding processes and dedicated acceleration modules are used to speed up the computationally intensive tasks. The accelerators are realized with programmable logic modules to retain the flexibility. In addition, a specific system bus is used to remove the bottleneck for data communications between modules. Subsequently, the proposed architecture is evaluated on an ARM966 platform. Our results show that the optimized software without hardware acceleration can achieve a decoding rate up to 5 frames per second (fps) for the video sequences in QCIF resolution. With the new dedicated accelerators, the decoding throughput is increased by about 30% to reach 6.6 fps on the average and is up to 10.3 fps for slow motion video sequences.

2. MPEG-4 AVC Decoder

Fig. 1 shows an MPEG-4 AVC decoder architecture where the decoding tasks are partitioned into four main modules as follows.

1. Context-adaptive variable length decoding (CAVLD).
2. Inverse quantization and inverse 4x4 discrete cosine transform (IQ-IDCT).
3. Motion compensation (MC).
4. Reconstruction and loop filtering.

The decoding is performed by first parsing the compressed bit-stream by CAVLD. After the parsing, the quantized prediction residues and MB side information including the MB type (MB_Type), the prediction mode, and the motion vector difference (MVD) are extracted. The extracted MB_type controls the switches S_0 and S_1 in Fig. 1 to determine the prediction type. The intra prediction values are derived based on the neighboring pixels without loop

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Table 2. Key operations for AVC decoding modules.

Modules	MC	IQ-IDCT	CAVLD	Loop Filter
Operation	Mul., Add, Shift, MemA	Add, Shift	Branch, MemA	Add, MemA

Mul.: multiplication; MemA: memory access

memory access. The firmware of the accelerators and the software for the decoding modules are stored in the embedded SRAM. In addition to the embedded memory, our decoder also requires external memory for frame buffering. The external memory is accessed via an external memory interface.

4. Design Methodology

4.1 Software and Hardware Partition

In the ARM platform based design, a task can be done with either the software executing on CPU or the dedicated hardware running in parallel with CPU. Thus, to optimize the overall performance through parallel processing, it's challenging to partition the tasks to separately match CPU capability and the dedicated accelerators.

Computational characteristic is a good criterion for task partition [2]-[4]. The modules with regular and computational intensive tasks are perfect for hardware implementation and the modules with lots of branches are more suitable for software realization. Table 2 illustrates the kernel operations of each AVC decoding module. Most modules except the IQ-IDCT require a great amount of memory access (MemA). In addition, the MC and loop filter require intensive arithmetic operations for interpolation and filtering, respectively. The CAVLD uses lots of branching instructions for context-adaptive table switching. Thus, to optimize the performance, the MC, loop filter, and IQ-IDCT are implemented in hardware and the CAVLD is realized in software.

Fig. 3 shows the decoding profiling in relative execution time for different modules. From the Amdahl's law and the observations of Fig. 3, we reduce the computational loads by adding two dedicated accelerators for the MC and IQ-IDCT, respectively. The remaining coding modules are implemented and optimized in software.

4.2 Software and Hardware Synchronization

To save the buffers for intermediate data and maximize the throughput, module synchronization is required. In Fig. 4, we design a scheduling approach for MB-level pipelining based on data dependency and working load distribution. The subscript n denotes the MB index. Basically, a MB is decoded through the three stages including (1) CAVLD; (2) IQ-IDCT and MC; (3) reconstruction and loop filtering. Without a dedicated accelerator for the loop filtering, an ideal pipelining schedule in Fig.4 is changed into that in Fig. 5, where the CAVLD, reconstruction, and loop filtering share one CPU.

In Fig.5, the data dependency at the same stage may decrease the overall throughput. To address this problem,

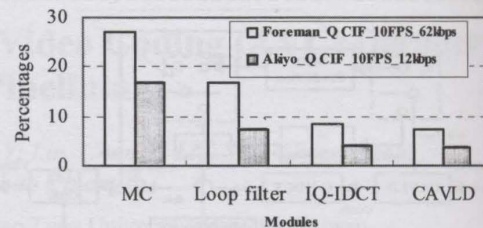


Fig. 3. Decoding profiling for AVC on ARM 966 CPU.

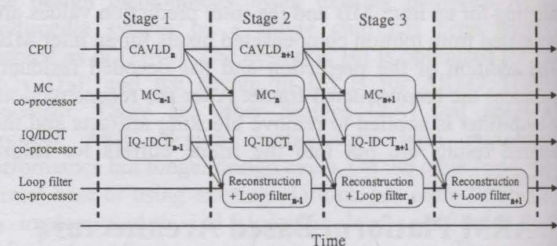


Fig. 4. Illustration of ideal MB level pipeline.

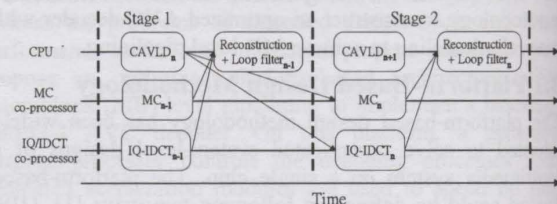


Fig. 5. Modified MB level pipeline.

we maximize the CPU cache performance to have the throughput close to that of the ideal scheduling in Fig.4. Thus, the modified pipeline schedule performs the reconstruction and loop filtering of a MB once CPU has received the results of IQ-IDCT and MC from the dedicated accelerators.

Fig. 6 shows the flow chart to synchronize CPU with the two accelerators at MB-level. At the beginning of each stage,

1. Send the data to the MC accelerators for motion compensation of the n -th MB.
2. Send the data to the IQ-IDCT accelerators for IQ-IDCT of the n -th MB.
3. Proceed to decode the $(n+1)$ -th MB header on the CPU.
4. Check the ready signals from the two accelerators.
5. If the data in the two accelerators are both ready, pass the data through the reconstruction and loop filtering to reconstruct the n -th MB. Otherwise, go to Stage 4.

4.3 Software Optimization

To retain the flexibility and portability across different platforms, our software optimization is mainly from algorithm level improvement. Our optimization techniques are as follows.

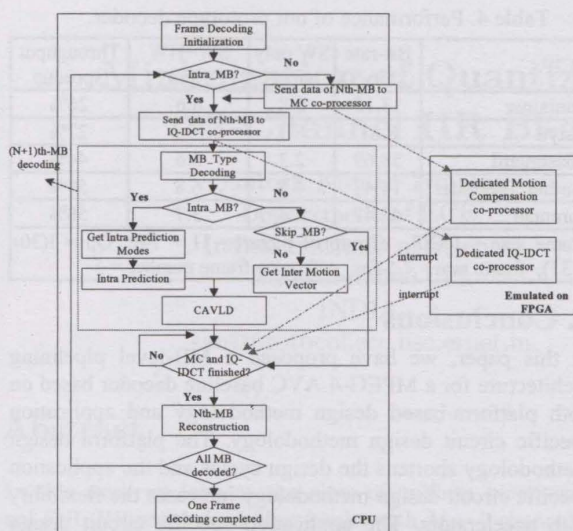


Fig. 6. Flow chart for the MB level pipeline in software.

A. Frame buffer management

We improve the frame buffer management to save execution time for memory copy as follows.

1. The frame copy is done by swapping the pointers of frame buffers.
2. The motion compensated frame or intra prediction pixels are stored directly in the decoded frame buffer to avoid memory copy.
3. The decoded residuals are stored in the frame buffers with 4-byte alignment to match the 32-bit access architecture for ARM.

B. Boundary padding for motion compensation

Costly branching instructions for boundary checking can be saved if we perform padding in advance. Since unconstrained motion vector and the 6-tap filter [1, -5, 20, 20, -5, 1] are used for MC with half-pel interpolation, the locations of the reference pixels could exceed the frame boundaries. To avoid costly branching instructions, the reference frame are padded before MC. The padding length for the left and upper boundaries is (16+2) points while the padding length for the right and bottom boundaries is (16+3) points. In addition to padding, we also speed up the interpolation by replacing the multiplication for fixed filter tap weight with a table look-up.

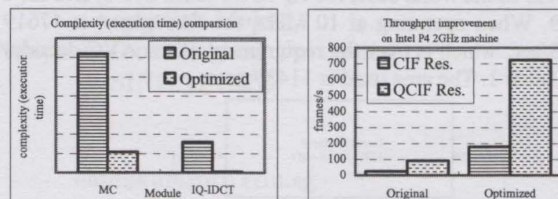
C. Content aware IQ-IDCT

Due to correlation removal from inter frame prediction; most DCT coefficients after quantization are zero. Table 3 shows the percentage of all zero blocks in fast motion and slow motion sequences. For fast motion sequences, about 25% of DCT blocks are classified as the all zero case. For slow motion sequences, the percentage is increased to 47%. Besides, we also find that a large percentage of DCT blocks only have one DC coefficient. Thus, we can classify DCT blocks into three cases and conduct IQ-IDCT differently as follows:

1. For the blocks with nonzero AC coefficients, perform the normal IQ-IDCT.

Table 3. Percentage of all zero blocks at 64 kbits/sec.

Sequence(QCIF)	Fast motion	Slow motion
	Foreman	Mother-Daughter
All zero blocks	24.8%	47.0%



(a) Complexity

(b) Decoding frame rate

Fig. 7. Comparison of MPEG-4 AVC decoders with and without optimization

2. For the blocks with only nonzero DC coefficient, perform only the inverse DC transform.

3. For the blocks with all zeros, skip the transform.

With our optimization, the entire code size is reduced to 80 kilo-bytes and the complexity for the MC, loop filter and IQ-IDCT are greatly reduced. Fig. 7 (a) shows the complexity comparison in execution time with and without our optimization. Further, Fig. 7 (b) shows the decoding throughput improvement (on an Intel P4 2GHz PC). With our optimization, the overall throughput is improved by 6 to 7 times on the average.

4.4 Dedicated Accelerator Design

By allocating dedicated co-processors with only regular and computation intensive tasks, we design the co-processors as simple as possible. With the MB level scheduling, each co-processor operates at the granularity of one MB.

A. MB-based MC

To speed up interpolation, we design a dedicated co-processor in Fig. 8. For a MB interpolation, the co-processor uses a local memory to store 1500 integer pixels and two interpolation engines for parallel processing of the luminance and chrominance components. Each engine consists of multiple multipliers and accumulators. Particularly, the multiplier is implemented in a hardwired manner to maximize performance. To get one interpolated MB, the intermediate results (output) of row and column filtering in each engine may be fed back to conduct the filtering of another columns and rows.

The AVC specification uses variable block size motion compensation. The minimum granularity for motion compensation is a 4x4 block. Therefore, our interpolation engine is designed for a 4x4 block. The interpolation of each MB takes 16 iterations. In the worst case, our design takes 1280 cycles to interpolate one MB. As operating at 10 MHz, the throughput for each MB is 7812 MB/sec, which is over the requirements in Table 1. The area used is 11172 gates.

B. MB based IQ-IDCT

The IQ-IDCT involves two main steps. The first step is to store the input data of a MB in local memory with the size 3 kbits. The second step is to perform the 4x4 integer IDCT,

which consists of two multiplication-free transforms and one transpose operation. In addition, the IQ task is done by a hardwired multiplier. In our implementation, we integrate three different types of inverse transform for luminance 4x4 DC block, chrominance 2x2 DC block, and luminance 4x4 block. In the worst case, the IQ-IDCT takes 210 cycles for a MB. When operating at 10 MHz, the throughput is 47619 MB/sec, which is over the requirement of the AVC decoder in Table 1. The area used is 11489 gates.

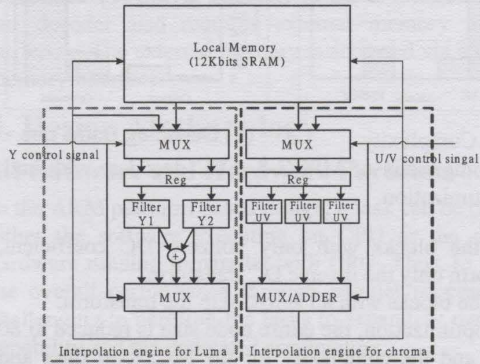


Fig. 8. Interpolation architecture for quarter-pel motion compensation

5. Experiment Results and Analysis

A. Decoding Throughput

Our decoding system is emulated with the configuration in Fig. 3. The ARM966 CPU (system clock running at 130MHz), embedded SRAM (1 Mbytes), and external memory interface are replaced with a dedicated hard core while the other parts including the dedicated accelerators are implemented on a FPGA module (running at 10MHz). In addition, the AHB bus is running at 33MHz.

Table 4 lists the decoding throughput in frames per second (fps) on ARM966 CPU. With our software only optimization, the decoding speed is about 2.3 to 8.1 fps. With hardware acceleration, the throughput is increased by 30%~60%. The overall throughput ranges from 3.3 to 10.3 fps. As shown in Table 4, the decoding throughput is sequence dependent. Our decoder performs better for slow motion sequences, which have more zero DCT blocks and high probability of using integer pixel resolution MC. The decoding rate is increased due to less computation for the MC and IDCT-IQ modules with slow motion sequences. The improvement ratio using accelerators for decoding slow motion sequences is smaller, which is consistent of the observations of Amdahl's law and the results in Table 4.

To analyze the performance of the proposed method, the ideal upper bound is reached as 7.7 fps¹ following Amdahl's law. (The dedicate hardware occupies almost 35% for Foreman sequence according to Fig. 3) The performance gap can be explained with the overhead for synchronization and bus communication. Due to the sub-optimal synchronization scheme, it causes some overhead and makes the decoding rate slower than the ideal 7.7 fps.

¹
$$fps_{ideal} = fps_{SW} \times \frac{100\%}{100\% - P_{MC+IDCT}(\%)} = 7.7(fps)$$

Table 4. Performance of our prototype decoder.

QCIF	Bit-rate (kbits/s)	SW only (fps)	SW+HW (fps)	Throughput Speedup
Container	13.15	6.8	8.6	26%
Akiyo	8.67	8.1	10.3	27%
Coastguard	58.69	2.3	3.6	44%
Mother_Daughter	14.43	4.5	6.8	50%
Foreman	42.47	2.4	3.7	56%

Frame size = QCIF, Group of picture= I1 + 74P, Qp = I(30) P(31), frame rate = 7.5 fps, reference frame number = 5

6. Conclusions

In this paper, we have proposed a MB-level pipelining architecture for a MPEG-4 AVC baseline decoder based on both platform-based design methodology and application specific circuit design methodology. The platform design methodology shortens the design cycles and the application specific circuit design methodology increases the flexibility with accelerators. The application specific circuit design methodology includes the task partitioning and scheduling in the MB-level to enhance the overall decoding throughput. With the task partitioning, the software parts control the branching data flow and the hardware accelerators speed up the regular and computationally intensive modules. In addition, without branching operations, the accelerator design is simplified. With the platform-based design methodology, the software procedures and hardware modules retain a high degree of reusability. The proposed MB-level pipelining achieves significant improvement in speed using both software and hardware co-design.

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Proceedings of the 2003 Joint Conference of the Fourth International Conference on Information, Communications and Signal Processing and Fourth Pacific-Rim Conference on Multimedia (ICICS-PCM 2003)

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IEEE Catalog Number: 03EX758

ISBN: 0-7803-8185-8

Library of Congress: 2003111734

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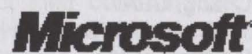
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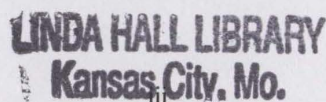


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MESSAGE

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On behalf of the Conference Organising Committee, we would like to welcome you to the 2003 Joint Conference of the Fourth International Conference on Information, Communications & Signal Processing (ICICS 2003) and the Fourth Pacific-Rim Conference on Multimedia (PCM 2003). The Committee has been working very hard during the last 12 months, especially during the SARS period, to ensure the success of this event. The Committee is very pleased to have received over 600 technical papers from 33 countries.

The joint conference promises to be a superb platform for individual engineers, companies and academia to report their recent developments and exchange their research ideas in the exciting areas of information engineering, communications, signal processing and multimedia. The invaluable interaction will allow us to stay on top of current technologies and meet the challenges ahead.

The Committee has invited two renowned keynote speakers, Professor Lawrence RABINER of Rutgers University and UC Santa Barbara, and Professor S Y KUNG of Princeton University. We are certain that you will enjoy their inspiring speeches.

The success of this conference would not have been possible without the support of many individuals and organizations. The joint conference is organized and sponsored by the School of Electrical and Electronic Engineering, Nanyang Technological University. Special thanks go to the Dean of the School, Professor Meng Hwa ER, for his guidance and encouragement throughout the whole event. We wish to thank the technical co-sponsorship of IEEE, especially IEEE Singapore Section, IEEE Singapore Communications Chapter and IEEE Singapore Signal Processing Chapter. The generous financial assistance from Microsoft and Singapore Exhibition & Convention Bureau is greatly appreciated.

It is a pleasure to thank the members of the Conference Organising Committee and the International Program Committee for their contributions. In particular, we are grateful to our Advisors, Professor Soo Ngee KOH and Professor Alex KOT from Nanyang Technological University and Dr. Hong-Jiang ZHANG from Microsoft Research Asia, for sharing their valuable ideas and experience with us. Last but not least, we would like to convey our appreciation to the keynote speakers, special session organizers, session chairs, authors and reviewers of technical papers, tutorial speakers and all the delegates for their contributions.

Singapore is one of Asia's most exciting and dynamic regions, where East blends harmoniously with West, tradition with modernity and sophistication with nature, creating a unique and stimulating urban experience. We trust that you will take back with you happy memories of Singapore and of this joint conference.

Kwok Hung LI

Ping XUE



MESSAGE

PROGRAM CHAIRS – ICICS-PCM 2003



On behalf of the Technical Program Committee, it is our pleasure and privilege to welcome you all to ICICS-PCM 2003. This is the first time that the ICICS and PCM are organised by the School of Electrical and Electronic Engineering, Nanyang Technological University as a Joint Conference. As a result the Technical Program Committee has organized an exciting technical program covering the areas of Communications, Signal Processing and Multimedia.

We have received a total of 623 papers from 33 countries, covering Asia, Australia, Europe and the Americas. Each paper was subjected to a thorough and comprehensive review by at least two independent reviewers. Based on the reviews we have selected 461 high quality papers for oral presentation, of which 46 papers appear in the special sessions. The technical papers have been arranged into 6 parallel sessions, covering the main technical areas of the conference - Multimedia Systems, Computer Systems, Signal Processing, Communications and Networking. The 8 special sessions of the technical program deal with topical and emerging areas of research.

Besides technical sessions, the conference also features 2 keynote speeches and 4 short courses/tutorials. In these, we are fortunate to have 5 well known authorities presenting in depth matter related to communications, signal processing and multi-media. We are extremely delighted to have two distinguished keynote addresses discussing issues on developments and trends in cutting-edge technologies. The first keynote address on Tuesday morning is "Telecom Technology for the 21st Century" by Professor L Rabiner (Rutgers University, U.S.A.), while the other keynote address "Data Mining on DNA Micro-array Data for Gene Selection and Classification" by Professor S Y Kung (Princeton University, U.S.A.), is on Wednesday morning.

Finally, we would like to thank the International Program Committee members as well as all our authors, reviewers, track-chairs, tutorial and special session organizers, for their hard work. Without their efforts this fine technical program would not have been a reality. We would also like to express our deep appreciation to our keynote speakers for giving us their valuable time.

We look forward to your participation in ICICS-PCM 2003 and hope you will enjoy your visit to Singapore and take with you some fond memories and new ideas to pursue.

Saman S ABEYSEKERA

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