PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/614,275, filed on March 22, 2012, which is incorporated herein by reference.

BACKGROUND

Image sensors are typically formed on various forms of semiconductor materials such as, for example, silicon. Imagers can be incorporated into a variety of devices, including digital cameras, camcorders, computers, cell phones, etc. Due to the ever decreasing size (foot print) of these devices, image sensors have correspondingly seen a decrease in size. Backside illuminated (BSI) image sensors have increased in importance due to the small size of these imagers as compared to front side illuminated (FSI) image sensors. However, pixel size reduction can lead to a significant sacrifice in image quality. As pixel sizes continue to decrease, image signal to noise tends to decrease while electrical and optical cross-talk between adjacent sensor pixels tends to increase. Traditional attempts to reduce the impact of these effects have included adding microlenses above each image sensor in front side pixel sensors to focus the light on the active detector regions, thereby increasing efficiency and reducing cross-talk. Backside illuminated pixel sensors can present different design considerations. For example, significant cross-talk can be generated due to reflection off the often planar back surface of the device.

SUMMARY

The present disclosure provides for light trapping pixels, devices incorporating such pixels, photovoltaic solar cells, and other optoelectronic devices, including various associated methods. In one aspect, for example, a light trapping device can include at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also

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include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping material is thus reflected back toward the pixel. In another aspect, the present disclosure additionally provides an array of light trapping pixels.

A variety of light trapping materials can be utilized and are contemplated, and any such material capable of being used to trap light in a pixel is considered to be within the present scope. In one aspect, at least one of the backside light trapping material and the peripheral light trapping material can include a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials. It is contemplated that the two low refractive index materials have a refractive index of less than about 2.1. Non-limiting examples of low refractive index material can include nitrides, oxynitrides, gasses, at least a partial vacuum, and the like, including appropriate combinations thereof. Other non-limiting examples of low refractive index materials can include silicon oxide, silicon nitride, silicon dioxide, and the like. Furthermore, in another aspect a light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined above, but are rather defined by the relative difference in refractive index.

Furthermore, it is contemplated that high refractive index materials have a refractive index of greater than or equal to about 2.1. Non-limiting examples of high refractive index material can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In one aspect, the peripheral sidewall can extend completely around the pixel periphery. In another aspect, the peripheral sidewall can extend from the light incident surface towards the backside surface.

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In some aspects it is also contemplated that the light incident surface can include a frontside light trapping material at least partially covering the surface thereof. In one aspect, the frontside light trapping material can be an antireflective layer coating. In another aspect, the frontside light trapping material can be a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel. In some aspects it can be beneficial to include a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

In another aspect the present disclosure additionally provides a substantially light trapping pixel device including a light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending from the light incident surface to the backside surface and extending around the pixel periphery. The pixel additionally includes a backside light trapping material substantially covering the backside surface, and a peripheral light trapping material substantially covering the peripheral sidewall. Furthermore, an internally reflective frontside light trapping material can cover at least a portion of the light incident surface that is operable to allow entrance of light into the pixel and is operable to reflect light impinging thereupon from inside the pixel back into the pixel, and the light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

In yet another aspect, the present disclosure provides a method of making a light trapping device, including forming at least one pixel by forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include etching a trench circumscribing the pixel device layer and filling the trench with a light trapping material. In some aspects, the trench can be etched to a depth that contacts at least the first low refractive index material. In some aspects, an incident light trapping material can be applied to the pixel device layer. It is also noted that the light trapping material can be located anywhere in

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the backside region of the device, and that the current scope is not limited to the location of materials or the manufacturing method described above.

In another aspect, filling the trench with the light trapping material can further include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space.

In another aspect, the method can include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of techniques for forming the textured region include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, the like, including appropriate combinations thereof. In one specific aspect, forming the textured region includes laser texturing.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of multiple image sensor pixels in accordance with an embodiment of the present disclosure;

FIG. 2 is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of multiple image sensor pixels in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure;

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FIG. 6 is a cross-sectional view of a light trapping pixel in accordance with another embodiment of the present disclosure; and

FIG. 7 is a depiction of a method of making a light trapping pixel in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "light" and "electromagnetic radiation" can be used interchangeably and can refer to electromagnetic radiation in the ultraviolet, visible, near infrared and infrared spectra. The terms can further more broadly include electromagnetic radiation such as radio waves, microwaves, x-rays, and gamma rays. Thus, the term "light" is not limited to electromagnetic radiation in the visible spectrum. Many examples of light described herein refer specifically to electromagnetic radiation in the visible and infrared (and/or near infrared) spectra. For purposes of this disclosure, visible range wavelengths are considered to be from approximately 350 nm to 800 nm and non-visible wavelengths are considered to be longer than about 800 nm or shorter than about 350 nm. Furthermore, the infrared spectrum is considered to include a near infrared portion of the spectrum including wavelengths of approximately 800 to 1100 nm, a short wave infrared portion of the spectrum including wavelengths of approximately

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1100 nm to 3 micrometers, and a mid-to-long wavelength infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

As used herein, "quantum efficiency" (QE) is typically referring to "external quantum efficiency" (EQE) which is defined as the ratio of electrons collected per photons incident on an optoelectronic device. "Internal quantum efficiency" is defined as the ratio of electrons collected per photons absorbed by an optoelectronic device..

As used herein, the terms "3D" and "three dimensional" can be used interchangeably, and refer to obtaining distance information using electromagnetic radiation.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Such a surface topology can be formed by the irradiation of a laser pulse or laser pulses, chemical etching, wet or dry etching including masked or maskless etching, lithographic patterning, interference of multiple simultaneous laser pulses, reactive ion etching, plasma etching or any other technique that can be used to form such a topology. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 1 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm. A variety of criteria can be utilized to measure the size of such structures. For example, for cone-like structures the above ranges are intended to be measured from the peak of a structure to the valley formed between that structure and an adjacent neighboring structure. For structures such as nanopores, the above ranges are intended to be approximate diameters. Additionally, the surface structures can be spaced at various average distances from one another. In one aspect, neighboring structures can be spaced at a distance of from about 50nm to about 50 μm. In another aspect, neighboring structures can be spaced at a distance of from about 50nm to about 2 μm. Such spacing is

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intended to be from a center point of one structure to the center point of a neighboring structure.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term "monolithic" refers to an electronic device in which electronic components are formed on the same substrate. For example, two monolithic pixel elements are pixel elements that are formed on the same semiconductor substrate.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

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As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. More specifically, in one aspect the disclosure relates to image sensor pixels and elements for trapping light within such pixels. In other aspects, various light trapping elements can additionally isolate neighboring pixels in an image sensor. Isolation elements can be configured to optically and/or electrically isolate neighboring

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pixels from one another in addition to trapping light with in the pixel. It is additionally contemplated that the present disclosure is applicable to other optoelectronic devices such as solar cells, and that all such should be included in the present scope.

In various aspects, image sensors can be front side or backside illuminated, 3D sensors, or any other device or system that incorporate a unique isolation element configured to reduce cross-talk between pixel elements. For example, in one aspect an image sensor can be capable of detecting visible and infrared light, whereas an isolation element associated with such an imager can be designed and configured to reduce and in some cases eliminate electrical and/or optical cross-talk between neighboring pixels from straying visible and infrared light. In some cases, isolation elements can be doped with a dopant that enables the repelling of electrical carriers from the isolation elements or in other words from the side walls of the device. In other cases, isolation elements can include light trapping or reflective materials to optically isolate neighboring pixels. It is additionally contemplated that isolation elements can include both a dopant and a light trapping or reflective material to both electrically and optically isolate the pixels. Moreover, isolation elements can also include surface features formed thereon or associated therewith. Additionally, in some cases a pixel can include a textured region to enhance the detection of infrared light among other things.

In one aspect, a variety of optoelectronic devices are provided such as, without limitation, photosensitive diodes, pixels, and imagers capable of detecting visible and infrared light while exhibiting reduced optical and electrical cross-talk between neighboring pixels or diodes. It is also contemplated that the present scope include methods associated with such devices, including methods of making and using. The present devices can additionally exhibit enhanced absorption and quantum efficiencies. Such devices can also include a plurality of photodiodes or pixels. In some cases, the present devices can achieve a quantum efficiency of 10% for wavelengths at 1064nm and having a thickness of less than 10 microns. In another embodiment, the present device can achieve a quantum efficiency of about 20% for wavelengths at 940nm and a thickness of less than 10 microns.

In one aspect, a device can include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side. Either or

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both the first or second sides can include at least one doped region. Furthermore, the image sensor can include at least one isolation element or feature for at least partially separating and isolating neighboring pixels. FIG. 1 illustrates a simplified drawing of an imager having a first pixel 102 and a second pixel 104, that are formed monolithically on a common semiconductor substrate 106 and are isolated from one another by an isolation element 114. Doped regions 108 and 110 can be disposed on either the first side 120 or second side 122 of the semiconductor substrate, or in some cases on opposite sides of the device. In the present figure, the device is configured such that the first side is capable of receiving incident light. A textured region 112 having surface features is shown on the second side 122 of the semiconductor substrate 106. This architecture having the texture region 112 on the back side 122 can enable enhanced detection and absorption of electromagnetic radiation having wavelengths in the range of about 600 nm to about 1200 nm. It should be noted that this architecture can be used in either a FSI or BSI image sensor architecture. Furthermore, the textured region can be located on the first side 120, the second side 122, or both the first and second sides.

In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, scatters off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. BSI imagers, one the other hand, are configured to have the light sensing portion of the device opposite the circuitry. Incident light enters the device via the light sensing portion and is at least partially absorbed by the device prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the devices according to aspects of the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures, as well as other optoelectronic devices.

Regarding isolation elements, also referred to herein as trench isolation features or sidewalls, various processes can be employed to form the isolation elements. It is

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contemplated that the isolation features can extend from either the first surface or the second surface into the semiconductor material and depending on the depth of the trench can be considered either deep trench isolation or shallow trench isolation. The dimensions of the trench can vary, depending on the application. For example, trenches can have parallel walls, or they can have sloping walls, bottle neck architecture, or any other useful configuration. The depth of the trench isolation feature can be in the range of from about 100 nm to about 50 μm depending on the design of the device. The width can be in the range of from about 100 nm to about 10 μm. For simplicity, the figures in this disclosure show deep trench isolation but it should be understood that shallow trench isolation architectures can be utilized, and that deep trench isolation need not completely extend from one side to the other. The processes contemplated for forming trenches or other isolation features can include, reactive ion etch, isotropic plasma etch, wet chemical etch, laser irradiation, or any other known etch technique.

A variety of reflective materials can be utilized in constructing the isolation features in order to provide optical isolation, light trapping, and/or electrical isolation, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one specific aspect, the dielectric layer can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation. In addition, in some aspects trench isolation features can be doped to further affect the properties of the material with respect to electrical isolation.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

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In some cases, materials having disparate properties can be utilized in the trench isolation features in order to derive a useful combined interaction. As is shown in FIG. 2, for example, an imager having at least two pixels or photodiodes (202 and 204) and at least one isolation element 214. The pixels are shown formed monolithically on a common semiconductor substrate 206. Doped regions 208 and 210 can be disposed on either the first side 220 or second side 222 of the semiconductor substrate. A textured region 212 having surface features is created on the second side 222 of the semiconductor substrate 206.

In some aspects, the isolation element 214 can be designed to function as a Bragg reflector. In such cases, the isolation element 214 includes at least two layers 216 comprised of material having a lower refractive index (n) as compared to the material of the third layer 218 disposed or sandwiched therebetween. In other words, the isolation element includes a high refractive index material sandwiched between two low refractive index materials, and such a configuration forms a Bragg reflector. Additionally, in some aspects the low reflective index materials can be chosen to have a lower refractive index as compared to the semiconductor substrate 206.

Furthermore, in another aspect an isolation element or light trapping material can include a higher refractive index material sandwiched between two materials having a refractive index that is at least 0.2 lower as compared to the higher refractive index material. In this case, the materials are not limited by the definition of low vs. high refractive index outlined below, but are rather defined by the relative difference in refractive index. For example, in one aspect a light trapping material can include silicon dioxide/silicon nitride/silicon dioxide, each material of which would be considered to be a low refractive index material. There is, however, a greater than 0.2 difference in the refractive indexes between silicon dioxide and silicon nitride, and thus such an isolation element would be included within the present scope. It is also noted that the light trapping material can have greater than three layers. As one non-limiting example, a material can have silicon dioxide/silicon nitride/polysilicon/silicon nitride/silicon dioxide.

As has been described, in some aspects a Bragg reflector can be utilized as an isolation element to trap electromagnetic radiation within the pixel. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive

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indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, a Bragg reflector can be made as in FIG. 2, whereby a high refractive index material sandwiched between two low refractive index materials. In one specific aspect, for example, the Bragg reflector can be constructed of a layer of polysilicon sandwiched between two layers of silicon dioxide. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

In terms of optical isolation from pixel to pixel, the large index of refraction mismatch can result in total reflection at the trench side walls. To prevent excessive dark current in the pixels, a passivation layer may be disposed on the side walls of the trench to prevent the generation of carriers and leakage current. Silicon nitride deposited over a thin grown oxide layer is also commonly used, in this case the oxide may be a low temperature grown plasma oxide.

It can be shown through calculations that a low recombination velocity of silicon oxide and silicon nitride is the result of moderately high positive oxide charge ($5x10^{11}$ to $1x10^{12}$ cm^{-2}) and relatively low midgap interface state density ($1x10^{10}$ to $4x10^{10}$ cm^{-2} eV^{-1}). The addition of silicon oxide or nitride can reduce surface recombination and surface generation. Reducing the surface recombination can increase quantum efficiency of photon collection and surface generation can cause excessive dark current in the imagers thereby reducing the quality of the image.

Since the positive oxide charge of silicon nitride or silicon oxynitride is relatively low on silicon on insulator imagers a p-type layer can be adjacent the silicon oxide,

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silicon oxynitride and/or silicon nitride layers as an alternative embodiment. In this case the p-type layer will accumulate the surface or the backside of the p-type silicon layer and p-type sidewalls.

Other possible passivation techniques include a hot steam anneal of hydrogenated silicon nitride or the use of amorphous silicon.

Aluminum oxide can also be deposited in the trench to form an isolating barrier. Aluminum oxide can have low stress, a negative fixed charge and higher index of refraction than silicon oxide or low stress silicon oxynitride nitride. Low surface recombination velocities, as low as 10 cm/s can be obtained through various deposition processes of Al_2O_3 layers on the silicon substrate. Low surface recombination can be achieved by field induced surface passivation due to a high density of negative charges stored at the interface. PECVD aluminum oxide is described here for the backside passivation of the backside and backside trenches in backside illuminated image sensors.

The index of refraction of the aluminum oxide can be increased slightly as required by the addition of other metallic elements to make ternary insulators like Aluminum Oxynitride (AlON), Hafnium Aluminum Oxide (HfAlO), Zirconium Aluminum Oxide (ZrAlO), Lanthanum Aluminum Oxide (LaAlO), Titanium Aluminum Oxide (TiAlO) or quaternary dielectrics like Hafnium Aluminum Oxynitride (HfAlON), Tantalum Aluminum Oxynitride (TaAlON), Lanthanum Aluminum Oxynitride (LaAlON).

Low temperature PECVD deposition processes are contemplated for the backside passivation of the backside and backside trenches in backside illuminated image sensors. As previously mentioned the large index of refraction mismatch between silicon and the insulators in the trenches results in reflection of the incident light and provides optical isolation. The trenches also provide electrical isolation. Additionally, it can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.

Returning to FIG. 2, layers the silicon oxide and polysilicon can optically and electrically isolate the adjacent pixels, as well as function to trap light within the pixel. While any thicknesses capable of forming such a reflector are considered to be within the

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present scope, layer 216 can have a thickness in the range of from about 50 nm to about 500 nm. Layer 118 can have a thickness in the range of from about 5 nm to about 100 nm. Thus, the difference in refractive indexes and thickness can determine the intensity of the internal reflection of electromagnetic radiation. Notably, other materials such as metals, as well as other material not listed herein can be used to increase internal reflection of the light.

It is noted that, for the purposes of the present disclosure, in one aspect a low refractive index material can have a refractive index of less than about 2.1. In the case of the sandwiched materials, the two low refractive index materials can be the same or different materials having a refractive index of less than about 2.1. Non-limiting examples of low refractive index materials can include oxides, nitrides, oxynitrides, gasses, at least a partial vacuums, and the like, including appropriate combinations thereof. Non-limiting specific examples of such materials can include silicon oxide, silicon nitride, silicon oxynitride, and the like, including combinations thereof. Additionally, a high K dielectric material can also make a suitable low reflective index material due to their low refractive index properties and good dielectric properties, and as such, are considered to be within the present scope. One example is Hafnium oxide, which has a refractive index of about 1.9. Other examples of high K dielectrics include hafnium silicate, zirconium silicate, zirconium dioxide, and the like.

Additionally, in another aspect a high refractive index material can include a material having a refractive index of greater than or equal to about 2.1. Thus, in the case of the sandwiched materials, the high refractive index material disposed between the low refractive index materials has a refractive index of about 2.1 or greater. Non-limiting examples of high refractive index materials can include polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and the like, including appropriate combinations thereof.

In still another aspect of the present disclosure, a photosensitive imager having at least two pixels (302 and 304) and at least one trench isolation region 314 is shown in FIG. 3. The pixels can include a semiconductor substrate 306, having a first and second surface, 320 and 322 respectively; at least two doped regions 308 and 310, and a textured region 312 formed at least on the opposite side of the light incident surface (i.e. the

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second side 322). The textured region 312 can have surface features configured to reflect and disperse light. Further, the sidewalls can include a texture region 312 to increase the internal reflections of light. Regarding the isolation element 314 in FIG. 3, the isolation element can include several layers of materials that can passivate the sidewalls and each have a different index of refraction, as was described in FIG. 2. Further, a textured region 312 can be formed on the side walls of the isolation element(s) 314.

The present disclosure additionally provides pixels and imager devices, including imager arrays, which trap light therewithin. In one aspect as is shown in FIG. 4, for example, a light trapping pixel device can include a light sensitive pixel or device 402 having a light incident surface 420, a backside surface 422 opposite the light incident surface 420, and a peripheral sidewall 424 disposed into at least a portion of the pixel 402 and extending at least substantially around the pixel periphery. It is noted that the pixel sidewall is also known as a trench. The pixel can also include a backside light trapping material 426 substantially covering, partially covering, or completely covering the backside surface 422. A peripheral light trapping material 428 can be substantially covering, partially covering, or completely covering the peripheral sidewall 424. As such, light contacting the backside light trapping material 426 or the peripheral light trapping material 428 is reflected back toward the pixel 402. Also shown in FIG. 4 are at least two doped regions 408 and 410 and an optional textured region 412. It is noted that, in addition to a single pixel as shown, pixel arrays are also contemplated and are to be included in the present scope.

The light trapping materials of FIG. 4 can be as described above, either single or multiple layer structures. In one aspect, for example, at least one of the backside light trapping material 426 and the peripheral light trapping material 428 includes a high refractive index material sandwiched between two low refractive index materials. In another aspect, the backside light trapping material 426 and the peripheral light trapping material 428 includes a high refractive index material sandwiched between two low refractive index materials. It is noted that these light trapping materials are shown in FIG. 4 as a single layer for clarity, and that multiple layers are contemplated. Furthermore, the peripheral sidewall can extend for a portion, a substantial portion, or completely around the pixel periphery. Additionally, as has been described herein, the

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peripheral sidewall can extend partially into the pixel, substantially through the pixel, or completely through the pixel to the backside surface. Thus, both deep and shallow trenches are contemplated.

In another aspect, as is shown in FIG. 5, a pixel 502 can include a frontside light trapping material 530 that at least partially covers, substantially covers, or completely covers the light incident surface 520. The frontside light trapping material 530 can be multiple layer of materials have a variety of properties and uses, including passivation, antireflection, light trapping, and the like, including combinations thereof. Note that numerical indicators in FIG. 5 from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. 4.

In another aspect, as is shown in FIG. 6, a pixel 602 can include a frontside light trapping material 632 associated with the light incident surface 620 that is an internal reflective layer having an aperture 634 to allow entry of light 690 into the pixel 602. The frontside light trapping material 632 is thus operable to reflect light impinging thereupon from inside the pixel 602 back into the pixel. Additionally, in some aspects a lens 636 can be functionally coupled to the aperture 634 to focus incident light 690 through the aperture 634 and into the pixel 602. The effective surface area of the aperture compared to the frontside surface area of the pixel can vary depending on the design of the device and the presence, absence, or particular properties of a lens. In one aspect, however, the aperture can be large enough to accept and trap incoming light to a degree that increases the efficiency of the pixel. In one specific aspect, the aperture has an effective surface area of less than about 90% of the incident light surface total surface area. It is noted that various elements such as the doped regions and the optional textured layer are not shown in FIG. 6 for clarity. Furthermore, numerical indicators in FIG. 6 from previous figures are intended to reflect the previous descriptions for those elements, and as such, reference is made to FIG. 4.

The frontside light trapping material can be made of a variety of materials including metals as have been described herein with respect to other light trapping materials. As such, any material that can be applied to the light incident surface and that is internally reflective toward the inside of the pixel is considered to be within the present scope. Thus, the aforementioned pixel is reflective on 6 internal sides, and as such, light

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entering the pixel that is not absorbed will interact with and be reflected internally be either the backside, peripheral sidewall, or frontside light trapping materials. Light is thus effectively maintained inside the pixel until it is absorbed.

In another aspect of the present disclosure, a method of making a light trapping pixel device is provided. Such a method can include, as is shown in FIG. 7, 702 forming a pixel by: 704 forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials, and 706 forming a pixel device layer on the semiconductor layer opposite the light trapping material. The method can additionally include 708 etching a trench circumscribing the pixel device layer and 710 filling the trench with a light trapping material. Further details regarding the wafer bonding and wafer-bonded structures described can be found in copending US Application Serial No. 13/069,135, filed on March 22, 2011, which is incorporated herein by reference.

The formation of the backside light trapping material can be accomplished by a variety of techniques, all of which are considered to be within the present scope. In one aspect, for example, depositing a first low refractive index material onto the semiconductor layer, bonding the first low refractive index material to a high refractive index material having a second low refractive index material coupled thereto such that the high refractive index material is sandwiched in between the first and second low refractive index materials. In some cases the second low refractive index material can be coupled to a carrier wafer. In another aspect, the first low refractive index can be deposited onto the semiconductor layer followed by deposition of the high refractive index material and then the second low refractive index material. In another aspect, the layered structure can be formed on a carrier wafer, and the outermost low refractive index material can then be bonded to the semiconductor layer. The carrier wafer can then be optionally removed. In yet another aspect, the first refractive index material can be deposited onto the semiconductor layer, the second refractive index material can be deposited onto a carrier wafer, and the high refractive index material can be deposited onto either the first or second refractive index material, followed by bonding of the structure together.

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As has been described, the trench can be a shallow trench or a deep trench. In one aspect, however, etching the trench circumscribing the pixel device layer can further include etching the trench to a depth that contacts at least the first low refractive index material. Furthermore, the method can also include applying an incident light trapping material to the pixel device layer.

In some aspects the various trenches can be filled with a material, or they can be gas filled or have a partial vacuum applied thereto. For those aspects whereby the trenches will be filled in with a non-gas material, a variety of deposition techniques are contemplated and all are considered to be within the present scope. In one aspect, however, the trench can be filled with a high refractive index material and a low refractive index material in a sandwich structure as has been described. In one exemplary technique, the filling of the trench with such light trapping material can include depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward, ceasing deposition of the low refractive index material to leave an internal space within the trench, and depositing a high refractive index material into the trench to fill the internal space. As such, the sandwiched layer of low-high-low refractive index materials is thus created in the trench.

In another aspect, the method can also include forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the first low refractive index prior to depositing the first low refractive index material onto the semiconductor layer. Non-limiting examples of texture formation techniques can include plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof. In one specific aspect, the textured region includes laser texturing.

A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and

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the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface.

The textured region can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm. In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm. In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm. In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm. In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, micolenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm. As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured film layer. In one aspect, for example, the textured region can include a substantially conformal textured film layer. Such a textured film layer can have an average thickness of from about 1 nm to about 20 μm. In those aspects where the textured region includes surface features, the conformal textured film layer can have a varying thickness relative to the location on the surface features upon which is deposited.

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In the case of cones, for example, the conformal textured film layer can become thinner toward the tips of the cones. Such a conformal film layer can include various materials, including, without limitation, SiO_2, Si_3N_4, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured film layer can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

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One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material. In some aspects, the features or structures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

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A variety of semiconductor materials are contemplated for use with the pixel devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN),

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indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during manufacture and/or use. The semiconductor substrate can be made from various

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materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the

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scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, $POCl_3$, P_2O_5, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

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CLAIMS

What is claimed is:

1. A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall;

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

2. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

3. The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

4. The device of claim 3, wherein the two low refractive index materials have a refractive index of less than about 2.1.

5. The device of claim 4, wherein at least one of the two low refractive index material includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

6. The device of claim 4, wherein the at least one of the two low refractive index materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

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7. The device of claim 3, wherein the high refractive index material includes a material having a refractive index of greater than or equal to about 2.1.

8. The device of claim 7, wherein the high refractive index material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.

9. The device of claim 2, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.

10. The device of claim 9, wherein the dopant is boron or antimony.

11. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.

12. The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.

13. The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

14. The device of claim 1, further comprising a frontside light trapping material at least partially covering the light incident surface.

15. The device of claim 14, wherein the frontside light trapping material is an antireflective layer coating.

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16. The device of claim 14, wherein the frontside light trapping material is a reflective layer having an aperture to allow entry of light into the pixel, wherein the reflective layer is operable to reflect light impinging thereupon from inside the pixel back into the pixel.

17. The device of claim 16, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

18. The device of claim 16, wherein the aperture has an effective surface area of _____ % of the incident light surface total surface area.

19. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.

21. The device of claim 1, further comprising a textured layer positioned to interact with light proximal to the backside surface.

22. The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.

23. An array of light trapping pixel devices of claim 1.

24. A substantially light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall extending from the light incident surface to the backside surface and extending around the pixel periphery;

a backside light trapping material substantially covering the backside surface;

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a peripheral light trapping material substantially covering the peripheral sidewall; and

an internally reflective frontside light trapping material covering at least a portion of the light incident surface operable allow entrance of light into the pixel and operable to reflect light impinging thereupon from inside the pixel back into the pixel, and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

25. The device of claim 24, wherein the internally reflective frontside light trapping material includes an aperture to allow entry of light into the pixel.

26. The device of claim 25, further comprising a lens functionally coupled to the aperture and operable to focus incident light through the aperture and into the pixel.

27. A method of making a light trapping device, comprising:

forming a pixel by:

forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials; and

forming a pixel device layer on the semiconductor layer opposite the light trapping material;

etching a trench circumscribing the pixel device layer; and

filling the trench with a peripheral light trapping material.

28. The method of claim 27, wherein etching the trench circumscribing the pixel device layer can further include etching the trench to a depth that contacts at least the backside light trapping material.

29. The method of claim 27, further comprising applying an incident light trapping material to the pixel device layer.

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30. The method of claim 27, wherein filling the trench with the peripheral light trapping material further includes:

depositing a low refractive index material into the trench to fill a portion of the trench from the trench walls inward;

ceasing deposition of the low refractive index material to leave an internal space within the trench; and

depositing a high refractive index material into the trench to fill the internal space.

31. The method of claim 27, further comprising forming a textured region on at least a portion of the semiconductor layer between the semiconductor layer and the backside light trapping material.

32. The method of claim 31, wherein forming the textured region includes a technique selected from the group consisting of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

33. The method of claim 32, wherein forming the textured region includes laser texturing.

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ABSTRACT OF THE DISCLOSURE

Light trapping pixels, devices incorporating such pixels, and various associated methods are provided. In one aspect, for example, a light trapping pixel device can include a light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. The pixel can also include a backside light trapping material substantially covering the backside surface and a peripheral light trapping material substantially covering the peripheral sidewall. The light contacting the backside light trapping material or the peripheral light trapping material is thus reflected back toward the pixel.

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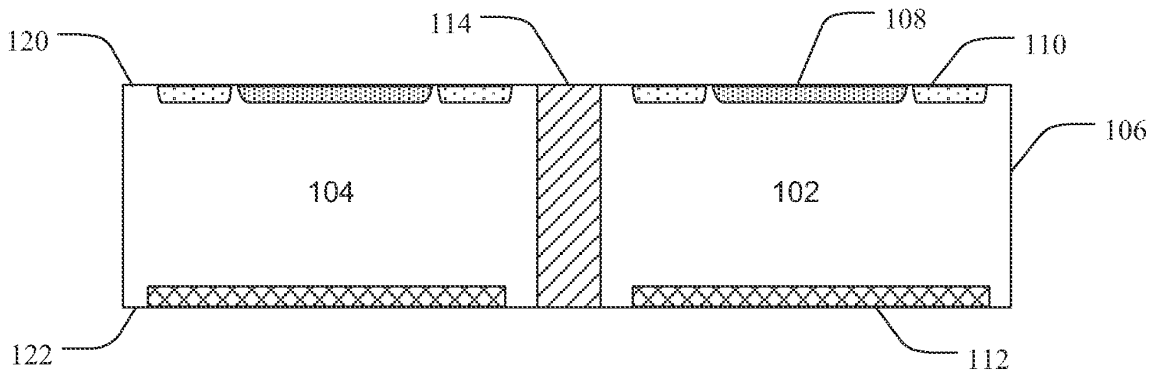

120
114
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122
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FIG. 1

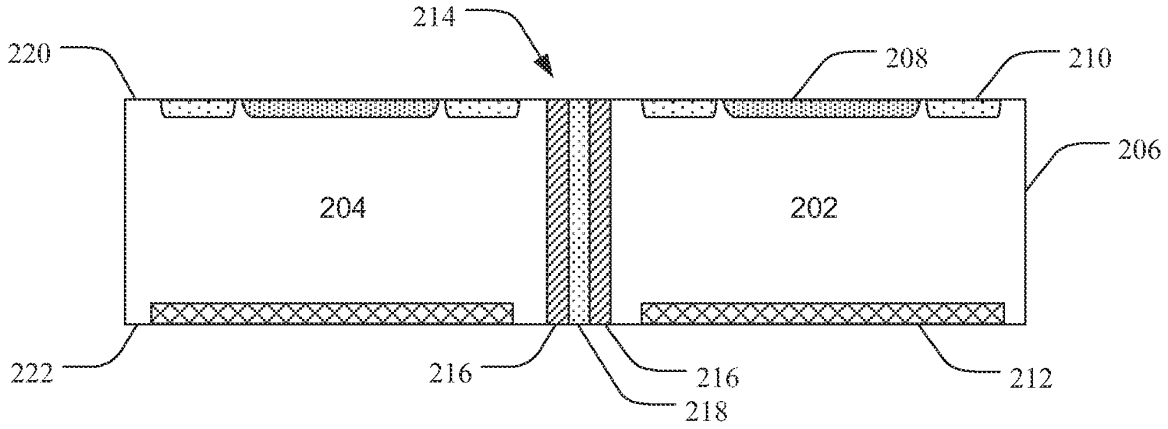

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FIG. 2

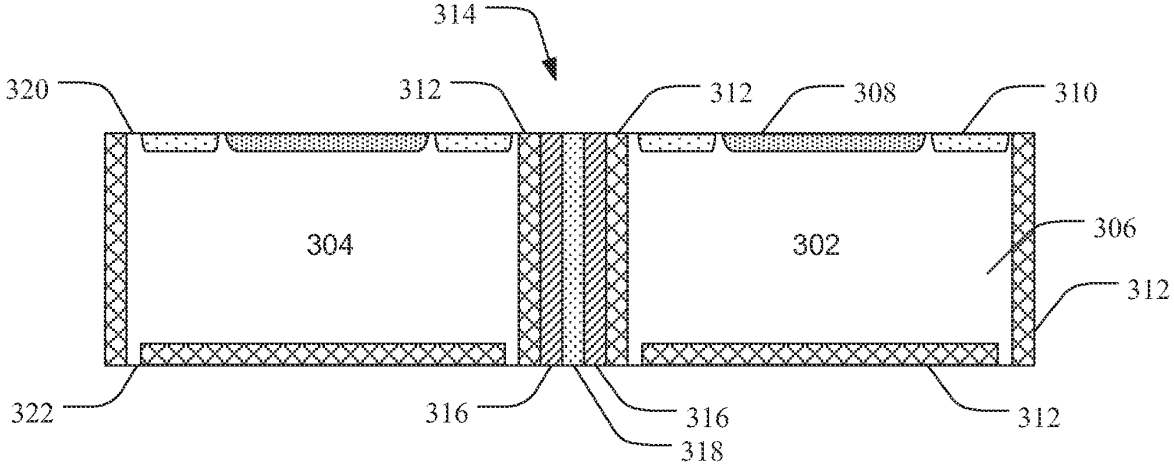


FIG. 3

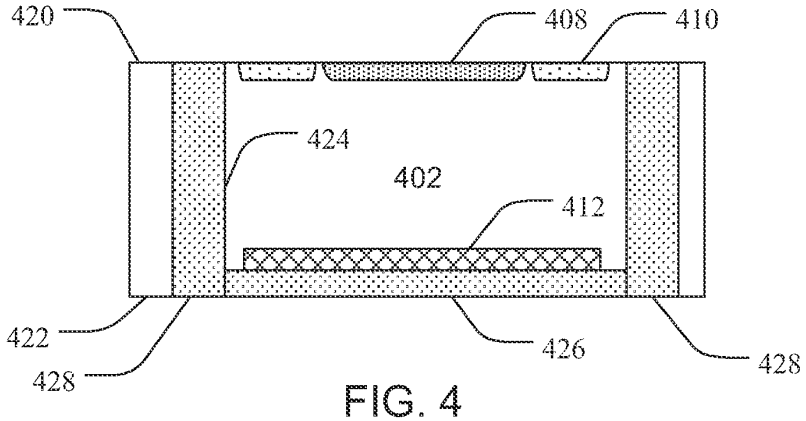


FIG. 4

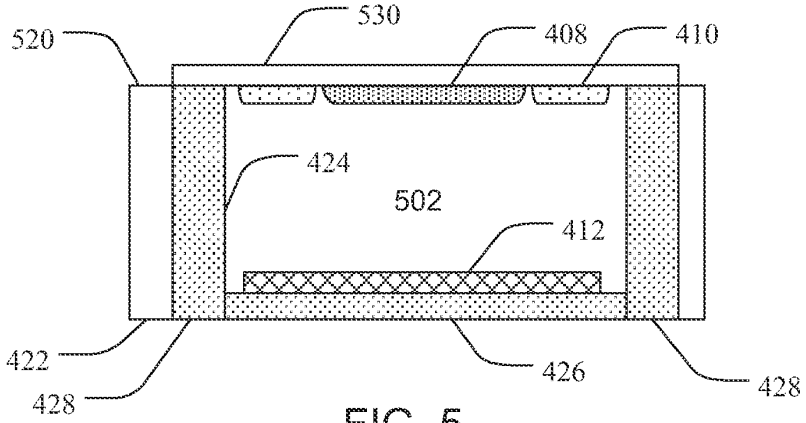


FIG. 5

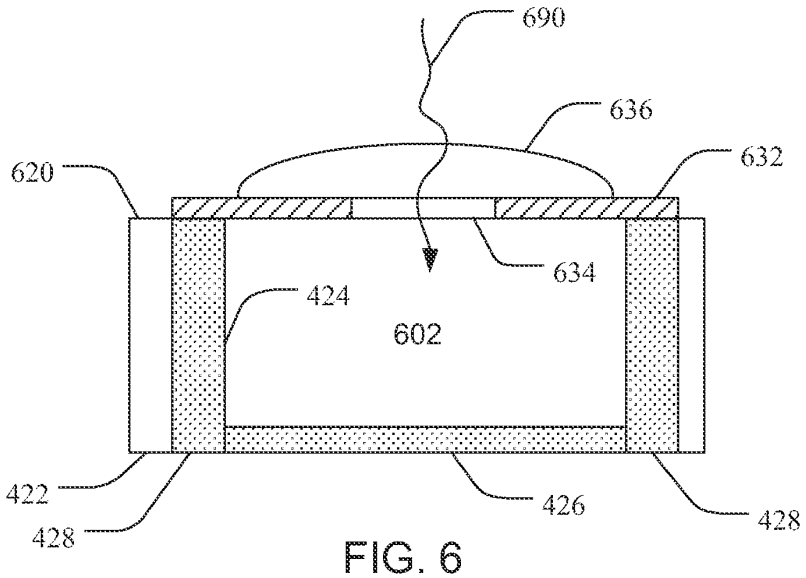


FIG. 6

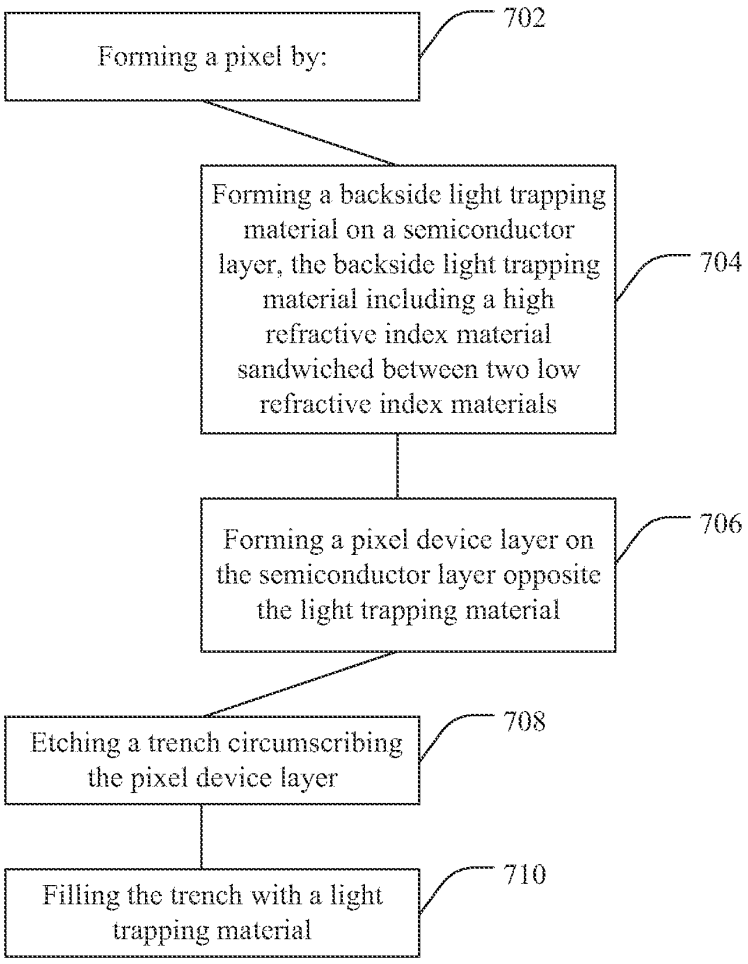

Forming a pixel by:
702
Forming a backside light trapping material on a semiconductor layer, the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials
704
Forming a pixel device layer on the semiconductor layer opposite the light trapping material
706
Etching a trench circumscribing the pixel device layer
708
Filling the trench with a light trapping material
710

FIG. 7

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Martin	U.	Pralle	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Wayland	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	15 Rice Spring Lane		
Address 2			
City	Wayland	State/Province	MA
Postal Code	01778	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	20551		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS		
Attorney Docket Number	3035-052.NP	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	20551		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	61614275	2012-03-22

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country i	Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Remove

◉	Assignee	○	Legal Representative under 35 U.S.C. 117
○	Person to whom the inventor is obligated to assign.	○	Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :	

If the Assignee is an Organization check here. ☒

Organization Name	SiOnyx, Inc.

PTO/AIA/14 (08-12)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	

Mailing Address Information:			
Address 1	100 Cummings Ctr., Suite 243-F		
Address 2			
City	Beverly	**State/Province**	MA
Country [i]	US	Postal Code	01915-6506
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Todd B. Alder/			Date (YYYY-MM-DD)	2013-03-15
First Name	Todd B.	Last Name	Alder	Registration Number	54598

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Electronic Acknowledgement Receipt

EFS ID:	15266881
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP
Receipt Date:	15-MAR-2013
Filing Date:	
Time Stamp:	18:42:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		3035-052NPapplication.PDF	334388 30c754ccbf3a31a6acf7f717d348b108632d3198	yes	32

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	26	
	Claims		27	31	
	Abstract		32	32	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	3035-052NPdrawings.pdf	34723 3f65ba1969d9079392f41965c3da2f42bbc7b00d	no	4
Warnings:					
Information:					
3	Application Data Sheet	3035-052NPappdata.pdf	1381683 ef3ff8084eeccf2644ab91fb87c5540a6888a6c0	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	1750794		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

FORMALITIES LETTER

OC000000061343307

Date Mailed: 05/28/2013

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  *Applicant must submit $**70** to complete the basic filing fee for a small entity.*

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of $ **520** as a small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- A surcharge (for late submission of the basic filing fee, search fee, examination fee or inventor's oath or declaration) as set forth in 37 CFR 1.16(f) of $ **70** for a small entity in compliance with 37 CFR 1.27, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is $ **1320** for a small entity
- $ **70** Statutory basic filing fee.
- $ **70** Surcharge.
- The application search fee has not been paid. Applicant must submit $ **300** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit $ **360** to complete the examination fee for a small entity in compliance with 37 CFR 1.27.
- Total additional claim fee(s) for this application is $ **520**
  - $ **520** for **13** total claims over 20.

Items Required To Avoid Processing Delays:

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Apple-Sony EX1002 Page 44

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  ALL
  Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/bcao/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IPR2025-00811
Apple-Sony EX1002 Page 45

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/841,120

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	33 minus 20 =	* 13	x 40 =	520	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1250		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/841,120	03/15/2013	2883	0.00	3035-052.NP	33	3

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

FILING RECEIPT

OC000000061343306

Date Mailed: 05/28/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)
Martin U. Pralle, Wayland, MA;

Applicant(s)
SIONYX, INC., Beverly, MA

Assignment For Published Patent Application
SIONYX, INC., Beverly, MA

Power of Attorney: None

Domestic Priority data as claimed by applicant
This appln claims benefit of 61/614,275 03/22/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 05/17/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/841,120**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

IPR2025-00811
Apple-Sony EX1002 Page 47

Title

PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

Preliminary Class

385

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Application Number:	13841120
Filing Date:	15-Mar-2013
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Todd Brent Alder/Nicole Solomon
Attorney Docket Number:	3035-052.NP

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	70	70
Utility Search Fee	2111	1	300	300
Utility Examination Fee	2311	1	360	360
Pages:				
Claims:				
Claims in excess of 20	2202	13	40	520
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	2051	1	70	70

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1320**

Electronic Acknowledgement Receipt

EFS ID:	16447487
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP
Receipt Date:	29-JUL-2013
Filing Date:	15-MAR-2013
Time Stamp:	20:05:05
Application Type:	Utility under 35 USC 111(a)

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Art Unit	2883
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Attorney Docket Number	3035-052.NP

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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Examiner Signature		Date Considered	

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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		WO 2011/119618	09/29/2011	Sionyx, Inc.		

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

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(12) AUSTRALIAN PATENT ABRIDGMENT
(19) AU (11) AU-B-36664/84

(54) LASER GROOVED SOLAR CELLS

(71) UNISEARCH LIMITED

(21) 36664/84 565214 (22) 23.12.83
(23) 13.12.84 (24) 23.12.83
(43) 27.6.85 (44) 10.9.87
(51)[3] H01L 31/18 H01L 31/06

(72) STUART ROSS WENHAM AND MARTIN ANDREW GREEN
(74) RI

(56) AU 78802/75 488420 H01L 15/04
US 4046594
US 4137123
EP 14759

(57) Claim

1. A method of manufacturing solar cells, said method comprising the steps of scribing a pattern of grooves or holes in a surface of semiconductor substrate with a laser scriber and subsequently forming a rectifying junction on said surface, said junction extending into said holes or grooves.

3. The method of claims 1 or 2 wherein after said scribing step and before forming the rectifying junction, an etching step is performed, said etching step comprising etching said grooves or holes with a chemical etchant, the etching step being used to control the shape of the grooves or holes in the final cell.

4. The method of claim 3 wherein the chemical etchant is selected to etch the base region of the grooves or holes more slowly than the top region to convert the grooves into V-shaped troughs and to convert the holes to shapes approximating inverted pyramids, and said junction extending into said troughs or inverted pyramids.

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565214

COMMONWEALTH OF AUSTRALIA

Patents Act 1952

APPLICATION FOR A STANDARD PATENT

I/WE, UNISEARCH LIMITED a company limited by guarantee and incorporated under the laws of the State of New South Wales, Australia, of 221-227 Anzac Parade, Kensington, New South Wales, Australia,

hereby apply for the grant of a Standard Patent for an invention entitled

"The Laser Grooved Solar Cell"

which is described in the accompanying provisional specification.

~~This application is made under the provision of Para XVI of the Patents Act 1952 for a patent or similar protection~~

~~is~~

~~APPLICATION ACCEPTED AND AMENDMENTS~~

ALLOWED 27-7-87

~~My~~/Our address for service is: F.B. RICE & CO.,
28A Montague Street,
Balmain, NSW 2041

Dated this 23rd day of December, 1983.

UNISEARCH LIMITED

LODGED AT SUB-OFFICE
23 DEC 1983
Sydney

By: Patent Attorney

To : The Commissioner of Patents
COMMONWEALTH OF AUSTRALIA

F.B. RICE & CO.,
Patent Attorneys,
Sydney

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~~DIVISIONAL~~ PROVISIONAL SPECIFICATION No. 36664/84

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Commonwealth of Australia
The Patents Act 1952
DECLARATION IN SUPPORT

In support of the (Convention) Application made by: UNISEARCH LIMITED

for a patent for an invention entitled: The Laser Grooved Solar Cell,

I (We) RICHARD PIERRE CARTMER
of and care of the applicant company do solemnly and sincerely declare as follows:

---

a) I am (We are) the applicant(s) for the patent

b) I am (We are) authorised by the applicant(s) for the patent to make this declaration on its behalf.

Delete the following if not a Convention Application.

The basic application(s) as defined by subsection 141(2) of the Act was (were) made

by

This is the case because (state reasons why the person who made the basic application(s) is not the applicant or why there is more than one applicant)

---

a) (Each) (We) believe the actual inventor(s) of the invention

b) STUART ROSS WENHAM of 17 Fortescue Street, Bexley North, N.S.W., 2207 and
MARTIN ANDREW GREEN, of 10 Blandford Avenue, Waverley, N.S.W., 2024

are) the actual inventor(s) of the invention and the facts upon which Unisearch Limited

is (are) entitled to make the application are as follows:

The applicant is the assignee of the invention from the said actual inventors.

Declared at KENSINGTON this 4th day of DECEMBER 19 94

Signed [signature] Status SENIOR OFFICER (LEGAL)

Declarant's Name RICHARD PIERRE CARTMER

F. B. RICE & CO PATENT ATTORNEYS
This form is suitable for any type of Patent Application. No legalisation required.

COMMONWEALTH OF AUSTRALIA

565214

Patent Act 1952

COMPLETE SPECIFICATION

(ORIGINAL)

Class Int. Class

Application Number : PG 3004
Lodged : 23 December 1983

Complete Specification Lodged :
Accepted :
Published :

Priority :

Related Art : 36664/84.

Name of Applicant : UNISEARCH LIMITED

Address of Applicant : 221-227 Anzac Parade, Kensington N.S.W. 2033

Actual Inventors : Stuart Ross Wenham; Martin Andrew Green

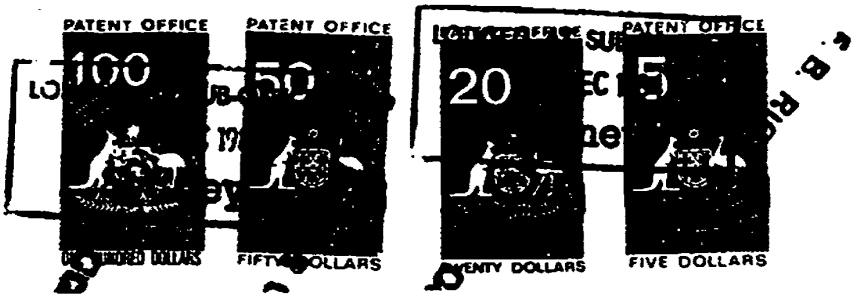
Address for Service : F.B. RICE & CO., Patent Attorneys, 28A Montague Street, BALMAIN. 2041.

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Sydney

Complete Specification for the invention entitled:

The Laser Grooved Solar Cell

The following statement is a full description of this invention including the best method of performing it known to us:-



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The present invention relates to improvements in the fabrication of solar cells whereby the structure of the cell facilitates collection of photon generated minority carriers from deep within the wafer substrate.

Long wavelength light striking a photocell will penetrate much further into the cell than shorter wavelength light, on average, before being absorbed and therefore minority carriers generated by photons of long wavelength energy must travel much further before being collected by the rectifying junction of the cell. As a result, the chances of a minority carrier resulting from a long wavelength photon, being collected before recombination occurs are greatly reduced over those of a minority carrier resulting from a shorter wavelength photon. This effect is even more pronounced in solar cells used in space, due to the radiation damage which is caused to a solar cell in this environment, and which results in a reduction in minority carrier life times.

In an attempt to overcome the effects of reduced minority carrier life time in the space environment, prior art solar cells have been produced wherein a plurality of grooves were chemically etched into the surface of the substrate prior to the formulation of the rectifying junction of the cell, such that the junction provided within the grooves penetrates deep into the bulk of the substrate to aid in the collection of minority carriers formed in the bulk regions.

However, while the formation of grooves in the substrate provides an improvement in short circuit current densities, complications associated with the chemical etching step make this solution too expensive to be of practical use, particularly in the case of mass produced cells for terrestrial use.

A laser scriber has previously been used to separate cells formed on a common wafer, by scribing a groove between

a pair of adjacent cells and then breaking the wafer along the scribe line in a similar manner to that used when cutting glass or ceramic tiles. Lasers have also been used to isolate doped regions of a substrate by cutting or drilling an opening between the two adjacent regions to be isolated, however, it has not previously been considered feasible to use lasers in the processing of the active regions of semiconductor devices, due to the damage to the crystal structure caused by the laser.

A first aspect of the present invention relies upon the unexpected result that grooves scribed in the surface of a substrate by way of a laser scriber do not cause a significant deleterious effect upon the solar cell subsequently formed on the substrate, due to crystal damage caused by the laser, but to the contrary the crystal damage provides getterring sites to which impurities in the substrate migrate during subsequent high temperature processing, thereby enhancing the performance of the solar cell by increasing the life time of minority carriers in the bulk of the substrate.

It has also been found that grooving of the surface of the cell enhances the anti-reflective properties of the cell, as light falling within the grooved area, if it is not initially absorbed by the cell, will be reflected onto another surface of the groove, thereby increasing the possibility of absorption. In order to escape from the grooved area, a photon will need to be reflected several times within the groove, and therefore the probability of escape is low.

The provision of grooves in the substrate also increases greatly the area of the cell junction and additionally provides the possibility of having differing sheet resistivities in the top layer of the cell, with a high resistivity in the region between the grooves to enhance the photovoltaic effect and a lower resistivity within the

grooves to decrease the series resistance of the cell and to allow the wider spacing of the contact fingers used to conduct current from the top layer.

According to a first aspect, the present invention consists in a method of manufacturing solar cells, said method comprising the steps of scribing a pattern of holes or grooves in a surface of a semiconductor substrate with a laser scriber and subsequently forming a rectifying junction on said surface, said junction extending into said holes or grooves.

Preferably embodiments of the invention achieve a plurality of parallel grooves or a regular pattern of holes by scribing the surface of the substrate using a laser scriber adapted to simultaneously scribe a repeating pattern of grooves or holes.

In a preferred embodiment of the invention, a chemical etching step is employed between the step of laser scribing and the step of forming the rectifying junction, such that precise control of the shape of holes and grooves is achieved.

Some embodiments of the invention will also make use of holes bored through the substrate during the laser etching step to allow contact to be made with the surface layer of the cell from the rear of the substrate.

Embodiments of the invention may also employ grooving of the rear surface of the substrate to form thin strong cell structures which have high efficiency and are radiation resistant.

In further embodiments of the present invention a solar cell is produced having a substrate, one surface of which has a plurality of grooves or hollows formed therein, and a rectifying junction formed on said surface and extending into said grooves, a top layer of said junction having a sheet resistivity which is greater in the region between the grooves than in the region within the grooves.

In yet further embodiments of the present invention

~~consists in~~ is produced having a solar cell ~~comprising~~ a substrate, opposite surfaces of which each have a plurality of grooves or hollows formed therein, a rectifying junction being formed on one of said surfaces and extending into the grooves or hollows of that surface.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings wherein:

Figure 1 schematically illustrates a sectional view of a solar cell manufactured in accordance with a first embodiment of the present invention;

Figure 2 schematically illustrates the solar cell of Figure 1 when viewed from the top;

Figure 3 schematically illustrates a sectional view of a solar cell manufactured in accordance with a second embodiment of the present invention;

Fig. 4 schematically illustrates a sectional view of a fully etched substrate according to an embodiment of the invention;

Fig. 5 schematically illustrates (a) a plan view of a laser scribing pattern; (b) a plan view of a fully etched substrate and (c) a perspective view of a fully etched substrate for a fourth embodiment of the invention;

Fig. 6 schematically illustrates (a) a plan view of a laser scribing pattern; (b) a plan view of a fully etched substrate and (c) a perspective view of a fully etched substrate for a fifth embodiment of the present invention;

Figs. 7, 8 and 9 schematically illustrate (a) a plan view of a laser scribing pattern and (b) a perspective view of a fully etched substrate for sixth, seventh and eighth embodiments respectively, of the present invention; and

Fig. 10 schematically illustrates an improved method of connecting electrodes to the embodiment of Fig. 8.

Referring to Figure 1, a substrate 10 is provided with a back contact 11 and a rectifying junction 12 on opposite

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surfaces, the junction being formed between the substrate 10, which may be of either p-type or n-type semiconductor material, but in this embodiment is p-type material, and a top layer 13 extending over the top surface of the substrate and which is formed of a semiconductor material of opposite impurity type to the substrate 10. Grooves 14 scribed in the top surface of the substrate by a laser scriber, prior to formation of the junction 12, greatly increase the junction area and at the same time facilitate the collection of minority carriers 15 generated deep within the bulk of the substrate, by placing sections of the junction in closer proximity to the region in which these carriers are generated.

Grooves 14 in the cell surface also improve the anti-reflection properties of the cell by acting as light traps. Light 16a striking the surfaces of the cell between the grooves, and which is not absorbed by the cell, will be reflected by the surface and wasted, however, light 16b striking a surface of one of the grooves 14, and which is not absorbed, will generally be reflected onto another surface of the groove, depending upon the angle of incidence of the light and the shape of the grooves. For light 16b falling normal to the top surface of the cell, the number of reflections within the groove 14 will be large, thereby reducing the percentage of light which is reflected out of the grooves.

A further improvement in the anti-reflective properties of the cell may be achieved by filling the grooves with a transparent material such as silicon oxide, and the slope of the groove walls can be optimized after scribing by an unmasked etch of the entire substrate surface.

As well as the improvement in current density due to the physical positioning of the junction within the groove and the increased area of the junction, a further improvement can be attributed to the production of getterring sites during the laser scribing of the surface of the substrate, thereby

allowing an increased degree of getterring during subsequent high temperature processing.

Getterring is the process by which impurities are attracted to certain areas of the substrate during high temperature processing, and typical getterring sites are regions of stress causd by diffusion processes and areas of crystal structure damage as caused by laser scribing. The laser scribing process, being a particularly robust process, creates a significant amount of damage to the crystal structure and accordingly a large number of getterring sites will be produced by this process.

The reduction in the number of impurities in the bulk of the substrate, as a result of getterring, has the effect of increasing the minority carrier life time and accordingly increasing the probability of a minority carrier being collected at the rectifying junction 12 before recombination occurs.

The series resistance of the grooved solar cell can also be decreased by selecting a lower sheet resistivity for the portion of the top layer 13 formed in the grooves 14 than for that used in the portion of the top layer between the grooves. In a non-grooved solar cell, manufactured for terrestrial use, the metal contact grid applied to the top layer is often applied by screen printing in order to keep cost to a minimum, however, screen printing imposes restrictions upon the minimum dimensions achievable, these being a minimum contact width of typically 150μm and a mimimum spacing of at least 3mm. With these contact dimensions, it is necessary to provide a top layer sheet resistivity in the order of 25 Ω/□ to 50 Ω/□ to minimize lateral resistance, however, such low values of sheet resistivity degrade the photovoltaic properties of the cell. This problem is less pronounced in cells produced for use in space, as in these cells a more sophisticated method of contact formation is used which allows the use of thinner

contacts having a closer spacing, such that higher sheet resistivities can be used without degrading the series resistance of the cell. However, the method of contact formation used in space cells adds considerably to their manufacturing costs.

In the case of grooved cells made according to the present invention, sheet resistivities in the order of 25Ω/□ to 50Ω/□ can be provided for that portion of the top layer 13 within the grooves 14, while sheet resistivities in the order of 100-200Ω/□ can be achieved in the top layer portions between the grooves. Typically the groove would be in the order of 50μm wide and the space between the grooves would be 100μm, the metal contact fingers 17 (see Fig. 2) running in the direction normal to the grooves and having the dimensions previously stated for screen printed contacts.

A lower sheet resistivity can be achieved in the grooved regions in numerous ways, some examples of which are:

(a) Diffuse the entire surface, oxidise and/or deposit nitride, form laser grooves through the oxide and/or nitride and first diffusion, chemically clean the grooves, complete a second heavy diffusion. This second diffusion will be localized to the grooved areas due to the blocking action of oxide and/or nitride.

(b) Oxidise wafer . as a thinner oxide than in (a) above results, form laser grooves through the oxide, chemically clean the grooves, and diffuse heavily. Oxide will partly block the diffusion in non-grooved areas resulting in a lighter diffusion in these areas.

(c) Dilute commercially available 'spin on' dopant source and apply to grooved surface. The source will coat non-grooved areas to a thickness determined by source viscosity and spin speed, but can completely fill grooves. This will result in a larger volume of source per unit surface area in grooved as opposed to non-grooved areas. Consequently more dopants will enter the surface in grooved

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areas in subsequent high temperature treatments than non-grooved areas.

(d) Diffuse entire grooved wafer surface heavily. Use dilute chemical etch to etch back diffused areas. The etch will have less opportunity for replenishment in grooved areas and will quickly become depleted and ineffective in these regions. Hence, diffused material will be selectively removed from non-grooved areas. A similar technique which makes use of plasma etching is also possible.

(e) Use a laser to locally heat the silicon in grooved regions subsequent to the application of a diffusion source.

The low sheet resistivity of the top layer in the grooved regions will have a detrimental effect on the response of the cell to short wavelength (blue) light due to the increased top layer thickness and therefore the sheet resistivity chosen will be a compromise between a value which gives low series resistance and a value which does not seriously degrade the response to blue light. It will be recognised, however, that while low sheet resistivity will degrade the response to blue light, the beneficial effects of

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low series resistance and improved current density due to increased junction area and the provision of a portion of the junction deep within the bulk of the substrate, will more than make up for this degradation. Further, the low sheet resistivity in the grooves will not seriously affect the response of the cell to long wavelength (red) light.

The use of a low sheet resistivity top layer in the grooved regions of space cells will also allow the contact fingers in these cells to be spaced more widely, thereby, allowing the use of less costly formation process and accordingly reducing the manufacturing costs of the cell.

Referring now to Figure 3 the metal contact fingers 17 in Figure 2 may be replaced by Conductor-Insulator-Silicon (CIS) contacts wherein the top layer 13 is a lightly doped region, the rectifying effect of the junction 12 being reinforced by the MIS contact comprising a thin layer of insulation 18 over the top layer and a metal, or a highly doped polycrystalline, contact finger 19 formed over the insulation layer 18. The fingers 19 will be arranged in a similar configuration to the metal fingers 17 shown in Figure 2, however, the insulation layer may either be formed over the entire surface of the cell, by using a transparent insulation layer such as a silicon oxide, or alternatively the insulation layer may be only formed in the region of the conductor finger 19.

Referring to Fig. 4 of the drawings, reflection properties of the laser groove cell can be optimised by arranging the grooving so that the sloping groove walls intersect with one another, thereby substantially eliminating the flat intergroove regions illustrated in Figs. 1, 2 and 3. With the structure of Fig. 4, the only ungrooved regions required are flat paths 21 (refer to Fig. 5) provided for the top contact metallisation.

As illustrated in Fig. 4, very precise control can be obtained of such structures in single crystal material by

using chemical etches with anisotropic properties, combined with laser grooving. For example, dilute caustic soda solutions etch silicon very slowly in the [111] crystal direction but etch very rapidly in other directions. Therefore, if the surface 22 of a wafer has [100] orientation and is grooved by a laser to form grooves 23 and then subsequently etched in dilute caustic soda solutions, the silicon is very quickly etched away until the [111] crystal planes are exposed to form the grooved surface 24 of Fig. 4. Once the [111] crystal planes, coinciding with the faces of the surface 24, are exposed, the rate of etching slows markedly, allowing precise control of the final etched surface shape, thereby allowing the resulting surface geometry of the device to be precisely defined by the depth and spacing of the original grooves 23.

Regardless of the method used to control the slope of the groove walls, interesting and useful structures can be obtained by the use of intermittent grooving of the cell surface and several such structures will now be described with reference to Figs. 5, 6, 7, 8 and 9.

Referring to Fig. 5, a "slat" structure is illustrated wherein the laser grooving 23 is intermittently broken by gaps 25 in order to provide strengthening ribs or struts 26 in the final etched substrate of Fig. 5(c). In addition, a larger gap 27 in the laser grooving pattern results in the flat path 21 in the final etched substrate which provides a location for top contact metallisation in the completed cell.

Turning to Fig. 6, the laser grooves 23 of Fig. 5 are replaced by holes 33 which are bored by the laser scriber in the square pattern illustrated in Fig. 6a, such that after etching, an inverted pyramid structure as illustrated in Fig. 6b and Fig. 6c is produced with the top surface 34 of the inverted pyramid structure again corresponding to the [111] crystal planes of the substrate.

Combined grooving of the front and rear surfaces of the

wafer and subsequent etching gives rise to a further class of cells which have been termed "crinkle cut" cells. Referring to Fig. 7, if a grooving pattern 43, similar to the pattern 23 of Fig. 5a is provided in a top surface of the wafer and a second grooving pattern 53, again similar to the pattern 23 of Fig. 5a, is provided in the bottom surface of the wafer and the wafer is subsequently etched, a structure of the form illustrated in Fig. 7b will be produced, wherein parallel grooves run along both sides of the wafer, the grooves in one side corresponding with the peaks in the other side of the wafer to provide a corrugated structure having strengthening struts or ribs 46 and (ribs 56 not shown) and the surfaces 44 and 54 each corresponding to [111] crystal planes of the substrate.

Figs. 8 and 9 illustrate additional "crinkle cut" structures, the structure of Fig. 8 comprising inverted pyramids similar to those of Fig. 6 on each side of the wafer, with the pyramids on one side of the wafer being offset from those on the other side, while the structure of Fig. 9 has inverted pryamids on the top surface and a crossed groove structure on the bottom surface to provide an etched wafer structure having a substantially constant thickness as is the case with the structure of Fig. 7. The structures of Fig. 7 and Fig. 9 allow very thin strong cells having good reflection properties to be fabricated and these structures will assist in the production of very high efficiency cells with good radiation resistance. The structure of Fig. 8 on the other hand will produce cells having good reflection properties with moderate thickness but great strength.

The laser grooving technique can also be used to produce structures which have holes extending right through the cell from one side to the other. The structures illustrated in Figs. 6, 8 and 9 are particularly suited to this technique. The advantage of a structure which employs holes passing completely through the cell is that it is then possible to

have both contacts to the cell made on the rear surface of the cell, thereby avoiding the losses associated with top contact shading. For example, a section of a structure similar to that of Fig. 6 is illustrated in Fig. 10, wherein the grooving is much greater than that previously illustrated such that the apex 35 of inverted pyramids extends to the back surface of the wafer. With this structure, once the top layer 13 has been formed, metallised top contacts 36 can be provided from the back of the cell at each apex point. This technique allows an improvement in overall cell efficiency by removing the problem of top contract shading which would otherwise occur, while at the same time allowing connections to the top contacts to be of greater current carrying capacity, as the trade off between current carrying capacity and degree of shading is no longer necessary.

The laser used to produce any of the previous laser groove structures can be programmed very simply to punch holes through the cell in any prescribed location so that a variety of such punch through structures are possible with this approach and clearly the punch through technique can be used with any of the structures previously described.

A preferred method of manufacturing laser groove cells requires starting with a silcon wafer of desired surface orientation (for example [100])and then grooving one or both sides of the cell in the desired pattern using a laser. The wafer is then etched in an appropriate chemical solution to define the shape of the walls of the groove. Thereafter, cell processing proceeds as it would with prior art devices. The top junction is formed by the diffusion of an appropriate dopant and, if desired, a back surface field region is formed at the rear of the cell. Top and rear contact metallization can then be formed by any chosen sequence, e.g. vacuum deposition, screen printing or electroplating, as can the antireflection coating.

It will be recognised by persons skilled in the art that

numerous variations and modifications may be made to the invention as described above without departing from the spirit or scope of the invention as broadly described.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A method of manufacturing solar cells, said method comprising the steps of scribing a pattern of grooves or holes in a surface of semiconductor substrate with a laser scriber and subsequently forming a rectifying junction on said surface, said junction extending into said holes or grooves.

2. The method of claim 1 wherein said laser scriber is adapted to simultaneously scribe a plurality of grooves or holes in said substrate.

3. The method of claims 1 or 2 wherein after said scribing step and before forming the rectifying junction, an etching step is performed, said etching step comprising etching said grooves or holes with a chemical etchant, the etching step being used to control the shape of the grooves or holes in the final cell.

4. The method of claim 3 wherein the chemical etchant is selected to etch the base region of the grooves or holes more slowly than the top region to convert the grooves into V-shaped troughs and to convert the holes to shapes approximating inverted pyramids, and said junction extending into said troughs or inverted pyramids.

5. The method of claims 1, 2, 3 or 4 wherein the laser scriber is used to bore holes through the substrate during the laser scribing step and the junction extends through said holes to cover a portion of the rear surface thereof such that contact can be made with the top layer of the cell from the rear of the substrate.

6. The method of any one of the preceding claims, wherein grooving of the rear surface of the substrate is employed to reduce the thickness of the cell structure, grooves in the rear surface being located between grooves in the top surface of the substrate.

7. A solar cell manufactured using the method as claimed in any one of the preceding claims wherein said rectifying

junction has a top layer with a sheet resistivity which is greater in the region between the grooves than in the region within the grooves.

8. A solar cell as claimed in claim 7, wherein the sheet resistivity of the top layer within the grooves is in the order of 25-50 Ω/□ while sheet resistivity of the top layer between the grooves is in the order of 100-200 Ω/□ .

9. A solar cell as claimed in any one of claims 7 or 8 wherein holes are provided through the substrate, the top layer of the rectifying junction extending into the through holes and metalized top contacts being provided on the back of the substrate at each of said holes to make an electrical connection with the top layer of the junction.

10. A solar cell, made in accordance with the method of claim 1.

11. A method of manufacturing a solar cell as claimed in claim 1, substantially as hereinbefore described.

12. A solar cell substantially as hereinbefore described with reference to the accompanying drawings.

DATED this 7th day of July 1987

UNISEARCH LIMITED
Patent Attorneys for the
Applicant:

F.B. RICE & CO.

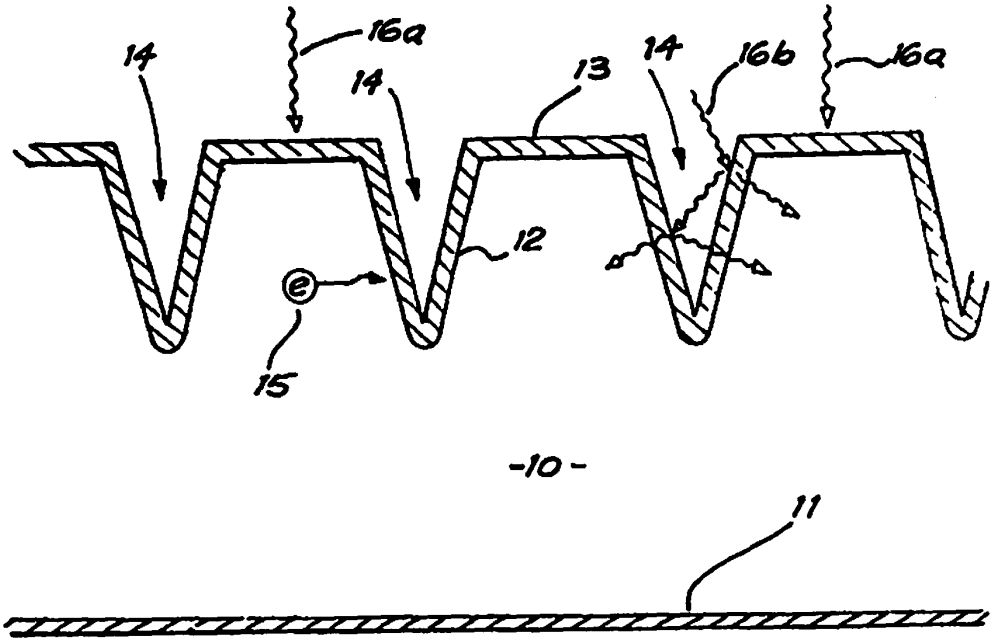


FIG.1

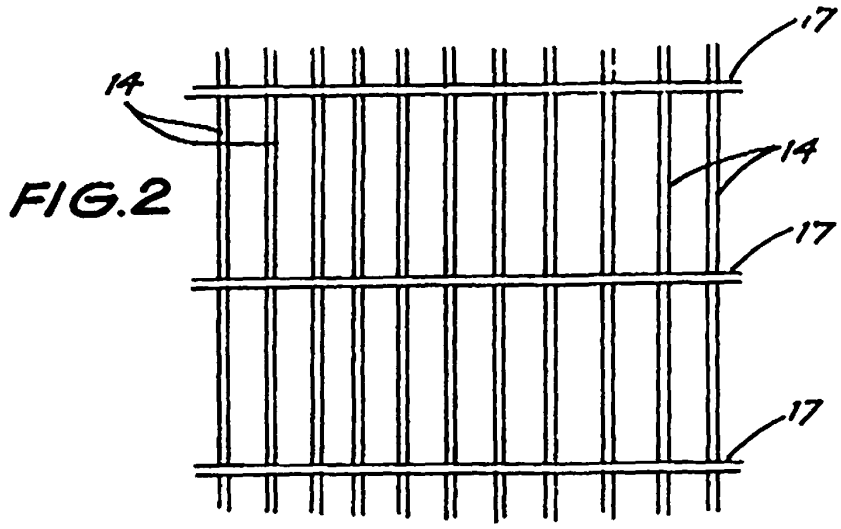


FIG.2

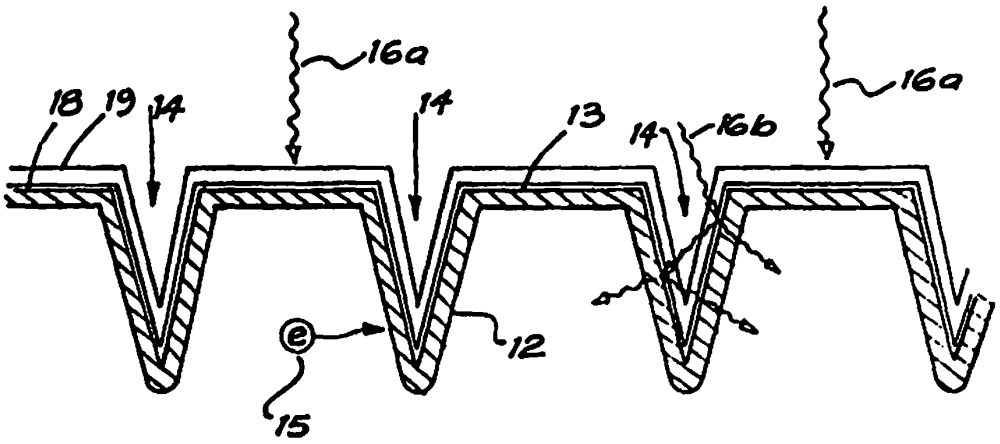


FIG. 3

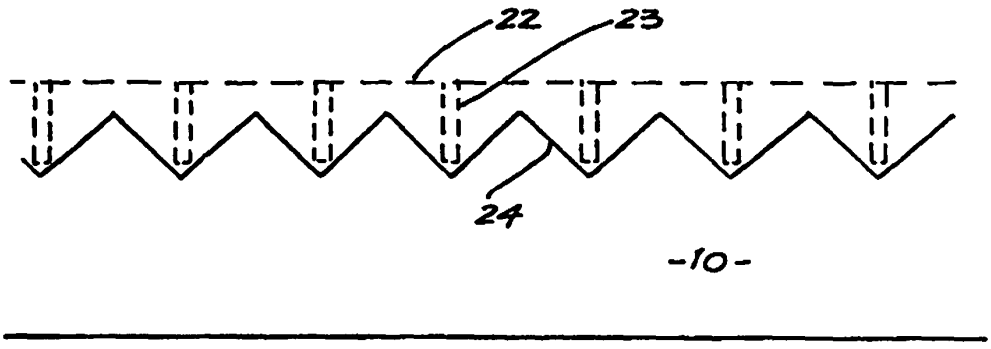


FIG. 4

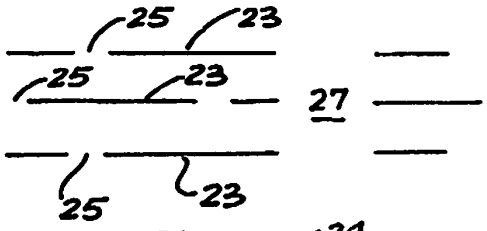


FIG. 5a

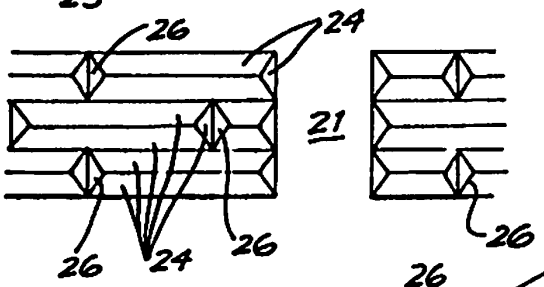
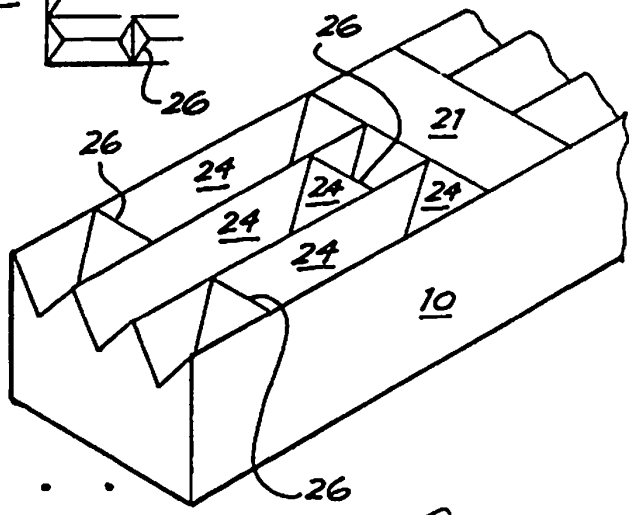


FIG. 5b

FIG. 5c



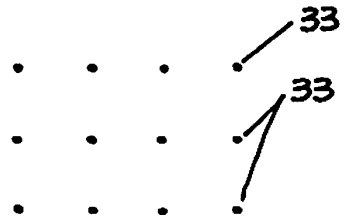


FIG. 6a

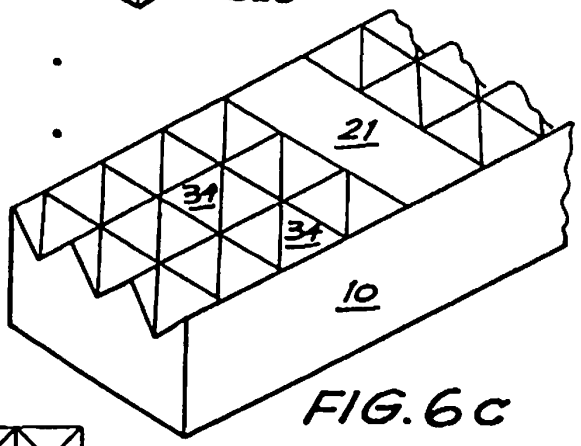


FIG. 6b

FIG. 6c

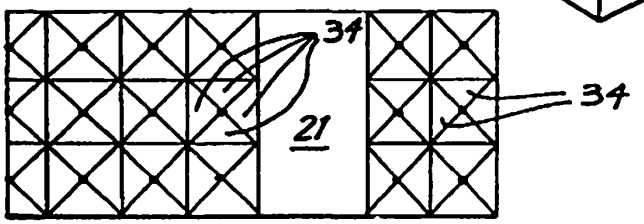


FIG. 7a

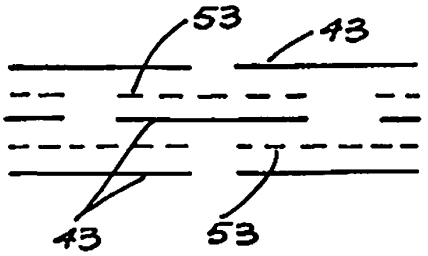
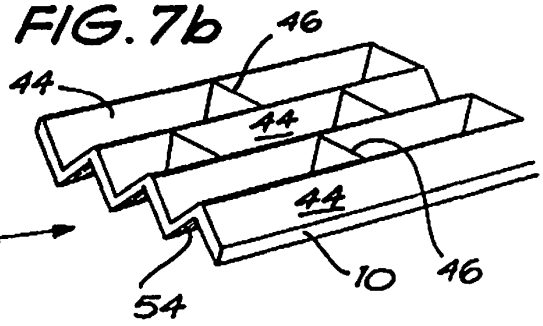


FIG. 7b



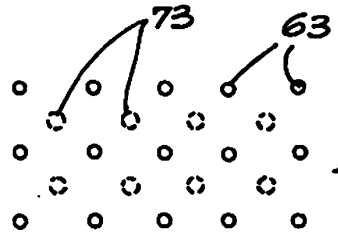


FIG. 8a

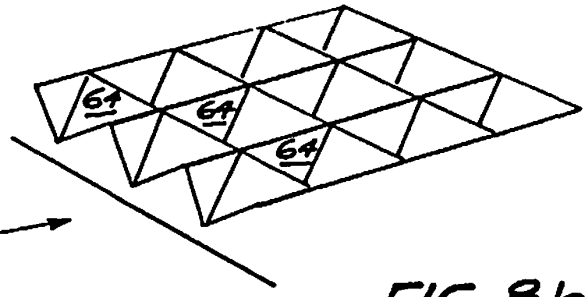
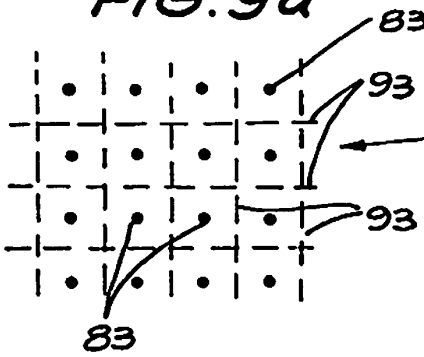


FIG. 8b

FIG. 9a



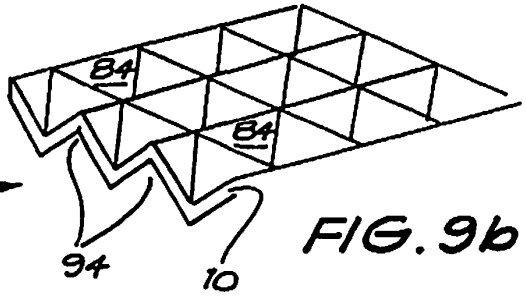


FIG. 9b

FIG. 10

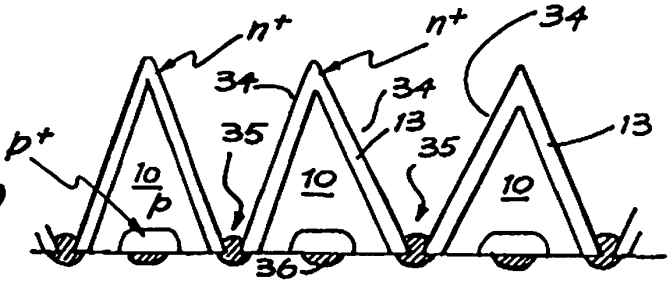


FIG. 7a

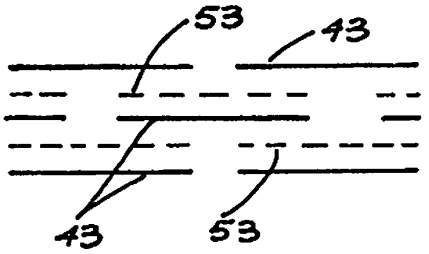
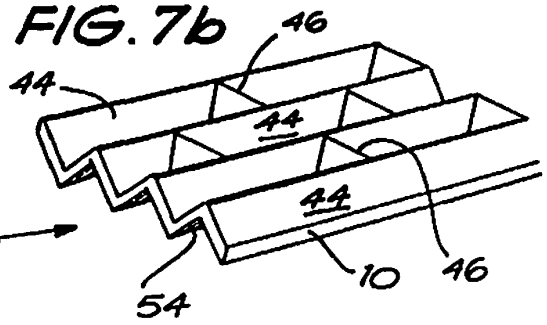


FIG. 7b



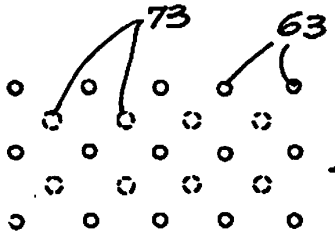


FIG. 8a

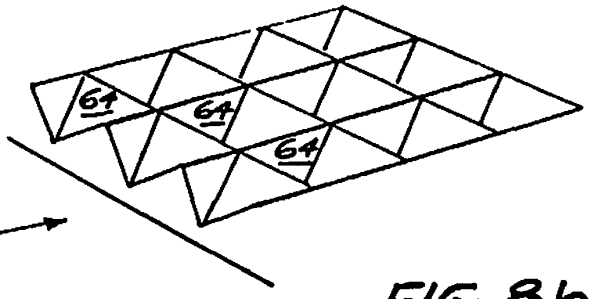
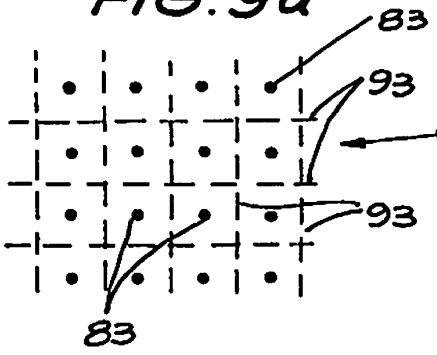


FIG. 8b

FIG. 9a



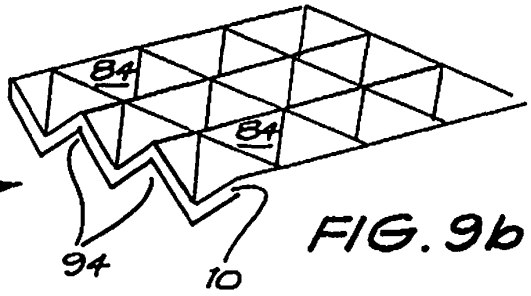
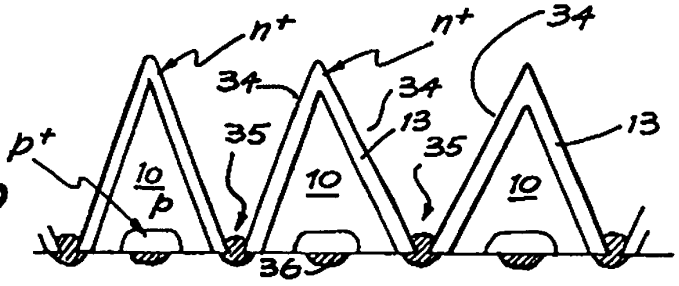


FIG. 9b

FIG. 10



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10 Apr 1980
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9C3 9L 9R1 LCX
(56) Documents cited
GB 1477670
GB 1258657
GB 1176889
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H1K
(71) Applicant
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Essex
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Ricardo Simon Sussmann
Allen William Mabbitt
(74) Agents
C Goodman

(54) **Laser treatment of semiconductor material**

(57) A layer or layers of amorphous material deposited on a non-crystalline amorphous substrate are subjected to treatment by exposure to a laser beam. The treatment may either recrystallise or anneal the amorphous material depending on the laser power and improves its suitability for such devices as solar cells by improving the life times and diffusion lengths within the material as compared to the untreated material.

The use of P type SiC or polycrystalline silicon on superposed i and n type amorphous silicon layers to improve the transmissivity of the outer layers of solar cells, and the use of varying composition SiC layers for visible light emission devices are also disclosed.

GB 2 030 766 A

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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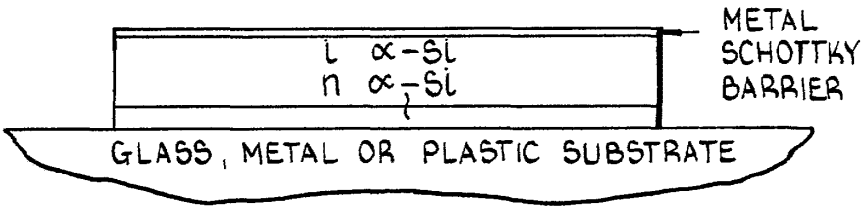


FIG. 1.

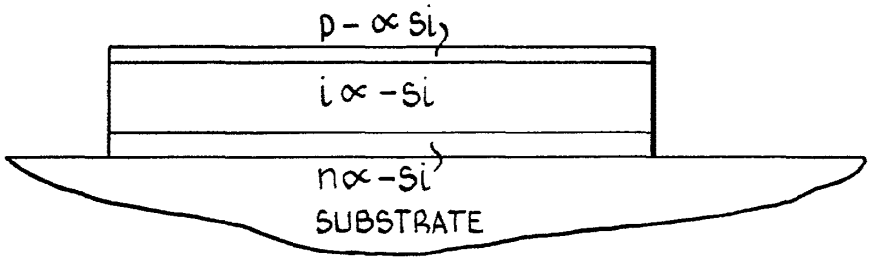


FIG. 2.

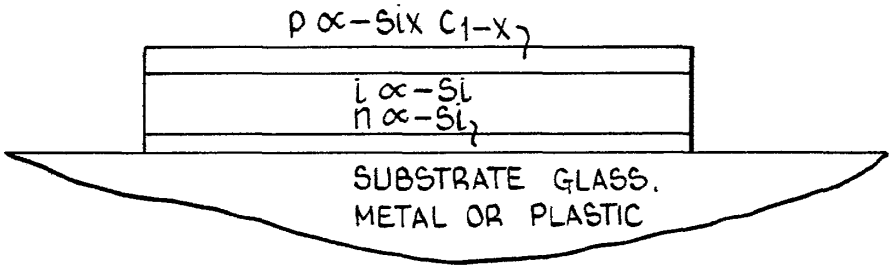


FIG. 3.

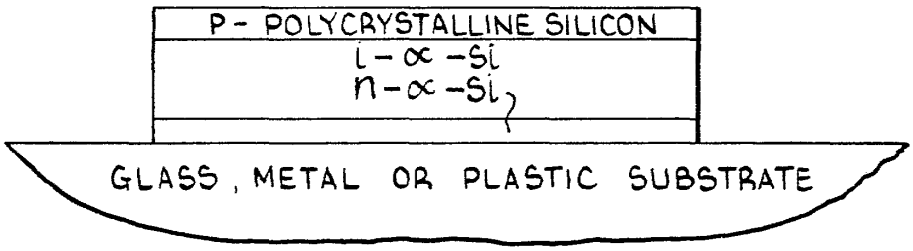


FIG. 4.

SPECIFICATION

Improvements in or relating to solar cells and other devices.

The present invention relates to method of treatment of amorphous material layers to make them more suitable for the production of solar cells and other similar devices and to the solar cells and or other devices produced using the treated materials.

The possible use of thin film amorphous materials for solar cells, (or other devices such as p–n junctions, Schottky diodes, zener diodes) integrated into large area systems such as displays is extremely attractive due to the relatively low cost in terms of materials and energy. A disadvantage however, is that device performance has previously been severely limited by the short life times and diffusion lengths typical of amorphous materials. For example, the present state of the art A.M.I. efficiencies for polycrystalline silicon solar cells is about 10% which is a factor of 2 higher than the best cell produced with amorophous material.

It is an object of the present invention to produce a treated layer of amorphous material which is substantially superior to that known at present and thus to be able to combine the advantages in terms of the low cost and large area capability of amorphous thin film with the superior device performance of the polycrystalline material.

According to the present invention there is provided a method of treating one or more layers of amorphous material deposited on a non-crystalline substrate, to improve the suitability of the material for use in solar cells or similar devices as hereinbefore defined, by subjecting the layer of amorphous material to exposure by a laser.

The present invention also provides an amorphous silicon solar cell comprising an upper layer of p type Si_xC_{1-x} an intermediate layer of i_x–Si and a lower layer of n Si on a suitable substrate.

The invention also provides an amorphous silicon solar cell comprising an upper layer of p type polycrystalline silicon an intermediate layer of i –Si and a lower layer of n Si on a suitable substrate.

In a preferred embodiment the amorphous material is silicon.

Embodiments of the present invention will now be described, by way of example with reference to the accompanying drawings, in which:

Figure 1 shows a conventional schottky barrier cell,

Figure 2 shows a conventional P–i–n barrier cell,

Figure 3 shows a first solar cell heterostructure according to the present invention and,

Figure 4 shows a second solar cell structure according to the present invention.

An amorphous silicon layer or multi-layer amorphous structure of 6,000Å was grown on an amorphous non-crystalline substrate e.g. glass, metallised glass or stainless steel by known methods, for example the glow discharge decomposition of SiH_4 or by sputtering. The amorphous layer or layers are then subjected to exposure by a suitable laser. The effect of the exposure to the laser is either to crystallise a controlled thickness of the amorphous structure when a high power is used to anneal the amorphous layer when a lower power is used.

The recrystallised layer possesses optical and electronic properties which make it more suitable as part of a solar cell, p–n junction or other devices.

In the case of the annealed, non-recystalised layer the properties will tend to reduce the density of the defect states in the gap.

Referring now to the drawings current practise when using amorphous-silicon (α– Si) for solar cells is to use p–i–n or Schottky barrier – i – n structures, as shown in Figs. 1 and 2. These approaches limit the attainable solar conversion efficiency, for any quality *i*–Si, because of the p layer or metal Schottky barrier prevents a large proportion of the incident light from reaching the depleted *i* region. If these surface layers could be replaced by a relatively optically transparent material, which still forms an electrically active junction, then the device efficiency would be improved.

This invention replaces the pα –Si or metal Schottky barrier with an amorphous layer of 'p' type Si_xC_{1-x} in which 0×1 as shown in Fig. 3. Amorphous $S1_xC_{1-x}$ forms a continuous series of solid solutions with a bandgap that increases as x decreases, thus a larger fraction of the incident light reaches the junction depletion than with conventional structures. This application therfore provides a heterojunction α–SiC/Si structure.

Further uses of this concept includes

$$Si_xC_{1-x}/Si_yC_{1-y}/Si_xC_{1-x}/\text{glass/metal}$$

or plastic substrate structures for visible light emission which would have applications for flat panel displays.

Referring now to Fig. 4 a second preferred solar cell according to the present invention is shown. Current amorphous silicon solar cells are limited in efficiency because of absorption or reflection of light by the top pα–Si or metal Schottky barrier layer. The solar cell shown in Fig. 4 reduces the wastage of input photons by forming a p–n junction between p-type polycrystalline silicon and the conventional i–nα–Si layers as shown in Figs. 1 and 2. The cell is therefore more efficient than previously known solar cells.

In the above shown solar cells suitable front

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and rear contact metallisations are applied to realise a working structure.

CLAIMS

1. A method of treating one or more layers of amorphous material deposited on a non-crystalline substrate, to improve the suitability of the material for use in solar cells or similar devices as hereinbefore defined by subjecting the layer of amorphous material to exposure by a laser.

2. A method of treating one or more layers of amorphous material as claimed in claim 1 in which the amorphous material is silicon, or hydrogenated amorphous silicon or silicon carbide or gallium arsenide or gallium phosphide.

3. A method of treating one or more layers of amorphous material as claimed in claim 2 in which the amorphous silicon or hydrogenated amorphous silicon is deposited on the amorphous substrate using the glow discharge decomposition of SiH_4.

4. A method of treating one or more layers of amorphous material as claimed in any one of the preceding claims in which the exposure is at a low enough level so that the material is not recrystallised but is annealed so as to reduce the number of defect states in the gap with a consequent improvement in lifetime and diffusion lengths.

5. A method of treating one or more layers of amorphous material as claimed in any one of the preceding claims in which the exposure is at a level high enough to recrystallise at least one layer of the amorphous material.

6. A method of treating one or more layers of amorphous material substantially as described.

7. An amorphous silicon solar cell comprising an upper layer of p type Si_xC_{1-x}, and intermediate layer of iα–Si and a lower layer of nαSi mounted on a suitable substrate.

8. An amorphous silicon solar cell comprising an upper layer of p type polycrystalline silicon an intermediate layer of iα–Si and a lower layer of nαSi mounted on a suitable substrate.

9. An amorphous silicon solar cell substantially as described with reference to Fig. 3 or 4 of the accompanying drawings.

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PATENT ABSTRACTS OF JAPAN

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G02B 6/13
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H01L 31/02
H01S 3/18

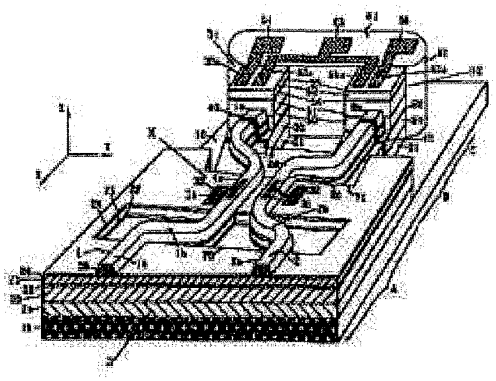
(21)Application number : **06-256229**
(22)Date of filing : **26.09.1994**

(71)Applicant : **FR TELECOM**
(72)Inventor : **GHIRARDI FREDERIC**
GIRAUDET LOUIS

(30)Priority
Priority number : **93 9311404** Priority date : **24.09.1993** Priority country : **FR**

(54) MONOLITHIC INTEGRATED STRUCTURE, ITS FABRICATION AND MONOLITHIC INTEGRATED HETERODYNE RECEIVING CIRCUIT

(57)Abstract:
PURPOSE: To provide a monolithic integrated structure including two photoelectric components connected optically through an optical guide by forming, in si.tu, at least one insulation barrier permitting optical transmission between two photoelectric components.
CONSTITUTION: A new silicon nitride protective mask is deposited on the entire structure and a groove-like window is made in the mask over the entire width thereof along a plane extending in parallel with YZ plane. The window is useful for forming an insulation barrier 40 by preferably diffusing a p+ conductivity type element deeply up to a substrate 10. The barrier 40 can isolate two detection diodes D1, D2 electrically from a coupler K by forming an npn double junction in the direction along the X axis and can transmit light between them. The double junction formed in si.tu corresponds to head/tail fixing of two diodes.



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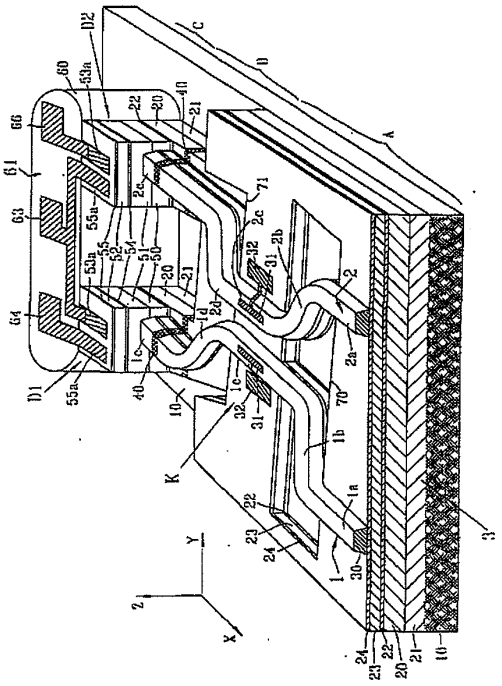
(74)代理人　弁理士　佐藤　一雄　（外３名）

(54)【発明の名称】　モノリシック集積構造体及びその製造方法、並びにモノリシック集積ヘテロダイン受信回路

(57)【要約】

【目的】　光電要素を含むモノリシック集積構造体及びその製造方法、並びにモノリシックヘテロタイン受信回路を提供する。

【構成】　本発明は光ガイドによって光学的に相互に接続された２つの光電成分（Ｋ，Ｄ１）を含むモノリシック集積構造の製造方法に関するものである。この方法は、２つの光電成分の間に光を伝送することのできる少なくとも１つの絶縁バリヤ（４０）を、下記の手段の少なくとも１つによってこれらの光電成分間にインシチュ形成する段階を含む：与えられた導電型の元素による反対導電型の構造区域の局所ドーピング、または半絶縁物質層のエピタキシャル蒸着。



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【特許請求の範囲】

【請求項１】光ガイドによって光学的に接続された２つの光電成分を含むモノリシック集積構造体の製造方法において、前記２つの光電成分の間の光伝送を可能とする少なくとも１つの絶縁バリヤを形成する段階を含み、前記バリヤ（４０、２４０）はインシチュ（in situ）形成されることを特徴とするモノリシック集積構造体の製造方法。

【請求項２】少なくとも一方の光電成分と光ガイドとの間の光伝送はエバネッセンス(Evanescence) 効果によって実施されることを特徴とする請求項１に記載の方法。

【請求項３】少なくとも一方の光電成分と光ガイドとの間の光伝送は突き合わせ接合によって実施されることを特徴とする請求項１に記載の方法。

【請求項４】絶縁バリヤ（４０）は与えられた導電型の元素をもって構造の反対導電型の少なくとも１つの区域を局所ドーピングすることによって形成されることを特徴とする請求項１乃至３のいずれかに記載の方法。

【請求項５】ドーピングは、構造の表面から、前記元素を光ガイドを通して構造の絶縁基板（１０）まで深部拡散することによって実施されることを特徴とする請求項４に記載の方法。

【請求項６】ドーピングは、構造の表面から、前記元素を光ガイドを通して構造の絶縁基板（１０）までイオン注入することによって実施されることを特徴とする請求項４に記載の方法。

【請求項７】構造は重ね合された相異なる導電型の少なくとも１つの第１層と少なくとも１つの第２層とを含み、前記第１層の１つの区域のドーピングが前記第１層の導電型と反対の導電型を有する第１元素によって実施され、前記第１層のドーピング区域から片寄った前記第２層の１つの区域のドーピングが前記第２層および前記第１元素の導電型と反対の導電型を有する第２元素によって実施され、２つの光電成分の間にｎｐｎ型およびｐｎｐ型の２つの絶縁接合を形成することを特徴とする請求項５または６に記載の方法。

【請求項８】ドーピングは与えられた型の元素を構造の中間層の中に混入させることによって実施され、この中間層は前記元素の導電型と反対の導電型を有する２つの層の中間にエピタキシャル成長によって付着されることを特徴とする請求項２に記載の方法。

【請求項９】前記元素はｐ＋導電型を有することを特徴とする請求項５、６および８のいずれかに記載の方法。

【請求項１０】絶縁バリヤ（２４０）は半絶性縁物質層のエピタキシャル成長によって実施されることを特徴とする請求項２に記載の方法。

【請求項１１】前記半絶縁性物質は鉄を含有するリン化インジウムから成ることを特徴とする請求項１０に記載の方法。

【請求項１２】ｎ＋導電型の光インピーダンス整合層

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（５０）が、光ガイドと、この光ガイドによりエバネッセンス(Evanescence) 効果で光を伝送される少なくとも一方の光電成分との間に配置されることを特徴とする請求項４乃至１１のいずれかに記載の方法。

【請求項１３】前記モノリシック集積構造体はヘテロダイン受信回路であって、この受信回路は直列に接続された２つの検出ホトダイオード（Ｄ１，Ｄ２）と、電気的に平衡されうる３ｄＢカプラー（Ｋ）とを含み、前記カプラー（Ｋ）が前記光電成分の一方を成し、また前記のホトダイオード（Ｄ１，Ｄ２）がそれぞれ前記光電成分の他方を成すことを特徴とする請求項１乃至１２のいずれかに記載の方法。

【請求項１４】２つの光電成分の間において光を伝送することのできる絶縁性バリヤ（４０）をこれらの成分間にインシチュ形成されたことを特徴とする光ガイドによって光電的に相互に接続される２つの光電成分を含むモノリシック集積構造体。

【請求項１５】前記バリヤは与えられた導電型の元素をもって構造の反対導電型の少なくとも１つの区域をドーピングすることによって形成されることを特徴とする請求項１４に記載のモノリシック集積構造体。

【請求項１６】前記バリヤは、前記光ガイドと前記の光電成分との間に半絶縁物質層をエピタキシャル成長することによって形成されることを特徴とする請求項１５に記載のモノリシック集積構造体。

【請求項１７】直列に接続された２つの検出ホトダイオードと、電気的に調整可能の３ｄＢ－カプラーとを含み、前記検出ホトダイオードと前記カプラーとの間に絶縁バリヤ（４０、２４０）がインシチュ形成され、このバリヤが前記カプラーと前記検出ホトダイオードとの間の光伝送を可能とすることを特徴とするモノリシック集積ヘテロダイン受信回路。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は光電分野に関するものであり、さらに詳しくは本発明は別個に形成された成分の組立てよりは、成分そのものの製造テクノロジーを含むモノリシック集積構造体の分野に関するものである。特に本発明は非限定的にヘテロダイン受信回路の製造に関するものである。

【０００２】

【従来の技術、及び発明が解決しようとする課題】文献、"Integrated balanced mixer receiver on InP（Ｉｎｐ上の集積平衡ミキサ受信機），トロンマーほか、4th InP and Related Compounds Conference, WE3, Newport 1992" は、直列に接続された２つの検出ホトダイオードと、２つの光ガイドを含む３ｄＢ－カプラーとを有するモノリシック集積ヘテロダイン受信回路を記載している。カプラーがそれぞれの入力としての光ガイドにおいて、変調される信号Ｓと、局所発振器によって

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発生される基準信号Ｒとを受け、出力としての２検出ホトダイオードにおいて、それぞれ前記信号ＳとＲの半和と半差に対応する２つの信号を出力する。ホトダイオードは、それぞれS^2＋２Ｓ・Ｒ＋R^2 およびS^2－２Ｓ・Ｒ＋R^2 の形の前記半和と半差の係数の平方を表わす電気信号を出力する。直列の２つのホトダイオードの搭載により、これらの２つの式の差、すなわち４Ｓ・Ｒの形の電気信号を共通点に集めることができる。このような受信機の利点は、局所発振器からノイズR^2 が除去され、また信号Ｒの振幅が信号Ｓの振幅よりはるかに大であるので、有効信号Ｓを増幅することにある。しかし実際上、完全に平衡されたカプラー、すなわち入力信号ＳとＲの半和と半差を正確に出力することのできるカプラーを作製することは困難であるので、多数の集積構造を作製し、適正に平衡されていないカプラーを有する集積構造を選別して放棄しなければならない。前記の構造においては、２つの光ガイドが半絶縁物質の基板上に形成されるので、これらの２つの光ガイドの絶縁の問題は生じない。

【０００３】他の集積モノリシック構造の例として、文献、"Directional Coupler,Balanced PIN Pair and JFET integrated on Inp Towards Receiver OEICs"L.Giraudet et al., Proceeding of fourth optoelecronic conference,PDP, 14July 1992" が挙げられる。この構造においては、カプラーの２つの光ガイドが導電性物質で形成され、２つの直列搭載ホトダイオードの電極の間に光ガイドを通して流れる漏れ電流が観察され、この漏れ電流が構造の性能を低下させる。しかし、カプラーの２つの光ガイドを導電性物質で形成することは、カプラー上にそれぞれ一方の光ガイドと組合わせて形成された２つの電極を通して電圧を加えまたは電流を注入することによりカプラーを電気的に平衡させうるという利点がある。この電流注入または電圧印加は、光ガイドの案内層を成す物質の指数の変動を生じ、従って物質中を伝播する光信号の位相を調整することが可能である。

【０００４】また他の文献、"Balanced Operation of a GaInAs/GaInAsp multiple-quantum-well Integrated Heterodyne Receiver, IEEE Photonics Technology LettersVol.2, No.8., August 1990" には、同一構造体上に２つの光ガイドを直列に接続せず、このようにして２つのホトダイオードの電極間の漏れ電流の問題を回避する方法が提案されている。２つのホトダイオードがそれぞれ出力する電気信号を別個に増幅し、次にその一方から他方を減算して前記の項S^2 とR^2 とを除去する。各ホトダイオードによって出力される電気信号のそれぞれ別個の増幅は、R2 の変動によるノイズをもはや抑止しないという欠点がある。

【０００５】米国特許第５，１２２，８５２号明細書には、共通基板上に搭載されてそれぞれ光ガイドと組合わされた２つの半導体検出器を含む集積構造が記載されている。前記基板と光ガイドは非半導体絶縁物質から成り、これは電気絶縁の問題を生じないが、検出器のモノリシック集積が不可能であり、これらの検出器は複雑ないわゆる「エピタキシャル・リフトオフ」法によって形成されなければならない。従ってモノリシック集積構造でないこのような構造は製造コストが高い。

【０００６】文献、"ELECTRONICS LETTERS, V1.24,No.23, 10 November 1988, STEVENAGEGB, PAGES 1457-1458, S.Chandrasekhar et al., "Balanced dual photodiode sintegrated with a 3dB directional coupler for coherent lightwave receiv-ers" には、光ガイドについて導電性物質を使用して光ガイドの断面積を低減させその長さを増大することによって漏れ電流を低減させる方法が提案された。しかし光ガイドの抵抗率がなおも相当に低く、メグオーム（ＭΩ）のオーダであり、いずれにせよ光ガイドの長さに依存するので、容積および製造コストの問題を生じる。

【０００７】文献、"22 GHz Photodiode monolithically integrated with optical wave-guide on semei-insulating InP using novel Butt-Joint structure, Kato etal., Electronic Letters, 1992, pp.1140-1143" には、光ガイドの端面上に、この光ガイドとホトダイオードとの間に絶縁層を形成する方法が記載されている。光ガイドとホトダイオードの形成後にこれらのホトダイオードと光ガイドとを分離するために反応性イオンビーム腐食法（ＲＩＢＥ）によって垂直溝をエッチングし、この溝の中に絶縁層としてのシリカ薄膜がマグネトロンによって蒸着される。しかしこの方法によれば、エッチングされる溝の幅を制御することが困難であり、従ってホトダイオードと光ガイドとの間に形成される無定形シリカ薄膜の厚さを制御してこれらの光ガイドとホトダイオードとの間に最適光伝送を保証することが困難である。

【０００８】特開平３－２９２，７７７号公報に記載の集積構造体においては、半導体レーザおよび検出器の成分層の形成後に絶縁性バリヤがエピタキシャル成長させられる。これらの２つの成分が導電性基板上に形成されて共通電極を保持するので、２成分間の絶縁が不完全である。同様にＥＰ４２２，８５４号公開明細書の中に提案された構造体においては、ホトダイオードと光増幅器が共通電極を保持する。本発明は前記の問題点を解決しようとするものである。

【０００９】

【課題を解決するための手段】従って本発明の目的は、光ガイドによって光学的に接続された２つの光電成分を含むモノリシック集積構造の製法において、前記２つの光電成分の間の光伝送を可能とする少なくとも１つの絶縁バリヤを形成する段階を含み、本発明によれば前記バリヤはインシチュ（in situ ）形成されることを特徴とするモノリシック集積構造体の製造方法を提供するにあ

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る。

【００１０】従って、先行技術による提案と相違し、本発明によれば、後で絶縁物質によって充填されるべき溝を予め正確にエッチングする必要がない。本発明によれば、構造体の成分の製造中にまたは製造後に、この構造中にこれら２成分間の光通路に配置された溝をエッチングすることなく、絶縁バリヤを形成することができる。

【００１１】望ましくは、光電成分の少なくとも一方と光ガイドとの間の光伝送はエバネッセンス(Evanescence) によって実施される。他の実施態様として、この光伝送は突き合わせ接合によって実施される。

【００１２】本発明の第１実施態様によれば、絶縁バリヤは与えられた導電型の元素をもって構造の反対導電型の少なくとも１つの区域を局所ドーピングすることによって形成される。

【００１３】好ましくは、ドーピングは、構造の表面から、前記元素を光ガイドを通して構造の絶縁基板まで深部拡散することによって実施される。他の実施態様において、ドーピングは、構造の表面から、前記元素を光ガイドを通して構造の絶縁基板までイオン注入することによって実施される。好ましくは前記元素はｐ＋導電型を有する。もし適当なら、構造が重ね合された相異なる導電型の少なくとも１つの第１層と少なくとも１つの第２層とを含む場合、第１層の１つの区域のドーピングが前記第１層の導電型と反対の導電型を有する第１元素によって実施され、前記第１層のドーピング区域から片寄った前記第２層の１つの区域のドーピングが前記第２層および前記第１元素の導電型と反対の導電型を有する第２元素によって実施され、２つの光電成分の間にｎｐｎ型およびｐｎｐ型の２つの絶縁接合を形成する。絶縁を改良するため、直列に配置された数個の絶縁接合を同様に形成することができる。

【００１４】前記実施態様の変形として、ドーピングは与えられた型の元素を構造体の中間層の中に混入させることによって実施され、この中間層は前記元素の導電型と反対の導電型を有する２つの層の中間にエピタキシャル成長によって付着される。

【００１５】好ましくは前記元素はｐ＋導電型とする。

【００１６】本発明による方法の第２実施態様においては、絶縁バリヤは半絶縁物質層のエピタキシャル成長によって形成される。好ましくは前記半絶縁物質は鉄を含有するリン化インジウムから成る。

【００１７】望ましくは、ｎ＋導電型の光インピーダンス整合層が、光ガイドと、この光ガイドによりエバネッセンス(Evanescence) 効果で光を伝送される少なくとも一方の光電成分との間に配置される。

【００１８】本発明による方法は、直列に接続された２つの検出ホトダイオードと、電気的に平衡されうる３ｄＢカプラーとを含み、前記カプラーが前記光電成分の一方を成し、また前記のホトダイオードがそれぞれ前記光電成分の他方を成すように成されたヘテロダイン受信回路のモノリシック集積構造体を製造するために使用される。

【００１９】また本発明は、２つの光電成分の間において光を伝送することのできる絶縁性バリヤをこれらの成分間にインシチュ形成されたことを特徴とする光ガイドによって光電的に相互に接続される２つの光電成分を含むモノリシック集積構造体にある。

【００２０】本発明のモノリシック集積構造体の１実施態様においては、前記バリヤは与えられた導電型の元素をもって構造の反対導電型の少なくとも１つの区域をドーピングすることによって形成される。

【００２１】本発明のモノリシック集積構造体の他の実施態様においては、前記バリヤは、前記光ガイドとこの光電成分との間に半絶縁物質層をエピタキシャル蒸着することによって形成される。

【００２２】本発明のさらに他のモノリシック集積構造体においては、直列に接続された２つの検出ホトダイオードと、電気的に調整可能の３ｄＢ－カプラーとを含み、前記検出ホトダイオードと前記カプラーとの間に絶縁バリヤがインシチュ形成され、このバリヤが前記カプラーと前記検出ホトダイオードの間の光伝送を可能とする。

【００２３】

【実施例】下記の説明において、用語および用語結合、「長さ、前方、後方」、「側方」、および「厚さ、垂直、上方、下方」は付図の参照フレーム（Ｘ，Ｙ，Ｚ）のそれぞれＸ軸、Ｙ軸およびＺ軸にそった距離または位置を示す。

【００２４】図１乃至図４に図示の２つのモノリシック集積構造例はそれぞれ本発明の方法によって構成されたものであって、いずれもヘテロダイン受信回路に関するものであり、これらの回路はそれぞれ、直列に接続されたＰＩＮ型の２つの検出ホトダイオードＤ１，Ｄ２と、電気的に調整可能の３ｄＢカプラーＫとを含み、前記カプラーＫは２つの光ガイドを含み、これらの光ガイドはその上部にそれぞれの案内ストリップ１、２を有する。

【００２５】これら２つの集積構造は、ＸＺ面に対して平行な対称中面に対して対称的である。

【００２６】光ガイドの中への光の導入は構造の正面３から実施され、この正面３は平面であって、Ｘ軸線に対して垂直であり、案内層２０の中にあり、この案内層２０は下記に説明するように下方閉込め層２１と上方閉込め層２２とに挟まれている。案内ストリップ１、２は、これらのストリップの被覆する案内層区域の中に光を閉込め、またこれらのストリップは正面３から始まって、Ｘ軸に対して平行な相互に離間する直線部分１ａ，２ａを示し、これらの直線部分から後方に２つの湾曲部分１ｂ，２ｂが延長され、これらの湾曲部分から２つの相互に近接した直線部分１ｃ，１ｄが延長され、これらの直

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線部分１ｃ，１ｄはＸ軸に対して平行に並列されてカプラーＫの作動区域を成し、次に２つの後方に湾曲した部分１ｄ，２ｄが延在し、これらの湾曲部分は相互に離間して、これらの湾曲部分からそれぞれ２つの直線部分１ｅ，２ｅが延長され、これらの直線部分１ｅ，２ｅは相互に離間してＸ軸に対して平行に延在しそれぞれホトダイオードＤ１，Ｄ２に終わっている。

【００２７】下記において、Ａ、ＢおよびＣはそれぞれ構造の３区域を示し、これらの区域はＸ軸に対して垂直な２つの面P_{AB}とP_{BC}とによって区画されている。

【００２８】案内ストリップ１と２は区域ＡとＢの上に延在し、ホトダイオードＤ１，Ｄ２は区域Ｃの中に形成される。面P_{AB}は、後方湾曲部分１ｄ，２ｄと後方直線部分１ｅ，２ｅとの接合部分近くで案内ストリップ１、２と交わっている。

【００２９】図１および図２のモノリシック集積構造は本発明の第１実施態様に対応する。この構造は半絶縁性物質の基板１０を含み、この基板は付図においてダイシング後にＸ軸にそった細長い平行六面体として図示され、この基板はこの実施例においては鉄の含有によって半絶縁性に成されたリン化インジウムから成り、その抵抗は10^{7} Ωｃｍである。

【００３０】半絶縁性基板組立体１０の上に、例えば金属－有機化学蒸着法（ＭＯＣＶＤ）または分子－ビームエピタキシャル成長法（ＭＢＥ）による第１エピタキシャル成長によって逐次下記の層が蒸着される。

【００３１】ａ）０．５μｍの厚さとｎ導電型のＩｎＰから成る指数n_1の下方閉込め層２１、

ｂ）ｎまたはｎ－導電型と０．６５μｍの厚さを有する４元ＩｎＧａＡｓＰから成るn_1より大きな指数n_2の光案内層２０と、

ｃ）ｎ－導電型のＩｎＰから成り、０．０５μｍの厚さを有する指数n_2以下のn_3の上方閉込め層２２と、

ｄ）０．４μｍの厚さを有し、ｎ＋導電型の４元ＧａＩｎＡｓＰ物質から成る光インピーダンス整合層５０と、

ｅ）０．９μｍの厚さを有し、ｎ－型固有導電性を有する３元ＧａＩｎＡｓ物質から成るＰＩＮホトダイオードの吸収層５１と、

ｆ）５０ｎｍの厚さを有し、それ自体公知のように次の２元物質層との漸進的結合を成すための４元ＧａＩｎＡｓＰの薄層５４と、

ｇ）０．４μｍの厚さを有し、ｎ導電型のＩｎＰから成るＰＩＮホトダイオードの上方閉込め層５２と、

ｈ）０．０５μｍのオーダの厚さを有し、ｎ導電型の３元ＧａＩｎＡｓ物質から成るホトダイオードの接触薄層５５と、

ｉ）図示されていない、エピタキシャル成長再開用の厚さ０．１μｍのＩｎＰ保護層。

【００３２】次に、カプラーＫの２つの光ガイドが形成される構造部分（区域ＡおよびＢ）において、前記ＩｎＰ保護層および前記層５５，５２，５４，５１および５０が除去される。このようにして露出された薄い上方閉込め層２２上に第２エピタキシャル成長が実施されて、これらの構造部分Ａ、Ｂにおいて逐次、下記層が形成される。

【００３３】ｊ）層２２と同一組成の厚さ０．１５μｍのＩｎＰから成る上方閉込め層２３と、

ｋ）厚さ２５ｎｍのｎ導電型の４元ＧａＩｎＡｓＰ物質から成る薄いブロッキング層２４と、

ｌ）厚さ０．８ｍｍで、案内ストリップ１、２をその上にエッチングするためのｎ導電型のＩｎＰから成る上方閉込め層３０。

【００３４】次に、窒化ケイ素保護マスクが構造全体に蒸着され、次に案内ストリップ１、２の線図に従って前記マスクを乾式エッチングし、次に上方閉込め層３０の保護されていない部分を除去することによりこれらのストリップが形成される。

【００３５】案内ストリップ１、２のエッチング後に、樹脂から成る第２保護マスクが構造全体の上に配置され、このマスクは案内ストリップ１、２のそれぞれ湾曲部分１ｂ，２ｂおよび１ｄ，２ｄに跨るウインド７０と７１を示す。これらのウインドの中においてブロッキング層２４と上閉込め層２２、２３を化学腐食によって除去し、図１に図示のようにこれらのウインドの中において案内層２０の上側面を露出させる。

【００３６】次に構造全体の上に新しい窒化ケイ素保護マスクを蒸着し、次にこのマスクの中に構造の幅全体に延在する溝穴状のウインドをＹＺ面に対して平行な面にそって形成する。このウインドは、本発明の方法の第１実施態様により、望ましくは亜鉛のｐ＋導電型の元素を基板１０まで前記ウインドを通して深く拡散させることによって絶縁バリヤ４０を形成するのに役立つ。このバリヤ４０は、Ｘ軸にそった方向にｎｐｎ二重接合を形成して、２つの検出ホトダイオードＤ１，Ｄ２とカプラーＫとを相互に電気的に絶縁させ同時にこれらの間に光を伝送させることができる。５００℃の温度での光照射に際して、上方閉込め層２２、２３、２４、３０のＩｎＰの厚さ約１μｍと、４元物質案内層２０の厚さ０．６５μｍと、下方閉込め層２１のＩｎＰの厚さ０．５μｍとを通して拡散するためには約３０分が必要である。光ガイドの中において、ｐ＋ドーピングは、相互に平行でＸ軸に対して垂直な２面４０ａ，４０ｂの間に局限される。これらの２つの面は、構造のｎ導電型またはｎ－導電型の区域Ｂの中に配置されている。このようにインシチュ形成された二重接合は２つのダイオードの頭／尾取付けに相当し、電流の横断に抵抗すると共にこの光ガイド中の光通過を可能とする。

【００３７】本発明による方法の第１実施態様の変形においては、構造の表面からＺ軸方向に基板まで延在する長方形断面の潜函の形状の２つの絶縁バリヤを形成し、

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それぞれのバリヤの内部に２つのダイオードを配置することができる。

【００３８】光ガイドを形成する層の全部が同一型の導電性でない場合、または光ガイドの導電型と反対の導電型を有する他の層がこの光ガイドの上に蒸着された場合、ＹＺ面に対して平行でＸ軸にそって片寄った２つの面にそって延在する２つの深いドーピングによって絶縁が実施される。この場合、与えられた型の各導電層上に２つのｎｐｎダイオード接合とｐｎｐダイオード接合とを頭／尾形成するように、２つの反対導電型の元素を使用してドーピングを実施することができる。

【００３９】図示の実施例において絶縁バリヤ４０は光ガイド中の光通路の中に配置されている。

【００４０】また本発明の主旨の範囲内において、段階（ｂ）後に、段階（ｃ）前に、ｎ導電型またはｎ－導電型の案内層２０上に、ｐ＋導電型層を蒸着し、次にこのｐ＋導電型層の上にｎ導電型またはｎ－導電型の上方閉込め層２２を蒸着することによって、エピタキシャル成長段階中に絶縁層をインシチュ形成することができる。この場合、絶縁バリヤは、光ガイドを出てホトダイオードに向かう光のエバネッセント型通路の中に配置される。

【００４１】亜鉛の深部拡散による絶縁バリヤ４０の形成後に、案内ストリップ１、２の相互に近接した直線部分１ｃ，２ｃ上にそれぞれ配置された２つのウインドと、ホトダイオードＤ１，Ｄ２の接触層５５上の他の２つのウインドとの合計４ウインドが同一窒化ケイ素マスクを通して拡散によって形成される。この場合、光ダイオードの層５５、５２の中にこれらのウインド５３ａを通して亜鉛が拡散されてｐ＋導電型の２区域５３を形成し、また層３０の中に案内ストリップ１、２の厚さの半分まで亜鉛が拡散されてカプラーＫを平衡させるための２つのｐ＋導電型電極区域３１を形成する。

【００４２】また前述のように、層３０と５２の中にＺｎの拡散による同時的ドーピングを可能とするように、これらの層３０、５２を同一素材で製造するのが望ましいことを注意しよう。

【００４３】次に、ブロッキング層２４上に、案内ストリップ１、２の相互に近接した直線部分１ｃ，２ｃの側方に、それぞれ隣接拡散区域３１に電気的に接続されたカプラーＫの２つの接点３２が配置されている。

【００４４】同様に、各ホトダイオードＤ１，Ｄ２上にそれぞれｎ－接点５５ａとｐ－接点５３ａが金属化によって配置され、これらの接点はそれぞれ各ホトダイオードの拡散区域５３の外側にある接点層５５の一部とこの拡散区域５３とに接続されている。

【００４５】望ましくは、４元物質から成る光インピーダンス整合層５０は、上方閉込め層２２の指数n_3より大きな指数n_4を示す。層５０の厚さは好ましくは反射防止層を成すように選定され、またこの層５０が光ガイドの上方に配置されていることはキャリヤの走行時間を制限させる。光が光ガイドから出てホトダイオードに向かうエバネッセンス(Evanescence) 伝送のために必要な吸収長さを短縮させ、従ってホトダイオードの容量を制限するように、層５０が案内層より大きな光指数を示すことが望ましい。

【００４６】次に、図１に図示の形状と合致するように、樹脂マスクを通してイオンビームエッチング法（ＩＢＥ法）によって、構造区域Ｂ，Ｃにおいて２つのホトダイオードＤ１，Ｄ２が基板１０まで彫刻される。彫刻区域は構造の前記面P_{AB}から後方に構造の後側面まで達する。前記の光ガイドは、その案内ストリップ１、２の後方直線部分１ｅ，２ｅによって覆われる部分において彫刻され、この彫刻部分はＸ軸にそって絶縁バリヤ４０の両側に延在し、従って光ガイドの絶縁バリヤ４０の前方に延在する部分とホトダイオードとの間に電気的接触はありえない。

【００４７】次にポリアミドから成る電気的接触支持パッド６０がそれ自体公知のように配備され、このパッドの上側面６１の上に金属化によって接点６４、６３、６６が形成され、これらの接点はそれぞれホトダイオードＤ１のｎ－接点５５ａ、ホトダイオードＤ１のｐ－接点５３ａおよびホトダイオードＤ２のｐ－接点５３ａに接続される。同様に接点６３はホトダイオードＤ２のｎ－接点５５ａに接続されているので、２つのホトダイオードＤ１，Ｄ２は支持パッド６０の接点６３によって直列に接続されている。

【００４８】図３と図４は本発明の方法の第２実施態様によって形成された構造を示す。

【００４９】図１と図２の素子と同様の図３と図４の素子は単に１００を加えた数字によって示される。もちろん、これらの素子の組成に関する説明は下記の説明に適用されるものとする。

【００５０】この実施態様において、第１エピタキシャル成長段階において光ガイドの上方閉込め層１２２の上に半絶縁物質の層２４０をエピタキシャル成長によって付着することによって電気的絶縁バリヤを形成する。この第１エピタキシャル成長段階においては層１５０、１５１、１５４、１５２、および１５５も付着される。あるいは変形として、層２４０を直接に光案内層１２０の上に付着することも考えられる。

【００５１】望ましくは層２４０は、鉄の含有によって半絶縁化されたＩｎＰ（ＩｎＰ：Ｆｅ）から成る。

【００５２】次に構造区域Ａ，Ｂの化学腐食によって層２４０を除去した後に、第２エピタキシャル成長段階を実施し、この段階において層１２３、１２４、１３０を付着する。

【００５３】案内ストリップ１０１、１０２をエッチングする際に、層２４０と短絡する接点を防止するため、ホトダイオードＤ１，Ｄ２の前縁を含む面P_{BC}から、こ

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れらのストリップ１、２の後側面２０２を分離するギャップ２０１をエッチングすることを注意しなければならない。このギャップ２０１は好ましくはＸ軸方向に３μｍのオーダの幅を有し、垂直に層１２２に達する。本出願の前文に記載の最後の公表と相違し、このギャップ２０１は単に絶縁の役割を有するのであって光によって横断されないのであるから、これを高度に精密に形成することは不必要である。

【００５４】本発明は前記の説明に限定されない。特に、カプラーの一方の案内ストリップに対して光学的に接続された局所発振器を使用することも考えられる。

【図面の簡単な説明】

【図１】本発明の第１実施態様によるモノリシック集積＊構造の概略斜視図。

【図２】図１の構造のＸ－Ｚ面に対して平行な面における断面図。

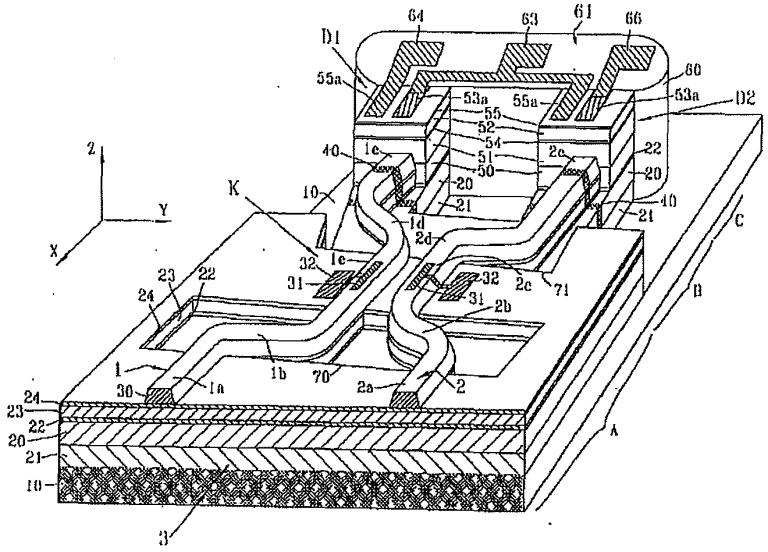
【図３】本発明の第２実施態様によるモノリシック集積構造の概略斜視図。

【図４】図３の構造のＸ－Ｚ面に対して平行な面における断面図。

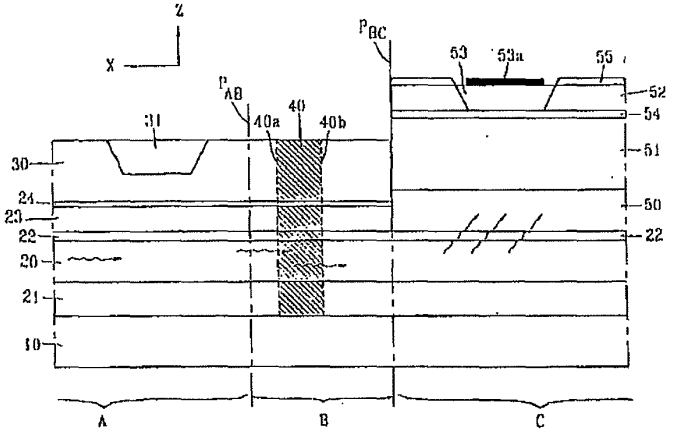
【符号の説明】

１０　基板
４０　絶縁性バリヤ
２４０　絶縁性バリヤ
Ｄ１，Ｄ２　検出ホトダイオード
Ｋ　３ｄＢ－カプラー

【図１】

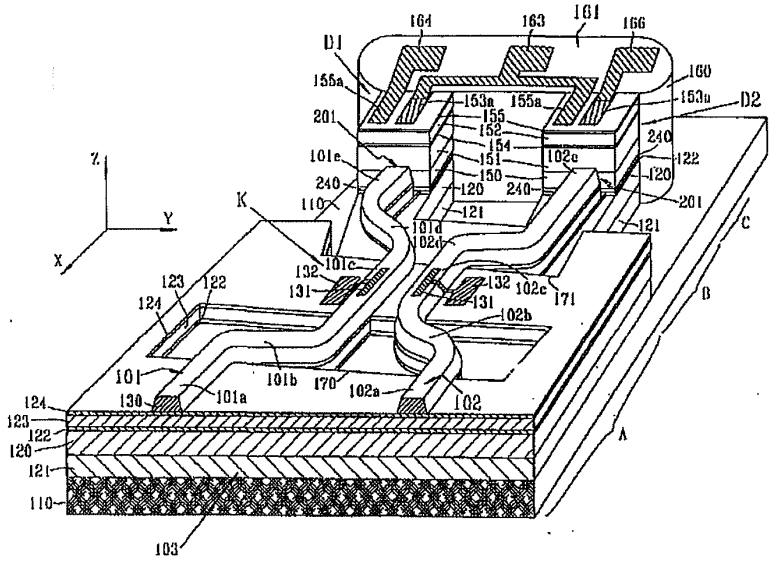


【図２】

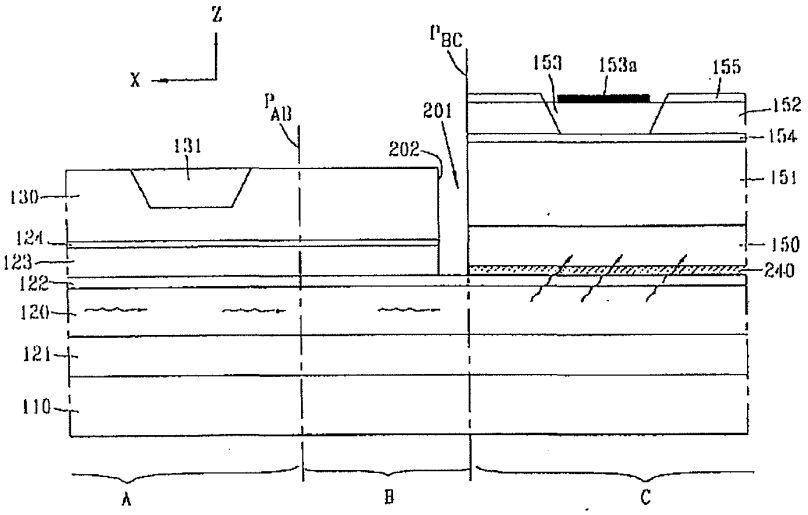


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【図3】



【図4】



フロントページの続き

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H01S 3/18				
		7630－4M	H01L 31/02	B

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No documents available for this priority number.

Espacenet

Bibliographic data: JP2008187003 (A) — 2008-08-14

INFRARED RADIATION DETECTOR

Inventor(s):	MATSUKURA YUSUKE ± (MATSUKURA YUSUKE)
Applicant(s):	FUJITSU LTD ± (FUJITSU LTD)
Classification:	**- international:*H01L31/0264*** **- cooperative: B82Y20/00; H01L31/035218; H01L31/035236; H01L31/109; H01L31/1844**
Application number:	JP20070019117 20070130
Priority number (s):	JP20070019117 20070130
Also published as:	JP4749351 (B2) US2010289061 (A1) US8368045 (B2)

Abstract of JP2008187003 (A)

PROBLEM TO BE SOLVED: To provide a quantum dot type infrared radiation detector using quantum dot in an infrared radiation sensitive part, which hardly lowers sensitivity in a low current region and is excellent in sensitivity characteristics. SOLUTION: The detector has: a contact layer 12 formed on a semiconductor substrate 10; a quantum dot layer 24 which is formed on the contact layer 12 and is formed by alternately and repeatedly laminating an interlayer and a quantum dot; and a contact layer 26 formed on the quantum dot layer 24. The interlayer in contact with the contact layer among a plurality of interlayers, has an impurity introduction region 16 wherein N-type impurities are introduced to an interface side between it and the contact layer 12. ; COPYRIGHT: (C)2008,JPO&INPIT

Last updated: 13.03.2013 Worldwide Database 5.8.6.7; 92p

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(P2008-187003A)
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(51)Int.Cl.	F I		テーマコード（参考）
H01L 31/0264 (2006.01)	H01L 31/08	N	5F088

審査請求 未請求　請求項の数 8　OL　（全 14 頁）

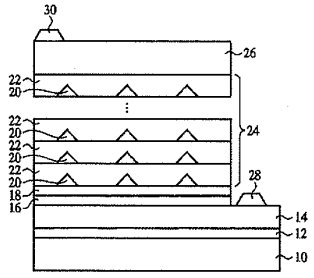
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(22)出願日　平成19年1月30日(2007.1.30)

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Ｆターム(参考)　5F088 AA11　AB07　BA01　BA15　CB01　LA01

(54)【発明の名称】赤外線検出器

(57)【要約】
【課題】赤外感知部分に量子ドットを用いた量子ドット型赤外線検知器に関し、低電流領域における感度低下が少なく感度特性の良好な赤外線検出器を提供する。
【解決手段】半導体基板１０上に形成されたコンタクト層１２と、コンタクト層１２上に形成され、中間層と量子ドットとが交互に繰り返して積層されてなる量子ドット層２４と、量子ドット層２４上に形成されたコンタクト層２６とを有し、複数の中間層のうちコンタクト層に接する中間層は、コンタクト層１２との間の界面側にN型不純物が導入された不純物導入領域１６を有する。
【選択図】図１



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【特許請求の範囲】
【請求項1】
半導体基板上に形成された第１のコンタクト層と、
前記第１のコンタクト層上に形成され、前記第１の半導体材料よりなる複数の中間層と、前記第１の半導体材料よりもバンド幅の狭い第２の半導体材料よりなる複数の量子ドットとが交互に繰り返して積層されてなる量子ドット層と、
前記量子ドット層上に形成された第２のコンタクト層とを有し、
複数の前記中間層のうち前記第１のコンタクト層に接する前記中間層は、前記第１のコンタクト層との間の界面側にＮ型不純物が導入された不純物導入領域を有する
ことを特徴とする赤外線検出器。
【請求項2】
請求項１記載の赤外線検出器において、
前記不純物導入領域は、前記第１のコンタクト層と前記第２のコンタクト層との間に駆動電圧を印加した状態において、前記不純物導入領域による電位降下量をV_1、前記中間層内におけるΓ伝導体とΓ伝導体に近接する他の伝導帯とのエネルギー差をE_0として、
$$V_1 < E_0$$
の関係を満たすように、厚さ及び不純物濃度が規定されている
ことを特徴とする赤外線検出器。
【請求項3】
請求項１記載の赤外線検出器において、
前記不純物導入領域は、前記第１のコンタクト層と前記第２のコンタクト層との間に駆動電圧を印加した状態において、電荷素量をｅ、前記不純物導入領域の不純物濃度をN_d、前記中間層の誘電率をε、前記不純物導入領域の厚さをｔ、前記第１のコンタクト層と前記第２のコンタクト層との間隔をＬ、前記駆動電圧をV_0、前記中間層内におけるΓ伝導体とΓ伝導体に近接する他の伝導帯とのエネルギー差をE_0として、
$$(1/2)(eN_d/\varepsilon)t^2+(t/L)V_0<E_0$$
の関係を満たすように、厚さｔ及び不純物濃度N_dが規定されている
ことを特徴とする赤外線検出器。
【請求項4】
請求項１乃至３のいずれか１項に記載の赤外線検出器において、
前記不純物導入領域は、前記第１のコンタクト層と前記第２のコンタクト層との間に駆動電圧を印加した状態において、前記駆動電圧をV_0、前記不純物導入領域による電位降下量をV_1、前記中間層の厚さを１、前記第１のコンタクト層と前記第２のコンタクト層との間隔をＬ、前記不純物導入領域の厚さをｔ、前記中間層内におけるΓ伝導体とΓ伝導体に近接する他の伝導帯とのエネルギー差をE_0として、
$$((V_0-V_1)l)/(L-t)<E_0$$
の関係を満たすように、厚さ及び不純物濃度が規定されている
ことを特徴とする赤外線検出器。
【請求項5】
請求項１乃至３のいずれか１項に記載の赤外線検出器において、
前記不純物導入領域は、前記第１のコンタクト層と前記第２のコンタクト層との間に駆動電圧を印加した状態において、前記駆動電圧をV_0、前記第１のコンタクト層と前記第２のコンタクト層との間隔をＬ、前記不純物導入領域の厚さをｔ、前記中間層内におけるΓ伝導体とΓ伝導体に近接する他の伝導帯とのエネルギー差をE_0、電荷素量をｅ、前記不純物導入領域の不純物濃度をN_d、前記中間層の誘電率をεとして、
$$V_0-((L-t)/l)E_0<(1/2)(eN_d/\varepsilon)t^2+(t/L)V_0$$
の関係を満たすように、厚さｔ及び不純物濃度N_dが規定されている
ことを特徴とする赤外線検出器。
【請求項6】

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請求項３乃至５のいずれか１項に記載の赤外線検出器において、
前記Γ伝導体に近接する他の伝導帯は、Ｘ伝導帯又はＬ伝導帯である
ことを特徴とする赤外線検出器。
【請求項7】
請求項１乃至６のいずれか１項に記載の赤外線検出器において、
前記第１の半導体材料は、ＧａＡｓ又はＡｌＧａＡｓであり、
ことを特徴とする赤外線検出器。
【請求項8】
請求項１乃至７のいずれか１項に記載の赤外線検出器において、
前記第２の半導体材料は、ＩｎＡｓ又はＩｎＧａＡｓである
ことを特徴とする赤外線検出器。

【発明の詳細な説明】
【技術分野】
【0001】
本発明は、赤外線検出器に係り、特に、赤外感知部分に量子ドットを用いた量子ドット型赤外線検知器に関する。
【背景技術】
【0002】
赤外線検出器の一つとして、赤外感知部分に量子ドットを用いた量子ドット型赤外線検出器が提案されている。量子ドット型赤外線検出器は、赤外感知部分に量子井戸を用いた量子井戸型赤外線検出器と比較して、素子面に垂直に入射する赤外光に対する検出感度が高い、光励起されたキャリアが再び捕獲される確率が少なく光電流利得が高い、などの利点を有している。このため、大きな光電流、つまり感度が得られる赤外線検出器として期待されている。
【0003】
光電流が大きい検出器では、比較的高い動作温度でも雑音源となる暗電流（動作温度に対して指数関数的に増大する）に埋もれずに信号電流を検出できるため、暗電流抑制のために検出器を冷却する必要が少なくなる。したがって、冷却装置を簡素化することができ、赤外線検出器の小型化並びに低コスト化を図ることが可能となる。
【0004】
なお、量子ドット型赤外線検出器は、例えば特許文献１や非特許文献１に記載されている。
【特許文献1】特開平１０－２５６５８８号公報
【非特許文献1】V. Ryzhii, "The theory of quantum-dot infrared photodiodes", Semicond. Sci. Technol., Vol. 11, 1996, p.759
【非特許文献2】I. Vurgaftman et al., "Band parameters for III-V compound semiconductors and their alloys", Journal of Applied Physics, Vol. 89, No. 11, 2001, pp. 5815-5875
【発明の開示】
【発明が解決しようとする課題】
【0005】
提案されている量子ドット型赤外線検出器としては、量子ドットとしてＩｎＡｓを、量子ドットを埋め込む中間層並びに電極層としてＧａＡｓを用いたものが知られている。しかしながら、このような量子ドット型赤外線検出器を実際に作製すると、期待されるほどの感度が得られなかった。
【0006】
赤外線検出器としての動作を決める量子ドット内での量子閉じ込めは、量子ドットの材料であるＩｎＡｓと、その周りを取り囲んで量子ドットを埋め込んでいるＧａＡｓ中間層との間の電位障壁高さで決まる。期待されるよりも感度が低いことは、この量子閉じ込めのための電位障壁高さが不十分であることが、その一つの原因であると考えられる。した

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がって、量子ドット型赤外線検出器の感度を向上するためには、ＧａＡｓ中間層よりもバンド幅の大きな材料、例えばＡｌＧａＡｓ中間層を用いることが有効であると考えられる。

【0007】

しかしながら、このような構造にすることによって確かに全体的には感度が向上するのであるが、信号雑音特性のよい低電流領域での感度改善が相対的に劣化することが判明した。

【0008】

図１０は量子ドット型赤外線検出器の動作電圧を変えたときの感度と暗電流との関係を模式的に示した図である。図中、点線が中間層としてＧａＡｓを用いた場合、実線が中間層としてＡｌＧａＡｓを用いた場合である。

【0009】

中間層としてＧａＡｓよりもバンド幅の大きなＡｌＧａＡｓを用いた場合、ＧａＡｓ中間層を用いた場合の特性と同様の傾きを有する特性（図中、破線で示す）が期待される。しかしながら、実際に作製した素子では、実線で示すように、低電流領域において相対的に感度が低下してしまう。赤外線検出器は、良い信号雑音特性を得るために、このような低い電流領域を用いることが多いため、この領域での感度の相対的な低下は重大な問題である。

【0010】

本発明の目的は、赤外感知部分に量子ドットを用いた量子ドット型赤外線検知器に関し、低電流領域における感度低下が少なく感度特性の良好な赤外線検出器を提供することにある。

【課題を解決するための手段】

【0011】

本発明の一観点によれば、半導体基板上に形成された第１のコンタクト層と、前記第１のコンタクト層上に形成され、前記第１の半導体材料よりなる複数の中間層と、前記第１の半導体材料よりもバンド幅の狭い第２の半導体材料よりなる複数の量子ドットとが交互に繰り返して積層されてなる量子ドット層と、前記量子ドット層上に形成された第２のコンタクト層とを有し、複数の前記中間層のうち前記第１のコンタクト層に接する前記中間層は、前記第１のコンタクト層との間の界面側にＮ型不純物が導入された不純物導入領域を有する赤外線検出器が提供される。

【発明の効果】

【0012】

本発明によれば、赤外感知部分に量子ドットを用いた量子ドット型赤外線検知器において、量子ドットを埋め込む中間層と電極層との間に、電極層側からの電子の注入を促進し、電子がΓ伝導体以外の伝導帯に散乱されるのを抑制するための不純物導入層を形成するので、中間層としてＡｌＧａＡｓのようなバンド幅の広い材料を用いて量子閉じ込め効果を向上した場合にも、低電流領域における相対的な感度の低下を抑制することができる。これにより、赤外線検出器の感度特性を改善することができる。

【発明を実施するための最良の形態】

【0013】

本発明の一実施形態による赤外線検出器及びその製造方法について図１乃至図９を用いて説明する。

【0014】

図１は本実施形態による赤外線検出器の構造を示す概略断面図、図２はＡｌＧａＡｓにおけるΓ帯からのエネルギー高さ及びＧａＡｓに対する電位障壁高さのＡｌ組成に対する依存性を示すグラフ、図３は中間層としてＧａＡｓ又はＡｌ組成の低いＡｌＧａＡｓを用いた赤外線検出器の動作状態を模式的に表すエネルギーバンド図、図４は中間層が感度改善に必要なだけの高いＡｌ組成のＡｌＧａＡｓを用いた赤外線検出器の動作状態を模式的に表すエネルギーバンド図、図５は本実施形態による赤外線検出器の原理を示すエネルギ

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ーバンド図、図６は不純物導入層の最適化のための検討に用いたエネルギーバンド構造のモデルを示す図、図７は本実施形態による赤外線検出器の評価結果を示すグラフ、図８及び図９は本実施形態による赤外線検出器の製造方法を示す工程断面図である。

【0015】

はじめに、本実施形態による赤外線検出器の構造について図１乃至図７を用いて説明する。

【0016】

ＧａＡｓよりなる半導体基板１０上には、例えば膜厚１００ｎｍのＧａＡｓ層よりなる緩衝層１２が形成されている。緩衝層１２上には、例えば膜厚５００ｎｍのＧａＡｓ層よりなる下部コンタクト層１４（第1のコンタクト層）が形成されている。

【0017】

下部コンタクト層１４上には、例えば膜厚１０ｎｍのＡｌＧａＡｓ層よりなる不純物導入層１６（不純物導入領域）が形成されている。不純物導入層１６には、N型の導電型を示す不純物が導入されている。不純物として例えばシリコンを用いる場合、III族元素のサイトにシリコンが入ることで、N型となる。不純物導入層１６上には、例えば膜厚４０ｎｍのＡｌＧａＡｓ層よりなる下地層１８が形成されている。なお、本実施形態では、便宜上、不純物導入層１６と下地層１８とを区別しているが、不純物導入層１６は、下地層１８の一部分の、不純物が導入された領域と考えることができる。

【0018】

下地層１８上には、量子ドット積層体２４が形成されている。量子ドット積層体２４（量子ドット層）は、ＩｎＡｓよりなる量子ドット２０と、例えば膜厚５０ｎｍのＡｌＧａＡｓよりなる中間層２２とを繰り返し（例えば１０回）積層することにより構成されている。なお、本実施形態では、便宜上、下地層１８と量子ドット積層体２４とを区別しているが、下地層１８は中間層２２と同じく量子ドット２０を埋め込み障壁層として機能するものであり、機能的には、中間層の一部分、すなわち量子ドット積層体２４の一部分でもある。かかる観点から、本願明細書では、不純物導入層１６及び下地層１８を、中間層と呼ぶこともある。

【0019】

量子ドット積層体２４上には、例えば膜厚１５０ｎｍのＧａＡｓ層よりなる上部コンタクト層２６（第2のコンタクト層）が形成されている。下部コンタクト層１４の一部の領域上は、上部コンタクト層２６、量子ドット積層体２４、下地層１８及び不純物導入層１６が除去されており、この領域の下部コンタクト層１４上に、下部電極層２８が形成されている。上部コンタクト層２６上には、上部電極層３０が形成されている。

【0020】

このように、本実施形態による赤外線検出器は、量子ドットがＩｎＡｓにより構成され、量子ドットを埋め込む中間層がＡｌＧａＡｓにより構成された量子ドット型赤外線検出器において、下部コンタクト層１４と下地層１８との間に、不純物導入層１６が形成されていることに主たる特徴がある。

【0021】

以下に、下部コンタクト層１４と下地層１８との間に不純物導入層１６を形成する理由及び効果について説明する。

【0022】

上述のように、量子ドットとしてＩｎＡｓを用いた赤外線検出器において、中間層をＧａＡｓからＡｌＧａＡｓに変更すると、低電流領域における感度が相対的に低下する。本願発明者が鋭意検討を行った結果、感度が低下する原因は、中間層の材料変更に伴う本質的な現象であることを突き止めた。

【0023】

一般的な半導体デバイスでは、考察する電子のエネルギーが比較的低いため、半導体中の伝導帯として、通常はいわゆるΓ伝導帯（Γ帯）のみを考える。しかしながら、実際には、よりエネルギー的に高い領域に、Ｌ帯やX帯と呼ばれる伝導帯が存在する。

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【0024】
図２は、Ｘ帯及びＬ帯の、Γ帯からのエネルギー高さ及びＧａＡｓに対する電位障壁高さについての、ＡｌＧａＡｓ中のＡｌ組成に対する依存性を示すグラフである。なお、計算に用いた物性定数は、非特許文献２に記載されたものを用いた。ＧａＡｓに対する障壁高さは、バンド幅の差に対して伝導帯側の寄与がその６０％であるとしている。また、素子温度は、７７Ｋを仮定した。
【0025】
図２から判るように、ＡｌＧａＡｓ中間層でのＡｌ組成を増加させることにより、Γ帯で形成されるＧａＡｓに対する電位障壁高さは増加するが、Γ帯からみたＸ帯及びＬ帯のエネルギー高さは減少している。このため、Ａｌ組成が高いＡｌＧａＡｓ中間層を用いる場合、Ｘ帯及びＬ帯の影響も無視できなくなる。
【0026】
図３及び図４は、このような場合の素子動作について模式的に表したエネルギーバンド図である。図３は中間層がＧａＡｓ又はＡｌ組成の低いＡｌＧａＡｓの場合であり、図４は中間層が感度改善に必要なだけの高いＡｌ組成のＡｌＧａＡｓの場合である。
【0027】
なお、図３及び図４では、量子ドット部分でのＸ帯及びＬ帯と、中間層部分でのＸ帯及びＬ帯との間におけるエネルギーの差違を省略している。これは、そもそも量子ドット赤外線検出器としての伝導帯の電位分布は、Γ帯を基準として設計がなされるものであり、Ｘ帯及びＬ帯において電子がどのように伝導しようとも、Γ帯に電子が戻ってこない限り、ここでの議論には本質的ではないことによる。
【0028】
図３に示すように、中間層がＧａＡｓ又は比較的低いＡｌ組成のＡｌＧａＡｓの場合、Γ帯に対してＸ帯或いはＬ帯の伝導帯はエネルギー的に十分に高い位置にあるため、電極層（図面、左側）から注入された電子は、概ねΓ帯にとどまって素子内を伝導していくため、量子ドット層内に捕獲されやすい。
【0029】
これに対し、中間層が、感度改善に必要なだけの高いＡｌ組成のＡｌＧａＡｓの場合、図４に示すように、Ｘ帯又はＬ帯の伝導帯がエネルギー的にΓ帯に近づくため、電極層（図面、左側）から注入された電子の一定部分が、Ｘ帯又はＬ帯の伝導帯に散乱される。したがって、主にΓ帯で設計されている量子ドット部分に捕獲されにくくなり、感度が低下する。
【0030】
更に、中間層をＡｌＧａＡｓのような障壁の高い材料とした場合、電極層から電子が注入されるためにはより高いエネルギーを必要とする。その結果、同じ暗電流値で比較した場合、中間層をバンド幅の大きな材料とした素子では、より高い電圧を印加する必要が生じる。このことは、電子がＸ帯又はＬ帯に散乱されるのに必要なエネルギーを得ることを更に促進し、ひいては感度の相対的な低下を促進してしまう。
【0031】
ところで、そもそもバンド幅の大きな中間層を導入する目的は、量子ドットにおける量子閉じ込め効果の強調によって感度を増加させることにある。したがって、上述の感度劣化の問題は、中間層の電位障壁を高いまま維持しつつ、電極層と中間層との間における電子の注入を促進することで、解決することができる。
【0032】
そこで、本実施形態による赤外線検出器では、下部コンタクト層１４と下地層１８との間に、ＡｌＧａＡｓ不純物導入層１６を設けている。ＧａＡｓ下部コンタクト層１４と下地層１８との間の所定領域に所定濃度の不純物導入層１６を設けることにより、不純物導入層１６が形成された領域での電位分布を変化することができ、下部コンタクト層１４側からの電子の注入を促進することができる。
【0033】

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中間層を電極層（コンタクト層）に比較してバンド幅の大きな材料とした場合、中間層の電極層に接した近傍の領域に不純物を導入すると、イオン化したその不純物による空間電荷によって電位分布が曲がる。例えば図１に示すように、下部コンタクト層１４と下地層１８との間にＮ型不純物が導入された不純物導入層１６を設けると、不純物導入層１６中のイオン化した不純物による空間電荷により、不純物導入層１６内の伝導帯のエネルギーが低エネルギー側にシフトする（図５参照）。

【0034】

これにより、不純物導入層１６が形成された領域の電位障壁が実効的に薄くなり、トンネル電流が生じやすくなる。この結果、一定の素子印加電圧での素子電流が増加する。また、下部コンタクト層１４側から注入された電子は、不純物導入層１６の電位障壁の上を超えることなくトンネリングによって流れることが可能となり、電子がＸ帯又はＬ帯に散乱されるほどのエネルギーを得ることを防止することが可能となる。

【0035】

次に、このような効果を奏する不純物導入層１６に好適な不純物濃度Ｎｄ及び厚さｔについて検討する。この検討にあたり、図６に示すようなエネルギーバンド構造のモデルを考える。図中、Ｌは電極部分（コンタクト層）に挟まれた活性領域の厚さ（素子長）であり、１は量子ドットの１周期に相当する距離である。

【0036】

体積密度N_dの空間電荷を持つ領域の電位分布Ｖは、ｅを電荷素量、εをその領域の誘電率として、下記のポアソン方程式で記述される。

【0037】

$$d^2V/dx^2 = eN_d/\varepsilon$$

素子に印加する電圧をV_0としたとき、下部コンタクト層１４と不純物導入層１６との間の電位障壁の頂点（図中、Ａ点）からみた不純物導入層１６の端部との電位差V_1（図６参照）は、ポアソン方程式を解くことにより、

$$V_1 = (1/2)(eN_d/\varepsilon)t^2 + (t/L)V_0$$

と求めることができる。なお、ここでは、$V_1 \ll V_0$とした近似を用いている。

【0038】

したがって、この電位差V_1が、Γ帯とＸ帯とのエネルギー差（図中、ΔEg_X）及びΓ帯とＬ帯とのエネルギー差（図中、ΔEg_L）のうち低い方（これをエネルギー差E_0とする）よりも小さければ、少なくとも、図６のＡ点から注入された電子がそのままＸ帯又はＬ帯に注入されてしまうことを抑制することができる。したがって、下記の式（１）は、不純物導入層１６に導入すべき不純物の濃度N_d及びその領域幅ｔの上限値を与える。

【0039】

$$(1/2)(eN_d/\varepsilon)t^2 + (t/L)V_0 < E_0 \quad \cdots(1)$$

なお、式（１）の左辺第１項は、一様な空間電荷状態での電位分布を示すものであり、ｘ＝ｔでの電位と電界＝０という境界条件によりポアソン方程式から求められるものである。この境界条件が、上述の$V_1 \ll V_0$とする近似に該当する。また、式（１）の左辺第２項は、この近似に対する補正項であり、ｘ＝０からｘ＝ｔでの間でのバイアス電圧V_0による電位変化分（線形近似）を考慮したものである。

【0040】

式（１）を満たす不純物導入層１６を設けることによって、低電圧での暗電流を確保しつつ、下部コンタクト層１４側から注入される電子がＸ帯又はＬ帯に散乱されてしまい量子ドット型赤外線検出器の感度に寄与しなくなることを抑制することが可能となる。

【0041】

ところで、通常このような量子ドット型赤外線検出器では、十分な量子効率を得るために、複数の量子ドット層を、中間層を介して積層した構造を用いることが多い。図１に示す本実施形態による赤外線検出器も同様である。この場合、素子内に存在する電子が、素子内の内部電界によって加速され、十分なエネルギーを得ると、やはりＸ帯やＬ帯に散乱

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され、より下流の量子ドットに捕獲されにくくなる。

【0042】

活性領域を流れる電子は、いわゆる濡れ層などの影響により、このような量子ドット積層構造（量子ドット積層体２４）の１周期相当以上の距離を、何らの散乱もされずに伝達することは考え難い。したがって、電子が量子ドット積層体２４の１周期分の距離１を流れる間に得るエネルギーの最大値が、やはりエネルギー差E_0を超えないように素子内電位分布を設計すれば、本発明の効果はより十分に発揮できる。

【0043】

不純物導入層１６により、電位差V_1分の電位効果が生じる。したがって、不純物導入層１６は、素子内部での電界を電位差V_1相当分だけ低減する効果も持つ。このとき、電子が量子ドット積層体２４の１周期相当の距離を加速されることによって得るエネルギーの最大値V_2は、

$$V_2=((V_0-V_1)/(L-t))\times l$$

であるから、

$$V_0-((L-t)/l)E_0<(1/2)(eN_d/\varepsilon)t^2+(t/L)V_0 \quad \cdots(2)$$

を満たすことが、より望ましい。上記式（２）は、ＡｌＧａＡｓ不純物導入層１６に導入すべき不純物の濃度N_d及びその領域幅ｔの上限値を与える。

【0044】

なお、$(V_0-V_1)/(L-t)$は、不純物導入部分以外のところでの電圧V_0による電界（一様電界と近似）であり、その電界中での距離１離れた２点間の電位差（V_2）が、電界×距離＝$(V_0-V_1)/(L-t)\times l$であることを表している。

【0045】

以上の結果から、不純物導入層１６の不純物濃度N_d及び厚さｔは、素子に印加する電圧をV_0、電極部分に挟まれた活性領域の厚さをＬ、中間層の厚さの最小値を１、中間層におけるΓ伝導体とΓ伝導体以外の伝導帯とのエネルギー差のうちの最小値をE_0、電荷素量をｅ、中間層の誘電率をεとして、下記2式のうち少なくとも一方の関係を満たすように、適宜設定することが望ましい。

【0046】

$$(1/2)(eN_d/\varepsilon)t^2+(t/L)V_0<E_0$$

$$V_0-((L-t)/l)E_0<(1/2)(eN_d/\varepsilon)t^2+(t/L)V_0$$

本実施形態による赤外線検出器では、素子長Ｌが５００ｎｍ、量子ドット２０の１周期相当の距離（中間層２２の厚さ）が５０ｎｍ、不純物導入層１６の厚さｔが１０ｎｍ、不純物導入層１６の不純物濃度N_dが$8.5\times10^{17}cm^{-3}$、ＡｌＧａＡｓ層のＡｌ組成が１５％では、中間層２２の比誘電率が１２．７、Γ伝導帯とＸ伝導帯又はＬ伝導帯との間のエネルギー差E_0が１６３ｍＶであるため、素子に印加する電圧V_0を１Ｖとすると、

$$V_1=(1/2)(eN_d/\varepsilon)t^2+(t/L)V_0=78.8mV$$

となり、上記式（１）の関係を満たしている。また、

$$V2=V_0-((L-t)/l)\times E_0=-628mV$$

となり、上記式（２）の関係も満たしている。

【0047】

図７に、本実施形態による赤外線検出器を実際に作製して評価した結果を示す。図中、○印は不純物導入層１６を形成していない従来構造の試料、●印は不純物導入層１６を形成した本発明の試料である。なお、赤外線検出器の素子サイズは５００μｍ角とし、測定温度は８０Ｋとした。

【0048】

図７中に点線の○印で示した動作点は、$V_0=2.2V$である。この場合、電位差V_1，V_2は、それぞれ、

$$V_1=(1/2)(eN_d/\varepsilon)t^2+(t/L)V_0=105mV$$

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$V2=V_0-((L-t)/l)\times E_0=572mV$

となり、式（１）の関係は満たすが、式（２）の関係は満たしていない。しかしながら、図7から明らかなように、不純物導入層１６を形成した本発明の試料では、不純物導入層１６を形成しない従来構造の試料と比較して、低電流領域での相対的な感度の低下を抑制できていることが判る。

【0049】

上記式（１）の関係及び式（２）の関係は、必ずしも双方ともに満たす必要はなく、少なくとも一方の関係を満たすように不純物導入層１６を設計することにより、本発明の効果を得ることができる。

【0050】

次に、本実施形態による赤外線検出器の製造方法について図８及び図９を用いて説明する。

【0051】

まず、ＧａＡｓ基板１０上に、周知の結晶成長技術、例えば分子線エピタキシー法により、ＧａＡｓ緩衝層１２を成長する。ＧａＡｓ緩衝層１２の膜厚は、素子構造設計によって異なるが、例えば１００ｎｍとする。

【0052】

次いで、ＧａＡｓ緩衝層１２上に、周知の結晶成長技術、例えば分子線エピタキシー法により、ＧａＡｓ下部コンタクト層１４を成長する（図８（ａ））。ＧａＡｓ下部コンタクト層１４の膜厚は、素子構造設計によって異なるが、例えば５００ｎｍとする。ＧａＡｓ下部コンタクト層１４へのドーピングは、不純物として例えばＳｉを用い、濃度を例えば$1\times10^{18}cm^{-3}$とする。

【0053】

次いで、ＧａＡｓ下部コンタクト層１４上に、周知の結晶成長技術、例えば分子線エピタキシー法により、例えば５８０℃の基板温度で、ＡｌＧａＡｓ不純物導入層１６を成長する（図８（ｂ））。ＡｌＧａＡｓ不純物導入層１６の膜厚は、目的とする量子ドット型赤外線検出器の特性によって異なるが、例えば１０ｎｍとする。また、ＡｌＧａＡｓ不純物導入層１６へのドーピングは、目的とする量子ドット型赤外線検出器の特性によって異なるが、不純物として例えばＳｉを用い、濃度を例えば$8.5\times10^{17}cm^{-3}$とする。また、ＡｌＧａＡｓ不純物導入層１６の組成は、目的とする量子ドット型赤外線検出器の特性によって異なるが、Ａｌ組成を例えば１５％とする。

【0054】

次いで、ＡｌＧａＡｓ不純物導入層１６上に、周知の結晶成長技術、例えば分子線エピタキシー法により、例えば５８０℃の基板温度で、ＡｌＧａＡｓ下地層１８を成長する。ＡｌＧａＡｓ下地層１８の膜厚は、目的とする量子ドット型赤外線検出器の特性によって異なるが、例えば４０ｎｍとする。また、ＡｌＧａＡｓ下地層１８の組成は、目的とする量子ドット型赤外線検出器の特性によって異なるが、Ａｌ組成を例えば１５％とする。

【0055】

次いで、ＡｌＧａＡｓ下地層１８上に、周知の結晶成長技術、例えば分子線エピタキシー法を用いた自己組織化成長により、ＩｎＡｓ量子ドット２０を成長する。ＩｎＡｓ量子ドット２０は、例えば４７０℃の基板温度にて、総供給量が例えば２．３分子層相当の原料を、例えば０．２分子層毎秒の速度で供給することにより、成長する。この条件で成長したＩｎＡｓ量子ドット２０の形状は、同じ成長条件の試料を評価したところ、高さが１．４ｎｍ、横幅が１６ｎｍであった。

【0056】

次いで、ＩｎＡｌ量子ドット２０が形成されたＡｌＧａＡｓ下地層１８上に、周知の結晶成長技術、例えば分子線エピタキシー法により、例えば５８０℃の基板温度で、ＡｌＧａＡｓ中間層２２を成長する（図８（ｃ））。ＡｌＧａＡｓ中間層２２の膜厚は、目的とする量子ドット型赤外線検出器の特性によって異なるが、例えば５０ｎｍとする。また、ＡｌＧａＡｓ中間層２２の組成は、目的とする量子ドット型赤外線検出器の特性によって

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異なるが、Ａｌ組成を例えば１５％とする。

【0057】

次いで、ＡｌＧａＡｓ中間層２２上に、上記の手順と同様にして、ＩｎＡｓ量子ドット２０とＡｌＧａＡｓ中間層２２とを、所望の回数、例えば１０回繰り返して成長し、ＩｎＡｓ量子ドット２０とＡｌＧａＡｓ中間層２２とが繰り返し積層されてなる量子ドット積層体２４を形成する。

【0058】

次いで、量子ドット積層体２４上に、周知の結晶成長技術、例えば分子線エピタキシー法により、ＧａＡｓ上部コンタクト層２６を成長する（図９（ａ））。ＧａＡｓ上部コンタクト層２６の膜厚は、素子構造設計によって異なるが、例えば１５０ｎｍとする。ＧａＡｓ上部コンタクト層２６へのドーピングは、不純物として例えばＳｉを用い、濃度を例えば$1\times10^{18}\ cm^{-3}$とする。

【0059】

次いで、フォトリソグラフィ及びドライエッチングにより、下部電極の形成予定領域のＧａＡｓ上部コンタクト層２６、量子ドット積層体２４、ＡｌＧａＡｓ下地層１８及びＡｌＧａＡｓ不純物導入層１６を除去し、ＧａＡｓ下部コンタクト層１４の表面を露出する。

【0060】

次いで、例えば蒸着法やスパッタ法等により、露出したＧａＡｓ下部コンタクト層１４条及びＧａＡｓ上部コンタクト層２６上に、それぞれ下部電極層２８及び上部電極層３０を形成し、本実施形態による赤外線検出器を完成する（図９（ｂ））。

【0061】

このように、本実施形態によれば、下部コンタクト層１４と下地層（中間層）１８との間に、下部コンタクト層１４側からの電子の注入を促進し、電子がΓ伝導体以外の伝導帯に散乱されるのを抑制するための不純物導入層１６を形成するので、中間層としてＡｌＧａＡｓのようなバンド幅の広い材料を用いて量子閉じ込め効果を向上した場合にも、低電流領域における相対的な感度の低下を抑制することができる。これにより、赤外線検出器の感度特性を改善することができる。

【0062】

［変形実施形態］

本発明は上記実施形態に限らず種々の変形が可能である。

【0063】

例えば、上記実施形態では、赤外線検出器の製造に分子線エピタキシー法を用いた場合を例にして説明したが、赤外線検出器の製造には量子ドットの形成が可能な他の結晶成長法を用いることも可能である。このような結晶成長法としては、例えば有機金属気相成長法が挙げられる。

【0064】

また、上記実施形態では、ＩｎＡｓよりなる量子ドットとＡｌＧａＡｓよりなる量子ドット埋め込み層との組み合わせにより構成した量子ドット型赤外線検出器を示したが、量子ドットの材料と量子ドット埋め込み層の材料との組み合わせは、上記実施例に限定されるものではない。例えば、量子ドットとしては、ＩｎＡｓ、ＩｎＧａＡｓ、ＧａＮ、ＩｎＮ、ＧａＡｓ等の材料を適用することができ、量子ドット埋め込み層としては、ＡｌＧａＡｓ、ＩｎＧａＰ、ＩｎＰ、ＩｎＡｌＡｓ等の材料を適用することができる。

【0065】

量子ドット／量子ドット埋め込み層の具体的な組み合わせ例としては、ＩｎＡｓ／ＧａＡｓ、ＩｎＧａＡｓ／ＧａＡｓ、ＩｎＡｓ／ＡｌＧａＡｓ、ＩｎＡｓ／ＩｎＧａＰ、ＩｎＧａＡｓ／ＩｎＧａＰ、ＩｎＡｓ／ＩｎＰ、ＩｎＧａＡｓ／ＩｎＰ、ＩｎＡｓ／ＩｎＡｌＡｓ、ＩｎＧａＡｓ／ＩｎＡｌＡｓ、ＩｎＡｓ／ＡｌＧａＮ、ＧａＡｓ／ＡｌＧａＮ、ＩｎＮ／ＡｌＧａＮ、ＧａＮ／ＡｌＧａＮ等が挙げられる。

【0066】

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また、上記実施形態では、活性領域内で電子がＸ伝導帯又はＬ伝導帯に散乱される場合を例にして説明したが、Γ伝導体に近接する他の伝導帯に電子が散乱される場合についても本発明を適用することができる。

【図面の簡単な説明】

【0067】

【図1】本発明の一実施形態による赤外線検出器の構造を示す概略断面図である。

【図2】ＡｌＧａＡｓにおけるΓ帯からのエネルギー高さ及びＧａＡｓに対する電位障壁高さのＡｌ組成に対する依存性を示すグラフである。

【図3】中間層としてＧａＡｓ又はＡｌ組成の低いＡｌＧａＡｓを用いた赤外線検出器の動作状態を模式的に表すエネルギーバンド図である。

【図4】中間層が感度改善に必要なだけの高いＡｌ組成のＡｌＧａＡｓを用いた赤外線検出器の動作状態を模式的に表すエネルギーバンド図である。

【図5】本発明の一実施形態による赤外線検出器の原理を示すエネルギーバンド図である。

【図6】不純物導入層の最適化のための検討に用いたエネルギーバンド構造のモデルを示す図である。

【図7】本発明の一実施形態による赤外線検出器の評価結果を示すグラフである。

【図8】本発明の一実施形態による赤外線検出器の製造方法を示す工程断面図（その１）である。

【図9】本発明の一実施形態による赤外線検出器の製造方法を示す工程断面図（その２）である。

【図10】量子ドット型赤外線検出器の動作電圧を変えたときの感度と暗電流との関係を模式的に示した図である。

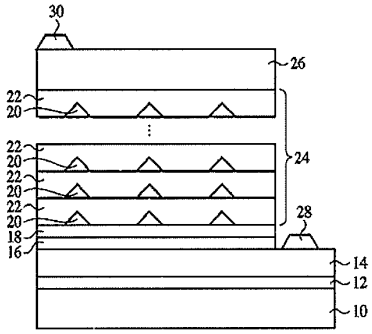
【符号の説明】

【0068】

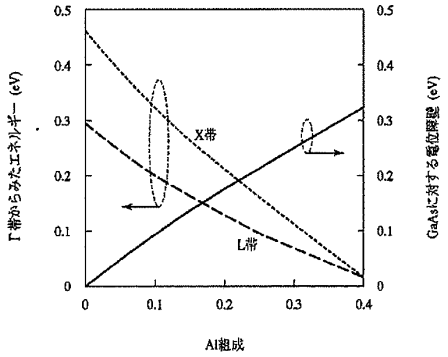
１０…半導体基板
１２…緩衝層
１４…下部コンタクト層
１６…不純物導入層
１８…下地層
２０…量子ドット
２２…中間層
２４…量子ドット積層体
２６…上部コンタクト層
２８…下部電極層
３０…上部電極層

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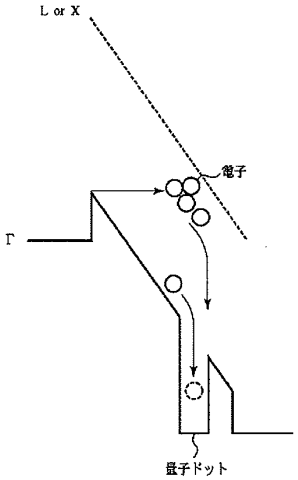
【図1】



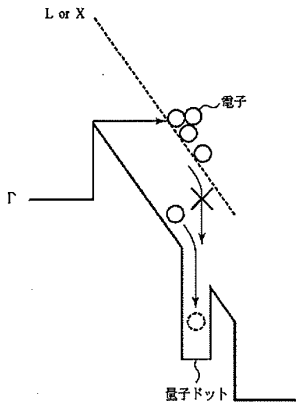
【図2】



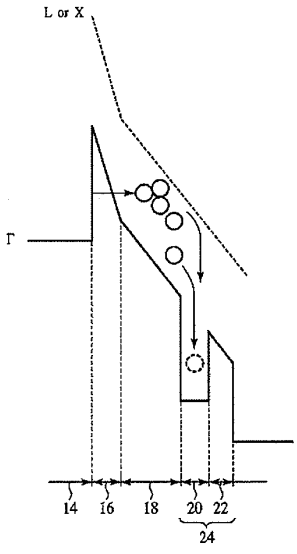
【図3】



【図4】

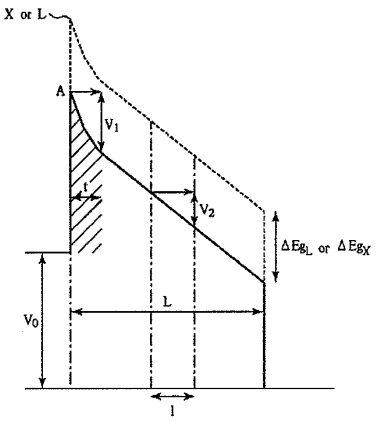


【図5】

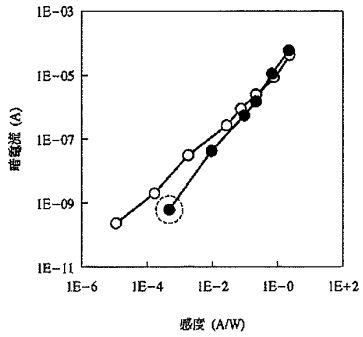


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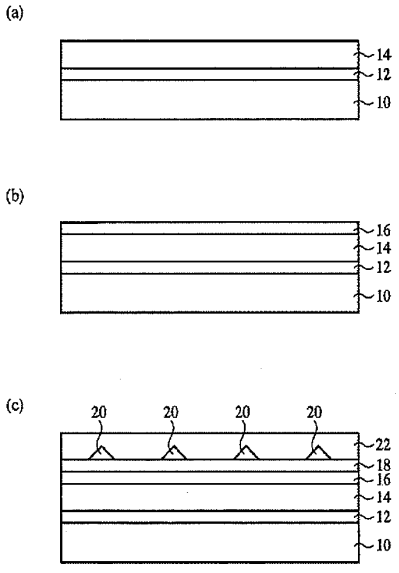
【図6】


X or L
A
V_1
t
V_2
ΔEg_L or ΔEg_X
V_0
L
l

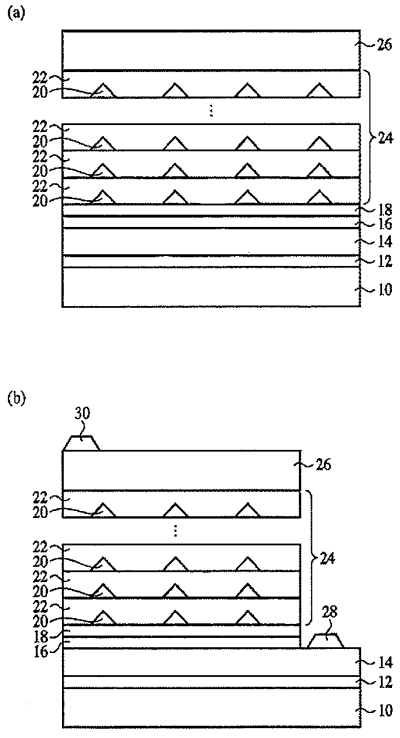
【図7】


1E-03
1E-05
1E-07
1E-09
1E-11
暗電流 (A)
1E-6
1E-4
1E-2
1E-0
1E+2
感度 (A/W)

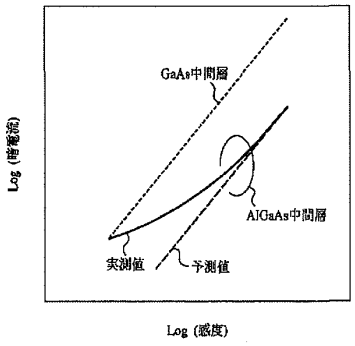
【図8】

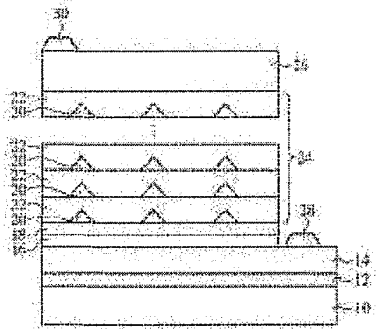

(a)
14
12
10
(b)
16
14
12
10
(c)
20
20
20
20
22
18
16
14
12
10

【図9】


(a)
26
22
20
24
18
16
14
12
10
(b)
30
26
24
28
14
12
10

【図10】





Espacenet

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SOLID-STATE IMAGE PICKUP ELEMENT

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Applicant(s): CANON KK ± (CANON INC)

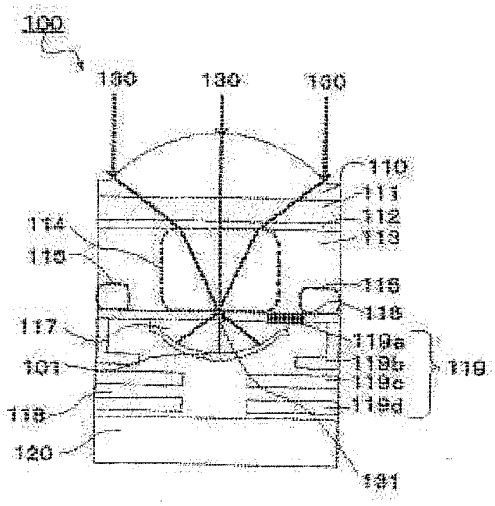
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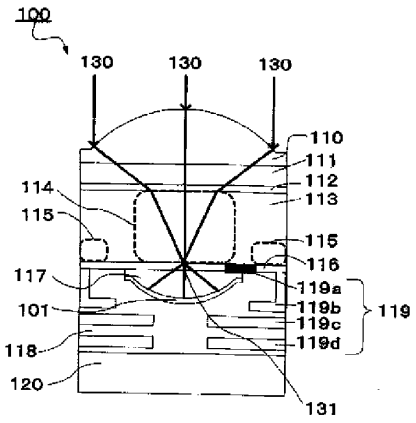
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(54)【発明の名称】固体撮像素子

(57)【要約】
【課題】基板を透過する入射光を光電変換部に反射させる構造の固体撮像素子を構成するに当たり、反射光によるノイズの発生を低減し、光利用効率を向上させることが可能となる固体撮像素子を提供する。
【解決手段】画素ごとに基板内部に形成された光電変換部と、
前記基板に対して入射光が入射する側に設けられ、該入射光を前記光電変換部に集光する集光部と、を有する固体撮像素子であって、
前記基板に対して前記集光部の反対側に設けられ、該基板に向かって凹型形状を有する反射部を有し、
前記反射部は、該反射部の等倍結像位置を前記集光部の集光位置と一致させる構成を備えている。
【選択図】　図１



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【特許請求の範囲】
【請求項１】
画素ごとに基板内部に形成された光電変換部と、
前記基板に対して入射光が入射する側に設けられ、該入射光を前記光電変換部に集光する集光部と、を有する固体撮像素子であって、
前記基板に対して前記集光部の反対側に設けられ、該基板に向かって凹型形状を有する反射部を有し、
前記反射部は、該反射部の等倍結像位置を前記集光部の集光位置と一致させる構成を備えていることを特徴とする固体撮像素子。
【請求項２】
前記反射部は、金属で形成されていることを特徴とする請求項１に記載の固体撮像素子。
【請求項３】
前記固体撮像素子は、前記基板に対して前記集光部と反対側に配線部を有する裏面照射型固体撮像素子であることを特徴とする請求項１または請求項２に記載の固体撮像素子。
【請求項４】
前記等倍結像位置と前記焦点位置は、前記基板における前記反射部を有する側の面上にあることを特徴とする請求項１から３のいずれか１項に記載の固体撮像素子。
【請求項５】
前記配線部は、ゲート電極と複数の配線層によって構成され、
前記反射部は、前記配線層よりも前記基板側に配置されていることを特徴とする請求項１から４のいずれか１項に記載の固体撮像素子。
【請求項６】
前記固体撮像素子が複数配列された該固体撮像素子の周辺画素において、
前記集光部の焦点位置が、前記周辺画素の中心軸に変位するように、
前記集光部を、前記周辺画素の中心軸より前記固体撮像素子の中心画素側に変位させて配されていることを特徴とする請求項１から５のいずれか１項に記載の固体撮像素子。
【請求項７】
前記固体撮像素子が複数配列された該固体撮像素子の周辺画素において、
前記配線層を、前記周辺画素の中心軸より前記固体撮像素子の中心画素側と反対側に変位させて配されていることを特徴とする請求項１から６のいずれか１項に記載の固体撮像素子。
【請求項８】
前記固体撮像素子が複数配列された該固体撮像素子の周辺画素において、
前記ゲート電極が、該周辺画素の中心軸より前記固体撮像素子の中心画素側に変位させて配されていることを特徴とする請求項１から７のいずれか１項に記載の固体撮像素子。
【請求項９】
前記配線層は、前記反射部を形成している金属と同一の材料で形成されていることを特徴とする請求項１から８のいずれか１項に記載の固体撮像素子。
【請求項１０】
前記基板と前記絶縁部の間に反射防止層が形成されていることを特徴とする請求項１から９のいずれか１項に記載の固体撮像素子。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、固体撮像素子に関し、特に、デジタルスチルカメラ等の撮像装置に用いる固体撮像素子に関する。
【背景技術】
【０００２】
近年、ＣＣＤやＣＭＯＳ素子などを２次元状に複数配列した固体撮像素子が、デジタル

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ビデオカメラやデジタルスチルカメラなどで用いられている。
固体撮像素子は、基板にイオン注入などの不純物導入によって光電変換部や拡散層を形成し、その後、膜を堆積・加工することで配線層や絶縁膜を形成して製造される。
固体撮像素子に入射した光は、光電変換部で吸収され、電荷に変換される。この電荷を光電変換部で蓄積し、蓄積した全電荷量の大きさを検出することで、入射光強度に応じた信号を得ることができる。
【０００３】
しかしながら、基板の深さより入射光の侵入長が長いと、入射光は光電変換部で十分吸収されずに、一部が基板を透過する。
そのため、入射光の一部は電荷信号に変換できず、光利用効率が低下する。
このようなことから、特許文献１では、透過した光を再び光電変換部に反射させるようにした撮像装置が提案されている。
但し、ここでの入射光の侵入長とは、光強度が吸収損失により入射光強度の１／ｅ倍になるまでの伝播距離を意味している。
【先行技術文献】
【特許文献】
【０００４】
【特許文献１】特開２００７－０２７６０４号公報
【発明の概要】
【発明が解決しようとする課題】
【０００５】
しかしながら、上記特許文献１の撮像装置における反射膜の構造では、図１０に示すように、マイクロレンズ９１０によって屈折された入射光９３０は反射膜９０１で反射され、隣接画素へ伝播する。
このため、反射光によりクロストークなどのノイズが発生し、画像のＳＮ比を低下させる。
【０００６】
本発明は、上記課題に鑑み、基板を透過する入射光を光電変換部に反射させる構造の固体撮像素子を構成するに当たり、反射光によるノイズの発生を低減し、光利用効率を向上させることが可能となる固体撮像素子の提供を目的とする。
【課題を解決するための手段】
【０００７】
本発明の固体撮像素子では、画素ごとに基板内部に形成された光電変換部と、
前記基板に対して入射光が入射する側に設けられ、該入射光を前記光電変換部に集光する集光部と、を有する固体撮像素子であって、
前記基板に対して前記集光部の反対側に設けられ、該基板に向かって凹型形状を有する反射部を有し、
前記反射部は、該反射部の等倍結像位置を前記集光部の集光位置と一致させる構成を備えていることを特徴としている。
【発明の効果】
【０００８】
本発明によれば、基板を透過する入射光を光電変換部に反射させる構造の固体撮像素子を構成するに当たり、反射光によるノイズの発生を低減し、光利用効率を向上させることが可能となる固体撮像素子を実現することができる。
【図面の簡単な説明】
【０００９】
【図１】本発明の実施例１における裏面照射型のＣＭＯＳ撮像素子の構成例について説明する断面図。
【図２】本発明の実施例１における可視光用の固体撮像素子の数値実施例を説明する図。
【図３】本発明の実施例１における撮像素子の反射部での反射率を示すグラフ。

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【図４】本発明の実施例１における撮像素子の光利用効率を示すグラフ。
【図５】反射部がない場合の固体撮像素子の光利用効率を示すグラフ。
【図６】本発明の実施例２における２次元配列構造を備えたＣＭＯＳ撮像素子の構成例について説明する断面図。
【図７】本発明の実施例２における２次元的に配列されたＣＭＯＳ撮像素子の構成例について説明する図。
【図８】本発明の実施例２における中心画素と周辺画素における光線とマイクロレンズを含む光学配置について説明する概略図。
【図９】本発明の実施例３における裏面照射型のＣＭＯＳ撮像素子の製造方法について説明する図。
【図１０】従来例における固体撮像素子の構成を説明する図。
【発明を実施するための形態】
【００１０】
本発明を実施するための形態を、以下の実施例により図を用いて説明する。
なお、以下の実施例を説明するための全図において、同一の機能を有するものには同一符号を付け、その重複する構成についての説明は省略する。
【実施例】
【００１１】
［実施例１］
図１を用いて、本発明を適用した裏面照射型のＣＭＯＳ撮像素子の構成例について説明する。
図１において、１００は裏面照射型のＣＭＯＳ撮像素子である。
１１３は基板であり、この基板内部に画素ごとに設けられた光電変換部１１４と、基板１１３に向かって特定の曲率半径をもつ凹型形状の反射部１０１が構成されている。
また、１１０は集光部であるマイクロレンズであり、基板より入射側に設けられている。
また、本実施例の撮像素子は、カラーフィルタ１１１、絶縁部１１２、拡散層１１５、反射防止層１１６、凸型絶縁部１１７、層間絶縁膜１１８、配線部１１９、支持基板１２０を備える。
配線部１１９は、ゲート電極１１９ａと３層の配線層１１９ｂ、１１９ｃ、１１９ｄで構成される。
【００１２】
入射光１３０は、マイクロレンズ１１０によって集光され、焦点位置１３１で結像する。
また、入射光１３０の一部は光電変換部を透過し、凹型形状の反射部１０１で反射される。
この反射光の等倍結像位置とマイクロレンズの焦点位置１３１とを一致させることが可能に構成されている。そのため、反射光は再び焦点位置１３１で結像する。
このような構成により、反射部１０１に到達した光はすべて反射光となり、この反射光は入射時とほぼ同じ光路を逆進する。
このため、全反射光は再び光電変換部へ入射するため、固体撮像素子の感度が高くなる。
【００１３】
これに対して、例えば、入射光と反射光が同じ光路を通らない構成の場合には、反射光の一部は隣接画素へ伝播し、また、配線部などによって散乱され、クロストークなどのノイズの原因になる。
特に、マイクロレンズを含む固体撮像素子では、光電変換部へ入射する角度が大きくなるため、入射光を単純に反射させても、光電変換部へは通らず、隣接画素へ伝播し易くなる。
また、固体撮像素子の画素サイズが小さくなれば、ますます隣接画素との距離が短くなるため、クロストークなどのノイズが大きくなる。
【００１４】

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本実施例では、以上のように入射光と反射光が同じ光路となるように反射部１０１を構成したことにより、入射光１３０はクロストークなどのノイズを低減し、かつ、光電変換部内の伝播距離が長くなり光利用効率が向上する。
このため、画像のＳＮ比を向上させることができる。

【００１５】

図２を用いて、画素サイズが２．０μｍ、シリコンから成る基板１１３の膜厚が２．５０μｍである可視光用の固体撮像素子の数値実施例を説明する。
ただし、基板１１３の入射側表面を第一面１３４、基板１１３の反射部１０１を有する側の表面を第二面１３５とする。
マイクロレンズ１１０、カラーフィルタ１１１、絶縁部１１２、凸型絶縁部１１７の屈折率は全て１．５０であり、画素の中心での膜厚はそれぞれ０．７５０μｍ、０．７５０μｍ、０．５００μｍ、１．００μｍある。
入射光１３０が基板１１３中の光電変換部に効率よく入射するため、焦点位置１３１を光電変換部の中心で基板１１３と反射防止層１１６との界面（第二面１３５）になるように、マイクロレンズ１１０の曲率半径を０．９７９μｍとした。また、マイクロレンズから入射した複数の角を持つ光が、反射部１０１で全て同じ焦点位置１３１に逆進するように、曲率半径を１．００μｍとした。
このような構成にしたことで、反射部１０１の等倍結像位置とマイクロレンズ（集光部）１１０の焦点位置（集光位置）は、第二面１３５上で一致する。

【００１６】

本実施例において、この反射部１０１は、凸型絶縁部１１７の表面にアルミニウムを堆積させて形成される。
これにより、図３に示す反射率が得られ、可視全域で反射率が８０％以上を得ることが可能となる。
このとき、固体撮像素子の光利用効率を図４に示す。
また、反射部１０１がない場合の固体撮像素子の光利用効率を図５に示す。
波長５００ｎｍより長波長側において、反射部１０１を設けることで光利用効率が高くなり、波長７００ｎｍでは１．５倍程度高くなる。
但し、カラーフィルタ１１１の吸光率は本発明の内容と無関係であるため、吸光率が零として見積もった。
このように、反射部１０１の等倍結像位置とマイクロレンズ１１０の焦点位置とを一致させることで、光利用効率を向上させ、感度を高くすることができる。
また、反射部からの反射光は入射時とほぼ同じ光路を逆進するため、配線部などで生じる散乱を低減し、クロストークを低減することができる。
このため、画像のＳＮ比が向上する。

【００１７】

また、本実施例の固体撮像素子の反射部は金属で形成したが、必ずしも金属である必要はなく、誘電体などによる反射膜であってもよい。
誘電体による反射膜であっても入射光を反射させることさえできれば、同様に光利用効率は向上する。
しかしながら、誘電体の反射膜であれば、屈折率差を大きくすることが材料選択性の観点から困難であるため、高反射率が得られない。
また、誘電体多層膜による反射膜を用いると、波長依存性が大きいため、可視光全域で高反射率を得ることはできない。
一方、金属を用いれば、波長依存性が小さく、かつ、高反射率を得ることができる。このため、反射部に金属を用いた方が光利用効率が向上するため望ましい。
また、本実施例の固体撮像素子は基板１１３に対してマイクロレンズ１１０と反対側に配線部１１９を配した裏面照射型としたが、必ずしも裏面照射型である必要はなく、マイクロレンズと配線部が同じ側に配した表面照射型であってもよい。
表面照射型の固体撮像素子においても、本発明の構成であれば裏面照射型の固体撮像素子

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と同様に、光利用効率が向上する。
しかしながら、表面照射型固体撮像素子の場合、入射光側に支持基板を作製することが困難であるため、基板を薄くして、入射光と対向する側に反射部を作製するのが困難である。
一方、裏面照射型固体撮像素子は後述するように、入射光と対向する側に支持基板を貼り合わせ、基板を薄くすることができる。このため、裏面照射型固体撮像素子の方が、容易に作製することができるため望ましい。
【００１８】
また、本実施例のマイクロレンズ１１０の焦点位置１３１と反射部１０１の等倍結像位置は、基板１１３の反射部を有する側の第二面１３５上に形成したが、必ずしも基板の第二面上に形成する必要はない。
基板中または基板の外部に結像させても、光電変換部１１４中に入射光１３０が伝播さえすれば、入射光は電荷信号として検出できる。
しかしながら、裏面入射型固体撮像素子は光電変換部で得られた電荷を転送するトランジスタのドレイン領域となる拡散層１１５が、基板１１３の第二面１３５側に形成される。この拡散層１１５に入射光が伝播すると、拡散層に電荷が発生する。この電荷は、白点ノイズなどのノイズの要因となる。
このため、拡散層に光を入射しないように、第二面に入射光を結像させることが望ましい。
また、本実施例では配線部１１９が複数の配線層１１９ｂ～ｄを有し、反射部１０１はすべての配線層１１９ｂ～ｄより基板側に配した構造としたが、必ずしも、そのような構成である必要はない。
反射部が配線層より支持基板側に配した構造としても、光電変換部を透過した入射光は、反射部によって光電変換部へ反射させることができ、光利用効率は向上する。
但し、光電変換部を透過した光は広がって伝播するため、一部の光は、反射部に到達する前に配線層によって散乱される。
この散乱光は隣接画素の光電変換部に到達すると、クロストークとなる。
このため、反射部は配線層より基板側にあった方が望ましい。
【００１９】
また、本実施例では、配線層１１９ｂ～ｄと反射部１０１をアルミニウムで形成したが、必ずしも同一の材料で形成しなくてもよい。
例えば、配線層１１９ｂ～ｄを銅で形成し、反射部をアルミニウムで形成しても、本発明の効果が得られる。
但し、同一の材料で形成すれば、作製コストを低くすることができるため望ましい。
また、本実施例では基板１１３と凸型絶縁部１１７との間に反射防止層１１６を形成した。
反射防止層がなくても、光電変換部を透過する光は、反射部で反射され光電変換部に再入射するため、光利用効率は向上する。
しかしながら、基板と凸型絶縁部との界面の反射光は、図１０で示した反射膜と同様に、光電変換部に集光せず拡散層１１５や隣接画素へ伝播する。
このため、白点ノイズやクロストークの要因となり、画像のＳＮ比を低下させる。
このようなことから、基板と凸型絶縁部の間に反射防止層を形成し、界面からの反射光を抑制する方が望ましい。
【００２０】
［実施例２］
実施例では、図６を用いて本発明を適用した２次元配列構造を備えたＣＭＯＳ撮像素子の構成例について説明する。
図６において、２００は固体撮像素子であり、本実施例では光電変換部を含む画素２１０を２次元状に複数配列した構造とされている（図７（ａ））。
このとき、通常、カメラレンズの射出瞳２１１と固体撮像素子２００との距離が有限長で

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あるため周辺画素では、主光線２３１が傾いて入射する（図７（ｂ））。
このため、周辺画素では入射光を効率よく光電変換部に入射させるため、入射光を光電変換部へ屈折させるマイクロレンズなどの集光部が必要となる。
仮に、集光部を用いなければ、斜入射光は隣接画素へ伝播しクロストークノイズの要因となる。

【００２１】

図６は、マイクロレンズ１１０によって入射光２３１が集光され、また反射部１０１により反射した光が入射光と同じ光路を逆進する構成をとっている。
このため、反射光は再び光電変換部へ入射するため、固体撮像素子の感度が高くなる。
一方、例えば、入射光と反射光が同じ光路を通らない構成で、特に主光線２３１が傾いている場合、反射部からの反射光は、光電変換部を通らず、主光線の傾きと同じ方向の隣接画素へ伝播する。
このため、クロストークなどのノイズの要因となる。特に、入射光を集光させる集光部を用いない構成では、反射光は固体撮像素子内部で広がるため、クロストークなどのノイズが大きくなる。

【００２２】

以上により、入射光と反射光が同じ光路となるように反射部１０１を構成したことで、入射光１３０はクロストークなどのノイズを低減し、かつ、光電変換部内の伝播距離が長くなり光利用効率を向上させる。このため、画像のＳＮ比が向上する。

【００２３】

次に、主光線が傾いた場合における入射光と反射光が同じ光路となるための構成を説明する。
図８に中心画素と周辺画素における光線とマイクロレンズを含む光学配置の概略図を示す。
中心画素の場合、入射光２３０は垂直入斜となるため、焦点位置１３１は中心画素の中心軸２３５上に位置する（図８（ａ））。
一方、周辺画素の場合、入射光２３１は傾いて入射するため、焦点位置は周辺画素の中心軸上に位置せず、該中心軸より中心画素側と反対側にズレて位置することになる。
このため、マイクロレンズ１１０を周辺画素の中心軸より中心画素側に変位させて配することで、焦点位置１３１を周辺画素の中心軸２３５に変位させることができる（図８（ｂ））。

【００２４】

以上のように、マイクロレンズを中心画素側へ変位させることで、すべての画素で焦点位置を画素中心軸２３５に位置させることができる。
この場合、反射部１０１の曲率中心を焦点位置１３１と一致させると、すべての画素で反射部の曲率中心は入射光の焦点位置である画素中心軸２３５上に位置し、反射光を入射光と同じ光路となるように設計できる。
このとき、反射部１０１はすべての画素で同じように設計すればよく、マイクロレンズとは独立に設計できる。
但し、マイクロレンズ１１０を中心画素側に変位させなくて、反射部の曲率中心を面内で変位させれば、焦点位置と等倍結像位置が一致する。
この場合においても、本発明による光利用効率の向上の効果が得られる。
しかしながら、焦点位置が画素中心軸にないと、光電変換部を透過した光は広がって伝播するため、配線部などによる散乱が生じる。散乱光はクロストークの要因となり、画像のＳＮ比の低下を引き起こす。
そのため、マイクロレンズを変位させて、マイクロレンズの焦点位置と反射部の等倍結像位置を画素中心軸上で一致させた方が、画像のＳＮ比が向上し望ましい。

【００２５】

また、このとき、図６に示すように、光電変換部１１４側から入射した透過光２３３は、周辺画素側に伝播する。

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この透過光２３３を反射させるためには、反射部１０１を周辺画素側にまで大きく形成する必要がある。
しかしながら、反射部１０１を周辺画素側にまで大きく形成すると、反射部１０１と配線層１１９ｂは近接するため、電気的に導電し、固体撮像素子２００は正常に動作しなくなる。
よって、配線層１１９ｂを周辺画素の中心軸より中心画素側と反対側に変位させて配し、反射部１０１と配線層１１９ｂの距離を長くし、絶縁させる。
以上により、周辺画素において、反射部を周辺画素側まで形成しても、配線層を周辺画素側に変位させることで、感度が高く、ノイズの小さな固体撮像素子を得ることができる。
また、本実施例では、ゲート電極１１９ａを周辺画素の中心軸より中心画素側に変位させて配置したことで、透過光２３３は周辺画素側に伝播し、ゲート電極１１９ａに入射しにくくなる。
通常、ゲート電極１１９ａはポリシリコンで形成されるため、ゲート電極１１９ａに透過光が入射すると、透過光は吸収され、光電変換部に再入射する光量が減少する。
このため、ゲート電極１１９ａを周辺画素の中心軸より中心画素側に形成する方が光利用効率が向上するため望ましい。

【００２６】

［実施例３］

実施例３では、図９は、本発明を適用した裏面照射型のＣＭＯＳ撮像素子を製造する際の製造方法の構成例について説明する。
本実施例の製造方法においては、まず、熱酸化によりシリコン基板１１３の表面にシリコン酸化膜を形成する。
続いて、シリコン基板１１３中に光電変換部１１４を形成するために、フォトレジストにより所定位置にレジストマスクを形成し、不純物のイオン打ち込みを行う。
その後、レジストマスクをアッシング等により除去する。続いて、同様のイオン打ち込みの方法で、拡散層１１５を形成する（図９（ａ））。
次に、光電変換部１１４にて発生した電荷を転送するためのゲート電極１１９ａを形成するために、ポリシリコン膜を形成する。
その後、フォトリソ工程を用いてポリシリコンを所定パターンにエッチングしてゲート電極１１９ａを形成する。
その後、シリコン基板１１３、およびゲート電極１１９ａ上に例えばＢＰＳＧなどの層間絶縁膜を形成し、ＣＭＰ法により平坦化を行う（図９（ｂ））。
さらに、レジストマスクを形成し、１６０℃前後でリフロー処理を行い、凸型形状のレジスト３０１を作製する（図９（ｃ））。
その後、ドライエッチングによりレジストマスクの凸型形状を層間絶縁膜に転写し凸型絶縁部１１７を形成する（図９（ｄ））。

【００２７】

続いて、凸型絶縁部１１７にアルミニウムなどの金属を堆積させて、凸型絶縁部１１７の形状を転写した反射部１０１を形成する（図９（ｅ））。
次に、電気的な接続のため、コンタクトホールなどの接続孔を層間絶縁膜に形成して、他の金属配線層に電気的に接続させる。
同様に、第一配線層１１９ｂ、第二配線層１１９ｃおよび第三配線層１１９ｄをそれぞれ形成し、これら配線層を層間絶縁膜１１８で覆う（図９（ｆ））。
続いて、層間絶縁膜１１８の上部に支持基板１２０を貼り合わせ、支持基板１２０を下側にし、基板１１３を光電変換部１１４が形成されている領域までＣＭＰ法により研磨する（図９（ｇ））。
さらに、シリコン基板１１３の第一面１３４側に、絶縁部１１２を形成する。また、必要に応じて、遮光膜を形成する（不図示）。
その後、カラーフィルタ１１１を形成し、マイクロレンズ１１０をリフロー処理によって形成する（図９（ｈ））。

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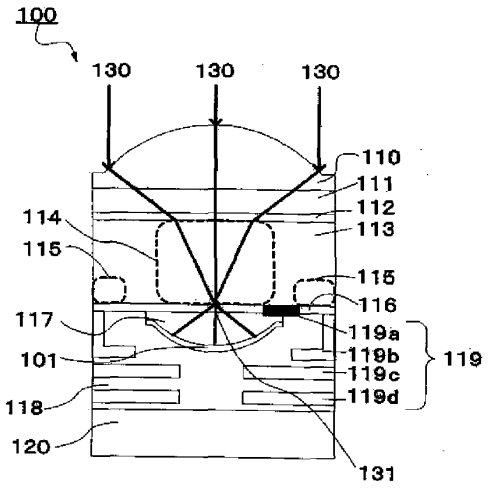
なお、上記の実施例１から実施例３においては、すべてＣＭＯＳ撮像素子に関して説明したが、本発明はＣＭＯＳ撮像素子に限られるものではない。
例えば、ＣＣＤ撮像素子などその他の固体撮像素子に関しても同様に適用できる。

【符号の説明】

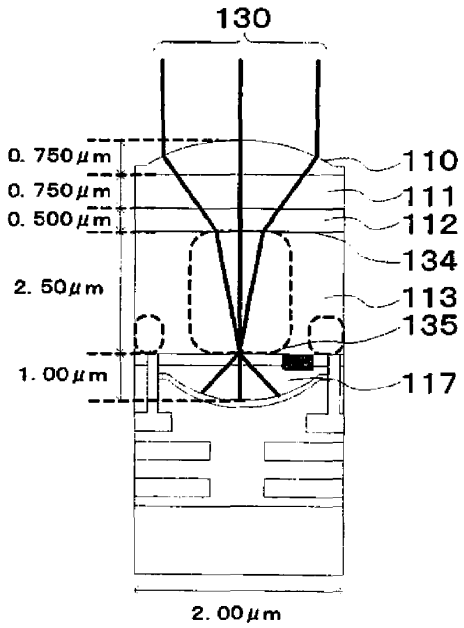
【００２８】

１００：固体撮像素子
１０１：反射部
１１０：マイクロレンズ
１１１：カラーフィルタ
１１２：絶縁部
１１３：基板
１１４：光電変換部
１１５：拡散層
１１６：反射防止層
１１７：凸型絶縁部
１１８：層間絶縁膜
１１９：配線部
１１９ａ：ゲート電極
１１９ｂ、１１９ｃ、１１９ｄ：配線層
１２０：支持基板
１３０：光線
１３１：焦点位置

【図１】

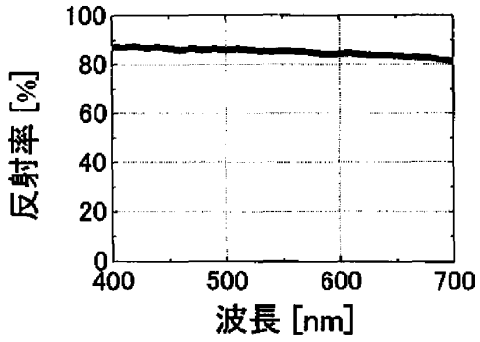


【図２】

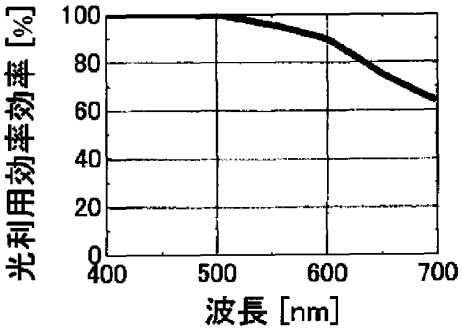


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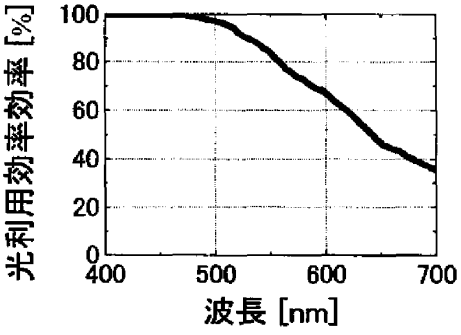
【図３】


反射率 [%]
100
80
60
40
20
0
400
500
600
700
波長 [nm]

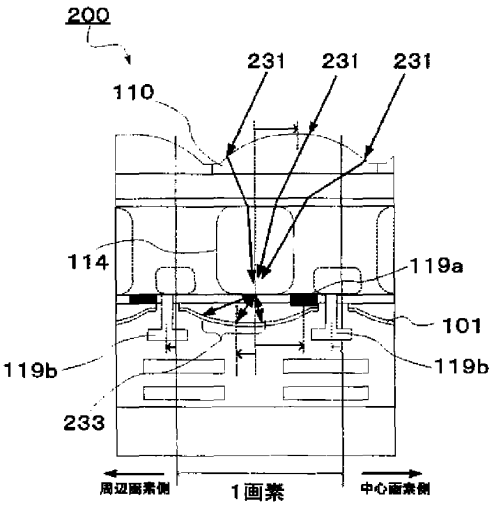
【図４】


光利用効率効率 [%]
100
80
60
40
20
0
400
500
600
700
波長 [nm]

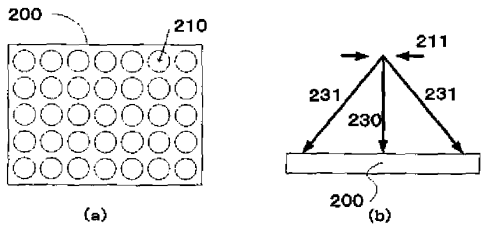
【図５】


光利用効率効率 [%]
100
80
60
40
20
0
400
500
600
700
波長 [nm]

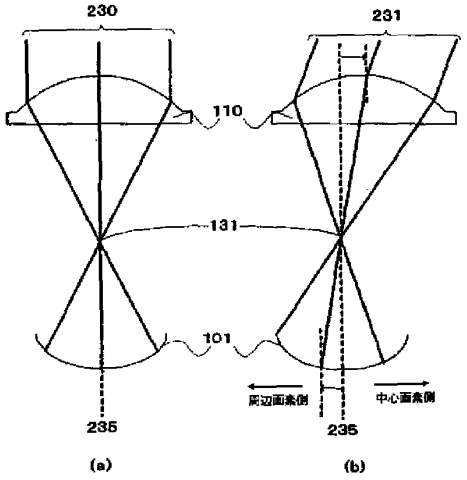
【図６】


200
231
231
231
110
114
119a
101
119b
119b
233
周辺画素側
1画素
中心画素側

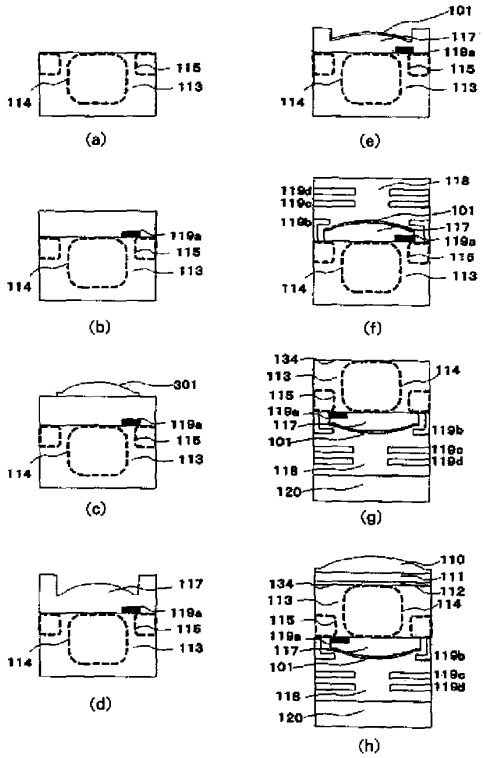
【図７】



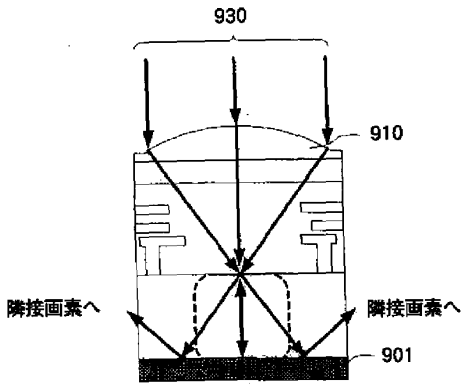
【図８】



【図９】



【図１０】



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PROBLEM TO BE SOLVED: To provide a solid-state image pickup element reducing a noise generation by reflection light and improving a light utilization efficiency when constituting the solid-state image pickup element configured to cause a photoelectric conversion part to reflect an incident light passing through a substrate. ; SOLUTION: The solid-state image pickup element includes the optical conversion part formed inside the substrate with respect to each pixel, and a light condensing part provided on a side of the substrate that the incident light enters and condensing the incident light to the optical conversion part, wherein the solid-state image pickup element includes a reflector provided on a side opposite to the light condensing part and having a recessed shape toward the substrate, and the reflector has a configuration to orient a same-size imaging position of the reflector to a condensing position of the light condensing part. ;
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Last updated: 09.10.2013 Worldwide Database 5.8.11.5; 92p

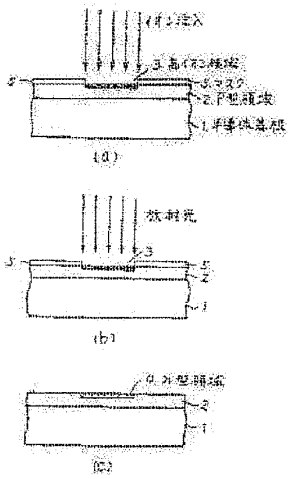
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MANUFACTURE OF SEMICONDUCTOR DEVICE

Publication number: JP2152226 (A)
Publication date: 1990-06-12
Inventor(s): SUGITA YOSHIHIRO +
Applicant(s): FUJITSU LTD +
Classification:
- international: ***H01L21/22; H01L21/26; H01L21/265; H01L21/316;*** **H01L21/02;** (IPC1-7): H01L21/22; H01L21/26; H01L21/265; H01L21/316
- European:
Application number: JP19880306346 19881202
Priority number(s): JP19880306346 19881202

Abstract of **JP 2152226 (A)**

PURPOSE:To heat the extreme surface of an element formation region and to activate this region by a method wherein the element formation region of a semiconductor is irradiated with a non-coherent radiated beam having a continuous spectrum of a soft X-ray region from an extreme vacuum ultraviolet- ray region. CONSTITUTION:A mask 5 is formed on a p-type region 2 formed on a semiconductor substrate 1; n-type impurity ions, e.g. phosphorus ions (P<+>), are implanted very shallowly, e.g. down to a depth of about 50nm, from the upper part; a high-ion region 3 is formed. The high-ion region 3 is irradiated with a synchrotron radiation having a continuous spectrum of a soft X-ray region from an extreme vacuum ultraviolet-ray region. The high-ion region 3 is heated and activated; an n-type region 4 is formed; the mask 5 is removed.



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⑲日本国特許庁(JP)　⑪特許出願公開

⑫公開特許公報(A)　平2−152226

⑤1Int.Cl.⁵	識別記号	庁内整理番号	⑬公開　平成2年(1990)6月12日
H 01 L 21/26	L	7738−5F	
21/22	E	7738−5F	
21/265			
21/316	S	6810−5F	
		7522−5F　H 01 L 21/265	B

審査請求　未請求　請求項の数 1　(全4頁)

⑤4発明の名称　半導体装置の製造方法

⑳特　願　昭63−306346
㉒出　願　昭63(1988)12月2日

⑦2発明者　杉田　義博　神奈川県川崎市中原区上小田中1015番地　富士通株式会社内
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⑦4代理人　弁理士　井桁　貞一

明細書

1．発明の名称

半導体装置の製造方法

2．特許請求の範囲

極真空紫外光領域から軟X線領域の連続スペクトルを持つ非干渉性の放射光を半導体の素子形成領域に照射することにより，該素子形成領域の極表面を加熱して活性化する工程を含むことを特徴とする半導体装置の製造方法。

3．発明の詳細な説明

〔概要〕

半導体装置の製造方法に係り，特に半導体装置の素子形成領域の表面加熱方法に関し，

半導体装置の素子形成領域の表面に極めて薄い活性領域を形成することを目的とし，

極真空紫外光領域から軟X線領域の連続スペクトルを持つ非干渉性の放射光を半導体の素子形成領域に照射することにより，該素子形成領域の極表面を加熱して活性化する工程を含む半導体装置の製造方法により構成する。

〔産業上の利用分野〕

本発明は半導体装置の製造方法に係り，特に半導体装置の素子形成領域の表面加熱方法に関する。

半導体デバイスの微細化に伴い，浅い接合の形成技術や薄膜の活性化技術の開発が必要とされ，盛んに研究が行われている。

〔従来の技術〕

従来，紫外光を用いた半導体の極表面加熱法が試みられており，放電ランプによるラピッドサーマルアニール(Rapid Thermal Anneal)法や，それより短波長で出力密度の高いエキシマレーザを用いた方法が研究されている。

半導体の極表面加熱には，200乃至300nmという短波長光を利用できるエキシマレーザは，ランプ光源よりも有望であるが，一方，光照射損傷によるデバイスの歩留り低下，信頼性低下を引き起

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こすおそれがある。

第5図（a），（b）は従来例としてレーザ光を用いる加熱の工程例を示し，1は半導体基板，2はp型領域，4はn型領域，5はマスク，6はドーピング原料を表す。以下，これらの図を参照しながら説明する。

第5図（a）参照

半導体基板1上に形成されたp型領域2上にマスク5を形成してその開口部にドーピング原料6を付着させる。ドーピング原料6はn型不純物を含むものであって，例えばフォスフィン（PH_3）である。

開口部の上からエキシマレーザによるレーザ光を照射してp型領域2の表面を加熱する。

第5図（b）参照

ドーピング原料6はp型領域2の中に拡散して極く薄いn型領域4が形成される。その後マスク5を除去する。

ところで，レーザ光を物質に照射した場合，光照射損傷のおそれがあり，その光照射損傷には熱的なものの他にレーザ光の単色性，可干渉性に起因するアバランシェ破壊がある。

第6図はレーザ光照射の場合の電界振幅を示す。

真空から物質に入射したレーザ光には界面を節とする定在波が立ち，表面から1／4波長入ったところで電界振幅は最大となる。したがって，その深さで電界集中が起こりアバランシェ破壊を生じ易くなる。

さらに，物質中にレーザ光特有の波長を吸収する吸収センタが含まれているとき，そこが熱発生源となって不均一な熱歪みが発生するといった問題もある。

〔発明が解決しようとする課題〕

従って，レーザ光による加熱の場合は表面を均一に加熱出来ないという問題，デバイスに局部的な損傷を与えるといった問題がある。

本発明は，上記の欠点を克服して，デバイスに損傷を与えることなく極めて薄い表面を均一に加熱し，極めて薄い活性領域を形成する方法を提供することを目的とする。

〔課題を解決するための手段〕

上記課題は，極真空紫外光領域から軟X線領域の連続スペクトルを持つ非干渉性の放射光を半導体の素子形成領域に照射することにより，該素子形成領域の極表面を加熱して活性化する工程を含む半導体装置の製造方法によって解決される。

〔作用〕

高速荷電粒子の制動放射光であるシンクロトロン放射光は，紫外線領域からX線領域までの連続光光源として知られ，結晶の分析評価に用いられている。その波長域はエキシマレーザでは達成できない数十nm域の極真空紫外光から1nm程度の軟X線を含む。

本発明では，かかる放射光を利用する。波長が短ければ物質への進入深さが浅くなり，極表面の加熱に有利となる。

さらに，シンクロトロン放射光を光源とした場合，利用できる光は広い範囲の連続光となり，しかも非干渉性であるので，レーザ光に見られる前記の欠点を避けることができる。

第4図に放射光照射の場合の電界振幅を示す。この場合は真空から物質への界面で干渉による定在波は発生せず，進入深さとともに電界振幅は漸減する。したがって，レーザ光を用いる場合のような1／4波長深さでのアバランシェ破壊といった現象は生じない。

したがって，シンクロトロン放射光のような放射光を用いれば半導体の素子形成領域を均一にしかもデバイスに損傷を与えることなく極表面だけ加熱して，そこを活性化することができる。

〔実施例〕

以下，本発明の実施例について説明する。

第1図（a）乃至（c）は実施例Iで，極く薄い接合を作成する工程の例であり，1は半導体基板，2はp型領域，3は高イオン領域，4はn型領域，5はマスクを表す。

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第1図（a）参照

半導体基板1上に形成されたp型領域2上にマスク5を形成し，上部からn型の不純物イオン，例えば燐イオン（P^+）を極く浅く例えば50nm程度の深さまで打ち込んで，高イオン領域3を形成する。

第1図（b）参照

極真空紫外線光領域から軟X線領域の連続スペクトルを有するシンクロトロン放射光を高イオン領域3に照射する。

第1図（c）参照

高イオン領域3は加熱され，活性加されてn型領域4を形成する。

マスク5を除去する。

第2図（a），（b）は実施例Ⅱで，極く薄い接合を作成する別の工程例であり，1は半導体基板，2はp型領域，4はn型領域，5はマスク，6はドーピング原料を表す。

第2図（a）参照

半導体基板1上に形成されたp型領域2上にマスク5を形成し，その開口部にn型の不純物を含むドーピング原料6として，例えばフォスフィン（PH_3）を吸着させる。あるいはドーピング原料雰囲気中に半導体基板1を配置する。

上部から極真空紫外線光領域から軟X線領域の連続スペクトルを有するシンクロトロン放射光を照射する。

第2図（b）参照

p型領域2の表面付近は加熱されて，ドーピング原料6の不純物イオンがp型領域2中に拡散して，極く浅いn型領域4が形成される。マスク5を除去する。

この実施例は，イオン注入過程がなく，また，光照射損傷もないため極めて結晶性の高いドーピング領域のn型領域4が形成される。

第3図（a），（b）は実施例Ⅲで，半導体基板上にドーパントを含む絶縁膜を作成する例であり，1はSi基板，6はドーピング原料，7はSiO_2膜，71はドーパントを含むSiO_2膜を表す。

第3図（a）参照

半導体基板1として，例えばSi基板を用い，表面に熱酸化により厚さ約50nmのSiO_2膜7を形成する。

不純物固着トラップとして働く原子，例えば塩素（Cl）原子を含むドーピング原料6をSiO_2膜7上に吸着させる。あるいはドーピング原料雰囲気中にSi基板1を配置する。

上部から極真空紫外線光領域から軟X線領域の連続スペクトルを有するシンクロトロン放射光を照射する。

第3図（b）参照

SiO_2膜7は加熱されて塩素（Cl）原子を取込み，ドーパントを含むSiO_2膜71が形成される。

ドーパントを含むSiO_2膜71中の塩素（Cl）原子はSi基板1とドーパントを含むSiO_2膜71の界面に存在する重金属イオンを吸い寄せて固着する。

したがって，このように活性化された絶縁膜を用いればSi基板1の界面特性を改善することができる。

なお，極真空紫外線光領域以下の波長の放射光を用いることにより，従来のエキシマレーザ光では達成できない極めて浅い表面層を加熱することができるが，軟X線領域よりも短い波長では逆に侵入深さが大きくなって目的が達成されない。

〔発明の効果〕

以上説明した様に，本発明によれば，半導体装置の素子形成領域の極表面を均一にしかもデバイスに損傷を与えることなく加熱することができ，極く浅い接合や不純物トラップ機能を有する極く薄い絶縁膜等の活性領域を形成することができ，半導体デバイスの微細化，高速化に寄与するところが大きい。

4．図面の簡単な説明

第1図は実施例Ⅰ，

第2図は実施例Ⅱ，

第3図は実施例Ⅲ，

第4図は放射光照射の場合の電界振幅，

第5図は従来例，

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第6図はレーザ光照射の場合の電界振幅である。図において，

1は半導体基板であってSi基板，

2はp型領域，

3は高イオン領域，

4はn型領域，

5はマスク，

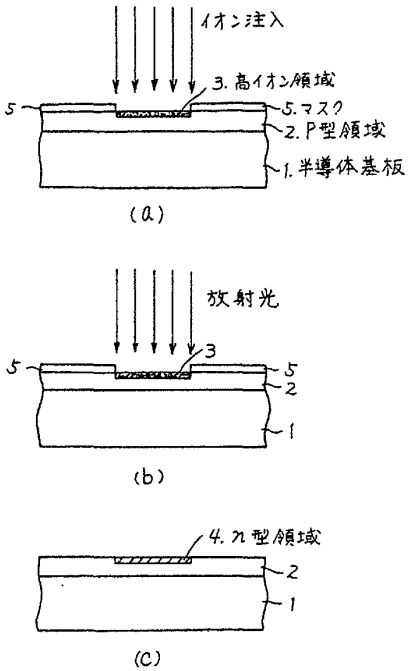
6はドーピング原料，

7は絶縁膜であってSiO_2膜，

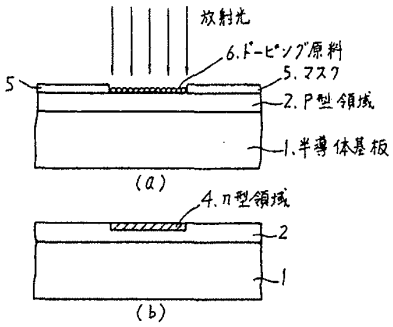
71はドーパントを含むSiO_2膜

を表す。

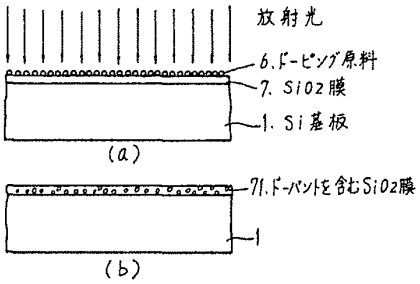
代理人　弁理士　井桁貞一



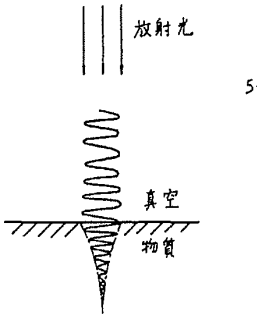
実施例 I
第1図



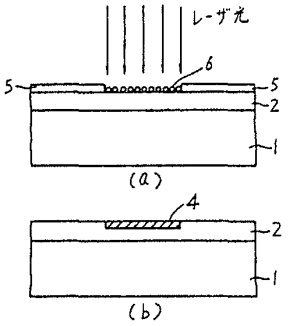
実施例 II
第2図



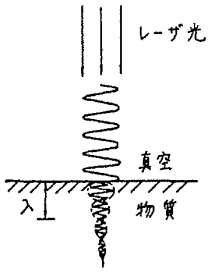
実施例 III
第3図



放射光照射の場合の電界振幅
第4図



従来例
第5図



レーザ光照射の場合の電界振幅
第6図

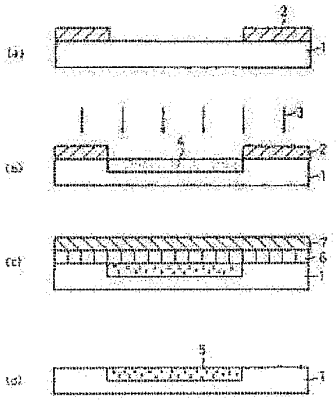
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MANUFACTURE OF SEMICONDUCTOR DEVICE

Publication number: JP63116421 (A)
Publication date: 1988-05-20
Inventor(s): OSAWA MASARU +
Applicant(s): MITSUBISHI ELECTRIC CORP +
Classification:
- international: ***H01L21/265; H01L21/324;*** **H01L21/02;** (IPC1-7): H01L21/265; H01L21/324
- European:
Application number: JP19860263160 19861105
Priority number(s): JP19860263160 19861105

Abstract of **JP 63116421 (A)**

PURPOSE:To prevent As from oozing from a GaAs substrate thereby to obtain a semiconductor device having good characteristics by depositing an amorphous As layer on an ion implanted surface as is after implanting, continuously depositing an insulating layer on the surface of the amorphous As layer, and then annealing it. CONSTITUTION:An active layer forming photoresist pattern 2 is formed by photocomposing technique on a GaAs substrate 1. Si<+29> ions 3 are implanted to form an ion implanted region 4. It is dipped in acetone to remove the pattern 2, and an a-As layer 6 and an insulating layer 7 are continuously deposited by a CVD method on the ion 3 implanted surface. It is heat treated at 800 deg.C for 40 min in a reducing atmosphere to obtain a highly activated active layer 5. It is dipped in a fluoric acid to remove the insulating layer, and dipped in a hydrochloric acid to remove the layer 6 to thereby expose the surface of the substrate 1. Thus, it can prevent As from oozing from the substrate 1 to obtain a semiconductor device having good characteristics.



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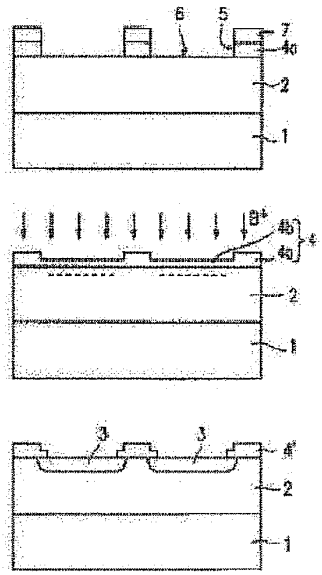
PHOTO DETECTOR AND MANUFACTURE THEREOF

Publication number: JP9298308 (A)
Publication date: 1997-11-18
Inventor(s): FUKUNAGA NAOKI; KUBO MASARU +
Applicant(s): SHARP KK +
Classification:
- international: ***H01L21/265; H01L31/10;*** **H01L21/02; H01L31/10;** (IPC1-7): H01L21/265; H01L31/10
- European:
Application number: JP19960109765 19960430
Priority number(s): JP19960109765 19960430

Also published as:
JP3516552 (B2)

Abstract of **JP 9298308 (A)**

PROBLEM TO BE SOLVED: To reduce the proportion of those carriers recombined to disappear on a semiconductor structure among carriers caused by a light incidence by distributing impurity in a diffused layer forming a photo detecting part of a semiconductor layer so that its concn. increases toward the surface of the semiconductor layer. SOLUTION: The surface 6 of an epitaxially grown layer 2 exposed in openings 5 of a first insulation film 4a is oxidized to form a first thermal oxide layer 4b, and a p-type impurity is implanted into the grown layer 2 under the condition of an implanting incident range less than the thickness of the second oxide layer 4b. This condition is to locate peaks of an impurity profile just after the ion implanting, not in the interior of the epitaxially grown layer 2 but in that of the second oxide film 4b.; For activating the impurity, it is heat treated in a nonoxidative atmosphere to activate and diffuse the impurity to form impurity diffused regions 3.



Data supplied from the ***espacenet*** database — Worldwide

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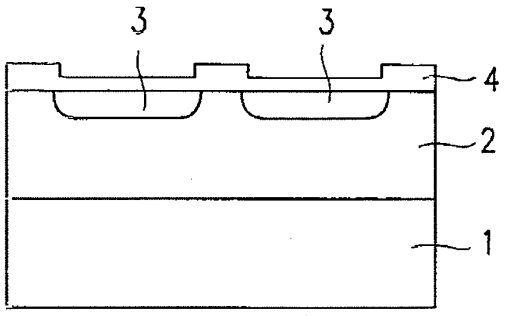
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(54)【発明の名称】　受光素子及びその製造方法

(57)【要約】

【課題】　半導体表面で再結合して消滅する光キャリアを減少させ、侵入長の比較的短い光に対して高い感度で光電変換を達成する。

【解決手段】　表面を有する第１導電型の半導体層２と、半導体層２の受光部に形成された少なくともひとつの第２導電型の不純物拡散層３とを備え、不純物拡散層３によってフォトダイオードが形成されている。不純物拡散層３内の第２導電型不純物は、半導体層２の表面に近づくほど濃度が高くなるように分布している。



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【特許請求の範囲】
【請求項１】　表面を有する第１導電型の半導体層と、該半導体層の受光部に形成された少なくともひとつの第２導電型の不純物拡散層とを備え、該不純物拡散層によってフォトダイオードが形成されている受光素子であって、
該不純物拡散層内の第２導電型不純物は、該半導体層の該表面に近づくほど濃度が高くなるように分布している受光素子。
【請求項２】　前記半導体層の前記表面において前記不純物拡散層に接触する絶縁膜を更に備えており、
前記第２導電型不純物の濃度は、該絶縁膜の内部で極大値を示している請求項１に記載の受光素子。
【請求項３】　前記絶縁膜は、反射防止膜として機能する請求項２に記載の受光素子。
【請求項４】　前記半導体層は、基板上にエピタキシャル成長した膜から形成されている請求項１から３の何れかに記載の受光素子。
【請求項５】　前記半導体層には、前記受光部からの信号を処理するための回路が形成されている請求項４に記載の受光素子。
【請求項６】　凹部を有する絶縁膜を第１導電型の半導体層の上に形成する工程と、
該絶縁膜を介して第２導電型不純物イオンを該半導体層に注入し、該絶縁膜の凹部の直下にフォトダイオードのための第２導電型不純物拡散層を形成する工程と、を包含する受光素子の製造方法であって、
該不純物拡散層を形成する工程は、該絶縁膜の凹部の厚さよりも注入飛程が小さくなる加速エネルギーで該不純物イオンを注入する工程を含んでいる、受光素子の製造方法。
【請求項７】　前記凹部を有する絶縁膜を形成する工程は、
第１の絶縁層を前記半導体層上に形成する工程と、
該第１の絶縁層を加工することによって、該第１の絶縁膜層に少なくとも一つの開口部を形成する工程と、
該第１の絶縁層の開口部内で露出する該半導体層の表面を熱酸化することによって、該開口部内に第２の絶縁層を形成する工程と、を包含している請求項６に記載の受光素子の製造方法。
【請求項８】　開口部を有する絶縁膜を第１導電型の半導体層の上に形成する工程と、
該絶縁膜の開口部内で露出する該半導体層の表面を覆うように、該絶縁膜上に反射防止膜を堆積する工程と、
該反射防止膜を介して第２導電型不純物イオンを該半導体層に注入し、該絶縁膜の開口部の直下にフォトダイオードのための第２導電型不純物拡散層を形成する工程と、を包含し、
該不純物拡散層を形成する工程は、該反射防止膜の厚さよりも注入飛程が小さくなる加速エネルギーで該第２導電型不純物イオンを注入する工程を含んでいる、受光素子の製造方法。
【請求項９】　開口部を有する絶縁膜を第１導電型の半導体層の上に形成する工程と、
第２導電型不純物を含む拡散ソース膜を、該絶縁膜の開口部内で露出する該半導体層の表面を覆うように該絶縁膜上に堆積する工程と、
該拡散ソース膜から該第２導電型不純物を該半導体層に拡散させ、該絶縁膜の開口部の直下にフォトダイオードのための第２導電型不純物拡散層を形成する工程と、を包含する受光素子の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、受光素子及びその製造方法に関しており、特に、波長の短い光に対して高い感度で応答することのできる受光素子及びその製造方法に関する。特に、本発明は、デジタルビデオディスク（ＤＶＤ）再生装置の光ピックアップに適した受光素子及びその製造方法に関する。
【０００２】
【従来の技術】受光素子は、光エネルギーを受けて、それを電気エネルギーに変換する素子である。このような受光素子は、様々な装置に用いられている。近年、ＣＤ、ＭＯ、ＰＤ、及びＤＶＤ等の光学記録媒体の需要が増大するにつれ、光ピックアップに用いられる受光素子の研究開発が積極的に進められている。光学記録媒体の記録密度は、記録媒体に集光される光ビームのスポットサイズが小さいほど高くなる。光ビームのスポットサイズは、光の波長の二乗に比例するので、光源である半導体レーザ素子の発振波長を短くすることが検討されている。ＤＶＤの再生装置では、まず、波長６５０ｎｍまたは６３５ｎｍのレーザ光が使用され、将来的には、波長４３０ｎｍ前後のレーザ光が使用される。
【０００３】受光素子による光電変換は、半導体中に形成されたＰＮ接合に逆バイアスを印加し、それによって形成した空乏層及びその近傍に、光を照射することによって行われる。光の照射は半導体中にキャリアを励起（生成）し、励起されたキャリア（光キャリア）は拡散層及び空乏層に生じた電位勾配に従って移動し、ＰＮ接合に到達することによって光起電力（光電流）が生まれる。
【０００４】半導体表面に照射された光は、半導体に吸収されながら内部に侵入してゆくので、半導体中の光の強度は、半導体表面からの距離（深さ）に応じて指数関数的に減少する。上記キャリアは半導体に吸収された光によって生成されるため、吸収係数αの大きな光ほど、半導体表面の近傍にキャリアを生成することになる。光の吸収係数αは、光の波長と半導体の種類によって異なる。
【０００５】半導体内部に侵入した光の強度が、半導体

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表面における強度の１０％に低下する位置の半導体表面から計測した距離（深さ）を、本願明細書では、「侵入長（侵入深さ）」と呼ぶことにする。図９は、シリコンにおける光の強度（表面における光の強度を１とした場合の、光強度の割合）が、シリコン表面からの深さに依存してどのように変化するかを示すグラフである。図９からわかるように、例えば、波長が７８０ｎｍの光の「侵入長」は、約２０μｍである。

【０００６】以下に、図１０（ａ）～（ｄ）を参照しながら、従来の受光素子の製造方法を説明する。

【０００７】まず、図１０（ａ）に示されるように、公知のエピタキャル成長法を用いて、Ｎ型単結晶シリコン基板１０１の主面の上、全面に、Ｎ型エピタキシャル成長層１０２を形成する。次に、酸化性雰囲気中で熱処理を行うことによって、Ｎ型エピタキシャル成長層１０２の表面を熱酸化し、SiO_2膜１０４を形成する。

【０００８】次に、図１０（ｂ）に示すように、公知のリソグラフィ技術及びエッチング技術を用いて、絶縁膜１０４に開口部１０５を設け、Ｎ型エピタキシャル成長層１０２の表面１０６を部分的に露出させる。この開口部１０５の形状及び位置は、フォトダイオードを形成すべき領域を規定する。

【０００９】次に、図１０（ｃ）に示されるように、Ｎ型エピタキシャル成長層１０２の表面１０６のうち、開口部１０５で露出する領域に、Ｐ型不純物イオンを注入する。イオン注入直後の不純物濃度プロファイルのピークは、エピタキシャル成長層１０２の内部に位置する。

【００１０】次に、不純物活性化のための熱処理を行う。この熱処理によって、不純物が活性化されるとともに、不純物が拡散し、図１０（ｄ）に示されるように、不純物拡散領域１０３が形成される。このようして形成された受光素子のフォトダイオードは、図１１に示すような不純物濃度プロファイルを有している。

【００１１】

【発明が解決しようとする課題】上述の従来技術によれば、比較的に波長の短い光に対して感度が極めて低く、高いＳ／Ｎ比が得られないという問題がある。

【００１２】例えば、従来の光ピックアップに用いられる受光素子では、せいぜい、波長が７８０ｎｍ程度のレーザ光を検出できれば良かったが、今後は、更に短い波長の光、例えば、４３０ｎｍ程度のレーザ光を高い感度で検出することが強く望まれるようになってくる。このような短い波長の光は、図９から明らかなように、シリコン表面から約１μｍの範囲内でほとんど吸収される。

【００１３】従来の受光素子に形成されたフォトダイオードは、図１１に示すような不純物濃度プロファイルを有している。図１１から明らかなように、表面近傍で不純物濃度の低下がみられる。この不純物濃度の低下は、従来の製造方法を採用している限り、避けられない現象である。特に、不純物イオンの注入後にシリコン表面を熱酸化して、清浄なシリコン／酸化膜界面を形成する場合、シリコン中の不純物が熱酸化膜中に取り込まれ（パイルアップ）、シリコン表面の不純物濃度が低下する（偏析現象）。このため、従来の製造方法を実施する限り、図１１に示されるように、シリコン表面近傍で不純物濃度が低下してしまう。

【００１４】波長が７８０ｎｍまたはそれ以上の光に対して用いられる受光素子では、このような表面近傍での不純物濃度の低下は、ほとんど問題になることなく、特に重要視されない現象であった。それは、波長が７８０ｎｍまたはそれ以上の光に対しては、シリコンにおける光の侵入長が約２０μｍを越える大きさを持ち、シリコン表面から深い位置まで光が到達していたため、表面近傍（深さが約０．５μｍ以下の領域）でのキャリアの振る舞いが、受光素子の感度にほとんど影響を与えていなかったからである。

【００１５】しかし、シリコンにおける光の侵入長は、波長が青色領域（例えば、４３０ｎｍまたはそれ以下）の光に対しては約１μｍを下回るため、シリコン表面から深い位置まで光が到達しない。このため、受光素子が青色領域の光を受けた場合は、表面近傍（例えば、深さが約０．５μｍ以下の領域）でのキャリアの振る舞いが、受光素子の感度に重要な影響を与えると考えられる。

【００１６】より詳細に述べれば、図１１に示すような不純物濃度プロファイルを持つフォトダイオードでは、ＰＮ接合に逆バイアスを印加した場合、光の照射によって発生したキャリアのうち半導体表面の近傍で発生したものは、表面より内部にピークを持つＰ型拡散層のポテンシャル分布によって、表面側に移動し、表面再結合によって消滅することになる。

【００１７】従来のような不純物プロファイルを持つ受光素子において、このような表面再結合（界面再結合）によって消滅する光キャリアの割合は、波長が４３０ｎｍの光の場合、全体の最大６０％にも達すると考えられる。このため、光電変換効率は、理論的には、０．３５Ａ／Ｗ程度になるが、現実には、０．１５Ａ／Ｗ程度にしかならないと計算される。

【００１８】本願発明者は、デジタルビデオディスク（ＤＶＤ）等の光情報記録媒体から青色レーザ光を用いて高密度情報を再生する場合において、上記現象が光ピックアップの感度を著しく低下させると予測する。

【００１９】本発明は、上記課題を解決するためになされたものであり、その目的とするところは、光の入射によって半導体中に発生したキャリア（光キャリア）のうち、半導体表面で再結合して消滅するものの割合を低減し、侵入長の比較的短い光に対して高い感度で光電変換を達成できる受光素子及びその製造方法を提供することにある。

【００２０】

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【課題を解決するための手段】本発明の受光素子は、表面を有する第１導電型の半導体層と、該半導体層の受光部に形成された少なくともひとつの第２導電型の不純物拡散層とを備え、該不純物拡散層によってフォトダイオードが形成されている受光素子であって、該不純物拡散層内の第２導電型不純物は、該半導体層の該表面に近づくほど濃度が高くなるように分布しており、そのことにより上記目的が達成される。

【００２１】ある実施形態では、前記半導体層の前記表面において前記不純物拡散層に接触する絶縁膜を更に備えており、前記第２導電型不純物の濃度は、該絶縁膜の内部で極大値を示している。

【００２２】前記絶縁膜は、反射防止膜として機能してもよい。また、前記半導体層は、基板上にエピタキシャル成長した膜から形成されていてもよい。更に、前記半導体層には、前記受光部からの信号を処理するための回路が形成されてもよい。

【００２３】本発明の受光素子の製造方法は、凹部を有する絶縁膜を第１導電型の半導体層の上に形成する工程と、該絶縁膜を介して第２導電型不純物イオンを該半導体層に注入し、該絶縁膜の凹部の直下にフォトダイオードのための第２導電型不純物拡散層を形成する工程と、を包含する受光素子の製造方法であって、該不純物拡散層を形成する工程は、該絶縁膜の凹部の厚さよりも注入飛程が小さくなる加速エネルギーで該不純物イオンを注入する工程を含んでおり、そのことにより上記目的が達成される。

【００２４】ある実施形態では、前記凹部を有する絶縁膜を形成する工程は、第１の絶縁層を前記半導体層上に形成する工程と、該第１の絶縁層を加工することによって、該第１の絶縁膜層に少なくとも一つの開口部を形成する工程と、該第１の絶縁層の開口部内で露出する該半導体層の表面を熱酸化することによって、該開口部内に第２の絶縁層を形成する工程と、を包含している。

【００２５】本発明の他の受光素子の製造方法は、開口部を有する絶縁膜を第１導電型の半導体層の上に形成する工程と、該絶縁膜の開口部内で露出する該半導体層の表面を覆うように、該絶縁膜上に反射防止膜を堆積する工程と、該反射防止膜を介して第２導電型不純物イオンを該半導体層に注入し、該絶縁膜の開口部の直下にフォトダイオードのための第２導電型不純物拡散層を形成する工程とを包含し、該第２導電型不純物拡散層を形成する工程は、該反射防止膜の厚さよりも注入飛程が小さくなる加速エネルギーで該不純物イオンを注入する工程を含んでおり、そのことにより上記目的が達成される。

【００２６】本発明の更に他の受光素子の製造方法は、開口部を有する絶縁膜を第１導電型の半導体層の上に形成する工程と、第２導電型不純物を含む拡散ソース膜を、該絶縁膜の開口部内で露出する該半導体層の表面を覆うように該絶縁膜上に堆積する工程と、該拡散ソース膜から該第２導電型不純物を該半導体層に拡散させ、該絶縁膜の開口部の直下にフォトダイオードのための第２導電型不純物拡散層を形成する工程とを包含し、そのことにより上記目的が達成される。

【００２７】

【発明の実施の形態】以下に、本発明の実施の形態を説明する。

【００２８】本発明による受光素子は、第１導電型の半導体層と、この半導体層内に形成された第２導電型の不純物拡散層とを備えている。不純物拡散層の不純物濃度は、第１導電型半導体層の表面近傍において半導体層の内部よりも高く、そのことによって、光の入射によって半導体層の表面近傍に発生したキャリアが半導体層の内部に流れる。

【００２９】（実施例１）以下、図面を参照しながら、本発明による受光素子の第１の実施例を説明する。

【００３０】まず、図１を参照する。図１に示す受光素子は、Ｎ型単結晶シリコン基板１と、その上に形成されたＮ型エピタキシャル成長層（単結晶シリコン層）２と、Ｎ型エピタキシャル成長層２の受光部内に形成された複数のＰ型不純物拡散層３とを備えている。Ｎ型エピタキシャル成長層２の表面は、凹部を有する絶縁膜（SiO_2膜）４によって覆われている。本願明細書においては、絶縁膜４の「凹部」とは、絶縁膜４の他の部分よりも厚さの薄い部分を指し、不純物拡散層３は、この凹部の直下に形成されている。

【００３１】なお、図１には受光素子の受光部だけが示されているが、エピタキシャル成長層２の不図示の部分（非受光部）に、例えば、受光部からの信号を処理するための周辺回路が形成されてもよい。このような信号処理回路は、バイポーラトランジスタ等によって形成されることが好ましい。

【００３２】Ｎ型単結晶シリコン基板１としては、例えば、面方位が（１１１）で、比抵抗が０．０１～０．１Ω・ｃｍの基板が用いられる。本実施例のＮ型エピタキシャル成長層２は、厚さが１．０～１０μｍで、不純物濃度は例えば$1\times10^{15}cm^{-3}$である。

【００３３】Ｐ型不純物拡散層３は、Ｎ型エピタキシャル成長層２の選択された領域の表面からＰ型不純物が拡散され、導電型がＮ型からＰ型へ反転した領域であり、エピタキシャル成長層２のＮ型領域との間でＰＮ接合を形成している。受光素子が動作するとき、このＰＮ接合には逆バイアス電圧が印加され、それによって空乏層が形成される。空乏層及びその近傍（空乏層端から拡散長程度の距離内）で光照射によって生じたキャリアは、光の強度に応じた大きさを持つ電流を形成する。この電流（または電圧）を測定することによって、受けた光の強度を検出することができる。

【００３４】なお、Ｎ型エピタキシャル成長層２をシリコン基板１の上に形成することなく、Ｐ型不純物拡散層

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３を、直接、N型シリコン基板１内に形成しても良い。本実施例で、N型エピタキシャル成長層２をシリコン基板１の上に形成している理由は、周辺回路のバイポーラトランジスタをN型エピタキシャル成長層２に形成することを念頭に置いているからである。一般に、バイポーラトランジスタを形成するためには、エピタキシャル成長層の形成が必要となる。

【００３５】図２は、本実施例の受光素子の受光部において、N型エピタキシャル成長層２の表面から深さ方向に沿って計測した不純物濃度のプロファイル（Depth Profile）を示している。図２から明らかなように、エピタキシャル成長層２の表面（深さ：０μｍ）から内部に向かって、P型不純物の濃度は単調に減少している。言い換えると、エピタキシャル成長層２の表面近傍で不純物濃度は低下しておらず、表面に近づくにつれ不純物濃度は高くなる。図１に示す例では、表面で不純物濃度は、約$2\times10^{18}cm^{-3}$という値を示している。

【００３６】このような不純物濃度プロファイルの不純物拡散領域は、光キャリアが半導体表面に向かって移動するときのポテンシャルバリアとなる。そのため、光の照射を受けて不純物拡散層３の表面近傍に生じたキャリアは、不純物拡散層３の表面側にではなく、内部側に移動することができる。

【００３７】このような不純物プロファイルを持つ受光素子においては、表面再結合（界面再結合）によって消滅する光キャリアの割合は、波長が４３０ｎｍの光の場合、全体の約１０％以下に減少すると考えられる。このため、フォトダイオードの光感度は、エピタキシャル層の再結合による光キャリアの消滅が支配的となり、光電変換効率は、０．２５～０．３Ａ／Ｗにまで向上する。

【００３８】次に、図３（ａ）～（ｄ）を参照しながら、上記受光素子の製造方法を説明する。

【００３９】まず、図３（ａ）に示されるように、公知のエピタキャル成長法を用いて、N型単結晶シリコン基板１の主面の全面に、N型エピタキシャル成長層２を形成する。次に、酸化性雰囲気（例えば、酸素や水蒸気）中で熱処理を行い、N型エピタキシャル成長層２の表面を熱酸化することによって、第１の絶縁膜（SiO_2膜）４ａを形成する（第１の熱酸化工程）。例えば、水蒸気雰囲気で、約５０分間、温度１０００～１１００℃の熱処理を行えば、３００～６００ｎｍの厚さを持った熱酸化膜が得られる。本実施例では、厚さ約５００ｎｍの熱酸化膜を形成している。この第１の熱酸化膜４ａは、あとの不純物イオン注入工程でマスクとして機能する。従って、その厚さは、注入された不純物イオンがN型エピタキシャル成長層２の表面に到達しないように設定される。

【００４０】次に、図３（ｂ）に示すように、公知のリソグラフィ技術及びエッチング技術を用いて、第１の絶縁膜４ａに開口部５を設け、N型エピタキシャル成長層２の表面６を部分的に露出させる。この開口部５の形状及び位置は、フォトダイオードを形成すべき領域、言い換えると、不純物拡散層３を形成すべき領域の形状及び位置を規定する。開口部５の形成は、開口部５のパターンを持ったレジスト層７を第１の絶縁膜４ａ上に形成した後、第１の絶縁膜４ａのレジスト層７に覆われていない部分をエッチングすることにより行われる。エッチングは、ドライエッチングまたはウェットエッチングの何れであっても良い。また、一般に、ウェットエッチングはドライエッチングに比較して表面６に損傷を与えにくいので、ドライエッチングで第１の絶縁膜４ａを薄膜化した後、引き続いてウェットエッチングで薄膜化した部分を除去するという２段階エッチングを行っても良い。

【００４１】なお、受光素子が、光ピックアップ用に用いられるとき、受光部には複数のフォトダイオードが形成されるので、当然、第１の絶縁膜４ａに設けられる開口部５の数は複数である。

【００４２】レジスト層７を除去した後、第２の熱酸化工程を行う。この工程は、前記第１の熱酸化工程と同様の方法で行われ得る。図３（ｃ）に示されるように、この熱酸化工程によって、第１の絶縁膜４ａの開口部５内で露出していたエピタキシャル成長層２の表面６を酸化し、そこに比較的に薄い第２の熱酸化膜（例えば、５０ｎｍ）４ｂを形成することができる。この熱酸化工程によって、第１の熱酸化膜４ａの厚さも増加する。なお、厳密に言えば、この熱酸化によって、エピタキシャル成長層２の表面６の位置はエピタキシャル成長層２の内部に向かって僅かに移動する。本実施例では、第１の熱酸化膜４ａ及び第２の熱酸化膜４ｂによって、「凹部を有する絶縁膜４」が構成されている。

【００４３】次に、公知のイオン注入法によって、P型不純物（本実施例では「ボロン（Ｂ）」）をエピタキシャル成長層２に注入する。このイオン注入は、注入の投影飛程（Ｒｐ）が第２の熱酸化膜４ｂの厚さ以下になる条件で行われる。このようにする理由は、イオン注入直後の不純物濃度プロファイルのピークを、エピタキシャル成長層２の内部ではなく、第２の熱酸化膜４ｂの内部に位置させるためである。第２の熱酸化膜４ｂの厚さが５０ｎｍの場合、例えば、加速エネルギーを１５ｋｅＶにすれば良い。この場合、第２の熱酸化膜４ｂの中にあって、エピタキシャル成長層２の表面６から約１０ｎｍ程度離れた位置に不純物濃度プロファイルのピーク（極大値）が位置する。

【００４４】次に、不純物活性化のため、非酸化性雰囲気（例えば　窒素ガス）中で、例えば、３０分間、９００～１０００℃の熱処理を行う。この熱処理によって、不純物が活性化されるとともに、不純物が拡散し、不純物拡散領域３が形成される（図３（ｄ））。この熱処理によって不純物が深く拡散することを避けるため、ランプアニール法などによって比較的に高温で短時間の熱処

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理を行ってもよい。

【００４５】上記工程によって、図２に示す不純物濃度分布を持った不純物拡散領域３が得られる。

【００４６】なお、図３（ｄ）では、第２の熱酸化膜４ｂの大部分が除去され、不純物拡散領域３の表面が露出している状態が示されている。この工程は必ずしも必要ない。

【００４７】次に、図４（ａ）～（ｃ）を参照して、上記製造工程の間に生じる不純物の再分布を説明する。

【００４８】まず、図４（ａ）は、不純物イオンの注入直後の濃度分布を模式的に示している。不純物濃度のピークは、エピタキシャル成長層２の表面６と第２の熱酸化膜４ｂの表面３６との間に位置している。

【００４９】図４（ｂ）は、不純物活性化のための熱処理後における不純物イオンの濃度分布を模式的に示している。不純物濃度のピークは、なおも、エピタキシャル成長層２の表面６と第２の熱酸化膜４ｂの表面３６との間に位置している。この例では、浅い接合を形成するため、不純物の拡散（不純物の再分布）が大きく進行しないように熱処理を行っている。もし、熱処理の温度が高く、また、時間が長いと、不純物が深く拡散してしまうため、拡散層のプロファイルがなだらかになり、不純物拡散層３の内蔵電界が弱まる。このため、拡散層中のキャリアの移動時間が長くなり、不純物拡散層３中で発生したキャリアが再結合により消滅してしまう問題がある。従って、不純物活性化のための熱処理条件は、図２のグラフに示すような不純物の濃度プロファイルが失われないように選択されなければならない。

【００５０】図４（ｃ）は、第２の熱酸化膜４ｂを除去し、反射防止膜８を堆積した後における不純物イオンの濃度分布を模式的に示している。この場合、反射防止膜８の中には、ほとんど不純物は拡散していない。このため、不純物濃度のピークは、エピタキシャル成長層２の表面６（反射防止膜８とエピタキシャル成長層２との界面）に位置している。

【００５１】不純物活性化のための熱処理は、第２の熱酸化膜４ｂを除去する前に行っても、あるいは、反射防止膜８を堆積した後に行っても良い。

【００５２】また、第２の熱酸化膜４ｂを開口部５内に形成する代わりに、第２の熱酸化膜４ｂと同様の厚さを持つ絶縁膜を基板上にＣＶＤ法やスパッタリング法によって堆積しても良い。ただし、一般に、そのような方法で堆積された絶縁膜とエピタキシャル成長層２との界面に比較して、熱酸化膜（４ｂ）とエピタキシャル成長層２との界面は清浄である。そのため、熱酸化膜（第２の熱酸化膜４ｂ）を形成する方が、表面再結合（界面再結合）の原因となる表面準位（界面準位）が形成されにくいので好ましいといえる。

【００５３】なお、図５に示すように、不純物拡散層３の表面を覆っている第２の熱酸化膜４ｂを除去して、開口部を有する絶縁膜４’を形成した後、例えばシリコンナイトライド膜からなる反射防止膜８を基板上に堆積しても良い。反射防止膜８の厚さは、受光素子の受ける光の波長に応じて適宜選択される。レーザ光等の単色性の強い光のための受光素子である場合は、反射防止膜８の厚さは、λ／（４ｎ）の奇数倍に等しくなるように設定される。なお、λは光の波長、ｎは反射防止膜８の屈折率である。反射防止膜８は、単層構造の代わりに多層構造を有していても良い。

【００５４】また、反射防止膜８は、不純物拡散層３の表面を覆っている第２の熱酸化膜４ｂを除去することなく、その上に形成しても良い。その場合、反射防止膜８の厚さは、第２の熱酸化膜４ｂの存在を考慮して最適化される。

【００５５】（実施例２）次に、図６（ａ）及び（ｂ）を参照しながら、本発明による受光素子の他の製造方法を説明する。

【００５６】まず、実施例１で説明した方法と同様の方法を用いて、図６（ａ）に示される構成を得る。図６（ａ）では、Ｎ型単結晶シリコン基板１１の上にＮ型エピタキシャル成長層１２が形成されており、Ｎ型エピタキシャル成長層１２の表面１６が、開口部１５を有する絶縁膜（厚さ：３００～６００ｎｍ）１４で覆われている。開口部１５の形状及び位置は、フォトダイオードを形成すべき領域、言い換えると、不純物拡散層を形成すべき領域の形状及び位置を規定する。

【００５７】次に、図６（ｂ）に示されるように、シリコンナイトライドからなる反射防止膜（厚さ：約３０～２００ｎｍ）１８を絶縁膜１４上に堆積した後、イオン注入法によってＰ型不純物（本実施例では「ボロン（Ｂ）」）をエピタキシャル成長層１２に注入する。このイオン注入は、注入の投影飛程（R_p）が反射防止膜１８の厚さ以下になる条件で行われる。このようにする理由は、イオン注入直後の不純物濃度プロファイルのピークを、エピタキシャル成長層１２の内部ではなく、反射防止膜１８の内部に位置させるためである。

【００５８】反射防止膜１８の厚さが約５０ｎｍの場合、例えば、加速エネルギーを１７ｋｅＶにすれば良い。この場合、反射防止膜１８の中にあって、エピタキシャル成長層１２の表面から約３０～４０ｎｍ程度離れた位置に不純物濃度プロファイルのピークが位置する。

【００５９】次に、不純物活性化のため、非酸化性雰囲気（例えば　窒素ガス）中で、例えば、約３０分間、９００～１０００℃の熱処理を行う。この熱処理によって、不純物が活性化されるとともに、不純物が拡散し、不純物拡散領域１３が形成される。

【００６０】上記工程によって、図２に示す不純物濃度分布を持った不純物拡散領域１３が得られる。

【００６１】このように本実施例では、フォトダイオードのための不純物イオン注入を、反射防止膜１８を堆積

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した後に行っており、しかも、注入直後の不純物濃度プロファイルのピークが反射防止膜１８中に位置するようにしている。

【００６２】反射防止膜１８は、単層構造の代わりに多層構造を有していてもよい。反射防止膜が多層構造を有している場合、まず、反射防止膜を構成する幾つかの層を基板上に堆積した後に上記不純物イオン注入を行い、その後に、残りの層を堆積することによって反射防止膜１８の形成を完了してもよい。

【００６３】なお、反射防止膜１８に不純物イオンの一部が注入された結果、反射防止膜１８の屈折率が変化する可能性がある。そのような屈折率の変化が大きい場合は、その屈折率の変化を考慮したうえで、反射防止膜１８の厚さを決定することが好ましい。

【００６４】上記実施例１及び実施例２の何れの場合も、不純物拡散層３を形成するために、絶縁膜（熱酸化膜やシリコンナイトライド膜）を透過するようにして不純物イオンを注入する方法を採用した。特に、不純物の濃度プロファイルのピークがその絶縁膜の内部に位置するように、不純物イオンの注入加速エネルギや絶縁膜の厚さを調整した。そうすることによって、図２に示すような不純物濃度プロファイルを持つフォトダイオードが形成できた。

【００６５】なお、不純物イオン注入時に、不純物拡散層３または１３の形成領域を覆う膜は、上記実施例１及び実施例２で用いた膜に限定されない。また、上記実施例では、何れも、不純物拡散層３及び１３の導電型をＰ型とし、これらの不純物拡散層３または１３が形成される半導体層の導電型をN型としているが、これらの導電型を反転させた構造を用いても良い。Ｐ型の不純物拡散層３及び１３を形成するために使用する不純物イオンとしては、B以外にBF_2等を使用しても良いし、また、他のIII族元素のイオンを用いても良い。N型の不純物拡散層を形成するためには、Ｖ族元素のイオン（例えば砒素（Ａｓ））を用いる。

【００６６】本願発明は、比較的に波長の短い光（例えば、４３０ｎｍ）に対して高い感度（高い量子効率）で応答できる受光素子を提供することを目的としているので、不純物拡散層の３及び１３の厚さ（接合深さ）は、そのような波長の短い光の侵入長程度以下に設定されることが好ましい。

【００６７】（実施例３）実施例１及び実施例２では、イオン注入法を用いて不純物拡散領域３及び１３をそれぞれ形成した。本実施例では、イオン注入法に代えて、固相拡散法を用いる。

【００６８】図７を参照して、本実施例の製造方法を説明する。

【００６９】まず、実施例１で説明した方法と同様の方法を用いて、図６（ａ）に示される構成を得る。図７では、N型単結晶シリコン基板２１の上にN型エピタキシャル成長層２２が形成されており、N型エピタキシャル成長層２２の表面２６が、開口部２５を有する絶縁膜（厚さ：３００～６００ｎｍ）２４で覆われている。開口部２５の形状及び位置は、フォトダイオードを形成すべき領域、言い換えると、不純物拡散層を形成すべき領域の形状及び位置を規定する。

【００７０】次に、図７に示されるように、Ｐ型不純物（本実施例では「ボロン（Ｂ）」）のドープされた絶縁膜（拡散ソース膜）２９を絶縁膜２４上に堆積する。絶縁膜２９は、絶縁膜２４の開口部２５を介してN型単結晶シリコン基板２１の表面２６に接触する。Ｐ型不純物がドープされた絶縁膜２９として、本実施例では、ボロンを２０重量％含むボロシリケートガラス（ＢＳＧ、厚さ：約５０～５００ｎｍ）を用いた。

【００７１】この後、例えば、９００～１０５０℃で、５～１０秒間の熱処理を行す。この熱処理によって、絶縁膜２９から不純物（ボロン）をN型単結晶シリコン基板２１に熱拡散し、不純物拡散層２３を形成する。熱処理の温度及び時間を調節することにより、前述の実施例の場合よりも、浅い接合を形成することができる。なお、絶縁膜２４の厚さは、絶縁膜（拡散ソース膜）２９からの不純物拡散のバリアとして十分に機能する厚さや膜質を持つように選択される。

【００７２】絶縁膜２９を除去した後、シリコンナイトライドからなる反射防止膜を堆積しても良い。また、絶縁膜２９の厚さを調整することによって、この絶縁膜２９をそのまま反射防止膜として使用しても良い。

【００７３】（実施例４）次に、受光部が形成されている基板上に信号処理回路部を一体的に内蔵した受光素子の実施例を説明する。この実施例は、複数のフォトダイオードが配置された受光部と、ＮＰＮトランジスタを主要な回路素子として含む信号処理回路部とを、同一半導体基板上に有している。

【００７４】以下、図８を参照し、製造工程の順序に従いながら本実施例の構成を説明する。

【００７５】まず、Ｐ型単結晶シリコン基板４１の主面のうち、その上にＮＰＮトランジスタが形成されるべき領域とフォトダイオードが形成されるべき領域とに、N型埋込拡散層４２を形成する。また、受光部に形成される各フォトダイオードを分離する領域と、信号処理回路部に形成される各回路素子を分離する領域に、Ｐ型埋込拡散層（不純物：ボロン、不純物濃度：$4\times10^{17}cm^{-3}$）４４を形成する。

【００７６】次に、Ｐ型単結晶シリコン基板４１上にN型エピタキシャル成長層（厚さ：約３μｍ）４３を形成する。この後、N型エピタキシャル成長層４３のうちＰ型埋込拡散層４４に対応した領域に、表面からＰ型不純物を拡散し、それによってＰ型埋込拡散層４５を形成する。Ｐ型埋込拡散層４５は、Ｐ型埋込拡散層４４の上部にまで到達し、Ｐ型埋込拡散層４４及び４５は、各フォ

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トダイオードや回路素子を相互に電気的に分離する。

【００７７】次に、ＮＰＮトランジスタを形成するために、周知の工程によって、Ｐ型ベース拡散層（不純物：ボロン、不純物濃度：$2\times10^{18}cm^{-3}$）４６、Ｎ型エミッタ拡散層（不純物：ヒ素、不純物濃度：$1\times10^{19}cm^{-3}$）４８、Ｎ型コレクタ取り出し用拡散層（不純物：ヒ素、不純物濃度：$1\times10^{19}cm^{-3}$）４７を順次形成する。Ｎ型エミッタ拡散層４８及びＮ型コレクタ取り出し用拡散層４７は、Ｐ型ベース拡散層４６を形成した後、Ｎ型エピタキシャル成長層４３上に形成した絶縁膜に開口部を設け、その開口部からＮ型不純物を拡散することによって形成される。

【００７８】一方、フォトダイオードが形成される領域に対しては、上記絶縁膜の開口部を介して、Ｐ型不純物が拡散されＰ型不純物拡散層４６’が形成される。このＰ型不純物拡散層４６’は、前述の方法によって形成され、図２に示すような濃度プロファイルを持つ。なお、ＮＰＮトランジスタのＰ型ベース拡散層４６と、フォトダイオードのＰ型不純物拡散層４６’とは、同一工程によって形成されても良い。ただし、ＮＰＮトランジスタのＰ型ベース拡散層４６は、図２のような不純物プロファイルを持つ必要がないので、Ｐ型不純物拡散層４６’を形成する工程とは異なる工程によって形成されてもよい。

【００７９】次に、シリコンナイトライドからなる反射防止膜（厚さ：５０ｎｍ）を形成する。その後、Ｐ型ベース拡散層４６、Ｎ型コレクタ取り出し用拡散層４７及びＮ型エミッタ拡散層４８のそれぞれに接触するように、ベース用電極５０、コレクタ用電極４９及びエミッタ用電極５１を形成する。これらの電極の形成には、公知のメタライゼーション技術が用いられる。

【００８０】本実施例では。フォトダイオードの分割領域に光が照射された場合の応答速度を改善するために、フォトダイオードの下方にもＮ型埋込拡散層（不純物：アンチモン、不純物濃度：$1\times10^{19}cm^{-3}$）４２を形成している。

【００８１】上記実施例としては、何れの場合も、シリコンからなる半導体層を用いた例を説明してきたが、本発明はシリコン以外の半導体層を用いた場合にも適用できるのは言うまでもない。

【００８２】また、図２に示すような不純物濃度プロファイルを得るには、図１１に示す不純物濃度プロファイルを持つシリコン層（又はシリコン基板）を形成した後、その表面の一部をエッチングや研磨等によって除去してもよい。

【００８３】

【発明の効果】本発明によれば、光の入射によって半導体中に発生したキャリア（光キャリア）が、半導体表面から遠ざかる方向にドリフトし、それによって効率的に電気信号が生成される。このため、半導体表面で再結合して消滅する光キャリアが減少し、侵入長の比較的短い光に対して高い感度で光電変換が達成される。

【００８４】本発明によれば、これから実用化されるであろう短波長レーザ光（例えば波長４３０ｎｍのレーザ光）に対して、シリコンを材料として極めて高い感度を持った受光素子を提供できるので、短波長レーザ素子を光源とする光情報媒体再生装置（例えばＤＶＤ装置）の光ピックアップを小型化・低消費電力化することが可能となる。

【図面の簡単な説明】

【図１】本発明による受光素子の実施例の断面図。

【図２】本発明による受光素子の実施例における不純物濃度プロファイルを示すグラフ。

【図３】（ａ）から（ｄ）は、本発明による受光素子製造方法の実施例を示す工程断面図。

【図４】（ａ）から（ｃ）は、製造工程の間に生じる不純物の再分布を示すグラフ。

【図５】本発明による受光素子の他の実施例の断面図。

【図６】（ａ）及び（ｂ）は、本発明による受光素子製造方法の他の実施例を示す工程断面図。

【図７】本発明による受光素子製造方法の更に他の実施例を示す工程断面図。

【図８】本発明による受光素子の更に他の実施例の断面図。

【図９】シリコンにおける光の吸収量（表面における光の強度を１とした場合の、光強度の割合）の深さ依存性を示すグラフ。

【図１０】（ａ）から（ｄ）は、受光素子製造方法の従来例を示す工程断面図。

【図１１】受光素子の従来例における不純物濃度プロファイルを示すグラフ。

【符号の説明】

１、１１、２１　Ｎ型単結晶シリコン基板

２、１２、２２　Ｎ型エピタキシャル成長層（単結晶シリコン層）

３、１３、２３　Ｐ型不純物拡散層

４、１４　絶縁膜（SiO_2膜）

４ａ　第１の絶縁膜

４ｂ　第２の熱酸化膜

５、１５、２５　開口部

６、１６、２６　エピタキシャル成長層２の表面

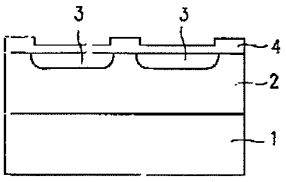
７　レジスト層

８、１８　反射防止膜

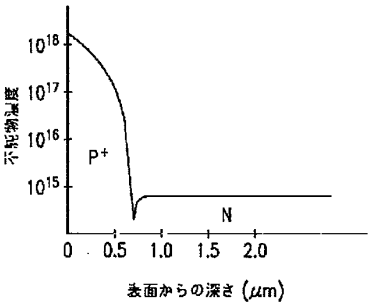
２９　絶縁膜

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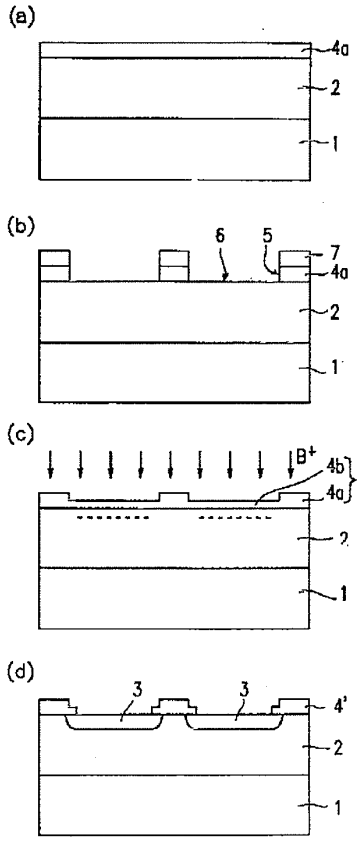
【図1】



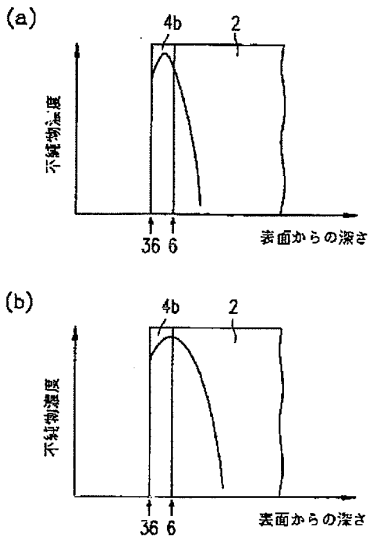
【図2】



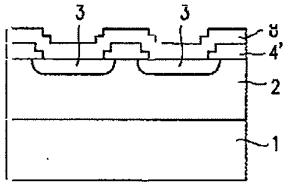
【図3】



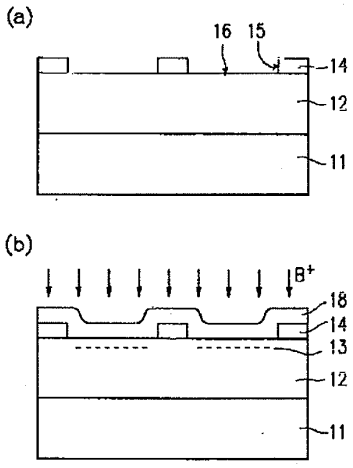
【図4】



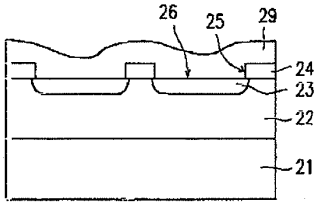
【図5】



【図6】

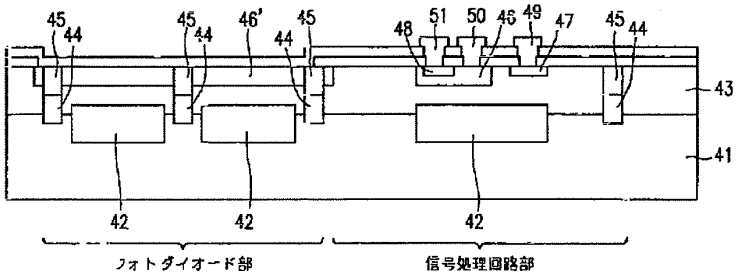


【図7】

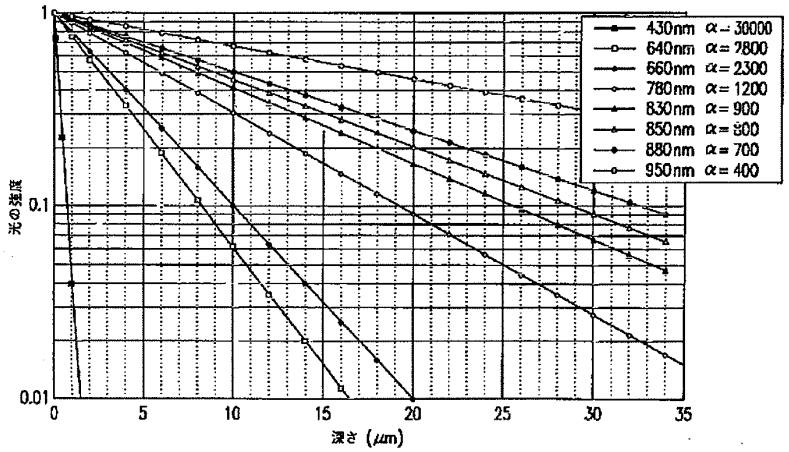


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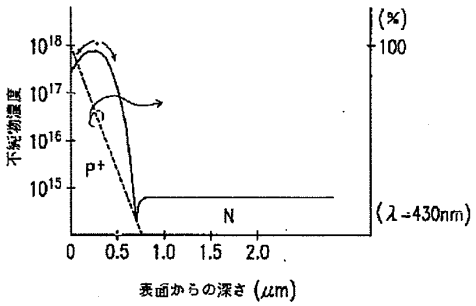
【図8】


45
44
46'
48
51
50
49
47
43
41
42
フォトダイオード部
信号処理回路部

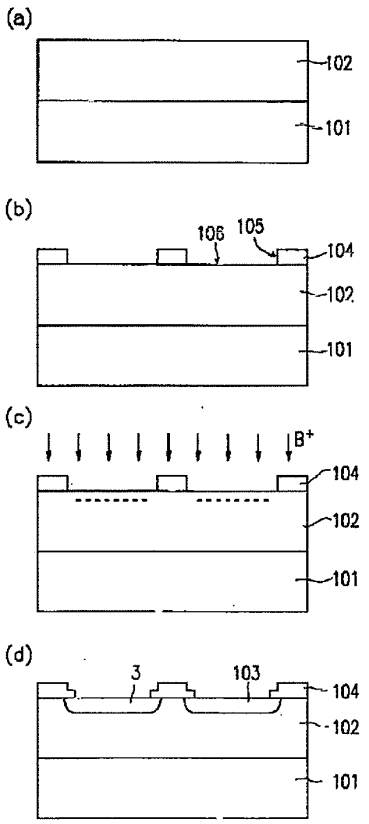
【図9】


430nm α=30000
640nm α=7800
660nm α=2300
780nm α=1200
830nm α=900
850nm α=800
880nm α=700
950nm α=400
光の強度
深さ (μm)

【図11】


(%)
100
(λ=430nm)
P+
N
表面からの深さ (μm)

【図１０】



No documents available for this priority number.

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METHOD FOR MANUFACTURING IMAGE SENSOR

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Abstract of KR20010061058 (A)

PURPOSE: A method for manufacturing an image sensor is provided to improve quantum efficiency and sensitivity, by additionally depositing a dielectric layer of a low absorption rate between a photodiode and an initial interlayer dielectric to improve illuminance of incident light. CONSTITUTION: A photodiode region and a peripheral device are formed on a substrate(41). The first insulating layer in which an index of refraction, Nx is a square root of N0N and a thickness, Tx is (2n-1)lambda/4Nx (n=0,1,2,3,...), is formed on the photodiode region. The first insulating layer is eliminated to be left only on the photodiode region. The second insulating layer is formed on the resultant structure.

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(54) 이미지센서의 제조 방법

요약

입사광의 조도를 향상시켜 양자효율 및 광감도를 개선하는데 적합한 이미지센서 제조 방법에 관한 것으로, 이를 위한 본 발명은 기판에 포토다이오드영역 및 주변소자를 형성하는 제 1 단계, 상기 포토다이오드영역 상부에 굴절율 $N_X=\sqrt{N_o N}$ 이고 두께 $\gamma_{x=(2n-1)\frac{\lambda}{4N_x}}\ [n=0,1,2,3,\ldots]$ 인 제1절연층을 형성하는 제 2 단계, 상기 포토다이오드영역의 상부에만 남도록 상기 제1절연층을 제거하는 제 3 단계, 상기 결과물 상에 제2절연층을 형성하는 제 4 단계를 포함하여 이루어진다.

대표도
도 3f

색인어
이미지센서, 포토다이오드, 조도, 굴절율, PMD

명세서

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도면의 간단한 설명

도 1 은 일반적인 CMOS 이미지센서의 단위화소를 나타낸 등가회로도,

도 2 는 종래기술의 이미지센서의 단위화소 제조 방법을 나타낸 제조 공정 단면도,

도 3a 내지 도 3f 는 본 발명의 실시예에 따른 이미지센서의 단위화소 제조 방법을 나타낸 제조 공정 단면도,

도면의 주요 부분에 대한 부호의 설명

41 : 반도체 기판 47 : 포토다이오드

51 : 버퍼유전층 53 : PMD

57 : 제1금속배선 60 : 층간절연막

63 : 소자보호막 64 : 컬러필터

66 : 마이크로렌즈

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 이미지센서에 관한 것으로, 특히 입사광의 조도(Illuminance)를 향상시킨 CMOS 이미지센서(Image sensor)에 관한 것이다.

일반적으로 이미지센서에는 CCD(Charged Coupled Device) 이미지센서와 CMOS 이미지센서를 이용하는데, 통상의 CCD 이미지센서는 외부의 피사체이미지를 촬상한 빛을 흡수하여 광전하를 모으고 축적하는 광전변환 및 전하축적부, 상기 광전변환 및 전하축적부에서 발생된 전하를 운송하기 위한 전하운송부 및 상기 전하운송부로부터 운송된 광전하를 전기적신호로 출력하는 신호변환부로 구성된다.

여기서 광전변환 및 전하축적부는 주로 포토다이오드(Photodiode;PD)를 사용하는데, 포토다이오드(PD)는 PN접합을 이용하여 포텐셜웰(Pontential well)을 형성시키고 빛(Light)에 의해 발생된 전하를 포텐셜웰에 축적해 두는 소자이다. 그리고 전하축적부에서 발생된 전하는 포토다이오드(PD)의 포텐셜웰에 갇혀있는데, 이 포텐셜웰을 움직임으로써 필요한 곳으로 전하를 운송할 수 있다. 또한 신호변환부는 운송된 전하로부터 전압을 발생시킨다. 한편, 신호검출이 끝나면 다음 차례를 기다리는 전하를 위하여 현재 포텐셜웰의 전하는 배출할 필요가 있는데, 이를 위하여 신호변환부의 포텐셜웰의 장벽을 제거하여 전하를 배출하는데 이를 리셋(Reset)이라고 한다.

이처럼 CCD 이미지센서는 CMOS 이미지센서와 달리 트랜지스터에 의한 스위칭방식이 아니라 전하결합에 의해서 신호를 검출한다. 그리고, 단위화소(Unit pixel)에 해당하고 광감지역할을 하는 포토다이오드(PD)는 광전류를 즉시 추출하지 않고 일정시간 누적시킨 다음 추출하므로 신호전압을 누적시간만큼 증가시킬 수 있어 광감도(Sensitivity)가 좋고, 노이즈(Noise)를 감소시킬 수 있는 장점이 있는 반면, 광전하를 계속 운송해야 하므로 구동방식이 복잡하고, 약 8 ~ 10V의 고전압 및 1W이상의 고전력이 소모된다.

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반면 CMOS 이미지센서는 CCD 이미지센서에 비하여 전기광학적 특성에서 열세를 보이고 있으나, 저소비전력과 집적도 측면에서는 CMOS 이미지센서가 CCD 이미지센서보다 우수하다.

이러한 전기광학적 특성 중 외부양자효율(External Quantum Efficiency) 및 광감도(Sensitivity) 특성은 이미지센서의 품질(Quality)을 좌우하는 특성으로서, 특히 단위 시간당 포획할 수 있는 이미지프레임(Image frame) 및 이미지 품질(Image quality) 등을 결정하는 매우 중요한 특성이다.

도 1은 통상의 CMOS 이미지센서의 단위화소를 나타낸 등가회로도로서, 1개의 포토다이오드(PD)와 4개의 NMOS트랜지스터(Tx,Rx,Sx,Dx)로 구성되며, 상기 4개의 NMOS트랜지스터(Tx,Rx,Sx,Dx)는 포토다이오드(PD)에서 집속된 광전하를 플로팅노드 (Floating node; X)로 운송하기 위한 트랜스퍼트랜지스터(Tx), 원하는 값으로 노드의 전위를 세팅하고 전하를 배출하여 플로팅노드를 리셋(Reset) 시키기 위한 리셋트랜지스터(Rx), 소오스팔로워 버퍼증폭기(Source Follower Buffer Amplifier) 역할을 하는 드라이브트랜지스터(Dx), 스위칭(Switching) 역할로 어드레싱(Addressing)을 할 수 있도록 하는 셀렉트트랜지스터(Sx)로 구성된다.

도 2 는 종래기술에 따른 CMOS 이미지센서의 단위화소 제조 방법을 개략적으로 나타낸 도면이다.

도 2 에 도시된 바와 같이, 종래기술의 CMOS 이미지센서의 단위화소는, P형 반도체기판(11)에 국부적으로 P형 웰(12)을 형성한 다음, 단위화소간의 분리를 위한 필드절연막(13)을 형성한다. 이어 상기 P형 반도체기판(11) 내부에 P-N접합층 (17a,17b)을 형성하여 포토다이오드(PD)를 이루고, 상기 반도체기판(11)에 상기 포토다이오드(PD)로부터 생성된 전하를 전달받아 저장하는 플로팅접합층(18a)을 형성한다.

이어 상기 포토다이오드(PD)로부터 플로팅접합층(18a)으로 상기 광전하를 전달하기 위한 트랜스퍼트랜지스터(Tx)의 게이트전극을 형성하며, 상기 플로팅접합층 (18a)을 리셋시키기 위한 리셋트랜지스터(Rx)의 게이트전극을 형성한다. 이어 상기 플로팅접합층(18a)에 전기적으로 접속된 게이트전극을 갖는 드라이브트랜지스터 (Dx)와 어드레싱을 위한 신호를 자신의 게이트전극으로 인가받는 셀렉트트랜지스터 (Sx)를 형성한다. 이 때, 상기 리셋트랜지스터(Rx)와 드라이브트랜지스터(Dx)는 공통접합층(18b)을 가지며, 상기 공통접합층(18b)은 상기 반도체기판(11)과 P형 웰(12)의 경계에 형성된다. 이어 상기 필드절연막(13)의 일측에 셀렉트트랜지스터 (Sx)의 게이트전극을 형성하며, 상기 드라이브트랜지스터(Dx)와 셀렉트트랜지스터 (Sx)는 LDD(Lightly Doped Drain) 구조의 불순물접합층(19)이 형성된다. 여기서 게이트전극은 게이트산화막(14), 폴리실리콘(15)과 텅스텐실리사이드(16)로 이루어지며, 게이트전극의 측벽에는 측벽스페이서(20)가 형성된다.

그리고 상기 4개의 트랜지스터(Tx,Rx,Dx,Sx) 상부에 광투과를 위한 제1층간절연막(21,22)과 제2층간절연막(23,24,25)을 형성하고, 상기 제1,2층간절연막들 (21,22,23,24,25)을 선택적으로 식각하여 상기 트랜지스터들(Tx,Rx,Dx,Sx)을 외부소자와 연결하기 위해 티타늄/알루미늄/티타늄나이트라이드(26,27,28)의 적층막으로 이루어진 제1,2금속배선을 형성한다. 또한 상기 제2금속배선 상부에 습기 또는 스크래치(Scratch)로부터 소자를 보호하기 위해 산화막(29) 및 질화막(30)으로 이루어진 소자보호막을 형성하며, 상기 소자보호막 상부에 컬러이미지 구현을 위해서 상기의 단위화소 배열위에 적색, 초록색 및 청색 또는 황색, 자홍색, 청록색으로 구성된 컬러필터(31)의 배열(Color Filter Array; CFA) 공정을 진행한다. 이어 상기 컬러필터(31)의 배열 상부에 평탄층(32)을 형성한 다음, 상기 평탄층(32) 상부에 컬러필터(31) 배열에 대향하는 마이크로렌즈(33)를 형성한다.

이와 같은 공정이 모두 완료된 후 광감지영역인 포토다이오드 상부에는 광투과를 위한 제1,2층간절연막(21,22,23,24,25), 소자보호막(29,30), 컬러필터(31) 및 마이크로렌즈(33)만이 위치하게 된다.

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상술한 바와 같이, 종래기술에서는 외부양자효율 및 광감도의 특성을 향상시키기 위해 단위화소마다 마이크로렌즈(33)를 형성하여 입사광을 집속시키고 있으나, 마이크로렌즈(33)로 집속된 입사광은 마이크로렌즈(33)의 중심부와 주변부의 입사각도가 달라지므로 같은 수의 광량(Photon flux)이 집속되었다 하더라도 단위화소의 중심부와 주변부로 입사되는 광자(Photon)의 조도는 달라지게 된다.

즉 단위화소의 중심(θ = "θ_c = "0)으로" 입사되는 광자의 조도를 i_c라 하면, 단위화소의 주변으로 입사각도 θ = "θ_E로 입사되는 광자의 조도 i_E는 $i_c \times \cos^4\theta$ 에 비례하므로 $\cos^4\theta$ 만큼 감소하게 된다. 따라서 단위화소로 입사되는 광자의 입사각도를 줄여주어야만 한다.

이러한 이미지센서의 특성을 향상시키기 위해 반도체기판(11)은 동일한 가시광선영역에서 4.72~ 3.48의 굴절율(N_S)을 가지며, 단위화소의 포토다이오드(PD)를 형성한 후 포토다이오드(PD) 표면에 최초로 증착되는 절연층(PMD)(21,22)은 통상적으로 가시광선영역대(450~635nm)에서 1.48~ 1.46의 굴절율(N_O)을 갖는다. 그리고 마이크로렌즈(33)는 폭이 7.5㎛, 높이가 2.6㎛로 형성된다.

이와 같은 조건의 단위화소로 입사되는 입사광의 최초 입사각은 0(degree)이지만, 마이크로렌즈(33)에 부딪히는 순간 입사광의 입사각은 공기에서 마이크로렌즈로(33)의 매질차와 마이크로렌즈(33)의 곡률에 의하여 변하게 된다. 즉, 최초 공기중에서 입사각이 0(degree)인 입사광이 마이크로렌즈(33)의 중심부로 입사될 때의 입사각은 0(degree)이 되고 마이크로렌즈(33)의 가장자리 부분으로 입사될 때의 입사각은 33.5(degree)가 된다. 이렇게 단위화소의 포토다이오드(PD) 부분으로 입사광이 전파되어 입사되며, 최종 포토다이오드(PD)로 입사되는 입사광의 입사각도가 포토다이오드(PD)에로의 입사광 조도를 결정하게 된다.

따라서, 이미지센서에서 포토다이오드(PD)로 최종 입사되는 입사각도는 37 (degree)가 된다. 그러므로 단위화소의 포토다이오드(PD)가 받아들일 수 있는 중심대비 주변의 상대 조도량은 $\cos^4(37)$ = "0.488" 이 된다. 다시말하면, 포토다이오드(PD) 중심에서의 조도가 100%이면 마이크로렌즈(33)의 가장자리에서 입사된 입사광이 포토다이오드(PD)로 입사될 때의 조도는 48,8% 로, 포토다이오드(PD)의 주변부에서는 약 51.2%의 광량이 손실되는 문제점이 있다.

발명이 이루고자 하는 기술적 과제

본 발명은 상기의 문제점을 해결하기 위해 안출한 것으로서, 포토다이오드와 최초 층간절연막 사이에 흡수율이 낮은 유전층을 추가로 증착하므로써 입사광의 조도를 향상시켜 양자효율 및 광감도를 개선하는데 적합한 이미지센서의 제조 방법을 제공함에 그 목적이 있다.

발명의 구성 및 작용

상기의 목적을 달성하기 위한 본 발명의 일실시예에 따른 이미지센서 제조 방법은 기판에 포토다이오드영역 및 주변소자를 형성하는 제 1 단계, 상기 포토다이오드영역 상부에 굴절율 $N_X = \sqrt{N_o N_n}$ 이고 두께 $T_x = (2n-1)\frac{\lambda}{4N_x}\ [n = 0,1,2,3,\ldots]$ 인 제1절연층을 형성하는 제 2 단계, 상기 포토다이오드영역의 상부에만 남도록 상기 제1절연층을 제거하는 제 3 단계, 상기 결과물 상에 제2절연층을 형성하는 제 4 단계를 포함하여 이루어짐을 특징으로 한다.

이하, 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 본 발명의 기술적 사상을 용이하게 실시할 수 있을 정도로 상세히 설명하기 위하여, 본 발명의 가장 바람직한 실시예를 첨부 도면을 참조하여 설명하기로 한다.

첨부도면 도 3a 내지 도 3f는 본 발명의 실시예에 따른 이미지센서의 단위화소 제조 방법을 나타낸 공정단면로서, 본 발명의 이미지센서의 단위화소는 통상의 단위화소와 동일한 구조를 갖는다.

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도 3a에 도시된 바와 같이, 실리콘기판(41)에 웰 형성을 위한 마스크공정을 실시하고 보론이온을 주입한 다음, 열공정을 실시하여 측면확산(Lateral diffusion)에 의한 P형 웰(42)을 형성한다. 여기서 상기 P형 웰(42)은 셀렉트트랜지스터(Sx)와 드라이브트랜지스터(Dx)가 형성되는 영역이다.

이어 단위화소간의 분리막 필드절연막(43)을 형성한 후 게이트산화막(44)을 형성하고 상기 게이트산화막(44) 상부에 단위화소 내 트랜지스터들의 게이트전극을 형성하기 위해 폴리실리콘(45)과 텅스텐실리사이드막(46)을 연속적으로 형성하고 마스크 및 식각 공정을 통해 다수의 게이트전극을 형성한다. 여기서 상기 다수의 게이트전극들은 각각 트랜스퍼트랜지스터(Tx), 리셋트랜지스터(Rx), 드라이브트랜지스터(Dx), 셀렉트트랜지스터(Sx)의 게이트전극으로 이용된다.

이어 상기 결과물 상부에 포토다이오드(PD)를 형성하기 위한 마스크 공정을 실시하고 N^- 도핑영역과 P^0 도핑영역을 형성하기 위한 N^- 이온주입과 P^0 이온주입을 트랜스퍼트랜지스터(Tx)의 게이트전극 일측면에서 자기정렬하도록 실시한다. 이 때 상기 P형 기판(41), N^- 도핑영역(47a) 및 P^0 도핑영역(47b)은 PNP구조의 포토다이오드(47)를 형성한다.

이어 드라이브트랜지스터(Dx)와 셀렉트트랜지스터(Sx)의 N형 LDD(Lightly Doped Drain) 이온주입을 위한 마스크 패턴을 형성하고 보론이온을 주입하여 LDD영역 (49a)을 형성한다.

이어 트랜지스터들의 소오스/드레인 영역을 형성하기 위해 저압화학적기상증착법(Low Pressure Chemical Vapor Deposition; LPCVD)을 이용하여 저압산화막(LP- Oxide)을 증착하고 전면식각하여 게이트전극의 측벽에 접하는 산화막스페이서(50)를 형성한 후, 고농도 N형 불순물 이온을 위한 마스크패턴을 형성하여 N형 불순물 이온주입을 실시하여 불순물접합층들(49b)을 형성한다.

도 3b에 도시된 바와 같이, 상기 결과물 상부 특히 포토다이오드(PD)의 상부에 버퍼유전층(51)을 형성한다.

이 때 버퍼유전층(51)은 가시광선영역인 450~ 635nm 범위에 대하여 2.25~ 2.65의 굴절율을 갖는 유전층, 425~ 2113Å 의 두께를 갖는 유전층 또는 가시광의 흡수가 없는 물질 예를 들면, 실리콘이 다수 함유된 산화막(Silicon- rich Oxide), 옥시나이트라이드(Oxynitride) 또는 실리콘나이트라이드(Silicon nitride)를 포함하는 유전층 중 하나를 이용한다. 상기의 버퍼유전층(51)은 상기 포토다이오드(PD)로 입사되는 입사광의 조도를 증가시킨다.

이어 상기 버퍼유전층(51) 상부에 감광막을 도포하고 노광 및 현상으로 패터닝한 다음, 상기 패터닝된 감광막을 마스크로 하여 상기 포토다이오드영역을 제외한 부분의 버퍼유전층(51)을 습식 또는 건식식각한다.

도 3c에 도시된 바와 같이, 상기 결과물 상부에 저압화학적기상증착법 (LPCVD)으로 제1TEOS(TetraEthylOrthoSilicate)막(52a)을 증착한 후, 상기 제1TEOS막(52a) 상에 상압화학적기상증착법(Atmospheric Pressure CVD; APCVD)을 이용하여 BPSG막(52b)을 증착한다. 이어 열처리를 실시하여 상기 BPSG막(52b)을 리플로우시킨다. 여기서 상기 제1TEOS막(52a) 및 BPSG막(52b)을 PMD(Premetal Dielectric Layer)(53)라 한다.

이어 상기 PMD(53) 상에 마스크공정을 거쳐 완충산화막식각용액(BOE)을 이용하여 등방성식각을 하고 플라즈마식각공정을 이용한 비등방성식각을 진행하여 상기 접합층들(49b)의 표면에 콘택홀을 형성한다. 이어 상기 콘택홀을 포함한 전면에 티타늄/알루미늄/티타늄나이트라이드(Ti/Al/TiN)(54,55,56)를 순서대로 증착한다음 마스크공정과 식각공정을 하여 제1금속배선(57)을 형성한다.

도 3d에 도시된 바와 같이, 상기 제1금속배선 상부에 플라즈마화학적기상증착법(Plasma Enhanced CVD; PECVD)을 이용하여 제2TEOS산화막(58)을 증착한 다음, SOG(Spin On Glass)산화막(59)을 두 번 도포하여 형성하고 열처리 및 플라즈마를 이용한 전면식각으로 평탄화한다. 이어 상기 평탄화된 SOG산화막(59) 상부에 플라즈마화학적기상증착(PECVD)법을 이용하여 층간절연막(60)을 증착한다.

도 3e에 도시된 바와 같이, 마스크공정을 거쳐 상기 층간절연막(60)을 완충산화막식각용액(BOE)으로 등방성식각하고

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플라즈마를 이용한 비등방성식각을 진행하여 제2금속배선을 위한 콘택홀을 형성한다. 이어 상기 콘택홀을 포함한 결과물 상부에 티타늄/알루미늄/티타늄나이트라이드(54a,55a,56a)를 순서대로 증착한 다음, 마스크공정과 식각공정을 하여 제2금속배선(61)을 형성한다. 이어 상기 제2금속배선(61) 상부에 플라즈마화학적기상증착법(PECVD)을 이용하여 소자보호막(63)으로서 산화막(62a) 및 질화막(62b)을 증착한다.

도 3f에 도시된 바와 같이, 패드오픈(Pad open)을 위해 상기 질화막(62b) 및 산화막(62a)을 선택적으로 제거하여 상기 제2금속배선(61)의 소정 표면을 노출시킨다. 이어 상기 패드오픈지역과 단위화소 상부에 컬러물질(Dyed photoresistor;이하 컬러감광막)을 도포하고 현상공정으로 컬러필터(64)를 형성한다. 이어 상기 컬러필터(64) 상부에 마이크로렌즈의 균일한 형성을 위하여 마이크로렌즈평탄층(65)을 형성한 후 상기 마이크로렌즈평탄층(65) 상부에 마이크로렌즈(66)를 형성한다.

이와 같이 본 발명에서는 PMD 형성 전 포토다이오드(PD) 상부에 2.25~ 2.65의 굴절율을 가지며 425~ 2113Å 의 두께를 갖는 유전층을 형성하여 포토다이오드로 입사되는 입사광의 조도를 증가시킬 수 있다. 즉 입사광의 조도는 유전층의 굴절율과 두께에 의존한다.

상기 유전층 굴절율(Nx)은,

$$N_x = \sqrt{N_o N_s}$$

이고, 또한 상기 유전층의 두께(Tx)는,

$$T_x = (2n-1)\frac{\lambda}{4N_x} \quad [n=0,1,2,3,\ldots]$$

이다. 이 때 상기 N_O는 후속공정에서 형성되는 PMD의 굴절율(="1.48~ 1.46)이고," N_S는 기판(41)의 굴절율(="4.72~ 3.48)이다.

이와 같이 흡수율이 낮은 버퍼유전층을 추가로 증착하면 입사광의 가시광선영역대에서 포토다이오드의 중심부 대비 주변부의 상대 조도량을 약 50% 향상시킬 수 있다. 예를 들면 λ ="635nm," Nx="2.261," Tx="700Å " 조건으로 증착된 버퍼유전층은 중심 대비 주변의 상대 조도량이 71.9%로 입사광의 조도를 현저히 향상시킬 수 있다.

본 발명의 기술 사상은 상기 바람직한 실시예에 따라 구체적으로 기술되었으나, 상기한 실시예는 그 설명을 위한 것이며 그 제한을 위한 것이 아님을 주의하여야 한다. 또한, 본 발명의 기술 분야의 통상의 전문가라면 본 발명의 기술 사상의 범위 내에서 다양한 실시예가 가능함을 이해할 수 있을 것이다.

발명의 효과

상술한 본 발명은 통상의 CMOS 및 CCD 이미지센서의 제조공정을 적용하고 포토다이오드 상부에 버퍼유전층을 형성하여 입사광에 대한 포토다이오드의 중심부 대비 주변부의 상대 조도량을 증가시키므로써 이미지센서의 양자효율 및 광감도를 향상시킬 수 있는 효과가 있다.

(57) 청구의 범위

청구항 1.

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이미지센서 제조 방법에 있어서,

기판에 포토다이오드영역 및 주변소자를 형성하는 제 1 단계;

상기 포토다이오드영역 상부에 굴절율 $N_X=\sqrt{N_o N_.}$ 이고 두께 $T_x \ (2n-1)\frac{\lambda}{4N_x}$ $(n=0,1,2,3,\ldots)$ 인 제1절연층을 형성하는 제 2 단계;

상기 포토다이오드영역의 상부에만 남도록 상기 제1절연층을 제거하는 제 3 단계; 및

상기 결과물 상에 제2절연층을 형성하는 제 4 단계

를 포함하여 이루어짐을 특징으로 하는 이미지센서 제조 방법.

청구항 2.

제 1 항에 있어서,

상기 제 4 단계 후,

상기 결과물 상부에 금속배선 및 소자보호막을 형성하는 제 5 단계를 포함하여 이루어지며,

상기 결과물 상부에 컬러필터와 마이크로렌즈를 형성하는 제 6 단계를 더 포함하여 이루어짐을 특징으로 하는 이미지센서 제조 방법.

청구항 3.

제 1 항에 있어서,

상기 제 2 단계에서,

상기 제1절연층은 425~ 2113Å 의 두께인 것을 특징으로 하는 이미지센서 제조 방법.

청구항 4.

제 1 항에 있어서,

상기 제 2 단계에서,

상기 제1절연층은 2.25~ 2.65의 굴절율인 것을 특징으로 하는 이미지센서 제조 방법.

청구항 5.

제 1 항에 있어서,

상기 제 2 단계에서,

상기 제1절연층으로 무반사층을 이용함을 특징으로 하는 이미지센서 제조 방법.

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청구항 6.

제 1 항에 있어서,

상기 제 2 단계에서,

상기 N_O는 상기 제2절연층의 굴절율이고, 상기 N_S는 상기 기판의 굴절율인 것을 특징으로 하는 이미지센서 제조 방법.

청구항 7.

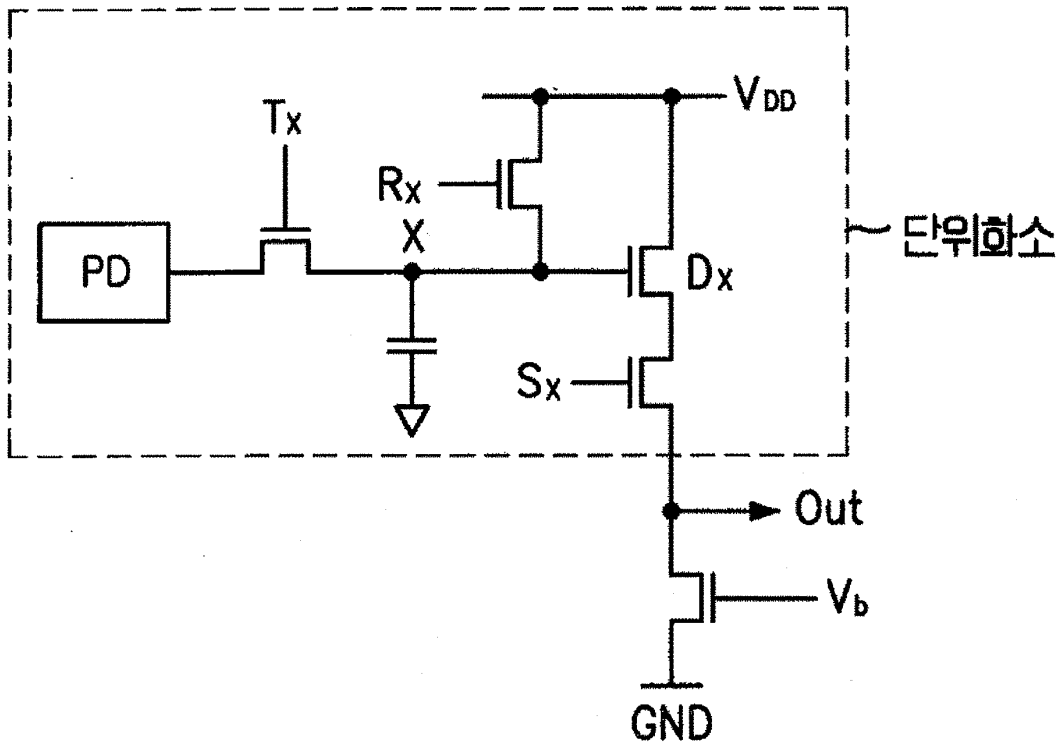
제 1 항에 있어서,

상기 제 2 단계에서,

상기 제1절연층은 실리콘이 다량 함유된 산화막, 옥시나이트라이드 또는 실리콘나이트라이드 중 어느 하나를 이용함을 특징으로 하는 이미지센서 제조 방법.

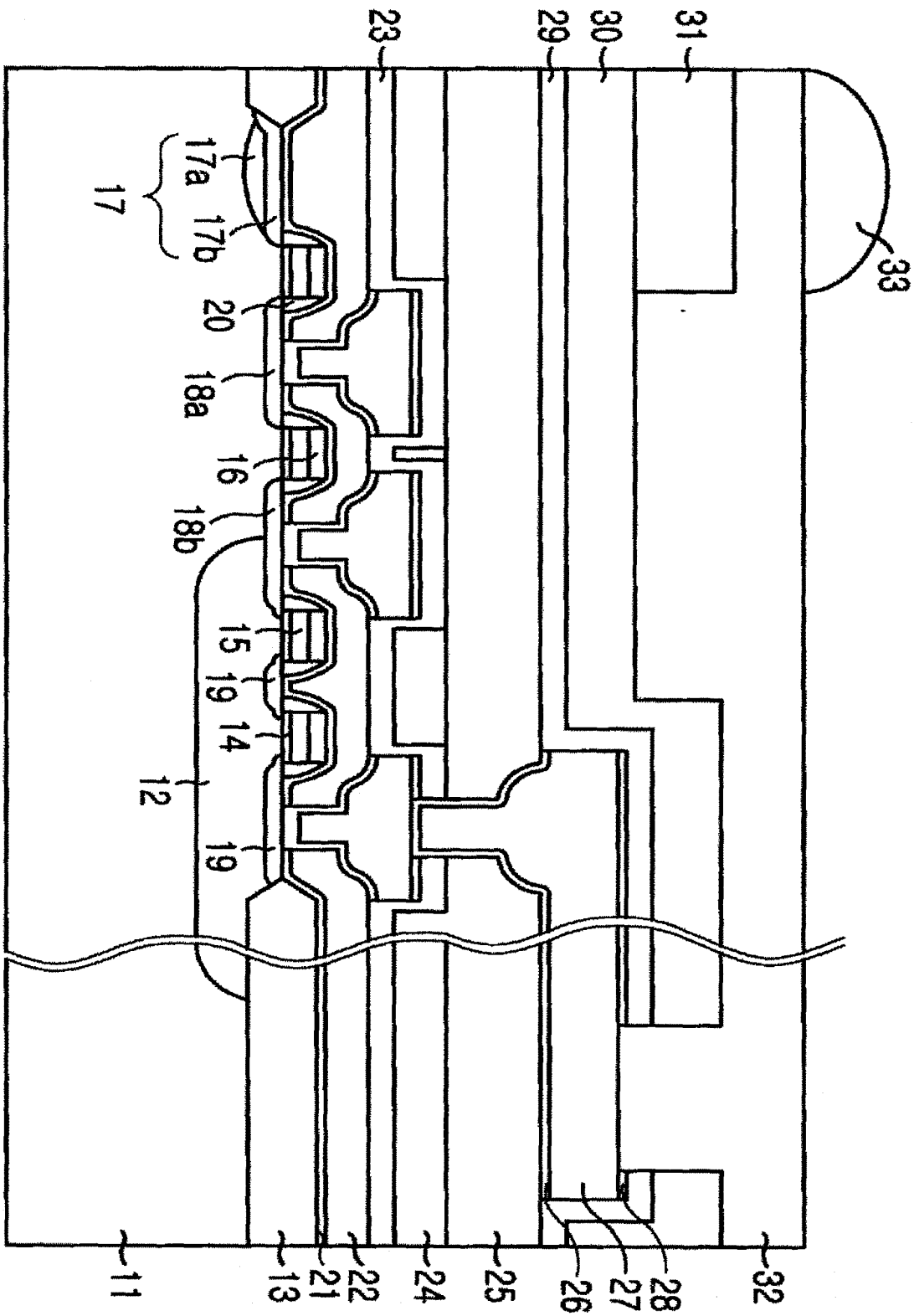
도면

도면 1



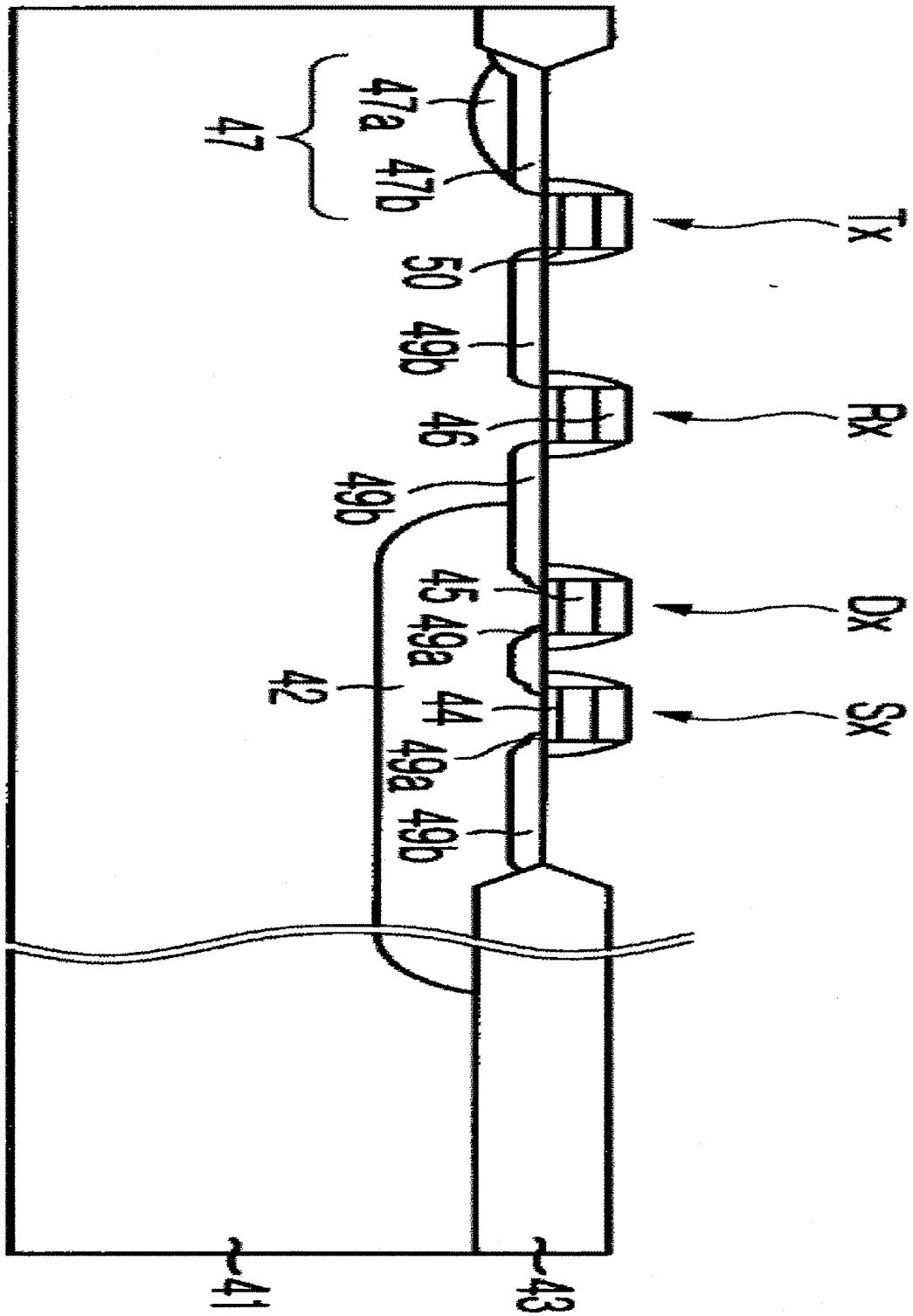
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도면 2



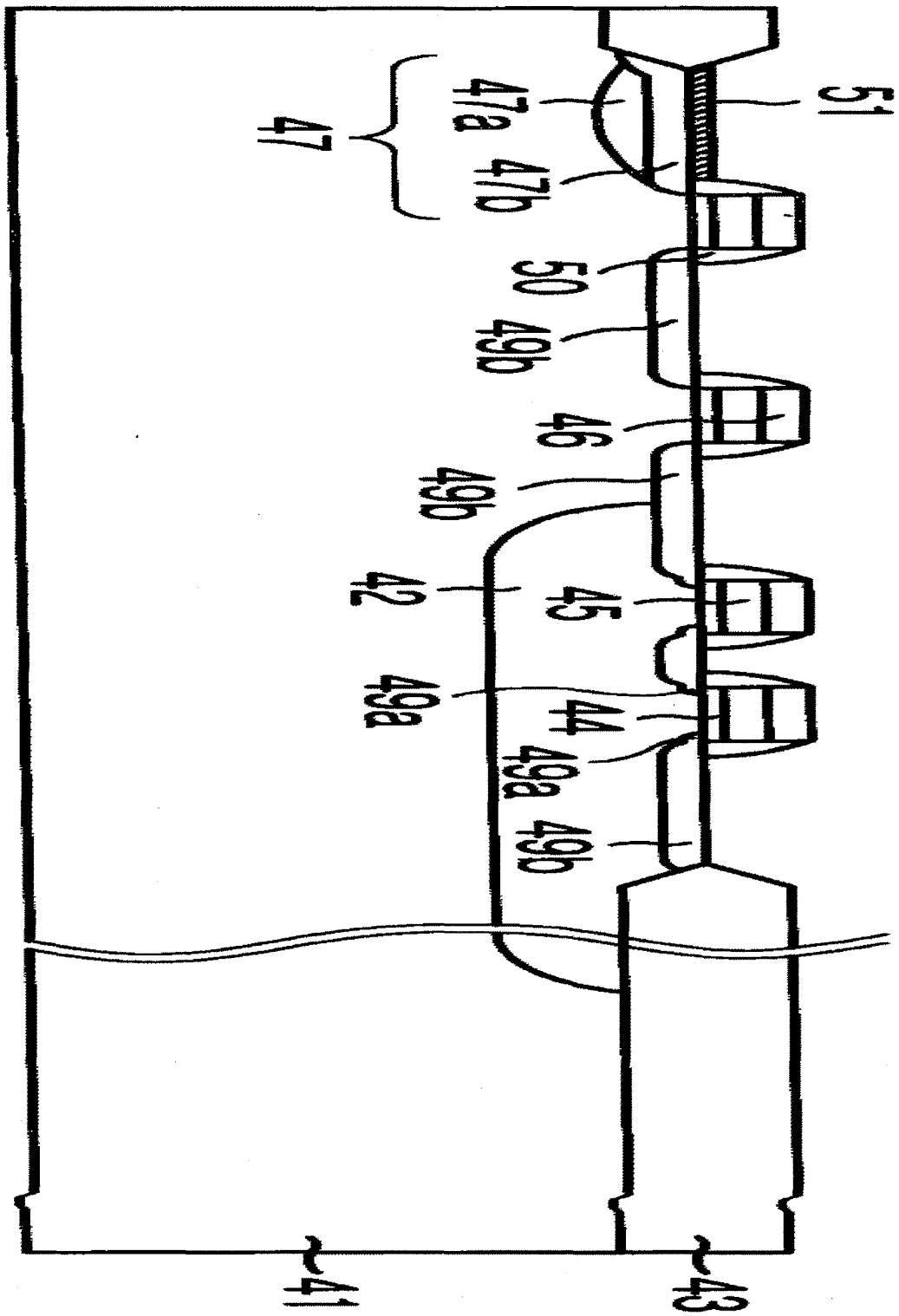
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도면 3a



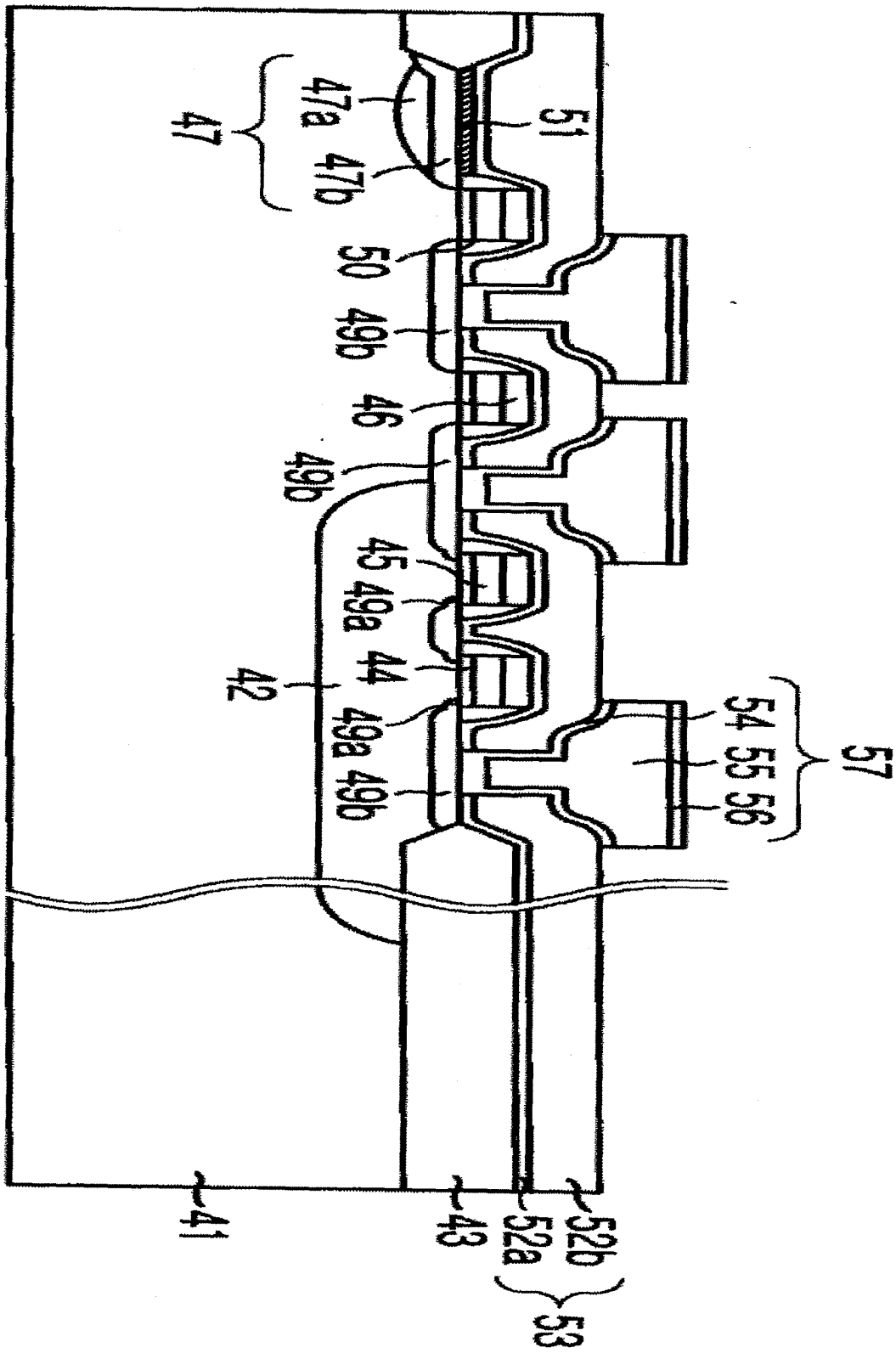
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도면 3b



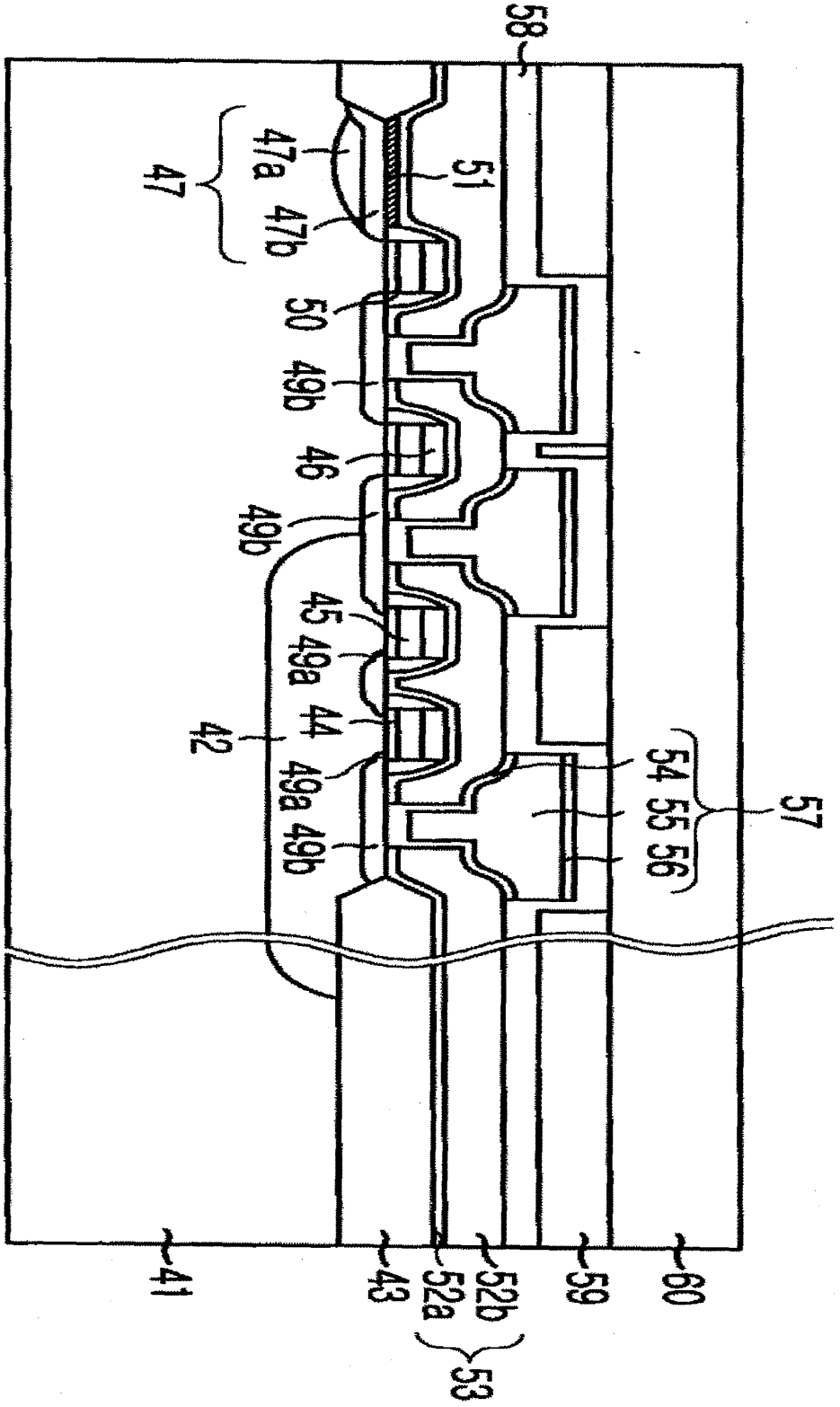
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도면 3c



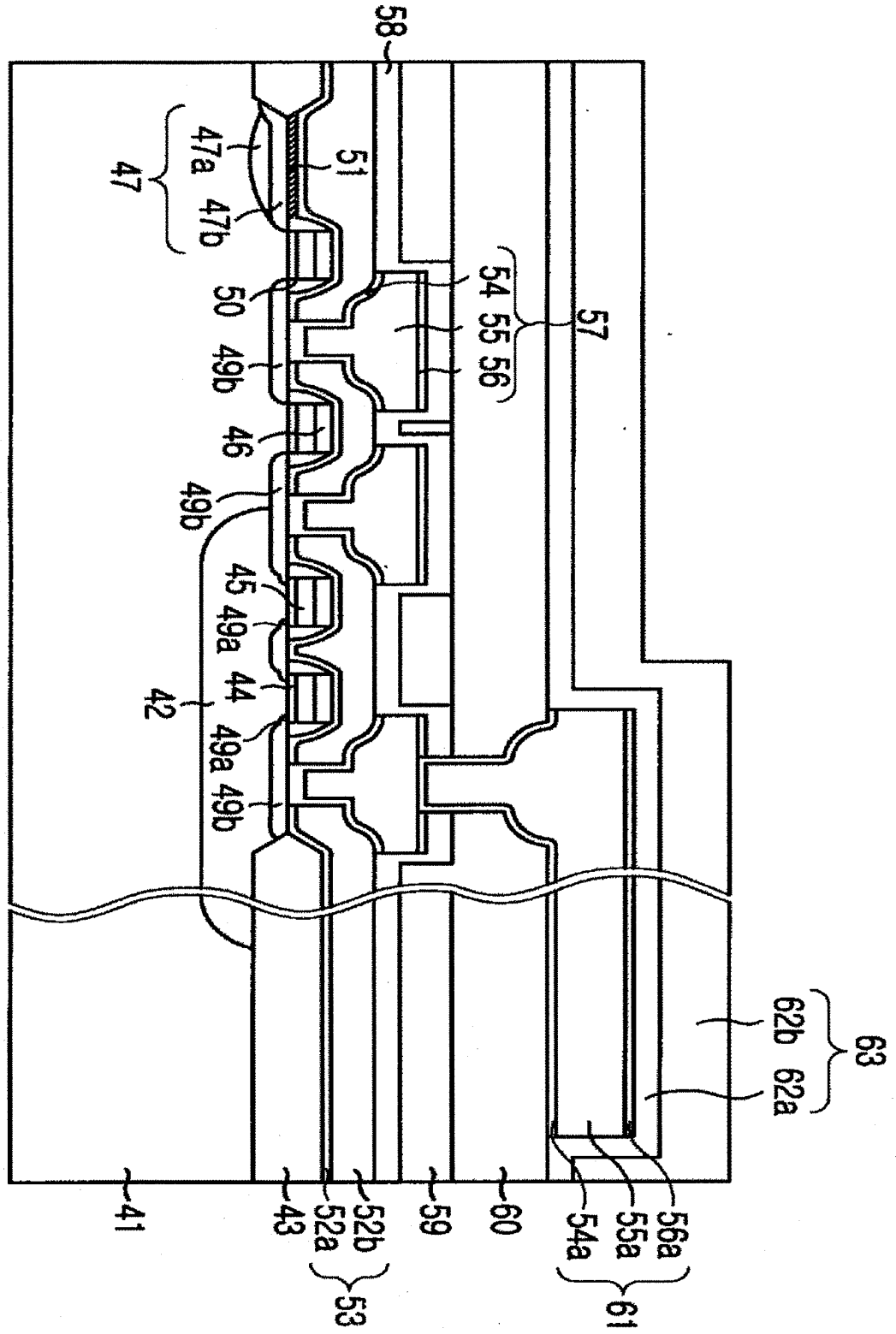
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도면 3d



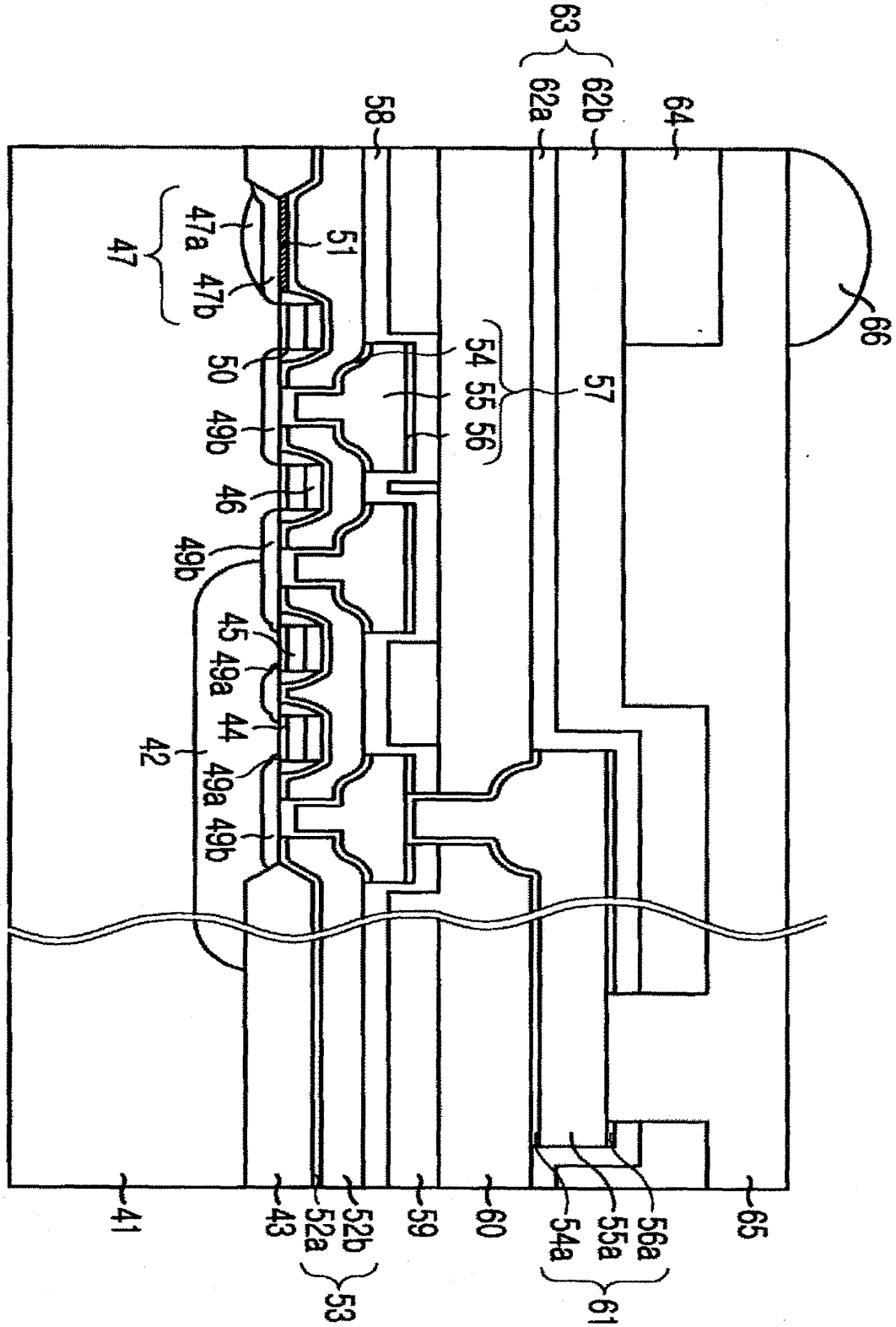
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도면 3e



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도면 3f



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A FABRICATING METHOD OF BURIED CONTACT SOLAR CELL

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Abstract of KR20100118864 (A)

PURPOSE: A method for manufacturing a buried contact solar cell is provided to simplify solar cell manufacturing processes by forming a selective emitter layer through one doping process. CONSTITUTION: A mask layer(110) is formed on a semiconductor substrate(100). A part of the mask layer is eliminated. A groove(G) for forming an electrode is formed on a semiconductor substrate to correspond to the eliminated part of the mask layer. An emitter layer(120) is formed by doping dopants in the mask layer and the groove. An anti-reflection layer(130) is formed on the upper side of the emitter layer. A front electrode(142) is formed in the groove of the semiconductor substrate.

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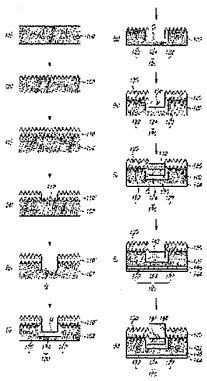
전체 청구항 수 : 총 11 항

(54) 함몰전극형 태양전지의 제조방법

(57) 요 약

본 발명은 함몰전극형 태양전지의 제조방법에 관한 것이다. 본 발명에서는 먼저 텍스처링된 실리콘 기판(102)의 상부 전체 면적에 형성된 마스크 층(110)의 일부분을 제거하여 패터닝된 마스크 층(110')을 형성한다. 그런 다음 텍스처링된 실리콘 기판(102) 상에 전면전극용 홈(G)을 형성하기 위해 식각공정을 수행한다. 이때 텍스처링된 실리콘 기판(102)의 일부(112)에 대해서만 식각이 이루어지고, 상기 패터닝된 마스크 층(110')과 접하는 부분에 대해서는 식각이 되지 않는다. 상기 식각공정에 따라 전면전극용 홈(G)이 형성된 다음에는 도핑공정을 수행한다. 이때 상기 도핑공정 시 상기 형성된 홈(G)의 주위는 고농도로 도핑되고, 상기 패터닝된 마스크 층(110')과 접하는 부분은 저농도로 도핑된다. 즉, 한 번의 도핑공정으로 선택적 에미터(selective emitter) 층(120)이 형성되는 것이다. 그리고 상기 패터닝된 마스크 층(110')을 제거하고, 상기 형성된 선택적 에미터 층(120) 상부에 반사방지막(130)을 형성한다. 그런 다음 상기 텍스처링된 실리콘 기판(102)의 전면에 형성된 홈(G)에는 전면전극(142)을 형성하고 후면 전체 면적에는 후면전극(144)을 형성한다. 이와 같은 본 발명에 의하면, 일반적인 식각공정에 의해 전면전극용 홈을 형성할 수 있고, 선택적 에미터 층을 한 번의 공정으로 형성할 수 있어 전체 공정을 간소화할 수 있는 이점이 있다.

대 표 도 - 도3



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특허청구의 범위

청구항 1

반도체 기판의 상부 전체 면적에 마스크 층을 형성하는 마스크 층 형성단계;

상기 형성된 마스크 층의 일부분을 제거하는 마스크 층 패터닝단계;

상기 제거된 마스크 층의 일부분과 대응하는 상기 반도체 기판에 전극형성용 홈(Groove)을 형성하는 홈 형성단계;

상기 마스크 층 및 홈에 불순물을 도핑하여 에미터 층을 형성하는 에미터 층 형성단계;

상기 에미터 층이 형성되면, 상기 마스크 층의 나머지 부분과 부산물을 동시에 제거하는 마스크 층 제거단계;

상기 형성된 에미터 층 상부에 반사방지막을 형성하는 반사방지막 형성단계;

상기 반도체 기판에 형성된 홈에는 전면전극을 형성하고 후면의 전체 면적에는 후면전극을 형성하는 전극 형성단계; 그리고

상기 형성된 전면전극 및 후면전극이 상기 반도체 기판에 전기적으로 연결되도록 열처리하는 열처리단계;를 포함하는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 2

제 1항에 있어서,

상기 반도체 기판을 텍스처링(Texturing)하는 텍스처링 공정단계가 상기 마스크 층 형성단계 이전에 수행되는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 3

제 1항 또는 제 2항에 있어서, 상기 마스크 층 형성단계는,

화학증착(Chemical Vapor Deposition: CVD), 증류(evaporation), 스퍼터링(sputtering), 스핀 코팅(Spin Coating), 잉크젯(Inkjet), 스크린 프린팅, 열 산화(thermal oxidation) 방법 중 어느 하나에 의해 실시되는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 4

제 1항에 있어서, 상기 마스크 층 패터닝단계에서,

상기 마스크 층은, 광식각(Photo-lithography) 방법, 식각 페이스트(Etching Paste)를 이용한 잉크젯(Inkjet) 또는 스크린 프린팅 방법, 레이저를 이용한 패터닝(Laser ablation) 방법 중 어느 하나에 의해 패터닝되는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 5

제 1항에 있어서, 상기 마스크 층 패터닝단계는,

상기 텍스처링된 반도체 기판의 상부에 상기 마스크 층을 미형성한 상태에서, 일정 모양으로 패터닝된 마스크 층을 상기 반도체 기판 상부에 직접 형성하고,

상기 패터닝된 마스크 층은 잉크젯(Inkjet) 방법 또는 스크린 프린팅 방법 중 어느 하나를 이용하여 형성됨을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 6

제 4항에 있어서,

상기 마스크 층은, 디퓨전 배리어(Diffusion Barrier)로 사용가능한 Oxide 계열 또는 Nitride 계열의 유전체 물질, 페이스트(Paste), 유기물 중 어느 하나의 물질로 형성되는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

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청구항 7

제 1항에 있어서, 상기 홈 형성단계는,

반응성 이온 식각(Reactive Ion Etching: RIE), 플라즈마 식각(Plasma Etching), 습식식각(Wet Etching) 방법 중 어느 하나에 의해 상기 반도체 기판에만 선택적으로 식각공정이 실시되는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 8

제 7항에 있어서,

상기 반응성 이온 식각(Reactive Ion Etching: RIE) 또는 플라즈마 식각(Plasma Etching) 방법이 실시되는 경우, F 계열 또는 Cl 계열의 반응 가스를 이용하는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 9

제 8항에 있어서,

상기 습식식각 방법이 실시되는 경우에는 산(Acid) 계열의 화학물질 또는 알카라인(Alkaline) 계열의 화학물질을 이용하는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 10

제 1항에 있어서, 상기 에미터 층 형성단계에서,

상기 일부분이 제거된 마스크 층은 디퓨전 배리어로 이용되어 상기 일부분이 제거된 마스크 층과 접하는 반도체 기판은 저농도로 도핑되고, 상기 반도체 기판에 형성된 홈 주위는 상대적으로 고농도로 도핑되는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

청구항 11

제 1항 또는 제 10항에 있어서,

상기 에미터 층 형성단계는, 튜브 퍼니스(tube furnace)를 이용한 디퓨전(Diffusion) 방법 또는 벨트 퍼니스(belt furnace)를 이용한 디퓨전(Diffusion), 스프레이(Spray), SOD(Spin On Dopant), 플라즈마 도핑(Plasma Doping) 방법 중 어느 하나에 의해 실시되는 것을 특징으로 하는 함몰전극형 태양전지의 제조방법.

명 세 서

발명의 상세한 설명

기 술 분 야

[0001] 본 발명은 태양전지에 관한 것으로, 특히 반도체 기판 표면에 홈(Groove)을 내고 홈 안에 전극을 형성하는 함몰전극형 태양전지의 제조방법에 관한 것이다.

배 경 기 술

[0002] 최근 석유나 석탄과 같은 기존 에너지 자원의 고갈이 예측되면서 이들을 대체할 대체 에너지에 대한 관심이 높아지고 있다. 그 중에서도 태양전지는 에너지 자원이 풍부하고 환경오염에 대한 문제점이 없어 특히 주목받고 있다. 태양전지에는 태양열을 이용하여 터빈을 회전시키는데 필요한 증기를 발생시키는 태양열 전지와, 반도체의 성질을 이용하여 태양빛(photons)을 전기에너지로 변환시키는 태양광 전지가 있으며, 태양전지라고 하면 일반적으로 태양광 전지(이하 '태양전지'라 함)를 일컫는다.

[0003] 상기 태양전지는 반도체의 광 기전력 효과를 이용한 것으로서, p형 반도체와 n형 반도체를 조합하여 만든다. p형 반도체와 n형 반도체가 접한 부분(pn 접합부)에 빛이 들어오면, 빛 에너지에 의하여 반도체 내부에서 마이너스의 전하(전자)와 플러스의 전하(정공)가 발생한다. 상기 빛 에너지에 의해 발생된 전자와 정공은 내부의

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전계에 의하여 각각 n형 반도체측과 p형 반도체측으로 이동하여 양쪽의 전극부에 모아진다. 이러한 두 개의 전극을 도선으로 연결하면 전류가 흐르고 외부에서 전력으로 이용할 수 있게 된다.

[0004] 이러한 태양전지는 전극의 형태에 따라 스크린 프린팅형 태양전지(Screen Printing Solar Cell: 이하 'SPSC'라 약칭함)와 함몰전극형 태양전지(Buried Contact Solar Cell: 이하 'BCSC'라 약칭함)로 구분할 수 있다.

[0005] 상기 'SPSC'는 일반적으로 제조하기가 용이하지만 에너지 변환 효율이 낮은 편이다. 이는 금속 전극에서의 반사, 후면 전류 흐름에서 기인된 저항 및 일반적으로 깊게 도핑되어 있는 에미터 영역에서의 캐리어들의 높은 재결합률 때문이다. 또한 상기와 같은 이유로 'SPSC'에서는 단락회로전류밀도와 블루우 리스폰스(blue response) 특성이 불량하다.

[0006] 반면, 상기 'BCSC'는 상기 'SPSC'에 비해 제조 원가가 비싸고 공정이 복잡한 단점이 있으나, 변환 효율을 획기적으로 향상시킬 수 있는 장점으로 인해 최근에는 'BCSC'에 대한 많은 연구가 이루어지고 있다.

[0007] 도 1에는 일반적인 'BCSC'의 제조공정도가 도시되어 있다. 설명의 편의상 'BCSC'의 제조 재료인 반도체 기판으로서, 결정질 실리콘(Si) 기판을 예로 들어 설명한다.

[0008] 도 1을 설명하면, 먼저 실리콘 기판을 필요한 크기로 자른 뒤 절단시 발생한 실리콘 기판의 표면 결함이나 손상 부분을 제거하는 절단 및 에칭(Saw damage etching) 공정이 수행된다(S10).

[0009] 상기 에칭공정을 마친 실리콘 기판에 대해 반응성 이온 식각(Reactive Ion Etching:RIE) 방법 또는 습식 식각(Wet Etching) 방법을 이용하여 텍스처링(Texturing) 공정을 수행한다(S12). 상기 텍스처링 공정이 수행되면 상기 실리콘 기판의 전면은 입사되는 빛의 반사를 감소시키는 구조로 형성된다.

[0010] 상기 텍스처링 공정된 실리콘 기판과 다른 타입의 불순물(도펀트)을 도핑하여 저농도 에미터층을 형성하는 제1도핑공정이 수행된다(S14). 여기서, 만약 상기 에미터층이 고농도로 도핑되어 형성되는 경우, 표면에 존재하는 고농도의 도펀트들이 실리콘 기판 내에 과잉으로 존재함으로써 응집물이 형성되고, 이로 인해 전하의 수명이 감소되어 태양전지의 작동효율이 저하될 수 있다. 그렇기 때문에 저농도의 에미터층을 형성하는 것이다.

[0011] 상기 저농도 에미터층이 형성된 다음에는 상기 저농도 에미터층 형성시 발생하는 부산물을 제거하는 제1부산물 제거공정이 수행된다(S16). 상기 부산물은, p형 기판에 n형 도펀트를 확산시키는 경우 생성되는 PSG(Phosphor-Silicate Glass) 또는 n형 기판에 p형 도펀트를 확산시키는 경우 생성되는 BSG(Boro-Silicate Glass)를 말한다. 상기 PSG 또는 BSG는 전지의 전류를 차폐시키는 역할을 하기 때문에 전지효율을 높이기 위해서 식각용액 등을 이용하여 반드시 제거해 주어야 한다.

[0012] 상기 부산물이 제거되면, 상기 에미터층 상부에 태양광 반사를 막기 위한 반사방지막을 형성시키는 공정이 수행된다(S18). 상기 반사방지막은 실리콘 기판의 표면 보호막(Passivation) 역할도 한다.

[0013] 상기 반사방지막이 형성된 다음에는 실리콘 기판의 전면 내부까지 홈(Groove)를 형성시키는 공정이 수행된다(S20). 상기 홈은, 함몰전극(Buried Contact)이 형성될 공간으로, 레이저(Laser) 또는 절단톱(Dicing Saw)을 이용하여 형성된다.

[0014] 상기 홈이 형성되면 상기 함몰전극과의 접촉저항을 줄이기 위해 홈 표면에 실리콘 기판과 다른 타입의 불순물을 도핑하여 고농도 에미터층을 형성하는 제2도핑공정을 수행한다(S22). 이와 같이, 상기 제1도핑공정과 제2도핑공정을 통해 서로 다른 농도를 가지는 에미터층을 형성하는 것을 선택적 에미터(selective emitter)로 칭하고 있다.

[0015] 상기 고농도 에미터층이 형성된 다음에는 상기 고농도 에미터층 형성시 발생하는 부산물을 제거하는 제2부산물 제거공정이 수행된다(S24). 상기 부산물은 상술하였듯이, PSG 또는 BSG를 말한다.

[0016] 이어서, 상기 실리콘 기판의 전면에 형성된 홈 내부 및 후면의 모든 부분에 금속 페이스트를 사용하여 전극을 형성하는 공정이 수행된다(S26). 상기 금속 페이스트는 은(Ag), 알루미늄(Al) 등이 이용될 수 있다. 이때에는 스크린 프린팅 기법 등이 적용된다. 상기 전면에 형성된 전극은 태양광 흡수로 생성된 전자를 수집하는 역할을 하고, 후면에 형성된 전극은 실리콘 기판 후면에서의 광 반사를 높이고 전자의 재결합을 방지하는 역할을 한다.

[0017] 상기 전·후면에 형성된 전극이 실리콘 기판에 전기적으로 연결되도록 열처리 공정을 수행한다(S28). 이때, 상기 실리콘 기판의 후면에는 상기 금속 페이스트가 상기 열처리 공정에 의해 소정의 두께만큼 확산되어 후면 전계층(Back Surface Field: BSF)을 형성한다. 상기 'BSF'는 전계를 형성하여 광여기된 전자가 실리콘 기판의 후

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면으로 이동하는 것을 방지하는 역할을 한다.

[0018] 한편, 상기 형성된 전면 전극은 그 자체로 전면 전극 기능을 수행할 수도 있지만, 시드층(seed layer)으로도 사용될 수 있다. 이 경우 상기 형성된 전면 전극 상에 도금층을 형성하는 공정이 추가로 실시될 수 있다(S30). 이는 상기 전면 전극의 저항을 감소시키고 완성된 'BCSC' 기판의 종횡비를 높일 수 있다.

[0019] 그러나, 종래의 'BCSC'의 제조방법에는 다음과 같은 문제점이 있다.

[0020] 먼저, 레이저(Laser) 또는 절단톱(Dicing Saw)을 이용하여 홈을 형성하는 경우에는 실리콘 기판에 물리적인 손상을 유발시킬 수 있다. 특히 레이저(Laser)를 이용하여 홈을 형성하는 경우에는 높은 온도로 인해 기판 표면과 내부에 재결정 현상이 발생한다. 이는 빛을 흡수하여 생성된 전자를 재결합시키는 요인이 되어 표면 재결합 속도를 증가시키고 전자의 라이프 타임(life time)을 감소시키는 문제점이 있다.

[0021] 다음으로, 상기 선택적 에미터층을 형성하기 위해서는 제1 및 제2도핑공정을 반드시 수행하여야 한다. 이는 선택적 에미터층을 형성 시 공정이 복잡하고, 이에 따라 공정 비용이 증가하는 문제점이 있다.

[0022] 또한, 통상적으로, 도핑공정은 불순물을 실리콘 기판에 디퓨전시키기 위해 열처리공정을 수행하게 되는데, 이러한 고온의 열처리공정은 실리콘 기판의 품질을 저하시키는 원인으로 작용한다. 그런데, 상기 'BCSC'는, 상술한 바와 같이 제1 및 제2도핑공정을 수행하고 있어 실리콘 기판의 품질을 더욱 저하시키는 문제점이 있다.

발명의 내용

해결 하고자하는 과제

[0023] 따라서 본 발명의 목적은 상기한 문제점을 해결하기 위한 것으로서, 캐리어의 라이프 타임(life time)이 감소되는 것을 방지하면서도 선택적 에미터의 형성공정을 간소화하기 위한 함몰전극형 태양전지의 제조방법을 제공하는 것이다.

과제 해결수단

[0024] 상기한 바와 같은 목적을 달성하기 위한 본 발명의 특징에 따르면, 본 발명은 반도체 기판의 상부 전체 면적에 마스크 층을 형성하는 마스크 층 형성단계; 상기 형성된 마스크 층의 일부분을 제거하는 마스크 층 패터닝단계; 상기 제거된 마스크 층의 일부분과 대응하는 상기 반도체 기판에 전극형성용 홈(Groove)을 형성하는 홈 형성단계; 상기 마스크 층 및 홈에 불순물을 도핑하여 에미터 층을 형성하는 에미터 층 형성단계; 상기 에미터 층이 형성되면, 상기 마스크 층의 나머지 부분과 부산물을 동시에 제거하는 마스크 층 제거단계; 상기 형성된 에미터 층 상부에 반사방지막을 형성하는 반사방지막 형성단계; 상기 반도체 기판에 형성된 홈에는 전면전극을 형성하고 후면의 전체 면적에는 후면전극을 형성하는 전극 형성단계; 그리고 상기 형성된 전면전극 및 후면전극이 상기 반도체 기판에 전기적으로 연결되도록 열처리하는 열처리단계;를 포함한다.

[0025] 상기 반도체 기판을 텍스처링(Texturing)하는 텍스처링 공정단계가 상기 마스크 층 형성단계 이전에 수행된다.

[0026] 상기 마스크 층 형성단계는, 화학증착(Chemical Vapor Deposition: CVD), 증류(evaporation), 스퍼터링(sputtering), 스핀 코팅(Spin Coating), 잉크젯(Inkjet), 스크린 프린팅, 열 산화(thermal oxidation) 방법 중 어느 하나에 의해 실시된다.

[0027] 상기 마스크 층 패터닝단계에서, 상기 마스크 층은, 광식각(Photo-lithography) 방법, 식각 페이스트(Etching Paste)를 이용한 잉크젯(Inkjet) 또는 스크린 프린팅 방법, 레이저를 이용한 패터닝(Laser ablation) 방법 중 어느 하나에 의해 패터닝된다. 또는 상기 텍스처링된 반도체 기판의 상부에 상기 마스크 층이 미형성된 상태에서, 일정 모양으로 패터닝된 마스크 층을 상기 반도체 기판 상부에 직접 형성할 수도 있다. 여기서, 상기 패터닝된 마스크 층은 잉크젯(Inkjet) 방법 또는 스크린 프린팅 방법 중 어느 하나를 이용하여 형성된다.

[0028] 상기 마스크 층은, 디퓨전 배리어(Diffusion Barrier)로 사용가능한 Oxide 계열 또는 Nitride 계열의 유전체 물질, 페이스트(Paste), 유기물 중 어느 하나의 물질로 형성된다.

[0029] 상기 홈 형성단계는, 반응성 이온 식각(Reactive Ion Etching: RIE), 플라즈마 식각(Plasma Etching), 습식식각(Wet Etching) 방법 중 어느 하나에 의해 상기 반도체 기판에만 선택적으로 식각공정이 실시된다.

[0030] 상기 반응성 이온 식각(Reactive Ion Etching: RIE) 또는 플라즈마 식각(Plasma Etching) 방법이 실시되는 경우, F 계열 또는 Cl 계열의 반응 가스를 이용한다.

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[0031] 상기 습식식각 방법이 실시되는 경우에는 산(Acid) 계열의 화학물질 또는 알카라인(Alkaline) 계열의 화학물질을 이용한다.

[0032] 상기 에미터 층 형성단계에서, 상기 일부분이 제거된 마스크 층은 디퓨전 배리어로 이용되어 상기 일부분이 제거된 마스크 층과 접하는 반도체 기판은 저농도로 도핑되고, 상기 반도체 기판에 형성된 홈 주위는 상대적으로 고농도로 도핑된다.

[0033] 상기 에미터 층 형성단계는, 튜브 퍼니스(tube furnace)를 이용한 디퓨전(Diffusion) 방법 또는 벨트 퍼니스(belt furnace)를 이용한 디퓨전(Diffusion), 스프레이(Spray), SOD(Spin On Dopant), 플라즈마 도핑(Plasma Doping) 방법 중 어느 하나에 의해 실시된다.

효 과

[0034] 이와 같은 구성을 갖는 본 발명의 함몰전극형 태양전지의 제조방법에 따르면, 실리콘 기판의 전면에는, 마스크 층(Mask Layer)을 형성하고 패터닝한 다음 상기 패터닝된 마스크 층에 일반적인 식각공정을 이용하여 홈(Groove)을 형성함으로써, 레이저(Laser)를 이용하여 홈을 형성했을 때 발생하는 캐리어의 라이프 타임(life time) 감소 현상을 방지하는 효과가 있다.

[0035] 또 상기 패터닝된 마스크 층을 디퓨전 배리어(Diffusion Barrier)로 이용하여 한 번의 도핑공정을 통해 선택적 에미터(selective emitter) 층을 형성하는바, 태양전지 제조공정을 간소화할 수 있다. 그래서 공정 비용을 절감시키고, 결국 생산단가를 낮추는 효과를 기대할 수 있다.

발명의 실시를 위한 구체적인 내용

[0036] 이하, 본 발명에 의한 함몰전극형 태양전지의 제조방법을 첨부된 도면에 도시된 바람직한 실시 예를 참고하여 상세하게 설명한다. 본 발명의 실시 예에서는 태양전지의 제조 재료로 반도체 기판으로서, 결정질 실리콘(Si) 기판을 예로 설명하기로 한다.

[0037] 도 2에는 본 발명의 바람직한 실시 예에 따른 함몰전극형 태양전지의 제조공정도가 도시되어 있고, 도 3에는 도 2의 함몰전극형 태양전지의 제조방법의 공정도가 단면도로 도시되어 있다.

[0038] 도 2를 설명하면, 먼저 실리콘 기판을 필요한 크기로 자르고 표면의 결함 및 손상을 제거하는 절단 및 에칭(Saw damage etching) 공정이 수행된다(S100).

[0039] 상기 에칭된 실리콘 기판에 대해 반응성 이온 식각(Reactive Ion Etching:RIE) 방법 또는 습식 식각(Wet Etching) 방법을 이용하여 텍스처링(Texturing) 공정을 수행한다(S102). 상기 텍스처링 공정이 수행되면 상기 실리콘 기판은 표면에 입사되는 빛의 반사를 감소시키는 구조로 형성된다.

[0040] 상기 텍스처링 공정된 실리콘 기판의 전면 상부에 마스크 층(Mask Layer)을 형성시키는 공정이 수행된다(S104). 상기 마스크 층은, 상기 실리콘 기판과의 식각 선택비(Etching Selectivity)가 높으면서도 아래에서 설명하는 도핑공정에서 디퓨전 배리어(Diffusion Barrier)로 사용가능하게 형성되어야 한다. 그렇기 때문에, 상기 마스크 층은, SiO_2, SiN_x, TiO_2, Al_2O_3 등의 Oxide 계열 또는 Nitride 계열의 유전체 물질뿐만 아니라, 디퓨전 배리어(Diffusion Barrier)로 사용가능한 페이스트(Paste)와, 유기물 등이 사용되는 것이 좋다. 상기 식각 선택비는 식각 작업시 두 물질이 식각되는 식각율의 비를 말한다. 한편, 상기 마스크 층은 화학증착(Chemical Vapor Deposition: CVD), 증류(evaporation), 스퍼터링(sputtering), 스핀 코팅(spin coating), 잉크젯(Inkjet), 스크린 프린팅, 열 산화(thermal oxidation) 등의 방법에 의해 형성된다.

[0041] 상기 마스크 층이 형성되면, 상기 실리콘 기판의 전면 중 홈(Groove)이 형성될 부분에 해당하는 마스크 층의 일부분을 제거하는 패터닝(Patterning)공정이 수행된다(S106). 상기 패터닝공정은, 광식각(Photo-lithography) 방법, 식각 페이스트(Etching Paste)를 이용한 잉크젯(Inkjet) 또는 스크린 프린팅 방법, 레이저를 이용한 패터닝(Laser ablation) 방법 등에 의해 식각된다.

[0042] 여기서, 상기 패터닝된 마스크 층을 형성하는 공정에 있어, 상술한 바와 같이 상기 실리콘 기판 전면의 모든 영역에 마스크 층을 형성한 상태에서 패터닝공정을 수행할 수도 있지만, 잉크젯(Inkjet) 또는 스크린 프린팅 방법을 이용하여 별도의 패터닝공정 없이 한 번에 패터닝된 마스크 층을 형성시킬 수도 있다.

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[0043] 상기 패터닝된 마스크 층을 이용하여 실리콘 기판에 홈을 형성하기 위한 선택적 식각공정이 수행된다(S108). 상기 선택적 식각공정은 상기 패터닝된 마스크 층에 의해 상기 실리콘 기판의 전면 중 홈이 형성되는 부분만을 식각하도록 수행된다. 이때에는 반응성 이온 식각(Reactive Ion Etching: RIE), 플라즈마 식각(Plasma Etching) 및 습식식각(Acid Wet Etching, Alkaline Wet Etching) 등의 방법이 이용되어 선택적 식각공정이 수행된다. 이 중에서, 상기 반응성 이온 식각과 플라즈마 식각 방법을 이용하는 경우, 식각 가스(Gas)는 F 계열 또는 Cl 계열 등의 반응 가스를 이용한다. 그러나, 상기 식각 가스는 이에 한정되는 것은 아니고, 상기 마스크 층과 실리콘 기판 간의 식각 선택비가 높은 가스이면 이용가능하다. 또 상기 습식식각 방법을 이용하는 경우에는 산(Acid) 계열의 화학물질 또는 알카라인(Alkaline) 계열의 화학물질을 이용한다. 상기 산 계열의 화학물질은 HCL, HF, NHO_3, CH_3COOH 또는 상기 산 계열의 화학물질의 혼합물이 이용된다. 그리고, 상기 알카라인 계열의 화학물질은 KOH, $NaOH$, IPA 또는 상기 알카라인 계열의 화학물질의 혼합물이 이용된다. 그러나, 상기 산 계열의 화학물질과 알카라인 계열의 화학물질은 이에 한정되는 것은 아니고, 상기 마스크 층과 실리콘 기판 간의 식각 선택비가 좋은 화학물질이면 이용가능하다.

[0044] 상기 선택적 식각공정에 의해 실리콘 기판에 홈이 형성되면, 상기 실리콘 기판과 다른 타입의 불순물(도펀트)을 도핑하여 선택적 에미터(selective emitter) 층을 형성하는 도핑공정이 수행된다(S110). 즉, 상기 도핑공정이 수행되면, 상기 마스크 층이 제거된 영역, 즉 홈 주위는 상기 도펀트가 직접 실리콘 기판으로 확산되어 고농도로 도핑되고, 반면 상기 마스크 층이 존재하는 영역은 상기 도펀트가 상기 마스크 층에 확산된 다음 실리콘 기판으로 확산되어야 하기 때문에, 확산속도가 느려져 상대적으로 저농도로 도핑되게 되는 것이다. 즉, 상기 패터닝된 마스크 층은 디퓨전 배리어(Diffusion Barrier)로서의 역할을 수행하게 되는 것이다. 이때, 상기 고농도 도핑은 90 ohm/squar 이상의 면 저항을 가지도록 도핑되고, 상기 저농도 도핑은 40 ohm/squar 이하의 면 저항을 가지도록 도핑되게 하는 것이 좋다. 또 상기 선택적 에미터 층은, 튜브 퍼니스(tube furnace)를 이용한 디퓨전(Diffusion), 벨트 퍼니스(belt furnace)를 이용한 디퓨전, 스프레이(Spray), SOD(Spin On Dopant), 플라즈마 도핑(Plasma Doping) 등의 방법에 의해 형성된다. 이와 같이, 한 번의 도핑공정으로 선택적 에미터 층을 형성할 수 있기 때문에 함몰전극형 태양전지를 제조 시 전체공정을 간소화할 수 있고, 이에 따라 공정 비용을 절감할 수 있다.

[0045] 상기 선택적 에미터 층이 정상적으로 형성되면, 상기 마스크 층과, 상기 선택적 에미터 층 형성시 발생하는 부산물을 제거하는 공정이 수행된다(S112). 상기 마스크 층과 부산물은 같은 계열(Oxide)의 유전체 물질이므로, 동일한 식각용액을 이용하여 제거될 수 있다. 상기 부산물은, p형 기판에 n형 도펀트를 확산시키는 경우 생성되는 PSG(Phosphor-Silicate Glass) 또는 n형 기판에 p형 도펀트를 확산시키는 경우 생성되는 BSG(Boro-Silicate Glass) 등을 말한다. 상기 PSG 또는 BSG는 전지의 전류를 차폐시키는 역할을 하기 때문에 전지효율을 높이기 위해서 반드시 제거해 주어야 한다.

[0046] 상기 마스크 층 및 부산물이 제거된 다음에는 상기 선택적 에미터층 상부에 태양광 반사를 막기 위한 반사방지막을 형성시키는 공정이 수행된다(S114). 상기 반사방지막은 SiO_2, SiN_x, Al_2O_3, SiO_xN_y 등과 같이 1.1 ~ 2.5 사이의 굴절율을 가지는 유전체 물질로 형성하고, 이는 화학증착(CVD), 스퍼터링(sputtering), 열 산화(thermal oxidation), 스프레이 등의 방법에 의해 형성된다. 이러한 반사방지막은 실리콘 기판의 표면 보호막(Passivation) 역할도 한다.

[0047] 이어서, 상기 실리콘 기판의 전면에 형성된 홈 내부 및 후면의 모든 부분에 금속 페이스트를 사용하여 전극을 형성하는 공정이 수행된다(S116). 상기 금속 페이스트는 니켈(Ni), 은(Ag), 크로뮴(Cr), 알루미늄(Al) 등이 이용될 수 있다. 이때에는 스크린 프린팅, 스텐실(Stencil), 잉크젯(Inkjet), 에어로졸 젯(Aerosol Jet), 스퍼터링(Sputturing), 증착법(evaporation) 등의 방법이 적용될 수 있다. 상기 전면의 홈에 형성된 전극(이하 "전면전극"이라 함.)은 태양광 흡수로 생성된 전자를 수집하는 역할을 하고, 후면에 형성된 전극(이하 "후면전극"이라 함.)은 실리콘 기판 후면에서의 광 반사를 높이고 전자의 재결합을 방지하는 역할을 한다.

[0048] 그리고 상기 전면전극 및 후면전극이 실리콘 기판에 전기적으로 연결되도록 700도 이상의 고온에서 열처리 공정이 수행된다(S118). 그러면, 전면전극 내의 금속원자가 반사방지막으로 침투하여 결국 상기 반사방지막이 전면전극화 되게 된다. 따라서, 전면전극은 실리콘 기판에 접합하게 되어 저항 전극(Ohmic Contact) 형태로 형성되는 것이다. 그리고 상기 후면전극은 상기 후면전극의 금속 페이스트가 소정의 두께만큼 상기 실리콘 기판에

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확산되어 후면 전계층(Back Surface Field: BSF)을 형성한다. 상기 후면 전계층은 전계를 형성하여 광여기된 전자가 실리콘 기판의 후면으로 이동하는 것을 방지하는 역할을 한다.

[0049] 한편, 상기 저항 전극(Ohmic Contact)을 형성한 전면전극은 그 자체로 전면 전극의 기능을 수행할 수도 있지만, 시드층(seed layer)으로도 사용될 수 있다. 이 경우 상기 전면전극의 저항을 낮추고 종횡비를 높이기 위하여 상기 형성된 전면전극 상에 도금 층을 형성하는 도금공정이 추가적으로 수행될 수 있다(S120). 이때 상기 도금 층은 복수 개로 형성할 수도 있다. 상기 도금 층은, 구리(Cu), 주석(Sn), 크로뮴(Cr), 은(Ag), 니켈(Ni) 등의 도금 물질 또는 상기 도금 물질의 혼합물이 사용될 수 있다.

[0050] 다음, 도 3을 참조하여 도 2에서 설명한 공정을 다시 살펴보기로 한다.

[0051] 먼저, 도 3(a)는 절단 및 에칭(Saw damage etching) 공정이 수행된 실리콘 기판(100)이다. 상기 실리콘 기판(100)에 대해 습식 식각(Wet Etching) 방법을 이용하여 텍스처링(Texturing) 하면, 도 3(b)와 같이 상기 실리콘 기판(100)의 전면은 표면적이 증가된 구조로 형성된다.

[0052] 상기 텍스처링된 실리콘 기판(102)의 전면 상부에는 디퓨전 배리어로 사용가능한 마스크 층(110)을 형성한다. 이는 도 3(c)에 도시되어 있다.

[0053] 상기 마스크 층(110)이 형성되면, 도 3(d)에 도시된 바와 같이 상기 텍스처링된 실리콘 기판(102)의 전면 중 홈(Groove)이 형성될 부분에 해당하는 마스크 층(110)의 일부를 제거하여 패터닝(Patterning)된 마스크 층(110')을 형성한다.

[0054] 그런 다음 상기 텍스처링된 실리콘 기판(102)에 홈(G)을 형성하기 위해 도 3(e)처럼 선택적으로 식각공정을 수행한다. 즉, 상기 텍스처링된 실리콘 기판(102)만이 식각될 수 있도록 상기 패터닝된 마스크 층(110')과 텍스처링된 실리콘 기판(102) 간의 식각 선택비가 높은 식각용액을 이용하여 식각공정을 수행하는 것이다. 그러면, 상기 텍스처링된 실리콘 기판(102)에서 상기 패터닝된 마스크 층(110')과 접하는 부분은 식각되지 않고, 상기 패터닝된 마스크 층(110')과 접하지 않는 부분(112)에 대해서만 선택적으로 식각이 이루어지게 된다.

[0055] 이러한 상태에서, 상기 텍스처링된 실리콘 기판(102)과 다른 타입의 불순물(도펀트)을 도핑하게 되면, 선택적 에미터(selective emitter) 층(120)이 형성된다. 상기 선택적 에미터 층(120)은, 도 3(f)에 도시된 바와 같이, 상기 텍스처링된 실리콘 기판(102)에서 상기 패터닝된 마스크 층(110')과 접하는 영역은 상기 패터닝된 마스크 층(110')이 디퓨전 배리어(Diffusion Barrier)로 작용함에 따라 저농도의 에미터 층(122)이 형성되고, 반면 상기 텍스처링된 실리콘 기판(102)에 형성된 홈(G) 주위는 상대적으로 고농도의 에미터 층(124)이 형성되게 되는 것이다. 이와 같이, 한 번의 도핑공정으로 선택적 에미터 층(120)을 형성할 수 있다.

[0056] 상기 선택적 에미터 층(120)이 형성되면, 도 3(g)과 같이 상기 패터닝된 마스크 층(110)과 상기 선택적 에미터 층(120) 형성시 발생하는 부산물(PSG 또는 BSG)을 제거한 다음, 도 3(h)과 같이 상기 선택적 에미터 층(120) 상부에 태양광 반사를 막기 위한 반사방지막(130)을 형성한다.

[0057] 이어서, 도 3(i)에 도시된 바와 같이, 상기 텍스처링된 실리콘 기판(102)에 형성된 홈(G)에는 전면전극(142)을 형성하고 후면의 전체 면적에는 후면전극(144)을 형성한다.

[0058] 그리고 상기 전면전극(142) 및 후면전극(144)이 상기 텍스처링된 실리콘 기판(102)에 전기적으로 연결되도록 열처리 공정을 수행한다. 그러면, 도 3(j)과 같이, 전면전극 내의 금속원자가 반사방지막으로 침투하여 상기 반사방지막이 전면전극화 되게 된다. 이렇게 형성된 전면전극은 결국 실리콘 기판에 접합하게 되어 저항 전극(Ohmic Contact) 형태로 형성된다. 그리고, 상기 후면전극(144)은 소정의 두께만큼 상기 텍스처링된 실리콘 기판(102)으로 확산되어 후면 전계층(Back Surface Field: BSF)(146)을 형성한다.

[0059] 한편, 상기 텍스처링된 실리콘 기판(102)의 전면에 형성된 전면전극(142)은 그 자체로 전극 기능을 수행할 수도 있지만, 시드층(seed layer)으로도 사용될 수 있다. 이 경우 도 3(k)와 같이, 상기 전면전극(142) 상에 도금 층(148)을 형성한다. 본 실시 예에서는 하나의 도금 층(148)이 형성된 것으로 설명하고 있지만, 반드시 그러한 것은 아니고 두 개 이상의 도금 층을 형성할 수도 있다. 이러한 도금 층(148)은 상기 전면전극(142)의 저항을 낮추고 종횡비를 높이기 위함이다.

[0060] 이와 같이 상기 실시 예에 설명되고 있는 본 발명은 실리콘 기판 상부에 형성된 마스크 층을 이용하여 한 번의 도핑공정에 의해 선택적 에미터 층을 형성시킬 수 있어, 공정이 간소화될 수 있고 이에 따라 공정 비용이 절감되는 이점이 있다.

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[0061] 이상과 같이 본 발명의 도시된 실시 예를 참고하여 설명하고 있으나, 이는 예시적인 것들에 불과하며, 본 발명의 속하는 기술분야의 통상 지식을 가진 자라면 본 발명의 요지 및 범위에 벗어나지 않으면서도 다양한 변형, 변경 및 균등한 타 실시 예들이 가능하다는 것을 명백하게 알 수 있을 것이다. 따라서 본 발명의 진정한 기술적 보호 범위는 첨부된 청구범위의 기술적인 사상에 의해 정해져야 할 것이다.

도면의 간단한 설명

[0062] 도 1은 일반적인 함몰전극형 태양전지의 제조방법의 공정도.

[0063] 도 2는 본 발명의 바람직한 실시 예에 따른 함몰전극형 태양전지의 제조방법의 공정도.

[0064] 도 3은 도 2의 함몰전극형 태양전지의 제조방법의 공정도를 도시하고 있는 단면도.

[0065] *도면의 주요 부분에 대한 부호의 설명*

[0066] 100 : 실리콘 기판 102 : 텍스처링된 실리콘 기판

[0067] 110 : 마스크 층(Mask Layer) 110' : 패터닝된 마스크 층

[0068] G : 홈(Groove) 120 : 선택적 에미터 층

[0069] 122 : 저농도 에미터 층 124 : 고농도 에미터 층

[0070] 130 : 반사방지막 142 : 전면전극

[0071] 144 : 후면전극 146 : 후면 전계층(BSF)

[0072] 148 : 도금층

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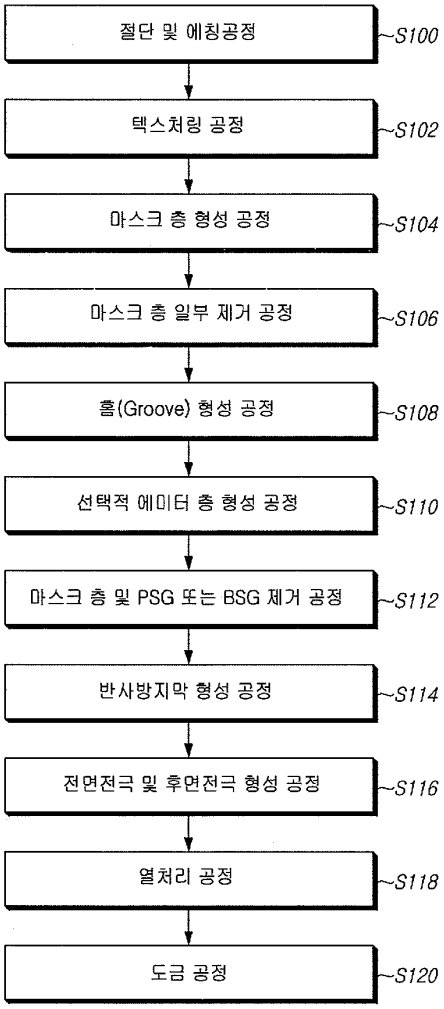
도면

도면1



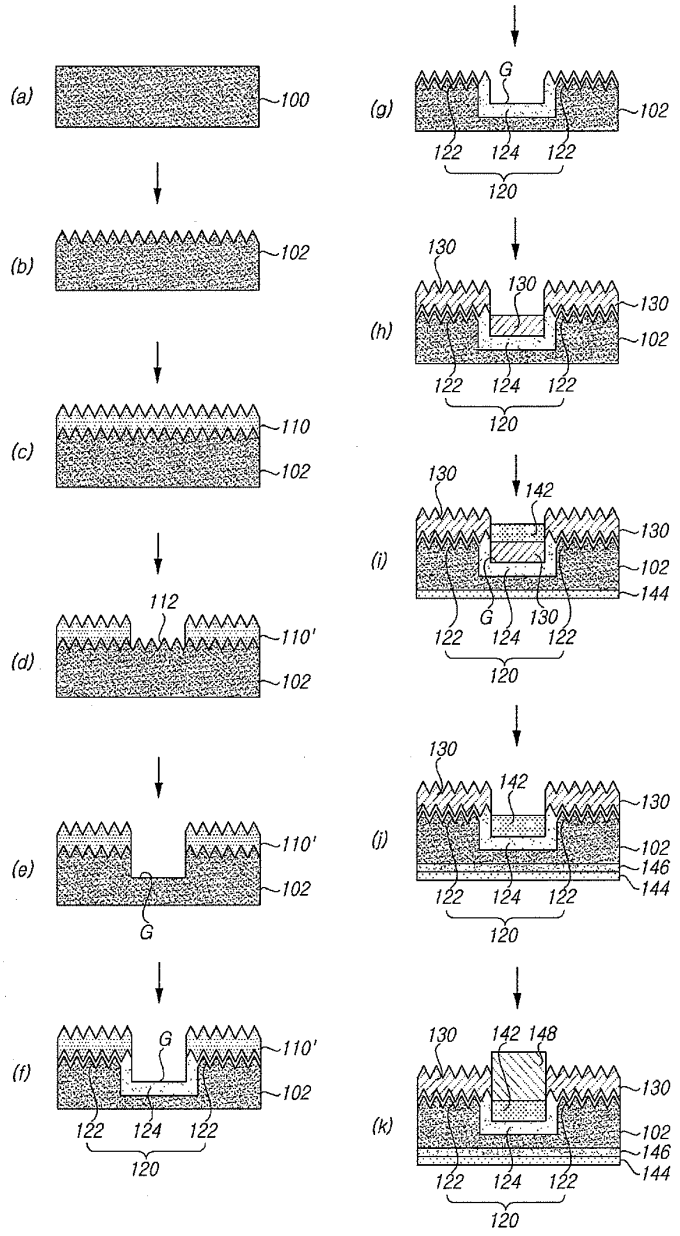
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도면2



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도면3



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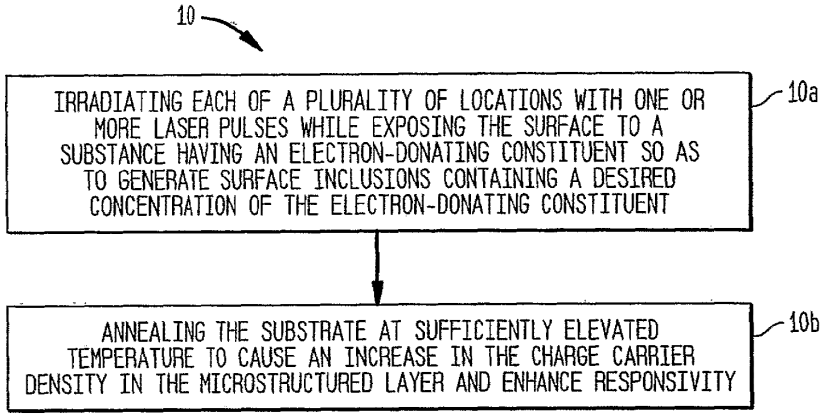
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(54) Title: MANUFACTURE OF SILICON-BASED DEVICES HAVING DISORDERED SULFUR-DOPED SURFACE LAYERS



(57) Abstract: The present invention provides methods of fabricating a radiation-absorbing semiconductor wafer by irradiating at least one surface location of a silicon substrate, e.g., an n-doped crystalline silicon, by a plurality of temporally short laser pulses, e.g., femtosecond pulses, while exposing that location to a substance, e.g., SF_6, having an electron-donating constituent so as to generate a substantially disordered surface layer (i.e., a microstructure layer) that incorporates a concentration of that electron -donating constituent e.g., sulfur. The substrate is also annealed at an elevated temperature and for a duration selected to enhance the charge carrier density in the surface layer. For example, the substrate can be annealed at a temperature in a range of about 700 K to about 900 K.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

MANUFACTURE OF SILICON-BASED DEVICES HAVING DISORDERED SULFUR-DOPED SURFACE LAYERS

Federally Sponsored Research

The invention was made with Government support under contract DE-FC36-016011051 awarded by Department of Energy (DOE). The Government has certain rights in the invention.

Related Applications

The present application is a continuation-in-part (CIP) of co-pending patent application entitled "Systems and Methods for Light Absorption and Field Emission Using Microstructured Silicon," filed on May 24, 2002, and having a Serial No. 10/155,429, which is herein incorporated by reference in its entirety.

Background of the Invention

The present invention relates generally to methods for fabricating radiation-absorbing semiconductor wafers, and more particularly, to methods for fabricating silicon wafers that can absorb radiation and exhibit diodic current-voltage characteristics.

Modern semiconductor circuits are predominantly based on silicon, which can be readily procured at a lower cost than any other semiconductor and can be easily oxidized. Further, a band gap of 1.05 eV renders silicon suitable for detection of visible light and conversion of sunlight into electricity. Silicon, however, has several shortcomings. For example, it is an indirect band-gap material, and hence it is a relatively poor light emitter. In addition, silicon is not particularly suitable for use in detecting radiation having long wavelengths, such as, infrared radiation employed for telecommunications. Although other semiconductor materials are available that can detect long wavelength radiation better than silicon, they are generally more costly and cannot be readily integrated in optoelectronic circuits that are primarily silicon-based.

Hence, there is a need for silicon-based semiconductor structures and wafers with enhanced radiation-absorbing properties, particularly in wavelengths beyond the band-gap of crystalline silicon. There is also a need for such wafers that can be utilized

in fabricating photodetectors that exhibit enhanced responsivity in detecting radiation over a wide wavelength range. Further, there is a need for methods of manufacturing such silicon-based wafers.

Summary of the Invention

In one aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor wafer by irradiating at least one surface location of a silicon substrate, e.g., a crystalline silicon, with a plurality of temporally short laser pulses while exposing that location to a substance having an electron-donating constituent so as to generate a substantially disordered surface layer that incorporates a desired concentration of the electron-donating constituent, e.g., a concentration in a range of about 0.5 atom percent to about 5 atom percent, or from about 0.5 atom percent to about 1 atom percent. The substrate is preferably annealed at an elevated temperature and for a duration selected to enhance charge carrier density, e.g., electron carrier density, in the disordered surface layer.

In a related aspect, an annealing temperature and duration can be selected to cause re-arrangement of atomic bonds in the surface layer so as to increase the concentration of free electrons in the surface layer. Further, the annealing temperature and duration can be selected to cause the surface layer to form a diode junction, e.g., a p-n junction, with the underlying silicon substrate. The term "diode junction" is known in the art and generally refers to a junction that can exhibit current rectification (e.g., a junction that exhibits drastically different conductivities in one bias direction relative to the other). Moreover, the annealing temperature and duration can be selected such that the annealed substrate would exhibit a responsivity in a range of about 1 Ampere/Watt (A/W) to about 200 A/W, or preferably in a range of about 10 A/W to about 200 A/W, upon exposure of the surface layer to visible radiation having wavelengths in a range of about 250 nm to about 1050 nm and application of a reverse bias in a range of about 0.1 V to about 15 V, or about 0.5 to about 15 V, to the substrate. Further, the annealing temperature and duration can be selected such that the annealed substrate will exhibit a responsivity in a range of about 0.1 Ampere/Watt (A/W) to about 100 A/W upon exposure of the surface layer to visible radiation having at least a wavelength in a range

of about 1050 nm to about 3500 nm and application of a reverse bias in a range of about 0.1 V to about 15 V to the substrate.

In a related aspect, the laser pulses irradiating the substrate's surface have pulse widths in a range of about a few nanoseconds to about 10 femtoseconds, and more preferably in a range of about 50 to about 500 femtoseconds. The laser pulse fluences can range from about 1 kJ/m^2 to about 30 kJ/m^2, or from about 3 kJ/m^2 to about 15 kJ/m^2, or from about 3 to about 8 kJ/m^2. The annealing temperature can be in a range of about 500 K to about 1100 K, preferably in a range of about 500 K to about 900 K, and more preferably in a range of about 700 K to about 900 K, and the annealing duration can be from about a few seconds to about a few hours.

In another aspect, the substance containing an electron-donating constituent can be a gas, a fluid or a solid. Some examples of such substances include, without limitation, SF_6, H_2S, Cl_2, and N_2. For example, when SF_6 is utilized, the exposure of the silicon surface to the laser pulses generates sulfur inclusions in a surface layer of the substrate. The silicon substrate is preferably n-doped, but it can also be p-doped. The substrate's bulk doping level can be in a range of about 10^{11} to about 10^{18} cm^{-3}.

In another aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor structure that calls for irradiating each of a plurality of locations on a surface of a silicon substrate with one or more femtosecond laser pulses while exposing the surface to a sulfur-containing substance so as to generate a plurality of sulfur inclusions in a surface layer of the substrate. The substrate is annealed at a temperature in a range of about 500 K to about 1100 K for a time duration in a range of about a few seconds to about a few hours. The annealing step can be performed subsequent to, or simultaneously, with irradiation of the substrate's surface with laser pulses. Further, the annealing step can be performed in an inert atmosphere or in vacuum (i.e., a low-pressure atmosphere).

In a related aspect, the light emitted in each laser pulse can have a narrow spectrum and a central wavelength in a range of about 200 nm to about 1200 nm (e.g., 800 nm or 1064 nm), fluences in a range of about 1 kJ/m^2 to about 30 kJ/m^2, and more preferably in a range of about 1 kJ/m^2 to about 10 kJ/m^2 ,and a repetition rate in a range of about 1 kHz to about 50 MHz, or in a range of about 1 kHz to about 1 MHz.

In another aspect, the invention provides a method of fabricating a semiconductor wafer by irradiating a plurality of locations on a surface of a silicon substrate with one or more laser pulses having pulse widths in a range of about 50 to about 500 femtoseconds while exposing the surface to a substance having an electron-donating constituent so as to generate a microstructured surface comprising inclusions that incorporate the electron-donating constituent. The laser pulses can be directed at the substrate in a direction forming a selected angle relative to the substrate's surface, e.g., normal to the surface. The substrate is annealed at an elevated temperature in range of about 500 K to about 1100 K for a selected time duration, e.g., in a range of about a few seconds to about a few hours. In certain applications, the annealing temperature can be between about 500 K and 1000 K, and more preferably between 575 K and 875 K.

In another aspect, the invention provides a method of fabricating a semiconductor wafer by irradiating at least one location on a surface of a silicon substrate with temporally short laser pulses, e.g., femtosecond pulses, while exposing the surface to a substance having an electron-donating constituent so as to generate a microstructured surface layer having inclusions containing the electron-donating constituent. The substrate can be annealed, either following the laser irradiation or simultaneous therewith, at a temperature and for a duration selected to enhance the responsivity of the microstructured substrate to electromagnetic radiation having at least one wavelength in a range of about 250 nm to about 1100 nm by a factor of about 10, or preferably about 20, or more preferably about 100, relative to a similarly microstructed substrate but without annealing. The responsivity can be measured upon application of a reverse bias voltage in a range of about 0.5 V to about 15 V to the substrate. A suitable annealing temperature for effecting such enhancement of the wafer's responsivity lies in a range of about 600 K to about 900 K, and more preferably in a range of about 700 K to about 900 K, and a suitable annealing duration lies in a range of about a few seconds to about a few hours.

In another aspect, the present invention provides a photodetector that includes a silicon substrate having a surface layer, configured for exposure to external radiation, that is doped with sulfur inclusions with an average concentration in a range of about 0.5 atom percent to about 5 atom percent so as to exhibit a diodic current-voltage characteristic. The photodetector further includes a plurality of electric contacts, e.g., in

the form of metallic coatings, that are disposed on selected portions of the substrate for applying a selected reverse bias voltage, e.g., in a range of about 0.1 to about 15 volts, to the surface layer for facilitating generation of an electrical signal, e.g., a photocurrent, in response to exposure of the surface layer to electromagnetic radiation. The surface layer is configured such that an electrical signal in response to an incident radiation having at least a wavelength in a range of about 250 nm to about 1050 nm can be generated at a responisivity greater than about 1 A/W. Preferably, the responsivity over the entire range of about 250 nm to about 1050 nm is greater than about 1 A/W. For example, the responsivity to at least one wavelength in this wavelength span, and preferably to all wavelengths in this span, can be in a range of about 1 A/W to about 100 A/W, or in a range of about 10 A/W to about 100 A/W, or in a range of about 10 A/W to about 200 A/W.

In another aspect, the photodetector can exhibit an average responsivity (i.e., responsivity averaged over a wavelength range) to wavelengths in a range of about 250 nm to about 1050 nm that is greater than about 1 A/W, e.g., an average responsivity in a range of about 1 A/W to about 100 A/W, or an average responsivity in a range of about 10 A/W to about 200 A/W.

In another aspect, the photodetector can exhibit a responsivity greater than about 1 A/W (e.g., in a range of about 1 A/W to about 100 A/W) for wavelengths in a range of about 250 nm to about 600 nm, as well as in a range of about 600 nm to about 1050 nm. In a related aspect, the photodetector can exhibit a responsivity greater than about 0.1 A/W for incident radiation having at least one wavelength in a range of about 1050 nm to about 2000 nm, and preferably in a range of about 1050 nm to about 3500 nm. Preferably, the photodetector's responsivity to all wavelengths in this range (about 1050 nm to about 3500 nm) is greater than about 0.1 A/W. For example, the detector's responsivity in this wavelength span can be in a range of about 0.1 A/W to about 100 A/W.

In another aspect, the photodetector can exhibit an average responsivity greater than about 0.1 A/W (e.g., a responsivity in a range of about 0.1 A/W to about 100 A/W) for radiation having wavelengths in a range of about 1050 nm to about 2000 nm, and preferably in a range of about 1050 nm to about 3500 nm.

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Photodetectors according to the teachings of the invention, such as those described above, provide a marked improvement over conventional silicon photodiodes where responsivities greater than 1 A/W for wavelengths in a range of about 250 nm to about 1050 nm are unknown. Further, responsivities of conventional silicon photodiodes degrade drastically for wavelengths beyond 1050 nm, and are significantly less than those that can be achieved by photodetectors of the present invention.
In another aspect, the surface layer can have a thickness in a range of about 10 nanometers to about 1 micron, and a microstructured morphology. For example, the microstructured layer can be formed by a plurality of conical microstructures, each of which can be composed of a core silicon portion forming a junction with a surface portion that is doped with sulfur. A term "conical structure or microstructure" as used herein refers to a generally cone-like or columnar protrusion above the silicon surface that can have vertical walls, or slanted walls that taper in the vertical direction. The microstructures can have a height in a range of about 0.5 micron to about 30 microns protruding from a base portion on the surface of the silicon substrate to a tip portion having a radius of curvature of about a few hundred nanometers. The gradient of sulfur concentration across the junction is substantially abrupt, although in some cases it can be gradual with the core portion having some sulfur dopants. The sulfur-doped surface layer can comprise silicon nanocrystals having diameters in a range of about 10 about 50 nanometers.

In another aspect, the invention provides a photodetector that includes a silicon substrate having a microstructured layer incorporating inclusions containing an electron-donating constituent. The microstructured layer is adjacent an underlying bulk silicon portion and forms a diode junction therewith. The term "diode junction" is known in the art and generally refers to a junction that can exhibit current rectification (e.g., a junction that exhibits drastically different conductivities in one bias direction relative to the other). A well-known example of a diode junction is a p-n junction. An electrical contact is disposed on a surface portion of the microstructured layer such that at least another surface portion of that layer remains available for receiving incident electromagnetic radiation. The photodetector can further include another electrical contact disposed on a surface of the bulk silicon portion opposed to the microstructured layer. The electrical contact layers allow application of a reverse bias voltage to the

substrate to facilitate generation of an electrical signal, e.g., a photocurrent, in response to exposure of the microstructured layer to incident radiation having wavelengths in range of about 250 nm to about 1050 nm at a responsivity in a range of about 1 A/W to about 200 A/W.

In a related aspect, the substrate can generate a photocurrent in response to irradiation of the microstructured layer with radiation having wavelengths in a range of about 1050 nm to about 3500 nm at a responsivity in a range of about 0.1 A/W to about 100 A/W.

In another aspect, the electron-donating constituent can be, for example, sulfur, chlorine or nitrogen, and can be present in the microstructured layer at a concentration in a range of about 0.5 to about 5 atom percent, or in a range of about 0.5 to about 1.5 atom percent, or in a range of about 0.5 to about 1 atom percent.

In another aspect, the present invention provides a photodetector for use in the visible and the infrared regions of the electromagnetic spectrum that includes a crystalline silicon substrate having a microstructured surface layer characterized by a plurality of substantially conical microstructures. The microstructured layer includes a doped layer having a plurality of silicon nanocrystals that contain an electron-donating dopant, such as sulfur, chlorine or nitrogen, with an average concentration in a range of about 0.5 to about 1.5 atom percent. The microstructured layer exhibits a diodic current-voltage curve and is configured to receive an external radiation. A plurality of electrical contacts are disposed on selected portions of the substrate for applying a reverse bias voltage to the microstructured layer in order to facilitate generation of an electrical signal in response to irradiation of at least a portion of that layer. The photodetector exhibits a responsivity greater that about 1 amperes/watt (A/W) for radiation wavelengths in a range of about 250 nm to about 1050 nm and a responsivity greater than about 0.1 amperes/watt for radiation wavelengths in a range of about 1050 nm to about 3500 nm.

Further understanding of the invention can be obtained by reference to the following detailed description in conjunction with the associated drawings, which are briefly described below.

Brief Description of the Drawings

FIGURE 1 is a flow chart depicting various steps in an exemplary embodiment for generating a microstructured silicon wafer suitable for absorbing radiation,

FIGURE 2 is a schematic diagram of an exemplary apparatus for microstructuring silicon wafers in accordance with one aspect of the invention,

FIGURE 3 is a scanning electron micrograph of a silicon surface, obtained at a 45-degree angle relative to the surface, after irradiation of the surface with 100 fsec pulses having a central wavelength of 800 nm and a fluence of about 5 kJ/m^2,

FIGURE 4 schematically illustrates an experimental set-up for performing resistivity and Hall effect measurements on a silicon sample microstructured in accordance with the teachings of the invention,

FIGURE 5 presents a plurality of graphs depicting wavelength absorptance of prototype microstructured silicon wafers as a function of an average number of 100 laser shots (8 kJ/m^2) per location employed for microstructuring the wafers in the presence of SF_6,

FIGURE 6 presents a plurality of graphs depicting wavelength dependence of absorptance of a plurality of prototype silicon wafers annealed at different temperatures subsequent to their microstructuring by a plurality of femtosecond laser pulses (the room temperature (300 K) data corresponds to a wafer that was not annealed),

FIGURE 7 presents graphs depicting wavelength dependence of absorptance for exemplary femtosecond-laser-formed and nanosecond-laser-formed microstuctured silicon wafers, before and after thermal annealing at 875 K for about 30 minutes (the absorptance of an unstructured silicon substrate as a function of wavelength is also shown for comparative purposes),

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FIGURE 8A presents graphs depicting absorptance as a function of wavelength for a plurality of prototype silicon wafers microstructured by exposure to 500 laser shots of femtosecond pulses (fluence of 8 kJ/m^2) in the presence of different gases in the absence of annealing (the graph designated vacuum relates to wafer microstructured in a vacuum chamber at a base pressure less than about 10^{-6} bar),

FIGURE 8B presents absorptance data as a function of wavelength for a plurality of prototype silicon wafers microstructured by exposure to 500 shots of 100 femtosecond laser pulses (fluence of 8 kJ/m^2 in the presence of sulfur-bearing and non-sulfur-bearing gases) indicating the positive effects of sulfur incorporation in enhancing below band-gap absorptance,

FIGURE 9 presents graphs depicting wavelength dependence of absorptance for a plurality of prototype silicon wafers microstructured by femtosecond laser pulses in the presence of SF_6 at different partial pressures,

FIGURE 10 schematically illustrates a p-n junction in thermal equilibrium,

FIGURE 11A is a perspective view of a photodetector formed in accordance with one embodiment of the invention,

FIGURE 11B is a side view of the photodetector depicted in FIGURE 11A,

FIGURE 12 presents graphs depicting current-voltage characteristics of a plurality of exemplary silicon wafer microstructured by exposure to femtosecond laser pulses in the absence of annealing as well as in the presence of annealing at different annealing temperatures,

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FIGURE 13 presents graphs depicting responsivity of a plurality of silicon wafers microstructured by exposure to femtosecond laser pulses in the presence of SF_6 (with no annealing and with annealing at different temperatures) as a function of wavelength in comparison with that of a commercial photodiode illustrating that a significantly enhanced responsivity can be obtained by judicious annealing of wafers subjected to laser microstructuring,

FIGURE 14 present graphs depicting current-voltage characteristics of a plurality of exemplary prototype silicon wafers microstructured by femtosecond laser pulses at different laser fluences and each annealed at 825 K,

FIGURE 15A presents comparative responsivity measurements for prototype silicon wafers microstructured by femtosecond laser pulses at different fluences and each annealed at 825 K for about 30 minutes,

FIGURE 15B presents comparative responsivity measurements for prototype silicon wafers microstructured by femtosecond laser pulses at different fluences and each annealed at 1075 K for about 30 minutes,

FIGURE 16A presents current-voltage characteristics for n-doped and p-doped silicon substrates microstructured by exposure to femtosecond laser pulses at a fluence of 6 kJ/m^2 followed by annealing at 825 K for about 30 minutes,

FIGURE 16B presents current-voltage characteristics for n-doped and p-doped silicon substrates microstructured by exposure to femtosecond laser pluses at a fluence of 4 kJ/m^2 followed by annealing at 1075 K for about 30 minutes,

FIGURE 17A presents responsivity measurements for prototype exemplary n-doped and p-doped silicon substrates microstructured at two different laser fluences (4 kJ/m^2 and 6 kJ/m^2) and annealed at 825 K for about 30 minutes,

FIGURE 17B presents responsivity measurements for prototype exemplary n-doped and p-doped silicon substrates microstructured by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 1075 K for about 30 minutes,

FIGURE 18 presents a graph depicting responsivity as a function of back bias for an n-doped silicon substrate microstructured via irradiation by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 825 K for about 30 minutes (the measurement was performed by employing a white light source with an approximate power of 50 microwatts),

FIGURE 19A presents graphs depicting current-voltage characteristics of an n-doped silicon sample microstructuured by femtosecond laser pulses at a fluence of 4 kJ/m^2 and annealed at 825 K as a function of operating temperature,

FIGURE 19B presents a graph depicting the responsivity of a microstructured silicon wafer to incident radiation having a wavelength of 1064 nm as a function of operating temperature,

FIGURE 20 illustrates current-voltage characteristics for a high resistivity (resistivity greater than 1 Ohm-m) microstructured silicon wafer that can be utilized as a solar cell, with and without one sun illumination,

FIGURE 21 illustrates current-voltage characteristics for a low resistivity (e.g., a resistivity in a range of about 0.01 to about 0.1 Ohm-m) microstructured silicon wafer that can be utilized as solar, with and without one sun illumination,

FIGURE 22 schematically depicts an exemplary experimental set-up for measuring field emission of a silicon substrate microstructured in accordance with the teachings of the invention, and

FIGURE 23 shows a graph depicting field emission current generated by a silicon wafer microstructured by exposure to femtosecond laser pulses in the presence of SF_6 as a function of a potential difference applied thereto.

Detailed Description

With reference to a flow chart 10 of FIGURE 1, in one aspect, the present invention provides a method of fabricating a radiation-absorbing semiconductor structure in which, in an initial step 10a, each of a plurality of locations on a surface of a silicon substrate is irradiated with one or more laser pulses while exposing the surface to a substance having an electron-donating constituent so as to generate surface inclusions containing a concentration of the electron-donating constituent. The laser pulses can have a central wavelength in a range of about 200 nm to about 1200 nm, and a pulse width in a range of about tens of femtoseconds to about hundreds of nanometers. Preferably, the laser pulse widths are in a range of about 50 femtoseconds to about 50 picoseconds. More preferably, the laser pulse widths are in the range of about 50 to 500 femtoseconds. The number of laser pulses irradiating the silicon surface can be in a range of about 2 to about 2000, and more preferably, in a range of about 20 to about 500. Further, the repetition rate of the pulses can be selected to be in a range of about 1 kHz to about 50 MHz, or in a range of about 1 kHz to about 1 MHz. Moreover, the fluence of each laser pulse can be in a range of about 1 kJ/m^2 to about 12 kJ/m^2, and more preferably in a range of about 3 kJ/m^2 to about 8 kJ/m^2.

While in some embodiments, the electron donating constituent is a fluid (gas or liquid), in other embodiments it can be a solid deposited over the silicon surface exposed to laser pulses. By way of example, in some embodiments, the silicon surface can be exposed to a sulfur-containing gas (e.g., SF_6 or H_2S) while irradiated with the laser pulses. In some other embodiments, Cl_2 or N_2 is employed as the electron-donating substance with which the silicon surface is in contact during laser irradiation. In yet other embodiments, selenium or tellurium can be employed. Without any loss of generality, in the following discussion, it is assumed that SF_6 is employed as the substance containing an electron-donating constituent, and that the irradiating pulses have femtosecond pulse widths, unless otherwise indicated. However, it should be clear to those having ordinary skill in the art that various embodiments of the invention

described below can also be practiced with other fluids or solids and laser pulses having other pulse widths, such as those listed above.

In some embodiments, the silicon substrate is p-doped (e.g., doped with Boron) with a doping level in a range of about 10^{11} to about 10^{18}. In other embodiments, the silicon substrate is slightly n-doped (e.g., doped with Phosphorus) with a doping level in a range of about 10^{11} to about 10^{18}, and preferably in a range of about 10^{12} to about 10^{15}. The substrate thickness is not typically a critical parameter, and can be in a range of about 2 microns to about 1000 microns. The substrate can have an electrical resistivity in a range of about 0.001 ohm-m to about 10 ohm-m.

FIGURE 2 schematically depicts an exemplary apparatus 12 that can be utilized for irradiating a silicon sample with a plurality of femtosecond pulses. The apparatus 12 includes a sample processing chamber 14 that comprises a stainless steel cube 16 with Conflat flange connections on each of its six sides. A three-axis, precision motion controller 18 is attached to the back side of the cube. This controller contains two orthogonal micrometer precision axes driven by computer controlled motors. The third axis is hand-controlled with about 1 mil precision. The controller can translate a one-inch diameter stainless steel rod 20 that supports a 2-inch diameter mounting magnet 22 in the center of the cube to which a magnetizable sample holder can be mounted. A two-stage roughing pump 24 is coupled to the cube to evacuate the chamber to a base pressure of approximately 10^{-3} torr. Two pressure gauges 26 and 28 are employed to monitor the chamber's pressure. A leak valve 30 and a gas-handling manifold (not shown) allow introduction of gases of interest into the chamber. An optical grade, 4.5 inch quartz window 32 is attached to the front of the chamber for providing laser access. Further, a quick-access viewport door 34 allows rapid loading and removal of samples as well as safe viewing of the sample during microstructuring.

In this exemplary apparatus, a regeneratively amplified, femtosecond Ti:Sapphire laser system (not shown) provides approximately 100 fs laser pulses having a central wavelength of 800 nm at a repetition rate of 1 kHz. The laser pulses are focused by a anti-reflection coated, plano-convex lens 36 (e.g., having a focal length of about 250-nm) through the quartz window onto the sample surface. In this exemplary embodiment, the lens is mounted on a single axis linear translation stage and positioned such that its focal point is behind the sample. By moving the lens, and hence its focal

point, the laser spot size can be varied at the sample surface (e.g., from a diameter of about 30 microns to 250 microns). In order to measure the laser spot size, a CCD (charge coupled device) camera 38 can be placed at the same distance as the sample surface from the lens. A flipper mounted mirror 40 can redirect the laser beam onto the camera to determine its spot size on the sample surface. A second CCD camera 42 can measure reflections of light generated by a white light fiber lamp 44 from the sample surface to monitor progress during microstructuring.

In one exemplary mode of operation, samples attached to a magnetizable sample holder can be loaded through the access door and attached to the mounting magnet. Samples can be then positioned in the center of the magnet to allow for maximum translation. The chamber can be evacuated to a base pressure of 10^{-3} torr and then filled to the desired pressure with an ambient gas (e.g., 0.67 bar of sulfur hexafluoride). The sample can then be irradiated with a 1-kHz train of 100-femtosecond 800-nm laser pulses. The fluence of each pulse can be set by selecting a spot size (e.g., 150 microns) and employing a waveplate/polarizing cube combination to vary the pulse energy. Either a single spot can be irradiated, or more typically the sample can be translated by utilizing the motion controller relative to the laser beam. For example, the sample can be translated in a raster scan pattern. An average number of pulses irradiating a given spot on the sample can be controlled by utilizing a shutter and varying the horizontal translation speed.

The irradiation of the silicon surface with the laser pulses in the presence of SF_6 at a selected partial pressure, for example, a partial pressure in a range of about 0.005 bar to about 1 bar, can cause formation of a sulfur-rich layer having a sulfur concentration in a range of about 0.1 atom percent to about 5 atom percent, and more preferably, in a range of about 0.5 atom percent to about 1 atom percent. This sulfur-rich layer exhibits an undulating surface morphology (topography) with micron-sized surface height variations. Such a textured surface obtained by irradiating a silicon surface with a plurality of temporally short laser pulses in the presence SF_6 (or other substances having an electron-donating constituent) is herein referred to as a micro-structured surface. By way of example, FIGURE 3 shows a scanning electron micrograph (SEM) of a such a micro-structured silicon surface (obtained in a direction forming a 45 degree angle relative to the surface) after irradiation of the silicon surface

with an average of 5 shots of femtosecond laser pluses (100 femtoseconds) at a wavelength of 800 nm and having a fluence of 8 kJ/m2 in 0.67 bar of SF_6.

The sulfur-rich layer can be a substantially disordered layer that is several hundred nanometers thick and made up of nanocrystallites (e.g., about 10 – 50 nm in diameter) and nanopores. Selected area diffraction (SAD) measurements indicate that the surface layer retains a substantial crystalline order with a strong possibility that amorphous-like material is present between the nanocrystalline grains. Further, SAD measurements performed on silicon substrates exposed to either 10 or 500 pulses per location indicate that the substrate below the disordered layer comprises substantially undisturbed crystalline silicon (when a crystalline silicon substrate is utilized). Further, Rutherford backscattering spectroscopy (RBS) and energy dispersive X-ray (EDX) emission spectroscopy performed on such exemplary substrates show a large concentration of sulfur is present in the disordered layer (about 1 atom percent). Further, RBS spectra obtained from silicon samples exposed to different femtosecond (100 femtoseconds) laser shots per irradiation location show that the concentration of sulfur increases with increasing laser pulse numbers up to about 50 pulses. In particular, the measured sulfur concentration increases from about 0.2 atom percent for a sample exposed to 2 pulses per location to about 0.7 atom percent for a sample exposed to 50 laser pulses per location with the sulfur concentration exhibiting a plateau for laser pulses higher than about 50. It should be, however, understood that the above experimental results are provided simply for further elucidation of salient features of the invention, and not as limiting the scope of the invention. For example, higher sulfur concentrations in the disordered layer than those described above can also be obtained, and higher laser shots per location can be utilized.

A number of factors can affect the morphology of the microstructured surface. For example, samples microstructured by irradiating a portion thereof with laser pulses, without moving them relative to the laser beam (i.e., single spot irradiation), exhibit a subtle difference in their morphology relative to samples microstructured by irradiating a plurality of their surface locations via translation relative to the laser beam. With the rest of the experimental parameters left the same, there are two visible differences between translated and stationary samples. The microstructures in the stationary samples have a micrometer-sized sphere at the tip while the translated samples are

sharper and lack the spheres. Further, the translated samples have a larger amount of nanoscale particles spread across the microstructured surface.

In addition, the wavelength of the irradiating laser pulses, their fluence, and pulsewidths can also affect the morphology of the microstructured surface. For example, in a number of prototype samples microstructured by femtosecond pulses, with increasing the fluence (at constant shot number) the morphology showed a transition from laser-induced periodic surface structures, to a coarsened surface, to sharp microstructures, such as those depicted in the above FIGURE 3. As the laser pulse fluence increases, there is typically an increase in both the microstructure height and distance between the microstructures. In general, the fluence is preferably selected to be above a threshold fluence that would cause melting (e.g., 1.5 kJ/m^2). At very high fluences (e.g., greater than 12 kJ/m^2), material removal can become extreme and gaussian-shaped holes, rather than conical structures, can be formed in the surface.

Although in many embodiments described herein, femtosecond laser pulses are employed, in other embodiments, the microstructuring of the surface can also be achieved by employing picosecond or nanosecond pulses. For example, a number of silicon samples were microstructured by utilizing a train of 248-nm, 30-ns laser pulses with a flat-top spatial profile and a fluence of 30 kJ/m^2 generated by a KrF+ excimer laser in the presence of 1 bar of SF_6 (an average of 1500 pulses per spot were employed). The nanosecond-laser-formed microstructures showed some similarities and some differences relative to the femtosecond-laser-formed microstructures. In both cases, the microstructures were roughly conical, but the structures formed with the femtosecond laser pulses were smaller and more densely packed. For example, the femtosecond structures were roughly 8 microns tall and separated by about 4 microns while the nanosecond-formed structures were roughly 40 microns tall and separated by about 20 microns. Further, the femtosecond-formed structures were covered with nanoparticles 10 – 50 nm in diameter while the surface of the nanosecond-formed structures were much smoother.

Sample silicon wafers exposed to picosecond pulses (e.g., 10 picosecond) in the presence of SF_6 also showed a microstructured surface. The average separation between the microstructures exhibited a decrease from about 100 femtosecond pulse widths to

about 5 picosecond pulse widths but then showed an increase for pulse widths longer than about 5 picoseconds.

The laser wavelength can also affect the final morphology of the microstructures. By way of example, a prototype silicon sample microstructured with a train of 400 nm pulses exhibited a higher density of microstructures (but smaller) than those generated by 800 nm pulses at a similar fluence.

Other factors that can affect the microstructures' morphology include laser polarization and laser propagation direction relative to the irradiated silicon surface. For example, the direction of microstructure growth is parallel to the direction of incident light, and appears to be independent of the substrate's crystallographic planes. The base of microstructure can have an elliptical shape with the long axis perpendicular to the polarization of the irradiating laser light. Without being limited to any theory, this elliptical shape can be understood as being due to a higher absorption of p-polarized light relative to s-polarized light. For circularly polarized light, there is no preferential ablation, and the base of the microstructures can be substantially circular.

The fluid or solid in contact with the silicon surface during its microstructuring can also affect the resultant surface morphology. For example, utilizing SF_6 or Cl_2 as the ambient gas can lead to sharp-tipped conical structures with a radius of curvature of about 500 nm. In contrast, structures made in air, N_2 or vacuum are much more rounded (the radius of curvature of their tips is approximately 2 – 3 microns) than those made in these halogen-containing gases. In a number of exemplary samples microstructured in the presence of different gases, those made in SF_6 exhibited the greatest density of microstructures followed by those made in Cl_2. The microstruture densities produced in the presence of N_2 were approximately equal to those made in air, but approximately a factor of two less than the densities obtained by employing SF_6.

In some embodiments, the laser microstructuring of a silicon wafer is performed in the presence of a mixture of two or more substances. For example, samples microstructured in the presence of a mixture of SF_6 and Cl_2 exhibited an increase in the microstructure density at higher partial pressure of SF_6.

The sulfur-rich mircrostructured layer has unique optical and electrical properties. For example, it can exhibit a sheet charge carrier density in a range of about 10^{12} cm^{-2} to about 10^{14} cm^{-2}. By way of example and only for illustrative purposes, the

results of some resistivity and Hall effect measurements performed on a number of exemplary microstructured samples, each formed in an n-doped silicon substrate in accordance with the teachings of the invention, such as those described above, are presented below. For resistivity and Hall effect measurements, the van der Pauw technique, well-known to those having ordinary skill in the art, was employed. Briefly, four ohmic electrical contacts were formed on the disordered microstructured layer. The electrical contacts were formed by initially dipping a microstructured sample in a 5% HF solution for 5 minutes to remove any native oxide layer. Subsequently, with a mask covering all but the very corners of a selected microstructured surface area (e.g., a 10 x 10 mm^2 surface area), chromium/gold (Cr/gold) was evaporated onto the surface to form metal contacts at the exposed corners. A dicing saw was then used to cut slivers (e.g., 0.25 mm slivers) from each side. Cutting the sample edges ensures that the contacts are only connected to the surface layer and not the substrate layer. Finally, a wire bonder is utilized to connect the contacts on the corners of the sample to four Cr/Au contact pads evaporated onto a glass slide. It should be understood that this experimental arrangement, shown schematically in FIGURE 4, is sensitive primarily to the electronic properties of the microstructured layer, and not that of the substrate.

With continued reference to FIGURE 4, the resistivity measurements can be performed by applying a small DC current (e.g., 10 microamperers) from corner 2 to corner 1 while measuring a voltage from corner 3 to corner 4. Hall effect measurements can be performed by placing the sample in a strong magnetic field (e.g., a field of several thousand gauss) with the magnetic field perpendicular to the silicon surface. In one experiment, a small AC current (about 1-2 microamperes) was then applied from contact 1 to contact 3 while measuring an induced voltage across contacts 2 and 4. Control measurements were also performed on an n-doped (resistivity = 8 – 12 ohm-m) unstructured silicon wafer. Table 1 below lists the results of these measurements for microstructured layers formed in an n-doped silicon wafer having a resistivity in a range of about 8 – 12 ohm-m at a number of different laser pulse fluences.

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Original doping	Average fluence (kJ/m^2)	Doping after structuring	Sheet resistance Rs (Ohm)	Sheet carrier density n_s (cm^{-2})	Hall mobility μ ($cm^2V^{-1}s^{-1}$)
n	unstructured	-	31931	$1.78x10^{11}$	1101
n	4.0	n	4865	$7.37x10^{12}$	174
n	6.0	n	4992	$7.15x10^{12}$	175
n	8.0	n	6253	$4.52x10^{12}$	221
n	10.0	n	4554	$8.83x10^{12}$	155

This data shows that microstructured layer exhibits a higher sheet carrier density than the original substrate, but a lower carrier mobility – presumably as a result of the disorder in the microstructured layer.

Referring again to the flow chart 10 of FIGURE 1, subsequent to irradiation of the silicon surface with a plurality of laser pulses (step 10a), the substrate can annealed (step 10b) at a sufficiently elevated temperature for a selected time duration so as to cause an increase in the charge carrier density in the microstructured layer, e.g., by a factor in a range of about 10 percent to about 200 percent. For example, the substrate can be annealed at a temperature in a range of about 500 K to about 1100 K, and more preferably, in a range of about 500 K to about 900 K, for a selected time duration, e.g., a time duration in a range of about a few minutes to about a few hours (e.g., one-half hour).

The annealing step can be performed by employing a variety of different techniques. For example, the substrate can be placed in a thermal oven to be exposed to an elevated temperature for a selected duration. Alternatively, the substrate can be exposed to laser radiation, e.g., radiation having a wavelength in a range of about 200 to about 1200 nm, to cause its heating to a desired temperature. Further, the annealing step can be performed, for example, in an inert atmosphere (e.g., an argon atmosphere) or in a vacuum (a low-pressure environment). Alternatively, the annealing step can be applied simultaneously with the irradiation step. That is, the irradiation of the silicon substrate with the laser pulses can be performed while the substrate is maintained at an elevated temperature.

Without being limited to any theory, the annealing step is designed to cause a rearrangement of the atomic bonds within the metastable microstructured layer to enhance the density of charge carriers – electrons – within that layer. The term "charge carrier density" is known to those having ordinary skill in the art. To the extent that any further explanation may be required, it refers to density of those charged particles, e.g., electrons, that are primarily responsible for current conduction, e.g., electrons in the conduction band states or in shallow impurity states below the conduction band. Such charged carriers are also herein referred to as free electrons or holes.

In other words, the annealing temperature and duration are selected to cause structural changes in the microstructured layer that result in increasing the carrier density in that layer while substantially maintaining responsivity of the layer for generating an electrical current when exposed to radiation within a selected wavelength range at a given applied back bias voltage, as discussed in more detail below. The structural changes caused in the microstructured sulfur-rich layer by an annealing step according to the teachings of the invention can be appreciated by considering that in many embodiments in which a p-doped silicon substrate is exposed to a plurality of laser pulses to generate a microstructured surface layer therein, holes, rather than electrons, constitute the dominant charge carriers even after incorporation of about 1 atom percent sulfur having two possible donor electrons per atom. However, after annealing, electrons can constitute the dominant charge carriers in the microstructured layer. Without being limited to any particular theory, such observations suggest that sulfur in the microstructured layer, before annealing, is incorporated in silicon such that its donor electrons do not substantially contribute to conduction (the donor electrons are likely locked up in a trap, or perhaps the coordination number of the implanted sulfur is larger than four). An annealing step according to the teachings of the invention causes atomic bond rearrangements in the microstructured layer so as to free up donor electrons for contributing to electrical conduction. In fact, in case of p-doped silicon substrates, the number of donor electrons released during annealing can be sufficiently large to eliminate the holes as the dominant charge carriers and turn the microstructured layer into an n-doped layer having a sheet carrier concentration on the order of about 10^{14} cm^{-2}.

A microstructured silicon wafer formed in accordance with the teachings of the invention exhibits absorption of incident electromagnetic radiation, particularly radiation having wavelengths in a range of about 250 nm to about 2500 nm. By way of example, FIGURE 5 presents absorption data for a microstructured silicon wafer (an n-Si (111) wafer having a thickness of about 260 microns and a resistivity in a range of about 8 – 12 ohm-m), each of which was generated by exposing its surface to 100 femtosecond laser pulses (2 to 500 shots per location) having a central wavelength of 800 nm and a fluence of about 8 kJ/m^2. This exemplary absorption data was recorded in a manner known in the art, prior to annealing the wafer, by employing an spectrophotometer equipped with an integrating sphere. The absorption data for an unstructured silicon wafer is also provided for comparative purposes.

This exemplary data indicates that the microstructured wafers exhibit an enhanced absorption of incident electromagnetic radiation, relative to unstructured silicon, across the entire recorded wavelength range, and particularly for wavelengths above about 1050 nm, which corresponds to the band-gap energy of crystalline silicon (1.05 eV). In the unstructured silicon, light photons having wavelengths longer than a wavelength corresponding to the band-gap energy do not contain sufficient energy to promote an electron from the valence band to the conduction band, leading to a drastic drop in absorption.

In contrast, the silicon wafers microstructured in accordance with the teachings of the invention exhibit significant absorption not only for wavelengths below the band-gap but also for those above it. In fact, the exemplary data of FIGURE 5 shows that silicon wafers structured by exposure to 20 pulses per location or higher (e.g., 500 pulses in this exemplary data set) exhibit near-unity, featureless absorption of wavelengths from about 0.4 micron to about 1 micron, a small decrease in absorption for wavelengths around about 1.05 micron (a wavelength corresponding to the band edge of unstructured silicon), and strong featureless absorption from about 1.05 microns to about 2.5 microns. It should be understood that this data is presented only for illustrative purposes, and is not necessarily intended to present the optimal absorption of a silicon wafer structured in accordance with the teachings of the invention.

As noted above, in many embodiments of the invention, a microstructured wafer is annealed at a temperature and for a duration designed to enhance the charge carrier concentration in its microstructured layer. Such annealing can be performed at a variety of different temperatures. By way of example, FIGURE 6 schematically illustrates electromagnetic radiation absorptance data for a plurality of microstructured silicon wafers generated by utilizing 500 laser pulses per surface location (100 fs pulses at a central wavelength of 800 nm and a fluence of 8 kJ/m2) in the presence of 0.67 bar of SF_6 relative to that of unstructured silicon. Each structured wafer was annealed at a selected temperature in a range of about 575 K to about 875 K for about 30 minutes. This exemplary data shows that annealing at temperatures below about 575 K has little effect on the observed absorptance. On the other hand, such annealing performed at a temperature between about 575 K and 875 K does not substantially affect absorptance above the bandgap, but lowers the below band-gap absoptance – the higher the annealing temperature, the greater is the reduction in absorptance. It should, however, be understood that this data is only exemplary, and different results may be obtained for microstructured wafers generated by employing different parameters (e.g., difference fluence or laser shot numbers).

A microstructured silicon wafer according to the teachings of the invention can be generated not only by utilizing femtosecond pulses, but also other pulse widths (e.g., nanosecond and picosecond pulse widths). By way of example and only for illustrative purposes, FIGURE 7 illustrates exemplary absorptance graphs as a function of incident radiation wavelength for femtosecond-laser-formed and nanosecond-laser-formed microstructured silicon surfaces, before and after annealing at about 875 K for about 30 minutes, as well as that of an unstructured silicon wafer. The femtosecond-formed mircrostructures were generated by employing 100 fs laser pulses (500 shots per location) having a central wavelength of about 800 nm and a fluence of about 8 kJ/m^2. The nanosecond-formed microstructures were generated by employing 30 ns laser pulses (about 1500 shots per location) having a central wavelength of 248 nm and a fluence of about 30 kJ/m^2. It should be understood that this data is presented only for illustrative purposes and is not intended to necessarily indicate absorptance exhibited by a microstructured silicon formed in accordance with the teachings of the invention under all circumstances.

In some embodiments of the invention, microstructuring of a silicon wafer can be accomplished in the presence of a background fluid rather than SF_6. For example, H_2S, Cl_2, N_2 or air can be utilized. By way of example, FIGURE 8A and 8B compare absorptance of some exemplary prototype microstructured silicon wafers generated by employing femtosecond laser pulses (100 fs, 800 nm, 8 kJ/m^2 and 500 shots per location) in the presence of various fluids – without an annealing step – with that of unstructured silicon. The vacuum data corresponds to microstructuring the wafer in a chamber evacuated to a base pressure that is less than about 10^{-6} bar. While all microstructured samples exhibit an enhanced absorption relative to unstructured silicon, this exemplary data shows the microstructuring in SF_6 and H_2S brings about the most dramatic change in absorptance relative to unstructured silicon. In particular, samples structured with SF_6 exhibit near-unity, substantially featureless absorptance across the entire measured spectrum.

A variety of background fluid pressures can be employed in many embodiments of the invention for generating microstructured silicon wafers. By way of example, FIGURE 9 shows absorptance data for a number of exemplary prototype microstructured silicon wafers generated in SF_6 (100 fs pulses, 800 nm, 500 shots per location) at different ambient pressures, as well as a wafer microstructured in vacuum (e.g., a pressure of less than 10^{-6}). The greatest rate of increase is observed at low pressures. In this exemplary data set, at pressures above about 27 mbar, the below band-gap absorptance does not show much variation with wavelength, while at lower pressures, it decreases with increasing wavelength.

The microstructured silicon wafers generated in accordance with the teachings of the invention, particularly those subjected to an annealing step at an elevated temperature in a range of about 500 K to about 900 K, not only exhibit enhanced absorption of electromagnetic radiation over a wide range (e.g., from ultraviolet wavelengths to near infrared), but they also exhibit voltage-versus-current profiles that are characteristic of diodes. As discussed in more detail below, these properties allow the use of such microstructured silicon wafers in fabricating photodetectors that exhibit enhanced responsivity relative to conventional silicon photodetectors.

More specifically, a microstructured silicon layer formed in accordance with the teachings of the invention, particularly one formed by exposure of a wafer surface to laser pulses followed by, or simultaneous with, an annealing step designed to release electrons in the layer structured by the pulses, forms a diode junction, e.g., a p-n junction, with the underlying silicon substrate. It should be understood that a diode junction as used herein can also refer a junction formed between two n-doped portions having different free electron densities. As shown schematically in FIGURE 10, a p-n junction can be formed by bringing a semiconductor material having acceptor impurity atoms (p-doped) into contact with a semiconductor material having donor impurity atoms (n-doped). The difference in charge carrier concentration between the p-doped and the n-doped portions generates a diffusion potential across the junction – electrons and holes begin to diffuse across the junction to portions having a respective lower concentration. As they cross to the other side of the junction, they recombine with their oppositely charged electrical counterparts in a region very close to the junction. This migration of charge carries across the junction causes formation of space charges (immobile ions) with opposite polarities on the two sides of junction. As the number of space charges increases (positively charged for the n-type side and negatively changed for the p-type side), a potential difference builds up across the junction, which results in an electric field in a direction opposite that of the diffusion potential.

Upon reaching thermal equilibrium, a thin insulating layer is present near the junction in which charge carriers have been depleted by recombination (depletion region). A strong electric field is present in the depletion region and a large electric potential exists across this region. The junction can be reverse-biased by applying an electric field across it that reinforces this internal electric field. Such a reverse-bias voltage expands the insulating depletion region and enhances both the internal electric field and the potential difference across the junction. The junction can also be forward-biased by applying an electric field that is opposite to the internal field across it. Such a forward-bias voltage shrinks the depletion region, thereby diminishing the internal electric field and the potential difference across the junction. When forward-biased, a current flows across the junction with electrons injected into the n-doped portion and leaving from the p-doped portion. In other words, the p-n junction can act as a rectifier

by allowing current flow in only one direction. This behavior gives rise to a current-voltage (I-V) curve characteristic of a diode.

As discussed above, a silicon wafer in which a microstructured layer is formed according to the teachings of the invention can exhibit an I-V curve characteristic of that obtained by a diode junction. Without being limited to any theory, such a current-voltage behavior can be understood by considering that the wafer includes two adjacent, yet distinct, layers: a surface layer in which a concentration of an electron-donating constituent is incorporated and an underlying substantially undisturbed silicon substrate layer. These two layers exhibit different crystalline structures, chemical compositions, and charge carrier doping concentrations. In addition, the microstructured layer has unique optical properties including high absorptance of incident electromagnetic radiation from the near ultraviolet into the near-infrared wavelengths. In one aspect, the invention employs such microstructured silicon wafers for fabricating photodiodes, as discussed in more detail below.

By way of example, FIGURE 11A schematically illustrates a photodetector 46 according to one embodiment of the invention that includes a microstructured silicon wafer 48 having a microstructured surface layer 50 that is formed in a silicon substrate 51 by irradiating a plurality of locations on a substrate's surface with short laser pulses (e.g., pulse widths in a range of about tens of femtoseconds to tens of nanoseconds) while exposing the surface to a substance having an electron-donating consitutent (e.g., SF_6). The laser-irradiated wafer is then annealed under conditions (e.g., at an elevated temperature and for a selected duration) designed to enhance concentration of electrons in the microstructured surface layer (e.g., annealing at a temperature in a range of about 500 K to about 900 K for a duration of a few minutes to a few hours).

The exemplary photodetector 46, functioning as a photodiode, also includes a plurality of metallic electrical contacts 52, which have a finger grid geometry, that are disposed on the microstructured surface layer. In addition, an electrical contact 54, in the form of a metallic coating layer, is disposed on the back surface of the silicon substrate (i.e., the undisturbed silicon surface opposite the microstructured surface) that substantially covers the entire surface. In this exemplary embodiment, a chromium/gold alloy (Cr/Au) is employed for fabricating the electrical contact. However, those having

ordinary skill in the art will appreciate that the contacts can be formed of other metals, as well.

The metallic contacts 52 and 54 allow applying a bias voltage, e.g., a reverse bias voltage, across the wafer by employing, for example, a voltage source 56. The reverse bias voltage can reinforce the internal electrical field in the depletion layer of a diode junction formed between the microstructured layer 50 and the underlying silicon substrate 51. As discussed in detail below, the photodetector 46 can operate with small bias voltages, e.g., voltages in a range of about 0.1 V to about 15 V, with a responsivity (i.e., photocurrent generated per unit of power of incident light (amperes/watts)) that is considerably better than that typically exhibited by a conventional silicon photodetector. These attributes allow incorporating silicon photodetectors formed according to the teachings of the invention, such as the exemplary photodetector 46, into integrated silicon photo-electronic circuits as high sensitivity detectors.

In operation, radiation (i.e., photons) incident on the microstructured surface layer of the photodiode's silicon wafer is absorbed (when the radiation wavelength is in the operating range of the photodetector), e.g., by valence electrons, in the microstructured layer. The absorption of the incident radiation causes generation of electron-hole pairs. The electric field within the depletion region causes separation of the generated electron-hole pairs, especially those created at or in proximity of the diode junction, which is formed between the microstructured silicon layer and the underlying silicon substrate. The separated electron-hole pairs provide a photocurrent that is proportional to the number of incident photons (those skilled in the art appreciate that such a photocurrent is added to a generation current and a recombination current that can be inherently present in a diode junction). Hence, incident radiation can be detected, and quantified, by measuring the induced photocurrent.

A photodetector formed according to the teachings of the invention not only exhibits absorptance across a wide range of wavelengths (the absoptance is generally commensurate with that exhibited by the photodetector's microstructured silicon wafer), but it also exhibits a diodic I-V behavior. By way of example and further elucidation of the salient features of a photodetector of the invention, FIGURE 12 illustrates a plurality of graphs, each representing current as a function of bias voltage for a plurality of microstructured silicon samples prepared under different conditions in an n-doped

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silicon substrate for use as the active component of photodetectors. All samples were irradiated with a plurality of femtosecond laser pulses (800 nm, 100 fs, fluence of 4 kJ/m^2) in the presence of SF_6, but were subjected to different annealing conditions. The graph A represents the current-voltage curve associated with a microstructured sample that was not annealed. This curve is substantially linear, indicating that the junction between the microstructured layer and the underlying silicon substrate in this sample is not diodic, but is merely resistive. In other words, such a wafer is not optimal for fabricating a photodetector.

In contrast, graphs B, C, and D illustrate current-versus-voltage behavior of those microstructured silicon samples that were subjected to annealing at different temperatures (the annealing duration was about 30 minutes in all cases). This exemplary data indicates that with an increase in the annealing temperature, the measured I-V curve approaches one expected from a diode. For example, at an annealing temperature of about 825 K, the I-V curve is diodic, characterized by an exponentially increasing current for a forward bias and a smaller, less rapidly increasing current for a reverse bias. The I-V curve corresponding to an annealing temperature of about 1075 K is also diodic. However, annealing a microstructured silicon wafer for a significant duration at a very elevated temperature can lead to a degradation of the below-band gap absorptance, and hence a degradation in the performance of a photodetector utilizing such a microstructured wafer in the near-infrared. In this exemplary data set, the substrate annealed at 825 K exhibit an optimal I-V characteristic. It should, however, be understood that such very elevated annealing temperatures may be employed so long as the annealing duration is sufficiently short. In general, the annealing of a microstructured silicon wafer to be employed in a photodetector of the invention should be carefully designed (i.e., annealing temperature and duration) to cause release of electrons in the microstructured surface layer without significantly degrading the wafer's absorptance of and responsivity to incident radiation.

A photodetector of the invention, such as the above exemplary photodetector 46, exhibits a responsivity that can be superior across a wavelength range of about 250 nm to about 10 microns to that of a conventional silicon photodiode. By way of example and only for illustration and corroboration purposes, FIGURE 13 presents experimental graphs representing responsivity of exemplary photodetectors formed in accordance with

the teachings of the invention, over a selected wavelength range, in comparison with a conventional photodiode and those fabricated by employing microstructured silicon, but with no annealing or annealing at too high a temperature. In particular, graphs A and B show that photodetecotors of the invention that employ silicon wafers microstructured by femtosecond laser pulses in the presence of SF_6 (100 fs, 800 nm central wavelength and a fluence of 4 kJ/m^2) followed by annealing at 825 K or 725 K, exhibit a significantly enhanced responsivity relative to that of a conventional commercially available silicon photodiode. In particular, these photodetectors exhibit a responsivity that is more than an order of magnitude greater that that of the conventional photodiode in a wavelength range of about 250 nm to about 1050 nm. Although the responsivity shows a decrease for wavelengths longer than the band-gap edge (i.e., wavelengths longer than about 1050 nm), nonetheless, it remains significantly higher than that exhibited by a conventional silicon detector. In fact, conventional silicon detectors typically do not operate at useful levels of responsivity at wavelengths that are longer than the band-gap edge. For example, in this exemplary illustration, the responsivity of the commercial photodiode drops steeply to about 10^{-6} A/W for wavelengths longer than about 1050 nm

Further, the responsitivy data for wafers formed according to the teachings of the invention (e.g., graphs A and B) were obtained by applying small bias voltages (e.g., a bias voltage of about –0.5 volts in this exemplary embodiment). In contrast, conventional silicon photodetectors exhibit much lower responsivities, or require much higher bias voltages (e.g., 100 to 1000 volts) and/or have more complex structures. This indicates that while photodetectors formed in accordance with the teachings of the invention can be readily incorporated in integrated silicon circuitry, the incorporation of conventional silicon detectors, which require large bias voltages, into integrated silicon circuits can be impractical.

The data depicted in FIGURE 13 also shows that proper annealing of a silicon wafer irradiated by a plurality of short laser pulses, as described above, can considerably enhance the responsivity of a photodetector that employs that wafer. In particular, a photodetector fabricated by utilizing a wafer that, though exposed to laser pulses, was not annealed, exhibits a much degraded responsivity relative to those that were subjected to an annealing step at appropriate temperatures, e.g., at 725 K or 825 K. This

exemplary data also shows that a photodetector that incorporates a microstructured wafer annealed, subsequent to irradiation by laser pulses, at a temperature of 1075 for thirty minutes exhibits a much degraded responsitivy relative to those annealed at 725 K or 825 K.

Hence, one aspect of the invention relates to annealing a silicon wafer, subsequent to – or simultaneous with – its irradiation by a plurality of short pulses in the presence of a substance having an electron-donating constituent, under conditions that would release electrons in the microstructured layer while preserving the responsivity of the wafer for detecting electromagnetic radiation. For example, in some embodiments of the invention, the annealing temperature is selected to be in range of about 500 K to about 1100 K, and more preferably in a range of about 700 K to about 900 K, and the annealing duration is selected to be in a range of about 1 minute to about several hours, and more preferably in a range of about 5 minutes to about 30 minutes. Alternatively, higher annealing temperatures can be employed so long as the annealing duration is properly selected to avoid degrading the responsivity of the resultant annealed wafer. For example, although the above data indicates that annealing the wafer at temperature of about 1075 K for about 30 minutes may not be desirable, this annealing temperature with a lower annealing duration can be suitable for practicing the invention in certain applications. To certain extent, annealing temperature and duration are inter-related. For example, shorter annealing time at a higher temperature can be employed in certain applications.

In other words, it is not simply annealing at an elevated temperature that is required. Rather, the annealing temperature and its duration need to be properly selected to ensure that a photodetector exhibiting enhanced responsivity over a wide wavelength range can be fabricated by utilizing the annealed wafer. It has been discovered that annealing a silicon wafer subsequent to, or simultaneous with, its exposure to short laser pulses in presence of a substance having an electron-donating constituent at a temperature that is too low can lead to noisy photodiode and annealing at too high a temperature and duration can lower the wafer's response to both visible and infrared wavelengths. More specifically, the annealing temperature and duration are preferably selected to enhance the concentration of carrier electrons in the microstructured layer – formed by laser irradiation in presence of a substance having an electron-donating

constituent – by a factor in a range of about 10% to about 200% while ensuring that the resultant annealed wafer exhibits a responsivity greater than about 20 A/W at least at one wavelength, and preferably over the entire span, of a wavelength range of about 250 nm to about 1050 nm, and a responsivity greater than about 0.1 A/W at least at one wavelength, and preferably over the entire span, of a wavelength range of about 1050 nm to about 3500 nm. By way of example, in some embodiments of the invention, the annealing temperature is preferably selected to be in a range of about 700 to about 900 K.

The choice of the fluence of laser pulses irradiating a silicon wafer to generate a microstructured layer therein can also affect the performance characteristics of a photodetector that incorporates the microstructured wafer for detecting radiation. By way of example, FIGURE 14 presents exemplary data corresponding to current-voltage characteristics of a plurality of silicon wafers irradiated with a plurality of femtosecond laser pulses (100 fs, 800 nm central wavelength, 200 pulses per location) in the presence of SF_6 followed by annealing at 825 K for about 30 minutes. The laser pulse fluences, however, differed from one wafer to another. More particularly, the following laser fluences were employed: 4 kJ/m^2, 6 kJ/m^2, 8 kJ/m^2, and 10 kJ/m^2. This exemplary data indicates that increasing the fluence decreases the dark current for a given reverse bias voltage.

FIGURE 15A illustrates the responsivity of a plurality of photodetectors incorporating the above silicon wafers that were microstructured with different laser pulse flunces (the wafers were annealed at 825 K for 30 minutes). This exemplary responsivity data indicates that, in this sample set, the photodetector's responsivity decreases, and the wavelength of peak response shifts to longer wavelengths, with increasing fluence (the sample made with a fluence of 4 kJ/m^2 exhibits the highest response). By way of further illustration, FIGURE 15B presents responsivity data for photodetectors made with microstructured silicon wafers that were generated through irradiation with femtosecond pulses (100 fs, 800 nm central wavelength, 200 pulses per location) in the presence of SF_6 followed by annealing at 1075 K for about 30 minutes. The laser pulse fluences, however, varied from one sample to the next (4 kJ/m^2, 6 kJ/m^2, 8 kJ/m^2, and 10 kJ/m^2). A comparison of this data with the data presented in FIGURE 15A shows that the responsivity exhibited by the samples subjected to the higher

annealing temperature of 1075 is much lower that that of the samples annealed at 825 K. However, the samples annealed at the higher temperature exhibit much less variation in responsivity as a function of fluence. Further, the samples annealed at 1075 K – though exhibiting a lower responsivity – are less noisy and have a higher quantum efficiency.

It should be understood that the above data is presented only for illustration purposes, and is not intended to necessarily indicate an optimal fluence under all conditions. For example, the above exemplary samples were made with an average laser shot number of about 200 pulses, and may exhibit improved characteristics with a greater shot number. In general, in various embodiments of the invention, the laser pulse fluence is selected to be greater than about 3 kJ/m^2. More preferably, the fluence is chosen to be in a range of about 3 kJ/m^2 to about 10 kJ/m^2, or a range of about 3 kJ/m^2 to about 8 kJ/m^2.

In many embodiments of the invention an n-doped silicon substrate is employed for forming a microstructured wafer, as described above. Alternatively, a p-doped silicon wafer can be utilized. By way of example, FIGURE 16A presents graphs comparing the diodic characteristics of a microstructured wafer generated according to the teachings of the invention, such as those described above, employing a p-doped silicon substrate (p-Si(100), 350 micron thick, resistivity (ρ) greater than 1 ohm-cm) with one fabricated utilizing an n-doped silicon substrate. In both cases, a laser pulse fluence of about 6 kJ/m^2, an annealing temperature of about 825 K, and an annealing duration of about 30 minutes were utilized. Similar data is presented in FIGURE 16B for p-dopend and n-doped samples annealed at 1075 K for about 30 minutes.

This exemplary data shows that the p-doped samples annealed at 825 K exhibit a higher forward bias current than equivalently generated n-doped samples. The dark current for back biases also increases more rapidly for p-doped samples. Upon annealing at 1075 K, the p-doped samples exhibit very good diodic properties with the back bias decreasing to substantially the same level as that in equivalently generated n-doped samples. Further, the forward bias current increases more rapidly, resulting in good rectification ratios. As noted above, annealing at higher temperatures can increase donor concentration from sulfur doping. Such increase in the donor concentration can lead p-doped samples annealed at higher temperature to exhibit better rectification.

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A silicon substrate's doping can also affect the responsivity of a silicon wafer formed by microstructuring that substrate in accordance with the teachings of the invention. By way of example, FIGURE 17A shows measured responsivity data for two n-doped microstructured wafers and two p-doped microstructured wafers, both of which were annealed at 825 K for about 30 minutes. This exemplary data indicates that the responsivity of n-doped substrates is higher over the measured spectral range. However, FIGURE 17B shows that the responsivities of microsturctured wafers formed in p-doped and n-doped substrates, via laser irradiation and annealing at a higher temperature of about 1075 K, are nearly identical.

In general, the above illustrative data indicates that microstructured p-doped samples have a lower response but exhibit a better quantum efficiency. It should be understood that the above data is presented only for illustrative purposes and is not intended to limit the scope of the invention. In general, both p-doped and n-doped substrates can be employed in the practice of the invention, and the resultant diodic characteristics and responsivity of microstuctured wafers generated by utilizing such substrates can be different than those depicted above based on selection of other parameters, such as laser fluence, number of pulses, etc.

In addition to responsivity, another parameter of interest associated with performance of a photodetector can be its quantum efficiency. The term 'quantum efficiency' is known in the art, and is generally defined as the number of electron-hole pairs generated per incident photon at a zero applied voltage. In some cases, a microstructured sample that exhibits a high level of responsivity may not show a correspondingly high level of quantum efficiency. For example, in the above exemplary prototype microstructured silicon wafers, samples fabricated by employing n-doped substrates, laser pulses having a fluence of 4 kJ/m^2, and an annealing temperature of about 825 K exhibit the highest responsivity, but not the highest quantum efficiency. In fact, samples fabricated by employing similar conditions but a higher annealing temperature of 1075 K show higher quantum efficiencies, though lower responsivities. Similarly, the measured responsivities of samples made on p-doped substrates and annealed at 825 K or 1075 K are lower, but their quantum efficiencies are higher. Such variations of responsivity and quantum efficiency are preferably considered when

selecting various parameters in practicing the teachings of the invention for fabricating a silicon photodetector.

The responsivity of a photodetector fabricated in accordance with the teachings of the invention can also vary as a function of a back bias applied thereto. Typically, the responsivity increases as the applied back bias increases. By of example, FIGURE 18 exhibits the responsivity of a silicon wafer microstructured in accordance with the teachings of the invention through irradiation by a plurality of femtosecond pulses at a fluence of $4kJ/m^2$ followed by annealing at 825 K for about 30 minutes, as a function of an applied back bias voltage. The sample was illuminated with a white light source with an approximate power of 50 microwatts. The responsivity, and hence gain, increases quickly up to a bias voltage of –5 volts and more slowly up to –15 volts. At voltages beyond –15 volts, the responsivity begins to fall. In some cases, the responsivity of a photodetector that exhibits a large gain may not be sufficiently linear for certain applications. Hence, in selecting a proper back voltage, in addition to responsivity, other factors, such as the linearity of the response should be considered. In addition, in applications in which the photodetectors are incorporated in an integrated silicon circuit, the bias voltage should be compatible with the requirements of that circuit.

A photodetector formed according to the teachings of the invention can operate within a wide range of temperatures. In some cases, it may be advantageous to cool the photodetector to decrease its average noise level. By way of example, FIGURE 19A presents current-voltage curves corresponding to an n-doped microstructured silicon sample made with femtosecond pulses at a fluence of about 4 kJ/m^2 and annealed at 825 K at different operating temperatures. The measured current in both the back bias and forward bias conditions decreases with decreasing the temperature. At very low temperatures (below 100 K), conduction becomes very low for both forward and back biases. FIGURE 19B shows the responsivity of such a microstructured wafer to incident radiation having a wavelength of 1064 nm (a wavelength close to the band gap of silicon at room temperature) at a back bias of –0.5 V as a function of operating temperature. The measured responsivity drops with temperature. This behavior may be, however, different if the wavelength of the illuminating light is far from the silicon band gap. A graph of the dark current at a bias voltage of –0.5 V as a function of temperature, however, shows that the noise decreases much more rapidly that the responsivity.

In sum, photodiodes formed according to the teachings of the invention can exhibit responsivities in a wide region of the electromagnetic spectrum (e.g., wavelengths in a range of about 250 nm to about 1100 nm) that are nearly two orders of magnitude higher than those exhibited by conventional commercial silicon photodiodes. Further, responsivities at longer wavelengths, e.g., as long as 1600 nm, can be nearly five orders of magnitude greater than those exhibited by conventional silicon photodiodes in this range. In some of the above prototype samples fabricated according to the teachings of the invention for illustration purposes, the carrier mobility in the surface layer was measured to be about 101 $cm^2V^{-1}s^{-1}$; the response times included a rise time of about 10 ns and a fall time of about 30 ns; and a diode capacitance of about 63.9 nF at a back bias of –0.5 V was measured. A photodiode of the invention can exhibit a large gain at very small applied bias voltages, e.g., a gain greater than 1000 for an applied bias voltage of – 0.5 V.

A silicon photodetector according to the teachings of the invention, such as the above exemplary photodetector 46 (FIGURE 11A), can be fabricated by employing a variety of techniques. By way of example, in one exemplary method of fabricating such a photodetector, a selected portion of a silicon wafer, e.g., a 5 x 5 mm^2 area, is microstructured via exposure to short laser pulses in the presence of a suitable material, e.g., SF_6, in a manner described above. The wafer is then dipped in a solution of HF (e.g., a 5% solution) in order to remove any native oxide layer before forming electric contacts with the microstructured layer. Subsequently, a mask is deposited over the surface of the microstructued layer having exposed portions which correspond to a desired pattern of a conductive electrode to be formed on that surface. A selected metal, e.g., a Cr/Au alloy, is then evaporated over the masked surface, and the mask is removed to leave behind a patterned conductive layer, such as the conductive layer 52 shown in FIGURE 11A, and uncoated portions suitable for receiving radiation. Further, a conductive layer can be formed on a back surface of the wafer, an unstructured surface opposed to the microstructured layer, such as the layer 54 shown in FIGURE 11A. In many embodiments, the entire back surface is coated with the metal. The wafer can be then be coupled to a voltage source, such as the source 56 shown in FIGURE 11A, that can apply a bias voltage thereto and optionally other electronic elements, e.g.,

capacitors, in a manner known in the art. Further, a the wafer and its associated circuitry can be placed in an appropriate housing by employing techniques known in the art.

The applications of microstructured silicon wafers formed according to the teachings of the invention, such as those discussed above, are not limited to photodetectors. For example, such silicon wafers can be employed in fabricating solar cells. In some cases, the optimal values of various parameters, such as substrate doping, associated with the microstructured wafer utilized in generating solar cells can be different than those in fabricating silicon photodetectors. A solar cell can be considered a p-n junction photodiode with high quantum efficiency. The conversion of photons into photocarriers is the physical mechanism by which light is converted in a solar cell into electricity. However, there is a fundamental difference between a photodetector and a solar cell. A photodetector is generally operated in a "photoconductive" mode: a back bias is applied thereto and a current is measured. In contrast, a solar cell is operated in a "photovoltaic" mode: it is operated in an open circuit mode or attached to a load without application of a bias voltage.

In one embodiment, a microstructured layer is formed in a p-doped crystalline silicon substrate by initially irradiating a plurality of locations on a surface thereof with femtosecond (e.g., 100 fs, and a central wavelength of 800 nm) laser pulses having a fluence of about 4 kJ/m^2 followed by annealing at 1075 K for about one hour. The wafer can then be utilized in fabricating a solar cell. More specifically, metal contacts, e.g., Cr/Au contacts, can be evaporated on the microstructure layer's surface so as to coat selected portions thereof while leaving at least a portion of the surface uncovered for receiving radiation, e.g., a finger grid metallic pattern can be disposed on the surface. In addition, the back surface of the substrate, the unstructured surface opposing the structured surface, can be coated, e.g., via evaporation, with a metallic coating. A load can be attached the wafer via electrical coupling to the metallic layers on the both sides of the wafer.

FIGURE 20 presents data comparing current-voltage (*I-V*) behavior of such a wafer, formed in a high resistivity (resistivity greater than about 1 ohm-m) silicon substrate, that can be utilized as a solar cell in the presence and in the absence of illumination. And FIGURE 21 presents a similar comparative data for a wafer formed in low resistivity silicon substrate (resistivity in a range of about 0.01 – 0.1 ohm-m). The

solar cell fabricated by employing the high resistivity substrate has an open circuit voltage of 0.4 volts and a short circuit current of 13.4 mA while the solar cell fabricated by utilizing the low resistivity substrate has an open circuit voltage of 0.31 volts and a short circuit current of 13.45 mA. It should be understood that this data is presented only for illustration purposes, and to show the possibility of utilizing a wafer microstructured in accordance with the teachings of the invention in forming a solar cell. However, this data is not intended to indicate optimal performance of a solar cell generated in accordance with the teachings of the invention. For example, the deposition of electrical contacts on the substrate can be optimized to obtain better performance than that described above.

In another application, a silicon wafer microstructured in accordance with the teachings of the invention can be utilized as a field emitter. In other words, an electric field can be applied to the microstructured surface to cause emission of electrons therefrom. To show the possibility of utilizing a microstructured wafer for generating field emission current, a number of prototype exemplary microstructured wafers were fabricated and field emission currents generated by them were measured. The experimental step-up for performing these measurements is shown schematically in FIGURE 22. A microstructured silicon sample 58 with a gold coating 60 evaporated on a back surface is mounted to a silicon wafer 62 having a gold coating 64, which functions as an anode, and is separated therefrom by a pair of mica spacers 66 and 68. The mounted sample is placed in a vacuum chamber, which is evacuated to a pressure of about 10^{-6} torr. A potential difference can be applied between the microstructured sample 58 and the gold-coated anode. And emission current can be measured at each applied voltage, e.g., via a picoammeter 70, a resistive elements 72 placed in series with the ammeter to protect it from unexpected surges in current.

FIGURE 23 shows exemplary results of field emission currents measured for silicon samples microstructured in SF_6. The typical figures of merit for a field emitting surface are turn-on-field, defined as the electric field (bias voltage divided by the tip-to-anode spacing) for which a current density of 0.01 microampere/mm^2 is observed, and threshold field, defined as the field at which a current density of 0.1 microamperes/mm^2 is produced. The turn-on field for a plurality of exemplary prototype substrates microstructured in SF_6 was measured as 1.3 V/micrometer, and the threshold field was

measured as 2.15 V/micrometer – excellent values that are on par with those exhibited by nanotubes.

Those having ordinary skill in the art will appreciate that various modifications can be made to the above embodiments without departing from the scope of the invention. It should also be understood that various exemplary data presented above are intended only for illustrating salient features of various aspects of the invention, and is not intended to limit the scope of the invention.

What is claimed is:

1. A method of fabricating a radiation-absorbing semiconductor structure, comprising:

irradiating each of a plurality of locations on a surface of a silicon substrate with one or more femtosecond laser pulses while exposing said surface to a sulfur-containing substance so as to generate a plurality of sulfur inclusions in a surface layer of said substrate, and

annealing said substrate at a temperature in a range of about 500 K to about 1100 K for a time duration in a range of about a few seconds to about a few hours.

2. The method of claim 1, further comprising selecting a duration of each laser pulse to be in a range of about 50 femtoseconds to about 500 femtoseconds.

3. The method of claim 1, further comprising selecting a fluence of each pulse to be in a range of about 1 kJ/m^2 to about 15 kJ/m^2.

4. The method of claim 1, further comprising selecting a central wavelength of said laser pulses to be in a range of about 200 nm to about 800 nm.

5. The method of claim 1, wherein said irradiating step comprises exposing each location to a number of laser pulses ranging from 2 to about 500.

6. The method of claim 1, further comprising subjecting each of said surface locations to successive laser pulses separated from one another by a time interval in a range of about 1 microsecond to about 1 millisecond.

7. The method of claim 1, further comprising performing said annealing step in any of an inert atmosphere or a low-pressure atmosphere.

8. The method of claim 1, further comprising selecting said sulfur-containing substance to be any of SF_6 and H_2S.

9. The method of claim 1, wherein said semiconductor structure absorbs radiation having wavelength components in a range of about 0.25 to about 10 microns.

10. The method of claim 1, wherein said semiconductor structure absorbs radiation having wavelength components in a range of about 0.35 to about 2.5 microns.

11. The method of claim 1, wherein said semiconductor structure exhibits a substantially uniform absorption for wavelength components in a range of about 1.2 to about 2.5 microns.

12. A method of fabricating a photodetector, comprising:

forming a semiconductor structure absorbing radiation in a wavelength range of about 0.25 to about 3.5 microns and exhibiting a diodic current-voltage characteristic in said wavelength range, said forming step comprising:

irradiating a surface of a silicon substrate at one or more locations thereof with one or more laser pulses having short pulse widths while exposing said surface to a sulfur-containing gas to generate a micro-structured layer having sulfur inclusions,

annealing said substrate at a temperature in a range of about 500 K to about 1000 K for a time duration in a range of about a few seconds to about a few hours, and

depositing a plurality of metallic contacts on selected portions of said semiconductor structure to allow applying a reverse bias voltage thereto.

13. The method of claim 12, wherein said pulse widths are selected to be in a range of about tens of femtoseconds to about tens of nanoseconds.

14. The method of claim 12, further comprising selecting said sulfur-containing substance to be any of SF_6 and H_2S.

15. The method of claim 12, further comprising performing said annealing step in an inert atmosphere.

16. The method of claim 12, wherein said depositing step comprises thermally evaporating one or more selected metals on said selected portions of the semiconductor structure.

17. The method of claim 12, further comprising selecting a thickness of said metal contacts to be in a range of about 5 nm to about 100 nm.

18. The method of claim 16, wherein said depositing step comprises thermally evaporating a chromium layer followed by thermally evaporating a gold layer on a selected portion of said semiconductor structure to generate at least one of said metal contacts.

19. The method of claim 18, further comprising selecting a thickness of said chromium layer to be in a range of about 1 nm to about 5 nm.

20. The method of claim 19, further comprising selecting a thickness of said gold layer to be in a range of about 4 nm to about 100 nm.

21. The method of claim 12, further comprising configuring said metal contacts so as to ensure that at least a portion of said micro-structured layer remains capable of receiving an external radiation.

22. A method of fabricating a semiconductor structure, comprising

irradiating a plurality of locations on a surface of a silicon substrate with one or more laser pulses having pulse widths in a range of about 50 to about 500 femtoseconds while exposing said surface to a substance having an electron-donating constituent so as to generate a micro-structured surface layer comprising inclusions incorporating said electron-donating constituent, and

annealing said substrate at an elevated temperature in a range of about 500 K to about 1100 K for a selected time period.

23. The method of claim 22, further comprising selecting said electron-donating constituent to be any of chlorine (Cl_2), nitrogen (N_2) and air.

24. The method of claim 22, wherein said irradiating step further comprises directing said laser pulses at said surface along a direction substantially perpendicular to said surface.

25. The method of claim 22, wherein said selected annealing period is in a range of about a few seconds to about a few hours.

26. The method of claim 22, wherein said annealing step is performed in an inert atmosphere.

27. A method of fabricating a radiation-absorbing semiconductor wafer, comprising:

irradiating at least one surface location of a silicon substrate with a plurality of temporally short laser pulses while exposing said location to a substance having an electron-donating constituent so as to generate a substantially disordered surface layer incorporating a concentration of said electron-donating constituent, and

annealing said substrate at an elevated temperature and for a duration selected to enhance charge carrier density in said substantially disordered surface layer.

28. The method of claim 27, wherein said elevated temperature and duration are selected to cause re-arrangement of atomic bonds in said surface layer so as to increase concentration of carrier electrons in surface layer.

29. The method of claim 27, wherein said elevated temperature and duration are selected to enhance electron carrier density in the surface layer by a factor of about 10% to about 200% relative to a pre-annealing level.

30. The method of claim 27, wherein said elevated temperature and duration are selected to cause said surface layer to form a diode junction with underlying silicon substrate.

31. The method of claim 27, wherein said elevated temperature and duration are selected such that said annealed substrate exhibits a responsivity in a range of about 1 A/W to about 200 A/W upon exposure of said surface layer to radiation having wavelengths in a range of about 250 nm to about 1100 nm and application of a reverse bias in a range of about 0.1 V to about 15 V to said wafer.

32. The method of claim 27, wherein said elevated temperature is selected to be in a range of about 500 K to about 1100 K.

33. The method of claim 33, wherein said duration is selected to be in a range of about a few seconds to about few hours.

34. The method of claim 27, further comprising selecting said short laser pulses to have pulse widths in a range of about tens of femtoseconds to about tens of nanoseconds.

35. The method of claim 27, further comprising selecting a fluence of said pulses and a partial pressure of said substance having an electron-donating constituent such that the concentration of said electron-donating constituent incorporated in said surface layer ranges from about 0.5 to about 5 atom percent.

36. A method of fabricating a radiation-absorbing semiconductor wafer, comprising

irradiating at least one surface location of a silicon substrate with temporally short laser pulses while exposing the substrate to a substance having an electron-donating constituent so as to generate a microstructured surface layer having inclusions containing the electron-donating constituent, and

annealing the substrate at an elevated temperature and for a duration selected to enhance a responsivity of the microstructured substrate to radiation having at least one wavelength in a range of about 250 nm to about 1100 nm incident on the microstructured surface layer by at least a factor of about 10.

37. The method of claim 37, wherein the annealing temperature lies in a range of about 700 K to about 900 K.

FIG. 1

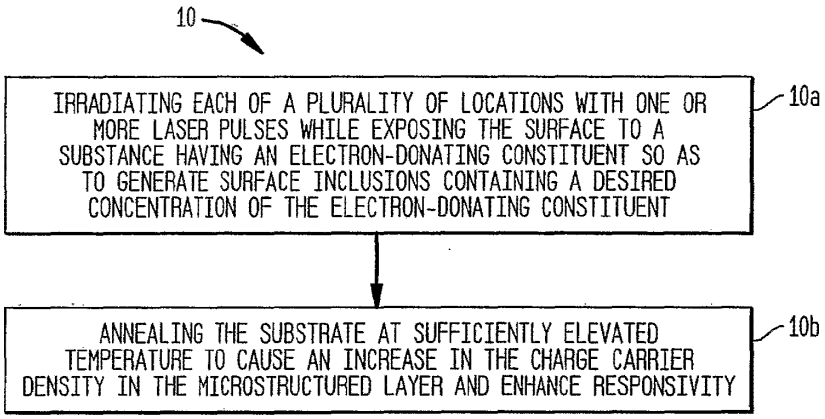

10
IRRADIATING EACH OF A PLURALITY OF LOCATIONS WITH ONE OR MORE LASER PULSES WHILE EXPOSING THE SURFACE TO A SUBSTANCE HAVING AN ELECTRON-DONATING CONSTITUENT SO AS TO GENERATE SURFACE INCLUSIONS CONTAINING A DESIRED CONCENTRATION OF THE ELECTRON-DONATING CONSTITUENT
10a
ANNEALING THE SUBSTRATE AT SUFFICIENTLY ELEVATED TEMPERATURE TO CAUSE AN INCREASE IN THE CHARGE CARRIER DENSITY IN THE MICROSTRUCTURED LAYER AND ENHANCE RESPONSIVITY
10b

FIG. 2

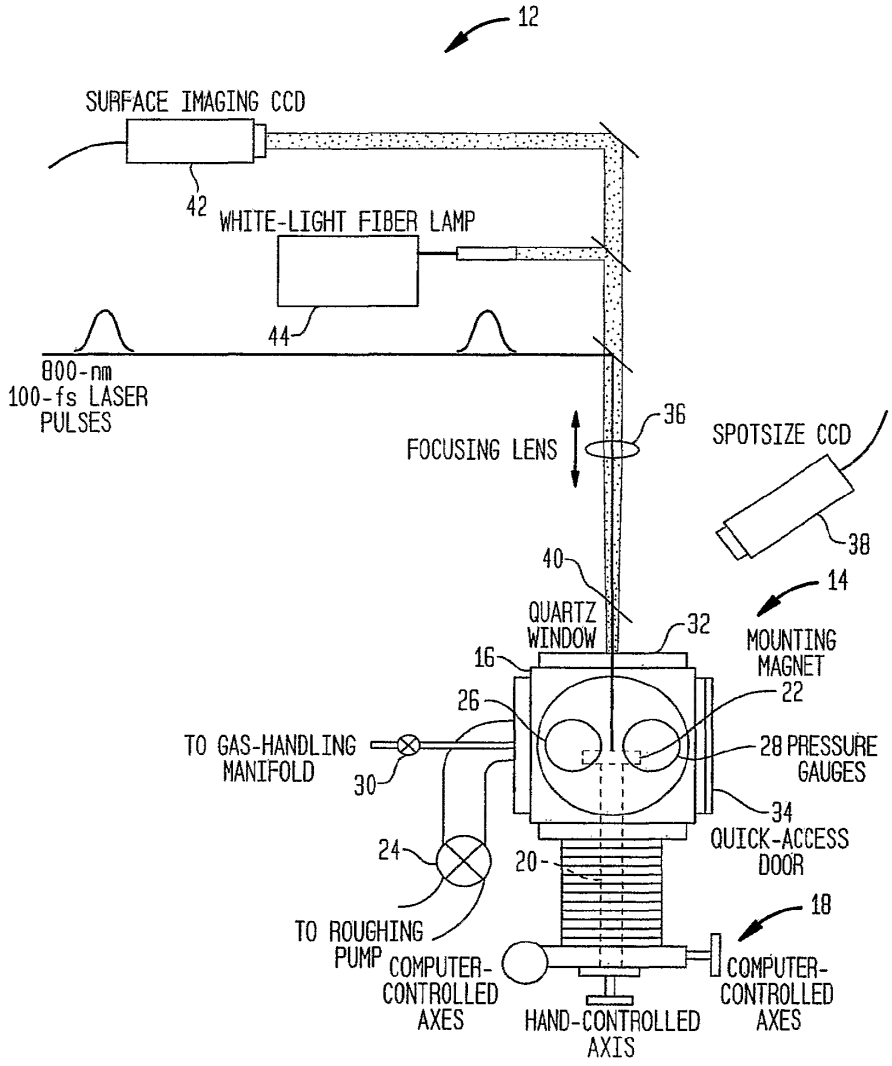

12
SURFACE IMAGING CCD
42
WHITE-LIGHT FIBER LAMP
44
800-nm
100-fs LASER
PULSES
FOCUSING LENS
36
SPOTSIZE CCD
38
40
14
QUARTZ
WINDOW
32
MOUNTING
MAGNET
16
22
26
TO GAS-HANDLING
MANIFOLD
30
28 PRESSURE
GAUGES
34
QUICK-ACCESS
DOOR
24
20
18
TO ROUGHING
PUMP
COMPUTER-
CONTROLLED
AXES
HAND-CONTROLLED
AXIS
COMPUTER-
CONTROLLED
AXES

FIG. 3

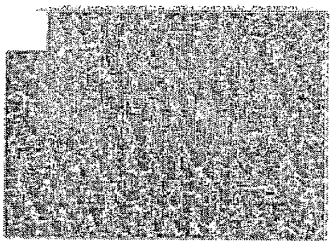


FIG. 4

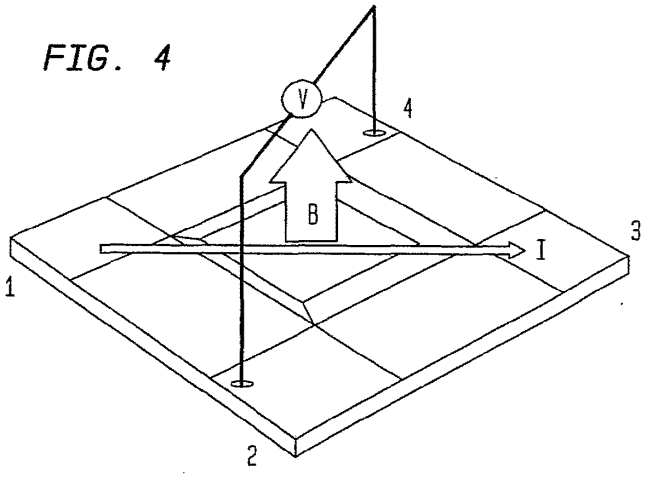

V
4
B
I
3
1
2

FIG. 5

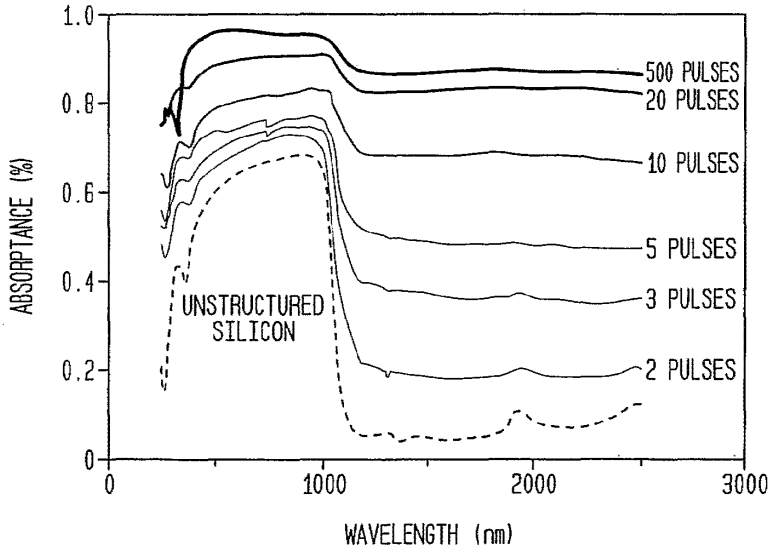

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
500 PULSES
20 PULSES
10 PULSES
5 PULSES
3 PULSES
2 PULSES
UNSTRUCTURED SILICON
0
1000
2000
3000
WAVELENGTH (nm)

FIG. 6

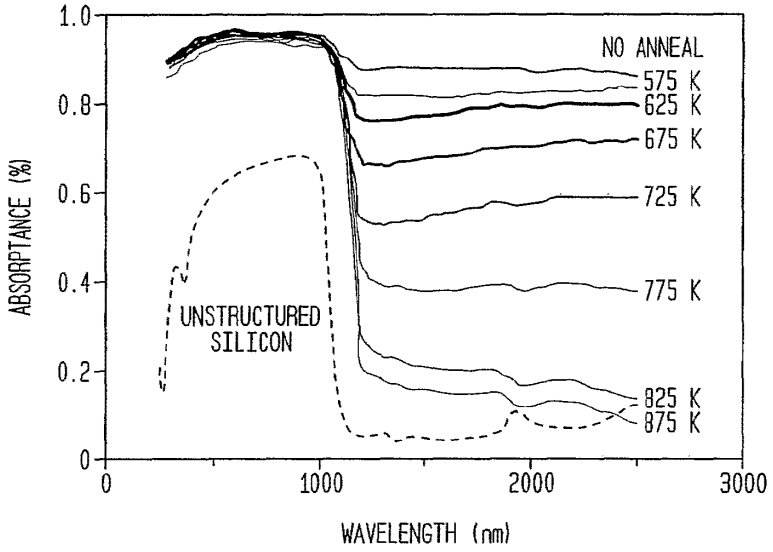

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
NO ANNEAL
575 K
625 K
675 K
725 K
775 K
825 K
875 K
UNSTRUCTURED SILICON
0
1000
2000
3000
WAVELENGTH (nm)

FIG. 7

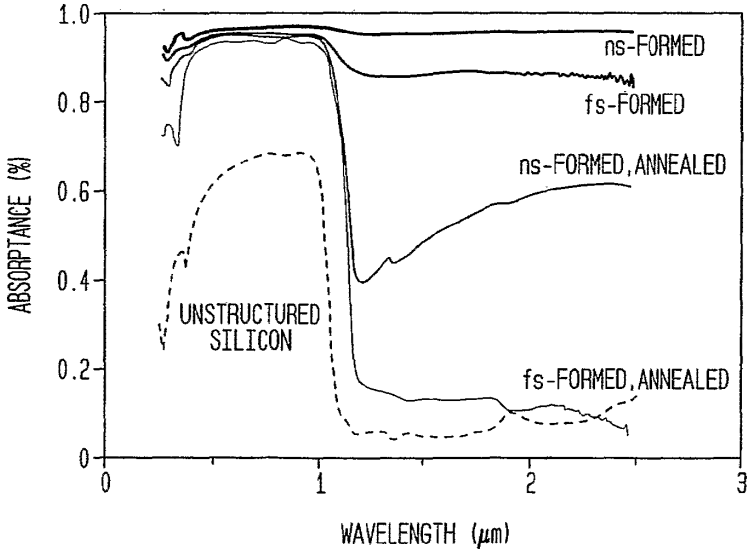

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
ns-FORMED
fs-FORMED
ns-FORMED, ANNEALED
UNSTRUCTURED SILICON
fs-FORMED, ANNEALED
0
1
2
3
WAVELENGTH (μm)

FIG. 8A

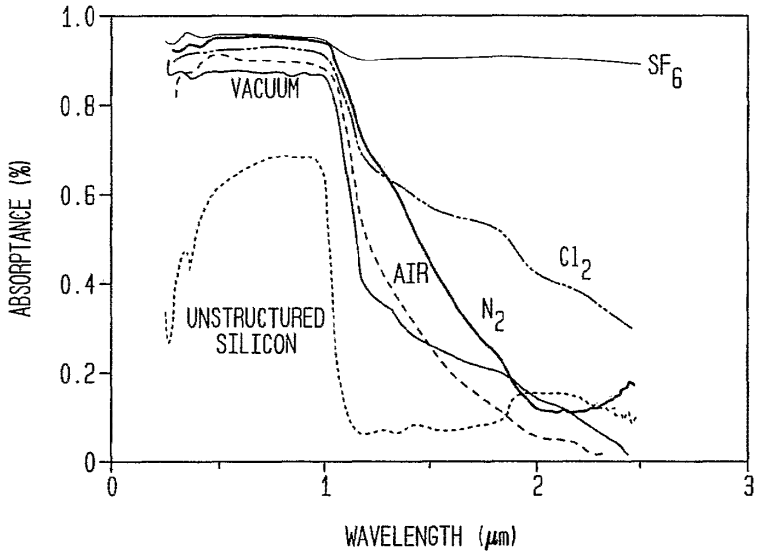

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
0
1
2
3
WAVELENGTH (μm)
VACUUM
SF6
Cl2
AIR
N2
UNSTRUCTURED
SILICON

FIG. 8B

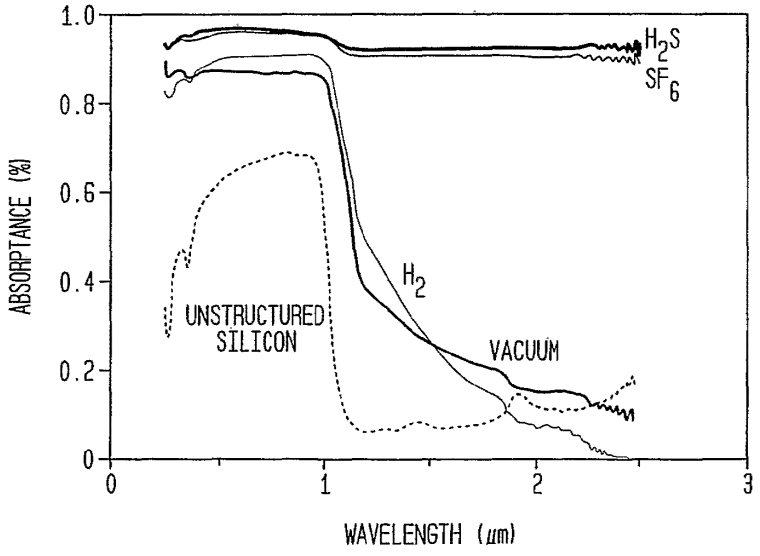

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
0
1
2
3
WAVELENGTH (μm)
H2S
SF6
H2
UNSTRUCTURED
SILICON
VACUUM

FIG. 9

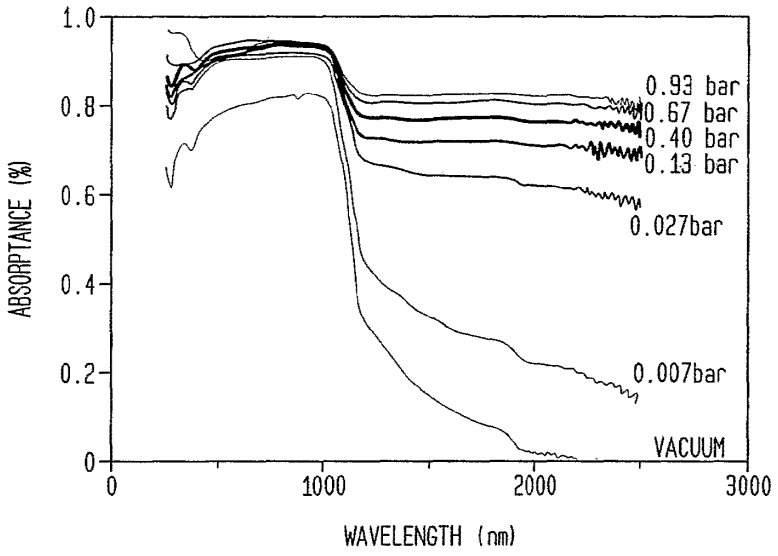

1.0
0.8
0.6
0.4
0.2
0
ABSORPTANCE (%)
0
1000
2000
3000
WAVELENGTH (nm)
0.93 bar
0.67 bar
0.40 bar
0.13 bar
0.027bar
0.007bar
VACUUM

FIG. 10

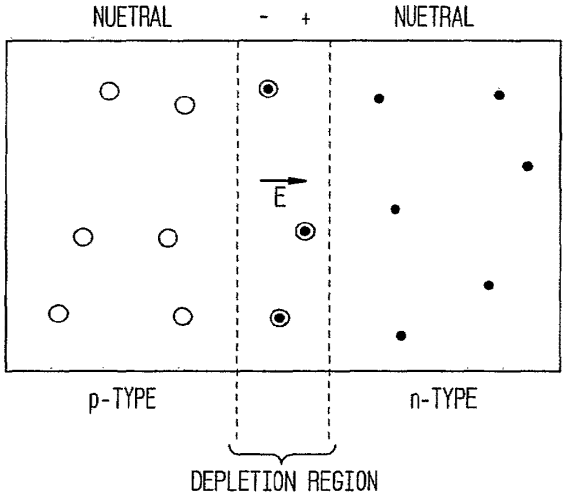

NUETRAL
-
+
NUETRAL
E
p-TYPE
n-TYPE
DEPLETION REGION

FIG. 11A

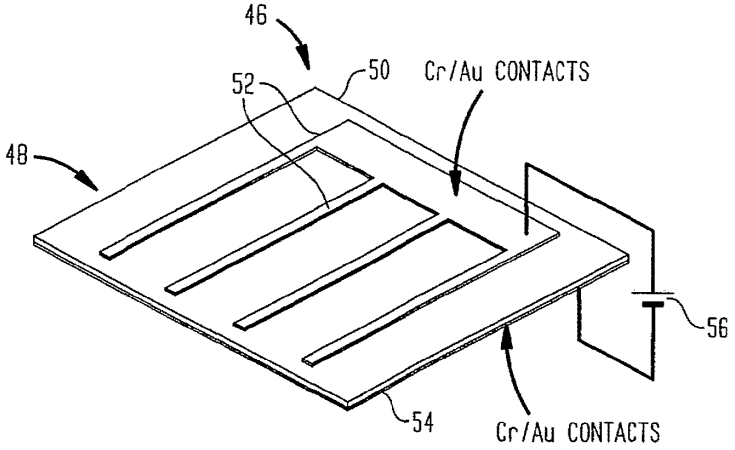


FIG. 11B

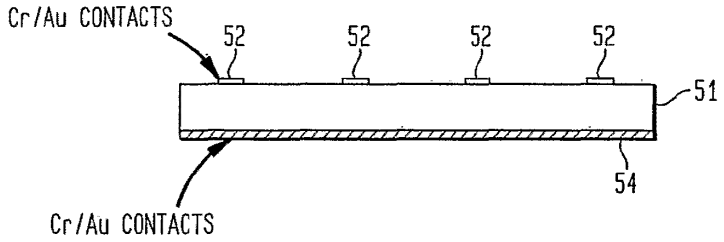


FIG. 12

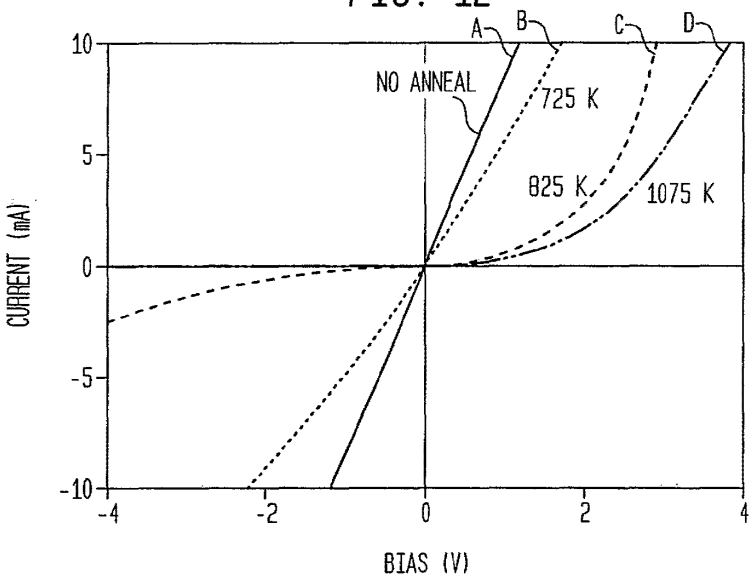

A
B
C
D
NO ANNEAL
725 K
825 K
1075 K
10
5
0
-5
-10
-4
-2
0
2
4
CURRENT (mA)
BIAS (V)

FIG. 13

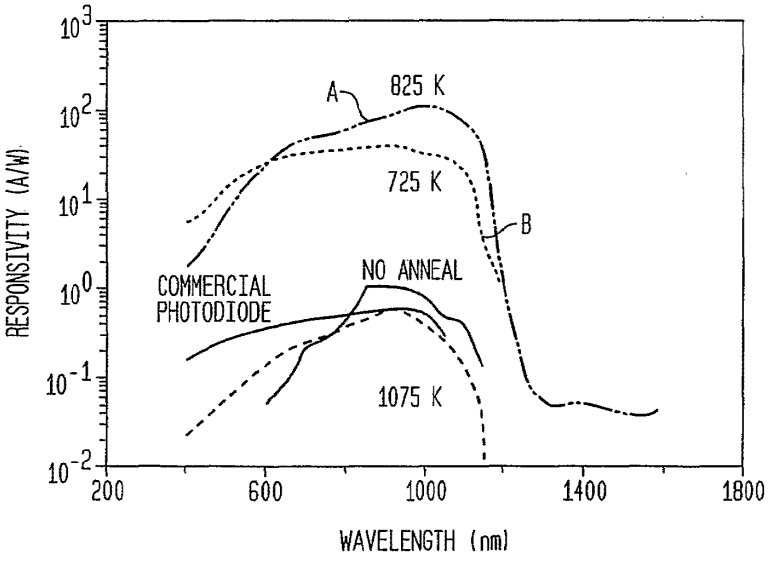

A
825 K
725 K
B
NO ANNEAL
COMMERCIAL
PHOTODIODE
1075 K
10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
200
600
1000
1400
1800
RESPONSIVITY (A/W)
WAVELENGTH (nm)

FIG. 14

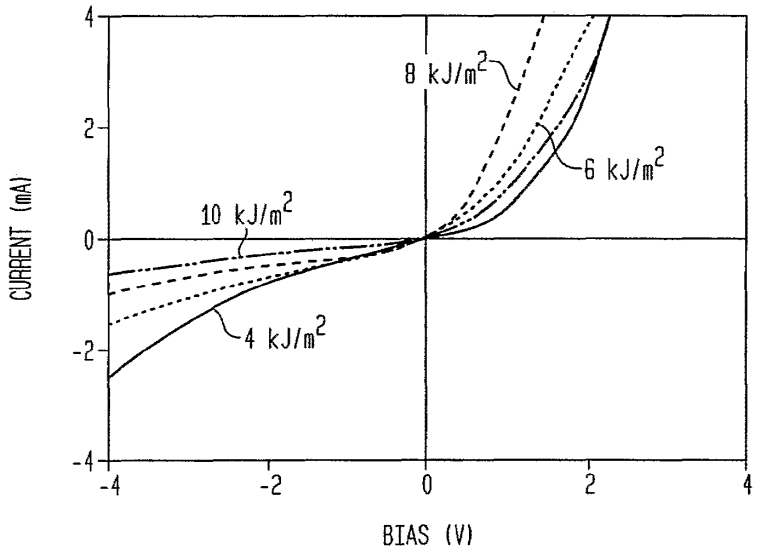


FIG. 15A

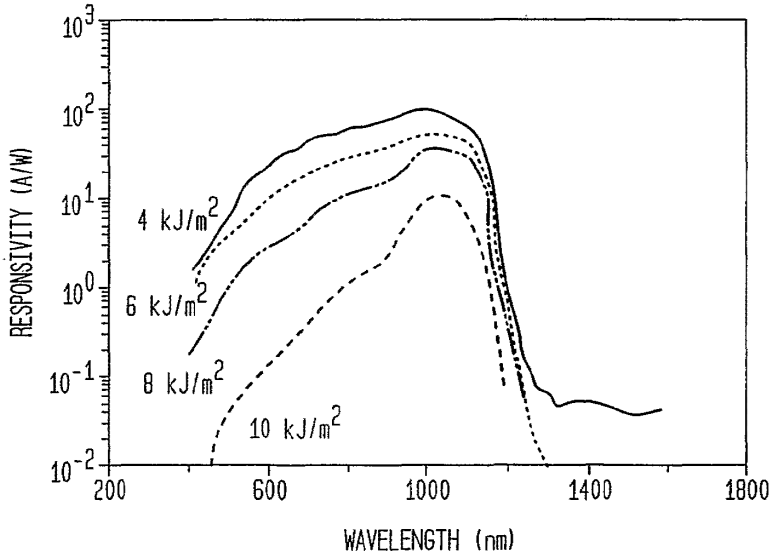


FIG. 15B

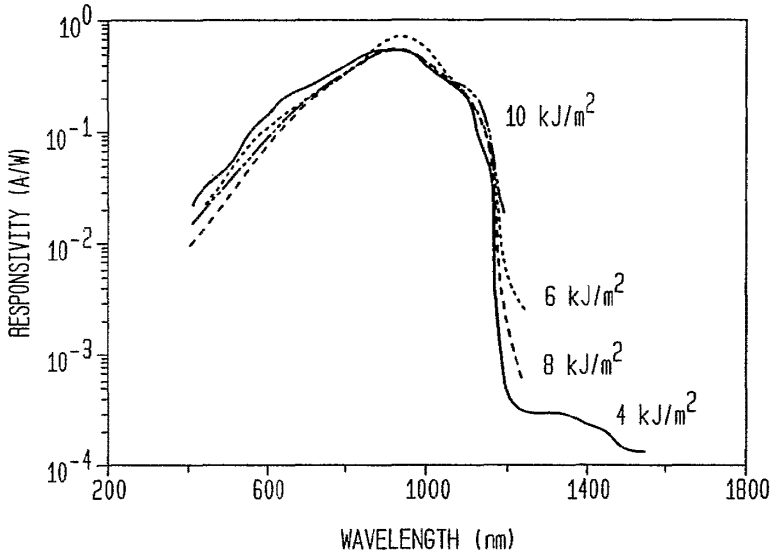


FIG. 16A

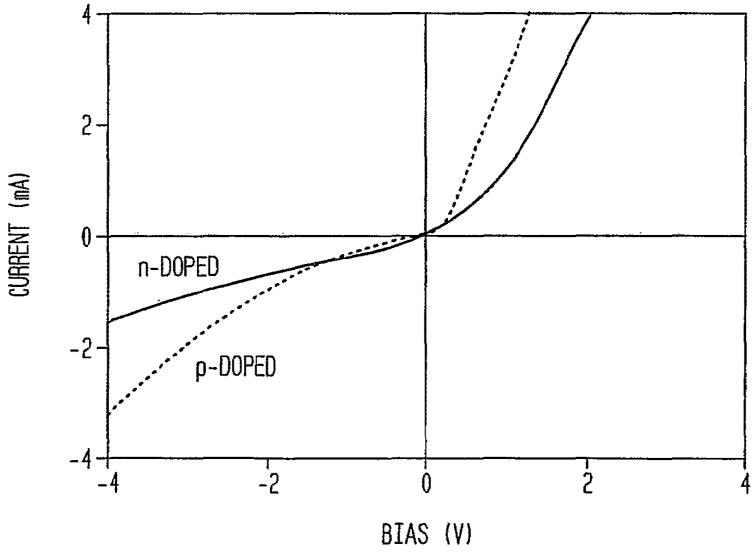


FIG. 16B

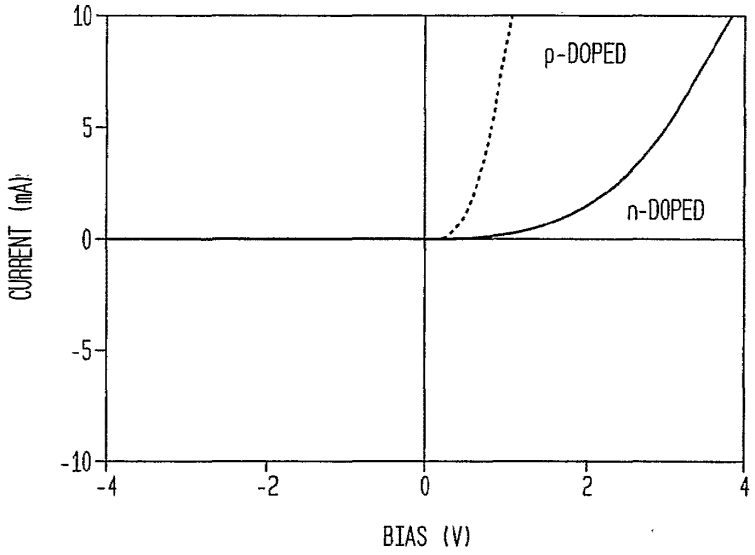


FIG. 17A

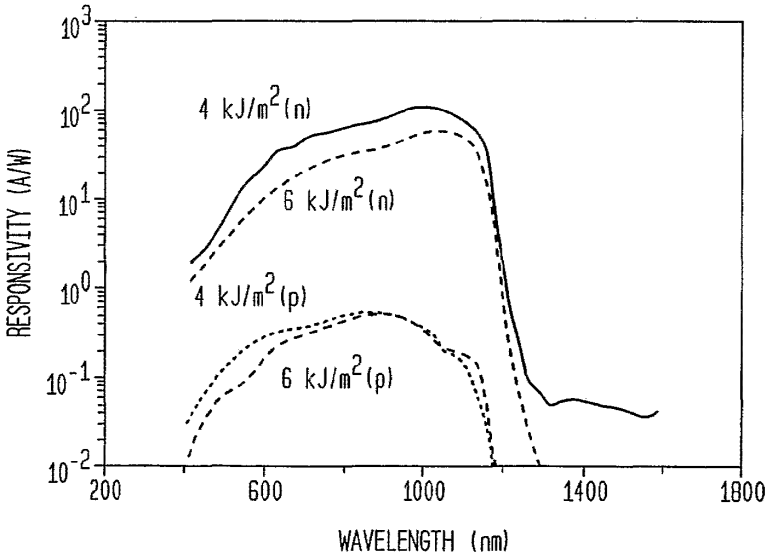


FIG. 17B

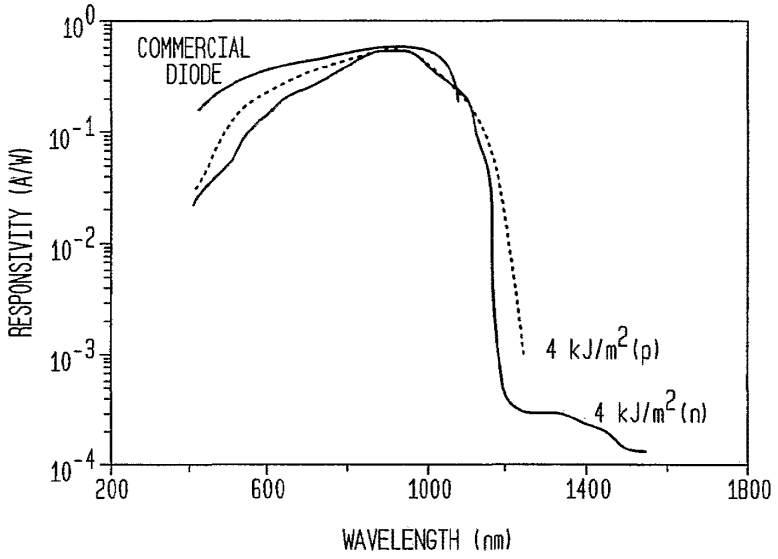


FIG. 18

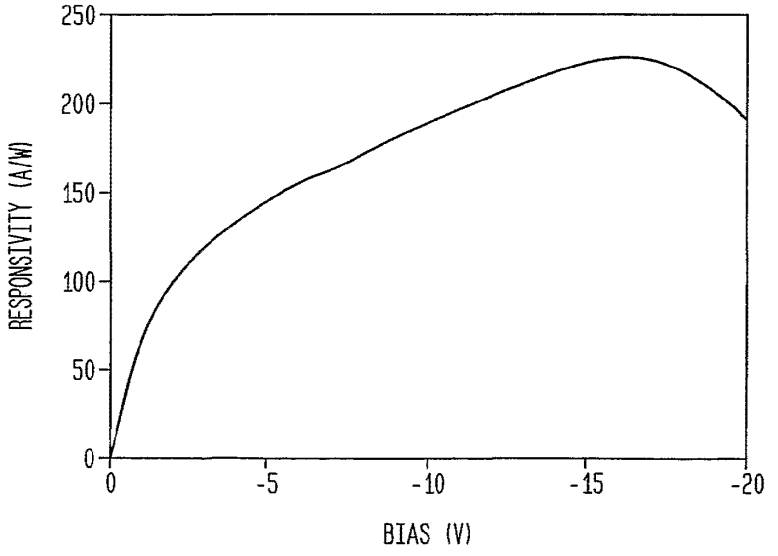


FIG. 19A

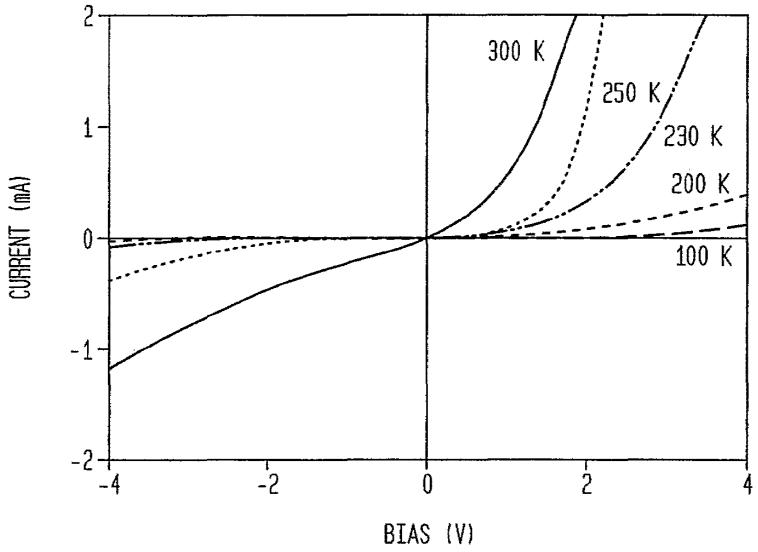


FIG. 19B

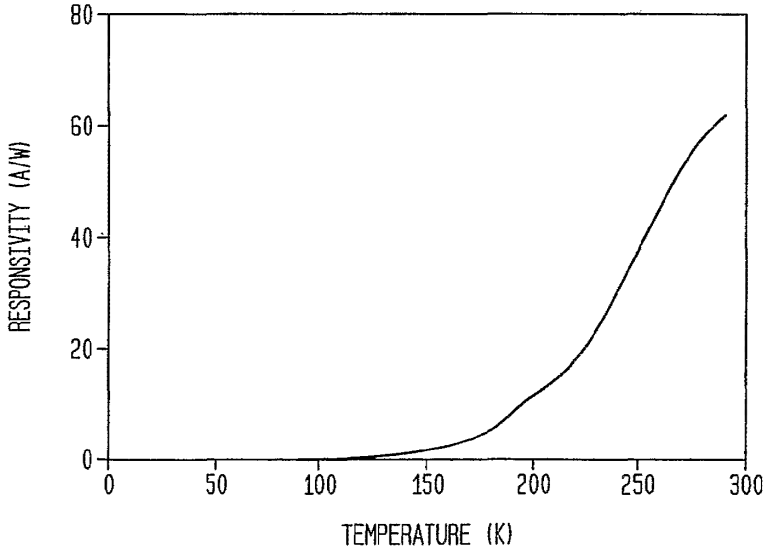


FIG. 20

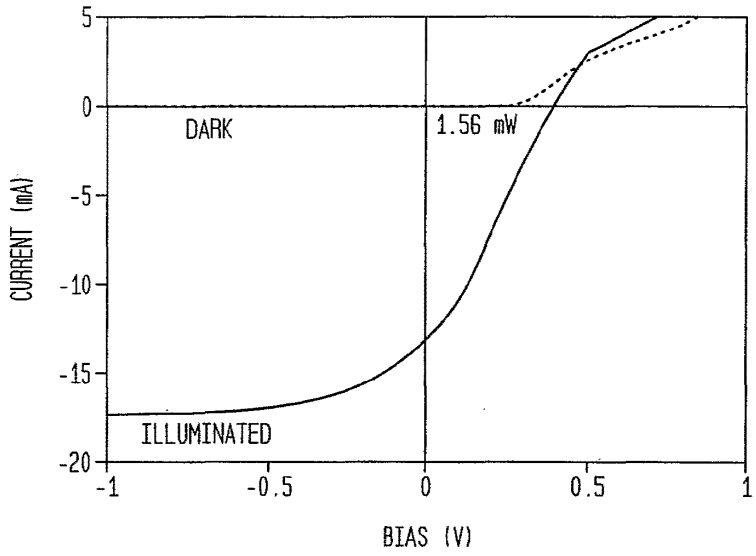

5
0
-5
-10
-15
-20
-1
-0.5
0
0.5
1
DARK
1.56 mW
ILLUMINATED
CURRENT (mA)
BIAS (V)

FIG. 21

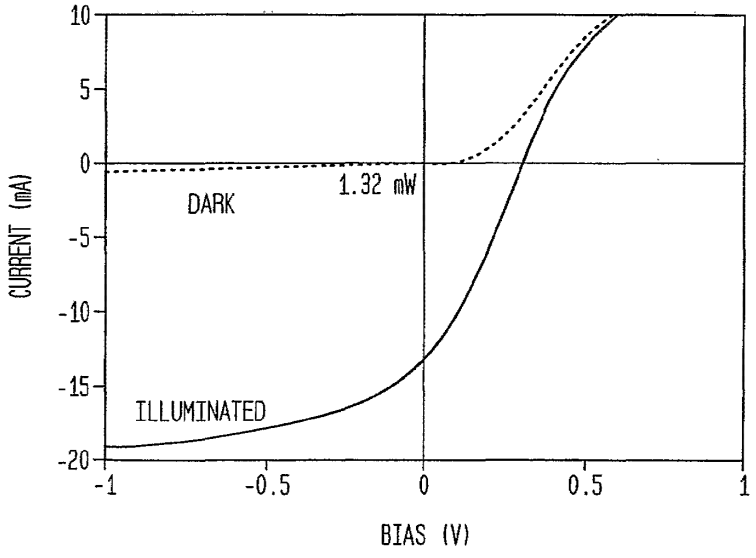

10
5
0
-5
-10
-15
-20
-1
-0.5
0
0.5
1
DARK
1.32 mW
ILLUMINATED
CURRENT (mA)
BIAS (V)

FIG. 22

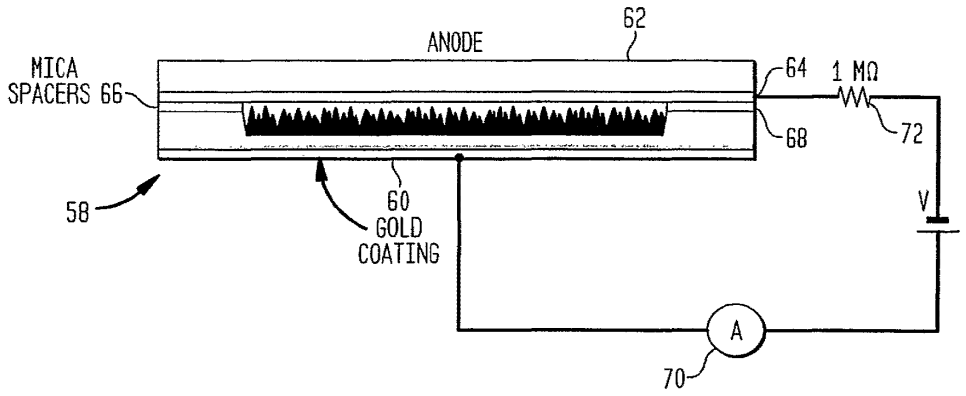
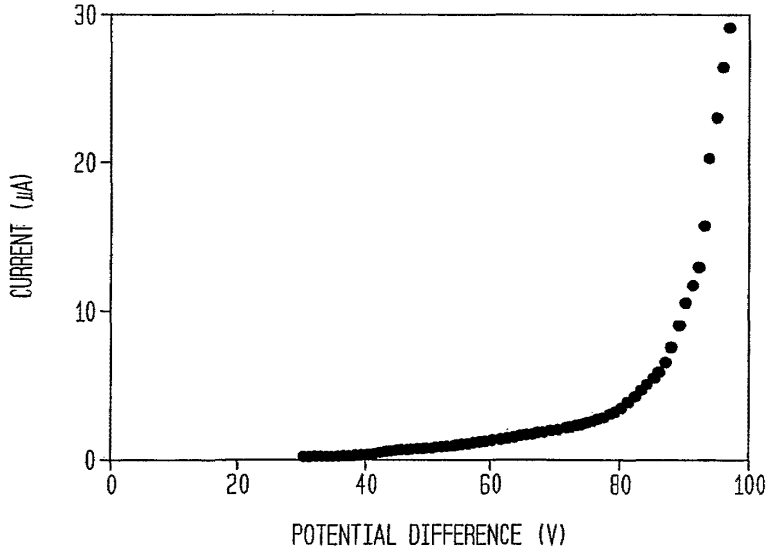

62
ANODE
MICA
SPACERS 66
64
1 MΩ
68
72
58
60
GOLD
COATING
V
A
70

FIG. 23


30
20
10
0
CURRENT (μA)
0
20
40
60
80
100
POTENTIAL DIFFERENCE (V)

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(74) Agents: **MOLLAAGHABABA, Reza** et al.; Nutter Mclennen & Fish Llp, World Trade Center West, 155 Seaport Boulevard, Boston, MA 02210-2604 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

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(54) Title: A MULTIJUNCTION PHOTOVOLTAIC DEVICE

(57) Abstract: Photovoltaic devices (e.g., solar cells) are disclosed that include at least three radiation absorbing layers, each capable of absorbing radiation over a different wavelength range of the solar radiation spectrum. Any two of these three wavelength ranges can be partially overlapping, or alternatively they can be distinct. The layers are disposed relative to one another so as to form two junctions, each of which includes a depletion region. In some cases, the radiation absorbing layers can collectively absorb radiation over a wavelength range that spans at least about 60%, or 70%, or 80%, and preferably 90% of the solar radiation wavelength spectrum. By way of example, in some embodiments, one layer can exhibit significant absorption of solar radiation (e.g., it can absorb at least one radiation wavelength at an absorptance greater than about 90%) at wavelengths less than about 0.7 microns while another layer can exhibit significant absorption of the solar radiation at wavelengths in a range of about 0.7 microns to about 1 micron. The third layer can in turn exhibit a significant absorption of solar radiation at wavelengths greater than about 1 micron.

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A MULTIJUNCTION PHOTOVOLTAIC DEVICE

Related Application

The present application claims priority to provisional application entitled "All Silicon Multijunction Photovoltaic (Solar Cell)" filed on February 1, 2008 and having a serial number 61/025,499 as well as provisional application entitled "A Multijunction Photovoltaic Device" filed on May 14, 2008 and having a serial number 61/053,080. Both of these provisional applications are herein incorporated by reference.

Background

The present invention relates generally to photovoltaic devices and methods for their fabrication.

Photovoltaic devices produce electric power via conversion of the planet's most abundant and renewable energy input: sunlight. Crystalline silicon solar cells are among the most mature and efficient photovoltaic technologies. Additionally, silicon is the second most abundant element in the earth's crust. Although silicon would seem as the premier candidate for renewable and environmentally friendly solar energy conversion, high manufacturing costs and a recent shortage of device grade silicon have prevented such cells from economically competing with the combustion of fossil fuels as a source of electricity on a large scale.

Hence, there is a need for enhanced photovoltaic devices as well as improved fabrication techniques, particularly as they relate to enhanced silicon photovoltaic cells.

Summary

Photovoltaic devices (e.g., solar cells) are disclosed that include at least three radiation absorbing layers, each capable of absorbing radiation over a different wavelength range of the solar radiation spectrum. Any two of these three wavelength ranges can be partially overlapping, or alternatively they can be distinct from each other. The layers are disposed relative to one another so as to form two junctions, each of which includes a depletion region. In some cases, the radiation absorbing layers can collectively absorb radiation over a wavelength range that spans at least about 60%, or about 70%, or about 80%, and preferably at least about 90% of the solar radiation

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wavelength spectrum. By way of example, in some embodiments, one layer can exhibit significant absorption of solar radiation (e.g., it can absorb at least one radiation wavelength at an absorptance greater than about 90%) at wavelengths less than about 0.7 microns while another layer can exhibit significant absorption of the solar radiation at wavelengths in a range of about 0.7 microns to about 1 micron. The third layer can in turn exhibit a significant absorption of solar radiation at wavelengths greater than about 1 micron.

In a related aspect, the photovoltaic device is configured such that at least a portion of a surface of one of the layers can be exposed to the solar radiation. In many embodiments, the layer that is capable of absorbing high energy photons (shorter wavelengths) is the first layer that receives the radiation. A portion of the radiation is absorbed by that layer and the remaining radiation passes through the other two layers, each of which in turn absorbs a portion of the radiation corresponding to its wavelength absorption range. The absorption of the solar radiation can generate electron-hole pairs. At least some of such electron-hole pairs can be separated under the influence of the electric fields present in the depletion regions associated with the junctions between the layers so as to generate a voltage across the device.

In some embodiments, the radiation absorbing layers can collectively absorb at least about 60%, or at least about 70%, or at least about 80%, or at least about 90%, of solar radiation incident on a portion of at least one of the layers that is adapted for exposure to solar radiation.

Two electrically conductive electrodes, one of which is electrically coupled to the upper layer and the other to the lower layer, can be employed to apply the voltage generated across the device, in response to exposure to the solar radiation, to an external load. By way of example, in some embodiments, the photovoltaic device includes a radiation transparent substrate (e.g., a substrate that allows the passage of at least about 50% of incident solar radiation) on which the radiation absorbing layers are disposed. Although the term substrate is used it should be appreciated that, in a typical embodiment, the substrate will be the uppermost element of the device, upon which the solar radiation impinges. A radiation transparent electrically conductive layer (e.g., a layer formed of indium tin oxide or zinc oxide) disposed between the electrically conductive transparent layer and the upper layer, which is in electrical contact with at

least a portion of the upper layer, forms one of the electrodes. The other electrode can be formed by a metallic layer disposed over at least a portion of the lower layer so as to form an electrical contact therewith.

As noted above, at least a portion of the electron-hole pairs generated in response to the exposure of the radiation absorbing layers to solar radiation can drift in opposite directions under the influence of the electric fields in the depletion regions to generate a voltage across the electrodes, which can be applied to an external load.

In a related aspect, the various layers of the above photovoltaic device can be formed of silicon doped with a suitable dopant. By way of example, in some cases, the upper layer includes a p-doped layer of amorphous silicon (e.g., a layer having a thickness in a range of about 10 nanometers (nm) to about 500 nm) while the intermediate layer includes an n-doped layer of crystalline or polycrystalline silicon (e.g. a layer having a thickness in a range of about 5 μm (microns) to about 50 μm). The lower layer can include a thin layer of highly doped silicon that includes a high concentration of an n-type dopant (e.g., an atomic concentration of at least about 0.1%, e.g., in a range of about 0.1% to about 2%) that can absorb radiation wavelengths greater than about 1 micron (or 1.1 microns corresponding to the band gap of crystalline silicon) with a high absorptance (e.g., greater than about 50%, and preferably greater than about 90%) to generate electron-hole pairs.

In another aspect, the invention provides a photovoltaic device (e.g., a solar cell), which comprises a first semiconductor layer capable of absorbing radiation at wavelengths greater than about 1 micron with an absorptance greater than about 60% for at least one of those wavelengths, and a second semiconductor layer capable of absorbing radiation at one or more wavelengths in a range of about 0.7 microns to about 1 micron, where the second layer forms a junction with the first layer. The photovoltaic device can further include a third semiconductor layer that is capable of absorbing radiation at wavelengths less than about 0.7 microns, e.g., in a range of about 0.25 microns to about 0.7 microns, where the third layer forms a junction with said second layer. Each junction can comprise a depletion region in which an electric field is present.

In another aspect, a method of fabricating a photovoltaic device is disclosed that includes forming a radiation transparent conductive layer, which can function as an electrode, over a surface of a radiation transparent substrate. A layer of amorphous silicon doped with a p-type dopant can then be formed, e.g., via plasma enhanced chemical vapor deposition, over the transparent conductive layer. A layer of crystalline or polycrystalline silicon can then be formed over the amorphous layer, e.g., via low pressure chemical vapor deposition. A plurality of short laser pulses (e.g., pulses having temporal durations in a range of about 100 femtoseconds to about 500 femtoseconds) can be applied to an exposed surface of the crystalline or polycrystalline layer (that is a surface opposed to the one that is in contact with the amorphous layer) while exposing the surface to a fluid (e.g., a liquid or gas) having an electron-donating constituent to form a thin highly doped surface layer (e.g., one having a thickness in a range of about 10 nm to about 1000 nm) that functions as another radiation absorbing layer of the cell. Subsequently, a metallic layer can be deposited over the disordered layer (e.g., by evaporating a metal onto a top surface of the disordered layer) so as to generate another electrode. The highly doped layer, which can in some cases be a crystalline or polycrystalline layer, can also be formed to have these high doping levels using other techniques that yield similar optical properties. These techniques include irradiating with a plurality of short laser pulses having longer durations, e.g., as long as 1 picosecond, or even as long as 1 nanosecond, to about 100 nanoseconds. Other techniques to implant large quantities of dopants can also be used.

Further understanding of the invention can be obtained by reference to the following detailed description in conjunction with the associated drawings, which are discussed briefly below.

Brief Description of Drawings

FIGURE 1 schematically depicts a photovoltaic cell in accordance with one embodiment of the invention,

FIGURE 2 shows the spectral irradiance of solar radiation as a function of wavelength at the earth above the atmosphere (solid line) relative to radiation from a black body at a temperature of about 5900 K (dashed line),

FIGURE 3A schematically depicts an exemplary implementation of the photovoltaic cell of FIGURE 1,

FIGURE 3B schematically depicts the photovoltaic cell of FIGURE 3A attached to a load,

FIGURE 4 depicts absorption of radiation by three layers of a hypothetical solar cell according to an embodiment of the invention over different wavelength ranges of the solar spectrum,

FIGURE 5 depicts schematically absorption of photons in various layers of a solar cell according to an embodiment of the invention,

FIGURE 6A schematically depicts absorption of photons in a conventional homojunction solar cell,

FIGURE 6B schematically depicts the thermalization energy loss of an electron of an electron-hole pair generated in a conventional homojunction solar cell,

FIGURE 6C schematically depicts that absorption of a photon in conventional homojunction solar cell can yield work corresponding to the energy associated with the band gap,

FIGURE 7 schematically depicts depletion regions associated with junctions between various layers of a solar cell according to an embodiment of the invention,

FIGURE 8A shows surface structures generated in a silicon substrate via exposure of the substrate to femtosecond laser pulses in presence of SF_6,

FIGURE 8B is a cross-sectional TEM image of one of the spikes shown in FIGURE 8A,

FIGURE 9 shows radiation absorptance as a function of wavelength exhibited by a laser-processed silicon substrate relative to that exhibited by unstructured silicon,

FIGURE 10 shows rectification exhibited by a junction formed between a surface layer formed in silicon substrate by application of short laser pulses in presence of SF_6 and the underlying silicon substrate, and

FIGURE 11 shows I-V curve of a prototype solar cell.

Detailed Description

The present invention generally provides a multi-junction photovoltaic device (e.g., a solar cell) that can include, e.g., a first, a second and a third radiation absorbing layer, each capable of absorbing radiation over a different wavelength range within the solar wavelength spectrum. The first and the second layer can have, respectively, p-type and n-type doping (or *vice versa*) and can contact one another, e.g., along a surface, to form a junction characterized by a depletion region. In some cases, the third layer can have the same type of doping as that of the second layer (e.g., both the second layer and the third layer can have an n-type doping) but at a different (e.g., higher) concentration level (e.g., at least about 1% atomic), or it can have a different type of doping, such that a junction it forms with the intermediate layer would also include a depletion region. The term "depletion region," also commonly known as "depletion layer" or "depletion zone," is known in the art and can be formed across a junction between two semiconductors (e.g., a p-n junction) having different concentrations of electrons or holes via diffusion of carriers from the semiconductor having a higher concentration to the other until an electric field generated across the junction impedes the diffusion, thus leading to the formation of a region that is substantially lacking in mobile charge carriers and supports an electric field.

FIGURE 1 schematically depicts a multijunction photovoltaic device 10, e.g., a solar cell, that includes three radiation absorbing layers (regions) 12, 14, and 16 that are disposed relative to one another to form two junctions A and B. For ease of description, the layers 12, 14, and 16 are herein referred to in some cases, respectively, as the upper (first), intermediate (second) and lower (third) layers. Each layer is formed of a

material, e.g., a semiconductor, in which electron-hole pairs can be generated in response to the absorption of optical radiation having suitable wavelengths. The layers are disposed on a support substrate 18, which can be formed of a suitable radiation transparent material such as glass. In many embodiments, the substrate 18 can allow the passage of at least about 50% of the sun's radiation, and preferably at least about 80% and more preferably at least about 90% of the incident sun's radiation. A radiation transparent electrically conducting layer 20, which functions as one of two electrodes for coupling a voltage generated across the cell in response to solar radiation to an external load, separates the radiation absorbing layer 12 from the support substrate 18 and forms electrical contact with that absorbing layer.

A metallic layer 22 disposed over the lower layer 16 provides another electrode that in combination with the electrode 16 can be utilized to apply a voltage generated across the device to an external load (not shown). As discussed in more detail below, upon exposure of the layers 12, 14 and 16 to solar radiation, electron-hole pairs can be generated in those layers. At least a portion of these electron-hole pairs can be separated under the influence of the electric fields associated with the junctions A and B to drift in opposite directions toward the electrode 20 or 22. In this manner, a voltage can be generated across the device.

By way of example, in some implementations of the multijunction solar cell 10, each of the radiation absorbing layers 12, 14 and 16 can show a significant absorption, e.g., an absorption greater than about 60% (e.g., in a range of about 60% to about 100%), for radiation in a different wavelength band of the solar radiation spectrum. In some cases, such wavelength bands can have overlapping portions and can collectively cover the wavelengths of the sun's radiation not only in the visible wavelength range but also in the infrared range. For example, the layers can be collectively capable of absorbing all radiation wavelengths over a span of the sun's radiation spectrum extending from about 250 nm to about 2500 nm.

The sun's radiation spectrum exhibits wavelengths that span a range of about 0.25 microns to about 2.5 microns, with significant decrease in intensity for wavelengths beyond this range. Accordingly, the term "solar wavelength spectrum," as used herein can refer to a wavelength range extending from about 0.25 microns to about 2.5 microns.

The solar spectrum can be approximated by that of a black body radiating at a temperature of about 5900 K. The spectral irradiance, M, emitted by a black body in the units of $Wm^{-2}\mu m$ is given by:

$$M = \frac{2\pi hc^2}{\lambda^5} \frac{1}{\exp[\frac{hc}{kT\lambda}]-1} \qquad \text{Eq. (1)}$$

where h is Planck's constant, c is the speed of light, k is the Boltzmann constant, T is the temperature of the black body in units of Kelvin (K) and λ is the wavelength in units of microns (μm).

By way of example, FIGURE 2 shows a solar radiation spectrum indicating solar radiation irradiance as a function of the radiation wavelength. In some implementations, the layers 12 can exhibit a high absorption of the solar radiation with wavelengths less than about 0.7 microns while the region 14 can exhibit a high absorption of the solar radiation with wavelengths in a range of about 0.7 microns to about 1 micron. The layer 16 can in turn show a high absorption of the solar radiation with wavelengths greater than about 1 micron, e.g., in a range of about 1 micron to about 2.5 microns. The term "high absorption" refers to an absorption of radiation with an absorptance greater than about 60%, or greater than about 70%, or preferably greater than about 80%, and more preferably greater than about 90% (e.g., near unity).

FIGURE 3A shows a multijunction solar cell 24 that corresponds to an exemplary implementation of the aforementioned solar cell 10 in which each of the layers 10, 12 and 14 is formed primarily of silicon (that is, it is formed of silicon in which some dopants are incorporated). More specifically, the solar cell 24 includes a radiation transparent support substrate 26 that extends from an external surface 26a that is adapted for exposure to solar radiation to an internal surface 26b on which a layer of a transparent conductor 28 is disposed. In this embodiment, the substrate 26 is formed of glass, though in other embodiments it can be formed of other materials such as transparent dielectrics (e.g. quartz) or plastics or polymers. The radiation transparent conductor layer 28 can be formed, for example, of indium tin oxide (ITO) or zinc oxide (ZnO).

The exemplary multijunction solar cell 24 further includes a radiation-absorbing layer 30 formed of p-doped amorphous silicon (αSi) that is disposed over the transparent conductor layer 28. The layer 30 can exhibit a thickness in a range of about 1 nm to about 1000 nanometers, and preferably in a range of about 10 nm to about 100 nanometers (e.g., about 50 nm). The doping level of the layer 30 can be, e.g., in a range of about 10^{14} cm^{-3} to about 10^{19} cm^{-3}, and preferably in a range of about 10^{16} cm^{-3} to about 10^{17} cm^{-3}. The layer 30 can be doped with a variety of p-type dopants, such as boron or aluminum or gallium.

Another radiation absorbing layer 32 is disposed over the layer 30 to form a junction J1 therewith, where the junction includes a depletion region. More specifically, in some embodiments the layer 32 can be formed of crystalline silicon (c-Si) or polycrystalline silicon (p-Si) that is appropriately doped. In this exemplary implementation, the layer 32 comprises polycrystalline silicon that is doped with an n-type dopant. The doping concentration of the layer 32 can be, for example, in a range of about 10^{12} cm^{-3} to about 10^{18} cm^{-3}, and preferably in a range of about 10^{14} cm^{-3} to about 10^{16} cm^{-3}. Further, the thickness of the layer 32 can be in a range of about 1 micrometer to about 500 micrometers, and preferably in a range of about 5 micrometers to about 50 micrometers (e.g., about 10 microns). The contact junction J1 formed between the layers 30 and 32 includes a depletion region. As discussed in more detail below, an electric field in the depletion region can facilitate the separation of the electron-hole pairs generated in that region or in vicinity thereof by incident solar photons. In some implementations, the layer 32 can be a thin layer having a thickness, e.g., in a range of about 1 micrometer to about 10 micrometers. In some cases, such a thin layer (e.g., a thickness in a range of about 1 mircon to about 10 microns) can exhibit an absorptance of about 25% or less in response to exposure to radiation wavelengths in a range of about 0.7 microns to about 1 micron.

In this embodiment, a thin highly-doped disordered layer 34 forms another junction J2 with the crystalline or polycrystalline layer 32 (in some other embodiments the heavily doped layer 34 can be crystalline exhibiting in some cases a highly ordered structure). Similar to the junction J1, the junction J2 can also include a depletion region that can facilitate the separation of electron-hole pairs generated by solar photons. As discussed in detail below, in some cases, the layer 34 can be fabricated by applying a

plurality of short laser pulses to the top surface of the underlying layer 32 while exposing the surface to an electron-donating compound (e.g., SF_6). The layer 34 can have a thickness in a range of about 10 nm to about 1000 nm, and preferably in a range of about 50 nm to about 200 nm. In many implementations, the layer 34 includes a high level of n-doping (e.g., at an atomic concentration of at least about 1%) so as to exhibit a higher n-type doping concentration level than that of the underlying layer 32.

As discussed in more detail below, in this embodiment, the highly-doped silicon layer 34 can absorb radiation with wavelengths greater than about 1 micron (e.g., greater than about 1.1 microns) with an absorptance significantly greater than that exhibited by crystalline silicon at those wavelengths. While crystalline silicon exhibits a precipitous drop in radiation absorption for wavelengths greater than that corresponding to its bandgap (e.g., greater than about 1.1 microns), the highly-doped silicon layer can exhibit in some cases near unity absorptance (e.g., an absorptance greater than about 90%) for those radiation wavelengths.

The absorption characteristics of the three layers 30, 32 and 34 in the exemplary multijunction solar cell 24 can allow the cell to absorb the incident solar photon flux over a wide wavelength range. By way of illustration, FIGURE 4 shows a plot indicating the absorption of solar photons by different layers 30, 32, and 34 of a hypothetical implementation of the solar cell 24, illustrating the number of photons absorbed by each of those layers (it should be understood that this figure is presented only for illustrative purposes and is not intended to necessarily indicate the optimal radiation absorption characteristics of a multijunction solar cell in accordance with the teachings of the invention). The plot shows the photon flux (number of photons per unit area) at a given energy in the AM1.5 solar spectrum. The area under the curve represents the number of photons in a given energy range. The amorphous silicon layer can absorb photons with energies greater than about 1.7 eV, while the polycrystalline or crystalline silicon layer can absorb photons with energies greater than about 1.1 eV. The highly-doped disordered layer (in some cases the highly-doped layer is not disordered) can in turn absorb photons with energies greater than about 0.5 eV. In some cases, the highly-doped layer can absorb photons with energies greater than about 0.25 eV.

Referring again to FIGURE 3A, a thin metallic layer 36 is disposed over the thin layer 34. The metallic layer 36 together with the aforementioned radiation transparent conductive layer 28 allow extracting a voltage from the solar cell 24 to be applied to an external load 38, as shown schematically in FIGURE 3B, and discussed in more detail below.

In use, upon exposure of the multijunction solar cell 24 to solar radiation, incident solar photons pass through the glass substrate 26 and the transparent conductor to be incident on the amorphous silicon layer 30. A portion of these photons are absorbed by the amorphous silicon layer so as to generate electron-hole pairs. The photons absorbed by the amorphous layer 30 are typically high energy photons, e.g., photons having energies greater than an energy corresponding to the band gap of amorphous silicon (e.g., 1.7 eV).

The remaining photons, or at least a large portion of them, enter the polycrystalline (or crystalline) layer 32. These photons have typically lower energy as many of the higher energy photons were previously absorbed by the amorphous layer 30. For example, many of these photons can have energies in a range of about 1.1 eV to about 1.7 eV. The absorption of these photons can also lead to the generation of electron-hole pairs. Finally, those photons that were not absorbed by the layers 30 and 32 reach the highly-doped layer 34 and are absorbed by that layer (at least a portion of those photons are absorbed by the layer 34) to generate additional electron-hole pairs. The energies of many of these photons lie in a range less than about 1.1 eV. In many implementations, the layer 34 exhibits micron-sized surface undulations that can help in trapping photons. In addition, the metallic layer 36 can reflect photons not absorbed by the radiation absorbing layers back to those layers.

Hence, the multijunction solar cell 24 absorbs photons over substantially the entire range of the solar radiation spectrum. Such absorption of photons corresponding to different wavelength ranges of the solar spectrum is schematically shown in a graph in FIGURE 5 for a hypothetical multijunction solar cell according to the teachings of the invention. The graph schematically indicates each material with its associated band gap (for example, in the solar cell shown in FIGURE 5, Material 1 corresponds to amorphous silicon, Material 2 corresponds to crystalline or polycrystalline silicon and Material 3 corresponds to a highly-doped disordered layer). The graph shows that the

band gap of the three material progressively decreases such that the photons having higher energies are absorbed primarily in Material 1 to generate electron-hole pairs while lower energy photons are absorbed in the Materials 2 and 3 (in cases where a surface of Material 1 is exposed to solar radiation, high energy photons, which can be absorbed near the surface, can suffer less thermalization loss). Many device details, such as the bending of the bands at the junctions, are not shown in this figure.

By way of contrast, FIGURES 6A-6C schematically show the absorption of solar photons in a hypothetical homojunction photovoltaic cell (e.g., a solar cell). FIGURE 6A shows that only those photons having energies that are at least equal to that of the band gap can be absorbed. All absorbed photons yield about ε_{gap} of work, as shown schematically in FIGURE 6C. But many low energy photons are not absorbed. Further, some energy from high energy photons are lost to lattice thermalization (e.g., FIGURE 6B schematically shows energy (ε_{th}) lost by an electron of an electron-hole pair generated by a high energy photon to the lattice). By way of example, in a near ideal silicon homojunction material, photons representing more than about 20% of the solar energy are not absorbed and about 30% of the energy of the absorbed photons is lost to heat.

Referring again to FIGURE 3A, the junctions J1 and J2 include depletion regions. These depletion regions are shown schematically in FIGURE 7 as regions DP1 and DP2. The electron-hole pairs generated in each of the two depletion regions or in vicinity thereof are separated by the electric field present in the depletion regions to drift towards the upper or the lower conductors 36 and 28. Some of such electrons and holes are lost to electron-hole recombination events, while others are lost to non-radiative recombination at traps, and still others may be lost to Auger recombination. Those that reach the respective upper and lower metal electrodes can provide a voltage across the cell that can be applied to an external load, such as the light bulb shown in FIGURE 3B.

In some embodiments, the highly-doped layer exhibits not only a high doping concentration level but also good charge carrier mobility so as to minimize electron-hole recombination events and scattering. By way of example, the electron mobility in the highly doped layer 34 can be greater than about 500 $cm^2/V \cdot s$, e.g., in a range of about 100 $cm^2/V \cdot s$ to about 1000 $cm^2/V \cdot s$. As discussed in more detail below, in some cases the fabrication of the highly-doped layer can include a high-temperature annealing

protocol to ensure high electron mobility in that layer.

A variety of techniques can be employed to fabricate the multijunction solar cell 24. By way of example, in one such fabrication method, the transparent conductive electrode can be formed on a surface of glass substrate, e.g., by radio frequency sputtering from an indium tin oxide (ITO) target. Subsequently, the amorphous silicon layer can be grown on the exposed surface of the transparent metal electrode, in a manner known in the art, for example by decomposition of silane gas (SiH_4) in plasma enhanced chemical vapor deposition. Similarly, the crystalline or polycrystalline layer is grown on the amorphous layer. By way of example, thin films of amorphous and microcrystalline silicon can be produced by plasma-enhanced chemical vapor deposition using a mixture of silane (SiH_4) and hydrogen gases. The films can include a substantial amount of hydrogen (e.g., 5-20 at. %). Amorphous silicon films can be fabricated by utilizing pure silane while crystalline grains can be fabricated via high dilution in hydrogen. The degree of crystallinity can be varied by varying the concentration of silane, e.g., in a range of about 4.5% to about 8%. For example, in some cases, at a concentration of about 4.5%, the film can exhibit a high degree of crystallinity with an average grain size of, e.g., about 25 microns. Amorphous and microcrystalline silicon can be doped with a suitable n-type and p-type dopant, such as phosphorous or boron, during the deposition process. Polycrystalline films are also commonly grown via low-pressure chemical vapor deposition, via thermal decomposition of silane gas in a tube furnace.

The highly-doped layer 34 can then be generated by applying short radiation pulses to the exposed surface of the crystalline or polycrystalline layer 32 while the surface is exposed to an electron-donating compound (e.g., sulfur hexafluoride gas), as discussed in more detail below. It can also be generated via other techniques for implanting impurities beyond the solid solubility limit. Finally, the metallic electrode can be formed over the disordered layer 34, e.g., by evaporating a metal over that layer.

As discussed above, in this exemplary embodiment, the layer 34 is in the form of a disordered layer formed primarily of silicon in which a large quantity of an electron-donating dopant, e.g., sulfur, is incorporated. As noted in more detail below, such a layer can be formed by irradiating a silicon surface with short radiation pulses (e.g., pulses having temporal durations in a range of about 10 femtoseconds (fs) to about a few

hundred nanoseconds) while exposing to the surface to an electron-donating constituent (e.g., SF_6). Such processing of silicon can generate the disordered layer 34 with a thickness, e.g., in a range of 10 nanometers to about 1000 nanometers, which exhibits not only significant absorption in the visible radiation wavelengths but also at wavelengths that are larger than that corresponding to the band gap of silicon (e.g., at wavelengths greater than about 1.1 microns).

By way of example, in some embodiments, the layer 34 can be fabricated by applying radiation pulses having temporal durations in a range of about 10 fs to about 500 fs (though longer pulse widths can also be utilized) and having wavelengths in a range of about 400 nm to about 800 nm to a surface of a crystalline silicon substrate; longer and shorter wavelengths can be used, for example from about 200 nm to wavelengths of several microns, e.g., 5 microns. The fluence (energy per unit area) of the pulses at the substrate surface can be, e.g., in a range of about 1 kJ/cm^2 to about 40 kJ/cm^2. In some cases, the substrate is moved relative to the radiation beam (or *vice versa*) such that different areas of the surface are irradiated with the pulses. The rate of movement of the substrate can be selected such that each irradiated area is exposed to a plurality of pulses, e.g., in a range of about a few tens to a few thousands (e.g., 500 pulses).

In some embodiments, the irradiation of the surface with the pulses is performed while the surface is exposed to a dopant chosen, e.g., from heavy chalcogens (e.g., sulfur, selenium, and tellurium). Without being limited to any particular theory, the train of the pulses can cause ultrafast melting of the substrate's lattice so as to yield a resolidification front that moves very fast, and can trap foreign atoms (e.g., sulfur) in its vicinity with a surface layer of the substrate at concentration levels that substantially exceed the respective solid solubility limit. These foreign atoms can be introduced in a variety of ways. For example, the substrate surface can be irradiated with the short (e.g., femtosecond) pulses while the surface is exposed to sulfur hexafluoride gas (e.g., the irradiation can be done in the presence of 500 torr sulfur hexafluoride gas). As another example, when doping the substrate with selenium or tellurium, a film of selenium or tellurium (e.g., a 100-nm film) can be thermally evaporated onto the substrate surface and then the coated surface can be irradiated with the short laser pulses.

The resulting substrate surface can exhibit micron-scale or sub-micron scale morphologies depending on the conditions utilized. By way of example, FIGURE 8A quasi-ordered array of microspikes that are about 1 – 15 microns tall and spaced by about 1 – 5 microns that were generated in a surface layer of a silicon substrate by exposing the surface to 100-fs laser pulses having a central wavelength of 800 nm and a fluence of about 8 kJ/m^2. Each area of the surface was exposed to about 600 pulses. A cross-sectional transmission electron microscopy (TEM) image of one of the spikes shown in FIGURE 8B reveals a doped, 300-nm thick polycrystalline disordered surface layer. In particular, the X-ray diffraction pattern shown in the inset of FIGURE 8B indicates that the disordered layer is in fact polycrystalline. Further, Rutherford backscattering data (not shown) indicates that the polycrystalline layer exhibits about 1% atomic doping, and diffraction studies reveal an average grain size of about 30 nm.

Further details regarding various ways of generating a doped surface layer by exposing a substrate surface to short laser pulses can be found U.S. Published Patent Application No. 2003/0029495 entitled "Systems and Methods for Light Absorption and Field Emission Using Microstructured Silicon," U.S. Published Patent Application No. 2006/0079062 entitled "Femtosecond Laser-Induced Formation of Submicrometer Spikes On a Semiconductor Substrate," U.S. Patent No. 7,057,256 entitled "Silicon-based Visible and Near-infrared Optoelectronic Devices," pending U.S. Patent Application No. 12/038209 entitled "Laser-Induced Structuring of Substrate Surfaces," each of which is herein incorporated by reference in its entirety. The present application also incorporates by reference a thesis entitled "Femtosecond Laser Ablation of Silicon: Nanoparticles, Doping and Photovoltaics," which was presented to Harvard University by Brian Tull in 2007.

The morphology of the disordered surface layer, e.g., characterized by a disordered array of microspikes, can be distinct from doping of the layer. For example, adjusting laser parameters (e.g., fluence) as well as the distribution of laser pulses over the surface can be employed to enhance or reduce the sizes of the surface features while still providing a requisite degree of doping (e.g., 1% atomic concentration). In some cases, the spikes or similar surface features generated by laser processing of the substrate can be used to amplify absorption of solar radiation incident on the surface due to multiple reflections. In other cases, it may advantageous to fabricate a highly doped

disordered surface layer that exhibits a substantially smooth top surface. By way of example, an international (PCT) application entitled "Engineering Flat Surfaces on Material Doped Via Femtosecond Laser Irradiation", which is concurrently filed herewith and is herein incorporated by reference in its entirety, describes a method of processing a substrate by irradiating at least a portion of the substrate surface with a plurality of short radiation pulses while exposing the surface to a dopant. The pulses are selected to have a fluence at the substrate surface that is greater than a melting fluence threshold and less than an ablation fluence threshold. In this manner, a quantity of the dopant can be incorporated into the substrate while ensuring that the roughness of the substrate's surface is significantly less than the wavelength of the applied radiation pulses.

Although the above description relates to generating a highly doped layer in crystalline silicon, the methods discussed above can be employed to generate such doping layers in amorphous silicon (e.g., in thin films of amorphous silicon) or other semiconductors by exposing them to short laser pulses in the presence of a dopant.

The radiation absorbing layer 34 generated by the above methods can exhibit a substantially uniform absorption of electromagnetic radiation incident thereon from ultraviolet to the near-infrared (e.g., in a range of about 250 nm to about 2500 nm). As such, it can be particularly useful in absorbing the solar radiation at wavelengths greater than about 1.1 microns, where crystalline silicon shows very low absorption. By way of illustration, FIGURE 9 shows the radiation absorptance as a function of wavelength for a highly doped surface layer formed in silicon via application of 100-fs pulses at a central wavelength of about 800 nm and a fluence of about 8 kJ/m^2 (each area was exposed to about 500 pulses), indicating a near-unity absorptance over a wide range of wavelengths. In contrast, as shown in the figure, the absorptance exhibited by a crystalline silicon substrate drops precipitously for wavelengths greater than about 1.1 microns.

Moreover, the highly-doped layer can form a diode junction with the underlying substrate that can be characterized by a depletion region. That is, in many cases, the dopant atoms are not only optically active but they can also act as electron donors. In some embodiments, subsequent to irradiation of substrate with laser pulses in the presence of a dopant, the substrate (and consequently the generated highly doped surface

layer) is annealed at an elevated temperature (e.g., at 900 K for about 30 minutes) to facilitate the formation of a diode junction between the doped surface layer and the underlying substrate. Such an annealing step is further discussed in Published U.S. Patent Application No. 2008/0044943 entitled "Manufacture of Silicon-based Devices Having Disordered Sulfur-doped Surface Layers," which is incorporated herein by reference in its entirety.

By way of illustration, FIGURE 10 shows that a junction between a surface layer formed in a silicon substrate by application of 100-fs pulses (800 nm central wavelength at a fluence of 8 kJ/m^2) and the underlying substrate demonstrates rectification. Additionally, regardless of the original substrate doping, room-temperature Hall measurements performed on a number of silicon substrates in which such highly doped surface layers are generated demonstrate a negative charge carrier concentration in a range of about 10^{19} to about 10^{20} cm^{-3} in that layer.

A multijunction photovoltaic cell according to the teachings of the invention can provide a number of advantages relative to conventional multijunction photovoltaic cells. For example, a multijunction photovoltaic cell of the invention can utilize a significant portion of the solar wavelength spectrum for generating electron-hole pairs. In addition, it can be fabricated by utilizing abundant raw materials and known techniques. In contrast, conventional cells typically include a combination of exotic materials that are expensive, both to acquire as raw materials as well as to incorporate into a device.

The following example is provided for illustrative purposes to generally indicate the feasibility of utilizing a highly-doped disordered layer, such as the aforementioned layer 34, as a radiation absorbing layer in a multijunction solar cell.

Example

A homojunction prototype solar cell was fabricated by generating a highly doped disordered layer as a top surface layer of a p-type silicon substrate (resistivity ρ = 800 Ohm-cm) by applying a plurality of 100-fs laser pulses having a central wavelength of 800-nm to a surface of the silicon substrate at a fluence of about 4 kJ/m^2 while exposing the surface to SF_6. Cr/Au electrical contacts were deposited, one on each opposed side of the substrate, to allow measuring a voltage generated across the cell in response to

exposure to solar radiation.

FIGURE 11 shows a current versus voltage (I-V) curve measured for the prototype homojunction cell. The open circuit voltage (V_{oc}) refers to a voltage developed across a solar cell, which is not connected to an external load, as a result of the electron-hole pairs generated in response solar radiation. The open circuit voltage can be measured, e.g., by determining a voltage needed to be applied to an illuminated solar cell to prevent flow of a current. The short circuit current (I_{sc}) refers to a current that flows through an external source having a vanishing resistance that is coupled across an illuminated cell. By way of example, the V_{oc} and I_{sc} can be determined by sweeping a voltage applied across

A power delivered by a solar cell to an external load connected across the cell having a given resistance can be determined by multiplying the current through the load by the voltage across the load. A variable used to characterize the quality of a solar cell is known as the fill factor (FF), which can be defined as follows:

$$FF = \frac{I_{\max} V_{\max}}{I_{SC} V_{OC}} \qquad \text{Eq. (2)}$$

where I_{max} and V_{max} correspond to current and voltage associated with a maximum power delivered by the cell, and V_{oc} and I_{sc} represent the open circuit voltage and short circuit current, respectively.

The efficiency of a solar cell, η(%), for converting solar power into electrical energy can be defined as:

$$\eta = \frac{I_{\max} V_{\max}}{T_1 A} \times 100\% \quad \text{Eq. (3)}$$

where T_1 represents the intensity of the light incident on the a surface of the cell exposed to the solar radiation, A represents the area exposed to the solar radiation, and I_{max} and V_{max} correspond to current and voltage associated with a maximum power delivered by the cell.

The efficiency of the aforementioned prototype cell under irradiation of an $AM_{1.5}$ solar spectrum was measured to be about 2.2% with an open circuit voltage of about 0.42 V, a short circuit current of 14.4 mA/cm^2, and a fill factor of about 0.36.

Those having ordinary skill in the art will appreciate that various changes can be made to the above embodiments without departing from the scope of the invention.

Claims:

1. A photovoltaic device, comprising

a first layer ,

a second layer forming a junction characterized by a depletion region with said first layer, and

a third layer forming a junction characterized by a depletion region with said intermediate layer,

each of said layers being adapted to absorb radiation over a different wavelength range of the solar spectrum so as to generate electron-hole pairs,

wherein at least one of said layers is capable of absorbing radiation at wavelengths greater than about 1 micron with an absorptance greater than about 60%.

2. The photovoltaic device of claim 1, wherein said wavelength ranges corresponding to absorption by the layers collectively span a wavelength range extending from 250 nm to about 2500 nm.

3. The photovoltaic device of claim 1, wherein said at least one layer exhibits an absorptance greater than about 70% for wavelengths greater than about 1 micron.

4. The photovoltaic device of claim 1, wherein said at least one layer exhibits an absorptance greater than about 80% for wavelengths greater than about 1 micron.

5. The photovoltaic device of claim 1, wherein said at least one layer exhibits an absorptance greater than about 90% for wavelengths greater than about 1 micron.

6. The photovoltaic device of claim 1, wherein one of said layers comprises amorphous silicon.

7. The photovoltaic device of claim 1, wherein one of said layers comprises any of crystalline or polycrystalline silicon.

8. The photovoltaic device of claim 1, wherein one of said layers comprises a silicon layer doped with a dopant at an atomic concentration greater than about 1%.

9. A photovoltaic device, comprising

a first radiation absorbing layer formed of silicon doped with a dopant so as to absorb electromagnetic radiation at one or more wavelengths greater than about 1 micrometers with an absorptance greater than about 70%,

a second radiation absorbing layer formed of any of doped crystalline or polycrystalline silicon disposed over said first layer, said second layer forming a junction with said first layer characterized by a depletion region, and

a third radiation absorbing layer formed of doped amorphous silicon disposed on said second layer so as to form a junction therewith characterized by a depletion region.

10. The photovoltaic device of claim 9, wherein said first layer comprises a layer containing said dopant with an atomic concentration greater than about 1%.

11. The photovoltaic device of claim 10, wherein said first layer has a thickness in a range of about 10 nm to about 1000 nm.

12 The photovoltaic device of claim 9, wherein at least a portion of one of said layers is configured for exposure to an external source of radiation.

13. The photovoltaic device of claim 9, further comprising a pair of electrodes each of which is in electrical coupling with one of said regions so as to facilitate generation of an electrical signal in response to exposure of said at least a portion of one of said regions to radiation from said source.

14. The photovoltaic device of claim 13, wherein said electrical signal comprises any of a voltage or a current.

15. The photovoltaic device of claim 9, wherein said first layers includes an n-type dopant.

16. The photovoltaic device of claim 9, wherein said first layer exhibits an electron mobility greater than about 100 $cm^2/V \cdot s$.

17. A photovoltaic device, comprising

a first semiconductor layer capable of absorbing radiation at wavelengths greater than about 1.1 microns, said layer exhibiting an absorptance greater than about 25% for at least one of said wavelengths,

a second semiconductor layer capable of absorbing radiation at wavelengths in a range of about 0.7 microns to about 1.1 microns, said second layer forming a junction with said first layer,

a third semiconductor layer capable of absorbing radiation at wavelengths in a range of about 0.25 microns to about 0.7 microns, said third layer forming a junction with said second layer,

wherein said of said junctions comprises a depletion region.

18. The photovoltaic device of claim 17, wherein said first layer exhibits an absorptance in a range of about 0.25 to about 1.0 at radiation wavelengths in a range of about 1 micron to about 2 microns.

19. The photovoltaic device of claim 17, wherein said second layer exhibits an absorptance in a range of about 0.5 to about 1.0 at radiation wavelengths in said range of about 0.7 microns to about 1 micron.

20. The photovoltaic device of claim 17, wherein said third layer exhibits an absorptance in a range of about 0.5 to about 1 at radiation wavelengths in said range of about 0.25 microns to about 0.7 microns.

21. The photovoltaic device of claim 17, wherein each of said layers is formed primarily of silicon.

22. A photovoltaic device, comprising

an upper layer capable of generating electron-hole pairs in response to exposure to radiation having one or more wavelengths within a first wavelength range,

an intermediate layer forming a junction characterized by a depletion region with said upper layer, said intermediate layer being capable of generating electron-hole pairs in response to radiation having one or more wavelengths within a second wavelength range,

a lower layer forming a junction characterized by a depletion region with said intermediate layer, said lower layer being capable of generating electron-hole pairs in response to radiation having one or more wavelengths within a this wavelength range,

said wavelength ranges spanning different portions of the solar wavelength spectrum,

wherein at least a portion of one of said layers is configured for exposure to solar radiation, and wherein said layers are adapted to collectively absorb at least about 70% of solar radiation energy incident on said portion configured for exposure to solar radiation

23. The photovoltaic device of claim 22, wherein said layers are adapted to collectively absorb at least about 80% of solar radiation energy incident on said portion configured for exposure to solar radiation.

24. The photovoltaic device of claim 22, wherein said layers are adapted to collectively absorb at least about 90% of solar radiation energy incident on said portion configured for exposure to solar radiation.

25. A method of fabricating a photovoltaic device, comprising

forming a radiation transparent electrically conductive layer over a surface of a radiation transparent substrate,

disposing a first semiconductor radiation absorbing layer over said electrically conductive layer,

disposing a second semiconductor radiation absorbing layer over said first layer so as to form a junction with said first layer characterized by a depletion region,

applying a plurality of short radiation pulses to an uncovered surface of said second layer while said surface portion is exposed to a compound having an electron donating constituent in order to convert a portion of said second layer into a third radiation absorbing layer forming a junction characterized by a depletion region with said second layer, and

depositing an electrically conductive layer over said third layer.

FIG. 1

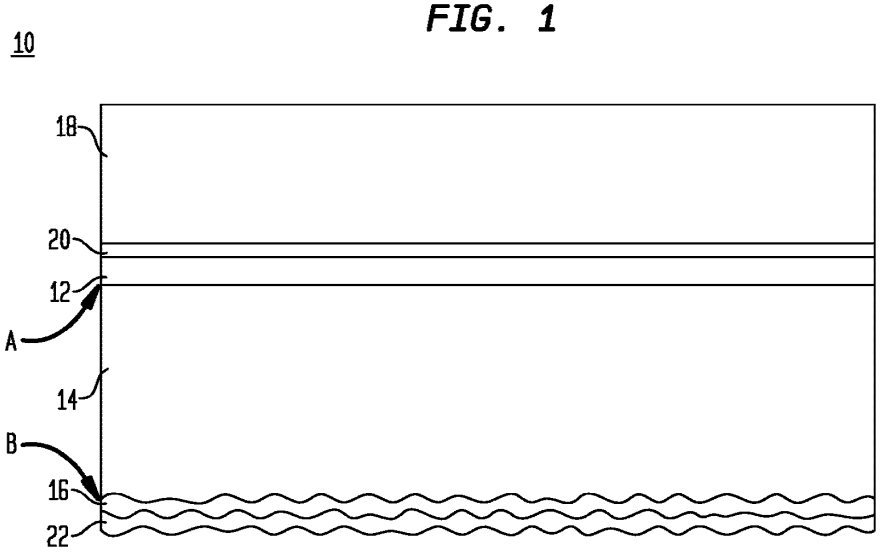
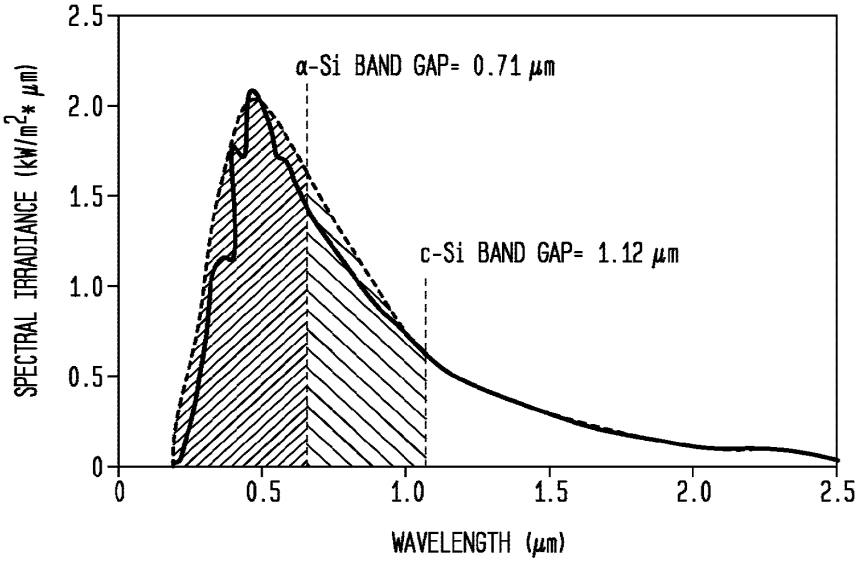


FIG. 2



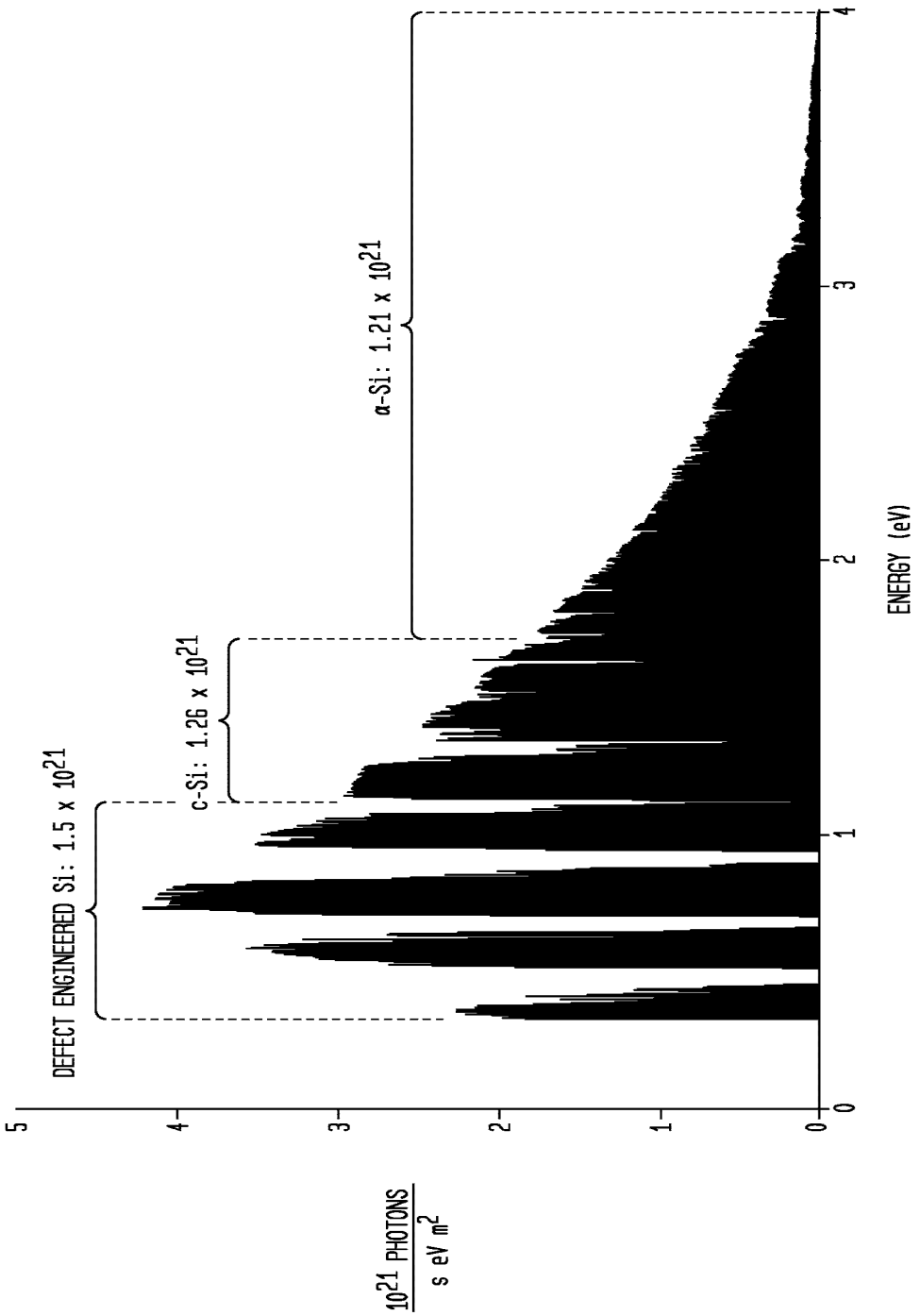
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FIG. 3A

FIG. 3B

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FIG. 4



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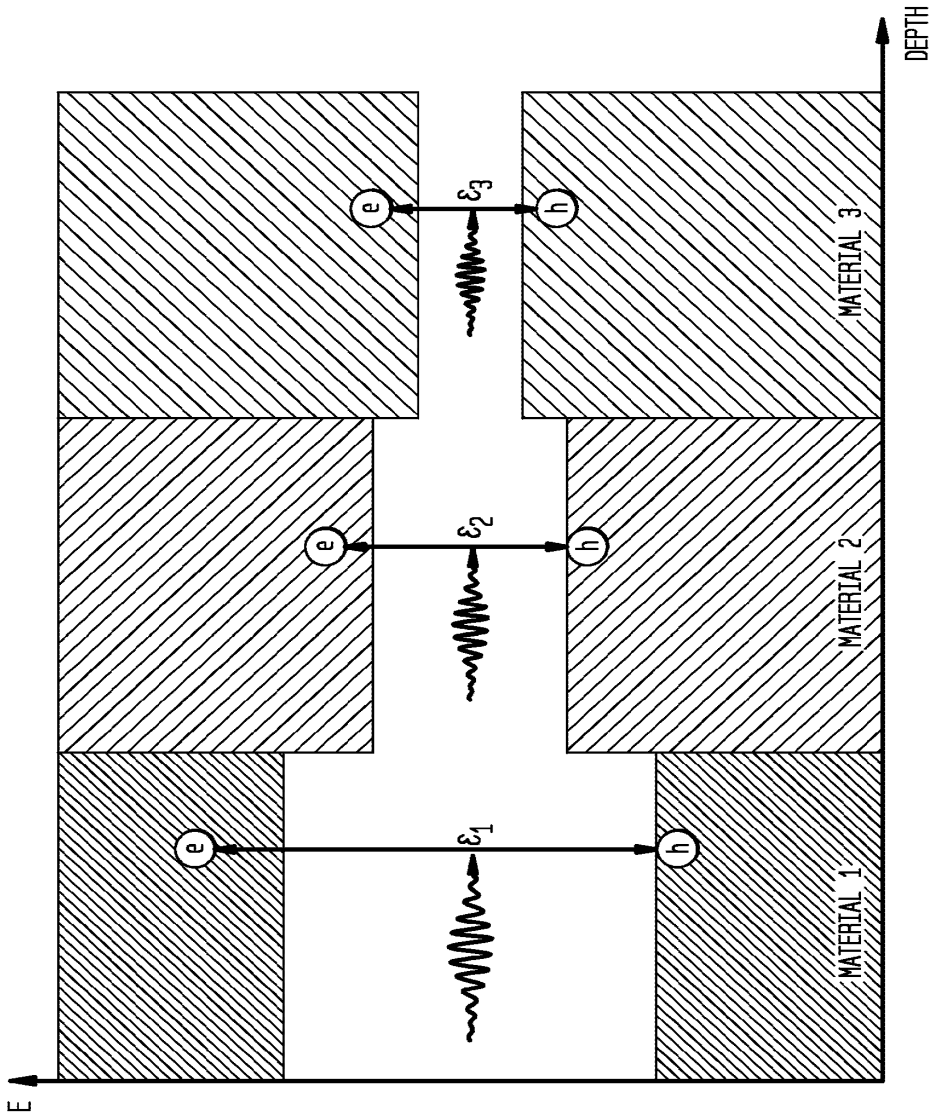


FIG. 5

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FIG. 6A

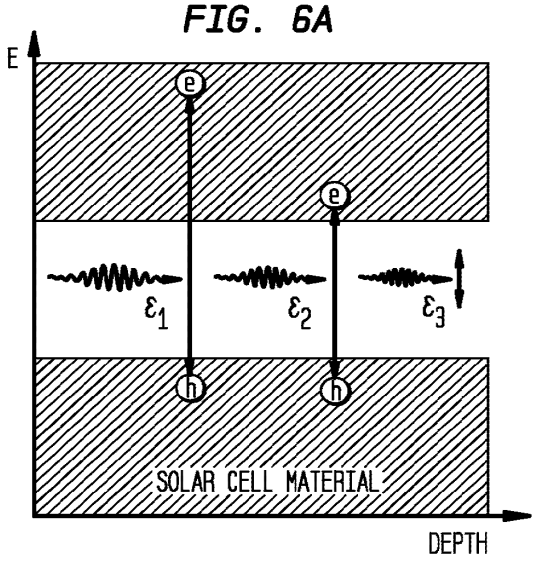


FIG. 6B

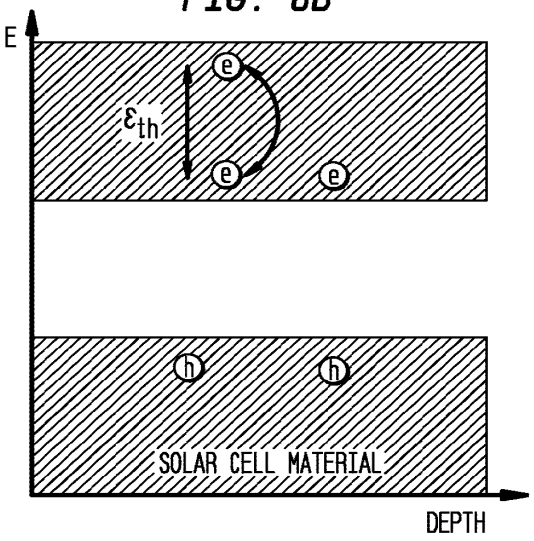
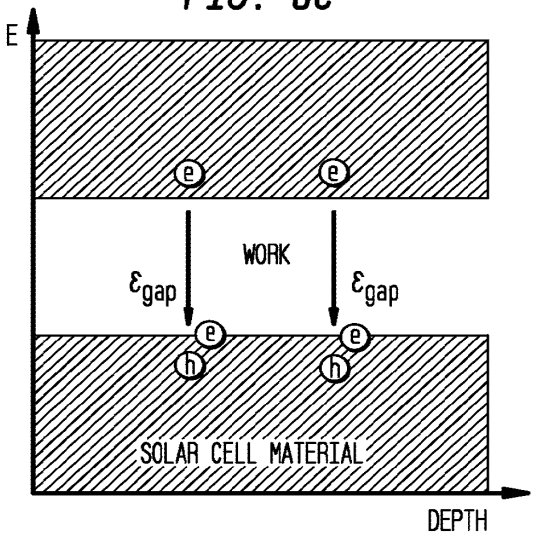
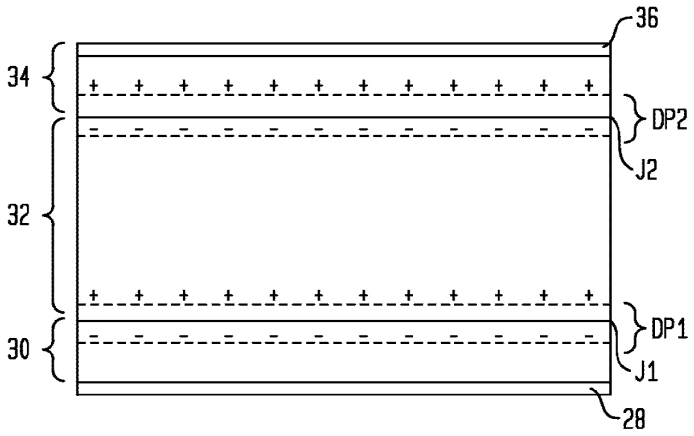


FIG. 6C



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FIG. 7



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FIG. 8A

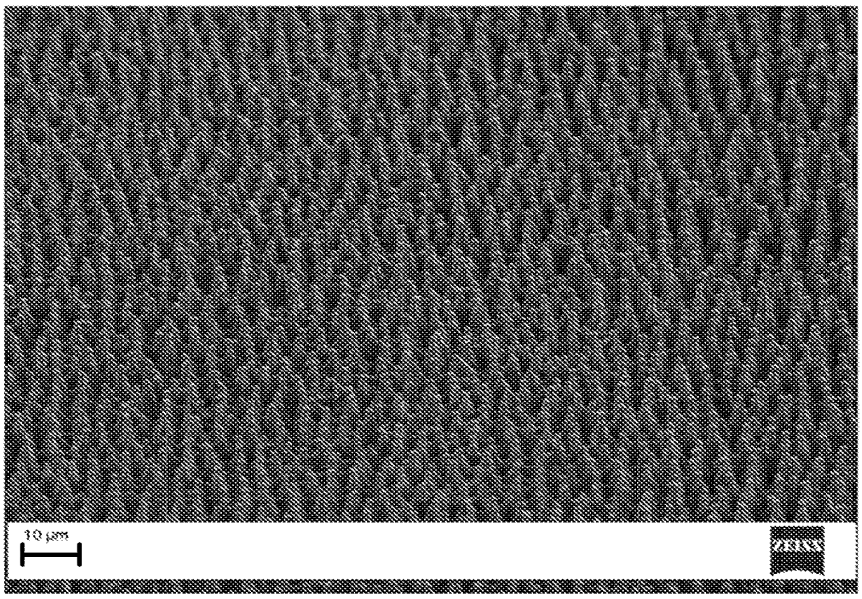
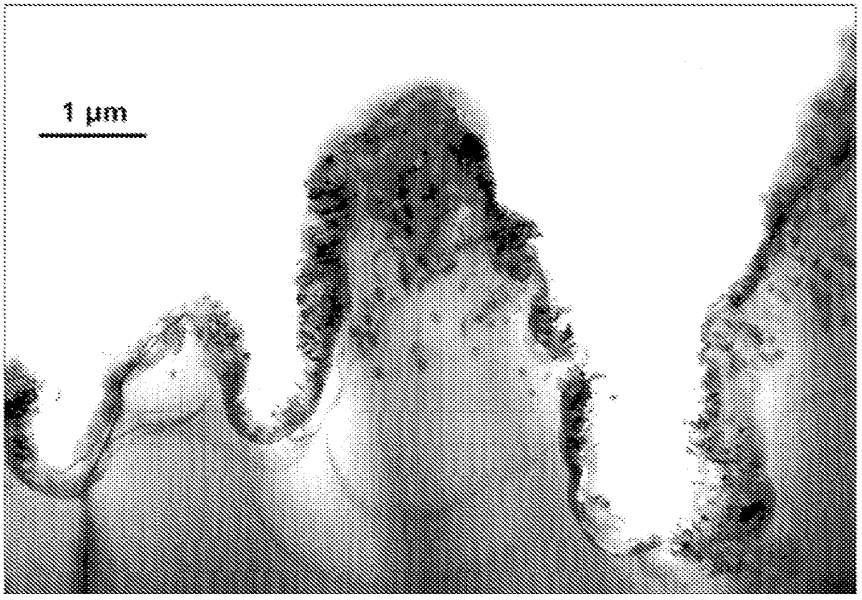


FIG. 8B



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FIG. 9

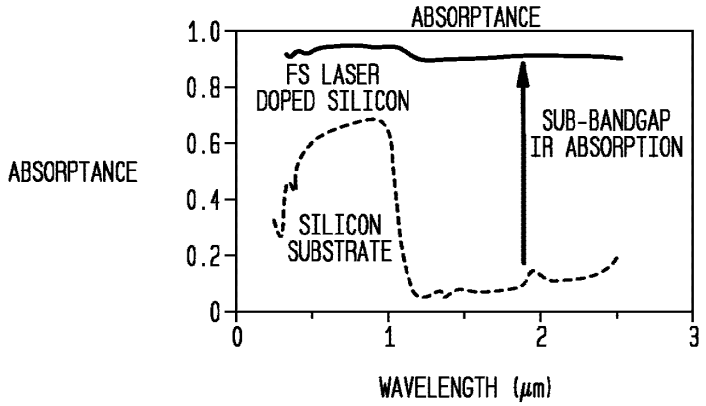


FIG. 10

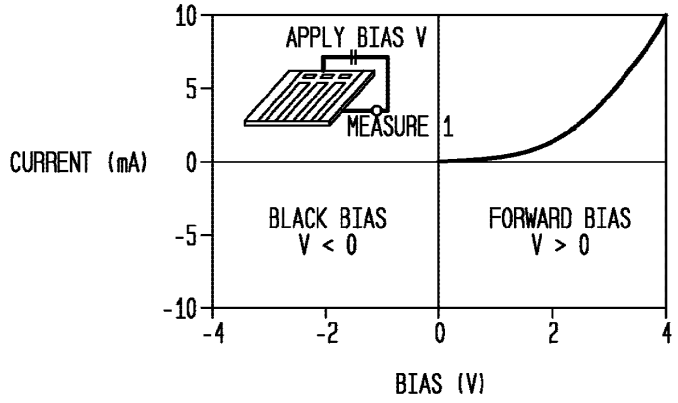
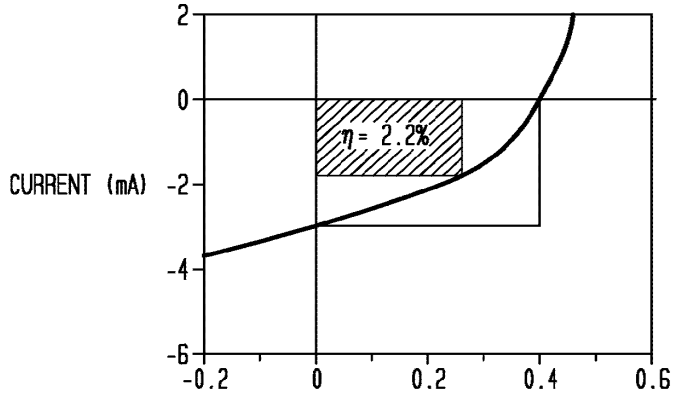


FIG. 11



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(54) **Title**: PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

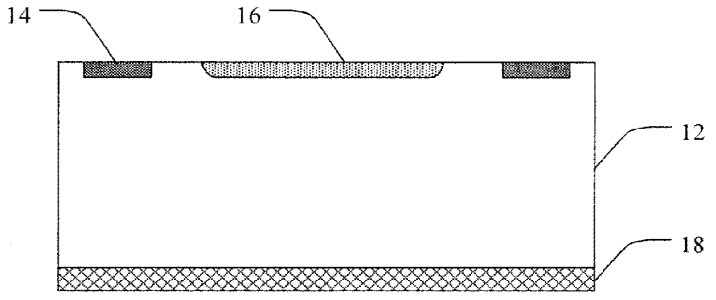


FIG. 1

(57) **Abstract**: Photosensitive devices and associated methods are provided. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption wavelength as compared to a semiconductor substrate lacking a textured region.

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PHOTOSENSITIVE IMAGING DEVICES AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/243,434, filed on September 17, 2009, U.S. Provisional Patent Application Serial No. 61/311,004 filed on March 5, 2010, and U.S. Provisional Patent Application Serial No. 61/311,107, filed on March 5, 2010, each of which is incorporated herein by reference.

BACKGROUND

The interaction of light with semiconductor materials has been a significant innovation. Silicon imaging devices are used in various technologies, such as digital cameras, optical mice, video cameras, cell phones, and the like. Charge-coupled devices (CCDs) were widely used in digital imaging, and were later improved upon by complementary metal-oxide-semiconductor (CMOS) imagers having increased performance. CMOS sensors are typically manufactured from silicon and can covert visible incident light into a photocurrent and ultimately into a digital image. Silicon-based technologies for detecting infrared incident electromagnetic radiation have been problematic, however, because silicon is an indirect bandgap semiconductor having a bandgap of about 1.1eV. Thus the absorption of electromagnetic radiation having wavelengths of greater than about 1100 nm is, therefore, very low in silicon.

SUMMARY

The present disclosure provides photosensitive devices and associated methods. In one aspect, for example, a photosensitive imager device can include a semiconductor substrate having multiple doped regions forming at least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. In one aspect, the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation. In another aspect, interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region. In one specific aspect, the transfer

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element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

The textured region can be positioned in a variety of locations relative to the doped regions. In one aspect, for example, the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In one specific aspect, the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate. The surface morphology of the textured region relative to the semiconductor substrate can include a variety of configurations, including, without limitation, sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

In another aspect, the textured region can be positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions. In a more specific aspect, an additional textured region can be positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions. In this manner, textured regions can thus be positioned adjacent to multiple doped regions and opposite the multiple doped regions.

Various aspects of the textured region can vary depending on the desired configuration of the device. In one aspect, however, the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof. Numerous surface feature morphologies are contemplated, nonlimiting examples of which include cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof. Additionally, the textured region can be formed by a variety of processes. Nonlimiting examples of such texturing processes can include lazing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, and combinations thereof.

Additional layers and/or structures can be included in various devices according to aspects present disclosure. In one aspect, for example, a reflective layer can be coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate. In another aspect, a lens can be optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

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In another aspect of the present disclosure, a method of making a photosensitive imager device is provided. Such a method can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation and coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction.

In one aspect, the photosensitive imager device can be tuned to be selected to filter out specific electromagnetic radiation wavelengths. In one specific aspect, tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation. In another aspect, tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type and/or thickness of the textured region, dopant type of the textured region, doping profile of the texture region, dopant profile of the semiconductor substrate, material type and/or thickness of the semiconductor substrate, and combinations thereof.

In another aspect of the present disclosure, a photosensitive imager device is provided. Such a device can include a semiconductor substrate having multiple doped regions forming a least one junction, a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic view of a photosensitive device in accordance with one aspect of the present disclosure;

FIG. 2 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 3 is a schematic view of a photosensitive device in accordance with yet another aspect of the present disclosure;

FIG. 4 is a schematic view of a photosensitive device in accordance with a further aspect of the present disclosure;

FIG. 5 is a schematic view of a photosensitive device in accordance with yet a further aspect of the present disclosure;

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FIG. 6 is a schematic view of a photosensitive device in accordance with another aspect of the present disclosure;

FIG. 7 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 8 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 9 is a schematic view of a photosensitive pixel device in accordance with yet a further aspect of the present disclosure;

FIG. 10 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 11 is a schematic view of a photosensitive pixel device in accordance with yet another aspect of the present disclosure;

FIG. 12 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 13 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure;

FIG. 14 is a schematic view of a photosensitive imager device in accordance with yet another aspect of the present disclosure;

FIG. 15 is a schematic view of a photosensitive pixel device in accordance with a further aspect of the present disclosure;

FIG. 16 is a schematic view of a photosensitive pixel device in accordance with another aspect of the present disclosure; and

FIG. 17 is a depiction of a method of making a photosensitive imager device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

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Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the term "low oxygen content" refers to any material having an interstitial oxygen content that is less than or equal to about 60 ppm atomic.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations formed by the irradiation of laser pulses. While the characteristics of such a surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers) and nanopores. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the terms "surface modifying" and "surface modification" refer to the altering of a surface of a semiconductor material using laser radiation. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping of a semiconductor material.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

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As used herein, the term "detection" refers to the sensing, absorption, and/or collection of electromagnetic radiation.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include

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not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

Electromagnetic radiation can be present across a broad wavelength range, including visible range wavelengths (approximately 350nm to 800nm) and non-visible wavelengths (longer than about 800nm or shorter than 350 nm). The infrared spectrum is often described as including a near infrared portion of the spectrum including wavelengths of approximately 800 to 1300 nm, a short wave infrared portion of the spectrum including wavelengths of approximately 1300 nm to 3 micrometers, and a mid to long wave infrared (or thermal infrared) portion of the spectrum including wavelengths greater than about 3 micrometers up to about 30 micrometers. These are generally and collectively referred to herein as "infrared" portions of the electromagnetic spectrum unless otherwise noted.

Traditional silicon photodetecting imagers have limited light absorption/detection properties. For example, infrared light is mostly transparent to such silicon based detectors. While other materials (e.g. InGaAs) can be used to detect infrared electromagnetic radiation having wavelengths greater than about 1000 nm, silicon is still commonly used because it is relatively cheap to manufacture and can be used to detect wavelengths in the visible spectrum (i.e. visible light, 350 nm – 800 nm). Traditional silicon materials require substantial absorption depths to detect photons having wavelengths longer than approximately 700 nm. While visible light can be absorbed at relatively shallow depths in silicon, absorption of longer wavelengths (e.g. 900 nm) in silicon of a standard wafer depth (e.g. approximately 750 μm) is poor if at all. The devices of the present disclosure increase the absorption of semiconductor materials by decreasing the effective absorption length to longer wavelengths as compared to traditional materials. For example, the absorption depth of silicon can be reduced such that these longer wavelengths can be absorbed at depths of less than or equal to about 850 μm. In other words, by decreasing the

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effective absorption length these devices are able to absorb longer wavelengths (e.g. >1000 nm for silicon) within a thin semiconductor material. In addition to increasing the effective absorption length, the response rate or response speed can also be increased using thinner semiconductor materials.

The present disclosure additionally provides broadband photosensitive diodes, pixels, and imagers capable of detecting visible as well as infrared electromagnetic radiation, including associated methods of making such devices. A photosensitive diode can include a semiconductor substrate having multiple doped regions forming at least one junction, and at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. In one aspect the multiple doped regions can include at least one cathode region and at least one anode region. In some aspects, doped regions can include an n-type dopant and/or a p-type dopant as is discussed below, thereby creating a p-n junction. In other aspects, a photosensitive device can include an i-type region to form a p-i-n junction.

A photosensitive pixel can include a semiconductor substrate having multiple doped regions forming at least one junction, at least one textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation, and an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction. A photosensitive imager can include multiple photosensitive pixels. Additionally, an electrical transfer element can include a variety of devices, including without limitation, transistors, sensing nodes, transfer gates, transfer electrodes, and the like.

Photosensitive or photodetecting imagers include photodiodes or pixels that are capable of absorbing electromagnetic radiation within a given wavelength range. Such imagers can be passive pixel sensors (PPS), active pixel sensors (APS), digital pixel sensor imagers (DPS), or the like, with one difference being the image sensor read out architecture. For example, a semiconducting photosensitive imager can be a three or four transistor active pixel sensor (3T APS or 4T APS). Various additional components are also contemplated, and would necessarily vary depending on the particular configuration and intended results. As and example, a 4T configuration can additionally include, among other things, a transfer gate, a reset, a source follower, and row select transistors. Additionally, devices having greater than 4 transistors are also within the present scope.

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Photosensitive imagers can be front side illumination (FSI) or back side illumination (BSI) devices, and there are advantages and disadvantages to both architecture types. In a typical FSI imager, incident light enters the semiconductor device by first passing by transistors and metal circuitry. The light, however, can scatter off of the transistors and circuitry prior to entering the light sensing portion of the imager, thus causing optical loss and noise. A lens can be disposed on the topside of a FSI pixel to direct and focus the incident light to the light sensing active region of the device, thus partially avoiding the circuitry. In one aspect the lens can be a ulens. BSI imagers, one the other hand, are configured to have the depletion region of the junction extending to the opposite side of the device. In one aspect, for example, incident light enters the device via the light sensing portion and is mostly absorbed prior to reaching the circuitry. BSI designs allow for smaller pixel architecture and a high fill factor for the imager. As mentioned, the present disclosure can be adapted for either configuration. It should also be understood that devices according to aspects of the present disclosure can be incorporated into complimentary metal-oxide-semiconductor (CMOS) imager architectures or charge-coupled device (CCD) imager architectures.

In one aspect, as is shown in FIG. 1, a photosensitive diode 10 can include a semiconductor substrate 12 having multiple doped regions 14, 16 forming at least one junction, and at least one textured region 18 coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation. The different doped regions can have the same doping profile or different doping profiles, depending on the device. Such an architecture is a FSI design where light enters the semiconductor substrate from the direction of the multiple doped regions. While the device shown in FIG. 1 contains three doped regions, it should be noted that aspects containing one or more doped regions are considered to be within the present scope. Additionally, the semiconductor substrate can be doped, and thus can be considered to be a doped region in some aspects. It should also be noted that the photosensitive diode can be configured with a BSI architecture, and thus electromagnetic radiation would enter the semiconductor substrate from the direction of the textured region.

The various devices according to aspects of the present disclosure can exhibit increased quantum efficiency over traditional photosensitive devices. Any increase in the quantum efficiency makes a large difference in the signal to noise ratio. More complex structures can provide not only increased quantum efficiency but also good

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uniformity from pixel to pixel. In addition, devices of the present disclosure exhibit increased responsivity as compared to traditional photosensitive devices. For example, in one aspect the responsivity can be greater than or equal to 0.8A/W for wavelengths greater than 1000 nm for semiconductor substrate that is less than 100 μm thick.

Photosensitive imagers can be maintained under constant conditions (fixed voltage or current) to provide enhanced linearity and uniformity. Connections between the imager and the underlying device layers can be achieved using vias fabricated from a refractory metal, such as tungsten or tantalum. Placing storage elements under the imager may provide various photonic benefits. For example, the entire pixel array may be dedicated to signal processing. This may enable higher performance by permitting access to low level pixel signals. Furthermore, massively parallel operations can be performed by pixel processors. For example, analog to digital conversion, noise reduction (ie., true correlated double sampling), power conditioning, nearest neighbor pixel processing, compression, fusion, and color multiplexing operations can be performed.

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc

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telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows electromagnetic radiation detection and conversion functionality, and thus any such thickness of semiconductor material is considered to be within the present scope. In some aspects the laser processed region of the semiconductor increases the efficiency of the device such that the semiconductor material can be thinner than has previously been possible. Decreasing the thickness of the semiconductor reduces the amount of semiconductor material required to make such a device. In one aspect, for example, the semiconductor material has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

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Additionally, various types of semiconductor material are contemplated, and any such material that can be incorporated into an electromagnetic radiation detection device is considered to be within the present scope. In one aspect, for example, the semiconductor material is monocrystalline. In another aspect, the semiconductor material is multicrystalline. In yet another aspect, the semiconductor material is microcrystalline. It is also contemplated that the semiconductor material can be amorphous. Specific nonlimiting examples include amorphous silicon or amorphous selenium.

The semiconductor materials of the present disclosure can also be made using a variety of manufacturing processes. In some cases the manufacturing procedures can affect the efficiency of the device, and may be taken into account in achieving a desired result. Exemplary manufacturing processes can include Czochralski (Cz) processes, magnetic Czochralski (mCz) processes, Float Zone (FZ) processes, epitaxial growth or deposition processes, and the like. Whether or not low oxygen content is desired in the device can also affect the choice of a manufacturing process for the semiconductor material. Various processes produce semiconductor materials containing varying amounts of oxygen, and as such, some applications having more stringent tolerances with respect to oxygen levels may benefit more from specific manufacturing procedures as compared to others. For example, during CZ crystal growth oxygen from the containment vessel, usually a quartz crucible, can become incorporated into the crystal as it is pulled. Additionally, other sources of oxygen contamination are also possible with the CZ process. Such contamination may be reduced, however, through the use of non oxygen-containing crucible materials, as well as the development of other crystal growth methods that do not utilize a crucible. One such process is the FZ process.

Materials grown with the CZ method can also be made to have lowered oxygen concentration through enhancements to the crystal growth process, such as growing the crystal in the presence of a magnetic field (i.e. the mCz process). Also, gettering techniques can be employed to reduce the impact of oxygen or other impurities on the finished device. These gettering techniques can include thermal cycles to liberate or nucleate impurities, or selective ion implantation of species to serve as gettering sites for the impurities. For example, oxygen concentrated in the semiconductor can be removed by the performing a furnace cycle to form a denuded zone. During heating with an inert gas, oxygen near the surface of the semiconductor

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diffuses out of the material. During the furnace cycle but after the denuding step, nucleating and growing steps may be performed. Nucleating sites for precipitates are formed during the nucleating step, and the precipitates are grown from the nucleating sites during a growing step. The precipitates are formed from interstitial oxygen within the bulk of the semiconductor material and beneath the denuded zone. The precipitation of oxygen in the bulk of the semiconductor material can be desired because such precipitates can act as gettering sites. Such precipitate formation can also be performed to "lock up" interstitial oxygen into the precipitates and reduce the likelihood that such oxygen can migrates from the bulk of the semiconductor material into the denuded zone.

In those aspects where low oxygen content of the device is desired, further processing of the semiconductor material can be performed so as to minimize the introduction of oxygen. Oxygen can exist in different states or at different sites (for example, interstitially or substitutionally) within a semiconductor such as silicon, dependent upon the thermal processing the semiconductor has received. If the semiconductor is subjected to temperatures higher than, for example, about 1000° C, oxygen can form aggregates or clusters that serve as defect sites in the crystal lattice. These sites may result in trap states and a reduction in carrier lifetime within the semiconductor material and device can occur. At lower temperatures (for example, around 400° C to 700° C), oxygen can behave as electrically active thermal donors. Thus, oxygen can have a negative impact on carrier lifetime and on carrier mobility. In a device fabricated to have photoconductive gain, the presence of oxygen causing reduced carrier lifetime may result in reduced levels of photoconductive gain.

It may be beneficial, therefore, to produce semiconductor devices such that a low oxygen content is obtained or maintained. This can be accomplished in a variety of ways, including using semiconductor materials having low levels of oxygen contained therein to begin with, processing these materials in a manner that minimizes the uptake of oxygen into the semiconductor lattice, and utilizing techniques that eliminate or reduce oxygen that may be present in the semiconductor. Such processes and techniques can include, for example, annealing the semiconductor material and any laser treated region to lower temperatures as compared to previous annealing procedures. Annealing processes are discussed more fully below.

Additionally, texture processing of the semiconductor material and/or any annealing process can be performed in a substantially oxygen-depleted environment

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in order to minimize the introduction of oxygen into the semiconductor. An oxygen-depleted or substantially oxygen-depleted environment can include a variety of environments. In one aspect, for example, the oxygen-depleted environment can be an environment whereby oxygen from the air or other sources has been replaced with a gas or other fluid containing little to no oxygen. In another aspect, processing can occur in a vacuum environment, and thus contain little to no oxygen. Additionally, oxygen-containing materials or materials that introduce oxygen into the semiconductor, such as, for example, quartz crucibles, can be avoided. As a practical matter, the term "oxygen-depleted environment" can be used to describe an environment with low levels of oxygen, provided a semiconductor material can be processed therein within the desired tolerances. Thus, environments having low oxygen, or little to no oxygen, are environments in which a semiconductor can be processed as a low-oxygen content semiconductor while maintaining oxygen levels within the tolerances of the present disclosure. In one aspect, an oxygen-depleted environment can be an oxygen-free environment. Further details regarding low-oxygen content semiconductor materials can be found in US Patent Application No. 12/771848, filed on April 30, 2010, which is incorporated herein by reference.

The semiconductor material can have varying levels of interstitial oxygen depending on the desired efficiency of the device. In some aspects, oxygen content may be of no concern, and thus any level of oxygen within the lattice is acceptable. In other aspects, a low oxygen content is desired. In one aspect a semiconductor material can have an oxygen content that is less than or equal to about 50 ppm atomic. In another aspect, a semiconductor material can have an oxygen content that is less than or equal to about 30 ppm atomic. In yet another aspect, the semiconductor material can have an oxygen content less than or equal to about 10 ppm atomic. In another aspect the semiconductor can have an oxygen content less than about 5 ppm atomic. In yet another aspect the semiconductor can have an oxygen content less than about 1 ppm atomic.

As has been described, the textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to increase the effective absorption length of the photosensitive pixel. The surface features can be cones, pyramids, pillars, protrusions, microlenses, quantum dots, inverted features and the like. Factors such

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as manipulating the feature sizes, dimensions, material type, dopant profiles, texture location, etc. can allow the diffusing region to be tunable for a specific wavelength. In one aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be absorbed. In another aspect, tuning the device can allow specific wavelengths or ranges of wavelengths to be reduced or eliminated via filtering.

Tuning can also be accomplished through the location of the texture region within the device, modifying the dopant profile(s) of regions within the device, dopant selection, and the like. Additionally, material composition near the textured region can create a wavelength specific photosensing pixel device. It should be noted that a wavelength specific photosensing pixel can differ from one pixel to the next, and can be incorporated into an imaging array. For example a 4 x 4 array can include a blue pixel, a green pixel, a red pixel, and infrared light absorbing pixel, or a blue pixel, two green pixels, and a red pixel.

Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor substrate. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The textured region can be formed by various techniques, including lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, additional material deposition, and the like. For example, pillar features can be incorporated into pixels by thinning or removing material from the backside of a FSI semiconductor substrate by using deep trench isolation and etching techniques. In one aspect material can be removed to a thickness of about 20 μm. Anisotropic etching can be used to produce a sloping backside pyramid structure, spherical, structure parabolic structure , a lens structure with reflectors, and the like. Such features on the backside of pillars will also serve to diffuse and reflect electromagnetic radiation.

In one aspect, the texturing process can be performed during the manufacture of the photosensitive device. In another aspect, the texturing process can be performed on a photosensitive device that has previously been made. For example, a CMOS, CCD, or other photosensitive element can be textured following manufacture. In this case, material layers may be removed from the photosensitive element to

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expose the semiconductor substrate or bulk material upon which a textured region may be formed.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete locations of the semiconductor substrate to be textured. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection. The laser treated region can be associated with the surface nearest the impinging electromagnetic radiation, or the laser treated surface can be associated with a surface opposite in relation to impinging electromagnetic radiation, thereby allowing the radiation to pass through the semiconductor material before it hits the laser treated region.

In one aspect, for example, a target region of the semiconductor material can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a semiconductor material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can be directed through a dopant carrier and onto the semiconductor surface. In this way, dopant from the dopant carrier is introduced into the target region of the semiconductor material. Such a region incorporated into a semiconductor material can have various benefits in accordance with aspects of the present disclosure. For example, the target region typically has a textured surface that increases the surface area of the laser treated region and increases the probability of radiation absorption via the mechanisms described herein. In one aspect, such a target region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of semiconductor material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the semiconductor. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the semiconductor material is chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the

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formation of surface features appearing as microstructures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the semiconductor material. In some aspects, the features or microstructures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed by the semiconductor material.

The type of laser radiation used to surface modify a semiconductor material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a semiconductor material. A short-pulsed laser is one capable of producing femtosecond, picosecond and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a semiconductor target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated, and any such material that can be used in the laser treatment process to surface modify a semiconductor material according to aspects of the present disclosure is considered to be within the present

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scope. It should be noted that the particular dopant utilized can vary depending on the semiconductor material being laser treated, as well as the intended use of the resulting semiconductor material. For example, the selection of potential dopants may differ depending on whether or not tuning of the photosensitive device is desired.

A dopant can be either electron donating or hole donating. In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of between about 5×10^{14} and about 1×10^{16} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. SF_6 gas is a good carrier for the incorporation of sulfur into the semiconductor material via a laser process without significant adverse effects on the semiconductor material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

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The semiconductor substrate can be annealed for a variety of reasons, including dopant activation, semiconductor material damage repair, and the like. In those aspects including a laser textured region, the semiconductor material can be annealed prior to laser treatment, following laser treatment, during laser treatment, or both prior to and following laser treatment. Annealing can enhance the semiconductive properties of the device, including increasing the photoresponse properties of the semiconductor materials. Additionally, annealing can reduce damage done by the lasing process. Although any known anneal can be beneficial and would be considered to be within the present scope, annealing at lower temperatures can be particularly useful. Such a "low temperature" anneal can greatly enhance the photoconductive gain and external quantum efficiency of devices utilizing such materials. In one aspect, for example, the semiconductor material can be annealed to a temperature of from about 300° C to about 1100 C°. In another aspect, the semiconductor material can be annealed to a temperature of from about 500° C to about 900° C. In yet another aspect, the semiconductor material can be annealed to a temperature of from about 700° C to about 800° C. In a further aspect, the semiconductor material can be annealed to a temperature that is less than or equal to about 850° C.

The duration of the annealing procedure can vary according to the specific type of anneal being performed, as well as according to the materials being used. For example, rapid annealing processes can be used, and as such, the duration of the anneal may be shorter as compared to other techniques. Various rapid thermal anneal techniques are known, all of which should be considered to be within the present scope. In one aspect, the semiconductor material can be annealed by a rapid annealing process for a duration of greater than or equal to about 1 μs. In another aspect, the duration of the rapid annealing process can be from about 1 μs to about 1 ms. As another example, a baking or furnace anneal process can be used having durations that may be longer compared to a rapid anneal. In one aspect, for example, the semiconductor material can be annealed by a baking anneal process for a duration of greater than or equal to about 1 ms to several hours. As has been described, if low oxygen content semiconductor materials are used it may be beneficial to anneal such materials in a substantially oxygen-depleted environment.

As has been described, annealing can help reduce defects inherent to the semiconductor substrate and otherwise reduce electron/hole recombination. In other

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words, the annealing can help create electron states that effectively reduce the undesirable recombination processes. Annealing the semiconductor material may also improve the responsivity or photoconductive gain of the device. Photoconductive devices can have dopants, impurities, or defects that can introduce energy levels that can trap carriers. Trapping carriers and reducing recombination of photocarriers can lead to an increase in photoconductive gain of the device. The relationship of photoconductive gain and trapping time can be represented by Equation (I):

$$\text{Gain} = \tau_L/\tau_t \quad \text{(I)}$$

where "τ_L" is the lifetime of an excess carrier and "τ_t" is the transit time of the carriers across the device. It is understood that the lifetime of an excess carrier can be increased by trapping a carrier species and reducing the recombination rate. An increase in gain can be achieved by trapping centers in the semiconductor that have millisecond trapping times at room temperature and short transit times in thinned lightly doped wafers. These trapping locations can decrease the recombination of carriers and therefore improve or increase the photoconductive gain of the device by allowing more electrons to traverse the different regions without being recombined.

Turning to FIG. 2, a reflecting layer 20 can be coupled to the semiconductor substrate 12. The reflecting layer can be coupled to any side or portion of the semiconductor substrate in order to reflect electromagnetic radiation back into the device. Accordingly, in one aspect the reflecting layer can be located on the semiconductor substrate opposite the incoming electromagnetic radiation. Thus, as is shown in FIG. 2, electromagnetic radiation passing though the semiconductor substrate and the textured region 16 can be reflected back into the semiconductor substrate. Additionally, a passivation layer 22 can be coupled to the semiconductor substrate. The passivation layer is shown coupled to the side of the semiconductor substrate facing the incoming electromagnetic radiation, however a passivation layer can be located anywhere on the device and still be within the present scope.

As has been described, location of the textured region can be used to provide enhancement and/or filtering of the incoming electromagnetic radiation. For example, a textured region located at the point of entry of the electromagnetic radiation into the photosensitive device tends to bend the electromagnetic radiation, particularly the blue wavelengths. Accordingly, one level of tuning can be accomplished by locating

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the textured region on the surface adjacent the incident electromagnetic radiation to purposely effectuate the filtering of blue wavelengths. Additionally, absorption of particular wavelengths of electromagnetic radiation occurs at different depths in the semiconductor layer and/or textured region. By increasing the absorption to green wavelengths, for example, the electrical signal as a result of green wavelengths can be increased in a diode or pixel. Certain traditional 4 pixel imagers have one red, one blue, and two green pixels, with the greater number of green pixels to account for increased sensitivity of the human eye to green colors. Thus in one aspect, a 4 pixel imager can have one blue, one red, and one green pixel having an increased green wavelength absorption. The fourth pixel can be used for an IR or other wavelength selective pixel depending on the desired application of the imager.

FIG. 3 shows a photosensitive device having textured regions 30 located on the sides of the semiconductor substrate 12. Such a configuration allows electromagnetic radiation normally exiting through the sides of the device to be further defused and absorbed within semiconductor substrate. The textured region(s) can be located on one or more sides to facilitate the enhanced absorption.

FIG. 4 shows a photosensitive device having a textured region 40 having a nonparallel surface with respect to the semiconductor substrate 12. Thus the overall configuration of the textured region can be designed to further enhance absorption and/or selectively tune the device. As has been described, the nonparallel surface can have a variety of configurations, such as, without limitation, nonparallel slope, a pyramid, an inverted pyramid, a concave shape, a convex shape, and the like. In some cases the configuration of the textured region can function to direct or focus electromagnetic radiation into the semiconductor substrate, and in other cases the configuration of the textured region can function to direct or focus electromagnetic radiation away from the semiconductor substrate.

As is shown in FIG. 5, a lens 50 can be coupled to the semiconductor substrate 12 on a side facing incoming electromagnetic radiation. Thus the lens can focus the electromagnetic radiation into the semiconductor substrate. In those aspects having circuitry or other structures disposed on the incoming electromagnetic radiation surface, the lens can further focus light around such structures, thereby reducing optical scattering and noise.

As is shown in FIG. 6, a textured region 60 is located on the semiconductor substrate 12 adjacent to the multiple doped regions 14, 16. The textured region can be

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associated with at least one of the doped regions as is shown, or the textured region can be distinct from the doped regions (not shown). Electromagnetic radiation can enter the photosensitive device at the side adjacent the doped regions, or alternatively at the side opposite the doped regions.

FIGs. 7-11 show various steps in the manufacture of a photosensitive pixel according to aspects of the present disclosure. FIG. 7 shows a cross-section of a front side illumination (FSI) photosensitive pixel device. The photosensitive pixel device can include a semiconductor substrate 72, and can be referred to as bulk semiconductor material. The semiconductor substrate includes at least one doped region 74 that can be doped with an electron donating or hole donating species to cause the region to become more positive or negative in polarity as compared to the semiconductor substrate. In one aspect, for example, the doped region can be p doped. In another aspect the doped region can be n doped. A highly doped region 76 can be formed on or near the doped region to create a pinned diode. In one example, the semiconductor substrate can be negative in polarity, and the doped region and the highly doped region can be doped with p+ and n- dopants respectively. In some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type doping of the regions can be used. It should be noted that in one aspect the highly doped region can be the textured region. In other words, textured surface features can be formed on or in the highly doped region.

The device of FIG. 7 can further include various metal regions 78, at least one via 80, a passivation layer 82, trench isolation 84, and an electrical transfer element 86. Trench isolation elements can maintain pixel to pixel uniformity by reducing optical and electrical crosstalk. The trench isolation can be shallow (FIG. 7) or deep (FIG. 12) trench isolation. The trench isolation can include various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, and the like. These trench isolation regions can be configured to reflect incident light until it is absorbed, thereby increase the effective absorption length of the device.

As is shown in FIG. 8, a carrier substrate or carrier wafer 88 can be coupled to the photosensing pixel. In one aspect, the carrier substrate can be disposed on the passivation layer 82, although the carrier substrate can be disposed on any surface of the device. In one aspect, for example, the carrier substrate can be disposed on the semiconductor substrate (not shown). The carrier substrate can be coupled to the

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photosensing pixel by various techniques, and any such coupling mechanism is within the present scope. In one aspect, for example, the coupling can occur by way of a bonding layer or adhesive layer disposed on the device, for example, on the passivation layer. The support substrate can provide support to the semiconductor device both during and after manufacture, depending on whether or not the support is removed. The carrier substrate can be made of a semiconductor material that is the same or similar to the bulk semiconductor material, or it can be made of a different material.

As is shown in FIG. 9, a textured region 90 is coupled to the semiconductor substrate 72 opposite the doped regions 74,76. Thus light entering from the direction of the doped regions passes through the semiconductor substrate prior to contacting the textured region. The textured region can be disposed across an entire surface of the semiconductor substrate, as is shown in FIG. 9, or it can be disposed on one or more discrete regions (not shown).

As is shown in FIG. 10, an additional carrier support substrate 100 can be coupled to the device on an opposing side from the carrier support substrate 88. The additional carrier support substrate can be utilized for a variety of purposes, including providing additional support to the device, facilitating the removal of the first carrier support substrate, and the like. A reflective layer 102 can be disposed between the textured region 90 and the carrier support substrate. Thus the reflective layer can reflect electromagnetic radiation that passes through the textured region back toward the semiconductor substrate 72, thus reducing optical loss and backscattering. Thus, in some aspects a reflective layer can increase the quantum efficiency of the device. The reflective layer material can be any reflective material that can be incorporated into such a device. Nonlimiting examples can include materials such as silver, aluminum, and the like.

As is shown in FIG. 11, the carrier support substrate can be removed to expose the passivation layer 82 or any other material layer that was previously covered by the carrier support substrate. The additional carrier substrate 100 can be maintained in the device, removed from the device, or thinned to reduce the thickness of the substrate depending on the intended use of the device. The removal of material from the device, including the carrier support substrate and the additional carrier substrate, can be accomplished by a variety of methods including, without limitation, etching, chemical mechanical polishing, ion implanting (i.e. smart cut), and the like.

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Various types of trench isolation are contemplated, and any such isolation is considered to be within the present scope. As has been described, trench isolation can be shallow (FIG. 7, 84) or deep (FIG. 12, 120) trench isolation. The trench isolation can also include depths between shallow and deep, depending on the device design. Trench isolation can include dielectric materials, reflective materials, conductive materials, and combinations thereof, including textured regions and other light diffusing features. Thus the trench isolation layer can be configured to reflect incident electromagnetic radiation, in some cases until it is absorbed, thereby increasing the effective absorption length of the device. Additionally, in some aspects pillar features can be incorporated into pixels by thinning or removing material from the semiconductor substrate using deep trench isolation and etching techniques. As is shown in FIG. 13, the textured region 130 can have a nonparallel surface with respect to the semiconductor substrate 72 as has been described. This nonparallel morphology, when included with the deep trench isolation 120, can effectively focus electromagnetic radiation into the semiconductor substrate from multiple sides.

It is also contemplated, that a non-bulk material can be formed or disposed near a doped region in the device. The addition of the non-bulk material can allow for electromagnetic radiation diffusing features to be formed on or in the non-bulk material. A metal layer defining an aperture can also be included in one aspect of the present disclosure. The metal layer can be formed near the doped regions and can have a light entering region that defines an aperture. This light entering region can also include an antireflecting material.

Fig. 14 shows a photosensitive imager comprising two photosensitive pixels 140. Each photosensitive pixel includes a boundary region 142 that can include metal circuitry and a textured region 144. Each photosensitive pixel can include at least one transistor 146 or other electrical transfer element. Additional read out and circuitry elements 148 can be utilized and shared by both photosensitive pixels.

Turning to FIG. 15, a backside illuminated (BSI) photosensitive pixel according to one aspect present disclosure is provided. A lens 150 and an anti-reflective coating 152 are disposed on the backside of the pixel following thinning and trench isolation. A color filter 154 can be optically coupled to the lens to allow specific wavelengths filtering of the electromagnetic radiation. A textured region 156 can be coupled to the semiconductor substrate 72 opposite the lens in order to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes

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through to the front side of the pixel. Thus the electromagnetic radiation can be focused within the semiconductor substrate to the combined action of the textured region and the trench isolation 120

Fig. 16 shows a front side illuminated (FSI) imager according to another aspect of the present disclosure. A lens 160 and an antireflecting passivation layer on 62 are coupled to the front side of the pixel. A textured region 90 and a reflecting layer 102 are coupled to the semiconductor substrate 72 opposite the lens to provide diffusive scattering and reflection of the incident electromagnetic radiation that passes through the semiconductor substrate. An aperture 164 formed in a metal or other reflective material layer 166 can increase the effectiveness of the optical cavity. Thus the lens focuses electromagnetic radiation through the aperture.

In other aspects of the present disclosure, various methods of making photosensitive diodes, pixels, and imagers, are contemplated. In one aspect, as is shown in FIG. 17, a method of making a photosensitive imager device can include forming a textured region on a semiconductor substrate having multiple doped regions forming a least one junction, wherein the textured region is formed in a position to interact with electromagnetic radiation 170. The method also includes coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction 172. In one aspect, multiple pixels can be associated together to form an imager. A passivation layer can also be disposed on the photosensitive imager device to protect and/or reduce the dark current of the device.

In another aspect of the present disclosure, a method for making a photosensitive diode is provided. Such a method can include forming at least one cathode and at least one anode on a surface of a semiconductor substrate, coupling a textured region to the semiconductor substrate, and coupling a support substrate to the semiconductor substrate. The textured region can be located adjacent to the anode and cathode, opposite the anode and cathode, or both adjacent and opposite the anode and cathode. An electrical transfer on the can be electrically coupled to at least one of the anode and cathode to form a photosensitive pixel. In another aspect, the semiconductor substrate can be thinned to improve the response rate and/or speed of the device. A passivation layer can also be disposed on the photosensitive diode to protect and/or reduce the dark current of the device. An additional support substrate can be attached to the device to provide additional support. In one aspect, the

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additional support substrate can be located on the opposite side of the photosensitive diode from the support substrate. The support substrate can subsequently be removed to allow for further processing.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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CLAIMS

What is claimed is:

1. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

an electrical transfer element coupled to the semiconductor substrate and operable to transfer an electrical signal from the at least one junction.

2. The device of claim 1, wherein the textured region is operable to facilitate generation of an electrical signal from the detection of infrared electromagnetic radiation.

3. The device of claim 1, wherein interacting with electromagnetic radiation further includes increasing the semiconductor substrate's effective absorption length as compared to a semiconductor substrate lacking a textured region.

4. The device of claim 1, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

5. The device of claim 1, further comprising a reflective layer coupled to the semiconductor substrate and positioned to maintain the electromagnetic radiation in the semiconductor substrate.

6. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

7. The device of claim 6, wherein the textured region has a surface morphology operable to direct electromagnetic radiation into or out of the semiconductor substrate.

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8. The device of claim 7, wherein the surface morphology of the textured region relative to the semiconductor substrate is a member selected from the group consisting of sloping, pyramidal, inverted pyramidal, spherical, parabolic, asymmetric, symmetric, and combinations thereof.

9. The device of claim 1, wherein the textured region is positioned on a surface of the semiconductor substrate that is adjacent the multiple doped regions.

10. The device of claim 9, further comprising an additional textured region positioned on a surface of the semiconductor substrate that is opposite the multiple doped regions.

11. The device of claim 1, wherein the textured region is coupled directly to at least one of the multiple doped regions.

12. The device of claim 1, wherein the textured region includes surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

13. The device of claim 12, wherein surface features include a member selected from the group consisting of cones, pillars, pyramids, micolenses, quantum dots, inverted features, and combinations thereof.

14. The device of claim 1, wherein the textured region has been formed by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

15. The device of claim 1, further comprising a lens optically coupled to the semiconductor substrate and positioned to focus incident electromagnetic radiation into the semiconductor substrate.

16. A photosensitive imager array, comprising at least two photosensitive imager devices of claim 1.

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17. The array of claim 16, further comprising at least one trench isolation positioned between the at least two photosensitive imager device.

18. A method of making a photosensitive imager device, comprising:

forming a textured region on a semiconductor substrate, wherein the semiconductor substrate has multiple doped regions forming a least one junction, and wherein the textured region is formed in a position to interact with electromagnetic radiation; and

coupling an electrical transfer element to the semiconductor substrate such that the electrical transfer element is operable to transfer an electrical signal from the at least one junction .

19. The method of claim 18, wherein forming the textured region is by a process selected from the group consisting of lazing, chemical etching, nanoimprinting, material deposition, and combinations thereof.

20. The method of claim 18, wherein forming the textured region includes irradiating a target region with laser radiation to form surface features having a size selected from the group consisting of micron-sized, nano-sized, and combinations thereof.

21. The method of claim 20, wherein irradiating the target region includes exposing the laser radiation to a dopant such that the irradiation incorporates the dopant into the textured region.

22. The method of claim 20, wherein the irradiation is performed using a pulsed laser including a member selected from the group consisting of a femtosecond laser, a picosecond laser, a nanosecond laser, and combinations thereof.

23. The method of claim 18, further comprising tuning an electrical response of the photosensitive imager device.

24. The method of claim 23, wherein tuning includes forming surface features to have dimensions that selectively diffuse or selectively absorb a desired wavelength of electromagnetic radiation.

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25. The method of claim 23, wherein tuning is accomplished through a factor selected from the group consisting of placement of the textured region, material type of the textured region, thickness of the textured region, dopant type of the textured region, doping profile of the texture region, doping profile of the semiconductor substrate, thickness of the substrate, and combinations thereof.

26. The method of claim 18, wherein the transfer element is selected from the group consisting of a transistor, a sensing node, a transfer gate, and combinations thereof.

27. The method of claim 18, further comprising annealing the semiconductor substrate to a temperature of from about 300° C to about 1100° C.

28. A photosensitive imager device, comprising:

a semiconductor substrate having multiple doped regions forming a least one junction;

a textured region coupled to the semiconductor substrate and positioned to interact with electromagnetic radiation; and

at least 4 transistors coupled to the semiconductor substrate and with at least one of the transistors electrically coupled to the at least one junction.

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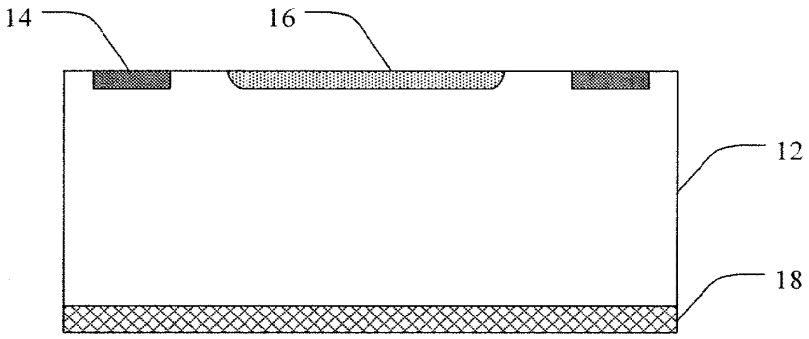


FIG. 1

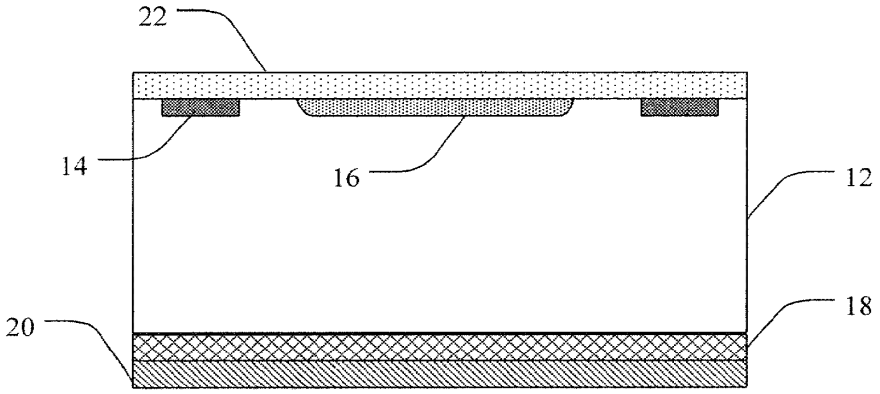


FIG. 2

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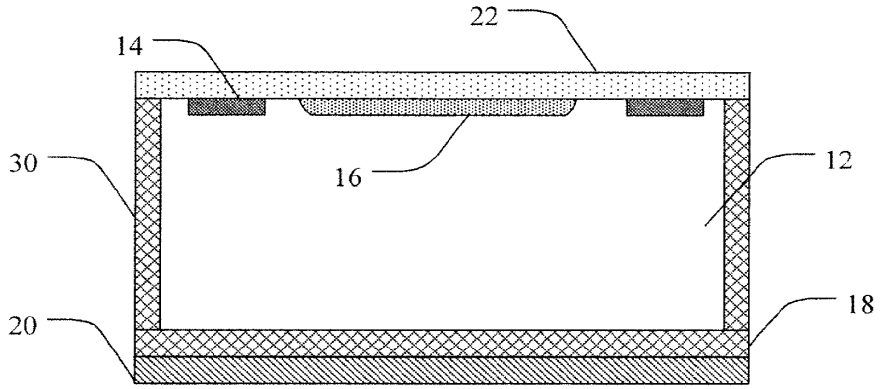


FIG. 3

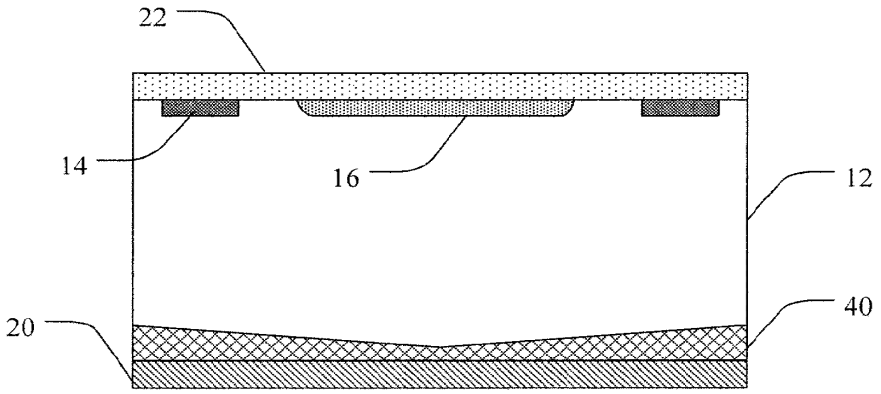


FIG. 4

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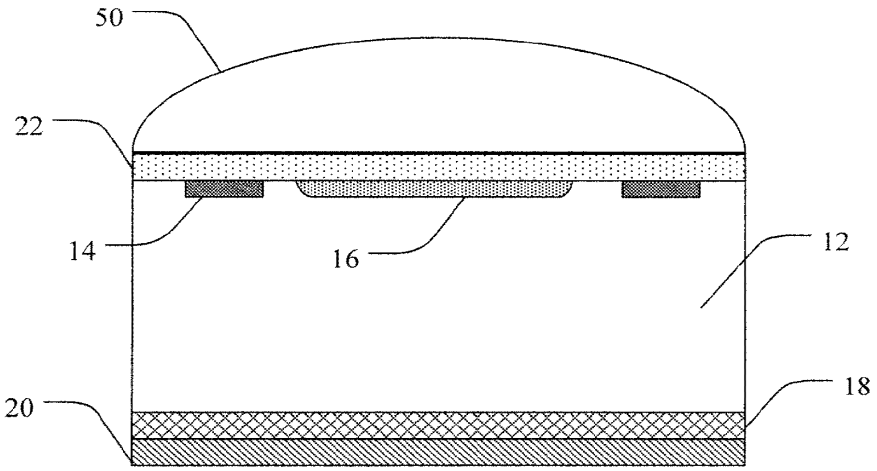


FIG. 5

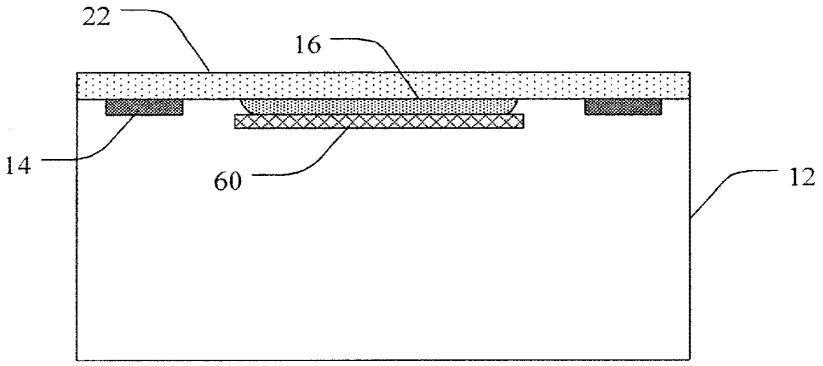


FIG. 6

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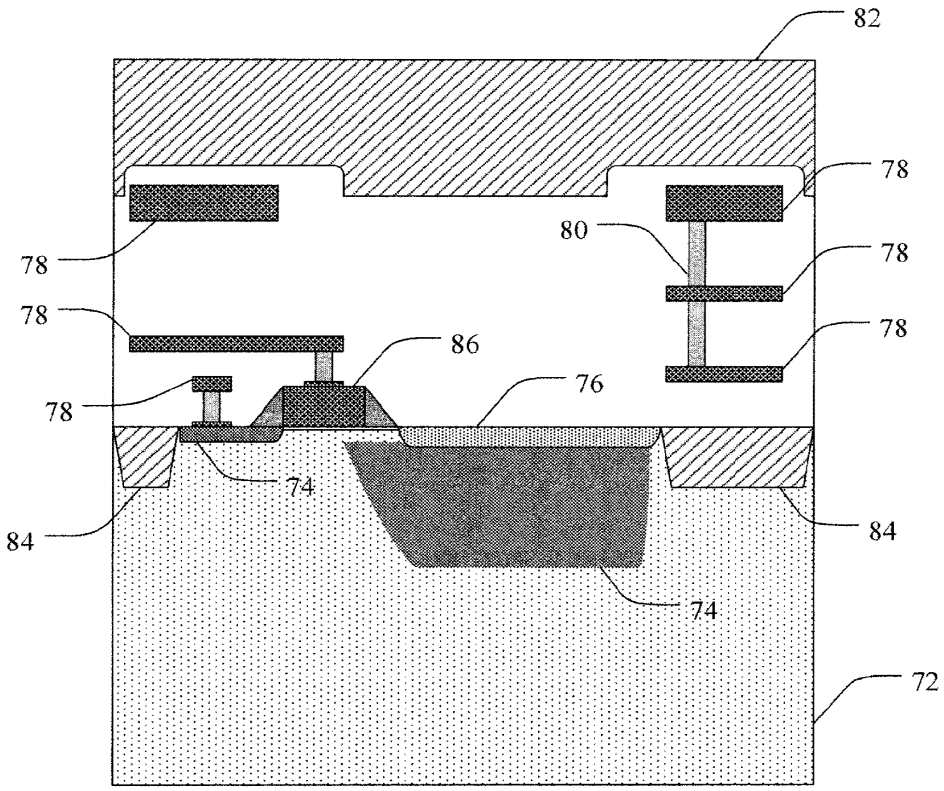


FIG. 7

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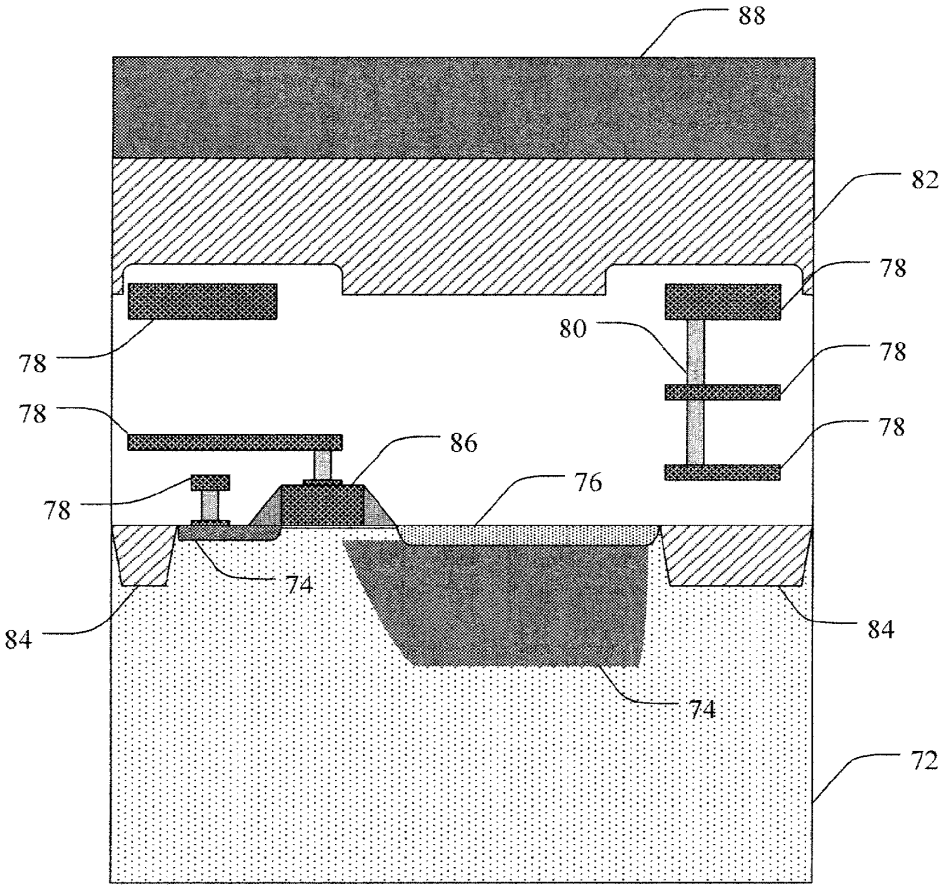


FIG. 8

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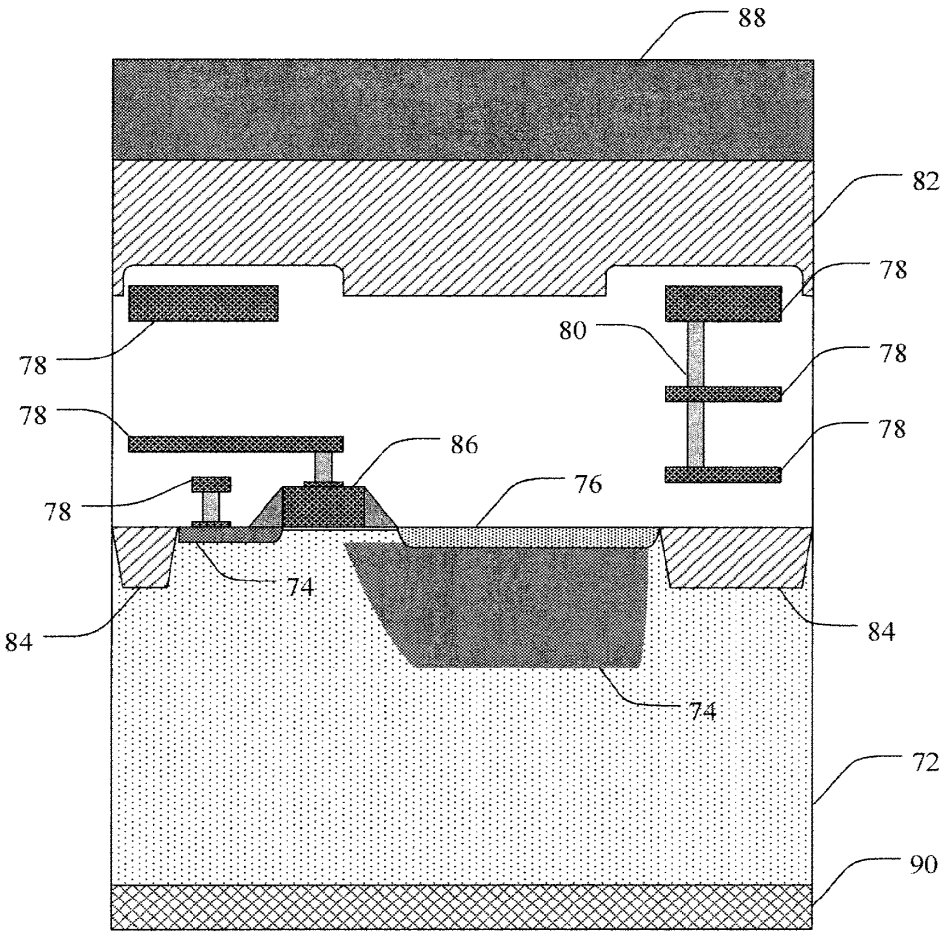


FIG. 9

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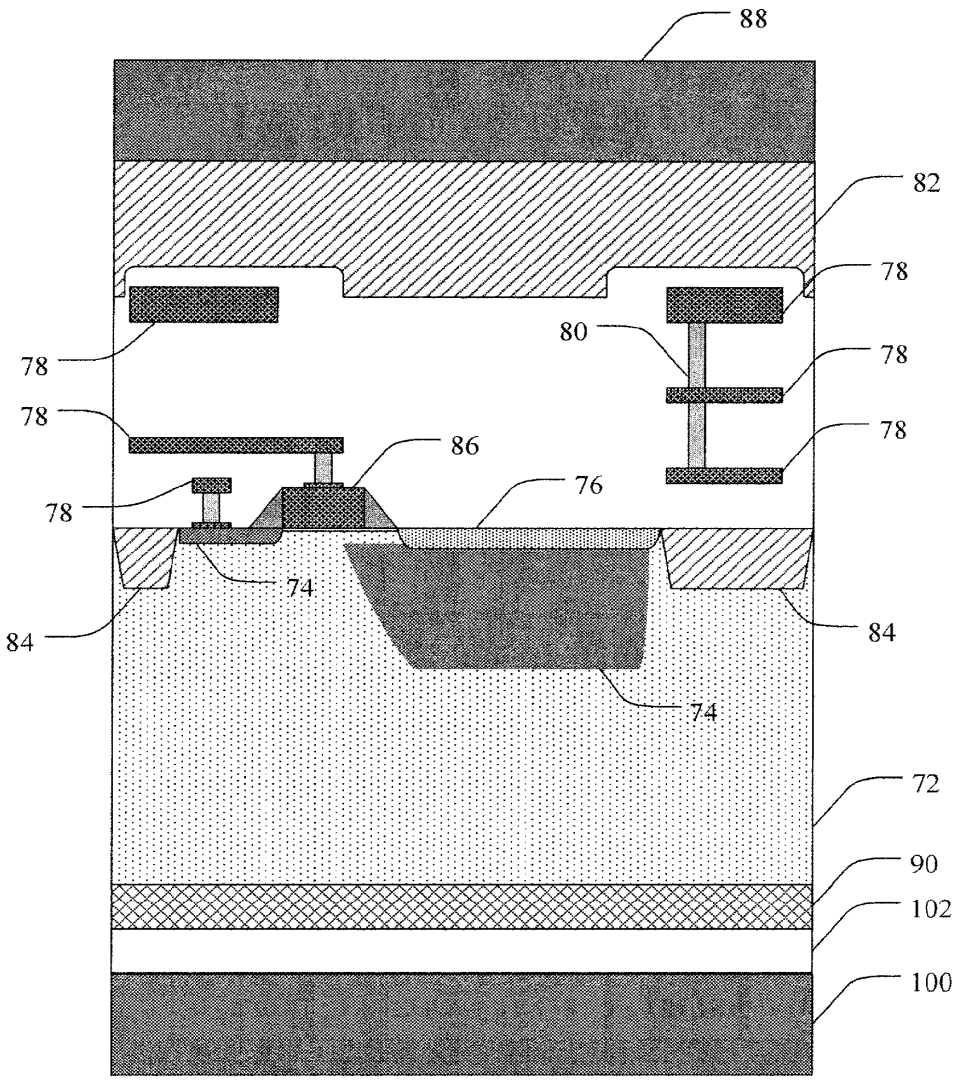


FIG. 10

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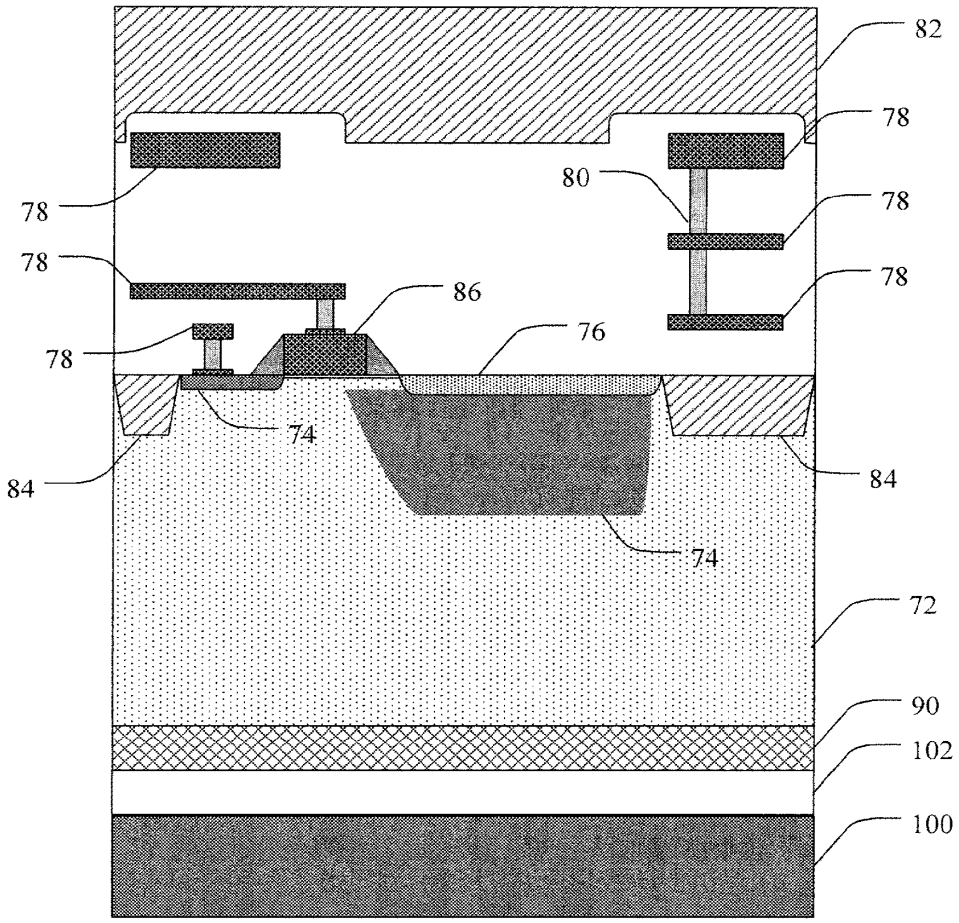


FIG. 11

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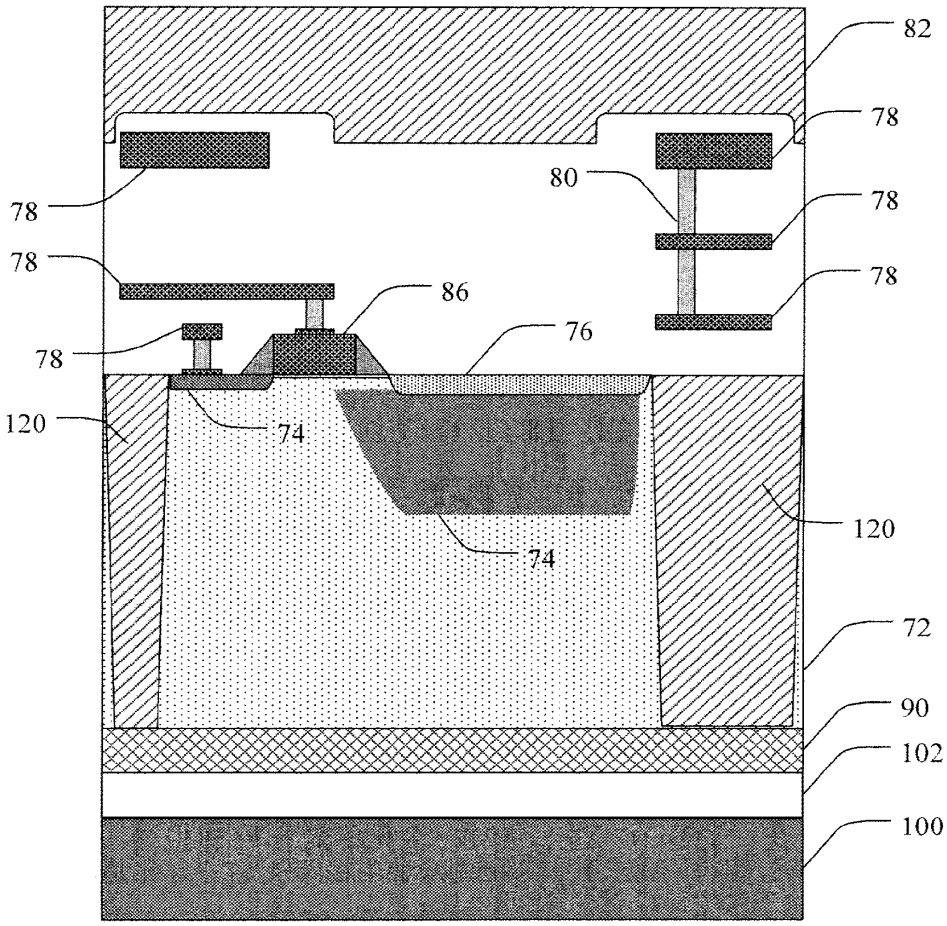


FIG. 12

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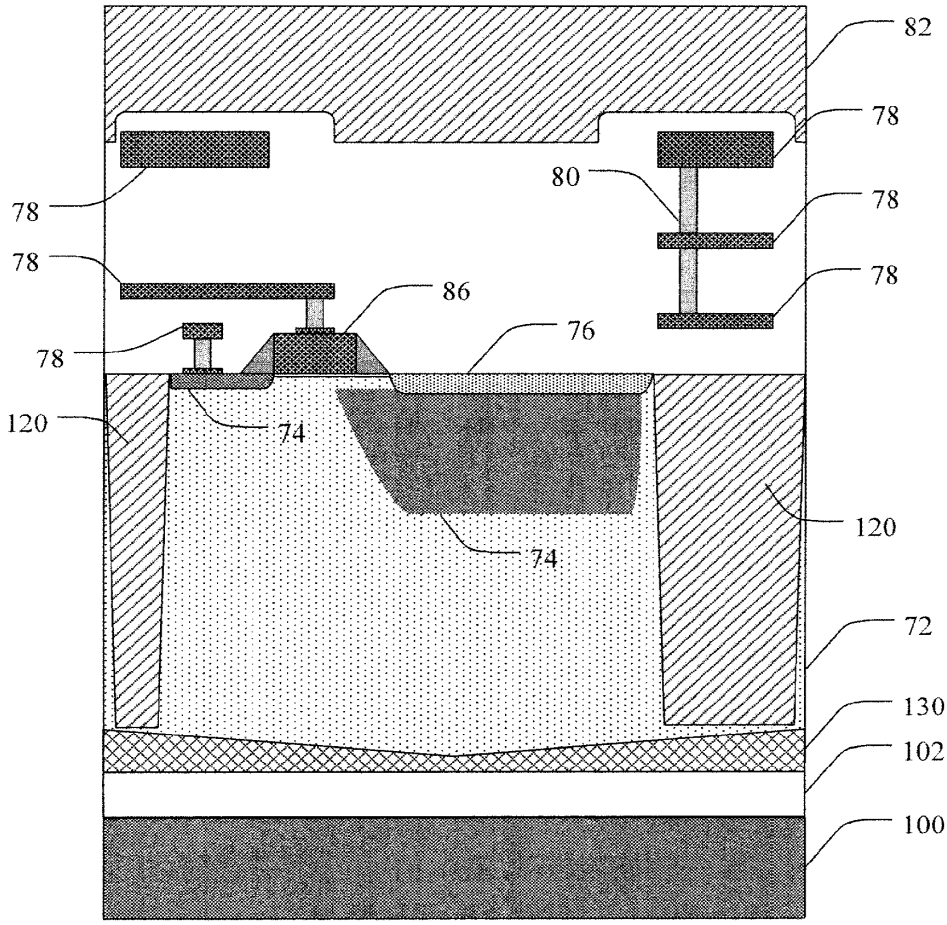


FIG. 13

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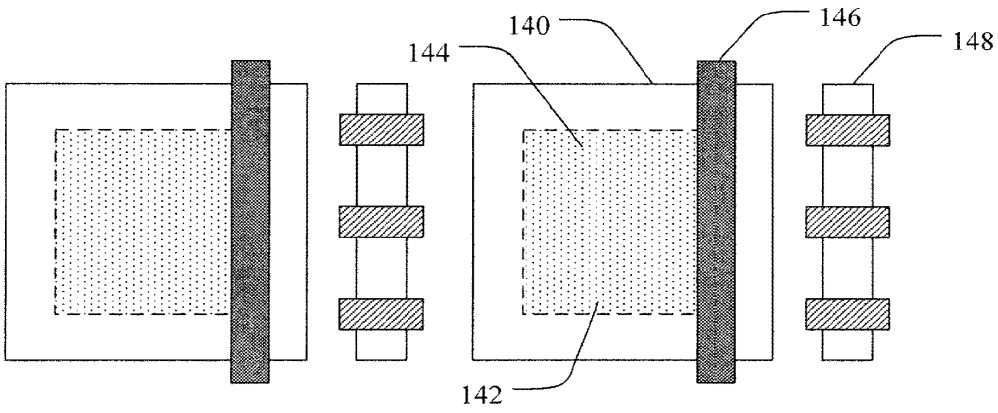


FIG. 14

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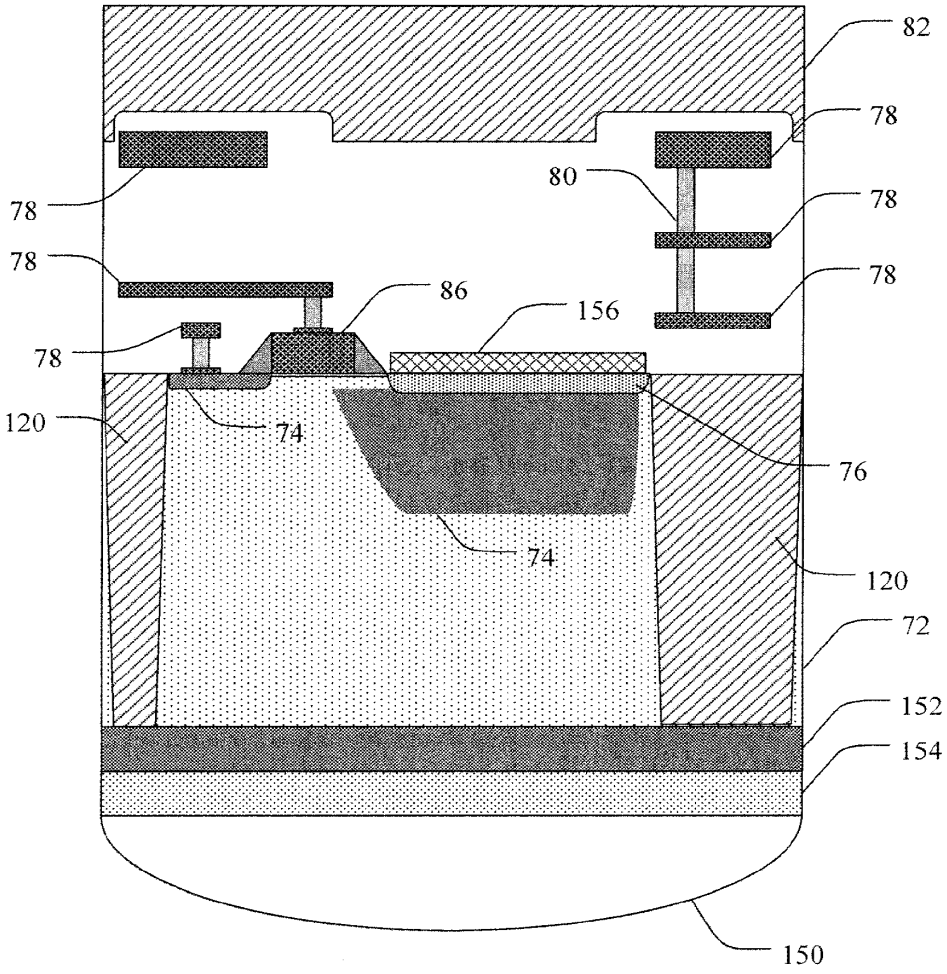


FIG. 15

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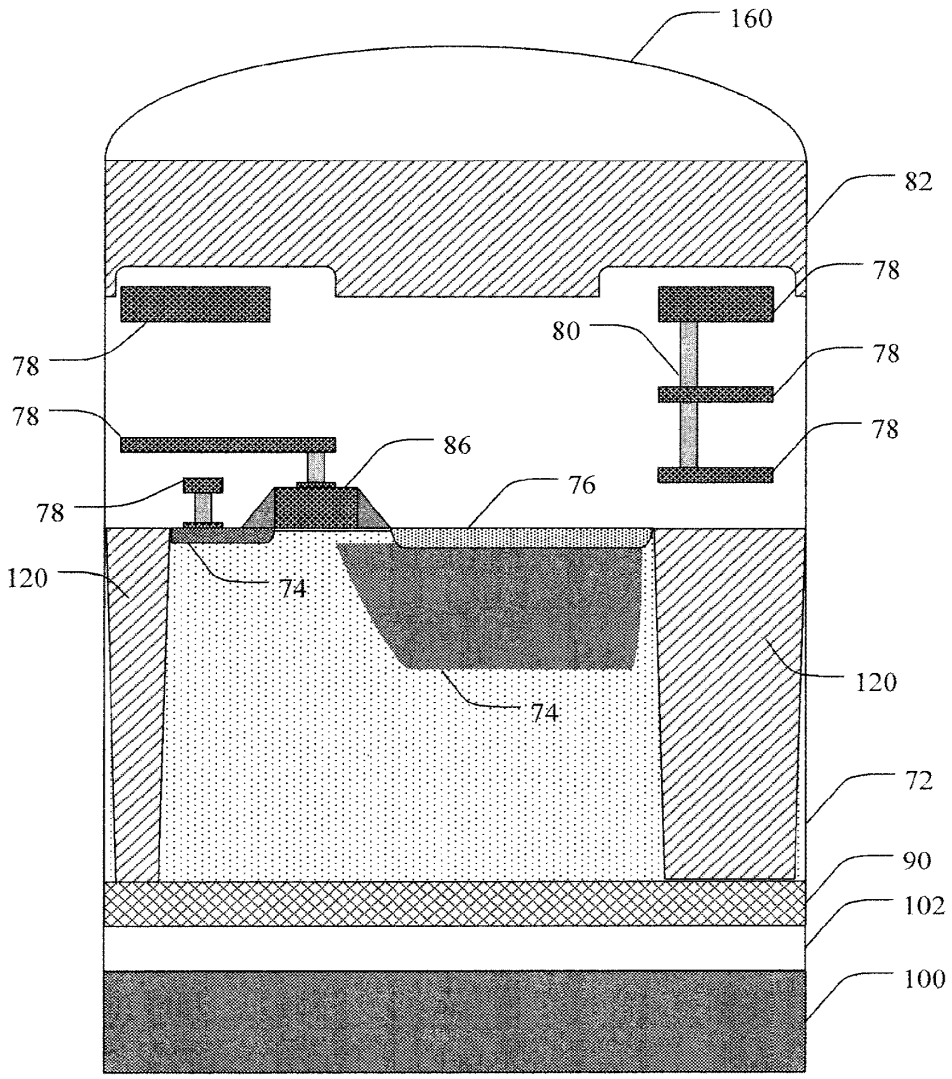


FIG. 16

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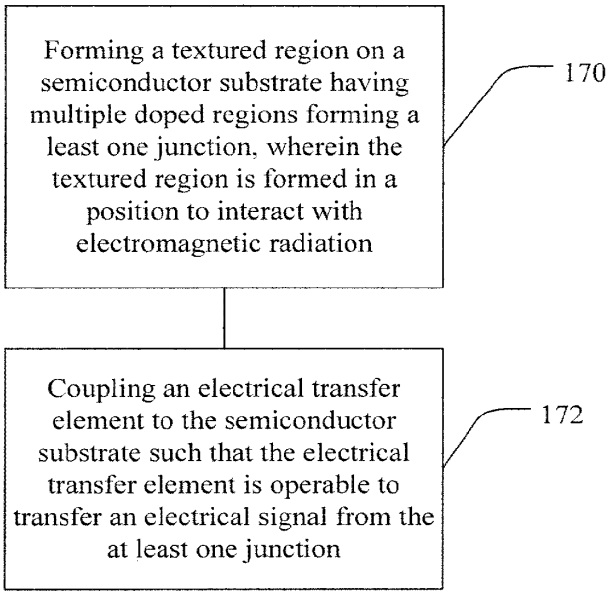


FIG. 17

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(54) **Title**: DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

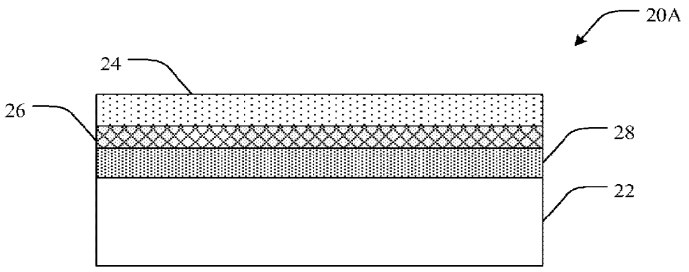


FIG. 2A

(57) **Abstract**: Photosensitive semiconductor devices and associated methods are provided. In one aspect, a semiconductor device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

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DEVICES HAVING ENHANCED ELECTROMAGNETIC RADIATION DETECTION AND ASSOCIATED METHODS

PRIORITY DATA

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/317,147, filed on March 24, 2010, which is incorporated herein by reference.

BACKGROUND

Semiconductor on Insulator (SOI) wafer technology is an outgrowth of MicroElectroMechanical Systems (MEMS) technologies. An SOI wafer is a stacked wafer substrate where a device wafer (typically silicon) is bonded to a dielectric layer that is bonded to a support wafer, otherwise known as a handle wafer. A typical process flow for the fabrication of SOI wafers can be as follows: two wafers are polished and coated with an oxide or other dielectric material. The wafers are mounted polished side face to face and bonded under high temperature and pressure. Then one of the two wafers is ground down using mechanical grinding and chemical mechanical polishing to a specific thickness. In this way it is possible to generate semiconductor wafers that are electrically isolated from the underlying substrate.

SUMMARY

The present disclosure provides semiconductor structures and devices that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. In one aspect, a semiconductor device is provided. Such a device can include a semiconductor substrate and a semiconductor layer coupled to the semiconductor substrate, where the semiconductor layer has a device surface opposite the semiconductor substrate. The device also includes at least one textured region coupled between the semiconductor substrate and the semiconductor layer. In another aspect, the device further includes at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, the semiconductor layer is a silicon layer. In a further aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer.

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Various positional configurations for the layers according to aspects of the present disclosure are contemplated, and any such configuration is considered to be within the present scope. In one specific aspect, for example, the dielectric layer is coupled between the semiconductor substrate and the textured region, and the textured region is disposed between the dielectric layer and the semiconductor layer. In one specific aspect, a reflective region is disposed between the semiconductor substrate and the textured region. In another specific aspect, the textured region is coupled directly to the semiconductor layer. In yet another specific aspect, a secondary semiconductor layer is disposed between the textured region and the semiconductor layer. In a further specific aspect, at least one cavity region disposed between the textured region and the dielectric layer. As another aspect of positional arrangement, the textured region is disposed between the semiconductor substrate and the dielectric layer, and the dielectric layer is disposed between the textured region and the semiconductor layer.

In one aspect of the present disclosure, a polysilicon layer is directly coupled to the dielectric layer. In another aspect, the polysilicon layer is disposed between multiple dielectric layers. In some aspects, the polysilicon layer can be doped.

In one aspect of the present disclosure, at least one photodiode optically active region is disposed on the device surface. In another aspect, the photodiode optically active region comprises a doped region. In yet another aspect, the device forms at least one photodetector. In a further aspect, the at least one photodetector is a plurality of photodetectors arranged in an array. In yet a further aspect, the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors. In another aspect, the device includes a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, where the isolation features isolate each photodetector electrically, optically, or both electrically and optically. In yet another aspect, the device includes at least one optical lens associated with the at least one photodetector. In a further aspect, the device includes at least one color filter associated with the at least one photodetector.

In one aspect of the present disclosure, the textured region is doped with a dopant to form an electrical back surface field. In another aspect, the electrical back surface field has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations

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thereof. In yet another aspect, the textured region has a higher dopant concentration than the semiconductor layer. In a further aspect, the dopant has the same polarity as the semiconductor layer. Non-limiting examples of such dopants can include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. Additionally, in other aspects a back surface field can be created by doping the semiconductor layer outside of the textured region. In one aspect, for example, the semiconductor layer is doped with a dopant to form an electrical back surface field, where the electrical back surface field is distinct from the textured region.

The present disclosure additionally provides methods of making semiconductor devices. In one aspect, one such method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate. In one aspect, the semiconductor layer is an epitaxially grown semiconductor layer. In another aspect, texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes forming the epitaxially grown semiconductor layer on a growth substrate and texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region. In yet another aspect, the method includes removing the growth substrate to expose the epitaxially grown semiconductor layer. In an alternative aspect, the method can include forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

In another aspect, wafer bonding includes depositing a polysilicon layer on the first dielectric layer and then bonding the polysilicon layer between the first dielectric layer and the second dielectric layer. In yet another aspect, at least a portion of the polysilicon layer can be doped. It is also contemplated that the present scope can include multiple dielectric and/or semiconductor material layers disposed between the semiconductor substrate and semiconductor layer.

In a further aspect, texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer and texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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In another aspect, the present disclosure provides a method of protecting a textured region from contamination during manufacture of a semiconductor device. Such a method includes texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

For a further understanding of the nature and advantage of the present disclosure, reference is being made to the following detailed description of embodiments and in connection with the accompanying drawings, in which:

FIG. 1 is a cross-sectional view of a semiconductor structure in accordance with an embodiment of the present disclosure;

FIG. 2A is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2B is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2C is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 2D is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 4 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 5 is a cross-sectional view of a semiconductor photodiode in accordance with another embodiment of the present disclosure;

FIG. 6 is a cross-sectional view of a semiconductor photodetecting imager in accordance with another embodiment of the present disclosure;

FIG. 7 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

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FIG. 8 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 9 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 10 is a cross-sectional view of a semiconductor structure in accordance with another embodiment of the present disclosure;

FIG. 11A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 11C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 12C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13A is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13B is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

FIG. 13C is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure;

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FIG. 13D is a cross-sectional view of a semiconductor structure showing the manufacture of a semiconductor device in accordance with another embodiment of the present disclosure; and

FIG. 14 is a depiction of a method of making a semiconductor device in accordance with yet another aspect of the present disclosure.

DETAILED DESCRIPTION

Before the present disclosure is described herein, it is to be understood that this disclosure is not limited to the particular structures, process steps, or materials disclosed herein, but is extended to equivalents thereof as would be recognized by those ordinarily skilled in the relevant arts. It should also be understood that terminology employed herein is used for the purpose of describing particular embodiments only and is not intended to be limiting.

Definitions

The following terminology will be used in accordance with the definitions set forth below.

It should be noted that, as used in this specification and the appended claims, the singular forms "a," and, "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a dopant" includes one or more of such dopants and reference to "the layer" includes reference to one or more of such layers.

As used herein, the terms "disordered surface" and "textured surface" can be used interchangeably, and refer to a surface having a topology with nano- to micron-sized surface variations. Although any texturing technique is considered to be within the present scope, in one aspect the texturing is formed by the irradiation of laser pulses. Furthermore, while the characteristics of a textured surface can be variable depending on the materials and techniques employed, in one aspect such a surface can be several hundred nanometers thick and made up of nanocrystallites (e.g. from about 10 to about 50 nanometers), nanopores, and the like. In another aspect, such a surface can include micron-sized structures (e.g. about 2 μm to about 60 μm). In yet another aspect, the surface can include nano-sized and/or micron-sized structures from about 5 nm and about 500 μm.

As used herein, the terms "surface modifying," "surface modification," and "texturing" can be used interchangeably, and refer to the altering of a surface of a

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semiconductor material using a texturing technique. In one specific aspect, surface modification can include processes using primarily laser radiation or laser radiation in combination with a dopant, whereby the laser radiation facilitates the incorporation of the dopant into a surface of the semiconductor material. Accordingly, in one aspect surface modification includes doping the material.

As used herein, the term "fluence" refers to the amount of energy from a single pulse of laser radiation that passes through a unit area. In other words, "fluence" can be described as the energy density of one laser pulse.

As used herein, the term "target region" refers to an area of a semiconductor material that is intended to be doped or surface modified using laser radiation. The target region of a semiconductor material can vary as the surface modifying process progresses. For example, after a first target region is doped or surface modified, a second target region may be selected on the same semiconductor material.

As used herein, the term "absorptance" refers to the fraction of incident electromagnetic radiation absorbed by a material or device.

As used herein, the term "substantially" refers to the complete or nearly complete extent or degree of an action, characteristic, property, state, structure, item, or result. For example, an object that is "substantially" enclosed would mean that the object is either completely enclosed or nearly completely enclosed. The exact allowable degree of deviation from absolute completeness may in some cases depend on the specific context. However, generally speaking the nearness of completion will be so as to have the same overall result as if absolute and total completion were obtained. The use of "substantially" is equally applicable when used in a negative connotation to refer to the complete or near complete lack of an action, characteristic, property, state, structure, item, or result. For example, a composition that is "substantially free of" particles would either completely lack particles, or so nearly completely lack particles that the effect would be the same as if it completely lacked particles. In other words, a composition that is "substantially free of" an ingredient or element may still actually contain such item as long as there is no measurable effect thereof.

As used herein, the term "about" is used to provide flexibility to a numerical range endpoint by providing that a given value may be "a little above" or "a little below" the endpoint.

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As used herein, a plurality of items, structural elements, compositional elements, and/or materials may be presented in a common list for convenience. However, these lists should be construed as though each member of the list is individually identified as a separate and unique member. Thus, no individual member of such list should be construed as a de facto equivalent of any other member of the same list solely based on their presentation in a common group without indications to the contrary.

Concentrations, amounts, and other numerical data may be expressed or presented herein in a range format. It is to be understood that such a range format is used merely for convenience and brevity and thus should be interpreted flexibly to include not only the numerical values explicitly recited as the limits of the range, but also to include all the individual numerical values or sub-ranges encompassed within that range as if each numerical value and sub-range is explicitly recited. As an illustration, a numerical range of "about 1 to about 5" should be interpreted to include not only the explicitly recited values of about 1 to about 5, but also include individual values and sub-ranges within the indicated range. Thus, included in this numerical range are individual values such as 2, 3, and 4 and sub-ranges such as from 1-3, from 2-4, and from 3-5, etc., as well as 1, 2, 3, 4, and 5, individually.

This same principle applies to ranges reciting only one numerical value as a minimum or a maximum. Furthermore, such an interpretation should apply regardless of the breadth of the range or the characteristics being described.

The Disclosure

The present disclosure provides semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties. Additionally, the present disclosure provides an integrated approach for the fabrication and application of textured semiconductor materials resulting in enhancement of image sensors and photodetectors. Specific types of semiconductor texturing can enhance the spectral bandwidth, absorption, and quantum efficiency of a semiconductor material. Performance can also be enhanced through various architecture configurations. Such configurations can also significantly improve the process integration of a particular device architecture with traditional process flows such as, for example, traditional CMOS process flows.

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A device design having a textured region located on, for example, the back surface of a photodetector, provides significant performance benefits. The textured region can have surface features that can lead to higher recombination of photocarriers for short wavelengths (e.g. in the blue green part of the spectrum) due to the very shallow penetration of those wavelengths into the detecting volume of the device. By physically locating the textured on the back surface of the device, a pristine surface is provided for the collection of short wavelengths on the top surface (i.e. the light incident surface), and the longer wavelengths that penetrate deep into or through the detecting region of the semiconductor material are collected by or with the help of the textured region opposite the light incident surface. It should be noted that, in addition to backside illuminated, front side illuminated architectures are also contemplated to be within the present scope. In addition, enhanced performance and ease of manufacture can also be accomplished by locating a textured region within a semiconductor stack or wafer. In some aspects, the textured layer can be located within the semiconductor stack early in the manufacturing process prior to the deposition of structures or circuitry that may be negatively affected by a texturing process. Additionally, such a semiconductor stack can be sent to an outside fabrication process for further manufacturing without exposing technological details regarding the textured region embedded between the semiconductor layers or any interaction between the textured region and the semiconductor layers.

In one aspect, as is shown in FIG. 1, a semiconductor device 10 is provided. While various semiconductor functions are contemplated, in one aspect the semiconductor device can exhibit enhanced electromagnetic radiation detection. Such a device can include a semiconductor substrate 12 and a semiconductor layer 14 coupled to the semiconductor substrate. The semiconductor layer has a device surface 15 opposite the semiconductor substrate. The device also includes at least one textured region 16 located or coupled between the semiconductor substrate and the semiconductor layer. As such, the textured region is enclosed between the semiconductor substrate and the semiconductor layer. Subsequent processing of the semiconductor device such as, for example, the formation of structures on the device surface, does not affect this buried textured region. In one aspect, the textured region can be formed on the semiconductor substrate. In another aspect, the textured region can be formed on the semiconductor layer. Additionally, for FIG. 1 and subsequent figures, the textured region can be a single textured region as is shown, or the textured

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region can be multiple discrete textured regions. Also, the textured region can cover only a portion of the surface area between the semiconductor substrate and the semiconductor layer as is shown, or the textured region can cover the entire surface area there between.

In another aspect, as is shown in FIG. 2A, a semiconductor device 20A is provided. Such a device can include a semiconductor substrate 22 and a semiconductor layer 24 coupled to the semiconductor substrate. The device also includes at least one textured region 26 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 28 coupled between the semiconductor substrate and the semiconductor layer. While various utilities are contemplated for the dielectric layer, in one aspect such a layer can be used to wafer bond the semiconductor layer to the semiconductor substrate. In one aspect, the dielectric layer can be formed on the semiconductor substrate. In another aspect, the dielectric layer can be formed on the textured region. Also, in some aspects the textured region can be formed on the dielectric layer. Additionally, in one aspect the semiconductor layer can be an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the epitaxially grown semiconductor layer.

It should be noted that, for all aspects, the present scope can also include multiple dielectric layers and/or multiple semiconductor material layers disposed between the semiconductor substrate and semiconductor layer. Additionally, the semiconductor layer itself can be multiple semiconductor layers and the semiconductor substrate can include multiple layers. It should also be noted that the semiconductor substrate refers to a substrate for a semiconductor, and can be comprised of semiconductor materials and/or non-semiconductor materials.

FIG. 2B shows a semiconductor device 20B having a secondary semiconductor layer 27 located between the textured region and the semiconductor layer. A semiconductor layer 24 is formed on the secondary semiconductor layer. In one aspect the semiconductor layer is an epitaxially grown semiconductor layer. Thus in some aspects, the textured region can be formed on the secondary semiconductor layer or on the dielectric layer 28. It should be noted that all reference numbers in FIGs. 2B-D that have been reused from FIG. 2A denote the same or similar materials and/or structures whether or not further description is provided.

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FIG. 2C shows a semiconductor device 20C whereby the dielectric layer 28 coupled between the semiconductor layer and the textured region. In this case, the dielectric layer can be formed on the semiconductor layer 24, the textured region 28, or on both the semiconductor layer and the textured region. In one aspect, the textured region can be formed on the semiconductor substrate 22. In another aspect, the textured region can be formed on the dielectric layer.

Additionally, in some aspects, as is shown in FIG. 2D for semiconductor device 20D, the dielectric layer can be a plurality of dielectric layers 28. In the case of wafer bonding, for example, a first dielectric layer can be associated with the textured layer and a second dielectric layer can be associated with the semiconductor substrate. The first dielectric layer and the second dielectric layer are heated and pressed together, with or without the aid of further pressure, temperature, or plasma surface activation, to cause the dielectric layers to bond to one another, thus forming a single wafer-bonded structure. It should be noted, however, that wafer-bonding can be accomplished without one or more dielectric layers, and as such the present scope should also include wafer-bonding that lacks such dielectric materials. Additionally, in some aspects, the textured region can be located in between the plurality of dielectric layers (not shown).

A variety of semiconductor materials are contemplated for use with the devices and methods according to aspects of the present disclosure. Such materials can be utilized as the semiconductor layer and/or the semiconductor substrate, as well as for the secondary semiconductor layer and the epitaxially grown semiconductor layer. Non-limiting examples of such semiconductor materials can include group IV materials, compounds and alloys comprised of materials from groups II and VI, compounds and alloys comprised of materials from groups III and V, and combinations thereof. More specifically, exemplary group IV materials can include silicon, carbon (e.g. diamond), germanium, and combinations thereof. Various exemplary combinations of group IV materials can include silicon carbide (SiC) and silicon germanium (SiGe). In one specific aspect, the semiconductor material can be or include silicon. Exemplary silicon materials can include amorphous silicon (a-Si), microcrystalline silicon, multicrystalline silicon, and monocrystalline silicon, as well as other crystal types. In another aspect, the semiconductor material can include at least one of silicon, carbon, germanium, aluminum nitride, gallium nitride, indium gallium arsenide, aluminum gallium arsenide, and combinations thereof.

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Exemplary combinations of group II-VI materials can include cadmium selenide (CdSe), cadmium sulfide (CdS), cadmium telluride (CdTe), zinc oxide (ZnO), zinc selenide (ZnSe), zinc sulfide (ZnS), zinc telluride (ZnTe), cadmium zinc telluride (CdZnTe, CZT), mercury cadmium telluride (HgCdTe), mercury zinc telluride (HgZnTe), mercury zinc selenide (HgZnSe), and combinations thereof.

Exemplary combinations of group III-V materials can include aluminum antimonide (AlSb), aluminum arsenide (AlAs), aluminum nitride (AlN), aluminum phosphide (AlP), boron nitride (BN), boron phosphide (BP), boron arsenide (BAs), gallium antimonide (GaSb), gallium arsenide (GaAs), gallium nitride (GaN), gallium phosphide (GaP), indium antimonide (InSb), indium arsenide (InAs), indium nitride (InN), indium phosphide (InP), aluminum gallium arsenide (AlGaAs, $Al_xGa_{1-x}As$), indium gallium arsenide (InGaAs, $In_xGa_{1-x}As$), indium gallium phosphide (InGaP), aluminum indium arsenide (AlInAs), aluminum indium antimonide (AlInSb), gallium arsenide nitride (GaAsN), gallium arsenide phosphide (GaAsP), aluminum gallium nitride (AlGaN), aluminum gallium phosphide (AlGaP), indium gallium nitride (InGaN), indium arsenide antimonide (InAsSb), indium gallium antimonide (InGaSb), aluminum gallium indium phosphide (AlGaInP), aluminum gallium arsenide phosphide (AlGaAsP), indium gallium arsenide phosphide (InGaAsP), aluminum indium arsenide phosphide (AlInAsP), aluminum gallium arsenide nitride (AlGaAsN), indium gallium arsenide nitride (InGaAsN), indium aluminum arsenide nitride (InAlAsN), gallium arsenide antimonide nitride (GaAsSbN), gallium indium nitride arsenide antimonide (GaInNAsSb), gallium indium arsenide antimonide phosphide (GaInAsSbP), and combinations thereof.

The semiconductor material can be of any thickness that allows the desired property or functionality of the semiconductor device, and thus any such thickness of semiconductor material is considered to be within the present scope. The textured region can increase the efficiency of the device such that, in some aspects, the semiconductor material can be thinner than has previously been possible. Decreasing the thickness reduces the amount of semiconductor material used to make such a device. In one aspect, for example, a semiconductor material such as the semiconductor layer has a thickness of from about 500 nm to about 50 μm. In another aspect, the semiconductor material has a thickness of less than or equal to about 500 μm. In yet another aspect, the semiconductor material has a thickness of from about 1 μm to about 10 μm. In a further aspect, the semiconductor material can have a

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thickness of from about 5 μm to about 750 μm. In yet a further aspect, the semiconductor material can have a thickness of from about 5 μm to about 100 μm.

Additionally, various configurations of semiconductor materials are contemplated, and any such material configuration that can be incorporated into a semiconductor device is considered to be within the present scope. In one aspect, for example, the semiconductor material can include monocrystalline materials. In another aspect, the semiconductor material can include multicrystalline materials. In yet another aspect, the semiconductor material can include microcrystalline materials. It is also contemplated that the semiconductor material can include amorphous materials.

As has been described, the semiconductor substrate can be of any size, shape, and material capable of supporting the semiconductor layer and associated components during manufacture and/or use. The semiconductor substrate can be made from various materials, including the semiconductor materials described above, as well as non-semiconductor materials. Non-limiting examples of such materials can include metals, polymeric materials, ceramics, glass, and the like. In some aspects, the semiconductor substrate and the semiconductor layer have the same or substantially the same thermal expansion properties.

Furthermore, the semiconductor material according to aspects of the present disclosure can comprise multiple layers. In some aspects, layers can vary in majority carrier polarity (i.e. donor or acceptor impurities). The donor or acceptor impurities are typically determined by the type of dopant/impurities introduced into the device either through a growth process, deposition process, epitaxial process, implant process, lasing process or other known process to those skilled in the art. In some aspects such semiconductor materials can include an n-type layer, an intrinsic (i-type) layer, and a p-type layer, thus forming a p-i-n semiconductor material stack that creates a junction and/or depletion region. A semiconductor material devoid of an i-type layer is also contemplated in accordance with the present disclosure. In other aspects the semiconductor material may include multiple junctions. Additionally, in some aspects, variations of n(--), n(-), n(+), n(++), p(--), p(-), p(+), or p(++) type semiconductor layers can be used. The minus and positive signs are indicators of the relative magnitude of the doping of the semiconductor material.

As has been described, the textured region is buried between the semiconductor substrate and the semiconductor layer in various architectural

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arrangements. The textured can be of various thicknesses, depending on the desired use of the material. In one aspect, for example, the textured region has a thickness of from about 500 nm to about 100 μm. In another aspect, the textured region has a thickness of from about 500 nm to about 15 μm. In yet another aspect, the textured region has a thickness of from about 500 nm to about 2 μm. In a further aspect, the textured region has a thickness of from about 500 nm to about 1 μm. In another aspect, the textured region has a thickness of from about 200 nm to about 2 μm.

The textured region can function to diffuse electromagnetic radiation, to redirect electromagnetic radiation, and/or to absorb electromagnetic radiation, thus increasing the quantum efficiency of the device. The textured region can include surface features to further increase the effective absorption length of the device. Non-limiting examples of shapes and configurations of surface features include cones, pillars, pyramids, micolenses, quantum dots, inverted features, gratings, protrusions, sphere-like structures, and the like, including combinations thereof. Additionally, surface features can be micron-sized, nano-sized, or a combination thereof. For example, cones, pyramids, protrusions, and the like can have an average height within this range. In one aspect, the average height would be from the base of the feature to the distal tip of the feature. In another aspect, the average height would be from the surface plane upon which the feature was created to the distal tips of the feature. In one specific aspect, a feature (e.g. a cone) can have a height of from about 50 nm to about 2 μm. As another example, quantum dots, microlenses, and the like can have an average diameter within the micron-sized and/or nano-sized range.

In addition to or instead of surface features, the textured region can include a textured layer. In one aspect, for example, the textured region can include a substantially conformal textured layer. Such a textured layer can have an average thickness of from about 1 nm to about 20 μm. In those aspects where the textured region includes surface features, the conformal textured layer can have a varying thickness relative to the location on the surface features upon which is deposited. In the case of cones, for example, the conformal textured layer can become thinner toward the tips of the cones. Such a conformal layer can include various materials, including, without limitation, SiO_2, Si_3N_4, amorphous silicon, polysilicon, a metal or metals, and the like, including combinations thereof. The conformal textured layer can also be one or more layers of the same or different materials, and can be formed during the creation of surface features or in a separate process.

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Textured regions according to aspects of the present disclosure can allow a photosensitive device to experience multiple passes of incident electromagnetic radiation within the device, particularly at longer wavelengths (i.e. infrared). Such internal reflection increases the effective absorption length to be greater than the thickness of the semiconductor layer. This increase in absorption length increases the quantum efficiency of the device, leading to an improved signal to noise ratio.

The materials used for making the textured region can vary depending on the design and the desired characteristics of the device. As such, any material that can be utilized in the construction of a textured region is considered to be within the present scope. In one aspect, for example, the texture region can be a textured portion of a specific material, such as a portion of the semiconductor layer or the semiconductor substrate. If the texture layer is to be associated with the semiconductor layer, for example, a surface facing the semiconductor substrate can be textured prior to an attachment process such as wafer bonding. In another aspect, the textured region can be formed from a material that is deposited onto the semiconductor layer or semiconductor substrate, or the textured layer itself can be deposited. Such materials can include a semiconductor material, a dielectric material, or the like, including combinations thereof. In one specific example, the deposited material can include a silicon material. In another specific example, the deposited material can be polysilicon. In yet another aspect, the deposited material can be a dielectric material.

The texturing process can texture the entire substrate to be processed or only a portion of the substrate. In one aspect, for example, a substrate such as the semiconductor layer can be textured and patterned by an appropriate technique over an entire surface to form the texture region. In another aspect, a substrate such as the semiconductor layer can be textured and patterned across only a portion of a surface by using a selective etching technique, such as a mask, photolithography, and an etch or a laser process to define a specific structure or pattern.

In addition to surface features, the textured region can have a surface morphology that is designed to focus or otherwise direct electromagnetic radiation. For example, in one aspect the textured region has a surface morphology operable to direct electromagnetic radiation into the semiconductor layer. Non-limiting examples of various surface morphologies include sloping, pyramidal, inverted pyramidal, spherical, square, rectangular, parabolic, asymmetric, symmetric, and the like, including combinations thereof.

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The textured region, including surface features as well as surface morphologies, can be formed by various techniques, including plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching (e.g. anisotropic etching, isotropic etching), nanoimprinting, material deposition, selective epitaxial growth, and the like.

One effective method of producing a textured region is through laser processing. Such laser processing allows discrete target areas of a substrate to be textured, as well as entire surfaces. A variety of techniques of laser processing to form a textured region are contemplated, and any technique capable of forming such a region should be considered to be within the present scope. Laser treatment or processing can allow, among other things, enhanced absorption properties and thus increased electromagnetic radiation focusing and detection.

In one aspect, for example, a target region of the substrate to be textured can be irradiated with laser radiation to form a textured region. Examples of such processing have been described in further detail in U.S. Patents 7,057,256, 7,354,792 and 7,442,629, which are incorporated herein by reference in their entireties. Briefly, a surface of a substrate material is irradiated with laser radiation to form a textured or surface modified region. Such laser processing can occur with or without a dopant material. In those aspects whereby a dopant is used, the laser can passed through a dopant carrier and onto the substrate surface. In this way, dopant from the dopant carrier is introduced into the target region of the substrate material. Such a region incorporated into a substrate material can have various benefits in accordance with aspects of the present disclosure. For example, the textured region typically has a textured surface that increases the surface area and increases the probability of radiation absorption. In one aspect, such a textured region is a substantially textured surface including micron-sized and/or nano-sized surface features that have been generated by the laser texturing. In another aspect, irradiating the surface of a substrate material includes exposing the laser radiation to a dopant such that irradiation incorporates the dopant into the substrate. Various dopant materials are known in the art, and are discussed in more detail herein.

Thus the surface of the substrate at the target region is thus chemically and/or structurally altered by the laser treatment, which may, in some aspects, result in the formation of surface features appearing as structures or patterned areas on the surface and, if a dopant is used, the incorporation of such dopants into the substrate material.

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In some aspects, the features or structures can be on the order of 50 nm to 20 μm in size and can assist in the absorption of electromagnetic radiation. In other words, the textured surface can increase the probability of incident radiation being absorbed.

The type of laser radiation used to surface modify a material can vary depending on the material and the intended modification. Any laser radiation known in the art can be used with the devices and methods of the present disclosure. There are a number of laser characteristics, however, that can affect the surface modification process and/or the resulting product including, but not limited to, the wavelength of the laser radiation, pulse width, pulse fluence, pulse frequency, polarization, laser propagation direction relative to the semiconductor material, etc. In one aspect, a laser can be configured to provide pulsatile lasing of a material. A short-pulsed laser is one capable of producing femtosecond, picosecond, and/or nanosecond pulse durations. Laser pulses can have a central wavelength in a range of about from about 10 nm to about 8 μm, and more specifically from about 200 nm to about 1200 nm. The pulse width of the laser radiation can be in a range of from about tens of femtoseconds to about hundreds of nanoseconds. In one aspect, laser pulse widths can be in the range of from about 50 femtoseconds to about 50 picoseconds. In another aspect, laser pulse widths can be in the range of from about 50 picoseconds to 100 nanoseconds. In another aspect, laser pulse widths are in the range of from about 50 to 500 femtoseconds.

The number of laser pulses irradiating a target region can be in a range of from about 1 to about 2000. In one aspect, the number of laser pulses irradiating a target region can be from about 2 to about 1000. Further, the repetition rate or frequency of the pulses can be selected to be in a range of from about 10 Hz to about 10 μHz, or in a range of from about 1 kHz to about 1 MHz, or in a range from about 10 Hz to about 1 kHz. Moreover, the fluence of each laser pulse can be in a range of from about 1 kJ/m^2 to about 20 kJ/m^2, or in a range of from about 3 kJ/m^2 to about 8 kJ/m^2.

A variety of dopant materials are contemplated for both the formation of doped regions in the semiconductor layer and for doping of the textured region, and any dopant that can be used in such processes to modify a material is considered to be within the present scope. It should be noted that the particular dopant utilized can vary depending on the material being doped, as well as the intended use of the resulting material.

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A dopant can be either a charge donating or a charge accepting dopant species. More specifically, an electron donating or a hole donating species can cause a region to become more positive or negative in polarity as compared to the substrate upon which the rests. In one aspect, for example, the doped region can be p-doped. In another aspect the doped region can be n-doped.

In one aspect, non-limiting examples of dopant materials can include S, F, B, P, N, As, Se, Te, Ge, Ar, Ga, In, Sb, and combinations thereof. It should be noted that the scope of dopant materials should include, not only the dopant materials themselves, but also materials in forms that deliver such dopants (i.e. dopant carriers). For example, S dopant materials includes not only S, but also any material capable being used to dope S into the target region, such as, for example, H_2S, SF_6, SO_2, and the like, including combinations thereof. In one specific aspect, the dopant can be S. Sulfur can be present at an ion dosage level of from about 5×10^{14} to about 3×10^{20} ions/cm^2. Non-limiting examples of fluorine-containing compounds can include ClF_3, PF_5, F_2 SF_6, BF_3, GeF_4, WF_6, SiF_4, HF, CF_4, CHF_3, CH_2F_2, CH_3F, C_2F_6, C_2HF_5, C_3F_8, C_4F_8, NF_3, and the like, including combinations thereof. Non-limiting examples of boron-containing compounds can include $B(CH_3)_3$, BF_3, BCl_3, BN, $C_2B_{10}H_{12}$, borosilica, B_2H_6, and the like, including combinations thereof. Non-limiting examples of phosphorous-containing compounds can include PF_5, PH_3, $POCl_3$, P_2O_5, and the like, including combinations thereof. Non-limiting examples of chlorine-containing compounds can include Cl_2, SiH_2Cl_2, HCl, $SiCl_4$, and the like, including combinations thereof. Dopants can also include arsenic-containing compounds such as AsH_3 and the like, as well as antimony-containing compounds. Additionally, dopant materials can include mixtures or combinations across dopant groups, i.e. a sulfur-containing compound mixed with a chlorine-containing compound. In one aspect, the dopant material can have a density that is greater than air. In one specific aspect, the dopant material can include Se, H_2S, SF_6, or mixtures thereof. In yet another specific aspect, the dopant can be SF_6 and can have a predetermined concentration range of about 5.0×10^{-8} mol/cm^3 to about 5.0×10^{-4} mol/cm^3. As one non-limiting example, SF_6 gas is a good carrier for the incorporation of sulfur into a substrate via a laser process without significant adverse effects on the material. Additionally, it is noted that dopants can also be liquid solutions of n-type or p-type dopant materials dissolved in a solution such as water, alcohol, or an acid or basic

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solution. Dopants can also be solid materials applied as a powder or as a suspension dried onto the wafer.

In one aspect, the textured region can be doped with a dopant to form an electrical back surface field (EBSF). The EBSF impedes the movement of minority carriers from reaching the textured region, thus keeping such carriers away from potential recombination sites near the interface. Similarly, dark current generation can also be minimized by pinning the interface generation states at certain band energy states through band structure optimization so that the dark carrier generation mechanism is suppressed. Band structure optimization can be achieved by using a variety of methods. It should be noted that any method that forms an electrical field near or within the textured region can be used. Non-limiting examples of such methods can include shifting the Fermi level energy, bending the minority carrier band, inserting a material with a different bandgap, and the like, including combinations thereof.

In one aspect, for example, the band structure optimization can be realized by modifying the interface doping concentration. For example, for a p-type laser textured region, a more heavily p-doped layer that partially overlaps with the laser modified interface can be used. The conduction band thus bends toward the higher energy direction when reaching towards the more p-doped layer, and hence the laser modified interface. One specific aspect is a heavily doped p++ layer that partially overlaps with the laser modified interface layer in a p-epi substrate where both the p++ layer and the modified interface layer sit between the bottom of an epitaxial device layer and the top of a carrier wafer.

As such, in one aspect, the EBSF has been doped by a technique such as, without limitation, laser doping, ion implanting, diffusion doping, in situ doping, and the like, including combinations thereof. In another aspect, the textured region or the EBSF has a higher dopant concentration than the semiconductor layer. In yet another aspect, the dopant has the same polarity as the semiconductor layer. Various dopants for use in generating an EBSF are contemplated. Non-limiting examples include boron, indium, gallium, arsenic, antimony, phosphorus, and the like, including combinations thereof. It should also be noted that an EBSF can be produced in the semiconductor layer, the dielectric layer, or the semiconductor substrate. In one aspect, for example, semiconductor layer or the semiconductor substrate is doped with

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a dopant to form an electrical back surface field, where the EBSF is distinct from the textured region.

In another aspect, the band structure optimization can be realized by forming a heterojunction along a modified semiconductor interface. For example, a layer of amorphous silicon can be deposited on the textured region interface, thus forming a heterojunction that bends the minority carrier band towards the desired energy direction.

The dielectric layer can be made from a variety of materials, and such materials can vary depending on the device design and desired characteristics. One use for such a layer involves the coupling of the semiconductor layer to the semiconductor substrate. In some cases, wafer bonding can be used as a coupling technique. The dielectric layer can thus facilitate the attachment of these materials together, as has been described. The dielectric layer can be associated with the semiconductor layer, the semiconductor substrate, or both the semiconductor layer and the semiconductor substrate prior to bonding. In those aspects having a dielectric layer associated with both materials, the dielectric layers can be bonded directly together, or in some cases, bonded together with an intervening textured region. Additionally, in some aspects a textured region can be formed on one or more dielectric layers. In some aspects, a dielectric layer can be bonded to a semiconductor material such as, for example, polysilicon. In other aspects, the semiconductor layer and the semiconductor substrate can be bonded together without an intervening dielectric layer.

Non-limiting examples of dielectric layer materials can include oxides, nitrides, oxynitrides, and the like, including combinations thereof. In one specific aspect, the dielectric layer includes an oxide. In another aspect, the dielectric layer includes a buried oxide. Additionally, the dielectric layer can be of various thicknesses. In one aspect, for example, the dielectric layer has a thickness of from about 100 nm to about 4 microns. In another aspect, the dielectric layer has a thickness of from about 500 nm to about 2 microns. In yet another aspect, the dielectric layer has a thickness of from about 500 nm to about 1000 microns.

The devices according to aspects of the present disclosure can additionally include one or more reflecting regions. In one aspect, as is shown in FIG. 3, a photosensitive semiconductor device 30 can include a semiconductor substrate 32 and a semiconductor layer 34 coupled to the semiconductor substrate. The device also

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includes at least one textured region 36 located or coupled between the semiconductor substrate and the semiconductor layer, and at least one dielectric layer 38 coupled between the semiconductor substrate and the semiconductor layer. A reflecting region 39 is coupled to the semiconductor substrate, and positioned to interact with electromagnetic radiation. The reflecting region can be separated from the textured region by a dielectric layer as is shown, or the reflecting region can be associated directly with the textured region without an intervening dielectric layer. The reflecting region can be deposited over the entire interface between the semiconductor substrate and the next adjacent layer, or only over a portion of the interface. In some aspects, the reflecting region can be deposited over a larger area of the device compared to the textured region. The reflecting region can be positioned to reflect electromagnetic radiation that has passed through the texture region back through the textured region toward the semiconductor layer. In other words, as electromagnetic radiation passes through the semiconductor layer, a portion that is not absorbed contacts the textured region. Of that portion that contacts the textured region, a smaller portion may pass though the textured region to strike the reflecting region and be reflected back through the textured region toward the semiconductor layer.

A variety of reflective materials can be utilized in constructing the reflecting region, and any such material capable of incorporation into a photosensitive device is considered to be within the present scope. Non-limiting examples of such materials include a Bragg reflector, a metal reflector, a metal reflector over a dielectric material, a transparent conductive oxide such as zinc oxide, indium oxide, or tin oxide, and the like, including combinations thereof. Non-limiting examples of metal reflector materials can include silver, aluminum, gold, platinum, reflective metal nitrides, reflective metal oxides, and the like, including combinations thereof. In one aspect, a dielectric material can be coupled to the reflecting region along the side facing the textured region. In one specific aspect, the dielectric material can include an oxide layer and the reflecting region can include a metal layer. The surface of the metal layer on an oxide acts as a mirror-like reflector for the incident electromagnetic radiation from the backside.

Additionally, the textured surface of a metal on a roughened oxide can act as a diffusive scattering site for the incident electromagnetic radiation and also as a mirror-like reflector. Other aspects can utilize porous materials for the texturing. Porous polysilicon, for example, can be oxidized or oxide deposited and a reflective region

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such as a metal reflector can be associated therewith to provide a scattering and reflecting surface. In another aspect, aluminum can be subjected to anodic oxidation to provide porous aluminum oxide, a high dielectric constant insulator. This insulator can be coated with aluminum or other metals to provide a scattering and reflecting surface.

In one specific aspect, a reflective region can include a transparent conductive oxide, an oxide, and a metal layer. The transparent oxide can be textured and a metal reflector deposited thereupon. The textured surface of the metal on a roughened transparent conductive oxide can act as a diffusive scattering site for the incident electromagnetic radiation.

In another specific aspect, a Bragg reflector can be utilized as a reflective region. A Bragg reflector is a structure formed from multiple layers of alternating materials with varying refractive indexes, or by a periodic variation of some characteristic (e.g. height) of a dielectric waveguide, resulting in periodic variation in the effective refractive index in the guide. Each layer boundary causes a partial reflection of an optical wave. For waves whose wavelength is close to four times the optical thickness of the layers, the many reflections combine with constructive interference, and the layers act as a high-quality reflector. Thus the coherent super-positioning of reflected and transmitted light from multiple interfaces in the structure interfere so as to provide the desired reflective, transmissive, and absorptive behavior. In one aspect, the Bragg reflector layers can be alternating layers of silicon dioxide and silicon. Because of the high refractive index difference between silicon and silicon dioxide, and the thickness of these layers, this structure can be fairly low loss even in regions where bulk silicon absorbs appreciably. Additionally, because of the large refractive index difference, the optical thickness of the entire layer set can be thinner, resulting in a broader-band behavior and fewer fabrications steps.

Additional scattering can be provided by positioning a textured forward scattering layer on the side of the device that receives incident electromagnetic radiation. These forward scattering layers can be, without limitation, textured oxides or polysilicon without a reflector.

In another aspect, as is shown in FIG. 4, a photosensitive semiconductor device 40 can also include a polysilicon layer 42 disposes between multiple dielectric layers 38. It should be noted that all reference numbers in FIG. 4 that have been reused from previous figures denote the same or similar materials and/or structures

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whether or not further description is provided. The addition of the polysilicon layer can provide various improvements in manufacturing in some cases. For example, a rough surface of a textured region can be challenging to wafer bond. By depositing a thin dielectric layer followed by a thick polysilicon layer it can be possible to create a surface that can be polished. Thus, the polysilicon layer can be planarized and polished until smooth, and the resulting surface can be wafer bonded to the dielectric layer on the opposing material, e.g. the semiconductor substrate if the polysilicon is deposited on the semiconductor layer structure. It is also contemplated that such a process can be performed with only one dielectric layer or even without any dielectric layers being present. In another aspect, the polysilicon layer can be doped with a dopant. In yet another aspect, the polysilicon layer can be a monosilicon layer. In one specific aspect, the polysilicon layer is a monosilicon layer and the semiconductor layer is an epitaxial layer that has been etched from the backside to form the textured region.

In another aspect, as is shown in FIG. 5, a photodiode 50 having enhanced light detection performance is provided. The photodiode includes contacts 52 and a photodiode junction 54 formed on the semiconductor layer 34. In another aspect, as is shown in FIG. 6, a CMOS image sensor having improved light detection performance is provided. The CMOS image sensor includes photodiode junctions 64 and circuitry 62 formed on the semiconductor layer 34. It should be noted that all reference numbers in FIGs. 5 and 6 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. In this way, the textured region 36 can be introduced into fabrication process at the start of the flow, at a lower cost and lower technical risk approach. Because the textured region is buried within the semiconductor materials at an early stage in the flow, the textured region can be protected from contamination during the further fabrication of the device. Additionally, potentially proprietary details such as the specific architecture of the texture region can be protected from view during the later stages of fabrication. This method could further include a step of removing the semiconductor substrate. It is understood that once the semiconductor device is formed the semiconductor substrate may no longer be necessary in some cases. In this way the semiconductor device can be mounted on various substrates as necessary for specific applications.

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In one aspect, isolation features can be utilized in order to isolate various portions of the device from one another. For example, in one aspect a semiconductor device can include a plurality of isolation features in at least the semiconductor layer that function to isolate each photodetector in an array of photodetectors from one another. The isolation features isolate each photodetector electrically, optically, or both electrically and optically. Isolation features can thus maintain uniformity across an array by reducing optical and electrical crosstalk between the photodetectors. FIG. 7 shows a semiconductor device 70 having an array of photodetectors 72. It should be noted that all reference numbers in FIG. 7 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. The photodetectors are separated by a plurality of isolation features, in this case extending through the semiconductor layer 34 and the textured region 36. In one aspect, the isolation features extend through the semiconductor layer but not through the textured region. In another aspect, the isolation features extend beyond the textured region and into the dielectric layer or even into the semiconductor substrate. In some aspects, other structures such as polysilicon layers and reflective regions can contain isolation features. Accordingly, the isolation features can be deep or shallow, depending on the desired configuration of the device.

Isolation features can be made from various materials, including, without limitation, dielectric materials, reflective materials, conductive materials, light diffusing features, voids, and the like, including combinations thereof. Conductive materials used to fill the isolation feature etches or voids can be passivated in order to maintain electrical isolation. In other aspects, conductive materials can be utilized as vias. The isolation can be fabricated at the substrate level prior to fabrication of circuitry, the detector device, or the imaging array. In one aspect, voids can be created and either left as voids or filled with such materials to form the isolation features. For example, a layer surface can be photolithographically patterned and vertically etched to a desired depth (e.g. from the device surface of the semiconductor layer to the dielectric layer). Dielectric material can then be deposited conformally on surfaces within the etch until filled with the dielectric or other material. Any dielectric material remaining on the device surface of the semiconductor layer can be removed by chemical etching and/or mechanical polishing. As has been described, the isolation feature does not need to fully bisect the semiconductor structure, but

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rather only a portion can be isolated; this is known as shallow trench isolation as opposed to deep trench isolation.

Additionally, isolation features regions can be configured to reflect incident electromagnetic radiation until it is absorbed, thereby increase the effective absorption length of the device. In other aspects, the sides of isolation features can be doped. In some aspects, a doped isolation feature can form an electrical surface field, similar to an electrical back surface field as has been described. The isolation features can be formed before or after bonding of the semiconductor substrate to the semiconductor layer. Furthermore, the isolation features can be formed from either side of the semiconductor layer or from either side of the semiconductor substrate, depending on the depth and extent of the features.

In some aspects, the textured region can be arranged in a discontinuous pattern. As is shown in FIG. 8, for example, a semiconductor device 80 can have a discontinuous textured region 82. It should be noted that all reference numbers in FIG. 8 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided. Such a discontinuous pattern may correspond to structures elsewhere in the device, such as the spatial pattern of an array of photodetectors on the device surface (not shown).

In other aspects, one or more cavities can be disposed in the semiconductor device and associated with the textured region or regions. As is shown in FIG. 9, for example, a semiconductor device 90 can include a cavity region 92 associated with the textured region 36. The cavity region can enhance the functionality of the textured region, and can be particularly effective when optically coupled to a reflective region, whether the reflective region is on the near side or the far side of the dielectric layer 38. FIG. 10 shows a semiconductor device 100 having a plurality of cavity regions 102 arranged in a discontinuous pattern to correspond with the discontinuous pattern of the textured region 82. The cavity regions shown in FIGs. 9 and 10 can be formed prior to wafer bonding or following wafer bonding. If a cavity region is formed following wafer bonding, etching through the semiconductor substrate 32 may be required, following which the etch cavity can be partially filled. Additionally, a cavity region can be formed before or after formation of the textured region. In those aspects whereby a cavity region is formed after formation of the textured region, the intervening material would be etched until reaching the textured region. In those aspects whereby a cavity region is formed prior to formation of the

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textured region, an etch can be formed into the semiconductor layer 34 and the textured region can be formed thereon through the etch cavity. The formation of the textured region in this manner can be accomplished prior to wafer bonding or following wafer bonding by etching through the semiconductor substrate. It should be noted that all reference numbers in FIGs. 9 and 10 that have been reused from previous figures denote the same or similar materials and/or structures whether or not further description is provided.

The present disclosure additionally provides various methods. In one aspect, as is shown in FIG. 14, for example, a method of making a semiconductor device can include texturing at least a portion of a surface of a semiconductor layer to form a textured region 142, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer 144, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate 146. In another aspect, the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

In another aspect, a method of making a semiconductor device can include laser texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In yet another aspect, a method of making a semiconductor device can include wet etch texturing at least a portion of a surface of a semiconductor layer to form a textured region, depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer, and wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

In one specific aspect, FIGs. 11A-C show one method of manufacturing a semiconductor device. As is shown in FIG. 11A, a semiconductor material 114 can be textured to create a textured region 112, and a dielectric layer 115 can be deposited over the textured region. In one aspect, the textured region can be formed by laser processing the semiconductor material. In another aspect, the textured region can be formed by wet etching the semiconductor material. The dielectric layer can then be

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polished until smooth with a process such as CMP processing. The resulting structure can then be wafer bonded to a semiconductor substrate 116, as is shown rotated 180° in FIG. 11B, with the polished surface of the dielectric layer being bonded to the semiconductor substrate. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). After wafer bonding, the semiconductor material can be polished to a specified thickness. In another aspect, an epitaxially grown semiconductor layer 118 can be grown on the polished surface of the semiconductor material to generate a low defect device region as shown in FIG. 11C.

In another aspect, FIGs. 12A-C show another method of manufacturing a semiconductor device. As is shown in FIG. 12A, a semiconductor material 124 can be textured to create a textured region 122, and a dielectric layer 125 can be deposited over the textured region. In one aspect, the semiconductor material can be an epitaxially grown semiconductor material. The dielectric layer can then be polished and a polysilicon layer 126 can be deposited thereupon, as is shown in FIG. 12B. In an alternative aspect, the polysilicon layer can be formed directly on the textured region without an intervening dielectric layer (not shown). The polysilicon layer can then be polished and wafer bonded to a semiconductor substrate 126, as is shown rotated 180° in FIG. 12C. The polysilicon layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer 129 formed on the semiconductor substrate. After wafer bonding, the semiconductor material can be polished to a specified thickness.

In another aspect, FIGs. 13A-D show another method of manufacturing a semiconductor device. As is shown in FIG. 13A, a semiconductor layer 134 can be epitaxially grown on a temporary semiconductor support 139. The epitaxially grown semiconductor layer is textured to create a textured region 132, and a dielectric layer 135 is deposited over the textured region as is shown in FIG. 13B. Following polishing, the dielectric layer is wafer bonded to a semiconductor substrate 136, as is shown rotated 180° in FIG. 13C. The dielectric layer can be bonded directly to the semiconductor substrate, or to a second dielectric layer formed on the semiconductor substrate (not shown). The temporary semiconductor support can then be removed from the epitaxially grown semiconductor layer. This can be accomplished by any known process, such as wafer splitting, CMP processing, etc. The exposed epitaxial semiconductor layer can be further polished and thinned to produce a desired surface

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for further device deposition. In this manner semiconductor materials used to grow the epitaxial layer can be removed, leaving a higher quality surface with fewer crystal defects and dislocations.

Of course, it is to be understood that the above-described arrangements are only illustrative of the application of the principles of the present disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the present disclosure and the appended claims are intended to cover such modifications and arrangements. Thus, while the present disclosure has been described above with particularity and detail in connection with what is presently deemed to be the most practical embodiments of the disclosure, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

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CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

a semiconductor layer coupled to the semiconductor substrate, the semiconductor layer having a device surface opposite the semiconductor substrate; and

at least one textured region coupled between the semiconductor substrate and the semiconductor layer.

2. The device of claim 1, further comprising at least one dielectric layer coupled between the semiconductor substrate and the semiconductor layer.

3. The device of claim 2, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

4. The device of claim 2, wherein the semiconductor layer is a silicon layer.

5. The device of claim 2, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

6. The device of claim 2, wherein the dielectric layer is coupled between the semiconductor substrate and the textured region, and wherein the textured region is disposed between the dielectric layer and the semiconductor layer.

7. The device of claim 6, further comprising a reflective region disposed between the semiconductor substrate and the textured region.

8. The device of claim 6, wherein the textured region is coupled directly to the semiconductor layer.

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9. The device of claim 6, further comprising a secondary semiconductor layer disposed between the textured region and the semiconductor layer.

10. The device of claim 6, further comprising at least one cavity region disposed between the textured region and the dielectric layer.

11. The device of claim 2, further comprising a polysilicon layer directly coupled to the dielectric layer.

12. The device of claim 11, wherein the polysilicon layer is disposed between multiple dielectric layers.

13. The device of claim 2, wherein the textured region is disposed between the semiconductor substrate and the dielectric layer, and wherein the dielectric layer is disposed between the textured region and the semiconductor layer.

14. The device of claim 2, wherein the textured region is doped with a dopant to form an electrical back surface field.

15. The device of claim 14, wherein the electrical back surface field has been doped by a technique selected from the group consisting of laser doping, ion implanting, diffusion doping, in situ doping, and combinations thereof.

16. The device of claim 15, wherein the textured region has a higher dopant concentration than the semiconductor layer.

17. The device of claim 15, wherein the dopant has the same polarity as the semiconductor layer.

18. The device of claim 15, wherein the dopant is a member selected from the group consisting of boron, indium, gallium, arsenic, antimony, phosphorus, and combinations thereof.

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19. The device of claim 2, wherein the semiconductor layer is doped with a dopant to form an electrical back surface field, and wherein the electrical back surface field is distinct from the textured region.

20. The device of claim 2, further comprising at least one photodiode optically active region disposed on the device surface.

21. The device of claim 2, wherein the photodiode optically active region comprises a doped region.

22. The device of claim 2, wherein the device forms at least one photodetector.

23. The device of claim 22, wherein the at least one photodetector is a plurality of photodetectors arranged in an array.

24. The device of claim 23, wherein the textured region is arranged in a discontinuous pattern that corresponds spatially to the array of photodetectors.

25. The device of claim 23, further comprising a plurality of isolation features in at least the semiconductor layer to isolate each photodetector in the array of photodetectors, wherein the isolation features isolate each photodetector electrically, optically, or both electrically and optically.

26. The device of claim 23, further comprising at least one optical lens associated with the at least one photodetector.

27. The device of claim 23, further comprising at least one color filter associated with the at least one photodetector.

28. A method of making a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric

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layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate.

29. The method of claim 28, wherein the semiconductor layer is an epitaxially grown semiconductor layer.

30. The method of claim 29, wherein texturing at least a portion of a surface of a semiconductor layer to form a textured region further includes:

forming the epitaxially grown semiconductor layer on a growth substrate; and

texturing at least a portion of a surface of the epitaxially grown semiconductor layer to form a textured region.

31. The method of claim 30, further comprising removing the growth substrate to expose the epitaxially grown semiconductor layer.

32. The method of claim 28, further comprising forming an epitaxially grown semiconductor layer on the semiconductor layer on an opposite side from the textured region.

33. The method of claim 28, wherein wafer bonding further includes:

depositing a polysilicon layer on the first dielectric layer; and

bonding the polysilicon layer between the first dielectric layer and the second dielectric layer.

34. The method of claim 33, further comprising doping at least a portion of the polysilicon layer.

35. The method of claim 28, wherein texturing at least a portion of a surface of the semiconductor layer to form the textured region further includes:

forming an opening in the semiconductor substrate, the second dielectric layer, and the first dielectric layer to expose a portion of the semiconductor layer; and

texturing at least a portion of the exposed portion of the semiconductor layer to form the textured region.

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36. The method of claim 28, wherein texturing includes a technique selected from the group consisting of plasma etching, reactive ion etching, porous silicon etching, lasing, chemical etching, nanoimprinting, material deposition, selective epitaxial growth, and combinations thereof.

37. The method of claim 28, wherein texturing includes lasing.

38. A method of protecting a textured region from contamination during manufacture of a semiconductor device, comprising:

texturing at least a portion of a surface of a semiconductor layer to form a textured region;

depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the dielectric layer; and

wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate, wherein the textured region is protected from contamination during further manufacturing processes by the semiconductor layer and the semiconductor substrate.

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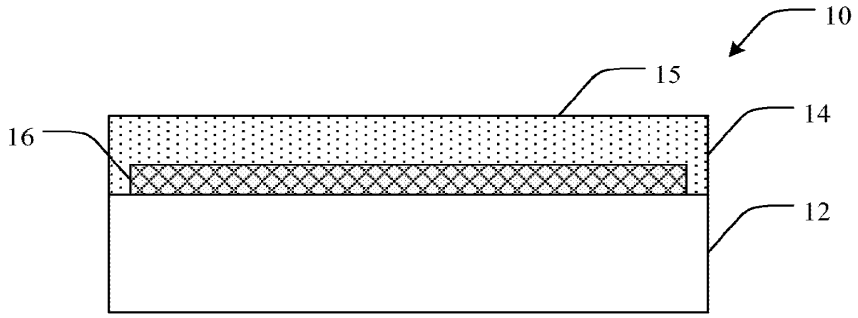


FIG. 1

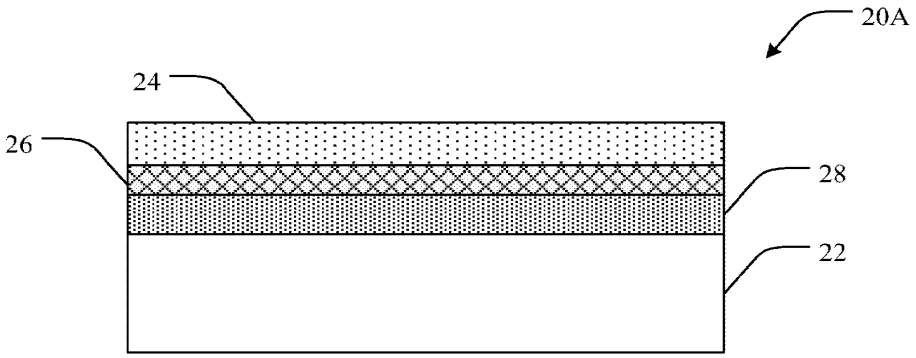


FIG. 2A

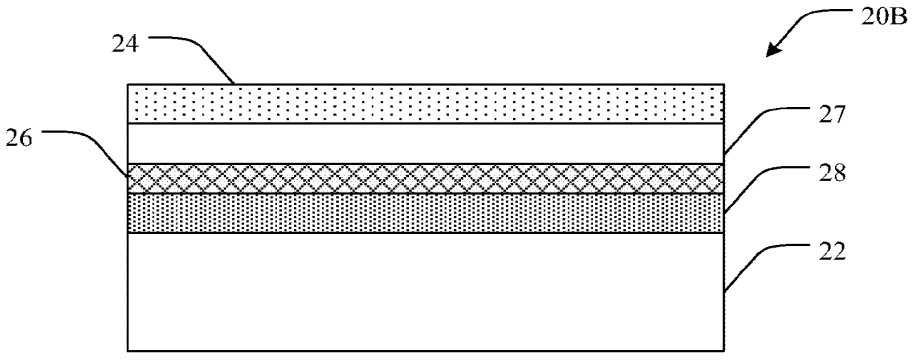


FIG. 2B

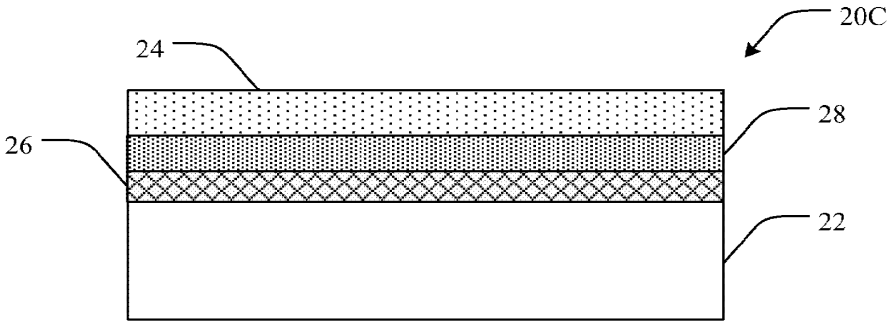


FIG. 2C

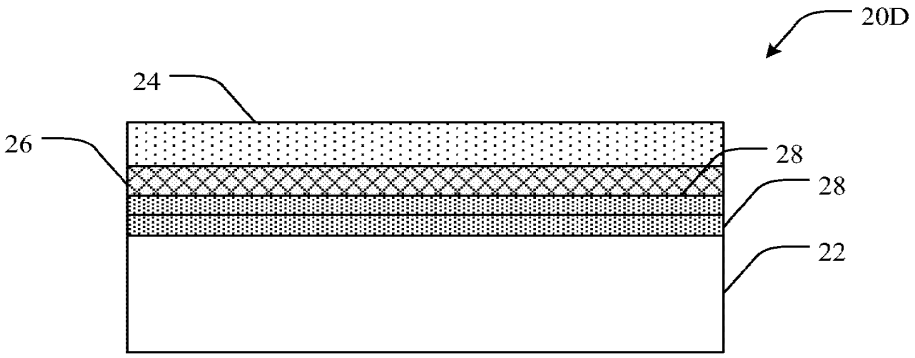


FIG. 2D

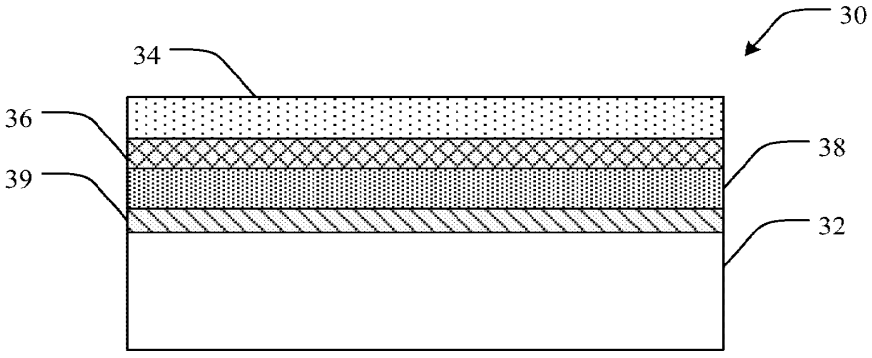


FIG. 3

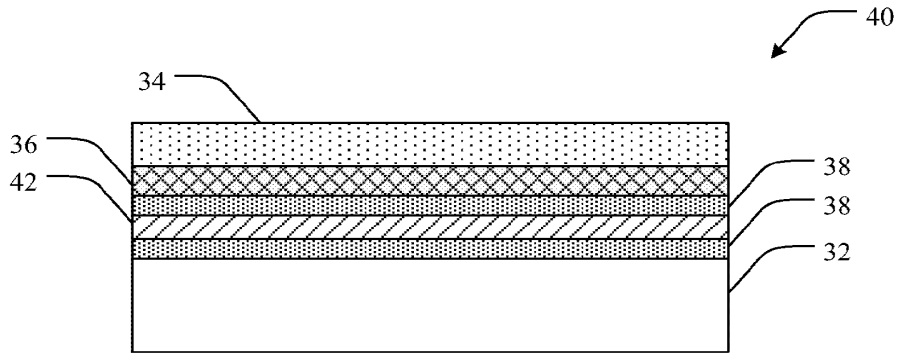


FIG. 4

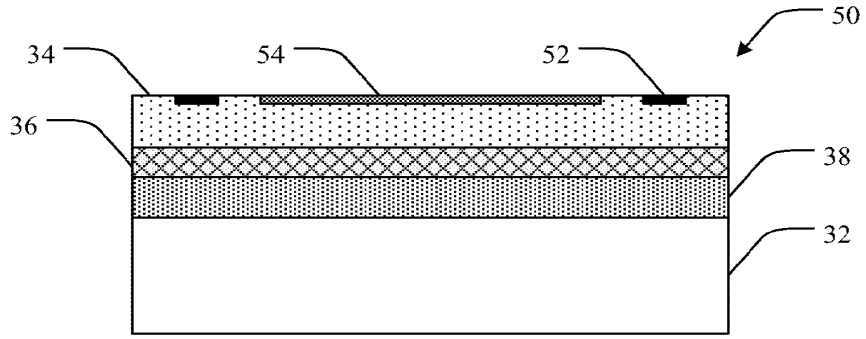


FIG. 5

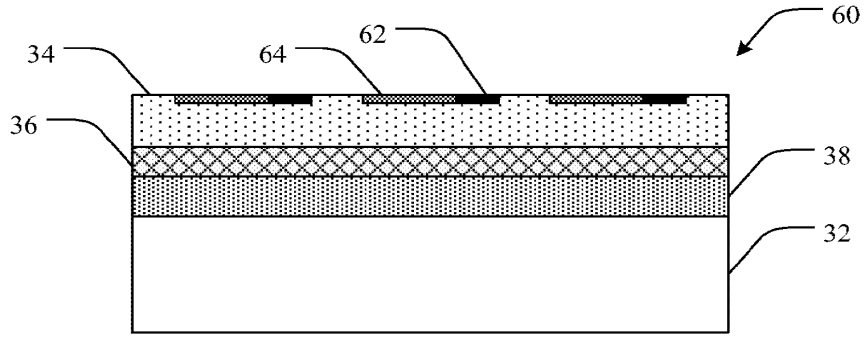


FIG. 6

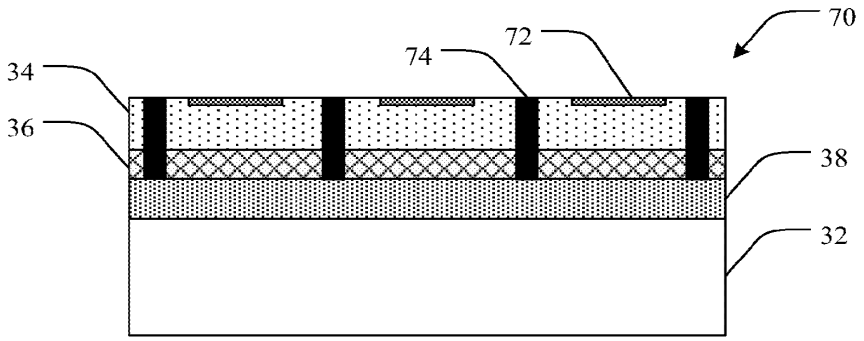


FIG. 7

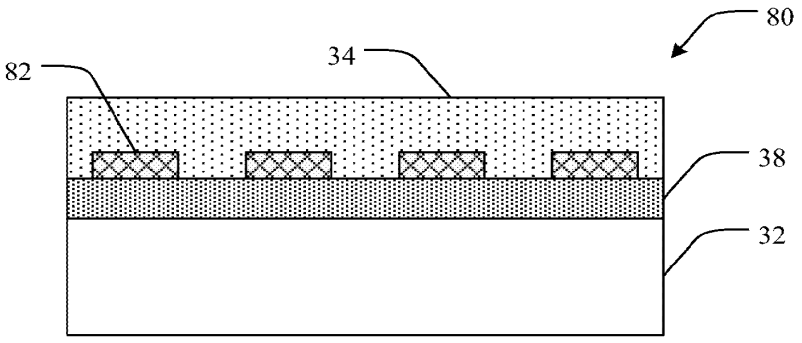


FIG. 8

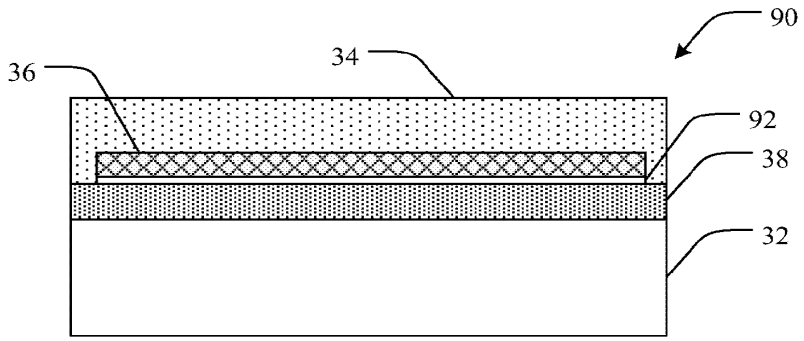


FIG. 9

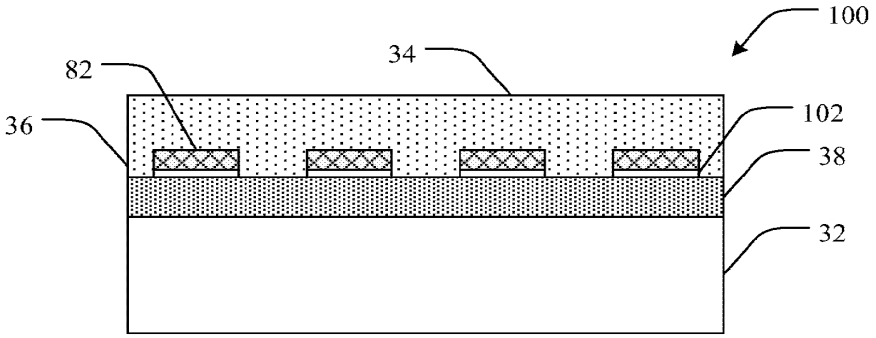


FIG. 10

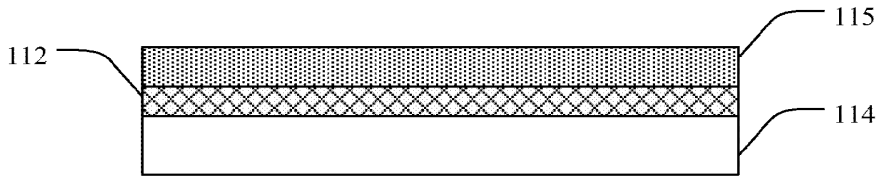


FIG. 11A

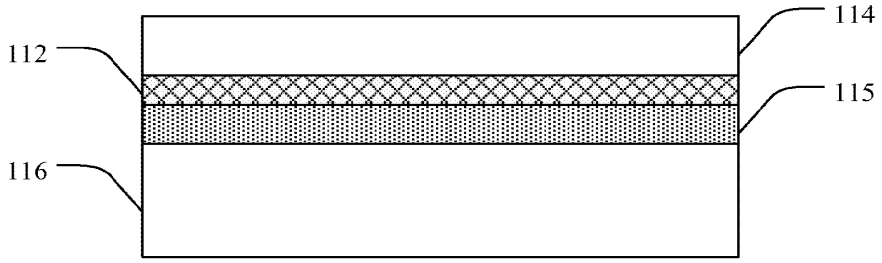


FIG. 11B

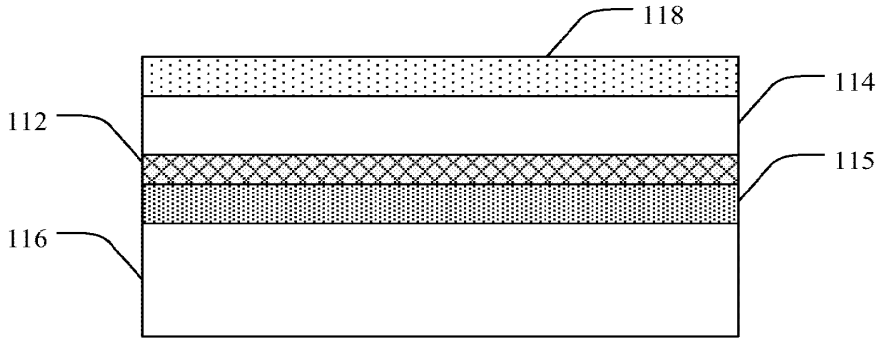


FIG. 11C

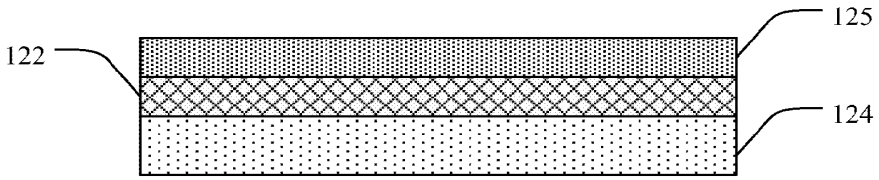


FIG. 12A

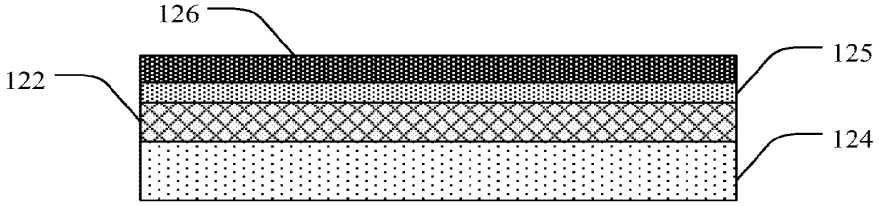


FIG. 12B

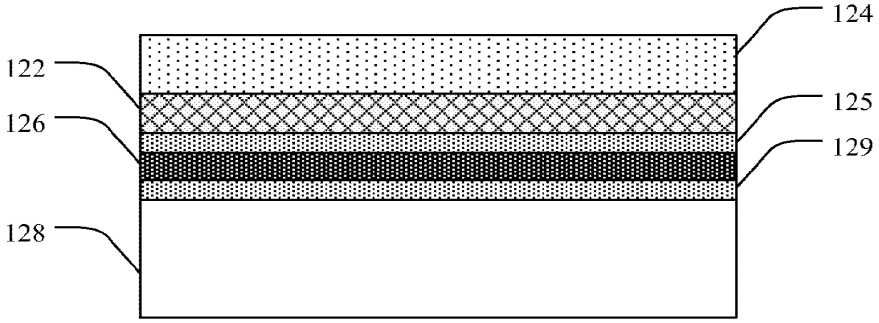


FIG. 12C

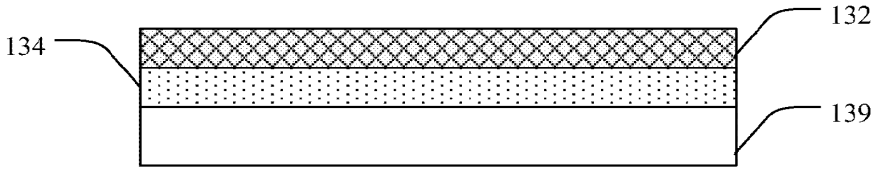


FIG. 13A

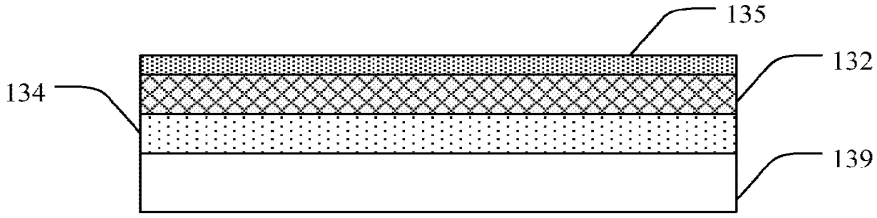


FIG. 13B

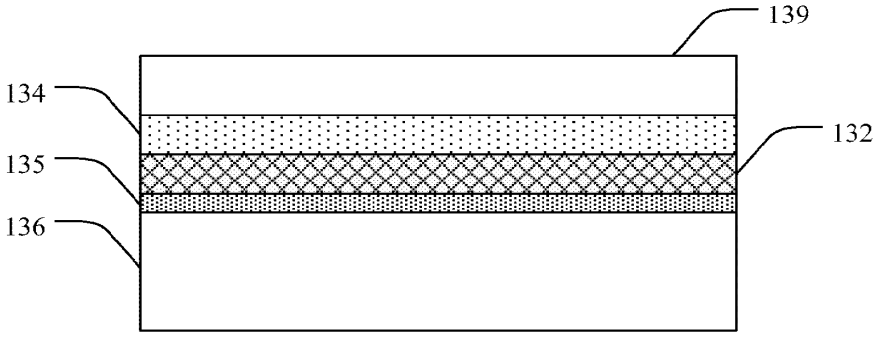


FIG. 13C

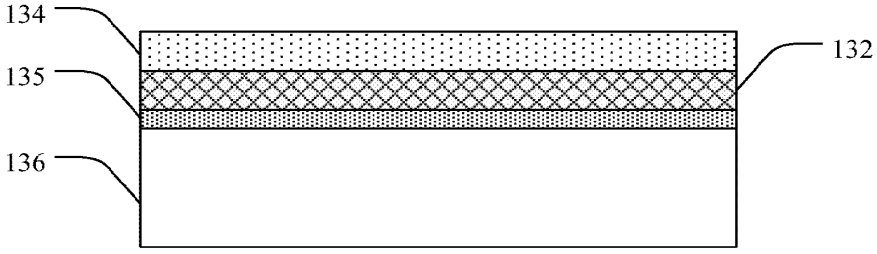


FIG. 13D

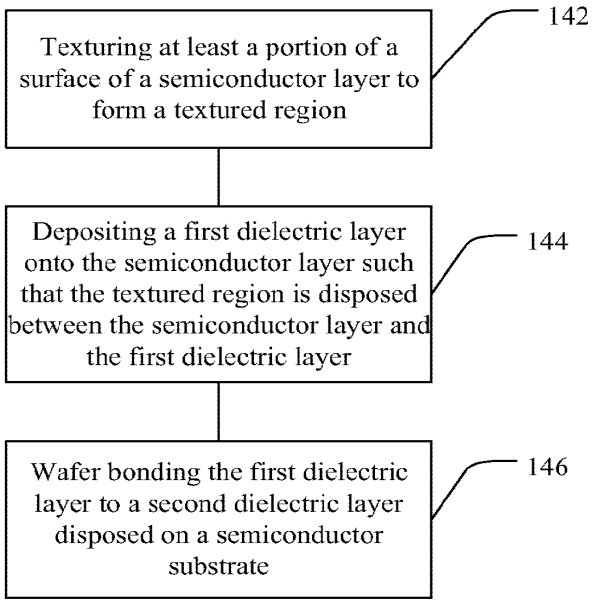

Texturing at least a portion of a surface of a semiconductor layer to form a textured region
142
Depositing a first dielectric layer onto the semiconductor layer such that the textured region is disposed between the semiconductor layer and the first dielectric layer
144
Wafer bonding the first dielectric layer to a second dielectric layer disposed on a semiconductor substrate
146

FIG. 14

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
ALDER TODD B.

P.O. BOX 1219 SANDY UT 84091-1219 USA

RECEIVED
AUG - 6 2013
THORPE NORTH & WESTERN

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	25 July 2013 (25.07.2013)
Applicant's or agent's file reference 3035-052-PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2013/033554**	International filing date *(day/month/year)* **22 March 2013 (22.03.2013)**
Applicant **SIONYX, INC.**	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 . 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea	Authorized officer COMMISSIONER
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8755

Form PCT/ISA/220 (July 2010)

DOCKETED

Description	Due Date	Initials
modify Abstract	8-25-13	
Article 19	9-25-13	
Chpt II Demand	1-22-14	
052.NP IDS	10-25-13	

INITIAL

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **NQY3E39H**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com

Email: ipkc@ipkcenter.com

Notes to Form PCT/ISA/220 (July 2010)

DOCKETED
AUG - 8 2013
TNW

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 3035-052-PCT	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/US2013/033554**	International filing date *(day/month/year)* **22 March 2013 (22.03.2013)**	(Earliest) Priority Date *(day/month/year)* 22 March 2012 (22.03.2012)
Applicant **SIONYX, INC.**		

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 4
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

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Apple-Sony EX1002 Page 357

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/033554

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/146(2006.01)i, H01L 27/148(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/146; H01L 31/101; H01L 31/0236; H01L 31/18; H01L 31/052; H01L 27/14; H01L 31/0232; H01L 31/00; H01L 27/148

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: image sensor, pixel, isolation, reflect, backside, trench

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6498336 B1 (HUI TIAN et al.) 24 December 2002 See abstract, column 2, lines 55-58, column 3, line 3, column 4, lines 40-42, 51-52, 58-59, claims 1,6 and figures 2-3.	1,12-13,19-23
Y		2-11,14-18,24-26
A		27-33
Y	US 2008-0036022 A1 (SUNG-HO HWANG et al.) 14 February 2008 See paragraphs [0014], [0037], [0056], [0063], [0082], claim 1 and figures 3-4.	2-11,14-18,24-26
A		1,12-13,19-23 ,27-33
A	JP 2011-091128 A (CANON INC.) 06 May 2011 See abstract, claim 1 and figures 1-2.	1-33
A	US 2011-0140221 A1 (VENEZIA VINCENT et al.) 16 June 2011 See abstract, claim 1 and figures 6A-6G.	1-33
A	WO 2011-119618 A2 (SIONYX, INC. et al.) 29 September 2011 See abstract and figures 8-10.	1-33

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 July 2013 (24.07.2013)	**25 July 2013 (25.07.2013)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	OH Eung Gie Telephone No. +82-42-481-8744

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/033554

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6498336 B1	24/12/2002	None	
US 2008-0036022 A1	14/02/2008	KR 10-0745991 B1	06/08/2007
JP 2011-091128 A	06/05/2011	US 2011-0090384 A1	21/04/2011
		US 8330847 B2	11/12/2012
US 2011-0140221 A1	16/06/2011	EP 1916714 A1	30/04/2008
		EP 1916714 B1	25/07/2012
		US 2008-0099804 A1	01/05/2008
		US 7888159 B2	15/02/2011
		US 8338900 B2	25/12/2012
WO 2011-119618 A2	29/09/2011	EP 2550683 A2	30/01/2013
		US 2012-068289 A1	22/03/2012

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PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
ALDER TODD B.

P.O. BOX 1219 SANDY UT 84091-1219 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**25 July 2013 (25.07.2013)**
Applicant's or agent's file reference: 3035-052-PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2013/033554	**22 March 2013 (22.03.2013)**	22 March 2012 (22.03.2012)

International Patent Classification (IPC) or both national classification and IPC
H01L 27/146(2006.01)i, H01L 27/148(2006.01)i

Applicant
SIONYX, INC.

DOCKETED
Description Due Date Initials
Response 1.22-14 JL

1. This opinion contains indications relating to the following items:

WJB/A INITIAL

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	24 July 2013 (24.07.2013)	OH Eung Gie Telephone No. +82-42-481-8744

Form PCT/ISA/237 (cover sheet) (July 2011)

DOCKETED AUG - 8 2013 TNW

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/033554

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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Apple-Sony EX1002 Page 361

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2013/033554

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-33	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	27-33	YES
	Claims	1-26	NO
Industrial applicability (IA)	Claims	1-33	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 6498336 B1 (HUI TIAN et al.) 24 December 2002
D2: US 2008-0036022 A1 (SUNG-HO HWANG et al.) 14 February 2008
D3: JP 2011-091128 A (CANON INC.) 06 May 2011
D4: US 2011-0140221 A1 (VENEZIA VINCENT et al.) 16 June 2011
D5: WO 2011-119618 A2 (SIONYX, INC. et al.) 29 September 2011

1 Novelty and Inventive Step

1.1. Concerning Claims 1-23

1.1.1 Independent Claims 1 and 23

D1, which is considered to be the closest prior art to the subject matter of claim 1, discloses a light sensor comprising: an incident light absorbed within the light-sensing element (see claim 1), a light-reflecting element positioned in relation to the light-sensing element back towards the light-sensing element (see claim 1), light-reflecting vertical via structures (322) (see column 4, lines 51-52) and light that passes through the light-sensing element and is reflected back towards the light-sensing element (see column 2, lines 55-58). Claim 1 differs from D1 in a backside light trapping material and a peripheral light trapping material. However, said differences are virtually suggested by D1 considering the various light-reflecting regions (314) (see column 4, lines 58-59). Accordingly, a person skilled in the art would easily conceive the idea of employing the feature. Therefore, claim 1 lacks an inventive step under PCT Article 33(3).

Claim 23 relates to an array of light trapping device of claim 1 and has the same technical features as claim 1 except the number of device. Thus, the same reasoning as in claim 1 could be applied to claim 23. Therefore, claim 23 lacks an inventive step under PCT Article 33(3).

1.1.2 Dependent Claims 2-22

The additional features of claims 2-3, dependent on claim 1, are disclosed in D1 in that each light-reflecting region (314) formed within substrate (306) is made of a suitable material (see column 4, lines 40-41). Claims 2-3 differ from D1 in that the peripheral

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Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of: Box No. V

light trapping material includes a high refractive index material sandwiched between two low refractive index materials. However, the difference can be easily derived from D2 in each having a laminated structure of a first refractive film (191a) and a second refractive film (192a) (see paragraph [0056]). As the art of D1 and D2 is the same, the technical feature of D1 and D2 can be easily combined. Accordingly, claims 2-3 would have been obvious over D1 in view of D2.

The additional feature of claim 4, dependent on claim 3, is merely a variation of the disclosure of the cited document and a person skilled in the art would arrive at the claimed invention by general experimentation alone without exercising any ingenuity in D1.

The additional feature of claims 5-6, dependent on claim 4, is merely a matter of design option in that each light-reflecting region (314) is made of a suitable material, such as a silicon oxide, a silicon oxynitride, or a silicon nitride in D1 (see column 4, lines 40-42).

The additional feature of claim 7, dependent on claim 3, is merely a matter of design option in view of D1 when the general knowledge in relevant field of the art is used. Hence, no inventive step is present in the subject matter of claim 7.

The additional feature of claim 8, dependent on claim 7, is merely a matter of design option in view of D1 when the general knowledge in relevant field of the art is used. Hence, no inventive step is present in the subject matter of claim 8.

The additional feature of claim 9, dependent on claim 2, is disclosed in D2 in that the photoelectric converter (110) may be a photodiode, a phototransistor, a photogate, a pinned photodiode (PPD) or a combination thereof (see paragraph [0037]). As the art of D1 and D2 is the same, the technical feature of D1 and D2 can be easily combined. Accordingly, claim 9 would have been obvious D1 in view of D2.

The additional feature of claim 10, dependent on claim 9, is merely a matter of design option in view of D2 when the general knowledge in relevant field of the art is used. Accordingly, claim 9 would have been obvious D1 in view of D2.

The additional feature of claim 11, dependent on claim 1, is disclosed in D1 in that each light-reflecting region (314) formed within substrate (306) is made of a suitable material (see column 4, lines 40-41). Claim 11 differs from D1 in that the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials and the difference is refractive index between the first material and the two second materials is at least 0.2. However, D2 discloses each having a laminated structure of a first refractive film (191a) and a second refractive film (192a) (see paragraph [0056]), and the difference of refractive index is merely a matter of design option in view of D2 when the general knowledge in relevant field of the art in used. Hence, no inventive step is present in the subject matter of claim 11. As the art of D1 and D2 is the same, the technical feature of D1 and D2 can be easily combined. Accordingly, claim 11 would have been obvious D1 in view of D2.

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Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
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The additional features of claims 12-13, dependent on claim 1, are merely variations of an light-reflecting vertical via structures (322) in D1 (see column 4, lines 51-52).

The additional feature of claim 14, dependent on claim 1, is merely a matter of design option forming a reflecting film on one surface of the substrate in D2 (paragraph [0014]). Accordingly, claim 14 would have been obvious D1 in view of D2.

The additional feature of claim 15, dependent on claim 14, is merely a matter of design option of the planarizing film in D2 (paragraph [0082]). Accordingly, claim 15 would have been obvious D1 in view of D2.

Claim 16, dependent on claim 14, differs from D1 in a reflective layer having an aperture. However, the difference is virtually suggested by D2 considering a reduced aperture ratio (see paragraph [0063]). Therefore, a person skilled in the art would easily conceive the idea of employing the feature of aperture. Accordingly, claim 16 would have been obvious D1 in view of D2.

The additional feature of claim 17, dependent on claim 16, is merely a variation of microlenses in D2 (see claim 1). Accordingly, claim 17 would have been obvious D1 in view of D2.

The additional feature of claim 18, dependent on claim 16, is merely matter of design option in view of D2 when the general knowledge in relevant field of the art is used. Hence, no inventive step is present in the subject matter of claim 18. Accordingly, claim 18 would have been obvious D1 in view of D2.

The additional feature of claim 19, dependent on claim 1, is disclosed in D1 in the various light-reflecting regions (314) consist of conductive layers (see column 3, line 3, column 4, lines 58-59).

The additional feature of claim 20, dependent on claim 1, is merely a matter of design option in view of D1 when the general knowledge in relevant field of the art is used.

The additional features of claims 21-22, dependent on claims 1 and 21 respectively, are merely matters of design option in view of D1 when the general knowledge in relevant field of the art is used.

Therefore, claims 2-22 lack an inventive step under PCT Article 33(3).

1.2 Concerning Claims 24-26

1.2.1 Independent Claim 24

D1, which is considered to be the closest prior art to the subject matter of claim 24, discloses a light sensor, comprising: an incident light absorbed within the light-sensing element (see claim 1), a light-reflecting element positioned in relation to the

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In case **the space in any of the preceding boxes is not sufficient.**
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light-sensing element back towards the light-sensing element (see claim 1), an light-reflecting vertical via structures (322) (see column 4, lines 51-52), the various light-reflecting regions (314) (see column 4, lines 58-59) and light that passes through the light-sensing element and is reflected back towards the light-sensing element (see column 2, lines 55-58). Claim 24 differs from D1 in frontside light trapping material covering at least a portion of the light incident surface. However, it is well known to form a reflecting film on one surface of the substrate in D2 (see paragraph [0014]). As the art of D1 and D2 is the same, the technical feature of D1 and D2 can be easily combined. Accordingly, claim 24 would have been obvious over D1 in view of D2. Therefore, claim 24 lacks an inventive step under PCT Article 33(3).

1.2.2 Dependent Claims 25-26

The additional feature of claim 25, dependent on claim 24, is not explicitly disclosed in D1. However, said feature is virtually suggested by D2 considering a reduced aperture ratio (see paragraph [0063]). Therefore, a person skilled in the art would easily conceive the idea of employing the feature of aperture. Accordingly, claim 25 would have been obvious over D1 in view of D2.

The additional feature of claim 26, dependent on claim 25, can be easily derived from D2 in that a photoresist having high light transmittance may be used as the microlens (320) (see paragraph [0085]). Accordingly, claim 26 would have been obvious over D1 in view of D2.

Therefore, claims 25-26 lack an inventive step under PCT Article 33(3).

1.3 Concerning Claims 27-33

The subject matter of claim 27 differs from these prior art documents in etching a trench circumscribing the pixel device layer and filling the trench with a peripheral light trapping material. And these features are not obvious to a person skilled in the art by the documents, taken alone or in combination. Therefore, claim 27 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

Claims 28-33 are dependent on claim 27 and therefore meet the requirements of PCT Article 33(2) and (3).

2 Industrial Applicability

Claims 1-33 are industrially applicable under PCT Article 33(4).

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Electronic Acknowledgement Receipt

EFS ID:	17283610
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/eileen fuessel
Filer Authorized By:	Todd Brent Alder
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Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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Information:					

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

ART UNIT: 2883 EXAMINER: FIRST NAMED INVENTOR: Martin U. Pralle SERIAL NO.: 13/841,120 FILED: 3/15/2013 CONF. NO.: 5133 FOR: PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS DOCKET NO.: 3035-052.NP	**CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8** DATE OF DEPOSIT: October 31, 2013 I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being submitted on the date indicated above via: ☒ EFS Web ☐ facsimile to _____ ☐ the United States Postal Service with sufficient postage as first class mail addressed to: Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. /Todd B. Alder/ Todd B. Alder, Ph.D.

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.56, 1.97 and 1.98

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Pursuant to the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, the Applicant requests consideration of this Information Disclosure Statement, which is being submitted in accordance with:

☒ 37 C.F.R. § 1.97(b)(1) or (3), within three months of the filing date of the application, or before a first office action on the merits, whichever occurs last;

☐ 37 C.F.R. § 1.97(c), after a first office action on the merits, but before a Final Office Action or a Notice of Allowance, whichever occurs first, and is accompanied by **EITHER** a statement in accordance with 37 C.F.R. § 1.97(e), **OR** the fee set forth in 37 C.F.R. § 1.17(p); or

☐ 37 C.F.R. § 1.97(d), after a Final Office Action or Notice of Allowance, whichever occurs first, but on or before payment of the issue fee, and is accompanied by **BOTH** a statement in

accordance with 37 C.F.R. § 1.97(e), **AND** the fee set forth in 37 C.F.R. § 1.17(p).

SUBMISSIONS

Please find enclosed, pursuant to 37 C.F.R. §§ 1.97 and 1.98:

☒ Form **PTO/SB/08A** and/or **PTO/SB/08B** listing the references submitted for consideration, which contains a list of all patents, publications and all other items that have come to the attention of one or more of the individuals designated in 37 C.F.R. § 1.56(c).

☒ Legible copies of the listed non-patent documents, unpublished U.S. applications and foreign documents or their relevant portions are included.

☒ All English translations of each non-English reference, if any, within the possession, custody, control or availability of anyone designated in 37 C.F.R. § 1.56(c) (see 37 C.F.R. §1.98 are included.

☐ For all listed references that are not either in the English language, or accompanied by a translation into English, a concise explanation of relevance as required under 37 C.F.R. § 1.98(a)(3) is enclosed attached to each.

Copies of references listed on the enclosed PTO/SB/08A and/or PTO/SB/08B are **not** enclosed:

☐ because, under 37 C.F.R. § 1.98.(d), they were previously cited by or submitted to the Office in application number _____, which is relied upon for an earlier filing date under 37 C.F.R. § 1.20.

☐ because they are substantially cumulative of an enclosed reference.

STATEMENT IN ACCORDANCE WITH 37 C.F.R. § 1.97(e)

☐ I hereby certify that each item contained in the information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

☐ I hereby certify that no item contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in §1.56(c) more than three months prior to the filing of the information disclosure statement.

REMARKS

While no representation is made that any of these references may be "prior art" within the meaning of that term in accordance with 37 C.F.R. §§ 102 or 103, the enclosed list of references is disclosed so as to comply with the duty of disclosure set forth in 37 C.F.R. § 1.56.

Moreover, while no representation is made that a specific search of office files or patent office records has been conducted or that no better art exists, the undersigned attorney of record believes that the references listed, together with any other references which may have been previously submitted or listed, are the closest to the claimed invention (taken in its entirety) of which the undersigned is presently aware, and no art which is closer to the claimed invention (taken in its entirety) has been knowingly withheld.

☐ Check No. ____ in the amount of $ ____(amount in § 1.17(p)) constituting the submission fee set forth in 37 C.F.R. § 1.17(p) is enclosed.

In the event that 37 C.F.R. § 1.97(c) applies and the Examiner is not satisfied that the Statement meets the requirements of 37 C.F.R. § 1.97(e), or in any other event remediable by a fee, please credit any over payment or charge any additional fees to Deposit Account No. 20-0100 of the undersigned.

Dated this 31st day of October, 2013.

Respectfully submitted,

/Todd B. Alder/

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/841,120	03/15/2013	2883	1320	3035-052.NP	33	3

CONFIRMATION NO. 5133

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OC000000066459851

Date Mailed: 02/11/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)
Martin U. Pralle, Wayland, MA;

Applicant(s)
SiOnyx, Inc., Beverly, MA

Assignment For Published Patent Application
SiOnyx, Inc., Beverly, MA

Power of Attorney: None

Domestic Priority data as claimed by applicant
This appln claims benefit of 61/614,275 03/22/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 05/17/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/841,120**

Projected Publication Date: 05/22/2014

Non-Publication Request: No

Early Publication Request: No
** **SMALL ENTITY** **

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Title

PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

Preliminary Class

385

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

NOTICE

OC000000066459852

Date Mailed: 02/11/2014

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  ALL

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/841,120

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	33 minus 20 =	* 13	x 40 =	520	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1250		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP	5133

20551 7590 03/06/2014
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
03/06/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

causse@tnw.com
patentdocket@tnw.com
rich@tnw.com

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Office Action Summary	Application No. 13/841,120	Applicant(s) PRALLE, MARTIN U.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-33* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-33* are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 27-33, drawn to a process, classified in 438.

II. Claims 1-26, drawn to a device, classified in 257.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process such as one in which the trench is formed and filled before the formation of the pixel.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the

reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

The searches for the device and process inventions are not co-extensive.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of an invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or

clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

This application contains claims directed to the following patentably distinct species: embodiment or species 1 of fig. 1, embodiment or species 2 of fig. 2, embodiment or species 3 of fig. 3, embodiment or species 4 of fig. 4, embodiment or species 5 of fig. 5, embodiment or species 6 of fig. 6, embodiment or species 7 of fig. 7. The species are independent or distinct because **the patentability or unpatentability of one species does not necessarily imply the patentability or unpatentability of another species**. In addition, these species are not obvious variants of each other based on the current record.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species, or a single grouping of patentably indistinct species, for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no independent claim appears to be generic to other independent claims.

There is a search and/or examination burden for the patentably distinct species as set forth above because at least the following reason(s)

apply: **The searches of the patentably distinct species are not co-extensive**.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a species to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected species or grouping of patentably indistinct species**, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

The election may be made with or without traverse. To preserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the election of species requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected species or grouping of patentably indistinct species.

Should applicant traverse on the ground that the species, or groupings of patentably indistinct species from which election is required, are not patentably distinct, applicant should submit evidence or identify such

evidence now of record showing them to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the species unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other species.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which depend from or otherwise require all the limitations of an allowable generic claim as provided by 37 CFR 1.141.A telephone call was made to -- on -- to request an oral election to the above restriction requirement, but did not result in an election being made.

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn,

and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	Examiner	Art Unit

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original									

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PTO/AIA/80 (07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

■ Practitioners associated with Customer Number: 20,551

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

■ The address associated with Customer Number: 20,551

OR

☐	Firm or Individual Name		
	Address		
	City	State	Zip
	Country		
	Telephone	Email	

Assignee Name and Address: SiOnyx, Inc.
100 Cummings Ctr.
Suite 243-F
Beverly, MA 01915-6506

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	12/16/2013
Name	John Zielkowski	Telephone	
Title	CFO		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Martin U. Pralle et al.

Application No./Patent No.: 13/841,120 Filed/Issue Date: 3/15/2013

Titled: Pixel Isolation Elements, Devices and Associated Methods

SiOnyx, Inc., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Todd B. Alder/	April 29, 2014
Signature	Date
Todd B. Alder, Ph.D.	54598
Printed or Typed Name	Title or Registration Number

WHEN RECORDED RETURN TO:
Todd B. Alder, Ph.D.
Thorpe North & Western, LLP
P.O. Box 1219
Sandy, UT 84091-1219

Docket No. 3035-052.NP

ASSIGNMENT

WHEREAS, we, Martin U. Pralle (resident of the State of MA, whose postal mailing address is 15 Rice Spring Lane, Wayland, MA 01778), Jeffrey McKee (resident of the State of OR, whose postal mailing address is 22850 SW Eno Pl.Tualatin, OR 97062), and Jason Sickler (resident of the State of MA, whose postal mailing address is 53 Varnum Street Arlington, MA 02474), (hereinafter "Assignors") have invented a certain new and useful improvement in a **PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS** for which an application for United States Letters Patent is being filed concurrently herewith OR which was filed on March 15, 2013 as THORPE NORTH & WESTERN, LLP Docket No. 3035-052.NP, and given U.S. Patent Application Serial No.13/841,120; (Thorpe North & Western, LLP is hereby authorized to insert the specified data, when known) and:

WHEREAS, SiOnyx, Inc., a corporation, organized and existing under the laws of the State of DE, having a business address of 100 Cummings Ctr., Suite 243-F, Beverly, MA, 01915 (hereinafter "Assignee"), is desirous of acquiring Assignor's entire right, title, and interest in the same;

NOW, THEREFORE, in consideration of one dollar ($1.00) and other good and valuable consideration paid to us by the Assignee, the receipt and sufficiency whereof is hereby acknowledged, we the said Assignors, hereby grant and assign unto the said Assignee, our entire right, title and interest in said invention and in all patent applications based thereon, including but not limited to the above identified United States Patent Application and in all provisionals, divisions, continuations, and continuations-in-part of said application, or reissues or extensions of Letters Patent or Patents granted thereon, and in all corresponding applications filed in countries foreign to the United States, and in all patents issuing thereon in the United States and

foreign countries; the right, power and authority to file and prosecute U.S. and foreign patent applications on said invention, and to do so in its own name wherever such right may be legally exercised, and including the right to claim the priority and benefits of the International Convention for such applications; and the right to bring actions for infringement of any right in said invention in its own name, including past infringement, in any jurisdiction.

We hereby authorize and request the United States Commissioner of Patents and Trademarks, and such Patent Office officials in foreign countries as are duly authorized by their patent laws to issue patents, to issue any and all Letters Patent on said invention to the said Assignee as the owner of our entire interest, for the sole use and behoof of the said Assignee, its successors, assigns and legal representatives, to the full end of the term for which said Letters Patent may be granted, as fully and entirely as the same would have been held by us had this assignment and sale not been made.

We hereby agree, without further consideration and without expense to us, to sign all lawful papers and to perform all other lawful acts which the Assignee may request of us to make this Assignment fully effective, including, by way of example but not of limitation, the following: prompt execution of all original, divisional, substitution, reissue, and other United States and foreign patent applications on said invention, and all lawful documents as requested by the Assignee to further the prosecution of any of such patent applications; and cooperation to the best of our ability including, but not limited to, the execution of all lawful documents, the production of evidence in any actions or proceedings concerning the invention, including, but not limited to, nullification, reissue, extension, and infringement proceedings involving said invention.

This assignment and agreement shall be binding upon our heirs and legal representatives.

Executed this 3rd day of April, 2014 at Beverly, MA
(place)

Martin U. Pralle

STATE OF _____)
: ss
County of _____)

Before me personally appeared Martin U. Pralle and acknowledged the foregoing instrument to be his free act and deed this ___ day of _____, 2014.

Notary Public

Executed this 7th day of April, 2014 at 1:28 PM Beaverton, OR (place)

Jeffrey McKee

STATE OF Oregon)
: ss
County of Washington)

Before me personally appeared Jeffrey McKee and acknowledged the foregoing instrument to be his free act and deed this 7th day of April, 2014.

OFFICIAL STAMP
DEBBIE GAY ZYGMUNTOWICZ
NOTARY PUBLIC - OREGON
COMMISSION NO. 926290
MY COMMISSION EXPIRES MARCH 28, 2018

Notary Public

Executed this 3rd day of April, 2014 at
(place)

Jason Sickler

STATE OF Connecticut)
: ss
County of Middlesex)

Before me personally appeared Jason Sickler and acknowledged the foregoing instrument to be his free act and deed this 3 day of April, 2014.

Notary Public

DARLENE D. ALLEN
NOTARY PUBLIC OF CONNECTICUT
My Commission Expires 3/31/2018

Electronic Acknowledgement Receipt

EFS ID:	18896354
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP
Receipt Date:	29-APR-2014
Filing Date:	15-MAR-2013
Time Stamp:	18:51:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	3035-052-NP-App-Data.pdf	1264938 9d314521fa0a50f77d797aa33bdbefbd20a54a8b	no	7
Warnings:					
Information:					

2	Oath or Declaration filed	3035-052-NP-Declarations.pdf	626449 d63c72dabdb5a12ec99281fc844b468ae2d7c09b	no	3
Warnings:					
Information:					
3	Power of Attorney	3035-052-NP-POA.pdf	76963 aa66da2a44b29923b633125eddba3ac54de331ff	no	1
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73.	3035-052-NP-Statement.pdf	290144 3fb5dc669877994035936e2c480cee86585c550a	no	7
Warnings:					
Information:					
		Total Files Size (in bytes):	2258494		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (11-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Martin	U.	Pralle	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Wayland	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	15 Rice Spring Lane		
Address 2			
City	Wayland	State/Province	MA
Postal Code	01778	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey		McKee	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Tualatin	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	22850 SW Eno Pl.		
Address 2			
City	Tualatin	State/Province	OR
Postal Code	97062	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jason		Sickler	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

City	Arlington	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	53 Varnum Street		
Address 2			
City	Arlington	State/Province	MA
Postal Code	02474	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	20551		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Pixel Isolation Elements, Devices and Associated Methods		
Attorney Docket Number	3035-052.NP	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Customer Number	20551

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
13841120	Claims benefit of provisional	61614275	2012-03-22

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (11-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	SiOnyx, Inc.

PTO/AIA/14 (11-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Mailing Address Information:			
Address 1	100 Cummings Ctr., Suite 243-F		
Address 2			
City	Beverly	**State/Province**	MA
Country [i]	US	Postal Code	01915
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country [i]		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (11-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Todd B. Alder/			Date (YYYY-MM-DD)	2014-04-29
First Name	Todd B.	Last Name	Alder	Registration Number	54598
Additional Signature may be generated within this form by selecting the Add button. Add					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IPR2025-00811
Apple-Sony EX1002 Page 410

Docket Number: 3035-052.NP

Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 13/841,120 filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Martin U. Pralle Date (Optional): 4/3/14

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Docket Number: **3035-052.NP** Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 13/841,120 filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Jeffrey McKee Date (Optional): 4-7-14

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Docket Number: 3035-052.NP

Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 13/841,120 filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Jason Sickler Date (Optional): 4/3/2014

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

POA ACCEPTANCE LETTER

OC000000068182592

Date Mailed: 05/05/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/29/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tpetros/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ART UNIT: 2814 EXAMINER: Long Pham FIRST NAMED INVENTOR: Martin U. Pralle SERIAL NO.: 13/841,120 FILED: 3/15/2013 CONF. NO.: 5133 FOR: PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS DOCKET NO.: 3035-052.NP	**CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8** DATE OF DEPOSIT: May 5, 2014 I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being submitted on the date indicated above via: ☐ EFS Web ☐ facsimile to _____ ☐ the United States Postal Service with sufficient postage as first class mail addressed to: Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450. /Nicole Solomon/ Nicole Solomon

THORPE NORTH & WESTERN, LLP
8180 South 700 East, Suite 350
Sandy, Utah 84070

RESTRICTION AND ELECTION OF SPECIES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the communication mailed March 6, 2014, please enter the following Restriction and Election of Species.

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RESTRICTION AND ELECTION OF SPECIES

Examiner has issued a restriction requirement under 35 U.S.C. § 121 as follows:

Group I: Claims 27-33, drawn to a process, classified in 438.

Group II: Claims 1-26, drawn to a device, classified in 257.

Furthermore, Examiner has also issued a species election requirement to one of the following species:

Species 1: embodiment of FIG. 1

Species 2: embodiment of FIG. 2

Species 3: embodiment of FIG. 3

Species 4: embodiment of FIG. 4

Species 5: embodiment of FIG. 5

Species 6: embodiment of FIG. 6

Species 7: embodiment of FIG. 7

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REMARKS

Pursuant to the restriction requirement detailed above, Applicant hereby elects, without traverse: Group II, claims 1-26, drawn to a device, classified in 257. Applicant also elects Species 4, embodiment of FIG. 4. Claims containing limitations relating to Species 4 include claims 1-13 and 19-23.

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CONCLUSION

In view of the foregoing, Applicant respectfully requests examination of claims 1-13 and 19-23. If any impediment to the prompt examination of these claims is found and could be removed during a telephone interview, the Examiner is invited to telephone the undersigned attorney, so that such issues may be resolved as expeditiously as possible.

Please charge any additional fees except for Issue Fee or credit any overpayment to Deposit Account No. 20-0100.

Dated this 5th day of May, 2014.

Respectfully submitted,

THORPE, NORTH & WESTERN, LLP

/Todd B. Alder/

Todd B. Alder Ph.D.
Reg. No. 54,598
8180 South 700 East, Suite 350
Sandy, UT 84070
Telephone: (801) 566-6633
Facsimile: (801) 566-0750

TBA/ns

IPR2025-00811
Apple-Sony EX1002 Page 418

Electronic Acknowledgement Receipt

EFS ID:	18948970
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP
Receipt Date:	05-MAY-2014
Filing Date:	15-MAR-2013
Time Stamp:	20:09:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		3035-052-NP-restriction.pdf	62305 1e058ee570ba39e67e5a286d243fa4347d56a690	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Response to Election / Restriction Filed	2	4
Warnings:			
Information:			
	Total Files Size (in bytes):	62305	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

PUBLICATION NOTICE

OC00000068592478

Title:PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

Publication No.US-2014-0138785-A1
Publication Date:05/22/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP	5133

20551 7590 07/09/2014
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

EXAMINER	
PHAM, LONG	
ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
07/09/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@tnw.com
rich@tnw.com
laron.lemon@tnw.com

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Office Action Summary	Application No. 13/841,120	Applicant(s) PRALLE, MARTIN U.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/5/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-33* is/are pending in the application.

5a) Of the above claim(s) *14-18 and 24-33* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-8,12,13,19 and 23* is/are rejected.

8)☒ Claim(s) *9-11 and 20-22* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *10/31/13,10/31/13*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-13 and 19-23 in the reply filed on 5/5/14 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 12, 13, and 23 are rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by Velichko (US pub 20130200251).

With respect to claim 1, Velichko teaches a light trapping device, comprising (see figs. 1-23 and associated text):

at least one light sensitive pixel 34 having a light incident surface, a backside surface opposite the light incident surface, and a peripheral

sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material 50 substantially covering the backside surface; and

a peripheral light trapping material 36 substantially covering the peripheral sidewall;

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

With respect to claim 12, Velichko teaches the peripheral sidewall extends completely around the pixel periphery.

With respect to claim 13, Velichko teaches the peripheral sidewall extends from the light incident surface to the backside surface.

With respect to claim 23, Velichko teaches an array of light trapping pixel devices.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-8 and 19 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Velichko (US pub 20130200251) as applied to claims 1, 12, 13, and 23 above, and further in view of Yanagisawa (JP 403183037).

With respect to claims 2 and 3, Velichko fails to teach the light trapping layer or reflector is made of a high refractive index layer sandwiched between 2 low refractive index layers.

Yanagisawa teaches a reflector made of a high refractive index layer sandwiched between 2 low refractive index layers to improve reflectivity.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Yanagisawa into the device of Velichko to achieve the above benefit.

With respect to claims 4, 5, and 6, Yanagisawa further teaches the two low refractive index materials or oxide have a refractive index of less than about 2.1 (oxide).

With respect to claims 7 and 8, Yanagisawa further teaches the high refractive index material or germanium includes a material having a refractive index or greater than or equal to about 2.1.

With respect to claim 19, Velichko fails to teach the light trapping material or reflector is made of metal.

However, the use of metal as light trapping material or reflector is well-known in semiconductor art.

Allowable Subject Matter

Claims 9-11 and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG PHAM whose telephone number is (571)272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/LONG PHAM/
Primary Examiner, Art Unit 2814

Notice of References Cited	Application/Control No. 13/841,120	Applicant(s)/Patent Under Reexamination PRALLE, MARTIN U.	
	Examiner LONG PHAM	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2013/0200251	08-2013	Velichko, Sergey	250/208.1
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP403183037	08-1991	Japan	Yanagiswa	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　平3－183037

⑤Int. Cl.⁵	識別記号	庁内整理番号	㊸公開　平成3年(1991)8月9日
G 11 B 7/24	B	8120－5D	

審査請求　未請求　請求項の数 2　（全6頁）

㊹発明の名称　光記憶体

㉑特　願　平1－318799
㉒出　願　平1(1989)12月11日

㉒発明者　柳沢　雅広　東京都港区芝5丁目33番1号　日本電気株式会社内
㉑出願人　日本電気株式会社　東京都港区芝5丁目7番1号
㉔代理人　弁理士　舘野　千恵子

明　細　書

1．発明の名称

光記憶体

2．特許請求の範囲

(1) 透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層または低屈折率層および高屈折率層の順よりなる組み合わせ層を少なくとも1層以上を備えてなることを特徴とする光記憶体。

(2) 透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層を少なくとも1層以上と、該組み合わせ層上に被覆される反射層とを備えてなることを特徴とする光記憶体。

3．発明の詳細な説明

［産業上の利用分野］

本発明は音響機器または情報機器などに用いられる光記憶体に関する。

［従来の技術］

従来、光記憶体の一つであるコンパクトディスク（以下、CDと略す。）の反射膜の材料としては、アルミニウムや金が使用されている。しかし、近年、CDにコンピュータデータを記録したCD－ROMが普及し、従来にも増して、高温・高湿下での保存性の高いものが望まれている。

［発明が解決しようとする課題］

従来の金あるいはアルミニウムの反射膜を使用した光記憶体は、かかる過酷な環境下において、蒸着された反射膜がアルミニウムの場合は腐食、また金の場合は下地体から剥離し、信号読み取りの指標とされるエラーレートが増加し、上記したようなニーズに適応できないという問題があった。またアルミニウムや金以外の反射膜材料は、反射率が不足するため使用できない状態にあった。

本発明は、以上述べたような従来の課題を解決するためになされたもので、耐候性、特に優れた耐食性と付着性を有し、かつ高反射率の反射膜を具備する光記憶体を提供することにある。

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［課題を解決するための手段］

本発明は、透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層または低屈折率層および高屈折率層の順よりなる組み合わせ層を少なくとも１層以上を備えてなることを特徴とする光記憶体、および透明基板と、該透明基板の記録ピット形成面上に被覆される高屈折率層および低屈折率層の順よりなる組み合わせ層を少なくとも１層以上と、該組み合わせ層上に被覆される反射層とを備えてなることを特徴とする光記憶体である。

本発明で用いられる高屈折率層は主としてシリコン，ゲルマニウム，ほう素，硫化亜鉛，酸化チタン，酸化ジルコニウム，酸化インジウム，酸化アンチモン，硫化アンチモン，テルル，テルル化カドミウム，テルル化鉛などを使用することができる。

また本発明で用いられる低屈折率層は酸化珪素，ふっ化マグネシウム，酸化アルミニウム，ふっ化セリウム，酸化マグネシウム，ふっ化カルシウム，ふっ化ナトリウム，ふっ化リチウム，カーボン（非晶質またはダイアモンド）などを使用することができる。

本発明で用いられる反射層はクロム，モリブデン，タングステン，バナジウム，ニオブ，タンタル，チタン，ジルコニウム，ハフニウム，マンガン，レニウム，ルテニウム，鉄，オスミウム，コバルト，ロジウム，イリジウム，ニッケル，パラジウム，白金，亜鉛，カドミウム，錫，鉛，タリウム，アンチモン，ビスマス，インジウム，ガリウムなどの金属またはそれらの合金または窒化チタン，窒化ジルコニウム，窒化ハフニウムなどの金属窒化物を使用することができる。また、金または銀の単体を反射層として用いることは付着性の面で、さらに銅，アルミニウムの場合は腐食性の点で望ましくないため、これらの金属を用いる場合には、前記反射層として使われる金属との合金として使用することが望ましい。

本発明で用いられる透明基板は、アクリル樹脂，ポリカーボネート樹脂，ポリオレフィン樹脂，エポキシ樹脂，フッ素樹脂，ガラス，ゾルゲルガラスなどを用いることができる。

本発明の光記憶体は、射出成形あるいはスタンパからの密着転写などにより記録ピットを形成した透明基板の上に、高屈折率層および低屈折率層を交互にスパッタ法、イオンプレーティング法、クラスターイオンビーム法、プラズマＣＶＤ法あるいは蒸着法等により被覆し、さらに必要に応じて反射層を上記と同様に組み合わせ層上に被覆して形成する。

透明基板は、例えば、ガラス基板の上に珪酸重合物をスピン塗布し、スタンパを密着させてピットを転写させ、ピット付きの透明基板を形成する。またスタンパの型の中に樹脂を射出し、型から取り出してピット付きの透明基板を形成してもよい。

このように作製した本発明の光記憶体は、高反射率と高耐候性（高付着および高耐食性）を併せ持ち、従来の金またはアルミニウム反射膜を直接透明基板に被覆したものよりはるかに優れた長期のデータ保存に関する信頼性を有する。

［作用］

本発明の光記憶体は、透明基板上に高屈折率層と低屈折率層よりなる組み合わせ層を形成する。この組み合わせ層によって、各層からの反射光が多重干渉を起こし、この時、各層の膜厚を適切な値に選択すると位相が一致し、反射率を 100%近くにまで高めることができる。従って、従来のように透明基板上に直接Ａℓ やＡｕ等よりなる反射膜を形成しなくともよく、信頼性の高い光記憶体が提供される。

高屈折率層と低屈折率層の組み合わせ層のみでも反射率を 100%近くにすることができるが、多層の組み合わせが必要となる。そこで低屈折率層と高屈折率層の組み合わせ層上に反射層を設けると、少ない組み合わせ層数で高反射率を得ることができる。また高屈折率層と低屈折率層の屈折率の差が大きいほど該２層の膜厚を薄くすることができ、ピットの形状（深さ，巾，長さ）を損ねる

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ことが少ない。

[実施例]

以下に、図面を参照して本発明の実施例を詳細に説明する。

第1図は本発明の光記憶体の一実施例を示したもので、第1図(a)はその部分断面図、第1図(b)は(a)におけるA部の拡大断面図である。ここで、透明基板1、高屈折率層2、低屈折率層3がそれぞれ第1表のIおよびIIに示す材質，構成および膜厚で被覆された2個の試料を作製した。

第2図は本発明の光記憶体1の他の一実施例を示したもので、第2図(a)はその部分断面図、第2図(b)は(a)におけるB部の拡大断面図である。ここで、透明基板1、低屈折率層3、高屈折率層2がそれぞれ第1表のIIIおよびIVに示す材質，構成および膜厚で被覆された2個の試料を作製した。

第3図は本発明の光記憶体1の他の一実施例を示す部分断面図である。ここで、透明基板1、高屈折率層2、低屈折率層3、反射層4がそれぞれ第1表のV，VI，VIIに示す材質，構成および膜厚で被覆された3個の試料を作製した。

得られた各試料の反射率を併せて第1表に示す。

(以下余白)

第　1　表

試料	透明基板	高屈折率層			低屈折率層			層数	反射層	反射率
		材質	膜厚(nm)	屈折率	材質	膜厚(nm)	屈折率		(膜厚nm)	(%)
I	ポリカーボネート	Si	40	3.5	SiO_2	60	1.5	10	なし	90
II	ゾルゲルガラス	TiO_2	60	2.7	MgF_2	60	1.4	10	なし	70
III	ポリオレフィン	PbTe	30	5.5	LiF	40	1.4	9	なし	96
IV	ゾルゲルガラス	Ge	40	4.0	CaF_2	50	1.2	7	なし	85
V	ポリカーボネート	Si	40	3.5	SiO_2	60	1.5	1	Cr (200)	80
VI	ポリオレフィン	Ge	40	4.0	MgF_2	60	1.4	1	Ta (200)	75
VII	ゾルゲルガラス	Si	40	3.5	CaF_2	50	1.2	1	TiN (300)	70

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次に、これらの試料とポリカーボネート樹脂からなる透明基板の上にアルミニウムおよび金を反射膜として形成した比較試料について、温度 70 ℃、相対湿度 95 %の耐候性試験を6ヶ月間行い、信号の良否の指標となるエラー数を測定した。6ヶ月の耐候性試験後、本発明の試料のエラー数は全く劣化がみられなかったが、アルミニウム反射膜を用いた比較試料は腐食により、また金反射膜を用いた比較試料は剥離によりエラーの測定が不能になるほど劣化した。

［発明の効果］

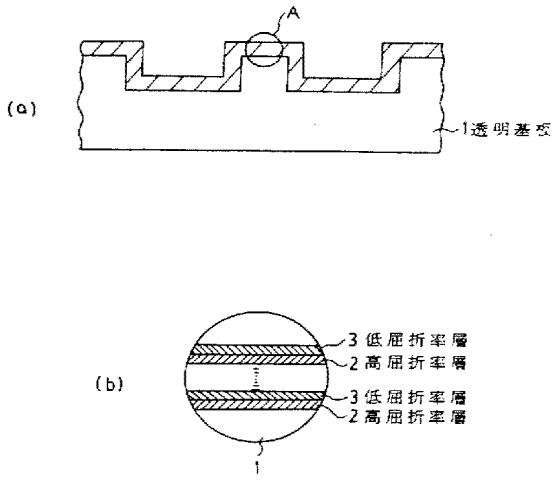
以上、詳細に述べたように、本発明の光記憶体は透明基板との密着性に優れ、かつ耐食性および高反射率を有しており、アルミニウムや金の反射膜を使用した光記憶体に比べてはるかに信頼性を向上させることができる。

4．図面の簡単な説明

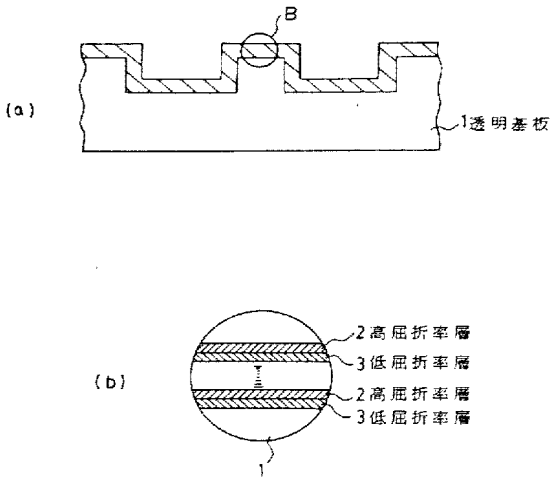
第1図から第3図はそれぞれ本発明の光記憶体の一実施例の部分断面図である。

1…透明基板
2…高屈折率層
3…低屈折率層
4…反射層

特許出願人　日本電気株式会社
代理人　弁理士　舘野千恵子

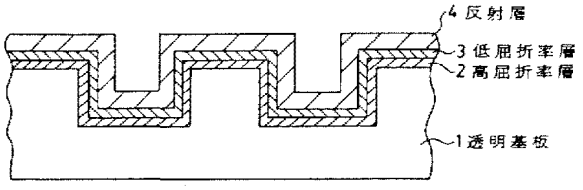


第1図



第2図

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第３図

手続補正書（自発）

平成３年３月５日

特許庁長官殿

１．事件の表示

特願平１－３１８７９９号

２．発明の名称

光記憶体

３．補正をする者

事件との関係　・特許出願人

住　所　東京都港区芝五丁目７番１号

名　称　(423) 日本電気株式会社

代表者　関　本　忠　弘

４．代　理　人　〒158

住　所　東京都世田谷区玉川４丁目12番16号

チロル玉川 202号　☎03(3707)1639

氏　名　(9052) 弁理士　舘　野　千恵子

特許庁
3.3.6

５．補正の対象

明細書の「発明の詳細な説明」の欄と
明細書の「図面の簡単な説明」の欄、
および図面

６．補正の内容

(1) 明細書第３頁 19 行目～ 20 行目に「酸化珪素，ふっ化マグネシウム」とあるのを「酸化珪素，酸化ジルコニウムを含む酸化珪素，ふっ化マグネシウム」と補正する。

(2) 明細書第８頁３行目のあとに以下の文を挿入する。

「第４図は本発明を再生専用光記憶体に適用した一実施例の部分断面図である。ここで１はゾルゲル法により記録ピットを設けた強化ガラス基板、高屈折率層２、低屈折率層３、反射層４がそれぞれ第１表のⅧに示す材料、構成および膜厚で被覆した１個の試料を作製した。反射層４の上には試料を操作する際に反射層等に傷が発生することを防止する意味でシリコン系の樹脂膜５が 10 μm被覆されている。また、強化ガラスの基板面側にはガラスの腐食を防止するための保護膜６として 10 %の酸化ジルコニウムを含む酸化珪素を 100nm被覆した。」

(3) 明細書第９頁第１表を以下のように補正する。

（以下余白）

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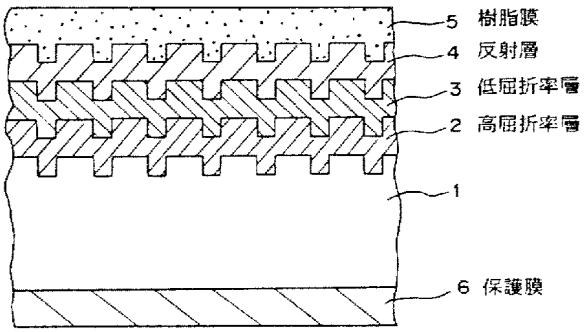
第　1　表

試料	透明基板	高屈折率層			低屈折率層			層数	反射層	反射率
		材質	膜厚	屈折率	材質	膜厚	屈折率		(膜厚nm)	(%)
I	ポリカーボネート	Si	40 nm	3.5	SiO_2	60 nm	1.5	10	なし	90
II	ゾルゲルガラス	TiO_2	60	2.7	MgF_2	60	1.4	10	なし	70
III	ポリオレフィン	PbTe	30	5.5	LiF	40	1.4	9	なし	96
IV	ゾルゲルガラス	Ge	40	4.0	CaF_2	50	1.2	7	なし	85
V	ポリカーボネート	Si	40	3.5	SiO_2	60	1.5	1	Cr (200)	80
VI	ポリオレフィン	Ge	40	4.0	MgF_2	60	1.4	1	Ta (200)	75
VII	ゾルゲルガラス	Si	40	3.5	CaF_2	50	1.2	1	TiN (300)	70
VIII	ゾルゲルガラス	Si	60	3.5	SiO_2 − 10%ZrO_2	40	1.5	1	Cr (100)	82

(4) 明細書第 10 頁 18 行目に「第1図から第3図」とあるのを「第1図から第4図」と補正する。

(5) 明細書第11頁1行目～3行目に「2…高屈折率層　3…低屈折率層　4…反射層」とあるのを「2…高屈折率層　3…低屈折率層　4…反射層　5…樹脂膜　6…保護膜」と補正する。

(6) 本願添付図面の第3図の次に別紙図面の第4図を追加する。



第4図

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PAT-NO: JP403183037A

DOCUMENT-IDENTIFIER: JP 03183037 A

TITLE: OPTICAL MEMORY MEDIUM

PUBN-DATE: August 9, 1991

INVENTOR-INFORMATION:

NAME	COUNTRY
YANAGISAWA, MASAHIRO	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
NEC CORP	N/A

APPL-NO: JP01318799

APPL-DATE: December 11, 1989

INT-CL (IPC): G11B007/24

US-CL-CURRENT: 369/283

ABSTRACT:

PURPOSE: To improve reliability by forming combined layers of high-refractive index layers of adequate film thicknesses on a transparent substrate, thereby obtaining a high reflectivity.

CONSTITUTION: The combinations of the high-refractive index layers 2 consisting of silicon, germanium, etc., and the low-refractive index layers 3 consisting of silicon oxide, magnesium fluoride, etc., are formed in ≥1 layers on the transparent substrate 1. The reflecting layers consisting of the respective layers generate multiple interferences in this way. The phases coincide and the reflectivity can be increased up to about 100% when the film thicknesses of the respective layers are selected at adequate values. There is, therefore, no need for forming the reflecting films consisting of Al, Au, etc., directly on the transparent substrate and the optical recording medium having the high reliability is obtd.

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13841120	PRALLE, MARTIN U.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/26/2014								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	O								
	10	O								
	11	O								
	12	✓								
	13	✓								
	14	N								
	15	N								
	16	N								
	17	N								
	18	N								
	19	✓								
	20	O								
	21	O								
	22	O								
	23	✓								
	24	N								
	25	N								
	26	N								
	27	N								
	28	N								
	29	N								
	30	N								
	31	N								
	32	N								
	33	N								

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PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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(Use as many sheets as necessary)

Sheet		of	

Complete if Known	
Application Number	13/841,120
Filing Date	3/15/2013
First Named Inventor	Martin U. Pralle
Art Unit	2883
Examiner Name	
Attorney Docket Number	3035-052.NP

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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		BODEN, S.A. et al.; Nanoimprinting for Antireflective Moth-Eye Surfaces; 4 pages; 2008	
		Carey et al., "Femtosecond-Laser-Assisted Microstructuring of Silicon Surfaces", Optics and Photonics News, 2003. 14, 32-36.	
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PTO/SB/08B (08-03)
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Application Number	13/841,120
Filing Date	3/15/2013
First Named Inventor	Martin U. Pralle
Art Unit	2883
Examiner Name	
Attorney Docket Number	3035-052.NP

Sheet | | of | |

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		MOLONEY, A.M. et al.; Novel Black Silicon PIN Photodiodes; 8 pages; January 25, 2006; SPIE	
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Application Number	13/841,120
Filing Date	3/15/2013
First Named Inventor	Martin U. Pralle
Art Unit	2883
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Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	26925	(high adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
L2	27823	(low adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
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L5	611	(reflector or Bragg) near10 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
L6	4200	2 near5 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49

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		7511750-$.DID. OR US-7745901-$.DID. OR US-7781856-$.DID. OR US-7816220-$.DID. OR US-7847253-$.DID. OR US-7884439-$.DID. OR US-7884446-$.DID. OR US-8030726-$.DID. OR US-8058615-$.DID. OR US-8207051-$.DID. OR US-8476681-$.DID. OR US-3666484-$.DID. OR US-2030766-$.DID. OR JP-07173484-$.DID. OR JP-071734840721-$.DID. OR JP-2008187003-$.DID. OR JP-2011091128-$.DID. OR JP-2152226-$.DID. OR JP-63116421-$.DID. OR JP-9298308-$.DID. OR KR-20010061058-$.DID. OR KR-20100118864-$.DID. OR WO-2006086014-$.DID. OR WO-2009100023-$.DID. OR WO-2011035188-$.DID. OR WO-2011119618-$.DID.				
S3	7768	(light adj2 (trapping or trapped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S4	11	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S5	2251	(reflector or Bragg) and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:40
S6	14	(reflector or Bragg) and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:41

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S7	888	(reflector or Bragg) near3 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S8	51623	(reflector or Bragg) near3 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S9	112640	pixel near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S10	143	S7 same S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S11	2	S9 same4 S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S12	3	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S13	1	S12 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S14	179	S7 same4 S8	US-PGPUB;	OR	ON	2014/06/25 15:58

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			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S15	145	S14 and (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S16	129	S14 same10 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S17	128	S14 same8 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S18	1204	(reflector or Bragg) near5 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S20	280	S18 same4 S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S21	195	S20 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR;	OR	ON	2014/06/25 16:09

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S22	7	S18 same2 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S23	7	S22 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S24	217	S18 same S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:13
S25	0	(light adj2 sensitive adj2 pixel) same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S26	0	(light adj2 sensitive adj2 pixel) and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S27	14	pixel same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S28	7	S27 and index	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/06/25 16:18

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			DERWENT; IBM_TDB			

EAST Search History (Interference)

< This search history is empty>

6/26/2014 1:26:02 PM
C:\Users\lpham\Documents\EAST\Workspaces\13-841,120.wsp

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Apple-Sony EX1002 Page 454

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ART UNIT:	2814
EXAMINER:	Long Pham
FIRST NAMED INVENTOR:	Martin U. Pralle
SERIAL NO.:	13/841,120
FILED:	03/15/2013
CONFRM. NO.:	5133
FOR:	Pixel Isolation Elements, Devices, and Associated Methods
DOCKET NO.:	3035-052.NP

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

DATE OF DEPOSIT: **November 10, 2014**

I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being submitted on the date indicated above via:

☒ EFS Web
☐ facsimile to _____
☐ the United States Postal Service with sufficient postage as first class mail addressed to: Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

/Nicole Solomon/
Nicole Solomon

THORPE NORTH & WESTERN, LLP
8180 South 700 East, Suite 350
Sandy, Utah 84070

RESPONSE UNDER 37 C.F.R. § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of July 9, 2014, please enter this amendment and reconsider this application in view of the remarks provided below. A petition for a one-month extension of time and the associated fee are filed herewith.

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AMENDMENTS TO THE CLAIMS

1. (currently amended) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall,~~;~~ wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field, and

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

2. (canceled).

3. (original) The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.

4-9. (canceled)

10. (currently amended) The device of claim ~~9~~1, wherein the dopant is boron or antimony.

11. (canceled)

12. (original) The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.

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13. (original) The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

14-18. (canceled)

19. (original) The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

20-22. (canceled)

23. (original) An array of light trapping pixel devices of claim 1.

24-33. (canceled)

34. (new) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall,

wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2, and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

35. (new) The device of claim 34, wherein the two second materials have a refractive index of less than about 2.1.

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36. (new) The device of claim 35, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.

37. (new)The device of claim 35, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.

38. (new) The device of claim 34, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.

39. (new) The device of claim 38, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.

40. (new) The device of claim 34, wherein the peripheral sidewall extends completely around the pixel periphery.

41. (new) The device of claim 34, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

42. (new) The device of claim 34, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

43. (new) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall,

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wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface, and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

44. (new) The device of claim 43, wherein the peripheral sidewall extends completely around the pixel periphery.

45. (new) The device of claim 43, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

46. (new) The device of claim 43, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

47. (new) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface;

a peripheral light trapping material substantially covering the peripheral sidewall; and

a textured layer positioned to interact with light proximal to the backside surface, wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

48. (new) The device of claim 47, wherein the textured layer is located between the backside surface and the backside light trapping material.

49. (new) The device of claim 47, wherein the peripheral sidewall extends completely around the pixel periphery.

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50. (new) The device of claim 47, wherein the peripheral sidewall extends from the light incident surface to the backside surface.

51. (new) The device of claim 47, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

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REMARKS

In the Office Action of July 9, 2014, claims 1-13 and 19-23 were pending for consideration. Examiner has indicated that claims 9-11 and 20-22 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claim. The remaining claims have been rejected under 35 USC 102(e) and 35 USC 103(a). Applicant has made the claim amendments outlined in detail below to take the allowable subject matter, thus rendering these rejections moot. As such, these rejections are not discussed in detail. It is noted, however, that the present amendments should not be seen as being in agreement with Examiner, and Applicant reserves the right to pursue any relinquished subject matter, and to address any point raised by Examiner, at a later time.

By the present amendment, claims 1 and 10 have been amended, and claims 2, 4-9, 11, 14-18, 20-22, and 24-33 have been canceled, which includes the previously withdrawn claims. Additionally, claims 34-51 have been added as rewritten claims. Applicant submits that no new matter is added thereby. Accordingly, claims 1, 3, 10, 12, 13, 19, 23, and 34-51 remain pending in the present application. The Applicant respectfully submits that the present claims are in condition for allowance.

The following list shows the amended and new claims, and where the support for each was derived.

Claim 1 contains all of the limitations of prior claims 1, 2, and 9

Claim 34 contains all the limitations of prior claims 1 and 11

Claim 35 is rewritten claim 4

Claim 36 is rewritten claim 5

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Claim 37 is rewritten claim 6

Claim 38 is rewritten claim 7

Claim 39 is rewritten claim 8

Claim 40 is rewritten claim 12

Claim 41 is rewritten claim 13

Claim 42 is rewritten claim 19

Claim 43 contains all the limitations of prior claims 1 and 20

Claim 44 is rewritten claim 12

Claim 45 is rewritten claim 13

Claim 46 is rewritten claim 19

Claim 47 contains all the limitations of prior claims 1 and 21

Claim 48 is rewritten claim 22

Claim 49 is rewritten claim 12

Claim 50 is rewritten claim 13

Claim 51 is rewritten claim 19

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CONCLUSION

Applicant expresses appreciation to Examiner for the examination of the present application, including the allowable subject matter. In view of the foregoing, Applicant submits that claims 1, 3, 10, 12, 13, 19, 23, and 34-51 present allowable subject matter. If any impediment to the allowance of these claims remains after consideration of the present amendment and above remarks, and such impediment could be removed during a telephone interview, the Examiner is invited to telephone the undersigned attorney so that such issues may be resolved as expeditiously as possible.

It is believed that no fee is due herewith: however, the Commissioner is hereby authorized to charge any required fee (except for Issue Fees) or credit any overpayment to Deposit Account No. 20-0100.

Dated this 10th day of November, 2014.

Respectfully submitted,

THORPE, NORTH & WESTERN, LLP

/Todd B. Alder/

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Telephone: (801) 566-6633
Facsimile: (801) 566-0750

TBA/ns

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Electronic Patent Application Fee Transmittal

Application Number:	13841120
Filing Date:	15-Mar-2013
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Todd Brent Alder/Nicole Solomon
Attorney Docket Number:	3035-052.NP

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	2251	1	100	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**100**

Electronic Acknowledgement Receipt

EFS ID:	20657570
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP
Receipt Date:	10-NOV-2014
Filing Date:	15-MAR-2013
Time Stamp:	19:01:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$100
RAM confirmation Number	5473
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Extension of Time	3035-052-NP-Extension.pdf	59047 8baedbebaf0d6ba310a9a4adfc13a99ea0683c5b	no	1
Warnings:					
Information:					
2		3035-052-NP-Response.pdf	75547 65f1dfdc8c937a79139df2b7edad937f49603416	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	9

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	29995 253aea82a457b9ac1af8bfa8ac529447f340467a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	164589		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/22 (03-13)
Approved for use through 3/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): 3035-052.NP

Application Number	Filed
13/841,120	3/15/2013

For: Pixel Isolation Elements, Devices and Associated Methods

Art Unit	Examiner
2814	Long Pham

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☑ One month (37 CFR 1.17(a)(1))	$200	$100	$50	$ 100
☐ Two months (37 CFR 1.17(a)(2))	$600	$300	$150	$
☐ Three months (37 CFR 1.17(a)(3))	$1,400	$700	$350	$
☐ Four months (37 CFR 1.17(a)(4))	$2,200	$1,100	$550	$
☐ Five months (37 CFR 1.17(a)(5))	$3,000	$1,500	$750	$

☑ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☑ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 20-0100.

☑ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).

☑ attorney or agent of record. Registration number 54598.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Todd B. Alder/	November 10, 2014
Signature	Date
Todd B. Alder, Ph.D.	801-566-6633
Typed or printed name	Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/841,120	Filing Date 03/15/2013	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **11/10/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 25	Minus	** 33	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X $210 =	210
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**210**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/TONYA MCBRIDE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

20551 7590 01/22/2015
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

EXAMINER
PHAM, LONG

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/22/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP	5133

TITLE OF INVENTION: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	04/22/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20551 7590 01/22/2015
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP	5133

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APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	04/22/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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P.O. Box 1219
SANDY, UT 84091-1219

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/22/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/841,120	Applicant(s) PRALLE, MARTIN U.	
	Examiner LONG PHAM	Art Unit 2814	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment dated 11/10/14*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1, 3, 10, 12, 13, 19, 23, and 34-51* . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LONG PHAM/
Primary Examiner, Art Unit 2814

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13841120	PRALLE, MARTIN U.
	Examiner	Art Unit
	LONG PHAM	2814

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/26/2014	01/05/2015							
	1	✓	=							
	2	✓	-							
	3	✓	=							
	4	✓	-							
	5	✓	-							
	6	✓	-							
	7	✓	-							
	8	✓	-							
	9	O	-							
	10	O	=							
	11	O	-							
	12	✓	=							
	13	✓	=							
	14	N	-							
	15	N	-							
	16	N	-							
	17	N	-							
	18	N	-							
	19	✓	=							
	20	O	-							
	21	O	-							
	22	O	-							
	23	✓	=							
	24	N	-							
	25	N	-							
	26	N	-							
	27	N	-							
	28	N	-							
	29	N	-							
	30	N	-							
	31	N	-							
	32	N	-							
	33	N	-							
	34		=							
	35		=							
	36		=							

IPR2025-00811
Apple-Sony EX1002 Page 475

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	13841120	PRALLE, MARTIN U.
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/26/2014	01/05/2015							
	37		=							
	38		=							
	39		=							
	40		=							
	41		=							
	42		=							
	43		=							
	44		=							
	45		=							
	46		=							
	47		=							
	48		=							
	49		=							
	50		=							
	51		=							

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("20140138785").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:26
L2	3930	(257/432).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
L4	218	(257/228).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2015/01/05 11:54
S2	84	US-3035052-$.DID. OR US-20030029495-$.DID. OR US-20040222187-$.DID. OR US-20050127401-$.DID. OR US-20050227390-$.DID. OR US-20060011955-$.DID. OR US-20060079062-$.DID. OR US-20060118781-$.DID. OR US-20060180885-$.DID. OR US-20060231914-$.DID. OR US-20070145505-$.DID. OR US-20080026550-$.DID. OR US-20080036022-$.DID. OR US-20080044943-$.DID. OR US-20080076240-$.DID. OR US-20080099804-$.DID. OR US-20080178932-$.DID. OR US-20080258604-$.DID. OR US-20090065051-$.DID. OR US-20090142879-$.DID. OR US-20090160983-$.DID. OR US-20090194671-$.DID. OR US-20090200586-$.DID. OR US-20090213883-$.DID. OR US-3487223-$.DID. OR US-4277793-$.DID. OR US-4419533-$.DID. OR US-4493942-$.DID. OR US-4514582-$.DID. OR US-4536608-$.DID. OR US-4663188-$.DID. OR US-4829013-$.DID. OR US-5080725-$.DID. OR US-5081049-$.DID. OR US-5100478-$.DID. OR US-5114876-$.DID. OR US-5164324-$.DID. OR US-	US-PGPUB; USPAT; USOCR; JPO; IBM_TDB	OR	ON	2014/06/25 14:14

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		5322988-$.DID. OR US-5346850-$.DID. OR US-5597621-$.DID. OR US-5714404-$.DID. OR US-5731213-$.DID. OR US-5792280-$.DID. OR US-6147297-$.DID. OR US-6498336-$.DID. OR US-6580053-$.DID. OR US-6583936-$.DID. OR US-6667528-$.DID. OR US-6759262-$.DID. OR US-6800541-$.DID. OR US-7057256-$.DID. OR US-7091411-$.DID. OR US-7109517-$.DID. OR US-7247527-$.DID. OR US-7314832-$.DID. OR US-7354792-$.DID. OR US-7390689-$.DID. OR US-7442629-$.DID. OR US-7456452-$.DID. OR US-7482532-$.DID. OR US-7498650-$.DID. OR US-7504325-$.DID. OR US-7504702-$.DID. OR US-7511750-$.DID. OR US-7745901-$.DID. OR US-7781856-$.DID. OR US-7816220-$.DID. OR US-7847253-$.DID. OR US-7884439-$.DID. OR US-7884446-$.DID. OR US-8030726-$.DID. OR US-8058615-$.DID. OR US-8207051-$.DID. OR US-8476681-$.DID. OR US-3666484-$.DID. OR US-2030766-$.DID. OR JP-07173484-$.DID. OR JP-071734840721-$.DID. OR JP-2008187003-$.DID. OR JP-2011091128-$.DID. OR JP-2152226-$.DID. OR JP-63116421-$.DID. OR JP-9298308-$.DID. OR KR-20010061058-$.DID. OR KR-20100118864-$.DID. OR WO-2006086014-$.DID. OR WO-2009100023-$.DID. OR WO-2011035188-$.DID. OR WO-2011119618-$.DID.				
S3	7768	(light adj2 (trapping or trapped))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16

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S4	11	S2 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 14:16
S5	2251	(reflector or Bragg) and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:40
S6	14	(reflector or Bragg) and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:41
S7	888	(reflector or Bragg) near3 backside	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S8	51623	(reflector or Bragg) near3 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:55
S9	112640	pixel near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S10	143	S7 same S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:56
S11	2	S9 same4 S10	US-PGPUB;	OR	ON	2014/06/25 15:56

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			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S12	3	S9 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S13	1	S12 not S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:57
S14	179	S7 same4 S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:58
S15	145	S14 and (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S16	129	S14 same10 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S17	128	S14 same8 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 15:59
S18	1204	(reflector or Bragg) near5 backside	US-PGPUB; USPAT; USOCR;	OR	ON	2014/06/25 16:09

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S19	71202	(reflector or Bragg) near5 (side or sidewall or edge or wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S20	280	S18 same4 S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S21	195	S20 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:09
S22	7	S18 same2 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S23	7	S22 same4 (photodiode or pixel or light)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:10
S24	217	S18 same S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:13
S25	0	(light adj2 sensitive adj2 pixel) same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/06/25 16:14

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			DERWENT; IBM_TDB			
S26	0	(light adj2 sensitive adj2 pixel) and S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S27	14	pixel same4 S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:14
S28	7	S27 and index	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/25 16:18
S29	26925	(high adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S30	27823	(low adj2 index) near3 (layer or film)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S31	12802	S29 near10 S30	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:48
S32	1170	(reflector or Bragg) same S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49

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S33	611	(reflector or Bragg) near10 S31	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S34	4200	S30 near5 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:49
S35	1972	S34 near10 S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S36	81	(reflector or Bragg) near10 S35	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:50
S37	188	S29 near5 (polysilicon or polycrystalline or poly or (amorphous adj2 silicon) or germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S38	2500	S30 near5 (oxide or nitride or oxynitride or oxynitrides)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S39	14	S37 near20 S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:53
S40	0	(reflector or Bragg) same S39	US-PGPUB;	OR	ON	2014/06/26 12:54

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			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S41	0	S39 near20 ("between")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 12:54
S42	51	backside near6 (textured near2 (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:12
S43	10	S42 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25

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S44	5	S39 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25
S45	2	S36 AND ((H01L21/02686 OR H01L27/1214 OR H01L21/02532 OR H01L21/02595 OR H01L31/0236 OR H01L21/0237 OR H01L21/02403 OR H01L21/0243 OR H01L21/02472 OR H01L21/02483 OR H01L21/02494 OR H01L21/02554 OR H01L21/02565 OR H01L21/02573 OR H01L21/02587 OR H01L21/02609 OR H01L21/0262 OR H01L21/365 OR H01L2224/16 OR H01L27/14625 OR H01L27/14627 OR H01L27/14629 OR H01L27/1463 OR	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/06/26 13:25

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Apple-Sony EX1002 Page 485

		H01L27/14685 OR H01L31/02168 OR H01L31/022425 OR H01L31/02363 OR H01L31/042 OR H01L31/0527 OR H01L31/0682 OR H01L31/18 OR H01L31/1804 OR H01L33/0087 OR H01L33/22 OR H01L33/24 OR H01L33/28 OR H01L33/385 OR H01L33/405 OR H01L33/483 OR H01L33/60 OR H01L33/62).CPC.)				

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	1	(257/432).CCLS.	UPAD	OR	OFF	2015/01/05 11:54

1/5/2015 11:55:42 AM
C:\Users\lpham\Documents\EAST\Workspaces\13-841,120.wsp

IPR2025-00811
Apple-Sony EX1002 Page 486

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13841120	PRALLE, MARTIN U.
	Examiner	**Art Unit**
	LONG PHAM	2814

CPC						
Symbol					**Type**	**Version**
H01L		27	/	14625	F	2013-01-01
H01L		27	/	14627	A	2013-01-01
H01L		27	/	14629	I	2013-01-01
H01L		27	/	1463	I	2013-01-01
H01L		27	/	14685	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	25	
/LONG PHAM/ Primary Examiner.Art Unit 2814	01/05/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3,4

IPR2025-00811
Apple-Sony EX1002 Page 487

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13841120	PRALLE, MARTIN U.
	Examiner	**Art Unit**
	LONG PHAM	2814

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
257	432	H	0	1	L	27 / 146 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	228				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	25	
/LONG PHAM/ Primary Examiner.Art Unit 2814	01/05/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3,4

IPR2025-00811
Apple-Sony EX1002 Page 488

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13841120	PRALLE, MARTIN U.
	Examiner	**Art Unit**
	LONG PHAM	2814

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	43												
2	3	18	44												
3	10	19	45												
4	12	20	46												
5	13	21	47												
6	19	22	48												
7	23	23	49												
8	34	24	50												
9	35	25	51												
10	36														
11	37														
12	38														
13	39														
14	40														
15	41														
16	42														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 25	
/LONG PHAM/ Primary Examiner.Art Unit 2814 (Primary Examiner)	01/05/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 3,4

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Apple-Sony EX1002 Page 489

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13841120	PRALLE, MARTIN U.
	Examiner	Art Unit
	LONG PHAM	2814

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	432, 228	1/5/2015	LP

SEARCH NOTES		
Search Notes	Date	Examiner
Updated text and interference searches	1/5/2015	LP

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	432	1/5/2015	LP

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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5133

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/841,120	03/15/2013 RULE	257	2814	3035-052.NP

APPLICANTS
SiOnyx, Inc., Beverly, MA, Assignee (with 37 CFR 1.172 Interest);

INVENTORS
Martin U. Pralle, Wayland, MA;

**** CONTINUING DATA ***************************
This appln claims benefit of 61/614,275 03/22/2012

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
05/17/2013

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /LONG PHAM/ Examiner's Signature	☐ Met after Allowance LP Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		MA	4	33	3

ADDRESS

THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219
UNITED STATES

TITLE

PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

FILING FEE RECEIVED		
1320	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

IMPROPER CFR REQUEST

OC000000073842267

Date Mailed: 03/10/2015

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Power of Attorney, Claims, Fees, System Limitations, and Miscellaneous

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- The request to correct inventorship or inventor name(s) under 37 CFR 1.48 is deficient because the fee set forth in 37 CFR 1.17(i) (for a nonprovisional application) or 37 CFR 1.17(q) (for a provisional application) has not been submitted.
- The ADS submitted on 04/29/2014 was not properly marked up to show the desired changes. For information being changed relative to the information already of record, additions must be shown with underlining, and deletions must be shown with strike-through or brackets. See 37 CFR 1.76(c)(2)

/ctuazon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IPR2025-00811
Apple-Sony EX1002 Page 492

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

ART UNIT:	2814
EXAMINER:	Long Pham
FIRST NAMED INVENTOR:	Martin U. Pralle
SERIAL NO.:	13/841,120
FILED:	March 15, 2013
CONF. NO.:	5133
FOR:	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS
DOCKET NO.:	3035-052.NP

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

DATE OF DEPOSIT: **April 21, 2015**

I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being submitted on the date indicated above via:

☒ EFS Web
☐ facsimile to _____
☐ the United States Postal Service with sufficient postage as first class mail addressed to: Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

/Nicole Solomon/
Nicole Solomon

REQUEST FOR CORRECTION OF INVENTORSHIP

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Pursuant to 37 C.F.R. § 1.48, Applicant respectfully requests that the above-identified application be amended to add the following inventors:

Jeffrey McKee
Jason Sickler

The fee as required under 1.17(i) and an updated Application Data Sheet reflecting these changes is enclosed. Please charge any additional fees due, or deposit any overpayments, to Deposit Account No. 20-0100 of the undersigned.

Dated this 21st day of April, 2015.

Respectfully submitted,

/Todd B. Alder/

Todd B. Alder, Ph.D.
Attorney for Applicant
Registration No. 54598

THORPE NORTH & WESTERN, LLP
Customer No. 20,551
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Sandy, Utah 84091-1219
(801) 566-6633

PTO/SB/17i (03-13)
Approved for use through 03/31/2013. OMB 0651-0031
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PROCESSING FEE Under 37 CFR 1.17(i) TRANSMITTAL

(Fees are subject to annual revision)

Send completed form to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Application Number	13/841,120
Filing Date	3/15/2013
First Named Inventor	Martin U. Pralle
Art Unit	2814
Examiner Name	Long Pham
Practitioner Docket No.	3035-052.NP

Enclosed is a paper filedunder 37 CFR 1.48 **that requires a processing fee (37 CFR 1.17(i)(1) or (2)).**

Payment of $ 70 **is enclosed.**

This form should be included with the above-mentioned paper and faxed or mailed tothe Office using the appropriate Mail Stop, if applicable. *For transmittal of petition fees under 37CFR 1.17(f), (g) or (h), see form PTO/SB/17p.*

☑ Applicant assertssmall entitystatus. See37 CFR 1.27.

☐ Applicant certifiesmicro entitystatus. See37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

Payment of Fees

☑ The Commissioner is hereby authorized tocharge the following fees to Deposit Account No. 20-0100:

☐ processing fee under 37 CFR 1.17(i)(1) ☐ processing fee under 37 CFR 1.17(i)(2) ☑ any deficiency of fees and credit of any overpayments

☐ Check in the amount of $ _____ is enclosed. ☑ Payment via EFS-Web.

☑ Payment by credit card (Form PTO-2038 or equivalent is enclosed). Do not provide credit card information on this form.

Processing Fees Under 37 CFR 1.17(i)(1):

Undiscounted Fee $140 (Fee Code 1053) Small Entity Fee $70 (Fee Code 2053) Micro Entity Fee $35 (Fee Code 3053)

For papers filed under:
§ 1.28(c)(3) - for processing a nonitemized fee deficiency based on an error in small entity status.
§ 1.41 - for supplying the name or names of the inventor or inventors after the filing date without an oath or declaration as prescribed by § 1.63, except in provisional applications.
§ 1.48 - for correcting inventorship, except in provisional applications.
§ 1.52(d) - for processing a nonprovisional application filed with a specification in a language other than English.
§ 1.53(b)(3) - to convert a provisional application filed under § 1.53(c) into a nonprovisional application under § 1.53(b).
§ 1.55 - for entry of late priority papers.
§ 1.71(g)(2) - for processing a belated amendment under § 1.71(g).
§ 1.99(e) - for processing a belated submission under § 1.99.
§ 1.102(e) - for requesting prioritized examination of an application.
§ 1.103(b) - for requesting limited suspension of action, continued prosecution application for a design patent (§ 1.53(d)).
§ 1.103(c) - for requesting limited suspension of action, request for continued examination (§ 1.114).
§ 1.103(d) - for requesting deferred examination of an application.
§ 1.291(c)(5) - for processing a second or subsequent protest by the same real party in interest.
§ 1.497(d) - for filing an oath or declaration pursuant to 35 U.S.C. 371(c)(4) naming an inventive entity different from the inventive entity set forth in the international stage.
§ 3.81 - for a patent to issue to assignee, assignment submitted after payment of the issue fee.

Processing Fees Under 37 CFR 1.17(i)(2):

Fee $130(small andmicro entity discounts are not available for the 37 CFR 1.17(i)(2) processing fee)

For papers filed under:
§ 1.217 - for processing a redacted copy of a paper submitted in the file of an application in which a redacted copy was submitted for the patent application publication. **FEE CODE 1808**
§ 1.221 - for requesting voluntary publication or republication of an application. **FEE CODE 1803**

SUBMITTED BY

Signature	/Todd B. Alder/	Registration No. (Attorney/Agent) 54598	Telephone 801-566-6633
Name (Print/Type)	Todd B. Alder		Date April 21, 2015

This collection of information is required by 37 CFR 1.17. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (11-13)
Approved for use through 01/31/2014. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Martin	U.	Pralle	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Wayland	State/Province	MA	Country of Residence	US

Mailing Address of Inventor:

Address 1	15 Rice Spring Lane		
Address 2			
City	Wayland	State/Province	MA
Postal Code	01778	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
***	Jeffrey		McKee	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Tualatin	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	22850 SW Eno Pl.		
Address 2			
City	Tualatin	State/Province	OR
Postal Code	97062	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
***	Jason		Sickler	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

PTO/AIA/14 (11-13)
Approved for use through 01/31/2014. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

City	Arlington	State/Province	MA	Country of Residence	US

Mailing Address of Inventor:

Address 1	53 Varnum Street		
Address 2			
City	Arlington	State/Province	MA
Postal Code	02474	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	20551		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	Pixel Isolation Elements, Devices and Associated Methods		
Attorney Docket Number	3035-052.NP	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

PTO/AIA/14 (11-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Customer Number	20551

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
*** 13841120	Claims benefit of provisional	61614275	2012-03-22

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (11-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

*** ◉ Assignee ○ Legal Representative under 35 U.S.C. 117 ○ Joint Inventor

○ Person to whom the inventor is obligated to assign. ○ Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

*** Organization Name: SiOnyx, Inc.

IPR2025-00811
Apple-Sony EX1002 Page 499

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Mailing Address Information For Applicant:			
Address 1	100 Cummings Ctr., Suite 243-F		
Address 2			
City	Beverly	**State/Province**	MA
Country i	US	Postal Code	01915
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

PTO/AIA/14 (11-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	Pixel Isolation Elements, Devices and Associated Methods	

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
Signature	/Todd B. Alder/			Date (YYYY-MM-DD)	2015-04-21
First Name	Todd B.	Last Name	Alder	Registration Number	54598
Additional Signature may be generated within this form by selecting the Add button.					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Docket Number: 3035-052.NP

Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 13/841,120 filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Martin U. Pralle Date (Optional): 4/3/14

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Docket Number: **3035-052.NP** Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 13/841,120 filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT International filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Jeffrey McKee Date (Optional): 4-7-14

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Docket Number: 3035-052.NP

Substitute Form PTO/AIA/01

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	Pixel Isolation Elements, Devices and Associated Methods

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application or,

☑ United States application or PCT international application number 13/841,120 filed on 3/15/2013.

The above-identified application was made or authorized to be made by me.

I have reviewed and understand the contents of the above-identified application, including the claims. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

LEGAL NAME OF INVENTOR

Inventor: Jason Sickler Date (Optional): 4/3/2014

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

Electronic Patent Application Fee Transmittal

Application Number:	13841120
Filing Date:	15-Mar-2013
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	Todd Brent Alder/Nicole Solomon
Attorney Docket Number:	3035-052.NP

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
PROCESSING FEE, EXCEPT PROV. APPLS.	2830	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**70**

Electronic Acknowledgement Receipt	
EFS ID:	22126611
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Todd Brent Alder/Nicole Solomon
Filer Authorized By:	Todd Brent Alder
Attorney Docket Number:	3035-052.NP
Receipt Date:	21-APR-2015
Filing Date:	15-MAR-2013
Time Stamp:	16:48:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$70
RAM confirmation Number	3767
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request under Rule 48 correcting inventorship	3035-052_NP_Correction_Inventorship.PDF	60547 f86af6384ac66e811252aad3b74901cbdcb57185	no	1
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	3035-052_NP_Fee_Trans_sb0017i.pdf	241837 0bf1435640cd26ae674dcc125d2f85f3d0e7ae58	no	2
Warnings:					
Information:					
3	Application Data Sheet	3035-052_NP_Updated_ADS.pdf	484560 b8c608db7b13ea86a4033c6b496b1f20923379e1	no	7
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
4	Oath or Declaration filed	3035-052_NP_Declarations.pdf	618592 cc3f932028e8cd356aafcde586bbe3de6d467153	no	3
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30062 078e797528bd0b5d7bd26173dff190170520d310	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1435598		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 04/22/2015

CVORACHA SALE #00000014 Mailroom Dt: 04/21/2015 200100 13841120
01 FC : 2819 300.00 DA

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Nicole Solomon	(Depositor's name)
/Nicole Solomon/	(Signature)
April 22, 2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP	5133

TITLE OF INVENTION: Pixel Isolation Elements, Devices and Associated Methods

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$4480	$0	$0	$480	04/22/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
PHAM, LONG	2814	257-432000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Thorpe North & Western, LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SiOnyx, Inc.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Beverly, MA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☑ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

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5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Todd B. Alder/ Date April 22, 2015
Typed or printed name Todd B. Alder, Ph.D. Registration No. 54598

IPR2025-00811
Apple-Sony EX1002 Page 512

Electronic Patent Application Fee Transmittal

Application Number:	13841120
Filing Date:	15-Mar-2013
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Filer:	David William Osborne/Nicole Solomon
Attorney Docket Number:	3035-052.NP

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**480**

Electronic Acknowledgement Receipt

EFS ID:	22141766
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	David William Osborne/Nicole Solomon
Filer Authorized By:	David William Osborne
Attorney Docket Number:	3035-052.NP
Receipt Date:	22-APR-2015
Filing Date:	15-MAR-2013
Time Stamp:	19:06:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$480
RAM confirmation Number	5484
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	3035-052_NP_Issue_Fee.pdf	104946 d919a9863bfea75d2b81aa041a091a59cb06906f	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30311 4811e36bdb283ba4d42c948da8dbbbca204bf9d0	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	135257		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/841,120	03/15/2013	2814	1320	3035-052.NP	33	3

CONFIRMATION NO. 5133

CORRECTED FILING RECEIPT

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

OC000000074832226

Date Mailed: 04/28/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

Applicant(s)

SiOnyx, Inc., Beverly, MA

Assignment For Published Patent Application

SiOnyx, Inc., Beverly, MA

Power of Attorney: The patent practitioners associated with Customer Number 20551

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/614,275 03/22/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 05/17/2013
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/841,120**
Projected Publication Date: Not Applicable
Non-Publication Request: No
Early Publication Request: No
** **SMALL ENTITY** **

IPR2025-00811
Apple-Sony EX1002 Page 517

Title

PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Apple-Sony EX1002 Page 518

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/841,120	06/23/2015	9064764	3035-052.NP	5133

20551 7590 06/03/2015

THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

SiOnyx, Inc., Beverly, MA;
Martin U. Pralle, Wayland, MA;
Jeffrey McKee, Tualatin, OR;
Jason Sickler, Arlington, MA;

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PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | | of |

Complete if Known	
Application Number	13/841,120
Filing Date	3/15/2013
First Named Inventor	Martin U. Pralle
Art Unit	2883
Examiner Name	
Attorney Docket Number	3035-052.NP

Change(s) applied to document, /S.X.R./ 3/12/2013

		2012/0171804	07/2012	Moslehi et al.	
		~~2012/0222396~~	05/2012	Saylor et. at	20120111396
		2012/0312304	12/13/2012	~~Haddad et al.~~	Lynch et al.
		2012/0313204	12/13/2012	Haddad et al.	
		2012/0313205	12/13/2012	Haddad et al.	
		2012/0313205	~~12/13/2013~~	Haddad et al.	December 13, 2012
		2013/0168792	07/04/2013	Haddad et al.	
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		4663188	05/1987	Kane	
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		5164324	11/17/1992	Russell et al.	
		5322988	06/21/1994	Russell et al.	
		5346850	09/13/1994	Kaschmitter et al.	
		5597621	01/18/1997	Hummel et al.	
		5714404	02/03/1998	Mititsky et al.	
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		5792280	08/1998	Ruby et al	
		6147297	11-14-2000	Wettling et al.	
		6498336	12/24/2002	Tian et al.	
		6580053	06/2003	Voutsas	
		6583936	06/2003	Kaminsky et al.	
		6667528	12/23/2003	Cohen et al.	
		6759262	07/06/2004	Theil et al.	
		6800541	10/2004	Okumura	
		7057256	06/06/2006	Carey, III et al.	
		7091411	08/15/2006	Falk et al.	
		7109517	09/19/2006	Zaidi	
		7247527	07/24/2007	Shimomura et al.	
		7314832	01/01/2008	Kountz et al.	
		7354792	04/08/2008	Carey, III et al.	
		7390689	06/24/2008	Mazur et al.	
		7442629	10/28/2008	Mazur et al.	
		7456452	11-25-2008	Wells et al.	
		7482532	01/27/2009	Yi et al.	
		7498650	03-03-2009	Lauxtermann	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

PTO/SB/08A (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | | of |

Complete if Known	
Application Number	13/841,120
Filing Date	3/15/2013
First Named Inventor	Martin U. Pralle
Art Unit	2883
Examiner Name	
Attorney Docket Number	3035-052.NP

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2003/0029495	02/2003	Mazur et al.	
		2004/0222187	11/11/2004	Lin	
		2005/0127401	06/16/2005	Mazur et al.	
		2005/0227390	10/2005	Shtein et al.	
		2006/0011955	01/19/2006	Baggenstoss	
		2006/0079062	04/2006	Mazur et al.	
		2006/0118781	06/08/2006	Rhodes	
Change(s) applied to document, /S.X.R./ 3/12/2015		2006/0180885	~~02/14/2005~~	Rhodes August 17, 2006	
		2006/0231914	10/2006	Carey, III et al.	
		2007/0145505	06/28/2007	Kim et al.	
		2008/0026550	01/31/2008	Werner et al.	
		2008/0036022	02/14/2008	Hwang et al.	
		2008/0044943	02/21/2008	Mazur et al.	
		2008/0076240	03/27/2008	Yannick Veschtti et al.	
		2008/0099804	05-01-2008	Venezia	
		2008/0178932	07/31/2008	Willem Den Boer et al.	
		2008/0258604	10/23/2008	Mazur et al.	
		2009/0065051	03/12/2009	Chan et al.	
		2009/0142879	06/2009	Isaka et al.	
		2009/0160983	06/25/2009	Lenchenkov	
		2009/0194671	08/06/2009	Nozaki et al.	
		2009/0200586	08/13/2009	Mao et al.	
		2009/0213883	08/2009	Mazur et al.	
		2010/0037952	02-18-2010	Lin	
		2010/0052088	03/04/2010	Carey	
		2010/0055887	03/04/2010	Piwczyk	
		2010/0072349	03/2010	Veeder	
		2010/0074396	03-25-2010	Schmand et al.	
		2010/0143744	06-10-2010	Gupta	
		2010/0219506	09-02-2010	Gupta	
		2010/0224229	09/2010	Pralle et al.	
		2010/0240169	09/23/2010	Petti et al.	
		2010/0264473	10/21/2010	Adkisson et al.	
		2010/0290668	11/18/2010	Friedman et al.	
		2010/0300505	12/2010	Chen	
		2011/0073976	03/31/2011	Vaillant	
		2011/0140221	06/16/2011	Venezia et al.	
		2011/0220971	09/15/2011	Hadda	
		2011/0227138	09/22/2011	Hadda	
		2011/0266644	11/04/2011	Yamamura et al.	
		2011/0303999	12/15/2011	Sakamoto et al.	
Change(s) applied to document, /S.X.R./ 3/12/2015		2012/0024363	02/2012	~~Carey et al.~~ DIMER; Martin ; et al.	
		2012/0024364	02/02/2012	Carey, III et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.P./

PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 136549

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 136549

OR

☐	Firm or Individual Name		
	Address		
	City	State	Zip
	Country		
	Telephone	Email	

Assignee Name and Address: SiOnyx, LLC
100 Cummings Center, Suit 243F
Beverly, MA 01915

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	12/18/15
Name	Stephen Saylor	Telephone	508.561.4305
Title	CEO, SiOnyx LLC		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: SiOnyx, LLC

Application No./Patent No.: 9,064,764 Filed/Issue Date: June 23, 2015

Titled: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

SiOnyx, LLC, a Limited Liability Company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: SiOnyx, Inc.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 032782, Frame 0863, or for which a copy thereof is attached.

2. From: SiOnyx, Inc. To: SiOnyx, LLC

   The document was recorded in the United States Patent and Trademark Office at
   Reel 037449, Frame 0884, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Andrew W. Schultz/	January 13, 2016
Signature	Date
Andrew W. Schultz	66,869
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	24612514
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	3035-052.NP
Receipt Date:	13-JAN-2016
Filing Date:	15-MAR-2013
Time Stamp:	15:43:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	SiOnyxGeneralPOA.pdf	135238 e9afbd7bc0956680044b1515c2efca6b59ea1bc3	no	2
Warnings:					
Information:					

2	Assignee showing of ownership per 37 CFR 3.73	StatementUnder37CFR373.pdf	120213 057cbd6fc0a177d4dc05785fc52ca89c5073e63f	no	3

Warnings:	
Information:	
Total Files Size (in bytes):	255451

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: N572

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

OC000000080175289

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

Cc: PEPPER HAMILTON LLP/SIONYX LLC
ATTN: BOSTON IP DOCKETING DEPARTMENT
125 HIGH STREET
19TH FLOOR
BOSTON, MA 02110-2736

Date Mailed: 01/28/2016

DENIAL OF REQUEST FOR POWER OF ATTORNEY

The request for Power of Attorney filed 01/13/2016 is acknowledged. However, the request cannot be granted at this time for the reason stated below.

- ☐ The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.
- ☐ The revocation is not signed by the applicant, the assignee of the entire interest, or one particular principal attorney having the authority to revoke.
- ☐ The Power of Attorney is from an assignee and the Certificate required by 37 CFR 3.73(c) has not been received.
- ☐ The person signing for the assignee has omitted their empowerment to sign on behalf of the assignee.
- ☐ The inventor(s) is without authority to appoint attorneys since the assignee has intervened as provided by 37 CFR 3.71.
- ☐ The signature(s) of _____a co-inventor in this application, has been omitted. The Power of Attorney will be entered upon receipt of confirmation signed by said co-inventor(s).
- ☐ The person(s) appointed in the Power of Attorney is not registered to practice before the U.S. Patent and Trademark Office.
- ☐ Only one Customer Number can be designated for the Power of Attorney in an application. The Customer Number that was captured is the first Customer Number provided on the Power of Attorney document.
- ☐ A request under 37 CFR 1.48 to add an inventor was granted in this application, however, no power of attorney consistent with the power of attorney granted by the originally named inventive entity has

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been received. Thus, the addition of the inventor has resulted in the loss of power of attorney in the application. See 37 CFR 1.32(e).

☑ The power of attorney has not been accepted because the party who is giving power of attorney has not been identified. Power of attorney may only be signed by the applicant for patent (37 CFR 1.42) or the patent owner. A patent owner who was not the applicant must appoint any power of attorney in compliance with 37 CFR 3.71 and 3.73. See 37 CFR 1.32(b)(4).

☐ The power of attorney from the inventors has not been accepted because it is a copy from a prior national application for which benefit is claimed and the continuing application names an inventor who was not named as an inventor in the prior application.

☐ The power of attorney from the inventors has not been accepted because the power of attorney must be signed by the applicant for patent. See 37 CFR 1.32(b)(4).

☑ Any request to correct or update the name of the applicant must include an application data sheet (ADS) in compliance with 37 CFR 1.76 specifying the correct or updated name of the applicant in the applicant information section. Any request to change the applicant after an original applicant has been specified under 37 CFR 1.46(b) must include a new ADS in compliance with 37 CFR 1.76 specifying the applicant in the applicant information section and comply with 37 CFR 3.71 and 3.73. See 37 CFR 1.46(c).

Any inquiries regarding this notice should be directed to the Application Assistance Unit at 571-272-4200.

Application Assistance Unit
571-272-4200

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

IMPROPER CFR REQUEST

OC000000080175733

Date Mailed: 01/29/2016

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Power of Attorney, Claims, Fees, System Limitations, and Miscellaneous

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- Any request to correct or update the name of the applicant must include an application data sheet (ADS) in compliance with 37 CFR 1.76 specifying the correct or updated name of the applicant in the applicant information section. Any request to change the applicant after an original applicant has been specified under 37 CFR 1.46(b) must include a new ADS in compliance with 37 CFR 1.76 specifying the applicant in the applicant information section and comply with 37 CFR 3.71 and 3.73. See 37 CFR 1.46(c).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/yteferra/

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Apple-Sony EX1002 Page 532

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

MISCELLANEOUS NOTICE

OC000000080175289

Date Mailed: 01/29/2016

A communication which cannot be delivered in electronic form has been mailed to the applicant.

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Apple-Sony EX1002 Page 533

Attorney Docket No. 143705.05201

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Martin U. Pralle *et al.* Application No.: 13/841,120 Filed: March 15, 2013 For: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS	Confirmation No.: 5133 Art Unit: 2814 Examiner: Long Pham

VIA EFS-WEB
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being electronically filed via EFS-Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 12, 2016 — Dated

Electronic Signature: /Andrew W. Schultz/
Andrew Schultz, Reg. No. 66,869

RESPONSE TO DENIAL OF POWER OF ATTORNEY AND UPDATED ADS

Dear Sir:

In response to the Denial of Request for Power of Attorney dated January 28, 2016, Applicant respectfully re-submits the executed Power of Attorney and the Statement Under 37 CFR 3.73(c) filed on January 13, 2016, as well as a new Application Data Sheet. Please replace the Application Data Sheet filed February 6, 2014 with the enclosed new Application Data Sheet specifying the updated name of the applicant SiOnyx, LLC. Applicant respectfully requests that an updated Filing Receipt be issued to reflect the above-referenced changes.

No charges are believed to be due with this filing. However, the Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed, or which should have

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Apple-Sony EX1002 Page 534

been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 50-0436, under Attorney Docket No.: 143705.05201.

Dated: February 12, 2016

Respectfully submitted,
Electronic Signature: /Andrew W. Schultz/
Andrew W. Schultz, Reg. No. 66,869
Attorney for Applicants
Pepper Hamilton LLP
125 High Street
19th Floor, High Street Tower
Boston, MA 02210
Tel: (617) 204-5176
Fax: (617) 204-5150

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Apple-Sony EX1002 Page 535

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Martin	U.	Pralle	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Wayland	State/Province	MA	Country of Residence	US

Mailing Address of Inventor:

Address 1	15 Rice Spring Lane		
Address 2			
City	Wayland	State/Province	MA
Postal Code	01778	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey		McKee	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Tualatin	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	22850 SW Eno Pl.		
Address 2			
City	Tualatin	State/Province	OR
Postal Code	97062	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jason		Sickler	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

IPR2025-00811
Apple-Sony EX1002 Page 536

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	

City	Arlington	State/Province	MA	Country of Residence	US

Mailing Address of Inventor:

Address 1	53 Varnum Street		
Address 2			
City	Arlington	State/Province	MA
Postal Code	02474	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

*** Customer Number	~~20551~~ 136549		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS		
Attorney Docket Number	3035-052.NP	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	(•) Customer Number	( ) US Patent Practitioner	( ) Limited Recognition (37 CFR 11.9)
*** Customer Number	~~20551~~ 136549		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13841120	reissue of	61614275	2012-03-22

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

*** Organization Name ~~SiOnyx, Inc.~~ SiOnyx, LLC.

Mailing Address Information For Applicant:

Address 1	100 Cummings Ctr.		
Address 2	Suite 243-F		
City	Beverly	**State/Province**	MA
Country US		Postal Code	01915
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Andrew W. Schultz/			Date (YYYY-MM-DD)	2016-02-12
First Name	Andrew	Last Name	Schultz	Registration Number	66869

Additional Signature may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	3035-052.NP
	Application Number	13/841,120
Title of Invention	PIXEL ISOLATION ELEMENTS, DEVICES AND ASSOCIATED METHODS	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 136549

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 136549

OR

☐

Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address: SiOnyx, LLC
100 Cummings Center, Suit 243F
Beverly, MA 01915

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	12/18/15
Name	Stephen Saylor	Telephone	508.561.4305
Title	CEO, SiOnyx LLC		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: SiOnyx, LLC

Application No./Patent No.: 9,064,764 Filed/Issue Date: June 23, 2015

Titled: PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS

SiOnyx, LLC, a Limited Liability Company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: SiOnyx, Inc.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 032782, Frame 0863, or for which a copy thereof is attached.

2. From: SiOnyx, Inc. To: SiOnyx, LLC

   The document was recorded in the United States Patent and Trademark Office at
   Reel 037449, Frame 0884, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Andrew W. Schultz/	February 12, 2016
Signature	Date
Andrew W. Schultz	66,869
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	24902642
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	20551
Filer:	Andrew W. Schultz
Filer Authorized By:	
Attorney Docket Number:	3035-052.NP
Receipt Date:	12-FEB-2016
Filing Date:	15-MAR-2013
Time Stamp:	14:27:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	ResponseDenialPOA.pdf	108141 3b4ba3d4174d37c4120b996f33475f69d17a2037	no	2

Warnings:	
Information:	

2	Application Data Sheet	ADS.pdf	142001 7b7dacb2a0cadf11971b05a02a95453550c7f86a	no	9
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3	Power of Attorney	SiOnyxGeneralPOA.pdf	135238 e9afbd7bc0956680044b1515c2efca6b59ea1bc3	no	2
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73	Statemnt37CFR373C.pdf	120217 266ec57c8f16186aeabbb7662ad9f61b0ea6f123	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	505597		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	

CONFIRMATION NO. 5133

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

POA ACCEPTANCE LETTER

OC000000080679872

Date Mailed: 02/18/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/12/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtvernon/

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	3035-052.NP

CONFIRMATION NO. 5133

20551
THORPE NORTH & WESTERN, LLP.
P.O. Box 1219
SANDY, UT 84091-1219

POWER OF ATTORNEY NOTICE

OC000000080679805

Date Mailed: 02/18/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/12/2016.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtvernon/

IPR2025-00811
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
13/841,120	03/15/2013	Martin U. Pralle	143705.05201	32178

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 01/17/2017 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Andrew W. Schultz/
Name:	Andrew W. Schultz
Registration Number:	66869

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	13/841,120
Filing Date	15-Mar-2013
First Named Inventor	Martin U. PRALLE
Title	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
Art Unit	
Examiner Name	
Attorney Docket Number	143705.000331

SIGNATURE of Applicant or Patent Practitioner

Signature	/Gunnar G. Leinberg/	Date (Optional)	2022-09-01
Name	Gunnar G. Leinberg	Registration Number	35,584
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 11951

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SiOnyx, LLC

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Steven D. Saylor		
Title	President and CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	46532726
Application Number:	13841120
International Application Number:	
Confirmation Number:	5133
Title of Invention:	PIXEL ISOLATION ELEMENTS, DEVICES, AND ASSOCIATED METHODS
First Named Inventor/Applicant Name:	Martin U. Pralle
Customer Number:	136549
Filer:	Gunnar G. Leinberg/Mary Frances Heeks
Filer Authorized By:	Gunnar G. Leinberg
Attorney Docket Number:	143705.05201
Receipt Date:	01-SEP-2022
Filing Date:	15-MAR-2013
Time Stamp:	10:41:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	20220901_Corrected_POA_with_Transmittal_143705_000331.pdf	328406 adf6f8878228c4653b61485a8dc677e73ecf6e9a	no	2

Warnings:

Information:	
Total Files Size (in bytes):	328406

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	143705.000331

CONFIRMATION NO. 5133

11951
Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

POA ACCEPTANCE LETTER

OC000000136286070

Date Mailed: 09/16/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/byemane/

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/841,120	03/15/2013	Martin U. Pralle	143705.05201

CONFIRMATION NO. 5133

136549
Pepper Hamilton LLP/SiOnyx LLC
Attn: Boston IP Docketing Department
125 High Street
19th Floor
Boston, MA 02110-2736

POWER OF ATTORNEY NOTICE

OC000000136286052

Date Mailed: 09/16/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/01/2022.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/byemane/

IPR2025-00811
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