

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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APPLE INC. AND SONY GROUP CORPORATION,

PETITIONERS

v.

SIONYX LLC,

PATENT OWNER

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*Inter Partes* Review Case No. IPR2025-00811  
U.S. Patent No. 9,064,764

**DECLARATION OF DR. STANLEY SHANFIELD, PH. D.**

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I, Dr. Stanley Shanfield, declare as follows:

## **I. INTRODUCTION**

1. I have been retained by counsels for Petitioners as a technical expert in the above-captioned case. Specifically, I have been asked to render certain opinions regarding the IPR petition with respect to U.S. Patent No. 9,064,764 (the “’764 Patent”). I understand that the Challenged Claims are 1-25, and my opinions are limited to those claims. A true and correct copy of my Curriculum Vitae, which provides further details about my background and experience, is appended to this Declaration.

### **A. *Educational Background and Professional Experience***

2. In 1977, I received a B.S. Degree in Physics *cum laude* from the University of California, Irvine. I received a Ph.D. in Physics from Massachusetts Institute of Technology in 1981.

3. After obtaining my Ph.D. in 1981, I was a Staff Scientist at Spire Corporation in Bedford, Massachusetts. Among other activities, I developed new equipment and a new method for performing low temperature silicon epitaxy using PECVD. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, among other projects, I designed and fabricated experimental Si optical sensor arrays intended for visible and near-IR government applications. This involved my efforts in numerous areas, including layout optimization, materials

growth, process development in trench RIE and doped oxide deposition and reflow, wafer-scale bonding, and scalable sensor integration with mixed signal ASICs.

4. In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300-employee, \$60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. The research portion of Raytheon's Semiconductor Operations continued to develop optical sensing array components, including with materials other than Si. I was directly involved in design and critical processing choices, sensor fabrication management, and problem-solving, and I established the direction of research investment in sensor development over several years.

5. In 1999, I co-founded and became Vice President of Operations at AXSUN Technologies in Bedford/Billerica, Massachusetts, and later became Director of Manufacturing and Wafer Fab Technology. The company's product was based on a co-patented optical sensor, which was incorporated into a miniature spectrometer for fiber optic network monitoring. The company successfully released a commercial product and was eventually acquired.

6. In 2003, I joined the Draper Laboratory in Cambridge, Massachusetts. I have been the Division Leader of Advanced Hardware Development, with around 80 staff members; a Distinguished Member of Technical Staff; and Technical Director. I led the Advanced Hardware Development division in relaunching a multi-

chip integrated circuit module facility. Among other activities, we designed, fabricated and tested flat profile optical sensor arrays for a range of star-based space navigation systems. The arrays accommodated the space radiation environment using an innovative semiconductor layout and optical design.

7. I have received many awards at Draper, including the 2015 Distinguished Performance Award and the 2010 Best Patent Award.

**B. *Materials Considered***

8. I have relied upon my education, knowledge, and experience with mobile communication devices that send and/or receive wireless signals, object-finding location systems, as well as the other materials as discussed in this declaration in forming my opinions.

9. In developing my opinions, I have considered the following materials:

|                     |                                                                                             |
|---------------------|---------------------------------------------------------------------------------------------|
| <b>Exhibit 1001</b> | U.S. Patent No. 9,064,764 (the “’764 Patent”)                                               |
| <b>Exhibit 1002</b> | File History of the ’764 Patent (the “’764 File History”)                                   |
| <b>Exhibit 1004</b> | U.S. Patent No. 7,675,099 to Hwang et al. (“Hwang-099”)                                     |
| <b>Exhibit 1005</b> | U.S. Patent Publication No. 2010/0302432 to Komuro (“Komuro”)                               |
| <b>Exhibit 1006</b> | Certified English Translation of Korean Publication No. 2003-0001795 to Hwang (“Hwang-795”) |
| <b>Exhibit 1007</b> | U.S. Patent Publication No. 2011/0019050 to Yamashita (“Yamashita”)                         |

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| <b>Exhibit 1008</b> | U.S. Patent No. 7,709,775 to Konno et al. (“Konno”)                                                                                        |
| <b>Exhibit 1009</b> | <i>Intentionally Left Blank</i>                                                                                                            |
| <b>Exhibit 1010</b> | U.S. Patent No. 7,492,027 to Mouli (“Mouli”)                                                                                               |
| <b>Exhibit 1011</b> | U.S. Patent Publication No. 2009/0194671 to Nozaki et al. (“Nozaki”)                                                                       |
| <b>Exhibit 1012</b> | U.S. Patent Publication No. 2007/0108476 to Hong (“Hong”)                                                                                  |
| <b>Exhibit 1013</b> | Certified English Translation of Korean Patent No. 10-0688584 to Hwang (“Hwang-584”)                                                       |
| <b>Exhibit 1021</b> | S. M. Sze & Kwok Kwok Ng, <u>Physics of Semiconductor Devices</u> (3 <sup>rd</sup> ed. 2007) (“Sze”)                                       |
| <b>Exhibit 1022</b> | James R. Janesick, <u>Scientific Charge-Coupled Devices</u> (2001) (“Janesick”)                                                            |
| <b>Exhibit 1023</b> | Alistair Sproul, <u>Solar Cells: Resources for the Secondary Science Teacher</u> , University of New South Wales (2003) (“Sproul”)         |
| <b>Exhibit 1024</b> | U.S. Patent Publication No. 2007/0190681 to Lee et al. (“Lee”)                                                                             |
| <b>Exhibit 1025</b> | R. Daniel McGrath, <i>Image Sensor Technology, in</i> Single-Photon Imaging 27 (Peter Seitz & Albert JP Theuwissen eds., 2011) (“McGrath”) |

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|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Exhibit 1026</b> | Christopher Shea, <i>A Silicon p-i-n detector for a hybrid CMOS imaging system</i> , Rochester Institute of Technology, <a href="https://repository.rit.edu/theses/7116">https://repository.rit.edu/theses/7116</a> (2012) (“Shea”)                                                                      |
| <b>Exhibit 1027</b> | <i>Photodiode Characteristics and Applications</i> , OSI Optoelectronics (2005) (“OSI Whitepaper”)                                                                                                                                                                                                       |
| <b>Exhibit 1028</b> | H. A. Macleod, <i>Thin-Film Optical Filters</i> (3rd ed. 2001) (“Macleod”)                                                                                                                                                                                                                               |
| <b>Exhibit 1029</b> | Misha Boroditsky, Regina Ragan & Eli Yablonovitch, <i>Absorption Enhancement in Ultra-Thin Textured AlGaAs Films</i> , 57 <i>Solar Energy Materials and Solar Cells</i> 1 (1999) (“Boroditsky”)                                                                                                          |
| <b>Exhibit 1030</b> | Jan Provoost and Piet De Moor, <i>Backside-illuminated image sensors: Optimizing manufacturing for a sensitivity payoff</i> , <a href="https://www.vision-systems.com/print/content/16744520">https://www.vision-systems.com/print/content/16744520</a> (2011, retrieved February 24, 2025) (“Provoost”) |
| <b>Exhibit 1031</b> | A. Tournier et al., <i>R 5 Pixel-to-Pixel Isolation by Deep Trench Technology: Application to CMOS Image Sensor</i> (2011) (“Tournier”)                                                                                                                                                                  |
| <b>Exhibit 1032</b> | Vyshnavi Suntharalingam, Dennis D. Rathman, Gregory Prigozhin, Steven Kissel, and Mark Bautz, <i>Back-illuminated three-dimensionally integrated CMOS image sensors for scientific</i>                                                                                                                   |

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|                     | <i>applications</i> , Proc. SPIE 6690, Focal Plane Arrays for Space Telescopes III, 669009 (2007) (“Suntharalingam”)                                                                                                              |
| <b>Exhibit 1033</b> | <i>Intentionally Left Blank</i>                                                                                                                                                                                                   |
| <b>Exhibit 1034</b> | Kyriaki Minoglou et al., <i>Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers Using Deep Trench Isolation</i> , in IEEE 2008 International Interconnect Technology Conference 129 (2008) (“Minoglou”) |
| <b>Exhibit 1035</b> | U.S. Patent No. 6,710,370 to Street et al. (“Street”)                                                                                                                                                                             |
| <b>Exhibit 1036</b> | U.S. Patent Publication No. 2004/0251513 to Su et al. (“Su”)                                                                                                                                                                      |
| <b>Exhibit 1037</b> | Maximillian A. Perez et al., <i>Rubidium Vapor Cell with Integrated Bragg Reflectors for Compact Atomic MEMS</i> , 154 Sensors and Actuators A: Physical 295 (2009) (“Perez”)                                                     |
| <b>Exhibit 1038</b> | I. H. Malitson, Interspecimen Comparison of the Refractive Index of Fused Silica*,†, J. Opt. Soc. Am. 55 (1965) (“Maltison”)                                                                                                      |
| <b>Exhibit 1039</b> | U.S. Patent Publication No. 2011/0237060 to Lee et al. (“Lee-060”)                                                                                                                                                                |
| <b>Exhibit 1040</b> | U.S. Patent No. 7,824,983 to Juengling (“Juengling”)                                                                                                                                                                              |
| <b>Exhibit 1041</b> | U.S. Patent No. 7,767,485 to Ogawa et al. (“Ogawa”)                                                                                                                                                                               |
| <b>Exhibit 1042</b> | U.S. Patent Publication No. 2009/0091806 to Inuiya (“Inuiya”)                                                                                                                                                                     |

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| <b>Exhibit 1043</b> | U.S. Patent No. 7,911,006 to Chaudhry et al. (“Chaudhry-006”)             |
| <b>Exhibit 1044</b> | U.S. Patent No. 7,595,213 to Kwon et al. (“Kwon”)                         |
| <b>Exhibit 1045</b> | U.S. Patent No. 7,141,836 to Adkisson et al. (“Adkisson”)                 |
| <b>Exhibit 1046</b> | U.S. Patent No. 7,491,610 to Chaudhry et al. (“Chaudhry-610”)             |
| <b>Exhibit 1047</b> | <i>Intentionally Left Blank</i>                                           |
| <b>Exhibit 1048</b> | <i>Intentionally Left Blank</i>                                           |
| <b>Exhibit 1049</b> | <i>Intentionally Left Blank</i>                                           |
| <b>Exhibit 1050</b> | U.S. Patent No. 6,730,896 to Yamada (“Yamada”)                            |
| <b>Exhibit 1051</b> | U.S. Patent Publication No. 2011/0083722 to Atwater et al.<br>(“Atwater”) |
| <b>Exhibit 1052</b> | <i>Intentionally Left Blank</i>                                           |
| <b>Exhibit 1053</b> | <i>Intentionally Left Blank</i>                                           |
| <b>Exhibit 1054</b> | U.S. Patent Publication No. 2011/0005575 to Cao (“Cao”)                   |
| <b>Exhibit 1055</b> | U.S. Patent No. 6,809,008 to Holm et al. (“Holm”)                         |
| <b>Exhibit 1056</b> | U.S. Patent No. 6,033,968 to Sung (“Sung”)                                |
| <b>Exhibit 1057</b> | U.S. Patent No. 4,104,086 to Bondur et al. (“Bondur”)                     |
| <b>Exhibit 1058</b> | U.S. Patent No. 6,498,336 to Tian et al. (“Tian”)                         |

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| <b>Exhibit 1059</b> | A. Crocherie, Jérôme Vaillant & F. Hirigoyen, <i>Three-Dimensional Broadband FDTD Optical Simulations of CMOS Image Sensor</i> , 29 Electronic Imaging (2008) (“Crocherie”) |
| <b>Exhibit 1060</b> | U.S. Patent No. 7,485,940 to Hsu et al. (“Hsu”)                                                                                                                             |
| <b>Exhibit 1061</b> | J. Michelot et al., <i>Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage</i> , INTERNATIONAL IMAGE SENSOR WORKSHOP (2011) (“Michelot”)             |
| <b>Exhibit 1062</b> | U.S. Patent No. 7,800,192 to Venezia et al. (“Venezia”)                                                                                                                     |
| <b>Exhibit 1063</b> | U.S. Patent Publication No. 2008/0217720 to Fan et al. (“Fan”)                                                                                                              |
| <b>Exhibit 1064</b> | U.S. Patent Publication No. 2008/0265349 to Kasano et al. (“Kasano”)                                                                                                        |
| <b>Exhibit 1066</b> | U.S. Publication No. 2010/0275984 A1 to Kaes et al. (“Kaes”)                                                                                                                |
| <b>Exhibit 1067</b> | U.S. Patent No. 6,888,214 B2 to Moulit et al. (“Moulit-214”)                                                                                                                |
| <b>Exhibit 1068</b> | U.S. Publication No. 2011/0025892 A1 to Hibbeller et al. (“Hibbeler”)                                                                                                       |
| <b>Exhibit 1069</b> | U.S. Patent No. 8,357,984 to Mao et al. (“Mao”)                                                                                                                             |
| <b>Exhibit 1070</b> | U.S. Patent No. 7,490,486 to Naumann et al. (“Naumann”)                                                                                                                     |
| <b>Exhibit 1071</b> | U.S. Patent No. 5,296,045 to Banerjee et al. (“Banerjee”)                                                                                                                   |
| <b>Exhibit 1072</b> | U.S. Patent No. 5,101,260 to Nath et al. (“Nath”)                                                                                                                           |

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|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Exhibit 1073</b> | Hitoshi Sai and Michio Kondo, <i>Effect of self-orderly textured back reflectors on light trapping in thin-film microcrystalline silicon solar cells</i> , Journal of Applied Physics, 105, 094511 (June 2009) (“Sai”) |
| <b>Exhibit 1074</b> | Shrestha Basu Mallick, et al., <i>Coherent light trapping in thin-film photovoltaics</i> , Mrs Bulletin, Volume 36 (June 2011) (“Mallick”)                                                                             |
| <b>Exhibit 1075</b> | <i>Intentionally Left Blank</i>                                                                                                                                                                                        |
| <b>Exhibit 1076</b> | U.S. Patent No. 7,135,350 to Smith et al. (“Smith”)                                                                                                                                                                    |
| <b>Exhibit 1077</b> | U.S. Patent No. 4,419,533 to Czubatji et al. (“Czubatji”)                                                                                                                                                              |
| <b>Exhibit 1078</b> | U.S. Patent No. 6,072,117 to Matsuyama et al. (“Matsuyama”)                                                                                                                                                            |

10. I have considered these materials from the viewpoint of a POSITA as of the priority date of the '764 Patent. For the purposes of this declaration, I have been asked to assume that the priority date of the '764 Patent is March 22, 2012. I note that my opinions provided in this Declaration are made from the perspective of a POSITA as of this priority date of the '764 Patent unless expressly stated otherwise. To the extent that I use any verb tense in this Declaration that is present tense (e.g., “a POSITA would understand” instead of “a POSITA would have understood”), such verb tense should be understood to be my opinion as of the '764

Patent's priority date (again, unless expressly stated otherwise). I merely use the present verb tense for ease of reading.

## **II. OVERVIEW AND LEGAL STANDARDS**

11. In formulating my opinions, I have been instructed to apply certain legal standards. I am not a lawyer. I do not offer any testimony regarding what the law is. Instead, the following sections summarize the law as I have been instructed to apply it in formulating and rendering my opinions found later in this declaration. I understand that, in an *inter partes* review (“IPR”) proceeding, patent claims may be deemed unpatentable if it is shown that they are anticipated or rendered obvious in view of the prior art. I understand that prior art in an IPR review is limited to patents or printed publications that predate the priority date of the patent at issue. I understand that questions of claim clarity (definiteness) and enablement cannot be considered as a ground for considering the patentability of a claim in these proceedings.

### **A. *Person of Ordinary Skill in the Art***

12. I understand that the '764 Patent, the record of the proceedings at the Patent Office (which I understand is called the “File History” or “Prosecution History”), and the teachings of the prior art are evaluated from the perspective of a person of ordinary skill in the art (“POSITA”). I understand that the factors considered in determining the ordinary level of skill in the art may include: (i) the

levels of education of the inventor; (ii) the types of problems encountered in the art; (iii) prior art solutions to those problems; (iv) the rapidity with which innovations are made; (v) the sophistication of the technology; and (vi) the educational level of persons working in the field.

13. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above. The hypothetical person is presumed to have the same level of skill as the typical practitioner of the art and is presumed to have knowledge of all prior art in the relevant field. I understand that the inventor's actual knowledge or lack of knowledge of prior art reference is irrelevant to the obviousness determination.

**B. *Obviousness***

14. I understand that a claim may be invalid under 35 U.S.C. § 103(a) if the subject matter described by the claim as a whole would have been "obvious" to a POSITA in view of a single or combination of prior art references at the time the claimed invention was made. I further understand that a POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent-in-suit and all analogous prior art. I understand that obviousness in an IPR review proceeding is evaluated using a preponderance of the evidence standard, which means that the claims must be more likely obvious than nonobvious.

15. I also understand that an obviousness determination includes the consideration of various factors including: (1) the scope and content of the prior art, (2) the differences between the prior art and the claim at issue, and (3) the level of ordinary skill in the pertinent art. I understand that secondary considerations of non-obviousness such as commercial success, long-felt but unresolved needs, failure of others, and so forth may be assessed as well. I have been informed that an obviousness analysis must consider the full scope of the claims to avoid impermissibly using hindsight to invalidate a patent.

16. In considering whether certain prior art renders a particular patent claim obvious, I have been informed that I can consider the scope and content of the prior art, including the fact that a POSITA would regularly look to the disclosures in patents, trade publications, journal articles, conference papers, industry standards, product literature and documentation, texts describing competitive technologies, requests for comment published by standard setting organizations, and materials from industry conferences, as examples.

17. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. A reference is analogous art if: (1) the reference is from the same field of endeavor as the claimed invention (even if it addresses a different problem); or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it

is not in the same field of endeavor as the claimed invention). For a reference to be “reasonably pertinent” to the problem, it must logically have commended itself to an inventor’s attention in considering the problem. In determining whether a reference is reasonably pertinent, one should consider the problem faced by the inventor, as reflected either explicitly or implicitly, in the specification. I believe that the documents I considered in forming my opinions in this IPR are well within the range of documents a POSITA would have consulted to address the type of problems described in the Challenged Claims.

18. I have been informed that to establish that a claimed invention was obvious based on a combination of prior art elements, an articulation of the reason(s) why a claimed invention would have been obvious must be provided. Specifically, I have been informed that the prior art, either as a single reference or a combination of multiple items of prior art, renders a patent claim obvious when there was an apparent reason for a POSITA, at the time of the invention, to combine or modify the prior art. Rationales for combining or modifying the prior art include, but are not limited to, any of the following: (A) combining prior art methods according to known methods to yield predictable results; (B) substituting one known element for another to obtain predictable results; (C) using a known technique to improve a similar device in the same way; (D) applying a known technique to a known device ready for improvement to yield predictable results; (E) trying a finite number of

identified, predictable potential solutions, with a reasonable expectation of success;  
(F) identifying that known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; or (G) identifying an explicit teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine the prior art references to arrive at the claimed invention.

19. I have also been informed that where there is a motivation to combine, claims may be rejected as obvious provided a POSITA would have had a reasonable expectation of success regarding the proposed combination. I have also been informed that common sense may be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes. I have been informed that if the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than non-obvious innovation.

20. I have been informed that the existence of an explicit teaching, suggestion, or motivation to combine known elements of the prior art is a sufficient, but not a necessary, condition to a finding of obviousness. In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose described in the patent-in-suit controls. I have been further

informed that the obviousness analysis may consider the effects of demands known to the technological community or present in the marketplace and the background knowledge possessed by a POSITA. These issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent.

21. I have been informed that it is improper to combine references where the references teach away from their combination. A reference may be said to teach away when a POSITA, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the patent applicant. I have also been informed that a reference does not teach away if it merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed.

22. I am informed that even if a case of obviousness is established, the final determination of obviousness must also consider “secondary considerations” if presented. Secondary considerations include: (a) commercial success of a product due to the merits of the claimed invention; (b) a long-felt, but unsatisfied need for the invention; (c) failure of others to find the solution provided by the claimed invention; (d) deliberate copying of the invention by others; (e) unexpected results achieved by the invention; (f) praise of the invention by others skilled in the art; (g)

lack of independent simultaneous invention within a comparatively short space of time; and (h) teaching away from the invention in the prior art.

23. I have been further informed that secondary considerations evidence is only relevant if the offering party establishes a connection, or nexus, between the evidence and the claimed invention. The nexus cannot be based on prior art features. The establishment of a nexus is a question of fact. While I understand that Patent Owner here has not offered any secondary considerations at this time, I will supplement my opinions should Patent Owner raise secondary considerations during the course of this proceeding.

### **C. *Claim Construction***

24. I understand that the claim terms in an IPR proceeding are construed according to their plain and ordinary meaning as understood in light of the claim language, the patent's description, and the prosecution history viewed from the perspective of a POSITA. I further understand that where a patent defines claim language, the definition of the patent controls, even if there are other definitions that might be understood by those working in the art.

## **III. OVERVIEW OF THE '764 PATENT**

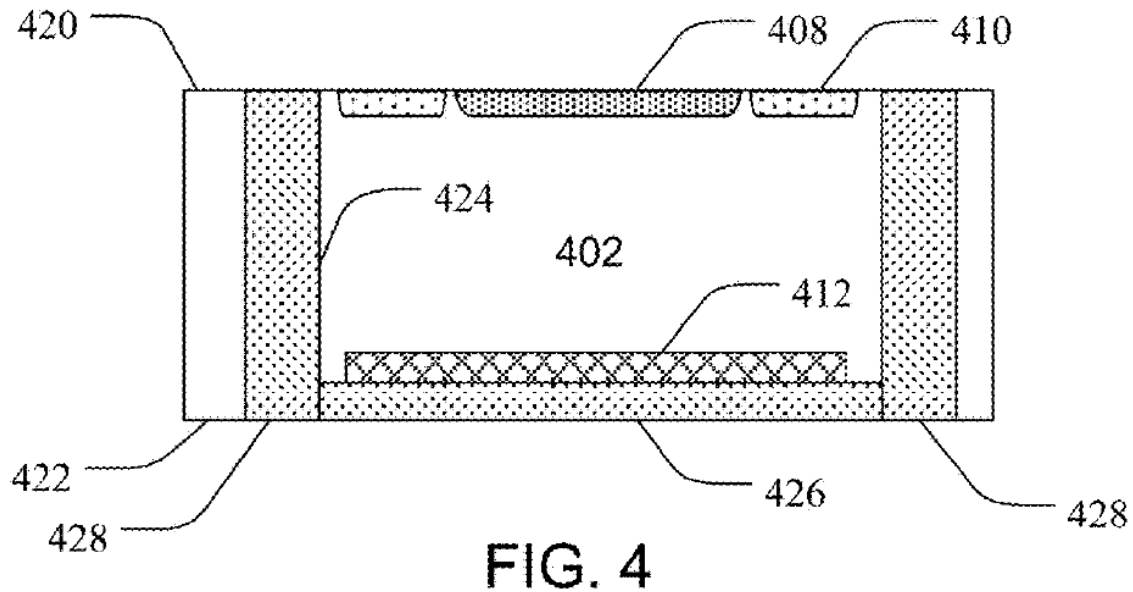
### **A. *Summary of the '764 Patent***

25. The '764 Patent describes "[l]ight trapping pixels" and "devices incorporating such pixels..." '764 Patent at Abstract. The '764 Patent utilizes "[a]

variety of light trapping materials...to trap light in a pixel[.]” *’764 Patent* at 1:52-55. For example, “a backside light trapping material substantially covering the backside surface, and a peripheral light trapping material substantially covering the peripheral sidewall[.]” and “an internally reflective frontside light trapping material[.]” *’764 Patent* at Abstract, 2:40-41. Per the *’764 Patent*, “[a] variety of light trapping materials can be utilized and are contemplated, and any such material capable of being used to trap light in a pixel is considered to be within the present scope.” *’764 Patent* at 1:52-55.

26. FIG. 4 is an exemplary light trapping pixel device having “a light sensitive pixel or device 402 having a light incident surface 420, a backside surface 422 opposite the light incident surface 420, and a peripheral sidewall 424 disposed into at least a portion of the pixel 402 and extending at least substantially around the pixel periphery.” *’764 Patent* at 10:59-64. “It is noted that the pixel sidewall is also known as a trench.” *’764 Patent* at 10:64-65. To trap light, the pixel includes “a backside light trapping material 426 substantially covering, partially covering, or completely covering the backside surface 422,” and “[a] peripheral light trapping material 428 ... substantially covering, partially covering, or completely covering the peripheral sidewall 424.” *’764 Patent* at 10:67–11:3. “As such, light contacting the backside light trapping material 426 or the peripheral light trapping material 428 is reflected back toward the pixel 402.” *’764 Patent* at 11:3-5. “Additionally, in some

cases a pixel can include a textured region to enhance the detection of infrared light among other things.” ’764 Patent at 6:29-31.



’764 Patent at FIG. 4.

27. To trap and reflect light within pixel 402, the aforementioned light trapping materials include “either single or multiple layer structures” (’764 Patent at 11:10-11), such as “a high refractive index material sandwiched between two low refractive index materials.” ’764 Patent at 1:55-58. Additionally, “the frontside light trapping material can be an antireflective layer coating[.]” ’764 Patent at 2:23-24. The ’764 Patent also recommends that “trench isolation features can be doped to further affect the properties of the material with respect to electrical isolation.” ’764 Patent at 7:63-65. Specifically, “it can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels.” ’764

*Patent* at 9:61-62. Further, either of the light incident or backside surfaces of the “semiconductor substrate” “can include at least one doped region.” *'764 Patent* at 6:47-50.

**B. *Field of Endeavor***

28. I have been informed that the field of endeavor of the claimed invention can be determined by reference to explanations of the invention’s subject matter in the patent application, including the embodiments, function, and structure of the claimed invention.

29. The *'764 Patent* generally relates to “light trapping pixels, devices incorporating such pixels, photovoltaic solar cells, and other optoelectronic devices . . .” *'764 Patent* at 1:36-28. The *'764 Patent* describes “an image sensor [that] can be capable of detecting visible and infrared light[.]” *'764 Patent* at 6:14-15. For example, “[i]n one aspect, a variety of optoelectronic devices are provided such as, without limitation, . . . imagers capable of detecting visible and infrared light[.]” *'764 Patent* at 6:32-34. The described embodiments “provide[] semiconductor devices and associated methods that can exhibit various enhanced properties, such as, for example, enhanced light detection properties.” *'764 Patent* at 5:64-67. FIGS. 1-6 depict embodiments of the *'764 Patent* that include structures for detecting light. *'764 Patent* at FIGS. 1-6, 3:19-40, 7:47-49. For these reasons, a POSITA would

understand that the field of endeavor of the '764 Patent includes semiconductor devices for detecting light.

**C. *Problem Solved by the Inventors of the '764 Patent***

30. I have been informed that a prior art reference is “reasonably pertinent” if a POSITA would have consulted it and applied its teachings when faced with the problem(s) that the inventor was trying to solve. As such, I have been asked to analyze the '764 Patent and determine the problem(s) that the inventors were trying to solve.

31. The '764 Patent recognizes problems caused by “electrical and optical cross-talk between adjacent sensor pixels....” *'764 Patent* at 1:23-32. The '764 Patent further describes that “[s]ignificant cross-talk can be generated due to reflection off the often planar back surface of the device.” *'764 Patent* at 1:30-32. The '764 Patent aims to prevent loss of light from pixels by proposing “image sensor pixels and elements for trapping light within such pixels.” *'764 Patent* at 6:1-2, 6:22-24, 7:25-51. Thus, a POSITA would have understood the '764 Patent is directed to solving the problems of reducing electrical and/or optical cross-talk between adjacent pixels and/or reducing the loss of light from each pixel.

**D. *File History of the '764 Patent***

32. The application that issued as the '764 Patent included 33 as-filed claims, including as-filed claims 1-2, 9-11, and 20-22, reproduced below:

1. A light trapping device, comprising:
  - at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
  - a backside light trapping material substantially covering the backside surface; and
  - a peripheral light trapping material substantially covering the peripheral sidewall;
  - wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.
2. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.
9. The device of claim 2, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field.
10. The device of claim 9, wherein the dopant is boron or antimony.
11. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.
20. The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface.
21. The device of claim 1, further comprising a textured layer positioned to interact with light proximal to the backside surface.
22. The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.

*'764 Patent File History* at 27-29.

33. As-filed claims 1, 12, 13, and 23 were rejected “as being anticipated by Velichko et al. (US pub 20130200251).” *'764 Patent File History* at 424. Regarding claim 1, the Examiner found that Velichko discloses:

“[A] light trapping device, comprising (see figs. 1-23 and associated text): at least one light sensitive pixel 34 having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery; a backside light trapping material 50 substantially covering the backside surface; and a peripheral light trapping material 36 substantially covering the peripheral sidewall; wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

*'764 Patent File History* at 424-425.

34. As-filed claims 2-8 and 19 were rejected “as being unpatentable over Velichko (US pub 20130200251) as applied to claims 1, 12, 13, and 23 above, and further in view of Yanagisawa (JP 403183037).” *'764 Patent File History* at 426; *see* ¶ 33. The Examiner found that Yanagisawa “teaches a reflector made of a high refractive index layer sandwiched between 2 low refractive index layers to improve reflectivity.” *'764 Patent File History* at 426. The Examiner also found that Yanagisawa teaches low and high refractive index materials having “a refractive index of less than about 2.1” and “greater than or equal to about 2.1[,]” respectively. *Id.*

35. As-filed claims 9-11 and 20-22 were “objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.” *'764*

*Patent File History* at 427. In response, Applicant amended claim 1 to include the limitations of dependent claim 9 and added independent claims 34 (drafted to include the limitations of independent claim 1 and dependent claim 11), 43 (drafted to include the limitations of independent claim 1 and dependent claim 20), and 47 (drafted to include the limitations of independent claim 1 and dependent claim 21), as shown below:

1. (currently amended) A light trapping device, comprising:

at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

a backside light trapping material substantially covering the backside surface; and

a peripheral light trapping material substantially covering the peripheral sidewall;

wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials, wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field, and

wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

34. (new) A light trapping device, comprising:

- at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

- a backside light trapping material substantially covering the backside surface; and

- a peripheral light trapping material substantially covering the peripheral sidewall,

- wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2, and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

43. (new) A light trapping device, comprising:

- at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

- a backside light trapping material substantially covering the backside surface; and

- a peripheral light trapping material substantially covering the peripheral sidewall,

- wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface, and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

47. (new) A light trapping device, comprising:

- at least one light sensitive pixel having a light incident surface, a backside surface opposite the light incident surface, and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;

- a backside light trapping material substantially covering the backside surface;

- a peripheral light trapping material substantially covering the peripheral sidewall; and

- a textured layer positioned to interact with light proximal to the backside surface, wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.

*'764 Patent File History* at 456-459. The Patent Office subsequently issued a notice of allowance. *'764 Patent File History* at 470-474.

36. As I have shown below, using a high refractive index material sandwiched between two low refractive index materials to trap light was known well prior to March 2012, as was making the difference in refractive index between the materials greater than 0.2. For example, Hwang-099, describes enclosing a pixel in backside and peripheral light trapping materials including layers of “silicon (with a refractive index of approximately 4)” sandwiched between layers of “silicon oxide (with a refractive index of approximately 1.46).” *See* ¶¶ 171-179.

37. Hong similarly teaches a pixel having a backside light trapping material with layers of high refractive index silicon sandwiched between layers of lower refractive index silicon dioxide. *See* ¶¶ 357-361. As another example, Hwang-584 describes a pixel surrounded by a peripheral light trapping material with layers of silicon with a refractive index of “around 3.7 to 5.7” sandwiched between layers of silicon dioxide with a refractive index of “around 1.46.” *See* ¶ 362. As demonstrated above, Hwang-099, Hong, and Hwang-584 also describe a difference greater than 0.2 in the refractive index between the low and high refractive index materials.

38. As I have also shown below, doping a low refractive index material, like silicon dioxide, to create a surface field in light trapping materials was similarly known before March 2012. For example, Hwang-795 describes a trench filled with

“a substance doped with P-type impurity” like “BSG (borosilicate glass)” that is then heated to form a “channel stop region (P+)[.]” See ¶¶ 181-183. As another example, Kaes describes “a boron doped silicon dioxide” on the backside surface of a “substrate” that diffuses “to form a back surface field[.]” See ¶¶ 189-190.

39. As I have also shown below, textured layers for trapping light were similarly known before March 2012. For example, Konno describes an image sensor with a transparent layer having “concaves and convexes” for improved internal reflection of light. See ¶¶ 305-308.

#### **IV. LEVEL OF A PERSON OF ORDINARY SKILL**

40. For purposes of this proceeding, I have been asked to apply the following level of ordinary skill as of March 22, 2012: “[A]t least a bachelor’s degree in electrical engineering, materials science, or physics (or an equivalent degree), at least two years of experience in optoelectronics, and at least three years of work experience in semiconductor manufacturing....[A] master’s degree or Ph.D. in a relevant field may substitute for some work experience or vice versa.” I meet this definition. When I refer to the understanding of a POSITA, I am referring to the understanding of such a person as of March 22, 2012.

#### **V. OVERVIEW OF THE TECHNOLOGY**

41. I was asked to briefly summarize the background of the prior art from the standpoint of a person having ordinary skill in the art prior to March 22, 2012.

As explained below, the image sensor technologies described by the '764 Patent were based on well-known principles of light-to-electrical signal conversion and semiconductor design. Thus, the techniques discussed in the '764 Patent were well-known and conventional prior to the invention of the '764 Patent.

**A. *Image Sensor Operation***

42. Image sensors are built on semiconductor technology, which provides the foundation for converting light into electrical signals. Semiconductors serve as the medium for photon absorption and the generation of electron-hole pairs, a foundational process in optoelectronic devices. *Sze* at p. 53 (“When light passes through a semiconductor, absorption of light and generation of electron-hole pairs (G,) occur...”). An electron-hole pair is “a carrier pair produced when a photon or particle photoelectrically interacts with a silicon atom.” *Janesick* at p. 879. “Interacting photons with sufficient energy will excite an electron into the conduction band, creating an electron-hole pair.” *Janesick* at p. 26 The pair is free to “move and diffuse in the silicon lattice structure.” *Janesick* at p. 26.

43. The structure that converts light into electron-hole pairs is known as a PN junction. A PN junction is formed by joining regions of positively doped (P-type) and negatively doped (N-type) material. *Sproul* at p. 16 (“Doping one side of a piece of silicon with boron (a p-type dopant) and the other side with phosphorus (an n-type dopant) forms a p-n junction”).

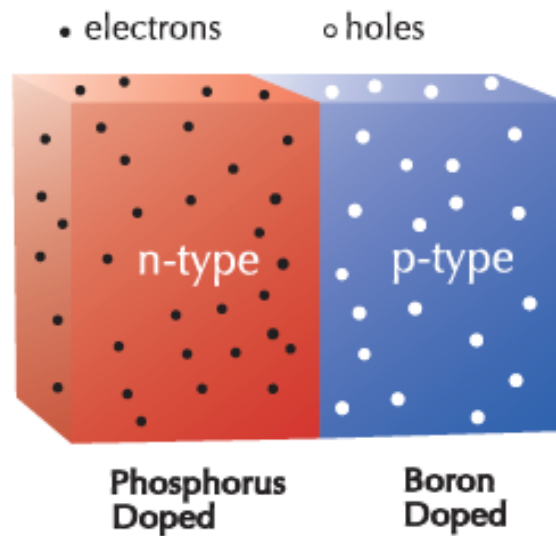
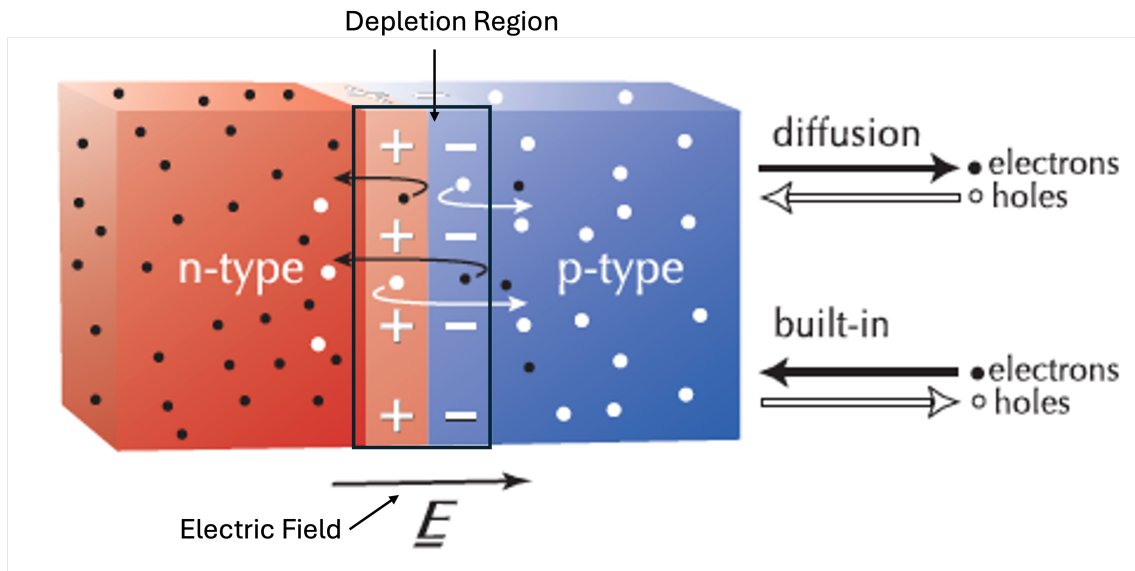


Figure 2 n-type and p-type materials brought together.

*Sproul* at p. 17.

44. A PN junction has a “depletion (or space charge region) at the junction interface [that] has a high electric field and readily separates photogenerated electron-hole pairs.” *Lee* at [0004]. As the electron-hole pairs diffuse, the electrons leave behind positively charged ions, and the holes leave behind negatively charged ions. *Sproul* at p. 18 (“As the electrons in the n-type material diffuse across towards the p-type side, they leave behind positively charged phosphorous ions. . . Similarly, the positive holes in the p-type region diffuse towards the n-type side and leave behind negatively charged boron ions...”). This process “set[s] up an electric field right at the junction between the n-type and p-type material.” *Sproul* at p. 18. The electric field “causes some of the electrons and holes to flow in the opposite direction to the flow caused by diffusion...” *Sproul* at p. 18. “These opposing flows eventually

reach a stable equilibrium” such that “the net flow of electrons across the junction is zero and the net flow of holes across the junction is also zero,” thereby forming a region depleted of mobile charges called the depletion region. *Sproul* at p. 19.



*Sproul* at p. 18.

45. The built-in electric field provided by the depletion region of the PN junction makes it such that “electrons are attracted towards the positive charge on the n-type material side” while “holes are attracted to the negative charge on the p-type material side.” *Sproul* at p. 22. “This separation of charges causes a current to flow across the junction[.]” *Sproul* at p. 22.

46. The electric field provided by the depletion region of a PN junction is essential for the generation of an electrical signal. Without it, “[e]lectrons and holes can remain excited only for a short period of time” and will undergo recombination where “excited electrons stray too close to holes and the two fall back into bonded

positions.” *Sproul* at p. 22. In such an instance, “the [electron-hole] pair’s electrical energy is lost as heat.” *Sproul* at p. 22. Thus, the separation of electron-hole pairs generates an electrical signal in image sensors.

47. This means that *both* P-type and N-type regions are needed to convert light into an electrical signal. Indeed, “[i]n a block of silicon that is not electrically biased,” (i.e., not doped) “photocarrier generation” (i.e., electron-hole pair generation) “would be balanced by an increase in recombination, providing net current neutrality.” *McGrath* at p. 33. “For an image sensor pixel, it is necessary to take advantage of the semiconductor behavior of silicon to create a region out of equilibrium (e.g., a depletion region completely drained of mobile charge carriers), so that the photocarriers can be collected before they recombine.” *McGrath* at p. 33. That is, a PN junction’s depletion region is required for electron-hole pairs to be separated.

**B. *Quantum Efficiency (QE)***

48. Quantum efficiency (QE) “is a measure of the effectiveness at converting photons into electrons.” *Shea* at p. 35. Specifically, QE “is a measure of the fraction of electrons extracted from a device per incident photon as a function of wavelength.” *Shea* at p. 25.

49. QE “varies with the wavelength of the incident light ... as well as applied reverse bias and temperature.” *OSI Whitepaper* at p. 4. QE is “related to

responsivity” of the semiconducting material. *OSI Whitepaper* at p. 5. “The responsivity of a silicon photodiode is a measure of the sensitivity to light, and it is defined as the ratio of the photocurrent to the incident light power at a given wavelength.” *OSI Whitepaper* at p. 5. The design of photodiodes directly influences QE because they affect the responsivity of the semiconductor. For example, “by controlling the thickness of the bulk substrate, the speed and responsivity of the photodiode can be controlled.” *OSI Whitepaper* at p. 2.

50. Often, anti-reflective coatings “are required for the reduction of surface reflection.” *Macleod* at p. 86. The reduction of surface reflections allows more incident light to enter the photodiode, thereby increasing the number of photons available for absorption. To further enhance the amount of light reaching the active region, optical coatings are applied in multiple layers. “Antireflection coatings can range from a simple single layer having virtually zero reflectance at just one wavelength, to a multilayer system of more than a dozen layers, having virtually zero reflectance over a range of several octave.” *Macleod* at p. 86.

51. Beyond coatings, surface texturing can be used to alter the interaction of light with the photodiode material. “A correlation between the degree of light randomization and trapping, with the scale length of the texturization geometry was found. The observed absorption enhancement corresponds to 90% of the best possible theoretical value, or 90% light randomization.” *Boroditsky* at p. 1. The

increased path length of photons within the material improves the probability of absorption, leading to greater carrier generation. “In all the textured samples, an increase in absorption was measured in comparison with the untextured films.” *Boroditsky* at p. 3.

52. The choice of semiconductor material also affects quantum efficiency, as different materials exhibit varying absorption properties across the electromagnetic spectrum. Silicon is commonly used in photodiodes due to its suitable bandgap energy. “Energy band, carrier concentration, and transport properties are briefly surveyed, with emphasis on the two most-important semiconductors: silicon (Si) and gallium arsenide (GaAs).” *Sze* at p. 1.

53. Material properties influence absorption efficiency, particularly in thin-film applications. “Amorphous silicon (a-Si) is a well-studied material for thin-film... [where] the difference between crystalline and amorphous Si is dramatic; the former has an indirect bandgap of 1.1 eV, whereas hydrogenated a-Si has an optical absorption characteristic resembles that expected for a crystal with a direct bandgap of 1.6 eV.” *Sze* at p. 88. These bandgap energies are well-suited for applications in the visible light spectral range.

54. By modifying materials and structures, photodiodes can achieve higher quantum efficiency. These methods collectively enhance the ability of the sensor to

convert incident photons into charge carriers, improving overall performance in imaging, sensing, and optical communication applications.

**C. *Backside and Frontside Illuminated Sensors***

55. The evolution of CMOS and CCD image sensors has driven the development of backside-illuminated (BSI) sensors, which outperform traditional frontside-illuminated (FSI) designs in many respects. “Backside-illuminated CMOS image sensors (BSI) capture light directly on the silicon light-sensitive layer. They have a higher sensitivity in a broader spectrum than the mainstream frontside-illuminated imagers (FSI).” *Provoost* at p. 1. The key innovation of BSI technology is its ability to optimize light absorption by repositioning the photodiode to the light-facing side of the sensor. Additionally, “in the fabrication process, after the CMOS circuitry and the interconnect layers have been created, the backside of the chip is ground and etched away until the photoactive layer is exposed. The resulting chip is very thin, sometimes below 5µm. When carefully engineered, such a sensor can improve the chance of capturing an input photon to over 90%. It will also be sensitive over a wider spectrum than is possible with FSI sensors, having a good efficiency even into the ultraviolet bands.” *Provoost* at p. 1.

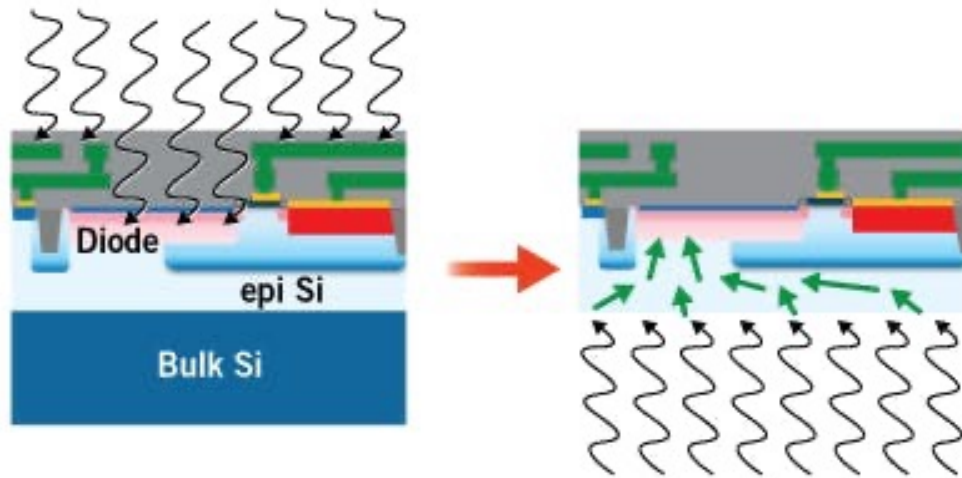


**FIGURE 2.** Schema of an FSI imager (left) and BSI imager (right).

*Provoost at Fig. 2.*

56. In FSI sensors, “incident photons must pass through the poly gates before they can interact with the epitaxial layer [and] gate absorption represents a significant QE loss mechanism, especially for photons with short absorption lengths. Reflection loss also degrades QE performance over a major portion of the working spectrum. Transmission loss is important for very long and very short wavelength photons that penetrate the epitaxial layer without interaction.” *Janesick at p. 167.* Crosstalk, both optical and electrical, poses further challenges in achieving high image fidelity. In FSI sensors, “the circuits share ground currents, which in turn causes cross-talk problems.” *Janesick at 706.* “[E]lectrical crosstalk consists in the diffusion of electrical charge (electrons or holes depending the pixel type) between adjacent pixels. It occurs in silicon material due to electrical mechanisms (diffusion

and drift).” *Tournier* at p. 1. Further, “optical crosstalk corresponds to a photon exchange between neighboring pixels before electron/holes pairs generation. It mainly appears in back-end stack due to optical mechanisms (reflection, refraction or diffraction) but can also occur in silicon substrate.” *Tournier* at p. 1.

57. BSI sensors address the challenges of FSI architecture by reversing the structure: the photodiode is positioned on the light-facing side of the sensor, while the circuitry is moved to the rear. *Tournier* at p. 8. In a back-illuminated (BSI) sensor, the chip is turned upside down, with the light falling on the backside.” *Provoost* at p. 4. “When carefully engineered, such a sensor can improve the chance of capturing an input photon to over 90%. It will also be sensitive over a wider spectrum than is possible with FSI sensors, having a good efficiency even into the ultraviolet bands.” *Provoost* at p. 4. The backside architecture significantly improves fill factor; in some cases, “a wafer-scale back-illumination process is used to achieve 100% fill factor photodiodes.” *Suntharalingam* at p. 1.

58. The unimpeded light path in BSI sensors results in higher quantum efficiency, as more photons are absorbed and converted into electrical signals and allows “the image sensor to be operated with light directly incident on the photo detector without obscuration from pixel circuitry” *Suntharalingam* at p. 2. Additionally, the BSI design is particularly advantageous in high-resolution sensors with small pixels and “permits aggressively small pixels which are 100% fill factor

after back illumination. The use of high resistivity detector tier substrates, similar to those used for scientific-grade CCDs, provides much greater spectral sensitivity.” *Suntharalingam* at p. 7.

59. BSI sensors also tackle crosstalk issues more effectively than their FSI counterparts while also “preserv[ing] the functionality of the sensor operation.” *Suntharalingam* at p. 7. Deep trench isolation (DTI) further enhances pixel isolation by confining charge carriers to their respective regions. “Comparison with other pixel isolation architectures show that Deep Trench is the best approach to suppress electrical crosstalk.” *Tournier* at p. 1. “With ... DTI integration... [c]rosstalk is extremely low and permits a great color fidelity to be achieved” *Tournier* at p. 3.

#### **D. Isolation Techniques**

60. “Deep Trench technology for CMOS image sensor was successfully developed and industrialized for best-in-class 1.4μm pixel Front-Side Illumination (FSI) technology. The performance achievements on QE both on and off-axis without any degradation of other pixel parameters show the need of a perfect pixel isolation for better color fidelity. Comparison with other pixel isolation architectures show that Deep Trench is the best approach to suppress electrical crosstalk.” *Tournier* at p. 1.

61. Shallow trench isolation (STI) is used in image sensor fabrication prior to the implementation of deep trench isolation (DTI). “DTI formation is performed

after Shallow Trench Isolation (STI) formation.” *Tournier* at p. 2. STI provides physical and electrical separation between adjacent pixels. *See e.g., Mouli-214* at 2:1-3 (“Shallow trench isolation (STI) is one technique, which can be used to isolate pixels, deices or circuitry from one another.”).

62. Despite its use in preventing pixel-to-pixel interference, using STI alone has certain limitations. “One drawback associated with shallow trench isolation in the case of CMOS image sensors is cross-talk from a photon impinging on a particular pixel of a photosensitive device causing changes that may diffuse under the shallow trench isolation structure to an adjacent pixel.” *Mouli-214* at 2:15-19. “Another drawback is that a hole accumulation layer along the sidewall of the trench is relatively small since it is limited by the depth of the shallow trenches.” *Mouli-214* at 2:19-22.

63. To address these concerns, deep trench isolation (DTI) is implemented to improve pixel separation. “Comparison with other pixel isolation architectures show that Deep Trench is the best approach to suppress electrical crosstalk.” *Tournier* at p. 2. The use of “deep trench structure” contributes to the physical isolation of pixels. *Tournier* at p. 2. These methods are also applicable to sensors with smaller pixel sizes. “This technology also permits improvement in performance of bigger pixels and will be key for 1.1µm or smaller pixels either in Front-Side or Back-side Illumination (FSI / BSI) technologies.” *Tournier* at p. 5.

64. Doped trenches enhance the functionality of isolation structures by introducing electric fields that repel charge carriers, complementing the physical isolation provided by the trench itself. For instance, “highly doped polysilicon filled high aspect ratio trenches” reduces crosstalk and enhances pixel isolation. *Minoglou* at p. 129. “By incorporating highly doped polysilicon filled high aspect ratio trenches in between pixels, a strong lateral drift field is generated. In theory, this blocks inter pixel diffusion and thus confines the collection volume to an individual pixel.” *Minoglou* at p. 129. Additionally, it is well-known that sloped sidewalls help to increase “light collection efficiency and, hence, the amount of light absorbed” by an image sensor. *Street* at 10:55-59. Further, a “sloped sidewall” provides an “advantage over vertical sidewalls” by “reducing the tendency for voids to form” in “dielectric layer deposition.” *Su* at [0035].

65. The materials used to fill isolation trenches have also evolved to improve their effectiveness in blocking both optical and electrical crosstalk. “Then standard gapfill, anneal and CMP are realized to finalize DTI formation.” *Tournier* at p. 2. “This waveguide-like structure at silicon level is due to differences in refractive index between SiO<sub>2</sub> (n=1.5 at 532nm) and Si (n=4 at 532nm).” *Tournier* at p. 3. Deep trench structures employing materials with different refractive indices serve to isolate pixels and in some cases function as “the interface Si-SiO<sub>2</sub> which is used as a wall against electron diffusion.” *Tournier* at p. 1. These materials work

alongside other light-management features, such as anti-reflective coatings, to maximize quantum efficiency.

**E. *Additional Efforts to Reduce Crosstalk***

66. The incorporation of CMOS image sensors into consumer devices, such as mobile phones and digital cameras, “led to the development of technology with pixel sizes down to  $2\mu\text{m} \times 2\mu\text{m}$ , and even sub- $1\mu\text{m}$  [1,2].” *Tournier* at p. 1. With smaller pixels, the major challenge was “the need to suppress all parasitic charge exchange between neighbouring pixels, also called crosstalk,” which “can cause a loss in image quality.” *Tournier* at p. 1. “Optical crosstalk corresponds to a photon exchange between neighbouring pixels before electron/holes pairs generation.” *Tournier* at p. 1. “[E]lectrical crosstalk consists in the diffusion of electrical charge (electrons or holes depending on the pixel type) between adjacent pixels.” *Tournier* at p. 1.

67. Another approach to mitigating optical crosstalk involves the use of Bragg reflectors. These structures have alternating layers of materials with different refractive indices, enabling control over the reflection and transmission of light through interference. “In the distributed Bragg reflector (DBR), light reflected at the interface between each layer is designed to constructively interfere to maximize the total reflected optical power at a specific wavelength.” *Perez* at p. 297. “The

reflectivity is maximized if the structure is composed of alternating layers of two materials of different indices of refractions.” *Perez* at p. 297.

68. Strategies for reducing electrical crosstalk include modifications to doping profiles, which create potential wells that confine charge carriers within individual pixels. Doping strategies provide an additional method of controlling charge carrier movement. “Starting from a conventional structure, a first solution is to isolate neighbored pixels by using dedicated P+ implants with varying energies to create a wall.” *Tournier* at p. 1. “The purpose is to optimize differently the photon collection for each color and to isolate laterally the pixels.” *Tournier* at p. 1.

#### **F. *Related Fields***

69. The principles underlying CMOS and CCD image sensors are closely connected to advancements in other optoelectronic technologies, such as solar cells and LEDs. “Solar cells which to some extent share some similarity with photodetectors in that they both convert light to electricity.” *Sze* at p. 667. These fields share fundamental processes involving the interaction of light with semiconductors to produce measurable electronic responses. “The purpose of the solar cells, however, is for power generation from the sunlight, as opposed to detection of faint light . . . [s]o one difference between them is the intensity of light involved.” *Sze* at p. 667. This similarity has fostered a transfer of knowledge and innovation between these technologies.

70. Solar cells have influenced the development of image sensors by advancing techniques for optimizing light absorption. One such advancement is the use of textured surfaces to trap and redirect light. “To reduce light reflection, a textured surface, either on the front or on the back, has been used to trap the light.” *Sze* at p. 731. By enhancing light absorption, these innovations have helped ensure that more photons reach the active region of the sensor, improving efficiency and reducing losses.

71. Anti-reflective coatings and light-trapping techniques for semiconductors have significantly influenced sensor design. “The addition of an anti-reflection coating reduces the overall reflection to a few percent.” *Sze* at p. 731. Originally developed to enhance light emission in LEDs and photon capture in solar cells, these techniques have been adapted to minimize reflection losses in CMOS and CCD sensors. “For detectors with internal photoemission, it is more efficient to direct the incoming light through the substrate. ... It is possible to choose a proper metal and antireflection coating so that a large fraction of the incident radiation will be absorbed near the surface of the semiconductor.” *Sze* at 682.

72. Multilayer anti-reflective coatings are specifically engineered to reduce unwanted reflections and maximize light transmission. If properly designed, the reflectance vectors “will completely cancel at these wavelengths, giving zero reflectance.” *MacLeod* at p. 102.

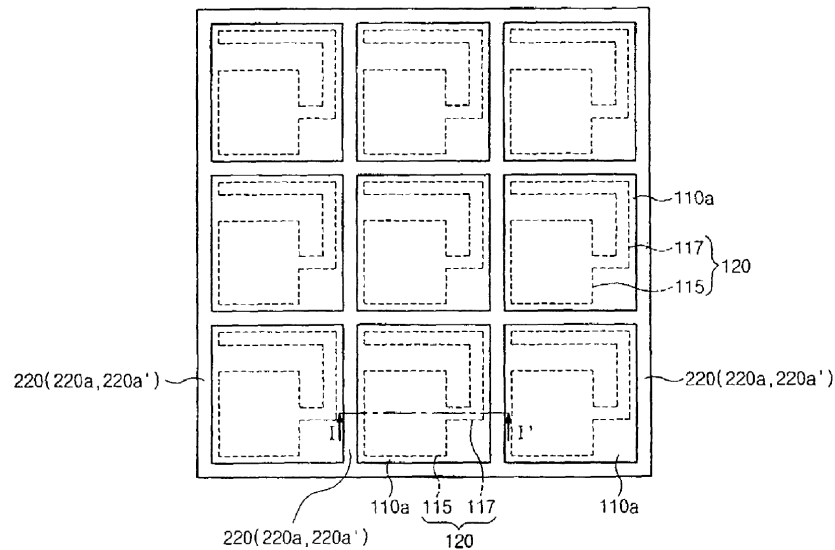
73. The anti-reflective coatings ensure that incident light is effectively directed toward the photodiode, enhancing quantum efficiency and overall sensor performance. “In optical instruments with multiple reflecting components, overall transmission is determined by the product of the reflectances of each element.” *MacLeod* at 164.

## **VI. SUMMARY OF THE PRIOR ART REFERENCES**

### **A. *Hwang-099***

74. Hwang-099 teaches “an image sensor that converts incident light into electrical signals and methods of forming the image sensor.” *Hwang-099* at 1:14-19. Hwang-099 recognizes that “there are many factors that can reduce the spectral sensitivity” and describes one example where “the amount of light absorbed by the photodiode” within an image sensor may be “reduced according to the wavelength of the light.” *Hwang-099* at 1:30-42. As such, “regions of light with a long wavelength...are likely not to be absorbed completely by the photodiode, thus reducing the spectral sensitivity.” *Hwang-099* at 1:44-47.

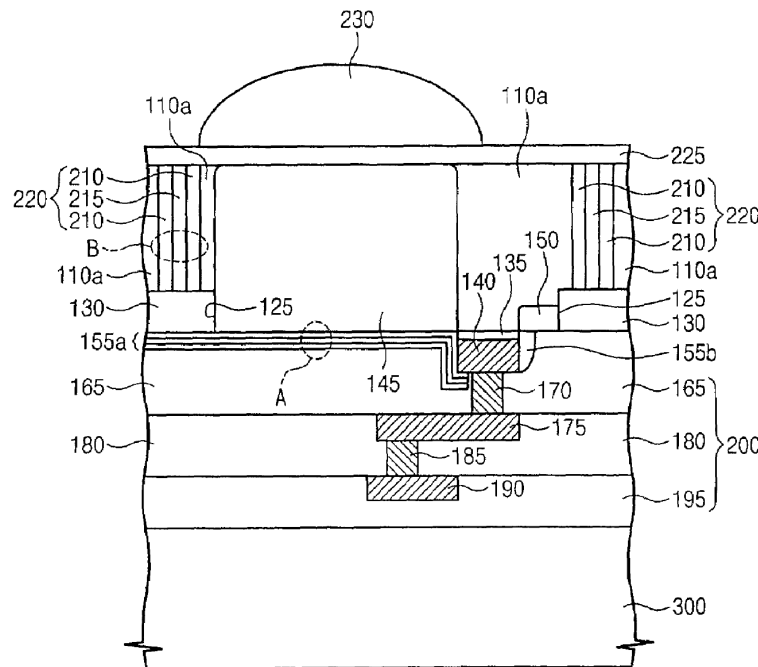
75. To solve this problem, Hwang-099 proposes an “image sensor with an increased spectral sensitivity” that is “capable of minimizing interference between neighboring pixels[.]” *Hwang-099* at 1:52-58. Hwang-099’s image sensor includes an array of pixels “arranged two-dimensionally in rows and columns on a substrate 300.” *Hwang-099* at 5:52-54.



*Hwang-099* at FIG. 1.

76. Each pixel semiconductor pattern 110a in the array is enclosed by sidewall multi-layered reflection layer 220. *Hwang-099* at 6:15-19 (“The sidewall multi-layered reflection layer 220 encloses the side walls of the pixel semiconductor patterns 110a. As shown, the sidewall multi-layered reflection layer 220 can be disposed between all of the pixel semiconductor patterns 110a.”), FIG. 1. The sidewall multi-layered reflection layer 220 includes a “plurality of layers sequentially stacked at the walls of the pixel semiconductor patterns 110a” where the layers have “different respective refractive indexes.” *Hwang-099* at 6:9-13, FIGS. 1-2. Similarly, a base multi-layered reflection layer 155a that “includes at least two stacked layers having different refractive indexes” contacts a surface of the “pixel semiconductor pattern 110a on which the photodiode 145 is formed.” *Hwang-099* at 8:32-37.

77. The base multi-layered reflection layer reflects incident light such that reflected light is “incident again on the photodiode 145,” which increases “the light sensitivity of the image sensor.” *Hwang-099* at 9:10-14. The sidewall multi-layered reflection layer 220 “minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels” and reflects light to be “incident again on the photodiode 145,” which minimizes “image distortion” and increases “absorption efficiency of incident light.” *Hwang-099* at 10:19-27, 10:31-35, 15:38-41.



*Hwang-099* at FIG. 2.

78. *Hwang-099* also teaches a micro lens 230 that “covers the photodiode 145 [and] is disposed on the color filter 225. External light passes through the micro

lens 230 and the color filter 225, and is incident on the second surface of the photodiode 145.” *Hwang-099* at 8:18-22. The positioning of Hwang-099’s micro lens 230 is such that quantum efficiency of Hwang-099’s pixel is enhanced. That is, Hwang-099 expressly teaches that “photodiodes 145 form a PN junction with the pixel semiconductor pattern 110” and are “doped at a low concentration, so that most or the entirety the photodiodes 145 become depletion regions.” *Hwang-099* at 6:3-6. Hwang-099 also states that “[w]hen external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals.” *Hwang-099* at 1:25-29. As such, a POSITA would appreciate that Hwang-099’s micro lens is strategically placed above photodiode 145, such that incident light is directed to the depletion region of the PN junction formed by photodiode 145 and pixel semiconductor pattern 110a. It was known that “electron-hole pairs that are generally formed outside of the depletion region are not separated as effectively as they would have been within the depletion region, and thus have a higher chance to recombine (which lessens the sensitivity of pixels).” *Mao* at 35-39. Thus, a POSITA would have appreciated that while pixel semiconductor pattern 110a and photodiode 145 *together* form a PN junction, having a micro lens to direct light specifically into photodiode 145 (depletion region) would advantageously increase the number of electron-hole pairs that are separated, which

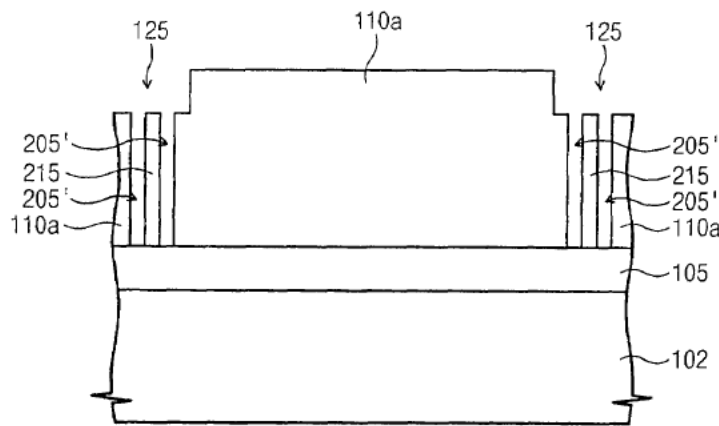
generates current, rather than undergo recombination where “no current or charge accumulation results.” *Hibbeler* at [0035].

79. To separate an electron-hole pair, a PN junction needs to be created. To create a PN junction, an N-doped material and a P-doped material are needed. To optimize incident light, it is common to place a microlens over the area comprising a depletion region, which in Hwang-099 is at least an area comprising photodiode 145. *Hwang-099* at 6:5-6. In Hwang-099, the semiconductor layer 110a is P-doped, and the photodiode formed in the layer 110a is formed by doping a portion of 110a with N+. Although the microlens could be placed over the entirety of the light incident surface of semiconductor layer 110a, the P-doped portion receiving incident light thereon is not going to be as effective in separating electron-hole pairs. Therefore, a POSITA would have understood there is no measurable advantage to extending the microlens across the entirety of layer 110a's light incident surface. On the other hand, however, pixel semiconductor layer 110a that is P-doped is needed for creation of the PN junction that facilitates the separation of the electron-hole pair. Therefore, the P-doped portion of the semiconductor layer is a pixel because it works with the N-doped, photodiode portion to create the PN junction for electron-hole pair separation.

80. FIGS. 18 and 19 represent the intermediate steps of a method of manufacturing the image sensor. Hwang-099 at 14:3-37. Regarding FIG. 18, “a first

substrate 100 having a semiconductor layer 110 is prepared, after which the semiconductor layer is patterned to form a trench 125 that restricts an active region.” *Hwang-099* at 14:3-6. After trench 125 is formed, the “floor of trench 125 is selectively etched to form a plurality of grooves 205’ that “define[] a pixel semiconductor pattern 110a.” *Hwang-099* at 14:7-9. Grooves 205’ are shown below in FIG. 18, where they are “spaced apart from one another” and a “residual portion 215 of semiconductor layer 110 is left between the grooves 205’.” *Hwang-099* at 14:10-12.

Fig. 18

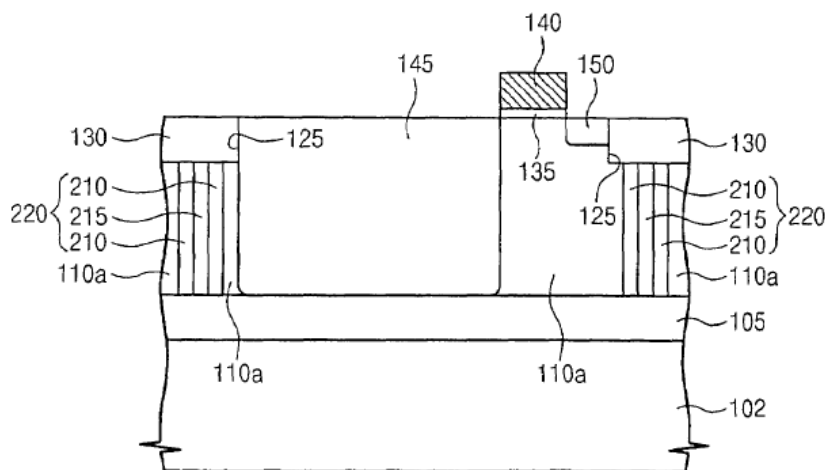


*Hwang-099* at FIG. 18.

81. The following manufacturing steps are disclosed with reference to FIG. 19, where “an oxide layer i[s] formed to fill the trench 125 and grooves 205’” such that “the portion of the oxide layer filling the trench 125 corresponds to a device isolation pattern 130, and the portion of the oxide layer filling groove 205’

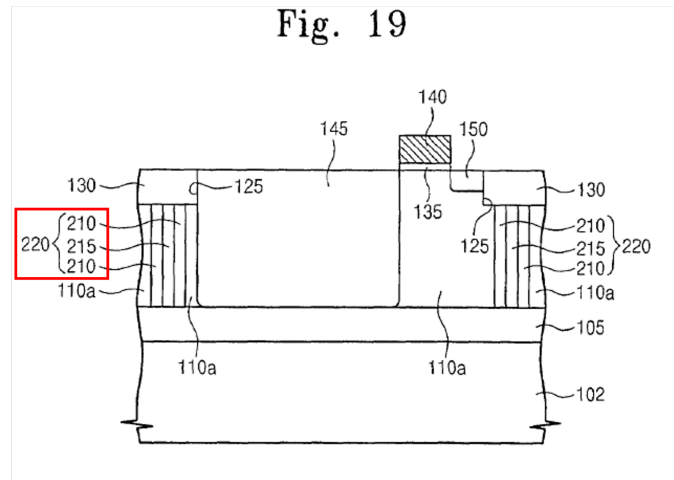
corresponds to a first sidewall reflection layer 210.” *Hwang-099* at 14:13-18. “The residual portion 215 of the semiconductor layer 110 between the grooves 205’ is a second sidewall reflection layer 215.” *Hwang-099* at 14:18-20.

**Fig. 19**



*Hwang-099* at FIG. 19.

82. The FIG. 18 and 19 method is a method describing the embodiment of FIG. 2. Indeed, *Hwang-099* expressly states that “[l]ike elements in the present embodiment use like reference numerals. *Hwang-099* at 13:61-63. I note that FIG. 19 is upside down (that is, what becomes the light incident surface of FIG. 19 is on the bottom), but as is clear from comparing FIG. 2 to FIG. 19, the reference numerals of each of the illustrated features are the same. Specifically, sidewall multi-layered reflection layer 220 (including layers 210/215), device isolation pattern 130, trench

[illegible]

83. Regarding FIG. 19, Hwang-099 expressly states that the portions of oxide filling trench 125 and grooves 205 **correspond** to device isolation pattern 130 and first sidewall reflection layer 210. *See* ¶ 81; *Hwang-099* at 14:13-18. Similarly, Hwang-099 expressly states that the residual portion 215 of semiconductor layer 110 in FIG. 19 corresponds to second sidewall reflection layer 215.” *See* ¶ 81; *Hwang-099* at 14:18-20. I note that reference numerals 210 and 215 are **only used in the FIG. 2 embodiment** of Hwang-099. *Hwang-099* at FIG. 2, FIG. 5, FIG. 6 (noting the different reference numerals used in sidewall multi-layered reflection layer 220 in FIGS. 5-6 compared to FIG. 2). Therefore, it is clear that the method of

manufacturing disclosed with reference to FIGS. 18 and 19 corresponds to the embodiment of FIG. 2.

84. I note that Hwang-099 references the use of “silicon oxide” through the specification. *Hwang-099* at 1:20-22, 4:3-4, 9:25-29, 10:2-3, 10:50-52, 11:54-55, 13:11-13. Hwang-099 teaches silicon oxide has a refractive index of “approximately 1.46” and discloses embodiments that are applicable to “external light having a long red-colored wavelength.” *Hwang-099* at 9:25-32, 10:48-55. Because Hwang-099 teaches that silicon oxide has a refractive index of 1.46, a POSITA would have understood that Hwang-099 is specifically referring to silicon dioxide because silicon dioxide has a refractive index of approximately 1.46 at the wavelength of red light. See e.g., *Maltison* at p. 1205-1206 (showing the refractive index of silicon dioxide across many wavelengths, including that of red light); *Komuro* at [0137], Table 1).

85. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

86. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Hwang-099 is directed to “an image sensor that converts incident light to electrical signals” and the embodiments described are directed to increasing the light sensitivity of an image sensor. Thus, Hwang-099 is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '764 Patent.

87. Hwang-099 is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. *See* ¶¶ 30-31. As demonstrated above, Hwang-099 describes a sidewall multi-layered reflection layer 220 that “minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels” (i.e., cross-talk). Thus, a POSITA would have consulted Hwang-099 and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

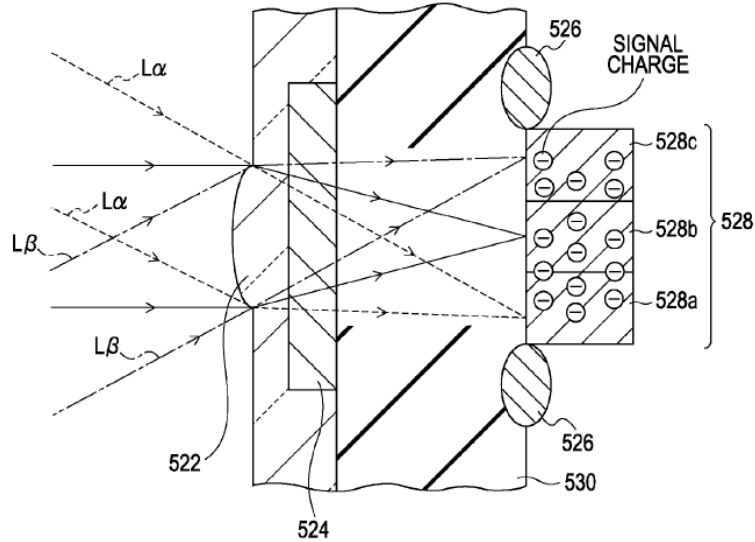
**B. *Komuro***

88. Komuro describes a “focus detection apparatus” including “first-type and second-type pixels” where “[e]ach first-type pixel includes a photoelectric converter that receives light from an image-pickup optical system...and outputs a

first charge signal corresponding to an amount of light received by the photoelectric converter[.]” (i.e., detects light). *Komuro* at Abstract. “In the first embodiment, each of the first-type pixels and the second-type pixels may further include a light-collecting unit” that “collect[s] incident light from the image-pickup optical system on the photoelectric converter.” *Komuro* at [0011]. “The first and second optical members are disposed between the light-collecting unit and the photoelectric converter” so “light from the image-pickup optical system can be efficiently collected.” *Komuro* at [0011], [0012]. *Komuro* describes that “the focus detection pixel for detecting the light  $L\alpha$  and the focus detection pixels for detecting the light  $L\beta$  can be selectively formed simply by changing the position of the boundary between the low-refractive index filter 550 and the high-refractive index filter 560.” *Komuro* at [0133].

89. “As shown in FIG. 4A, the image pickup pixel is structured such that a microlens 522, a color filter 524, element separation areas 526, the photodiode 528, and a silicon oxide film 530 are formed on a silicon substrate (not shown).” *Komuro* at [0087]. “The element separation areas 526 electrically separate the photodiode 528 from the surrounding area.” *Komuro* at [0090].

FIG. 4A



*Komuro* at FIG. 4A.

90. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

91. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, *Komuro* describes a photoelectric converter that detects light “and outputs a first charge signal corresponding to an amount of light received by the photoelectric converter.” *Komuro* at Abstract. Thus, *Komuro* is directed to the

field of semiconductor devices for detecting light and is in the same field of endeavor as the claimed invention of the '764 Patent.

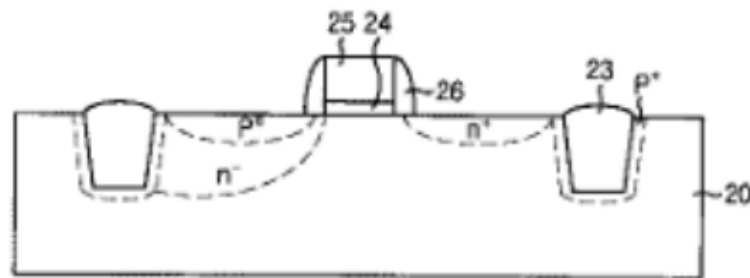
92. Komuro is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk and/or reducing loss of light. *See* ¶¶ 30-31. As demonstrated above, Komuro is similarly directed to solving problems associated with efficiently collecting light and electrical separation of a photodiode. Thus, a POSITA would have consulted Komuro and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

**C. *Hwang-795***

93. Hwang-795 recognizes that “[e]fforts are ongoing to increase the photosensitivity of image sensors,” including strategies “to increase the ratio (this is conventionally referred to as ‘fill factor’) of the photodiode-occupied area to the total area of the image sensor[.]” *Hwang-795* at [0009]. “For example, CMOS image sensors comprise photodiodes that detect light, and the part of the CMOS logic circuit that processes the detected light into electrical signals and converts them into data.” *Hwang-795* at [0009]. Specifically, Hwang-795 discloses “an image sensor that can prevent crosstalk” using “isolation between devices” using “BSG (borosilicate)” as a “field insulation film by using shallow trench isolation[.]”

*Hwang-795* at [0016], *see also, id.* at Abstract. To fabricate this image sensor, a “semiconductor layer (20)” is “etched” to form a “trench[.]” *Hwang-795* at [0026]. Then a “substance doped with P-type impurity” such as BSG “is deposited, thereby burying the trench” and forming an “STI” (shallow trench isolation) “field insulation film (23).” *Hwang-795* at [0027]. A “simple heat process is carried out” to diffuse the “doped P-type impurity inside the field insulation film (23)” to “form the channel stop region (P+).” *Hwang-795* at [0028]. *Hwang-795*’s device “minimize[s] crosstalk of data between pixels” as well as “dark current.” *Hwang-795* at [0036].

**FIG. 2c**



*Hwang-795* at FIG. 2c.

94. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

95. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Hwang-795 is directed to an image sensor that detects light. Thus, Hwang-795 is directed to semiconductor devices for detecting light and is in the same field of endeavor as the claimed invention of the '764 Patent.

96. Hwang-795 is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. *See* ¶¶ 30-31. As demonstrated above, Hwang-795 describes an “image sensor that can prevent crosstalk.” Thus, a POSITA would have consulted Hwang-795 and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

**D. *Kaes***

97. *Kaes* is directed to a “bifacial solar cell (BSC)[.]” *Kaes* at [0007]. *Kaes* acknowledges the need for “a solar cell design that achieves the benefits associated with bifacial solar cells while retaining the manufacturing simplicity of a monofacial solar cell.” *Kaes* at [0006]. To solve this problem, *Kaes* describes “a simplified manufacturing process” that includes “depositing a boron doped layer onto the back surface of a p-type silicon substrate....” *Kaes* at [0007]. “The boron doped layer

depositing step can be formed by depositing a boron doped silicon dioxide layer using CVD....” *Id.* Then, “a phosphorous diffusion step” forms “an active region” in the solar cell, and “during the phosphorous diffusion step 207, boron from region 103 is diffused into the back surface of substrate 101 to form a back surface field (BSF).” *Kaes* at Abstract, [0016], FIG. 2. The resultant “doping level of region 103, compared to substrate 101, lowers the contact resistance. Additionally, doped region 103 reduces back surface recombination and the effects of a positive potential in the back surface insulator to attract minority carriers to the back surface and thus away from the front surface collecting junction.” *Kaes* at [0013]. Finally, *Kaes*’ solar cell includes “a front surface passivation and anti-reflection (AR) dielectric layer 109[.]” *Kaes* at [0017]. Anti-reflection layers and coatings are commonly used in the art to reduce surface reflection. *See* ¶ 50.

98. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

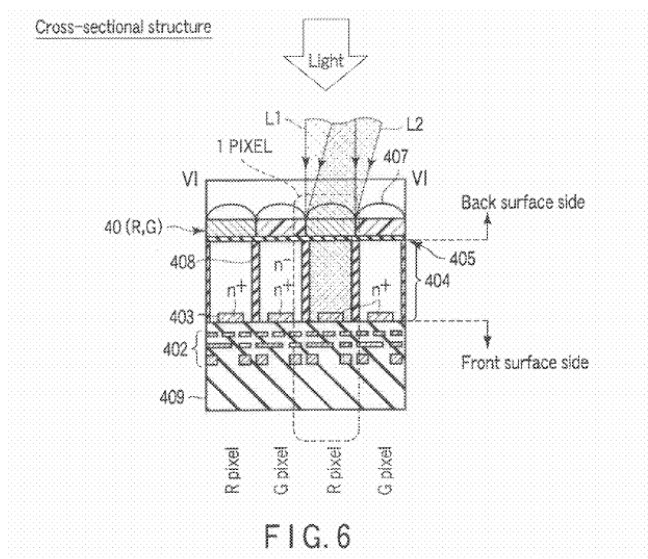
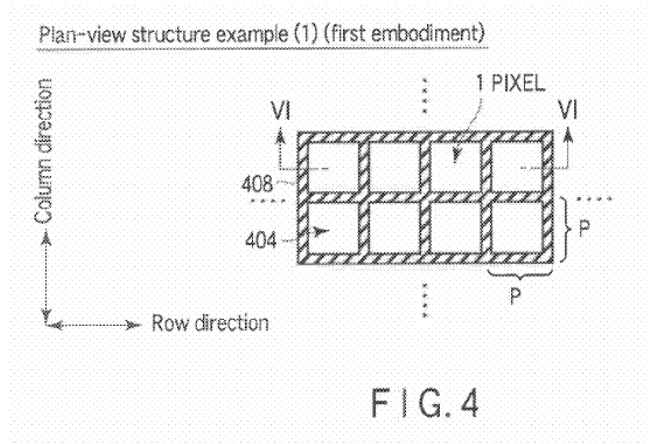
*Kaes* at FIGs. 1 and 2.

99. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As I also discussed above, the solar cell and image sensor fields are related, and the '764 Patent itself describes how “the present disclosure is applicable to other optoelectronic devices such as **solar cells**....” *'764 Patent* at 6:7-8 (emphasis added); *see also, id.*, 1:36-37; *see* ¶¶ 69-70. *Kaes* is directed to a device with a “silicon substrate,” with silicon being a well-known semiconductor material capable of carrying a “current flow[.]” *Kaes* at [0007], [0018]. Thus, *Kaes* is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '764 Patent.

100. *Kaes* is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. *See* ¶¶ 30-31. As demonstrated above, *Kaes* is concerned with solving the problem of reducing loss of light by including an “anti-reflection (AR) dielectric layer[.]” *Kaes* at [0017]. Thus, a POSITA would have consulted *Kaes* and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

**E. Yamashita**

101. Yamashita is directed to a “MOS solid-state imaging device.” *Yamashita* at [0003]. Yamashita recognizes that “if the area of the unit pixel is reduced, crosstalk increases between neighboring pixels.” *Yamashita* at [0007]; *see also, id.* at [0011] (“If the light enters the neighboring pixel beyond an inter-pixel boundary, the light causes photoelectrons in the neighboring pixel, leading to crosstalk...”). To solve this problem, Yamashita proposes a “device insulation film (insulation film) 408, which defines device isolation regions in a manner to surround boundary parts between neighboring unit pixels, is provided on the back surface of the silicon (Si) substrate 404.” *Yamashita* at [0077]; *see also, id.* at FIG. 4. “Consequently, the light, which is obliquely incident on the light-receiving region in the silicon (Si), travels in a direction toward a neighboring pixel...” *Yamashita* at [0091]. “As a result, the light causes photoelectrons in the neighboring pixel, leading to crosstalk.” *Yamashita* at [0091]. “On the other hand, as shown in FIG. 6” light that is obliquely incident “is reflected by device insulation film 408” such that “neither crosstalk nor color mixing occurs.” *Yamashita* at [0092]-[0093], *see also, id.* at [0015].



*Yamashita* at FIGS. 4 and 6.

102. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

103. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Yamashita is directed to a solid-state imaging device that detects light. Thus, Yamashita is directed to semiconductor devices for detecting light and accordingly is in the same field of endeavor as the claimed invention of the '764 Patent.

104. Yamashita is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. *See* ¶¶ 30-31. As demonstrated above, Yamashita is concerned with solving the problem of crosstalk. Thus, a POSITA would have consulted Yamashita and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

**F. *Konno***

105. Konno describes “a solid-state imaging element” including “a photoelectric conversion means which generates electric charges upon incidence of photons....” *Konno* at 2:56-58. Konno’s solid-state imaging element includes reflecting layers to “reflect incident photons,” thus improving internal reflection and absorption of light. *Konno* at 2:56-67. “The reflection parts consist of light reflective

surfaces such as mirror surfaces, and specifically, they can be formed by forming a thin film of a metal such as aluminum and silver by deposition or the like.” *Konno* at 8:35-38. Utilizing the reflective layer, “it becomes possible to return photons which go to the adjacent element to the element, and thereby reduction of cross-talk to the adjacent element and improvement of the detection efficiency...” *Konno* at 5:20-26.

106. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

107. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, *Konno* is directed to a solid-state imaging element that generates electric charges in response to incident photons. Thus, *Konno* is directed to semiconductor devices for detecting light and is in the same field of endeavor as the claimed invention of the '764 Patent.

108. *Konno* is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to

solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. *See* ¶¶ 30-31. As demonstrated above, Konno is similarly concerned with reducing cross-talk and reducing “escape of photons” (i.e., reducing loss of light). Thus, a POSITA would have consulted Konno and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

#### **G. *Mouli***

109. *Mouli* is directed to “trench isolation technology for use in semiconductor devices, including CMOS image sensors.” *Mouli* at 1:5-10. *Mouli*’s image sensor includes “a focal plane array of pixel cells, each one of the cells including a photo-conversion device for generating and accumulating charge in response to light incident on the pixel cell.” *Mouli* at 1:14-18. *Mouli* further describes that “[a]djacent pixels cells...can interfere with each other causing crosstalk,” which can “be either optical or electrical.” *Mouli* at 1:55-59. As such, *Mouli* describes a “deep trench isolation structure and method for reducing crosstalk...among adjacent photodiodes in pixel circuits.” *Mouli* at 2:49-53. A “trench 302 is etched into substrate 200, which is adjacent to photodiode region 20,” and extends “near, or directly above base layer 201” thereby forming a “deep trench.” *Mouli* at 5:50-54. An oxide, “such as silicon oxide, silicon dioxide, or other dielectric liner 304,” is “grown or deposited on sidewalls 310 but not on bottom 320

of trench 302[.]” *Mouli* at 5:60-62. A “suitable conductive material” such as “polysilicon or silicon-germanium” is “deposited to fill the trench 302.” *Mouli* at 6:11-15. The material filling the trench may also be “highly doped...n-type or p-type[.]” *Mouli* at 6:11-12. Mouli’s trench “provides improved isolation between pixels” because a deep trench “better inhibits electrons from diffusing under the isolation trench to an adjacent pixel thereby preventing crosstalk between neighboring pixels.” *Mouli* at 4:27-32. Mouli further describes a “layering structure of materials 410, 420, and 430 having different refractive indices,” which “is configured so that photons entering the trench 402 from adjacent circuitry will be reflected away from the photodiode region.” *Mouli* at 6:29-33; *see also, id.* at FIG. 5.

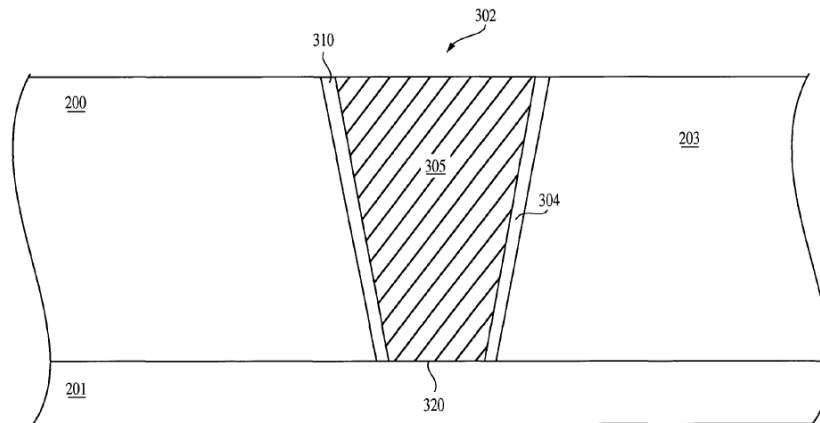


FIG. 4

*Mouli* at FIG. 4.

110. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed

invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

111. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Mouli is directed to semiconductor image sensors that detect light. Thus, Mouli is directed to semiconductor devices for detecting light and is in the same field of endeavor as the claimed invention of the '764 Patent.

112. Mouli is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. *See* ¶¶ 30-31. As demonstrated above, Mouli describes solves the crosstalk problem by utilizing deep trench isolation structures. Thus, a POSITA would have consulted Mouli and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

#### **H. *Nozaki***

113. Nozaki “relates to image sensors.” *Nozaki* at [0001]. Nozaki teaches “[a]n array of pixels” where “each pixel has...a photosensitive region formed in the

substrate.” *Nozaki* at Abstract. Nozaki describes that “[w]ith the ever-decreasing sizes of image sensors and the individual pixels that are part of a sensing array, it is important to more efficiently capture incident light[.]” *Nozaki* at [0001]. Nozaki describes that “using the backside [(e.g., underneath)] of the CMOS image sensor allows photons to be collected in an area that is relatively unobstructed[.]” *Nozaki* at [0016]. “A backside illuminated (BSI) image sensor can be made by thinning the silicon substrate,” but “when thinning the substrate of the image sensor, a tradeoff between the sensitivity of the pixel and crosstalk (with adjacent pixels) is encountered.” *Nozaki* at [0017]-[0018]. Nozaki further describes that “[w]ithin each pixel of the imaging device, some of the incident light is absorbed before reaching the active photodiode of the pixel and some of the incident light passes through without being absorbed in the photodiode.” *Nozaki* at [0018].

114. “A reflector helps to redirect the unabsorbed light towards the photodiode” which “increases the sensitivity of the photodiode and reduces crosstalk and blooming effects.” *Nozaki* at [0018]. Accordingly, Nozaki teaches “an array of pixels” where “each pixel has a photodiode and a reflector.” *Nozaki* at [0019]. Nozaki’s reflector 270 is shown below in FIG. 2, where “light is reflected by reflector 270” and “is directed towards photodiode 207 to be absorbed (e.g., detected).” *Nozaki* at [0033], *see also, id.* at [0036].

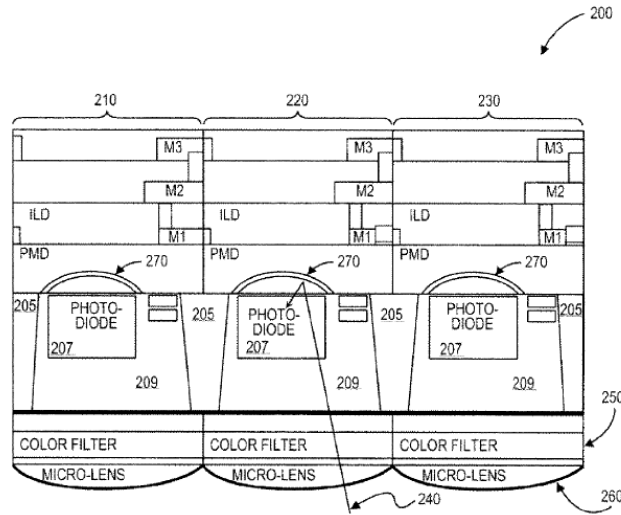


**FIG. 2**

*Nozaki* at FIG. 2.

115. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

116. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, *Nozaki* is directed pixels having a photodiode for detecting light. Thus, *Nozaki* is directed to semiconductor devices for detecting light and is in the same field of endeavor as the claimed invention of the '764 Patent.

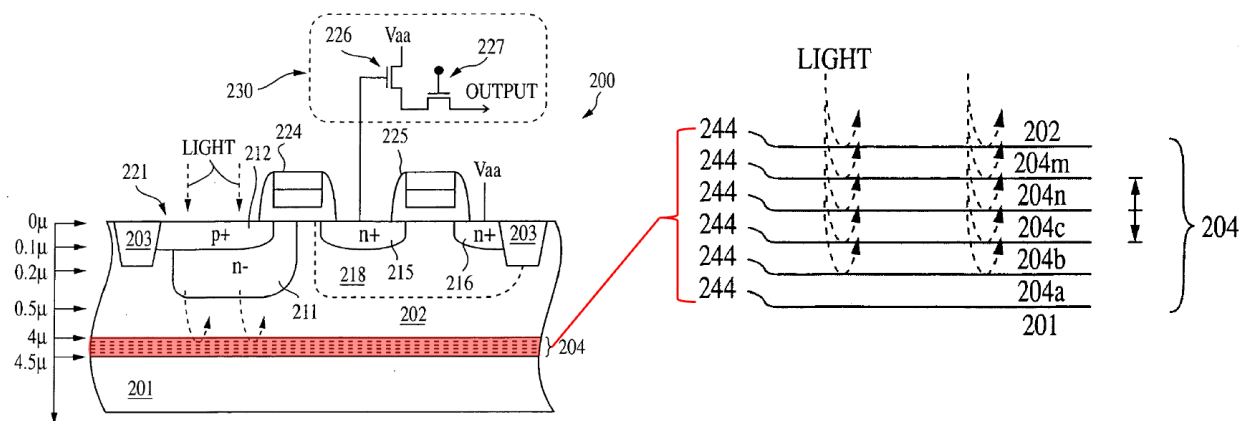
117. Nozaki is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. See ¶¶ 30-31. As demonstrated above, Nozaki describes a reflector that redirects incident light to the photodiode which reduces crosstalk. Thus, a POSITA would have consulted Nozaki and applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

#### **I. *Hong***

118. Hong relates to “semiconductor devices, particularly to an image sensor pixel with improved quantum efficiency and reduced cross talk.” *Hong* at [0001], [0017]. Hong describes that “[i]n the conventional pixel 10, when incident light strikes the surface of the photodiode 21, charge carriers (electrons), are generated...” *Hong* at [0005]. Hong recognizes that in conventional pixels, “a large amount of incident light of longer wavelengths will not be absorbed in the photodiode 21 leading to decreased quantum efficiency.” *Hong* at [0005], FIG. 1. “In order to capture light absorbed deep in the substrate 1, the depletion region of the photodiode 21 would have to be very deep, e.g., tens of microns deep.” *Hong* at [0005]. “Such a design, however, can lead to increased cross talk, where charge carriers from one pixel travel to adjacent pixels.” *Hong* at [0005]. Hong acknowledges the need for “a

pixel that can capture longer wavelengths of light, e.g., 650-750 nm or longer, with improved quantum efficiency and without increased cross talk.” *Hong* at [0005].

119. To solve this problem, *Hong* describes “an imager pixel comprising a reflective layer formed over a substrate.” *Hong* at [0006], [0047]. As shown below, *Hong*’s imager pixel 200 includes, among other things, a reflective layer 204, which is “a Distributed Bragg Reflector (DBR) mirror including sub-layers 204a, 204b, 204c, 204n, and 204m.” *Hong* at [0023].



*Hong* at FIGS. 2-3 (annotated).

120. *Hong* also teaches that the sub-layers are made of different materials having different refractive indices. *Hong* at [0024]-[0025]. In one example, “sub-layers 204b and 204n are silicon (Si) and sub-layers 204a, 204c, and 204m are silicon-germanium ( $\text{Si}_x\text{Ge}_{1-x}$ ), such that reflective layer 204 has an  $\text{Si}_x\text{Ge}_{1-x}/\text{Si}$  structure.” *Hong* at [0024]. In another example, “sub-layers 204b and 204n are Si and sub-layers 204a, 204c, and 204m are  $\text{SiO}_2$ , such that reflective layer 204 has an

SiO<sub>2</sub>/Si structure.” *Hong* at [0024]. Per *Hong*, “the quantum efficiency of the pixel 200 is increased as compared to a conventional pixel 10” and “cross talk can be reduced as reflected light will not travel to adjacent pixels.” *Hong* at [0026].

121. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

122. As discussed above, the field of endeavor of the claimed invention of the '764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, *Hong* is directed to a semiconductor image sensor that detects light. Thus, *Hong* is directed to semiconductor devices for detecting light and is in the same field of endeavor as the claimed invention of the '764 Patent.

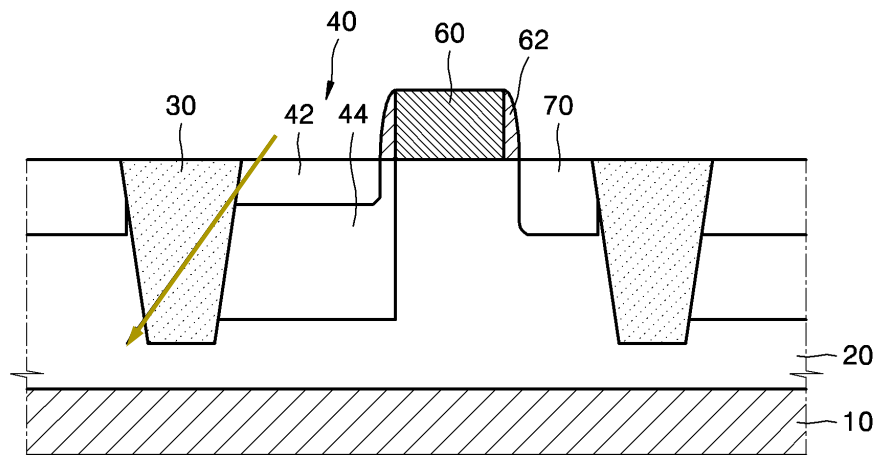
123. *Hong* is also reasonably pertinent to the problems solved by the inventors of the '764 Patent. As discussed above, the '764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels. and/or reducing loss of light *See* ¶¶ 30-31. As demonstrated above, *Hong* describes solving the problem of cross talk so that “reflected light will not travel to adjacent pixels.” Thus, a POSITA would have consulted *Hong* and applied

its teachings when faced with the reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

**J. *Hwang-584***

124. Hwang-584 describes that “an image sensor is a semiconductor device that converts optical image into electric signals.” *Hwang-584* at [0002]. Hwang-584 recognizes “[a] conventional image sensor...has the problem of crosstalk (CT) phenomenon between adjacent pixels which occurs when light entering in the direction of the arrow penetrates the device separation membrane (30) and generates electron-hole pair on the adjacent pixel” as shown below. *Hwang-584* at [0009], FIG. 1, *see also, id.* at Abstract, [0011].

Figure 1



*Hwang-584* at FIG. 1 (annotated).

125. Therefore, “light penetrating the device separation membrane and permeating into to an adjacent pixel creates the problem of reducing photodiode sensitivity.” *Hwang-584* at [0009]. Further, “red light entails deep permeation” which can “create electron-hole pair on epitaxial layer (20), becoming a causal factor for occurrence of CT phenomenon through the epitaxial layer (20) connected to an adjacent pixel.” *Hwang-584* at [0010].

126. To solve this problem, *Hwang-584* describes “forming the device separation membrane (300) using two different materials having different refractive indices, the reflectance of the device separation membrane may be raised, thereby allowing it to block permeation of side light from entering into an adjacent pixel.” *Hwang-584* at [0020], FIG. 2. “Also, the device separation membrane (300) should preferably be formed proximal to the substrate (100) to prevent CT phenomenon through the epitaxial layer (200).” *Hwang-584* at [0021].

127. In one example, device separation membrane 300 is formed with “a silicon dioxide membrane (320) and a silicon membrane (340).” *Hwang-584* at [0025], FIG. 3a. In another example, “device separation membrane (300a) [is] formed with another pair of different materials.” *Hwang-584* at [0026], FIG. 3b. Specifically, “the membranes of two different materials are the air layers (320a) and the silicon membrane (340a) between the air layers.” *Id.* Per *Hwang-584*, the

“difference between the refractive indices is 2.2 or more, allowing high reflectance in a device separation membrane (300)....” *Id.*

128. I have been informed that for a prior art reference to be proper for use in an obviousness analysis, the reference must be “analogous art” to the claimed invention. I have been informed that a prior art reference is analogous to the claimed invention if the reference is from the same field of endeavor as the claimed invention or if it is reasonably pertinent to the particular problem that the inventor was trying to solve.

129. As discussed above, the field of endeavor of the claimed invention of the ’764 Patent includes semiconductor devices for detecting light. *See* ¶¶ 28-29. As demonstrated above, Hwang-584 is directed to a semiconductor device that detects light and is in the same field of endeavor as the claimed invention of the ’764 Patent.

130. Hwang-584 is also reasonably pertinent to the problems solved by the inventors of the ’764 Patent. As discussed above, the ’764 Patent is directed to solving the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. *See* ¶¶ 30-31. As demonstrated above, Hwang-584 solves the problem of cross talk between adjacent pixels by forming a device separation membrane (300) using two different materials having different refractive indices, thereby allowing it to block permeation of side light from entering into an adjacent pixel. Thus, a POSITA would have consulted Hwang-584 and

applied its teachings when faced with the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light.

## VII. SUMMARY OF UNPATENTABILITY

131. I have reproduced the Proposed Grounds of Unpatentability from the Petition for ease of reference:

| Ground | Grounds of Unpatentability                                                                                      |
|--------|-----------------------------------------------------------------------------------------------------------------|
| 1      | Claims 1-5, 7 are obvious over Hwang-099 (Ex. 1004), Hwang-795 (Ex. 1006), and Kaes (Ex. 1066)                  |
| 2      | Claim 6 is obvious over Hwang-099, Hwang-795, Kaes, and Konno (Ex. 1008)                                        |
| 3      | Claims 8-12, 14-15 are obvious over Hwang-099                                                                   |
| 4      | Claim 13 is obvious over Hwang-099 and Komuro (Ex. 1005)                                                        |
| 5      | Claims 17-19 are obvious over Hwang-099 in combination with Mouli (Ex. 1010) and/or Nozaki (Ex. 1011)           |
| 6      | Claim 20 is obvious over Hwang-099 and Konno in combination with Mouli and/or Nozaki                            |
| 7      | Claims 16, 21-25 are obvious over Hwang-099 in combination with Konno                                           |
| 8      | Claims 1-5, 7 are obvious over Hong (Ex. 1012), Yamashita (Ex. 1007), Hwang-584 (Ex. 1013), Hwang-795, and Kaes |
| 9      | Claim 5 is obvious over Hong, Yamashita, Hwang-584, Hwang-795, Kaes, and Mouli                                  |
| 10     | Claim 6 is obvious over Hong, Yamashita, Hwang-584, Hwang-795, Keas, and Konno                                  |
| 11     | Claims 8-12, 14-15 are obvious over Hong, Yamashita, and Hwang-584                                              |
| 12     | Claim 13 is obvious over Hong, Yamashita, Hwang-584, and Komuro                                                 |
| 13     | Claims 17-19 are obvious over Hong, Yamashita, and Hwang-584 in combination with Mouli and/or Nozaki            |
| 14     | Claim 20 is obvious over Hong, Yamashita, Hwang-584, and Konno in combination with Mouli and/or Nozaki          |

|    |                                                                         |
|----|-------------------------------------------------------------------------|
| 15 | Claims 16, 21-25 are obvious over Hong, Yamashita, Hwang-584, and Konno |
|----|-------------------------------------------------------------------------|

# **VIII. GROUND 1: CLAIMS 1-5 AND 7 ARE OBVIOUS OF HWANG-099, HWANG-795, AND KAES**

## **A. *1[Pre]: “A light trapping device, comprising:”***

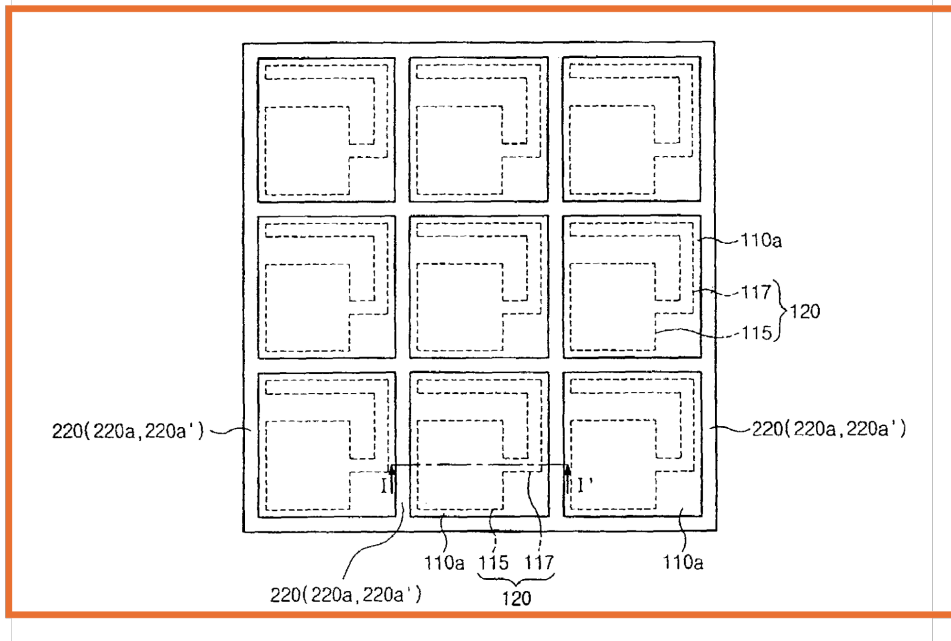
132. Hwang-099 describes an “image sensor capable of minimizing interference between neighboring pixels...” *Hwang-099* at 1:55-57, 1:14-18. A “plan view of an image sensor,” including an array of “neighboring pixels,” is illustrated in FIG. 1. *Hwang-099* at 4:59-63, 1:56-57, 3:20-26. For the reasons explained below, the image sensor of FIG. 1 is a *light trapping device*:<sup>1</sup>

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<sup>1</sup> I have emphasized and color-coded the claim elements for clarity.

## Light Trapping Device

Fig. 1



*Hwang-099* at FIG. 1 (annotated).

133. *Hwang-099*'s image sensor includes "a plurality of pixel semiconductor patterns 110a" that are "arranged two-dimensionally in rows and columns on a substrate 300." *Hwang-099* at 5:47-54, FIG. 1. Each semiconductor pattern 110a is surrounded by a sidewall multi-layered reflection layer 220. *Hwang-099* at 6:7-9 ("A sidewall multi-layered reflection layer 220 is provided between the side walls of the pixel semiconductor patterns 110a."), 6:17-23 ("As shown, the sidewall multi-layered reflection layer 220 can be disposed between all of the pixel semiconductor patterns 110a. That is, the sidewall multi-layered reflection layer 220 can be disposed along the boundaries of all of the pixel semiconductor patterns 110a, and

all of the pixel semiconductor patterns 110a can thus be separated by the sidewall multi-layered reflection layer 220.”), FIG. 1.

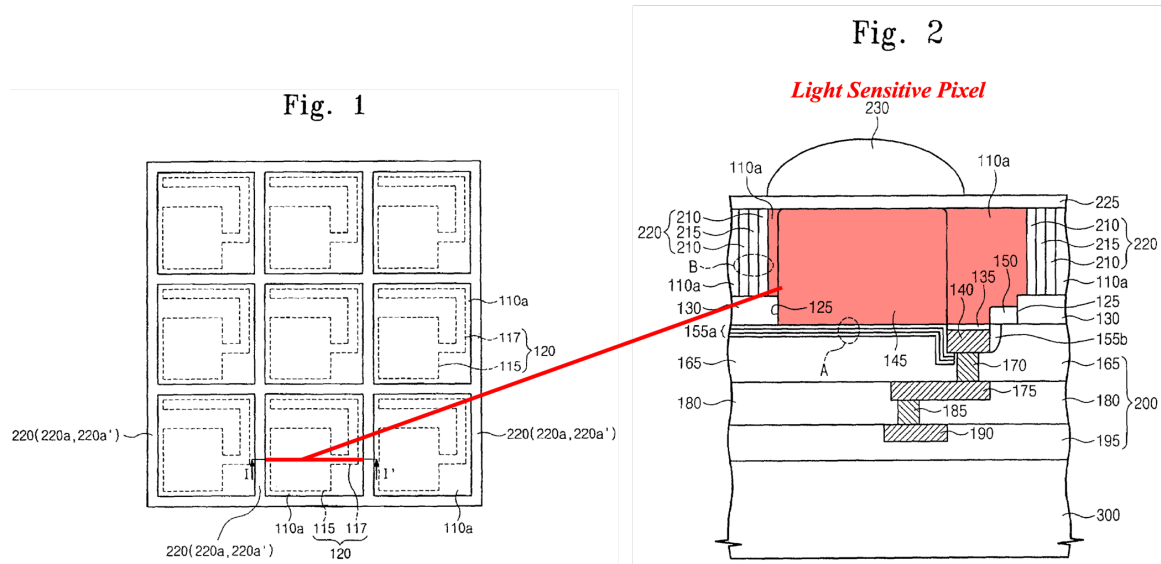
134. “The sidewall multi-layered reflection layer 220 minimizes incidence of the light ... on the photodiode 145 within another pixel semiconductor pattern 110a.” *Hwang-099* at 10:19-23. “In other words, the sidewall multi-layered reflection layer 220 minimizes incidence of the light incident on a photodiode 145 that it encloses being incident on other pixels.” *Hwang-099* at 10:23-26. Thus, Hwang-099’s image sensor traps light by reflecting it back into each individual pixel. *Hwang-099* at 10:31-35 (“As a result, the portion of the light reflected toward the sidewall multi-layered reflection layer 220 from the light reflected by the first and second boundary surfaces is incident again on the photodiode 145, so that the absorption efficiency of external light is increased.”). I note that this is similar to the ’764 Patent, which describes trapping light by reflecting it back into the pixel. ’764 *Patent* at 11:3-5 (“As such, light contacting the backside light trapping material 426 or the peripheral light trapping material 428 is reflected back toward the pixel 402.”). Therefore, Hwang-099’s image sensor is a *light trapping device*.

**B. 1[a]: “at least one *light sensitive pixel*”**

135. As I discussed above, Hwang-099’s image sensor includes an array of “neighboring **pixels**” that are “arranged two-dimensionally in rows and columns on

a substrate 300.” *Hwang-099* at 1:55-57<sup>2</sup>, 5:52-58, FIG. 1; *see also*, Claim 1[Pre].

“FIG. 2 is a sectional view of FIG. 1 taken along line I-I” and depicts *at least one light sensitive pixel*, which at least includes photodiode 145 and pixel semiconductor pattern 110a:



*Hwang-099* at FIGS. 1-2 (annotated); *see also, id.* at 4:61-62.

136. The silicon pixel semiconductor pattern 110a is “doped with a first conductive dopant” that is “a P-type dopant.” *Hwang-099* at 5:58-64. Photodiode 145 is a region in pattern 110a “doped with a second conductive dopant” that is “an

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<sup>2</sup> All emphases are added unless noted otherwise.

N-type dopant.” *Hwang-099* at 5:59-65.<sup>3</sup> “Therefore, the photodiodes 145 form a PN junction with the pixel semiconductor pattern 110a.” *Hwang-099* at 6:3-4.

137. As I discussed above, a PN junction facilitates converting light into an electrical signal by separating electron-hole pairs that causes generation of a charge, which is then stored in circuitry that will allow it to be accessed as a signal. *See ¶¶ 43-47.* A PN junction has a “depletion (or space charge region) at the junction interface [that] has a high electric field and readily separates photogenerated electron-hole pairs.” *See e.g., Lee* at [0004]. Due to the depletion region’s electric field, “electrons are attracted towards the positive charge on the n-type material side[,]” while “holes are attracted to the negative charge on the p-type material side.” *See e.g., Sproul* at p. 22.

138. *Hwang-099* confirms that photodiode 145 is “doped at a low concentration, so that most of the entirety of the photodiodes 145 become depletion regions.” *Hwang-099* at 6:4-6. “When external light is incident on a depletion region

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<sup>3</sup> Because photodiode 145 is a “region doped...within a predetermined region of a pixel semiconductor pattern 110a,” photodiode 145 is not a separate structure from pattern 110a. *Hwang-099* at 5:60-63. Instead, the box surrounding photodiode 145 in FIG. 2 merely delineates the locations of the P-type and N-type dopants within the silicon substrate. In other words, photodiode 145 and pattern 110a are a single, contiguous layer of silicon having different doped regions.

in the photodiode, electron-hole pairs are generated, and the **external light is converted to electrical signals.**” *Hwang-099* at 1:23-29.

139. Hwang-099 also teaches a micro lens 230 that “covers the photodiode 145 [and] is disposed on the color filter 225. External light passes through the micro lens 230 and the color filter 225, and is incident on the second surface of the photodiode 145.” *Hwang-099* at 8:18-22. The positioning of Hwang-099’s micro lens 230 is such that quantum efficiency of Hwang-099’s pixel is enhanced. That is, Hwang-099 expressly teaches that “photodiodes 145 form a PN junction with the pixel semiconductor pattern 110” and are “doped at a low concentration, so that most or the entirety the photodiodes 145 become depletion regions.” *Hwang-099* at 6:3-6. Hwang-099 also states that “[w]hen external light is incident on a depletion region in the photodiode, electron-hole pairs are generated, and the external light is converted to electrical signals.” *Hwang-099* at 1:25-29. As such, a POSITA would appreciate that Hwang-099’s micro lens is strategically placed above photodiode 145, such that incident light is directed to the depletion region of the PN junction formed by photodiode 145 and pixel semiconductor pattern 110a. It was known that “electron-hole pairs that are generally formed outside of the depletion region are not separated as effectively as they would have been within the depletion region, and thus have a higher chance to recombine (which lessens the sensitivity of pixels).” *Mao* at 3:35-39. Thus, a POSITA would have appreciated that while pixel

semiconductor pattern 110a and photodiode 145 *together* form a PN junction, having a micro lens to direct light specifically into photodiode 145 (depletion region) would advantageously increase the number of electron-hole pairs that are separated, which generates current, rather than undergo recombination where “no current or charge accumulation results.” *Hibbeler* at [0035].

140. To separate an electron-hole pair, a PN junction needs to be created. To create a PN junction, an N-doped material and a P-doped material are needed. To optimize incidence of light, it is common to place a microlens over the area comprising a depletion region, which in Hwang-099 is at least an area comprising photodiode 145. *Hwang-099* at 6:5-6. In Hwang-099, the semiconductor layer 110a is P-doped, and the photodiode formed in the layer 110a is formed by doping a portion of 110a with N+. Although the microlens could be placed over the entirety of the light incident surface of semiconductor layer 110a, the P-doped portion receiving incident light thereon is not going to be as effective in separating electron-hole pairs. Therefore, a POSITA would have understood there is no measurable advantage to extending the microlens across the entirety of layer 110a's light incident surface. On the other hand, however, pixel semiconductor layer 110a that is P-doped is needed for creation of the PN junction that facilitates the separation of the electron-hole pair. Therefore, the P-doped portion of the pattern 110a is a pixel

because it works with the N-doped, photodiode 145 portion to create the PN junction for electron-hole pair separation.

141. For these reasons, Hwang-099's *light sensitive pixel* includes a PN junction formed by photodiode 145 and pixel semiconductor pattern 110a that converts light into an electrical signal.

142. Further, as I discuss in more detail below, Hwang-099 teaches a "sidewall multi-layered reflection layer 220" that contacts a "pair of neighboring pixel semiconductor patterns 110a." *Hwang-099* at 10:14-17; ¶¶ 159-169. Sidewall multi-layered reflection layer 220 is expressly described as "enclosing" pixel semiconductor patterns 110a. *Hwang-099* at 3:38-40, 6:15-17. Sidewall multi-layered reflection layer 220 comprises "boundary surfaces" that minimize incidence of light on a neighboring photodiode 145 (disposed in pixel semiconductor pattern 110a. *Hwang-099* at 10:19-27. "Thus, the occurrence of interference between **neighboring pixels** can be minimized." *Hwang-099* at 10:18-19, 1:55-58. A POSITA would have understood that because 1) Hwang-099 describes sidewall multi-layered reflection layer 220 as enclosing pixel semiconductor patterns 110a, and 2) sidewall multi-layered reflection layer 220 minimizes interference between neighboring **pixels**, that Hwang-099's pixel semiconductor pattern 110a is a *pixel*. Collectively reading Hwang-099's teachings of an image sensor comprising an array of pixel semiconductor patterns 110a separated by a reflection layer 220 to minimize

incident light on “neighboring pixels,” a POSITA would have understood the pixel semiconductor pattern 110a is a *pixel* because patterns 110a form the “neighboring pixels” separated by sidewall layer 220.

**C. *1[a][i]: “having a light incident surface, a backside surface opposite the light incident surface,”***

143. Per the '764 Patent, “a device can include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side.” '764 Patent at 6:47-49; *see also, id.* at 13:20-21 (describing “...the top surface (i.e. the light incident surface)...”). Hwang-099 similarly teaches that pixel semiconductor pattern 110a and photodiode 145, which is “disposed” within pattern 110a, have “first and second surfaces in parallel, i.e., that face one another” and where “the first surface of a pixel semiconductor pattern 110a is more proximate to the substrate 300 than is the second surface.” Hwang-099 at 5:57-58, 6:37-40; *see also, id.* at 6:61-65 (“The photodiode 145 also has a first surface and a second surface that face each other. Here, the first surface of the photodiode 145 is coplanar with the first surface of the pixel substrate pattern 110a.”). As shown in the annotated figure, below, at least a portion of the first surface on the bottom of pattern 110a/photodiode 145 is a *backside surface* of the *pixel*, and at least a portion of the second surface on the top of pattern 110a/photodiode 145 is a *light incident surface* of the *pixel*:

A detailed cross-sectional view of a light-emitting device. The device features a top layer (110a) with a central dome-shaped structure (230). A red rectangular region (125) is located within the device, representing the light-emitting layer. A blue line (140) indicates the light incident surface, and a green line (145) indicates the backside surface. The device is mounted on a substrate (300) and includes various layers and structures labeled with reference numerals: 110a, 125, 130, 135, 140, 145, 150, 155a, 155b, 165, 170, 175, 180, 185, 190, 200, 210, 215, 220, 225, 230, and 300. A dashed line (A) indicates a cross-section through the device, and a dashed line (B) indicates a cross-section through the light-emitting layer.

144. While Hwang-099 acknowledges that “[e]xternal light...is incident on the second surface of the photodiode 145,” a POSITA would understand that external light would also be incident on at least the annotated second surface of pattern 110a. *Hwang-099* at 8:20-22; *see also, id.* at 9:6-7 (“Therefore, external light incident on the second surface of the photodiode 145....”). A POSITA would understand that light is incident on the entire exposed top surface of Hwang-099’s image sensor. *Hwang-099* at 1:24-26 (“The image sensor has a light receiver that receives light from the outside and converts it to electrical signals.”), FIG. 1. This

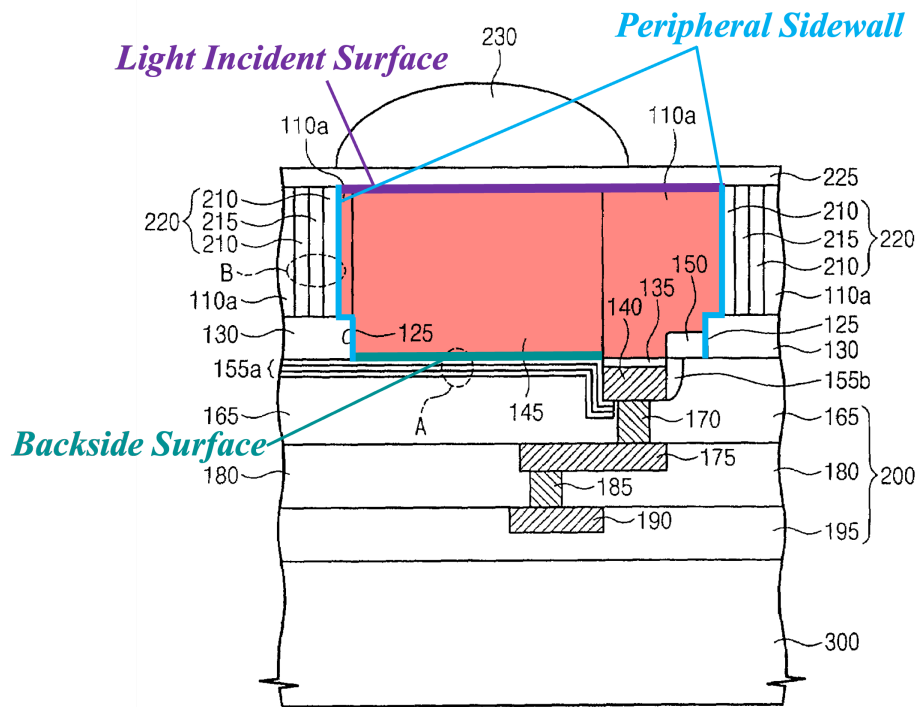
means that light is incident on the entire array of pixels shown in FIG. 1, including the top surface of pixel semiconductor pattern 110a and the photodiode 145 disposed in the pattern 110a shown in FIG. 2, and for each pixel in the array. Therefore, each pixel will include a light incident surface that includes more than just the portion of the surface coinciding with the photodiode that otherwise coincides with the width of the pixel.

145. Because the top/second and bottom/first surfaces of pattern 110 “face one another” and are “parallel,” the *backside surface is opposite the light incident surface*. Hwang-099 at 6:37-38, FIG. 2.

**D. 1[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;”**

146. For the reasons discussed below, the sidewall of a trench formed by etching into pixel semiconductor pattern 110a is a *peripheral sidewall*:

Fig. 2



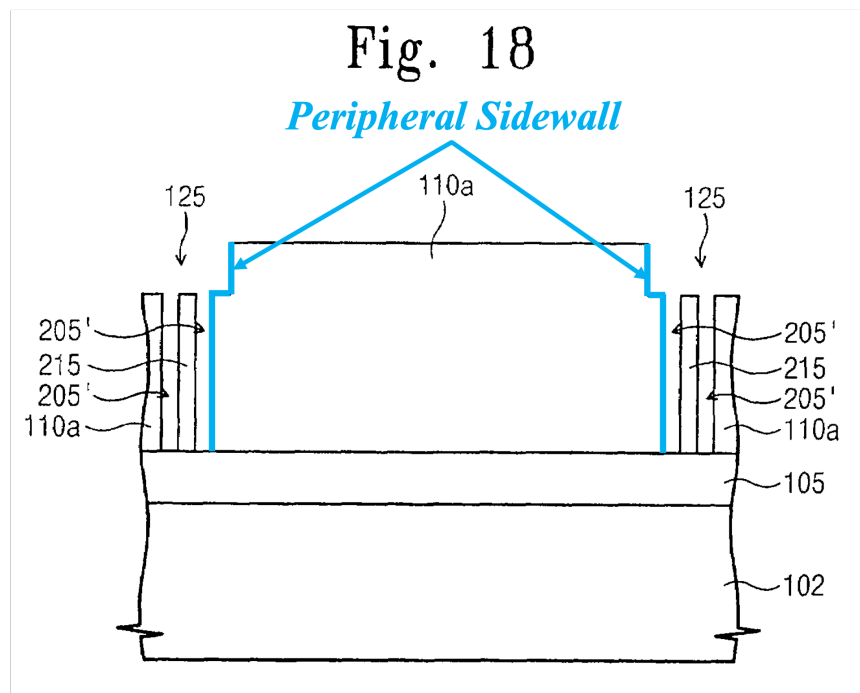
Hwang-099 at FIG. 2 (annotated).

147. As I discussed previously, FIGS. 18 and 19 correspond to a method of creating the *pixel* depicted in FIG. 2. See ¶¶ 80-83. Regarding FIG. 18, Hwang-099 discloses:

Referring to FIG. 18, a first substrate 100 having a semiconductor layer 110 is prepared, **after which the semiconductor layer 110 is patterned to form a trench 125** that restricts an active region. Next, the **floor of the trench 125 is selectively etched to form a plurality of grooves 205'.**

Hwang-099 at 14:3-7.

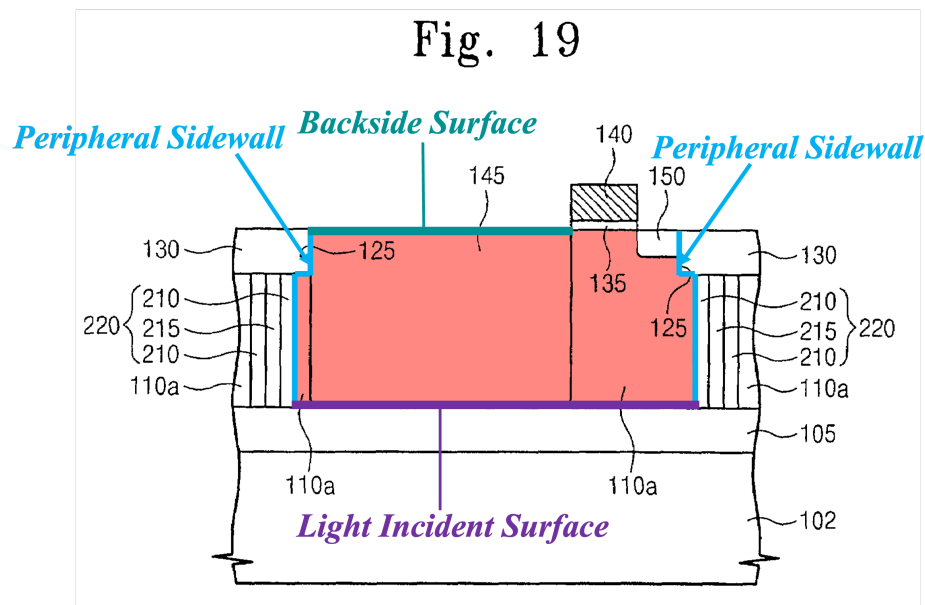
148. In other words, trench 125 is etched into semiconductor layer 110, then deeper trenches are etched into the floor of trench 125 to form grooves 205'. *Id.* Thus, the semiconductor layer 110 is etched to form trench 125 and grooves 205', which creates a sidewall along the boundaries of pixel semiconductor pattern 110a. As shown in FIG. 18, trench 125 and the grooves 205' closest to pixel semiconductor pattern 110a form the *peripheral sidewall* of the pixel:



*Hwang-099* at FIG. 18 (annotated).

149. That is, the grooves 205' “define[] a pixel semiconductor pattern 110a,” meaning “the plurality of grooves 205' encloses one pixel semiconductor pattern 110a in layers.” *Hwang-099* at 14:7-10. After formation of the grooves 205', “an oxide layer i[s] formed to fill the trench 125 and grooves 205'.” *Hwang-099* at 14:13-14, FIG. 19. The resulting structure in FIG. 19 illustrates how the pixel

semiconductor pattern 110a's *peripheral sidewall* is formed by trench 125 and the groove 205' adjacent to semiconductor pattern 110a:



*Hwang-099* at FIG.19 (annotated).

150. Grooves 205' are filled with the oxide layers of the sidewall multi-layered reflection layer 220. *Hwang-099* at 14:13-22. The sidewall multi-layered reflection layer 220a encloses “the **side walls of pixel semiconductor patterns 110.**” *Hwang-099* at 6:33-36; *see also, id.* at 6:7-9 (“A sidewall multi-layered reflection layer 220 is provided between the **side walls of the pixel semiconductor patterns 110a.**”), 6:15-17 (“The sidewall multi-layered reflection layer 220 encloses the **side walls of the pixel semiconductor patterns 110a.**”), 12:51-53 (“Thus, a sidewall multi-layered reflection layer 220 is formed on the **sidewall of the pixel semiconductor pattern 110a.**”), 14:20-22.

151. Moreover, the sidewall of pixel semiconductor pattern 110a is also *disposed into at least a portion of the pixel* because it is formed by etching into the semiconductor layer 110. *See ¶¶ 146-149. 149*In other words, trench 125 and grooves 205' are formed by removing semiconductor material from layer 110 to define pixel semiconductor pattern 110a. *Id.* Because the *peripheral sidewall* extends into the material forming pixel semiconductor pattern 110a, it is *disposed into at least a portion of the pixel*. *Hwang-099 at 5:52-57.*

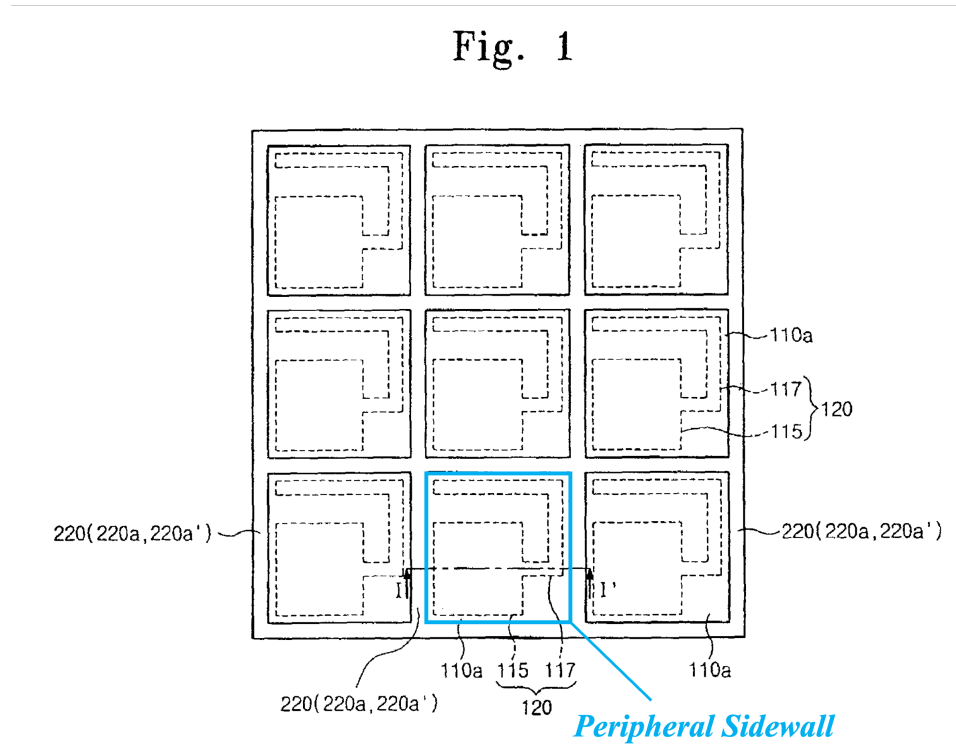
152. The *peripheral sidewall* also extend[s] *at least substantially around the pixel periphery*. Specifically, grooves 205' “define[] a pixel semiconductor pattern 110a” and “enclose[] one pixel semiconductor pattern in layers.” *Hwang-099 at 14:3-22.* Regarding grooves, Hwang-099 generally teaches:

The forming of the sidewall multi-layered reflection layer can include forming a plurality of grooves for defining the pixel semiconductor pattern through selectively etching the semiconductor layer. **Here, the grooves can surround the pixel semiconductor pattern in layers,** and a material filling the grooves and a portion of the semiconductor layer between the grooves can be included in the sidewall multi-layered reflection layer.

*Hwang-099 at 3:60-67.*

153. Because grooves 205' surround and enclose pixel semiconductor pattern 110a and because grooves 205' are formed by etching trench 125, the *sidewall* formed by trench 125 and grooves 205' is a *peripheral sidewall*...extending

at least substantially around the pixel periphery. *Hwang-099* at 12:42-61, 14:3-22, 3:60-67. Indeed, in FIG. 1, the **sidewall** is shown as extending completely around the periphery of pixel semiconductor pattern 110a without any gaps:



*Hwang-099* at FIG. 1 (annotated).

**E. 1[b]: “a **backside light trapping material** substantially covering the **backside surface** ; and”**

154. *Hwang-099* teaches a base multi-layered reflection layer 155a that “contacts the first surface of the pixel semiconductor pattern 110a on which the photodiode diode 145 is formed.” *Hwang-099* at 8:32-34. As I discussed above regarding Claim 1[a][i], the first surface of photodiode 145 is the **backside surface**. See Claim 1[a][i].

155. Base multi-layered reflection layer 155a includes “first and second base multi-layered reflection layers 151 and 152 alternately stacked a plurality of times.” *Hwang-099* at 8:54-56; *see also, id.* at 9:25-26 (“With the first and second base multi-layered reflection layers 151 and 152 alternately stacked three times...”). These first and second reflection layers are made of different materials having different refractive indexes used to reflect regions of light having long wavelengths (e.g., red) that are usually not absorbed completely by the photodiode. *Hwang-099* at 9:26-30 (“[T]he first and second base multi-layered reflection layers 151 and 152 respectively formed of silicon oxide (with a refractive index of approximately 1.46) and silicon (with a refractive index of approximately 4), the pixel semiconductor pattern 110a also being silicon, and the external light having a long red-colored wavelength ...”), 1:44-46 (“Thus, regions of light with a long wavelength (in the red spectrum, for example) are likely not to be absorbed completely by the photodiode, thus reducing the spectral sensitivity.”). Thus, base multi-layered reflection layer 155a is a *light trapping material* because it reflects unabsorbed light back into the photodiode:

Also, the base multi-layered reflection layer 155a has at least two layers with different refractive indexes. Thus, at least one boundary surface reflecting light is disposed in the base multi-layered reflection layer 155a. Hereinafter, the boundary surface in the base multi-layered reflection layer 155a is defined as the second boundary surface.

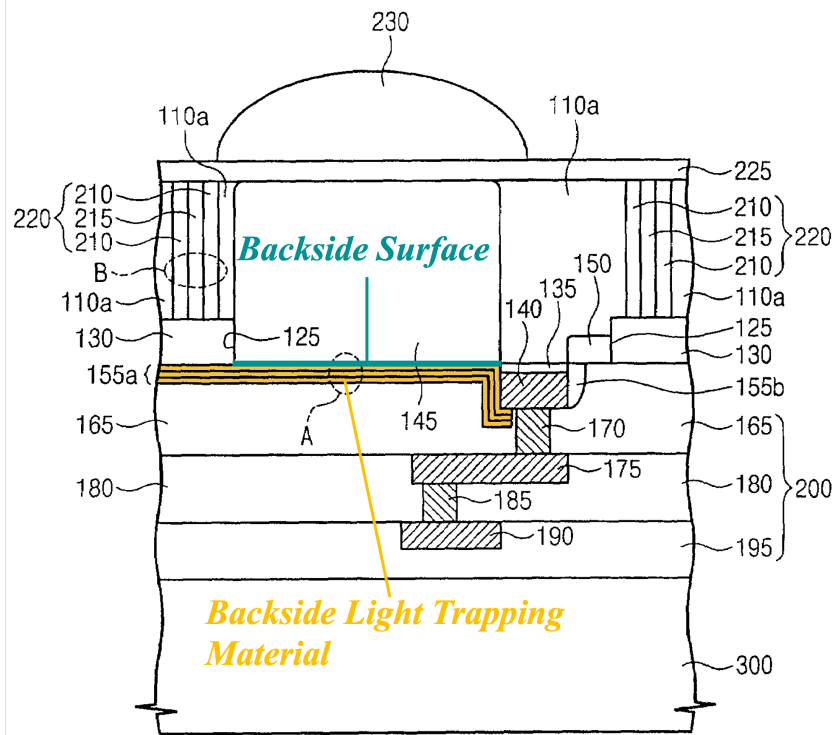
**Therefore, external light incident on the second surface of the photodiode 145 is reflected by the first boundary surface and at least one second boundary surface within the base multi-layered reflection layer 155a. The light reflected by the first and second boundary surfaces is incident again on the photodiode 145. As a result, the rate at which the external light is absorbed by the photodiode 145 is increased to increase the light sensitivity of the image sensor.**

*Hwang-099 at 9:1-14.*

156. The '764 Patent describes that “light contacting the backside light trapping material...is thus reflected back toward the pixel.” *'764 Patent* at Abstract. Because Hwang-099 teaches that light contacting boundary surfaces in the base multi-layered reflection layer 155a is reflected to be incident again on photodiode 145, Hwang's base multi-layered reflection layer 155a is a **backside light trapping material** as described by the '764 Patent.

157. As shown below in FIG. 2, the base multi-layered reflection layer 155a (i.e., **backside light trapping material**) is between the first surface of photodiode 145 (i.e., the **backside surface**) and layer 165 of interlayer insulating layer 200:

Fig. 2



*Hwang-099* at FIG. 2 (annotated).

158. Base multi-layered reflection layer 155a “is interposed between the photodiode 145 and the interlaying insulating layer 200.” *Hwang-099* at 7:45-47. As illustrated, base multi-layered reflection layer 155a comprises three layers extending completely across the first surface of photodiode 145 (i.e., *backside surface*) and beyond. *Hwang-099* at FIG. 2. Because (1) base multi-layered reflection layer 155a is directly underneath the first surface of photodiode 145, and (2) base multi-layered reflection layer 155a extends across the entirety of the first surface of photodiode 145, base multi-layered reflection layer 155a is a *backside light trapping material*

*substantially covering the backside surface*. That is, on the left-hand side of the *backside surface*, base multi-layered reflection layer is shown as extending to the far left of the pixel semiconductor pattern 110 to thereby overlap with the *backside surface*. Similarly, on the right-hand side of the *backside surface*, base multi-layered reflection layer 155a is shown as extending to the edge of photodiode 145, thereby overlapping with the *backside surface*. It makes sense within the context of Hwang-099 that base multi-layered reflection layer 155a *substantially cover[s] the backside surface* because Hwang-099 is concerned with reflecting light back to photodiode 145 (depletion region) which, as discussed above, is the function of base multi-layered reflection layer 155a. See ¶¶ 154-156.

**F. 1[c]: “a peripheral light trapping material substantially covering the peripheral sidewall,”**

159. For the reasons explained below, combining the embodiments of Hwang-099’s FIGS. 2 and 6 renders this limitation obvious.

**1. Hwang-099’s FIG. 2 Embodiment Discloses a Peripheral Light Trapping Material**

160. Hwang-099’s image sensor also includes a *peripheral light trapping material*. Specifically, Hwang-099 teaches a “sidewall multi-layered reflection layer 220 disposed on a sidewall of the pixel semiconductor pattern.” *Hwang-099* at 1:65-67. Sidewall multi-layered reflection layer 220 “includes a first sidewall reflection layer 210 and a second sidewall reflection layer 215” where “the refractive index of

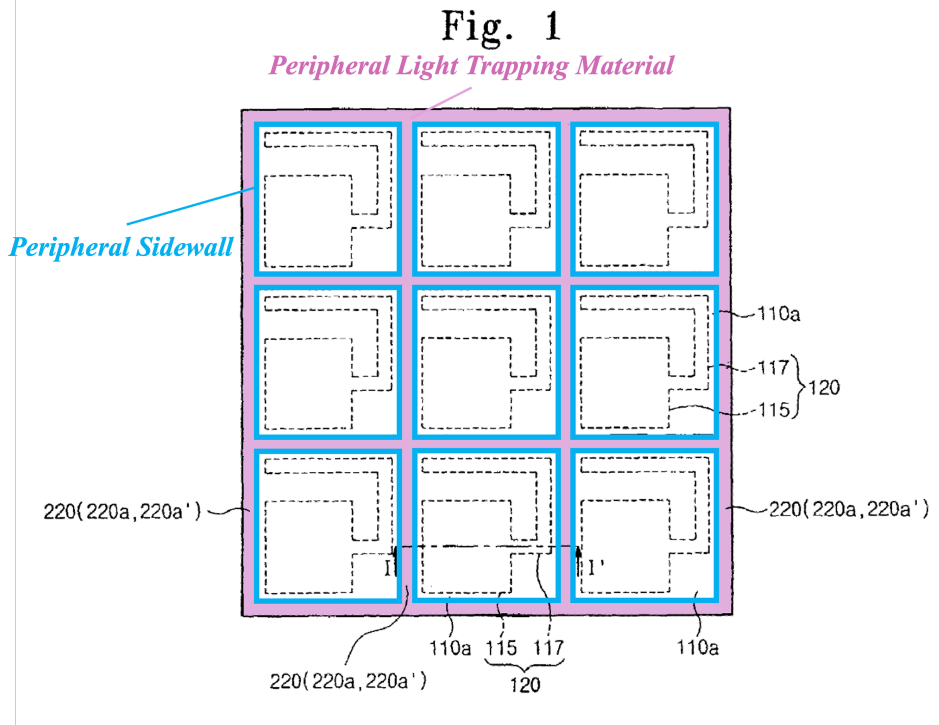
the first sidewall reflection layer is different from the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215.” *Hwang-099* at 9:58-63. The sidewall multi-layered reflection layer 220 further “includes a structure in which the first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner...on the sidewall of the pixel semiconductor pattern 110a.” *Hwang-099* at 10:6-10.

161. Per Hwang-099, the boundary surfaces at the interfaces between layers 210 and 215 reflect light back onto the photodiode 145 “so that the absorption efficiency of external light is increased.” *Hwang-099* at 10:29-35. In other words, when light is incident on the sidewall multi-layered reflection layer 220, it is reflected back toward the photodiode 145. The ’764 Patent similarly describes trapping light by reflecting it back toward the pixel. *’764 Patent* at 1:47-49. Therefore, Hwang-099’s sidewall multi-layer reflection layer 220 is *light trapping* in the same way described by the ’764 Patent because it traps light by reflecting light back into the photodiode.

162. The sidewall multi-layered reflection layer 220 is also *peripheral* to the pixel semiconductor pattern 110a. Per Hwang-099, “all of the side walls of the pixel semiconductor patterns 110a will be described as **enclosed** by the sidewall multi-layered reflection layer 220, as shown in FIG. 1.” *Hwang-099* at 6:33-36, FIG. 1. Specifically, layer 220 is “is provided between the side walls of the pixel

semiconductor patterns 110a” and “**encloses the side walls** of the pixel semiconductor patterns 110a.” *Hwang-099* at 6:7-23. “That is, the sidewall multi-layered reflection layer 220 can be **disposed along the boundaries of all of the pixel semiconductor patterns 110 a**, and all of the pixel semiconductor patterns 110 a can thus be separated by the sidewall multi-layered reflection layer 220.” *Hwang-099* at 6:19-23. As I discussed above with regard to Claim 1[a][ii], the sidewall of pixel semiconductor pattern 110a is *the peripheral sidewall*. See Claim 1[a][ii].

163. Because the sidewall multi-layered reflection layer 220 encloses and is “disposed along the boundaries...of the pixel semiconductor patterns 110a” (i.e., *the peripheral sidewall*), the sidewall multi-layered reflection layer 220 is a *peripheral light trapping material*. That is, it is *peripheral* to the pixel semiconductor pattern 110a because it surrounds the periphery of pixel semiconductor pattern 110a, and it is *light trapping* because it reflects light back into the pixel as established above:

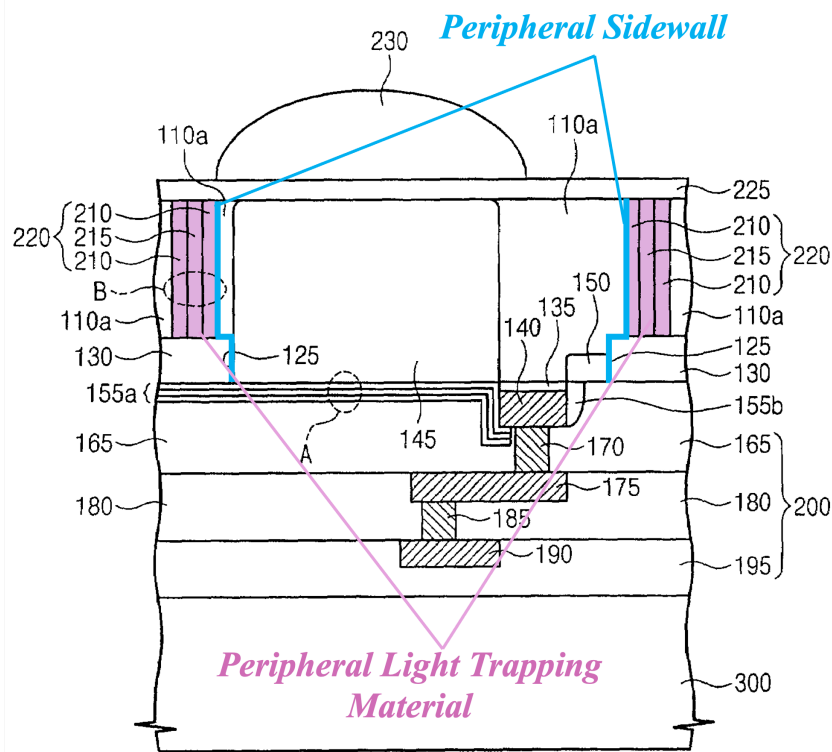


Hwang-099 at FIG. 1 (annotated).

**2. Hwang-099 Renders Obvious a *Peripheral Light Trapping Material* Substantially Covering the *Peripheral Sidewall***

164. As shown in FIG. 2, Hwang-099's sidewall multi-layered reflection layer 220 (i.e., *peripheral light trapping material*) covers part of pattern 110a's sidewall (i.e., the *peripheral sidewall*), while isolation element 130 covers the remaining portion of the sidewall:

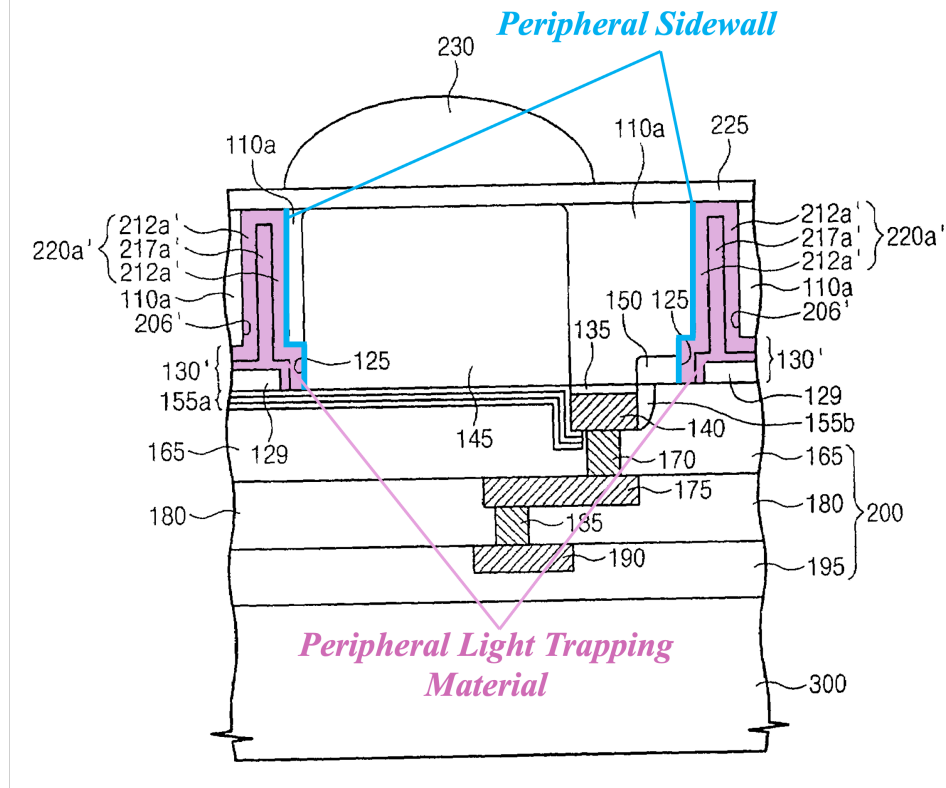
Fig. 2



*Hwang-099* at FIG. 2 (annotated).

165. However, *Hwang-099* also teaches an alternative embodiment in FIG. 6 where device isolation pattern 130' "include[s] extended portions of the first and second sidewall reflection layers 212a' and 217a'." *Hwang-099* at 12:26-28. As shown in FIG. 6 below, the first and second sidewall reflection layers extend through the isolation pattern 130' to base multi-layered reflection layer 155a such that the *sidewall* is substantially covered by a *peripheral light trapping material* 220a':

Fig. 6



Hwang at FIG. 6 (annotated).

166. A POSITA would have been motivated and found it obvious to modify the device isolation pattern 130 of the FIG. 2 embodiment such that portions of the first and second sidewalls layers 210/215 would extend through device isolation pattern 130 and completely cover the peripheral sidewall of pixel semiconductor pattern 110a. For example, Hwang-099 discusses the desire for increased spectral sensitivity of the image sensor and notes problems associated with long-wavelength light (such as red light):

Spectral sensitivity is one of crucial characteristics of an image sensor. The higher the percentage of incident light absorbed by the photodiode, the higher the spectral sensitivity. An increase in the spectral sensitivity leads to an increase in light sensitivity of the image sensor to external light, giving the image sensor favorable properties. However, there are many factors that can reduce the spectral sensitivity of the image sensor, such as the configuration of the image sensor, the wavelengths of incident light, etc. For example, many specific elements of an image sensor, such as its lines, can prevent light from being freely incident. Also, the amount of light absorbed by the photodiode can be reduced according to the wavelength of the light. For example, with a longer wave length, light penetration through the photodiode increases. Thus, regions of light with a long wavelength (in the red spectrum, for example) are likely not to be absorbed completely by the photodiode, thus reducing the spectral sensitivity.

*Hwang-099* at 1:30-47.

167. The modified device isolation pattern 130, having extended layers 215 and 210, would therefore possess the same *light trapping* ability as the sidewall multi-layered reflection layer 220 due to the alternating layers of materials with different refractive indexes reflecting light back into the photodiode, but with the increased performance capabilities for longer wavelength light due to the layered materials extending deeper into the semiconductor pattern 110a substrate and photodiode 145.

168. In more detail, a POSITA would also understand that, by replacing the single layer 130 in Fig. 2 with alternating layers of materials with different refractive indexes (labeled 130' in Fig. 6), the reflectivity and spectral selectivity in the lower section of sidewall surrounding the pixel would be increased. That is, replacing element 130 with multiple alternating layers in 130' forms a Bragg reflector, and relative to the single layer shown in Fig. 2, a multi-layer Bragg reflector will increase the number of photons returned to the photodiode from the lower part of the sidewall.

169. A POSITA would have been motivated to make this modification to increase the surface area of *light trapping material* covering the peripheral sidewall. By increasing the surface area of the peripheral sidewall that is covered by the *light trapping material*, light that is incident over the entirety of the peripheral sidewall will be reflected back toward the photodiode, just as the sidewall multi-layered reflection layer 220 functions to do. The modification would have had a reasonable expectation of success, at least because Hwang-099 provides methods for manufacturing a device isolation 130 having extended portions of sidewall multi-layered reflection layer 220. *Hwang-099* at 14:3-22, 12:35-13:3.

G. *1[c]/[i]: “wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials,”*

170. For the reasons discussed below, Hwang-099 teaches that both the *backside light trapping material* and the *peripheral light trapping material* include

a *high refractive index material* sandwiched between *two low refractive index materials*. I will refer to this as a “low-high-low sandwich” in my analysis below.

**1. Backside Light Trapping Material**

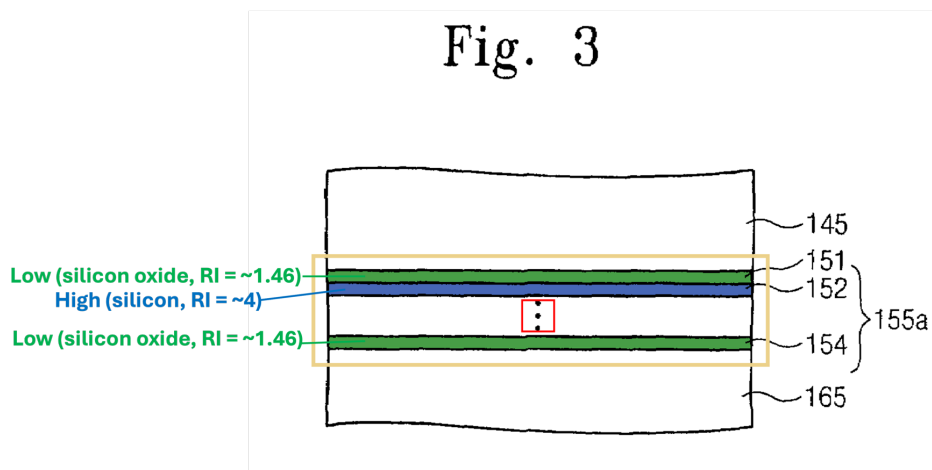
171. Hwang-099’s base multi-layered reflection layer 155a (i.e., *the backside light trapping material*) includes a low-high-low sandwich. Base multi-layered reflection layer 155a includes “a first base multi-layered reflection layer 151 and a second base multi-layered reflection layer 152” that have different refractive indexes. *Hwang-099* at 8:40-45. Specifically, the first base multi-layered reflection layer 151 is “silicon oxide (with a refractive index of approximately 1.46)” and the second base multi-layered reflection layer 152 is “silicon (with a refractive index of approximately 4).” *Hwang-099* at 9:25-34. Thus, the second base multi-layered reflection layer 152 has a higher refractive index than the first base multi-layered reflection layer 151.

172. The first and second layers 151 and 152 are “alternately stacked three times” such that base multi-layered reflection layer 155a includes six total sub-layers. *Hwang-099* at 9:25-26; *see also, id.* at 8:54-56 (“In other words, the base multi-layered reflection layer 155a can include the first and second base multi-layered reflection layers 151 and 152 alternately stacked a plurality of times.”).

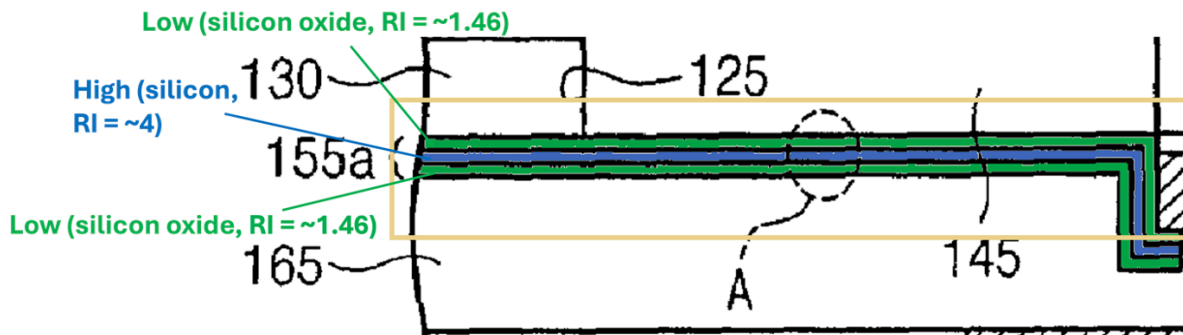
173. Further, because Hwang-099 teaches that the alternating first and second base multi-layered reflection layers 151 and 152 are stacked three times,

these layers qualify as a low-high-low sandwich as required by the claim. That is, when these layers are stacked three times, the resulting structure is layer 151-layer 152-layer 151, which is a low-high-low sandwich, repeating three times.

174. Hwang-099 also teaches that “layer 154” may be the “first base multi-layered reflection layer 151 or the second base multi-layered reflection layer 152.” *Hwang-099 at 8:57-60*. Hwang-099 illustrates the base multi-layered reflection layer 155a in FIG. 3 as including the first base multi-layered reflection layer 151, a second base multi-layered reflection layer 152, and layer 154. *Hwang-099 at FIG. 3*. The three dots between layers 152 and 154 denote that the stacking of layers 151 and 152. Because Hwang-099 teaches that layer 154 can be the first base multi-layered reflection layer 151, (*Hwang-099 at 8:57-60*) when there are three layers total, the base multi-layered reflection layer 155a (e.g., the *backside light trapping material*) includes a *high refractive index material* sandwiched between *two low refractive index materials*. *Hwang-099 at 8:57-60*.



Hwang-099 at FIG. 3 (annotated).



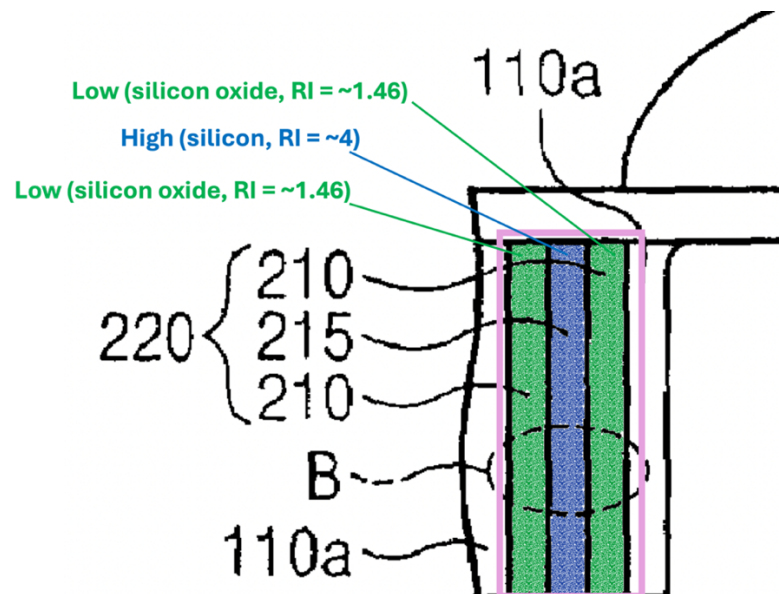
Hwang-099 at FIG. 2 (excerpted, annotated).

## 2. *Peripheral Light Trapping Material*

175. Hwang-099's sidewall multi-layered reflection layer 220 (i.e., *the peripheral light trapping material*) includes a low-high-low sandwich. In particular, sidewall multi-layered reflection layer 220 includes "a second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210, the first and second sidewall reflection layers 210 and 215 respectively formed of a silicon oxide layer and a silicon layer..." Hwang-099 at 10:48-52. As I discussed above, Hwang-099 discloses that silicon oxide has "a refractive index of approximately 1.46" and silicon has "a refractive index of approximately 4." Hwang-099 at 9:25-34. Thus, layer 210 is a *low refractive index material*, and layer 215 is a *high refractive index material*.

176. As shown in FIG. 2, sidewall multi-layered reflection layer 220 includes three layers, 210/215/210. Hwang-099 at FIG. 2, 12:66-67 ("[T]he sidewall multi-layered reflection layer 220 has three layers."). Thus, Hwang-099 teaches that

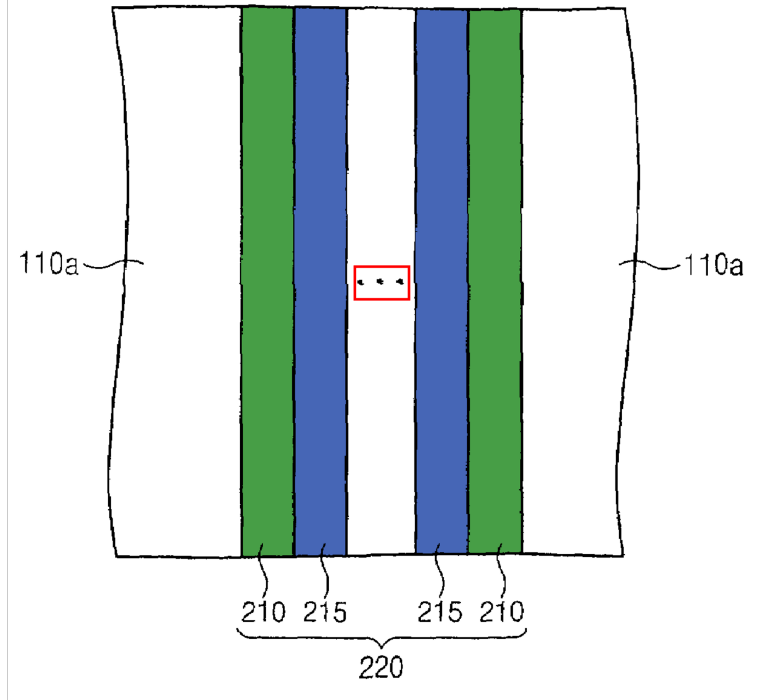
the sidewall multi-layered reflection layer 220 (i.e., the *peripheral light trapping material*) includes a high refractive index material (e.g., silicon) sandwiched between two low refractive index materials (e.g., silicon oxide):



*Hwang-099* at FIG. 2 (excerpted, annotated).

177. With reference to FIG. 4, *Hwang-099* further describes that the “first and second sidewall reflection layers 210 and 215 are stacked in an alternating manner a plurality of times.” *Hwang-099* at 10:6-10. The above example in FIG. 2 illustrates the case where there are three layers total in the sidewall, 210/215/210. In FIG. 4, *Hwang-099* denotes that these layers can be alternated any number of times:

Fig. 4



*Hwang-099* at FIG. 4 (annotated).

178. Due to *Hwang-099*'s teaching that the layers 210 and 215 are alternated and that "both the layers of the sidewall multi-layered reflection layer 220 contacting the pair of neighboring pixel semiconductor patterns 110 can be the first sidewall reflection layer 210[,]" no matter how many layers are present in the sidewall multi-layered reflection layer 220, a high refractive index layer is always sandwiched between two low refractive index layers. *Hwang-099* at 10:14-17. For example, if one more layer was added to the sidewall multi-layered reflection layer 220 shown

in FIG. 4, for a total of 5 layers, then there would be two instances of the required low/high/low sandwich.

179. Because Hwang-099 expressly teaches that sidewall multi-layered reflection layer 220 includes layers 210/215/210, where layer 215 has a higher refractive index than layers 210, Hwang-099 expressly teaches *wherein...the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.*

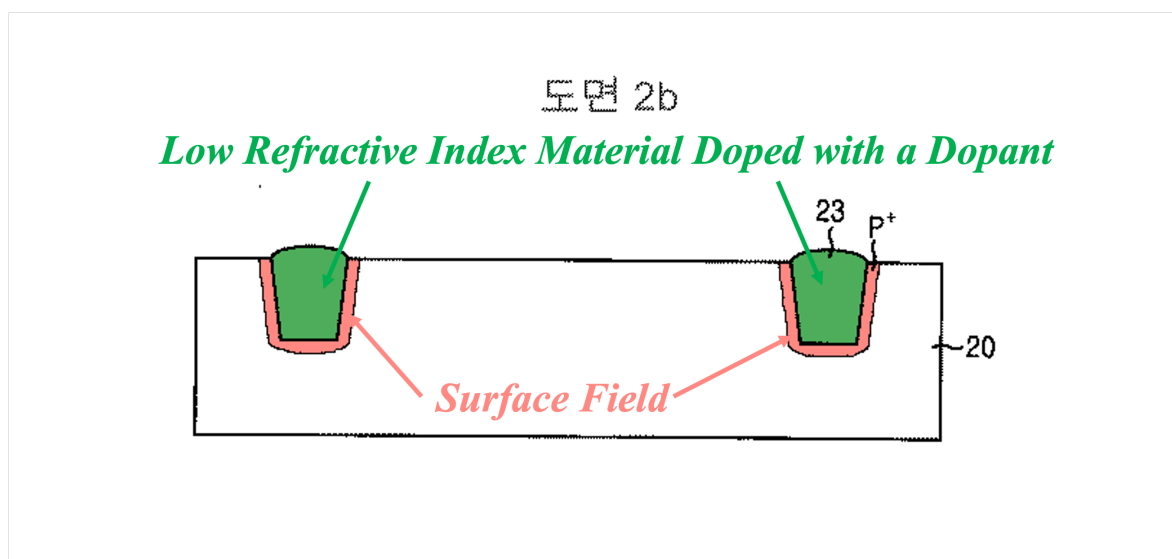
**H. 1[c][ii] “wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field, and”**

180. I note that the '764 Patent describes that “it can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation.” '764 Patent at 9:60-65.

**1. Peripheral Light Trapping Material: Hwang-795's Teachings**

181. Hwang-795 teaches “an image sensor that can prevent crosstalk...by acquiring a channel stop region without addition ion implantation[.] Hwang-795 at Abstract. To do this, Hwang-795 discloses forming a trench in a p-type semiconductor layer (20). Hwang-795 at [0021], [0025]-[0026], FIGS. 2a-2b. After the trench is formed, “a substance doped with P-type impurity, for example, BSG (borosilicate glass), or the like, is deposited, thereby burying the trench.” Hwang-

795 at [0026]. A POSITA would have understood that BSG, or borosilicate glass, is another name for boron-doped silicon dioxide. *See e.g., Chaudhry-006* at 4:59-60 (“BSG (boro-silicate glass, i.e., boron-doped silicon dioxide)”). After the trench is filled with BSG, “chemical mechanical polishing...is carried out, thereby forming a STI-structure field insulation film (23).” *Hwang-795* at [0026], FIG. 2b. Then, a “simple heat process is carried out, thereby diffusing the doped P-type impurity [(i.e., boron)] inside the field insulation film (23)” to form “the channel stop region (P+)[.]” *Hwang-795* at [0028], FIG. 2c.



*Hwang-795* at FIG. 2b.

182. A POSITA would have understood that *Hwang-795*’s channel stop region (P+) *create[s] a surface field* because an electric field is formed between the P+ region and the more lightly doped p-type semiconductor layer 20, at the surface of layer 20 adjacent the trench (i.e., a *surface field*). That is, due to the dopant

concentration gradient between channel stop region P+ and the semiconductor layer 20, an electric field is formed at the surface of the semiconductor layer 20 adjacent the trench. In the p+ -p dopant gradient, the density of mobile holes is higher where the doping level is higher, creating a concentration gradient that drives thermal diffusion of holes away from regions of higher hole density toward lower hole density regions. The spatially fixed negative charge left behind in the crystal lattice quickly establishes charge density equilibrium by forming an electric field with the diffusing holes.

183. I note that silicon dioxide is a low refractive index material as described by the '764 Patent. '764 *Patent* at 2:1, 8:35-36. I note that boron is an example of a dopant as described by the '764 Patent. '764 *Patent* at 17:11-12, Claim 2. Because Hwang-795 teaches boron doped silicon dioxide, Hwang-795 teaches a *low refractive index material is doped with dopant*. Additionally, because a POSITA would have understood or found obvious that an electric field is created by channel stop region (P+) at the surface of semiconductor layer 20 adjacent the trench, Hwang-795 teaches a *low refractive index material is doped with a dopant to create a surface field*.

## **2. Motivation to Combine**

184. A POSITA would have found it obvious and been motivated to dope Hwang-099's silicon oxide layers 210 (e.g., the *low refractive materials*) with boron,

per Hwang-795, so that a charged region and *surface field* around the trench would be formed. As I described above, Hwang-099's silicon oxide is silicon dioxide, based on the refractive index taught by Hwang-099. *See* ¶ 84. Because Hwang-099 already teaches a silicon dioxide layer filling grooves 205, a POSITA would have merely needed to dope silicon dioxide with boron to achieve the combination with Hwang-795. A POSITA would have been motivated to combine the prior art elements of Hwang-795's boron-doped silicon dioxide in a trench with Hwang-099's image sensor according to known methods to yield the predictable result of “*creat[ing] a surface field.*” A POSITA would have understood or found it obvious that by doping Hwang-099's silicon dioxide layer 210 with boron and creating the channel stop region (P+) per Hwang-795, an electric field at the surface of pixel semiconductor pattern 110a adjacent layer 210 would be formed (i.e., *create a surface field*). As I discussed above, a surface field is created to maintain charge equilibrium between higher and lower doped p-doped regions. *See* ¶ 182.

185. Hwang-795 expressly motivates doping Hwang-099's silicon dioxide layers 210 to “reduce intermixing and crosstalk between image data and unit pixels, through more precise isolation between unit pixels.” *Hwang-795* at [0015]. A POSITA would have understood that the formation of the channel stop region (P+) and resulting electric field at the surface of pixel semiconductor pattern 110 (*surface field*) would “reduce intermixing and crosstalk” specifically by reducing electrical

crosstalk. Electrical crosstalk would be reduced because the capacitance associated with the *surface field* electrically uncouples changes in potential (crosstalk) on each side of the doping gradient. Thus, the combination of Hwang-099 and Hwang-795 provides a similar improvement from doping as described by the '764 Patent. *See e.g., '764 Patent* at 6:19-21 (“[I]solation elements can be doped with a dopant that enables the repelling of electrical carriers from the isolation elements[.]”), 9:60-65 (Additionally, it can also be beneficial to dope the sidewalls to create a surface field that will improve electrical isolation between the pixels. In one aspect, it can also be beneficial to dope the low refractive index material of the Bragg-type reflectors to increase such electrical isolation).

186. Further, including a dopant, such as boron, would improve a pixel’s “charge transfer efficiency” and “minimize...dark current[.]” *Hwang-795* at [0029]-[0030], [0036]. Prior to the time of the alleged invention, it was well-known that image sensors “may exhibit crystalline defects such as dangling bond[s] at an interfacial surface between” a “device isolating region” (e.g., a trench) and “the substrate of the photodiode active region.” *See e.g., Kwon* at 1:38-42. Specifically, when “a trench formed by etching the substrate” of an image sensor is “filled with an insulating layer, crystalline defects may occur when etching the substrate.” *See e.g., Kwon* at 1:41-45. Such defects “act as traps capturing electrons” and may “become defect or noise components of each pixel” by “increasing the dark current,

i.e., the current that continues to flow in the photodiode when there is no incident light,” ultimately “degrad[ing] the imaging characteristics” of an image sensor.” *See e.g., Kwon* at 1:45-52. Accordingly, a POSITA would have been very familiar with the issue of dark current arising from defects at the interfacial surface between a trench and substrate in image sensor technology. Further, a POSITA would have recognized that the interface between Hwang’s layers 210 in the sidewall multi-layered reflection layer 220 and pixel semiconductor pattern 110a would have been susceptible to crystalline defects arising from the etching process and would have been a source for dark current. As such, a POSITA would have been motivated to modify Hwang-099 according to the teachings of Hwang-795, thereby improving similar image sensors in the same way.

187. Indeed, it was well-known that creating a doped region around the surface of a trench helped to prevent dark current in image sensors. *See, e.g., Adkisson* at 2:27-30 (“it is also advantageous to having doping on the STI sidewall...to minimize dark current.”); *Kwon* at 6:34-40 (“[T]he channel stop impurity region 106 conformally surrounds the bottom and the sidewall of the pixel trench...and the dark current and noise caused by an interfacial surface defect...can be decreased.”). Therefore, the modification would have predictably improved Hwang-099’s device by reducing dark current. The combination of Hwang-099 and Hwang-795 is the application of a known technique (doping at a trench

interface/depositing BSG in a trench) to a known device (image sensor) ready for improvement to yield predictable results.

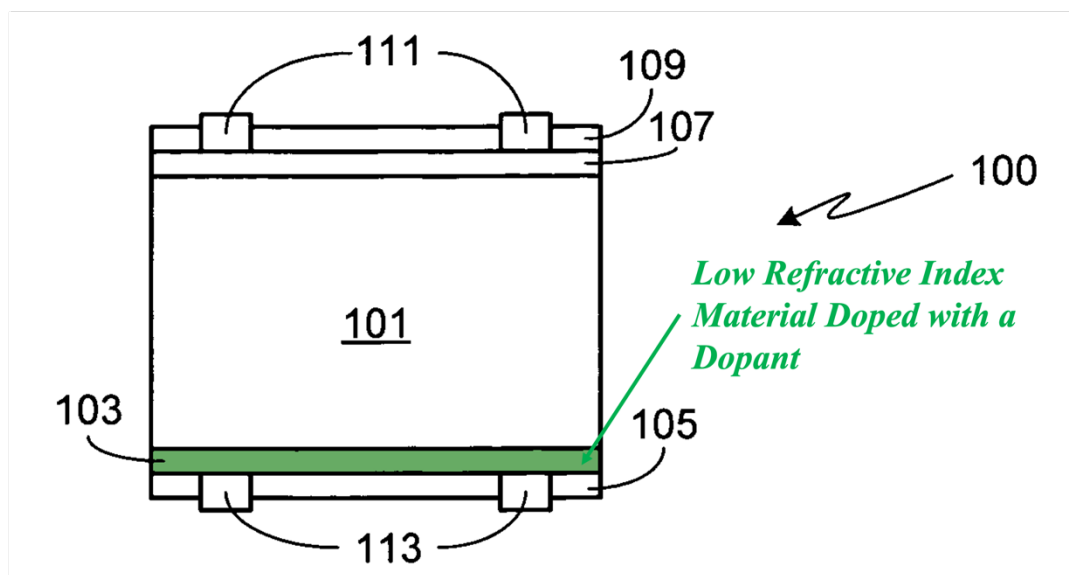
188. Given the benefits described above, the modification would have had a reasonable expectation of success. Moreover, BSG was a well-known and widely available material for use in manufacturing image sensors, and the processes for filling trenches with BSG were well established. *See, e.g., Adkisson* at 7:7-32 (“one technique that has been used to deposit thin films on semiconductor substrates is low-pressure chemical vapor deposition.”); *Chaudhry-610* at 11:28-32 (“One skilled in the art is aware of suitable expedients for forming a layer of...BSG on a substrate, e.g., plasma-enhanced chemical vapor deposition (PECVD).”). Thus, a POSITA would have merely needed to fill grooves 205 with BSG instead of undoped silicon oxide.

### **3. Backside Light Trapping Material: Kaes’ Teachings**

189. Kaes teaches a “simplified manufacturing process” of a “bifacial solar cell (BSC).” *Kaes* at Abstract. The BSC includes a “back surface” that “includes a doped region, the doped region having the same conductivity as the substrate but with a higher doping level.” *Kaes* at Abstract.

190. Kaes teaches that a p-type “silicon substrate 101” is “prepared using any of a variety of well-known substrate preparatory processes” then “the bottom surface of substrate 101 is doped, thereby forming a back surface doped region 103.”

*Kaes* at [0013]. “Region 103 can be formed using any of a variety of techniques” including by “depositing a boron doped silicon dioxide...layer using PE-CVD” onto “the back surface of substrate 101.” *Kaes* at [0014]. “Boron from region 103 is diffused into the back surface of substrate 101 to form a **back surface field**” (*surface field*). Because *Kaes* teaches that region 103 is made of boron doped silicon dioxide, *Kaes* teaches a *low refractive index material is doped with a dopant*. See ¶¶ 84, 171-174. Because *Kaes* teaches that region 103 is heated so that boron diffuses into the back surface of substrate 101 to create a back surface field, *Kaes* teaches a *low refractive index material is doped with a dopant to create a surface field*.



*Kaes* at FIG. 1 (illustrating doped region 103 on the backside surface of substrate 101).

#### 4. *Motivation to Combine*

191. A POSITA would have found it obvious and been motivated to dope Hwang-099's silicon dioxide layer 151 in base multi-layered reflection layer 155a (*backside light trapping material*) with boron to create a back surface field, per Kaes. As I described above, Hwang-099's silicon oxide is silicon dioxide, based on the refractive index taught by Hwang-099. See ¶ 84. Because Hwang-099 already teaches a silicon dioxide layer 215 on the *backside surface*, a POSITA would have merely needed to dope silicon dioxide with boron to achieve the combination with Kaes. A POSITA would have been motivated to combine the prior art elements of Kaes' boron-doped silicon dioxide on the backside surface of the substrate with Hwang-099's image sensor according to known methods to yield the predictable result of creating a back surface field (*create a surface field*). Kaes expressly motivates the combination, stating that "doped region 103 reduces back surface recombination." *Kaes* at [0013]. A POSITA would have been familiar with the issue of recombination and recognized that recombination of electron-hole pairs results in both the generation of dark current (noise) and "no current or charge accumulation[.]" *Hibbeler* at [0035]. As such, a POSITA would have been motivated to modify Hwang-099 according to Kaes such that a back surface field was created to reduce recombination in Hwang-099's *pixel*. The modification would have

predictably increased the quantum efficiency of Hwang-099's *pixel* and reduced the dark current noise by reducing recombination of electron-hole pairs.

192. The modification is application of a known technique (creating a back surface field) to a known device (image sensor) ready for improvement to yield a predictable result (reduced back surface recombination of electron-hole pairs). The modification would have had a reasonable expectation of success at least because Kaes teaches depositing boron doped silicon dioxide on the backside surface and diffusing the boron into the substrate. *Kaes* at [0014]-[0016]. Thus, a POSITA would have been able to easily implement Kaes' back surface field in Hwang-099's image sensors. Further, as I discussed above, the modification would have merely required doping Hwang-099's silicon dioxide 151 with boron and diffusing the boron into the *pixel*. Techniques to dope silicon dioxide and methods of diffusing dopants into silicon were well-known. *See, e.g., Naumann* at Abstract ("The process of producing a refined borosilicate glass includes..."); *Kaes* at [0016]; *Hwang-795* at [0028] ("Next, as simple heat process is carried out, thereby diffusing the doped P-type impurity...").

I. *1[d]: “wherein light contacting the **backside light trapping material** or **peripheral light trapping material** is reflected back toward the pixel.”*

193. For the reasons discussed below, Hwang-099 teaches that both light contacting the **backside light trapping material** and light contacting the **peripheral light trapping material** are reflected back toward the **pixel**.

194. As discussed with regard to Claims 1[b], light contacting Hwang-099’s base multi-layered reflection layer 155a (i.e., *the backside light trapping material*) is reflected back to “be incident again on photodiode 145,” which is part of the **pixel**. *Hwang-099* at 9:1-14; *see* Claims 1[a], 1[b]. Base multi-layered reflection layer 155a includes “first and second base multi-layered reflection layers 151 and 152 alternately stacked a plurality of times.” *Hwang-099* at 8:54-56; *see also, id.* at 9:25-26 (“With the first and second base multi-layered reflection layers 151 and 152 alternately stacked three times...”). “The refractive index of the first base multi-layered reflection layer 151 is different from the refractive indexes of the second base multi-layered reflection layer 152 and the pixel semiconductor pattern 110a.” *Hwang-099* at 8:42-45. “[E]xternal light is reflected at a high rate by a boundary surface (hereinafter referred to as the first boundary surface) between the pixel semiconductor pattern 110a and the base multi-layered reflection layer 155a” due to the substantial “difference in the refractive indexes of the pixel semiconductor

pattern 110a and the first base multi-layered reflection layer 151.” *Hwang-099* at 8:61-67.

195. Due to the differences in the refractive indexes between layers 151 and 152, there is also at least one additional boundary surface (i.e., a second boundary surface) within base multi-layered reflection layer 155a. *Hwang-099* at 9:1-6 (“Also, the base multi-layered reflection layer 155a has at least two layers with different refractive indexes. Thus, at least one boundary surface reflecting light is disposed in the base multilayered reflection layer 155a. Hereinafter, the boundary surface in the base multi-layered reflection layer 155a is defined as the second boundary surface.”). Thus, *light contacting* the base multi-layered reflection layer 155a (i.e., *the backside light trapping material*) *is reflected back toward* the photodiode 145 (i.e., the *pixel*) due to the first and second boundary surfaces associated with base multi-layered reflection layer 155a:

Therefore, external light incident on the second surface of the photodiode 145 is reflected by the first boundary surface and at least one second boundary surface within the base multi-layered reflection layer 155a. The light reflected by the first and second boundary surfaces is incident again on the photodiode 145. As a result, the rate at which the external light is absorbed by the photodiode 145 is increased to increase the light sensitivity of the image sensor.

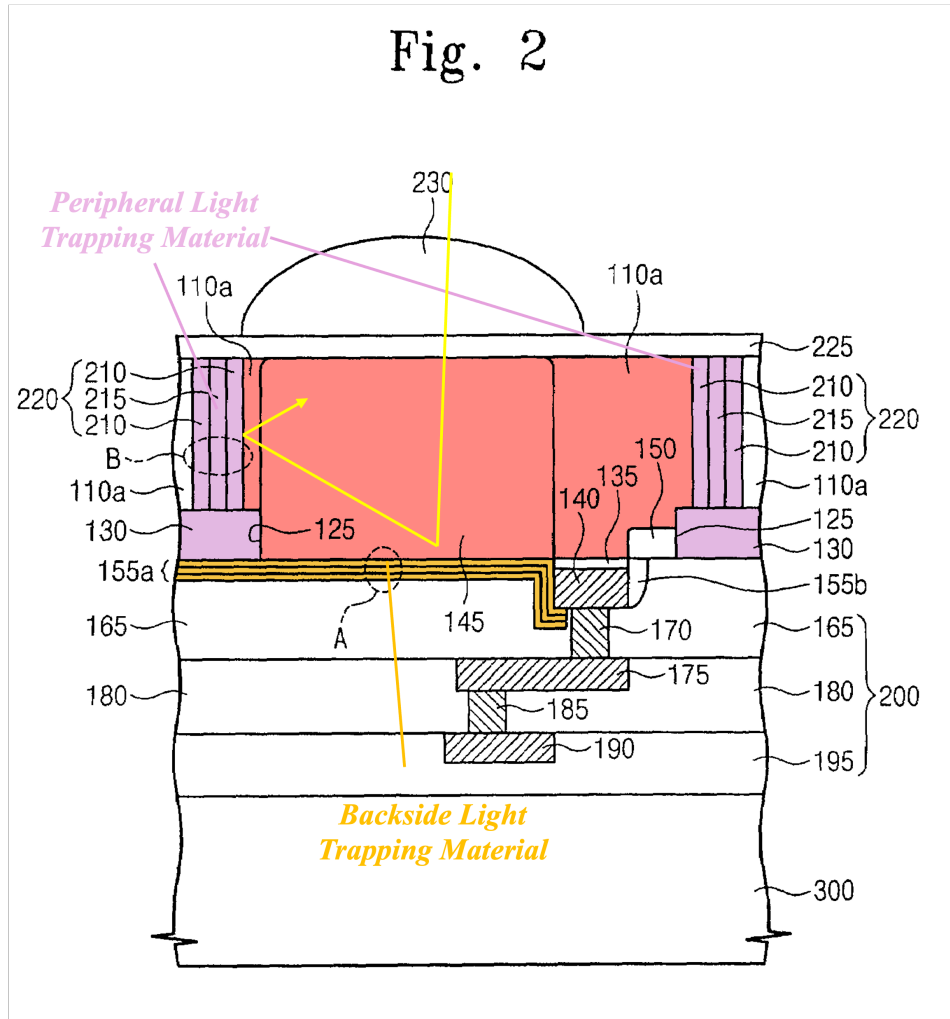
*Hwang-099* at 9:6-14.

196. Sidewall multi-layered reflection layer 220 (i.e., *the peripheral light trapping material*) similarly includes a third boundary surface “between the sidewall multi-layered reflection layer 220 and the pixel semiconductor pattern 110a” and a fourth boundary surface “present within the sidewall multi-layered reflection layer 220.” *Hwang-099* at 9:45-57. Specifically, “[t]he sidewall multi-layered reflection layer includes a first sidewall reflection layer 210 and a second sidewall reflection layer 215” having different refractive indexes. *Hwang-099* at 9:58-66. Thus, *light contacting the sidewall multi-layered reflection layer 220 (i.e., the peripheral light trapping material) is reflected back toward the photodiode 145 (i.e., the pixel)* due to the third and fourth boundary surfaces associated with sidewall multi-layered reflection layer 220:

Light that is reflected from the first and second boundary surfaces is also reflected by the third boundary surface and also the fourth boundary surface within the sidewall multi-layered reflection layer 220. **As a result, the portion of the light reflected toward the sidewall multi-layered reflection layer 220 from the light reflected by the first and second boundary surfaces is incident again on the photodiode 145**, so that the absorption efficiency of external light is increased.

*Hwang-099* at 10:28-35.

197. I have annotated FIG. 2 below to illustrate an exemplary path of light reflecting off the base multi-layered reflection layer 155a and sidewall multi-layered reflection layer 220 back toward photodiode 145:



*Hwang-099 at FIG. 2 (annotated).*

**J. Claim 2:** “The device of claim 1, wherein the *backside light trapping material* and the *peripheral light trapping material* includes a *high refractive index material* sandwiched between *two low refractive index materials*.”

198. As discussed above, Hwang-099 teaches that both the *backside light trapping material* and the *peripheral light trapping material* include a *high refractive index material* sandwiched between *two low refractive index materials*.

See Claim 1[c][i], ¶¶ 170-179, incorporated herein).

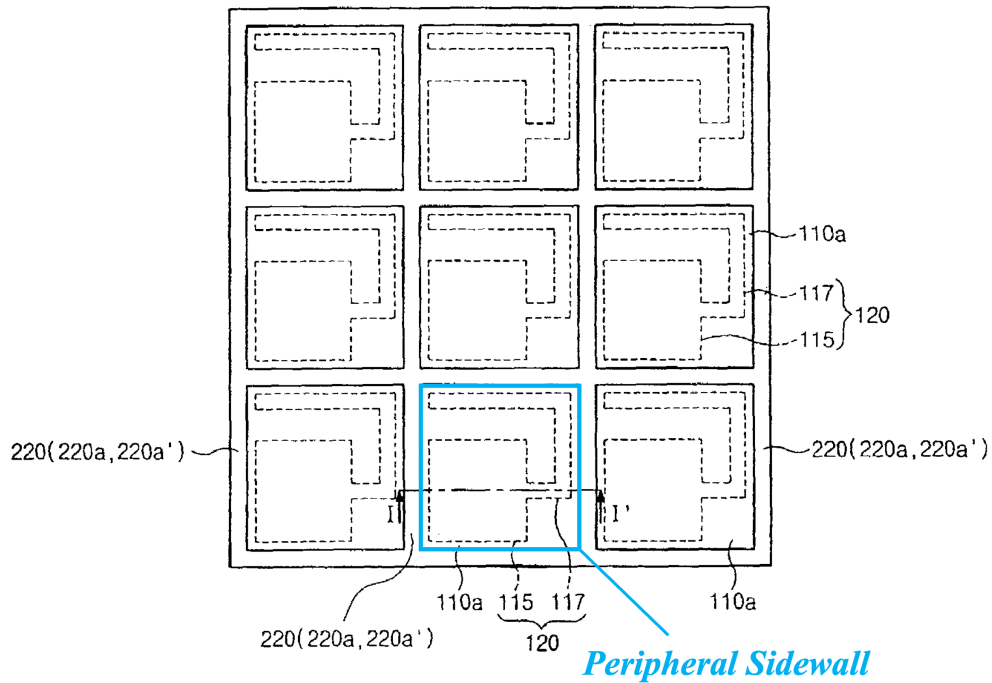
**K. Claim 3:** “The device of claim 1, wherein the dopant is boron or antimony.”

199. The combination of Hwang-099 and Hwang-795 I described above teaches *wherein the dopant is boron*. See Claim 1[c][ii].

**L. Claim 4:** “The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery”

200. As discussed above at Claim 1[a][ii], the *peripheral sidewall* of Hwang-099 extends completely around the pixel periphery:

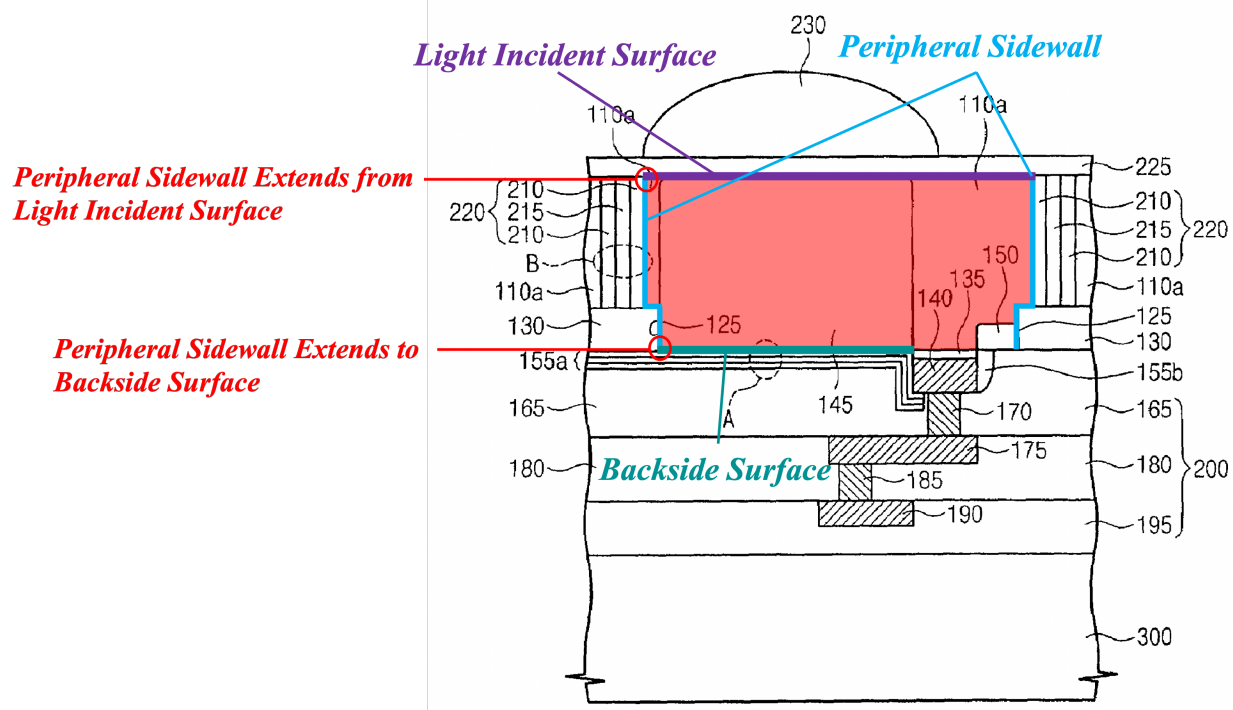
Fig. 1



Hwang-099 at FIG. 1 (annotated); see also, Claim 1[a][ii].

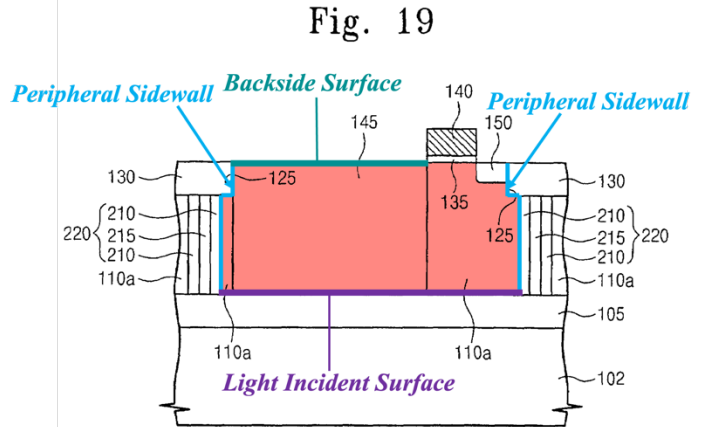
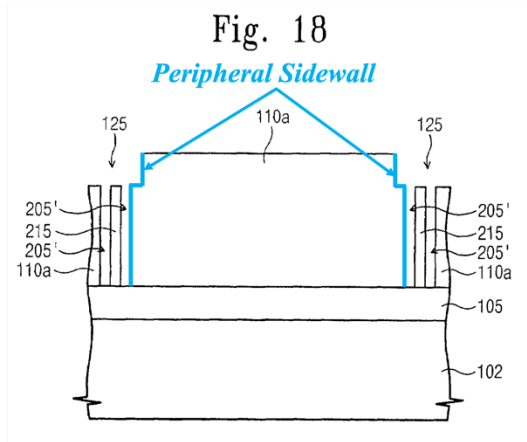
**M. Claim 5:** “The device of claim 1, wherein the *peripheral sidewall* extends from the *light incident surface* to the *backside surface*.”

201. Recall that the *peripheral sidewall* of Hwang-099 is mapped as the sidewall of pixel semiconductor pattern 110a. See Claima 1[a][ii], 1[c]. As shown below, the *peripheral sidewall* extends from the *light incident surface* to the *backside surface*:



*Hwang-099* at FIG. 2 (annotated); *see also*, Claims 1[a], 1[c].

202. Additionally, the etching of trench 125 and grooves 205 that forms the *peripheral sidewall* includes etching to a portion of the second surface of the semiconductor pattern 110a, which is the *light incident surface*. *See* Claim 1[a][ii]. Similarly, the semiconductor pattern 110a is etched through a portion of the first surface that is the *backside surface*:



*Hwang-099* at FIGS. 18-19 (annotated).

203. Therefore, FIGS. 18-19 further confirm the peripheral sidewall extends from the *light incident surface* to the *backside surface*.

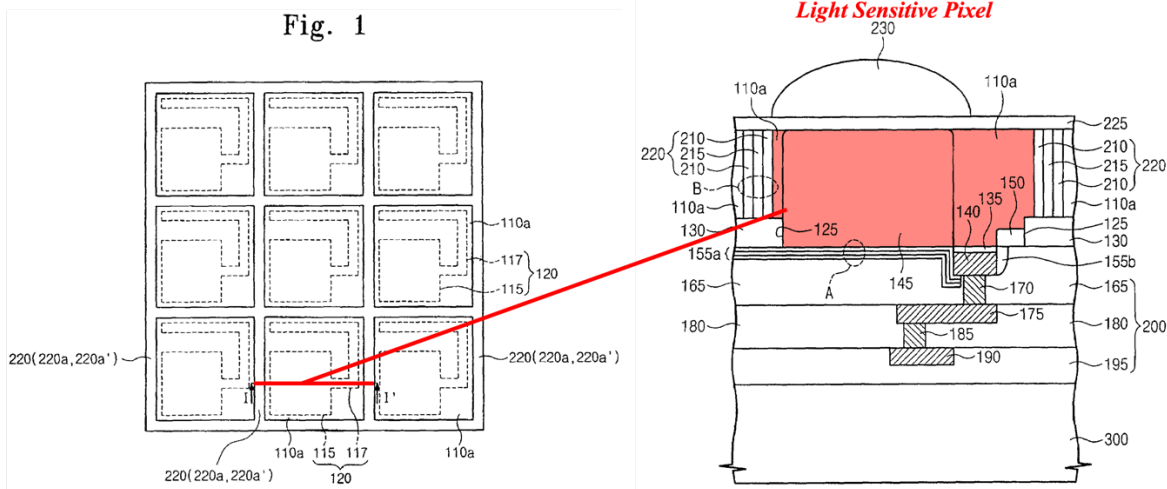
**N. Claim 7: “An array of light trapping pixel devices of claim 1.”**

204. The portion of the image sensor shown in FIG. 2 is a *pixel device* because it includes at least pixel semiconductor pattern 110a with photodiode 145 disposed therein, which is mapped as the claimed *pixel*. *Hwang-099* at 5:52-59; Claim 1[a]. In other words, FIG. 2 is a *pixel device* because it comprises the *pixel*.

205. The portion of the image sensor shown in FIG. 2 is *light trapping* at least because it comprises sidewall multi-layered reflection layer 220 and base multi-layered reflection layer 155a which, as described above, function to reflect light incident thereupon back toward photodiode 145. *See* Claims 1[b], 1[c], and 1[d].

206. Figure 1 depicts “a plurality of pixel semiconductor patterns 110a that can be arranged two-dimensionally in rows and columns on a substrate 300.”

*Hwang-099* at 5:52-59, Figure 1. As shown below, the portion of the image sensor in FIG. 2 is a cross-section taken from FIG. 1. Thus, that the *light trapping pixel device* of FIG. 2, including at least photodiode 145 disposed in pixel semiconductor pattern 110a” is what is arranged in rows and columns to form the image sensor of FIG. 1. Thus, the plurality of *light trapping pixel devices* shown in FIG. 1. is an *array of light trapping pixel devices*.



*Hwang-099* at FIGS. 1-2.

**IX. GROUND 2: CLAIM 6 IS OBVIOUS OVER HWANG-099, HWANG-795, KAES, AND KONNO**

**A. Claim 6: “The device of claim 1, wherein at least one of the *backside light trapping material* and the *peripheral light trapping material* is a *metal layer*.”**

**1. Konno’s Teachings**

207. Konno teaches that the “solid-state image element 110” has a “second reflecting layer 120” that, in combination with a “first reflecting layer 121” “confin[e] photons which entered into the solid-state imaging element 110[.]” *Konno* at 8:31-35. “Photons which entered into the solid-state imaging element from the light entrance window 128...reach the photoelectric conversion film 135, and a part of them are absorbed and cause photoelectric conversion[.]” *Konno* at 9:28-32. “The photons not absorbed by the photoelectric conversion film 125 transmit the pixel electrode 124 and the transparent layer 136, and reach the second reflecting layer 120.” *Konno* at 9:64-67. The photons that reach the second reflecting layer 120 “are reflected by the mirror surface of the second reflecting layer 120...and reach the photoelectric conversion film 125.” *Konno* at 9:67–10:4.

208. That is, the second reflecting layer 120 reflects photons that are incident on it back toward the photoelectric conversion element, as illustrated in FIG. 3. Also shown in FIG. 3, the second reflecting layer 120 covers the backside surface and is “formed by forming a thin film of **metal such as aluminum or silver by deposition** or the like.” *Konno* at 8:35-38; *see also, id.* at 11:42-45 (“Then, in Step 4, the first

reflecting layer 121 is formed. The reflecting layer 121 is manufactured by forming a film with a metal such as aluminum or silver by, for example, the deposition method.”). Thus, Konno teaches *the backside light trapping material ... is a metal layer*:

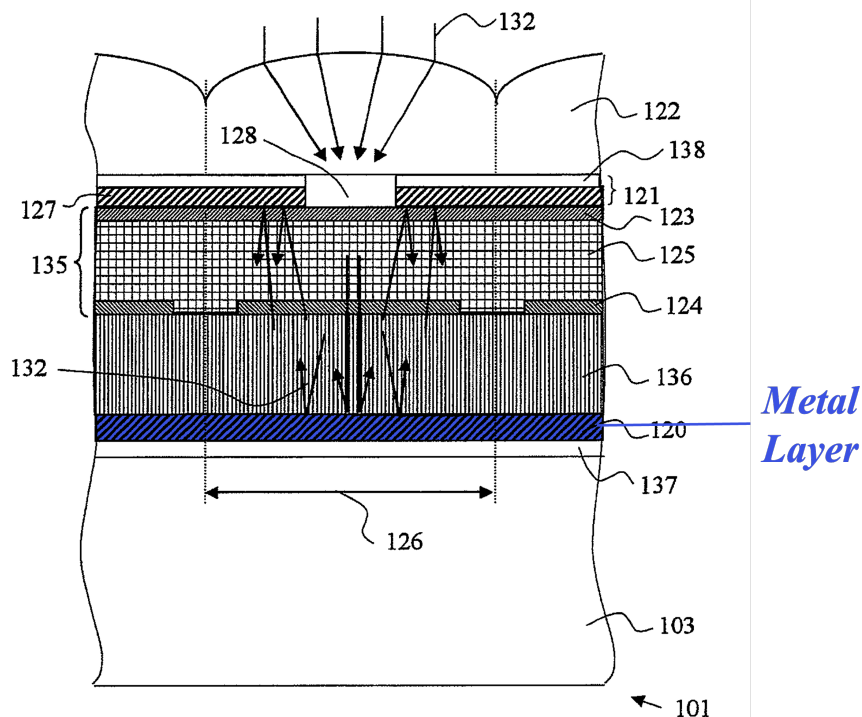


Fig.3

Konno at FIG. 3 (annotated).

## 2. Motivation to Combine

209. Based on the teachings of Konno, it would have been obvious to replace Hwang-099’s base multi-layered reflection layer 155a (i.e., *backside light trapping material*) with a metal layer. Using metal as reflectors in pixels was a common

practice well before the '764 Patent. *See, e.g., Cao* at Abstract (“The back reflector structure consists of...a first textured metal...such as aluminum.”). A POSITA would have understood that various metals were used in backside light trapping materials. *See, e.g., Nozaki* at [0035] (“The reflective layer 340 is typically a reflective metal such as aluminum or tungsten.”). Compared to Bragg reflectors, a metal layer would have offered more broadband reflectivity, as metals typically have higher reflectivity than other materials. Indeed, a “pure silver layer is the most highly reflective material having an integrated total reflectivity of about 95% or higher over the wavelength range from 600 nm to 1200 nm.” *See e.g., Cao* at [0006]. Bragg reflectors, on the other hand, were known to function at a “targeted wavelength.” *See e.g., Hong* at [0027]. Accordingly, “metallic reflectors offer the advantage of high reflectivity in thin films.” *See e.g., Holm* at 8:11:12. The ability to offer “high reflectivity in thin films” using metal layers is an advantage over Bragg reflectors because “multiple layer pairs are typically required to achieve sufficient reflectivity” with their use. *See e.g., Holm* at 8:17-19.

210. A POSITA would have recognized it would be easier using just one metal layer, per Konno, compared to designing a Bragg reflector where multiple layer pairs are required. Thus, a POSITA would have been motivated to improve similar image sensors in the same way to predictably result in the simplification in the manufacturing process and increased broadband light reflectivity. Such a

combination is a simple substitution of one known element (e.g., metal layer as a backside light trapping material) for another (e.g., a Bragg reflector as a backside light trapping material).

211. There would have been a reasonable expectation of success in implementing Konno's metal second reflecting layer 120 in Hwang-099's image sensor because Konno describes how to form reflecting layer 120. *Konno* at 11:42-56 ("[T]he first reflecting layer is manufactured by forming a film with a metal such as aluminum or silver by, for example, the deposition method. The second reflecting layer 120 can be manufactured in the same manner as that for the first reflecting layer 121."). Moreover, methods of forming metal layers were well-known and within the expertise of a POSITA. *See e.g., Yamada* at 7:1-2 ("The reflecting film 12a is formed by, for example, vapor deposition of a metal film."); *Atwater* at [0054] ("Metallic layer 230 may be deposited by a vapor deposition process, such as a vacuum evaporation process, a PVD or sputtering process, a CVD process, or an ALD process."); *Kim* at [0023] ("Reflective film layer 106A can be made of a metal material and can be formed by any metal film deposition method for forming a metal film[.] Preferably, reflective film 106A can be formed by a chemical vapor deposition (CVD) method or a physical vapor deposition (PVD) method.").

212. Additionally, in Hwang-099's image sensor, circuitry such as gate electrode 140, first and second contact plugs 170, 185, and lines 175, 190, are

provided on the backside of the pixel, which further includes insulating layer 200. *Hwang-099* at FIG. 2, 7:5-12, 7:64–8:16. In the combination of *Hwang-099* and *Konno* that includes a metal layer on the backside surface, a POSITA would have also known to evaluate the design of the image sensor for the potential need to add an insulating material between the metal layer and any electrically conductive components, such as *Hwang-099*’s electronic circuitry (140, 170, 175, etc.).

**X. GROUND 3: CLAIMS 8-12 AND 14-15 ARE OBVIOUS OVER HWANG-099**

**A. Claim 8[Pre]: “A *light trapping device*, comprising:”**

213. *Hwang-099* teaches *a light trapping device*. See the above discussion at Claim 1[Pre], ¶¶ 132-134, incorporated herein.

**B. 8[a]: “at least one light sensitive *pixel*”**

214. *Hwang-099* teaches *at least one light sensitive pixel*. See the above discussion at Claim 1[a], ¶¶ 135-142, incorporated herein.

**C. 8[a][i]: “having a *light incident surface*, a *backside surface* opposite the light incident surface,”**

215. *Hwang-099* teaches *having a light incident surface, a backside surface opposite the light incident surface*. See the above discussion at Claim 1[a][i], ¶¶ 143-145, incorporated herein.

- D. 8[a][ii] “and a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;”

216. Hwang-099 teaches a *peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery.*

See the above discussion at Claim 1[a][ii], ¶¶ 146-153, incorporated herein.

- E. 8[b]: “a *backside light trapping material* substantially covering the *backside surface*; and”

217. Hwang-099 teaches a *backside light trapping substantially covering the backside surface.* See the above discussion at Claim 1[b], ¶¶ 154-158, incorporated herein.

- F. 8[c]: “a *peripheral light trapping material* substantially covering the *peripheral sidewall*,”

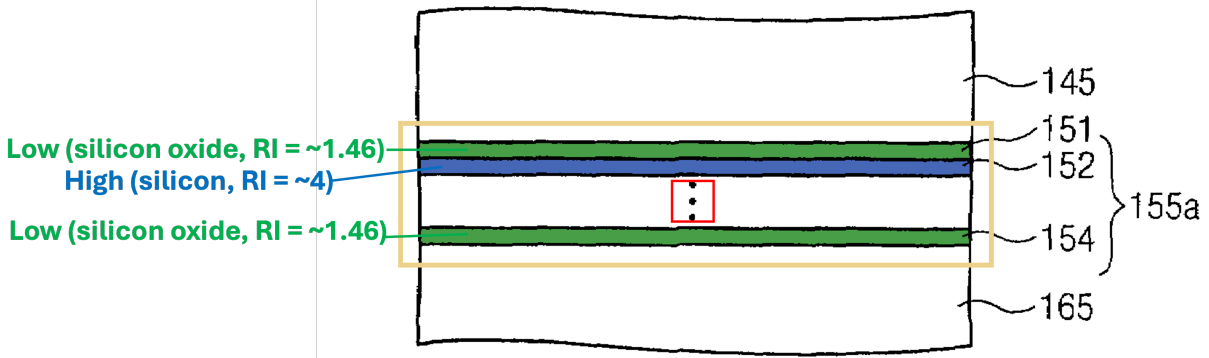
218. By combining the embodiments of Hwang-099’s FIGS. 2 and 6, Hwang-099 renders obvious a *peripheral light trapping material substantially covering the peripheral sidewall.* See the above discussion at Claim 1[c], ¶¶ 159-169, incorporated herein.

- G. 8[d]: “wherein at least one of the *backside light trapping material* and the *peripheral light trapping material* includes a first material sandwiched between two second materials, wherein the *first material* has a higher refractive index as compared to the *two second materials*, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2,”

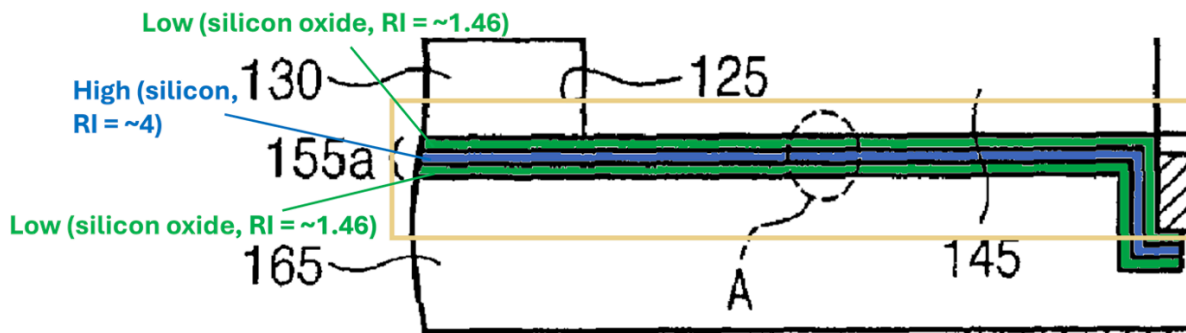
219. Both Hwang-099’s base multi-layered reflection layer 155a (i.e., the *backside light trapping material*) and sidewall multi-layered reflection layer 220 (i.e., the *peripheral light trapping material*) meet Claim 8[d].

220. Regarding base multi-layered reflection layer 155a, the first base multi-layered reflection layer 151 and second base multi-layered reflection layer 152 are alternately stacked three times to create a low-high-low sandwich. See Claim 1[c][i]. Additionally, layer 154 in the base multi-layered reflection layer is silicon oxide. *Id.* Hwang-099’s layer 152 is a *first material* having a higher refractive index than layers 151 (i.e., *two second materials*). The difference in the refractive index[es] of silicon (~4) and silicon oxide (~1.46) is approximately 2.54, which is at least 0.2. Thus, Hwang-099 teaches that the *backside light trapping material* includes a *first material* sandwiched between *two second materials*, wherein the *first material* has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the *first material* and the two second materials is at least 0.2:

Fig. 3



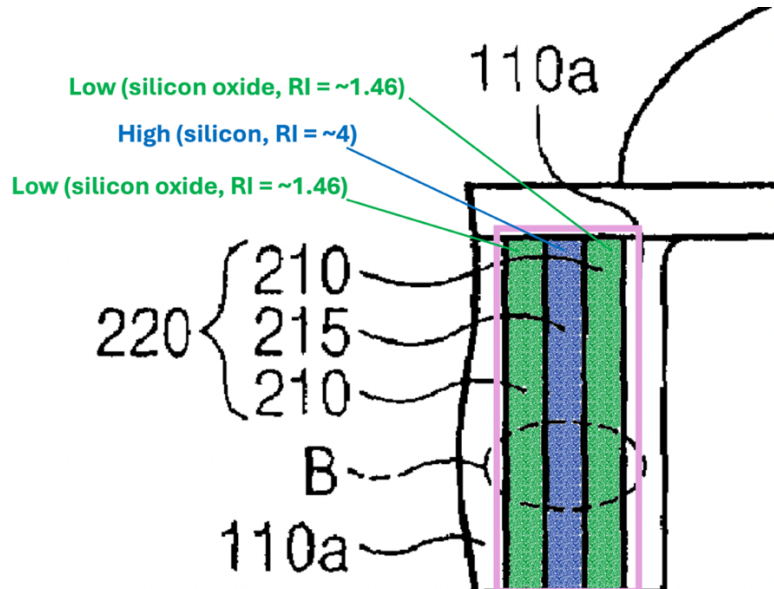
Hwang-099 at FIG. 3 (annotated).



Hwang-099 at FIG. 2 (excerpted, annotated).

221. Similarly, sidewall multi-layered reflection layer 220 (i.e., *the peripheral light trapping material*) includes layer 215 (i.e., a *first material*) sandwiched between layers 210 (e.g., *two second materials*). See Claim 1[e]. Layer 210 is silicon (RI = ~4) and layers 210 are silicon oxide (RI = ~1.46). *Id.* The difference in the refractive index[es] of silicon (~4) and silicon oxide (~1.46) is approximately 2.54, which is *at least 0.2*. Thus, Hwang-099 teaches that the

*peripheral light trapping material* includes a *first material* sandwiched between *two second materials*, wherein the *first material* has a higher refractive index as compared to the *two second materials*, and wherein the difference in refractive index between the *first material* and the *two second materials* is at least 0.2:



Hwang-099 at FIG. 2 (excerpted, annotated).

**H.** 8[d][i]: “and wherein light contacting the *backside light trapping material* or the *peripheral light trapping material* is reflected back toward the pixel.”

222. Hwang-099 teaches wherein light contacting the backside light trapping material and the peripheral light trapping material is reflected back toward the pixel. See the above discussion at Claim 1[d], ¶¶ 193-197, incorporated herein.

**I.** Claim 9: “The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.”

223. As discussed above, Hwang-099’s *two second materials*, in both the base multi-layered reflection layer 155a (i.e., *backside light trapping material*) and

sidewall multi-layered reflection layer 220 (i.e., *peripheral light trapping material*) are silicon oxide. See Claim 8[d]. Hwang-099 teaches silicon oxide has a refractive index of approximately 1.46, which is *less than about 2.1*. Hwang-099 at 9:28-29.

**J. Claim 10:** “*The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.*”

224. As discussed above, Hwang-099’s *two second materials*, in both the base multi-layered reflection layer 155a (i.e., *the backside light trapping material*) and sidewall multi-layered reflection layer 220 (i.e., *the peripheral light trapping material*) are silicon oxide. See Claim 8[d]. A POSITA would have understood that silicon oxide *an oxide*. See e.g., Lee-060 at [0036] (“Examples of oxides include silicon oxide...”). Thus, Hwang-099 teaches this *wherein at least one of the two low refractive index material includes a member selected from...an oxide*.

**K. Claim 11:** “*The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.*”

225. As described above, the two low refractive index materials are silicon oxide. See Claims 1[c][i], 8[d], 9. Thus, Hwang-099 teaches *wherein the at least one of the two low refractive index materials includes...silicon oxide*.

- L. **Claim 12:** “*The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.*”

226. As discussed above, Hwang-099’s *first material* is silicon, which has a refractive index of approximately 4 and is *greater than...about 2.1*. See Claims 1[c][i], 8[d].

- M. **Claim 14:** “*The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.*”

227. As discussed above, the *peripheral sidewall* of Hwang-099 *extends completely around the pixel periphery*. See Claims 1[a][ii], 4 (incorporated herein).

- N. **Claim 15:** “*The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.*”

228. As discussed above, the *peripheral sidewall* of Hwang-099 *extends from the light incident surface to the backside surface*. See Claims 1[a][ii], 5 (incorporated herein).

#### XI. GROUND 4: CLAIM 13 IS OBVIOUS OVER HWANG-099 AND KOMURO

- A. **Claim 13:** “*The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.*”

229. As discussed above, Hwang-099 discloses that the *first material* is silicon and has a refractive index of approximately 4. See Claim 8[d]. Also described above, Hwang-099 discloses embodiments applicable to “external light having a

long red-colored wavelength.” *Hwang-099* at 9:25-32, 10:48-55. However, *Hwang-099* does not describe what type of silicon is used as the *high refractive index material*.

### 1. *Komuro’s Teachings*

230. Komuro teaches silicon, which is “any one of single crystal silicon, amorphous silicon, and polysilicon” having a refractive index of 3.85 at the wavelength of red light:

| TABLE 1                    |                      |                       |                     |                            |                       |                     |
|----------------------------|----------------------|-----------------------|---------------------|----------------------------|-----------------------|---------------------|
|                            | Refractive Index (n) |                       |                     | Extinction Coefficient (k) |                       |                     |
|                            | Blue Light<br>450 nm | Green Light<br>550 nm | Red Light<br>650 nm | Blue Light<br>450 nm       | Green Light<br>550 nm | Red Light<br>650 nm |
| Germanium                  | 4.5                  | 6.0                   | 5.5                 | 2.3                        | 2.1                   | 1                   |
| Silicon                    | 4.69                 | 4.08                  | 3.85                | 0.151                      | 0.03                  | 0.017               |
| Tungsten                   | 3.31                 | 3.48                  | 3.76                | 2.47                       | 2.72                  | 2.95                |
| Plasma Silicon Nitride     | 2.07                 | 2.04                  | 2.01                | 0.004                      | 0                     | 0.002               |
| Aluminum                   | 0.618                | 0.958                 | 1.47                | 5.47                       | 6.69                  | 7.79                |
| Copper                     | 1.17                 | 0.9                   | 0.21                | 2.39                       | 2.6                   | 3.67                |
| Reference: Silicon Dioxide | 1.45                 | 1.45                  | 1.45                | 0.00                       | 0.00                  | 0.00                |

*Komuro* at Table 1; *see also, id.* at [0138].

### 2. *Motivation to Combine*

231. A POSITA would have found it obvious and been motivated to implement *Hwang-099*’s high refractive index material as “any one of single crystal

silicon, amorphous silicon, and polysilicon” at least because each type of silicon possesses a refractive index of 3.85, per Komuro. As I described above, Hwang-099 teaches that the silicon used in the embodiments described has a “refractive index of approximately 4.” *Hwang-099* at 9:29-33; *See* ¶ 155. A POSITA would understand that the refractive index of silicon is dependent on the wavelength of the light, as otherwise taught in Komuro, which provides in Table 1 the refractive indexes of silicon at various wavelengths (blue, green, and red light, with a refractive index range of 3.85-4.69). From Komura, and as otherwise known to a POSITA, the refractive index of silicon is therefore approximately 4. A POSITA desiring to utilize a silicon with a refractive index of approximately 4, per Hwang-099, would have found obvious to use a silicon including “single crystal silicon, amorphous silicon, and polysilicon,” as taught by Komura. Thus, a POSITA would have been motivated to use a known technique (e.g., types of silicon such as single crystal, amorphous, and polysilicon and image sensors having refractive index of approximately 4, namely 3.85) to improve similar devices (Hwang-099’s image sensor utilizing silicon with a refractive index of approximately 4) in the same way (selecting a specific silicon, per Komura). The modification is the combination of prior art elements (using one of single crystal silicon, amorphous silicon, and polysilicon) according to known methods to yield predictable results. Additionally, because the performance of Hwang-099’s Bragg reflectors is dependent on a difference in the

refractive indexes of the layers, a POSITA would have found obvious to use a material having a refractive index consistent with Hwang-099's refractive index of 4.

232. There would have been a reasonable expectation of success at least because each of single crystal silicon, amorphous silicon, and polysilicon were widely used in fabricating image sensors. *See, e.g., Ogawa* at 3:58-60 (“A silicon substrate 11 made of, for example, single crystal silicon...is provided in a CMOS image sensor[.]”); *Inuiya* at [0025] (“In the solid-state imaging device, each of the photoelectric conversion elements...are formed of amorphous silicon.”); *Mouli* at 2:57-59 (“Subsequently, a polysilicon deposition is used to fill the trench.”). Moreover, the modification would have been successful because single crystal silicon, amorphous silicon, and polysilicon each possess Hwang-099's desired refractive index of approximately 4 in the red wavelength.

## **XII. GROUND 5: CLAIMS 17-19 ARE OBVIOUS OVER HWANG-099 IN COMBINATION WITH MOULI AND/OR NOZAKI**

### **A. Claim 17[Pre]: “A *light trapping device*, comprising:”**

233. Hwang-099 teaches *a light trapping device*. *See* the above discussion at Claim 1[Pre], ¶¶ 132-134, incorporated herein.

### **B. 17[a]: “at least one light sensitive *pixel*”**

234. Hwang-099 teaches *at least one light sensitive pixel*. *See* the above discussion at Claim 1[a], ¶¶ 135-142, incorporated herein.

**C. 17[a][i]: “having a *light incident surface*, a *backside surface* opposite the light incident surface,”**

235. Hwang-099 teaches *having a light incident surface, a backside surface opposite the light incident surface*. See the above discussion at Claim 1[a][i], ¶¶ 143-145, incorporated herein.

**D. 17[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;”**

236. Hwang-099 teaches *a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. See the above discussion at Claim 1[a][ii], ¶¶ 146-153, incorporated herein.

**E. 17[b]: “a *backside light trapping material* substantially covering the backside surface; and”**

237. Hwang-099 teaches *a backside light trapping material substantially covering the backside surface*. See the above discussion at Claim 1[b], ¶¶ 154-158, incorporated herein.

**F. 17[c]: “a *peripheral light trapping material* substantially covering the peripheral sidewall,”**

238. By combining the embodiments of Hwang-099’s FIGS. 2 and 6, Hwang-099 renders obvious *a peripheral light trapping material substantially covering the peripheral sidewall*. See the above discussion at Claim 1[c], ¶¶ 159-169, incorporated herein.

**G. 17[c][i]: “wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface,”**

239. As I have described below, the combination of Hwang-099 and Mouli renders obvious the *backside light trapping material ... has a sloped surface at the pixel device interface*. Likewise, the requirement for the *peripheral light trapping material has a sloped surface at the pixel device interface* is further rendered obvious based on the combination of Hwang-099 and Nozaki.

**1. Mouli’s Teachings**

240. Mouli describes “isolation methods and devices for isolating regions of a semiconductor device[.]” *Mouli* at Abstract. Specifically, “[a]n anisotropic etch is performed into the silicon substrate 200 to create a deep trench 202,” and then an “oxide, i.e., silicon oxide or other dielectric liner 204 is grown or deposited on sidewalls 210 and bottom 220 of the trench 202.” *Mouli* at 4:45-49, 4:56-67.

241. Mouli also teaches that “high conical sidewalls without the use of high dose implants can create a good interface without defects for reduced dark current.” *Mouli* at 5:16-17. Thus, the sidewalls of Mouli’s trench are *sloped*, as seen FIG. 3B, and therefore provide a *sloped surface at the pixel device interface*:

*Sloped Surface of Peripheral Sidewall*

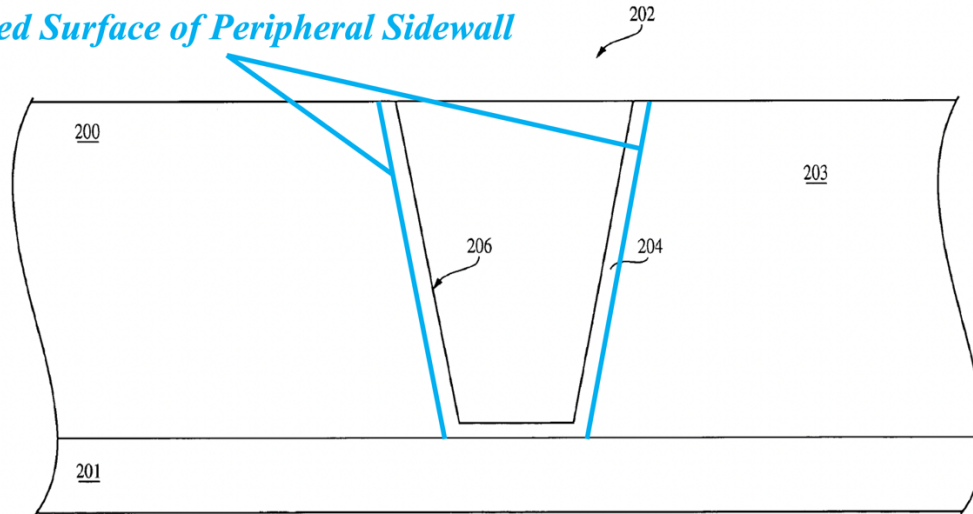


FIG. 3B

*Mouli* at FIG. 3B (annotated).

242. When modified according to *Mouli*'s sloped trench wall, Hwang-099's peripheral sidewall is sloped. The sidewall multi-layered reflection layer 220 (i.e., *peripheral light trapping material*) covering the sloped sidewall of Hwang-099-*Mouli* would be correspondingly sloped, at least because it covers the sloped surface of the sidewall. See ¶¶ 160-169. Thus, sidewall multi-layered reflection layer 220 (i.e., *peripheral light trapping material*) deposited on the sloped sidewall at the pixel device interface has a commensurate *sloped surface*.

## **2. Motivation to Combine Hwang-099 and Mouli**

243. A POSITA would have found it obvious and been motivated to incorporate *Mouli*'s *sloped* trench sidewalls into Hwang-099's pixel. It has been known since the 1970s that "in the case of vertical grooves" (i.e., trenches, and

correspondingly, sidewalls), the “dielectric filling deposition process results in a slightly thicker deposition near the top of the groove as opposed to the bottom of the groove,” which can result “in an overgrowth of the remaining narrow groove which results in poor dielectric material equality in the region below the overgrown area.” *See e.g., Bondur* at 5:7-15.

244. It was known that a “sloped sidewall” provides an “advantage over vertical sidewalls” by “reducing the tendency for voids to form” in “dielectric layer deposition.” *See e.g., Su* at [0035]. Thus, because it was known that sloped sidewalls reduced the tendency for voids to form during dielectric layer deposition, a POSITA would have understood that passivation of defects formed via etching would be significantly improved compared to vertical sidewalls and been motivated to modify Hwang-099’s peripheral sidewall (formed by groove 205 and trench 125) to be sloped, as taught by Mouli, so that the deposition of the silicon oxide layer 210 (dielectric layer deposition) would be improved compared to a vertical sidewall.

245. That is, a POSITA would have been familiar with the issues associated with vertical sidewalls, including damage to the silicon substrate and void formation in filling a trench, and would have been motivated to mitigate such issues by implementing Mouli’s sloped sidewalls.

246. Further, it was well-known that sloped sidewalls helped to increase “light collection efficiency and, hence, the amount of light absorbed” by an image

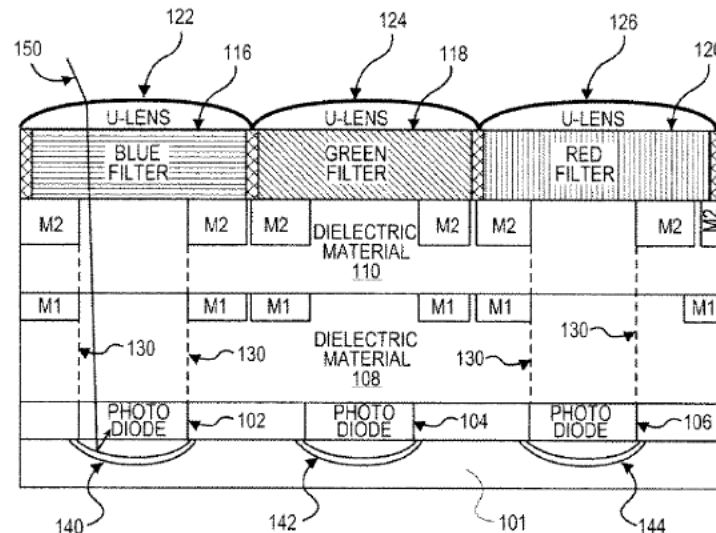
sensor. *See e.g., Street* at 10:55-59. Thus, a POSITA would have been further motivated to implement Mouli's sloped sidewalls into Hwang-099's device to further increase the light collection efficiency of the pixel. Specifically, A POSITA would have been motivated to apply a known technique (etching sloped sidewalls in trench isolation elements) to a known device (Hwang-099) ready for improvement.

247. The modification would have had a reasonable expectation of success at least because Hwang-099 already discloses etching trenches into the silicon substrate and that Mouli teaches etching sloped trenches. *See* ¶¶148, 240-241. Methods of etching sloped trenches into silicon were well-known. *See, e.g., Sung* at 2:60–3:36 (“Referring to FIG. 1C, the mask layer 102 and the spacer 108 are used as a hard mask, and a portion of the substrate 100 is removed, for example, by anisotropic etching to form a trapezoidal opening 110.”); *Su* at [0035] (“The etch process to form trenches 43, 44 preferably generates sloped sidewalls within substrate 40...”). Additionally, a POSITA would have appreciated that the figures of Mouli and other cited references are not to scale and would have understood how to make modifications to an image sensor to achieve desired operating functionality and using known manufacturing techniques.

### **3. *Nozaki's Sloped Backside Surface***

248. Nozaki teaches a pixel having a “an incident side for receiving incident light, a photosensitive region formed in the substrate, and a reflector having a

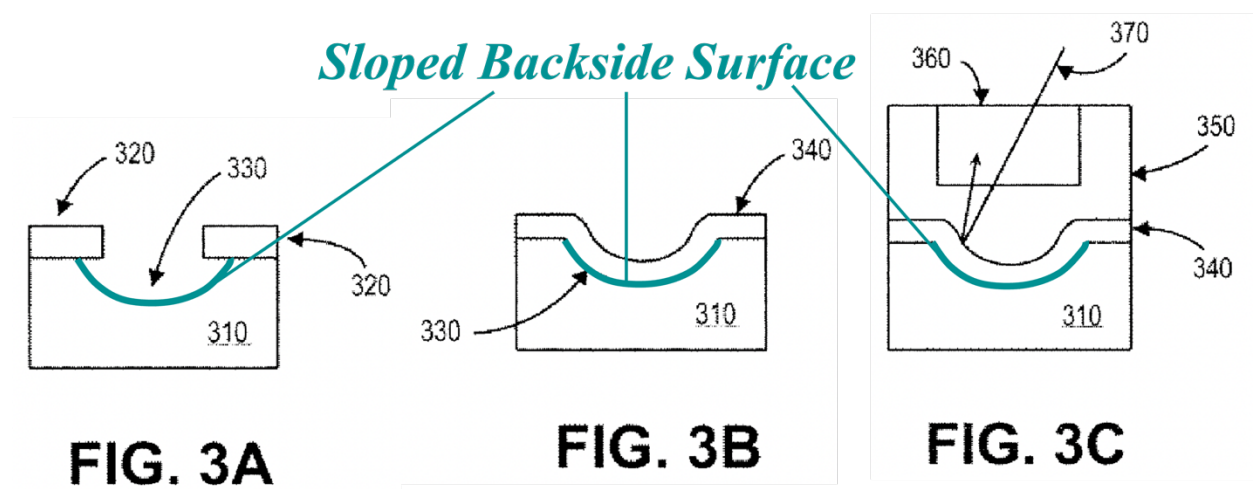
complex-shaped surface.” *Nozaki* at Abstract. “The reflector is formed in a portion of the substrate that is opposed to the incident side [(i.e., the reflector is formed on the *backside surface*)] such that light incident on the complex-shaped surface of the reflector is reflected towards the photosensitive region.” *Nozaki* at Abstract. FIG. 1 shows light entering through Nozaki’s light incident surface and reflecting back toward photodiode 207 after being incident on the curved backside reflector 270. *Nozaki* at FIG. 1. Specifically, reflectors 140, 142, and 144 “redirect the non-absorbed incident light towards the photodiode.” *Nozaki* at [0018], [0027], FIG. 1.



*Nozaki* at FIG. 1.

249. Nozaki teaches a *sloped backside surface*, and corresponding *sloped backside light trapping material* because, as shown in FIGS. 3A-3B, a “concave-shaped surface 330 [is] formed within substrate 310” (i.e., *sloped backside surface*) then a “reflective layer 340 is conformally deposited across the face of the concave-

shaped surface 330” (i.e., sloped *backside light trapping material*). *Nozaki* at 5:30-34. “The reflective layer 340 is typically a metal such as aluminum or tungsten.” *Nozaki* at 5:33-36. As can be seen in FIG. 3C, the concave-shaped surface is underneath a photodiode 360 and opposite a surface on which light is incident, thus making *Nozaki*’s concave-shaped surface a backside surface, which is *sloped*. *Nozaki* at 5:37-42.



*Nozaki* at FIGS. 3A-C.

250. In the combination of Hwang-099 and *Nozaki*, Hwang-099’s backside surface is modified to be sloped as taught by *Nozaki*. The backside light trapping material interfacing the (now modified) sloped backside surface at the pixel interface has a commensurate *sloped surface*.

251. The modification would have had a reasonable expectation of success at least because *Nozaki* discloses methods of manufacturing the concave-shaped backside surface and corresponding reflective layer. *Nozaki* at [0034]-0036].

#### 4. *Motivation to Combine Hwang-099 and Nozaki*

252. Based on the teachings of Nozaki, it would have been obvious to modify Hwang-099 to have a concave-shaped (i.e., *sloped*) backside surface. The modification would have resulted in Hwang-099's reflection layer 155a (*backside light trapping material*) being sloped. The complex shape of Nozaki's reflectors 140,142,144 allows for "multiple angles of reflection that reflect and focus incident light towards the photosensitive element[,]" thus expressly motivating the combination. *Nozaki* at [0027], [0019] ("reflector is shaped having multiple angles of reflection such that the incident light that has not been initially absorbed by the photodiode is focused and reflected towards the photodiode"). A POSITA would have also understood a *sloped backside light trapping material* would improve Hwang-099's image sensor "sensitivity" by "redirect[ing] the non-absorbed incident light towards the photodiode" to "increase the probability that the light will be absorbed[.]" *Nozaki* at 3:7-9; 4:42-43, FIG. 8. Additionally, the combination is the use of a known technique (implementing concave-shaped (sloped) backside reflectors) to improve similar image sensors in the same way.

253. This modification would have had a reasonable expectation of success given the method used to form concave-shaped surface 330 (an "isotropic etch" of a substrate before reflective layer 340 is "deposited across") was common in the art. *Nozaki* at 4:33-34, 5:25-32, FIG. 3A. Backside surfaces with a "complex shape (such

as a concave, convex, or trapezoidal shape)” were similarly well-known in the art. *See e.g., Tian* at 3:44-53, 4:40-50. Moreover, Hwang-099 already discloses a backside surface and methods for forming a backside light trapping material, Nozaki teaches methods of forming the concave-shaped surface, and because methods of providing sloped backside surfaces in pixels were well-known. *Hwang-099* at 8:28–9:34; *Nozaki* at [0034]-[0037].

**5. *Obviousness of Combining Both Mouli and Nozaki with Hwang-099***

254. A POSITA would have found obvious and been motivated to modify both Hwang-099’s backside surface (and commensurately, backside light trapping material on the backside surface) and peripheral sidewall (and commensurately, the peripheral light trapping material on the peripheral wall) to have a sloped surface, as the modification would have simply entailed combining the individual sloped surfaces and motivations discussed above, with the commensurate benefits and reasonable expectation of success. That is, the benefits achieved from each sloped surface modification would similarly be achieved in the combination including sloped surfaces for both the backside and peripheral light trapping materials. There would have been a reasonable expectation of success, as the peripheral and light trapping materials are distinct materials in the image sensor that would be independently formed to be sloped per the techniques discussed above.

- H. ***Claim [17][c][ii]: “and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.”***

255. Hwang-099 teaches *wherein light contacting the backside light trapping material and the peripheral light trapping material is reflected back toward the pixel*. See the above discussion at Claim 1[d], ¶¶ 193-197, incorporated herein.

- I. ***Claim 18: “The device of claim 17, wherein the peripheral sidewall extends completely around the pixel periphery.”***

256. As discussed above, the *peripheral sidewall* of Hwang-099 *extends completely around the pixel periphery*. See Claims 1[a][ii], 4 (incorporated herein).

- J. ***Claim 19: “The device of claim 17, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”***

257. As discussed above, the *peripheral sidewall* of Hwang-099 *extends from the light incident surface to the backside surface*. See Claims 1[a][ii], 5 (incorporated herein).

### **XIII. GROUND 6: CLAIM 20 IS OBVIOUS OVER HWANG-099 IN COMBINATION WITH MOULI AND/NOZAKI AND FURTHER IN VIEW OF KONNO**

- A. ***Claim 20: “The device of claim 17, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”***

258. As discussed above, Hwang-099 in view of Mouli and/or Nozaki renders obvious claim 20. See Claim 17[c][i].

## **1. Konno's Teachings**

259. As discussed above, Konno teaches a metal layer as the *backside light trapping material*. See Claim 6 for Konno's teachings, ¶¶ 207-208 (incorporated herein).

## **2. Motivation to Combine**

260. Based on the teachings of Konno, it would have been obvious to replace Hwang-099's base multi-layered reflection layer 155a (i.e., *backside light trapping material*) with a *metal layer*. Using metal as reflectors in pixels was a common practice well before the '764 Patent. See, e.g., Cao at Abstract ("The back reflector structure consists of...a first textured metal...such as aluminum."). A POSITA would have understood that various metals were used in backside light trapping materials. See, e.g., Nozaki at [0035] ("The reflective layer 340 is typically a reflective metal such as aluminum or tungsten."). Compared to Bragg reflectors, a metal layer would have offered more broadband reflectivity, as metals typically have higher reflectivity than other materials. Indeed, a "pure silver layer is the most highly reflective material having an integrated total reflectivity of about 95% or higher over the wavelength range from 600 nm to 1200 nm." See e.g., Cao at [0006]. Bragg reflectors, on the other hand, were known to function at a "targeted wavelength." See e.g., Hong at [0027]. Accordingly, "metallic reflectors offer the advantage of high reflectivity in thin films." See e.g., Holm at 8:11:12. The ability to offer "high

reflectivity in thin films” using metal layers is an advantage over Bragg reflectors because “multiple layer pairs are typically required to achieve sufficient reflectivity” with their use. *See e.g., Holm* at 8:17-19.

261. A POSITA would have recognized it would be easier using just one metal layer, per Konno, compared to designing to designing a Bragg reflector where multiple layer pairs are required. Thus, a POSITA would have been motivated to improve similar image sensors in the same way to predictably result in the simplification in the manufacturing process and increased broadband light reflectivity. Such a combination is a simple substitution of one known element (e.g., metal layer as a backside light trapping material) for another (e.g., a Bragg reflector as a backside light trapping material).

262. There would have been a reasonable expectation of success in implementing Konno’s metal second reflecting layer 120 in Hwang-099’s image sensor because Konno describes how to form reflecting layer 120. *Konno* at 11:42-56 (“[T]he first reflecting layer is manufactured by forming a film with a metal such as aluminum or silver by, for example, the deposition method. The second reflecting layer 120 can be manufactured in the same manner as that for the first reflecting layer 121.”). Moreover, methods of forming metal layers were well-known and within the expertise of a POSITA. *See* ¶ 211; *see also e.g., Yamada* at 7:1-2 (“The reflecting film 12a is formed by, for example, vapor deposition of a metal film.”);

*Atwater* at [0054] (“Metallic layer 230 may be deposited by a vapor deposition process, such as a vacuum evaporation process, a PVD or sputtering process, a CVD process, or an ALD process.”); *Kim* at [0023] (“Reflective film layer 106A can be made of a metal material and can be formed by any metal film deposition method for forming a metal film[.] Preferably, reflective film 106A can be formed by a chemical vapor deposition (CVD) method or a physical vapor deposition (PVD) method.”).

263. Additionally, in Hwang-099’s image sensor, circuitry such as gate electrode 140, first and second contact plugs 170, 185, and lines 175, 190, are provided on the backside of the pixel, which further includes insulating layer 200. *Hwang-099* at FIG. 2, 7:5-12, 7:64–8:16. In the combination of Hwang-099 and Konno that includes a metal layer on the backside surface, a POSITA would have also known to evaluate the design of the image sensor for the potential need to add an insulating material between the metal layer and any electrically conductive components, such as Hwang-099’s electronic circuitry (140, 170, 175, etc.).

#### **XIV. GROUND 7: CLAIMS 16, 21-24 ARE OBVIOUS OVER HWANG-099 IN COMBINATION WITH KONNO**

A. *Claim 16: “The device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”*

264. As discussed above, Hwang-099 teaches claim 16. *See* Claim 8.

## **1. Konno's Teachings**

265. As discussed above, Konno teaches a metal layer as the *backside light trapping material*. See Claim 6 for Konno's teachings, ¶¶ 207-208 (incorporated herein).

## **2. Motivation to Combine**

266. Based on the teachings of Konno, it would have been obvious to replace Hwang-099's base multi-layered reflection layer 155a (i.e., *backside light trapping material*) with a metal layer. Using metal as reflectors in pixels was a common practice well before the '764 Patent. See, e.g., *Cao* at Abstract ("The back reflector structure consists of...a first textured metal...such as aluminum."). A POSITA would have understood that various metals were used in backside light trapping materials. See, e.g., *Nozaki* at [0035] ("The reflective layer 340 is typically a reflective metal such as aluminum or tungsten."). Compared to Bragg reflectors, a metal layer would have offered more broadband reflectivity, as metals typically have higher reflectivity than other materials. Indeed, a "pure silver layer is the most highly reflective material having an integrated total reflectivity of about 95% or higher over the wavelength range from 600 nm to 1200 nm." See e.g., *Cao* at [0006]. Bragg reflectors, on the other hand, were known to function at a "targeted wavelength." See e.g., *Hong* at [0027]. Accordingly, "metallic reflectors offer the advantage of high reflectivity in thin films." See e.g., *Holm* at 8:11:12. The ability to offer "high

reflectivity in thin films” using metal layers is an advantage over Bragg reflectors because “multiple layer pairs are typically required to achieve sufficient reflectivity” with their use. *See e.g., Holm* at 8:17-19.

267. A POSITA would have recognized that using just one metal layer, per Konno, compared to the multiple layer pairs required by a Bragg reflector would reduce manufacturing cost and complexity. Thus, a POSITA would have been motivated to improve similar image sensors in the same way to predictably result in the simplification in the manufacturing process and increased broadband light reflectivity. Such a combination is a simple substitution of one known element (e.g., metal layer as a backside light trapping material) for another (e.g., a Bragg reflector as a backside light trapping material).

268. There would have been a reasonable expectation of success in implementing Konno’s metal second reflecting layer 120 in Hwang-099’s image sensor because Konno describes how to form reflecting layer 120. *Konno* at 11:42-56 (“[T]he first reflecting layer is manufactured by forming a film with a metal such as aluminum or silver by, for example, the deposition method. The second reflecting layer 120 can be manufactured in the same manner as that for the first reflecting layer 121.”). Moreover, methods of forming metal layers were well-known and within the expertise of a POSITA. *See* ¶ 211; *see also e.g., Yamada* at 7:1-2 (“The reflecting film 12a is formed by, for example, vapor deposition of a metal film.”);

*Atwater* at [0054] (“Metallic layer 230 may be deposited by a vapor deposition process, such as a vacuum evaporation process, a PVD or sputtering process, a CVD process, or an ALD process.”); *Kim* at [0023] (“Reflective film layer 106A can be made of a metal material and can be formed by any metal film deposition method for forming a metal film[.] Preferably, reflective film 106A can be formed by a chemical vapor deposition (CVD) method or a physical vapor deposition (PVD) method.”).

269. Additionally, in Hwang-099’s image sensor, circuitry such as gate electrode 140, first and second contact plugs 170, 185, and lines 175, 190, are provided on the backside of the pixel, which further includes insulating layer 200. *Hwang-099* at FIG. 2, 7:5-12, 7:64–8:16. In the combination of Hwang-099 and Konno that includes a metal layer on the backside surface, a POSITA would have also known to evaluate the design of the image sensor for the potential need to add an insulating material between the metal layer and any electrically conductive components, such as Hwang-099’s electronic circuitry (140, 170, 175, etc.).

**B. *Claim 21***

270. There are two alternative mappings for Claim 21, both relying on a combination of Hwang-099 and Konno. In the first mapping (i.e., following) of Claim 21, Hwang-099 is modified to comprise Konno’s textured transparent layer 136 from Konno’s second embodiment depicted in Figure 7. In the combination,

Hwang-099 is modified such that transparent layer 136 is placed between Hwang-099's *backside surface* and base multi-layered reflection layer 155a (*backside light trapping material*).

**C. Claim 21[Pre]: “A *light trapping device*, comprising:”**

271. Hwang-099 teaches *a light trapping device*. See the above discussion at Claim 1[Pre], ¶¶ 132-134, incorporated herein.

**D. 21[a]: “at least one light sensitive *pixel*”**

272. Hwang-099 teaches *at least one light sensitive pixel*. See the above discussion at Claim 1[a], ¶¶ 135-142, incorporated herein.

**E. 21[a][i]: “having a *light incident surface*, a *backside surface* opposite the light incident surface,”**

273. Hwang-099 teaches *having a light incident surface, a backside surface opposite the light incident surface*. See the above discussion at Claim 1[a][i], ¶¶ 143-145, incorporated herein.

**F. 21[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;”**

274. Hwang-099 teaches *a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. See the above discussion at Claim 1[a][ii], ¶¶ 146-153, incorporated herein.

G. 21[b]: “a *backside light trapping material* substantially covering the *backside surface*;

275. Hwang-099 teaches *a backside light trapping material substantially covering the backside surface*. See the above discussion at Claim 1[b], ¶¶ 154-158, incorporated herein.

H. 21[c]: “a *peripheral light trapping material* substantially covering the *peripheral sidewall*; and”

276. By combining the embodiments of Hwang-099’s FIGS. 2 and 6, Hwang-099 renders obvious *a peripheral light trapping material substantially covering the peripheral sidewall*. See the above discussion at Claim 1[c], ¶¶ 159-169, incorporated herein.

I. 21[d]: “a *textured layer* positioned to interact with light proximal to the backside surface,”

1. *Konno’s Teachings*

277. As shown in FIG. 7 below, Konno teaches a transparent layer 136 that comprises “concaves and convexes” (i.e., is a *textured layer*). *Konno* at 14:42-45. Transparent layer 136 is shown as underneath the backside surface of Konno’s photoelectric conversion film 135 and on top of Konno’s second reflecting layer 120. *Konno* at FIG. 7. Transparent layer 136 “is formed from a material which transmits photons, for example, glass and plastics such as acrylic resins.” *Konno*, 9:35-37.

278. These “concaves and convexes may be regular concaves and convexes or irregular concaves and convexes” and may be formed “by a known technique such

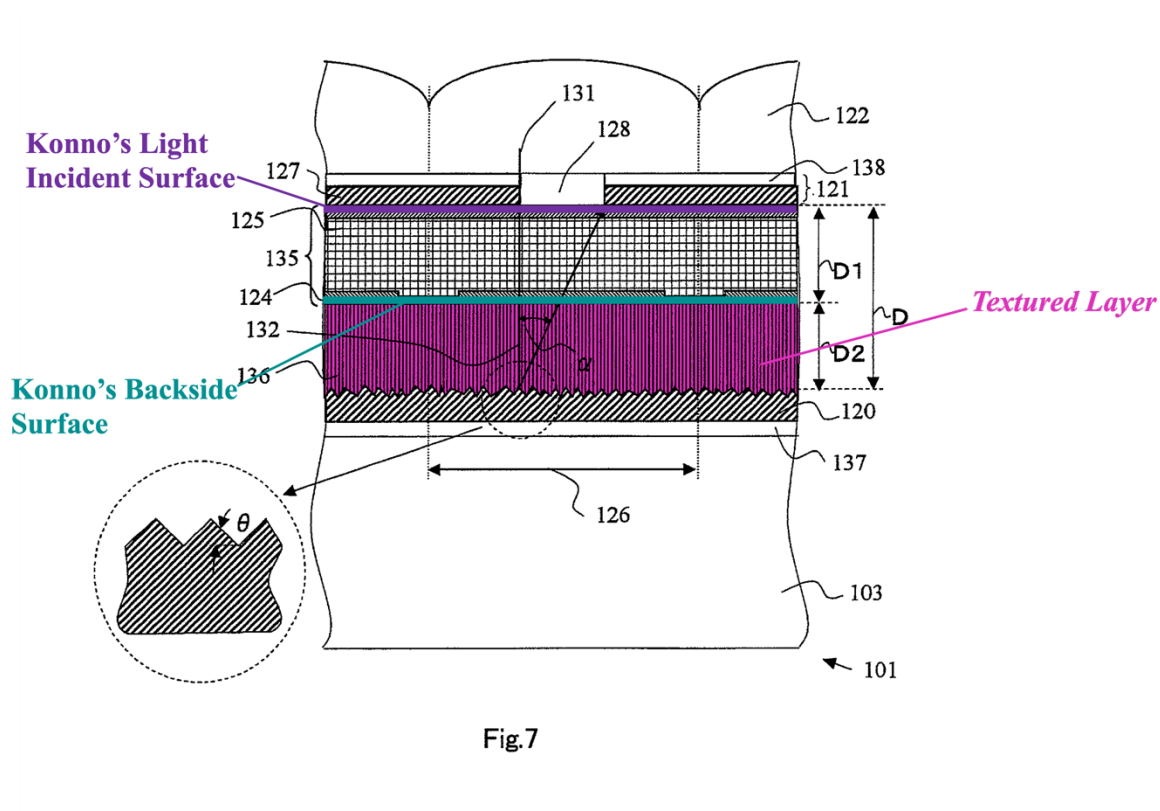
as sputtering and microlithography, *Konno* at 14:62-63, 14:42-45, Figure 7. I note that the '764 Patent describes that a textured surface can be “formed by...lithographic patterning.” '764 Patent at 4:29-35. Because Konno's textured layer is formed by microlithography (i.e., lithographic patterning), transparent layer 136 is a “textured layer” as contemplated by the '764 Patent.

279. A POSITA would have understood that Konno's transparent layer 136 (*textured layer*) *interacts with light proximal to the backside surface*. I note that the '764 Patent describes that “light entering the pixel that is not absorbed will interact with and be reflected internally...” '764 Patent at 12:1-2. Thus, Konno's transparent layer 136 *interact[s]* with light because it does not absorb it. Instead, because Konno's transparent layer 136 is comprised of a “material which transmits photons,” light is transmitted through transparent layer 136, as illustrated in FIG. 7. *Konno* at 9:35-37; FIG. 7. Also depicted in FIG. 7 is light transmitting through transparent layer 136 underneath the bottom of photoelectric conversion element 135 (i.e., the backside surface of Konno). Because transparent layer 136 (*textured layer*) transmits light photons underneath photoelectric conversion element 135, Konno's *textured layer* *is positioned to interact with light proximal to the backside surface*.

280. Konno's *textured layer* *is positioned to interact with light proximal to the backside surface* also because light is reflected by the concaves and convexes of transparent layer 136, as shown below in FIG. 7. “Furthermore, the photodetector of

this embodiment also has an effect that the transparent layer 136 can provide concaves and convexes which realizes a large reflection angle[.]” *Konno* at 15:2-5. Because transparent layer 136 reflects light up toward photoelectric conversion element 135, and is located underneath the backside surface, transparent layer 136 (*textured layer*) is positioned to interact with light proximal to the backside surface.

I note that Figures may not be to scale.



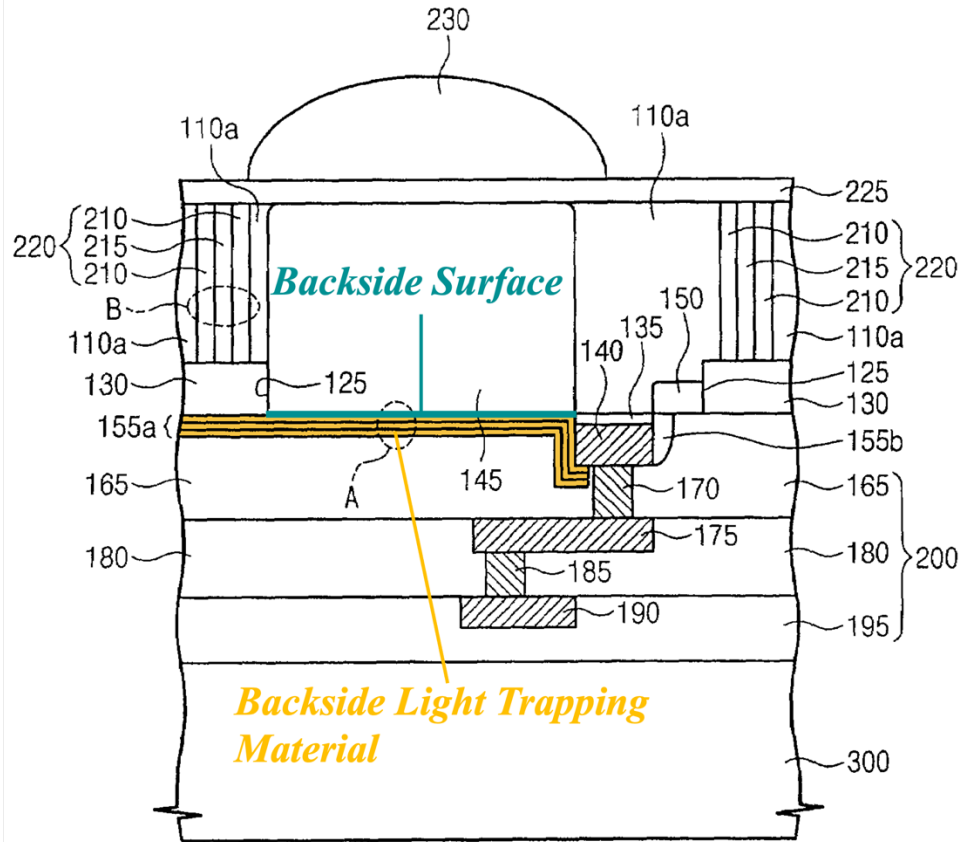
*Konno* at FIG. 7 (illustrating transparent layer 136 (*textured layer*) between the bottom of photoelectric conversion film 135 and second reflecting layer 120 and transmitting and reflecting light underneath photoelectric conversion element 135).

## 2. *Motivation to Combine*

281. A POSITA would have found and obvious and been motivated to include Konno's transparent layer 136 underneath the backside surface of Hwang-099's *pixel* and on top of the base multi-layered reflection layer 155a (*backside light trapping material*). In the combination, the transparent layer 136 (*textured layer*) is located underneath Hwang-099's *backside surface*, between it and the backside light trapping material. *Hwang-099* at Figure 2.

282. Because transparent layer 136 is underneath Hwang-099's backside surface, transparent layer 136 (*textured layer*) would transmit and reflect light that is incident on the backside surface. Thus, in the combination, a POSITA would have understood that because transparent layer 136 (*textured layer*) is positioned underneath the backside surface and does not absorb light and instead transmits and reflects light, that *is positioned to interact with light proximal to the backside surface*.

Fig. 2



Hwang-099 at FIG. 2 (illustrating the *backside surface backside light trapping material*, between which transparent layer 136 (*textured layer*) would be placed).

283. A POSITA would have known that providing a textured layer as taught by Konno on the backside surface would have offered the benefit of “provid[ing] a diffuse reflecting surface which increases the path length of the reflected light and also[] provide for enhanced internal reflection.” *Banerjee* at 1:26-29. Compared to smooth surfaces which provide specular reflection, light incident on a “textured back

reflector” is “scattered in addition to being redirected” through the active region of a photovoltaic device. *Nath* at 2:63–3:21. Indeed, “light trapping structures” in solar cells including “randomly textured surfaces” were known to “increase the optical path length of the incident light, due to...light scattering on textured surfaces at oblique angles[.]” *Sai* at p. 2. A POSITA would further understand that increasing the path length of light advantageously enhances quantum efficiency, because as the path length of light increases, the probability of light absorption increases. *See, e.g., Mallick* at p. 456 (...diffraction of light to increase optical path length contribute[s] to absorption enhancement in the a-Si cell.”)

284. Thus, a POSITA would have been motivated to modify Hwang-099 to include Konno’s transparent layer 136 (textured layer) such that light incident on the backside surface would be diffusely reflected instead of specularly reflected. The modification is the application of a known technique (providing a textured layer) to a known device (image sensor) in the same way. The modification would have predictably improved Hwang-099’s image sensor by working in conjunction with base multi-layer reflection layer 155a and enhancing internal reflection of light incident on the backside surface, thereby increasing quantum efficiency.

285. The modification would have had a REOS at least because it would have merely required depositing Konno’s transparent layer 136 on the backside surface of Hwang-099 prior to the formation of base multi-layered reflection layer

155a and/or a POSITA would have possessed the necessary skills to implement layer 136 into Hwang-099's manufacturing process. Additionally, Konno teaches how to form the texture (i.e., by microlithography or sputtering). *Konno* at 14:42-45.

286. A POSITA would have also understood that base multi-layered reflection layer 155a would have still been able to be formed on the textured surface of transparent layer 136. As described above, the first layer of Hwang-099's reflection layer 155 is a silicon oxide. Thus, a POSITA would have merely needed to form Hwang-099's silicon oxide form on the surface of transparent layer 136 and continue with the manufacturing process. Techniques to form a silicon oxide layer on a textured surface were known and it was well within the skills of a POSITA to it. *See, e.g., Smith* at 3:31-39, 3:58-65.

287. Additionally, transparent layer 136 (*textured layer*) would not impact the ability of Hwang-099's base multi-layered reflection layer 155a to reflect light back toward the *pixel* because each of the layers 151/152 having different refractive indexes would still be present in the combination, and light contacting base multi-layered reflection layer 155a would still be reflected at the boundary surfaces present in base multi-layered reflection layer 155a.

**J. 21[d][i]: “wherein light contacting the *backside light trapping material* or the *peripheral light trapping material* is reflected back toward the pixel.”**

288. Hwang-099 teaches *wherein light contacting the backside light trapping material and the peripheral light trapping material is reflected back toward the pixel*. See the above discussion at Claim 1[d], ¶¶ 193-197, incorporated herein.

**K. Claim 21**

**1. Explanation of Combination and Motivation for the Combination**

289. The following mapping of Claim 21 also relies on Hwang-099 and Konno. In this mapping, Hwang-099 is modified to comprise Konno’s combined textured transparent layer 136 and textured second reflecting layer 120 in the second embodiment depicted in FIG. 7. As I discuss below, a POSITA would have been motivated and found it obvious to replace Hwang-099’s base multi-layered reflection layer 155a (*backside light trapping material*) with Konno’s combined transparent layer 136 and second reflecting layer 120 in the FIG. 7 embodiment to leverage the combined benefits of both layers.

290. First, a POSITA would have found it obvious and been motivated to implement Konno’s textured second reflecting layer 120. Second reflecting layer 120 is formed of a metal such as “aluminum or silver.” *Konno* at 14:41-41, 11:42-52. As I have discussed previously, metal layers as backside light trapping materials

were well-known and provided many advantages. *See* ¶¶ 260-261. Specifically, metal layers were known to offer more broadband reflectivity because metals have higher reflectivity than other materials. *See* ¶¶ 260-261. Indeed, a “pure silver layer is the most highly reflective material having an integrated total reflectivity of about 95% or higher over the wavelength range from 600 nm to 1200 nm.” *See, e.g., Cao* at [0006]. Further, having a metal layer would offer the advantage of achieving “high reflectivity in thin films” versus a Bragg reflector where “multiple layer pairs are typically required to achieve sufficient reflectivity.” *See, e.g., Holm* at 8:17-19; ¶¶ 260. Thus, a POSITA would have recognized the advantage of implementing Konno’s second reflecting layer 120.

291. A POSITA would have also recognized that a textured metal layer, compared to a non-textured metal layer, would provide the same advantages that I discussed above. *See* ¶¶ 283. Specifically, layers having textured surfaces were known to reflect light diffusely versus specularly, which increases the path length of incident light and thereby increases the probability of light absorption. *See* ¶¶ 283. Thus, a POSITA would have recognized that Konno’s textured metal second reflecting layer 120 (as opposed to a textured layer alone or a metal layer alone) would simultaneously provide the advantages of both types of layers. Accordingly, a POSITA would have been motivated and found it obvious to implement Konno’s textured metal second reflecting layer 120 into Hwang-099’s image sensor.

292. Second, a POSITA would have found it obvious and been motivated include Konno's textured transparent layer 136 in the combination. A POSITA would have recognized that because transparent layer 136 comprises "concaves and convexes of various sizes" (i.e., is a *textured layer*) that it too would diffusely reflect light and provide the advantages associated with textured layers that I discussed above. *Konno* at 15:3-5, 9-11; See ¶¶ 283. Additionally, a POSITA would have recognized that including Konno's textured transparent layer 136 alongside second reflecting layer 120 would have provided the benefits of having a textured layer without the surface of the Hwang-099's *pixel* (pixel semiconductor pattern 110a with photodiode 145 disposed therein) having to be textured. Konno expressly teaches that having transparent layer prevents the photosensitive portion of Konno having to be textured, which would cause problems such as "increase in the dark current, generation of uneven electric field in the photoelectric conversion film 125, generation of trap of electric charge by energy level produced on the surface of photoelectric conversion film 125, uneven characteristics and variation thereof among the elements 110, [and] generation of cross-talk between the elements 110." *Konno* at 15:17-22. A POSITA would have similarly recognized that including textured transparent layer 136 in Hwang-099 would avoid issues associated with texturing the surface of Hwang-099's *pixel*. Indeed, it was known that "the surface state of the substrate is closely related to the photovoltaic characteristics of a

semiconductor film formed thereupon, and as the roughness of the substrate surface increases, the characteristics of the semiconductor film decrease.” *See, e.g., Matsuyama* at 2:38-49. Additionally, it was known that “metals can diffuse into the semiconductor of the devices in which they are employed, and in doing so, adversely affect the photoresponsive characteristics of the devices.” *See, e.g., Czubatji* at 5:9-13. Accordingly, a POSITA would have been motivated include textured transparent layer 136 between Hwang-099’s *backside surface* and textured metal second reflecting layer 120 to preserve the integrity of Hwang-099’s *pixel* and prevent diffusion of metal into the semiconductor substrate.

293. In the combination, transparent layer 136 is the ***textured layer***, as recited by Claim 21[d], and second reflecting layer 120 is the ***backside light trapping material***, as recited by Claim 21[b]. The modification would have been straightforward and merely required depositing Konno’s transparent layer 136 on Hwang-099’s *backside surface*, texturing the transparent layer 136 using microlithography or sputtering, as taught by Konno, and depositing a metal layer thereupon. *Konno* at 14:38-45. As I discussed above, metal was widely available material and techniques for depositing metal layers were well-known. *See* ¶¶ 266-268. Additionally, methods of texturing materials were well-known. *See, e.g., Konno* at 14:38-45; *Smith* at 3:31-35. A POSITA would have possessed the necessary skills to implement both transparent layer 136 and second reflecting layer 120 in Hwang-

099's image sensor. Thus, the modification would have had a reasonable expectation of success. The modification is nothing more than the combination of prior art elements (textured layer, metal backside layer) using known methods (microlithographic texturing, material deposition) to obtain predictable results (improved reflectivity of light).

**L. Claim 21[Pre]: “A *light trapping device*, comprising:”**

294. Hwang-099 teaches *a light trapping device*. See the above discussion at Claim 1[Pre], ¶¶ 132-134, incorporated herein.

**M. 21[a]: “at least one light sensitive *pixel*”**

295. Hwang-099 teaches *at least one light sensitive pixel*. See the above discussion at Claim 1[a], ¶¶ 135-142, incorporated herein.

**N. 21[a][i]: “having a *light incident surface*, a *backside surface* opposite the light incident surface,”**

296. Hwang-099 teaches *having a light incident surface, a backside surface opposite the light incident surface*. See the above discussion at Claim 1[a][i], ¶¶ 143-145, incorporated herein.

**O. 21[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;”**

297. Hwang-099 teaches *a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery*. See the above discussion at Claim 1[a][ii], ¶¶ 146-153, incorporated herein.

P. 21[b]: “a **backside light trapping material** substantially covering the backside surface;”

1. *Hwang-099’s Teachings*

298. As described above, Hwang-099’s base multi-layered reflection layer 155a is a backside light trapping material substantially covering the backside surface. *See* Claim 1[b]. However, as described below, a POSITA would have found it obvious to replace Hwang-099’s base multi-layered reflection layer with Konno’s metal second reflecting layer 120 in the second embodiment of FIG. 7.

2. *Konno’s Teachings*

299. I note that previous combinations with Konno rely on the first embodiment of FIG. 3 of Konno. *See* Claims 6, 16, and 20. The following analysis instead relies on Konno’s second embodiment, which is described with reference to FIG. 7.

300. Konno specifically teaches first and second reflecting layer 121 and 120, respectively, which function to “confine[] photons which entered into the solid-state imaging element 110[.]” *Konno* at 8:31-33.

301. “Photons which entered into the solid-state imaging element from the light entrance window 128...reach the photoelectric conversion film 135, and a part of them are absorbed and cause photoelectric conversion[.]” *Konno* at 9:28-32. “The photons not absorbed by the photoelectric conversion film 125 transmit the pixel electrode 124 and the transparent layer 136, and reach the second reflecting layer

120.” *Konno* at 9:64-67. The photons that reach the second reflecting layer 120 “are reflected by the mirror surface of the second reflecting layer 120...and reach the photoelectric conversion film 125.” *Konno* at 9:67–10:4.

302. That is, the second reflecting layer 120 reflects photons that are incident on it back toward the photoelectric conversion element, as illustrated in FIG. 7. Compared to FIG. 3, “the shape of the second reflecting layer 120 differs from that of the first embodiment.” *Konno* at 13:57-59. “That is, the second reflecting layer 120 of this embodiment has a plurality of convexes and concaves on the reflecting surface.” *Konno* at 13:60-63, Figure 7. Thus, Konno’s second reflecting layer 120 is textured and “formed by forming a thin film of metal such as aluminum or silver by deposition” *Konno* at 8:35-38, 11:42-52. In the second embodiment, second reflecting layer 120 is deposited on “concaves and convexes on the surface of the transparent layer 136.” *Konno* at 14:38-45. As shown in FIG. 7 below, second reflecting layer 120 extends completely along the length of the bottom of photoelectric conversion element 135 (i.e., Konno’s backside surface) and therefore, is a *backside light trapping material substantially covering the backside surface*. It makes sense within the context of Konno that second reflecting layer 120 completely (i.e., substantially) covers the backside surface of photoelectric conversion element 135 because Konno is concerned with confining light photons within photoelectric conversion element 135. *See, e.g., Konno* at 8:31-33, 14:35-37. If second reflecting

Figure 1 is a cross-sectional view of a multi-layered structure 101. The structure includes a top layer 122, a middle section 125, and a bottom layer 120. The middle section 125 contains a grid-like pattern 135 and a wavy line 132. A dashed line 126 indicates a horizontal boundary. A vertical line 128 is shown. Dimensions D1 and D2 are indicated. An inset shows a magnified view of the wavy line 132 with an angle  $\theta$ .

*Konno* at FIG. 7 (illustrating the metal second reflecting layer 120 having concaves and convexes).

303. See ¶¶ 289-293. In the combination, Hwang-099's base multi-layered reflection layer 155a (*backside light trapping material*) is replaced with Konno's metal second reflecting layer 120. Because Hwang-099's layer 155a is replaced with Konno's layer 120 (*backside light trapping material*), Hwang-099's *backside surface is substantially covered by the backside light trapping material*.

**Q. 21[c]: “a peripheral light trapping material substantially covering the peripheral sidewall; and”**

304. By combining the embodiments of Hwang-099’s FIGS. 2 and 6, Hwang-099 renders obvious *a peripheral light trapping material substantially covering the peripheral sidewall*. See the above discussion at Claim 1[c], ¶¶ 159-169, incorporated herein.

**R. 21[d]: “a textured layer positioned to interact with light proximal to the backside surface,”**

**1. Konno’s Teachings**

305. As shown in FIG. 7 below, Konno teaches a transparent layer 136 that comprises “concaves and convexes” (i.e., is a *textured layer*). *Konno* at 14:42-45. Transparent layer 136 is shown as underneath the backside surface of Konno’s photoelectric conversion film 135 and on top of Konno’s second reflecting layer 120. *Konno* at FIG. 7. Transparent layer 136 “is formed from a material which transmits photons, for example, glass and plastics such as acrylic resins.” *Konno* at 9:35-37.

306. These “concaves and convexes may be regular concaves and convexes or irregular concaves and convexes” and may be formed “by a known technique such as sputtering and microlithography, *Konno* at 14:62-63, 14:42-45, Figure 7. I note that the ’764 Patent describes that a textured surface can be “formed by...lithographic patterning.” ’764 Patent at 4:29-35. Because Konno’s textured layer is formed by microlithography (i.e., lithographic patterning), transparent layer 136 is a “textured layer” as contemplated by the ’764 Patent.

307. A POSITA would have understood that Konno's transparent layer 136 (*textured layer*) *interacts with light proximal to the backside surface*. I note that the '764 Patent describes that "light entering the pixel that is not absorbed will interact with and be reflected internally..." '764 Patent at 12:1-2. Thus, Konno's transparent layer 136 *interact[s]* with light because it does not absorb it. Instead, because Konno's transparent layer 136 is comprised of a "material which transmits photons," light is transmitted through transparent layer 136, as illustrated in FIG. 7. *Konno* at 9:35-37; FIG. 7. Also depicted in FIG. 7 is light transmitting through transparent layer 136 underneath the bottom of photoelectric conversion element 135 (i.e., the backside surface of Konno). Because transparent layer 136 (*textured layer*) transmits light photons underneath photoelectric conversion element 135, Konno's *textured layer* is positioned to interact with light proximal to the backside surface.

308. Konno's *textured layer* is positioned to interact with light proximal to the backside surface also because light is reflected by the concaves and convexes of transparent layer 136, as shown below in FIG. 7. "Furthermore, the photodetector of this embodiment also has an effect that the transparent layer 136 can provide concaves and convexes which realizes a large reflection angle[.]" *Konno* at 15:2-5. Because transparent layer 136 reflects light underneath the backside surface, transparent layer 136 (*textured layer*) is positioned to interact with light proximal to the backside surface. I note that Figures may not be to scale.

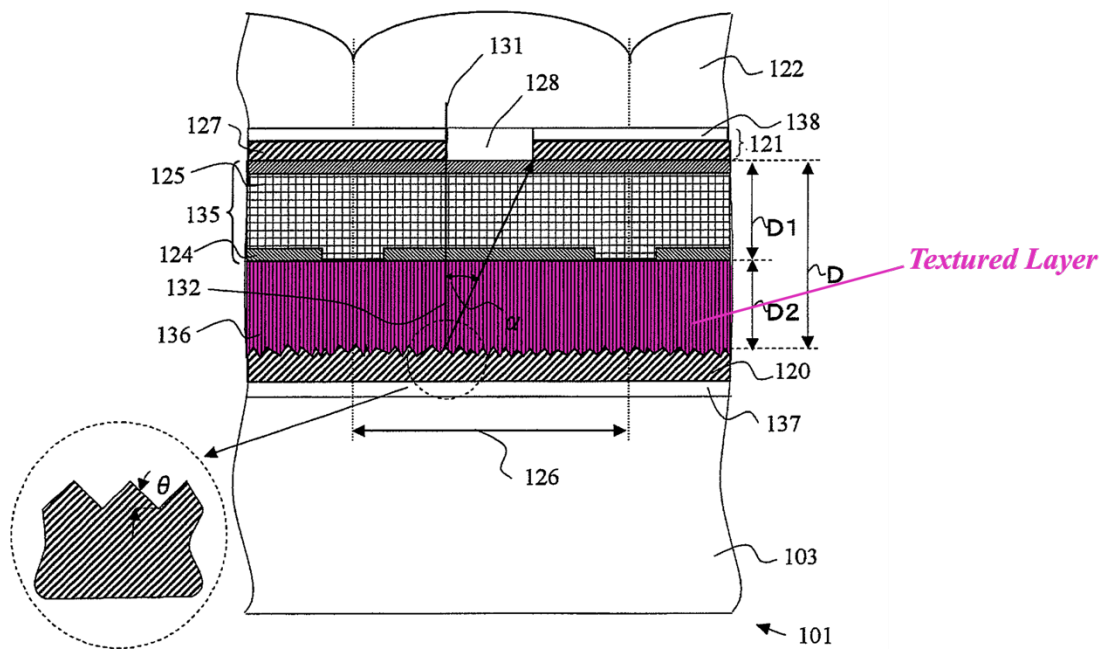


Fig.7

Konno at FIG. 7 (illustrating transparent layer 136 (*textured layer*) between the bottom of photoelectric conversion film 135 and second reflecting layer 120 and transmitting and reflecting light underneath photoelectric conversion element 135).

## 2. Motivation to Combine

309. See ¶¶ 289-293. In the combination, Konno's transparent layer 136 is located underneath Hwang-099's *backside surface* and on top of metal second reflecting 120 (*backside light trapping material*, per the combination at Claim 21[b]). See ¶¶ 298-303.

S. 21[d][i]: “wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.”

310. Hwang-099 teaches wherein light contacting...the peripheral light trapping material is reflected back toward the pixel. See Claim 1[d] (incorporated herein.

311. Recall that at 21[b], Hwang-099 is modified to comprise Konno’s second reflecting layer 120. See ¶¶ 298-303. Regarding second reflecting layer 220, Konno expressly teaches that it reflects incident light photons. *Konno* at 13:63-65. Specifically, “when it [second reflecting layer 120] the incident photons 132, it can thereby reflect them with a large amount of horizontal components, in other words, it can reflect them with a large reflection angle.” *Konno* at 12:63-66. The reflection of incident light is shown in FIG. 7 of Konno, where it can be seen that reflected light reflects off second reflecting layer 120 and is redirected back toward photoelectric conversion film 135. *Konno* at FIG. 7.

312. In the combination, because second reflecting layer 120 is underneath Hwang-099’s backside surface, light contacting second reflecting layer would similarly be reflected back up toward photodiode 145 in pixel semiconductor pattern 110a (the claimed pixel). See ¶ 295. Thus, in the above combination of Hwang-099-Konno, *light contacting the backside light trapping material...is reflected back toward the pixel.*

**T. Claim 22: “The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.”**

313. In both above mappings of Hwang-099-Konno, transparent layer 136 (textured layer) is located underneath the *backside surface* and on top of the *backside light trapping material*. In other words, in the first mapping of Hwang-099-Konno, transparent layer 136 is located underneath Hwang-099’s backside surface and on top of base multi-layer reflection layer 155a (backside light trapping material). See ¶¶ 277-287. In the second mapping of Hwang-099-Konno, transparent layer 136 is located underneath Hwang-099’s backside surface and on top of second reflecting layer 120 (backside light trapping material). See ¶¶ 289-309. Thus, both above mappings teach *wherein the textured layer is located between the backside surface and the backside light trapping material*.

**U. Claim 23: “The device of claim 21, wherein the peripheral sidewall extends completely around the pixel periphery.”**

314. As discussed above, the peripheral sidewall of Hwang-099 extends completely around the pixel periphery. See Claims 1[a][ii], 4 (incorporated herein).

**V. Claim 24: “The device of claim 21, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

315. As discussed above, the peripheral sidewall of Hwang-099 extends from the light incident surface to the backside surface. See Claims 1[a][ii], 5 (incorporated herein).

**W. Claim 25: “The device of claim 21, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

316. In the second mapping of the above combination of Hwang-099-Konno, Hwang-099’s base multi-layered reflection layer is replaced with Konno’s metal second reflecting layer 120 (i.e., metal layer) that is “formed by forming a thin film of metal such as aluminum or silver by deposition.” *Konno* at 8:25-38, 11:42-52; Claim 21[b]. Thus, the above combination of Hwang-099 and Konno renders obvious *wherein at least one of the backside light trapping material...is a metal layer*.

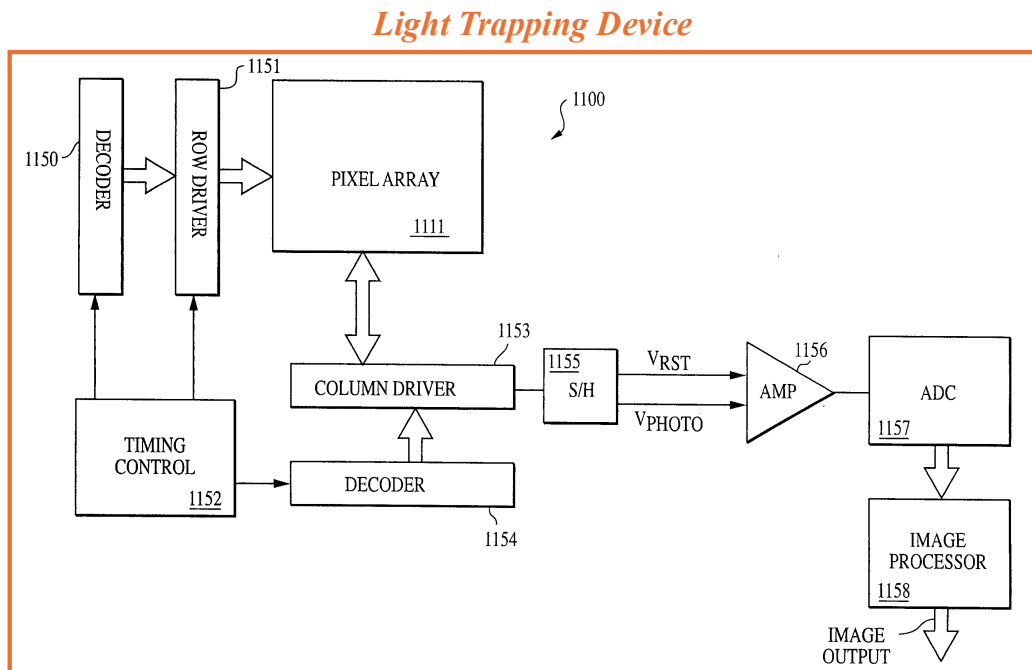
**XV. GROUND 8: CLAIMS 1-5 AND 7 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584, HWANG-795, AND KAES**

**A. Claim 1[Pre]: “A *light trapping device*, comprising:”**

317. Hong describes a “single chip CMOS image sensor 1100” having “a pixel array 1111 containing a plurality of pixel cells arranged in rows and columns.” *Hong* at [0047]. “The array 1111 includes one or more pixels 200 as described above in connection with FIGS. 2-10.” *Id.* Per Hong, a pixel is “a picture element unit cell containing a photo-conversion device for converting electromagnetic radiation [i.e., light] to an electrical signal.” *Hong* at [0017]. “Pixel 200 includes a photo-conversion device, which is, illustratively, a pinned photodiode 221.” *Hong* at [0018]. Each pixel 200 in image sensor 1100 includes a reflective layer that “serves to reflect incident light not initially absorbed into the photo-conversion device, back

to the photo-conversion device.” *Hong* at Abstract. This is similar to the ’764 Patent, which describes light trapping materials “covering” the backside of the pixel, for example, so that “light contacting the backside light trapping material ... is thus reflected back toward the pixel.” ’764 Patent at 1:44-47.

318. Thus, Hong’s image sensor 1100 traps light by reflecting it back into each individual pixel and is, therefore, a *light trapping device*:



*Hong* at FIG. 11 (annotated).

**B. 1[a]: “at least one light sensitive *pixel*”**

319. Hong’s image sensor 1100 includes “a pixel array 1111 containing a plurality of pixel cells arranged in rows and columns.” *Hong* at [0047]. “The array 1111 includes one or more pixels 200,” which are described “in connection with

FIGS. 2-10.” *Hong* at [0047]. Per *Hong*, “[t]he term ‘pixel’ refers to a picture element unit cell containing a photo-conversion device for converting electromagnetic radiation to an electrical signal.” *Hong* at [0017].

320. As shown in FIG. 2, each pixel 200 includes a silicon layer 202 having “a photo-conversion device, which is, illustratively, a pinned photodiode 221” that “is adjacent to an isolation region 203, which is illustratively a shallow trench isolation (STI) region.” *Hong* at [0018]; *see also, id.* at [0022] (Photodiode 221 is “located at a surface of a semiconductor layer 202. Illustratively, the semiconductor layer 202 is a layer of p-type silicon (Si).”). “The photodiode 221 includes an n-type region 211 underlying a p+ surface layer 212.” *Hong* at [0018]. As I discussed above, a PN junction is formed by joining regions of positively doped (P-type) and negatively doped (N-type) material, which generates electron-hole pairs in response to light passing through Si layer 202. *See* ¶¶ 42-47. Thus, *Hong*’s n-type region 211 and p+ surface layer 212 in photodiode 221 form a PN junction having a diffusion region that separates electron-hole pairs to generate an electrical signal. *Id.*

321. “Adjacent to the photodiode 221, is a floating diffusion region 215.” *Hong* at [0018]. “Between the photodiode 221 and the floating diffusion region 215 is a transfer transistor 224, which operates to transfer charge from the photodiode 221 to the floating diffusion region 215.” *Hong* at [0018]. In other words, the electric charge generated by the PN junction is transferred to region 215 via transistor 224.

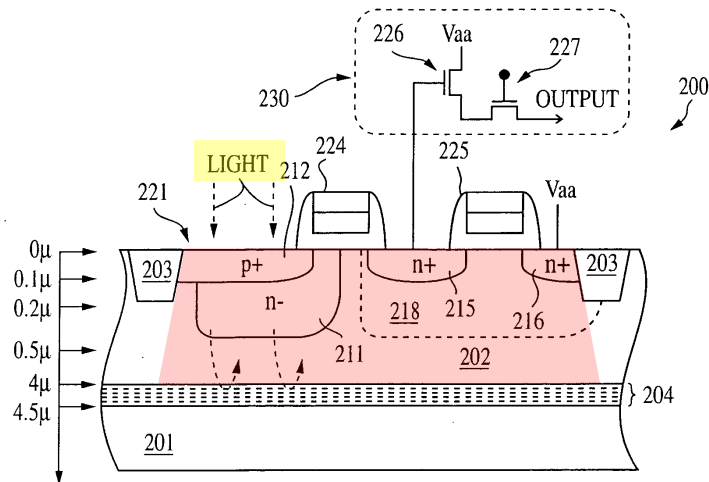
A readout circuit 230, including transistor 226, “is connected to the floating diffusion region 215,” and is used to extract the electric signal (i.e., pixel image signal  $V_{photo}$ ) generated in response to light hitting photodiode 221. *Hong* at [0020]; *see also, id.* at [0049] (“The signals on the column readout lines typically ... a pixel image signal ( $V_{photo}$ ) for each pixel.”).

322. Floating diffusion region 215 is located within a doped p-well 218 that “extends from the surface of Si layer 202 to a depth within Si layer 202, e.g., a depth greater than the n-type region 211.” *Hong* at [0022], FIG. 2. “The p-well 218 reaches from below an STI region 203 adjacent to the source/drain region 216 of the reset transistor 225 to a point below the transfer transistor 224.” *Hong* at [0022], FIG. 2.

323. The source/drain region 216, which is also located within the p-well 218 is connected to reset transistor 225, which is used to reset “the floating diffusion region 215 to a predetermined voltage, which is, for example, an array voltage  $V_{aa}$ .” *Hong* at [0021]; *see also, id.* at [0022] (“[T]he source/drain region 216 ... [is] located in the p-well 218.”). Thus, the floating diffusion region 215 is reset to a reference voltage, provided by source/drain region 216, before collecting charge from the photodiode 221 to be read out as pixel image signal  $V_{photo}$ .

324. Thus, at least pixel 200’s pinned photodiode 221, semiconductor layer 202, floating diffusion region 215, source/drain region 216, and p-well 218 collectively operate to convert light into an electrical signal:

### Light Sensitive Pixel

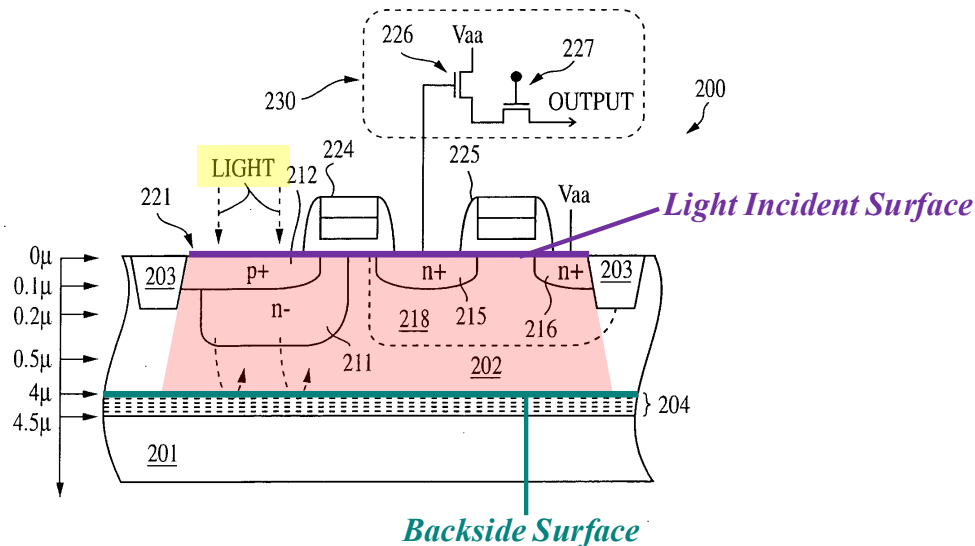


Hong at FIG. 2 (annotated).

C. *1[a][i]*: “having a **light incident surface**, a **backside surface opposite the light incident surface**,”

325. Per the '764 Patent, “a device can include at least a semiconductor substrate having a first side for receiving incident light and a second side opposite the first side.” '764 *Patent* at 6:47-49, 13:20-21 (describing “...the top surface (i.e. the light incident surface)...”). Similarly, Hong describes “[l]ight of a targeted wavelength (represented by dashed arrows) incident on photodiode 221, which is not initially absorbed into photodiode 221, is reflected by the reflective layer 204, as shown in FIGS. 2 and 3.” Hong at [0026]; *see also, id.* at FIGS. 2-3. “As shown in FIG. 2, transfer and reset transistors 224, 225, and photodiode 221 are located at a surface of a semiconductor layer 202.” Hong at [0022], FIG. 2. Because external light is incident on photodiode 221, which is “located at a surface of a semiconductor

layer 202[,],” the top semiconductor layer 202 is a light incident surface. Id. Likewise, the light incident surface (i.e., top of Si layer 202) is opposite Hong’s backside surface (i.e., the bottom of Si layer 202, above reflective layer 204) in pixel 200:



*Hong* at FIG. 2 (annotated).

326. I note that FIG. 2 of *Hong* “is a cross-sectional view of a pixel” and “transfer and reset transistors 224, 225, and photodiode 221 are located at a surface of a semiconductor layer 202.” *Hong* at [0009], [0022]. Because pixel 200 is a three-dimensional object having a length/height (top-to-bottom in FIG. 2), width (left-to-right in FIG. 2), and depth (front-to-back in three-dimensional space in FIG. 2), a POSITA would have understood that the purple line representing a light incident surface shown in annotated FIG. 2 is actually a plane extending the entire depth (front-to-back) and width (left-to-right) of pixel 200’s surface area. Thus, an

alternative view of pixel 200 at another cross-section would not include transistors 224, 225 on the light incident surface. Therefore, a POSITA would have understood that transistors 224, 225 are not covering a portion of the top surface of the substrate along the entire depth (front-to-back) of the pixel but instead, only a portion of the depth. Therefore, there is a width of the pixel that does not include transistors 224, 225, such that the light incident surface extends along the entire exposed width of the top surface of the silicon substrate 202 both in front of and to the back of the transistors. It was well understood that the transistors have a smaller surface area than that of the entire pixel. *See e.g., Crocherie* at 9 (Of the “whole pixel area[,]” only “a part is occupied by the transistors for the purpose of collecting, converting and reading photogenerated electrons.”). Indeed, if the transistors took up the majority of the surface area of the pixel’s light incident surface, then the pixel would not function as intended.

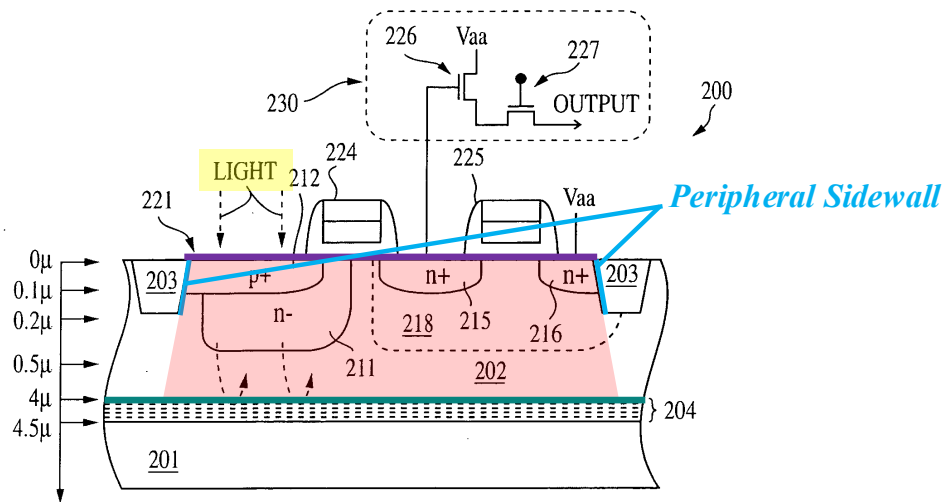
**D. 1[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the *pixel periphery*;”**

327. As shown below, this limitation is met by the combination of Hong and Yamashita.

**1. *Hong’s Teachings***

328. Per the ’764 Patent, “the pixel sidewall is also known as a trench.” ’764 *Patent* at 10:64-65. Similarly, isolation region 203 of Hong’s pixel 200 is “a shallow

trench isolation (STI) region” that includes a peripheral sidewall as it is adjacent to the elements of Hong’s pixel. *Hong* at [0018]; *see also, id.* at FIG. 2. For example, Hong describes how “photodiode 221 is adjacent to an isolation region 203” and “source/drain region 216 of the reset transistor 225...is adjacent to an STI region 203[,]” and photodiode 221 and source/drain region 216 are elements of Hong’s pixel. *Hong* at [0018], [0021]; Claim 1[a].



330. I note that this is consistent with the '764 Patent, which describes “isolation elements, also referred to herein as trench isolation features or sidewalls” “and depending on the depth of the trench can be considered either deep trench isolation or shallow trench isolation.” ’764 Patent at 7:25-32, 10:64-65 (“It is noted that the pixel sidewall is also known as a trench.”).

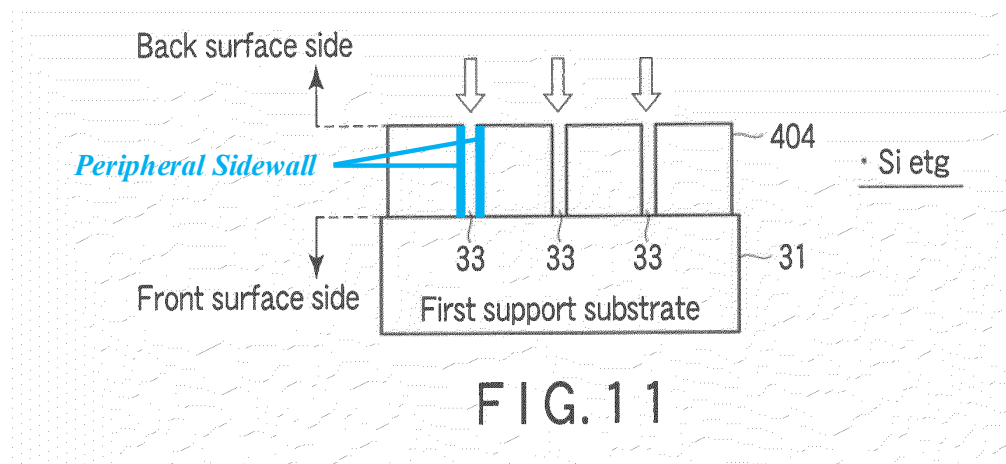
## 2. *Yamashita’s Teachings*

331. Yamashita teaches a solid-state imaging device having a pixel region. *Yamashita* at Abstract. Yamashita’s pixel region includes a trench 33 etched through silicon substrate 404 (also described as semiconductor substrate 404), which is similar to the silicon layer 202 in Hong’s pixel 200. Specifically, “selective etching is performed by, e.g. photolithography, on the surface (back side) of the silicon substrate 404, on which the light-receiving region is formed and which becomes the device isolation boundary of the unit pixel, to the surface of the first support substrate 31, and trenches 33 are formed.” *Yamashita* at [0102]. In other words, trench 33 “becomes the device isolation boundary of the unit pixel,” which means that the sidewall of trench 33 is peripheral to Yamashita’s pixel. *Id.*

332. The peripheral sidewall of trench 33 extends to the backside surface because it is etched “to the surface of the first support substrate 31,” which is the backside surface of Yamashita’s pixel 1. *Id.* Specifically, “a first support substrate 31...is attached to the surface of the substrate 404 on the side (front side) on which

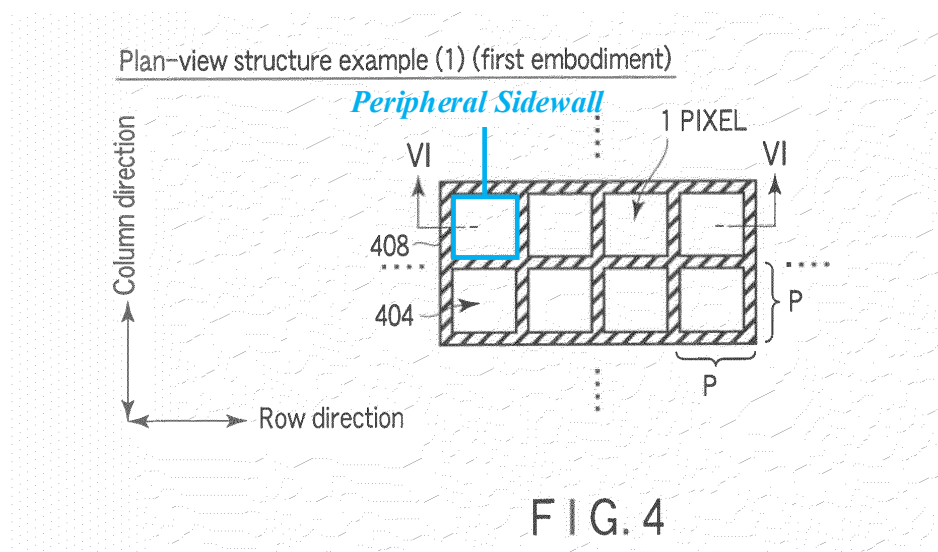
a signal scanning circuit, etc. are formed[.]” *Yamashita* at [0100]. The “front side” becomes the backside surface opposite the light incident surface in pixel 1 when silicon substrate 404 is “turned upside down, and a color filter 406 and a micro-lens 407 are successively formed on the back surface of the silicon substrate 404.” *Yamashita* at [0112]. “Thus, incident light can be radiated on the silicon (Si) surface (back surface) which is opposite to the silicon (Si) surface (front surface) on which the signal scanning circuit and the wiring layer thereof are formed.” *Yamashita* at [0120].

333. As shown in FIG. 11, *Yamashita*’s trench 33 extends through silicon substrate 404 (from the front to the back side), and substrate 404 is part of a pixel. Thus, the sidewall of trench 33 likewise extends through the substrate and is disposed into at least a portion of the pixel:



*Yamashita* at FIG. 11 (annotated).

334. Further, Yamashita's peripheral sidewall extends substantially around the pixel periphery as device insulation isolation film 408 that fills trench 33 "defines device isolation regions in a manner to surround boundary parts between neighboring unit pixels (PIXEL) 1." *Yamashita* at [0116], [0077] ("[D]evice insulation insulation film 408 is disposed in a lattice shape in a manner to surround the unit pixels 1 in the row direction and column direction."), [0084] ("[D]evice insulation insulation film 408 is provided at a boundary part between the pixels in the Si substrate 404."). Thus, Yamashita's sidewall of trench 33 is a peripheral sidewall extending at least substantially around the pixel periphery:



*Yamashita* at FIG. 4 (annotated).

### 3. *Motivation to Combine*

335. Based on the teachings of Yamashita, it would have been obvious to extend the sidewall of Hong's isolation region 203 substantially around the pixel

periphery. A POSITA would have understood that extending Hong's sidewall substantially around the pixel periphery would have predictably reduced or eliminated "crosstalk among various sensor pixels[.]" *See e.g., Hsu* at 3:38-39. It was well-known that "providing deep trenches around the red pixels" helps ensure "crosstalk between the red pixels (which have a deeper photon absorption than the green and blue pixels) is decreased and the image quality is accordingly increased." *See e.g., Mouli* at 7:46-52. Yamashita expressly motivates the combination, stating "device isolation insulation film 408 is continuously formed in a lattice shape along pixel boundaries without spacing, as shown in FIG. 4" so that "light is reflected at the device isolation insulation film 408 with no leak." *Yamashita* at [0095], [0104]. This helps "prevent [] light from entering the neighboring unit pixel" so that "crosstalk" "and the occurrence of color mixing can be prevented[.]" *Yamashita* at [0092]-[0093], [0097]. A POSITA would have appreciated that pixel cells 200 in pixel array 1100 of Hong with an extended peripheral sidewall would benefit from similarly reduced crosstalk and color mixing. Thus, a POSITA would have been motivated to use a known technique (etching a trench in a substrate around the pixel periphery, per Yamashita) to improve similar devices (improving the performance of Hong's image sensor pixel) in the same way (reducing crosstalk in Hong's system in the same manner as Yamashita's).

336. There would have been a reasonable expectation of success extending Hong's peripheral sidewall, per Yamashita, as it simply requires etching (by "selective etching...e.g., photolithography") Hong's isolation region 203 in Si layer 202 continuously around pixel 200. *Yamashita* at [0102]. A POSITA would have appreciated that the technique of etching a trench per Yamashita was well-known in the art. *See e.g., Mouli* at 2:3-6 (describing "[i]n general, for STI, a trench 120a, 120b is etched into the substrate 101 and filled with a dielectric to provide a physical and electrical barrier between adjacent pixels (100a, 110b), devices, or circuitry."). Moreover, Hong's silicon layer 202 and Yamashita's silicon substrate 404 are made of analogous materials (silicon), indicating the etching techniques used to form peripheral sidewalls in Yamashita's pixel 1 would be equally successful in Hong's pixel 200. *Yamashita* at [0076].

337. Additionally, it was well-known to extend sidewalls around the periphery of pixels in an image sensor array to achieve the benefits I noted above prior to the '764 Patent. *See e.g., Mouli* at 7:61-64 (describing "deep trench isolation structures...formed surrounding totally or partially other pixels of a color filter array" in addition to red.), FIG. 7; *Michelot* at 001-002 (describing "a deep trench isolation (DTI) technique to avoid cross-talk between neighboring pixels[.]"), FIG. 1 (demonstrating the trench extending around the pixel elements).

338. Therefore, extending the sidewall of Hong's isolation region 203 around the periphery of pixel 200 in the same manner as Yamashita's sidewalls of trench 33 would have been well within the skill level of a POSITA.

E. *1[b] “a backside light trapping material substantially covering the backside surface; and”*

339. The Si layer 202 of Hong's pixel 200 “overlies a reflective layer 204” that is a Distributed Bragg Reflector (DBR) mirror including sub-layers 204a, 204b, 204c, 204n, and 204m.” *Hong* at [0023]. “The reflective layer serves to reflect incident light not initially absorbed into the photo-conversion device, back to the photo-conversion device.” *Hong* at Abstract. The reflective layer 204 includes sub-layers 204a-m that “are stacked such that the (first refractive index sub-layer)/(second refractive index sub-layer) structure is periodic....” *Hong* at [0025]. This is similar to the '764 Patent, which describes a Bragg reflector as “a structure formed from multiple layers of alternating materials with varying refractive indexes, or by a periodic variation of some characteristic” thus “resulting in periodic variation in the effective refractive index in the guide.” *'764 Patent* at 8:47-52.

340. The '764 Patent also describes “the backside light trapping material including a high refractive index material sandwiched between two low refractive index materials and forming a pixel device layer on the semiconductor layer opposite the light trapping material.” *'764 Patent* at 2:50-54. Hong's reflective layer 204 similarly forms a “(first refractive index layer)/(second refractive index layer)

[sandwich] structure” that can “include more or fewer sub-layers” than layers 204a-m. *Hong* at [0023]-[0024]; FIG. 3. Therefore, the low/high/low refractive index material sandwich can be repeated multiple times in Hong’s layer 204. Further, a POSITA would have understood layer 204 is light trapping given “[l]ight is reflected at the discontinuity at the junctions 244 between the sub-layers 204a-m, where materials having differing refractive indexes meet. The total reflectivity of reflective layer 204 is a summation of the reflections from each of the junctions 244.” *Hong* at [0026], FIG. 3. The sub-layers 204a-m are illustrated in FIGS. 3 and 5:

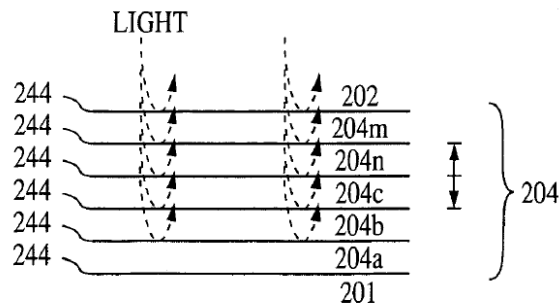


FIG. 3

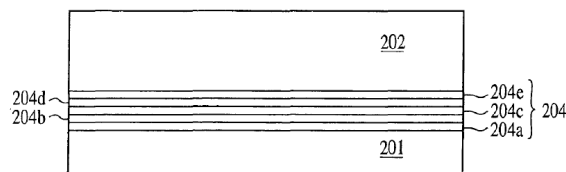
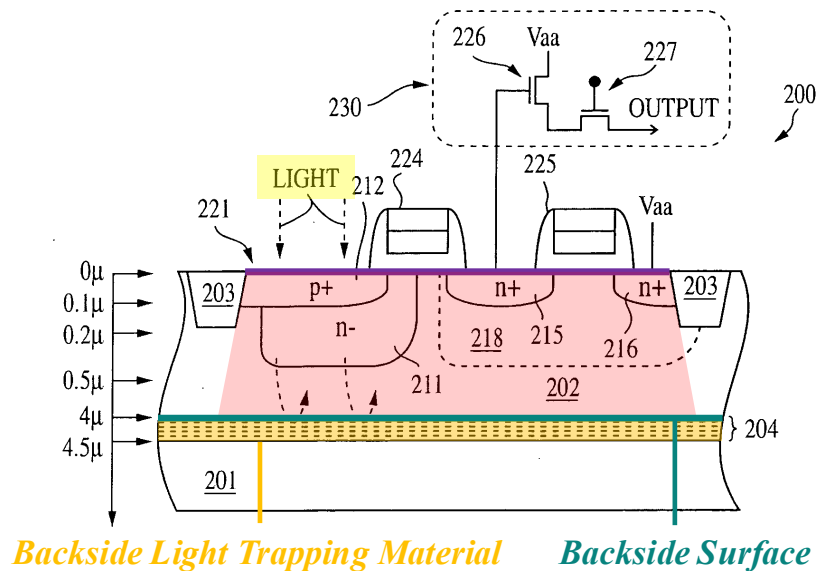


FIG. 5

*Hong* at FIGS. 3, 5.

341. Reflective layer 204 substantially cover[s] Hong’s backside surface (i.e., the bottom surface of Si layer 202), as illustrated in FIG. 2, since “Si layer 202

overlies a reflective layer 204, which in turn overlies a substrate 201.” *Hong* at [0023], FIGs. 2, 5. Further, “[l]ight... is reflected by the reflective layer 204.” *Hong* at [0026]. Reflective layer 204 covers the bottom of Si layer 202 and serves to reflect light, thus qualifying as a backside light trapping material at least partially covering the backside surface:



*Hong* at FIG. 2 (annotated).

F. *1[c]*: “a **peripheral light trapping material** substantially covering the **peripheral sidewall**,”

342. As shown below, this limitation is met by the combination of *Hong*, *Yamashita*, and *Hwang-584*.

### 1. *Hwang-584’s Teachings*

343. *Hwang-584* describes an “image sensor that blocks penetration of visible light into surrounding pixels using device separation membranes...” *Hwang-*

584 at [0001]. Each pixel “includes a p-type semiconductor substrate (100), p-type epitaxial layer (200) formed on the substrate (100), device separation membranes (300) that structurally separate each active region, and photodiodes (400) formed on the epitaxial layer (200).” *Hwang-584* at [0019], *see also, id.* at FIG. 2.

344. The device separation membrane 300 “is formed deeper than the photodiode (400), and membranes of two different materials having different refractive indices are formed alternately in the vertical direction to the substrate (100).” *Hwang-584* at [0020]. “By forming the device separation membrane (300) using two different materials having different refractive indices, the reflectance of the device separation membrane may be raised, thereby allowing it to block permeation of side light from entering into an adjacent pixel.” *Id.*

345. “[T]he device separation membrane (300) is formed with silicon dioxide membrane (320) and silicon membrane (340) and has 3 layers of membrane.” *Hwang-584* at [0024]. Specifically, “[t]he silicon dioxide membrane (320) is formed by first forming a trench on the epitaxial layer and depositing silicon dioxide (SiO<sub>2</sub>) on the bottom surface and side walls of the trench.” *Id.*; *see also, id.* at [0035] (“[A] trench (350) to form a device separation membrane is formed on the epitaxial layer (200).”). The sidewall of the trench is the peripheral sidewall of the pixel.

346. Hwang-0584's peripheral sidewall (i.e., sidewall of trench 350) is substantially cover[ed] by device separation membrane 300, which "is formed with silicon dioxide membrane (320) and silicon membrane (340) and has 3 layers of membrane." *Id.* "Figures 5a to 5e are cross-section drawings depicting the method of manufacturing a CMOS image sensor..." *Hwang-584* at [0046]. After the trench 350 (and peripheral sidewall) is formed in FIG. 5B, "a silicon oxide membrane (320) is formed by depositing silicon oxide onto the bottom surface and side walls of the interior of the trench (350)," as shown in FIG. 5C. *Hwang-584* at [0035]-[0036], FIGS. 5B-5C. Next, "silicon is filled into the trench where the silicon oxide membrane (320) is formed to form a silicon membrane (340)," which results in "device separation membrane (300) comprising membranes of two different materials – silicon oxide membrane and silicon membrane..." *Hwang-584* at [0037], FIG. 5D. As shown below, the device separation membrane 300 is a peripheral light trapping material substantially covering the peripheral sidewall:

Figure 5b

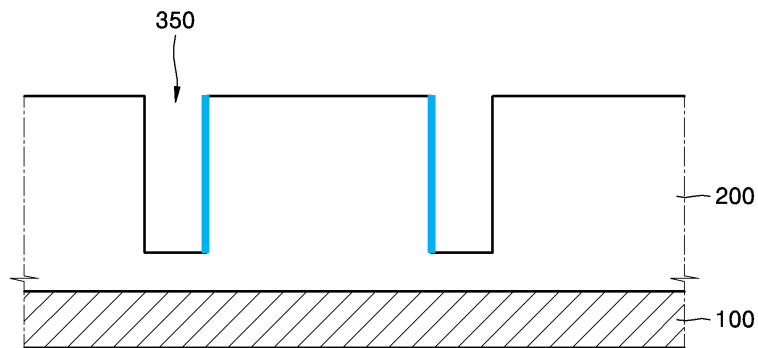


Figure 5c

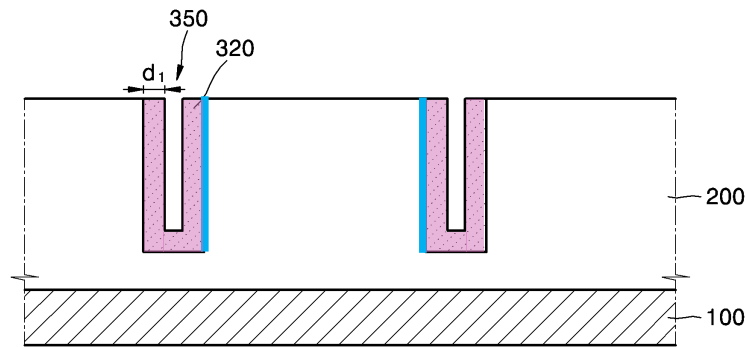
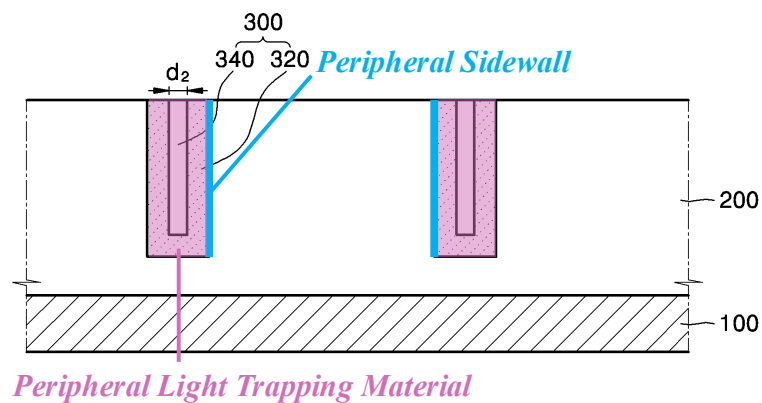
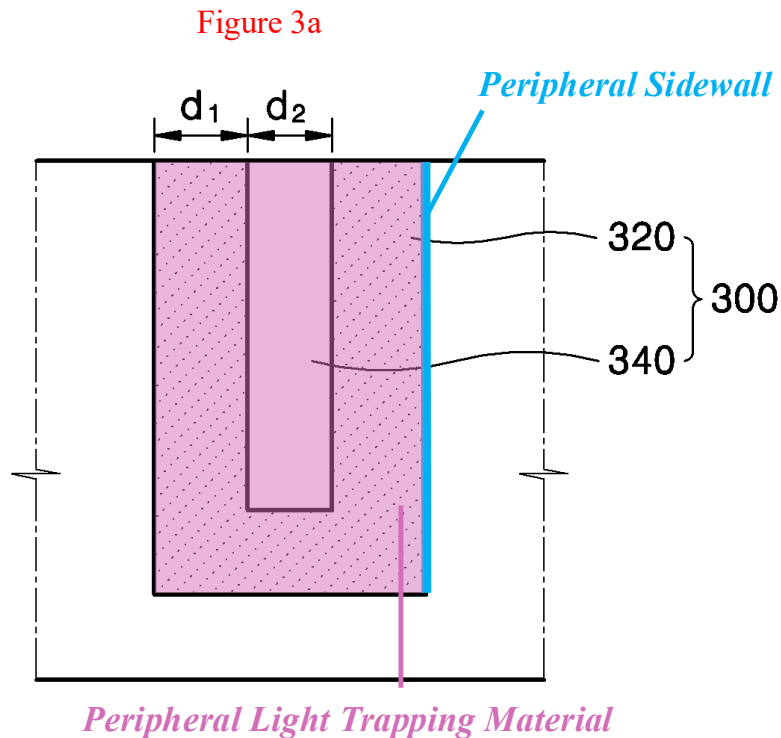
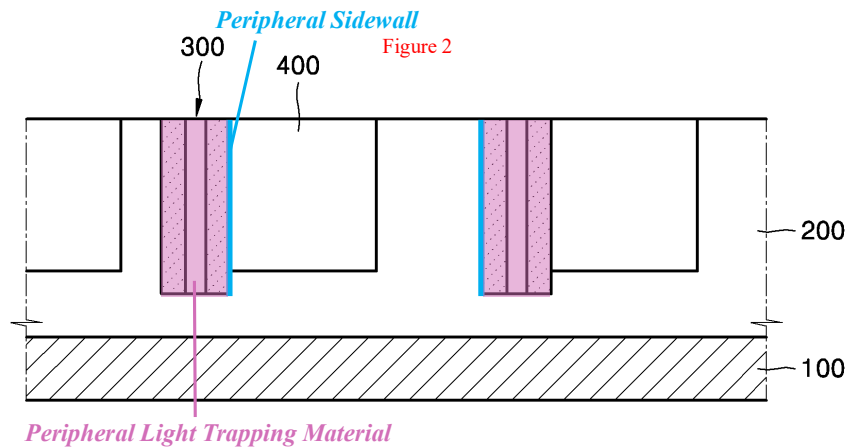


Figure 5d



*Hwang-584* at FIGS. 5B-5D (annotated).

347. FIG. 2 depicts “a 3-layer device separation membrane using membranes of two different materials,” as described above, and FIG. 3A depicts “the device separation membrane (300) is formed with silicon dioxide membrane (320) and silicon membrane (340) and has 3 layers of membrane.” *Hwang-584* at [0021], [0024].



*Hwang-584* at FIGS. 2, 3A (annotated).

348. “Figure 3a and Figure 3b are cross-section drawings depicting enlarged structure of the membranes of two different materials that could be used in the device separation membrane shown in Figure 2.” *Hwang-584* at [0023]. Therefore,

membranes 320, 340 as shown in FIG. 3A are the same membranes used to form membrane 300 in FIG. 2.

349. Device separation membrane 300 is *light trapping* because it reflects light back into Hwang-584's *pixel* due to the difference in refractive index between the "3 layers of membrane." *Hwang-584* at [0024]. Specifically, "forming the device separation membrane (300) using two different materials having different refractive indices, the reflectance of the device separation membrane may be raised, thereby allowing it to block permeation of side light from entering into an adjacent pixel." *Hwang-584* at [0020]. "Greater difference between the refractive indices of the two materials translates to higher reflectance of the device separation membrane." *Id.* "[B]lock[ing] permeation of side light from entering into an adjacent pixel" indicates device separation member 300 simultaneously retains said light within the intended pixel where light was originally incident. *Hwang-584* at [0009].

## **2. Motivation to Combine**

350. A POSITA would have found obvious and been motivated to modify the wall of the Hong-Yamashita isolation region 203 (*peripheral sidewall*) to be *substantially cover[ed]* by Hwang-584's device separation membrane 300 (*peripheral light trapping material*) in order to "significantly reduc[e] CT ([crosstalk]) phenomenon experienced in the existing [sensors]." *Hwang-584* at [0032].

351. In the modification, Hong's isolation region 203 completely surrounds the pixel periphery, per Yamashita, and is further modified to include Hwang-584's *peripheral light trapping material* (i.e., membrane 300), substantially covering Hong's peripheral sidewall. *See* Claim 1[a][ii]. Hwang-584 expressly motivates the combination by acknowledging that "forming device separation membrane with membranes of two different materials having different refractive indices can reflect most of long wavelength of light, especially the visible light range" "significantly" decreases crosstalk among pixels in Hong's modified array 1100 and increases light "reflect[ed]" back into pixel 200. *Hwang-584* at [0032], FIG. 4A; *Hong* at [0026] (describing how "[l]ight is reflected...where materials having differing refractive indexes meet.").

352. Hong's "isolation regions 203 are formed in the Si layer 202 and fil[l]ed with a dielectric material." *Hong* at [0033]. A POSITA would have appreciated replacing Hong's singular "dielectric material" with Hwang-584's "two different materials having different refractive indices formed alternately" configured as a Bragg reflector to substantially cover Hong's peripheral sidewall for improved reflection, and thus entrapment, of various wavelengths of light within Hong's pixel 200. *Hwang-584* at Abstract; *Hong* at [0033]. Thus, a POSITA would have been motivated to improve similar pixels in the same way.

353. The modification is a simple combination of prior art elements (a peripheral sidewall surrounding a pixel and materials having different refractive indices) to yield predictable results (improved entrapment of light within a pixel).

354. There would have been a reasonable expectation of success because depositing materials such as Hwang-584's membranes 320, 340 in trenches was conventional well prior to the invention of the '764 Patent. *See e.g., Venezia* at 5:8-10 (describing how "shallow trench isolation is typically a trench etched within a silicon substrate and subsequently filled with silicon dioxide."); *Fan* at [0057] (describing shallow trenches that "may be filled with a dielectric, such as, for example, a silicon oxide such as SiO or SiO<sub>2</sub>...").

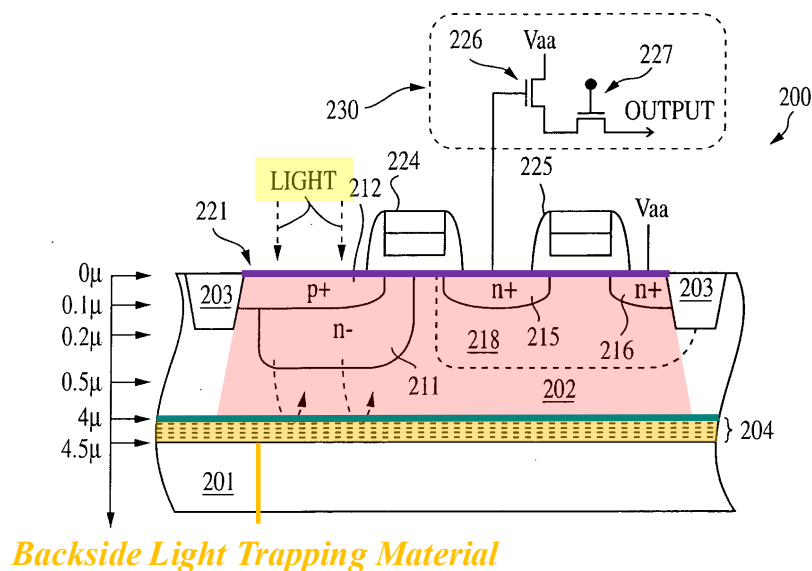
355. A POSITA would have also understood that silicon dioxide membrane 320 is removed from the bottom of trench 350 as shown in FIG. 3A to form the 3-layered sandwich structure shown in FIG. 2 of Hwang-584. Etching a material, for example, from the bottom of a trench, was well-known and routine in the art. *Hwang-584* at FIGS. 2, 3A; *see also, e.g., Mouli* at 5:1-7 (describing how "[a]n etching process, such as an HF dip for example, may be conducted to remove" a material, such as a "liner" made of silicon dioxide, "from the bottom of the trench" so that the material remains "only along the sidewalls of the trench.").

G. 1[c]/[i]: “wherein at least one of the **backside light trapping material** and the **peripheral light trapping material** includes a **high refractive index material** sandwiched between two **low refractive index materials**,”

356. As shown below, this limitation is met by the combination of Hong, Yamashita, and Hwang-584.

### 1. Hong’s Backside Light Trapping Material

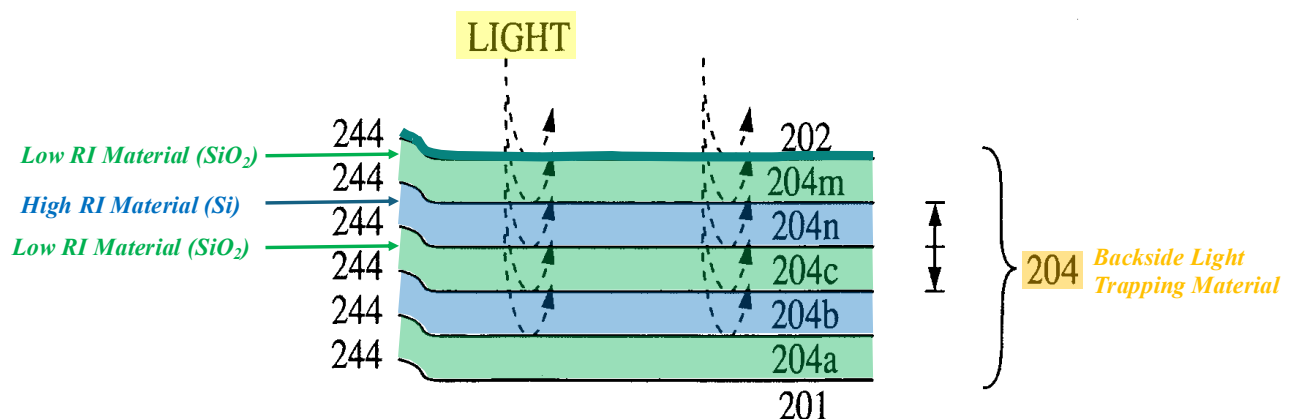
357. Hong’s reflective layer 204 (i.e., the **backside light trapping material**) includes a **high refractive index material** sandwiched between two **low refractive index materials**:



Hong at FIG. 2 (annotated).

358. Per Hong, “reflective layer 204 is illustratively a Distributed Bragg Reflector (DBR) mirror including sub-layers 204a, 204b, 204c, 204n, and 204m.”  
 Hong at [0023]. “Sub-layers 204b and 204n each have a first index of refraction,”

and “[s]ub-layers 204a, 204c, and 204m each have a second index of refraction.” Hong at [0023]. “Therefore, each sub-layer 204a-m is in contact with material having a different refractive index to form a (first refractive index layer)/(second refractive index layer) structure.” Hong at [0023]. In one example, “sub-layers 204b and 204n are Si and sub-layers 204a, 204c, and 204m are SiO<sub>2</sub>, such that reflective layer 204 has an SiO<sub>2</sub>/Si structure.” Hong at [0024]; *see also, id.* at [0031] (“[L]ayer 204 can be formed having an SiO<sub>2</sub>/Si structure. In such a case sub-layers 204a, 204c, and 204m are SiO<sub>2</sub> sub-layers and sub-layers 204b and 204n are Si sub-layers.”). Thus, Hong teaches a sandwich[] of one material having a first refractive index sandwiched between two materials having a second refractive index:



Hong at FIG. 3 (annotated).

359. Because “each sub-layer 204a-m is in contact with material having a different refractive index to form a (first refractive index layer)/(second refractive index layer),” the sub-layers include materials of high/low refractive indexes

because one layer has a “first refractive index” that is “different” from a “second refractive index.” *Hong* at [0023]. It is common sense that if one layer is a first refractive index and a second layer is a second, different refractive index, then one layer is a higher refractive index than the other layer. Because Hong describes layers alternating between first/second refractive indexes a number of times, Hong teaches a high refractive index material sandwiched between two low refractive index materials, regardless of whether the first material is the low or high-refractive index material.

360. Additionally, the claimed low-high-low sandwich is taught by Hong’s teaching of a SiO<sub>2</sub>/Si structure. Hong does not state what the refractive indexes of these materials are, but a POSITA would have understood that these are known properties of these materials. For example, a POSITA would have known from *Hwang-584* that an SiO<sub>2</sub> (silicon dioxide) layer has a refractive index of “around 1.46” and an Si (silicon) layer has a refractive index of “around 3.7 to 5.7 depending on the wavelength” of incident light. *Hwang-584* at [0025]; *see also, e.g., Kasano* at [0021] (describing the “refractive index of amorphous silicon, polysilicon, single-crystal silicon, or a material mainly containing silicon is about 4 to 5 and larger compared to a normal insulating film and the like (a refractive index of a silicon dioxide film is 1.46, for example).”). Therefore, Hong alone teaches or suggests the refractive indexes of its high refractive index material (Si) and low refractive index

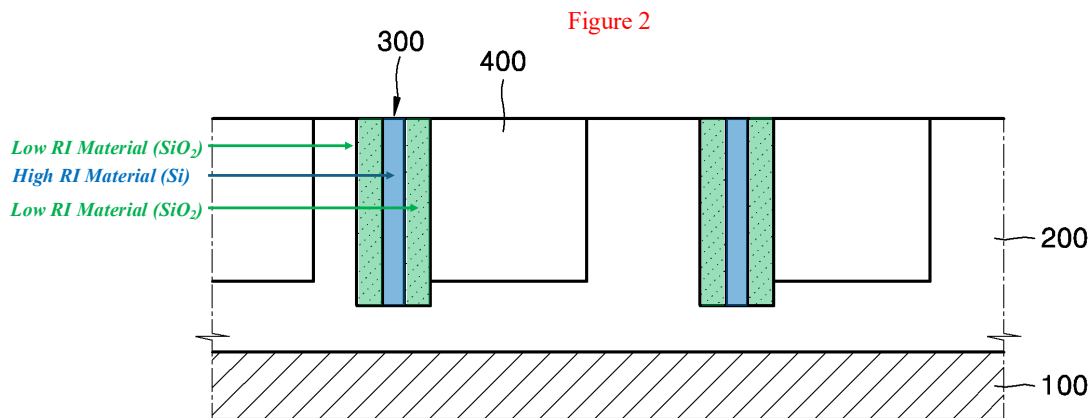
material (SiO<sub>2</sub>), or such would be obvious based on the knowledge of a POSITA, as evidenced by at least Hwang-584.

361. Alternatively, this limitation would have been obvious based on the teachings of Hwang-584. Specifically, a POSITA would have found obvious to use, in Hong's reflective layer 204, Hwang-584's layers with the expressly-taught refractive indexes. In the combination, Hong's modified SiO<sub>2</sub> layer has a refractive index of around 1.46, and Hong's modified Si layer has a refractive index of at least around 3.7, per Hwang-584. *Hwang-584* at [0025]. There would have been a reasonable expectation of success because the refractive index of the same materials in Hwang-584's separation membrane 300 (for deposition on a peripheral sidewall) would have the same refractive index when used in Hong's reflective layer 204 (i.e., the backside light trapping material). Also, while Hwang-584 applies Si and SiO<sub>2</sub> layers to the peripheral sidewalls, a POSITA would have understood that these materials would be equally effective on the backside of the pixel per Hong's express teachings. *Hong* at [0024], [0031].

## **2. *Hwang-584's Peripheral Light Trapping Material***

362. As I discussed above, Hwang-584's device separation membrane 300 (i.e., the peripheral light trapping material) includes layers of three layers where one silicon layer 340 is "formed" "between" two layers of silicon dioxide 320. *Hwang-584* at [0024]; see ¶¶ 343-349. Per Hwang-584, "silicon dioxide's refractive index

is around 1.46, whereas that of silicon is around 3.7 to 5.7 depending on the wavelength. Therefore, the difference between the refractive indices is 2.2 or more, allowing high reflectance in a device separation membrane (300) comprising a silicon dioxide membrane (320) and a silicon membrane (340).” *Hwang-584* at [0025], FIG. 3a. Therefore, *Hwang-584*’s peripheral light trapping material (i.e., device separation membrane 300) includes a high refractive index material (membrane 340’s silicon having a refractive index of at least 3.7) sandwiched between two low refractive index materials (layers of membrane 320 having a refractive index of 1.46):



*Hwang-584* at FIG. 2 (annotated).

H. *1[c][ii]: “wherein at least one of the two **low refractive index materials** is doped with a dopant to create a surface field, and”*

363. As shown below, this limitation is met by the combination of Hong, Yamashita, Hwang-584, Hwang-795, and Kaes.

1. *Peripheral Light Trapping Material: Hwang-795’s Teachings*

364. As I described above, Hwang-795 teaches *one of the two low refractive index materials* (silicon dioxide, e.g., borosilicate glass) is *doped with a dopant* (boron) *to create a surface field*. See ¶¶ 181-183.

2. *Motivation to Combine*

365. In the modification, A POSITA would have found it obvious and been motivated to dope Hwang-584’s silicon dioxide membrane 320 in the *peripheral light trapping material* of the Hong-Yamashita-Hwang-584 combination with boron, per Hwang-795, so that a charged region around the trench would be formed. Specifically, a surface field forms at the interface between the p<sup>+</sup> BSG dopant in trench 203 and p-type silicon 202. As I discussed above, a surface field is formed due to the dopant concentration gradient between p<sup>+</sup> and p<sup>-</sup>. See ¶182. Because Hong (as modified per Hwang-584) already teaches a silicon dioxide layer substantially covering the sidewall of Hong’s isolation region 203 (“a shallow trench isolation (STI) region”), a POSITA would have merely needed to dope silicon dioxide with boron to achieve the combination with Hwang-795. *Hong* at [0018]. A POSITA would have been motivated to combine the prior art elements of Hwang-795’s

boron-doped silicon dioxide in a trench with Hong's image sensor according to known methods to yield the predictable result of "creat[ing] a surface field."

366. Hwang-795 expressly motivates doping Hwang-584's silicon dioxide membrane 320 to "reduce intermixing and crosstalk between image data and unit pixels, through more precise isolation between unit pixels." *Hwang-795* at [0015]. Further, including a dopant, such as boron, would improve a pixel's "charge transfer efficiency" and "minimize...dark current[.]" *Hwang-795* at [0029]-[0030], [0036].

367. Prior to the time of the alleged invention, it was well-known that image sensors "may exhibit crystalline defects such as dangling bond[s] at an interfacial surface between" a "device isolating region" (e.g., a trench) and "the substrate of the photodiode active region." *See e.g., Kwon* at 1:38-42. Specifically, when "a trench formed by etching the substrate" of an image sensor is "filled with an insulating layer, crystalline defects may occur when etching the substrate." *See e.g., Kwon* at 1:41-45. Such defects "act as traps capturing electrons" and may "become defect or noise components of each pixel" by "increasing the dark current, i.e., the current that continues to flow in the photodiode when there is no incident light," ultimately "degrad[ing] the imaging characteristics" of an image sensor." *See e.g., Kwon* at 1:45-52. Accordingly, a POSITA would have been very familiar with the issue of dark current arising from defects at the interfacial surface between a trench and substrate in image sensor technology. Further, a POSITA would have recognized

that the interface between Hwang-584's membrane 320 covering the sidewall of isolation region 203 and Si substrate 202 would have been susceptible to crystalline defects arising from the etching process and would have been a source for dark current. As such, a POSITA would have been motivated to further modify Hong-Yamashita-Hwang-584 according to the teachings of Hwang-795, thereby improving similar image sensors in the same way.

368. Indeed, it was well-known that creating a doped region around the surface of a trench helped to prevent dark current in image sensors. *See, e.g., Adkisson* at 2:27-30 ("it is also advantageous to having doping on the STI sidewall...to minimize dark current."); *Kwon* at 6:34-40 ("[T]he channel stop impurity region 106 conformally surrounds the bottom and the sidewall of the pixel trench...and the dark current and noise caused by an interfacial surface defect...can be decreased."). Therefore, the modification would have predictably improved Hwang-099's device by reducing dark current. The combination of Hong-Yamashita-Hwang-584 and Hwang-795 is the application of a known technique (doping at a trench interface) to a known device (image sensor) ready for improvement to yield predictable results.

369. Given the benefits described above, the modification would have had a reasonable expectation of success. Moreover, BSG was a well-known and widely available material for use in manufacturing image sensors, and the processes for

filling trenches with BSG were well established. *See, e.g., Adkisson* at 7:7-32 (“one technique that has been used to deposit thin films on semiconductor substrates is low-pressure chemical vapor deposition.”); *Chaudhry-610* at 11:28-32 (“One skilled in the art is aware of suitable expedients for forming a layer of...BSG on a substrate, e.g., plasma-enhanced chemical vapor deposition (PECVD).”). Thus, a POSITA would have merely needed to “deposit[]” BSG instead of undoped silicon dioxide membrane 320 in Hong’s isolation region 203. *Hwang-584* at [0024].

### **3. *Backside Light Trapping Material: Kaes’ Teachings***

370. As I described above, Kaes teaches one of the *two low refractive index materials* (silicon dioxide) is *doped with a dopant* (boron) *to create a surface field* (back surface field). *See* ¶¶ 189-190.

### **4. *Motivation to Combine***

371. A POSITA would have found it obvious and been motivated to dope Hong’s silicon dioxide layer 204<sub>m</sub> in reflective layer 204 (***backside light trapping material***) with boron to create a back surface field, per Kaes. As I described above, layer 204<sub>m</sub> is silicon dioxide. *Hong*, [0024] (“...sub-layers 204<sub>a</sub>, 204<sub>c</sub>, and 204<sub>m</sub> are SiO<sub>2</sub>...”); *see* ¶ 358. Because Hong already teaches a silicon dioxide layer 204<sub>m</sub> on the *backside surface*, a POSITA would have merely needed to dope silicon dioxide with boron to achieve the combination with Kaes. A POSITA would have been motivated to combine the prior art elements of Kaes’ boron-doped silicon

dioxide on the backside surface of the substrate with Hong's image sensor 1100 according to known methods to yield the predictable result of creating a back surface field (*create a surface field*). Kaes expressly motivates the combination, stating that "doped region 103 reduces back surface recombination." *Kaes* at [0013]. A POSITA would have been familiar with the issue of recombination and recognized that recombination of electron-hole pairs results in "no current or charge accumulation[.]" *Hibbeler* at [0035]. As such, a POSITA would have been motivated to modify Hong according to Kaes such that a back surface field was created to reduce recombination in Hong's *pixel*. The modification would have predictably increased the quantum efficiency of Hong's pixel 200 by reducing recombination of electron-hole pairs.

372. The modification would have had a reasonable expectation of success at least because Kaes teaches depositing boron doped silicon dioxide on the backside surface and diffusing the boron into the substrate. *Kaes* at [0014]-[0016]. Thus, a POSITA would have been able to easily implement Kaes' back surface field in Hong's image sensor. Further, as I discussed above, the modification would have merely required doping Hong's silicon dioxide layer 204*m* with boron and diffusing the boron into the *pixel*. Techniques to dope silicon dioxide and methods of diffusing dopants into silicon were well-known. *See, e.g., Naumann* at Abstract ("The process of producing a refined borosilicate glass includes..."); *Kaes* at [0016]; *Hwang*-795

at [0028] (“Next, as simple heat process is carried out, thereby diffusing the doped P-type impurity....”).

**I. 1[d] “wherein light contacting the *backside light trapping material* or *peripheral light trapping material* is reflected back toward the *pixel*.”**

373. As shown below, this limitation is met by the combination of Hong, Yamashita, Hwang-584, Hwang-795, and Kaes.

**1. Hong’s Backside Light Trapping Material**

374. Per Hong, “[l]ight of a targeted wavelength (represented by dashed arrows) incident on photodiode 221, which is not initially absorbed into photodiode 221, is reflected by the reflective layer 204, as shown in FIGS. 2 and 3.” *Hong* at [0026], *see also, id.* at FIGS. 2, 3. “Thereby, the quantum efficiency of the pixel 200 is increased” and “cross talk can be reduced, as the reflected light will not travel to adjacent pixels.” *Hong* at [0026]. Thus, Hong expressly teaches that light contacting the backside light trapping material (i.e., reflective layer 204) is reflected back toward the pixel.

**2. Hwang-584’s Peripheral Light Trapping Material**

375. Hwang-584 teaches that the device separation membrane 300 (i.e., peripheral light trapping material) “reduces CT [(crosstalk)] phenomenon that occurs when incident light permeates into an adjacent cell by forming device separation membranes with membranes of two different materials having different refractive indices to increase the reflectance of the device separation membranes.”

*Hwang-584* at Abstract, [0030], [0032]. Thus, *Hwang-584* teaches that light contacting the device separation membrane 300 (i.e., the peripheral light trapping material) is reflected back toward the pixel.

376. For the reasons discussed above, it would have been obvious to modify the wall of the Hong-Yamashita isolation region 203 (peripheral sidewall) to be substantially cover[ed] by *Hwang-584*'s device separation membrane 300 (peripheral light trapping material). *See* Claim 1[c]. In the Hong-Yamashita-*Hwang-584*-*Hwang-795*-Kaes combination, the device separation membrane covering the isolation region 203 provides “reflectance” back toward pixel 200 of “incident light” contacting separation membrane 300 due to the “different refractive indices” between silicon dioxide membrane 320 and silicon membrane 340. *Hwang-584* at Abstract, [0041]. Therefore, this limitation is obvious for the same reasons as discussed with regard to Claim 1[c]. *See* Claim 1[c].

**J. Claim 2: “The device of claim 1, wherein the *backside light trapping material* and the *peripheral light trapping material* includes a *high refractive index material* sandwiched between two *low refractive index materials*.”**

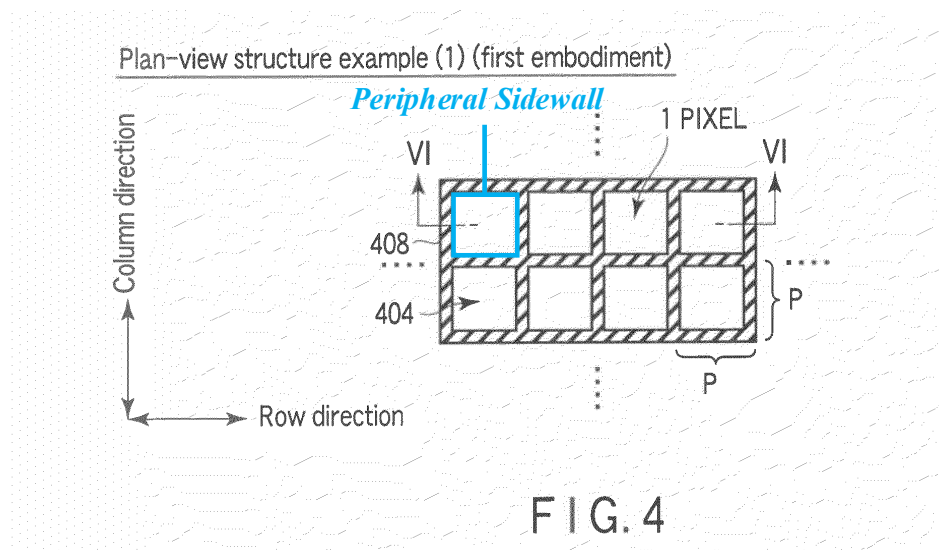
377. As described above for Claim 1[c][i], Hong's reflective layer 204 (i.e., the backside light trapping material) and Hong-Yamashita-*Hwang-584*-*Hwang-795*-Kaes's device separation membrane 300 (i.e., the peripheral light trapping material) meet Claim 2. *See* ¶¶ 356-362.

K. **Claim 3:** “The device of claim 1, wherein the dopant is boron or antimony.”

378. The combination of Hong-Yamashita-Hwang-584-Hwang-795-Kaes I described above teaches *wherein the dopant is boron*, per Hwang-795. See Claim 1[c][ii]; see ¶¶ 363-369.

L. **Claim 4:** “The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery”

379. The combination of Hong-Yamashita-Hwang-584-Hwang-795-Kaes I described above teaches *wherein the peripheral sidewall extends completely around the pixel periphery*, per Yamashita. Yamashita at [0077] (“[D]evice isolation insulation film 408 is disposed in a lattice shape in a manner to **surround** the unit pixels 1 in the row direction and column direction.”). See Claim 1[a][ii]; see ¶¶ 327-338.



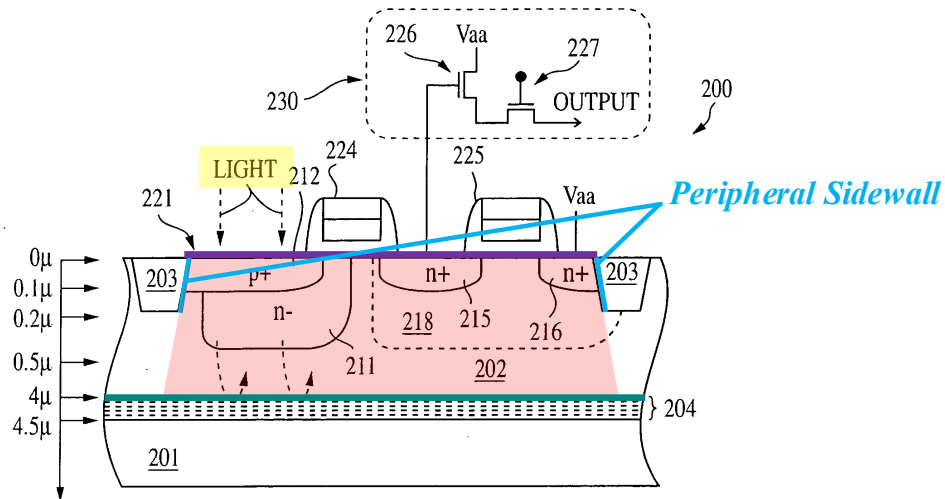
Yamashita at FIG. 4 (annotated).

**M. Claim 5: “The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

**1. Hong’s and Yamashita’s Teachings**

380. Hong’s *peripheral sidewall extends from the light incident surface* (see Claim 1[a][i]), as illustrated in the annotated FIG. 2 below. Hong teaches the isolation region is “formed in the Si layer 202 and fil[l]ed with a dielectric material.” *Hong* at [0033], [0018]. As I discussed for claim 1[a][i], the top surface of Si layer 202 is a light incident surface. Therefore, because the isolation region 203, including the sidewall of isolation region 203, is “formed in the Si layer[,]” per Hong at [0033] and as otherwise shown in FIG. 2, the sidewall of isolation region 203 extends from the light incident surface, i.e., a top surface of the substrate 202.

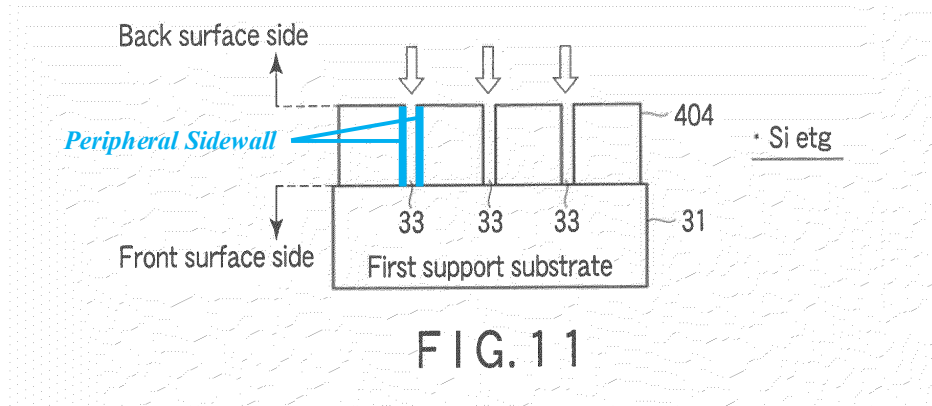
381. Hong teaches that its disclosed peripheral wall extends from the light incident surface. As I discussed for Claim 1[a][ii], Hong teaches a shallow trench isolation (STI) region 203 that includes a peripheral sidewall. *See* Claim 1[a][ii]. As shown in FIG. 2, below, Hong’s sidewall extends from the light incident surface:



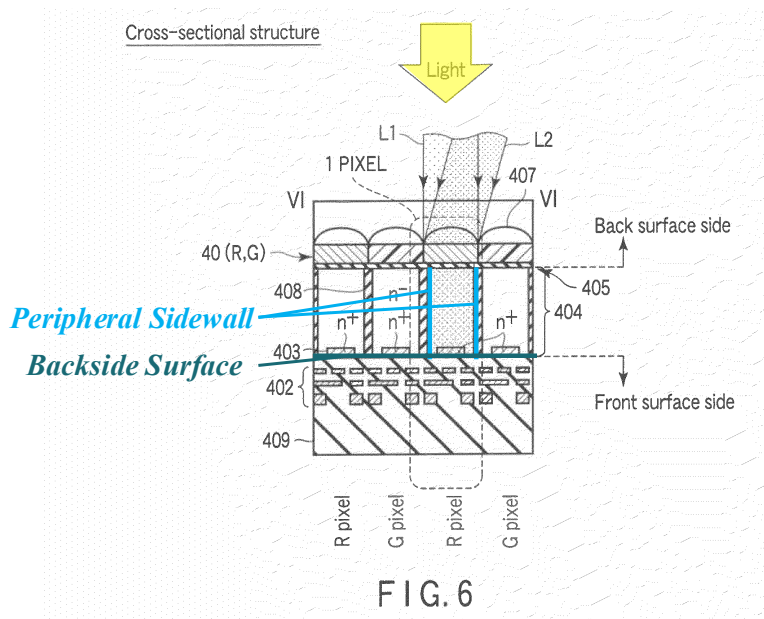
Hong at FIG. 2 (annotated).

382. Yamashita similarly discloses a pixel having a peripheral sidewall, namely sidewall of trench 33. *See* Claim 1[a][ii]; *see* ¶¶ 331-332. Yamashita explains that the imaging device of FIG. 6 is a “back-surface illumination type...wherein a light-receiving surface is provided on the back side of a semiconductor substrate, which is opposite to a semiconductor substrate surface on which a signal scanning circuit unit is formed.” *Yamashita* at [0049], *see* ¶¶ 57-59. As shown in FIG. 6, the “back surface side” of the semiconductor substrate 404 is the light incident surface, as indicated by the “light”-labeled arrow and expressly stated in Yamashita as the “light-receiving region.” *Yamashita* at [0101], FIG. 6. The side opposite the “back surface side” is the “front surface side.” *Id.*; *Yamashita* at [0049], [0101]. Yamashita describes the forming method of the FIG. 6 embodiment, including attaching a first support substrate 31 to the substrate 404 (see *Yamashita* at FIG. 9, [0100]), and

selectively etching the trench 33 on the back side surface of substrate 404 (which is the light-receiving region) “to the surface of the first support substrate 31.”  
*Yamashita* at [0102], [0107]-[0109] (disclosing removing support substrate 31 and turning substrate 404 upside down to complete forming the imager device).



*Yamashita* at FIG. 11, (annotated)



*Yamashita* at FIG. 6 (annotated)

383. “Thus, incident light can be radiated on the silicon (Si) surface (back surface) which is opposite to the silicon (Si) surface (front surface)....”. *Yamashita* at [0120]. Yamashita therefore teaches or suggests the trench (and therefore, the *sidewall* of the trench) *extends...to the backside surface*.

## 2. Motivation to Combine

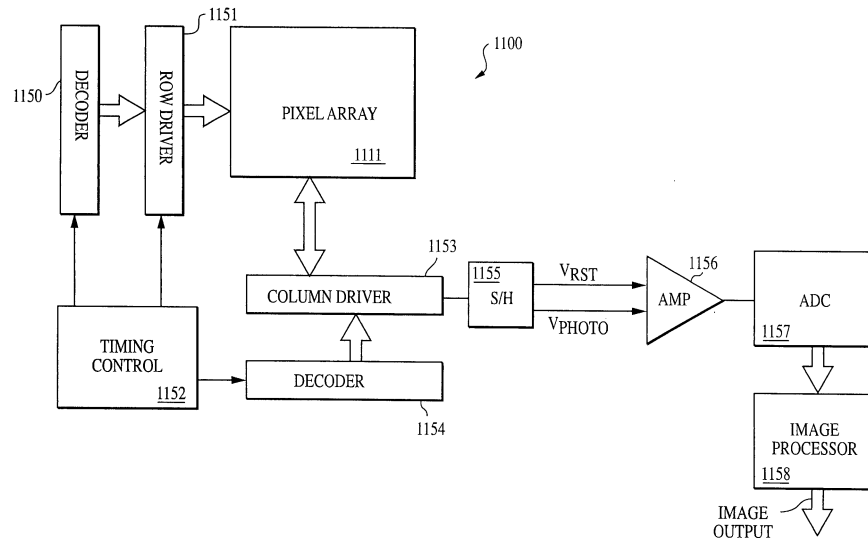
*Hong* at FIG. 2 (annotated).

386. A POSITA would have understood that “the deeper the trench 202 the better the isolation. With respect to CMOS image sensors in particular, the deeper the trench 202 the higher the electron storage capacitance of the CMOS image sensor.” *See e.g., Mouli* at 4:17-20. A POSITA would have also understood “longer sidewalls allow for a larger electrical connection region 323 along the sidewalls of the trench 202 such that electron storage capacitance, e.g., hole accumulation, in the electrical connection region 323 is increased[.]” *See e.g., Mouli* at 4:22-26. A POSITA would have further appreciated “deep trenches increase the sensitivity of a pixel while reducing crosstalk” including “electronic crosstalk” since electron-hole pairs cannot “migrate” between pixels. *See e.g., Venezia* at 3:35-40.

387. This modification would have had a reasonable expectation of success given etching trenches was well-known in the art, as I noted above. *See Claim 1[a][ii]; see ¶ 336.*

**N. *Claim 7: “An array of light trapping pixel devices of claim 1.”***

388. Hong expressly teaches “a pixel array 1111 containing a plurality of pixel cells arranged in rows and columns.” *Hong* at [0047]-[0048], FIG. 11.



Hong, FIG. 11.

389. Each pixel 200 in image sensor 1100 traps light by reflecting incident light back into the pixel. See ¶¶ 317-318. For example, each pixel 200 includes a reflective layer that “serves to reflect incident light not initially absorbed into the photo-conversion device, back to the photo-conversion device.” Hong at Abstract.

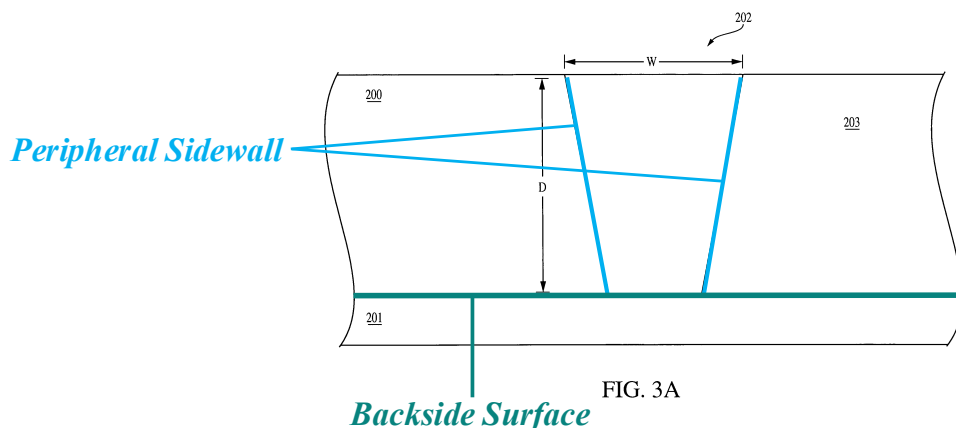
390. Pixel array 1111 is *[a]n array of light trapping pixel devices*, as Hong’s pixels 200 are *pixel devices* that are *light trapping*.

**XVI. GROUND 9: CLAIM 5 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, HWANG-795, KAES, AND MOULI**

**A. Claim 5: “The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

**1. Mouli’s Teachings**

391. Mouli teaches a trench (e.g., trench 202) that *extends to the backside surface*. Mainly, “a trench is etched into a substrate adjacent to a photodiode region, wherein the trench extends to an epitaxial layer below the substrate.” *Mouli* at 2:52-55. Similar to Hong, trench 202 is part of Mouli’s pixel (defined as “a picture element unit cell...containing a photo-conversion device...”) since “trench 202 is etched into substrate 200, which is adjacent to photodiode region 203. The trench 202 preferably extends near, or directly above base layer 201” therefore extending to the backside surface (base layer 201) of Mouli’s pixel. *Mouli* at 3:46-49, 4:45-47. Base layer 201 is “the bottom p-substrate epi layer” underneath “the top surface p-layer 203[.]” *Mouli* at 5:14-15, FIGS. 2, 3A.



*Mouli* at FIG. 3A.

## 2. *Motivation to Combine*

392. A POSITA would have been motivated and found it obvious to further modify Hong-Yamashita-Hwang-584 to similarly etch Hong's isolation region 203 (and the accompanying sidewall) to extend[]...to the backside surface, per Mouli. Mouli expressly motivates the combination, stating a "deeper trench better inhibits electrons from diffusing under the isolation trench to an adjacent pixel thereby preventing crosstalk between neighboring pixels." *Mouli* at 4:17-32, 2:9-10.

393. A POSITA would have understood that deeper trenches help overcome "a common problem associated with the formation of STI regions" "when ions are implanted in the substrate close to the bottom and edges or sidewalls of the trench, current leakage can occur at the junction between the active device regions and the trench resulting in 'hot pixels.'" *Fan* at [0004]. Further, a POSITA would have appreciated the additional benefits of a deeper trench, which I noted above. *See* ¶ 386.

394. The modification would have had a reasonable expectation of success. Mouli informs a POSITA how to make the trench using a "directional etching process, such as Reactive Ion Etching (RIE)[,]" which was well-known. Mouli at 5:57-58. The '764 Patent similarly describes "processes contemplated for forming trenches or other isolation features can include, reactive ion etch, isotropic plasma etch, wet chemical etch." '764 *Patent* at 7:43-46. Hong and Mouli are also similarly

concerned with “photons having long wavelengths.” *Mouli* at 2:45-46. For example, Hong describes the need for “a pixel that can capture longer wavelengths of light, e.g., 650-750 nm or longer, with improved quantum efficiency and without increased cross talk.” *Hong* at [0005]. Mouli also describes how “it is desirable to provide an improved isolation technique that prevents crosstalk from one pixel cell to another, and particularly from a pixel cell that absorbs photons having long wavelengths.” *Mouli* 2:43-46, 2:9-14 (describing a “drawback associated with STI is crosstalk from a photon that is absorbed deep within the substrate...”). Forming trench isolation features in pixels was well-known, indicating such modifications would have been within the expertise of a POSITA. *See* ¶ 336.

## **XVII. GROUND 10: CLAIM 6 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, HWANG-795, KAES, AND KONNO**

### **A. *Claim 6: “The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”***

#### **1. *Konno’s Teachings***

395. As I described above, Konno teaches *a backside light trapping material that is a metal layer*. *See* ¶¶ 207-208.

#### **2. *Motivation to Combine***

396. Based on the teachings of Konno, it would have been obvious to replace Hong’s reflective layer 204 (i.e., *backside light trapping material*) with a *metal layer*. Using metal as reflectors in pixels was a common practice well before the

'764 Patent. *See, e.g., Cao* at Abstract (“The back reflector structure consists of...a first textured metal...such as aluminum.”). A POSITA would have understood that various metals were used in backside light trapping materials. *See, e.g., Nozaki* at [0035] (“The reflective layer 340 is typically a reflective metal such as aluminum or tungsten.”). Compared to Bragg reflectors, a metal layer would have offered more reflectivity, as metals typically have higher reflectivity than other materials. Indeed, a “pure silver layer is the most highly reflective material having an integrated total reflectivity of about 95% or higher over the wavelength range from 600 nm to 1200 nm.” *See e.g., Cao* at [0006]. Conversely, Bragg reflectors like Hong’s reflective layer 204 “produce a highly reflective DBR mirror at a targeted wavelength.” *Hong* at [0027]. A POSITA would have appreciated that based on design choice dependent on use environment and desired functionality of the image sensor, various wavelengths of light may be targeted for a particular application, and that it is known and obvious to use various materials, such as metal, to achieve the desired light trapping properties for the particular use case or application.

397. Accordingly, “metallic reflectors offer the advantage of high reflectivity in thin films.” *See e.g., Holm* at 8:11-12. The ability to offer “high reflectivity in thin films” using metal layers is an advantage over Bragg reflectors because “multiple layer pairs are typically required to achieve sufficient reflectivity” with their use. *See e.g., Holm* at 8:17-19.

398. A POSITA would have recognized that using just one metal layer, per Konno, compared to designing the “optimal number of sub-layers” for a Bragg reflector, per Hong. *Hong* at [0027]. Thus, a POSITA would have been motivated to improve similar image sensors in the same way to predictably result in the simplification in the manufacturing process and increased broadband light reflectivity. Such a combination is a simple substitution of one known element (e.g., metal layer as a backside light trapping material) for another (e.g., a Bragg reflector as a backside light trapping material).

399. There would have been a reasonable expectation of success in implementing Konno’s metal second reflecting layer 120 in the Hong-Yamashita-Hwang-584-Hwang-795-Kaes modified image sensor because Konno describes how to form reflecting layer 120. *Konno* at 11:42-56 (“[T]he first reflecting layer is manufactured by forming a film with a metal such as aluminum or silver by, for example, the deposition method. The second reflecting layer 120 can be manufactured in the same manner as that for the first reflecting layer 121.”). Further, the materials used in Konno are similarly described in the ’764 Patent. *’764 Patent* at 7:56-59 (describing “examples of metal reflector materials can include silver, aluminum....”).

400. Moreover, methods of forming metal layers were well-known and within the expertise of a POSITA. *See also e.g., Yamada* at 7:1-2 (“The reflecting

film 12a is formed by, for example, vapor deposition of a metal film.”); *Atwater* at [0054] (“Metallic layer 230 may be deposited by a vapor deposition process, such as a vacuum evaporation process, a PVD or sputtering process, a CVD process, or an ALD process.”); *Kim* at [0023] (“Reflective film layer 106A can be made of a metal material and can be formed by any metal film deposition method for forming a metal film[.] Preferably, reflective film 106A can be formed by a chemical vapor deposition (CVD) method or a physical vapor deposition (PVD) method.”).

**XVIII. GROUND 11: CLAIMS 8-12 AND 14-15 ARE OBVIOUS OVER HONG, YAMASHITA, AND HWANG-584**

**A. Claim 8[Pre]: “A light trapping device, comprising:”**

401. As I described above, Hong teaches *a light trapping device*. See Claim 1[Pre], ¶¶ 317-318, incorporated herein.

**B. 8[a]: “at least one light sensitive *pixel*”**

402. As I described above, Hong teaches *at least one light sensitive pixel*. See Claim 1[a], ¶¶ 319-324 incorporated herein.

**C. 8[a][i]: “having a *light incident surface*, a *backside surface* opposite the light incident surface,”**

403. As I described above, Hong teaches *a pixel having a light incident surface, a backside surface opposite the light incident surface*. See Claim 1[a][i], ¶¶ 325-326, incorporated herein.

- D. 8[a][ii] “and a *peripheral sidewall* disposed into at least a portion of the *pixel* and extending at least substantially around the pixel periphery;”

404. As I described above, Hong-Yamashita teaches a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. See Claim 1[a][ii], ¶¶ 327-338, incorporated herein.

- E. 8[b]: “a *backside light trapping material* substantially covering the *backside surface*; and”

405. As I described above, Hong teaches a backside light trapping material substantially covering the backside surface. See Claim 1[b], ¶¶ 339-341, incorporated herein.

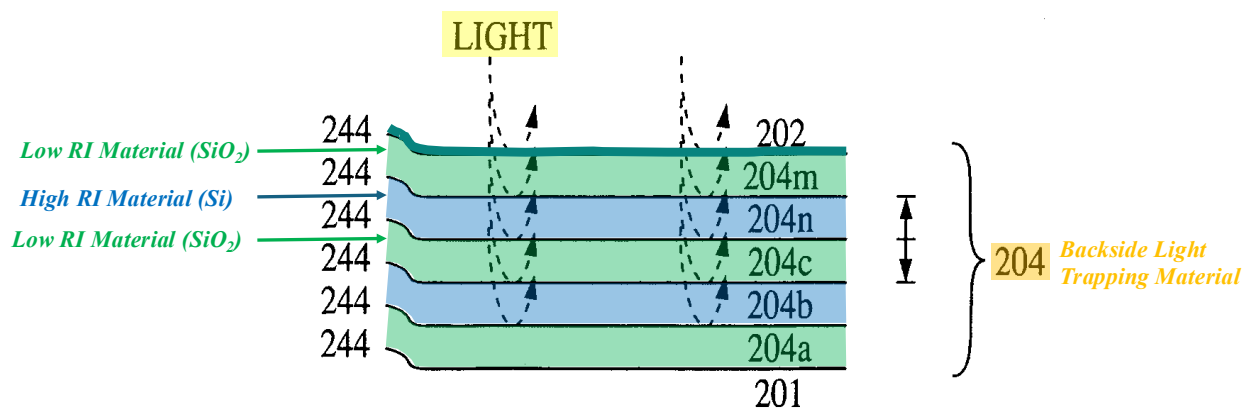
- F. 8[c]: “a *peripheral light trapping material* substantially covering the *peripheral sidewall*,”

406. As I described above, Hong-Yamashita-Hwang-584 teaches a *peripheral light trapping material* substantially covering the peripheral sidewall. See Claim 1[c], ¶¶ 342-355 incorporated herein.

- G. 8[d]: “wherein at least one of the *backside light trapping material* and the *peripheral light trapping material* includes a *first material* sandwiched between *two second materials*, wherein the *first material* has a higher refractive index as compared to the *two second materials*, and wherein the difference in refractive index between the *first material* and the *two second materials* is at least 0.2, and”

407. Both Hong’s reflective layer 204 (i.e., the *backside light trapping material*) and Hong-Yamashita-Hwang-584’s device separation membrane 300 (i.e., the *peripheral light trapping material*) meet Claim 8[d].

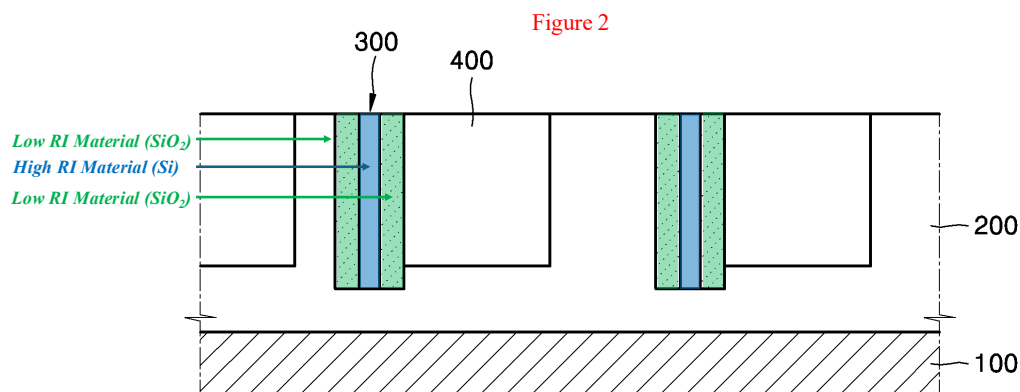
408. Regarding Hong's reflective layer 204, "sub-layers 204b and 204n are Si and sub-layers 204a, 204c, and 204m are SiO<sub>2</sub>, such that reflective layer 204 has an SiO<sub>2</sub>/Si structure." *Hong* at [0024] Therefore, the SiO<sub>2</sub> (i.e., the second material) and Si (i.e., the first material) sub-layers are alternately stacked to create a repeated low-high-low sandwich structure. *See* Claim 1[c][i]. Per Hwang-584's express teachings, the difference between the refractive indices of silicon ("around 3.7 to 5.7") and silicon dioxide ("around 1.46") is at least 2.24, which is at least 0.2. *Hwang-584* at [0025]; *see* ¶ 361. Thus, Hong teaches that the backside light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2:



*Hong* at FIG. 3 (annotated).

409. Hwang-584 expressly teaches that “the membranes of two different materials can be of any two materials whose difference in refractive indices is at least 2” in forming the device separation membrane (i.e., peripheral light trapping material). *Hwang-584* at [0014].

410. Similarly, device separation membrane (i.e., the peripheral light trapping material) includes silicon membrane 340 (i.e., a first material) sandwiched between silicon dioxide membranes 320 (e.g., two second materials). *See Claim 1[e]*. The difference in the refractive indices of silicon (“around 3.7 to 5.7”) and silicon oxide (“around 1.46”) is at least 2.24, which is at least 0.2. *Hwang-584* at [0025], FIG. 2. Thus, Hong-Yamashita-Hwang-584 teaches that the *peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2.*



*Hwang-584* at FIG. 2 (annotated).

**H. 8[d][i]: “and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.”**

411. As I described above, Hong-Yamashita-Hwang-584 teaches *light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. See Claim 1[d], ¶¶ 373-376, incorporated herein.

**I. Claim 9: “The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.”**

412. As described above, Hong-Yamashita-Hwang-584’s two second materials are silicon dioxide, which has a reflective index of less than 2.1 per Hwang-584, which expressly teaches that “[g]enerally, silicon dioxide’s refractive index is around 1.46[.]” *Hwang-584* at [0025]; see Claim 8[d], ¶¶ 407-410.

**J. Claim 10: “The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.”**

413. As discussed above, Hong-Yamashita-Hwang-584’s two second materials are silicon dioxide, which is an *oxide*. See *Hong* at [0033] (“a silicon oxide, such as SiO or SiO<sub>2</sub>...”).

- K. Claim 11: “The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.”**

414. As described above, the two second materials are silicon dioxide (SiO<sub>2</sub>). See Claims 1[d], 8[d], 9. Silicon dioxide is a member of the silicon oxide group, and silicon dioxide is extremely commonly used in semiconductors.

- L. Claim 12: “The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.”**

415. As discussed above, Hong-Yamashita-Hwang-584’s first material is silicon, which has a refractive index of “around 3.7 to 5.7 depending on the wavelength.” Hwang-584 at [0025]. Thus, the Hong-Yamashita-Hwang-584 combination teaches that first material includes a material having a refractive index of greater than or equal to about 2.1.

- M. Claim 14: “The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.”**

416. As I described above, Hong-Yamashita teaches the *peripheral sidewall extends completely around the pixel periphery*. See Claims 1[a][ii], 4 ¶¶ 327-337, ¶ 379, incorporated herein.

N. ***Claim 15: “The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”***

417. As I described above, Hong-Yamashita-Hwang-584 teaches the *peripheral sidewall extends from the light incident surface to the backside surface*. See Claim 5, ¶¶ 380-387, incorporated herein.

**XIX. GROUND 12: CLAIM 13 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, AND KOMURO**

A. ***Claim 13: “The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.”***

***1. Komuro’s Teachings***

418. Komuro teaches silicon, which is “any one of single crystal silicon, amorphous silicon, and polysilicon” having a refractive index between 3.85 and 4.69 at the wavelengths of blue, green, and red light:

| TABLE 1                    |                      |                       |                     |                            |                       |                     |
|----------------------------|----------------------|-----------------------|---------------------|----------------------------|-----------------------|---------------------|
|                            | Refractive Index (n) |                       |                     | Extinction Coefficient (k) |                       |                     |
|                            | Blue Light<br>450 nm | Green Light<br>550 nm | Red Light<br>650 nm | Blue Light<br>450 nm       | Green Light<br>550 nm | Red Light<br>650 nm |
| Germanium                  | 4.5                  | 6.0                   | 5.5                 | 2.3                        | 2.1                   | 1                   |
| Silicon                    | 4.69                 | 4.08                  | 3.85                | 0.151                      | 0.03                  | 0.017               |
| Tungsten                   | 3.31                 | 3.48                  | 3.76                | 2.47                       | 2.72                  | 2.95                |
| Plasma Silicon Nitride     | 2.07                 | 2.04                  | 2.01                | 0.004                      | 0                     | 0.002               |
| Aluminum                   | 0.618                | 0.958                 | 1.47                | 5.47                       | 6.69                  | 7.79                |
| Copper                     | 1.17                 | 0.9                   | 0.21                | 2.39                       | 2.6                   | 3.67                |
| Reference: Silicon Dioxide | 1.45                 | 1.45                  | 1.45                | 0.00                       | 0.00                  | 0.00                |

Komuro at Table 1; [0138].

419. A POSITA would have understood that polysilicon is another name for polycrystalline silicon. *See, e.g., Juengling* at 5:32 (“polycrystalline silicon (‘polysilicon’)...”). Thus, the combination of Hong-Yamashita-Hwang-584 and Komuro teaches *wherein the first material* (i.e., silicon) *includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon.*

## 2. Motivation to Combine

420. A POSITA would have found it obvious and been motivated to implement Hong-Yamashita-Hwang-584’s first material, silicon, as “any one of single crystal silicon, amorphous silicon, and polysilicon” because each possesses a

refractive index from 3.85 to 4.69 dependent on wavelength (i.e., “around 3.7 to 5.7 depending on the wavelength,” per Hwang-584’s express teaching of the refractive index for silicon). *Komuro* at [0137]-[0138].

421. A POSITA would consider the refractive indices of 3.85, 4.08, and 4.69 for different wavelengths of light as taught by *Komuro*, to fall in the range of “around 3.7 to 5.7 depending on the wavelength” provided by Hwang-584. Thus, a POSITA would have been motivated to combine prior art elements (e.g., types of silicon such as single crystal, amorphous, and polysilicon and image sensors) according to known methods to yield the predictable result of a first material, silicon, having a refractive index of approximately 3.85 to 4.69 in the red, green, or blue wavelengths. A POSITA would also understand that with small differences in the refractive index of the “first material”, the net reflectivity of a Bragg structure within the visible spectrum would be maintained with adjustments in other design parameters (e.g., the number or thickness of layers).

422. There would have been a reasonable expectation of success at least because each of single crystal silicon, amorphous silicon, and polysilicon were widely used in fabricating image sensors. *See, e.g., Ogawa* at 3:58-60 (“A silicon substrate 11 made of, for example, single crystal silicon...is provided in a CMOS image sensor[.]”); *Inuiya* at [0025] (“In the solid-state imaging device, each of the photoelectric conversion elements...are formed of amorphous silicon.”); *Mouli* at

2:57-59 (“Subsequently, a polysilicon deposition is used to fill the trench.”). Moreover, the modification would have been successful because single crystal silicon, amorphous silicon, and polysilicon each possess Hwang-584’s desired refractive index of “3.7 to 5.7 depending on the wavelength” in the Hong-Yamashita-Hwang-584 combination. *Hwang-584* at [0025].

**XX. GROUND 13: CLAIMS 17-19 ARE OBVIOUS OVER HONG, YAMASHITA, AND HWANG-584 IN COMBINATION WITH MOULI AND/OR NOZAKI**

**A. Claim 17[Pre]: “A *light trapping device*, comprising:”**

423. As I described above, Hong teaches a *light trapping device*. See Claim 1[Pre], ¶¶ 317-318, incorporated herein.

**B. 17[a]: “at least one light sensitive *pixel*”**

424. As I described above, Hong teaches *at least one light sensitive pixel*. See Claim 1[a], ¶¶ 319-324, incorporated herein.

**C. 17[a][i]: “having a *light incident surface*, a backside surface opposite the light incident surface,”**

425. As I described above, Hong teaches *a pixel having a light incident surface, a backside surface opposite the light incident surface*. See Claim 1[a][i], ¶¶ 325-326, incorporated herein.

- D. 17[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the *pixel* and extending at least substantially around the pixel periphery;”

426. As I described above, Hong-Yamashita teaches a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. See Claim 1[a][ii], ¶¶ 327-338, incorporated herein.

- E. 17[b]: “a *backside light trapping material* substantially covering the *backside surface*; and”

427. As I described above, Hong teaches a backside light trapping material substantially covering the backside surface. See Claim 1[b], ¶¶ 339-341, incorporated herein.

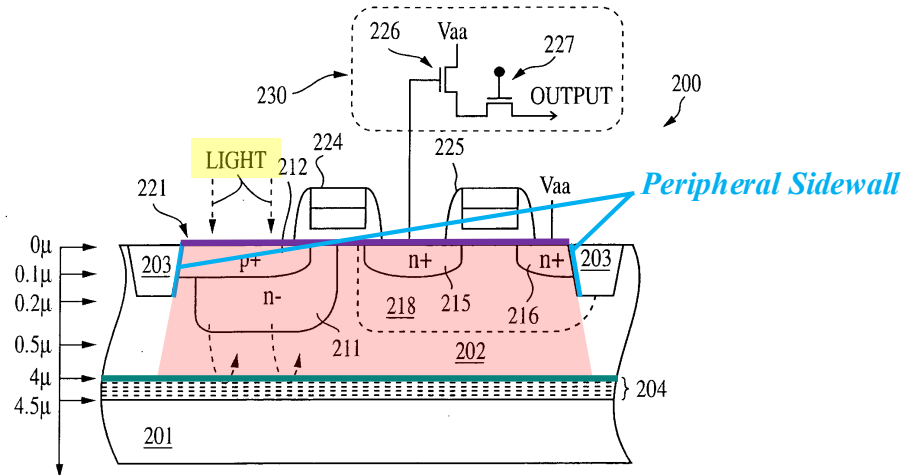
- F. 17[c]: “a *peripheral light trapping material* substantially covering the *peripheral sidewall*,”

428. As I described above, Hong-Yamashita-Hwang-584 teaches a peripheral light trapping material substantially covering the peripheral sidewall. See Claim 1[c], ¶¶ 342-355, incorporated herein.

- G. 17[c][i]: “wherein at least one of the *backside light trapping material* and the *peripheral light trapping material* has a sloped surface at the pixel device interface,”

1. *Hong’s Sloped Trench Wall*

429. As shown in FIG. 2, Hong teaches a *sloped* trench wall:

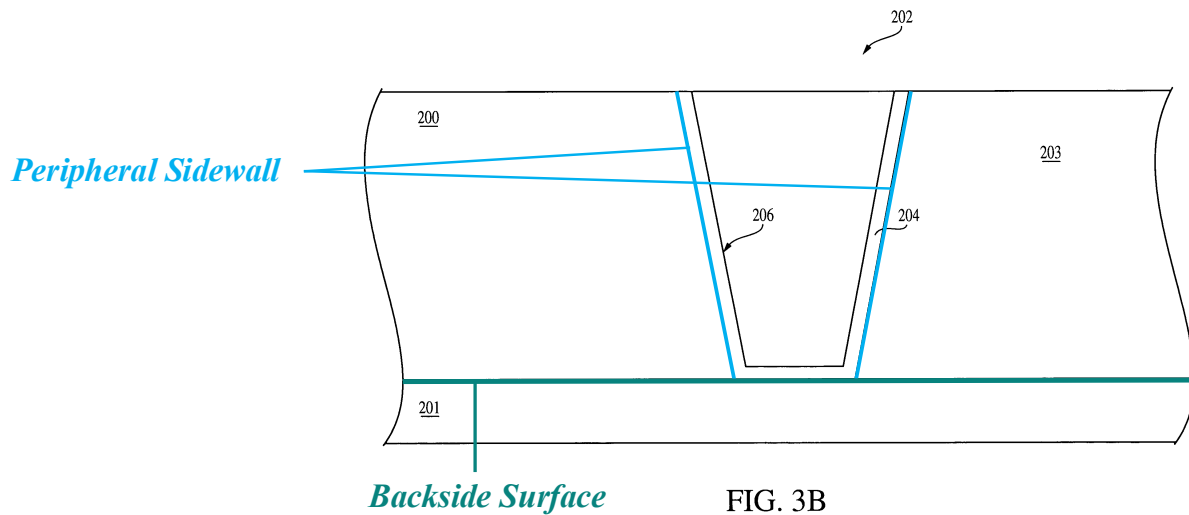


Hong at FIG. 2 (annotated).

430. In the modified Hong-Yamashita-Hwang-584 pixel, Hwang-584's peripheral light trapping material (i.e., device separation membrane 300), substantially covers Hong's peripheral sidewall (i.e., a sidewall of isolation region 203). *See* Claims 1[a][ii], 1[c]. Therefore, a POSITA would have understood the peripheral light trapping material has a sloped surface given the slope of Hong's peripheral sidewall.

## 2. Mouli's Sloped Trench Wall

431. To the extent SiOnyx contends Hong-Yamashita-Hwang-584 does not each Claim 17[c][i], as I described above, Mouli also teaches sloped sidewalls. *See* ¶¶ 240-241.



*Mouli* at FIG. 3B (annotated to show sloped sidewalls).

### 3. *Nozaki's Sloped Backside Surface*

432. As I described above, Nozaki teaches a *backside light trapping material that has a sloped surface*. See ¶¶ 248-249.

### 4. *Motivation to Combine*

433. Based on the teachings of Nozaki, it would have been obvious to modify Hong-Yamashita-Hwang-584 to have a concave-shaped (i.e., sloped) backside surface. The modification would have resulted in Hong's reflective layer 204 (backside light trapping material) being sloped. Pixels with conventionally flat backside reflectors provide one angle of reflection at which incident light reflects. *Nozaki* at [0027]. The complex shape of Nozaki's reflectors 140, 142, 144 allows for "multiple angles of reflection that reflect and focus incident light towards the photosensitive element[.]" thus expressly motivating the combination. *Nozaki* at

[0027], [0019]. A POSITA would have also understood a sloped backside light trapping material would improve the “sensitivity” of Hong’s image sensor 1100 by “redirect[ing] the non-absorbed incident light towards the photodiode” to “increase the probability that the light will be absorbed[.]” *Nozaki* at 3:7-9; 4:42-43, FIG. 8. Additionally, the combination is the use of a known technique (implementing concave-shaped (sloped) backside reflectors) to improve similar image sensors in the same way.

434. This modification would have had a reasonable expectation of success given the method used to form concave-shaped surface 330 (an “isotropic etch” of a substrate before reflective layer 340 is “deposited across”) was common in the art. *Nozaki* at 4:33-34, 5:25-32, FIG. 3A. Backside surfaces with a “complex shape (such as a concave, convex, or trapezoidal shape)” were similarly well-known in the art. *See e.g., Tian* at 3:44-53, 4:40-50. Moreover, Hong already discloses a backside surface and methods for forming a backside light trapping material, *Nozaki* teaches methods of forming the concave-shaped surface, and because methods of providing sloped backside surfaces in pixels were well-known. *Hong* at [0031]; *Nozaki* at [0034]-[0037].

## **5. Obviousness of Combining Both Mouli and Nozaki**

435. A POSITA would have been motivated and found it obvious to modify both Hong’s backside surface (and commensurately, backside light trapping material

on the backside surface) and peripheral sidewall (and commensurately, the peripheral light trapping material on the peripheral wall) to have a sloped surface, as the modification would have simply entailed combining the individual sloped surfaces and motivations discussed above.

436. That is, the benefits achieved from each sloped surface modification would similarly be achieved in the combination including sloped surfaces for both the backside and peripheral light trapping materials. There would have been a reasonable expectation of success, as the peripheral and light trapping materials are distinct materials in the image sensor that could be independently formed to be sloped per the techniques discussed above.

**H. [17][c][ii]: “and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.”**

437. As I described above, Hong-Yamashita-Hwang-584 teaches wherein *light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel*. See Claim 1[d], ¶¶ 373-376, incorporated herein.

**I. Claim 18: “The device of claim 17, wherein the *peripheral sidewall* extends completely around the pixel periphery.”**

438. As I described above, Hong-Yamashita teaches the *peripheral sidewall extends completely around the pixel periphery*. See Claims 1[a][ii], 4 ¶¶ 327-338, ¶ 379, incorporated herein.

**J. Claim 19: “The device of claim 17, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

439. As I described above, Hong-Yamashita-Hwang-584 teaches the peripheral sidewall extends from the light incident surface to the backside surface. See Claim 5, ¶¶ 380-387, incorporated herein. Alternatively, Hong-Yamashita-Hwang-584-Mouli teaches the peripheral sidewall extends from the light incident surface to the backside surface. See Claim 5, ¶¶ 391-394, incorporated herein.

**XXI. GROUND 14: CLAIM 20 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, AND MOULI AND/OR NOZAKI IN FURTHER VIEW OF KONNO**

**A. Claim 20: “The device of claim 17, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

440. As I described above, Hong-Yamashita-Hwang-584-Konno and Mouli and/or Nozaki teaches a *backside light trapping material that is a metal layer*. See Claim 6, ¶¶ 395-400, incorporated herein.

**XXII. GROUND 15: CLAIMS 16 AND 21-25 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584, AND KONNO**

**A. Claim 16: “The device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

441. As I described above, Hong-Yamashita-Hwang-584-Konno teaches a *backside light trapping material that is a metal layer*. See Claim 6, ¶¶ 395-400, incorporated herein.

**B. Claim 21**

442. There are two alternative mappings for Claim 21, both relying on a combination of Hong-Yamashita-Hwang-584 and Konno. In the first mapping (i.e., following) of Claim 21, Hong-Yamashita-Hwang-584 is further modified to comprise Konno's textured transparent layer 136 from Konno's second embodiment depicted in Figure 7. In the combination, Hong is modified such that transparent layer 136 is placed between Hong's *backside surface* and reflective layer 204 (*backside light trapping material*).

**C. Claim 21[Pre]: "A *light trapping device*, comprising:"**

443. As I described above, Hong teaches a *light trapping device*. See Claim 1[Pre], ¶¶ 317-318, incorporated herein.

**D. 21[a]: "at least one light sensitive *pixel*"**

444. As I described above, Hong teaches *at least one light sensitive pixel*. See Claim 1[a], ¶¶ 319-324, incorporated herein.

**E. 21[a][i]: "having a *light incident surface*, a *backside surface* opposite the light incident surface,"**

445. As I described above, Hong teaches a pixel *having a light incident surface, a backside surface opposite the light incident surface*. See Claim 1[a][i], ¶¶ 325-326, incorporated herein.

- F. 21[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the *pixel* and extending at least substantially around the pixel periphery;”

446. As I described above, Hong-Yamashita teaches a *peripheral sidewall* disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. See Claim 1[a][ii], ¶¶ 327-338, incorporated herein.

- G. 21[b]: “a *backside light trapping material* substantially covering the *backside surface*;”

447. As I described above, Hong teaches a *backside light trapping material* substantially covering the backside surface. See Claim 1[a][ii], ¶¶ 339-341, incorporated herein.

- H. 21[c]: “a *peripheral light trapping material* substantially covering the *peripheral sidewall*; and”

448. As I described above, Hong-Yamashita-Hwang-584 teaches a *peripheral light trapping material* substantially covering the peripheral sidewall. See Claim 1[c], ¶¶ 342-355, incorporated herein.

- I. 21[d]: “a *textured layer* positioned to interact with light proximal to the backside surface,”

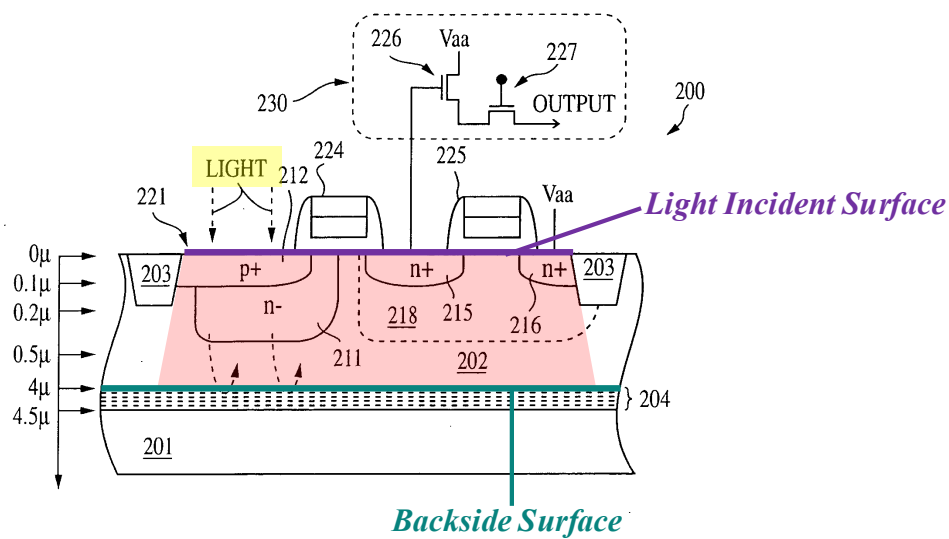
1. *Konno’s Teachings*

449. As I described above, Konno teaches a *textured layer* positioned to interact with light proximal to the backside surface. See Claim 21[d], ¶¶ 277-280, incorporated herein.

## 2. Motivation to Combine

450. A POSITA would have found and obvious and been motivated to include Konno's transparent layer 136 underneath the backside surface of Hong's *pixel* and on top of the base multi-layered reflection layer 155a (*backside light trapping material*). In the combination, the transparent layer 136 (*textured layer*) is located beneath Hong's *backside surface*, between it and the *backside light trapping material*. Hong at Figure 2.

451. Because transparent layer 136 is underneath Hong's backside surface, transparent layer 136 (*textured layer*) would transmit and reflect light that is incident on the backside surface. Thus, in the combination, a POSITA would have understood that because transparent layer 136 (*textured layer*) is positioned underneath the backside surface and does not absorb light and instead transmits and reflects light, that *is positioned to interact with light proximal to the backside surface*.



*Hong* at FIG. 2 (illustrating the *backside surface* under which transparent layer 136 (*textured layer*) would be placed).

452. A POSITA would have known that providing a textured layer as taught by Konno on the backside surface would have offered the benefit of “provid[ing] a diffuse reflecting surface which increases the path length of the reflected light and also[] provide for enhanced internal reflection.” *Banerjee* at 1:26-29. Compared to smooth surfaces which provide specular reflection, light incident on a “textured back reflector” is “scattered in addition to being redirected” through the active region of a photovoltaic device. *Nath* at 2:63–3:21. Indeed, “light trapping structures” in solar cells including “randomly textured surfaces” were known to “increase the optical path length of the incident light, due to...light scattering on textured surfaces at oblique angles[.]” *Sai* at p. 2. A POSITA would further understand that increasing the path length of light advantageously enhances quantum efficiency, because as the path length of light increases, the probability of light absorption increases. *See, e.g., Mallick* at p. 456 (...diffraction of light to increase optical path length contribute[s] to absorption enhancement in the a-Si cell.”)

453. Thus, a POSITA would have been motivated to modify *Hong* to include Konno’s transparent layer 136 (textured layer) such that light incident on the backside surface would be diffusely reflected instead of specularly reflected. The modification is the application of a known technique (providing a textured layer) to

a known device (image sensor) in the same way. The modification would have predictably improved Hong's image sensor by working in conjunction with reflective layer 204 and enhancing internal reflection of light incident on the backside surface, thereby increasing quantum efficiency.

454. The modification would have had a REOS at least because it would have merely required depositing Konno's transparent layer 136 on the backside surface of Hong prior to the formation of reflective layer 204 and/or a POSITA would have possessed the necessary skills to implement layer 136 into Hong's manufacturing process. *See Hong* at [0031] (describing how "[t]he SiO<sub>2</sub>/Si structure can be formed using known SOI techniques, such as, for example, wafer bonding techniques...or implantation techniques..."). Additionally, Konno teaches how to form the texture (i.e., by microlithography or sputtering). *Konno* at 14:42-45.

455. A POSITA would have also understood that reflective layer 204 would have still been able to be formed on the textured surface of transparent layer 136. As described above, the first layer of Hong's reflective layer 204 is a silicon oxide. Thus, a POSITA would have merely needed to form Hong's silicon oxide form on the surface of transparent layer 136 and continue with the manufacturing process. Techniques to form a silicon oxide layer on a textured surface were known and it was well within the skills of a POSITA to it. *See, e.g., Smith* at 3:31-39, 3:58-65.

456. Additionally, transparent layer 136 (*textured layer*) would not impact the ability of Hong's reflective layer 204 to reflect light back toward the *pixel* because each of the layers different refractive indexes would still be present in the combination, and light contacting reflective layer 204 would still be reflected back toward Hong's pixel due to the difference in refractive index of the layers comprising reflective layer 204.

**J. 21[d][i]: “wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.”**

457. As I described above, Hong-Yamashita-Hwang-584 teaches wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel. *See* Claim 1[d], ¶¶ 373-376, incorporated herein.

**K. Claim 21**

**1. Explanation of Combination and Motivation for the Combination**

458. The following mapping of Claim 21 also relies on Hong and Konno. In this mapping, Hong is modified to comprise Konno's combined textured transparent layer 136 and textured second reflecting layer 120 in the second embodiment depicted in FIG 7. As I discuss below, a POSITA would have been motivated and found it obvious to replace Hong's reflective layer 204 (*backside light trapping*

*material*) with Konno's combined transparent layer 136 and second reflecting layer 120 in the FIG. 7 embodiment to leverage the combined benefits of both layers.

459. First, a POSITA would have found it obvious and been motivated to implement Konno's textured second reflecting layer 120. Second reflecting layer 120 is formed of a metal such as "aluminum or silver." *Konno* at 14:41-41, 11:42-52. As I have discussed previously, metal layers as backside light trapping materials were well-known and provided many advantages. *See* ¶¶ 260-261. Specifically, metal layers were known to offer more broadband reflectivity because metals have higher reflectivity than other materials. *See* ¶¶ 260-261. Indeed, a "pure silver layer is the most highly reflective material having an integrated total reflectivity of about 95% or higher over the wavelength range from 600 nm to 1200 nm." *See, e.g., Cao* at [0006]. Further, having a metal layer would offer the advantage of achieving "high reflectivity in thin films" versus a Bragg reflector where "multiple layer pairs are typically required to achieve sufficient reflectivity." *See, e.g., Holm* at 8:17-19; ¶ 260. Thus, a POSITA would have recognized the advantage of implementing Konno's second reflecting layer 120.

460. A POSITA would have also recognized that a textured metal layer, compared to a non-textured metal layer, would provide the same advantages that I discussed above. *See* ¶ 283. Specifically, layers having textured surfaces were known to reflect like diffusely versus specularly, which increases the path length of

incident light and thereby increases the probability of light absorption. *See* ¶ 283. Thus, a POSITA would have recognized that Konno's textured metal second reflecting layer 120 (as opposed to a textured layer alone or a metal layer alone) would simultaneously provide the advantages of both types of layers. Accordingly, a POSITA would have been motivated and found it obvious to implement Konno's textured metal second reflecting layer 120 into Hong's image sensor 1100.

461. Second, a POSITA would have found it obvious and been motivated include Konno's textured transparent layer 136 in the combination. A POSITA would have recognized that because transparent layer 136 comprises "concaves and convexes of various sizes" (i.e., is a *textured layer*) that it too would diffusely reflect light and provide the advantages associated with textured layers that I discussed above. *Konno* at 15:3-5, 9-11; *See* ¶¶ 283. Additionally, a POSITA would have recognized that including Konno's textured transparent layer 136 alongside second reflecting layer 120 would have provided the benefits of having a textured layer without the surface of the Hong's *pixel* (including at least photodiode 221) having to be textured. *See* ¶¶ 320-324. Konno expressly teaches that having transparent layer prevents the photosensitive portion of Konno having to be textured, which would cause problems such as "increase in the dark current, generation of uneven electric field in the photoelectric conversion film 125, generation of trap of electric charge by energy level produced on the surface of photoelectric conversion film 125,

uneven characteristics and variation thereof among the elements 110, [and] generation of cross-talk between the elements 110.” *Konno* at 15:17-22. A POSITA would have similarly recognized that including textured transparent layer 136 in Hong would avoid issues associated with texturing the surface of Hong’s *pixel*. Indeed, it was known that “the surface state of the substrate is closely related to the photovoltaic characteristics of a semiconductor film formed thereupon, and as the roughness of the substrate surface increases, the characteristics of the semiconductor film decrease.” *See, e.g., Matsuyama* at 2:38-49. Additionally, it was known that “metals can diffuse into the semiconductor of the devices in which they are employed, and in doing so, adversely affect the photoresponsive characteristics of the devices.” *See, e.g., Czubatji* at 5:9-13. Accordingly, a POSITA would have been motivated include textured transparent layer 136 between Hong’s *backside surface* and textured metal second reflecting layer 120 to preserve the integrity of Hong’s *pixel* and prevent diffusion of metal into the semiconductor substrate.

462. In the combination, transparent layer 136 is the ***textured layer***, as recited by Claim 21[d], and second reflecting layer 120 is the ***backside light trapping material***, as recited by Claim 21[b]. The modification would have been straightforward and merely required depositing Konno’s transparent layer 136 on Hong’s *backside surface*, texturing the transparent layer 136 using microlithography or sputtering, as taught by Konno, and depositing a metal layer thereupon. *Konno* at

14:38-45. As I discussed above, metal was widely available material and techniques for depositing metal layers were well-known. See ¶¶ 266-268. Additionally, methods of texturing materials were well-known. *Konno* at 14:38-45; *Smith* at 3:31-35. A POSITA would have possessed the necessary skills to implement both transparent layer 136 and second reflecting layer 120 in Hong's image sensor 1100. Thus, the modification would have had a reasonable expectation of success. The modification is nothing more than the combination of prior art elements (textured layer, metal backside layer) using known methods (microlithographic texturing, material deposition) using known methods to obtain predictable results (improved reflectivity of light).

**L. Claim 21[Pre]: “A *light trapping device*, comprising:”**

463. As I described above, Hong teaches a light trapping device. See Claim 1[Pre], ¶¶ 317-318, incorporated herein.

**M. 21[a]: “at least one light sensitive *pixel*”**

464. As I described above, Hong teaches at least one light sensitive pixel. See Claim 1[a], ¶¶ 319-324, incorporated herein.

**N. 21[a][i]: “having a *light incident surface*, a *backside surface* opposite the light incident surface,”**

465. As I described above, Hong teaches a pixel having a light incident surface, a backside surface opposite the light incident surface. See Claim 1[a][i], ¶¶ 325-326, incorporated herein.

- O. 21[a][ii]: “and a *peripheral sidewall* disposed into at least a portion of the *pixel* and extending at least substantially around the pixel periphery;”

466. As I described above, Hong-Yamashita teaches a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery. See Claim 1[a][ii], ¶¶ 327-338, incorporated herein.

- P. 21[b]: “a *backside light trapping material* substantially covering the *backside surface*;”

1. *Hong’s Teachings*

467. As described above, Hong’s reflective layer 204 is a *backside light trapping material* substantially covering the *backside surface*. Claim 1[b], ¶¶ 339-341. However, as described below, a POSITA would have found it obvious to replace Hong’s reflective layer 204 with Konno’s metal second reflecting layer 120 in the second embodiment of FIG. 7.

2. *Konno’s Teachings*

468. As I described above, Konno teaches a *backside light trapping material* substantially covering the *backside surface*. See Claim 21[b], ¶¶ 299-302, incorporated herein.

3. *Motivation to Combine*

469. See ¶¶ 458-462. In the combination, Hong’s reflective layer 204 (*backside light trapping material*) is replaced with Konno’s metal second reflecting

layer 120 such that Hong's *backside surface* is *substantially covered* by Konno's *backside light trapping material*.

**Q. 21[c]: “a *peripheral light trapping material* substantially covering the *peripheral sidewall*; and”**

470. As I described above, Hong-Yamashita-Hwang-584 teaches a *peripheral light trapping material substantially covering the peripheral sidewall*.

See Claim 1[c], ¶¶342-355 incorporated herein.

**R. 21[d]: “a *textured layer* positioned to interact with light proximal to the backside surface,”**

**1. Konno's Teachings**

471. As I described above, Konno teaches a *textured layer positioned to interact with light proximal to the backside surface*. See Claim 21[d], ¶¶ 305-308, incorporated herein.

**2. Motivation to Combine**

472. See ¶¶ 458-462. In the combination, Konno's transparent layer 136 is located underneath Hong's *backside surface* and on top of metal second reflecting 120 (*backside light trapping material*, per the combination at Claim 21[b]).

**S. 21[d][i]: “wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.”**

473. Hong teaches wherein light contacting...the peripheral light trapping material is reflected back toward the pixel. See Claim 1[d] (incorporated herein).

474. Recall that at 21[b], Hong is modified to comprise Konno's second reflecting layer 120. *See* ¶¶ 467-469. Regarding second reflecting layer 220, Konno expressly teaches that it reflects incident light photons. *Konno* at 13:63-65. Specifically, "when it [second reflecting layer 120] the incident photons 132, it can thereby reflect them with a large amount of horizontal components, in other words, it can reflect them with a large reflection angle." *Konno* at 12:63-66. The reflection of incident light is shown in FIG. 7 of Konno, where it can be seen that reflected light reflects off second reflecting layer 120 and is redirected back toward photoelectric conversion film 135. *Konno* at FIG. 7.

475. In the combination, because second reflecting layer is underneath Hong's backside surface, light contacting second reflecting layer would similarly be reflected back toward at least photodiode 221 (part of the claimed pixel). *See* ¶¶ 319-324. Thus, in the above combination of Hong-Yamashita-Hwang-584-Konno, *light contacting the backside light trapping material...is reflected back toward the pixel.*

**T. Claim 22: "The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material."**

476. In both above mappings of Hong-Yamashita-Hwang-584-Konno, transparent layer 136 (textured layer) is located underneath the backside surface and on top of the backside light trapping material. In other words, in the first mapping of Hong-Yamashita-Hwang-584-Konno, transparent layer 136 is located underneath

Hong's backside surface and on top of reflective layer 204 (*backside light trapping material*). See ¶¶ 449-456. In the second mapping of Hong-Yamashita-Hwang-584-Konno, transparent layer 136 is located underneath Hong's backside surface and on top of second reflecting layer 120 (*backside light trapping material*). See ¶¶ 458-472, ¶¶ 471-472. Thus, both above mappings teach wherein the *textured layer is located between the backside surface and the backside light trapping material*.

**U. Claim 23: “The device of claim 21, wherein the peripheral sidewall extends completely around the pixel periphery.”**

477. As I described above, Hong-Yamashita teaches *a peripheral sidewall extending at least substantially around the pixel periphery*. See Claim 1[a][ii], ¶¶ 327-338, incorporated herein.

**V. Claim 24: “The device of claim 21, wherein the peripheral sidewall extends from the light incident surface to the backside surface.”**

478. As I described above, Hong-Yamashita teaches *a peripheral sidewall extending from the light incident surface to the backside surface*. See Claim 5, ¶¶ 3380-387, incorporated herein.

**W. Claim 25: “The device of claim 21, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.”**

479. In the above combination of Hong-Yamashita-Hwang-584-Konno, Hong's reflective layer 204 is replaced with Konno's metal second reflecting layer 120 (i.e., *metal layer*) that is “formed by forming a thin film of metal such as aluminum or silver by deposition.” *Konno* at 8:25-38, 11:42-52; Claim 21[b]. Thus,

the above combination of Hong and Konno renders obvious wherein at least one of the *backside light trapping material...is a metal layer*.

**XXIII. CONCLUSION**

480. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: April 16, 2025

By:

A handwritten signature in cursive script, reading "Stanley Shanfield", written in dark ink.

Dr. Stanley Shanfield

# Appendix A

# Stanley Shanfield



## Curriculum Vitae for Stanley Shanfield

### Education:

Massachusetts Institute of Technology, Ph.D., Physics, 1981

University of California, Irvine, B.S. Cum Laude, Physics, 1977

### Educational Awards:

Outstanding Research Project, U.C. Regents Award, 1977

Phi Beta Kappa, 1977

Four Year Scholarship, Tuition & Research, ERDA/DOE, 1977-1981

### Hands-On Professional Expertise:

Semiconductor Physics & Chemistry  
Semiconductor Fabrication: Silicon and III-V Materials  
Semiconductor Device & Integrated Circuit Engineering  
Semiconductor Equipment: Front & Back End  
Semiconductor Packaging Design and Manufacturing  
Passive Component Design and Manufacturing  
RF Design and Fabrication  
Digital Design & Fabrication  
Semiconductor Manufacturing in Silicon and III-V Materials  
MEMS Design and Fabrication: Electrical, Optical, & Sensing Devices  
Fiber Optic Device Design and Fabrication  
Integrated Optics & Electro-Optical Devices  
Plasma Physics

### Specialized Training:

Global Positioning Electronics, Systems and Components  
Six Sigma Semiconductor Manufacturing  
Microwave Engineering  
US Patent Law in Technology  
Patent Application and Prosecution  
Semiconductor Plasma Processing  
Thin Film Physics and Technology  
MEMS-based Gyroscopes and Accelerometers  
Thermoelectric Materials & Technology  
Phased Array Radar Engineering  
Antennas and Electromagnetic Propagation  
Solid State Optical Devices  
Fiber Optic Communication System Operation  
HALT and HAST Reliability Testing Methods

## **Professional Experience:**

### **Draper Laboratory Cambridge, MA**

**2003 – present**

#### **Division Leader, Advanced Hardware Development Distinguished Member of Technical Staff Technical Director**

Led division (about 80 staff) in re-invigorating multi-chip integrated circuit module facility, more than doubling associated revenues in two years. By most accounts, made division a viable business & technological entity again. Invented & led implementation of an ultra-miniature electronics fabrication technology which became a top laboratory priority. Led team in realization & fabrication of a newly designed precision MEMS-based gyroscope and associated ASIC. Found funding and led team in developing a miniature power source with energy density at least two orders of magnitude higher than any source previously built. Developed fabrication technology for semiconductor-based low phase noise oscillator design, allowing for receiver operation with extremely low signal strength. Many awards received, most recently, the Draper 2010 Distinguished Performance Award, and 2010 Best Patent Award.

### **Clarendon Photonics Newton, MA**

**2001 – 2003**

#### **Director, Packaging & Integration**

30 person photonic chip startup with \$18 million 2nd round funding. Invented and productized new, low cost and reliable semiconductor processing, packaging and pig-tailing technology for optical add-drop multiplexer. Established assembly and packaging process, and developed control electronics. Partner with Micron Technologies, using their R&D semiconductor facility.

### **AXSUN Technologies Bedford/Billerica, MA**

**1999 – 2001**

#### **Vice President, Operations 1999 – 2000**

Initially three staff members with \$6 million funding. Designed, fabricated and productized AXSUN's micro-electromechanical (MEM) Fabry-Perot optical filter. Patents granted on semiconductor processing and control electronics. Completed facility and semiconductor processing design, then completely equipped. Raised 2nd round funding for \$36 million. Established process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material.

#### **Director, Manufacturing & Wafer Fab Technology**

**2000 – 2001**

After 3rd round funding, led device manufacturing, creating wafer fab and assembly infrastructure; hired 70+ people, led production. Delivered first generation product for revenue to multiple customers. Converted pure technology to dominant company revenue with high yield.

Company purchased by Volcano Technologies, San Diego.

**Raytheon Corporation Lexington/Andover, MA**

**1985 - 1999**

**Manager, Semiconductor Operations**

**1996 – 1999**

Built and led a 300 employee, \$60 million revenue 24/7 semiconductor development and manufacturing operation resulting from the consolidation of a number of smaller organizations. Key player in technological development and recipient of Raytheon's 6 Sigma Leadership training. Decision maker in Texas Instrument group acquisition, providing significant expert opinion on semiconductor and design facilities. Obtained state-of-art yields using best available steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for steppers, deep reactive ion etching, plasma assisted CVD, and ion-implantation equipment, and disciplined design-for-manufacturing circuit design and layout methodology.

**Research Laboratory Manager**

**1992 – 1996**

Leader of a 90 employee development and contract research organization in high performance semiconductor devices and circuits, measurement, assembly and wafer fab. Led a team which invented and implemented a major revenue generating technology (\$.100 million) based on semiconductor device development (pseudomorphic high electron mobility transistor). Increased outside research funding by 50% in 3 years through superior technical performance relative to competitors.

**Section Manager, Semiconductors & ICs**

**1985 – 1992**

Led a MM-Wave Circuit and Module Development program over 2 years, leading to production win of a satellite terminal electronics generating \$320 million in sales. Developed processes for fabricating high power, high frequency multi-function integrated circuits, and combining high performance digital and analog devices in a single integrated circuit.

**Spire Corporation Bedford, MA**

**1981 – 1984**

**Staff Scientist  
Senior Staff Scientist**

Developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. Wrote joint papers with MIT professor, and had process adopted by equipment manufacturers. Built, operated and characterized ion-assisted deposition system for making coating for semiconductor and machine tool industries. Process eventually purchased by Kennametal, Inc.

**Publications**

**Restricted Publications & Reports**

**Process Sequence for Formation of Ultra-High Density Multi-Chip Modules:**

A high yield, low cost method for creating a system-in-a-package consisting of numerous semiconductor die, passive components, and sensors. Process formed basis for new (2008) facility.

**Design and Method of Fabrication of Ultra-High Density Radioisotope Power Source:**

In test, a miniature power source that achieves energy density more than 1000X the best chemical battery. Method uses planar semiconductor processing of bulk thermoelectric materials.

**Design and Method of Achieving Extremely Low Crystal Oscillator Phase Noise:**

Method developed for very low power refrigeration of quartz or sapphire crystal resonators, resulting in extremely low phase noise oscillators. The low phase noise allows extremely high sensitivity in digital receivers, including GPS receivers, leading to use in extremely low signal conditions.

**Design, Evaluation & Production of MEMS-based Fabry-Perot Interferometer:**

Design and method for ultra-compact spectral analyzer made using semiconductor and optical thin film processing.

**Design & Evaluation of Ultra-Fast Control Electronics for Integrated Optical Multiplexer:**

Design and performance evaluation of silicon-based integrated optical multiplexer using chip-based local heating

**Design and Fabrication of Q-band MILSTAR Communications Terminal Transmitter:**

Record power and efficiency 44 GHz transmitter design using new transistor design, and combined waveguide

**Key Publications (selected)**

**Process Characterization of PSG and BPSG Plasma Deposition**, J. Electrochem. Soc., Volume 131, Issue 9, pp. 2202-2203

**A double-recessed Al<sub>0.24</sub>GaAs/In<sub>0.16</sub>GaAs pseudomorphic HEMT for Ka- and Q-band power Applications**, Electron Device Letters, IEEE, Volume 14, Issue 9, pp. 456 - 458

**Formation of Thick Metal Structures on GaAs MMICs Using Image Reversal Lithography and Evaporated Metal Deposition**, J. Electrochem. Soc., Volume 136, Issue 9, pp. 2687-2690

**Contact Hole Etching in Load-Locked Hexagonal Reactive Ion Etch System**, J. Electrochem. Soc., Vol. 131, No. 8, 1984

**An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with Improved Breakdown Voltage for X and Ku-band power applications**, Microwave Theory and Techniques, IEEE Transactions on, Volume 41, Issue 5, May 1993, pp. 752 - 759

**Hot-electron-induced Degradation of Metal-Semiconductor Field-Effect Transistors**, Integrated Circuit Symposium, 1994. Technical Digest 1994., 16th Annual Volume , Issue , 16-19 Oct. 1994, pp. 259

**Ion Beam Deposition of Cubic Boron Nitride**, J. Vac. Sci. Technol. A Volume 1, Issue 2, pp. 323-325

**Patents****US Patent 6504235 - Passivation layer and process for semiconductor devices**

Method of coating semiconductor devices that prevented parametric shift in electrical performance. Solved key processing problem.

**US Patent 4440108 - Ion Beam Deposition Apparatus**

Design of equipment for deposition of thin films in the presence of ion bombardment. System produced thin films of interest for mechanical, electrical and optical properties and was sold as an equipment product.

**US Patent 6525880 - Integrated Tunable Fabry-Perot filter and Method of Making Same**

Design and method for fabricating very small, very high performance variable optical filter using semiconductor fabrication technology. In current use in fiber optical networks, chemical sensors, and 3-D medical imaging applications.

**US Patent 5175020 - Boron Nitride Films and Process of Making Same**

Ion assisted deposition of ultra-hard cubic boron nitride films for semiconductor and machine tool applications. Significant use in both areas.

**US Patent 4526673 - Coating Method**

Method for deposition of thin films used in semiconductor device fabrication. Method based on direct control of the kinetics of thin film deposition.

**US Patent 7727806 - Systems and Methods for High Density Multi-Component Modules**

Method for fabrication of electronic modules using multiple thinned integrated circuits, patterned multi-level interconnects, passive electronic components, and sensors

**US Patent Application 2009/TBD - Devices, systems, and methods for controlling the temperature of resonant elements**

Devices and systems for achieving low phase noise crystal oscillators using unique low power thermoelectric structures

**Expert Witness Experience:**

**See attachment**

**Contact information for Stanley Shanfield**

**STANLEY SHANFIELD**

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