

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC. AND SONY GROUP CORPORATION,
Petitioners

v.

SiOnyx LLC,
Patent Owner

Inter Partes Review Case No. IPR2025-00811
U.S. Patent No. 9,064,764

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,064,764**

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	LEVEL OF SKILL OF A POSITA.....	1
III.	REQUIREMENTS UNDER 37 C.F.R. §42.104	1
A.	GROUNDS FOR STANDING UNDER 37 C.F.R. §42.104(A)	1
B.	IDENTIFICATION OF CHALLENGE UNDER 37 C.F.R. §42.104(B)	2
C.	CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3).....	3
IV.	SHOWING OF ANALOGOUS, PRIOR ART	3
V.	GROUND 1: CLAIMS 1-5, 7 ARE OBVIOUS OVER HWANG-099, HWANG-795, KAES	4
A.	CLAIM 1	4
1.	1[Pre]	4
2.	1[a]	5
3.	1[a][i].....	7
4.	1[a][ii].....	9
5.	1[b]	12
6.	1[c]	13
	a) Hwang-099’s Teachings.....	13
	b) Motivation to Combine	16
7.	1[c][i].....	17
	a) Backside Light Trapping Material	17
	b) Peripheral Light Trapping Material	19
8.	1[c][ii].....	20
	a) Peripheral Light Trapping Material: Hwang-795’s Teachings	20
	b) Backside Light Trapping Material: Kaes’s Teachings	23
9.	1[d]	25
B.	CLAIM 2	27
C.	CLAIM 3	27
D.	CLAIM 4	27
E.	CLAIM 5	28
F.	CLAIM 7	29
VI.	GROUND 2: CLAIM 6 IS OBVIOUS OVER HWANG-099, HWANG-795, KAES, KONNO	30

A.	KONNO’S TEACHINGS	30
B.	MOTIVATION TO COMBINE.....	31
VII.	GROUND 3: CLAIMS 8-12, 14-15 ARE OBVIOUS OVER HWANG-099	32
A.	CLAIM 8.....	32
1.	8[d].....	32
B.	CLAIM 9.....	32
C.	CLAIM 10.....	33
D.	CLAIM 11.....	33
E.	CLAIM 12.....	33
F.	CLAIM 14.....	33
G.	CLAIM 15.....	33
VIII.	GROUND 4: CLAIM 13 IS OBVIOUS OVER HWANG-099 AND KOMURO.....	33
A.	HWANG-099’S TEACHINGS	33
B.	KOMURO’S TEACHINGS.....	34
C.	MOTIVATION TO COMBINE.....	34
IX.	GROUND 5: CLAIMS 17-19 ARE OBVIOUS OVER HWANG- 099 IN COMBINATION WITH MOULI AND/OR NOZAKI.....	35
A.	CLAIM 17.....	35
1.	17[c]/[i].....	35
a)	Mouli’s Sloped Trench Wall.....	35
b)	Nozaki’s Sloped Backside Surface	37
c)	Obviousness of Combining Both Mouli and Nozaki	39
B.	CLAIM 18.....	39
C.	CLAIM 19.....	39
X.	GROUND 6: CLAIM 20 IS OBVIOUS OVER HWANG-099 IN COMBINATION WITH MOULI AND/OR NOZAKI AND FURTHER IN VIEW OF KONNO.....	40
A.	CLAIM 20.....	40
1.	Konno’s Teachings	40
2.	Motivation to Combine.....	40
XI.	GROUND 7: CLAIMS 16, 21-24 ARE OBVIOUS OVER HWANG-099 IN COMBINATION WITH KONNO	40
A.	CLAIM 16.....	40

1.	<i>Konno's Teachings</i>	40
2.	<i>Motivation to Combine</i>	40
B.	CLAIM 21	41
1.	21[d]	41
	a) Konno's Teachings.....	41
	b) Motivation to Combine	44
C.	CLAIM 21	45
1.	<i>Explanation of Combination and Motivation for the Combination</i>	45
2.	21[b]	47
	a) Hwang-099's Teachings.....	47
	b) Konno's Teachings.....	48
	c) Motivation to Combine	49
3.	21[d]	49
	a) Konno's Teachings.....	49
	b) Motivation to Combine	50
4.	21[d][i]	50
	a) Hwang-099's Teachings.....	50
	b) Konno's Teachings.....	50
D.	CLAIM 22	51
E.	CLAIM 23	51
F.	CLAIM 24	51
G.	CLAIM 25	51

XII. GROUND 8: CLAIMS 1-5, 7 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584, KAES, HWANG-795 52

A.	CLAIM 1	52
1.	1[Pre]	52
2.	1[a]	53
3.	1[a][i]	54
4.	1[a][ii]	55
	a) Hong's Teachings.....	56
	b) Yamashita's Teachings	57
	c) Motivation to Combine	58
5.	1[b]	59
6.	1[c]	61
	a) Hwang-584's Teachings.....	61
	b) Motivation to Combine	65
7.	1[c][i]	66
	a) Hong's Backside Light Trapping Material	66

8.	b)	Hwang-584's Peripheral Light Trapping Material.....	69
	1[c][ii]		70
	a)	Peripheral Light Trapping Material: Hwang-795's Teachings	70
	b)	Backside Light Trapping Material: Kaes's Teachings	71
9.	1[d]		72
	a)	Hong's Backside Light Trapping Material	72
	b)	Hwang-584's Peripheral Light Trapping Material.....	72
B.		CLAIM 2	73
C.		CLAIM 3	73
D.		CLAIM 4	73
E.		CLAIM 5	74
	1.	<i>Hong's and Yamashita's Teachings</i>	74
	2.	<i>Motivation to Combine</i>	76
F.		CLAIM 7	78
XIII. GROUND 9: CLAIM 5 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, HWANG-795, KAES, MOULI			78
A.		HONG'S AND MOULI'S TEACHINGS	78
B.		MOTIVATION TO COMBINE.....	80
XIV. GROUND 10: CLAIM 6 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, HWANG-795, KAES, KONNO			82
A.		KONNO'S TEACHINGS	82
B.		MOTIVATION TO COMBINE.....	82
XV. GROUND 11: CLAIMS 8-12, 14-15 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584			83
A.		CLAIM 8	83
	1.	8[d]	83
B.		CLAIM 9	83
C.		CLAIM 10	83
D.		CLAIM 11	84
E.		CLAIM 12	84
F.		CLAIM 14	84
G.		CLAIM 15	84
XVI. GROUND 12: CLAIM 13 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, KOMURO.....			84
A.		KOMURO'S TEACHINGS.....	84

B.	MOTIVATION TO COMBINE.....	85
XVII.	GROUND 13: CLAIMS 17-19 ARE OBVIOUS OVER HONG, YAMASHITA, AND HWANG-584 IN COMBINATION WITH MOULI AND/OR NOZAKI.....	86
A.	CLAIM 17	86
1.	<i>17[c][i]</i>	86
a)	Hong’s Sloped Trench Wall.....	86
b)	Mouli’s Sloped Trench Wall.....	87
c)	Nozaki’s Sloped Backside Surface	88
d)	Obviousness of Combining Both Mouli and Nozaki	88
B.	CLAIM 18	89
C.	CLAIM 19	89
XVIII.	GROUND 14: CLAIM 20 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, MOULI AND/OR NOZAKI IN FURTHER VIEW OF KONNO	89
A.	KONNO’S TEACHINGS	89
B.	MOTIVATION TO COMBINE.....	89
XIX.	GROUND 15: CLAIMS 16, 21-25 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584, KONNO	90
A.	CLAIM 16	90
1.	<i>Konno’s Teachings</i>	90
2.	<i>Motivation to Combine</i>	90
B.	CLAIM 21	90
1.	<i>21[d]</i>	90
a)	Konno’s Teachings.....	90
b)	Motivation to Combine	91
C.	CLAIM 21	92
1.	<i>Explanation of Combination and Motivation for the Combination</i>	92
2.	<i>21[b]</i>	94
a)	Hong’s Teachings.....	94
b)	Konno’s Teachings.....	94
c)	Motivation to Combine	94
3.	<i>21[d]</i>	94
a)	Konno’s Teachings.....	94
b)	Motivation to Combine	94
4.	<i>21[d][i]</i>	95

a)	Hong’s Teachings.....	95
b)	Konno’s Teachings.....	95
D.	CLAIM 22	95
E.	CLAIM 23	96
F.	CLAIM 24	96
G.	CLAIM 25	96
XX.	DISCRETIONARY DENIAL	96
A.	GENERAL PLASTIC	96
B.	ADVANCED BIONICS	98
C.	FINTIV.....	99
XXI.	CONCLUSION.....	99
XXII.	MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)	101
A.	REAL PARTIES-IN-INTEREST	101
B.	RELATED MATTERS	101
1.	<i>District Court Litigation Matters</i>	<i>101</i>
2.	<i>ITC Matters</i>	<i>101</i>
3.	<i>IPR Matters</i>	<i>102</i>
C.	LEAD AND BACK-UP COUNSEL	102
D.	37 C.F.R. § 42.8(B)(4) – SERVICE INFORMATION	103

TABLE OF AUTHORITIES

REGULATIONS

37 C.F.R. § 42.104(b)(3)	3
37 C.F.R. § 42.8(b)(4)	104
37 C.F.R. §§ 42.6(e)	115
37 C.F.R. §42.104(a)	1
37 C.F.R. §42.104(b).....	2
37 C.F.R. §42.24	113

I. INTRODUCTION

IPR is requested of Claims 1-25 of USPN 9,064,764. The '764 Patent utilizes reflective layers of differing refractive indexes to reflect incident light on an image sensor back towards the image sensor's pixel. '764 Patent (Ex. 1001), 1:36–2:8. Such “sandwich” techniques for effecting desired light reflection were well-known, including use of Bragg reflectors. *Dec.*, ¶¶36-37, ¶66.¹

This Petition presents two distinct sets of grounds of unpatentability based on Hwang-099 (Grounds 1-7) and Hong (Grounds 8-15). Independent Claim 8 is obvious in view of Hwang-099 alone.

II. LEVEL OF SKILL OF A POSITA

For purposes of this IPR, Petitioners apply SiOnyx's POSITA level of skill, namely having “at least a bachelor's degree in electrical engineering, materials science, or physics (or an equivalent degree), at least two years of experience in optoelectronics, and at least three years of work experience in semiconductor manufacturing....[A] master's degree or Ph.D. in a relevant field may substitute for some work experience or vice versa.” (Ex. 1014, 18).

III. REQUIREMENTS UNDER 37 C.F.R. §42.104

A. Grounds for Standing Under 37 C.F.R. §42.104(a)

Petitioners certify the '764 Patent is eligible for IPR.

¹ Citations to *Dec.* are to Ex. 1003, Declaration of Dr. Stanley Shanfield.

B. Identification of Challenge Under 37 C.F.R. §42.104(b)

Petitioners request the Challenged Claims be found unpatentable on the following grounds.²

Ground	Grounds of Unpatentability
1	Claims 1-5, 7 are obvious over Hwang-099 (Ex. 1004), Hwang-795 (Ex. 1006), and Kaes (Ex. 1066)
2	Claim 6 is obvious over Hwang-099, Hwang-795, Kaes, and Konno (Ex. 1008)
3	Claims 8-12, 14-15 are obvious over Hwang-099
4	Claim 13 is obvious over Hwang-099 and Komuro (Ex. 1005)
5	Claims 17-19 are obvious over Hwang-099 in combination with Mouli (Ex. 1010) and/or Nozaki (Ex. 1011)
6	Claim 20 is obvious over Hwang-099 and Konno in combination with Mouli and/or Nozaki
7	Claims 16, 21-25 are obvious over Hwang-099 in combination with Konno
8	Claims 1-5, 7 are obvious over Hong (Ex. 1012), Yamashita (Ex. 1007), Hwang-584 (Ex. 1013), Hwang-795, and Kaes
9	Claim 5 is obvious over Hong, Yamashita, Hwang-584, Hwang-795, Kaes, and Mouli
10	Claim 6 is obvious over Hong, Yamashita, Hwang-584, Hwang-795, Keas, and Konno
11	Claims 8-12, 14-15 are obvious over Hong, Yamashita, and Hwang-584
12	Claim 13 is obvious over Hong, Yamashita, Hwang-584, and Komuro
13	Claims 17-19 are obvious over Hong, Yamashita, and Hwang-584 in combination with Mouli and/or Nozaki
14	Claim 20 is obvious over Hong, Yamashita, Hwang-584, and Konno in combination with Mouli and/or Nozaki
15	Claims 16, 21-25 are obvious over Hong, Yamashita, Hwang-584, and Konno

² All references qualify as prior art under §102(b).

C. Claim Construction Under 37 C.F.R. § 42.104(b)(3)

Petitioners do not believe claim construction is necessary to apply the claims to the present prior art.³

The '764 Patent is the subject of an ITC action involving SiOnyx and Samsung. §XXII.B.2. The ITC issued an Order construing certain claim terms. (Ex. 1014).

IV. SHOWING OF ANALOGOUS, PRIOR ART

The prior art is analogous to the claimed invention of the '764 Patent. The prior art is from the same field of endeavor of the '764 Patent, namely semiconductor devices for detecting light. *'764 Patent*, 5:64–6:2, 6:13-15, 5:64–6:36, 7:47-49; *Hwang-099*, 1:14-19, 1:52-57, 9:11-14, 10:23-27, 10:31-35, 15:38-41, Figures 1-2; *Hwang-795*, [0009], [0016]; *Kaes*, Abstract, [0007], [0008], [0013], [0016]-[0018]; *Konno*, 1:15-22, 2:56-58, 3:44-50; *Hong*, [0001], [0006], [0017], [0047]; *Mouli*, 1:6-9, 1:43-46, 3:45-48; *Hwang-584*, [0002], [0009]; *Yamashita*, [0003], [0047], [0049], [0053]; *Nozaki*, Abstract, [0033], [0036], Figure 2; *Komuro*, Abstract, [0012], [0087], [0133]; *Dec.*, ¶29, ¶86, ¶91, ¶95, ¶99, ¶103, ¶107, ¶111, ¶116, ¶122, ¶129.

³ Petitioners' application of prior art to the Challenged Claims is not a waiver of any argument in litigation regarding a claim term's construction or indefiniteness.

The prior art is also reasonably pertinent to at least one problem facing the '764 Patent's inventors, namely the problem of reducing electrical and/or optical cross-talk between adjacent sensor pixels and/or reducing loss of light. '764 Patent, 1:18-35, 5:64–6:13; *Hwang-099*, 1:55-58, 10:19-27; *Hwang-795*, Abstract, [0016]; *Kaes*, [0007], [0008], [0015], [0017], [0018]; *Konno*, 5:24-25, 4:15-16, 6:2-3; *Hong*, [0001], [0026]; *Mouli*, 1:55-59, 2:49-53, 4:27-32, 6:29-33; *Hwang-584*, Abstract, [0002], [0009], [0011], [0021]; *Yamashita*, [0007], [0011], [0091]-[0093], [0115], Figures 4-6; *Nozaki*, [0018]; *Komuro*, Abstract, [0011], [0090]; *Dec.*, ¶31, ¶87, ¶92, ¶96, ¶100, ¶104, ¶108, ¶112, ¶117, ¶123, ¶130.

V. GROUND 1: CLAIMS 1-5, 7 ARE OBVIOUS OVER HWANG-099, HWANG-795, KAES

A. Claim 1

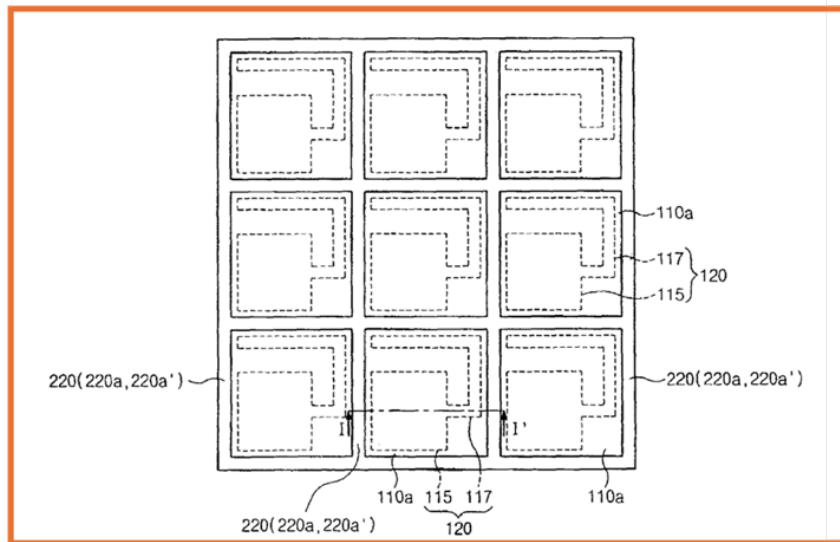
1. 1[Pre]

Hwang-099 teaches or suggests a *light trapping device*⁴, namely the image sensor shown in Figure 1:

⁴ Claim language provided in italics. All drawing annotations added. Claim language in colored font maps to same-colored regions in the annotated drawings. Citations to a claim limitation and/or section number are to the limitation's mapping in this Petition and are incorporated by reference, including the Motivations to Combine (MTC) and showing of reasonable expectation of success (REOS) provided in the

Light Trapping Device

Fig. 1



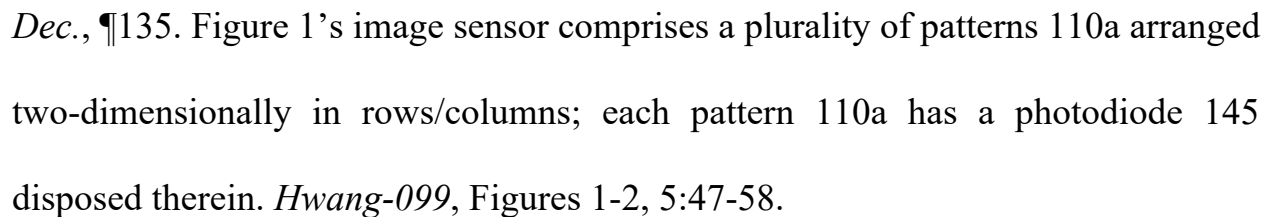
Dec., ¶132.

Hwang-099's image sensor is *light trapping* because it “minimiz[es] interference between neighboring pixels...” and/or is surrounded by sidewall multi-layered reflection layer 220 reflecting light back into the pixel. *Hwang-099*, 5:47-55, 1:55-58, 3:20-26, 10:19-35; cf. '764 Patent, 11:3-5; Dec., ¶¶133-134.

2. *1[a]*

Hwang-099 teaches or suggests *at least one light sensitive pixel*, namely at least the portion comprising pixel semiconductor pattern 110a and photodiode 145 formed therein, shown in Figures 1-2:

cross-referenced section. All REOS include the benefits described for the respective MTC. All emphases added unless otherwise noted.



6

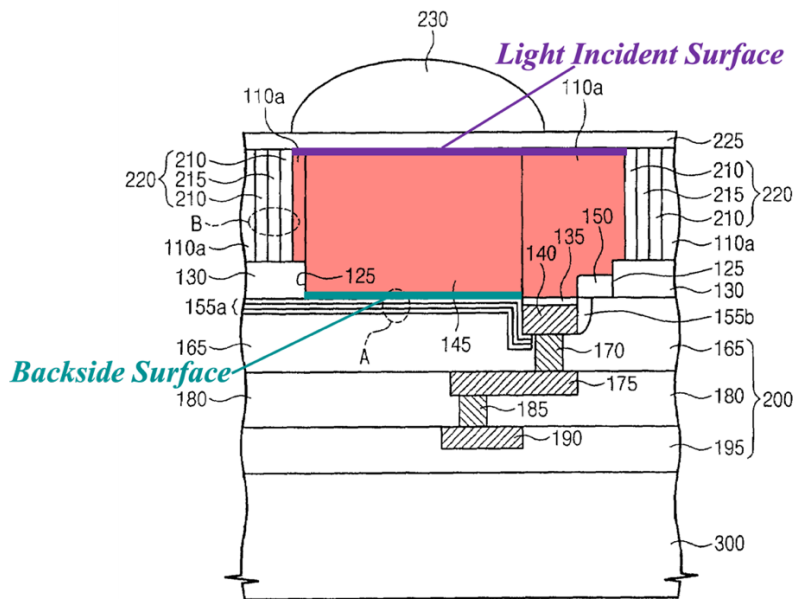
Hwang-099, 6:3-4. A PN junction facilitates converting light into an electrical signal by separating electron-hole pairs. *Dec.*, ¶¶42-47, 136-141. Because both semiconductor pattern 110a and photodiode 145 collectively form the PN junction, both pattern 110a and photodiode 145 are elements of an image sensor that convert light into an electrical signal. *Id.*

Additionally or alternatively, pattern 110a satisfies the claimed *pixel* because *Hwang-099*'s image sensor comprises the “plurality of pixel semiconductor patterns 110a [] arranged two-dimensionally in rows and columns on a substrate 300[,]” where “neighboring pixels” are “separated by” sidewall reflection layer 220. *Hwang-099*, 5:52-57, 6:7-23, 9:41-48, 10:10-14. Therefore, pattern 110a is a *pixel* because patterns 110a form the “neighboring pixels” separated by sidewall layer 220. *Dec.*, ¶142.

3. *1[a]/i/*

Hwang-099's *pixel* includes a *light incident surface* and a *backside surface*, namely portions of respective second and first surfaces of pattern 110a and photodiode 145 (collectively, the *pixel*):

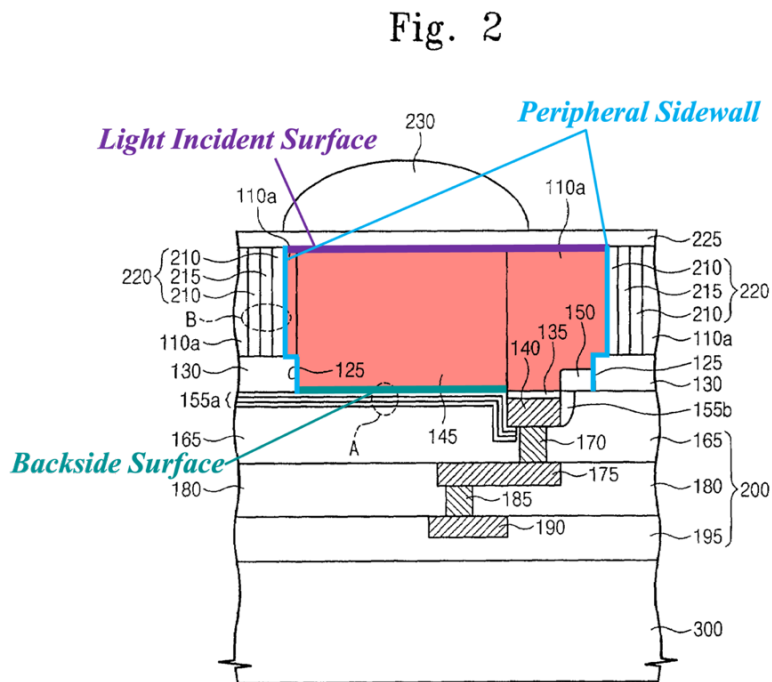
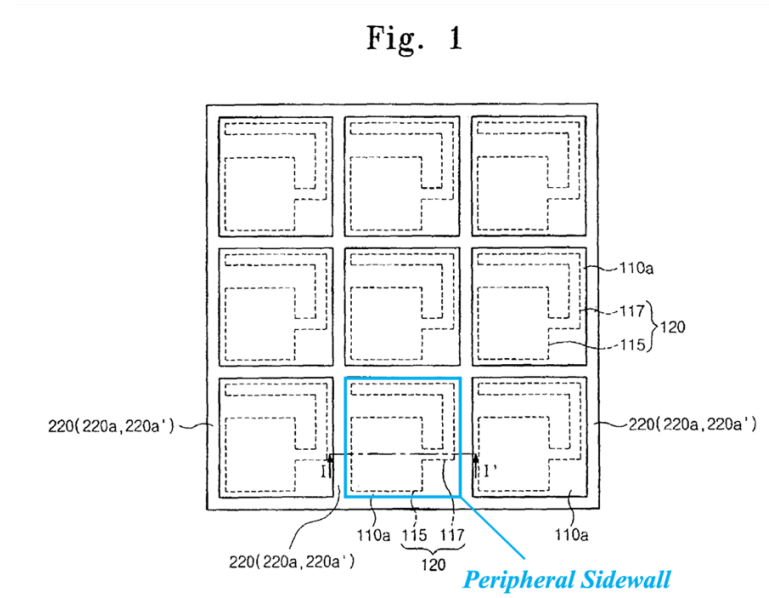
Fig. 2



Dec., ¶143; Claim 1[a], §V.A.2. Pattern 110a and photodiode 145, which is “disposed” within pattern 110a, “have first and second surfaces in parallel, i.e., that face one another.” *Hwang-099*, 5:57-58, 6:37-38, 6:61-65. In Figure 2, above, at least the portion of the first surface of 110a/145 as annotated is a bottom surface (*backside surface*) because it “is more proximate to the substrate 300[,]” and at least the portion of the second surface of 110a/145 as annotated is a top surface (*light incident surface*) because it receives incident light. *Hwang-099*, 6:38-40, 8:20-22, 9:6-7, 1:14-18; Dec., ¶144. Because the top/second and bottom/first surfaces of pattern 110a “face one another” and are “parallel,” the surfaces are *opposite*. *Hwang-099*, 6:37-38; Dec., ¶145.

4. 1[a][ii]

Hwang-099 teaches or suggests a *peripheral sidewall*, namely a sidewall of a trench formed in pattern 110a:



Dec., ¶¶146-148.

Hwang-099 teaches forming a trench in pattern 110a, where the sidewall of the trench formed in pattern 110a is a *peripheral sidewall*. Cf. '764 Patent, 10:64-65; Ex. 1014, 20 (providing ITC's construction of agreed-upon terms, including "sidewall" as "Plain and ordinary meaning. To the extent a construction is required: trench wall"). Hwang-099, Figures 18-19 describe a method of forming the Figure 2 image sensor. *Hwang-099*, 13:64–14:22; *Dec.*, ¶¶80-83, 147. "[S]emiconductor layer 110 is patterned to form a trench 125[,]” and then “the floor of the trench 125 is selectively etched to form a plurality of grooves 205” that “encloses one pixel semiconductor pattern 110a in layers.” *Hwang-099*, 14:3-12. Thus, pattern 110a material is removed from semiconductor layer/pattern 110a to form a sidewall via etching trench 125 and grooves 205:

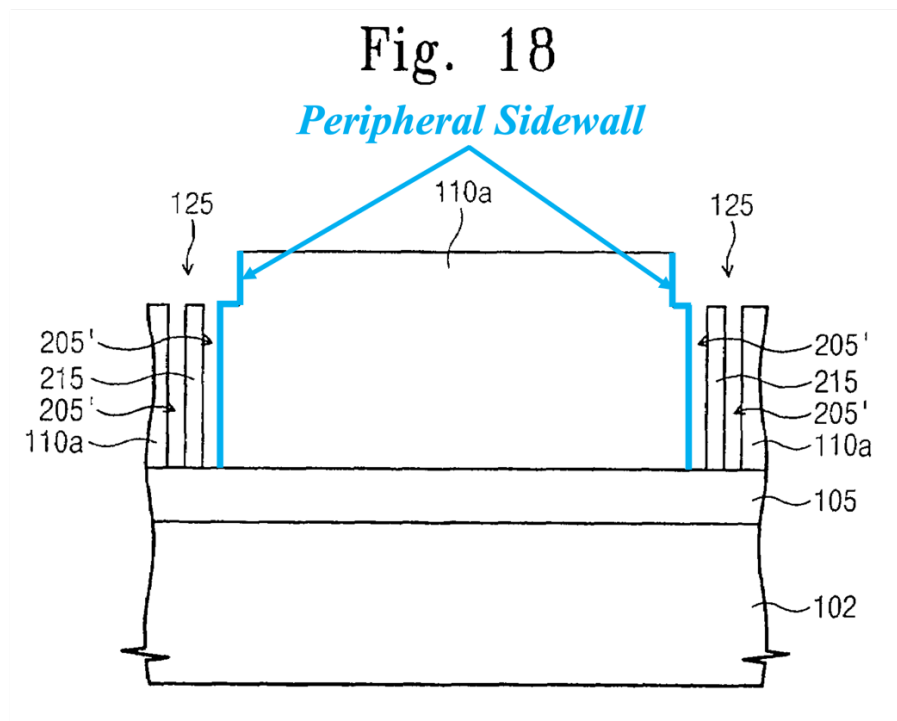
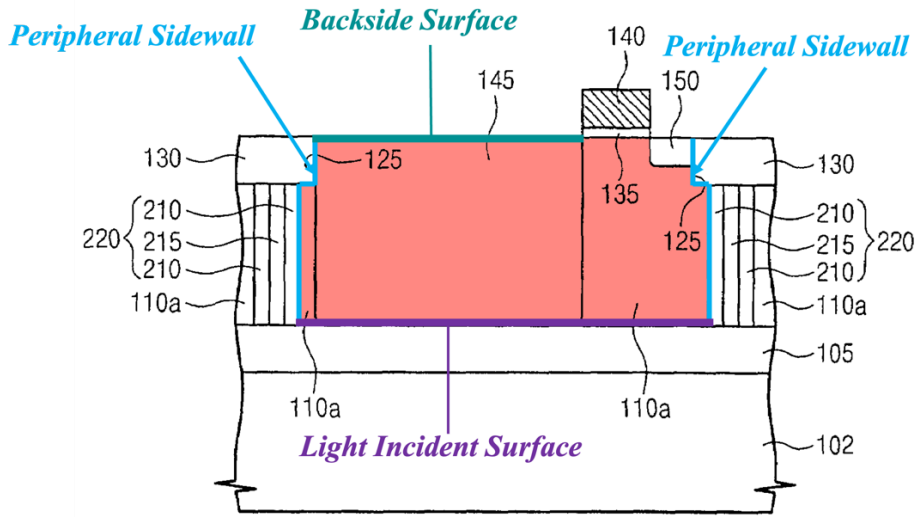


Fig. 19

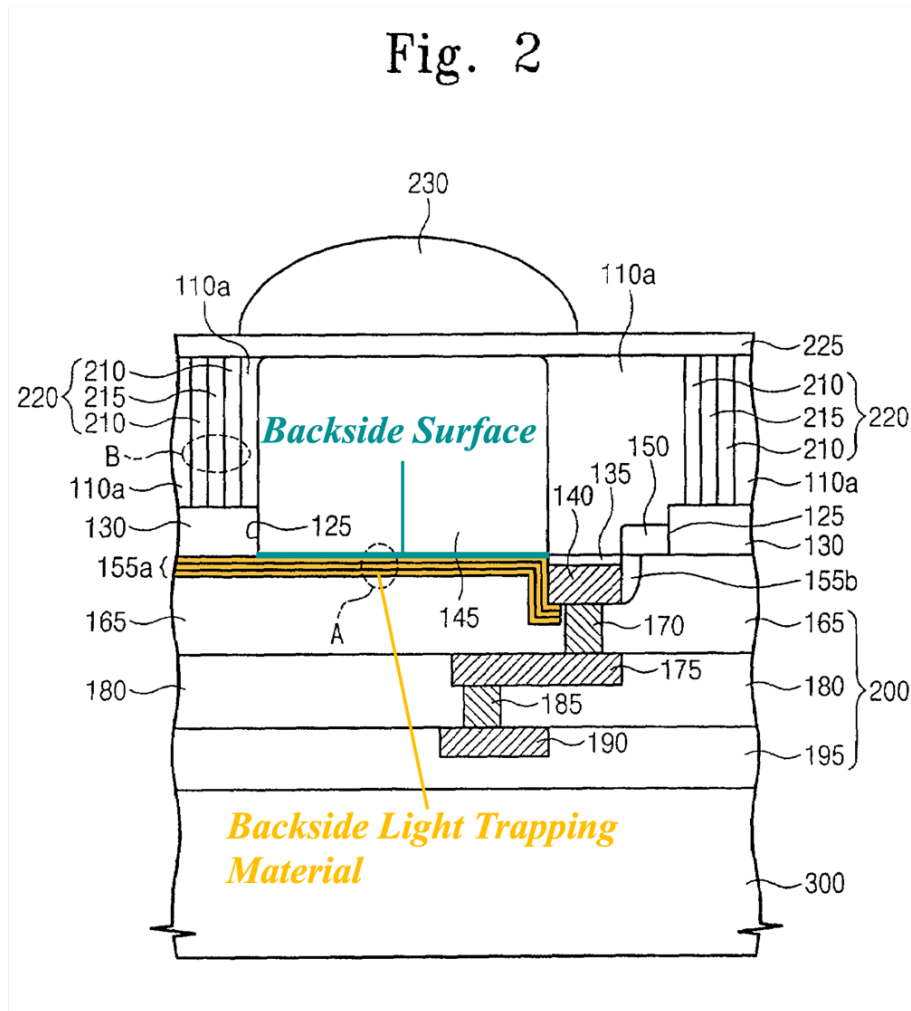


Dec., ¶¶148-150.

Hwang-099’s “sidewall of the pixel semiconductor pattern 110a” is *disposed into at least a portion of the pixel* because the semiconductor layer/pattern 110a (part of **pixel** (§V.A.2)) is etched to form trench 125 and grooves 205. *Hwang-099*, 14:20-22, 5:52-57; *Dec.*, ¶151. Hwang-099’s pattern 110a sidewall *extend[s] at least substantially around the pixel periphery* because grooves 205 “**surround**[] the pixel semiconductor patterns 110a” and are “formed between a pair of neighboring pixel semiconductor patterns 110a[,]” per Figure 1. *Hwang-099*, 12:42-53, 3:60-67; *Dec.*, ¶152. Additionally, in Figure 1’s plan view, the sidewall of pattern 110a (**peripheral sidewall**) extends completely around the pixel periphery because there are no gaps in the sidewall as it surrounds the pixel periphery. *Dec.*, ¶153.

5. 1[b]

Hwang-099 teaches or suggests a *backside light trapping material*, namely base multi-layered reflection layer 155a, “contact[ing] the first surface of the pixel semiconductor pattern 110a” (*backside surface*):



Dec., ¶157; Hwang-099, 7:45-47; Claim 1[a][i], §V.A.3.

Layer 155a “includes at least two stacked layers having different refractive indexes[,]” such as “first base multi layered reflection layer 151 and a second base multi-layered reflection layer 152.” Hwang-099, 8:32-44; Dec., ¶¶154-156. Because

layer 155a extends across the entire portion of the *backside surface* in Figure 2, layer 155a (*backside light trapping material*) is *substantially covering the backside surface*. Dec., ¶¶157-158.

Layer 155a is *light trapping* because “external light incident on the second surface of the photodiode 145 is reflected by” a “boundary surface” in layer 155a to be “incident again on the photodiode 145.” *Hwang-099*, 9:6-11; Dec., ¶¶154-156.

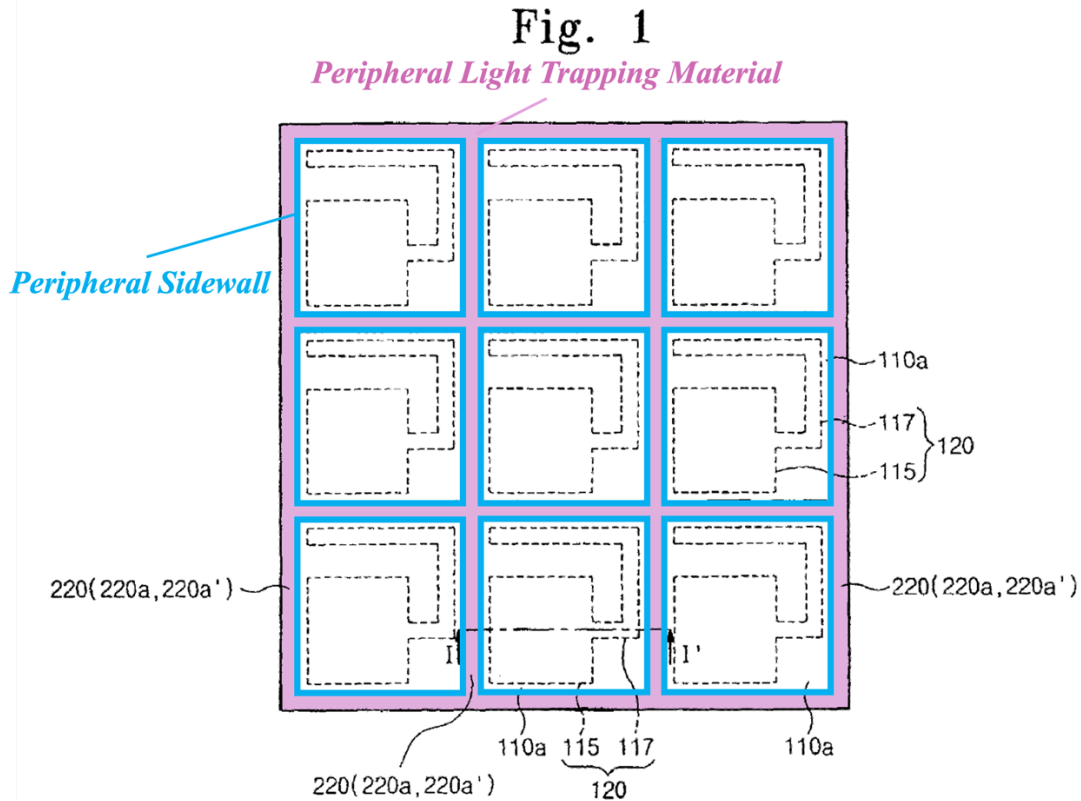
6. 1[c]

Claim 1[c]’s mapping modifies Hwang-099’s Figure 2 embodiment with Hwang-099’s Figure 6 embodiment, namely layer 220 extending into device isolation pattern 130. The *peripheral light trapping material* is met by Hwang-099’s layer 220 modified per Figure 6 to *substantially cover[] the peripheral sidewall*, where the collective layer 220 and modified pattern 130 meet Claim 1[c].

a) Hwang-099’s Teachings

Hwang-099 teaches a “[s]idewall multi-layered reflection layer 220 [that] encloses the side walls of the pixel semiconductor patterns 110a.” *Hwang-099*, 6:15-23 (further disclosing layer 220 separating patterns 110a and “disposed along the boundaries” of the patterns), 6:32-36, 3:63-67, Figure 1.

Because layer 220 “encloses” pattern 110a’s *sidewall*, a POSITA would have understood layer 220 is *peripheral*:

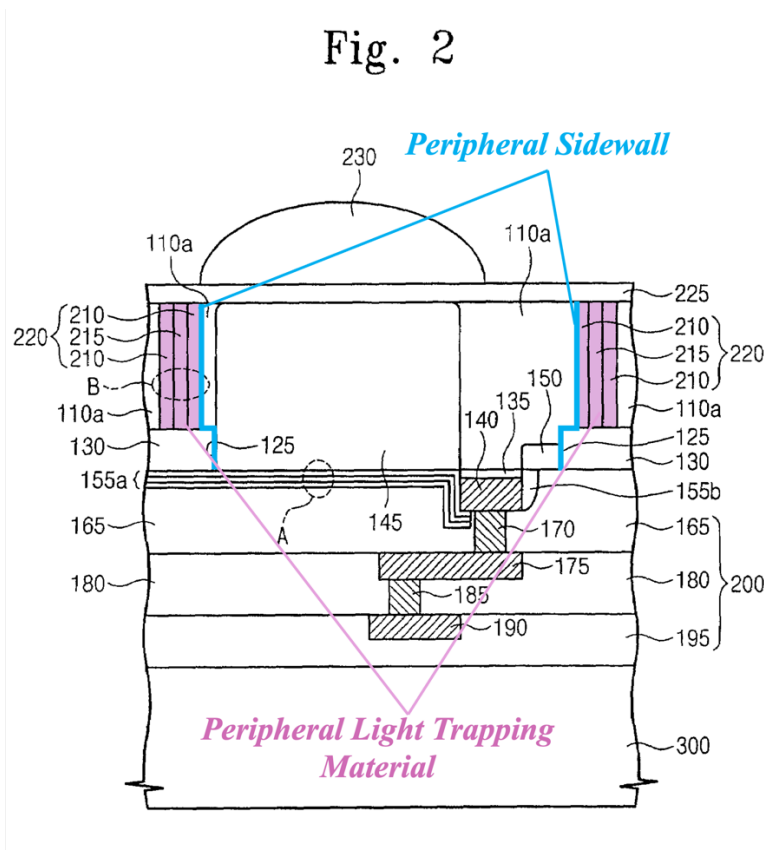


Dec., ¶¶162-163.

Reflection layer 220 “includes layers with different respective refractive indexes.” *Hwang-099*, 9:52-53. Layer 220 “includes a first sidewall reflection layer 210 and a second sidewall reflection layer 215” where “[t]he refractive index of the first sidewall reflection layer 210 is different from the refractive indexes of the pixel semiconductor pattern 110a and the second sidewall reflection layer 215.” *Hwang-099*, 9:58-63. Layer 220 is *light trapping* because “the portion of the light reflected toward the sidewall multi-layered reflection layer 220 from the light reflected by the first and second boundary surfaces is incident again on the photodiode 145 so that

absorption efficiency of external light is increased.” *Hwang-099*, 10:31-35; *Dec.*, ¶¶160-163.

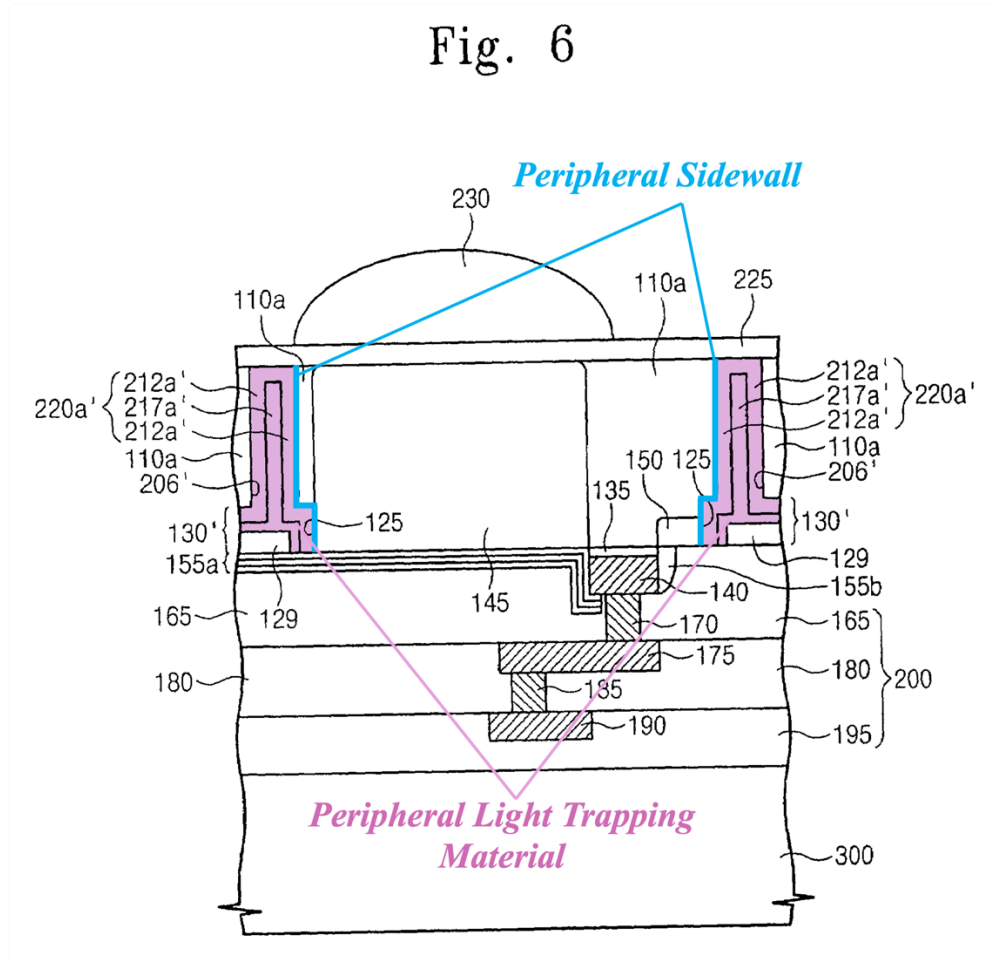
In the Figure 2 embodiment, below, layer 220 is a *peripheral light trapping material* covering part of pattern 110a’s sidewall (*peripheral sidewall*), while element 130 covers the remaining portion of the sidewall:



Dec., ¶¶163-164.

In the Figure 6 embodiment, *Hwang-099* teaches device isolation pattern 130' “include[s] **extended portions of the first and second sidewall reflection layers 212a' and 217a'.**” *Hwang-099*, 12:26-28, Figure 6. The first and second sidewall

reflection layers extend through the isolation pattern 130' to 155a, where the *sidewall* is *substantially cover[ed]* by *peripheral light trapping material* 220a':



Dec., ¶165.

b) Motivation to Combine

A POSITA would have found obvious and been motivated to modify Figure 2's pattern 130 such that first and second layers 210, 215 of layer 220 extend through pattern 130 to *substantially* and completely cover pattern 110a's sidewall, per Figure 6. Dec., ¶166. The modification would have given device isolation pattern 130 the same *light trapping* ability as layer 220 due to the difference in refractive indexes

between layers 210, 215. *Dec.*, ¶167. A POSITA would have understood increasing the surface area of the light-trapping material on the peripheral sidewall would predictably increase the amount of light reflected into the pixel, thereby providing the benefit of increased photons returned to the photodiode. *Dec.*, ¶168. There would have been a REOS at least because Hwang-099 provides methods for manufacturing an isolation pattern 130' having first and second sidewall reflection layers. *Hwang-099*, 14:3-22, 12:35–13:3; *Dec.*, ¶169.

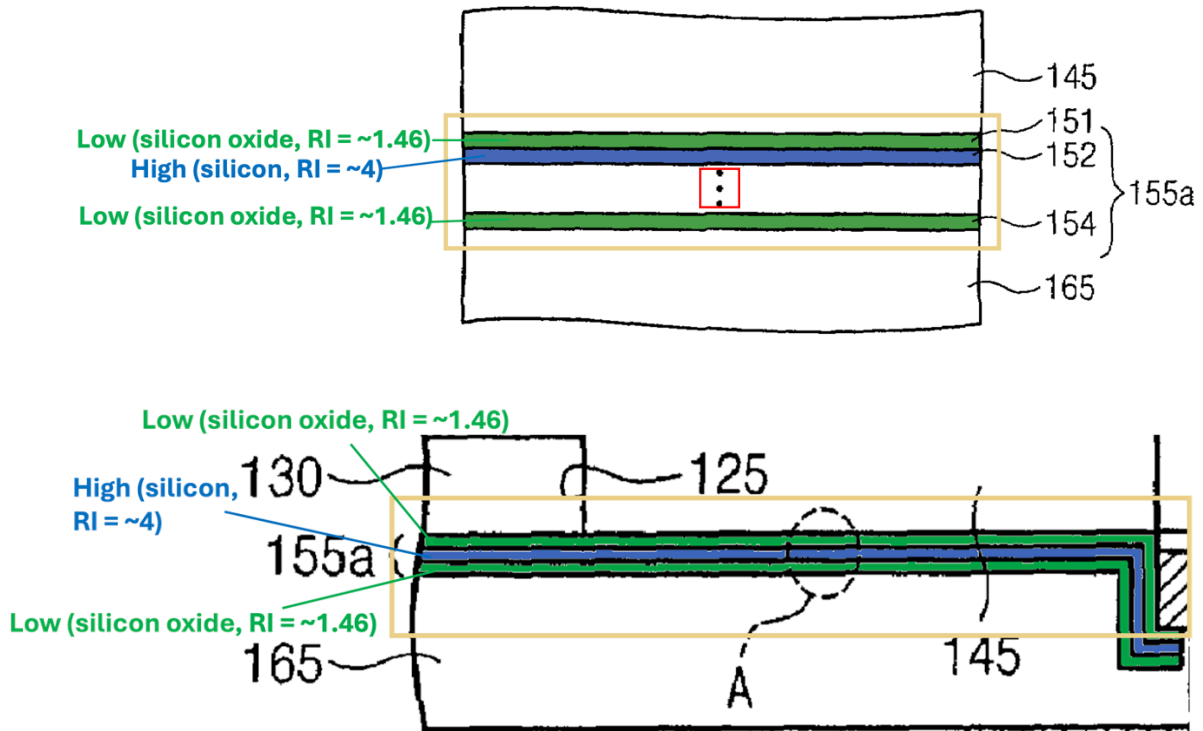
7. *1[c][i]*

a) **Backside Light Trapping Material**

Hwang-099's layer 155a (*backside light trapping material*) includes a *high refractive index material* sandwiched between *two low refractive index materials* (hereinafter "low-high-low sandwich"). *Dec.*, ¶170. Layer 155a includes "a first base multi-layered reflection layer 151 and a second base multi-layered reflection layer 152" having different refractive indexes. *Hwang-099*, 8:40-44. Layer 155a further includes layer 154 contacting the "interlayer insulating layer 200." *Hwang-099*, 8:57-58, Figure 3. Hwang-099 teaches stacking layers 151, 152 three times (indicated with red box, below). *Hwang-099*, 9:25-26. "[T]he first and second base multi-layered reflection layers 151 and 152 [are] respectively formed of silicon oxide (with a refractive index of approximately 1.46) and silicon (with a refractive

index of approximately 4)[.]” *Hwang-099*, 9:25-34. Therefore, layer 152 has a higher refractive index than layer 151. *Dec.*, ¶171.

Fig. 3



Dec., ¶¶172-174.

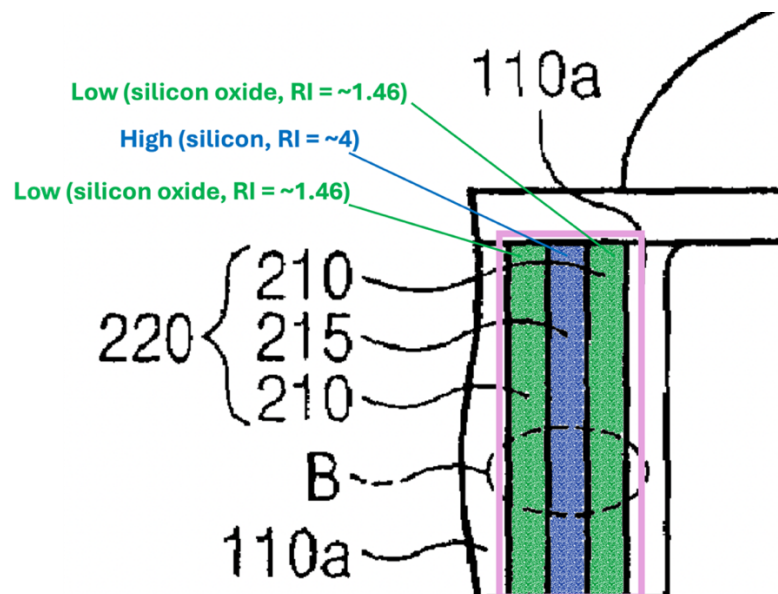
Because layers 151/152 may be stacked three times, the stacked layers satisfy Claim 1[c][i]’s recited low-high-low sandwich. *Dec.*, ¶173. Because “layer 154” may be the “first base multi-layered reflection layer 151 or the second base multi-layered reflection layer 152[.]” when there are 3 layers total, the layer 155 (*backside light trapping material*) stacked with layers 151/152 also satisfies Claim 1[c][i].

Hwang-099, 8:57-60; *Dec.*, ¶¶173-174.

b) Peripheral Light Trapping Material

Layer 220 (*peripheral light trapping material*) also satisfies Claim 1[c][i]’s low-high-low sandwich. *Dec.*, ¶¶175-179.

Hwang-099 teaches layer 220 “having a second sidewall reflection layer 215 interposed between two first sidewall reflection layers 210[,]” where layers 210, 215 are “respectively formed of a silicon oxide layer and a silicon layer[.]” *Hwang-099*, 10:48-55. Layer 210’s refractive index is lower than layer 215’s refractive index, thus forming Claim 1[c][i]’s low-high-low sandwich comprising layers 210/215/210. *Hwang-099*, 9:58-66.

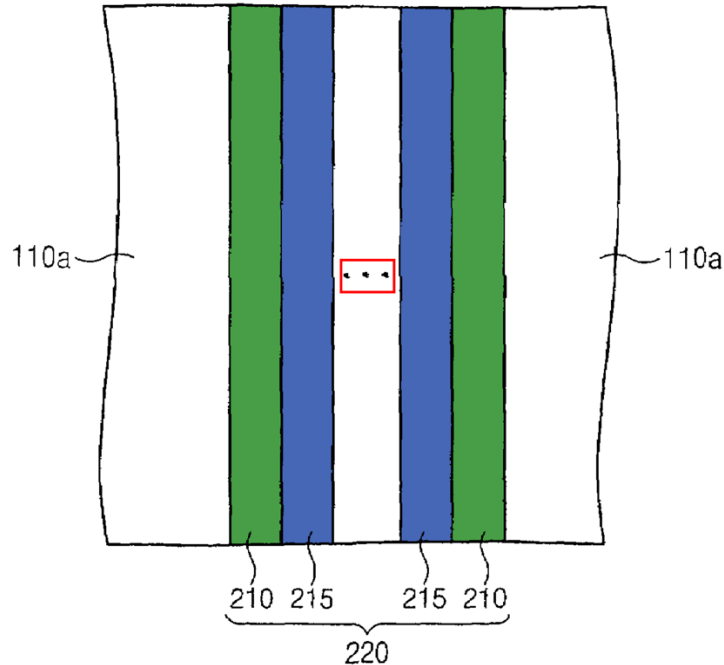


Dec., ¶176.

Layers 210/215 may be “stacked in an alternating manner a plurality of times[,]” and “both the layers of the sidewall multi-layered reflection layer 220

contacting the pair of neighboring pixel semiconductor patterns 110 can be the first sidewall reflection layer 210.” *Hwang-099*, 10:6-17.

Fig. 4



Dec., ¶177.

8. 1[c][ii]

The Claim 1[c][ii] mapping maps the low refractive index material for both the *peripheral light trapping material* and the *backside light trapping material*.

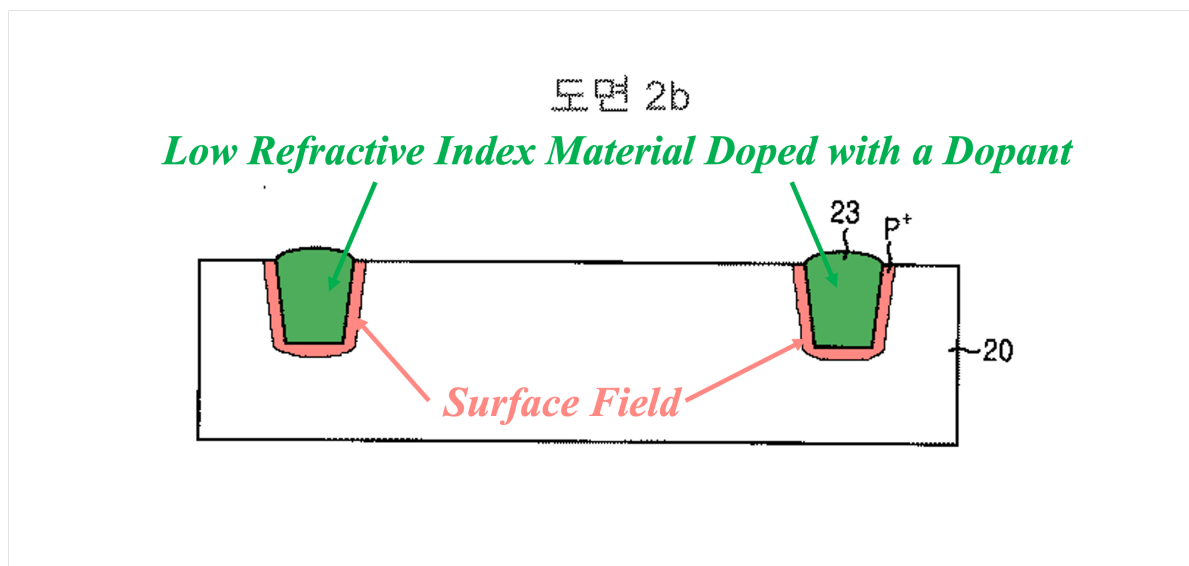
a) Peripheral Light Trapping Material: Hwang-795’s Teachings

Hwang-099 combined with Hwang-795 renders obvious Claim 1[c][ii] and specifically, doping the low refractive index material for the *peripheral light trapping*

material. Hwang-795 teaches borosilicate glass (BSG), which is silicon dioxide doped with boron. *Dec.*, ¶181.

Hwang-795 teaches an “image sensor that can prevent crosstalk[.]” *Hwang-795*, Abstract. A trench is formed in a “semiconductor layer” through “etching.” *Hwang-795*, [0017]. A “substance doped with P-type impurity, for example BSG (borosilicate glass), or the like, is deposited, thereby burying the trench.” *Hwang-795*, [0027]. *Dec.*, ¶181.

A POSITA would have understood Hwang-099’s silicon oxide is silicon dioxide (low refractive index material) based on the refractive index of 1.46 listed by Hwang-099. *Dec.*, ¶¶84, 184; Claim 1[c][i], §V.A.7. In the combination, Hwang-099’s silicon dioxide is doped with boron (*is doped with a dopant*), per Hwang-795’s BSG deposited in trench. *Dec.*, ¶184.



Dec., ¶181.

After the trench is filled with BSG, a “simple heat process is carried out, thereby diffusing the doped P-type impurity inside the field insulation film (23)” to “form the channel stop region (P+)[.]” *Hwang-795*, [0028]. The “channel stop region (P+)” results in precise “isolation between pixels” and “may resolve the problems such as crosstalk[.]” *Hwang-795*, [0028]; *Dec.*, ¶185. A POSITA would have understood or found obvious an electric field between the channel stop region (P+) and the more lightly doped p-type semiconductor layer 20 is created at the surface of the semiconductor layer 20 adjacent the trench (i.e., a *surface field*) due to the dopant concentration gradient. *Dec.*, ¶182. Thus, *Hwang-795* teaches a *low refractive index material is doped with a dopant to create a surface field*. *Dec.*, ¶183.

A POSITA would have found obvious and been motivated to dope *Hwang-099*’s layers 210 in layer 220 with boron, per *Hwang-795*, to *create a surface field* and “significantly improve the performance of the image sensor.” *Hwang-795*, [0036]; *Dec.*, ¶¶185-186. *Hwang-795* expressly motivates including boron in *Hwang-099*’s reflection layer 210 “to reduce intermixing and crosstalk between image data and unit pixels, through more precise isolation between unit pixels.” *Hwang-795*, [0015]. *Dec.*, ¶¶185-186. Including a dopant such as boron would improve a pixel’s “charge transfer efficiency” and “minimize dark...current[.]” *Hwang-795*, [0029]-[0030], [0036]; *Dec.*, ¶¶185-186. A POSITA would have recognized formation of “channel stop region” and resulting electric field created at

the surface pattern 110 (*surface field*) in Hwang-099's image sensor would have reduced electrical crosstalk and "increase[d] the photosensitivity" of the image sensor. *Hwang-795*, [0009], [0017]-[0018], [0028]; *Dec.*, ¶¶185-186. Because electrical crosstalk is decreased, the *surface field* improves electrical isolation, like the improvement from doping described in the '764 Patent, 9:60-65. *Dec.*, ¶¶184-185.

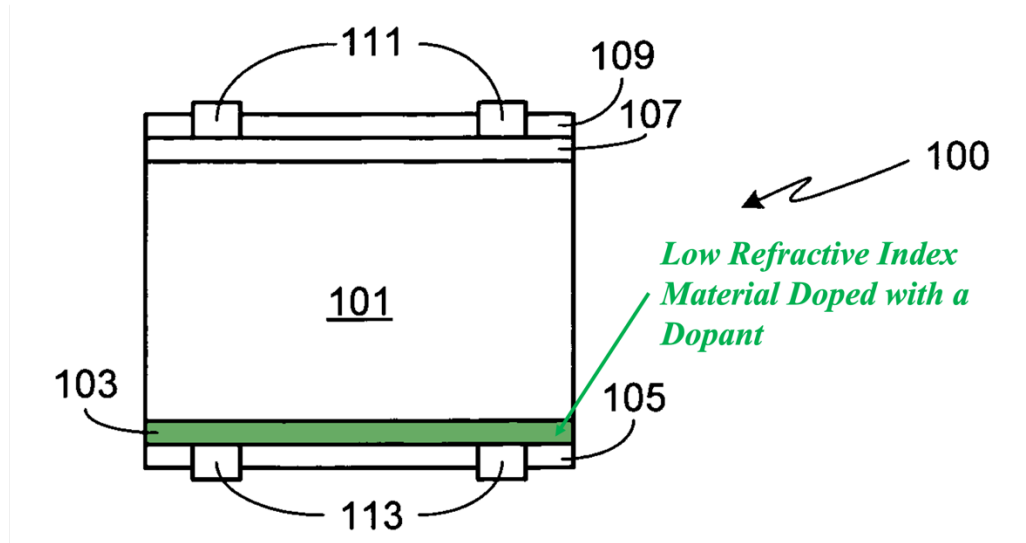
The modification uses a known technique (depositing BSG in a trench) to improve similar devices in the same way (Hwang-099's image sensor's performance is improved similar to Hwang-795's image sensor (e.g., decreased electrical crosstalk)). *Dec.*, ¶187.

The modification would have a REOS given techniques for doping and/or depositing borosilicate glass were well-known, and a POSITA would have merely needed to dope Hwang-099's silicon dioxide layers 210 with boron such that grooves 205 are filled with BSG instead of undoped silicon dioxide. *Dec.*, ¶¶187-188.

b) Backside Light Trapping Material: Kaes's Teachings

Kaes teaches a "bifacial solar cell" comprised of a p-type "silicon substrate." *Kaes*, [0013], Figure 1. "The bottom surface of substrate 101 is doped, thereby forming a back surface doped region 103." *Kaes*, [0013]. Region 103 "can be formed by...depositing a boron doped silicon dioxide...layer" on the "back surface of substrate 101." *Kaes*, [0014]. "[B]oron from region 103 is diffused into the back

surface of substrate 101 to form a back **surface field** (BSF).” *Kaes*, [0016]. “[D]oped region 103 reduces back surface recombination....” *Kaes*, [0013]. *Kaes* thus teaches a *low refractive index material* (silicon dioxide) *doped with a dopant* (boron) to *create a surface field* (back surface field). *Dec.*, ¶¶189-190.



Dec., ¶190.

A POSITA would have found obvious and been motivated to dope Hwang-099’s silicon dioxide layer 151 in layer 155a with boron (*wherein at least one of the two low refractive index materials is doped with a dopant*) to create a back surface field (*to create a surface field*), per *Kaes*. *Dec.*, ¶191. The combination is expressly motivated by *Kaes* and would have resulted in “reduce[d] back surface recombination” in Hwang-099’s pixel. *Kaes*, [0013]; *Dec.*, ¶191. It was well-known that recombination of electron-hole pairs prevents generating an electrical signal. *Dec.*, ¶191. Thus, a POSITA would have been motivated to dope the low refractive

index layer 151 of layer 155a (*backside light trapping material*) to create a back surface field (*surface field*) such that recombination of electron-hole pairs near the backside surface would be reduced, thereby increasing quantum efficiency of Hwang-099's pixel. *Dec.*, ¶191.

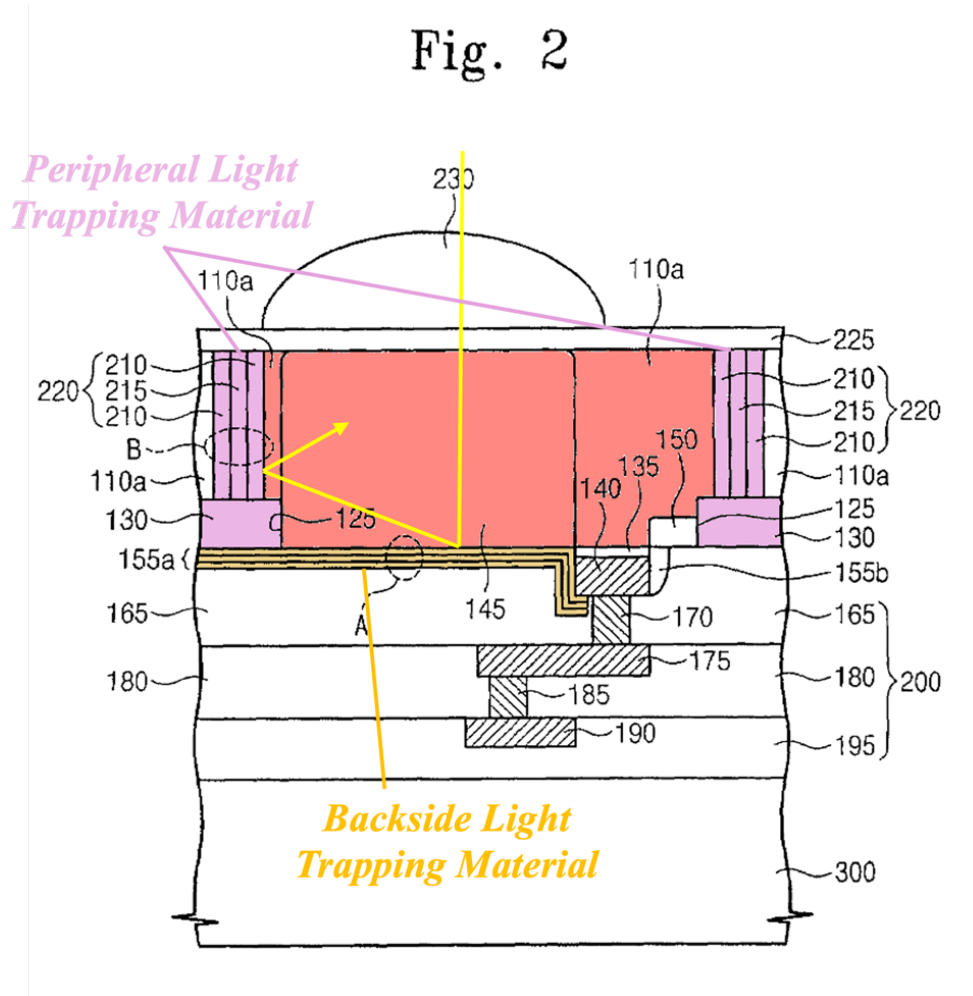
The combination is application of a known technique (creating a back surface field) to a known device (image sensor) ready for improvement to yield a predictable result (reducing back surface recombination). *Dec.*, ¶192. The modification would have a REOS because it would have merely required doping Hwang-099's silicon dioxide layer 210 with boron and diffusing boron into the backside of the pattern 110a. *Dec.*, ¶192. Methods to dope silicon dioxide with boron were well-known, and diffusion of dopants into silicon was common practice. *Dec.*, ¶192.

9. 1[d]

Layer 155a (*backside light trapping material*) reflects light back toward the *pixel*. Claim 1[b], §V.A.5. Layer 155a “has at least two layers with different refractive indexes[,]” with at least one “boundary surface reflecting light[.]” *Hwang-099*, 8:64–9:14. “[E]xternal light incident on the second surface of the photodiode 145” is “reflected by” at least layer 155a's boundary surface and another boundary surface and “is incident again on the photodiode 145.” *Hwang-099*, 9:6-14. Thus, Hwang-099 expressly teaches *light contacting* reflection layer 155 (*backside light*

trapping material) is reflected back toward the *pixel*, namely photodiode 145 forming part of *pixel*. Dec., ¶¶194-195.

Similarly, Hwang-099's layer 220 (*peripheral light trapping material*) reflects light back toward the *pixel*. Claim 1[c], §V.A.6. In layer 220, light "reflected from the first and second boundary surfaces" is "reflected by the third boundary surface" and the "fourth boundary surface" and "is incident again on the photodiode 145[.]" Hwang-099, 10:28-40; Dec., ¶¶196-197.



Dec., ¶¶197.

B. Claim 2

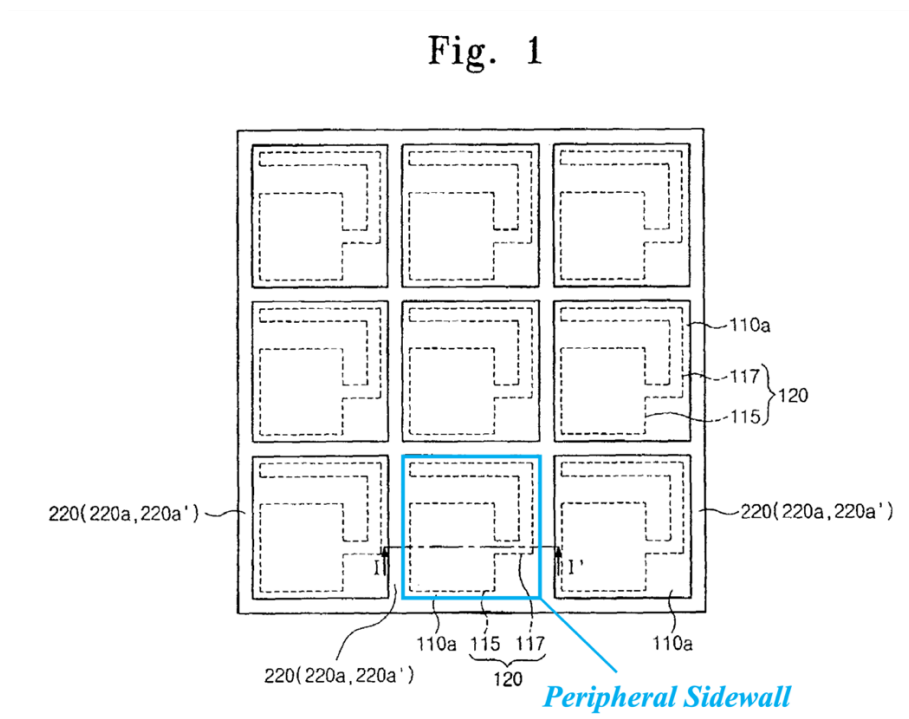
Hwang-099 teaches both layers 155a, 220 include silicon (i.e., a *high refractive material*) *sandwiched between* two layers of silicon oxide (i.e., *two low refractive index materials*). See Claim 1[c][i], §V.A.7 (incorporated herein). Dec., ¶198.

C. Claim 3

See Claim 1[c][ii], §V.A.8 (incorporated herein), *wherein the dopant is boron*. Dec., ¶199.

D. Claim 4

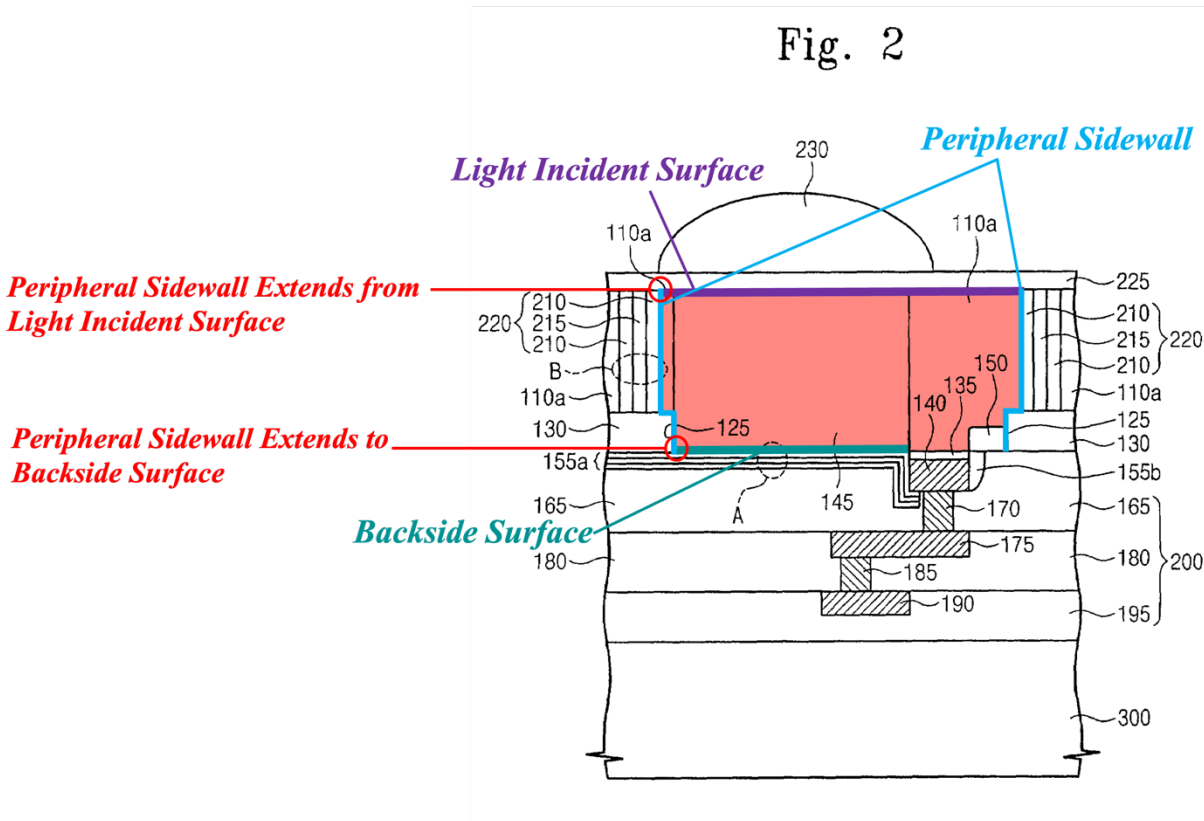
Hwang-099 teaches the *peripheral sidewall* extends completely around the *pixel periphery*, such that there are no gaps in the sidewall as it encloses the pixel:



Dec., ¶200; Claim 1[a][ii], §V.A.4.

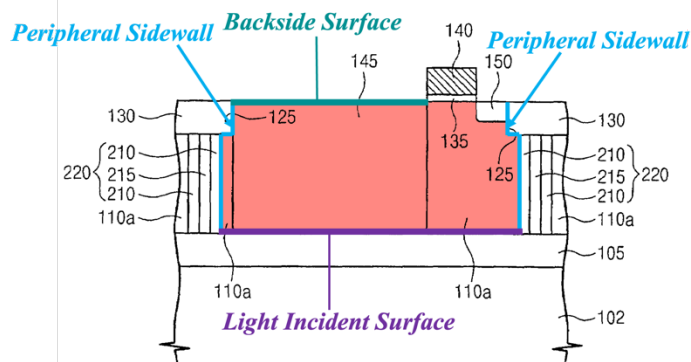
E. Claim 5

Hwang-099 teaches or suggests the *peripheral sidewall* extends from the *light incident surface* to the *backside surface*:



Dec., ¶201; Claims 1[a][i]-[ii], 1[c], §§V.A.3-4, V.A.8.

Additionally, etching of trench 125 and grooves 205 forming the *peripheral sidewall* includes etching to a portion of the second surface of pattern 110a (*light incident surface*). Claim 1[a][ii], §V.A.4; *Dec.*, ¶202. Similarly, pattern 110a is etched through a portion of the first surface (*backside surface*). *Id.*



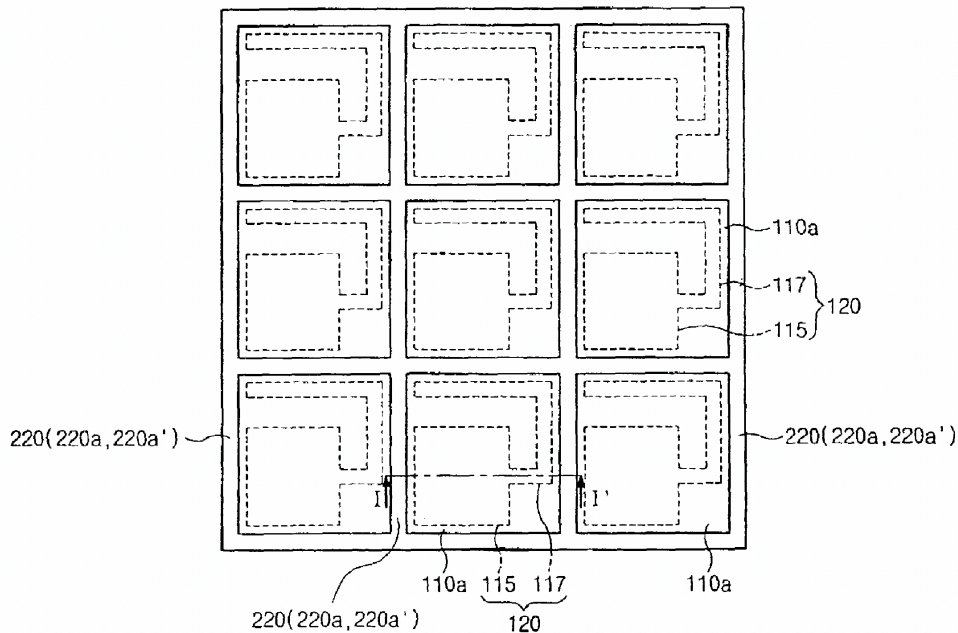
F. Claim 7

29

in each pattern 110a satisfies the claimed *array of light trapping pixel devices. Dec.*,

¶¶204-206; Claim 1[a], §V.A.2.

Fig. 1



Hwang-099, Figure 1.

VI. GROUND 2: CLAIM 6 IS OBVIOUS OVER HWANG-099, HWANG-795, KAES, KONNO

A. Konno's Teachings

Konno teaches a *backside light trapping material* that is a *metal layer*, namely second reflecting layer 120. Konno teaches first and second reflecting layers 121, 120, respectively, “hav[ing] a function of confining photons which entered the solid-state imaging element 110.” *Konno*, 8:31-38. Layer 120 covers the backside surface and may be formed of “**metal** such as aluminum or silver.” *Konno*, 8:35-38, 11:42-52.

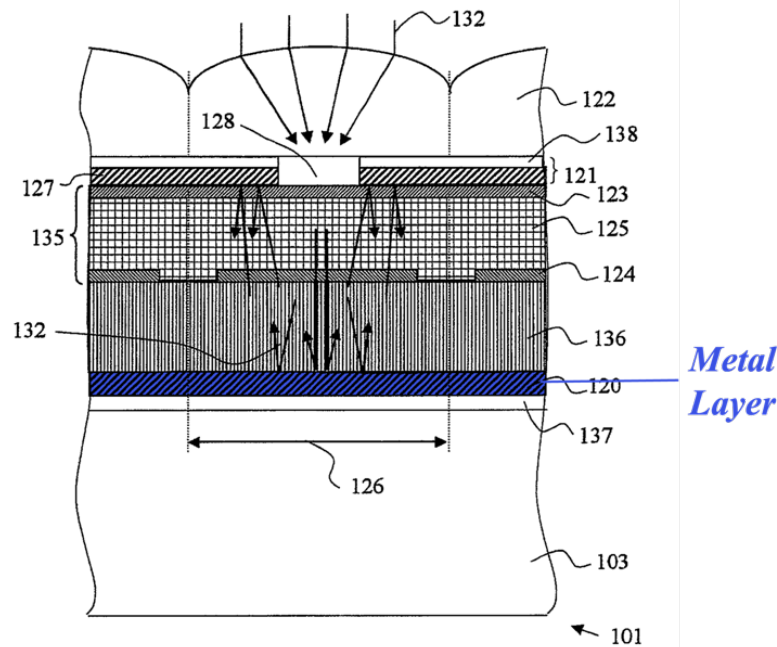


Fig.3

Dec., ¶¶207-208.

B. Motivation to Combine

A POSITA would have found obvious and been motivated to replace Hwang-099's backside light trapping material with a metal layer, per Konno. *Dec.*, ¶209. Using metal as reflectors in pixels, including as a backside light trapping material, was common prior to the '764 Patent. *Id.* Compared to Bragg reflectors, a metal layer would have offered more broadband reflectivity, as metals typically have higher reflectivity than other materials. *Id.* Additionally, a metal layer would have reduced manufacturing complexity as compared to a Bragg reflector. *Dec.*, ¶¶209-210. Such a combination is a simple substitution of one known element (metal layer

as a backside light trapping material) for another (a Bragg reflector as a backside light trapping material) to obtain predictable results (e.g., light reflectivity). *Id.*

The combination would have a REOS at least because metal was a widely available material and because techniques for depositing a metal layer in an image sensor were well-known. *Dec.*, ¶211; *cf.* '764 Patent, 7:56-99.

VII. GROUND 3: CLAIMS 8-12, 14-15 ARE OBVIOUS OVER HWANG-099

A. Claim 8

Limitations 8[Pre]-[c], 8[d][i] are identical to 1[Pre]-[c], [d]. *See* §§V.A.1-V.A.6, V.A.9, respectively (incorporated herein). *Dec.*, ¶¶213-218, 222.

1. 8[d]

See Claim 1[c][i], §V.A.7. In both *the backside light trapping material* and *the peripheral light trapping material*, the *first material* is silicon with a refractive index of ~ 4 , which is *sandwiched between two second materials* of silicon oxide with a refractive index of a ~ 1.46 . *Hwang-099*, 9:25-34, 10:48-55; *Dec.*, ¶¶219-221; *cf.* '764 Patent, 10:13-16 (describing the two low refractive index materials may be the same or different materials). The *difference in refractive index* is approximately 2.54, which is *at least 0.2*.

B. Claim 9

Hwangs-099's two second materials in both the *peripheral* and *backside light trapping materials* are silicon oxide, having a refractive index of 1.46, *less than about 2.1*. Claim 1[c][i], §V.A.7; *Dec.*, ¶223.

C. Claim 10

Hwangs-099's *two second materials* are silicon oxide, a *member* of the claimed group *oxide*. *Dec.*, ¶224; Claim 1[c][i], §V.A.7.

D. Claim 11

Hwangs-099's *two second materials* are silicon oxide, a *member* of the claimed group *silicon oxide*. *Dec.*, ¶225; Claim 1[c][i], §V.A.7.

E. Claim 12

Hwangs-099's *first material* is silicon, having a refractive index of approximately 4, which is *greater than or equal to about 2.1*. *Dec.*, ¶226; Claim 1[c][i], §V.A.7, (incorporated herein).

F. Claim 14

See Claim 4, §V.D. *Dec.*, ¶227.

G. Claim 15

See Claim 5, §V.E. *Dec.*, ¶228.

VIII. GROUND 4: CLAIM 13 IS OBVIOUS OVER HWANG-099 AND KOMURO

A. Hwang-099's Teachings

Hwang-099's *first material* is silicon with a refractive index of “approximately 4” at a “long red-colored wavelength.” *Hwang-099*, 9:29-33; Claim 1[c][i], §V.A.7; *Dec.*, ¶229.

B. Komuro's Teachings

Komuro teaches silicon, including “single crystal silicon, amorphous silicon, and polysilicon[,]” have a refractive index of 3.85 at the wavelength of red light. *Komuro*, [0137]-[0138].

TABLE 1

	Refractive Index (n)			Extinction Coefficient (k)		
	Blue Light 450 nm	Green Light 550 nm	Red Light 650 nm	Blue Light 450 nm	Green Light 550 nm	Red Light 650 nm
Germanium	4.5	6.0	5.5	2.3	2.1	1
Silicon	4.69	4.08	3.85	0.151	0.03	0.017
Tungsten	3.31	3.48	3.76	2.47	2.72	2.95
Plasma Silicon Nitride	2.07	2.04	2.01	0.004	0	0.002
Aluminum	0.618	0.958	1.47	5.47	6.69	7.79
Copper	1.17	0.9	0.21	2.39	2.6	3.67
Reference: Silicon Dioxide	1.45	1.45	1.45	0.00	0.00	0.00

Komura, Table 1.

Hwang-099 combined with Komuro teaches or suggests *the first material* (silicon) *includes a member selected from...polycrystalline silicon, amorphous silicon, single crystal silicon*. Polysilicon is known as polycrystalline silicon. *Dec.*, ¶230.

C. Motivation to Combine

A POSITA would have found obvious and been motivated to implement Hwang-099's silicon (*first material*) as “any one of single crystal silicon, amorphous silicon, and polysilicon” because each possess a refractive index of 3.85 (i.e., ~4 per

Hwang-099's refractive index for silicon). *Hwang-099*, 9:29-33; Claim 1[c][i], §V.A.7; *Dec.*, ¶231. The combination would have a REOS and yielded predictable results at least because each of single crystal silicon, amorphous silicon, and polysilicon were well-known for use in fabricating image sensors. *Dec.*, ¶232.

IX. GROUND 5: CLAIMS 17-19 ARE OBVIOUS OVER HWANG-099 IN COMBINATION WITH MOULI AND/OR NOZAKI

A. Claim 17

Limitations 17[Pre]-17[c], 17[c][ii] are identical to 1[Pre]-1[c], 1[d]. *See* §§ V.A.1-V.A.6, V.A.9, respectively (incorporated herein). *Dec.*, ¶¶233-238, 255.

1. 17[c][i]

Mouli teaches a sloped trench wall associated with the *peripheral light trapping material*; Nozaki teaches a sloped backside surface associated with the *backside light trapping material*. Therefore, the proposed grounds render obvious both the backside light trapping material and the peripheral light tapping material having a sloped surface.

a) Mouli's Sloped Trench Wall

Mouli teaches methods of “forming an isolating trench among pixels or other active areas of a semiconductor device.” *Mouli*, Abstract. A “deep trench 202” is created in “silicon substrate 200” through “anisotropic etch[ing].” *Mouli*, 4:48-49; *Dec.*, ¶¶240-241. Mouli's trench sidewalls are “high conical sidewalls” (*sloped*):

Sloped Surface of Peripheral Sidewall

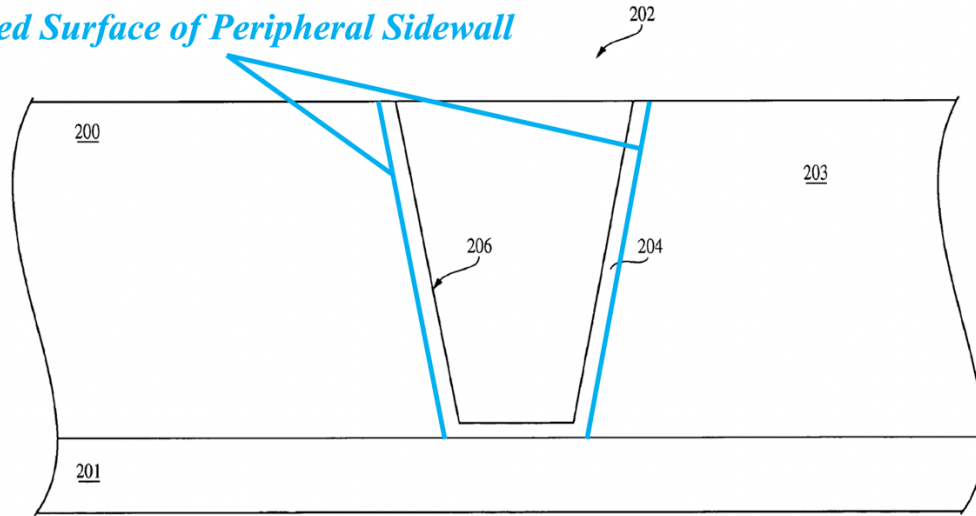


FIG. 3B

Dec., ¶241; *Mouli*, Figure 3B, 5:16-18.

In the combination, Hwang-099's trench sidewall is modified to be sloped, per *Mouli*. Hwang-099's peripheral light-trapping material deposited on the (now modified) sloped trench sidewall at the pixel interface has a commensurate *sloped surface*. *Dec.*, ¶242.

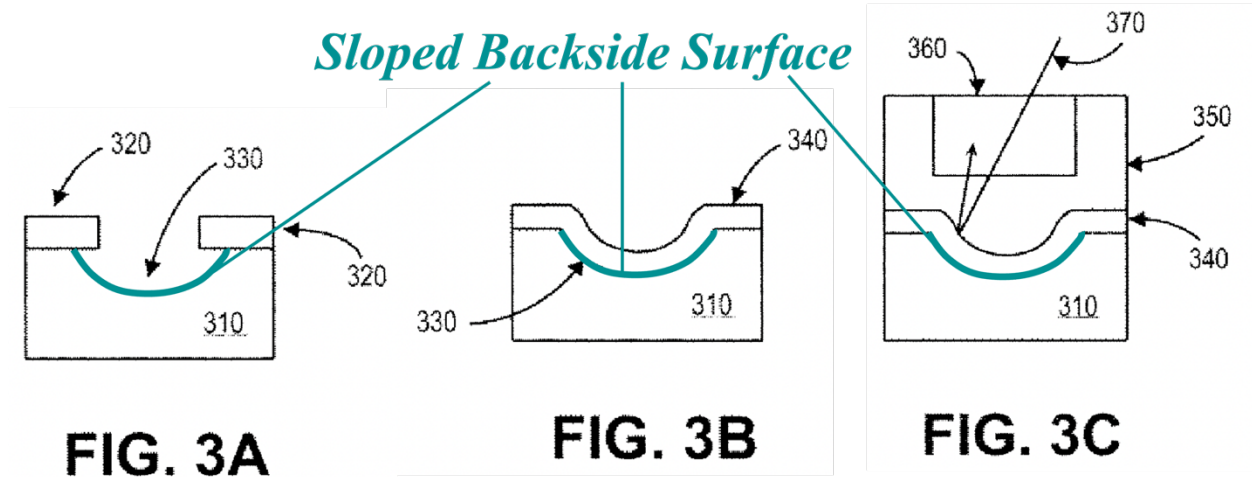
A POSITA would have found obvious and been motivated to incorporate *Mouli*'s "conical" (*sloped*) trench sidewalls into Hwang-099's pattern 110a. *Dec.*, ¶243. Etching trenches into semiconductor substrates commonly causes defects to form. *Dec.*, ¶243. Passivation of these defects through dielectric layer deposition was a well-known technique but difficult to achieve on vertical sidewalls. *Dec.*, ¶244. Passivation of defects was significantly improved when a dielectric liner was deposited on a sloped sidewall versus a vertical sidewall. *Id.* A POSITA would have

also understood sloped sidewalls improve light collection efficiency. *Dec.*, ¶246. A POSITA would have been motivated to modify Hwang-099 according to Mouli's teachings to form sloped sidewalls to improve the performance of the sensor. *Dec.*, ¶246. Such a combination represents use of a known technique (sloped sidewalls) to improve similar image sensors in the same way. *Dec.*, ¶246.

The combination would have a REOS at least because Hwang-099 already discloses etching trenches into the silicon substrate, Mouli discloses forming methods for etching sloped trenches into silicon, both Hwang-099 and Mouli disclose methods for depositing materials on the etched trench sidewalls, and etching sloped trenches was a well-known technique. *Dec.*, ¶247.

b) Nozaki's Sloped Backside Surface

Nozaki teaches a *sloped surface at the pixel device interface of the backside light trapping material*, namely a reflector having a complex-shaped surface. *Nozaki*, Abstract; *Dec.*, ¶248. Reflectors 140,142,144 “redirect the non-absorbed incident light towards the photodiode.” *Nozaki*, [0018], [0027], Figure 1. A “concave-shaped surface 330 [is] formed within substrate 310[,]” then a “reflective layer 340 is conformally deposited across the face of the concave-shaped surface 330.” *Nozaki*, [0035].



Dec., ¶¶248-249. Concave-shaped surface 330 is underneath photodiode 360 (Figure 3C) and opposite a surface on which light is incident, thus making Nozaki’s concave-shaped surface a backside surface. *Nozaki*, [0036].

In the combination, Hwang-099’s backside surface is modified to be sloped, per Nozaki. Hwang-099’s backside light trapping material interfacing the (now modified) sloped backside surface at the pixel interface has a commensurate *sloped surface*. Dec., ¶250; Claim 1[b], §V.A.5.

A POSITA would have found obvious and been motivated to modify Hwang-099 to have a concave-shaped (sloped) backside surface, per Nozaki. Dec., ¶252. The modification would have resulted in Hwang-099’s reflection layer 155a (*backside light trapping material*) being sloped. *Id.* The complex shape of Nozaki’s reflectors 140,142,144 allows for “multiple angles of reflection that reflect and focus incident light towards the photosensitive element[,]” thus expressly motivating the combination. *Nozaki*, [0027], [0019]; Dec., ¶252. The combination is the use of a

known technique (implementing sloped backside reflectors) to improve similar image sensors in the same way. *Dec.*, ¶252.

The modification would have a REOS at least because Hwang-099 already discloses a backside surface and methods for forming a *backside light trapping material*, Nozaki teaches methods of forming the concave-shaped surface, and methods of providing sloped backside surfaces in pixels were well-known. *Dec.*, ¶253; *Hwang-099*, 8:28–9:34; *Nozaki*, [0034]–[0037].

c) Obviousness of Combining Both Mouli and Nozaki

A POSITA would have found obvious and been motivated to modify both Hwang-099's backside surface (and commensurately, backside light trapping material on the backside surface) and peripheral sidewall (and commensurately, the peripheral light trapping material on the peripheral wall) to have a sloped surface. There is a REOS in each of the individual combinations (§§IX.A.1.a, IX.A.1.b). Modifying both the backside surface and peripheral sidewall to be sloped would achieve at least the same benefits as modifying either one of the backside surface or sidewall and there would be no adverse performance in implementing both modifications. *Dec.*, ¶254.

B. Claim 18

See Claim 4, §V.D. *Dec.*, ¶256.

C. Claim 19

See Claim 5, §V.E. *Dec.*, ¶257.

X. GROUND 6: CLAIM 20 IS OBVIOUS OVER HWANG-099 IN COMBINATION WITH MOULI AND/OR NOZAKI AND FURTHER IN VIEW OF KONNO

A. Claim 20

1. Konno's Teachings

Konno teaches a *metal layer* as a *backside light trapping material*. See Claim 6, §VI.A (incorporated herein). *Dec.*, ¶259.

2. Motivation to Combine

See Claim 6, §VI.B (MTC/REOS incorporated herein), providing reasons why a POSITA would have been motivated to modify Hwang-099's layer 155a (*backside light trapping material*) to be a *metal layer* per Konno. *Dec.*, ¶¶260-263.

XI. GROUND 7: CLAIMS 16, 21-24 ARE OBVIOUS OVER HWANG-099 IN COMBINATION WITH KONNO

A. Claim 16

Claim 16 depends from independent Claim 8. See Claim 8, §VII.A. *Dec.*, ¶264.

1. Konno's Teachings

Konno teaches a *metal layer* as a *backside light trapping material*. See Claim 6, §VI.A (incorporated herein). *Dec.*, ¶265.

2. Motivation to Combine

See Claim 6, §VI.B (MTC/REOS incorporated herein), providing reasons why a POSITA would have been motivated to modify Hwang-099's layer 155a (*backside light trapping material*) to be a *metal layer* per Konno. *Dec.*, ¶¶266-269.

B. Claim 21

Petitioners provide two alternative mappings for Claim 21 (*see* §§XI.B-C), both relying on a combination of Hwang-099-Konno. The first mapping of Claim 21 modifies Hwang-099 to include Konno's textured transparent layer 36 in the Figure 7 embodiment. *Dec.*, ¶270; § XI.B. In the second mapping, Hwang-099's layer 155a (*backside light trapping material*) is replaced with Konno's combined layer 120 and textured transparent layer 136 in the Figure 7 embodiment. *Dec.*, ¶289; §XI.C.

Limitations 21[Pre]-21[c], 21[d][i] are identical to 1[Pre]-1[c], 1[d]. *See* §§V.A.1-V.A.6, V.A.9, respectively (incorporated herein). *Dec.*, ¶¶271-276, 288.

1. 21[d]

a) Konno's Teachings

Konno teaches a *textured layer*, namely transparent layer 136 in Figure 7 between the bottom of photoelectric conversion element 135 and second reflecting layer 120. Transparent layer 136 "is formed from a material which transmits photons, for example, glass and plastics such as acrylic resins." *Konno*, 9:35-37. Transparent layer 136 is *textured* because it includes concave and convex elements: "The concaves and the convexes of the transparent layer 136 can be formed by...sputtering and microlithography." *Konno*, 14:42-45; *Dec.*, ¶¶277-278; *cf.* '764 *Patent*, 4:29-37.



Konno's Backside Surface

Textured Layer

Fig.7

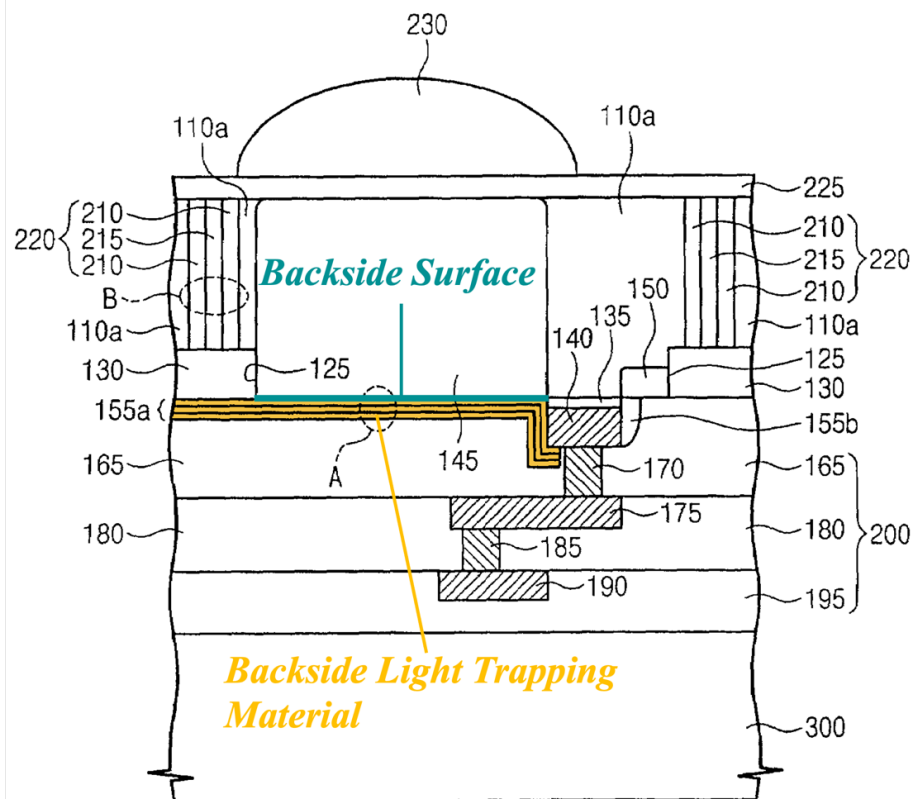
Dec., ¶280.

Konno teaches the *textured layer* is *positioned to interact with light proximal to the backside surface* because the transparent layer 136 is underneath the bottom (i.e., backside surface) of Konno's photoelectric conversion element 135. Specifically, transparent layer 136 is located on Konno's backside surface, opposite the light incident surface, as shown in Figure 7. *Dec.*, ¶¶279-280. Transparent layer 136 "can provide concaves and convexes which realizes a large reflection angle." *Konno*, 15:2-5. Thus, a POSITA would have understood transparent layer 136 *is positioned to interact with light proximal to the backside surface* because it transmits

and reflects light and is located underneath the *backside surface* of Konno's photoelectric conversion element 135. *Dec.*, ¶¶279-280.

In the combination, transparent layer 136 (*textured layer*) is located underneath Hwang-099's *backside surface*, between it and layer 155a (*backside light trapping material*). *Hwang-099*, Figure 2; Claim 21[b].

Fig. 2



Dec., ¶¶281-282. Therefore, in the combination, transparent layer 136 (*textured layer*) is positioned to interact with light proximal to [Hwang-099's] *backside surface*. Dec., ¶282.

b) Motivation to Combine

A POSITA would have found and obvious and been motivated to include Konno's transparent layer 136 in Hwang-099's sensor, specifically underneath Hwang-099's *backside surface* identified in Figure 2, above, and on top of layer 155a (*backside light trapping material*).

Per Dr. Shanfield, providing a textured layer on the backside surface would have enhanced internal reflection of incident light within Hwang-099's pixel. *Dec.*, ¶283. Compared to a smooth surface, Konno's textured surface would have diffusely scattered light, thereby increasing the path length of light throughout the geometry of the pixel. *Dec.*, ¶¶283-284. The textured layer provided by Konno's transparent layer 136 would have worked in conjunction with Hwang-099's layer 155a to increase the amount of incident light reflected toward photodiode 145, in part by increasing the range of angles that light reflects back into the pixel. *Dec.*, ¶¶283-284. Thus, the modification would have predictably increased the quantum efficiency of Hwang-099's pixel. *Dec.*, ¶283. The modification is nothing more than application of a known technique (providing a textured layer) to a known device (image sensor) in the same way. *Dec.*, ¶284.

The modification would have a REOS at least because it would have merely required depositing Konno's transparent layer 136 on the backside surface of Hwang-099 and texturing the transparent layer, which was well-within the skill set

of a POSITA. *Dec.*, ¶285. Indeed, Konno teaches transparent layer 136 is textured using “sputtering and microlithography.” *Konno*, 14:42-45.

A POSITA would have also understood that in the combination, layer 155a continues functioning as a Bragg reflector even with Konno’s transparent layer 136 present. *Dec.*, ¶287.

C. Claim 21

Limitations 21[Pre]-21[a][ii], 21[c] are identical to 1[Pre]-1[a][ii], 1[c]. *See* §§V.A.1-V.A.4, V.A.6, respectively (incorporated herein). *Dec.*, ¶¶294-297, 304.

1. Explanation of Combination and Motivation for the Combination

The following mapping of Claim 21 relies on Hwang-099-Konno. Rather than providing a motivation of the modification at each of Claims 21[b], 21[d], Petitioners provide a motivation for the modification here given the modification to Hwang-099 works to take advantage of Konno’s complementary textured transparent layer and metal reflecting layer.

A POSITA would have found obvious and been motivated to replace Hwang-099’s layer 155a with Konno’s combined metal reflecting layer 120 and textured transparent layer 136. *Dec.*, ¶289. Advantages from implementing Konno’s textured layer 120, comprised of aluminum or silver, as the *backside light trapping material* were discussed previously. *See* Claim 6, §§VI.A-B (MTC incorporated herein); *Dec.*, ¶290.

Additionally, a *textured* metal layer, per Konno, as opposed to a metal layer alone, would provide the same advantages discussed above for textured layers. *See* Claim 21[d], XI.B.1.b. That is, layer 120 comprising concaves and convexes would reflect light diffusely versus specularly, thereby increasing the path length of light and thus, the probability of light absorption. *Dec.*, ¶291. Thus, a textured metal layer (as opposed to a textured layer alone or a metal layer alone) would simultaneously provide the benefits of both types of layers and been motivated to implement Konno’s textured layer 120 in Hwang-099’s image sensor. *Dec.*, ¶291.

Yet further, textured transparent layer 136 would similarly reflect light diffusely versus specularly, thereby increasing the sensitivity of Hwang-099’s pixel. *Dec.*, ¶292. Konno expressly states “by providing the transparent layer 136, concaves and convexes of various sizes can be realized.” *Konno*, 15:3-5, 9-11; *Dec.*, ¶292. Further, modifying Hwang-099 to implement *both* transparent layer 136 and layer 120 would have allowed a POSITA to reap the benefits of a textured metal layer without having to physically texture the surface of Hwang-099’s *pixel*. *Dec.*, ¶292. As acknowledged by Konno, adding texture to the photosensitive portion of an image sensor would cause problems such as increased dark current, among others. *Konno*, 15:15-17; *Dec.*, ¶292. Additionally, having a textured transparent layer between the *backside surface* and textured layer 120 would prevent diffusion of the

metal into the pixel, which would “adversely affect the photoresponsive characteristics[.]” *Dec.*, ¶292.

Thus, a POSITA would have been motivated to replace layer 155a with both transparent layer 136 and layer 120. *Dec.*, ¶293. In the combination, transparent layer 136 is the *textured layer*, as recited by Claim 21[d], and layer 120 is the *backside light trapping material*, as recited by Claim 21[b]. *Dec.*, ¶293.

The modification is the combination of prior art elements (textured layer, metal backside layer) using known methods (microlithographic texturing, material deposition) to obtain predictable results (improved reflectivity of light). *Dec.*, ¶293. The modification would have a REOS because metal was a widely available material, methods of texturing materials were well-known, and Konno teaches methods for forming both textured transparent layer 136 and layer 120. *Dec.*, ¶293.

2. 21[b]

In the Claim 21 mapping, Hwang-099’s backside light trapping material, namely multi-layered reflection layer 155a, is replaced with Konno’s metal reflecting layer 120 (mapped for Claim 21[b]) and further modified to include Konno’s textured layer (mapped for Claim 21[d]), as explained in §XI.C.1, above.

a) Hwang-099’s Teachings

Hwang-099’s layer 155a is a *backside light trapping material* substantially covering the backside surface. See Claim 1[b], §V.A.5. *Dec.*, ¶298.

b) Konno's Teachings

Konno also teaches a *backside light trapping material*, namely layer 120 in Figure 7. Konno teaches first and second reflecting layers 121, 120, respectively, “hav[ing] a function of confining photons which entered the solid-state imaging element 110.” *Konno*, 8:31-38; *Dec.*, ¶300. Layer 120 covers the backside surface and may be formed of “a thin film of metal such as aluminum or silver by deposition.” *Konno*, 8:35-38, 11:42-52. In the second embodiment, “the shape of the second reflecting layer 120 differs from that of the second reflecting of the first embodiment” where it “has a plurality of convexes and concaves on the reflecting surface” as shown in FIG. 7.” *Konno*, 13:50-63. Additionally, Konno’s layer 120 extends completely along the length of the backside surface of photoelectric conversion element (i.e., *substantially covers*). *Konno*, Figure 7, 13:14-19; *Dec.*, ¶302. Hwang-099’s layer 155a also completely covers (*substantially covers*) the *backside surface* of Hwang-099’s *pixel*. See Claim 1[b], §V.A.5. Thus, in the combination, because Hwang-099’s layer 155a is replaced with Konno’s layer 120 (*backside light trapping material*), Hwang-099’s *backside surface* is *substantially covered* by the *backside light trapping material*. *Dec.*, ¶303.

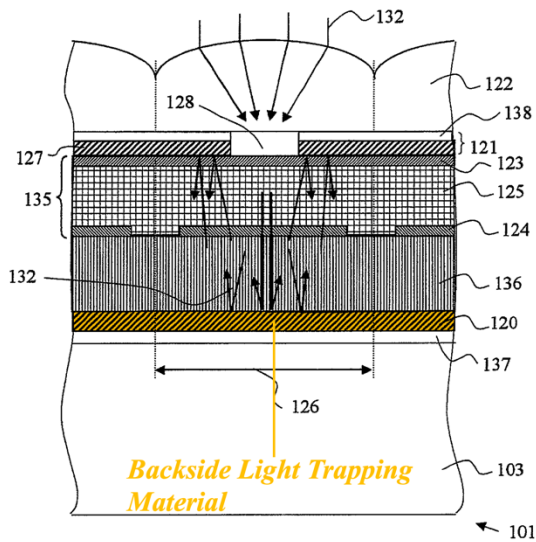


Fig.3

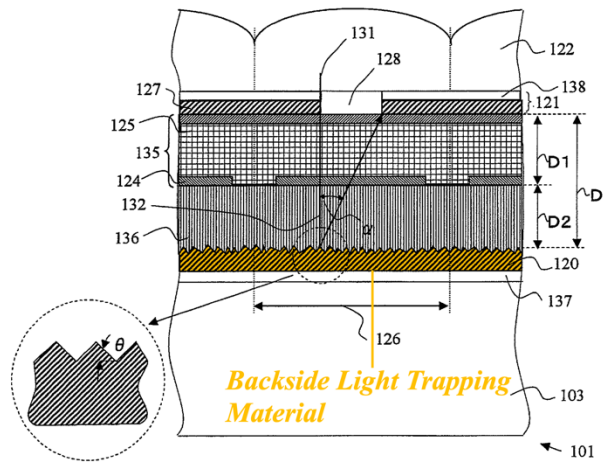


Fig.7

Dec., ¶¶299-302.

c) Motivation to Combine

See Claim 21, §XI.C.1. Dec., ¶303.

3. 21[d]

a) Konno's Teachings

As discussed for Claim 21[d], §XI.B.1.a (incorporated herein), Konno teaches a *textured layer* positioned to interact with light proximal to the backside surface, namely transparent layer 136, in the embodiment of Figure 7 that is between the bottom of photoelectric conversion element 135 and layer 120 (i.e., *backside light trapping material*). Konno, 14:42-45, 15:2-5; Dec., ¶¶305-308; cf. '764 Patent, 4:29-37.

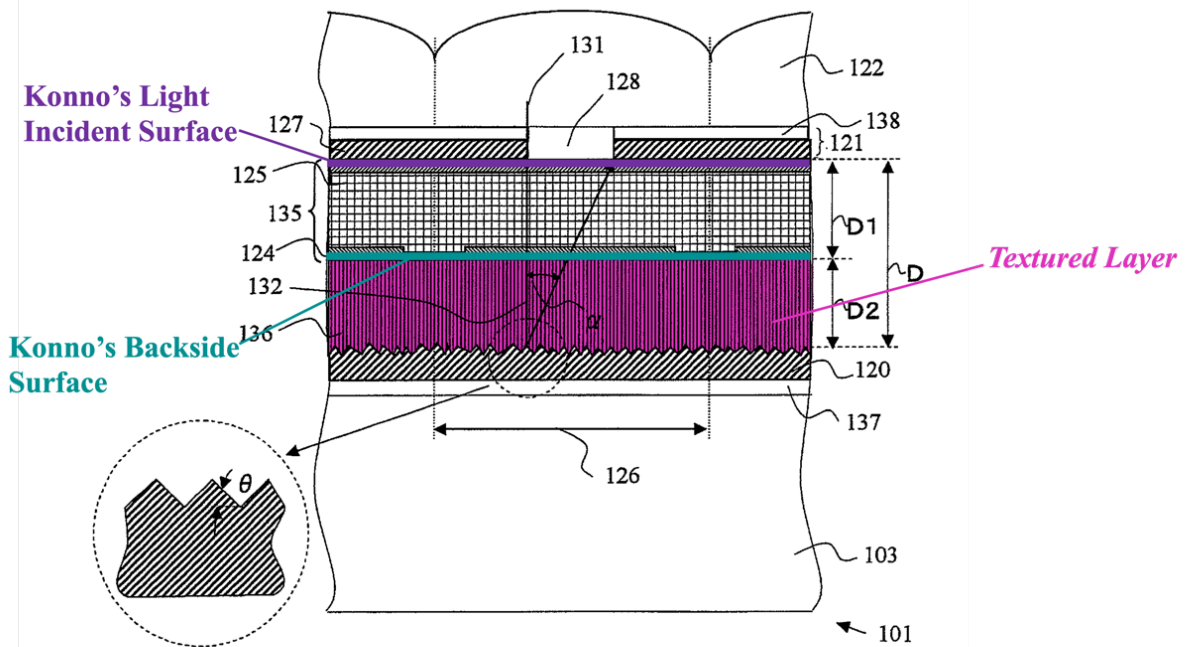


Fig.7

Konno, Figure 7.

b) Motivation to Combine

See Claim 21, §XI.C.1. Dec., ¶309.

4. 21[d][i]

a) Hwang-099's Teachings

Hwang-099 alone teaches *light contacting the peripheral light trapping material (layer 220) is reflected back toward the pixel. See Claim 1[d], §V.A.9; Dec., ¶310.*

b) Konno's Teachings

Additionally or alternatively, Konno teaches *light contacting the backside light trapping material (layer 120) is reflected back toward the pixel. Konno*

expressly teaches layer 120 “**reflects** incident photons 132,” wherein the “plurality of convexes and concaves on the reflecting surface” of layer 120 “can **reflect** them [(photons 132)] with a large reflection angle” toward photoelectric conversion element 135. *Konno*, 13:63-66; 14:10-16; Figure 7. *See* §XI.C.1 (MTC). In the combination, because layer 120 (*backside light trapping material*) is located underneath Hwang-099’s *backside surface*, light contacting it is reflected back up toward the *pixel*. *Dec.*, ¶¶311-312.

D. Claim 22

In both of the above mappings of the combination of Hwang-099-Konno for Claim 21, because transparent layer 136 (*textured layer*) is located underneath the *backside surface* and on top of layer 155a (in the first mapping) and layer 120 (in the second mapping), the *textured layer* is located between the *backside surface* and *backside light trapping material*. *See* Claims 21[b], 21[d], §§XI.B, XI.C; *Dec.*, ¶313.

E. Claim 23

See Claim 4, §V.D. *Dec.*, ¶314.

F. Claim 24

See Claim 5, §V.E. *Dec.*, ¶315.

G. Claim 25

In the second mapping of the Hwang-099-Konno combination of Claim 21 (§XI.C), layer 120 (*backside light trapping material*) is a *metal layer* because it is

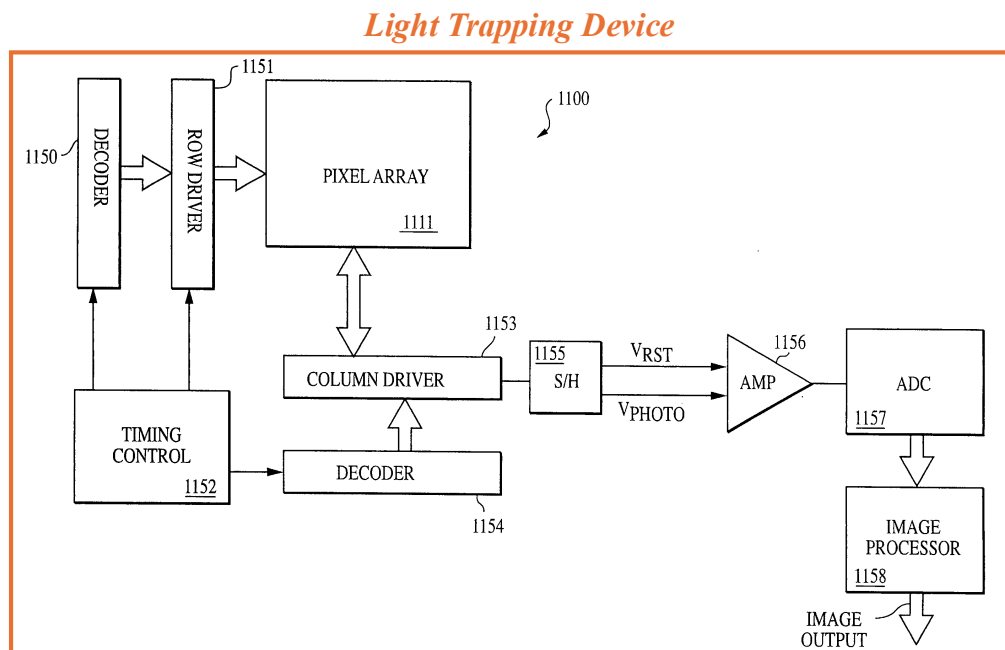
formed of “a thin film of metal such as aluminum or silver by deposition.” *See* Claim 21[b], §XI.C; *Konno*, 8:35-38, 11:42-52; *Dec.*, ¶316.

XII. GROUND 8: CLAIMS 1-5, 7 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584, KAES, HWANG-795

A. Claim 1

1. 1[Pre]

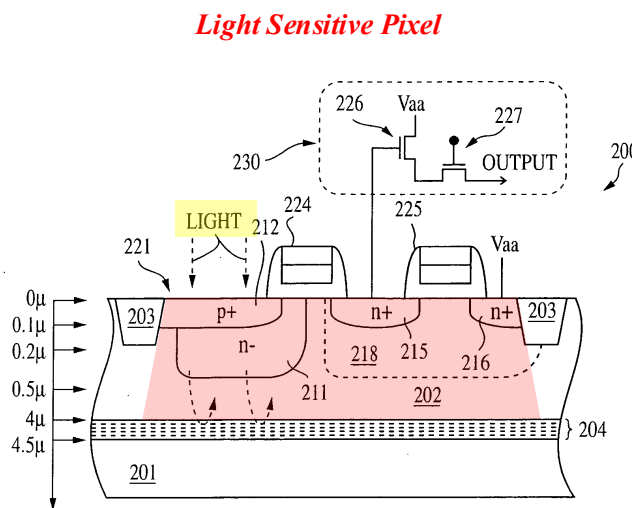
Hong teaches or suggests a *light trapping device*, namely “image sensor 1100 ha[ving] a pixel array 1111 containing a plurality of pixel cells arranged in rows and columns.” *Hong*, [0047], [0029], [0017]-[0018].



Dec., ¶318. Hong’s image sensor 1100 is *light trapping* because each pixel cell of image sensor includes elements “serv[ing] to reflect incident light, not initially absorbed into the photo-conversion device, back to the photo-conversion device.” *Hong*, [0006]; *Dec.*, ¶317.

2. 1[a]

Hong teaches or suggests a **pixel**, namely pixel cell 200 comprising at least semiconductor layer 202 including pinned photodiode 221 (the photo-conversion device comprising “an n-type region 211 underlying a p+ surface layer 212”), floating diffusion region 215, source/drain region 216, and p-well 218, which collectively operate to convert light into an electrical signal. *Hong*, [0017]-[0018]. Hong teaches “[t]he term ‘pixel’ refers to a picture element unit cell containing a photo-conversion device for converting electromagnetic radiation to an electrical signal[.]” *Hong*, [0017].



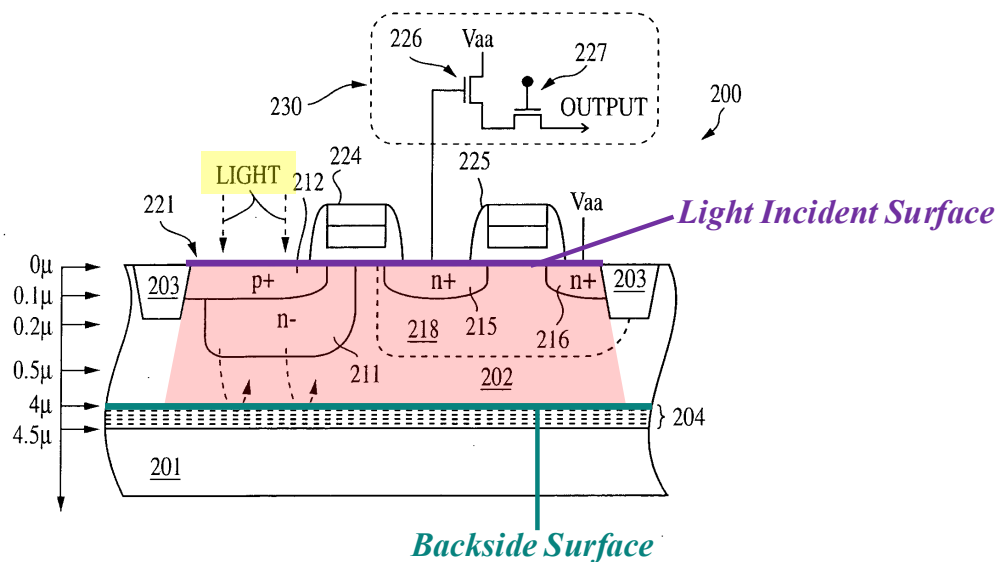
Dec., ¶324; *Hong*, [0009], [0018].

Photo-conversion device (photodiode 221) “convert[s] **electromagnetic radiation** [(e.g., light)] to an electrical signal[.]” and semiconductor layer 202 “is a layer of p-type silicon (Si)[.]” which operates with photodiode to collect electron-hole pairs. *Hong*, [0017], [0022]; *Dec.*, ¶320, ¶¶42-47.

Regarding elements 215, 216, transfer transistor 224 “operates to transfer charge from the photodiode 221 to the floating diffusion region 215” (located in p-well 218 with source/drain region 216), where electrical charge is stored prior to “readout” by readout circuit 230. *Hong*, [0018], [0022], [0048]; *Dec.*, ¶¶322-323. Before collecting charge, “the reset transistor 225 resets the floating diffusion region 215 to a predetermined voltage” provided by source/drain region 216, which is “connected to” “array voltage Vaa.” *Hong*, [0021]. Elements 215, 216, therefore, also facilitate collecting and converting light into an electrical signal, qualifying as *a light sensitive pixel*. *Dec.*, ¶¶322-324.

3. 1[a][i]

Hong’s *pixel* has a *light incident surface*, namely a top surface of semiconductor layer 202, shown by at least the purple line on top of pixel cell 200:



Dec., ¶325; *Hong*, [0022] (“transfer and reset transistors 224, 225, and photodiode 221 are located at a surface of a semiconductor layer 202”). Because the top surface of semiconductor layer 202 is a part of the claimed *pixel*, *Hong* teaches the *pixel* has a *light incident surface*. *Dec.*, ¶325; cf. '764 *Patent*, 6:47-49, 13:19-20.

The top surface of layer 202 is a *light incident* surface because light is incident on an exposed top surface of the pixel when the image sensor array is in use. *Hong* expressly teaches “[l]ight...incident on photodiode 221[,]” illustrated with the original text “LIGHT” in Figure 2. *Hong*, Figure 2, [0026], [0022], [0018]. Additionally, *Hong* teaches, suggests, or renders obvious light is incident on the entire exposed top surface of layer 202 and not just the portion of the top surface of the layer coinciding with the photodiode. *Dec.*, ¶326 (explaining Figure 2 is a cross-sectional view of *Hong*’s *pixel*).

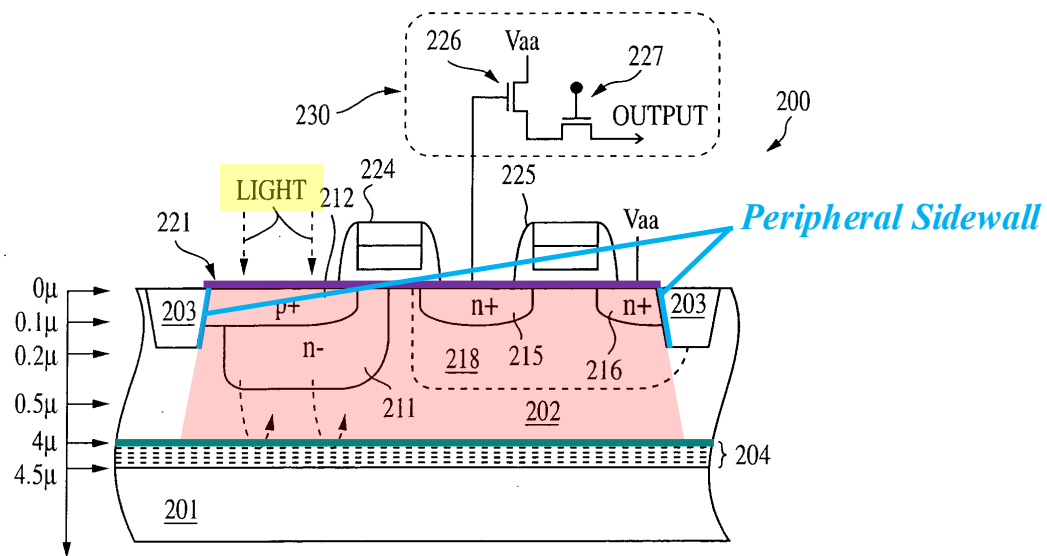
Hong also teaches a *backside surface* opposite the *light incident surface*, namely a bottom surface of semiconductor layer 202 indicated by the teal line in Figure 2, above, and opposite the *light incident surface*.

4. 1[a][ii]

Hong-Yamashita teaches, suggests, or renders obvious Claim 1[a][ii]. In the combination, *Hong*’s peripheral sidewall is modified to extend substantially around the pixel periphery, per *Yamashita*.

a) **Hong's Teachings**

Hong teaches a *peripheral sidewall*, namely a wall of isolation region 203. Isolation region 203 is a “shallow trench isolation (STI) region” “formed in the Si layer 202 and filled with a dielectric material.” *Hong*, [0018], [0033], [0021] (STI region 203 “adjacent” source/drain region 216), [0018] (photodiode 221 “adjacent” to isolation region 203).

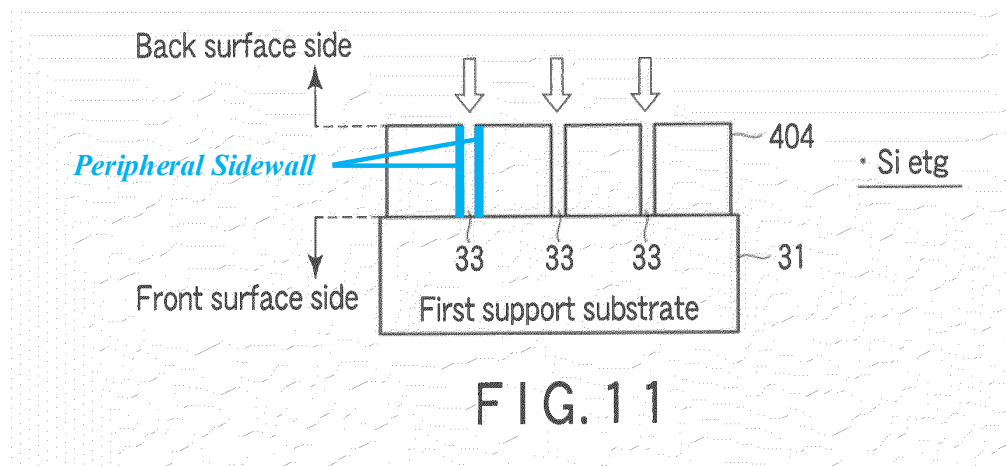


Dec., ¶329.

The sidewall of trenched isolation region 203 is a *peripheral sidewall* disposed into at least a portion of the pixel because the “trench” is “formed in” the semiconductor layer 202 (where layer 202 is part of the *pixel*) and on a periphery of pixel cell 200. *Hong*, [0033], Figure 2; *Dec.*, ¶¶329-330; *cf.* '764 Patent, 10:64-65.

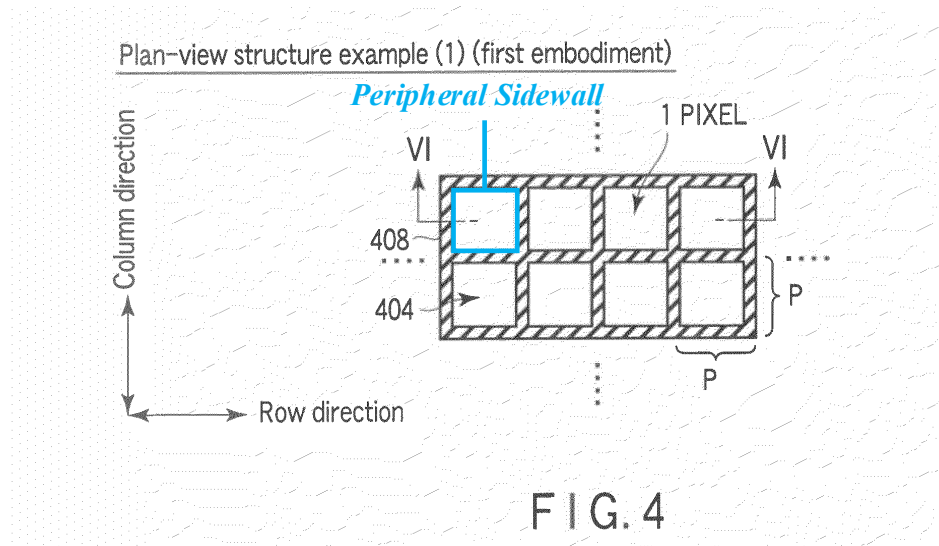
b) Yamashita's Teachings

Similarly, Yamashita teaches a *peripheral sidewall*, namely sidewall of trench 33. Trench 33 is etched through silicon substrate 404 from the “back side” “to the surface of the first support substrate 31” on the “front side” of substrate 404. *Yamashita*, [0100], [0102], Figures 10-11. *Dec.*, ¶¶331-333. Like Hong's isolation region 203 formed in Si layer 202 (*Hong*, [0033]) being part of the *pixel*, Yamashita's trench 33 formed in substrate 404 is part of a *pixel* (e.g., Yamashita's unit pixel 1) because “photodiode 2 [] is provided in the silicon substrate 404” and “photodiode 2 constitutes the photoelectric conversion unit.” *Yamashita*, [0061], Figure 6. Because Yamashita's trench 33 extends through silicon substrate 404, and substrate 404 is part of a pixel, a sidewall of the trench likewise extends through the substrate and is *disposed into at least a portion of the pixel*:



Dec., ¶333.

Yamashita's sidewall of trench 33 is a *peripheral sidewall* extending at least substantially around the pixel periphery. Yamashita teaches device isolation insulation film 408 is formed by filling trench 33 with "an insulative material, such as a silicon oxide film." Yamashita, [0104], [0102], Figures 11-12. Film 408 (i.e., filled trench 33) "is disposed in a **lattice shape**...to **surround the unit pixels 1** in the row direction and column direction." Yamashita, [0076]-[0077], [0084], [0092], [0095], [0104], [0116], Figure 4.



Dec., ¶334. Because film 408, comprising trench 33 that in turn comprises trench wall (*sidewall*), completely surrounds pixel 1, Yamashita's sidewall is peripheral to the *pixel* and extend[s] substantially around the pixel periphery, per Figure 4. *Id.*

c) Motivation to Combine

A POSITA would have found obvious and been motivated to combine Hong and Yamashita to extend Hong's sidewall of isolation region 203 substantially

around the pixel periphery. Dec., ¶335. A POSITA would have understood and found desirable extending isolation region 203 around each pixel 200 to reduce or eliminate crosstalk and color mixing between pixels in Hong’s pixel array 1100. *Id.* Yamashita expressly motivates the combination, stating “film 408 is continuously formed in a **lattice shape along pixel boundaries** without spacing” so that “light is reflected...with **no leak**.” *Yamashita*, [0095], [0104].

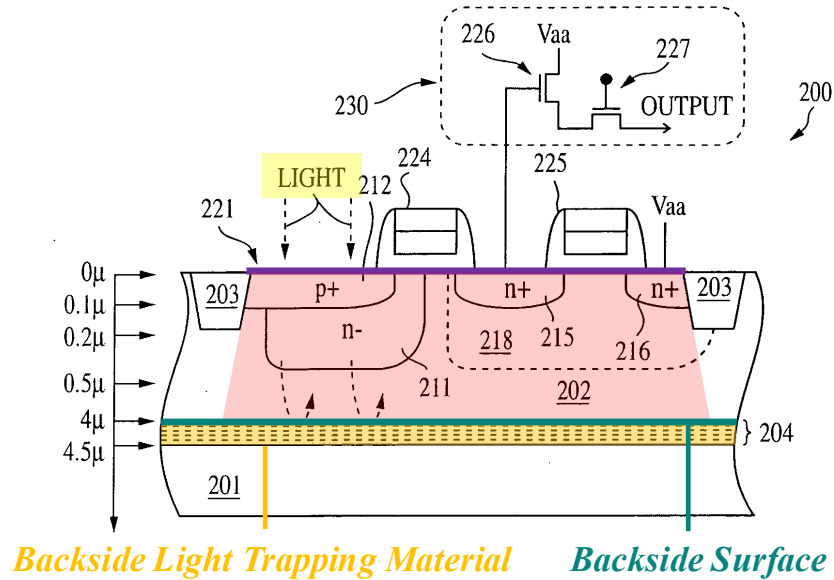
The modification entails using a known technique (etching a trench in a substrate around the pixel periphery) to improve similar devices (improving Hong’s image sensor performance) in the same way (reducing crosstalk). *Id.*

The modification would have a REOS. Both Hong and Yamashita comprise analogous trench isolation structures with *peripheral sidewalls disposed into the pixel*, making the combination straightforward and within a POSITA’s expertise. *Dec.*, ¶¶336-338.

5. 1[b]

Hong teaches or suggests a **backside light trapping material**, namely “reflective layer 204 [that] is illustratively a Distributed Bragg Reflector (DBR) mirror including sub-layers...” *Hong*, [0023], Figures 2-3; Claim 1[a][i], §XII.A.3. Like the ’764 Patent, Hong’s “reflective layer 204 has a (first refractive index sub-layer)/(second refractive index sub-layer) periodic structure.” *Hong*, [0025]; *cf.* ’764 *Patent*, 2:49-54.

Layer 204 (*backside light trapping material*) is *substantially covering the backside surface* (bottom surface of Si layer 202) because “Si layer 202 overlies a reflective layer 204”:



Dec., ¶341; Hong, [0023].

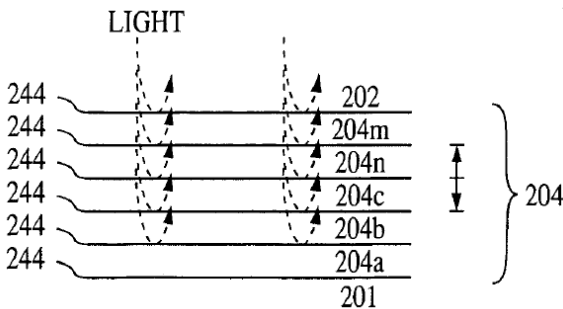


FIG. 3

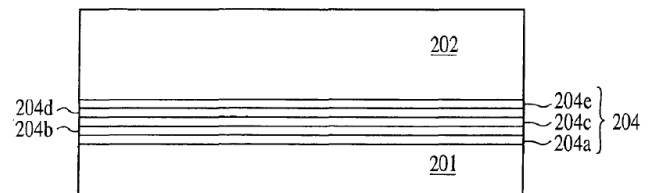


FIG. 5

Hong, Figures 3,5 (illustrating layer 204 (including sublayers) covering the bottom surface of Si layer 202). Dec., ¶¶339-340.

6. 1[c]

In the combination, Hong-Yamashita is combined with Hwang-584, where Hong's peripheral sidewall of trench is modified to include a *peripheral light trapping material substantially covering the peripheral sidewall*, per Hwang-584.

a) Hwang-584's Teachings

Like Hong, Hwang-584 teaches a *peripheral sidewall*, namely a "side wall[]" of trench 350. *Hwang-584*, [0024], [0035]-[0036], [0050]⁵, Figure 5B. Hwang-584 teaches Claim 1[c], namely "device separation membrane 300 comprising a silicon dioxide membrane 320 and a silicon membrane 340." *Hwang-584*, [0025], [0020], [0035]-[0037], Figures 2-3a; *Dec.*, ¶¶343-345.

Trench 350 is formed on p-type epitaxial layer 200, which is an element of Hwang-584's *pixel* because "photodiodes (400) [are] formed on the epitaxial layer (200)" and photodiode 400 "photoelectric[ally] transform[s]" light. *Hwang-584*, [0009], [0014], [0016], [0019], [0035].

Separation membrane 300 comprises membranes 320, 340 forming "3 layers of membrane" alternating "materials having different refractive indices[.]" *Hwang-584*, [0020]-[0021], [0024], Figures 5b-5d. Membrane 320 "is formed by first forming a trench on the epitaxial layer and depositing...(SiO₂) on the bottom surface

⁵ Petitioners added paragraph numbers to Hwang-584 for ease of reference.

and **side walls of the trench.**” *Hwang-584*, [0024], [0036]. Membrane 340 is formed when “silicon is charged into the trench where the [SiO₂] membrane (320) is formed[.]” *Hwang-584*, [0037]. As shown in Figures 5b-5d, below, membrane 300 *substantially cover[s] the peripheral sidewall* (sidewall of trench 350):

Figure 5b

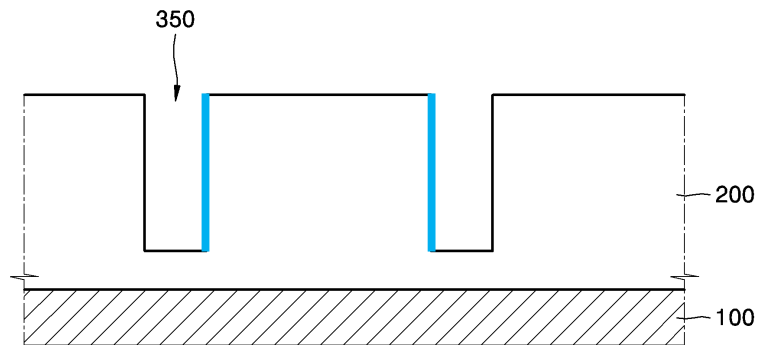


Figure 5c

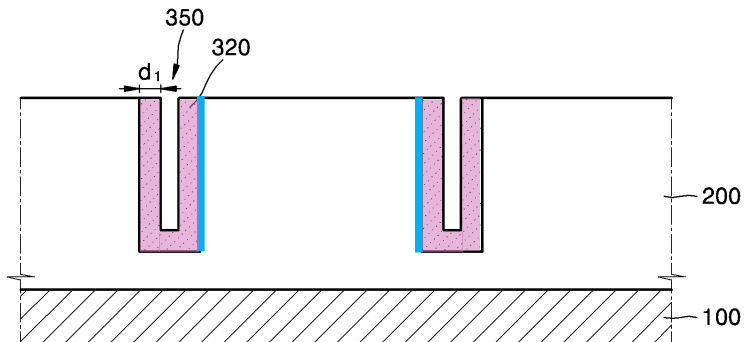
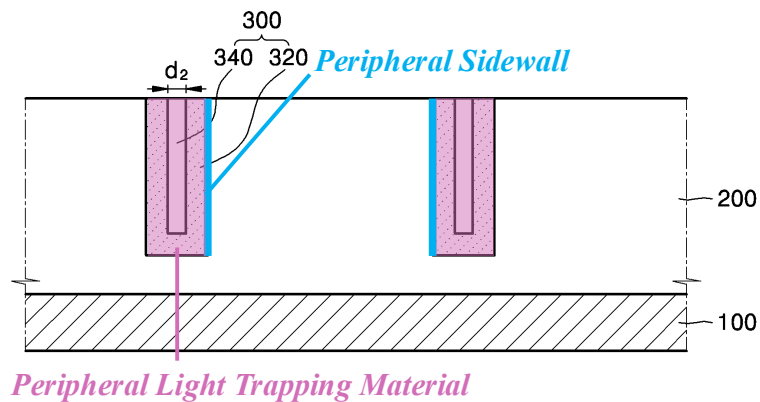
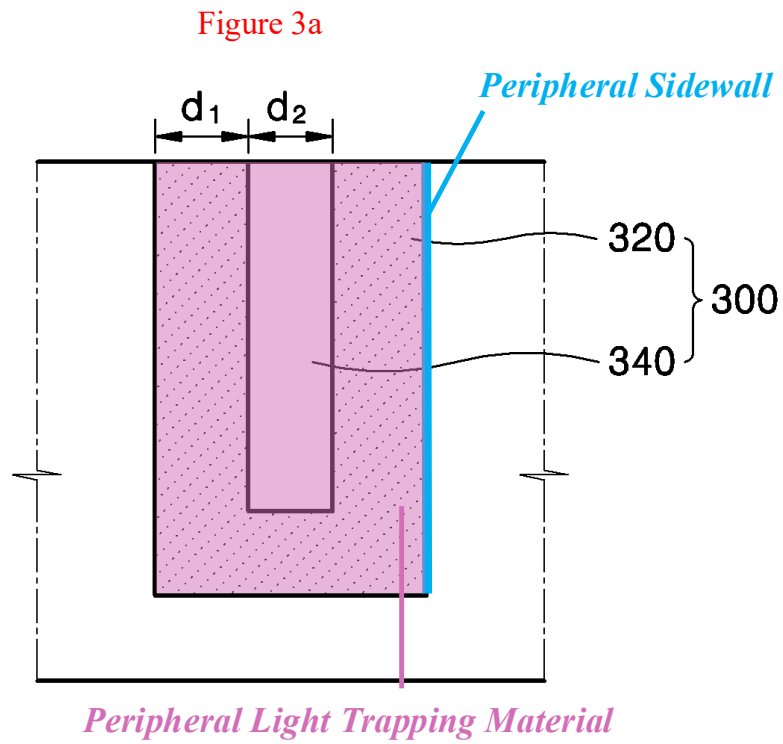
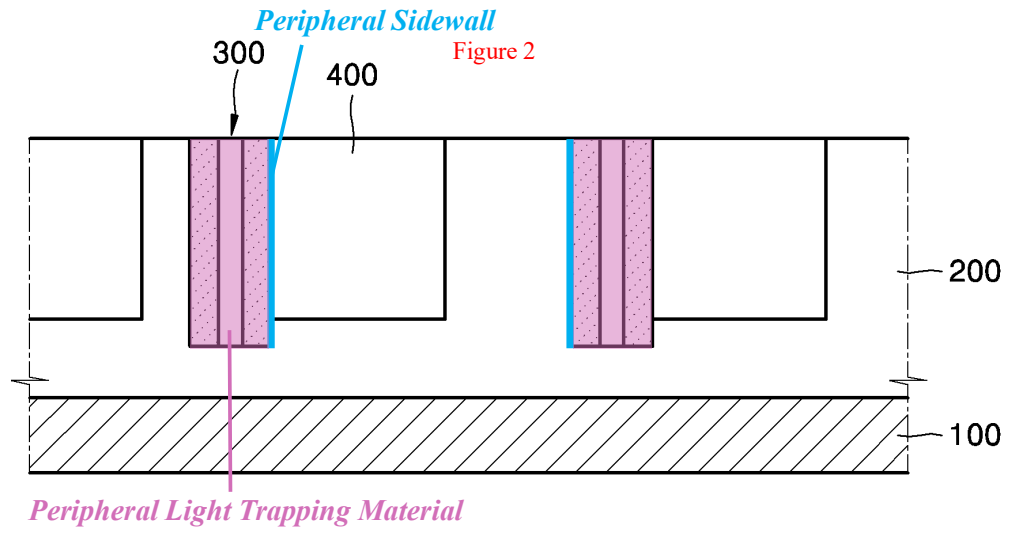


Figure 5d



Dec., ¶346.

Separation membrane 300 is *light trapping* because the difference in the refractive index between membranes 320, 340 raises “the **reflectance** of the device separation membrane...to **block** permeation of side light from entering into an adjacent pixel.” *Hwang-584*, [0020], [0029]-[0031], Figure 4a; *cf.* ’764 Patent, 10:67–11:5; Dec., ¶349. Further, “device separation membranes (300) [] **structurally separate** each active region[.]” *Hwang-584*, [0019]. Thus, separation membrane 300 operates to *trap light* within Hwang-584’s *pixel*. Dec., ¶349.



Dec., ¶¶347-348.

b) Motivation to Combine

A POSITA would have found obvious and been motivated to modify the wall of Hong's trenched isolation region 203 (*peripheral sidewall*) to be *substantially cover[ed]* by Hwang-584's device separation membrane 300 (*peripheral light trapping material*). *Dec.*, ¶¶350-351. In the combination, Hong's trench completely peripherally surrounds the pixel, per Yamashita (Claim 1[a][ii], §XII.A.4).

Hwang-584 expressly motivates the combination, discussing the benefit of “reflect[ing] most of [the] long wavelength[s] of light” back into pixel 200. *Hwang-584*, [0032], [0020], [0025]; *Dec.*, ¶351. Having “different materials having different refractive indices” in isolation trench 203 (thus *covering the peripheral sidewall*) would have greater reflectivity than Hong's singular “dielectric material.” *Id.*; *Hong*, [0033]; *Dec.*, ¶352. The modification is a simple combination of prior art elements (a peripheral sidewall surrounding a pixel and materials having different refractive indices) to yield predictable results (improved entrapment of light within a pixel). *Dec.*, ¶353.

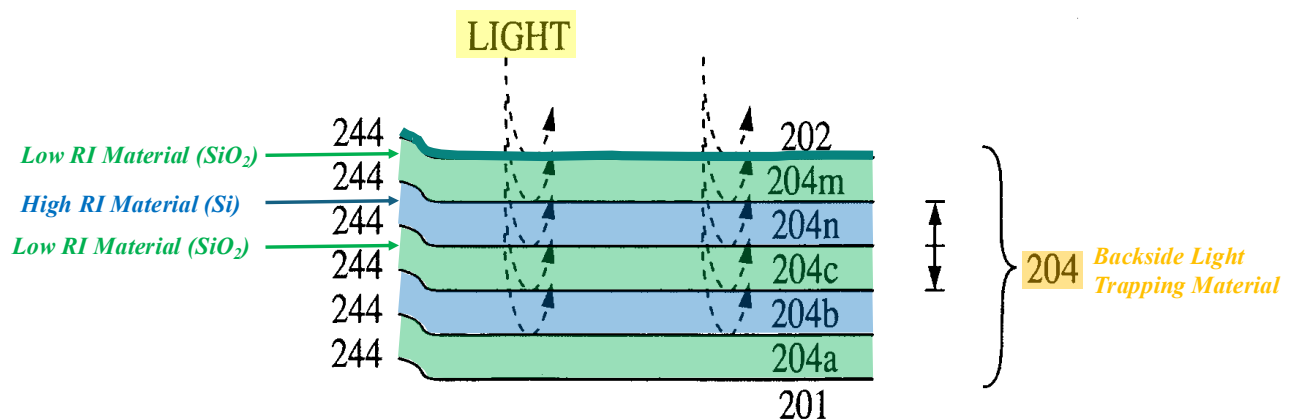
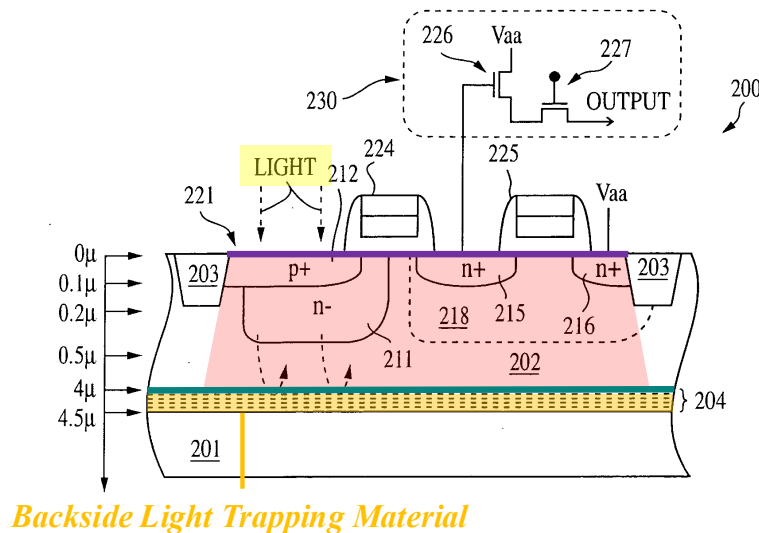
The combination would have a REOS given a POSITA would know how to form a trench and deposit the layered materials on the peripheral sidewall, as disclosed in Hwang-584. *Hwang-584*, [0023]-[0024]; *Dec.*, ¶¶354-355. Further, Hong's trenched isolation element 203 is originally filled with the same material used for Hwang-584's membrane 320 (SiO₂). Therefore, the combination would

have only required “filling silicon (Si) between” silicon dioxide, which is already present in isolation element 203. *Hwang-584*, [0024], Figure 3a; *Dec.*, ¶¶354-355.

7. 1[c][i]

a) Hong’s Backside Light Trapping Material

Hong’s *backside light trapping material* (layer 204) meets Claim 1[c][i].



Dec., ¶¶357-358.

Hong’s layer 204 comprises alternating layers of low/high refractive index materials to form a *sandwich*[] that “is illustratively a Distributed Bragg Reflector

(DBR) mirror[.]” *Hong*, [0023]; *Dec.*, ¶358. *Hong*’s “layer 204 can be formed having an SiO₂/Si structure. In such a case sub-layers 204*a*, 204*c*, and 204*m* are SiO₂ sub-layers and sub-layers 204*b* and 204*n* are Si sub-layers.” *Hong*, [0031]. “Therefore, each sub-layer 204*a-m* is in contact with material having a **different refractive index** to form a (first refractive index layer)/(second refractive index layer)” “periodic structure.” *Hong*, [0023], [0031], Figures 2-3; *cf.* ’764 *Patent*, 8:64–9:1. *Hong* thus teaches a *sandwich*[/] of one material having a first refractive index sandwiched between two materials having a second refractive index. *Dec.*, ¶358.

Additionally, *Hong* expressly teaches the sub-layers include materials of high/low refractive indexes because one layer has a “first refractive index” “different” from a “second refractive index.” *Hong*, [0023]. Applying common sense, if one layer is a first refractive index and another layer is a second, different refractive index, then one layer is a higher refractive index than the other. *Dec.*, ¶359. Because *Hong* describes layers alternating between first/second refractive indexes, *Hong* further teaches a *high* refractive index material sandwiched between two *low* refractive index materials, regardless of whether the first material is the low or high-refractive index material. *Id.*

Additionally or alternatively, *Hong* alone teaches or suggests the claimed high/low refractive indexes or such would be obvious based on the knowledge of a

POSITA because Hong teaches the sub-layers are a “SiO₂/Si structure.” *Hong*, [0031]; *Dec.*, ¶360. Although Hong is silent to the refractive indexes for SiO₂ and Si, a POSITA would have known such refractive indexes. *Dec.*, ¶360. A POSITA would have known from at least Hwang-584 that SiO₂ (silicon dioxide) layer has a refractive index of “around 1.46” and Si (silicon) layer has a refractive index of “around 3.7 to 5.7 depending on the wavelength” of incident light. *Hwang-584*, [0025]; *Dec.*, ¶360. Therefore, Hong alone teaches or suggests the refractive indexes of its high refractive index material (Si) and low refractive index material (SiO₂) or such would be obvious based on the knowledge of a POSITA as evidenced by at least Hwang-584. *Dec.*, ¶360.

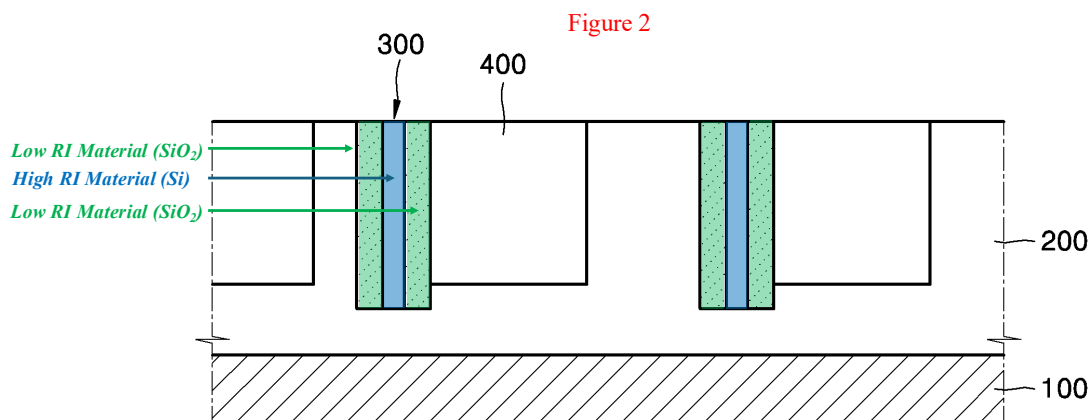
To the extent SiOnyx argues Hong does not teach or suggest the claimed high/low refractive indexes or such would not be obvious to a POSITA based on the POSITA’s knowledge, it would have been obvious to use Hwang-584’s high refractive index material (Si) sandwiched between two low refractive index materials (SiO₂) in Hong’s similar sandwich of SiO₂/Si layers. *Dec.*, ¶361. Both Hong and Hwang-584 teach a sandwich of periodic high/low refractive index layers (including alternating layers of SiO₂ and Si). Therefore, it would be obvious to use the periodic SiO₂/Si layers taught in Hwang-584 in Hong for achieving the specific refractive indexes with a low-high-low sandwich. *Id.* There would be a REOS because the refractive index of the same materials in Hwang-584’s separation

membrane 300 (for deposition on a peripheral sidewall) would have the same refractive index when used in Hong's layer 204 (*backside light trapping material*). *Id.* (noting the refractive indexes of the utilized materials would be the same when applied in Hwang-584 or Hong); §XII.A.6.

b) Hwang-584's Peripheral Light Trapping Material

Hwang-584's device separation membrane 300 is a *peripheral light trapping material*.

Hwang-584's *peripheral light trapping material* (comprising layers of silicon dioxide membrane 320 and silicon membrane 340) is a *sandwich* because silicon layer 340 is "formed" "between" layers of silicon dioxide 320. *Hwang-584*, [0024]. Membranes 320, 340 are "two different materials having different refractive indices[.]" *Hwang-584*, [0020], [0032].



Dec., ¶362.

Hwang-584 teaches "silicon dioxide's refractive index is around 1.46, whereas that of silicon is around 3.7 to 5.7 depending on the wavelength. Therefore,

the difference between the refractive indices is 2.2 or more, allowing high reflectance in a device separation membrane (300)...” *Hwang-584*, [0025], Figure 3a. Thus, *Hwang-584*’s *peripheral light trapping material* (membrane 300 comprising membranes 320, 340) *includes a high refractive index material* (membrane 340’s silicon having a refractive index of at least around 3.7) *sandwiched between two low refractive index materials* (layers of membrane 320 on either side of membrane 340, where membrane 320’s silicon dioxide has a refractive index of around 1.46). *Dec.*, ¶362.

8. 1[c][ii]

Claim 1[c][ii] includes mappings for the low refractive index material for both the *peripheral light trapping material* and the *backside light trapping material*.

a) Peripheral Light Trapping Material: Hwang-795’s Teachings

See Claim 1[c][ii], §V.A.8.a mapping *Hwang-795*’s teachings. *Dec.*, ¶364.

A POSITA would have found obvious and been motivated to dope *Hwang-584*’s silicon dioxide membrane 320 (*one of the two low refractive index materials*) in the *peripheral light trapping material* of the *Hong-Yamashita-Hwang-584* combination with boron, per *Hwang-795*, to *create a surface field* and “significantly improve the performance of the image sensor.” *Hwang-795*, [0036]. *Dec.*, ¶365. Specifically, a surface field forms at the interface between the p⁺ BSG dopant in trench 203 and p-type silicon 202 due to the dopant concentration gradient. *Dec.*,

¶365. Hwang-795 expressly motivates doping Hwang-584's silicon dioxide membrane 320 with boron to improve a pixel's "charge transfer efficiency" and "minimize...dark current[.]" *Hwang-795*, [0015], [0029]-[0030], [0036]; *Dec.*, ¶366. A POSITA would have recognized the formation of the "channel stop region" and resulting electric field created at the interface with semiconductor layer 202 (*surface field*) after heating doped silicon dioxide membrane 320 in Hong's image sensor would have further decreased electrical crosstalk and "increase[d] the photosensitivity" of image sensor 1100. *Hwang-795*, [0009], [0017]-[0018], [0028]; *Dec.*, ¶¶367-368.

The modification entails using a known technique (depositing BSG in a trench) to improve similar pixels in the same way (decreased electrical crosstalk and improved photosensitivity for better pixel performance). *Dec.*, ¶368.

The modification would have a REOS given BSG is a well-known material and the deposition techniques are within a POSITA's expertise. *Dec.*, ¶369.

b) Backside Light Trapping Material: Kaes's Teachings

See Claim 1[c][ii], §V.A.8.b mapping Kaes's teachings. *Dec.*, ¶370.

A POSITA would have found obvious and been motivated to dope Hong's layer 204m comprising silicon dioxide (*one of the two low refractive index materials*) in the *backside light trapping material* of the Hong-Yamashita-Hwang-584-Hwang-795 combination with boron to *create a surface field* (i.e., back surface

field), per Kaes. *Dec.*, ¶371. Kaes expressly motivates doping SiO₂ layer 204_m in Hong's layer 204 to create a back surface field to "reduce[] back surface recombination[,]" thereby increasing the quantum efficiency of Hong's pixel 200. *Hong*, [0024]; *Kaes*, [0013], [0016]; *Dec.*, ¶371.

The combination is merely the application of a known technique (creating a back surface field) to a known device (image sensor) ready for improvement to yield a predictable result (increasing quantum efficiency). *Dec.*, ¶372. The modification would have a REOS given methods to dope silicon dioxide with boron were well-known, and diffusion of dopants into silicon was common practice. *Dec.*, ¶372.

9. 1[d]

a) Hong's Backside Light Trapping Material

Hong teaches *light contacting the backside light trapping material* (layer 204) *is reflected back toward the pixel*. "The reflective layer serves to **reflect incident light** not initially absorbed into the photoconversion device, **back to the photo-conversion device**[]," where the photo-conversion device is part of the *pixel*. *Hong*, Abstract, [0006], [0023], Figure 3; *Dec.*, ¶374; Claim 1[b], §XII.A.5.

b) Hwang-584's Peripheral Light Trapping Material

Hwang-584 teaches *light contacting the peripheral light trapping material* (Hwang-584's device separation membrane 300) *is reflected back toward the pixel*. Hwang-584 teaches membrane having two separate membranes of "different refractive indices can **reflect** most of long wavelength of **light**, especially the visible

light range, thereby significantly reducing CT [(crosstalk)] phenomenon[.]” Hwang-584, [0009], [0032], [0020], [0041], [0001], Figure 4a; *Dec.*, ¶375.

In the combination for Claim 1[d], the modified Hong is further modified to include Hwang-584’s *light trapping material*. The motivations to combine Hong-Yamashita-Hwang-584, which specifically discuss reflection of light back toward the pixel, are discussed for Claims 1[a][ii], 1[c] (§§XII.A.4, XII.A.6). *Dec.*, ¶335, ¶¶349-352, ¶376.

B. Claim 2

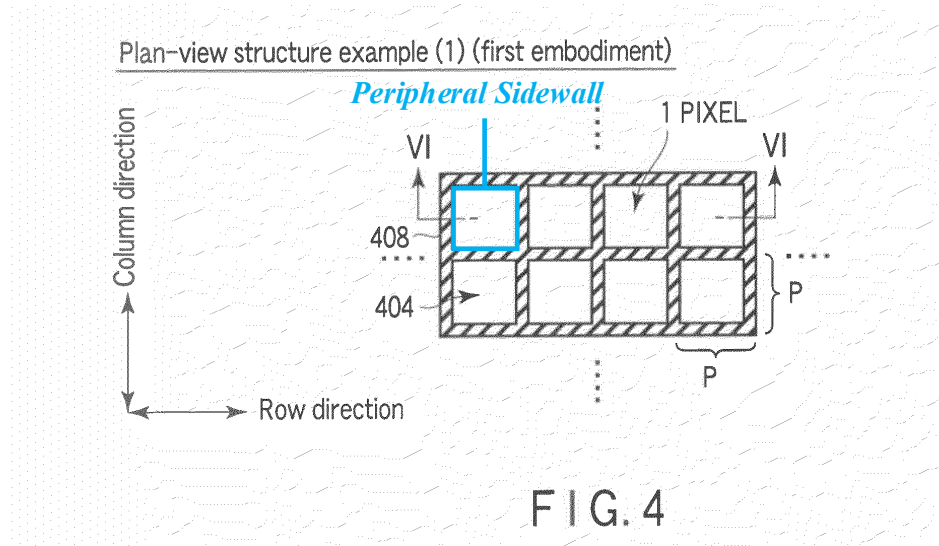
Hong’s layer 204 (i.e., *backside light trapping material*) is Si (i.e., a *high refractive material*) sandwiched between two layers of SiO₂ (i.e., *two low refractive index materials*). See Claim 1[c][i], §XII.A.7. Likewise, the Hong-Yamashita-Hwang-584-Hwang-795-Kaes combination renders obvious a *peripheral light trapping material* including silicon (i.e., a *high refractive material*) sandwiched between two layers of silicon dioxide (i.e., *two low refractive index materials*). *Dec.*, ¶377; see Claim 1[c][i], §XII.A.7.

C. Claim 3

See Claim 1[c][ii], §XII.A.8, wherein the dopant is boron. *Dec.*, ¶378.

D. Claim 4

See Claim 1[a][ii], §XII.A.4, wherein the *peripheral sidewall extends completely around the pixel periphery*, per Yamashita, Figure 4.

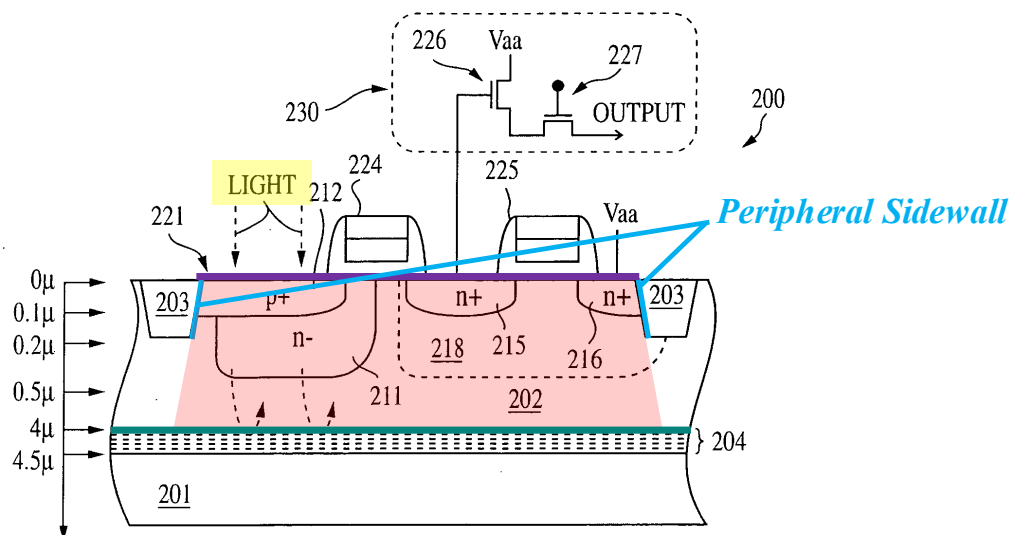


Dec., ¶379.

E. Claim 5

1. Hong's and Yamashita's Teachings

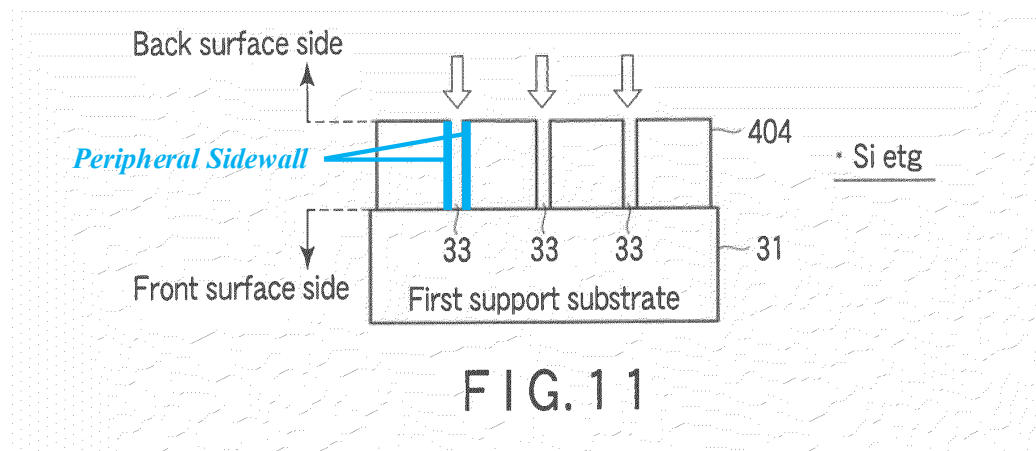
Yamashita combined with Hong's peripheral sidewall teaches Claim 5. Hong teaches a *peripheral sidewall* (wall of isolation region 203).

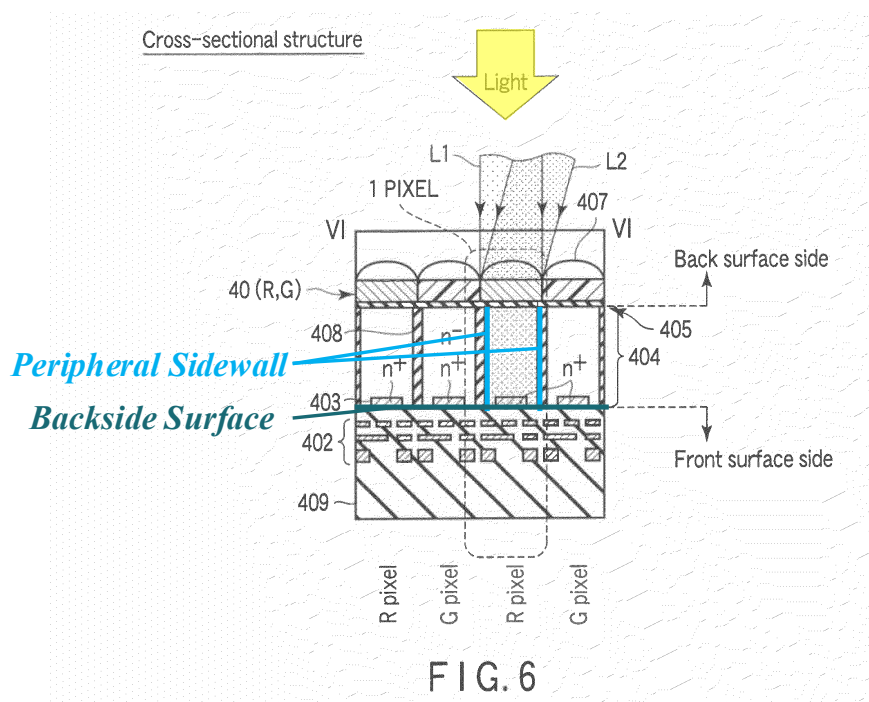


Dec., ¶381; Hong, [0018], [0033]; Claim 1[a][ii], §XII.A.4.a. Hong's wall of isolation region 203 *extends from the light incident surface*, i.e., from the top surface

of semiconductor layer 202 indicated with a purple line in the above Figure 2. *Dec.*, ¶381; Claim 1[a][i], §XII.A.3.

Yamashita similarly discloses a pixel having a *peripheral sidewall*, namely sidewall of trench 33, where trench 33 is filled with an insulative material to form device insulation film 408. Claim 1[a][ii], §XII.A.4.



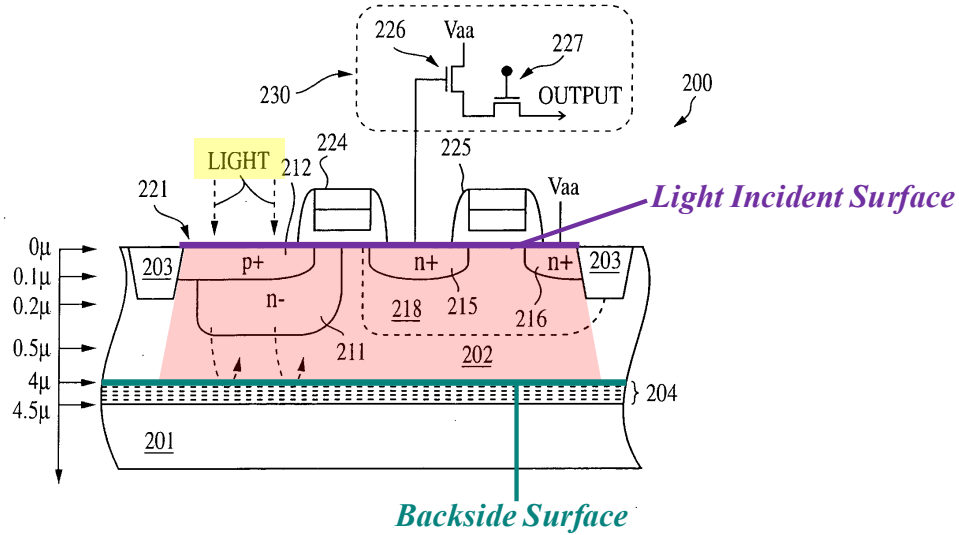


Dec., ¶382.

Yamashita's sidewall of trench 33, which is filled with insulative material to form the film 408 identified in Figure 6, *extends...to the backside surface* of the pixel. *Dec.*, ¶382 (explaining Figure 6's originally-labeled "front surface side" is the *backside surface* of the pixel). Yamashita expressly teaches forming the trench 33, and therefore the trench wall (*peripheral sidewall*), from the surface that is the light-receiving region ("back surface side" in Figure 6) to the opposite surface ("front surface side" in Figure 6). *Dec.*, ¶382. Because the trench is formed "**to the surface**" of substrate 31 (*Yamashita*, [0102]), Yamashita teaches or suggests the trench (and therefore, the trench wall) *extends...to the backside surface*. *Dec.*, ¶383.

2. Motivation to Combine

In the combination, Hong's sidewall of trenched isolation region 203 is modified to extend to Hong's *backside surface*, namely Hong's bottom surface of substrate 202 opposite the light incident surface, per Yamashita. *Dec.*, ¶384. The *light incident* and *backside surfaces* are shown again in Figure 2:



Dec., ¶384; Claim 1[a][ii], §XII.A.4. A POSITA would have found obvious and been motivated to modify Hong’s peripheral sidewall to extend from the light incident surface to the backside surface of Hong, per Yamashita, to prevent when “light enters the neighboring pixel beyond an inter-pixel boundary” “leading to crosstalk and color mixing.” *Yamashita*, [0093]; *Dec.*, ¶385-386.

The modification entails using a known technique (etching a trench sidewall through a substrate) to improve similar devices (improving Hong's pixel performance) in the same way (improved isolation between neighboring pixels).

Dec., ¶385-386.

The modification would have a REOS well within the expertise of a POSITA, at least because Yamashita already teaches methods of forming the sidewall to extend to the backside surface, and sidewalls extending through a pixel were well-known in the art. *Dec.*, ¶387; *Yamashita*, [0098]-[0102], Figure 11.

F. Claim 7

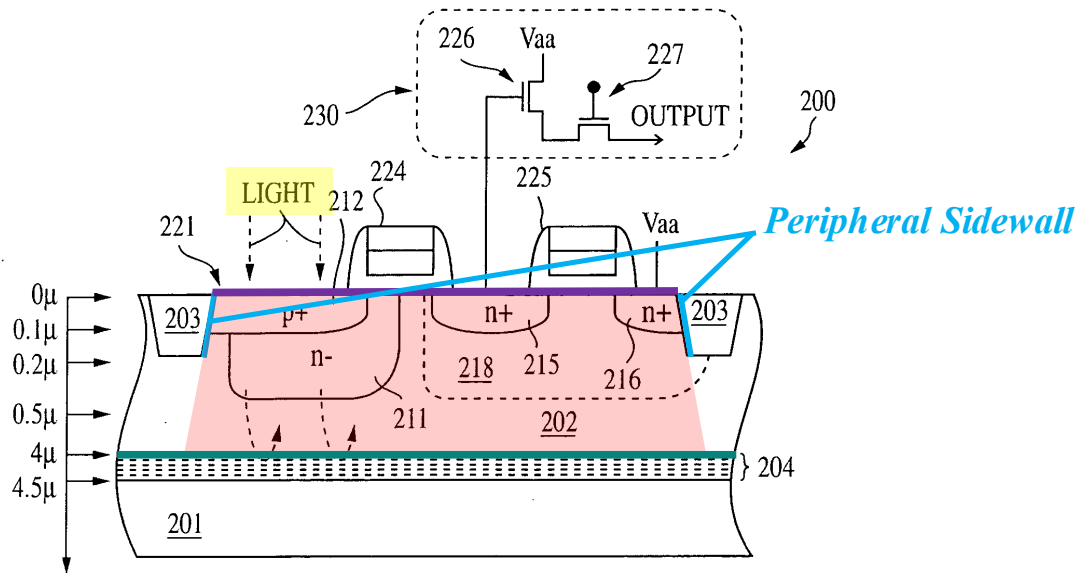
Hong teaches Claim 7. Hong expressly teaches “a pixel array 1111 containing a **plurality of pixel cells** arranged in rows and columns.” *Hong*, [0047]-[0048], Figure 11; *See* Claims 1[Pre], 1[b], §§XII.A.1, XII.A.5 (explaining pixel cells 200 are *light trapping*); *Dec.*, ¶¶388-389. Pixel array 1111 is *[a]n array of light trapping pixel devices*, as Hong’s pixels 200 are *pixel devices* that are light trapping. *Dec.*, ¶390.

XIII. GROUND 9: CLAIM 5 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, HWANG-795, KAES, MOULI

A. Hong’s and Mouli’s Teachings

To the extent SiOnyx contends Yamashita combined with the modified Hong does not teach Claim 5 (§XII.E), Mouli combined with the modified Hong teaches Claim 5.

Hong teaches a *peripheral sidewall* (wall of isolation region 203):



Dec., ¶329; Hong, [0018], [0033]; Claim 1[a][ii], §XII.A.4.

Like Hong, Mouli discloses a pixel having a *peripheral sidewall*, namely sidewalls 210 of trench isolation structure 202. *Mouli*, 3:3-4, 4:10-16, 4:45-53, Abstract, Figures 2, 3A-3C. Like Hong and Yamashita, Mouli's pixel has a *backside surface*, namely a bottom surface of silicon substrate 200. *Mouli*, 3:35-39, 5:32-40.

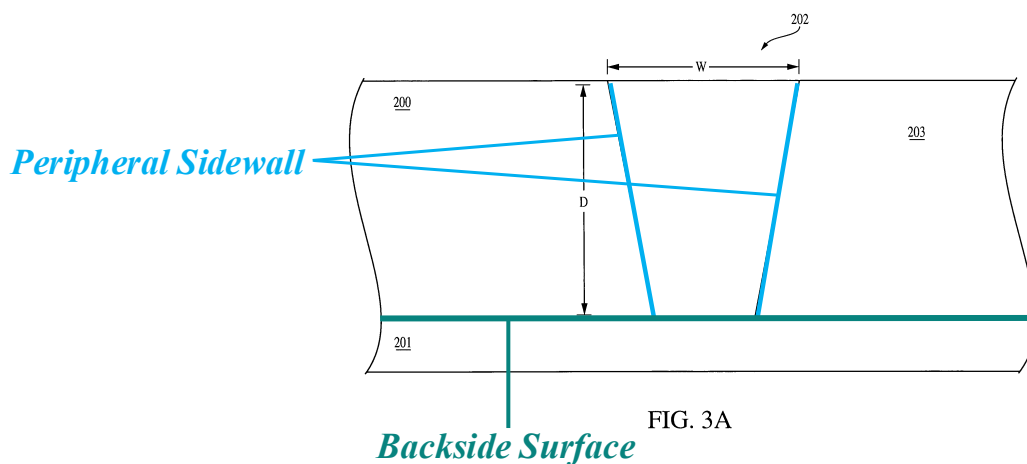


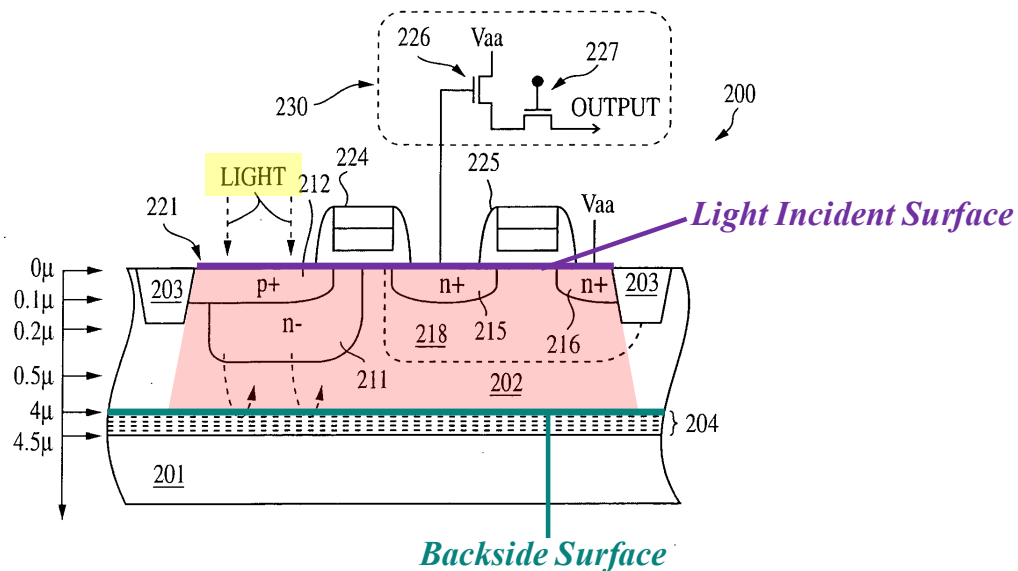
FIG. 3A

Dec., ¶391

Mouli teaches a peripheral sidewall *extend[ing]...to the backside surface* of pixel because (1) Mouli’s sidewall 210 is a sidewall of trench 202; and (2) trench “**extends through the substrate to the base layer**” (*backside surface*) of Mouli’s pixel. *Mouli*, Abstract, 4:15-16 (disclosing trench “extend[s]” to epi layer 201, which is below silicon substrate 200), 5:32-34, 4:45-49, 5:50-59, 8:53-59, 9:40-45, Figures 2, 4; *Dec.*, ¶391.

B. Motivation to Combine

In the combination, Hong's sidewall of trenched isolation region 203 is modified to extend to Hong's *backside surface*, namely Hong's surface of substrate 202 opposite the light incident surface, per Mouli:



Dec., ¶329; Claim 1[a][i], §XII.A.3.

A POSITA would have been motivated and found obvious to further modify Hong-Yamashita-Hwang-584 to similarly etch Hong's isolation region 203 (and the accompanying sidewall) to *extend[]...to the backside surface*, per Mouli. *Dec.*, ¶391. Mouli expressly motivates the combination, stating a “deeper trench better inhibits electrons from diffusing under the isolation trench to an adjacent pixel thereby preventing crosstalk between neighboring pixels.” *Mouli*, 4:17-32, 2:9-10; *Dec.*, ¶¶392-393.

The modification entails using a known technique (etching a deep trench into a substrate, per Mouli) to improve similar devices (improving the performance of Hong's image sensor pixel) in the same way (reducing crosstalk in Hong). *See* §XII.E.2 (providing additional MTC/REOS for etching a deep trench, incorporated herein); *Dec.*, ¶394.

The modification would have a REOS. *Dec.*, ¶394. Mouli informs a POSITA how to make the trench using a “directional etching process, such as Reactive Ion Etching (RIE)[,]” which was well-known. *Mouli*, 5:57-58; *Dec.*, ¶394; *cf.* '764 *Patent*, 7:43-46. Hong and Mouli are also similarly concerned with “photons having long wavelengths.” *Mouli*, 2:45-46; *cf. Hong*, [0005], *with Mouli*, 2:9-14, 2:32-46. Forming trench isolation features in pixels was well-known and thus within the expertise of a POSITA. *Dec.*, ¶394.

XIV. GROUND 10: CLAIM 6 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, HWANG-795, KAES, KONNO

A. Konno's Teachings

See Claim 6, §VI.A, mapping Konno's teachings. *Dec.*, ¶395.

B. Motivation to Combine

A POSITA would have found obvious and been motivated to implement Konno's layer 120 as the *backside light trapping material* in Hong's pixel 200 because "photons are reflected by the mirror surface of the second reflecting layer 120" from inside the pixel back into the pixel to increase "the detection efficiency and efficiency for conversion into electric signals." *Konno*, 1:37-38, 9:67-10:3; *Dec.*, ¶396. A POSITA would have appreciated a *backside light trapping material* comprising a *metal layer* would be reflective against all wavelengths of light, whereas layer 204 is "a highly reflective DBR mirror at a **targeted wavelength**." *Hong*, [0027]; *Dec.*, ¶¶396-397.

There would be a REOS at least because metal was a widely available material and because techniques for depositing a metal layer in an image sensor were very well-known. *Dec.*, ¶¶399-400; *cf.* '764 *Patent*, 7:56-59. The modification includes a simple substitution of one known element for another (a distributed Bragg reflector for a metal layer) to obtain predictable results (a pixel with backside material capable of reflecting unabsorbed photons back into the pixel). *Dec.*, ¶398.

XV. GROUND 11: CLAIMS 8-12, 14-15 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584

A. Claim 8

Limitations 8[Pre]-8[c], 8[d][i] are identical to 1[Pre]-1[c], 1[d]. See §§XII.A.1-XII.A.6, XII.A.9, respectively (incorporated herein). *Dec.*, ¶¶401-406, ¶411.

1. 8[d]

Both Hong's *backside light trapping material* (layer 204) and Hwang-584's *peripheral light trapping material* (membrane 300) in the Hong-Yamashita-Hwang-584 combination teach a *first material* (Si) sandwiched between *two second materials* (SiO₂). See Claim 1[c][i], §XII.A.7; *Dec.*, ¶¶407-408. Further, Both Hong and Hwang-584 teach a *first material* (Si) having a refractive index of at least around 3.7 and *two second materials* (SiO₂) having a refractive index of 1.46 (difference of 2.24, which is *at least 0.2*). See Claim 1[c][i], §XII.A.7; *Dec.*, ¶¶408-410.

B. Claim 9

The refractive index of the mapped *two second materials* (SiO₂) in both the peripheral and backside light trapping materials is around 1.46, which is *less than about 2.1*. Hwang-584, [0025]; *Dec.*, ¶412; Claim 1[c][i], §XII.A.7.

C. Claim 10

The *two second materials* are silicon dioxide, *a member* of the claimed group *oxide*. *Dec.*, ¶413; Hong, [0033]; Claim 1[c][i], §XII.A.7.

D. Claim 11

The *two second materials* are silicon dioxide, a member of the *silicon oxide* group. *Dec.*, ¶414; Claim 1[c][i], §XII.A.7.

E. Claim 12

The *first material* for both the backside and peripheral light trapping materials is silicon with a refractive index of at least 3.7, which is *greater than or equal to about 2.1*. *Hwang-584*, [0025]; *Dec.*, ¶415; Claim 1[c][i], §XII.A.7.

F. Claim 14

See Claim 4, §XII.D. *Dec.*, ¶416.

G. Claim 15

See Claim 5, §XII.E. *Dec.*, ¶417.

XVI. GROUND 12: CLAIM 13 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, KOMURO

Hong-Yamashita-Hwang-584's *first material* is silicon with a refractive index of "around 3.7 to 5.7 depending on the wavelength." *Hwang-584*, [0025].

A. Komuro's Teachings

See Claim 13, §VIII mapping Hwang-099's and Komuro's teachings (incorporated herein).

TABLE 1

	Refractive Index (n)			Extinction Coefficient (k)		
	Blue Light 450 nm	Green Light 550 nm	Red Light 650 nm	Blue Light 450 nm	Green Light 550 nm	Red Light 650 nm
Germanium	4.5	6.0	5.5	2.3	2.1	1
Silicon	4.69	4.08	3.85	0.151	0.03	0.017
Tungsten	3.31	3.48	3.76	2.47	2.72	2.95
Plasma Silicon Nitride	2.07	2.04	2.01	0.004	0	0.002
Aluminum	0.618	0.958	1.47	5.47	6.69	7.79
Copper	1.17	0.9	0.21	2.39	2.6	3.67
Reference: Silicon Dioxide	1.45	1.45	1.45	0.00	0.00	0.00

Komura, Table 1. *Dec.*, ¶418.

B. Motivation to Combine

A POSITA would have found obvious and been motivated to implement Hong-Yamashita-Hwang-584's *first material* as “any one of single crystal silicon, amorphous silicon, and polysilicon” because each possesses a refractive index from 3.85 to 4.69 dependent on wavelength (i.e., “around 3.7 to 5.7 depending on the wavelength,” per Hwang-584's refractive index for silicon). *Komuro*, [0137]-[0138]; *Dec.*, ¶¶419-422; Claim 13, §VIII.C (incorporating MTC/REOS).

XVII.GROUND 13: CLAIMS 17-19 ARE OBVIOUS OVER HONG, YAMASHITA, AND HWANG-584 IN COMBINATION WITH MOULI AND/OR NOZAKI

A. Claim 17

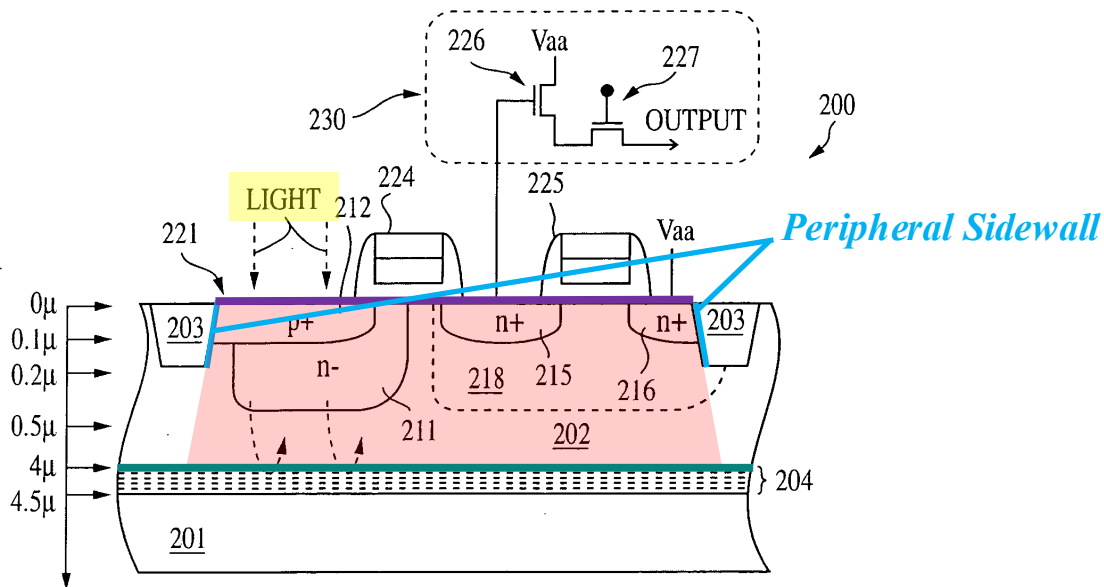
Limitations 17[Pre]-17[c], 17[c][ii] are identical to 1[Pre]-1[c], 1[d]. *See* §§XII.A.1-XII.A.6, XII.A.9 (incorporated herein); *Dec.*, ¶¶423-428, ¶437.

1. 17[c][i]

Mouli teaches a sloped trench wall associated with the *peripheral light trapping material*; Nozaki teaches a sloped backside surface associated with the *backside light trapping material*. Therefore, the proposed grounds render obvious both the *backside light trapping material* and the *peripheral light tapping material* having a sloped surface.

a) Hong's Sloped Trench Wall

Hong teaches a sloped trench wall; in the modified Hong combining Hwang-584's peripheral light trapping material, the material has a *sloped surface at the pixel device interface*:



Dec., ¶¶429-430; Claims 1[a][ii], 1[c], §§XII.A.4, XII.A.6.

b) Mouli's Sloped Trench Wall

To the extent SiOnyx contends Hong-Yamashita-Hwang-584 does not each Claim 17[c][i], Mouli also teaches sloped sidewalls, namely “high **conical** sidewalls....” *Mouli*, 5:16-18.

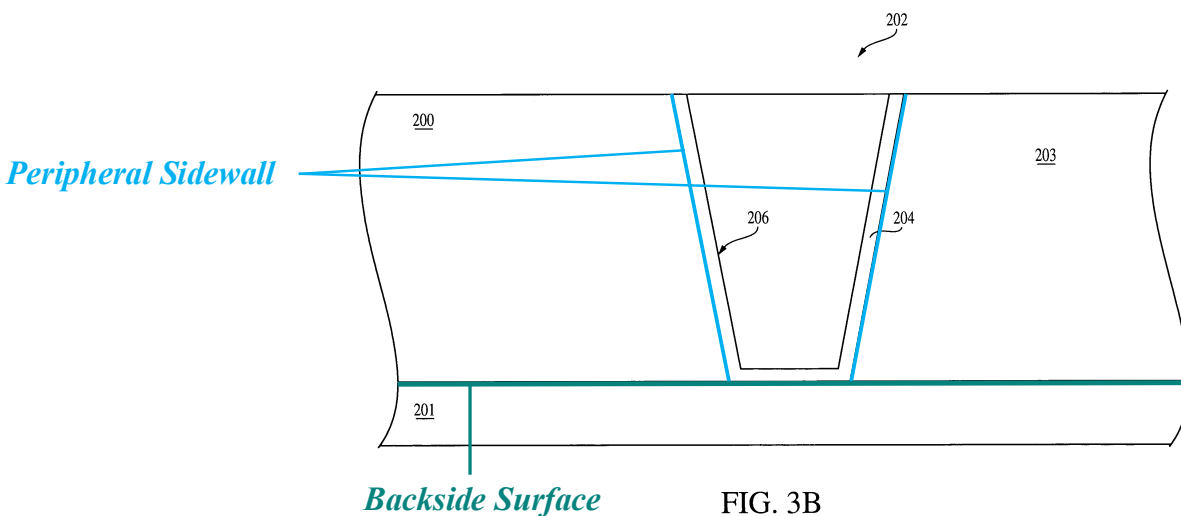


FIG. 3B

Dec., ¶431; §IX.A.1.a.

For the reasons provided in §IX.A.1.a, a POSITA would have similarly been motivated to modify Hong to have sloped sidewalls, to the extent not otherwise taught in Hong, such that the peripheral light trapping material deposited on the sidewall, per the modification with Hwang-584, had a *sloped surface*. *Dec.*, ¶431.

c) Nozaki's Sloped Backside Surface

Regarding the *backside light trapping material* having a *sloped surface*, see Claim 17[c][i], §IX.A.1.b, mapping Nozaki's teachings and MTC/REOS (incorporated herein). For the reasons provided in §IX.A.1.b, a POSITA would have similarly been motivated to modify Hong's *backside light trapping material* (layer 204), to achieve “multiple angles of reflection....” *Nozaki*, [0027], [0019]; *Dec.*, ¶¶432-433.

The modification would have a REOS, at least because Hong and Nozaki disclose methods for forming backside light trapping materials (layer 204; Claim 1[b], §XII.A.5) and concave-shaped surfaces, respectively. Methods of providing sloped backside surfaces in pixels were well-known. *Dec.*, ¶433-434; *Hong*, [0023]-[0025], [0030]-[0031]; *Nozaki*, [0034]-[0037].

d) Obviousness of Combining Both Mouli and Nozaki

Petitioners incorporate the MTC/REOS for Claim 17[c][i], §IX.A.1.c modifying both Hong's backside surface (and commensurately, backside light trapping material on the backside surface) and peripheral sidewall (and

commensurately, the peripheral light trapping material on the peripheral wall) to have a sloped surface, as the modification would have simply entailed combining the individual sloped surfaces and motivations discussed above, with the commensurate benefits and REOS. *Dec.*, ¶¶435-436.

B. Claim 18

See Claim 4, §XII.D. *Dec.*, ¶438.

C. Claim 19

See Claim 5, §§XII.E, XIII. *Dec.*, ¶439.

XVIII. GROUND 14: CLAIM 20 IS OBVIOUS OVER HONG, YAMASHITA, HWANG-584, MOULI AND/OR NOZAKI IN FURTHER VIEW OF KONNO

A. Konno's Teachings

Konno teaches a *metal layer* as a *backside light trapping material*. *See* Claim 6, §XIV. *Dec.*, ¶440.

B. Motivation to Combine

See Claim 6, §XIV (MTC/REOS incorporated herein) explaining why a POSITA would have been motivated to modify Hong's layer 204 (*backside light trapping material*) to be a *metal layer*, per Konno. *Dec.*, ¶440.

XIX. GROUND 15: CLAIMS 16, 21-25 ARE OBVIOUS OVER HONG, YAMASHITA, HWANG-584, KONNO

A. Claim 16

1. Konno's Teachings

Konno teaches a *metal layer* as a *backside light trapping material*. See Claim 6, §XIV. *Dec.*, ¶441.

2. Motivation to Combine

See Claim 6, §XIV (MTC/REOS incorporated herein) explaining why a POSITA would have been motivated to modify Hong's layer 204 (*backside light trapping material*) to be a *metal layer*, per Konno. *Dec.*, ¶441.

B. Claim 21

Petitioners provide two alternative mappings for Claim 21, both relying on a combination of Hong-Yamashita-Hwang-584 and Konno. The first (i.e., following) Claim 21 mapping modifies Hong-Yamashita-Hwang-584 to include Konno's textured transparent layer 36 depicted in the embodiment of Figure 7. Limitations 21[Pre]-21[c], 21[d][i] are identical to 1[Pre]-1[c], 1[d]. See §§XII.A.1-XII.A.6, XII.A.9, respectively (incorporated herein); *Dec.*, ¶443-448, ¶457.

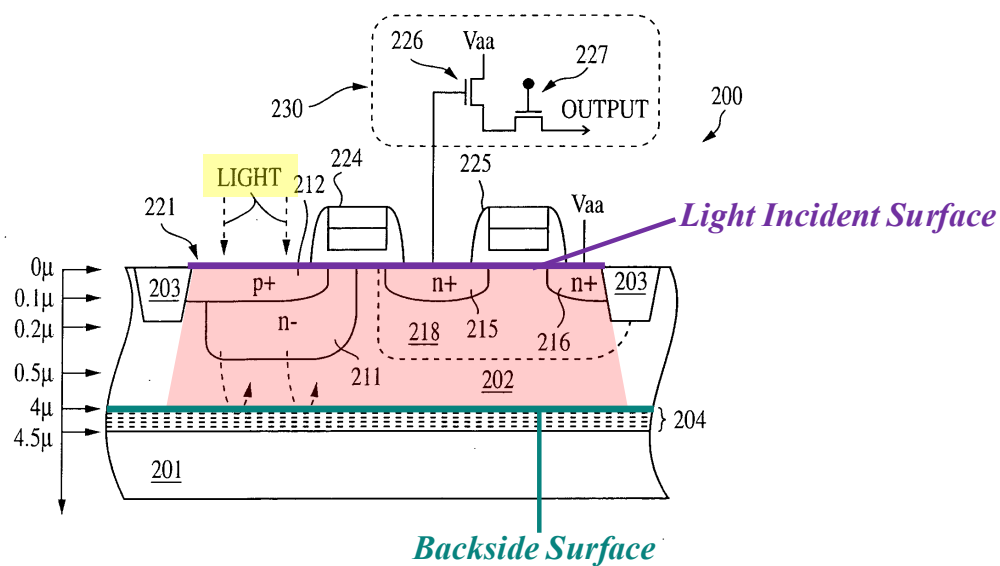
1. 21[d]

a) Konno's Teachings

See §XI.B.1.a mapping Konno's teachings. *Dec.*, ¶449.

b) Motivation to Combine

Regarding a textured layer positioned to interact with light proximal to the backside surface, see Hwang-099 Claim 21[d], §§XI.B.1.a-XI.B.1.b, mapping Konno's teachings and MTC/REOS (incorporated herein). For the reasons provided in §XI.B.1.b, a POSITA would have similarly found obvious and been motivated to modify the Hong-Yamashita-Hwang-584-Konno combination to include transparent layer 136 underneath the *backside surface* of Hong's pixel and on top of layer 204 (*backside light trapping material*). Hong, Figure 2.



Dec. ¶451.

In the combination, transparent layer 136 (*textured layer*) is positioned to interact with light proximal to the *backside surface* because transparent layer 136 is between the backside surface and backside light trapping material. Dec., ¶450-451.

In the modification, a POSITA would have appreciated providing a textured layer on the backside surface would have enhanced internal reflection of incident light within Hong's pixel (e.g., by increasing the path length of light and increasing the range of angles that light reflects back into the pixel), thus improving quantum efficiency. *Dec.*, ¶¶452-453, ¶456. The modification would have a REOS at least because it only requires depositing Konno's transparent layer 136 on the backside surface of Hong prior to the formation of layer 204. *Dec.*, ¶¶454-456.

C. Claim 21

Limitations 21[Pre]-21[a][ii], 21[c] are identical to 1[Pre]-1[a][ii], 1[c]. *See* §§XII.A.1-XII.A.4, XII.A.6, respectively (incorporated herein); *Dec.*, ¶¶463-466, ¶470.

1. Explanation of Combination and Motivation for the Combination

The following mapping of Claim 21 relies on Hong-Yamashita-Hwang-584-Konno. In the combination, Hong's layer 204 (*backside light trapping material*) is replaced with Konno's combined metal layer 120 and textured transparent layer 136 in the embodiment depicted in Figure 7. Like the Hwang-099-Konno combination (§XI.C), a POSITA would have similarly found obvious and been motivated to replace Hong's layer 204 with Konno's combined metal reflecting layer 120 and textured transparent layer 136. *See* §XI.C; *Dec.*, ¶458.

A POSITA would have been motivated to implement Konno's textured layer 120 due to the advantages of having a metal backside light trapping material discussed previously (e.g., broadband reflectivity). *See* Claim 6, §XIV; *Dec.*, ¶459. A POSITA would have also appreciated Konno's textured metal layer, like textured layers generally, would reflect light diffusely versus specularly to improve light absorption and sensitivity of image sensor 1100. *See* Claim 21[d], §XI.B.1; *Dec.*, ¶¶459-461.

Further, a POSITA would recognize modifying Hong-Yamashita-Hwang-584-Konno to include both transparent layer 136 and reflecting layer 120 would provide the benefits of a textured metal layer without physically texturing the surface of Hong's *pixel*. *Dec.*, ¶461. Additionally, having a textured transparent layer between the backside surface and layer 120 would prevent diffusion of metal into the pixel, which would "adversely affect the photoresponsive characteristics[.]" *Dec.*, ¶461.

Thus, a POSITA would have been motivated to replace Hong's layer 204 with Konno's combined transparent layer 136 and layer 120. *Dec.*, ¶¶460-461. In the combination, transparent layer 136 is the ***textured layer***, as recited by Claim 21[d], layer 120 is the ***backside light trapping material***, as recited by Claim 21[b].

The modification is the combination of prior art elements (textured layer, metal backside layer) using known methods (microlithographic texturing, material

deposition) to obtain predictable results (improved reflectivity of light). *Dec.*, ¶462. The modification would have a REOS because metal was a widely available material and methods for texturing materials were well-known and further taught by Konno. *Dec.*, ¶462.

2. 21[b]

a) Hong's Teachings

See Claim 1[b], §XII.A.5 mapping Hong's teachings. *Dec.*, ¶467.

b) Konno's Teachings

See §XI.C.2.b mapping Konno's teachings. In the Hong-Yamashita-Hwang-584-Konno combination for Claim 21, Hong's backside light trapping material comprising layer 204 is replaced with Konno's backside light trapping material comprising reflecting layer 120 as shown in Konno, Figure 7. *Dec.*, ¶468. Thus, Hong's *backside surface* is *substantially covered* by Konno's *backside light trapping material*.

c) Motivation to Combine

See Claim 21, §XIX.C.1. *Dec.*, ¶469.

3. 21[d]

a) Konno's Teachings

See §XI.C.3.a mapping Konno's teachings. *Dec.*, ¶471.

b) Motivation to Combine

See Claim 21, §XIX.C.1. *Dec.*, ¶472.

4. 21[d][i]

a) Hong's Teachings

Hong alone teaches *light contacting the peripheral light trapping material* (layer 204) *is reflected back toward the pixel*. See Claim 1[d], §XII.A.9; Dec., ¶473.

b) Konno's Teachings

Additionally or alternatively, Konno teaches *light contacting the backside light trapping material* (layer 120) *is reflected back toward the pixel*. Konno expressly teaches layer 120 “**reflects** incident photons 132,” and the “plurality of convexes and concaves on the reflecting surface” of layer 120 “can **reflect** them [(photons 132)] with a large reflection angle” toward photoelectric conversion element 135. *Konno*, 13:63-66; 14:10-16; Figure 7. In the combination, because layer 120 (*backside light trapping material*) is located underneath Hong's *backside surface*, light contacting it is reflected back up toward the *pixel*. Dec., ¶¶473-475; see §XIX.C.1 (MTC).

D. Claim 22

In both of the above mappings of the combination of Hong-Yamashita-Hwang-584-Konno for Claim 21, because transparent layer 136 (*textured layer*) is located underneath Hong's *backside surface* and above layer 204 (in the first mapping) and layer 120 (in the second mapping), the *textured layer* is located between the *backside surface* and *backside light trapping material*. *Konno*, Figure 7; see Claims 21[b], 21[d], §§XIX.C.2, XIX.C.3; Dec., ¶476.

E. Claim 23

See Claim 4, §XII.D. *Dec.*, ¶477.

F. Claim 24

See Claim 5, §XII.E. *Dec.*, ¶478.

G. Claim 25

In the above combination of Hong-Yamashita-Hwang-584-Konno, layer 120 (*backside light trapping material*) is a *metal layer* because it is formed of “a thin film of metal such as aluminum or silver by deposition.” *See* Claim 21[b], §XIX.C.2; *Konno*, 8:35-38, 11:42-52; *Dec.*, ¶479.

XX. DISCRETIONARY DENIAL

A. General Plastic

General Plastic factor 1 (GP1) outweighs the other factors unless the same petitioner (or petitioner having a significant relationship to that petitioner) previously filed a petition against the same claim(s). *GP*, 4; *Valve*, IPR2019-00062, Paper 11, 9-10; *Videndum*, IPR2023-01218, Paper 12, 6. Samsung is the first petitioner (IPR2025-00161); Apple/Sony is the second.

Apple/Sony began independently preparing this IPR in September 2024 and was not involved with Samsung’s IPR. *fubotv*, IPR2024-00919, Paper 14, 27-28; *Luminex*, IPR2024-00101, Paper 20, 9.

Apple/Sony are not Samsung’s co-defendants. Their respective petitions result from SiOnyx’s litigations. *Ancora*, IPR2021-00663, Paper 17, 10-11.

Sony supplies Samsung and Apple. At the same time, Sony and Samsung offer competing image sensors. SiOnyx accuses Sony's and Samsung's image sensors in Samsung's litigation, but a different Sony (and other suppliers') sensor(s) in Apple's litigation. Exs. 1015, 1016; Ex. 1065, 1-2; Ex. 1017, 1. Thus, Sony has a "strong and independent interest" in invalidating this patent. *Luminex*, 14; *Samsung*, IPR2022-00615, Paper 20, 17-18. Apple has its own interest as a direct competitor of Samsung defending litigation involving different products. *Ford*, IPR2023-00763, Paper 28, 3; *Greenthread*, IPR2024-00551, Paper 26, 10.

Sony is not an exclusive supplier. Thus, Sony has no exclusive relationship with Samsung—there is no proxy relationship. *Luminex*, 11; *WesternGeco*, 889 F.3d at 1321-22.

Sony nor Apple is indemnifying Samsung, nor would that create an RPI/proxy relationship. *Luminex*, IPR2024- 00101, Paper 20, 12-13.

Grounds 8-14 apply art not presented by Samsung. Grounds 1-7 rely on Hwang-099, applied by Samsung, but maps a different embodiment and different secondary references. Regardless, Hwang-099 does not demonstrate copying. *Signify*, IPR2023-00213, Paper 16, n.13; *Theta*, IPR2024-00819, Paper 12, 17; *Ascend*, IPR2024-00948, Paper 10, 32-34.

Consequently, GP1 is unmet, ending the analysis. However, the other factors all favor institution.

GP2: Apple/Sony independently identified Hwang-099 and started preparing this IPR before Samsung's IPR was filed.

GP3: PO has not filed a preliminary response in Samsung's IPR.

GP4-5: Apple/Sony started this Petition after Apple was sued. This technology is complex, and the prior art is extensive. Petitioners know of no case finding 6-7 months an undue delay in filing.

GP6-7: This Petition is not redundant, respecting the Board's finite resources. No roadblocks prevent a timely decision. *Honda*, IPR2018-00348, Paper 10, 19-20.

GP8-9: not applicable, as denial would prejudice Petitioners. *Id.*, 20-21.

B. Advanced Bionics

Advanced Bionics/Becton Dickinson favor institution—*Advanced Bionics* Part 1 is unsatisfied.

The unpatentability bases here are materially different from Samsung's. Grounds 8-14 rely on Hong-Yamashita-Hwang-584-Kaes-Hwang-795 and Ground relies on Hong-Yamashita-Hwang-584-Konno. Grounds 1-7 rely on Hwang-099's Figs. 2, 6 embodiments, while Samsung relies on the Fig. 6 embodiment alone. *Alivecor*, IPR2023-00950, Paper 12, 51.

Although Samsung presented Hwang-099 and Konno, Samsung's IPR remains pending, so none is considered "previously...presented[.]" *Verizon*

Connect, IPR2023-01162, Paper 12, 16-18; *Alivacor*, IPR2023-00950, Paper 12, 51-54.

While some applied references were cited in related patents, none (or Apple/Sony's combinations) were considered during their respective examinations.

C. Fintiv

The parallel district court litigation against Apple only is early; there is no ITC litigation against Apple/Sony. A Scheduling Order was entered in February. No trial date is set. Discovery just commenced. Claim construction has not begun and a hearing is not until November. Dispositive motions are not due until September 2026. (Ex. 1018, 1; Ex. 1019, 15-16). A trial is likely as late as February 2027. (Ex. 1020, 36). Combined with the Petition's strength, *Fintiv* favors institution.

Pursuant to the Office's Interim Process Concerning Institution published March 26, 2025, Petitioners reserve the right to address in further briefing any discretionary denial issues raised by SiOnyx.

XXI. CONCLUSION

Petitioners respectfully request IPR of the Challenged Claims.

Respectfully submitted,

ERISE IP, P.A.

BY: /s/ Jennifer C. Bailey
Jennifer C. Bailey, Reg. No. 52,583

COUNSEL FOR PETITIONER APPLE INC.

SMITH BUCHANAN LLP

BY: /s/ Matthew A. Smith
Matthew A. Smith, Reg. No. 49,003

*COUNSEL FOR PETITIONER SONY
GROUP CORPORATION*

XXII.MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Parties-In-Interest

Petitioners Apple Inc. and Sony Group Corporation are the real parties-in-interest. 37 C.F.R. § 42.8(b)(1) The other real parties-in-interest are Sony Semiconductor Solutions Corporation, Sony Semiconductor Manufacturing Corporation, Sony Corporation, Sony Corporation of America, and Sony Electronics Inc.

B. Related Matters

1. District Court Litigation Matters

The '764 Patent is presently the subject of a patent infringement lawsuit filed against Petitioner Apple Inc.:

SiOnyx, LLC v. Apple Inc., No. 1:24-cv-12354 (D. Mass. Sept. 12, 2024).

Additionally, Patent Owner has filed the following district court action against third-party Samsung:

SiOnyx, LLC v. Samsung Elecs. Co., Ltd., No. 2:24-cv-00291 (E.D. Tex. Apr. 30, 2024).

2. ITC Matters

Patent Owner has filed the following ITC action against third-party Samsung:

In the Matter of Certain Sensors with Pixels and Products Containing the Same, USITC Inv., No. 337-TA-1403, Apr. 30, 2024.

3. IPR Matters

Third-party Samsung has filed the following IPR challenging Claims 1-25 of the '764 Patent:

Samsung Elecs. Co., Ltd. v. SiOnyx, LLC, IPR2025-00164 (PTAB Nov. 29, 2024) (the Samsung IPR).

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioners identify the following matters related to the '764 Patent:

Apple Inc., et al. v. SiOnyx LLC, IPR2025-00689, regarding U.S. Patent No. 11,721,714; and

Apple Inc., et al. v. SiOnyx LLC, IPR2025-00845, regarding U.S. Patent No. 10,224,359.

C. Lead and Back-Up Counsel

Petitioners provide the following designation and service information for lead and back-up counsel. 37 C.F.R. §§ 42.8(b)(3) and (b)(4).

Lead Counsel	Back-Up Counsel
Jennifer C. Bailey (Reg. No. 52,583) jennifer.bailey@eriseip.com PTAB@eriseip.com	Matthew A. Smith (Reg. No. 49,003) smith@smithbaluch.com
<u>Postal and Hand-Delivery Address:</u> ERISE IP, P.A. 7015 College Blvd., Suite 700 Overland Park, Kansas 66211 Telephone: (913) 777-5600 Fax: (913) 777-5601 <i>Counsel for Petitioner Apple Inc.</i>	<u>Postal and Hand-Delivery Address:</u> SMITH BALUCH LLP 700 Pennsylvania Ave SE, Suite 2060 Washington, DC 20003 Telephone: (202) 669-6207 <i>Counsel for Petitioner Sony Group Corporation</i>

D. 37 C.F.R. § 42.8(b)(4) – Service Information

Please address all correspondence to the lead and back-up counsel as shown above. Petitioners consent to electronic service by e-mail at the e-mail addresses provided above.

CLAIM LISTING APPENDIX
U.S. Patent No. 9,064,764 for Claims 1-25

Claim Designation	Claim Language
Claim 1[Pre]	A light trapping device, comprising:
Claim 1[a]	at least one light sensitive pixel;
Claim 1[a][i]	having a light incident surface, a backside surface opposite the light incident surface,
Claim 1[a][ii]	and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
Claim 1[b]	a backside light trapping material substantially covering the backside surface; and
Claim 1[c]	a peripheral light trapping material substantially covering the peripheral sidewall,
1[c][i]	wherein at least one of the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials,
1[c][ii]	wherein at least one of the two low refractive index materials is doped with a dopant to create a surface field, and
Claim 1[d]	wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.
Claim 2	The device of claim 1, wherein the backside light trapping material and the peripheral light trapping material includes a high refractive index material sandwiched between two low refractive index materials.
Claim 3	The device of claim 1, wherein the dopant is boron or antimony.
Claim 4	The device of claim 1, wherein the peripheral sidewall extends completely around the pixel periphery.
Claim 5	The device of claim 1, wherein the peripheral sidewall extends from the light incident surface to the backside surface.
Claim 6	The device of claim 1, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.
Claim 7	An array of light trapping pixel devices of claim 1.

Claim Designation	Claim Language
Claim 8[Pre]	A light trapping device, comprising:
Claim 8[a]	at least one light sensitive pixel
Claim 8[a][i]	having a light incident surface, a backside surface opposite the light incident surface,
Claim 8[a][ii]	and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
Claim 8[b]	a backside light trapping material substantially covering the backside surface; and
Claim 8[c]	a peripheral light trapping material substantially covering the peripheral sidewall,
Claim 8[d]	wherein at least one of the backside light trapping material and the peripheral light trapping material includes a first material sandwiched between two second materials, wherein the first material has a higher refractive index as compared to the two second materials, and wherein the difference in refractive index between the first material and the two second materials is at least 0.2,
Claim 8[d][i]	and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.
Claim 9	The device of claim 8, wherein the two second materials have a refractive index of less than about 2.1.
Claim 10	The device of claim 9, wherein at least one of the two second materials includes a member selected from the group consisting of an oxide, a nitride, oxynitrides, a gas, at least a partial vacuum, and combinations thereof.
Claim 11	The device of claim 9, wherein the at least one of the two second materials includes a member selected from the group consisting of silicon oxide, silicon nitride, silicon dioxide, and combinations thereof.
Claim 12	The device of claim 8, wherein the first material includes a material having a refractive index of greater than or equal to about 2.1.

Claim Designation	Claim Language
Claim 13	The device of claim 12, wherein the first material includes a member selected from the group consisting of polycrystalline silicon, amorphous silicon, single crystal silicon, multicrystalline silicon, nanocrystalline silicon, germanium, and combinations thereof.
Claim 14	The device of claim 8, wherein the peripheral sidewall extends completely around the pixel periphery.
Claim 15	The device of claim 8, wherein the peripheral sidewall extends from the light incident surface to the backside surface.
Claim 16	The device of claim 8, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.
Claim 17[Pre]	A light trapping device, comprising:
Claim 17[a]	at least one light sensitive pixel
Claim 17[a][i]	having a light incident surface, a backside surface opposite the light incident surface,
Claim 17[a][ii]	and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
Claim 17[b]	a backside light trapping material substantially covering the backside surface; and
Claim 17[c]	a peripheral light trapping material substantially covering the peripheral sidewall,
Claim 17[c][i]	wherein at least one of the backside light trapping material and the peripheral light trapping material has a sloped surface at the pixel device interface,
Claim 17[c][ii]	and wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.
Claim 18	The device of claim 17, wherein the peripheral sidewall extends completely around the pixel periphery.
Claim 19	The device of claim 17, wherein the peripheral sidewall extends from the light incident surface to the backside surface.
Claim 20	The device of claim 17, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

Claim 21[Pre]	A light trapping device, comprising:
Claim 21[a]	at least one light sensitive pixel
Claim 21[a][i]	having a light incident surface, a backside surface opposite the light incident surface,
Claim 21[a][ii]	and a peripheral sidewall disposed into at least a portion of the pixel and extending at least substantially around the pixel periphery;
Claim 21[b]	a backside light trapping material substantially covering the backside surface;
Claim 21[c]	a peripheral light trapping material substantially covering the peripheral sidewall; and
Claim 21[d]	a textured layer positioned to interact with light proximal to the backside surface,
Claim 21[d][i]	wherein light contacting the backside light trapping material or the peripheral light trapping material is reflected back toward the pixel.
Claim 22	The device of claim 21, wherein the textured layer is located between the backside surface and the backside light trapping material.
Claim 23	The device of claim 21, wherein the peripheral sidewall extends completely around the pixel periphery.
Claim 24	The device of claim 21, wherein the peripheral sidewall extends from the light incident surface to the backside surface.
Claim 25	The device of claim 21, wherein at least one of the backside light trapping material and the peripheral light trapping material is a metal layer.

APPENDIX OF EXHIBITS

Exhibit 1001	U.S. Patent No. 9,064,764 (the “’764 Patent”)
Exhibit 1002	File History of the ’764 Patent (the “’764 File History”)
Exhibit 1003	Declaration of Dr. Stanley Shanfield (“Dec.”)
Exhibit 1004	U.S. Patent No. 7,675,099 to Hwang et al. (“Hwang-099”)
Exhibit 1005	U.S. Patent Publication No. 2010/0302432 to Komuro (“Komuro”)
Exhibit 1006	Certified English Translation of Korean Publication No. 2003-0001795 to Hwang (“Hwang-795”)
Exhibit 1007	U.S. Patent Publication No. 2011/0019050 to Yamashita (“Yamashita”)
Exhibit 1008	U.S. Patent No. 7,709,775 to Konno et al. (“Konno”)
Exhibit 1009	<i>Intentionally Left Blank</i>
Exhibit 1010	U.S. Patent No. 7,492,027 to Mouli (“Mouli”)
Exhibit 1011	U.S. Patent Publication No. 2009/0194671 to Nozaki et al. (“Nozaki”)
Exhibit 1012	U.S. Patent Publication No. 2007/0108476 to Hong (“Hong”)
Exhibit 1013	Certified English Translation of Korean Patent No. 10-0688584 to Hwang (“Hwang-584”)
Exhibit 1014	<i>Certain Sensors with Pixels and Products Containing the Same</i> , Inv. No. 337-TA-1403, USITC Pub. 841145, (2025)
Exhibit 1015	<i>SiOnyx, LLC vs. Samsung Electronics, CO., LTD. et al.</i> , Case No. 2:24-cv-00291-JRG (EDTX, Dkt. No. 4-13)
Exhibit 1016	<i>SiOnyx, LLC vs. Samsung Electronics, CO., LTD. et al.</i> , Case No. 2:24-cv-00291-JRG (EDTX, Dkt. No. 4-14)
Exhibit 1017	<i>SiOnyx, LLC v. Apple, Inc.</i> , Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 22-6)
Exhibit 1018	<i>SiOnyx, LLC v. Apple, Inc.</i> , Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 53)
Exhibit 1019	<i>SiOnyx, LLC v. Apple, Inc.</i> , Case No. 1:24-cv-12354 (D. Mass, Dkt. No. 51)
Exhibit 1020	D. Mass Local Patent Rules
Exhibit 1021	S. M. Sze & Kwok Kwok Ng, <u>Physics of Semiconductor Devices</u> (3 rd ed. 2007) (“Sze”)
Exhibit 1022	James R. Janesick, <u>Scientific Charge-Coupled Devices</u> (2001) (“Janesick”)
Exhibit 1023	Alistair Sproul, <u>Solar Cells: Resources for the Secondary Science Teacher</u> , University of New South Wales (2003) (“Sproul”)
Exhibit 1024	U.S. Patent Publication No. 2007/0190681 to Lee et al. (“Lee”)

Exhibit 1025	R. Daniel McGrath, <i>Image Sensor Technology</i> , in <i>Single-Photon Imaging 27</i> (Peter Seitz & Albert JP Theuwissen eds., 2011) (“McGrath”)
Exhibit 1026	Christopher Shea, <i>A Silicon p-i-n detector for a hybrid CMOS imaging system</i> , Rochester Institute of Technology, https://repository.rit.edu/theses/7116 (2012) (“Shea”)
Exhibit 1027	<i>Photodiode Characteristics and Applications</i> , OSI Optoelectronics (2005) (“OSI Whitepaper”)
Exhibit 1028	H. A. Macleod, <i>Thin-Film Optical Filters</i> (3rd ed. 2001) (“Macleod”)
Exhibit 1029	Misha Boroditsky, Regina Ragan & Eli Yablonovitch, <i>Absorption Enhancement in Ultra-Thin Textured AlGaAs Films</i> , 57 <i>Solar Energy Materials and Solar Cells</i> 1 (1999) (“Boroditsky”)
Exhibit 1030	Jan Provoost and Piet De Moor, <i>Backside-illuminated image sensors: Optimizing manufacturing for a sensitivity payoff</i> , https://www.vision-systems.com/print/content/16744520 (2011, retrieved February 24, 2025) (“Provoost”)
Exhibit 1031	A. Tournier et al., <i>R 5 Pixel-to-Pixel Isolation by Deep Trench Technology: Application to CMOS Image Sensor</i> (2011) (“Tournier”)
Exhibit 1032	Vyshnavi Suntharalingam, Dennis D. Rathman, Gregory Prigozhin, Steven Kissel, and Mark Bautz, <i>Back-illuminated three-dimensionally integrated CMOS image sensors for scientific applications</i> , Proc. SPIE 6690, Focal Plane Arrays for Space Telescopes III, 669009 (2007) (“Suntharalingam”)
Exhibit 1033	<i>Intentionally Left Blank</i>
Exhibit 1034	Kyriaki Minoglou et al., <i>Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers Using Deep Trench Isolation</i> , in IEEE 2008 International Interconnect Technology Conference 129 (2008) (“Minoglou”)
Exhibit 1035	U.S. Patent No. 6,710,370 to Street et al. (“Street”)
Exhibit 1036	U.S. Patent Publication No. 2004/0251513 to Su et al. (“Su”)
Exhibit 1037	Maximillian A. Perez et al., <i>Rubidium Vapor Cell with Integrated Bragg Reflectors for Compact Atomic MEMS</i> , 154 <i>Sensors and Actuators A: Physical</i> 295 (2009) (“Perez”)
Exhibit 1038	I. H. Malitson, <i>Interspecimen Comparison of the Refractive Index of Fused Silica*</i> , †, J. Opt. Soc. Am. 55 (1965) (“Maltison”)
Exhibit 1039	U.S. Patent Publication No. 2011/0237060 to Lee et al. (“Lee-060”)

Exhibit 1040	U.S. Patent No. 7,824,983 to Juengling (“Juengling”)
Exhibit 1041	U.S. Patent No. 7,767,485 to Ogawa et al. (“Ogawa”)
Exhibit 1042	U.S. Patent Publication No. 2009/0091806 to Inuiya (“Inuiya”)
Exhibit 1043	U.S. Patent No. 7,911,006 to Chaudhry et al. (“Chaudhry-006”)
Exhibit 1044	U.S. Patent No. 7,595,213 to Kwon et al. (“Kwon”)
Exhibit 1045	U.S. Patent No. 7,141,836 to Adkisson et al. (“Adkisson”)
Exhibit 1046	U.S. Patent No. 7,491,610 to Chaudhry et al. (“Chaudhry-610”)
Exhibit 1047	<i>Intentionally Left Blank</i>
Exhibit 1048	<i>Intentionally Left Blank</i>
Exhibit 1049	<i>Intentionally Left Blank</i>
Exhibit 1050	U.S. Patent No. 6,730,896 to Yamada (“Yamada”)
Exhibit 1051	U.S. Patent Publication No. 2011/0083722 to Atwater et al. (“Atwater”)
Exhibit 1052	<i>Intentionally Left Blank</i>
Exhibit 1053	<i>Intentionally Left Blank</i>
Exhibit 1054	U.S. Patent Publication No. 2011/0005575 to Cao (“Cao”)
Exhibit 1055	U.S. Patent No. 6,809,008 to Holm et al. (“Holm”)
Exhibit 1056	U.S. Patent No. 6,033,968 to Sung (“Sung”)
Exhibit 1057	U.S. Patent No. 4,104,086 to Bondur et al. (“Bondur”)
Exhibit 1058	U.S. Patent No. 6,498,336 to Tian et al. (“Tian”)
Exhibit 1059	A. Crocherie, Jérôme Vaillant & F. Hirigoyen, <i>Three-Dimensional Broadband FDTD Optical Simulations of CMOS Image Sensor</i> , 29 Electronic Imaging (2008) (“Crocherie”)
Exhibit 1060	U.S. Patent No. 7,485,940 to Hsu et al. (“Hsu”)
Exhibit 1061	J. Michelot et al., <i>Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage</i> , INTERNATIONAL IMAGE SENSOR WORKSHOP (2011) (“Michelot”)
Exhibit 1062	U.S. Patent No. 7,800,192 to Venezia et al. (“Venezia”)
Exhibit 1063	U.S. Patent Publication No. 2008/0217720 to Fan et al. (“Fan”)
Exhibit 1064	U.S. Patent Publication No. 2008/0265349 to Kasano et al. (“Kasano”)
Exhibit 1065	Joint Statement Identifying Accused Products, <i>In the Matter of Certain Sensors with Pixels and Products Containing the Same</i> , USITC Inv., No. 337-TA-1403, Apr. 30, 2024
Exhibit 1066	U.S. Publication No. 2010/0275984 A1 to Kaes et al. (“Kaes”)
Exhibit 1067	U.S. Patent No. 6,888,214 B2 to Moulit et al. (“Moulit-214”)
Exhibit 1068	U.S. Publication No. 2011/0025892 A1 to Hibbeler et al. (“Hibbeler”)
Exhibit 1069	U.S. Patent No. 8,357,984 to Mao et al. (“Mao”)

Exhibit 1070	U.S. Patent No. 7,490,486 to Naumann et al. (“Naumann”)
Exhibit 1071	U.S. Patent No. 5,296,045 to Banerjee et al. (“Banerjee”)
Exhibit 1072	U.S. Patent No. 5,101,260 to Nath et al. (“Nath”)
Exhibit 1073	Hitoshi Sai and Michio Kondo, <i>Effect of self-orderly textured back reflectors on light trapping in thin-film microcrystalline silicon solar cells</i> , Journal of Applied Physics, 105, 094511 (June 2009) (“Sai”)
Exhibit 1074	Shrestha Basu Mallick, et al., <i>Coherent light trapping in thin-film photovoltaics</i> , Mrs Bulletin, Volume 36 (June 2011) (“Mallick”)
Exhibit 1075	<i>Intentionally Left Blank</i>
Exhibit 1076	U.S. Patent No. 7,135,350 to Smith et al. (“Smith”)
Exhibit 1077	U.S. Patent No. 4,419,533 to Czubatji et al. (“Czubatji”)
Exhibit 1078	U.S. Patent No. 6,072,117 to Matsuyama et al. (“Matsuyama”)

CERTIFICATION OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. §42.24 that the foregoing Petition for *Inter Partes* Review, excluding any table of contents, mandatory notices under 37 C.F.R. §42.8, certificates of service or word count, or appendix of exhibits, contains 13,993 words according to the word-processing program used to prepare this document (Microsoft Word).

Dated: April 16, 2025

ERISE IP, P.A.

BY: /s/ Jennifer C. Bailey
Jennifer C. Bailey (Reg. No. 52,583)
jennifer.bailey@eriseip.com
7015 College Blvd., Suite 700
Overland Park, KS 66211
P: (913) 777-5600
F: (913) 777-5601

*COUNSEL FOR PETITIONER
APPLE INC.*

SMITH BUCHANAN LLP

BY: /s/ Matthew A. Smith
Matthew A. Smith, Reg. No. 49,003
smith@smithbaluch.com
SMITH BALUCH LLP
700 Pennsylvania Ave SE, Suite 2060
Washington, DC 20003
(202) 669-6207

*COUNSEL FOR PETITIONER SONY
GROUP CORPORATION*

**CERTIFICATE OF SERVICE ON PATENT OWNER
UNDER 37 C.F.R. § 42.105**

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that on April 16, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and Exhibits were provided via Federal Express to the Patent Owner by serving the correspondence address of record for the '764 Patent:

Troutman Pepper Hamilton Sanders LLP (Rochester)
70 Linden Oaks
Suite 210
Rochester, NY 14625

Further, a courtesy copy of this Petition for *Inter Partes* Review was sent via email to Patent Owner's litigation counsel:

Pepper Hamilton
125 High Street, 19th Floor
Boston, MA 02110
Gwendolyn E. Tawresey (Gwendolyn.Tawresey@Troutman.com)
Gregory D. Len (leng@pepperlaw.com)
Ryan C. Deck (ryan.deck@troutman.com)
William D. Belanger (William.Belanger@Troutman.com)

Respectfully submitted,

ERISE IP, P.A.

BY: /s/ Jennifer C. Bailey
Jennifer C. Bailey (Reg. No. 52,583)
jennifer.bailey@eriseip.com
7015 College Blvd., Suite 700
Overland Park, KS 66211
P: (913) 777-5600
F: (913) 777-5601

*COUNSEL FOR PETITIONER
APPLE INC.*

SMITH BALUCH LLP

BY: /s/ Matthew A. Smith
Matthew A. Smith, Reg. No. 49,003
smith@smithbaluch.com
700 Pennsylvania Ave SE, Suite 2060
Washington, DC 20003
(202) 669-6207

*COUNSEL FOR PETITIONER SONY
GROUP CORPORATION*