

See discussions, stats, and author profiles for this publication at: <https://www.researchgate.net/publication/2983681>

CMOS Single-Chip Electronic Compass with Microcontroller

Article in IEEE Journal of Solid-State Circuits · January 2008

DOI: 10.1109/JSSC.2007.908694 · Source: IEEE Xplore

CITATIONS

60

READS

3,928

4 authors, including:



Christian Schott

Melexis Technologies SA

41 PUBLICATIONS 742 CITATIONS

SEE PROFILE

All content following this page was uploaded by [Christian Schott](#) on 29 October 2013.

The user has requested enhancement of the downloaded file.

CMOS Single-Chip Electronic Compass With Microcontroller

Christian Schott, *Member, IEEE*, Robert Racz, Angelo Manco, and Nicolas Simonne

Abstract—We present a CMOS single-chip electronic compass sensor including the complete digital signal processing for accurate heading calculation. The device's analog part consists of Hall-based three-axis magnetic field transducer with integrated magnetic concentrator that operates as a passive magnetic amplifier. The analog amplification chain features a gain of up to 20 000. A true-12-bit extended counting ADC converts the amplified magnetic field signals into the digital domain, where a 16-bit microcontroller calculates the heading information and outputs it via an SPI interface. The compass sensor is realized in 0.35 μm low-voltage CMOS technology plus a simple batch processing step for deposition of a metal layer. The compact die size of 2.3 mm $\times$ 2.8 mm allows for packaging into a standard 4 mm $\times$ 5 mm $\times$ 1 mm surface-mount plastic package. The heading resolution is better than 0.5°, and the accuracy better than $\pm 2^\circ$.

Index Terms—Electronic compass, Hall sensor, magnetic concentrator, magnetic sensor.

I. INTRODUCTION

THE earth magnetic field is a three-dimensional (3-D) field with a flux density of about 50 μT . The field component parallel to the earth's surface, which can be used for a heading measurement, ranges from less than 10 μT in higher latitudes close to the poles to about 40 μT around the equator (Fig. 1).

A two-axis magnetometer held parallel to the earth's surface is therefore the minimum configuration for a magnetic heading measurement. For most portable applications, an accuracy of 1°–3° in a field of 20 μT over a temperature range from -40°C to 85 $^\circ\text{C}$ is requested.

Nowadays, various types of technologies are applied to electronic compasses, and they are based on the magneto-resistive [e.g., anisotropic magnetoresistance (AMR) or giant magnetoresistance (GMR)] effect [1], the fluxgate effect [2], [3], or on the magneto-impedance (MI) effect in zero-magneto-strictive amorphous wires [4].

These proposed solutions either have the drawback of not being compatible with CMOS technology, since they are manufactured in a dedicated technology and/or they are not compatible with low power requirements. For example, a low-field AMR sensor needs an integrated set–reset current pulse of several hundred milliamperes, and an integrated fluxgate sensor needs strong operation currents to drive the open-loop core into

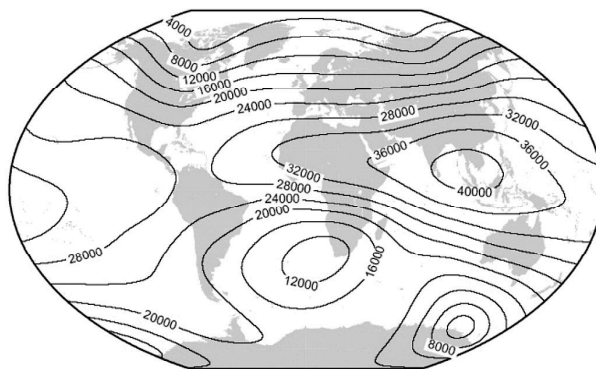


Fig. 1. Strength of surface-parallel magnetic flux density on earth in nT.

saturation. A major drawback of magnetic field sensors containing ferromagnetic material is that the offset of the sensor changes after exposure to a high magnetic field. This effect is known as perming and can be explained by the remnant field effect of the material. Perming is one of the most critical issues for low field measurements and has to be considered for compass applications.

In this paper, we present a single-chip electronic compass which contains the sensor and the electronics with microcontroller on the same silicon chip. Additionally, this chip is small of size and features low power consumption. The standard CMOS technology allows for embedding state-of-the-art analog and digital signal-processing hardware that is required for an accurate heading calculation with noise reduction circuit, A/D conversion, calibration, and interfacing.

As our target is to use a standard CMOS technology, the choice for integrated magnetic sensors is clearly limited to silicon Hall elements. A Hall-element sensitivity of 250 V/AT and a biasing current of 350 μA leads to a magnetic field sensitivity of 87.5 mV/T. This gives an output voltage of 1.75 μV for a 20 μT field.

On the other hand, the Hall element has a resistance of about 5 k Ω which results in an rms white noise spectral density of about 9.1 nV/sqrt(Hz) for $T = 300\text{ K}$. From this figure, we can expect an average peak noise indicating the maximum expected error of 26 nV/sqrt(Hz). These figures lead to a required integration time of over 2 s if we want to have a signal-to-noise ratio (SNR) of 40 dB at $B = 20\text{ } \mu\text{T}$. The situation becomes even worse if we also consider the amplifier noise contribution. Assuming matched amplifier inputs featuring the same noise power as the Hall elements, the required integration time doubles to over 4 s. Such a long integration time is certainly too long for practical compass application. Therefore, we provide for two

Manuscript received April 5, 2007; revised August 22, 2007.

C. Schott is with Melexis Technologies, CH-2200 Bevaix, Switzerland (e-mail: csc@melexis.com).

R. Racz and A. Manco are with the Sentron, A Melexis Company, CH-6300 Zug, Switzerland (e-mail: ror@melexis.com; anm@melexis.com).

N. Simonne is with Melexis, B-3980 Tessenderlo, Belgium (e-mail: nsm@melexis.com).

Digital Object Identifier 10.1109/JSSC.2007.908694

improvements in our estimation: (1) we use four Hall elements simultaneously and add their outputs in the amplifier and (2) we pre-amplify the magnetic field by a factor of six through an integrated concentrator. The first improvement increases the SNR by a factor of two, which is equivalent to a reduction of the integration time by a factor of four, and the second improvement further reduces the integration time by a factor of 36, so that the estimated necessary integration time reduces to about 30 ms per channel for the two in-plane axes X and Y . For the perpendicular axis Z , which does not take advantage of integrated magnetic concentrator (IMC) field amplification, we either need to integrate longer or accept lower resolution. Another limiting factor of Hall elements is their zero-field offset, which is caused by stress effects, doping variation, and mask alignment errors. Offset is typically on the order of a millivolt, a value that is equivalent to a magnetic input flux density of about 10 mT, which is more than two orders of magnitude higher than our signal.

This estimation brings us directly to our tasks.

We need the following:

- a solution to measure at least two axes;
- a signal gain of at least three to four orders of magnitude;
- a reduction of the influence of Hall-element offset of four to five orders of magnitude.

The only nonconventional step we use to achieve our goal is the addition of a structured metal layer on top of the silicon chip. This IMC operates as a passive magnetic field amplifier and significantly improves the ability to measure the flux density along two of the three axes.

In the following sections, we will guide the reader through the different technological and architectural steps to show how we mastered those challenges. After an architectural overview, we first explain the principle of operation of the magnetic front-end and describe our IMC technology. Finite-element simulation results are used to underline its robustness. Then, we go into detail on the very high analog amplification, the AD conversion, and the digital data processing by the microcontroller. After this, we describe the realized chip, and we show measurement results particularly related to sensitivity, linearity, and offset drift.

II. COMPASS ARCHITECTURE

The block architecture of our electronic compass is shown in Fig. 2. The magnetic concentrator amplifies the externally applied flux onto the three-axis Hall system. The electrical Hall output signals are multiplexed into the chopped amplification chain and converted to the digital domain. The 16-Bit on-chip microcontroller performs temperature and matching calibration by using prestored calibration data in the memory, and it also calculates the heading information. The processed heading data is finally available to an external host system via a serial peripheral interface (SPI).

III. MAGNETIC FRONTEND

The magnetic front-end is a three-axis magnetic field transducer based on a combination of Hall elements with a thin soft ferromagnetic layer, the IMC, which is structured onto the silicon surface.

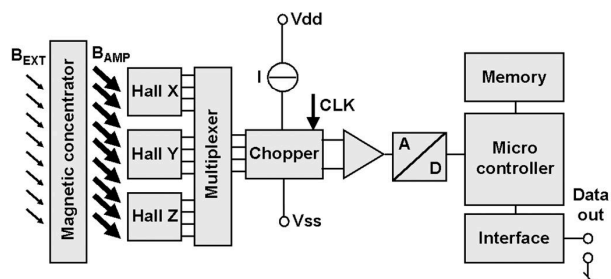


Fig. 2. Block schematic of the electronic compass with microcontroller.

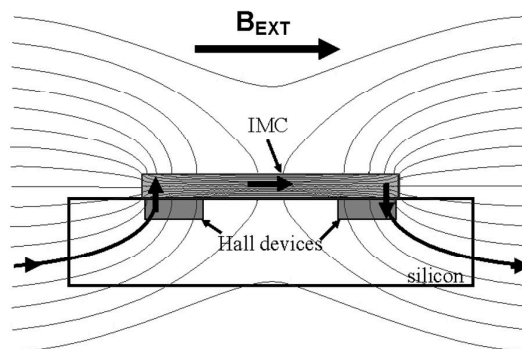


Fig. 3. Cross-sectional view of the IMC working principle. An external applied field is locally rotated and concentrated onto the Hall elements under the edge of the IMC.

A. Principle of Operation

The IMC brings two significant benefits: it locally rotates and amplifies the external in-plane magnetic field, so that it can be measured by conventional Hall devices (Fig. 3).

By arranging Hall elements under the edge of a round disk, a two-axis sensor is realized [6]. For good matching of the X - and Y -axes, the concentrator structure shall be at least rotation-symmetric by $\pi/2$, so the magnetic field components along both axes follow similar paths through the concentrator structure. We already presented earlier [7] that, by using ring structures, any remnant magnetization effect in the metal layer can be suppressed.

B. Magnetic Gain

For the compass application, we have maximized the magnetic gain by using several IMC structures and by placing the Hall devices close to the gaps between them. The fitting of experimental data shows that the magnetic gain depends on approximately the square root of the total length of the metallic structures (Fig. 4). For a high magnetic gain, we need to make them as large as possible by using almost the entire chip dimensions. For a 2 mm total length of the concentrator structure in the field direction, we can expect a passive magnetic gain of approximately a factor of six.

As we need to measure at least two axes in the plane, we decided to implement a structure consisting of five octagons as shown in Fig. 5. The Hall elements for the X - and Y -axes are positioned under the rings close to the gaps between the inner octagon ring and the outside rings, whereas the Hall elements

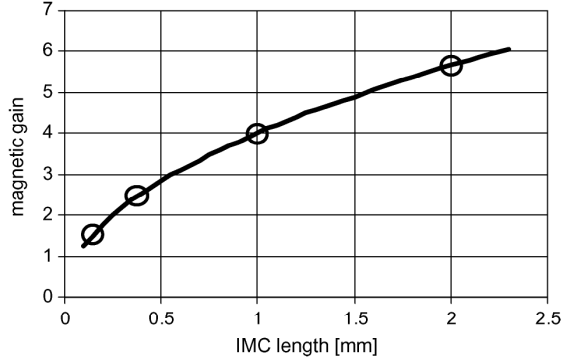


Fig. 4. Magnetic gain of the IMC increases with the square root of its length. The circles indicate experimental data, and the solid line is a square-root curve fit.

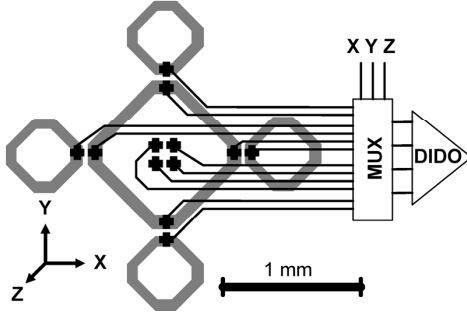


Fig. 5. Magnetic concentrator octagons with Hall elements and connection to the channel multiplexer and preamplifier.

for Z are positioned in the chip center close together. The new octagonal ring geometry replaces the circular rings published earlier [7]. In this new structure, the air gaps between two octagons feature parallel edges and can be better controlled in the etching process than the concave air gap between two ring structures. This reduces matching errors between the axes and makes the sensor more robust.

This three-axis field transducer generates three Hall voltages V_x , V_y , and V_z , corresponding to the three magnetic field components B_x , B_y , and B_z . The magnetic gain is about 6 for the X - and Y -axis and only one for the Z -axis, where the magnetic concentrator is very thin and has no gain effect. The octagons are about $60 \mu\text{m}$ wide. The Hall elements are realized in a pinched n -well of about $15 \mu\text{m} \times 15 \mu\text{m}$ in size, where four $n+$ contacts distributed equally around the perimeter are used for the supply input and the voltage output. The current-related sensitivity of the Hall elements is about 250 V/AT . With a biasing current of $350 \mu\text{A}$ per Hall element, we therefore obtain a sensitivity of 87.5 mV/T . Taking into account the magnetic gain of the IMC of 6 and applying a flux density of $20 \mu\text{T}$, we obtain a signal level at the output of the Hall elements of approximately $10 \mu\text{V}$.

C. IMC Technology

The integrated magnetic flux concentrators consists of a very high-permeability and very low-coercive-field (very soft) amorphous ferromagnetic layer. This material shows outstanding in-

trinsic characteristics, with a coercive field below 1 A/m , which is an order of magnitude better than what can be obtained by electroplated NiFe.

The IMC process is a simple post-process applied on completely manufactured CMOS wafers. First, the ferromagnetic layer is glued in the form of $20 \mu\text{m}$ thin ribbons onto the CMOS wafer containing the electronic circuitry and Hall elements. Then, we structure the covered wafer by using a standard photolithography process and wet-chemical etching. The wafer is then cleaned from glue residues and finally sent for dicing and packaging. Since the IMC layer is electrically isolated from the chip, the question of ESD robustness arises. However, as the IMC is only separated by a few micrometers from the chip and entirely covered by a few hundred micrometers of mold compound, it is not any more susceptible to attracting electric discharge than the silicon chip alone is. The use of small closed structures like disks or rings also reduces the generation of induced voltages from electromagnetic radiation.

The IMC process used for the compass prototypes (Fig. 6) was recently qualified for automotive applications and has already been applied on thousands of wafers at Melexis.

D. Magnetic Simulation

To study the performance of the IMC structures related to process tolerances, we have carried out 3-D magnetic finite-element simulations.

With an applied external flux density of $20 \mu\text{T}$, we can now monitor the resulting vertical component of the flux density around the gap. Fig. 7 shows that the regions with strong flux (white areas) are distributed close to the gap. The simulation has been performed with a vertical distance of $10 \mu\text{m}$ between the IMC and the result plane, which corresponds to the actual distance between the IMC and the Hall elements in the chosen technology.

For a more detailed analysis, we now plot the B_z component along the cross-sectional line $A - A'$. The results for three different vertical distances of 5 , 10 , and $20 \mu\text{m}$ are shown in Fig. 8.

We observe that the maxima are always just outside the gap and below the IMC edge. The amplification factor ranges from about 3.5 for $20 \mu\text{m}$ distance to about 8 for $5 \mu\text{m}$ distance, which indicates that our technology is very sensitive to the vertical distance between the IMC and Hall elements. The fact that the high-gain areas are only a few micrometers wide explains the choice of relatively small-size Hall elements.

E. Degaussing

The sensor additionally contains a circuit block for “low-energy” demagnetization of the ferromagnetic concentrator, to eliminate remnant magnetization caused by strong accidentally applied external fields [5]. The degaussing coil is a single-turn loop through the IMC ring structures, whose lower part is implemented as integrated metal tracks and whose upper part is finished during packaging by bonding connection [7]. The degaussing procedure in the presented compass consists of two successive current pulses of 20 mA with opposite polarity and $10 \mu\text{s}$ duration. A current pulse on a wire through the center of a ferromagnetic ring creates a circular magnetic field inside the ring, which aligns the magnetic domains of the ring in a

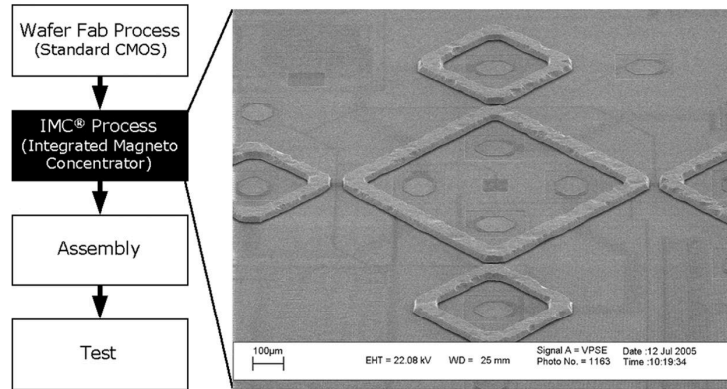


Fig. 6. IMC post-process is applied to entire wafer batches and constitutes a separate manufacturing step between the CMOS process and the packaging.

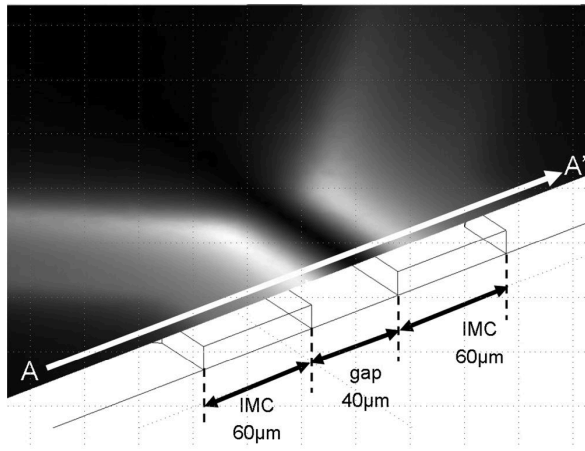


Fig. 7. Simulation result for the vertical component B_z in $10\ \mu\text{m}$ distance above the IMC layer. Dark areas denote a low field and white areas denote a strong field.

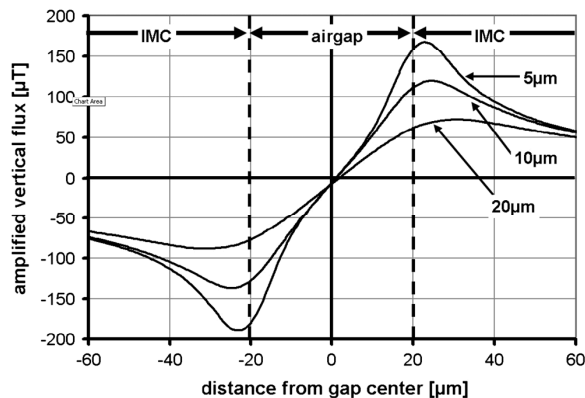


Fig. 8. Magnetic flux simulation results around the gap area for different distances between the IMC and Hall elements and applied external flux density of $20\ \mu\text{T}$.

closed manner, so that no stray field is seen on the outside anymore. This strongly reduces offset fields on the Hall elements from magnetic perming. The polarity change of the pulse further facilitates the alignment, so that a current of only 20%–30% compared with a current needed for full saturation is required.

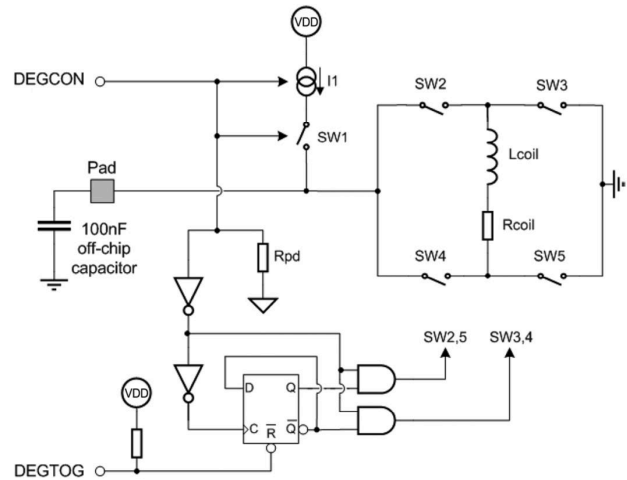


Fig. 9. Degaussing circuit.

Fig. 9 shows the degaussing circuit which operates in two phases controlled by DEGCON. In a first phase of about 10 ms when $\text{DEGCON} = 1$, SW1 is closed, all other switches are open, and the off-chip degaussing capacitor of 100 nF is charged by I1 of about 200 μA . In a second phase of about 10 μs when $\text{DEGCON} = 0$, SW1 is opened and one of the two switches couples (either SW2 and SW5 or SW3 and SW4) is closed, opening a path between the capacitance, the coil ($L_{\text{coil}} + R_{\text{coil}}$), and ground. The direction of the path is given by the flip-flop and toggles at each rising edge of DEGCON. This toggling is enabled by $\text{DEGT OG} = 1$. If it is connected to ground, the current flows always through SW3 and SW4.

The coil has a high-permeability core but only four windings in total, so that its inductance is very low ($4 \times L_{\text{coil}} = 8\ \text{nH}$), and inductive voltage spikes are limited to a few tens of millivolts and cannot cause damage to the circuitry.

Magnetic perming by this method is efficiently reduced from over $2\ \mu\text{T}$ to less than $0.2\ \mu\text{T}$, as shown with the measurements in Fig. 10.

To completely avoid errors from accidental magnetization, degaussing is performed once before every acquisition cycle by applying a current pulse of $\pm 20\ \text{mA}$.

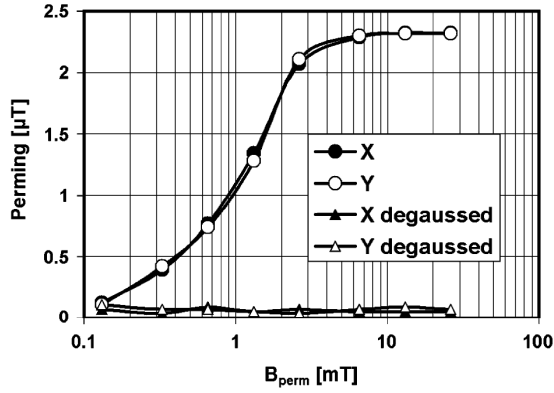


Fig. 10. Measurement of perming effect without and with degaussing versus applied flux density.

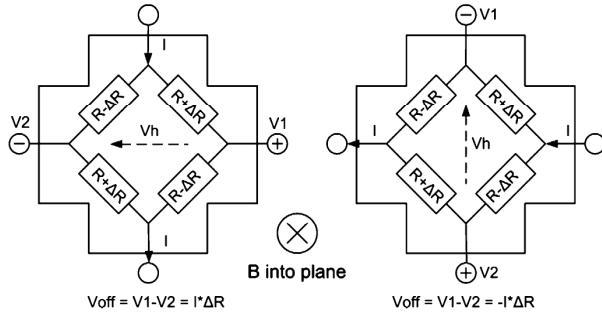


Fig. 11. Spinning current operation on a Hall element in a Wheatstone bridge representation.

Experiment has shown that the current needed for degaussing is four times lower than the comparable saturation current needed for operating a flux gate sensor.

IV. ANALOG AMPLIFICATION

As mentioned beforehand, the acquired Hall voltages of a few microvolts now need to be amplified by at least three orders of magnitude to obtain a good resolution from the ADC conversion.

The Hall elements are current biased and operated by using the spinning current technique (Fig. 11). By this technique, the current biasing and the readout terminals for each Hall element are periodically rotated in the opposite sense. The figure also shows how the bridge resistors are unbalanced by ΔR , for example, due to mechanical stress from packaging.

The spinning operation causes the Hall voltage to be modulated by the spinning frequency, whereas the offset unbalance is a dc signal. Both parts of the signal are then amplified, but only the modulated Hall signal can pass the following high-pass filter. In such a way, Hall-element offset and amplifier offset are suppressed (Fig. 12).

The fully differential amplification chain (Fig. 13) consists of three amplifier stages and has a programmable analog gain, which can be varied between 312.5 and 20 000. Gain is controlled digitally via the micro-controller. The amplification

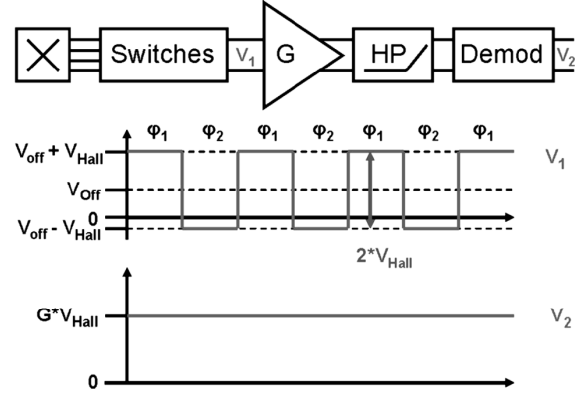


Fig. 12. By the spinning current principle, the signal voltage is separated by the offset voltage through modulation.

stages are connected via high-pass filters for further elimination of any dc-offset voltages from the amplifiers.

After demodulation, this signal is low-pass filtered (8 kHz corner frequency) and buffered by a voltage-follower pair to the ADC.

The first amplification stage (Fig. 14) is a low-noise differential input/differential output (DIDO) amplifier with 4 + 1 input ports. It adds and amplifies differential voltages of the four Hall devices, and the fifth input is used for feedback gain control. Its gain is defined by feedback resistors and can be set to 12.5, 25, and 50 (2-bit control via a micro-controller). Feedback resistors are implemented as low-ohmic polysilicon resistors with a small temperature coefficient ($\sim 10^{-5}/K$).

This low-noise preamplifier has a two-stage Miller amplifier topology. It has been designed to match the noise power of Hall elements (i.e., noise equivalent input resistor of 5 k Ω). For this reason, nMOS input pairs are preferred because of their higher transconductance compared with pMOS pairs, saving area and current. Their higher $1/f$ noise penalty is effectively reduced by the chopping principle and is therefore not dominant. The input-referred rms noise spectral density is 22 nV/sqrt(Hz) at the chopping frequency of 25 kHz (Fig. 15). The $1/f$ noise corner frequency is located at 92 kHz.

Common-mode regulation is ensured by a single-stage amplifier which senses the output common mode via resistors and compares it with an internal common-mode reference at half the supply voltage.

All amplifier stages are ac-coupled to eliminate offset using first-order high-pass filters with a corner frequency at 15 kHz.

The second and third amplifier stages are realized as two identical two-opamp differential instrumentation amplifiers, as shown in Fig. 16. The amplifiers are Miller opamps with pMOS input pair. The gain is defined by feedback resistors and can be set to 5, 10, and 20. To reduce the variation of the settling behavior due to gain programming, the compensation capacitor is increased for the two lower gain settings. Its bandwidth for maximum gain of 20 is kept low to 64 kHz to limit noise.

Those two gain stages further increase the signal level to be compliant with the A/D input range (which is typically 3.3 V) and the maximum external magnetic field. For typical compass

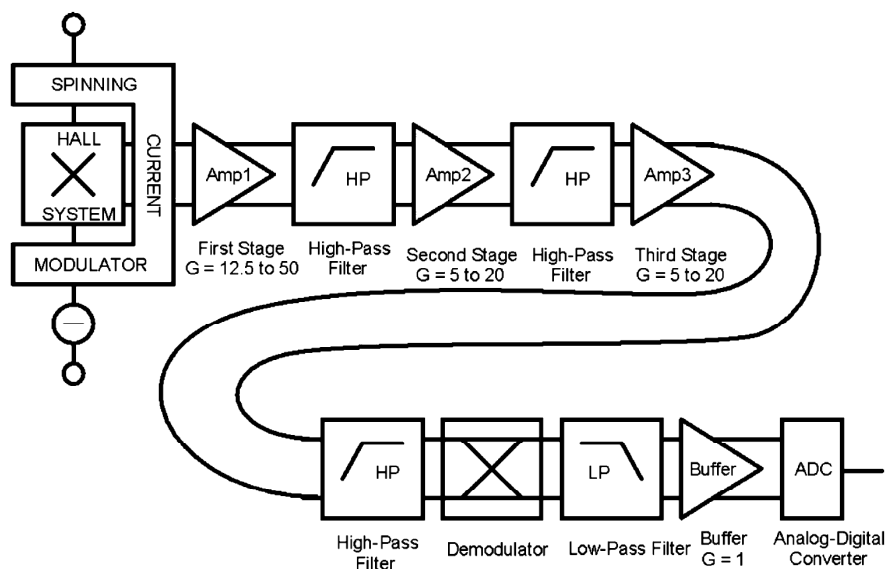


Fig. 13. Analog amplification chain consists of a series of three separate amplifiers with a total gain of up to 20 000.

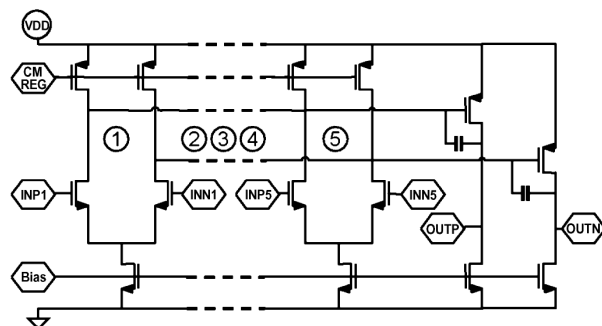


Fig. 14. Low-noise preamplifier in 4 + 1 DIDO configuration.

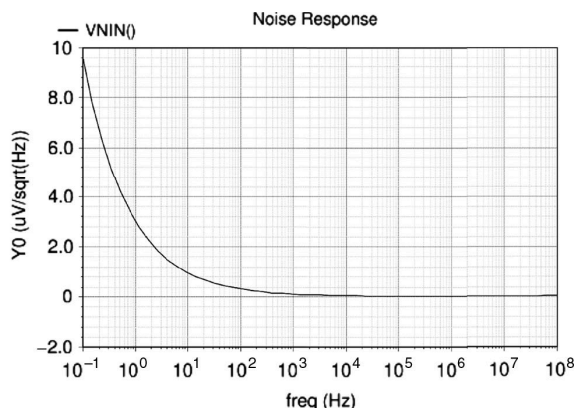


Fig. 15. Low-noise preamplifier input-referred noise spectral density.

application, analog gain is set to 2500, leading to an overall sensitivity of 7.25 LSB/ μ T and a magnetic input range of $\pm 280 \mu$ T.

A first-order low-pass filter after demodulation limits the noise spectrum and amplitude before sampling by the A/D. The corner frequency of the low-pass filter is 8 kHz.

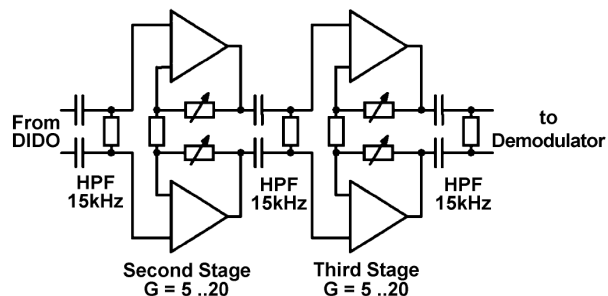


Fig. 16. Implementation of the second and third amplification stages in instrumentation amplifier configuration.

The signal is then buffered before being connected to the A/D. It consists of an amplifier in voltage-follower configuration. The major design constraint is the settling time (within 1 A/D clock cycle) when loaded with A/D input capacitance (2.8 pF).

V. A/D CONVERSION

After amplification and demodulation, the Hall signal is converted into the digital domain. The A/D will integrate the signal over time, limiting the bandwidth in order to reach SNR requirements.

The A/D architecture (Fig. 17) is based on the extended counting technique [8]. It is a compromise between first-order $\Sigma\Delta$ modulation with its high accuracy but relatively low speed, on the one hand, and algorithmic A/D conversion with its higher speed but lower accuracy, on the other hand.

For one A/D conversion, the converter passes through two modes. In the first mode, the system operates as a reset-able first-order $\Sigma\Delta$ modulator to convert the most significant bits (9–12 bits). This mode is called the “counting conversion.” Then, in a second mode, the same hardware is used to convert the least

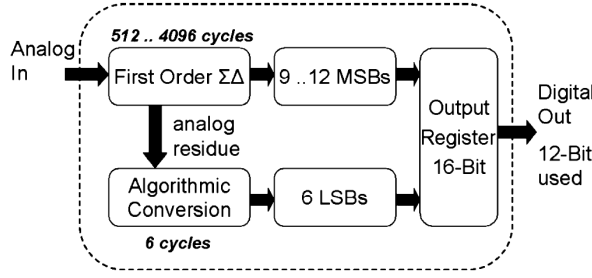


Fig. 17. Two-stage ADC provides for a first-order sigma-delta conversion and a subsequent algorithmic conversion of the integrated analog residual charge.

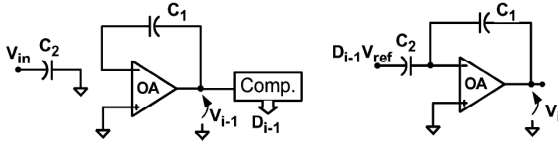


Fig. 18. Circuit configuration during both phases of a counting conversion step.

significant bits (6 bits fixed) by an algorithmic A/D conversion technique. This mode is called the “extended conversion.”

The circuit configuration during the counting conversion is depicted on Fig. 18. It consists of a switched-capacitor integrator and a comparator. In reality, the circuits are fully differential, but for simplicity the discussion is for a single-ended equivalent. After an initial reset, the normal operation in each step consists of two phases. In the first phase of the i th step, the input voltage V_{in} is sampled on the input capacitor C_2 . Meanwhile, the output voltage V_{i-1} of the previous step is still available at the integrator’s output. Based on this voltage, a comparator decides the code D_{i-1} . The value of this code is +1 if the voltage V_{i-1} is positive and -1 if it is negative. In the second phase, the top plate of the sampling capacitor C_2 is switched towards the opamp inverting node, and the bottom plate is switched towards $\pm V_{ref}$ depending on the code D_{i-1} . Then, the charge is transferred towards the feedback capacitor C_1 . This is the typical way a first-order $\Sigma\Delta$ modulator is implemented in switched-capacitor technology.

It can be shown that the output voltage V_{count} after the N steps in the counting conversion equals

$$V_{count} = N \frac{C_2}{C_1} V_{in} - \frac{C_2}{C_1} V_{ref} \sum_{i=1}^N D_i. \quad (1)$$

To reconstruct the input voltage V_{in} , (1) can be rewritten as

$$V_{in} = \frac{V_{ref} \sum_{i=1}^N D_i + \frac{C_1}{C_2} V_{count}}{N}. \quad (2)$$

We see that the input voltage can be reconstructed from the known values of the D_i codes and from the (unknown) value of the voltage V_{count} . After the counting steps, the system goes into the extended conversion mode where the voltage V_{count} is measured by a more efficient but less accurate algorithmic A/D conversion technique.

The extended conversion mode is not further described in this paper because it is not used for the signal processing. Only

the counting conversion ($\Sigma\Delta$) bits are significant versus the signal-to-noise level (40 dB–10 bits resolution).

A/D CMOS implementation is a fully differential device but, for simplicity, a single-ended schematic of the overall A/D converter is shown in Fig. 19. A timing diagram of all switch drive signals is shown in Fig. 20.

The system described above requires a digital controller to generate the appropriate switch control signals. It is implemented as a digital logic which generates the basic conversion signals and an asynchronous interface which generates the switch signals with all needed delays. The digital logic collects the all-analog output data D_i and processes them to a digital output code ADC[17:0]. The whole digital logic operates at twice the clock frequency of the switched-capacitor circuits.

Typical current consumption is 200 μ A in normal mode when operating at 400 kHz. The INL (Fig. 21) and DNL (Fig. 22) of ± 1.5 LSB has been measured for the lowest resolution of 15 bits.

At a sampling frequency of 200 kHz, the programmable $\Sigma\Delta$ part between 9 and 12 allows the range of integration time to be between 5 and 40 ms. Based on the 40 dB SNR target, integration time of 40 ms is used. Digital signal processing is then performed only on the 12 MSBs of the A/D converter.

For proper operation, the A/D sampling frequency and the chopping frequency are synchronized to ensure that A/D conversion starts synchronously with the spinning cycle. The nominal chopping frequency is 25 kHz. One spinning cycle lasts one period, i.e., 40 μ s. The measurement of each axis lasts 40 ms. Thus, the measurement signal of one axis is a sequence of 1000 spinning cycles.

VI. DIGITAL SIGNAL PROCESSING

The digitized data is transmitted to an on-chip microcontroller. From the data of both axes, the angle of the applied magnetic field (earth’s field) is computed with the help of a firmware algorithm stored in the ROM. This heading information is then output to an external host microcontroller via the digital interface.

Fig. 23 diagrammatically shows the firmware running by the microcontroller. By default continuous acquisition of the temperature sensor, X -, Y -, and Z -axes are running in the main cycle. Degaussing and analog input scanning rate is programmable. Thermal compensation and process correction are computed in a background loop based on calibration data. The heading information is transmitted on request via a digital interface (I2C or SPI).

The heading measurement is given by the following formula:

$$\alpha = \arctan \left(\frac{V_x}{V_y} \right)$$

where α is the angle measurement and V_x and V_y are the processed data given by

$$\begin{aligned} V_x &= X_{off}(T) + A_x(\alpha) \cdot \sin(90 - \alpha + \beta) \cdot \theta \\ V_y &= Y_{off}(T) + A_y(\alpha) \cdot \sin(\alpha) \end{aligned}$$

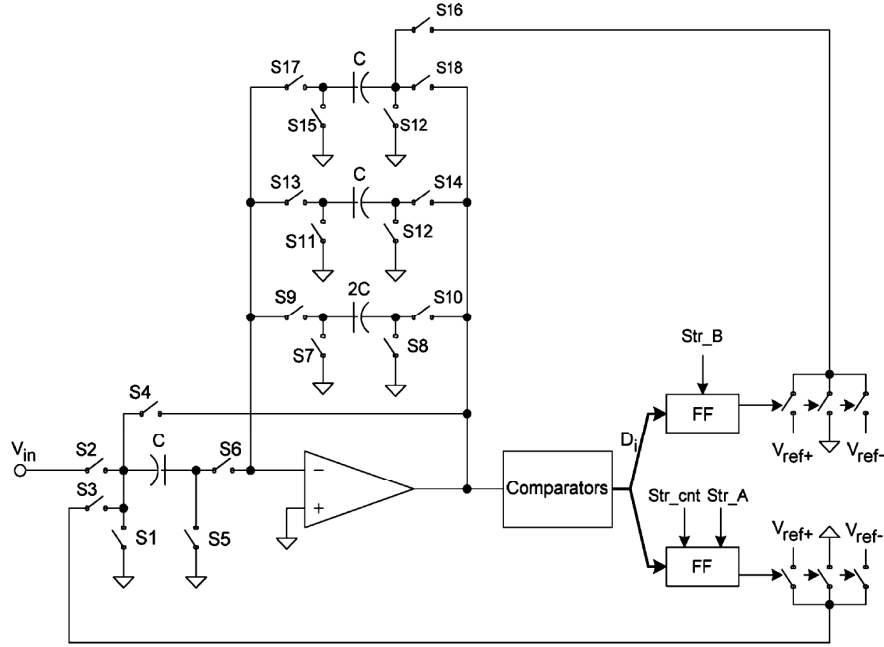


Fig. 19. Single-ended schematic of the overall A/D converter.

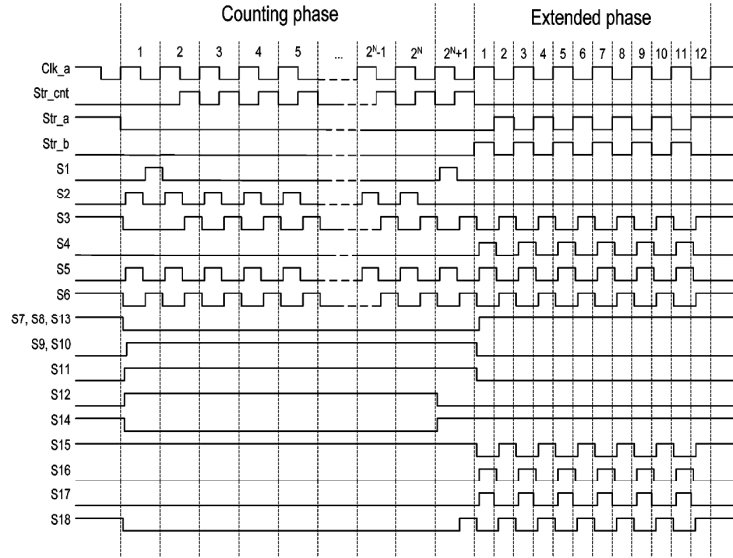


Fig. 20. Timing diagram for the extended counting A/D converter.

where:

- T is the temperature;
- $A_x(\alpha)$ and $A_y(\alpha)$ are the magnetic sensitivity along the X - and Y -axes, respectively;
- $X_{\text{off}}(T)$ and $Y_{\text{off}}(T)$ are the offsets of the X - and Y -axes, both of which are temperature-dependent and therefore require thermal compensation;
- β and θ are the orthogonality correction angle (phase error) and the sensitivity mismatch correction factor,

respectively; these corrections are required to compensate for the IMC process variation.

The last four items represent a very important step of our magnetic calibration, which is performed at three temperatures and which is mandatory to achieve the initially defined performance in terms of angular accuracy of around 2° . The temperature is measured during each acquisition cycle via an on-chip differential temperature sensor with an accuracy of $\pm 1.3^\circ\text{C}$ which is read via the A/D converter.

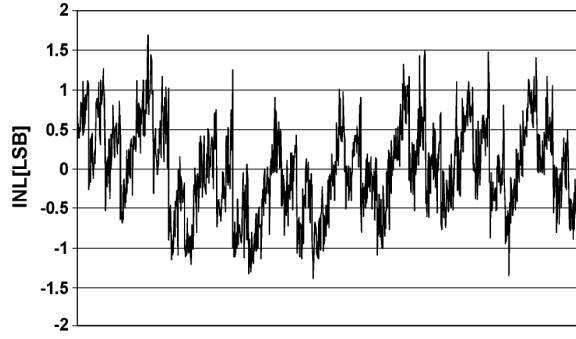


Fig. 21. Measured INL for 15 bit resolution.

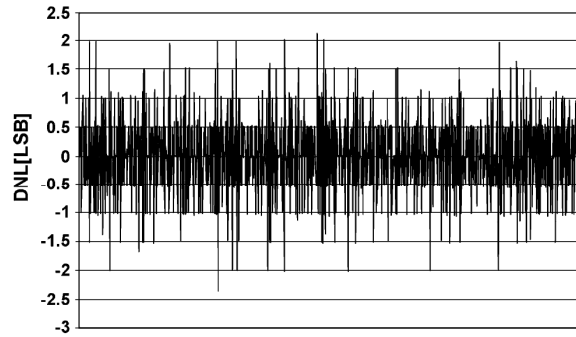


Fig. 22. Measured DNL for 15 bit resolution.

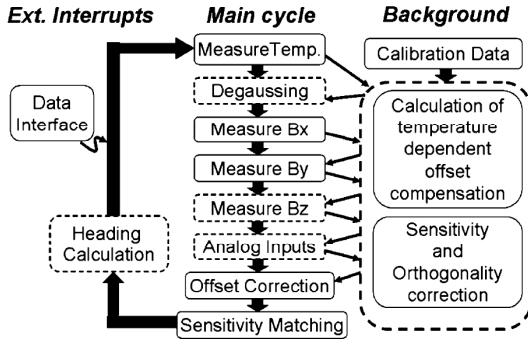
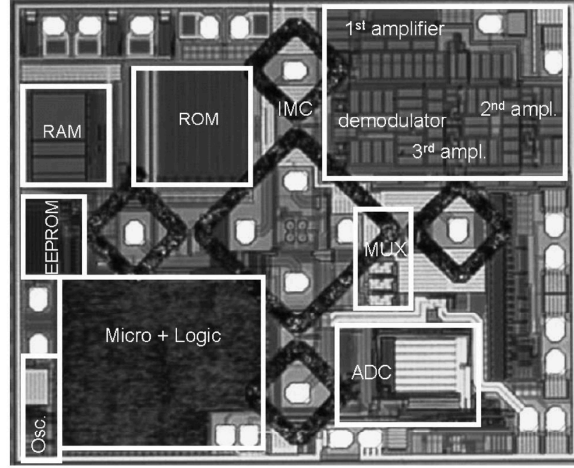


Fig. 23. Microcontroller performs the calibration of the acquired data and the heading calculation in an interrupt controlled loop. The minimum process steps are marked with solid lines, and the other steps are optional.

By using the on-board EEPROM, parameters like offset fields, axis selection, analog gain, and interface protocol (I2C or SPI) can be defined. Those parameters allow the end-user to entirely calibrate the single-chip compass even in the presence of magnetic field distortions caused by ferromagnetic objects, e.g., batteries, sensor housing, or car body. The sensor can also digitize four analog inputs from external sensors and transmit the results to a host system via the on-board digital interface.

VII. REALIZATION

The sensor chip has been realized in low-voltage 0.35 μm mixed-signal CMOS technology (Fig. 24). The five-octagon

Fig. 24. Realization of the electronic compass chip in 0.35 μm mixed-signal technology.

IMC structure is placed in the center, and about half of the chip area is used for analog and the other half for digital circuitry.

After completion of the CMOS process, the IMC layer is applied and photolithographically structured. The on-chip degaussing coil is then completed during the wire bonding to the package leadframe. The compact die size of 2.3 mm $\times$ 2.8 mm allows for packaging into a standard 20-pin plastic package, with outside dimensions of only 5 mm $\times$ 4 mm $\times$ 1 mm.

Due to rigorous low-voltage design of all circuit parts, the compass sensor works within a supply range of 2.2–3.6 V and features a current consumption of 5 mA in normal-power mode and less than 2 mA in low-power mode. Degaussing is performed before every acquisition cycle. The degaussing rate is programmable.

VIII. MEASUREMENT RESULTS

The output characteristics of the packaged sensor were measured by using a 3-D Helmholtz coil. The X - and Y -axes' sensitivity is programmable between 0.9 and 58 LSB/ μT , while the Z -axis sensitivity is about six times smaller due to the lack of IMC gain.

A. Resolution

The sensor acquires consecutively every 40 ms data on X and on Y . This results in a complete magnetic reading within 80 ms. Adding another 5 ms for the computation results in a full reading update every 85 ms. The heading resolution, which we obtain as the peak error for repetitive measurements at a given heading, was measured to better than 0.5°. This corresponds well to the 40 dB from our initial estimation.

B. Rotation in Earth Magnetic Field

The angular error of maximum 1.5° was measured by rotating the sensor within the earth magnetic field at constant temperature (Fig. 25).

The raw magnetic hysteresis of the IMC depends on the applied field strength. However, after degaussing the IMC ring, the maximum hysteresis is below 0.2 μT .

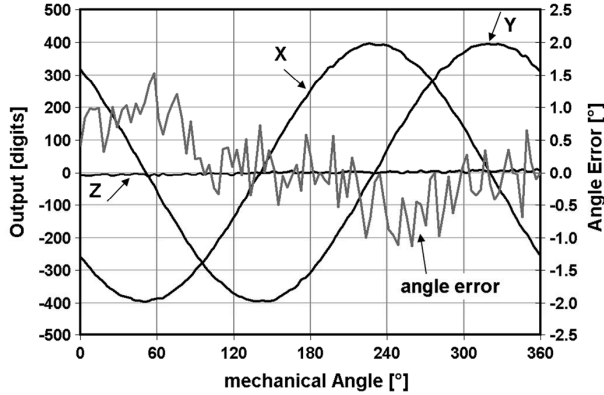


Fig. 25. Sensor output for a 360° rotation in the earth's magnetic field (20 μ T).

C. Offset Drift With Temperature

The first measurements on offset drift over the temperature range from -25°C to $+100^{\circ}\text{C}$ at a sensitivity set to 7.25 LSB/ μT show a value of 100 LSB on X and Y . This drift is relatively high compared with other recent work [9], and it has its origin in the variation of local stress with temperature under the edge of the IMC where the Hall elements are placed. The on-chip microcontroller is therefore used to apply a second-order drift compensation. As shown in Fig. 26, the remaining drift for X is reduced to less than 10 LSB, which corresponds to about 1 μT , which is an acceptable value for the application.

For Y , however, we obtained with the present samples only a reduction to about 2 μT (Fig. 27). Further reducing this value remains a challenge for the next sensor redesign.

D. Linearity

Nonlinearity of the system is given by the nonlinearity of the BH loop of the soft amorphous ferromagnetic material of the IMC ring. The sensor's nonlinearity was measured by a magnetic field sweep of $\text{FS} = \pm 200 \mu\text{T}$ to below 0.5% FS for X and Y (Fig. 28). The onset of magnetic saturation of the IMC is observed above 2 mT where nonlinearity was measured to 2%. Although the earth's flux density is always below 60 μT , the application may require an input range of up to 200 μT . The use of the electronic compass in the proximity of ferromagnetic materials, like car bodies, batteries, or screws, can locally amplify the flux density perceived by the transducer.

Possible host systems for such a miniature complete electronic compass system range from watches to mobile phones to automobiles. Due to its three-axis feature, the compass can either be used as conventional heading sensor, or as a recalibration reference for gyroscopes in more complex systems, or even as a three-axis low-field transducer in mapping applications.

IX. CONCLUSION

In Table I, we compare with two state-of-the-art fluxgate compass sensors with integrated metal layers [10], [11] and we summarize as follows.

Fluxgate sensors are based on continuous saturation of the ferromagnetic core. Although they are more sensitive and tem-

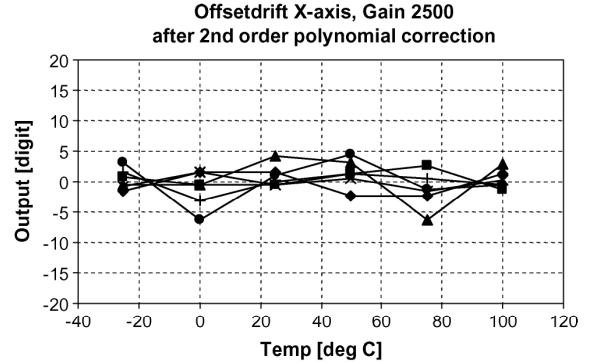


Fig. 26. For the X -axis, the remaining drift after second-order compensation is less than 1 μT .

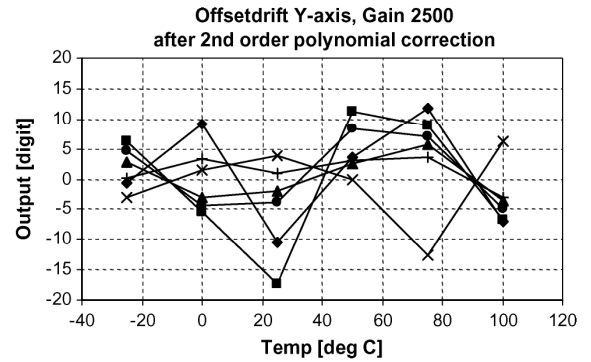


Fig. 27. For the Y -axis, the remaining drift after second-order compensation is more than 2 μT .

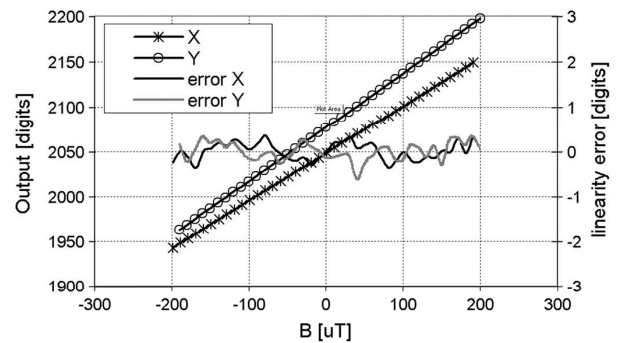


Fig. 28. $\pm 200 \mu\text{T}$ field sweep measurement with linearity error calculation for minimum gain setting.

perature-stable with higher bandwidth, they either require a lot of power or a very delicate post-processing of the ferromagnetic core. The Hall-IMC compass presented here combines the advantages of simple post-processing and low-power consumption. It is therefore well adapted for high-volume manufacturing for all applications where high bandwidth is not essential. It also has a large linear input range, so that external biasing fields from surrounding metal structures (e.g., car body) can be compensated without accuracy penalty.

TABLE I
ELECTRONIC COMPASS BENCHMARK

publication	Kawahito '99	Drljaca '04	this work
principle	fluxgate	fluxgate	IMC-Hall
technology	0.8 μ m CMOS	1.0 μ m CMOS	0.35 μ m CMOS
postprocess	electroplating	IMC + polishing + annealing	IMC
power consumption	325mW	17...35mW	30mW
linear range	<50 μ T	<50 μ T	>200 μ T
bandwidth/refresh time	unknown / -	2.5kHz/-	- / 85ms
digital signal processing	-	-	yes, on-chip μ C
output	digital	analog	digital
angular accuracy @T=300K	<4° for B=50 μ T	<1.5° for B=50 μ T	<2° for B=20 μ T

REFERENCES

- [1] M. J. Caruso, T. Bratland, C. H. Smith, and R. Schneider, "A new perspective on magnetic field sensing," *Sensors*, pp. 34–46, Dec. 1998.
- [2] J. Kubík, L. Pavel, and P. Ripka, "PCB racetrack fluxgate sensor with improved temperature stability," *Sens. Act. A*, vol. 130, pp. 184–188, 2006.
- [3] P. M. Drljaca, P. Kejik, B. Janossy, and R. S. Popovic, "Low noise CMOS micro-fluxgate magnetometer," in *Proc. 12th Int. Conf. Solid State Sens., Act., Microsyst.*, Boston, MA, Jun. 8–12, 2003, vol. 1, pp. 304–307.
- [4] K. Mohri and Y. Honkura, "Amorphous wire & CMOS IC based magneto-impedance sensors: Origin, topics and future," in *Proc. 6th Eur. Magn. Sens. Act. Conf.*, Bilbao, Spain, 2006.
- [5] R. S. Popovic and C. Schott, "Magnetic field sensor and method for operating the magnetic field sensor," U.S. patent App# 0164080, Aug. 2007.
- [6] R. S. Popovic, R. Racz, and C. Schott, "A new CMOS hall angular position sensor," *Technisches Messen*, vol. 68, pp. 286–291, Jun. 2001.
- [7] R. Racz, C. Schott, and S. Huber, "Electronic compass sensor," in *Proc. IEEE Sensors*, Oct. 24–27, 2004, vol. 3, pp. 1446–1449.
- [8] P. Rombouts and L. Weyten, "A versatile Nyquist-rate a/d converter with 16–18 bit performance for sensor readout applications," *Integr. VLSI J.*, vol. 39, no. 1, pp. 48–61, 2005.
- [9] J. van der Meer *et al.*, "A fully-integrated CMOS hall sensor with a 4.5 μ T, 3 σ offset spread for compass applications," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 6–10, 2005, pp. 246–247.
- [10] S. Kawahito, C. Maier, M. Schneider, M. Zimmermann, and H. Baltes, "A 2-D CMOS microfluxgate sensor system for digital detection of weak magnetic fields," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1843–1851, Dec. 1999.
- [11] P. M. Drljaca, P. Kejik, F. Vincent, D. Piguet, F. Gueissaz, and R. S. Popovic, "Single core fully integrated CMOS micro-fluxgate magnetometer," *Sens. Act. A*, vol. 110, no. 1–3, pp. 236–241, Feb. 1, 2004.



Christian Schott (M'01) received the M.S. degree in electrical engineering from the Technical University Karlsruhe, Karlsruhe, Germany, in 1992, and the Ph.D. degree from the Swiss Federal Institute of Technology Lausanne (EPFL), Lausanne, Switzerland, in 1999 in the field of Hall sensors.

Since 2000, he has been with Sentron AG, Zug, Switzerland, which in 2004 became part of Melexis. He is responsible for the research and development of future magnetic sensor technologies and system architectures for automotive and consumer applica-

tions, and his interests include sensors in general and magnetic sensors in particular. He holds more than ten patents and has written numerous articles in IEEE and other journals.



Robert Racz was born in Switzerland in 1967. He received the Dipl. Ing. degree in electrical engineering from the University of Central Switzerland for Applied Science, Lucerne, Switzerland, in 1991, and the postgraduate degree in microelectronics from the Microswiss Institute, Rapperswil, Switzerland, in 1995.

In 1991, he joined Landis and Gyr as an R&D Engineer working in the solid-state physics group. In 1993, he joined Sentron AG, Zug, Switzerland, where he was involved in the development of various micro-sensor-systems, interface electronics, magnetic field instrumentation and on novel CMOS Hall sensors for accurate current sensing and two- and three- axis position sensing. Since 2004, he has been with Sentron, a Melexis Company, where he is responsible for the product marketing of novel magnetic sensor products based on the technology of integrated magnetic field concentrators.



Angelo Manco was born in Lecce, Italy, in January 1979. After completing his diploma project on the development of human-computer interface for physical disabled users at the University of Applied Sciences Rapperswil, Rapperswil, Switzerland, he received the degree in electrical engineering.

Since the beginning of 2006, he has been with Sentron AG, a Melexis Company, Zug, Switzerland, as an Application Engineer for position-, compass-, and current-sensors. He is responsible for the magnetic characterization of the CMOS single-chip

electronic compass.



Nicolas Simonne was born in France in 1974. He received the Dipl. Ing. degree in industrial computing and electronics from the Science and Technical Institute of Grenoble (ISTG), Grenoble, France, in 1998.

From 1998 to 2000, he was with the European Organization for Nuclear Research (CERN) as an Electrical Engineer, where he was in charge of the software and hardware development for a test facility for super-conducting cable for the Large Hadron Collider (LHC) project. Since 2000, he has been with Melexis, Tessenderlo, Belgium, a major European automotive circuit manufacturer. Starting as a Test Engineer in the Hall-effect sensor business unit, he switched to the position of Analog Designer where he realized the CMOS Single-Chip Electronic Compass with embedded micro-controller. He is now a Project Leader for the current and future generations of E-Compass for automotive and consumer industries.