conductivity values similar to those of silicon oxides. As high-speed devices will generate more heat, such relatively-high thermal-conductivity represents a significant benefit. Manufacturers of OSG-CVD-systems include Applied Materials and Novellus.

A CVD-low-*k* film using organosilane and ozone was also recently reported.[25] This film can be easily integrated into an interconnect scheme that employs W- plugs and Al-lines. In the CVD process, the Si-H-bond of the organosilane precursor is selectively broken by an active O_3-molecule to form a highly mobile $Si(CH_3)_x$-intermediate to achieve good step-coverage and gap-filling between metal lines. Void-free filling was achieved at spacings of 0.12-μm and an aspect-ratio of 5:1. A post-deposition-anneal at 400°C polymerizes and forms a low-*k* film. A cap PECVD-oxide film is deposited over the low-*k*-layer to avoid direct CMP of the low-*k*-material. With the capping oxide, the normal ashing and cleaning process can be applied to remove resist-residue and etch by-products. The W-via-filling process is straightforward after standard de-gas and liner-deposition. No via-poisoning was observed after the W-CMP step.

14.5.2.2 2nd Generation Low-*k*-CVD Films: *FlowFill*® CVD Films: The *FlowFill*® films from Trikon Technologies are OSG-films (silsesquioxanes) deposited with a thermal-CVD process using a mixture of methylsilane and hydrogen peroxide (H_2O_2) gases.[26] These react in the gas-phase to form methylsilicic acid, which condenses on a cool wafer (i.e., the wafer is kept cooled to 0°C during the deposition process). The condensed material takes the form of a methyl-substituted oxide-gel that contains a considerable amount of water. The high flowability and surface-tension of this gel enables it to seamlessly fill gaps and provide a significant degree of local planarization. After deposition, this gel is converted into an amorphous methyl-doped silicon-oxide by a higher temperature cure in a separate chamber. That is, annealing at 400°C drives-off the water and densifies the film, leaving a high-quality methyl-incorporated silicon-oxide-film (which has a porous structure and a low dielectric constant). Figure 14-7 shows the process flow of this CVD approach.

The FlowFill-films exhibit a *k*-value of 2.8 and can be used for gap-filling applications in a subtractive-aluminum interconnect-process, or a Cu-damascene-process. For gap-fill, the deposition sequence involves first putting down a plasma-deposited base-layer, then depositing the low-temperature flow-layer and performing a cure step (and finally capping this layer with a standard PECVD film). The overall *k*-value of this composite-film is ~3.1. FlowFill layers can also be deposited thicker (to > 1.5-μm) with a modified cure step. This allows a

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U.S. Patent 7,579,227

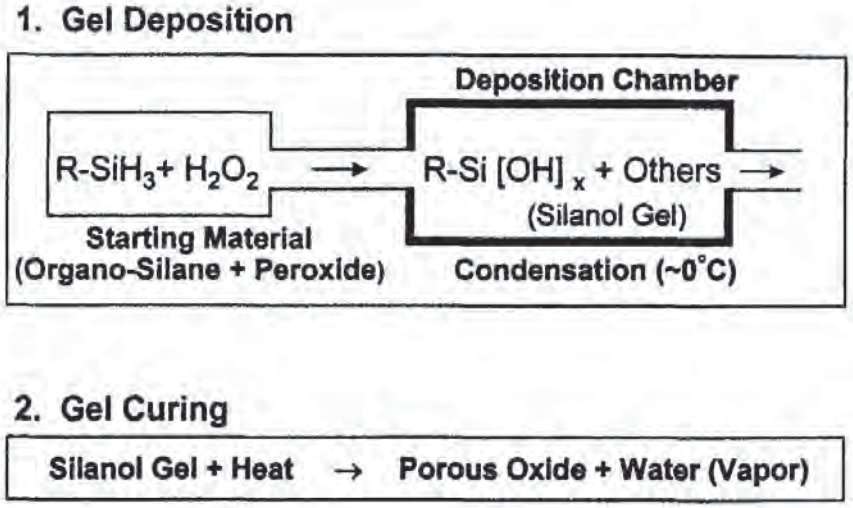

Fig. 14-7 Trikon *FlowFill*® CVD approach for depositing silsesquioxane films.

simple extension to timed-etch damascene structures using the same hardware and tool platform (i.e., the Trikon Planar® system). The film is attractive because its properties are very similar to spin-on glasses, whose process integration issues are well understood. However, its impact on circuit performance is limited by the need for encapsulation by the PECVD-SiO_2 capping layer.

14.5.2.3 2nd Generation Low-*k*-CVD Films: Black Diamond™ and Coral™ CVD Films: Applied Materials has developed a modification to the CVD OSG-films that they have termed Black Diamond.™ In this approach, a near-room-temperature PECVD-process is used to deposit a silsesquioxane film using the same organo-silane precursors, but with gaseous oxidizers like O_2 or N_2O instead of H_2O_2. By going from a cool deposition process (as is used in the *FlowFill* approach of Sect. 14.5.2.2) to a warmer one, Applied said it could eliminate the post-deposition furnace-cure step while positively influencing film-hardness and surface-roughness. This also produces an as-deposited film that already has a silsesquioxane type of porous structure, and which exhibits a *k*-value of about 2.7. Depending on the deposition temperature, curing may still be necessary to outgas the trapped reaction byproduct from the film. In addition, the high sticking-coefficients of the gaseous reactants result in poor step-coverage and gap-fill capability. Thus, Black Diamond films can be used as an inter-metal dielectric only in damascene interconnect schemes.

Applied Materials also claims that the same tool set used to deposit the first-generation FSG-films can also be used to deposit their Black Diamond films. This will allow the same equipment base to be used through several generations.

Applied Materials also announced that this material was validated for sub-0.18-μm devices by International SEMATECH.

Novellus calls their CVD OSG-films Coral.™ Their k-value is 2.7. Novellus claims that through process optimization, the hardness of the Coral film has been improved sufficiently so that it can be used in standard plastic packages. To protect the OSG-layer from attack during resist removal, a capping layer of SiO_2 is CVD typically deposited onto it (although SiC-layers are also being introduced).

14.5.2.4 2nd Generation Low-*k* -CVD Films: Parylene CVD-Films: Parylene (poly-*p*-xylylene)-based polymers are one of the most promising low-k CVD materials. Parylene polymers are high molecular weight (20,000-50,000 amu) linear chains of phenyl groups isolated by ethyl groups at the para positions. Figure 14-8 shows the different types of parylene polymers. The parylene precursors are low-melting-point solids that are composed of molecular dimers. The deposition consists of heating the solid in the presence of a carrier gas so that the dimers are carried to a cracking-furnace. The thermal energy in the furnace splits the dimers into the individual parylene monomers. The carrier gas then brings the monomers into a deposition chamber where they condense onto a wafer at temperatures below 0°C. Polymerization and cross-linking occur even at such low temperatures because the monomers are very reactive radicals. Parylene has a dielectric-constant of about 2.6. It does not absorb moisture, but is stable only up to about 300°C. Fluorinated parylene (parylene-F) exhibits a higher thermal stability (400°C). Parylene aliphatic tetrafluorinated poly-*p*-xylylene (parylene-AF4) demonstrates a k-value of 2.25 and even higher thermal-stability (greater than 450°C). Also it does not absorb moisture. A CVD process for depositing parylene AF4 is also commercially available from Novellus.[27]

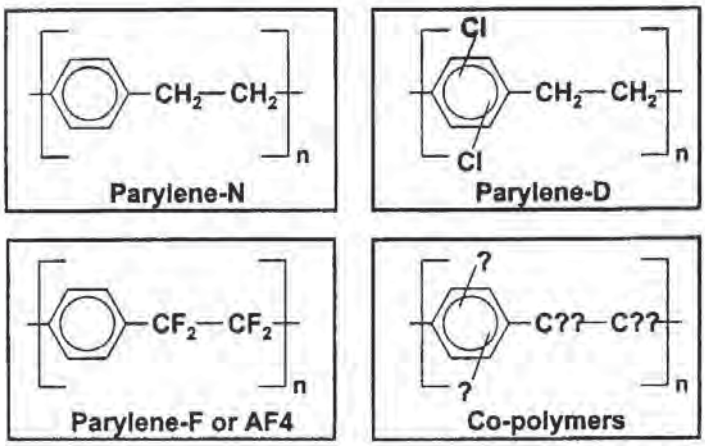

Fig. 14-8 Different types of parylene polymers.

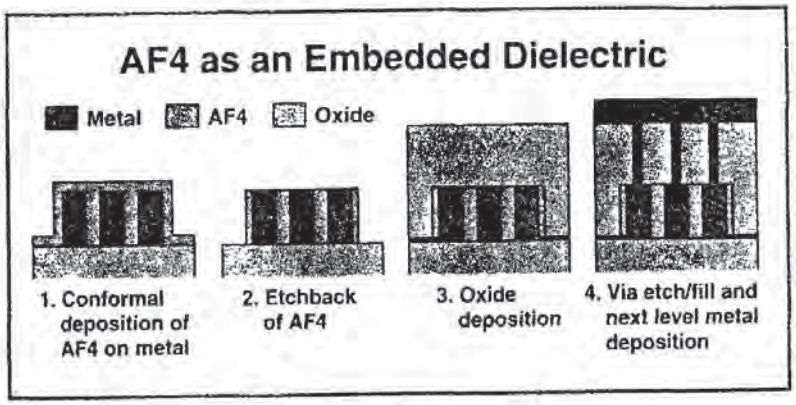

Fig. 14-9 In this integration scheme, the low-k material is encapsulated between the closely spaced metal lines where the low-k dielectric has its greatest influence on RC-delay. The interlevel dielectric is oxide, which has superior mechanical and thermal transport properties. Reprinted with permission of Semiconductor International.

In a subtractive Al-based interconnect structure, the parylene-AF4 layer is deposited first to conformally cover the Al lines. It is then etched back until the tops of the metal lines are exposed, at which point an oxide capping-layer is CVD deposited (Fig. 14-9). The parylene-AF4 remains in the spaces between the metal lines, where it does the most good in reducing side-by-side capacitance. The oxide above the metal lines is available as a layer through which via-etching takes place (a process that is mature). The chemical-vapor-deposition of parylene materials is a well-established technology, but the mechanical strength and applicability to via and damascene processes is still being researched. Adhesion is reportedly adequate for ULSI interconnect applications.[27]

14.6 ULTRA-LOW-k DIELECTRICS: (k < 2.3)

Ultra-low-k dielectric materials are also being investigated for their suitability as IC interconnect layers. Several different types were being considered, and are mentioned here. These types of ultra-low-k materials have not yet been proven for production-worthy devices. Specifically, according to the 2000 edition of the ITRS, it appears that such materials will not be included in commercial products until at least 2005.

One reason that ultra-low-k materials will be needed is that future high-performance circuits will use a copper damascene approach. Thus, the low-k dielectric likely be used in conjunction with an etch-stop (or polish-stop)

dielectric layer (which will have a higher dielectric constant). Consequently the *k*-value of the ultra-low-*k*-layers will need to be decreased so that the overall dielectric constant of such ILD-stacks can meet the desired *k*-value specifications. Furthermore, adhesion of the low-*k* material to the other materials in the structure may also involve use of *dielectric-liners* with higher *k*-values. Many of these liners will probably be new to semiconductor processing.

Note that numerous ways of producing films with $k < 2.2$ are available. However, all of these methods invariably rely on reducing the density of the dielectric material. The most commonly used approach is based on a porous-silica structure (although silsesquioxane and aromatic-organic-materials have also been formed into porous films). These types of films, however, exhibit deterioration of the mechanical properties with decreasing *k*-values, as shown in Table 14-4.[28] In order to improve the mechanical properties of the porous films, a number of methods are being pursued. For films produced by the standard sol-gel technique (see later paragraphs in this section for more on sol-gels), particular attention must be given to the gelation and aging procedure, and to the termination of bonds on the interior pore walls (which typically requires an additional process step of some kind (e.g., thermal or plasma). However, silsesquioxane-based precursors reportedly can be treated with a sol-gel technique without requiring additional pore-wall passivation. In order to produce sol-gel films with more order and uniform pore size, self-organization stimulated by surfactant templating has been utilized. (Note that the information contained in this paragraph was presented at the Ultra-Low-*k* Workshop sponsored by SEMATECH in March 1999.)

Besides the sol-gel techniques, porosity has been introduced into dielectric films by burning out sacrificial material.[29] Another porosity producing method involves the interpenetration of a low-*k* constituent with a silica structure that is formed by standard SOG coat and bake procedures. One such approach involves depositing a multiphase film by CVD (that contains one film material that has a thermally-unstable phase). This is followed by an anneal (400°C for 8 hours), which removes this labile phase from the material. The dual-phase materials used in this study were deposited by PECVD from mixtures of SiCOH precursors with gases containing mainly carbon- and hydrogen-atoms. Following the anneal, the *k*-value was found to be reduced to 2.4 from its pre-annealed value of 2.8. Efforts are also being undertaken to produce porous dielectrics by PECVD using organosilicate glasses from a number of silane-based precursors.

The challenges of integrating such porous ultra-low-*k*-materials in copper damascene are formidable. Not only must they meet the low-*k* requirements, but

the films should possess properties as close to the incumbent SiO_2-based materials as possible. These properties include low leakage-current, low thermal-coefficient-of-expansion, high dielectric-breakdown-voltage, low film-stress, low moisture-absorption, good adhesion to other materials, high thermal-conductivity, and mechanical-strength. Realistically, the materials properties of porous ultra-low-*k*-films will not match those of silicon dioxide, because they are compromised when pores are incorporated into a dielectric. Balancing low-*k* performance with sufficient mechanical properties (to survive mechanically intensive processes such as CMP), is one of the most significant hurdles facing ultra-low-*k* materials.

The first of the ultra-low-*k* materials considered here are the nanoporous-silica (SiO_2) xerogel materials whose *k*-value can be tuned from $k = 1.3$ to $k = 2.5$ (by varying the film porosity). Since the *k* of air is 1.0, by making a dielectric layer porous, more of it consists of air, and thus its overall *k*-value is lowered. In xerogels air is trapped as bubbles in a solidified gel. Xerogels are formed by evaporation drying, with some shrinkage. One commercial version is offered by Honeywell (formerly Allied Signal) under the name of Nanoglass.™ It was originally developed in 1996. In temperature testing of nanoporous-silica, feasibility studies indicated that such films are stable up to 500°C. Porous organic polymers are also being examined as low-*k*-layers. Note that all such porous materials (i.e., both oxide- and organic-based), must withstand such process steps as CMP, etching, and heat treatments without degradation of the pore structure. Other spin-on porous materials include porous-SiLK (from Dow Chemical), and porous versions of FLARE and HOSP (from Honeywell).

Dow-Corning has developed a spin-on film consisting of an interconnected pore structure based on HSQ-resin named XLK. In 2000 it could produce films with a *k*-value of 2.5, and the vendor claims it will be extendable to values of $k = 1.5$ in the future.[30,33] With a pore size of 2-3-nm, a 50% porosity, a tight pore-size-distribution, and a fully-interconnected network-structure, XLK appears to offer many of the characteristics needed for device integration. Pores are introduced through a three-step process on an SOD track system: **1**) gellation in the presence of a boiling-point solvent at ambient conditions; **2**) removal of the solvent without collapsing the resin structure; and **3**) formation of a strong network structure during cure near 400°C. Gellation occurs when the film is exposed to an NH_3 and H_2O environment for 30-120 seconds, which causes Si-H bonds to react with the H_2O to form SiOH. Then the SiOH bonds join together to form a SiOH gel. A plasma treatment in $H_2/N_2 + CF_4$ can be used to increase the mechanical properties of the XLK films.[31] In a single-level copper damascene

Fig. 14-10 Trench with 0.35-0.4-μm lines and spaces etched in 700-nm XLK film (ultra-low-k-dielectric) with 100-nm-thick oxide-cap-layer shows good sidewall etch-profiles.

integration study, 700-nm of XLK and 100-nm of an oxide-cap were deposited on a wafer with a 550-nm thermal oxide and a 100-nm nitride. A two-step recipe was used to etch the cap-oxide, then the low-k film, resulting in good etch-profiles (Fig 14-10). Following ashing in an HDP reactor, a 25-nm TaN barrier, with 100-nm Cu-seed and 1-μm of electroplated Cu were deposited. CMP of the structure showed no delamination. This work represented the first evidence of the feasibility of integrating an ultra-low-k film at the first-level of Cu-interconnect.

A second type of ultra-low-k-dielectric is formed with polyfluorotetraethylene (PTFE), a chemical related to Teflon (a DuPont tradename). PTFE is a chemical compound consisting of carbon and fluorine, made up of uncross-linked-CF_2-polymers (and so contains 67-at% F). A prototype spin-on version of a PTFE dielectric with a $k = 1.9$ has been introduced. The developer, W.L Gore and Associates gave it the name of SPEEDFILM. The material consists of an aqueous emulsion containing sub-20-nm PTFE particles and a surfactant. Films made with this material have good thermal-stability up to 400°C. Although Teflon does not adhere well to metals, SPEEDFILM has undergone adhesion testing (as well as CMP and etching studies). A thermal-CVD PTFE film first developed by Watkins-Johnson (now SVG Thermco Group), with a precursor from DuPont Electronic Gases Group, is also being offered.

Research continues on other ultra-low-k film materials. One possible class of candidates are porous organic-polymer materials. This is a fruitful pursuit, because if one starts with a k-value of 2.65 and makes it 20% porous, one can get

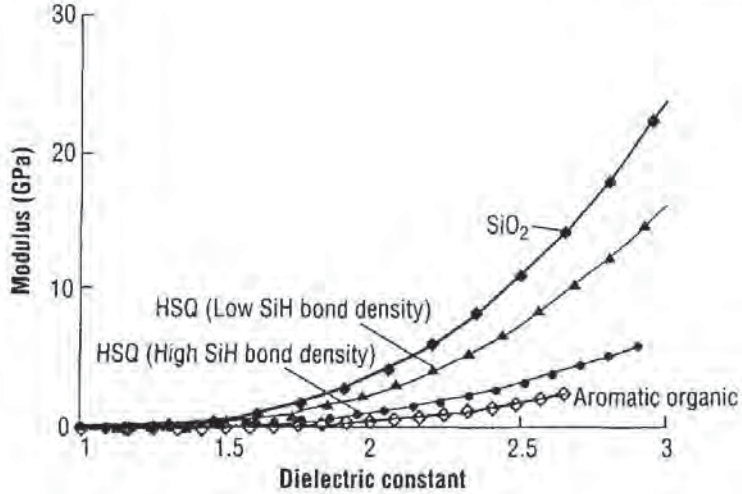

Fig. 14-11 Theoretical approximation of modulus of elasticity of porous ultra-low-k materials as a function of dielectric-constant indicates porous-SiO_2 offers the greatest mechanical stiffness.

a film with a k-value of 1.9. With an inorganic material like SiO_2 ($k = 3.9$), the film has to be 70% air to get k down to 2.0. Since the ultra-low-k films wont be commercially used until at least 2005, CVD companies still have time to develop a CVD film with a porous matrix.

In summary, the chief factor that determines the important characteristics of ultra-low-k materials is the pore structure. Each matrix material (whether it is silica-, silsesquioxane, or aromatic-organic based) has a unique pore structure.

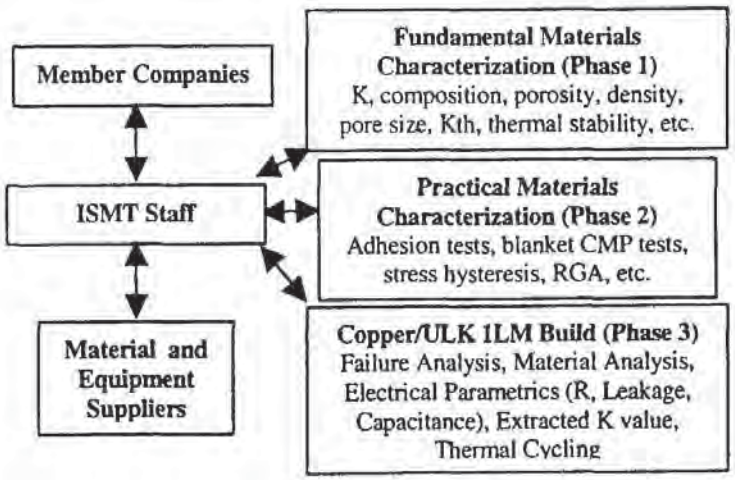

Fig. 14-12 Initial evaluation of candidate low-k materials at ISMT. The flow of information is meant to provide verification to material/equipment suppliers and probability of materials success in a two-level-metal integration.[32] (© IEEE 2001)

Material Property	Method	Specification	Guideline
K (relative permittivity)	MIS Capacitor 1MHz, RT, 40% RH	<2.5	<2.2
Thermal Stability (%loss/hr)	I-TGA In N2 and Ar, 425C	<1.0%	<0.5%
Film WIWNU, 1-sigma	Spectroscopic Ellipsometry	<3%	<2%
Young's Modulus (GPa)	Nanoindentation 1000nm thick film	>3	>4
Adhesion	ASTM Tape Pull	No Failures	No Failures
Maximum Pore Size	PALS/SANS+SXR	<25nm	<10nm
Film Quality	Visual Inspection Profilometry Light Scattering	No Striations, visual defects	Particles <100 @0.2um

Fig. 14-13 List of materials Specification and Guidelines. Specifications are the minimum expected material property, and Guidelines are the desired set of properties to ensure successful integration.[32] (© IEEE 2001)

For example, since air fills the pores, the k-value ultimately depends on that of the matrix material. In addition, the degradation of the modulus of elasticity E (which makes a material softer), is approximated by a power of the film porosity. Each type of porous dielectric-material exhibits a degradation of modulus of elasticity relative to fully dense silica (whose $E = 72$), as is shown in Fig. 14-11. Pore-size may also impact the continuity of Cu barrier-layer films, since these films are deposited with thicknesses comparable to the dimension of the pore size. Finally, compatibility with wet-chemical processing is influenced by pore structure. Open or connected pores are prone to absorb wet chemicals (such as water). Since the k-value of water is 72, any retained moisture in the pores degrades the dielectric constant. More details on this topic are given in Ref. 34.

One further change when ultra-low-k-dielectrics are used may involve going away from via-first dual-damascene interconnects (the approach most commonly used in 2000). With porous material, via-etching cannot be done first because after via opening the trenches are etched, and problems arise with resist absorption into the porous sidewalls of the via (see Chap. 15, Sect. 15.9.1.2).

Late in 2001 a report from Wetzel at International Sematech (ISMT) outlined a study that was being conducted there on candidate materials for ultra-low-k

ILDs.[32] Figure 14-12 shows the general scheme for the initial evaluation of such materials. The list of materials specifications sought for ultra-low-*k*-dielectrics is shown in Fig. 14-13. They suggested that integrating such low-*k* films into a dual-damascene process will face three main challenges: **1**) the ability to successfully survive CMP processing (especially with respect to the mechanical strength and adhesion of the films); **2**) the compatibility of ultra-low-*k* materials with DUV resist must be improved, especially when following a via-first dual-damascene approach; and **3**) porous-silica films must be able to maintain their initial *low-k* values through the processes that occur after the films are formed.

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Chapter 15

DUAL-DAMASCENE INTERCONNECTS

As the submicron era evolved in the 1990's, several novel manufacturing methods were adopted to keep pace with Moore's law. One such approach, namely the formation of interconnect structures with *damascene processes* was chosen to fabricate IC interconnects. In this chapter we describe this technique.

15.1 DAMASCENE VERSUS SUBTRACTIVE INTERCONNECT STRUCTURES

The conventional way of fabricating each conducting layer of an interconnect structure of an IC is a so-called *subtractive process*. In such a subtractive process, a blanket metal film is deposited onto an insulator-covered wafer surface (with contacts - or vias - having been previously etched in the insulator layer - Fig. 15-1). Next this metal film (e.g., Metal-1) is patterned by etching - to create metal interconnect lines. Finally a dielectric film is deposited over these etched metal lines. Vias are then etched in the overlying dielectric film to allow connection passages for the next layer of metal that is to be deposited onto the dielectric film covering the Metal-1 lines. This subtractive approach requires several process capabilities: **1**) It must be possible to effectively etch the metal and; **2**) It must be possible to deposit both the dielectric and metal layers with a deposition process that has good gap-filling capability. In some interconnect schemes (especially as the ICs are scaled below 0.5-μm), it becomes difficult if not practically impossible, to meet these goals. For example, for technology nodes smaller than 0.5-μm it is desirable to replace Al with Cu as the intercon-

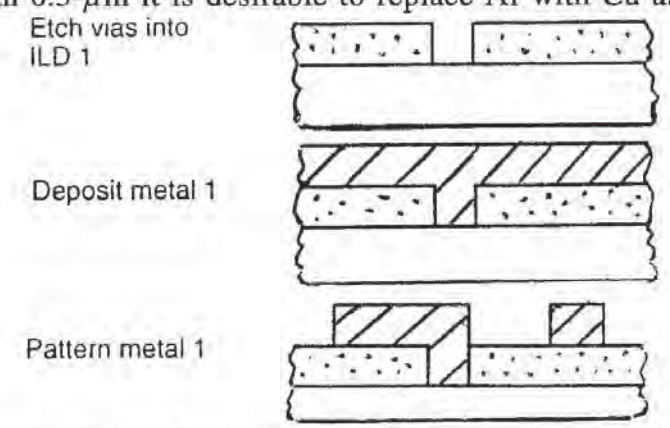

Fig. 15-1 Subtractive approach to forming interconnect structures for ICs.

nect conductor (i.e., because Cu has a higher conductivity than Al, and also exhibits superior electromigration characteristics). However, since it is difficult to etch Cu, an interconnect scheme that does not require Cu etching would be preferable. In addition, as the spaces between metal lines become smaller, it becomes progressively harder to fill such narrow gaps with an insulator film. Again, a significant advantage would be gained if it were possible to use a process that does not require gap-filling when insulator films are deposited. To achieve the above goals, an alternative interconnect fabrication technology to the subtractive method has thus been developed, called the *damascene method.*

15.2 DAMASCENE STRUCTURES AS ALTERNATIVE DEEP-SUBMICON INTERCONNECTS

In the damascene approach to forming interconnects on ICs, a trench is cut into the dielectric layer and then filled with metal. (The term *damascene* is derived from the decorative practice of creating metal inlays, as developed by the artisans of Damascus in the Middle Ages.) This method thus provides two major advantages over the subtractive method of forming interconnect structures:

1. In the damascene approach, no etching of the metal layers is required. The metal-etch process of the subtractive approach is replaced with a metal chemical-mechanical-polishing process (CMP). The metal-CMP step removes any metal deposited above the top surface of the trench (including the regions where the metal is deposited on the dielectric surface). This leaves a planarized dielectric surface with metal inlaid in trenches of the dielectric. Since the CMP process leaves a globally planarized surface, *the need for filling narrow gaps during the dielectric deposition process is eliminated.* The only gap-filling capability required by the damascene approach is during the deposition of metal into the recesses of the dielectric. Since metal etch (especially the etching of Cu) and dielectric gap-fill are viewed as two of the greatest challenges in the drive to smaller dimensions, elimination of these steps represents a major benefit. On the other hand, filling of even narrow, high-aspect-ratio trenches with metal (i.e., with W by CVD, or Cu by electroplating) is not as difficult.

2. There is only a bottom interface for Cu (versus top and bottom interfaces for Al-alloys with W plugs). This helps reduce overall via resistance.

We will also see that by using a *dual-damascene* process, the number of processing steps is smaller than for the subtractive approach. Hence, use of dual-damascene interconnects may also result in lower manufacturing costs. The

damascene approach was pioneered by IBM, and began to appear in commercial IC products at about the 0.25-μm node.[1]

15.3 SINGLE-DAMASCENE INTERCONNECT STRUCTURES

Damascene interconnects can be formed with either a *single-damascene* or *dual-damascene* process. The dual-damascene process offers the advantage of reducing the number of process steps, and thus most of our discussion focuses on it. However, the single-damascene process is always carried out on at least the first level of a multi-level interconnect structure of an IC. For this reason, it is useful to begin with a description of the single-damascene approach.

In the *single-damascene process* (see Fig. 15-2 [and Fig. 12-10 in Sect. 12.1.4]), the interlevel dielectric layer (ILD) is planarized after it is deposited. Next, a contact (or via) is patterned with a lithography step, and then the contact opening is etched into the ILD layer. After completion of the contact-hole etch step, a metal plug is formed in this opening - typically by blanket deposition of the metal, followed by an etchback or CMP step to form the plug (e.g., a W-plug). Thus, the surface of the dielectric containing the metal plug after such an etchback or polish step is globally planar (see Fig. 8-92). The metal lines of the interconnect level are formed next. This can be done using a subtractive process, as described in Sect. 15.1, or with another single-damascene process.

Assuming a single damascene process is applied twice (first to create plugs, and second to create metal lines), the second time it is employed involves the following process steps (Fig. 15-2). Another dielectric layer is deposited over the

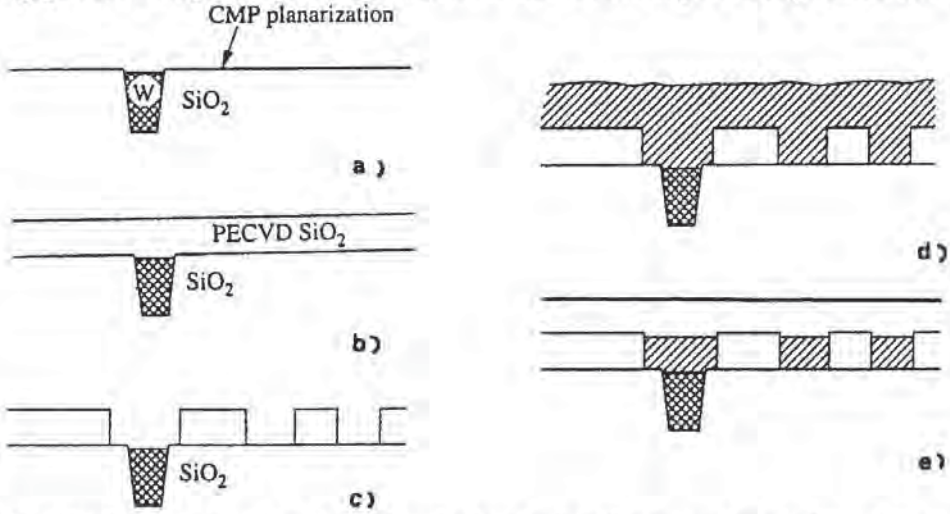

Fig. 15-2 A *single-damascene* process (applied twice) to form one level of an interconnect structure: (a) W-plugs formed after the SiO_2 is planarized; (b) IMD is deposited by CVD; (c) A trench is etched in the IMD; (d) Metal is deposited to fill trenches; (e) CMP metal.

underlying, plug-containing layer. This overlying dielectric film therefore also remains planarized. A second lithography step is then used to form the pattern of a trench, which is aligned to the previously fabricated via plug. With this aligned trench pattern acting as a template, a trench or groove is etched into the planarized overlying ILD. After the resist pattern is stripped, the trench is filled with a metal (such as aluminum or copper).[2] This metal is polished back by CMP to create a metal line embedded in a dielectric trench, and in contact with the underlying plugs. Finally, another dielectric layer is deposited onto the dielectric layer containing the metal-filled trenches. This dielectric layer will be the one through which the next level of vias (or holes to the contact pads) will be created.

It is worth emphasizing several important aspects of the single-damascene process: **1**) If CMP is used to form both the plug and the metal in the trench, no metal etch process is needed; **2**) No gaps have to be filled by the dielectric-film-deposition processes; **3**) The process still contains about the same number of steps as the subtractive interconnect process (i.e., the two polish steps replace the via and metal etch steps of the subtractive process, and the two metal-deposition steps replace the metal-plug-deposition step and main-metal-line deposition step of the plug/metal-line subtractive interconnect process); and **4**) Since the first-level interlevel dielectric layer is planarized before the contact holes are etched, *contact holes* will generally have different depths (e.g., those going to the substrate will be deeper than those going to the gates). Thus, to allow all contact holes to be opened, the shallower ones will expose the underlying material to the plasma etching reactants during the time the deeper contacts are being opened. To prevent the underlying material in the shallow contact holes from being attacked during this time, an etch-stop layer is often deposited after the salicide process is completed (typically using Si_3N_4 as such an etch-stop film). After the contact etch is completed, the nitride etch-stop layer is removed, Since the thickness of this layer is uniform on all regions, it can be etched away with a much shorter overetch time. This method allows all of the contact holes in a single-damascene process to be opened without damaging the underlying material on any part of the die.

15.4 INTRODUCTION TO DUAL-DAMASCENE INTERCONNECT PROCESSES

In a *dual-damascene (DD) structure*, only a single metal deposition step is used to simultaneously form the main metal lines and the metal in the vias. That is, both trenches and vias are formed in a single dielectric layer. The vias and trenches are defined by using two lithography steps (Fig. 15-3). Trenches are typically etched to a depth of 4000-5000-Å, and the vias are typically 5000-

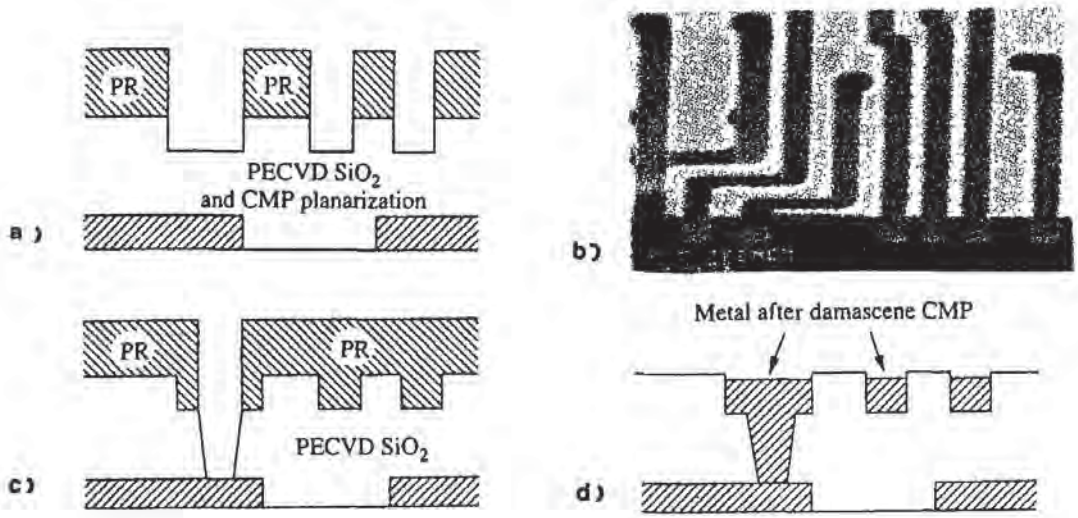

Fig. 15-3 *Dual-Damascene* process: (a) IMD is deposited by CVD and planarized by CMP. Trench is defined by PR #1 and then etched; (b) SEM of the etched trench after PR #1 has been stripped; (c) Vias are defined by PR #2 and then etched, using PR #2 to protect other regions of the IMD from etching; (d) Metal is deposited to simultaneously fill trenches and vias. CMP is used to remove excess metal. The sequence is repeated for the next level of metal.

7000Å-deep. After the via and trench recesses are etched, the via is filled in the same metal-deposition step that fills the trench. After filling, the excess metal that is deposited outside the trench is removed by a CMP process, and a planar structure with metal inlays is achieved. As in the single-damascene process, once a planarized surface is achieved, it is no longer necessary to perform CMP on the dielectric layers. Thus, one of the CMP steps needed for each metal level in the subtractive interconnect process is also eliminated.

It should also be mentioned that in early dual-damascene processes, the trench dimension was somewhat wider than that of the vias. This made the alignment of the via to the trench somewhat easier. However, with time, the via and trench widths have been made equal. (At the 0.18-μm node, the via and trench widths are 0.22-0.24-μm wide, while at the 0.13-μm node they will probably be ~0.18-μm wide.) Thus, modern dual-damascene processes are more sensitive to misalignment between the trench and via. However, this overlay sensitivity problem is mitigated to some degree by the nature of the damascene process, making it possible to maintain high interconnect packing density. That is, the alignment of the trenches to the vias in the dual-damascene sequences is an easier task than in the subtractive interconnect process. In the latter, aligning metal lines

to the underlying contact holes (or vias) must be done after the opaque, shiny, blanket-metal film has been deposited. In damascene approaches, aligning the trenches to the vias is done through the transparent dielectric film, which allows tighter design-rule tolerances to be used when performing this alignment.

When comparing the single-damascene process to the simple dual-damascene process described above, one observes one metal-deposition step and one CMP step are eliminated in the latter (as well as one dielectric-deposition step). The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes. Note that in single-damascene structures, plugs are typically filled with W, but in the dual-damascene-interconnects the metal that fills the holes is Al or Cu. The technology of filling of vias and trenches with Cu is described in Chap. 16. A dual-damascene process using Al was described by workers at IBM in 1998.[3]

15.5 THE THREE DUAL-DAMASCENE PROCESS SEQUENCES

Three different fabrication sequences have been developed to produce dual-damascene structures:

1. Trench-First Dual-Damascene
2. Via-First Dual-Damascene
3. Self-Aligned (or Buried-Via) Dual-Damascene

It should be noted that the *via-first* and the *trench-first* sequences are the processes currently being used in mainstream production. The trench-first sequence was probably the first one to be adopted, but the via-first sequence is currently the approach that has gained the greatest acceptance (and will likely remain so going forward). As a result, we will focus on these two sequences, and will point out the advantages and drawbacks of each one. While the third approach (the self-aligned process), has not been implemented in production (for reasons we will also explain), we will provide a brief description of it as well. However, whichever sequence is used, the final damascene structure is the same (see Fig. 15-4).

Before outlining the three dual-damascene processes, it should be mentioned that the dielectric layer in which the trenches and vias are etched actually consists of at least three layers of dielectric (see Fig. 15-8b). That is, SiO_2 (or a low-*k* dielectric is deposited to a depth of 5000-7000Å (and this will be the layer in which the *vias* will be etched). Next, a thin silicon nitride layer - or other material (which will serve as an *embedded etch-stop layer*), is deposited (about 30-nm thick). Finally, another SiO_2 layer (or a low-*k* dielectric layer) is deposited

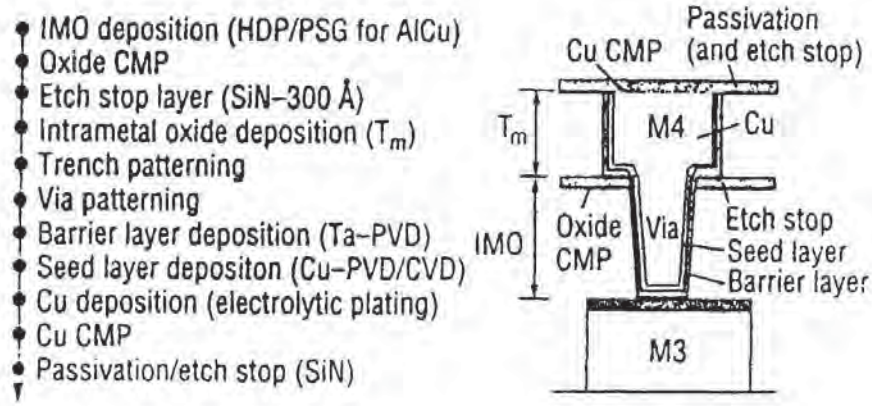

Fig. 15-4 A suggested dual-damascene-based Cu metallization flow and resulting cross-sectional structure.[8] Reprinted with permission of Solid State Technology. Published by PennWell.

(~4000-5000-Å thick). This will serve as the layer in which the *trenches* will be etched.

In the *trench-first* sequence (Fig. 15-5), the trench patterns are defined in the ILD first. That is, after spinning on the resist, the trench-pattern-mask is used to expose the resist. The trench is then produced by etching the dielectric down to the embedded etch-stop layer. After the trench-etching process, the first resist layer is stripped. A second resist layer is then spun on, and the via-pattern-mask is used to create openings in this resist layer - aligned to the trench that was etched previously. The resist protects the other parts of the wafer surface (including the etched regions of the trenches) so that the vias can be etched without further etching the dielectric in the trenches.

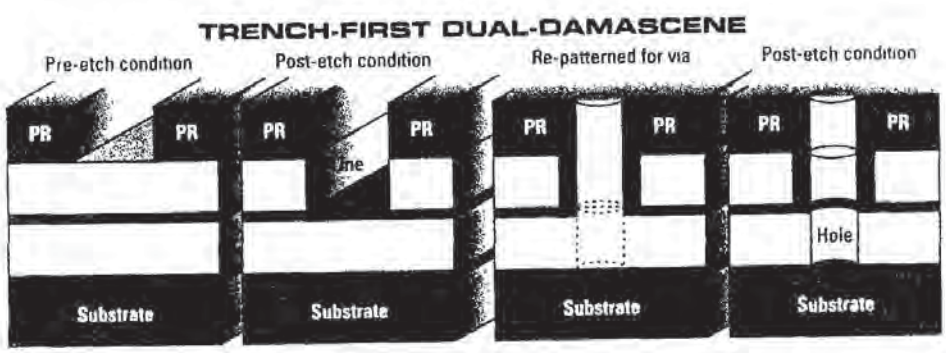

Fig. 15-5 In the trench-first approach, the vias are patterned & etched after trenches are etched.

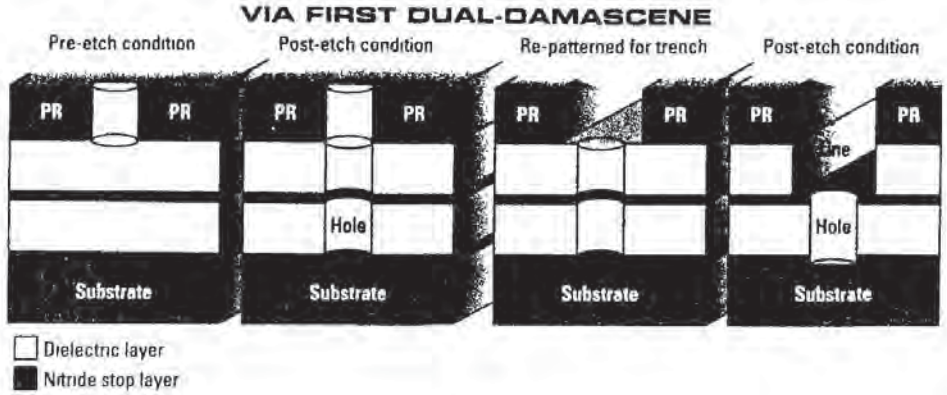

Fig. 15-6 In the via-first approach, the trench is patterned and etched after the via is formed.

The chief disadvantage of the trench-first sequence involves the fact that the vias must be patterned after the trench etch. That is, since resist is applied as a liquid onto the wafer surface, it fills recessed regions as water fills a lake. Hence, the top surface of the resist is planar. This means that the regions of resist over the damascene trenches is quite thick. Resolving fine features in thick resist is harder than in thinner resists. For features smaller than 0.25-μm the process latitude becomes too small for this to be a practical manufacturing process. Thus, while the trench-first sequence could be used for early dual-damascene processes (0.35-μm and some 0.25-μm processes), it is difficult to extend it to smaller technology nodes (i.e., in order to able to use it at such small dimensions, it may be necessary to implement a thin imaging-resist-layer process, as discussed later).

In the *via-first approach* the vias are defined first in the ILD, followed by patterning the trenches. As noted above, this is currently the most common method of fabricating dual-damascene interconnects (and is schematically shown in Fig. 15-6). The sequence of forming the damascene recesses in this approach begins by exposing the *via patterns* with the first mask. After etching the vias completely through the entire dielectric stack (except not through the barrier layer at the bottom of the dielectric stack) and stripping the resist, a second mask is used to pattern the trenches. The trenches are then created by etching the dielectric down to the embedded etch-stop layer. The barrier layer at the bottom of the vias is protected from further etching during the trench-etch either by resist or a BARC layer (applied for the trench-etch step) that floods the vias, or by using an etch process that is highly selective to the bottom etch-stop material (i.e., so that the etch-stop layer at the bottom of the via is not removed during the trench-etch step). After the resist is stripped and the etch-stop layer at the bottom of the via is removed by dry-etching, the metal that fills both the vias and the

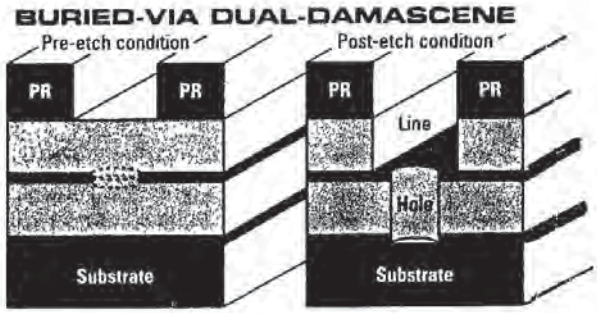

Fig. 15-7 In the self-aligned, or buried-via approach, a hard mask is patterned and etched. The trench and via can be etched in one step.

trenches can be deposited. After deposition, it is polished back to create the dual-damascene structure.

In the *self-aligned* dual-damascene process (Fig. 15-7), the via pattern is created in the embedded etch-stop layer with a lithography-and-etch sequence that is performed before the top dielectric layer of the stack is deposited. A special etch process is required for this step. After the via pattern is thus etched, the top dielectric layer is deposited. Finally, the trench mask is aligned to the via openings in the embedded nitride layer, and both the trench and via are opened with a single etch step. This sequence requires nearly perfect trench-to-via alignment, otherwise the via may no longer be round (but instead only half-moon shaped), resulting in high via resistance. In addition, an etch-process with high nitride-to-oxide selectivity is required. For these reasons this scheme has not found use in production.

15.6 THE EVOLUTION OF DUAL-DAMASCENE FROM SiO_2 TO LOW-*k* DIELECTRIC STACKS

In the first generation of dual-damascene processes (i.e., at the 0.25-μm node), Cu was used together with a conventional undoped PECVD-SiO_2 dielectric (with a PECVD-SiN layer beneath the SiO_2, which acts as both a Cu diffusion barrier and an etch-stop when the vias are etched, Fig. 15-8a).* The nitride and oxide layers may be deposited sequentially in the same tool (e.g., a PECVD reactor).

* This SiN layer is deposited first, and as noted, serves as a barrier against the diffusion of Cu between metal levels and also as an etch-stop in the dielectric etch that defines the vias. Because SiN has a high value of k, this layer should also be as thin as possible to avoid adding significantly to the interlevel capacitance. At the same time, the SiN layer must be low-stress, dense, and pinhole–free, so that its diffusion-barrier properties are not compromised. High-density is also critical to the nitride layer's role as an etch-stop.

This Cu/SiO_2 structure gave improved interconnect performance over the Al/W-plug subtractive process because Cu interconnects (i.e., with Cu in both the lines and vias) have a lower resistance than Al lines combined with W-plugs. Thus, the RC delay term was reduced through a decrease in R. A significant problem that occurs with using this dielectric structure is that the trench formation has no etch stop. Since the trenches are etched to an intermediate point part way through the dielectric layer, within-wafer etch-non-uniformity translates directly into within-wafer non-uniformity of the trench depths.

In second generation dual-damascene processes (down to about the 0.18-μm node), the CVD-SiO_2 material was replaced by a first generation low-k material, namely a PECVD-SiO_2 layer doped with fluorine (*fluorinated silicate glass, FSG*) whose $k = 3.5$. (FSG has many properties similar to SiO_2 and thus requires the smallest number of process integration changes.) A SiN layer, embedded halfway through the thick dielectric layer, was also added to the dielectric stack to serve as an etch-stop layer when the trenches are etched. However, since the k value of SiN is $k = 7.0$, the embedded-etch-stop SiN layer increases the net-k value of the resulting dielectric stack. In fact, the overall capacitance of the FSG dielectric stack with an embedded-SiN etch-stop layer was about the same as that of first generation SiO_2 layers - but it had the benefit of being able to ensure the trench is only etched halfway through the dielectric layer. The corresponding drawback is that fabricating a multi-layer dielectric stack adds cost and complexity to the manufacturing sequence.

The next step in the evolution of the dual-damascene dielectric stack was to incorporate a second generation low-k material ($k = 2.7$) into both the upper and lower segments of the dielectric stack, as this now allows the wiring capacitance to be reduced. (Note that the wiring capacitance is reduced by about 11% when a SiLK/SiN dielectric stack is implemented, compared to the wiring capacitance obtained when using a FSG/SiN stack.*) The first dual-damascene structure that incorporated a 2nd generation low-k dielectric in the stack (together with Cu), was announced by IBM in April 2000. It was intended for use in the IBM's Cu-15

* In a paper published in late 2001, an alternative dielectric stack to the SiLK/SiN stack was proposed. That is, it used FSG and a new embedded layer material (SiCN), whose k value of 5 is lower than that of SiN. The capacitance of this stack was about 9% lower than that of the FSG/SiN stack, making its wiring capacitance comparable to the SiLK/SiN stack. However, the authors claim that the SiLK/SiN stack is mechanically weak, and tends to fail during bonding and packaging processes, whereas the FSG/SiCN stack is more robust.[5]

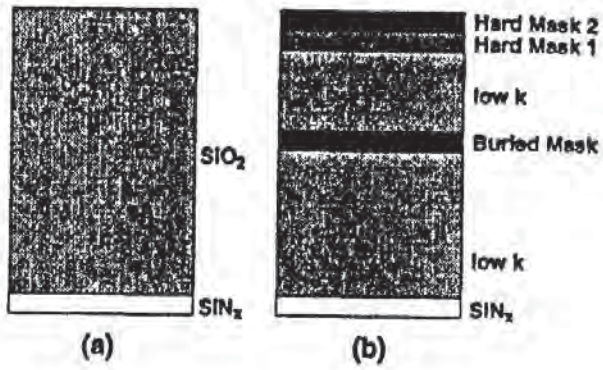

Fig. 15-8 a) First generation dual-damascene ILD stack, consisting of SiO_2 and a bottom SiN layer. b) Later generation dual-damascene ILD stack with low-k dielectric, embedded etch-stop layer, and hard-mask/capping layer (SiO_2).

0.13-μm CMOS technology.[4] The low-k dielectric material selected for this process was SiLK^{TM} from Dow Chemical (see Chap. 14). The dual-damascene process is used to form the #2 through #5 interconnect levels of the 5-level-metal interconnect structure used for this technology node.

It should also be noted that when a 2nd generation low-k dielectric replaces the FSG (or SiO_2) material in the stack, a hard mask must also be added to the top of the stack. The material chosen by IBM for this hard mask was SiO_2, giving the dielectric stack a structure as shown in Fig. 15-8b. SiO_2 was selected for this role because it has a significantly lower k-value than SiN. In addition, this SiO_2 hard mask remains in place during metal deposition, so it can later serve as a polish-stop during metal CMP. Since use of an SiO_2 hard mask maintains the same materials system encountered during the CMP of metal and a PECVD-SiO_2 dielectric stack (Cu/TaN/SiO_2), the developed consumables, equipment, and processes for Cu-CMP on plain SiO_2 should be extendable to Cu-on-SiO_2-capped low-k. However, since this oxide cap becomes a primary supporting structure against material loss by dielectric erosion during CMP, the allowable dielectric erosion (see Sect. 8.11.1) in a capped dielectric stack is dramatically decreased.

It should also be noted that in some cases different materials may be used for the dielectric at the via level than for the trench level. Since most of the capacitive coupling issues that a low-k material helps solve are encountered between adjacent metal lines, the *trench dielectric* will be where the lowest-k

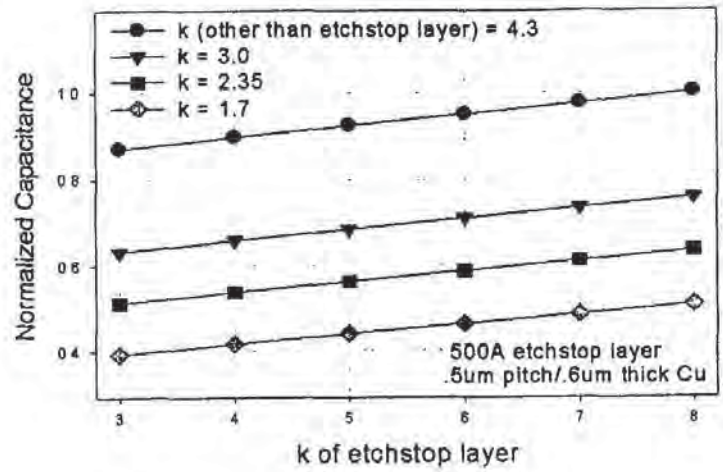

Fig. 15-9 Capacitance impact of the *k*-value of the etch-stop value in a dual-damascene structure for various dielectric constants. [32]

materials are first used. Since the via dielectric is less critical from a capacitance perspective, implementing a low-*k* material there may be delayed.

The use of SiN as an embedded etch-stop layer increases the capacitance. Figure 15-9 shows the effect of a 500-Å SiN on dielectric stacks with different low-*k* dielectrics.[32] To allow the capacitance of the dielectric stack to be reduced even further, a new material has been introduced to replace SiN for the embedded-etch-stop and hard-mask roles. This material is SiC (with $k = 4.5$). Figure 15-10 shows how much the use of Si-C instead of SiN reduces the effective *k*-value of the damascene dielectric stack.[33] Applied Materials introduced this material in 1999 under the name BLOk (barrier low-*k*).[6,7] In

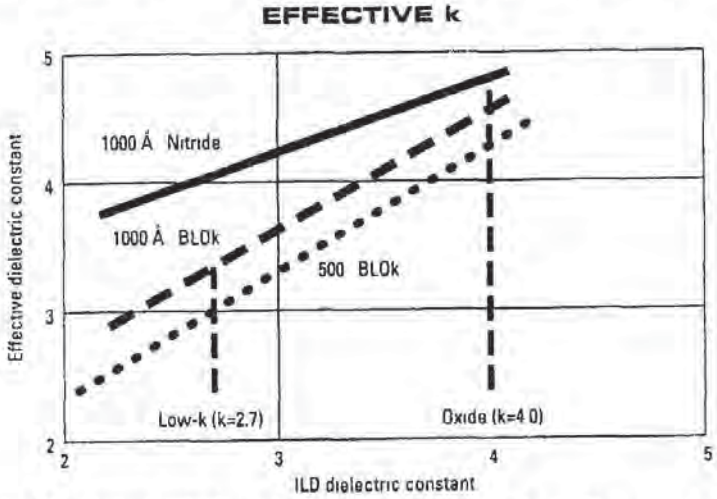

Fig. 15-10 The SiC-based dielectric barrier impacts the effective *k* value much less dramatically than the traditional nitride film. Courtesy Applied Materials.

addition, this material offers twice the etch selectivity of nitride to oxide-like films, has better Cu diffusion barriers than nitride, and shows good adhesion ot SiO_2, FSG, and organic-based low-k dielectrics. Furthermore, it exhibits the optical properties needed to make it behave like an anti-reflective coating in DUV imaging. The film is deposited in an HDP-CVD chamber using trimethylsilane at 350-400°C. The resulting Si-C film can also be etched using a "soft etch," which means it can also be used as the capping layer for Cu (i.e., at the bottom of the via of the via-first dual-damascene structure). Some companies have reportedly incorporated the Si-C films into damascene dielectric stacks which employ undoped SiO_2 or FSG, while others are using it with stacks containing lower-k films. Another vendor that supplies a tool and a process to deposit such an Si-C film is Novellus.

It is thought that the Si-C material will replace SiN as the etch-stop layer in low-k dielectric stacks for the 0.13-μm node. However, as devices are scaled even further, it is predicted that even the k value of 4.5 of Si-C will prove to be too large. Thus, it has been projected that at the 0.1-μm node, the embedded-etch-stop layer will be removed entirely. The ramifications of removing the embedded etch-stop layer will be discussed in a later section.

15.7 TRENCH-FIRST DUAL-DAMASCENE PROCESS FLOW

Here we present an example of a trench-first dual-damascene process flow, using undoped SiO_2 as the main dielectric material and Cu as the main interconnect metal. We assume that an STI isolation structure is used, so that the substrate is flat, up to the time of gate-stack formation. We will also see that both single-damascene and dual-damascene processing are used. Many variations of this example damascene-interconnect structure have been published.[8,9,10,11,12] Some advanced interconnect structures may elect to use both conventional W-plugs and etched Al-wire interconnects for some metal levels, and Cu-damascene for others. One such example is given in Ref. 13.

The fabrication sequence of this interconnect structure is begun by carrying out two single-damascene process sequences to form both the Metal-1 lines (Cu) and CVD-W plugs in the contact holes. The first process sequence is started by depositing a dielectric layer over the gate stack. This film serves as the *pre-metal dielectric* (PMD) layer in this structure, and it is polished flat with a CMP step. Vertical contact holes are etched into the PMD layer. A CVD-W process is then used to fill the contact holes. The W is then planarized, so that W-plugs are formed such that their top surface is flush with the top surface of the PMD.

The second single-damascene process is then performed. That is, an additional

dielectric film is deposited onto the PMD layer, and trenches (aligned to the W-plugs) are etched into it, deep enough so that the tops of the W-plugs are cleared of dielectric. A liner film (e.g., TaN) and a Cu seed-layer are sequentially blanket-deposited deposited by PVD. The main Cu film is then blanket deposited by electroplating. The Cu film (and TaN liner layer) are polished off of the top surface of the dielectric film with CMP, leaving the Metal-1 Cu lines inlaid in the grooves. The main challenge here is to obtain the same polishing rate on the tantalum nitride (which is a hard refractory-metal-containing nitride), and the copper (which is comparatively soft). This completes the formation of the Metal-1 and contact plugs by two single-damascene processes. The surface of the wafer is flat for the next dielectric film deposition.

The subsequent layers of metal are formed by a dual-damascene process sequence. The sequence begins by depositing a thin, low-stress silicon nitride layer. This layer forms a top encapsulation layer on the level-1 inlaid Cu lines, and also acts as an etch-stop layer when the vias are etched in the dual-damascene sequence. Next, a dielectric layer (here, undoped SiO_2) is deposited by a CVD process to a thickness required for the via-hole depth. Since the surface is flat, gap-filling by this layer is not required. Then, the embedded etch-stop layer is deposited by CVD (typically PECVD-silicon-nitride with a thickness of 30 nm). Finally, the inter-metal-dielectric stack (IMD) is completed by depositing a second dielectric film, whose thickness is determined by the next-metal-level thickness. (Note that the multi-layer dielectric film, containing two nitride etch-stop layers adds cost and complexity, as well as increasing the interlevel capacitance of the interconnect stack.) Photoresist is applied to the wafer surface. The trench pattern in the resist is formed by exposing the resist through a mask containing this pattern (Fig. 15-5). An etch step is performed next, with the etch creating the trenches in the upper part of the IMD stack. The trench etch is stopped by the silicon-nitride etch-stop layer embedded in the dielectric stack. The resist is then stripped, and a second layer of resist is applied. Another mask (this one containing the via pattern), is used to expose the second resist layer, with the via aligned to the previously etched trench-pattern. The via pattern is then etched in the lower part of the IMD stack. This may be a two-step etch process, as etching the nitride etch-stop layer at the bottom of the via to expose the Cu of Metal-1 may require a separate plasma chemistry than the one used to etch the underlying oxide material. Note that in practice, the trench width may be only slightly larger than the via width.

After the second resist layer is stripped, the formation of the metal line is begun. Again, a TaN (or Ta or TiN) liner and a Cu seed layer are sequentially

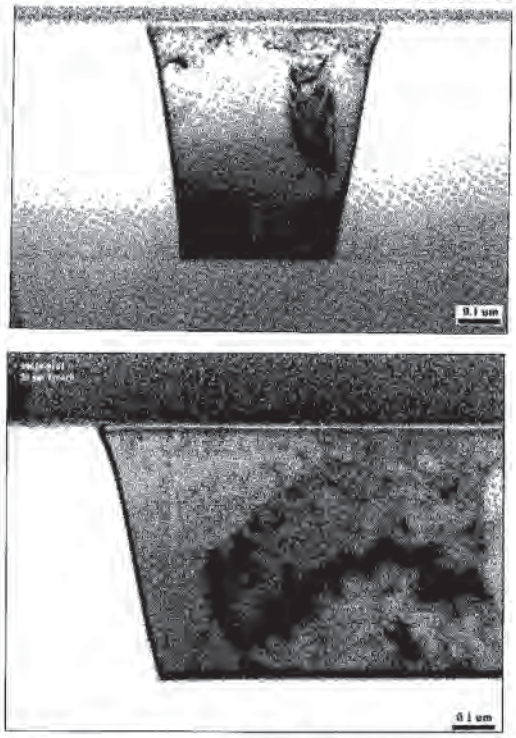

Fig. 15-11 SEM of an in-laid copper line in a dual-damascene interconnect-structure.[34] Reprinted with permission of Semiconductor International.

deposited. This may require an ionized-metal-plasma sputtering process, as the via hole is quite deep and has a high aspect ratio. The main part of the Cu interconnect is then deposited by electroplating. Note that both the via and the trench are filled simultaneously. A metal-CMP process is then used to remove the excess metal. A passivation/etch stop layer (silicon nitride) is deposited onto the top of the layer containing the grooves (trenches + vias) in the dielectric. This completely encapsulates the Cu with diffusion barriers. The entire interconnect structure is finally covered with an SiO_2/SiN passivation layer. Figure 15-11 shows an in-laid Cu-line in a dual-damascene interconnect structure.[34]

15.8 VIA-FIRST DUAL-DAMASCENE PROCESS WITH SiO_2 DIELECTRIC STACK

Many of the issues of forming the vias and trenches in the via-first process are common with the trench-first process and were described above. These include use of a single-damascene process to form the first layer of metal, and technologies for filling the damascene recesses with metal and polishing it back with CMP. We also assume that the via-first dual-damascene structure is being formed on the first level of metal, which has been covered with a SiN layer (that acts both as an etch-stop to the via etch and a barrier layer covering the top surface of the Metal-1 copper layer, to prevent its diffusion into the Si substrate).

However, there are also issues particular to the via-first sequence, and we will discuss them here.

For the purposes of opening this discussion, we assume that the dielectric stack consists of CVD-SiO_2/SiN/CVD-SiO_2. (The implications of using low-*k* material instead of SiO_2 in the stack were described in Sect 15-6.) The vias in this sequence are, of course, patterned first, using the via mask to align the vias to the Metal-1 lines produced previously (Fig. 15-6). The etch process used to open the via needs to be a multiple-step process because the first etch mechanisms must be *non-selective* (so that they can etch both SiO_2 and the embedded SiN etch-stop layer at about the same rates). However, the nitride capping layer at the bottom of the via should not be removed, and thus the etch mechanisms operating when the vias are close to being opened must be *selective* (to nitride).

After the via s are opened (but with the barrier-SiN layer at the bottom of the vias remains intact), the first layer of resist is stripped. Note that since SiO_2 is used in the dielectric stack, it can withstand the resist-stripping process (i.e., no extra hard mask is needed, as will be the case when most low-*k* materials are used in the ILD stack). The second layer of resist is then applied, and the trench mask is aligned to the opened vias. Note that the nitride at the bottom of the via must also remain intact throughout second (i.e., trench-etch) process.

Three methods are used to prevent removal of the nitride during trench etch:

1. The resist applied for the purpose of patterning the trenches will flood the open vias. If this resist is not exposed during the trench-patterning exposure step (i.e., because it is so deep beneath the top surface of the resist layer, that some may not develop after the exposure step. Thus, it remains to protect the via bottoms). However, due to pattern-density issues discussed later, such resist remaining in the vias may vary in thickness across the circuit. Thus, this approach will not always work.

2. A trench-etch process is used that is highly selective to the SiN that remains at the bottom of the open vias.

3. A bottom-anti-reflective coating (or BARC) is spun-on to partially (or completely) fill the open vias. This BARC remains after the resist is developed to protect the nitride at the via bottoms against the trench etch.[15] While this approach adds process control difficulties and process complexity (as the BARC must be applied, and separately removed later), this has been the method most widely adopted for preventing nitride-barrier attack during trench etching. We will continue the discussion of this approach in Sect 15.9.

In any case, the trench etch is carried out to create the trenches, stopping on the embedded SiN etch-stop layer. At that point the second resist layer is stripped.

After the second resist layer is stripped, the nitride at the bottom of the via must finally be opened. However, this procedure itself can cause some difficulties. First, the SiN-removal-step should be a "soft" etch. That is, the ions that bombard the surface being etched must not have enough energy to sputter Cu during the inevitable overetch time. If such sputtered Cu ends up on the via sidewalls it could be trapped on the wrong side of the subsequently deposited barrier-layer (exactly where you don't want it!). Another potential problem involves the possibility of slightly misaligning the via and the edge of the Cu film below. In this case a deep slit can be etched in the dielectric under the nitride. This slit would be difficult to fill with the barrier material, again leading to copper-diffusion problems. The way to avoid such slit-formation in the oxide, is to use a nitride-etch-process that is highly selective to oxide.

Another desired goal of the trench etching process is to reduce the handling of wafers between the various steps of the trench etching process (and the variability in waiting time between these steps). That is, the process actually contains four etch steps: **1**) organic ARC open (typically required for DUV resists); **2**) trench etch; **3**) resist strip; and **4**) nitride removal from the bottom of the via. Etching tools are now being made available that allow all four of these steps to be carried out in a single chamber, and use of such tools may be critical to achieving consistent device yield and lower overall cost-of-ownership.

15.9 PROCESS INTEGRATION ISSUES OF THE VIA-FIRST DUAL-DAMASCENE PROCESS WITH LOW-*k*-DIELECTRIC STACK

The process flow of forming each level of metal in a via-first dual-damascene interconnect system consists of the following steps:

- DEPOSIT Dielectric Stack (including the SiN barrier-layer over inlaid Cu);
- LITHO Step I (Via Patterning);
- Via ETCH;
- RESIST-STRIP I;
- Post-Via -Etch-Residue CLEAN;
- LITHO Step II (Trench Patterning);
- Trench ETCH;
- RESIST STRIP II;
- Post-Trench-Etch-Residue CLEAN;
- ETCH Barrier Film at Bottom of Via;

- Pre-Metal-Deposition CLEAN;
- Deposit Barrier Metal and "Seed" Cu Layer by PVD;
- Deposit Cu film by ELECTROPLATING;
- Post-Cu-Deposition ANNEAL;
- Remove Excess Cu/Barrier Metal (and do an SiO_2 Buff) by CMP;
- Post-CMP Residue CLEAN;
- CLEAN Top Surface of Cu Before Deposition of SiN Barrier/Etch-Stop Layer.

It can be seen that this process sequence contains: **1**) One Dielectric-Film-Stack Deposition sequence; **2**) Two Lithography processes; **3**) Two Resist-Strip processes; **4**) Three Etch processes; **5**) Five Cleaning processes; **6**) One CMP process; **7**) One PVD Deposition sequence; and **8**) One Electroplating (and Anneal) process.

Although many of these processes were mentioned earlier, there are some additional important process integration issues that should be discussed when considering the overall "via-first Cu/low-*k* dual-damascene" process flow. Thus, we will discuss these relevant process integration details here (Fig. 15-12). However, we will cover only those involved with Processes **2** through **5** above (since Process **1** is discussed in both Chap. 14 and in Sect. 15.6, and Process **6** is covered in Chaps. 8 and 16, and Processes **7** and **8** are described in Chap. 16).

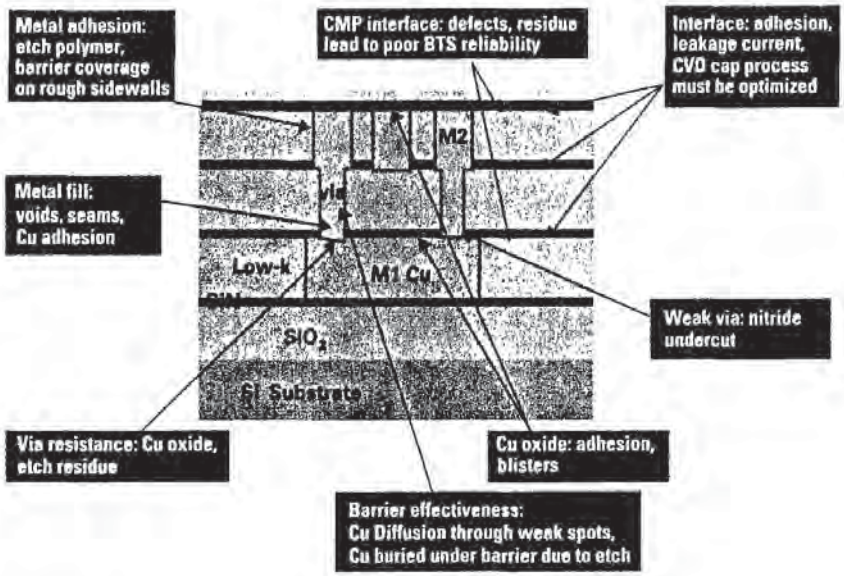

Fig. 15-12 Possible failure types associated with damascene processing pertain to film adhesion, barrier and metal fill capability, copper oxidation and CMP defects.

Besides the technical issues, there are those involving economics. In the face of increasingly difficult integration, the rise in the number of process steps per layer, and the 300-mm conversion, there will be the daunting economic challenges of containing interconnect processing cost, which in 2001 accounts for about 50% of the total wafer processing cost.[16]

15.9.1 Via-First-Damascene Integration Issues: Lithography

With the application of Cu/low-*k* dual-damascene integration, lithography and etch become more difficult because of the complex dielectric stack and intermediate topography. Here we consider the issues involved in carrying out lithography steps for the leading dual-damascene scheme, namely the *via-first approach*. There are two lithography processes needed in the via first approach, and each as its own challenges. They are: **1**) the *via-patterning lithography step*; and **2**) the *trench-patterning lithography step*.

Note that the issue of misalignment of the trench pattern to the via pattern is less severe for the via-first approach than for the trench-first approach. That is, as shown in Fig. 15-13b, even if the trench pattern and the via pattern are somewhat misaligned, since the via is already completely formed during the via etch process, it makes complete contact to the metal layer beneath it (provided it has been properly aligned to the underlying metal line). In the trench-first process, however, if the via is misaligned to the trench pattern, during the second etching step (via-etch) the entire via pattern will not be transferred to the bottom of the dielectric stack. This will cause the via resistance between the 2nd and first levels of metal to increase. Nevertheless, alignment of the via pattern to the underlying metal level below remain critical for both the via-first and trench-first processes, for reasons described in Sect. 15.9.2.3 (see also Fig. 15-13a).

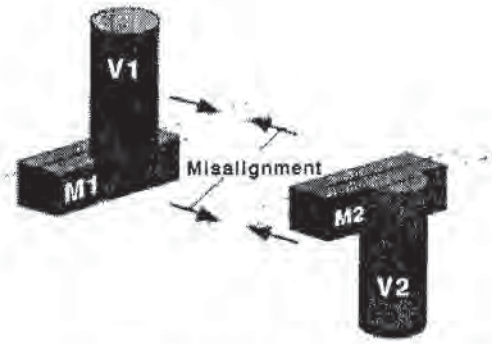

Fig. 15-13 Via-first damascene: a) Misalignment of the via to the underlying metal line is a problem; b) Partial misalignment of the trench to the previously formed via does not cause a problem because the via is completely etched through the ILD stack film.

15.9.1.1 Via-Patterning Lithography Issues: The major concern for the via-patterning lithography step is the ability of the resist to withstand the via etch process. This problem becomes worse as the vias are scaled because thinner resists have to be used to image smaller features, and the etch resistance of 193-nm resists is known to be inferior to that of 248-nm resists. The use of a bilayer resist process (as discussed in Sect. 15.9.1.3 below) may be required, since the imaging resist-layer contains silicon, making it more resistant to dry-etch attack than conventional DUV resists.

15.9.1.2 Trench-Patterning Lithography Issues - DUV Resist Poisoning: As is described in Chap. 6, DUV resists are sensitive to contamination by trace quantities of amines, a problem referred to as *DUV-resist poisoning*. While the most common source of such contamination is amines in the processing ambient, another source is amines in materials that are in direct contact with the resist. Some low-*k* dielectrics contain such amines (nitrogen compounds). For example, the SiOCH films (formed by PECVD using trimethylsilance and N_2O) entrap NH_3 products in the film as they are deposited. Such amines, if near the surface of the SiCOH films, can diffuse into and poison the DUV resist which is in direct contact with the dielectric surface. If an oxide hard mask is present on the top of the dielectric stack, the resist poisoning problem will not occur during the via-first etch. However, during the trench etch, the resist will come into contact with the exposed sidewalls of the SiOCH film under the hard mask, and resist poisoning can then occur during the trench-etch process. Performing an oxygen-plasma pre-treatment of the via sidewalls (perhaps as a part of the via-first resist stripping process) has been proposed as a way around this problem. Such a pre-treatment can leach out the amine compounds from the SiOCH surface on the sidewalls of the via. However, there is some concern that such a plasma pre-treatment may also take carbon out of SiOCH films and reduce their *k*-value.

As noted in Sect. 15.9.3, a plasma-treatment of the sidewalls of nanoporous low-*k* films with an NH_3 plasma has been proposed as a way to strengthen their surfaces against subsequent resist–stripping process of the via-patterning step. However, such a plasma-step can also trap amines in the film. These amines can later diffuse out and poison the resist during the trench-patterning step. (Figure 15-14 shows such a poisoned resist in the via after trench patterning.) Amines can readily diffuse in most low-density and nanoporous films, with diffusion lengths of hundreds of microns. The deposition processes, as well as etch and strip, must therefore be designed to avoid exposing the low-*k* film to any source of nitrogen. As mentioned above, if an SiO_2-capped low-*k* film is used, resist

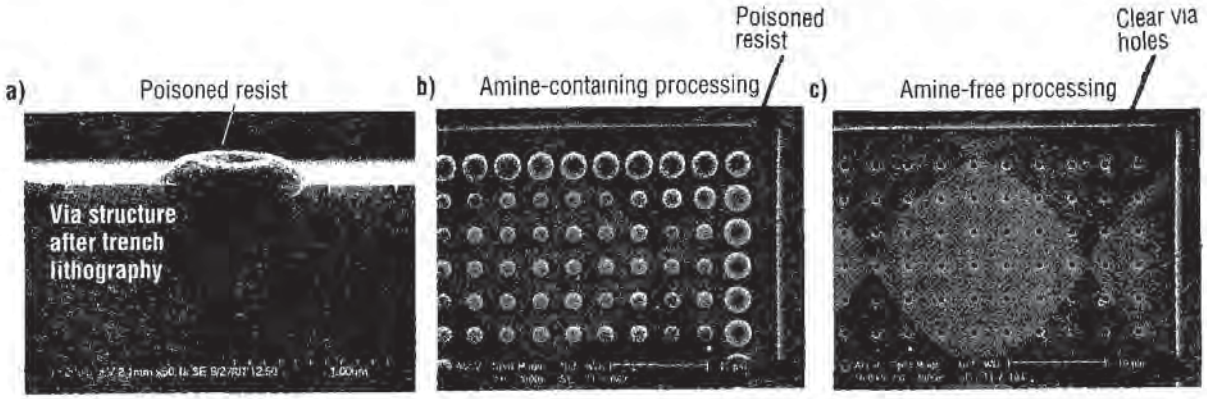

Fig. 15-14 DUV photoresist poisoning is indicated after trench patterning in a) cross-section, and in b) plan view. Poisoning was prevented in c) when the dielectric film was not exposed to nitrogen-containing plasma.[29]

poisoning may not be observed at the via lithography step, but poisoning can occur at the trench lithography step as a result of the trench-patterning resist coming in contact with exposed via sidewalls.[17]

15.9.1.3 Trench-Patterning Lithography Issues - Trench CD Control Issues: To be able to meet the stringent CD-control requirements (i.e., for trench width) for 0.18-μm technologies (and smaller), the resist film spun on a wafer should have the same thickness everywhere (to within ±100Å – see Vol. 1, 2nd Ed. Chap. 12). However, in the via-first damascene approach, since the resist floods the vias that were previously etched, the local thickness of the resist over the top surface of the oxide can be impacted by the presence of these vias. Namely, as shown in Figs. 15-15, and 15-16, the resist is considerably thinner in regions where a dense array of vias exists, compared to regions where only isolated vias exist. In addition, near the edge of such an array of vias, the resist thickness varies significantly, as also shown in these figures. Since higher resolution is generally

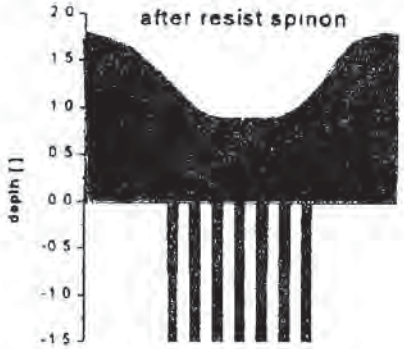

Fig. 15-15 Non-uniformity of resist layer within a chip due to pattern density variations.

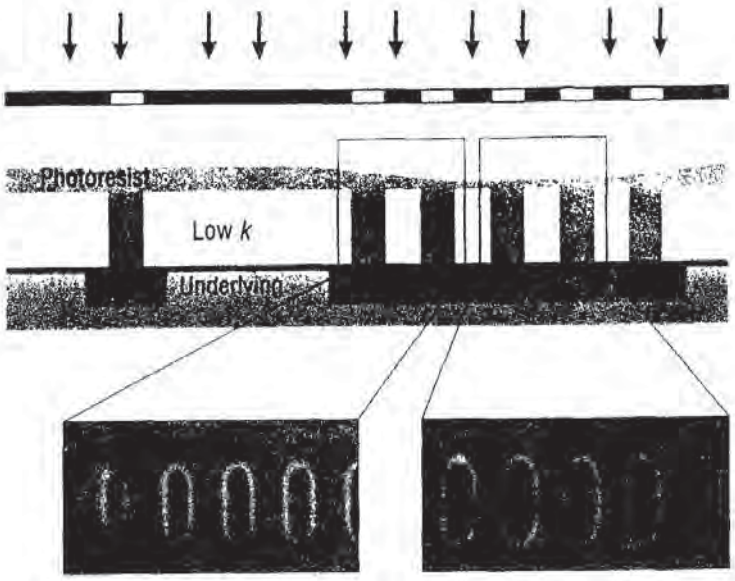

Fig. 15-16 Via-pattern density variations can lead to significant resist thickness non-uniformity during trench patterning in the via-first approach, and subsequent differences in trench widths. a) Trench widths vary at the edge of the via array. b) Trench widths do not vary at the center of the array of visas, where the local resist thickness is uniform.[20]

possible for thinner resist thicknesses, as the resist gets thicker the resolution degrades (e.g., the trench width in this case gets narrower). Figure 15-16 shows that the trench width in trenches patterned at the edge of an array of vias varies, compared to the trench widths patterned over vias at the center of the array. We will see in Sect. 15.9.1.5 that using bi-layer resist process (in which a planarizing underlayer produces more uniform resist thickness over the entire wafer) is a technique being explored to overcome this problem.

15.9.1.4 Trench-Patterning Lithography Issues - BARC Veils: Using a standard DUV lithography process for the trench patterning lithography step, a bottom antireflection coating (BARC) is applied. As noted earlier, the BARC serves two purposes. First, it improves pattern resolution by reducing substrate reflections. Second, the resulting partial fill of the vias with a BARC (Fig. 15-17b)[18] helps protect the SiN barrier layer from being attacked during the trench-etch step. This allows minimization of the barrier layer thickness. The BARC that partially fills the vias remains in place during trench etching and is removed later.

However, it is important to be able to control the depth to which the BARC fills the vias. (The BARC material that fills the via in this procedure is referred to a *via plug*.) That is if the via plug is not recessed below the buried SiN layer in

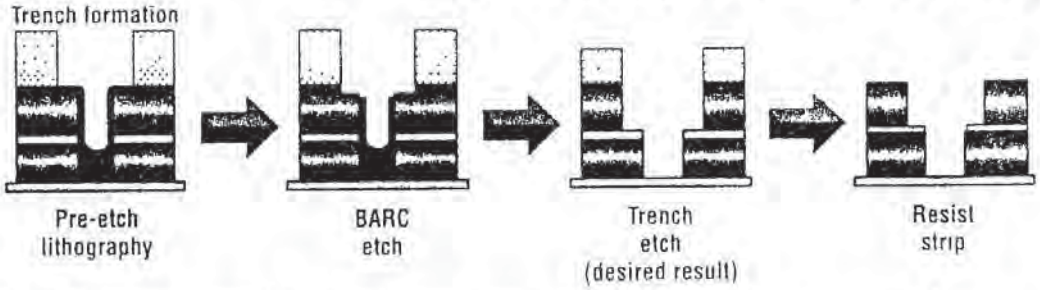

Fig. 15-17 Using a BARC to partially fill the vias prior to trench-PR deposition.[18]

the dielectric stack, "veils" (or "fences') may be created around the via opening at the bottom of the trench.

How such veils may arise is shown in Fig. 15-18. Here the BARC material (via plug) fills the via to a height that is above the top of the buried embedded-etch-stop SiN layer. As the trench is etched, the sidewalls of the via plug above the SiN layer are exposed to the etch ambient that removes the dielectric material to form the trench (Fig. 15-18a). The upwardly-protruding sidewalls of BARC can be chemically converted by an exposure to the plasma etching processes. This altered BARC-sidewall material may not be removable by the same resist stripping step that also removes unexposed BARC material. Thus, it may remain behind in the form of a "veil" surrounding the via opening. Figure 15-18b shows

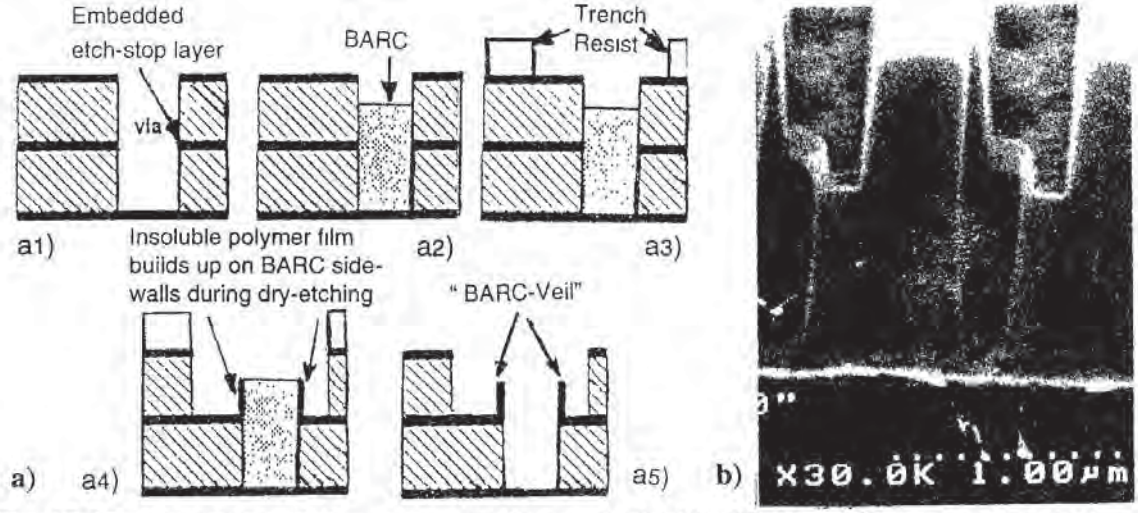

Fig. 15-18 a) BARC-veil formation mechanism in the Via-First Dual-Damascene process: **a**1) Etch Via, strip resist; **a**2) Via is filled with BARC to a level greater than that of the embedded etch-stop layer; **a**3) Deposit and pattern Trench photoresist; **a**4) Etch Trench. (*Note that during the dielectric etch step, neither the resist nor the BARC is attacked, BUT, an insoluble polymer builds up on the sidewalls of the BARC pillar that sticks up above the etch-stop layer.*); **a**5) After Trench resist and BARC are stripped, the insoluble film that was created during the dry-etch on the BARC-pillar sidewalls, remains behind as "BARC-Veils." **b**) SEM of BARC via-veils after trench-patterning and resist-strip.[18]

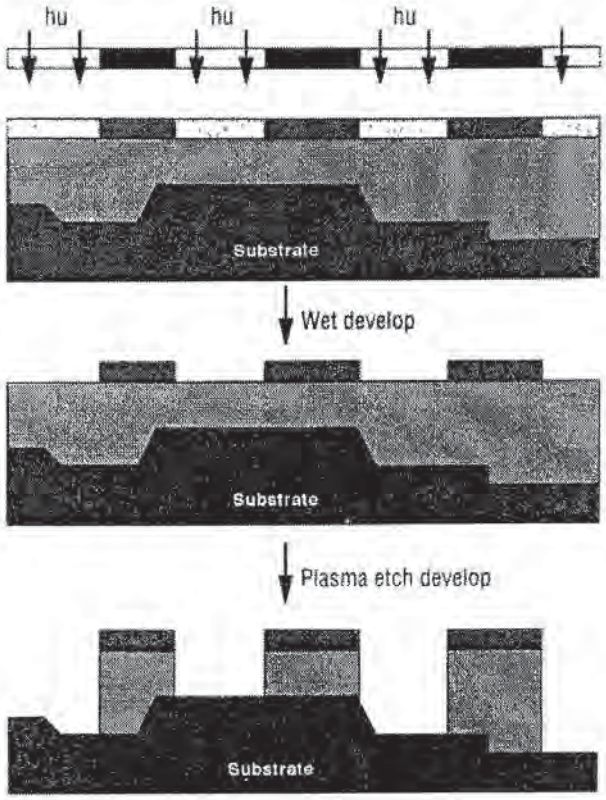

Fig. 15-19 TIS-2000 process flow with a thick planarizing underlayer and a silicon-containing imaging layer.

a SEM of such veils that remain in the trench around the via opening. Filling the trench/via openings with metal in the presence of such veils is problematic, and thus it is important that they be prevented from being allowed to form. To ensure that veils are not created by the trench etch step, it is necessary to control the degree to which the BARC fills the vias.

However, optimizing the BARC-fill of damascene vias is difficult, and often requires considerable process development and materials testing. It is possible to fill vias of different pitch equally by careful selection of the right BARC and coating conditions, but this only works if all the vias have the same size. A new BARC optimization also has to be done for each via diameter.

15.9.1.5 Bi-Layer Resist Process: To overcome the issues of resolution, critical-dimension control over arrays of vias, and the problem of via-plug depth-control that occur when the trenches are pattered in the via-first dual-damascene method, an alternative lithography approach has been proposed, namely a *bilayer, thin surface-imaging scheme* (Fig. 15-19) This method is based on a bilayer resist system developed by Arch Chemicals, called TIS-2000. The technique uses a

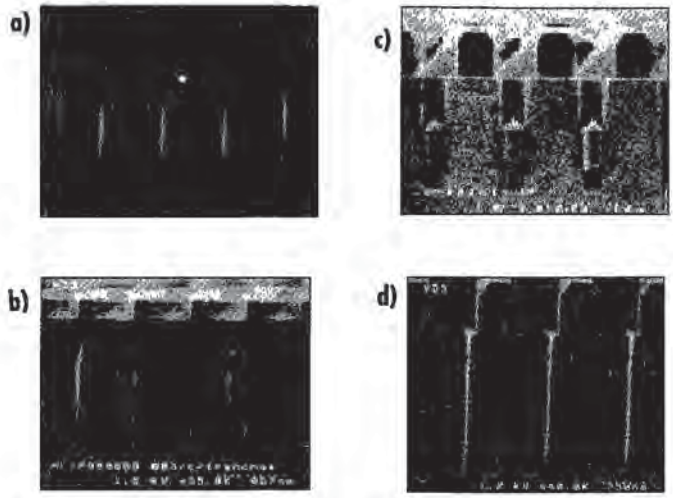

Fig. 15-20 SEMs of cleaved dual-damascene structures patterned with the TIS-2000 process: a) before exposure with vias filled; b) after wet development; c) after partial etch of underlayer and trench; d) after full underlayer etch (top resist still in place).[19]

thin silicon-containing top-imaging layer on top of a highly planarizing fully absorbing underlayer (chemically similar to a novolac resist). The processing sequence is similar to a process with an organic BARC. While this technique was developed for 248-nm lithography, it appears that it can be extended to 193-nm lithography (by using an alternate imaging layer and underlayer).

The thin imaging-layer on a planarized layer allows for very high resolution. The silicon present in the imaging-resist-layer also gives it a very-high etch resistance when the underlayer is dry-etched (developed). The underlayer effectively planarizes the topography of the via-containing dielectric stack (Fig. 15-20a).[19] In this figure (in which the underlayer fills 0.25-μm vias), the vias are completely filled and the top of the underlayer is flat without any topography caused by the vias underneath. The thickness of the underlayer over the substrate in the via-array region is about 350-nm, which is enough to insulate the imaging layer from any optical effects by substrate reflections (i.e., the underlayer also acts as an effective BARC layer). Figure 15-20b shows an array of vias after the *imaging layer* has been exposed and wet developed.

The next step is a dry-develop process done with an SO_2/O_2 plasma. This transfers the pattern created in the imaging-resist-layer to the underlayer. Dry-developing the underlayer to the dielectric surface below defines the trench pattern. At this point the vias are still completely filled with the underlayer material. If we stopped the develop step at this point, and proceeded with the etch step to remove the dielectric material which creates the trench, veils would again arise (in the same way they occur if the via plugs made from BARC material

filled the vias too full). Thus, the dry-develop step is extended so via-plugs (now consisting of underlayer material instead of BARC) are recessed. (Since trench open-areas are large compared to via areas, an optical endpoint signal can be used to determine when the recess etching begins, providing good control.)

Figure 15-21 shows the patterned trench-resist and the recessed via-plug (whose level is below the top of the buried-nitride etch-stop layer). When the trench dielectric is now etched, no veils remain as residue within the trenches. Figure 15-22 shows the trench and via after trench-etch and resist-stripping. The trench and via profiles are vertical and veils are not present. Since the via-plug covers the bottom SiN barrier-layer during the trench etch, the trench-etch process does not have to be made selective to the nitride. This also allows a trench etch process with higher etch rates to be used.

Comparison of trench lithography at the edge of large via arrays shows another advantage of the top-surface bilayer-imaging technique. As is shown in Fig. 15-23, while trenches over vias at the edge of dense array vary considerably in width for standard DUV lithography (Fig. 15-23a), those patterned with TIS-2000 show no variation in width.[20] This is because the underlayer of the TIS completely fills the vias. Thus, the resist thickness is constant and there is little (or no) trench-width variation.

15.9.2 Via-First-Damascene Integration Issues: Dielectric Etching

The plasma etching and resist/polymer strip steps are among the most critical for the successful integration of a *low*-k dielectric. The etch process must be able to

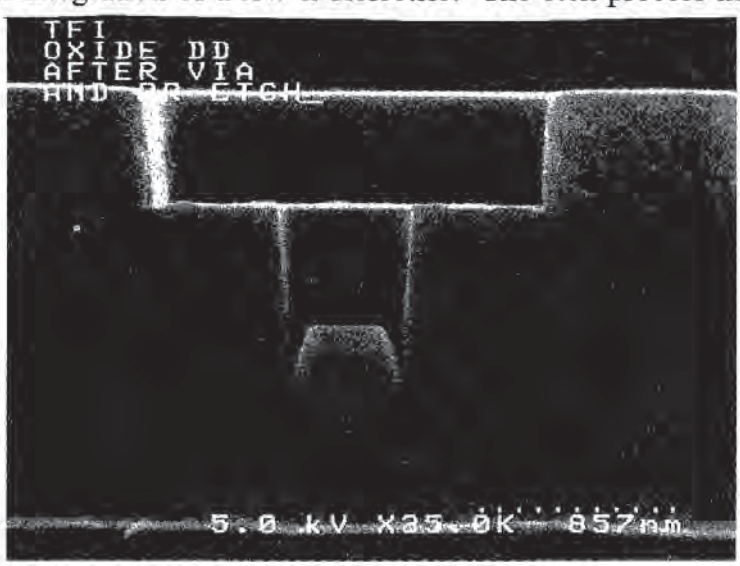

Fig. 15-21 Trench patterning using TIS-2000 bilayer resist. The dry-developed underlayer with recess etch brings the level of the via plug along the sidewalls below the nitride etch stop, which is important for the subsequent trench etch.[18]

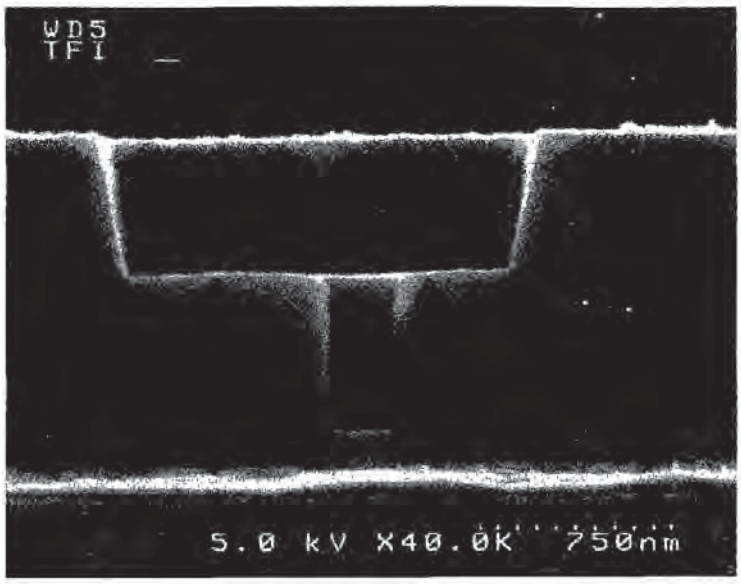

Fig. 15-22 Fully etched and stripped trenches over a via using the TIS-2000 bilayer resist process. The dual-damascene structure is nearly ideal in that there are no veils or faceting of the via due to trench etch.[18]

effectively perform the following tasks: **1**) Remove multi-layers of dielectric; **2**) Maintain a notch-free profile for optimum subsequent metal deposition; **3**) Achieve a high selectivity to resists (which is especially important as resists are getting thinner and 193-nm resists are less resistant to plasma etching than those used for 248-nm lithography); **4**) Retain the low-*k* value during the etch and strip processes so that ultimate device speed is not compromised; **5**) Achieve high selectivity to etch-stop layers, (especially since we want to make them as thin as possible to minimize the stack's effective *k*-value); **6**) Minimize microtrenching at the etch front; and **7**) Minimize aspect-ratio-dependent etch (ARDE) effects.

15.9.2.1 Via Etching for Low-*k* Processes: In the "via-first" dual-damascene process sequence, the vias are patterned and etched before the trenches. The via-

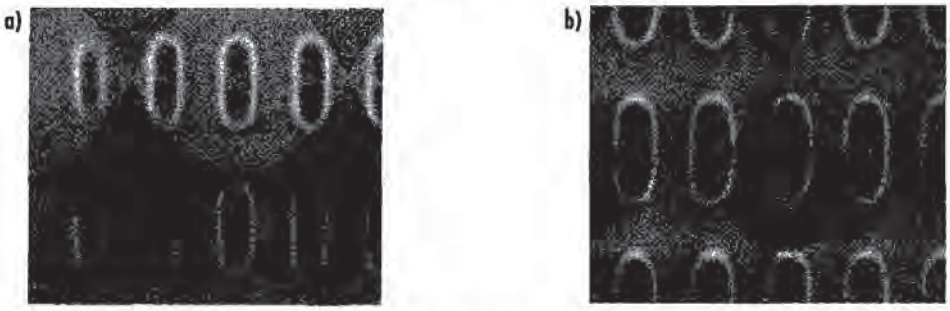

Fig. 15-23 Trenches over vias near the edge of a dense array: a) trench widths vary considerably for standard DUV lithography; b) the same area with TIS-2000 resist.[18]

etch process has some challenges, one of which was described in Sect. 15.9.1 (the resist must be able to withstand the deep via-etch process). To open the via, the following materials must be etched by the via-etch process in a low-*k* dielectric stack: **1**) BARC; **2**) SiO_2-hard-mask; **3**) upper low-*k* dielectric layer; **4**) thin SiN (or SiC) embedded etch-stop layer; and **5**) lower low-*k* dielectric layer. The etch step itself will therefore have to employ a multiple sub-steps (Fig. 15-17a).[18] The first such sub-step should be a non-selective etch, so that the BARC, SiO_2 hard-mask layer, low-*k* dielectric layers, and the embedded-etch-stop layers are all etched at about the same rate. This would ideally produce a via profile that is free of notching and bowing. This first sub-step would be terminated prior to removing all of the second low-*k* dielectric layer. The etching sequence would then switch to the second sub-step. The etch characteristic of this second-sub-step would be that it is highly selective to etching oxide and not nitride. This would allow it to remove the remaining lower low-*k* dielectric material from all of the vias without attacking the SiN etch-barrier layer at the bottom of the vias (i.e., a sufficiently long overetch time would be permitted to ensure that the lower low-*k* material was entirely removed from all of the vias).

While the above process is the desired goal, an even more complex etch process might be needed to produce a via-profile free of notching and bowing. That is, the etching characteristics of various low-*k* dielectrics are different from SiO_2, regardless of whether a spin-on organic-based material (such as SiLK® or FLARE®), or an SiCOH-CVD dielectric (such as Back Diamond,® Coral,® or Flowfill®) is used.

For example, a three-sub-step etch process might be needed for a SiO_2-hard-mask/SiLK stack. That is, fluorocarbon chemistries with high bias power might be used for the first-sub-step to etch the top SiO_2-hard-mask material and the embedded SiN layer (because this process can disrupt the strong Si-O and Si-N bonds), but when the SiLK layers are etched, a second-sub-step using oxygen as the active etchant is used. However, in an HDP tool, the high degree of gas-phase dissociation leads to high concentrations of atomic oxygen, which may produce some bowing of the via profile. Also, hard-mask undercut after via (and trench) etching can occur (Fig. 15-24), which would make it more difficult to achieve void-free metallization.[21]

When the low-*k* dielectric is a SiCOH-CVD film (having a higher porosity than normal CVD-SiO_2 films), the gas mixture for etching these low-*k* materials might be mixtures of CF_4 (the principal source of F atoms) and CH_2F_2 (a polymerizing gas for improving selectivity and providing sidewall passivation). Using such an etch procedure has reportedly allowed 0.3-μm vias to be etched in

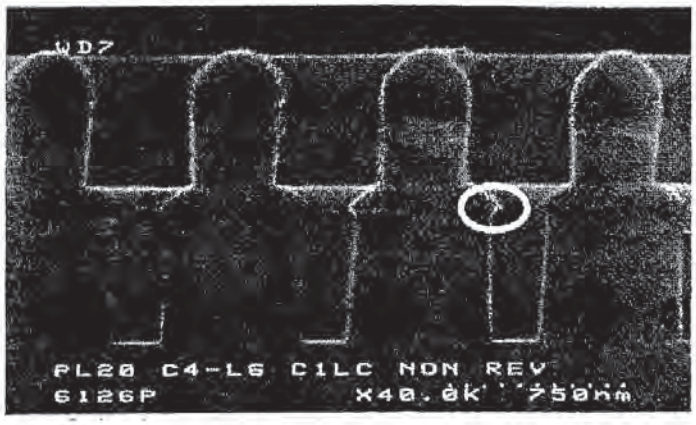

Fig. 15-24 Etched via profiles in SiLK® low-k dielectric showing hard-mask undercut.[21]

such stacks with the desired via profiles (Fig. 15-25).[22] The choice of gas mixture depends on the precise application being considered. That is, since these films contain some C and H, if their composition is changed (i.e., the more C, the lower the k-value), it will be necessary to re-tune the etch process in order to meet the selectivity and etch requirements.

15.9.2.2 Trench Etching: Following the via-etch-step in via-first, dual-damascene

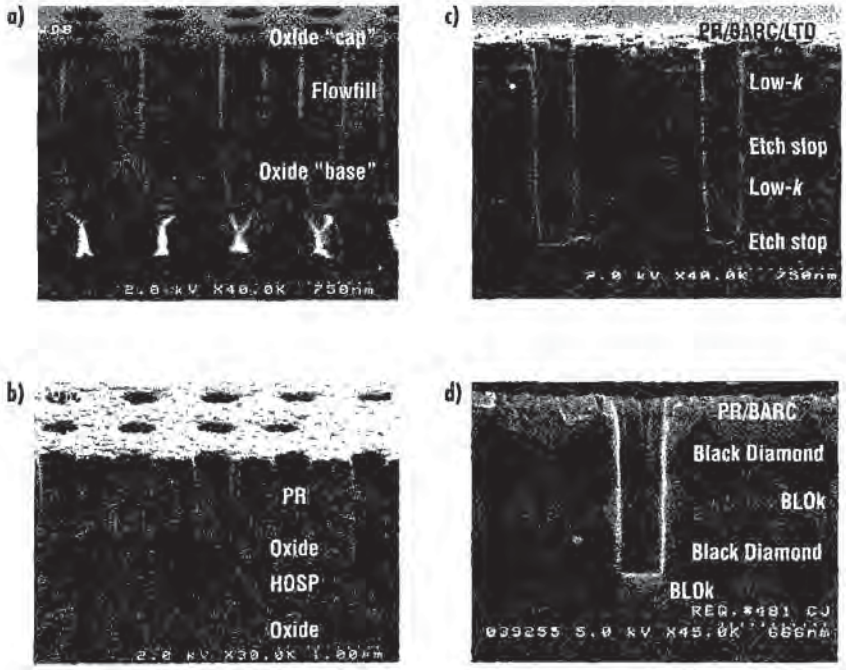

Fig. 15-25 Etching of: a) 0.3-μm vias through Trikon's low-k Flowfill (k = 2.9); b) 0.4-μm vias through Honeywells HOSP (k ~2.5); c) 0.28-μm vias through a Trikon dual-damascene stack (k ~2.8); and d) 0.29-μm vias through a dual-damascene stack containing Applied Materials Black Diamond film (k ~2.6) and BLOk (k ~4.5) etch stop.[22]

applications, trenches are etched down to the buried etch-stop layer. The issues involving protecting the barrier nitride at the bottom of the via (exposed during the previous via-etch step), from being etched during the trench-etch-step were previously considered in Sect. 15.9.1.

When a 2nd generation low-*k* dielectric is used, the top surface of the stack generally employs an SiO_2 hard-mask and a BARC to improve lithography resolution. Thus, the trench-etch process is also a multi-step procedure, involving: BARC-open; SiO_2-hard-mask etch; and low-*k* etch (down to the embedded etch-stop layer - Fig. 15-17b). Following the trench etch, the resist must be stripped, the BARC removed from the vias, and the barrier layer at the bottom of the vias etched away.

In early via-first, dual-damascene process flows, these steps were performed in several discrete tools. However, in the interests of improving cycle time (less handling and waiting), tool vendors are seeking to provide equipment that will allow an integrated-trench-etch process. That is, BARC opening, SiO_2-hard-mask etch, low-*k* dielectric etch, resist/BARC strip, and SiN barrier-layer open would all be carried out *in situ* in a single tool and a single process run.

15.9.2.3 Etching the SiN Barrier Layer at the Bottom of Vias: After the trench is completed and the second resist layer stripped, the nitride at the bottom of the via must be opened. As noted earlier, this etch process can cause some problems. First, the SiN etch step should be a "soft" etch. That is, the ions that bombard the SiN being etched should not have enough energy to sputter Cu during the inevitable overetch time. If such sputtering causes Cu to end up on the via sidewalls, it could be trapped on the wrong side of the subsequently deposited Cu-barrier-layer. Thus, any such sputtered Cu would have to be removed before the barrier metal was deposited. While a conventional dip in dilute HF is efficient for sidewall Cu contamination cleaning, this inevitably also cause some CD loss.

Another problem arises if the via is misaligned with the edge of the Cu line beneath it. In that case, during any overetch time of the nitride, a narrow slit would be etched in the dielectric alongside the Cu line (see Fig. 15-26).[31] This slit is hard to fill with barrier material, again leading to unwanted Cu diffusion. This issue can be addressed by employing a nitride etch process that is highly selective between nitride and oxide, and between nitride and Cu.

15.9.3 Via-First-Damascene Integration Issues: Resist Stripping

With the introduction of low-*k* and ultra-low-*k* porous dielectrics, existing resist-strip technology cannot be used without at least some modifications. Dry-etching in an oxygen plasma has become the most widely used stripping technology

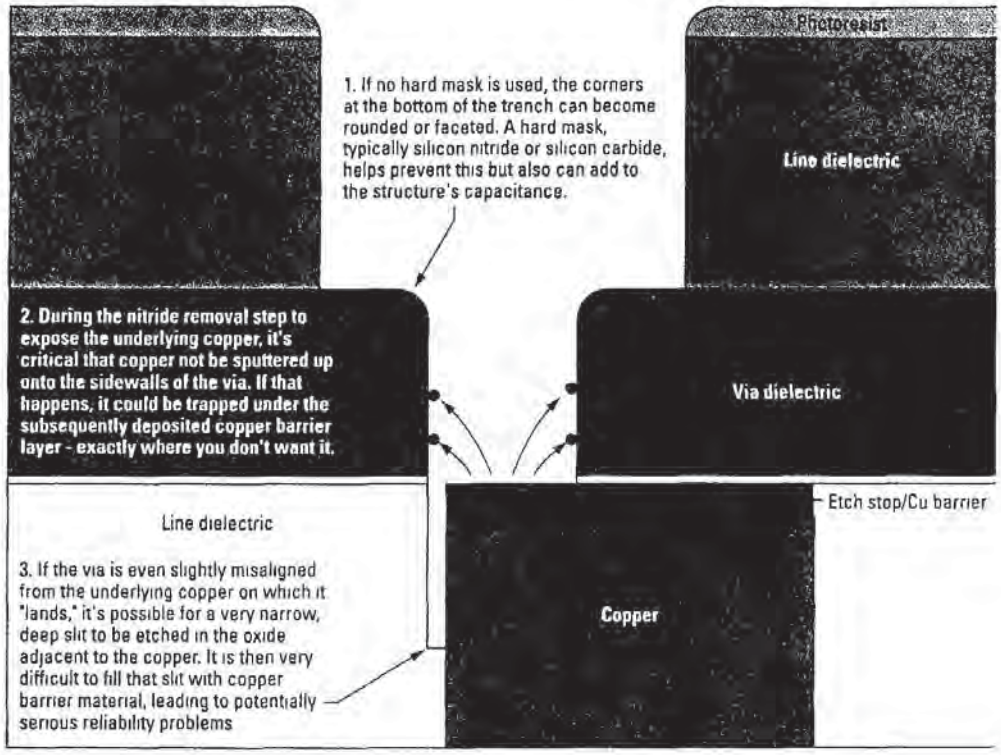

Fig. 15-26 Common problems in the via-first approach include rounding of the corners at the bottom of the trench; sputtering of the Cu onto the via sidewalls during nitride removal; and hard-to-fill slits etched next to the underlying Cu in the case of misalignment.[31]

(especially for back-end-of-line [BEOL] processes). However, many of the low-*k* dielectric materials are also etched by oxygen plasmas, and in some cases their *k* value may be degraded by reactive oxygen atoms as well. Here we discuss the issues facing resist stripping in such applications.

To begin, as noted earlier, SiO_2-hard-masks will typically be used on the top of the low-*k* dielectric stacks. These layers will actually serve multiple functions, including: **a**) as a hard-mask during via- and trench-etching; **b**) as a polish-stop layer for the Cu-CMP process; and **c**) as a dielectric anti-reflective coating (DARC). The use of a hard mask is mandatory if organic low-*k* films are used (since they are attacked by the same chemistries used when stripping the resists after an etch step). Even with a hard mask, however, difficulties arise when etching organic low-*k* materials. That is, if an etch-process is used that is based on an O_2 plasma, very reactive oxygen radicals are present in the plasma. These isotropically attack organic low-*k* dielectrics, causing bowing of the via and/or trench profiles (as shown in Fig. 15-27).[23] To stop such attack of the dielectric layer, sidewall-passivating gases must added to the O_2 etch gas. In one paper,

ethylene was added to the O_2 etch gas when an organic low-*k* material was being etched. Undercutting of the hardmask was prevented, and good CD control was maintained, as the hardmask itself was not eroded.[24]

Even if an HSQ or MSQ-based low-*k* material is used instead of an organic film (see Chap. 14), the resist stripping process is still a challenge. That is, while the resist is being stripped, the oxygen radicals will react with the exposed low-*k* material of the trench sidewalls. These reactions convert the Si-CH_3 bonds in the MSQ, and the Si-H bonds in HSQ films, back to Si-O bonds. This causes the *k*-value of the dielectric to rise back toward that of SiO_2 (~4.0). As a result, an alternative resist stripping process is needed. That is, an alternative anisotropic ashing process must be available.

One method of making low-*k* materials more robust against attack by oxygen radicals is *plasma treatment of the exposed low-k material surfaces.* An example of such a plasma treatment was reported to have carried out on an organic low-*k* material. After exposing this dielectric to an NH_3 plasma for 10 minutes, a nitrided layer is formed on its surface. The nitrided low-*k* layer exhibited lower leakage current after an ashing plasma exposure than did the untreated material. The film also acted as a better barrier against Cu diffusion.[25] In another paper, three such NH_3-plasma treatments in were performed on a dual-damascene via-first etched dielectric stack consisting of HSQ/PECVD-SiO_2/HSQ. The first treatment was carried out prior to depositing the embedded etch-stop PECVD-SiO_2 layer on the first HSQ segment of the stack. This improved adhesion of the embedded etch-stop layer to the HSQ. The second treatment was carried out after the second HSQ layer was deposited and the trench etch was completed. This purpose of this treatment was to strengthen the exposed HSQ sidewall surfaces against erosion during the resist stripping step.[26]

Carbon-doped low-*k* materials such as Coral® and Black Diamond® are ozone

Fig. 15-27 Cross-section SEM picture of single damascene structure made in 3M's low-*k* dielectric after strip and etch in a low-pressure, low-temperature strip.[23]

resistant. Resist stripping in processes that use these dielectric materials might potentially be carried out with a DI ozone strip process.

15.9.4 Via-First-Damascene Integration Issues: Cleaning

Cleaning issues are critical to producing dual-damascene interconnects with high yield and reliability. The cleaning challenges are especially severe for dual-damascene structures compared to front-end-of-line (FEOL) processes, because more aggressive chemicals can be used on silicon and thermal oxides. That is, the strong acids and bases in the FEOL flow effectively remove contamination and resist residues after critical FEOL steps. However, metals in back-end-of-line (BEOL) cannot be subjected to such chemicals since they are susceptible to chemical corrosion. Fortunately, the CMP process used in dual-damascene interconnects tends to remove particles on the dielectric surface during polish, another inherent advantage over the subtractive interconnect approach. However, other residual films must still be removed, as will be discussed here.

15.9.4.1 Post-Dielectric-Etch-and-Resist-Strip Residue Removal: After photoresist is stripped with a dry-stripping step (ashing), residue from the etch and the ashing step often remains on the via and trench sidewalls, and must be removed. Typically this is done with wet-chemical residue cleaners, in a separate cleaning step after the dry-strip step. One goal (as a way to improve cycle time), is to integrate these two steps into a single tool.

As long as SiO_2 was the material used in the dielectric stack, the post-etch residue removal step was easier, and proprietary organic solvents sold by such vendors as EKC Technologies, ASCI, J.T. Baker, and Olin could effectively remove the residues (Fig 15-28). However, with the introduction of low-*k* dielec-

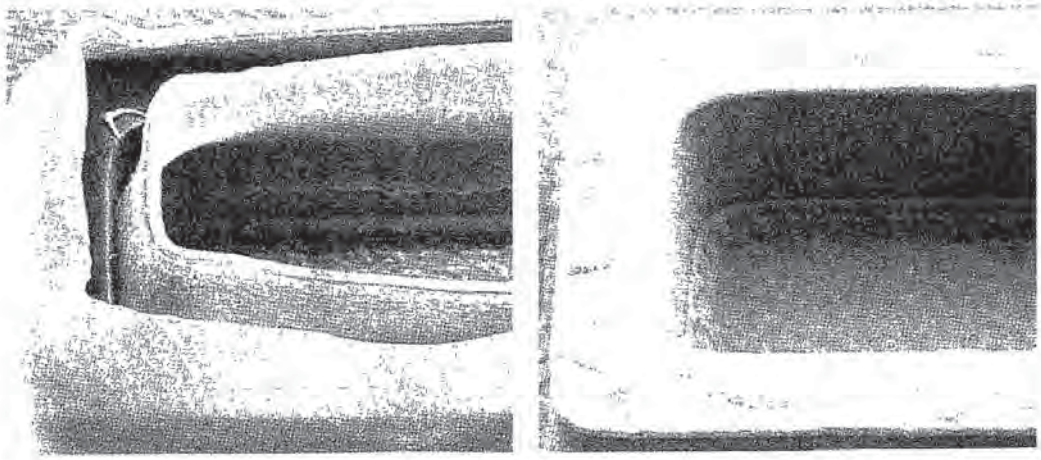

Fig. 15-28 Aqueous residue removers specifically target organometallic and inorganic residues left after ashing. Courtesy of J.T. Baker.

trics, the situation has changed. New cleaning chemicals must be used, and suppliers are working on chemistries for residue cleaning in Cu/low-*k* applications. However, a major issue in pursuing this goal is that it has not yet been decided exactly which low-*k* materials will be used for this application, and what are all of the material properties of the candidate materials. In addition, it appears that there will be a continuous transition from one material to another over the next few years, as ever lower-*k* materials are integrated into damascene structures. However, some general trends can be foretold.[27]

First, it must be ensured that residue-removal chemistries are compatible with specific the low-*k* dielectric and the metallurgy on the wafer. This is complicated by the lowering of the porosity of the new low-*k* materials and the thinning of the dielectric layers. Furthermore, since each low-*k* choice requires different plasma etching processes and chemistries to etch vias and trenches into the low-*k* materials, the nature of the residues can be different. Thus, no one product will likely to be able to meet all Cu/low-*k* applications. Nevertheless, it appears that some form of wet cleaning after etch and ashing will still be needed until below 0.13 μm. Fundamental barriers to wet cleaning approaches do not appear to be reached until well below 0.1 μm. At some point, however, there are concerns about liquids being able to go into and out of small, high-aspect-ratio features. At that time a dry-approach (or the use of supercritical fluids – see Sect. 15.9.4.5) may need to be used.

15.9.4.2 Pre-Metal-Deposition Clean: The pre-metal-deposition clean is carried out just before the barrier layer metal and Cu seed layers are deposited. The Cu film at the bottom of the vias must be free of organic residues and any native Cu oxide in order to ensure that low-resistance contact between the deposited barrier metal and the underlying Cu is fabricated with high yield. This clean step normally involves sputter etching of the wafer in the same tool in which the barrier layer metal and the seed Cu layer are sputter-deposited. Argon ion gas is used, and a dual-frequency rf sputtering module with a high-density plasma (HDP) source is required (so that a high degree of directionality can be obtained with the sputter-clean process).

During this pre-metal-deposition cleaning process, copper ejected from the lower layer can be re-deposited onto the via sidewalls, increasing the risk of line-to-line leakage. By 1999, however, the magnitude of this problem had not yet been quantified. It is hoped that the quantity of copper re-deposited will not be sufficient to degrade device performance. Nevertheless, if the problem becomes worse than expected, alternate via-clean methods will need to be developed that

selectively remove the etch residue and copper oxides without removing any copper.

Another special problem occurs when trying to integrate Cu with a fluorine-containing dielectric material, such as FSG. That is, the F bonds in many FSG films are reactive (particularly with water), and they can be broken during other process steps to produce free fluorine. At the interface between the FSG film and the barrier metal, Ta can react with such free fluorine to form volatile by-products at elevated temperatures. The resulting weakened interface can fail when subjected to the stress of an overlayer (such as that produced by the SiN diffusion barrier layer). A number of solutions to this problem have been proposed, including: use of a TaN barrier material (which is less reactive than Ta); using a more stable FSG film; or using a hydrogen-plasma treatment before depositing the Ta to remove mobile fluorine from the surface.

15.9.4.3 Post-CMP Clean: The post-CMP clean step is a critical one for Cu CMP. The bevel and backside of the wafer will most likely be exposed copper-containing solutions during the CMP step. Any copper remaining on the bevel or backside of the wafer risks contaminating other tools within the fab. As in the electroplating process, simple cleaning methods are available to remove residual copper, but the risks associated with copper cross-contamination demand careful monitoring of the post-CMP clean (see also Chap. 8).[28]

15.9.4.4 Clean of Top-Surface of Cu Prior to Diffusion-Barrier-SiN-Deposition Process: After the CMP step of the metal, and post-CMP clean, a SiN layer is deposited on top of the damascene structure. As noted earlier, this SiN film serves as barrier to keep the Cu from diffusing into the dielectric layer above it, and also as an etch-stop layer for the via etching step. However, the SiN may fail to adhere to the Cu surface if that surface is not properly cleaned. That is, the SiN may not adhere to the Cu interface if even a small amount of residue is left on the Cu surface following CMP. It turns out that there are two classes of such contaminants that must be removed from the Cu-surface: 1) residual organics that are present in the Cu-CMP slurry; and 2) native oxide that has formed on the Cu surface.

The residual organics can be removed by a pre-treatment with an *in situ* exposure to an aggressive hydrogen plasma just before depositing the SiN layer. Another technique is to remove such organics (corrosion inhibitors, usually BTA) from the CMP process. In addition, Cu forms a native oxide that can interfere with SiN adhesion. That is, if this oxide is not completely removed from the Cu surface, the Cu/SiN interface will be weak. Thus, a cleaning step

(consisting of a copper oxide reduction step using the same hydrogen plasma used to remove the residual organics) is recommended.[29]

15.9.4.5 Supercritical Fluids as Wafer Cleaners:* The temperature at which the vapor pressure above a pure liquid reaches one atmosphere is known as the normal boiling point – for water it is 100°C. In an open container, liquid water's temperature cannot be raised above 100°C because it would cause the vapor pressure to rise above one atmosphere, exceeding ambient pressure conditions. However, in a sealed container, liquid water can be heated to higher temperatures. As the water is heated, its density decreases (through thermal expansion), and simultaneously, the vapor density in the container increases.

This heating can be continued until the liquid's density has been so reduced – and that of the vapor so increased – that both densities are equal. This point is known as the *critical temperature*, and the pressure of the vapor at that point is called its *critical pressure.* Since the temperature and density of the water inside the sealed container are equal everywhere, thermodynamics dictates that the critical pressure inside the container also be equal everywhere. A fluid brought to conditions above its critical temperature and pressure (the *critical point*) is called a *super-critical fluid.*

Carbon dioxide (CO_2) is a material that is particularly attractive as a practically useful super-critical fluid. This is because it is non-toxic, non-flammable, and inexpensive. In addition, its critical conditions are easily achievable with existing process equipment. This unique set of characteristics has led workers to examine the possibility of using supercritical CO_2 instead of other solvents in such semiconductor processes as cleaning and photoresist stripping.

The attractiveness of using supercritical CO_2 as a replacement for traditional solvents in cleaning and stripping applications stems from the combination of gas- and liquid-like properties that it possesses. Table 15-1 compares the physico-chemical properties of a typical organic fluid in it's liquid, supercritical, and gaseous states. It can be seen that the supercritical fluid state possesses *gas-*

Table 15-1 PHYSICO-CHEMICAL PROPERTIES of TYPICAL ORGANIC FLUIDS

	Diffusivity (cm^2/sec)	Viscosity (mPa-sec)	Density (kg/m^3)
LIQUID	10^{-5}	1	1000
SUPERCRITICAL FLUID	10^{-3}	10^{-2}	700
GAS	10^{-1}	10^{-2}	1

* Written by James Rubin, Los Alamos National Laboratories. The material originally appeared in Semiconductor International. Reprinted with permission.

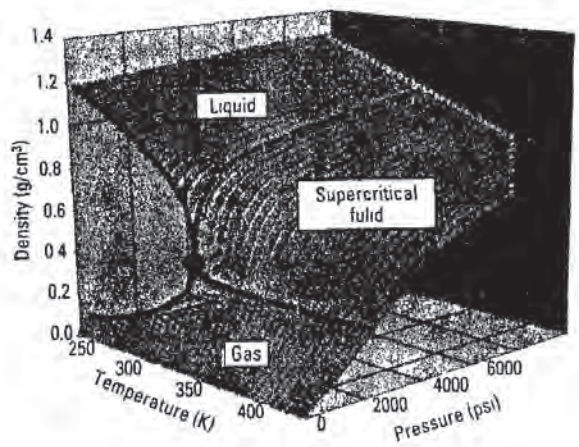

Fig. 15-29 Pressure-temperature-density surface for pure CO_2. The critical point is the small circle at the intersection of the contour lines.

like values of viscosity and diffusivity, and *liquid-like* density.

Figure 15-29 shows the density-pressure-temperature surface for pure CO_2. The critical point for pure CO_2 is 31°C (304K) and 1072 psi. To a first approximation, a fluid's solvent power is proportional to its density. Thus, high liquid-like densities achievable in supercritical fluids allow for liquid-equivalent solubilities. Figure 15-29 also indicates that small changes in pressure or temperature near the critical point result in large density changes. This implies that the density – and hence the solvent power – of a supercritical fluid is "tunable."

Figure 15-30 is a schematic pressure-temperature phase diagram for CO_2, incorporating the process flow for a closed-loop supercritical fluid treatment system. No uncontrolled waste streams can exit such a closed-loop system. All materials solubilized in the supercritical fluid are retained in the separation vessel

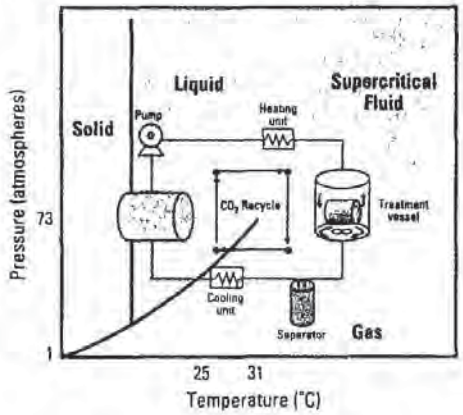

Fig. 15-30 Pressure-temperature phase diagram of pure CO_2 with a superimposed flow diagram for a closed-loop supercritical fluid treatment process.

for analysis, recycle, treatment, and/or disposal. In addition, these materials are concentrated in the separator, greatly reducing waste volume.

Several companies are working on commercializing tools that employ supercritical fluids in cleaning processes, including Supercritical Systems (a TEL-America company), and GT Equipment Technologies.

15.10 VIA-FIRST DUAL-DAMASCENE DIELECTRIC STACK WITH NO EMBEDDED ETCH-STOP LAYER

Eventually, the increase in the *k*-value of the damascene dielectric stack due to the embedded etch-stop layer (whether it is composed of SiN or SiC material) becomes too great. At that point, it may be necessary to use a damascene dielectric stack without an embedded etch-stop layer. Some predict that this approach will be needed for the 0.1-μm technology node.

The elimination of the etch-stop layer, however, produces some significant process integration issues. First, since there is no etch-stop layer, etch systems will have to have extremely good control of uniformity to ensure all trenches are of the same depth across the wafer, and from wafer-to-wafer. This could be difficult as there is no endpoint indicator, and the depth of the trench can only determined by the time of the etch step. Making the problem even more difficult is that low-*k* materials may not lend themselves to that kind of control. Second, if a hard etch-stop layer is not present, the top corner of the via can become rounded during the trench etch process (due to faceting, see Vol. 1, Chap. 11 - Physical Vapor Deposition, and also Fig. 15-26). A second issue involves the creation of microtrenches at the corners of the trenches themselves. This phenomenon is likely to be caused by enhanced ion-bombardment-flux at the corners of the trench (due to ions reflecting at shallow angles off of the sidewalls). Such microtrenches would provide locations that are poorly covered by the Cu diffusion barrier films. This could give rise to Cu diffusion through the barrier layer at such points where the barrier layer is thinned (or is even discontinuous).

15.11 PROCESS INTEGRATION ISSUES OF DUAL-DAMASCENE DIELECTRIC STACK WITH ULTRALOW-*k* DIELECTRICS

If damascene dielectric stacks are fabricated with ultra-low-*k* materials, additional process integration problems are encountered. That is, special techniques must be developed to protect these porous, less-robust materials during ashing and CMP. Two novel damascene processing steps have been proposed to handle such fragile films. The first is termed *half-via etch*. In this approach, the via is again etched first, but only half of the via is opened with this

process, down to the depth of the trench. Then the rest of the via is opened during the trench-etch step. This provides a simpler etch and alignment process and makes the lithography problem of resolving small feature sizes easier.

Another change may involve returning to the trench-first etching sequence. With a porous material, the via cannot be etched first because, after the via is etched and you begin etching the trench, problems will arise because the resist that flooded the vias will begin to be absorbed by the porous low-*k* dielectric.

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Chapter 16

COPPER INTERCONNECT PROCESS TECHNOLOGY

As described previously in Chap. 12, interconnects in deep-submicron ICs comprise a multilevel structure of fine wiring located on the top of the transistor circuitry of logic and memory chips. To avoid significant degradation of circuit speed, on-chip interconnections should permit rapid signal transmission among the various parts of the circuitry. Ever since the development of the integrated-circuit in the early 1960's, the materials most widely used for the wiring structures have been aluminum as the conductor (or eventually an aluminum-copper alloy for better reliability), and silicon dioxide as the insulator. In 1997 the transition to copper as the conductor was initiated with the announcement by IBM that they had developed a technology for forming copper interconnect lines and vias for IC applications. This was one of the most important changes in materials that the semiconductor industry has experienced since its inception. Since that breakthrough, AMD reportedly applied Cu to its microprocessor circuits at the 0.18-μm technology node, enabling it to introduce the first GHz-rated microprocessor in March 2000, ahead of competitors. In addition, circuit designers have also started to explore innovative layouts to take full advantage of the multiple benefits of Cu (as opposed to simply replacing Al with Cu in an existing design). Thus, it appears that the Age of Copper is dawning!

16.1 WHY COPPER FOR DEEP-SUBMICRON IC INTERCONNECTS?

As noted above, copper is now poised to take over as the main on-chip conductor for all types of ICs.[1,2] Early adopters of Cu technology put copper in production at the 0.25-μm node. Recent market-research studies indicate that for the 0.18-μm generation about 5% of the interconnect structures will be implemented with Cu. It also appears that most Cu in production (or pilot-line production) in 2001 was at the 0.18-μm and 0.13-μm technology nodes. For some manufacturers, 0.13-μm is a second-generation of Cu, for others 0.13-μm is the entry point for placing Cu into production (Fig. 16-1). It is predicted that Cu will represent about 60% of the interconnects for the 0.1-μm generation. The reasons why copper is displacing Al as the dominant conductive material for deep-submicron IC interconnects are explained next.

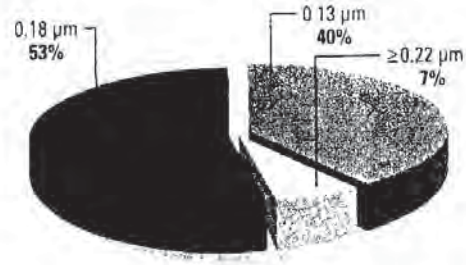


Fig. 16-1 Market analysis of device manufacturers using pilot production in 2001.[39]

16.1.1 The Advantages of Copper Interconnects

There are several critical advantages that copper interconnects provide over the traditional aluminum interconnects that have been used ever since ICs were invented in 1961:

1. Copper has a resistivity that is approximately 40% lower than Al (ρ_{Cu} = 1.7-$\mu\Omega$-cm versus ρ_{Al} = 2.7-$\mu\Omega$-cm), and 50% lower than the Al:Cu-alloys used in IC interconnects ($\rho_{Al:Cu(0.5\text{-at}\%)}$ = 2.9-3.3-$\mu\Omega$-cm). By referring to Eq. 12-7 for the interconnect *RC*-time-delay, it can be seen that *RC* scales directly with ρ. Specifically, if copper can be used instead of aluminum-alloys, the resistance of the wiring structures can also be proportionately reduced. That is, a reduction in the wiring resistance (and thus also the *RC*-delay) of as much as 45% can be obtained when copper replaces Al as the core-interconnect-metallurgy material.

It is important to note that a more complete analysis of the wire resistance must take into account not only the core-material of the interconnect (Al:Cu or Cu), but also any other (and usually higher-resistivity) materials used to surround the core-conductor. A comparison between the effective resistivity ρ_{eff} of Al:Cu wires and Cu wires is illustrated in Fig. 16-2. That is, the Al:Cu lines in Fig. 16-2 are fabricated by etching an Al:Cu film that has both bottom and top Ti layers. During sintering the Ti-layers react with the Al to form $TiAl_3$ (whose resistivity is ~35-$\mu\Omega$-cm, and the thickness of the resulting $TiAl_3$-layers is about 3.5 times the original Ti-layer thickness). The Cu wires are formed by a damascene process (see Chap. 15). This requires that the bottom and sides of the Cu wires be clad with a thin layer of a diffusion-barrier material. While this barrier-layer film also has high resistivity, it does not react with the Cu (unlike Ti, which reacts with Al), and this material also serves as an adhesion-layer. In any case, it is clear from Fig. 16-2 that copper offers a very significant reduction in the effective resistivity for both present and future technologies compared to aluminum.

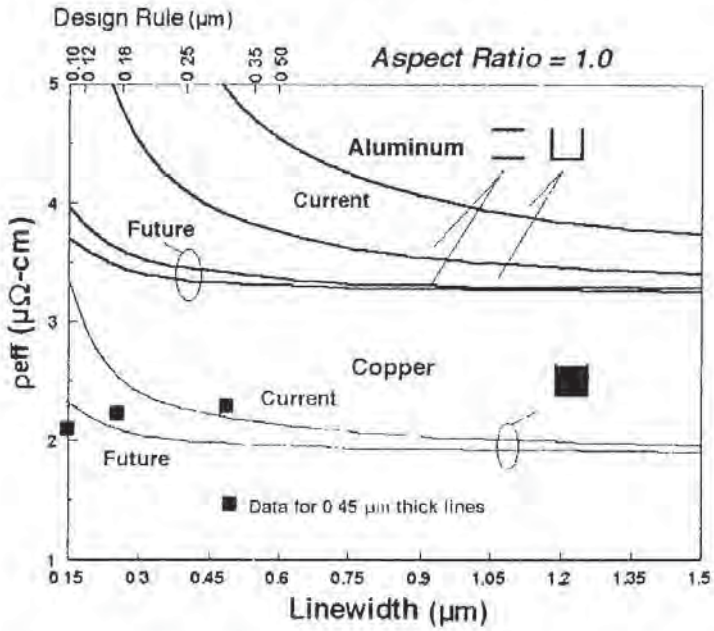


Fig. 16-2 Effective resistivity for aluminum and copper interconnects as functions of linewidth and design-rule generation. Computational results (*solid lines*) have been obtained for various combinations of conductor material and barrier location shown in the right side of the figure. Experimental points correspond to published results from real structures.[46]

This lower effective-resistivity of Cu-wiring can be exploited in one of two ways to reduce the RC-time-constant of Cu interconnect-systems:

i) The total resistance R_{int} of an interconnect line can be reduced (by retaining the same metal thickness [and cross-sectional area]), or;

ii) The side-by-side capacitance C_{LL} of interconnect lines can be reduced by decreasing the metal-film thickness. This allows R_{int} to remain the same as it was for a thicker Al line, but it reduces C_{LL}. Meanwhile, the same current is carried in a smaller-cross-sectional feature, without fearing EM-failure (see following paragraphs).

The primary clock-speed benefit derived from Cu is gained by using it in the upper-interconnect-levels of a multilevel-metal structure (where the conductor lengths can be of the same order as the chip size). As was shown in Chap. 12, Fig. 12-1, by utilizing Cu together with a low-k dielectric to replace Al and SiO_2, the overall delay (and power consumption) in technologies below 0.25-μm is dramatically reduced.[3]

As also discussed in Chap. 12, the interconnect RC-delay is predicted to become larger than the RC-delay of MOSFET transistors for technology nodes below about 0.5-μm. As an example, Fig. 16-3 shows that the RC-

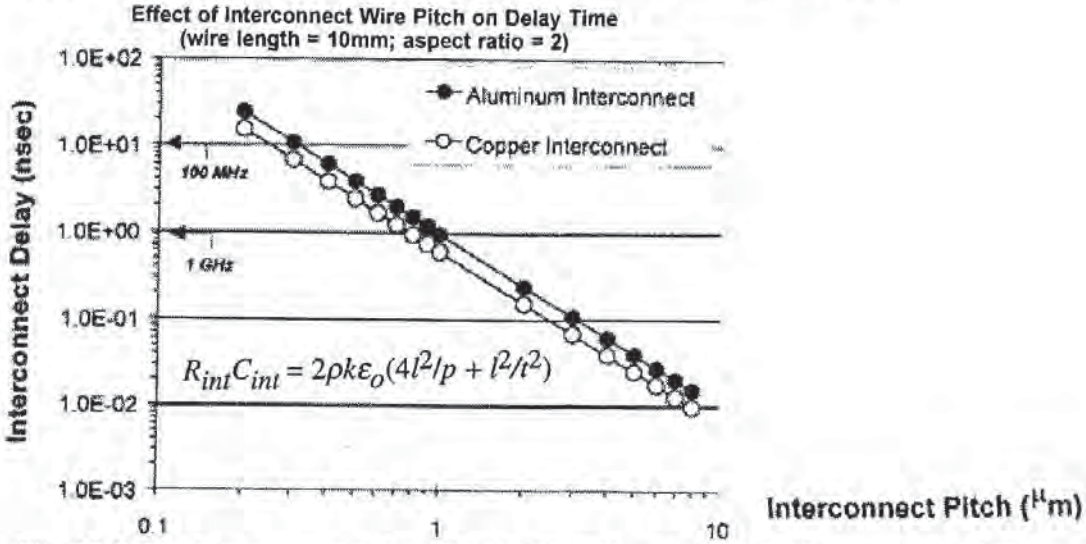


Fig. 16-3 The interconnect delay of both Cu and Al wiring has been calculated using Eq. 16-4 for *RC*. The delay-time in nanoseconds (1 nsec = 10^{-9} sec) is plotted versus the pitch of the wiring in microns (1 μm = 10^{-4} cm) for a line with an aspect-ratio = 2 and length l = 10-mm. The dielectric constant of the ILD has been set to k = 4.0, which is approximately equal to that of CVD deposited silicon-oxide. The graph shows that as the wire-pitch is decreased below 1-μm, the delay-time can become greater than the intrinsic switching-time of the transistors. The speed limit is increased by using Cu over Al.

delay of a dense array of 10-mm-long Al-alloy interconnect-lines with an aspect-ratio of 2 is longer than 1-nsec for pitches smaller than 0.8-μm. Since 1-nsec is equivalent to a frequency of 1-GHz, this implies that signal delays in IC wiring will limit circuit speed to about 1-GHz, (even though individual transistors may have faster intrinsic clock-rates). The interconnect thus represents a real limiter to high-performance ULSI chips – analogous to owning a sports car but only being allowed to drive it on a highway at rush hour. Switching to Cu is one way of improving this situation.

As was done in Chap. 12, Sect. 12-6, equations can be derived to calculate the interconnect delay-time $R_{int}C_{int}$. That derivation is repeated here, but for a simplified special case that exemplifies the impact of switching to copper. The following symbols apply to those aspects of the interconnect system depicted by the test-structure shown in Fig. 12-19.

That is, the metal-line *width* is w, the metal-line *thickness* is t, the *spacing* between the lines is s, the metal-line *pitch* is p ($p = w + s$), and the *thickness of the ILD between the top of the metal lines and the grounded planes* is d. Also the *length* of the metal lines is l, and the *resistivity* of the metal is ρ. Some equations can now be derived that allow the contributions made to R_{int} and C_{int} from: **1**) the materials properties; and **2**) the

interconnect architecture, to be expressed. Using this approach, the resistance of a metal-line is calculated from:

$$R_{int} = \rho l/wt \tag{16.1}$$

Next, the capacitance between the metal lines and the grounded planes C_{LG} (separated by an ILD whose relative constant is k), is calculated from:

$$C_{LG} = k\varepsilon_o wl/d \tag{16.2}$$

and the intralevel capacitance C_{LL} (assuming the same ILD) is found from:

$$C_{LL} = k\varepsilon_o tl/s \tag{16.3}$$

where ε_o is the permittivity of free space. For the $R_{int}C_{int}$ time-delay-constant, it follows that:

$$R_{int}C_{int} = 2\,R_{int}(C_{LG} + C_{LL}) = 2\rho(l/wt)k\varepsilon_o(wl/d + tl/s) \tag{16.4}$$

To simplify the discussion, we assume that the pitch is equal to twice the line width ($p = 2w$), which also implies that $s = w$, and the metal-thickness is equal to the insulator thickness ($t = d$). In this case, Eq. 16.4 becomes:

$$R_{int}C_{int} = 2\rho k\varepsilon_o(4l^2/p^2 + l^2/t^2) \tag{16.5}$$

Equation 16-5 is the relationship that is used here to calculate the value of $R_{int}C_{int}$. As also pointed out in Chap. 12, the dependence on ρ, k and l in Eq. 16-5 shows that $R_{int}C_{int}$ can be reduced by choosing metals with low-resistivity, insulators with low-k-values, and/or making line-lengths as short as possible.

Using Eq. 16-5, it is also possible to calculate the dependence of $R_{int}C_{int}$ on metal-pitch and metal-thickness. The results of such a calculation is illustrated in Fig. 16-4, which shows that for a given metal-

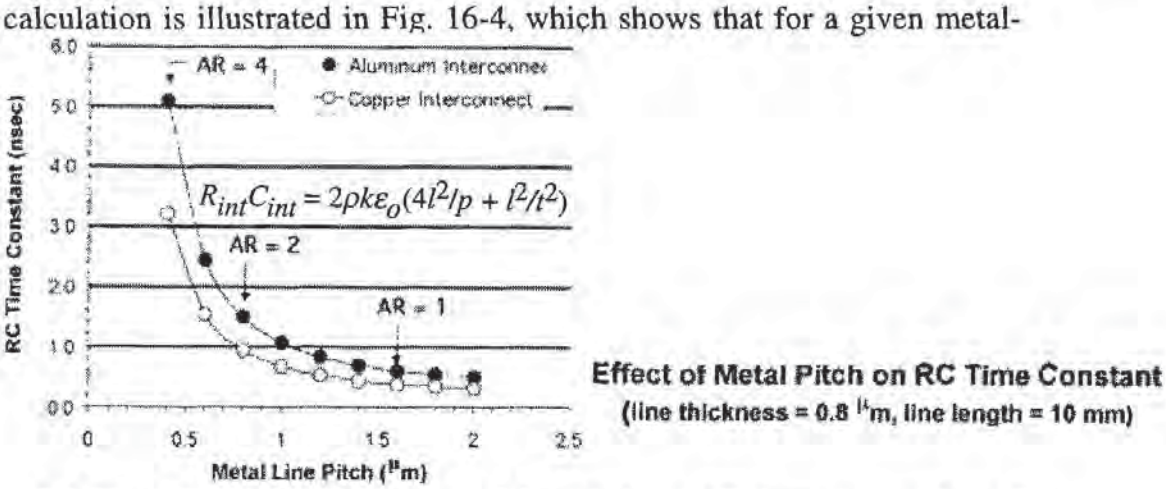


Fig. 16-4 The effect of Cu and Al metal-line-pitch on RC time-constant for a line thickness of $t = 0.8$-mm, a line-length of $l = 10$ mm for the case of both Cu and Al. Eq. 16-5 is shown on the graph and was used to calculate $R_{int}C_{int}$.

pitch and line-width that $R_{int}C_{int}$ can be reduced by increasing the aspect–ratio of the line (which of course reduces R_{int} due to the cross-sectional-area increase). However, for aspect-ratios greater than 2, this reduction in the $R_{int}C_{int}$-product is offset by a corresponding increase in the intra-line capacitance C_{LL}. This fact (and the practical difficulty of fabricating metal-lines with very-high-aspect-ratios), is consistent with industry roadmaps predicting metal-line aspect-ratios of less than about 2.7 through the 70-nm node.

After IBM debuted Cu interconnects in 1997, several other companies in 1998 announced the development of Cu-multilevel interconnect systems that they would implement in commercially-available ICs.[4,5] The resistivity of composite copper interconnects in these reports (with the diffusion-barrier in place) did not exceed 2.2-$\mu\Omega$-cm, a 40% improvement over that of comparable Ti/Al:Cu lines.

2. Copper films exhibit much better electromigration (EM) characteristics and stress-void resistance than do Al films. Electromigration is an atomic-scale phenomenon in which the electrons that constitute electric-current collide with the metal-atoms of an interconnect line and push them in the direction of the current-flow. If this "*electron wind*" is strong enough, a significant migration of the metal atoms will occur. Over time this transport of material can lead to the electrical failure of the interconnect in one of two ways: **1**) by a break in the line (causing an open-circuit) due to local depletion of material; or **2**) by the formation of a short-circuit to an adjacent line due to local accumulation of material. The strength of the electron wind increases as the current-density is increased, and the upper-limit of current-density to prevent electromigration in Al:Cu interconnects is 5×10^5 A/cm^2 (for a 20-year lifetime). This limit puts restrictions on circuit-design and chip-performance. (For example, a current of 5-mA in an interconnect-line of cross-section 0.5-μm x 1-μm (i.e., 0.5-μm^2 = 5×10^{-9} cm^2), represents a current-density 1×10^6 A/cm^2, which is twice as great as the current-density-limit for Al:Cu-lines. Scaling of interconnect wires to increase functional-density and chip-performance inevitably leads to increased current-densities (see also Chap. 12), making Al:Cu interconnects less attractive for future technology structures.

Since Cu-atoms are more massive and more tightly bound together than Al atoms, interconnects made of Cu are generally more resistant to electromigration than those made of Al or Al:Cu (i.e., they exhibit 10-100x

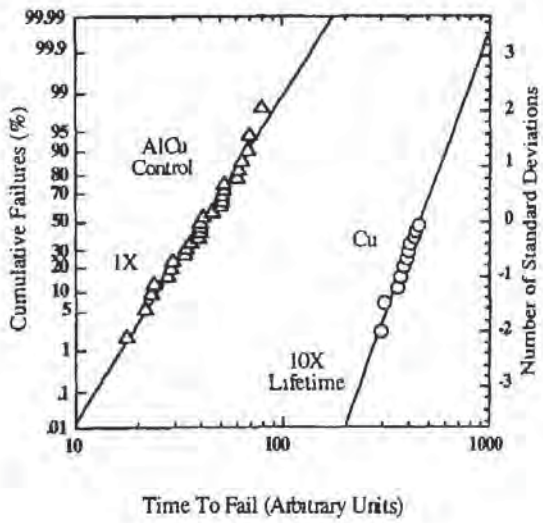


Fig. 16-5 Electromigration performance improvement using copper metallization.[5]

more EM-resistance). About an order of magnitude longer EM lifetimes are obtained for Cu lines of the same cross-section as Al lines, allowing Cu to deliver more reliability for a given interconnect design.[4] In addition to electromigration, stress-voiding (i.e., due to mass transport resulting from thermally-induced stress gradients), is another reliability concern.

Electromigration tests of 0.3-μm lines conducted at an elevated temperature (295°C) and a stress-current of 2.5×10^6 A/cm^2 showed a mean-time-to-failure (MTF) that was more than 10 times longer for Cu than for Ti/Al(Cu)/Ti lines (see Fig. 16-5). Excellent results were also obtained for stress migration testing.[6] Both sets of results argue strongly in favor of using copper interconnections for higher usable current densities and better overall performance.

Another benefit of Cu interconnects with respect to electromigration failures involves the current-flow in vias. As shown in Fig. 16-6, a small diameter via serves as the electrical bridge for current flow from metal-level-n to metal-level-n +1. A problem known as "current-crowding" arises because the current from the rectangular interconnect is compelled to flow through the much smaller circular-cross-section of the via. Due to the change of geometry and reduction in cross-sectional area, the current-flow in the via can be highly non-uniform, with local current-density much higher than in the interconnect line. If the via current-density exceeds the design specifications, excessive heating and/or electromigration can result. In turn, this can lead to circuit-reliability problems. Replacing W-plugs in

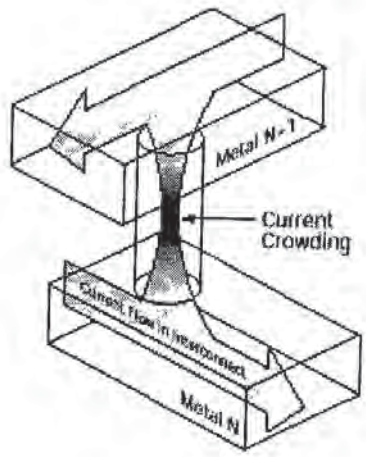


Fig. 16-6 Copper-filled vias can provide additional protection against structural failures associated with current crowding, thereby maintaining via reliability within designed specifications. In particular, the uncertainty in calculating the exact 3-D current-flow in the via is mitigated by the increased tolerance of Cu to electromigration at high current density.

the vias with Cu-plugs significantly reduces the electromigration problems observed in interconnects consisting of Al:Cu wires and W-plugs.

3. The third major benefit of employing copper (and some say it's the most important one) is that lower manufacturing costs can be obtained compared to using aluminum. The cost is lowered for two reasons.

First, because copper is difficult to etch, a new strategy called "damascene" or "in-laid" patterning was developed to form the Cu interconnect lines (see Chap. 15). IBM (which pioneered the process), claimed that the damascene approach requires 20-30% fewer steps than traditional subtractive patterning. Not only are there fewer steps, but dual-damascene eliminates or reduces the need for some of the most costly ones - including aluminum etch, and many of the tungsten-CMP and dielectric-CMP steps.

Second, using copper reduces costs because smaller lines can be employed to carry the same amount of current. Thus tighter packing-density can be achieved per level. This also implies that fewer levels of metal may be needed (see Fig. 16-7),[7] which significantly reduces manufacturing costs. This data indicates that for certain circuit applications only about half the number of levels are required if Cu is used instead of Al-lines and W-plugs.

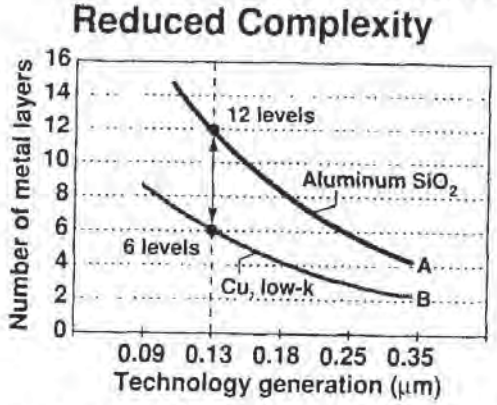


Fig. 16-7 One of the main benefits of copper, beyond the ability to increase chip speed and power consumption, is that the number of metal levels can potentially be reduced by as much as half.[1] Reprinted with permission of Semiconductor International.

4. The currently favored method for Cu deposition is electrolytic-plating, and this allows for much lower deposition temperatures that does Al sputtering or W-CVD. This enables the use of low-*k* dielectric materials whose thermal stability is lower than that of SiO_2.

16.1.2 Technological Challenges of Using Copper Interconnects

Although many powerful benefits can be gained if Cu is substituted for Al in the IC interconnect structure, a new set of technical challenges arise, including the following:

1. Cu does not form volatile copper fluorides and chlorides, making plasma etching of Cu impractical at temperatures below 200°C. Thus, another technique for forming Cu wires has been developed. Instead of patterning and etching Cu films, the Cu-films are first blanket-deposited over the entire wafer surface and into recesses in the dielectric layers. Then the Cu film is polished away by CMP in the flat areas, but is allowed to remain behind, in-laid in the recesses. This is the basis of *damascene* interconnect structure formation (as discussed in Chap. 15).

2. Unlike Al, Cu does not form a dense, self-passivating oxide on its surface. Thus, chemical reactions can continue to attack exposed Cu lines, making them more vulnerable to corrosion than Al lines.

3. Copper readily diffuses through SiO_2. If it is present in sufficient concentrations in a dielectric it can lead to shorts or leaky paths between conductors.

4. If the Cu manages to diffuse through the SiO_2 and then enters the silicon lattice, it will create deep impurity levels in the silicon bandgap. These levels act as *recombination/generation (R/G)* centers for free charge-

carriers. The presence of such R/G centers degrades transistor performance and causes *p-n* junction leakage. Copper can also precipitate at (or near) the silicon wafer-surface, and such metallic precipitates are known to cause defects in the gate-oxide as it is being grown. Cu is also a fast-diffuser in single-crystal silicon (i.e., it exhibits the highest diffusivity in silicon of all metal elements), and thus will quickly distribute itself everywhere within the bulk of the wafer (including in the device-regions near the wafer surface, where it can do the most harm). For these reasons, Cu is viewed as "poison" if it is present in the silicon lattice. As a result, special Cu processing areas are also set up in wafer fabs to keep trace amounts of Cu from contaminating any other areas of the cleanroom.*

5. Unlike Al (which reacts with SiO_2 to form a strong interface with excellent adhesion), Cu adheres very poorly to SiO_2.

6. The deposited copper films are polycrystalline in nature, and the preferred orientation of the crystal structure is a high (111)-orientation. Control of this orientation is important because resistivity, stress, adhesion strength, and electromigration resistance of copper layers are largely affected by the films crystal orientation.[17,53]

To prevent Cu from diffusing to the device areas of an IC, the interconnect structure must have the built-in reliability of several protective measures against this possibility. The primary line of defense involves totally encapsulating the Cu wires and plugs at all locations and at all levels to prevent copper from escaping. In dual-damascene interconnect processes, this is done in two-steps. In the first one, a *conductive* diffusion barrier-layer (e.g., Ta, TaN, or TiN) is deposited over the wafer after the trenches and vias of each level of metal have been etched in the dielectric stack, (but before the copper layer is put down). Thus, the insides of the trenches and vias of the damascene dielectric-stack are lined with a diffusion-barrier layer prior to deposition of the Cu into them. Such conductive barrier-layers must be effective against Cu out-diffusion and must simultaneously be thin enough to maximize the cross-section of the Cu-wires and plugs in the recesses. The second diffusion-barrier-layer is formed after the Cu-layer is deposited and the Cu structures have been polished with CMP. That is, a *non-conductive* diffusion-barrier-layer is deposited onto the wafer to seal the top-side of in-laid Cu structures (typically a CVD-silicon-nitride layer is selected to serve in this

* The use of Cu as an alloy in Al:Cu interconnects generates a completely different set of requirements for containing Cu atoms. That is, Cu-atoms alloyed with Al are immobilized by the aluminum matrix, which acts as a very efficient getter.

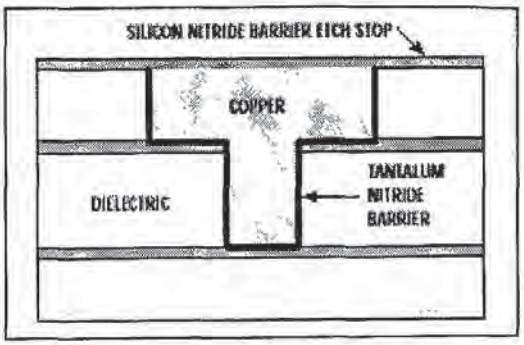


Fig. 16-8 Dielectric (silicon nitride) and conducting (tantalum nitride) barriers encapsulate copper in a damascene structure and protect against copper migration from interconnect structures to neighboring dielectrics and silicon.

role). Thus, Cu structures are ultimately enclosed on all sides by either a Ta (or TaN) or a silicon-nitride diffusion-barrier (Fig. 16-8).

The secondary on-chip line of defense is provided by W-plugs and phosphosilicate glass (PSG). The tungsten-plugs are used in the contact holes as a secondary barrier that keeps the first level of Cu-lines physically separated from the Si substrate (and this also means that a *single-damascene* process is used to form these W-plugs as well as the first level of Cu wires). PSG is known to getter metal atoms. The last level of protection on the chip itself is provided by a bottom silicon-nitride-layer, which further blocks the underlying silicon substrate from migrating Cu atoms.

While manufacturing protocols must also be modified to tightly control cross-contamination, the Cu-contamination problem does not seem to be as difficult as it first appeared to be. For example, fabrication tools cannot be shared between front-end and back-end processes, but copper manufacturing lines can be built in shared cleanroom facilities with aluminum interconnect manufacturing lines. Cleaning procedures must also be implemented to ensure that no detectable traces of copper are present on the bevels and backsides of wafers after processing.

Additional procedures have also been developed to heighten awareness of production workers and to contain copper contamination. For example, copper personnel in some fabs (especially maintenance technicians) wear cleanroom gowns that are used only in the copper bays, and they may not enter non-copper stations when wearing them. Specially colored wafer-carriers and conspicuous labels (indicating the presence of copper-products) are used to clearly identify wafers that have received copper processing and to segregate them from wafers that have not been subjected to copper processes.

Protocols also require that once a wafer has entered a copper bay it cannot return to a noncopper bay. In practice, however, wafers that leave the *front-end-of-line* (FEOL) after the contact holes to the silicon substrate have been opened, move to the *back-end-of-line* (BEOL), where the copper fabrication occurs. There is really no reason why the wafers should have to re-enter the FEOL part of the fab after that part of the process sequence is completed. Additional information on preventing cross-contamination from Cu is given in Sect. 16.7.

To counteract the problem of poor adhesion of Cu to oxide, the conductive diffusion-diffusion films under the Cu layers must also serve as adhesion promoters. The adhesion/diffusion layers used under the inlaid Cu features in damascene processes must therefore meet several criteria:

1. They must act as good adhesion-promoters for Cu onto SiO_2. That is, the adhesion/diffusion-layer materials should adhere well to oxide, and then the Cu films should adhere well to them.

2. They must be effective barriers against Cu diffusing through them under all post-copper-deposition temperatures.

3. They should exhibit low resistivity. That is, diffusion-barrier materials will be expected to exhibit resistivities of less than 1000-$\mu\Omega$-cm to meet the needs of advanced interconnect processes. This will keep the total resistivity of the composite Cu/barrier interconnect-structures below the resistivity of comparably-thick Al-alloy/barrier interconnect lines.

4. They should retain their diffusion-barrier properties when they are very thin, because they do not have the low-resistivity of Cu. That is, thinner diffusion barriers for Cu will be needed than for Al because in-laid-Cu interconnects require the barrier-layer to be formed on at least three sides of the Cu conductor (Fig. 16-9). To keep the lower-conductivity barrier-layers from impacting the resistance of the interconnect line, they must thus be relatively thinner for Cu lines.

5. They should protect the Cu from oxidation and corrosion.

6. They should be able to make a low-resistance contact to the copper layer of the metal-level under it, and this barrier-layer/Cu interface should exhibit good electromigration reliability characteristics.

7. They should provide a surface which will facilitate the nucleation of the Cu-seed layer deposited on it. Furthermore, the surface-condition and micro-

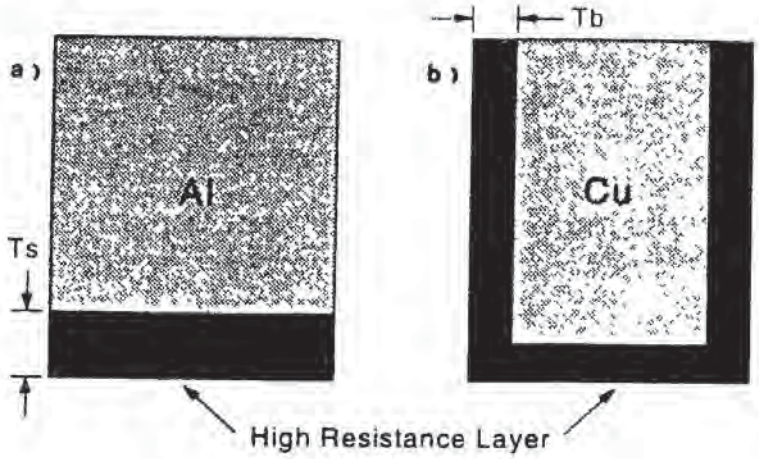


Fig. 16-9 Interconnect cross-sections showing the impact of higher resistance shunt or barrier layers: (a) Al interconnect; (b) Cu interconnect.[7] (© 1995 IEEE)

structure of the barrier-film can strongly affect the texture and grain-size of the deposited Cu (and these in turn, are critical in determining electromigration reliability).[50] Thus, the barrier-layer is also vital to seeding the desired Cu microstructure. Since the growth of Cu layers with a (111) preferred orientation provides Cu films with the best overall characteristics, the barrier-layer should enhance such Cu-structure.

In addition to the above materials-science issues associated with the use of copper, there are a number of difficult manufacturing challenges that will also have to be met when integrating Cu into an IC fabrication sequence. That is, getting a copper process (or any process) online and productive quickly is the key to profitability. The integration issues involved in bringing a Cu process to full-production are summarized in Fig. 16-10,[15] and they will be discussed in more detail in later sections of this chapter.

16.2 OVERVIEW OF COPPER PROCESS TECHNOLOGY

Before the details of depositing, polishing and cleaning copper IC interconnect structures are described, it is useful to give brief overview of the entire sequence of processes that are required to form a single-level of a copper dual-damascene structure. The sequence of process steps is as follows (and is also depicted in Fig. 16-11):

1. Non-Conductive Diffusion-Barrier-Layer Deposition
2. Dielectric Stack Deposition

3. Dual-Damascene Dielectric-Stack-Etch (Via, Trench, and Diffusion-Barrier-Layer Etch)

4. Conductive Barrier-Layer Deposition

5. Copper Seed-Layer Deposition

6. Copper Electrofill (and Annealing after Deposition))

7. Copper and Barrier-Layer CMP

8. Copper Clean

9. Non-Conductive Diffusion-Barrier-Layer Deposition.

The sequence starts by depositing a non-conductive diffusion-barrier-layer (e.g., a thin film of silicon nitride by PECVD) over the entire wafer (which has been planarized by a previous CMP step and may already contain one or more levels of metal). Next the remainder of the ILD stack is deposited (as described in detail in Chap. 15, Sect. 15.6). Using a lithography process, the vias and trenches of the dual-damascene structures are aligned to the previous layers of the circuit and are then etched with a dry-etch process. (This requires a sequence of two lithography and etch procedures, including stripping the resist after each etch step.) The SiN diffusion-barrier-layer at the bottom of the vias is also opened during the second of these etch steps, exposing the metal-layer of the previously formed level of the interconnect structure. Next, a conductive diffu-

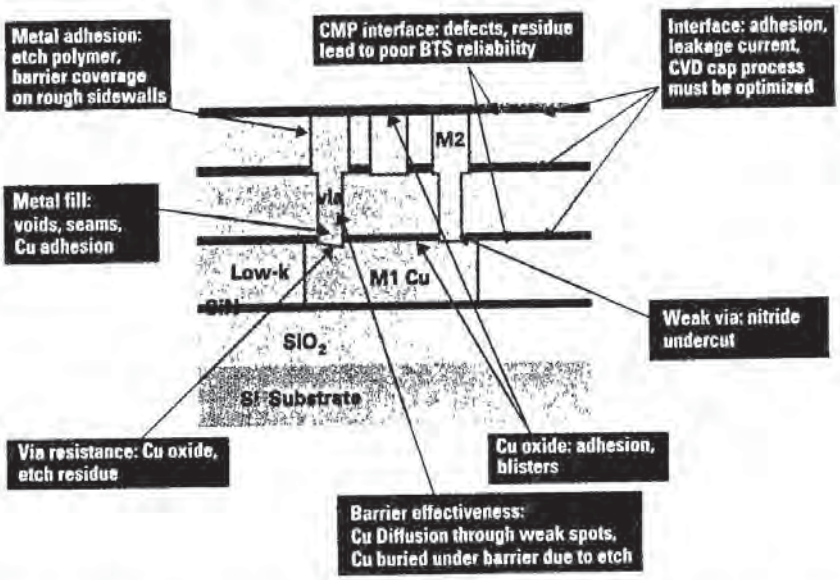


Fig. 16-10 Possible failure types associated with damascene processing pertain to film adhesion, barrier and metal fill capability, copper oxidation, and CMP defects.[9]

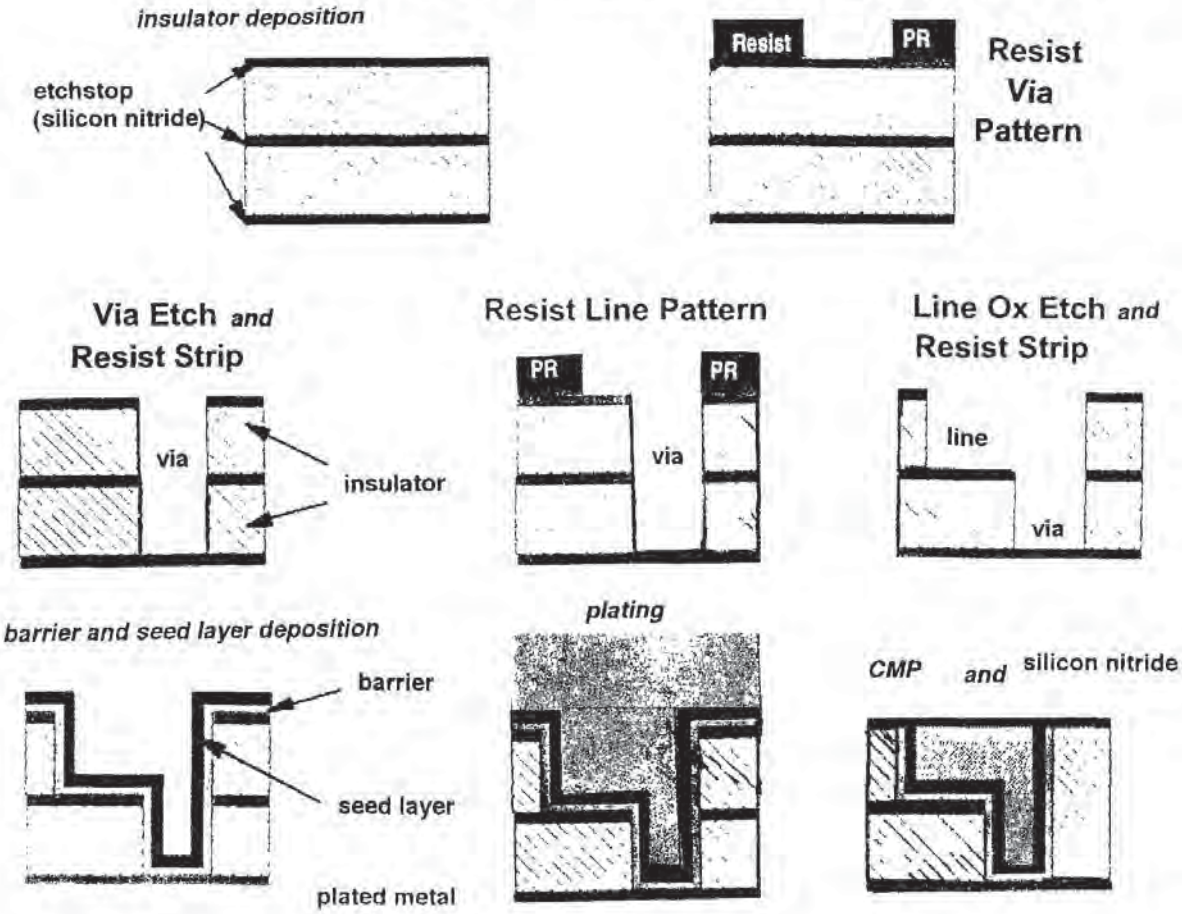


Fig. 16-11 Process sequence for forming a single-level of Cu metal in a dual-damascene interconnect structure (using a *via-first* approach).

sion-barrier/adhesion-layer is blanket-deposited onto the wafer, typically by PVD (with either a collimated-, a long-throw-, or [most typically] an ionized-metal-PVD process). Various materials have been selected to perform the role of this diffusion-barrier/adhesion-layer including Ta, TaN, TaSiN, TiN, TiSiN, WN, and WSiN (see Sect 16.3).

A copper seed-layer is deposited onto the diffusion-barrier/adhesion-layer to provide a low-resistance path for the copper electroplating process that comes next. The Cu-seed layer is also deposited *in situ* (i.e., without an air break) by one of same type of PVD-processes used to form the diffusion-barrier/adhesion layer film. Completing the process of filling the trenches and vias with Cu material is done with an electrolytic-plating technique. The key attributes of such Cu electrolytic-plating-processes include: **a**) the ability to fill the recessed structures without defects (i.e., no voids or seams should exist in the plated films after filling); **b**) the ability to achieve high-deposition rates; and **c**) the ability to

obtain uniform deposition-thickness across-the-wafer, and from wafer-to-wafer (e.g., ±2% across a 200-mm wafer with a 5-mm edge exclusion).

A CMP process is carried out next to remove any excess copper above the vias and trenches (called the *overburden*), but allowing metal to remain in the damascene recesses. During the CMP process, the diffusion-barrier-layer must also be removed. A key technological challenge involves achieving the same polishing rate on the diffusion-barrier layer, because such materials as Ta or TaN are hard, refractory metals (or metallic compounds), while copper is a comparatively much softer metal. After the CMP process is finished, it must be ensured that the wafer is cleaned, such that no copper residue remains on the oxide on the frontside of the wafer (nor on the wafer backside or beveled edges). Finally, another non-conductive diffusion-barrier film (e.g., CVD silicon-nitride) is deposited onto the wafer surface, which serves to cap-off the copper (i.e., this completes the encapsulation of the recessed-copper structures, ensuring they are surrounded by a diffusion-barrier-material on all sides).

The details of the first three steps of this sequence are described in Chap. 15, Sects. 15.6 and 15.9 (and thus will not be repeated here). The discussion that follows therefore begins with the Step **4** (Diffusion-Barrier-Layer Deposition, and the properties of such materials) and then proceeds to cover the details of the remaining steps of the process sequence.

16.2.1 The Transition from Aluminum to Copper Interconnects

The process of incorporating copper into the interconnect process of an IC technology may be done in one of two ways. Some manufacturers have decided to use Al:Cu (and W-plugs) for several of the lower levels of a multi-level metal interconnect structure, and limit copper to the upper levels. In one such example, Al:Cu was used in the four lower levels of the 6-level metal interconnect structure and Cu for the upper two levels (Fig. 16-12).[10] Another process described by TSMC also uses four aluminum levels of metal and two of copper.[11] The interface between the top aluminum interconnect level and the lower Cu interconnect level can be implemented either with a W-plug or with a Cu-damascene via structure.[12]

On the other hand, other manufacturers decided to use copper for the entire interconnect structure (with the exception of W-plugs being used in the contact holes). An example of such a 6-level Cu-interconnect-structure (with W-plugs used to make contact to the Si-substrate) was described by IBM (see Fig. 16-13).[13] Figure 16-14 shows a SEM of a perspective view of a six-level metal Cu interconnect structure (see also Fig. 12-16 in Chap. 12).

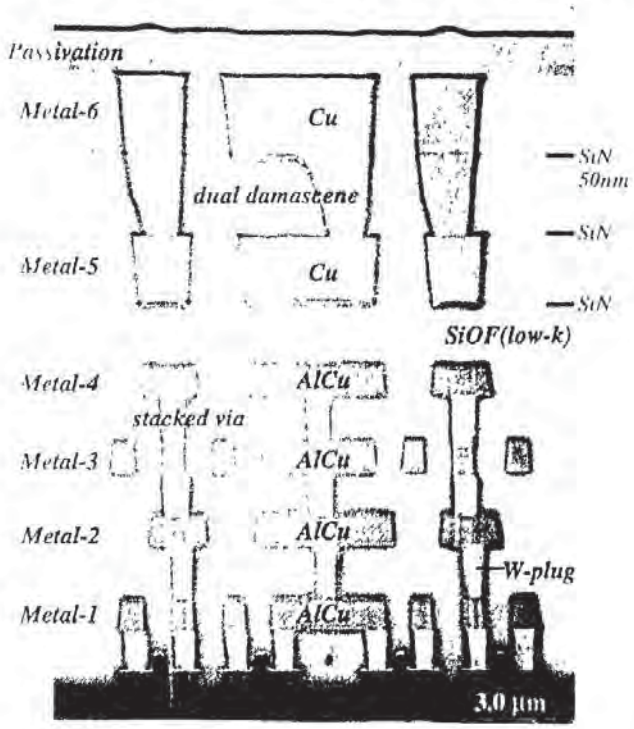


Fig. 16-12 Cross-section of six-level metal structure with the first four-levels being Al:Cu/W-plug interconnects and the top two levels of Cu metal.[10]

16.2.2 The Key Goal of Depositing Copper into Damascene Recesses

One of the most important aspects of depositing copper successfully into the recesses of a dual-damascene ILD stack is ensure it done without any voids or defects. The key to being able to do this is to fill the recesses with copper from

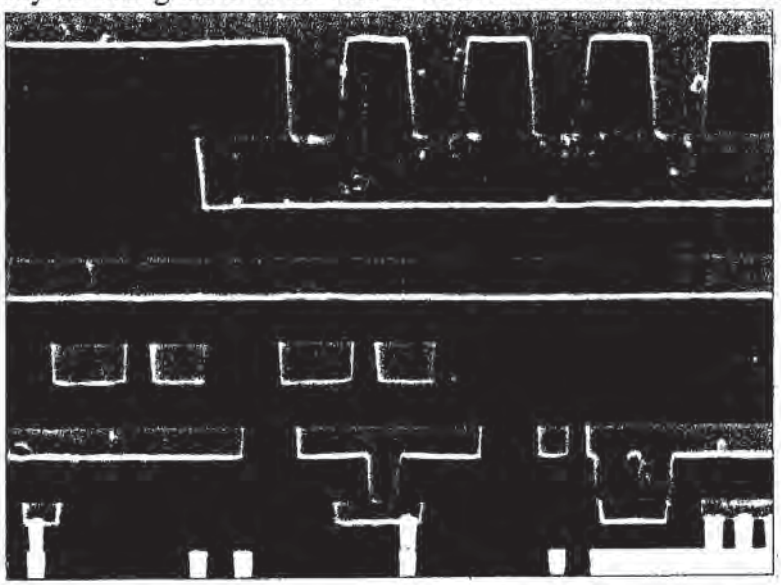


Fig. 16-13 Cross-section of six-level metal structure with all levels of Cu metal.[13]

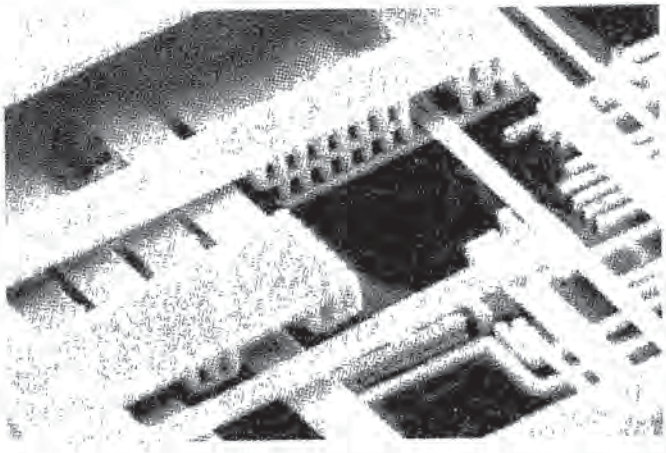


Fig. 16-14 An SEM of a perspective view of a six-level metal Cu interconnect structure.[32]

the bottom up, a technique called "bottom-up" filling, or "superfilling." However, successful superfilling is affected not only by the electrofill process but also by the dielectric etch process, the barrier-layer deposition-process and the seed-layer deposition-process. Thus, this topic has to be addressed in a piecemeal fashion, as will be done in the three upcoming sections.

16.3 BARRIER LAYERS FOR COPPER INTERCONNECTS

As discussed previously, to stop Cu from diffusing into the dielectric materials in which it is embedded (or into the Si substrate), it must be surrounded by a barrier-layer on all sides. The underlying layer is deposited prior to depositing the copper (as noted in Sect 16.2). In this section, the technology for forming these conductive barrier-layers is described. The subjects that will be covered are:

1. The impact of the barrier-layer on the Cu-electroplating process;
2. The technology of depositing barrier-layers into damascene recesses by PVD;
3. The material properties of tantalum (and TaN & TaSiN) barrier-layers;
4. The other candidate materials for Cu-technology barrier-layers (including CVD processes for depositing such materials).

16.3.1 The Impact of the Barrier-Layer Deposition Process on the Filling of Damascene Recesses with Copper

To recap, a barrier-layer for Cu interconnects must prevent Cu diffusion into the ILD and must assure good adhesion between the Cu and the ILD. Furthermore, the barrier must be thin, conformal, and have a low electrical resistivity. Deposition should be at a low temperature with few particles being produced.

The barrier-layer material should also be compatible with CMP of Cu and with the Cu electroplating process. Finally, there a number of other aspects involved with the deposition of the barrier-layer that impact the ability to completely fill damascene recesses with copper without voids. These include depositing a barrier-layer that is continuous and adequately thick everywhere along the recess surfaces (typically 25-30-nm-thick), and with little (or better yet, no) overhang. The PVD-process used to deposit the barrier-layer impacts these last two factors, and the PVD techniques for depositing seed and barrier layer is discussed next.

16.3.2 Introduction to the Technology of Depositing Barrier-Layers for Cu Interconnects

The conductive barrier-layer deposited into recessed damascene features before the Cu is deposited can be done by PVD or CVD. While PVD has been the most widely used method down to at least the 0.13-μm technology node, there may be a change to CVD at some point. One reason for such a technology replacement involves the formation of a film within a trench or contact hole by a *physical vapor deposition process*. Assume a contact-hole exists with the top face being open with the dimensions of a cube of side **a**. This represents a contact hole with an aspect ratio of 1:1. In such a case there are five inner surfaces of the cube that must be covered by material which would otherwise deposit on area $\mathbf{a}^2$ on the top surface of the cube (i.e., if the top of the cube was not open, see Fig. 16-15). However, if the top of the contact hole is open, the total area inside the hole that must be covered now is $5\mathbf{a}^2$. Thus, if the material that would have covered $\mathbf{a}^2$

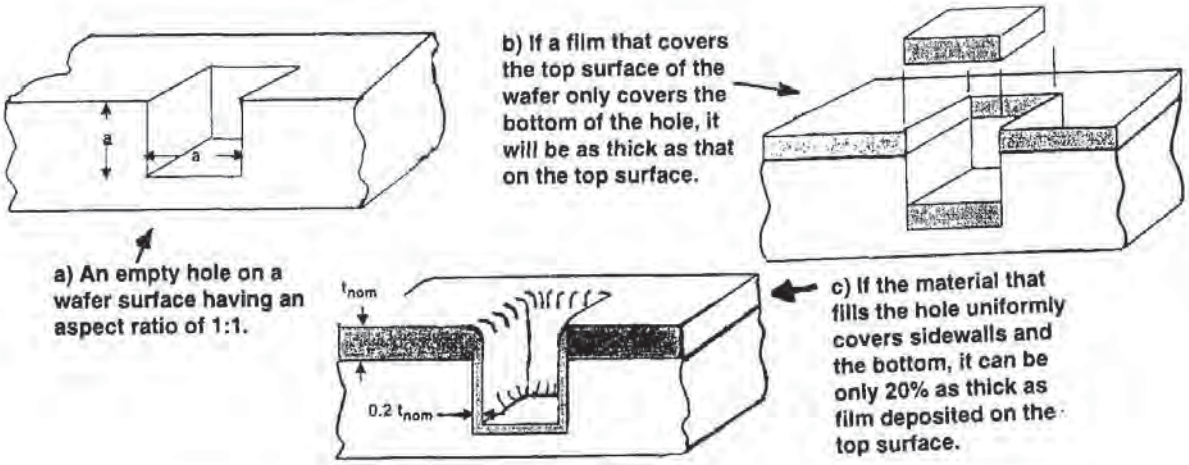


Fig. 16-15 One dilemma faced when forming films in high-aspect-ratio holes with PVD.

is evenly distributed onto all five insides of the contact hole, the film thickness will only be 20% as thick as that on the flat areas outside of the contact hole. Obviously, if the area of the hole-opening remains constant while its depth is increased, the aspect-ratio will also increase (e.g., if the square contact-hole opening-size remained at $\mathbf{a}^2$, but the depth became 2**a**, the aspect ratio will increase to 2:1, and the area that will have be covered by the material of $\mathbf{a}^2$ will now be $9\mathbf{a}^2$). Thus, for the case of a physical-vapor deposition process, as the aspect-ratio of a recessed feature is increased, the material entering the feature must be spread over a larger area, making the thickness per unit area decrease. Furthermore, if the film on the upper flat regions must be etched or polished away after the hole has been filled, a much thicker film now has to be removed (which makes the etch or CMP process task significantly more time consuming and difficult). Deposition by CVD may be able to avoid this problem because CVD processes can be reaction-rate limited (allowing deposition to be almost 100% conformal at a very high-aspect-ratio, see Vol.1, Chap. 6). Thus, CVD may be employed for depositing barrier-layer films for Cu in the lower levels of deep-submicron interconnects (where the aspect-ratios continue to increase).

In the previous discussion it was noted that it becomes progressively harder to fill contact holes by PVD as the aspect-ratio increases. A related problem further increases the difficulty of filling high aspect-ratio-recesses. Recall that the sputtered-atoms undergo collisions as they are transported in the gas-phase in the space between the target and the substrate. In addition, sputtered atoms leave a planar-target surface from each point at which sputtering occurs in directions that roughly exhibit a cosine distribution. As a result of these two mechanisms, in a conventional sputtering apparatus the sputtered-atoms will arrive at the upper corners of the trench or contact hole on the wafer from a larger arrival-angle than they will at surfaces inside the recess. Thus, the film deposition-rate at the top corners of the recess will be higher than along its sidewalls or bottom. As a result, the top opening will begin to close off (i.e., an *overhang* will start to form), as shown in Fig. 16-16a. Thus, for this case, as time goes on (Fig. 16-16b) the deposition-rate onto the sidewalls and bottom will continually decrease. If the overhang gets thick enough, the hole will close entirely, leaving a void or keyhole.

Even if deposition does not continue long enough to completely close-off the opening, the overhang will shadow the bottom corners of the contact hole, where the arrival angle for sputtered atoms is already the smallest (see Fig. 16-16b). Thus, the deposited film will be thinnest at the bottom corners of the hole. Since a barrier-film must have a minimum adequate thickness along the entire bottom

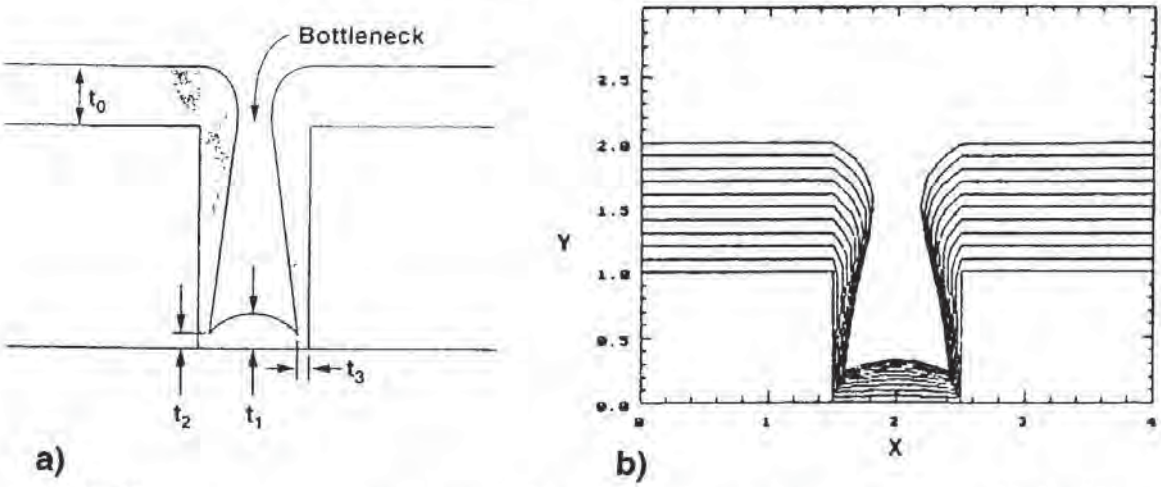


Fig. 16-16 a) Deposition of a sputtered film into a contact hole or via having a high aspect ratio. b) Development of a bottleneck due to the buildup of an overhang on the top corner.

of the hole in order to function effectively, such thin-spots at the corners can jeopardize the effectiveness of the barrier-layer.

Various methods have been explored to overcome this thinning of the film at the bottom corners of contact holes (including the use of CVD). However, modifications to the sputtering process have also been pursued. Two such early methods were *collimated sputtering* (in which a honeycomb baffle - i.e., a *collimator* - is inserted into the space between the target and the wafer to trap obliquely-directed vapor) and *long-throw-sputtering* (in which the target and wafer are separated by a distance 2–4 times longer than in a conventional magnetron source, and the plasma is also operated at a lower pressure). However, these two methods have proven to be inadequate for deep-submicron, dual-damascene applications. It is unlikely that they will even be commercially developed for 300-mm wafer processing. Thus, they will not be discussed further here (but more information on them is available in Vol.1, 2nd Ed, Chap. 11).

16.3.3 Ionized Magnetron Sputter Deposition

While the two sputtering techniques described above produce adequate barrier-layer films for contact-holes and vias for 0.35-μm (and some 0.25-μm) CMOS technologies, they appear to fall short for other 0.25-μm (and smaller) contact holes and vias when the aspect-ratio exceeds about 3:1. Thus, an alternative to collimated (or long-throw) sputtering, namely *ionized magnetron sputtering*, or *I-PVD* (also termed *ion metal plasma* [*IMP*] by Applied Materials), has been developed to deposit the next generation of ULSI barrier-layers with PVD. In this method, a large fraction of the neutral sputtered-metal-atoms are ionized while in flight between the target and the wafer. A bias on the wafer then causes an

electrical acceleration of these ionic species to the wafer-surface with a controlled energy and direction (i.e., perpendicular to the wafer surface).[14,15,16] There have been several sputtering-source configurations developed to implement the ionized magnetron sputtering technique.

Figure 16-17a shows a schematic drawing of an ionized magnetron sputtering chamber used in the first commercially available I-PVD tools. A conventional magnetron source (powered with a dc power-supply) remains in place to sputter neutral metal-atoms from the target. (The magnetron produces a plasma and dark space that is confined near the target surface.) However, an rf-powered (and water-cooled) coil is now also located within the chamber (Fig. 16-17b). This coil inductively couples energy from a second 13.56 MHz rf-power supply into a secondary plasma downstream of the magnetron plasma. By increasing the pressure in the chamber to 20-40-mtorr (up from the 5-mtorr of a conventional magnetron sputtering process), and by increasing the depth of the secondary plasma to 8–10 cm (by increasing the distance between the cathode and the wafer chuck), the number of collisions experienced by the sputtered atoms before they

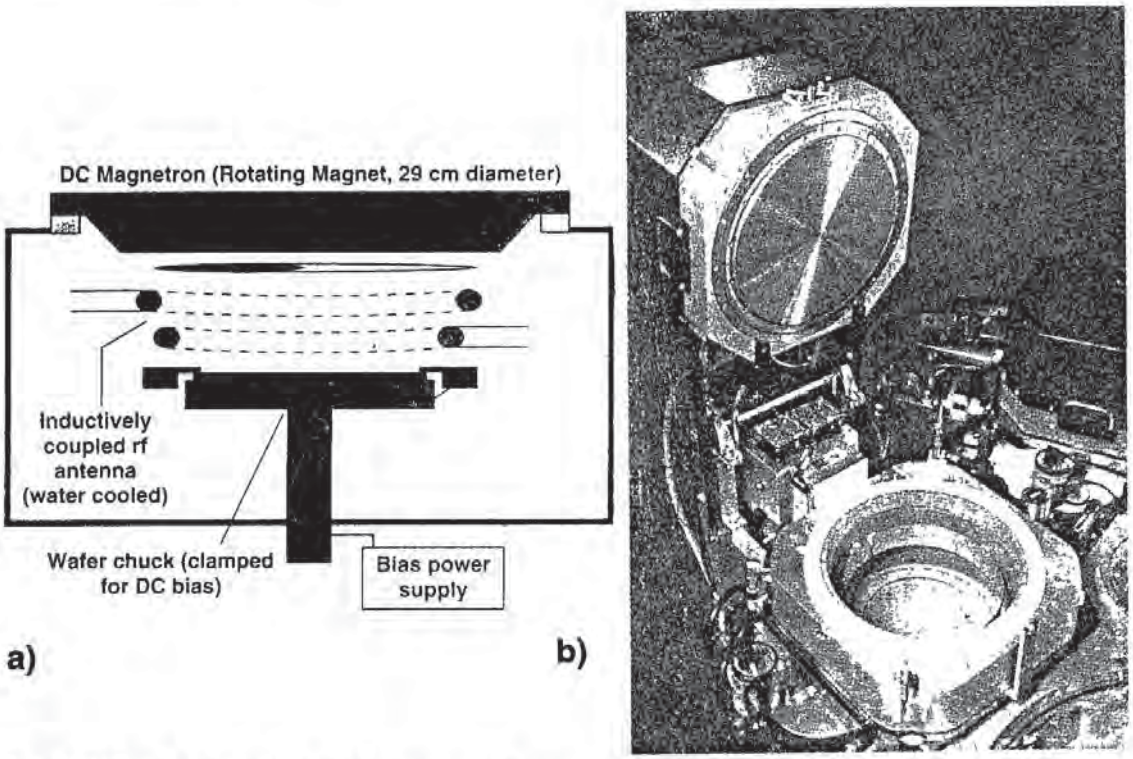


Fig. 16-17 a) Schematic of a magnetron sputter chamber fitted with an rf-coil which allows an ion magnetron sputtering process to be implemented. b) Photograph of an Applied Materials IMP system showing the internal coil. (Courtesy of Applied Materials)

arrive at the wafer (as well as their transport time through the gas phase), is increased. This longer transport time, and the fact that the ionization potential of metal atoms is much lower than that of Ar atoms, allows a much higher fraction of the metal atoms to be ionized by this secondary plasma (e.g., for a Ti-sputtering process, typically 50-70% of the sputtered Ti-atoms are ionized). A medium-density secondary-plasma is thus created in the region between the cathode and the wafer ($5x10^{11}$-10^{12} ions/cm^3).

The chief advantage of the I-PVD approach can now be exploited. That is, by applying a negative-bias to the wafers, the ionized metal-atoms can be accelerated toward the wafer surface (at voltages ranging from a few to several-hundred volts, depending on the specific application). Thus, the metal ions will strike the surface exactly at normal incidence to the wafer surface, regardless of their original trajectory. In addition, the third (substrate-bias) power-supply allows the kinetic energy of the metal ions striking the wafer to be controlled. Using an rf-power-supply to produce this bias overcomes the problems with insulating wafer surfaces (or backsides). Note that the ion-flux onto the wafer results in power dissipations ranging from about 25 watts to several hundred watts, which calls for some degree of wafer cooling.[16]

The bottom-coverage of high-aspect-ratio holes with I-PVD is better than that observed with collimated sputtering. That is, 40–80% bottom coverage has been achieved on 0.18-μm holes with aspect-ratios of up to 8:1.[17] Note that while the bottom-coverage is high, the sidewall-coverage is much thinner (although the film on the sidewall is continuous, see Fig. 16-18).

Several other advantages of I-PVD processes should be noted. First, much better target-utilization is obtained than with collimated sputtering (as almost all of the sputtered atoms arrive at the wafer surface, instead of some being intercepted by the collimator). Sputtering tool throughputs are therefore also increased. Second, the high flux of metal ions (as well as some Ar ions) directed perpendicularly onto the wafer surface appears to re-sputter the atoms that would otherwise form an overhang at the top-corners of a recess. This keeps the top opening of contact holes and vias from closing up. Figure 16-18 shows the coverage of the sidewall and bottom of a high-aspect ratio hole with I-PVD. Third, the negative-bias applied to the wafer not only causes the ionized metal atoms to preferentially strike the bottom of the via, but it allows the kinetic energy of these metal (and Ar) ions bombarding the wafer to be adjusted. For appropriate bias levels, re-sputtering from the feature base can be produced, which redistributes sputter-deposited material onto the lower sidewalls (Fig. 16-19). This is exactly where the lowest PVD coverage occurs in collimated and

Fig. 16-18 SEM showing the coverage of the sidewall and bottom of a high-aspect ratio hole deposited by I-PVD. (Courtesy of Applied Materials)

long-throw PVD-processes. The process of local re-sputtering can also be used to tailor the conformality of the deposit to a greater degree, and this has extended the use of PVD for depositing barrier-layer and seed-layer films.

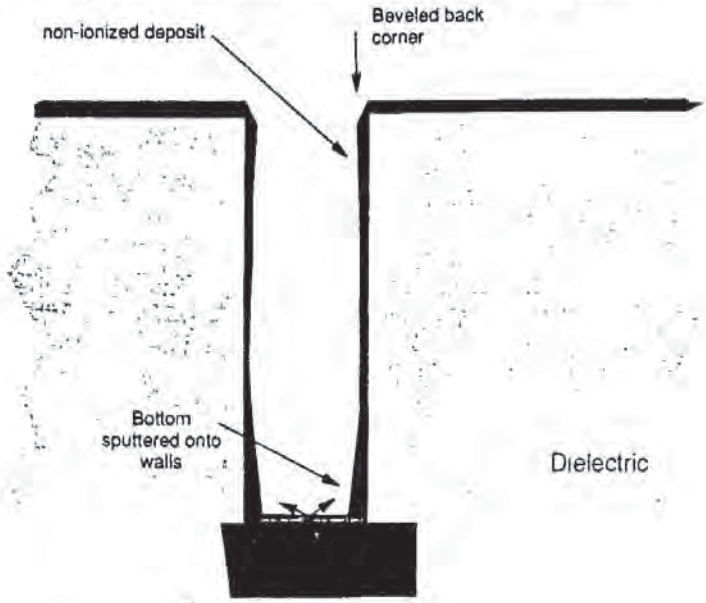


Fig. 16-19 Schematic drawing of I-PVD deposition of a high-aspect-ratio recess showing the effects of re-sputtering of the deposited film.

While the concept of I-PVD has the many advantages described above, the internal coil-configuration has some practical difficulties. First, the coil can get coated with the sputtered metal. If this gets too thick, the film may flake off and produce particles. Second, material from the coil itself can be sputtered, with some material ending up being re-deposited on the wafer. While a copper coil can be used to circumvent this problem when depositing Cu-seed-layers, this does not provide a fix when depositing Ta or Ti barrier-layers. Instead, a coil made of Ta (or Ti) would be needed, but forming such coils (which must also accommodate the flow of cooling water) is not a trivial task. As a result, two other I-PVD source configurations have recently been commercially introduced.

16.3.4 Hollow-Cathode Magnetron Sputtering Source

The *hollow-cathode magnetron* (HCM™) used in the Novellus INOVA™ sputtering system (Fig. 16-20) employs a similar technique to ionize sputtered atoms as they are transported to the substrate.[42,55] A uniform plasma throughout the volume of the cup-shaped hollow cathode target provides sputtering from a large fraction of the area of the target surface. Due to the geometry of the cup-shaped target a significant fraction of the sputtered neutrals are re-deposited on the target surface, where they can be sputtered again (instead of depositing on the chamber walls). This provides the benefit of high target utilization. In addition, no internal rf-coil is needed to generate the high-density plasma that ionizes the sputtered metal atoms. Instead, the orientation of the permanent magnets allows

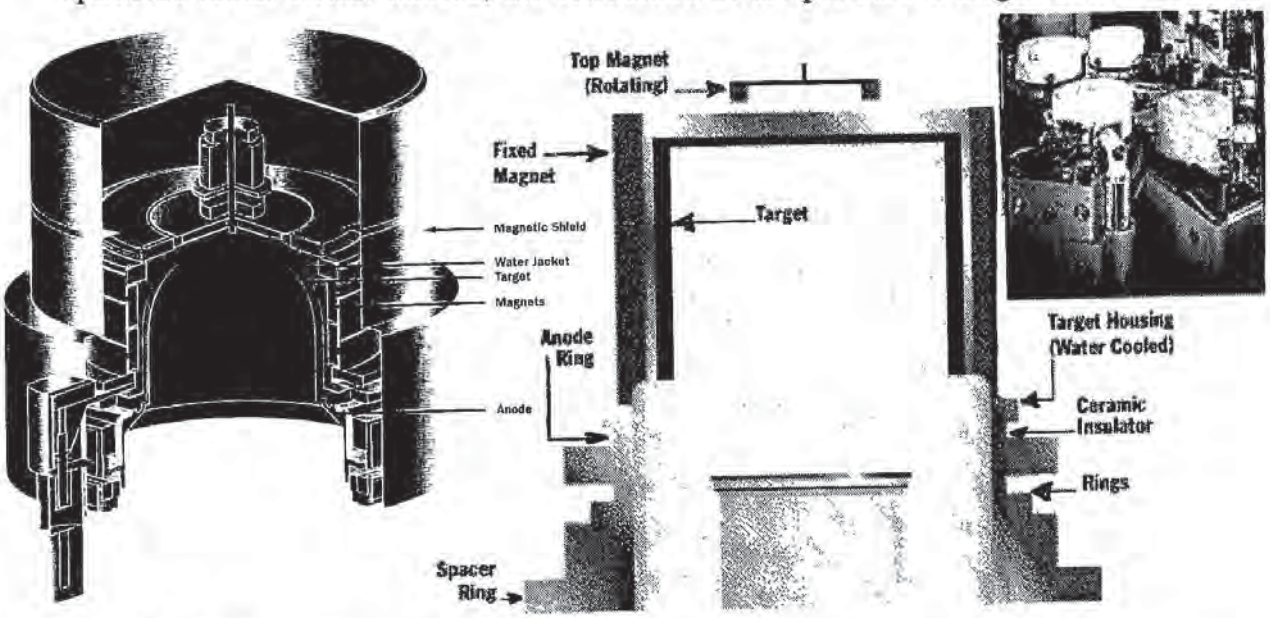


Fig. 16-20 Cutaway drawings of the hollow-cathode magnetron source used in the Novellus Systems's INOVA® sputtering system. Courtesy of Novellus Systems, Inc.

the electrons emitted by the target to efficiently ionize the sputtered neutrals (with the degree of ionization exceeding 90%). A bias on the wafer-chuck accelerates the ionized sputtered atoms toward the wafer in a direction perpendicular to its surface, allowing good coverage of high-aspect-ratio holes. The HCM can be used to sputter Ta, TaN, TiN, and Cu.

16.3.5 Self-Ionized-Plasma Sputtering Source

Another new sputtering source for implementing the I-PVD technique was recently introduced by Applied Materials. They refer to this source as *self-ionized-plasma* (SIP), and the internal rf-coil used in their IMP™ source to ionize the sputtered metal atoms is not needed. While few details about this source have been published, some of its aspects have been described.[18,19] The source operates at relatively low pressures (< 2 mTorr) with a target-to-substrate distance that is increased above the distance used in conventional magnetron sputtering sources. These measures increase the mean free path of the metal-ions and provide additional self-collimation to the metal-atom trajectories. The term *self-ionized-plasma* probably refers to the phenomenon in which some of the sputtered metal atoms that are ionized by the source, return to the target with enough energy to sputter other metal-atoms (and also produce additional electrons). These additional electrons, in turn, ionize more of the sputtered metal atoms, which keeps the plasma self-sustaining and produces more metal-ions. The phenomenon is apparently an efficient way of ionizing metal-atoms that have a small ionization energy (such as Cu). However, questions have been raised about whether it is effective for metals that have higher ionization energies (such as Ta).

16.3.6 Material Properties of Tantalum and Refining Tantalum Metal For Semiconductor Applications

The metal *tantalum* (or such tantalum-based compounds as TaN or TaSiN), have been the most commonly used barrier-layer materials for Cu-damascene interconnects. As such, it is useful to give some background about this element.

16.3.6.1 Material Properties of Tantalum: Tantalum is an uncommon (in nature) refractory metal, with an atomic-number of 73, an atomic-mass of ~181, a body-centered-cubic (BCC) crystal structure, and a steel gray color. It is an attractive Cu-barrier-material because of its high melting point (2996°C), and because it is immiscible with Cu. It is also a highly reactive metal that forms strong metal-metal and metal-oxygen bonds (much like titanium). Thus, it provides a low-resistance ohmic contact and good adhesion to the copper above (and to the

dielectric material below) it in the Cu-damascene metal scheme. Doping the Ta with a few percent nitrogen blocks grain-boundary diffusion-paths. More heavily nitrided Ta (produced by reactive sputtering of Ta in the presence of nitrogen) can also be used as a barrier-layer. Such TaN barrier-layers will be discussed further later.

16.3.6.2 Refining and Forming Tantalum Metal For Sputtering Targets: Tantalum exists in nature as an oxide Ta_2O_5. The principle ore of tantalum is *tantalite* (Fe, Mn)Ta_2O_5. Mines in western Australia are the largest producers of high-grade tantalite, and such concentrates are shipped to the tantalum metal manufacturers for refining.[20] The main market segments for refined tantalum are capacitor-grade powder (about 50%), mill-products and wires (16%), chemical compounds (such as tantalum carbides, 14%), and use as a metal-alloy additive (6%). High-performance tantalum products such as *sputtering targets*, represent less than 10% of the tantalum mill-product and wire business.

Tantalite ore is not the only source of tantalum. Nearly 25% of the total Ta production is recycled. In fact, if the market for high-quality sputtering targets outpaces the rate of increase in tantalite production, it might become necessary for wafer manufacturers to return spent targets to the Ta manufacturers in order to be assured of future availability.

The extraction and refining processes for tantalum conclude with a chemical precipitation reaction that yields Ta metal in powder form. The high-density, metallurgical-grade powders (and recycled Ta scrap) are used as feed for *vacuum melting*. (Because tantalum exhibits a great affinity for oxygen, nitrogen, and carbon, thermal treatments must be conducted in a vacuum or inert gas atmosphere.) For demanding applications (such as sputter deposition), the refined tantalum must possess a number of material properties that can be obtained by subjecting the tantalum powders to such vacuum melting processes.

Typically, tantalum ingots are melted several times to purge most of the impurities from the metal. Because the melting point of Ta is much higher than most materials, this is effective in volatilizing the interstitial gases (such as O, N, C) and many metal impurities. However, the other refractory metal elements (i.e., niobium, molybdenum, and tungsten) are not volatilized during vacuum melting, but remain as soluble impurities in tantalum. However, these refractory metal contaminants can be minimized through specialized front-end chemical extraction processes, resulting in extremely pure-Ta ingots. For example, the Performance Materials Division of Cabot Corp. (Boyartown, PA) offers Ta-ingots that are 99.999% pure.

The pure ingots consist of poly-crystalline Ta with small-sized grains. These ingots can be cold-worked (i.e., at ambient temperature) to cause a re-crystallization of the grain structure in the finished annealed product. The desired microstructure for Ta sputtering targets is a fine, homogeneous polycrystalline structure. Tantalum crystal grains predominantly have a (111) or (001) type structure. It is preferable to have a Ta ingot with a preponderance of (111) grains. This is because Ta sputtering-targets which contain large (001) clusters exhibit lower sputtering yields. The reason is that in such body-centered cubic (BCC) metals as Ta, the erosion-rate of (111) incident planes is predicted to be far greater than for (001) crystals.[21] The proportion of (111) to (001) grains is governed primarily by deformation history.

In summary, attaining microstructural and textural homogeneity in tantalum sputtering targets through the use of proper thermochemical processing is critical to assuring the performance of such targets. It should also be noted, that all of the refining and thermochemical processes are expensive. In turn, this also makes Ta sputtering targets quite costly (reaching $40,000 or more for some target configurations).[22]

16.3.6.3 The Properties of Tantalum (and TaN & TaSiN) as Cu-Barrier Layers: To prevent the drift or diffusion of Cu atoms, a barrier-layer should not react with Cu. Such a barrier-layer should remain thermally stable up to the maximum temperature that the wafer will be subjected to once the Cu has been deposited. Since this temperature is not likely to exceed 500°C, the barrier-layers should be stable to this temperature. Ta and TaN films are observed to remain thermally stable up to about 550°C, and thus they are capable of meeting this requirement for back-end processes.[23]

However, as noted in Sect. 16.1, the barrier-layer materials must also serve as adhesion layers for Cu. There is typically a tradeoff between barrier integrity and adhesion performance with Cu. If a thin-film of the barrier-layer material does not react with Cu at all, it may exhibit poor adhesion. If the material reacts too easily, it may not function as a good diffusion-barrier. For good barrier properties and good adhesion with Cu, an ideal barrier would react with Cu to some self-limiting extent.

Tantalum films, sputter-deposited using a Ta target in an Ar ambient, have been investigated for such Cu barrier-layer applications. For the case of Ta, an as-deposited Cu-layer on a Ta film displays an abrupt interface with Ta. However, a 3-nm thick amorphous layer is observed at the Ta/Cu interface after annealing for 1 hour at 400°C.[24] The mechanism for the amorphous layer

formation is not clearly understood because Ta has no equilibrium solubility with Cu at 400°C, and does not form compounds with Cu. Nevertheless, it is believed that the thin amorphous-layer improves the adhesion between Ta and Cu. In addition, the Ta film has the advantage of serving as a nucleation layer for Cu, enabling Cu films with (111)-orientation to be deposited.[25]

On the other hand, Ta barrier-layer films deposited by PVD are polycrystalline films. Thus, even though the reaction between Ta and Cu at 400°C occurs over only a short distance, the Cu may diffuse along the grain boundaries of the Ta film and escape into the neighboring dielectric material. Thus, by itself, Ta may not prove to be an adequate barrier-layer.

TaN is a related material to Ta, having a high melting point of 3087°C and a more dense microstructure. It is also typically deposited by PVD using a Ta target, but with nitrogen added to the argon gas in the sputtering gas ambient. Thus, as the reactive Ta is sputtered onto the wafer, it reacts with the nitrogen and forms a deposited film of TaN. The TaN material is more inert than Ta and does not react with Cu. In addition, TaN can be deposited as a polycrystalline film or an amorphous film by adjusting the nitrogen flow rate.

TaN films have been found to be better barrier diffusion-barrier films than Ta films. However, since TaN does not react with Cu, it exhibits worse adhesion behavior than Cu. For some Cu-CMP processes its adhesion properties are inadequate. To overcome the limitations that each film (i.e., Ta and TaN) exhibits when used alone, the implementation of bilayer films (TaN/Ta)[17] or trilayer films (Ta/TaN/Ta) have been investigated. These multilayer barrier-films reportedly offer better overall characteristics for Cu damascene interconnects.

TaSiN is another candidate for a Cu-barrier-layer material. It is formed by PVD of a TaSi target (with a low Si concentration) in an Ar/N_2 ambient. TaSiN is an amorphous refractory ternary material, and as such does not have any grain boundaries (which can serve as fast diffusion paths in polycrystalline films). It has been reported by Hara *et al.* that TaSiN exhibits better adhesion and barrier-layer characteristics than even TaN/Ta bilayers.[26,85] Furthermore, the same group reported that Cu-films deposited on TaSiN barrier-layers have a stronger (111) preferred orientation than do Cu films deposited on Ta or TaN layers.[27] A survey of over 75 papers from 1999-2000, indicated that TaSiN can maintain its diffusion-barrier properties for Cu to higher temperatures than Ta or TaN. However, since the Si containing ternary compounds (TaSiN and TiSiN) have higher resistivity, the Si industry tends to use TaN or Ta for Cu barrier-layers.[28]

16.3.7 Other Candidate Materials for Cu-Barrier Layers

Various other materials have been studied as Cu barrier-layers, and the most important of these (i.e., TiN, TiSiN, and WN) are discussed in this section. TiN is a good barrier-layer material for Al interconnects, and has been widely used for this application. While it also performs well as a barrier-layer for Cu, its behavior as an adhesion-layer and seed-layer for Cu is not as good as the Ta-based materials. CVD-TiN films have also been considered as Cu barrier-layer materials but they are reportedly less effective as diffusion barriers than PVD-deposited Ta and TaN films.[18,41] In addition, Cu films deposited on TiN have a weaker (111) structure than those deposited on Ta.[23] Hence, TiN deposited by either PVD or CVD has not been widely adopted for use in Cu interconnect metallurgy.[24] However, TiN deposited by ALD has been mentioned as a possible barrier-layer material for Cu. Work to deposit TiN by ALD has recently been reported.[29]

On the other hand, TiSiN-films deposited by CVD have been reported to exhibit significantly improved diffusion-barrier properties for Cu compared to TiN. The Si introduced into the TiN matrix bonds with the nitrogen (and this plays a role in producing improved barrier-layer behavior).[18] The TiSiN also has the additional benefit of good wetting to Cu, which has been correlated to improved Cu electromigration performance.[30] The CVD-TiSiN is deposited using TDMAT (tetrakis [dimethyl-amido] titanium) and silane as the precursors.[31,56] (Additional information CVD-TiN with TDMAT can also be found in Vol. 1, Chap. 6, Sect. 6.7.3.) The deposition of barrier-layers by CVD may become necessary for sub-0.1-μm technologies.

Tungsten nitride (WN) films deposited by CVD have also been considered as materials for Cu barrier-layers. Limited development of CVD-WN was described by Genus in 1999,[32] but they apparently decided not to commercialize this approach. Their decision may have been based on results indicating that such films are less effective than PVD-films of Ta or TaN as Cu diffusion-barriers.[18]

16.4 SEED-LAYER TECHNOLOGY FOR COPPER INTERCONNECTS

A *thin Cu seed-layer*, deposited by a method other than electroplating (e.g., PVD) must be deposited on top of the diffusion-barrier-layer.[9] This layer needs to be present to ensure that the subsequent Cu-electroplating operation can be performed successfully. Specifically, there are a number of requirements that the seed-layer must satisfy in order to enable the electroplating fill-process to be effectively carried out.[33] That is, if the seed-layer exhibits any one of a number of flaws, including poor morphology, inadequate sidewall- and bottom-coverage,

excessive overhang, or surface contamination, the electroplating results will be unsatisfactory (even if the best electroplating process is available). The details of the characteristics that must be possessed by the Cu-seed-layer are described as follows:

1. *Low-Resistivity* - At the start of the electroplating process, the seed-layer is the primary-conducting layer that carries current from the edge of the wafer to the center (allowing the plating current-source to contact the wafer only near the edge). Thus, the seed-layer should provide a low-resistance path from the edge to the center of the wafer, to make the current-density during the Cu-electroplating process uniform across the entire wafer (especially when the plating process is being initiated). Uniform-current density across the wafer-surface helps maintain a uniform plating-rate across the wafer.

2. *Film Continuity Along the Sidewalls and Bottom of the Trenches and Vias* - The electroplating process must also occur within the recessed features on the wafer surface. Since, the seed layer carries current from the top surface into the bottom of vias and trenches, the electrical path to the bottom of such features must be continuous and adequately thick. If there is insufficient seed-layer thickness at the bottom or sidewalls of the vias, this will lead to a slowdown in the plating-rate, which, in turn can cause a void during the Cu-fill process (Fig. 16-21a). To get adequate Cu-seed-

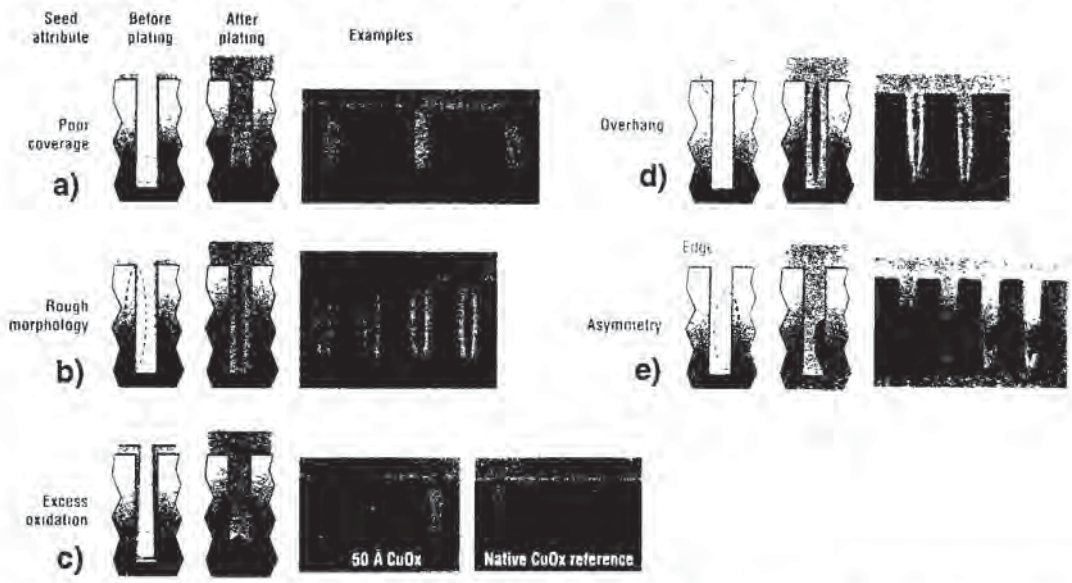


Fig. 16-21 Example set of illustrations and cross-sectional images showing key seed attributes and their impact on electroplating fill results.[33] Courtesy of Novellus Systems.

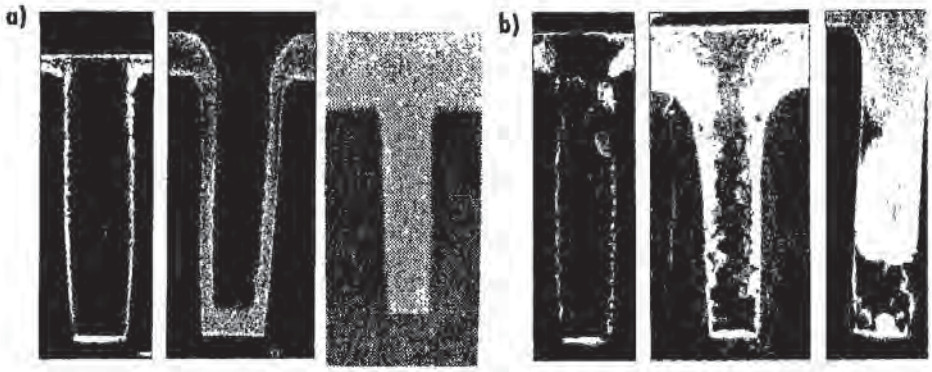


Fig. 16-22 Cross-sectional via images showing (left-to-right: a) Smooth seed coverage only, metal profile following partial fill, and complete fill by electroplating; b) Agglomerated seed coverage, metal profile following some electroplating, and resulting void at completion of electroplating.[33] Courtesy of Novellus Systems, Inc.

thickness along the sidewalls and bottom of deep-submicron, high aspect-ratio vias, either an ionized-PVD process or a CVD process is needed.

3. *Smooth Surface* - The seed layer must possess a smooth and continuous morphology. If the seed layer on the recess sidewalls is rough (or agglomerated) voids are also likely to form during plating. Rough sidewalls can lead to premature feature closure, and the discontinuity of an agglomerated film causes nucleation to fail at some locations. Either effect can give rise to creating a void (Fig. 16-21b). However, with a continuous, smooth seed-layer, plating readily occurs on all surfaces, thereby facilitating the subsequent as-desired, bottom-up filling (Fig. 16-22a).

It should be noted that the temperature of the wafer during the PVD process must be kept low to ensure that a smooth seed-layer surface is obtained (i.e., at room-temperature, or lower). Elevated wafer temperature during the seed-layer sputter-deposition process leads to a rough Cu surface (or even agglomeration, Fig. 16-23).

4. *Minimal Oxidation and Corrosion* – Oxidation and corrosion of the Cu seed-layer must be minimized both prior to plating and when the wafer is first immersed in the plating bath. Either effect can lead to seed-discontinuity and fill voiding. That is, the seed-surface must be largely free of oxide so that efficient charge-transfer can start to take place when the plating process is initiated. If the oxide on the PVD-Cu-surface is acid-soluble and sufficiently thin (i.e., in the thickness range of 10-20-Å), such initiation of the plating process is routine, and filling is complete.

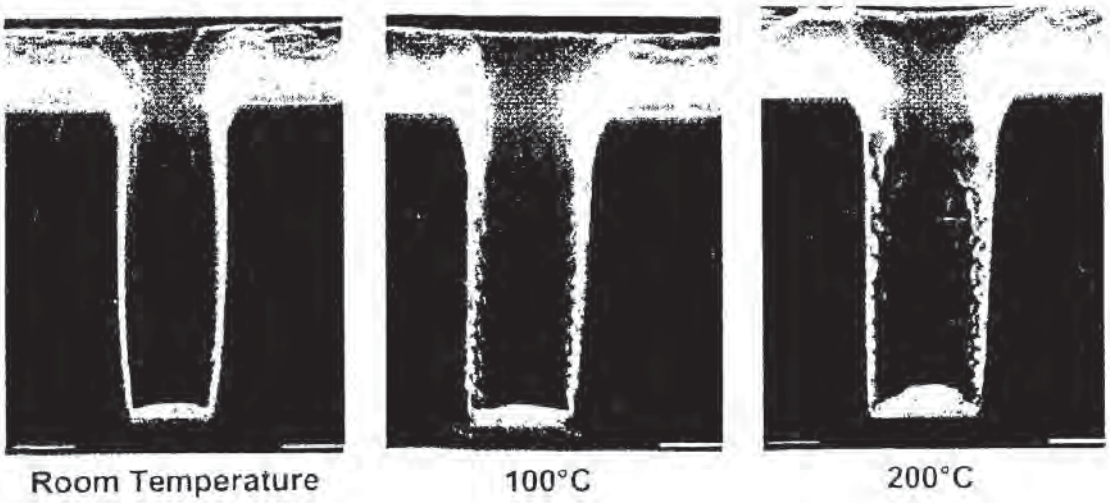


Fig. 16-23 Effect of wafer temperature on surface morphology of Cu deposited into vias by I-PVD. Courtesy of Applied Materials

However, when the cuprous oxides are thicker (i.e., 50-100-Å-thick), a greater degree of bottom voiding is observed (Fig. 16-21c).

5. *No Overhang at the Top Corners of Trenches and Vias* - Excessive overhang can lead to premature closure of the top of the recess during the plating process (Fig. 16-21d).

6. *No Asymmetry of Coverage Between Radially-Inward- and Radially-Outward-Facing Sidewalls* - Too thin a seed-layer on one side can impair nucleation and result in void-formation (Fig. 16-21e). That is, a much thinner seed-layer will form on that side than would be expected, and a void can thus result. This means that control of directional deposition during the PVD process must be maintained across the wafer plane from center-to-edge.

7. *Preferred Crystallographic Structure* – The crystallographic texture of the Cu seed-layer is influenced strongly by that of the underlying barrier-layer. This texture, in turn, determines the microstructure of the electroplated Cu deposited onto the seed layer. As noted previously, a (111)-orientation of the Cu is generally preferred because such films have the best overall film characteristics. A smooth Cu seed-layer-surface is also required to obtain this crystal orientation in the Cu layer that is subsequently deposited by electroplating.

In order to obtain a strong (111) Cu texture, it is also important that an *in situ* Cu-seed-layer deposition be performed. That is, the seed-layer

deposition process should be carried-out in the same cluster PVD-tool in which the barrier-layer PVD process is performed. This ensures that the surface of the barrier-layer (typically consisting of a reactive metal, such as Ta), does not form an oxide. If the barrier layer is exposed to air prior to Cu deposition, the resulting (111) Cu texture is much weaker than without an air break. This is probably attributable to oxidation of the barrier surface, and the resulting elimination of the pseudohexagonal surface that would otherwise allow for heteroepitaxial deposition.

Controlling the via shape itself is also important to ensure repeatable feature-filling. That is, the via-shape influences the filling by impacting the continuity of the seed-layer. Problems with the shapes of the vias often occur when trying to integrate an organic low-*k* ILD and Cu. That is, the via profiles of such materials frequently exhibit undercutting and notching as a result of the via-etch process (see Chap. 14). Such notches in the via sidewall profile can cause a discontinuity in the seed layer, and adversely impact the ability to completely fill the feature.

To get adequate seed-layer thickness into along the sidewalls and bottoms of high aspect-ratio recesses, either an ionized-PVD-Cu or a CVD-Cu process may be needed. (Ionized-PVD technology for such applications is discussed in Sect. 16.3, and additional information about seed-layer deposition with CVD is given in later paragraphs of this section.) As also noted in Sect. 16.3.2, the ionized-PVD process offers an additional advantage provided by the fact that a negative-bias can be applied to the wafer. This not only causes the ionized metal-atoms to preferentially strike the bottom of the via, but it allows the kinetic energy of these ions bombarding the wafer to be adjusted. For appropriate bias levels, this can cause re-sputtering from the feature base, which redistributes sputter-deposited material onto the lower sidewalls. The improvement in the conformality of the seed-layer thickness helps enhance filling of the recess without voids during plating. The impingement of the energetic ions on the top corners also helps keep the top opening from forming an overhang. Since the aspect-ratios of mid- and upper-level lines and vias is not likely to exceed 5:1, it is probable that ionized PVD techniques will continue to find use for these applications in future technology generations.

Unfortunately, as the feature sizes get smaller without a corresponding reduction in the ILD thickness, the aspect-ratio of the recesses gets larger. This is a situation that is likely to be encountered for the lower metal-levels of sub-0.1-μm interconnect structures. As noted in Sect. 16.3.1, for a PVD process the amount of material entering the recess must shared among all of the recess

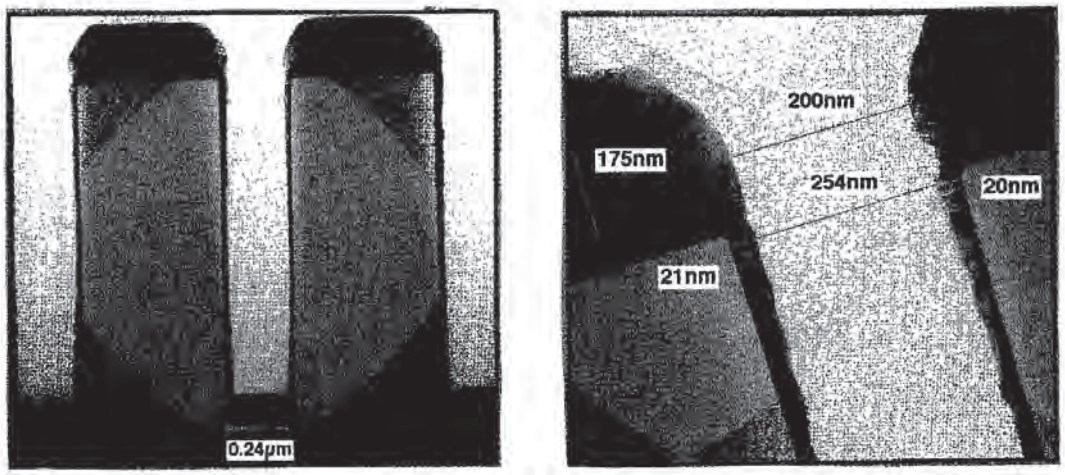


Fig. 16-24 SEM showing how thin the sidewall coverage is in high-aspect-ratio-features with I-PVD compared to the deposited layer thickness on the top surfaces of a wafer.

sidewall and bottom surface areas. For a via with an aspect-ratio of 5:1 the surface area of the sidewalls and bottom is 21x the surface area of the top opening. Thus, the material-thickness on all surfaces can only be 1/21 times as thick as the film deposited on the flat areas adjacent to the recess. Even at the 0.18-μm technology node, where the aspect ratio may be 5:1, a film-thickness of 2000-Å must be deposited in the flat regions to get a 200-Å-thick film on the via sidewalls (Fig. 16-24). Thus, at some time soon, it is predicted that PVD will no longer be capable of depositing an adequate seed-layer. Some have called the PVD-seed-layer the "weak-link" in the Cu-electroplating process.

At the point when the aspect-ratios for the lower levels of the interconnect system get to be too high to be adequately covered with any of the available PVD-processes (or if such a thick PVD-layer is needed that it causes too great an overhang), it may be necessary to switch to a CVD-Cu seed-layer. Some predict that this will occur for either the 100-nm or 70-nm CMOS nodes. Figure 16-25a shows a CVD Cu seed-layer on a CVD barrier layer deposited in a high-aspect-ratio recess that is only 0.14-μm wide. The CVD-Cu seed-layer is totally conformal and 500-Å-thick. The remaining 300-Å-wide slot was filled by electroplating without voids.[32] Figure 16-25b shows another example of a CVD-Cu seed-layer that is conformally deposited over high-aspect-ratio features.[34] One concern of using CVD-Cu seed-layers is the strength of their adhesion to the barrier-layer materials. Many freshly deposited barrier-layers (especially Ta-based), have highly reactive surfaces. These surfaces can degrade organic compounds resulting in interfacial contamination that prevents good adhesion.

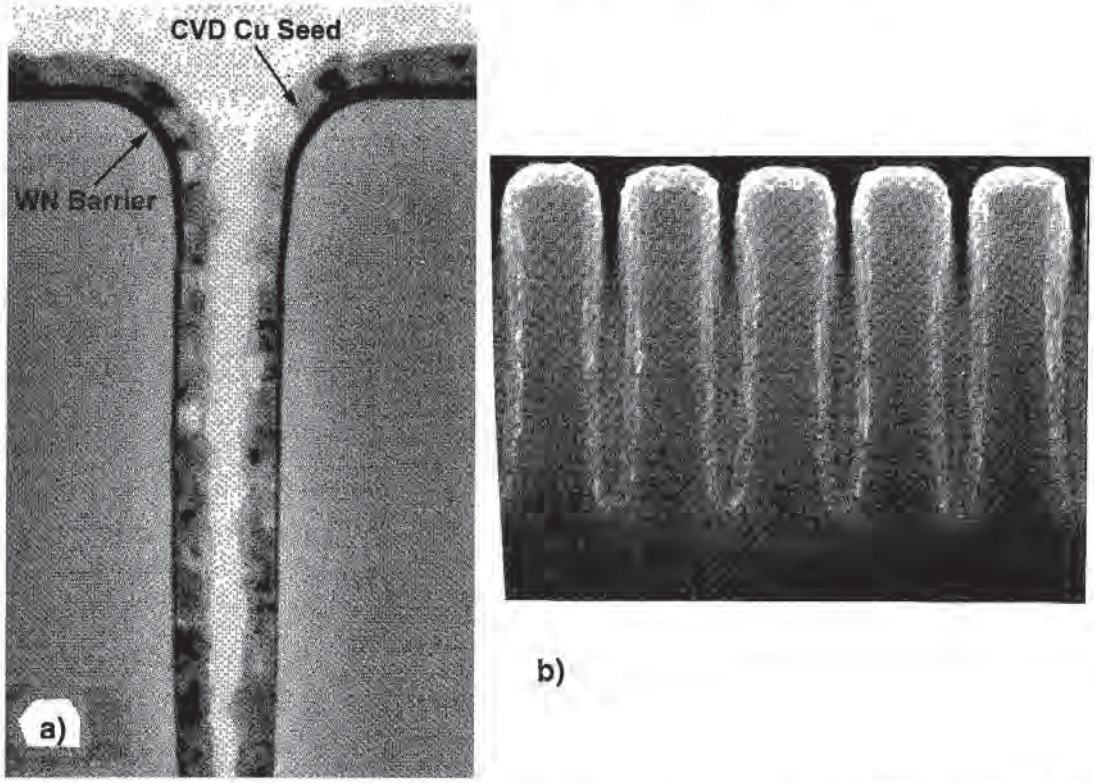


Fig. 16-25 a) SEM showing a CVD-Cu seed-layer integrated with clean and PECVD tungsten nitride (WN) barrier. (Courtesy Genus) b) SEM showing CVD-Cu seed-layer. (Courtesy Applied Materials)

This problem will need to be resolved by optimizing the barrier-layer choice, and improving the CVD deposition-process and precursor chemistry.

Two other alternative replacements for the PVD-Cu seed-layer have also been reported. The first is an electrochemical deposition process developed by Semitool. In their method, an ultra-thin Cu-layer (e.g., 200-Å-thick) is first deposited by PVD for adhesion purposes. This ultra-thin Cu-layer is then conformally thickened to provide a full-thickness seed-layer with an electrochemical process. Finally, the electrochemical process is switched over to a conventional electroplating chemistry to complete the feature fill.[35]

The other alternative replacement technology for PVD-Cu seed-layers is atomic-layer deposition (ALD - see Chap. 4, Sect. 4.6.1 for more background information on ALD).[36] ALD is a monolayer, stepwise growth-process that exploits the binding-energy-difference between chemisorption and physisorption. The growth proceeds by exposing the substrate-surface alternately to the precursors, and following each reaction, the excess species and by-products are removed with a nitrogen-pulse. The reactant-source pulses are thus separated by

a pulse of an inert gas. As a result, ALD is capable of depositing conformal-films with thicknesses that can be determined accurately by the number of deposition-cycles. The Cu precursor chosen for the work in Ref. 36 was $Cu(hfac)_2 \cdot XH_2O$ (see Sect. 16.5.3), and methanol, ethanol, and formalin were examined as the reducing agents. Smooth, conformal, near-bulk-resistivity Cu seed-layer films of 20-nm thickness with good adhesion were deposited by this ALD method.

As noted in Sect.16.3, another reported problem involving the PVD-seed-layer is its selective adhesion to barrier-layer materials. That is, the PVD-Cu seed-layers adhere well to Ta, but less well to TaN. Cu-films used with TaN barrier-layers can peel away during the later Cu-CMP process. Unfortunately Ta is not as good a diffusion barrier as TaN. To overcome this problem, use of a Ta/TaN bilayer has been reported.[37] Even better adhesion by the PVD Cu seed-layer was obtained by using a TaSiN barrier-layer.[26]

16.5 COPPER INTERCONNECT FILM DEPOSITION

Copper films for IC interconnect applications can be deposited in a number of ways, including: electrolytic-plating; electroless-plating; chemical-vapor-deposition (CVD); and physical-vapor deposition (PVD). Electrolytic-plating of Cu is the dominant technique used to fill recessed damascene features in deep-submicron ICs. Therefore, it is discussed in the greatest detail here (i.e., in Sect. 16.5.1). Electroless-plating of Cu and CVD-Cu are described more briefly in Sects. 16.8.2 and 16.5.3, respectively. PVD technology of Cu-films (used primarily to deposit Cu-seed-layers prior to the electrolytic-plating filling process), was covered in Sect. 16.4.

16.5.1 Electrolytic-Plating of Copper

As described in Chap. 15, dual-damascene processes have been developed for the multi-level Cu-interconnect structures of deep-submicron ICs. The damascene approach avoids the problems associated with having to etch Cu-films, but a challenge of a different sort arises from the need to fill the high-aspect-ratio damascene recesses without voids in the metal.

Line-of-sight PVD techniques are inadequate for filling such features because accumulation of deposits at the upper-corners of trenches closes-off the opening of the recess and this leads to void-formation. Chemical-vapor-deposition (CVD) has the potential for conformal coverage, but numerous chemical and hardware issues have hampered development of a manufacturable fill process for Cu. Thus, to the surprise of many in both the semiconductor and plating industries, electrolytic-plating has emerged as the deposition method of choice for

damascene-Cu interconnects (although advanced sputtering techniques are still needed for depositing thin barrier- and seed-layers, as described in Sects. 16.3 and 16.4) before the filling of the recesses with a Cu-plating process.

Electrolytic-plating (also often called *electroplating*) and *electroless-plating* of metals are older technologies still used in a variety of industries including hardware, auto, and electronics. In the electronics industry these processes have been (and still are) widely used in the printed-circuit-board (PCB) industry to plate copper layers on both sides of plastic boards for PCB interconnects. By the late 1990's, work was begun to develop electrolytic-plating processes for IC fabrication technologies (especially for depositing copper films for IC interconnect structures).

The key reasons why development of electroplating processes for on-chip metallization was pursued stemmed from the future requirements of IC interconnects. That is, it became clear that in deep-submicron ULSI technologies, low-temperature, low-cost, metal-deposition-processes compatible with thermally fragile low-*k* dielectrics would be needed. Electroplating of metals (especially Cu) represented a very attractive process for such applications. This is because deposition of Cu by metal-plating offers a high deposition-rate process (0.5-1.0-μm/min), which in turn permits high-throughput (50 wafers/hr), and thereby also a potentially much lower cost-of-ownership than PVD or CVD. In addition, such processes can be carried out at temperatures $\leq 40°C$, and a well-tuned electroplating-process can fill high-aspect-ratio structures without defects (i.e., trenches with aspect ratios of 5:1 can be completely filled). The details of electroplating copper-films for deep-submicron ICs are described here. As noted earlier, since electrolytic-electroplating requires a closed-conducting-path for continuous electric current, it is not possible to plate directly onto an insulator such as SiO_2. In this case, an electrically-conducting contact-layer must first be deposited (i.e., in Cu electroplating, a low-resistivity Cu seed-layer is deposited on the insulator).

Electroplating processes utilize conductive solutions containing ions of the metal to be deposited.[13,38] In the case of copper, the solution typically contains copper sulfate ($CuSO_4$ in the concentration range of 17.5-60g/L), sulfuric acid (H_2SO_4 in the concentration range of 45-325 g/L), and water. The $CuSO_4$ in this acidified solution breaks up into Cu^{2+} (cupric-ions) and SO_4^{2-} (sulfate-ions). The sulfuric acid added to the solution plays several roles: **a**) it dissolves any native copper-oxide on the copper seed-layer, so that the copper underneath is exposed, allowing the plating process to be reliably initiated across the entire wafer;* **b**) it

* Both CuO and Cu_2O (cuprous oxide) are unstable in a strongly acidic medium (pH < 3).

increases the conductivity of the electrolytic solution; and **c**) it improves the wetting capability of this solution. In commercial processes, proprietary organic additives are also added to the plating solution in order to improve the filling of recessed features by the deposited Cu film (as is described in more detail in Sect. 16.5.2.3). As with other types of deposition, the success of the process is measured by factors such as: deposition-rate, film-morphology, trench- and via-filling-capability, deposited-film-thickness-uniformity across-the-wafer and from wafer-to-wafer.** Plating chemistries were evolved from the plating bath formulations used in the PCB industry, and these were made to work for semiconductor applications.

In the Cu-electroplating-process for on-chip interconnects, wafers with a conductive top surface (which in this case is a PVD-Cu seed layer, as mentioned earlier) are immersed face-down in the electrolytic solution. The wafer-surface is also electrically connected to the negative-side of an external dc power-supply (by a conducting sealing-ring at the outer edge of the wafer, see Fig. 16-26a[50]), making it the *cathode* in this circuit. Electric-current is passed so that a chemical reaction occurs at the wafer surface which causes Cu plating to occur (with the cupric-ions that carry electric charge constituting the current in the electrolytic solution, see Fig. 16-26b). That is, as the positive cupric-ions arrive at the negative-biased-cathode they adsorb on its surface. They also acquire two electrons and are reduced to Cu metal (which plates out), with the reaction for Cu being:

$$Cu^{2+} + 2e^- \rightarrow Cu^0 \qquad \textbf{(16.6)}$$

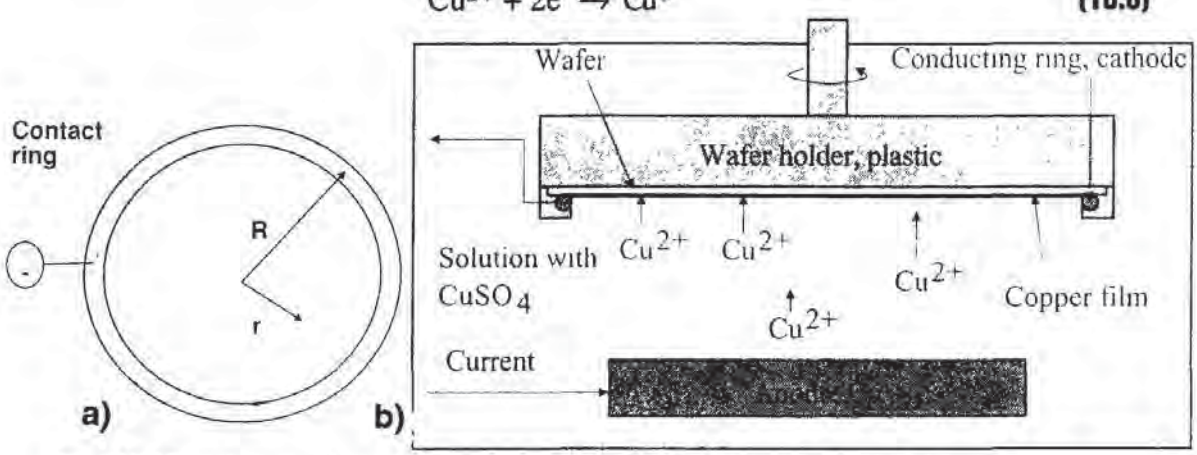


Fig. 16-26 a) Contact ring of a copper plating cell. b) Copper electroplating process.

** While the semiconductor industry has predominantly deposited Cu films electrochemically using acid baths, alkaline baths have also been considered. This is because alkaline baths can plate directly onto TiN diffusion barriers without a copper seed-layer and without the need for organic additives. On such bath studied by Semitool used an Cu-EDTA-complexed bath and the deposited Cu exhibited superior adhesion to TiN.[49]

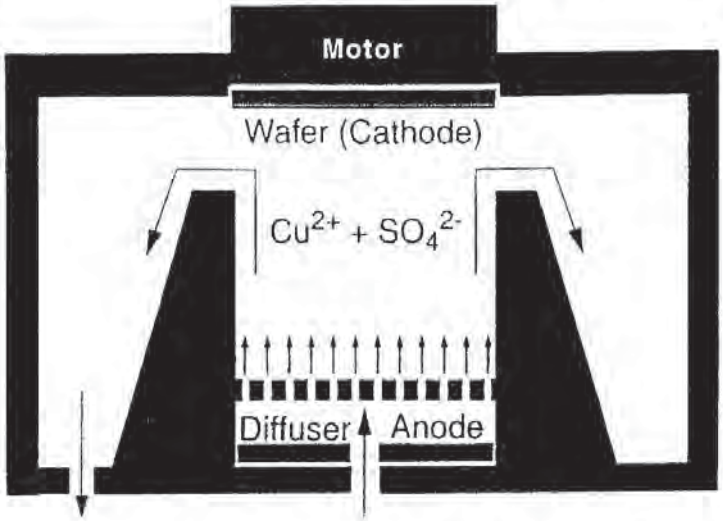


Fig. 16-27 a) Schematic drawing of a cross-section of a Cu electroplating cell.

Another electrically active surface (a solid-copper electrode which serves as the *anode*), is present in the conductive solution to complete the electric circuit (i.e., it is connected to the positive side of the power-supply). At the anode, the oxidation reaction occurs that balances the current flow at the cathode, thus maintaining the electrical neutrality in the solution. That is, all of the cupric-ions removed from solution by the plating of Cu onto the cathode are replaced by dissolution from a solid-copper anode immersed in the solution. (The copper atoms of the anode are oxidized to form the Cu^{2+} ions. These ions are released from the anode and dissolve into the solution.) The metal-ion formation-reaction is thus sustained by passing an electrical current through the bath.

If the applied potential is reversed, the cathode and anode are also reversed, and so are the locations where Cu deposition and dissolution occur. Alternating between deposition and dissolution (a process known as *pulse-plating*) may be useful in order to improve the filling capability of a plated film (see Sect. 16.5.2.5 for more details on pulse-plating). To enhance the uniformity of deposition across the wafer, the electrolyte is usually pumped against the wafer during the plating process, and the wafer may also be rotated at the same time (see Fig. 16-27).

The electroplating rate is a direct function of the current-density. To obtain uniform deposition across a wafer, the plating cell must be designed to give uniform potentials across the wafer surface. (Because of concerns about Cu contamination, it is also critical that the plating cell be designed so that no copper is deposited on the backside of the wafer.) The current delivered to a conductive surface is directly proportional to the quantity of metal deposited (according to

Faraday's Law of Electrolysis). By using this relationship, the mass deposited can be readily controlled through variations of plating current and time.

If no potential is applied across the interface between a metal and the electrolytic solution, an equilibrium potential exists between the two (see Fig. 16-28). Once the potential is shifted by an external power supply away from the equilibrium potential, a current will be driven across the interface. Under conditions typical of most plating processes, this current-flow is approximated by an exponential relationship known as the *Tafel equation*.

Figure 16-28 shows a current-vs.-potential curve of a copper electroplating process (also referred to as a *Tafel plot*). As the potential is increased from equilibrium to more negative values, the current increases in an exponential manner (Tafel region). In this region of operation the overall deposition-rate is determined largely by reaction-rate kinetics at the cathode. Ordinarily, conversion of Cu^{2+} ions to plated Cu-atoms occurs with nearly 100% efficiency, so that the electric current-density is a direct measure of the plating-rate. This also implies that ohmic effects (primarily through the uniformity of current distribution) are one of the important parameters that impact plating-thickness uniformity across a wafer. The strong dependence of current upon potential implies that the plating cells must be designed to enhance the uniformity of the potential across the wafer surface. The resistance of the barrier/seed-layer also impacts such ohmic effects, as will be described in later paragraphs.

As the potential continues to increase, mass-transfer effects become predominant and a limiting current-plateau is reached. This occurs because the Cu^{2+} species reacting at the cathode no longer reach the interface at a rate

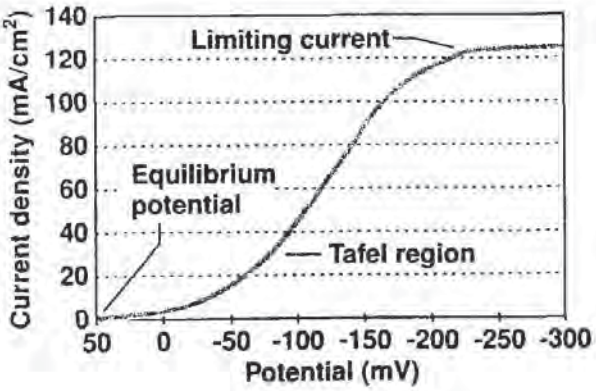


Fig. 16-28 A current-potential curve (Tafel plot) typical of a copper electroplating process.

sufficient to sustain the high reaction-rate. As a general guideline, Cu plating processes are operated at currents no greater than 30-50% of the limiting current to avoid undesirable film-deposition-characteristics.

To ensure that the rate of mass-transfer of Cu species to the interface is large compared to the reaction-rate (and that the mass-transfer rate is uniform across the wafer), the rates of migration, diffusion, and convection must be well understood and controlled. Convection is the most important mode of mass transfer in a liquid, and can vary from stagnant to laminar (or turbulent) flow. (See Vol. 1, p. 72 [Chap. 3] and p. 156 [Chap. 6] for a discussion of turbulent and laminar flow, and p. 157-8 [Chap. 6] for a discussion of mass-transfer in regions where movement by convection is zero [i.e., in stagnant regions].) In some electroplating systems, the wafer is also rotated while it is immersed in the electrolyte to get a uniform boundary-layer and to ensure that the fluid mechanics and material balance for the copper-diffusion match well everywhere on the wafer.

Generally, electroplating-processes have high deposition-rates (e.g., 400-1000 nm/min) and form desirable metallurgy. However, as noted in Sect. 16.4, electroplating requires a thin seed-layer of Cu (about 50-nm-thick) which must first be deposited by some other method (e.g., CVD or PVD) onto the barrier/adhesion-layer. As noted in Sect. 16.4, the characteristics of the seed-layer are another of the critical factors that impact the ability to completely-fill recesses by electroplating without voids or other defects. It would be ideal if a single layer could serve as both a barrier- and seed-layer, but currently two materials are used. An adhesion/barrier layer like Ta, TaN, Ta/TaN or TaSiN is first deposited, with a Cu seed-layer applied in a second step.

Note that to obtain uniform deposition across the entire wafer, the current-density should be equal at all locations. Since the conducting layer has some resistance, there will be a voltage-drop from the edge-to-center of the wafer. This means that the edges of the wafer will plate faster than the wafer center (and the deposition-rate non-uniformity is greatest at the initiation of the electroplating process). The problem also gets more severe as the wafer diameter is increased, and thus is worse for 300-mm- than for 200-mm-wafers. To minimize such deposition-rate non-uniformity-effects, the voltage-drop from edge-to-center must be kept tolerably small. Since the barrier-layer is very thin and typically has a relatively high resistivity, a Cu seed-layer must be formed on top of the barrier-layer to increase the conductivity to a sufficiently high degree. (It has also been reported that reverse pulse-plating [as discussed later], will help reduce the non-uniformity of deposition, as the copper also dissolves more rapidly during the part of reverse-plating cycle in places where it is most heavily plated.[25])

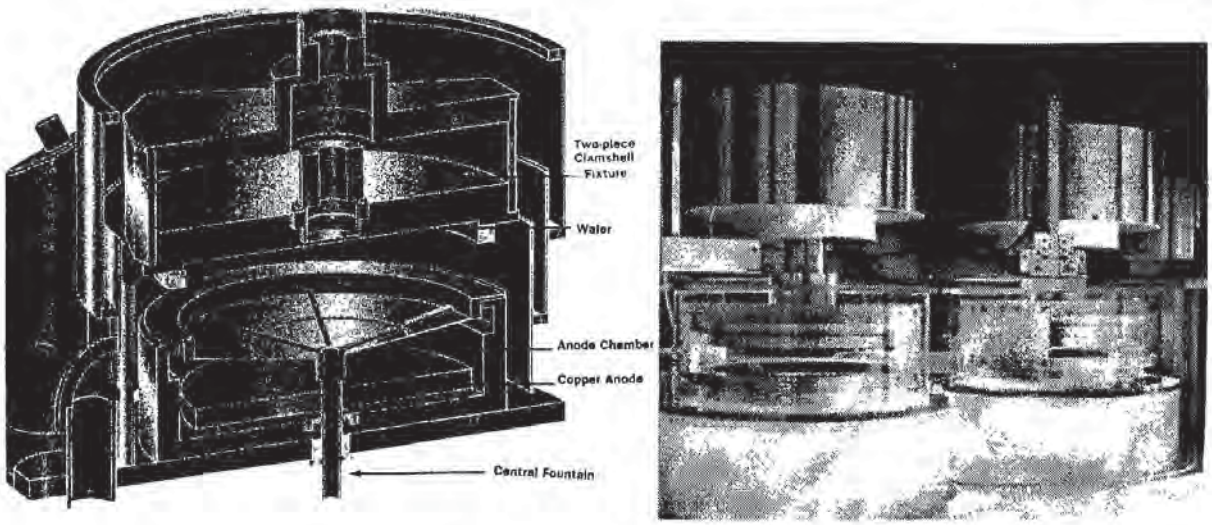


Fig. 16-29 Schematic drawings of plating cell of the Novellus SABRE™ electroplating tool. Courtesy of Novellus Systems.

Copper electroplating tools are commercially available from a number of companies. In 2000 the three companies with the largest market share were Novellus Systems, Semitool, and Applied Materials. The market for copper tools is expected to continue to grow significantly in the decade starting at 2001. Figure 16-29 shows illustrations of the Cu electroplating cell in the Novellus Systems SABRE™ elecroplating tool. Figure 16-30 is a drawing of the overall SABRE tool layout. This electrofill system enables void-free copper in extremely narrow high-aspect-ratio structures (up to 10:1) without backside contamination. Throughputs of up to 75 wafers are possible, with manufacturing availability above 90%.

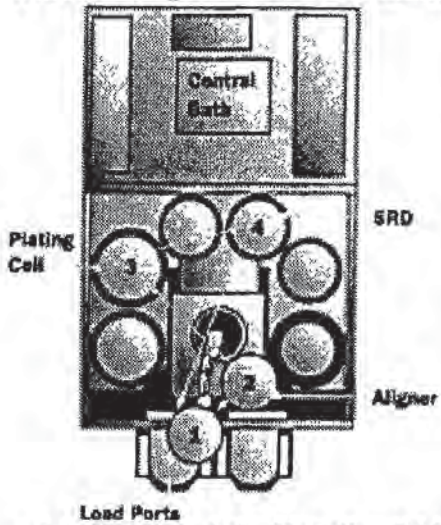


Fig. 16-30 Schematic drawing of the layout of the Novellus SABRE™ electroplating tool. Courtesy of Novellus Systems.

Figure 16-31 depicts the Applied Materials Electra™ Cu electroplating system. It has dual process cells and dual wafer handling blades for high throughput and reliability. Wafers are loaded into the twin plating cells. After plating they are processed in an edge-cleaning station followed by a spin-rinse-dry. The wafers are then moved to the integrated anneal chambers before being delivered back to the cassettes.

16.5.2 Filling High-Aspect-Ratio Recesses Without Voids Using a Cu Electrolytic Electroplating Process

The deposition process of Cu films for dual-damascene IC interconnects must not only have a high and uniform deposition-rate across the wafer, but it must also be capable of producing *void-free fill* of high-aspect-ratio damascene features. There a number of factors that impact the ability of the Cu electroplating process to fill such high-aspect-ratio recessed structures without the formation of voids or seams, including: **1**) the incoming feature profile; **2**) barrier-layer and seed-layer attributes; and **3**) key electroplating process parameters that are optimized to encourage acceleration of deposition near the base of damascene features ("bottom-up" fill). That is, for deep-submicron IC applications an accelerated plating rate is desired within submicron recessed features to achieve void-free fill. The attributes of the barrier- and seed-layers needed for permitting void-free fill were discussed in Sect. 16.3 and 16.4, respectively. The void-free filling factors involving the electroplating process are considered in the following subsections. They include: **1**) the electroplating solution must provide *rapid uniform wetting of the wafer surface*, especially within the area of high-aspect-ratio features; **2**) the deposition process must be *properly initiated*; **3**) appropriate

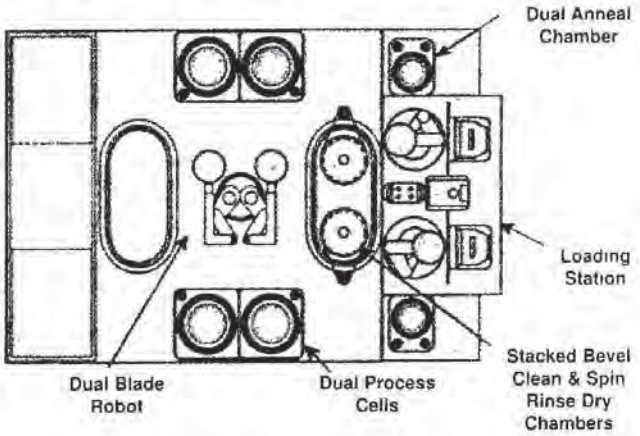


Fig. 16-31 Schematic drawing of the layout of the Applied Materials Electra™ Integrated ECP system. Courtesy of Applied Materials.

organic additives are added to the electroplating baths to facilitate void-free filling; and **4**) the *electric-current* waveform used for the deposition process can impact the filling characteristics. Topics **1**) and **2**) involving the electroplating process itself are described in Sect 16.5.2.1, while the effect of additives in the plating bath is covered in Sects. 16.5.2.2 and 16.5.2.3. The topic of plating-bath chemistry-management is discussed in Sect. 16.5.2.4 and the subject of pulsed plating in Sect. 16.5.2.5. The issue of topography in plated Cu-layers is addressed in Sect. 16.5.2.6.

16.5.2.1 The Electroplating Process Sequence: The electroplating process sequence typically consists of the following events. The wafers are immersed face down in the plating cell containing the electrolytic bath. Adequate surface wetting prior to initial deposition of the copper must occur. That is, rapid uniform wetting of the wafer surface and the inside of the high-aspect-ratio features is another critical requirement for good filling performance. For a solution with good wetting properties, capillary action should force solution into submicron features. Wetting is highly dependent on plating chemistry, seed-layer structure, composition, surface oxidation, and contaminants, as well as how the wafer is immersed into the plating bath and how the plating is initiated.[39]

The time the wafer is being wetted is referred to as the "zero-current-induction- time," or "induction-time" (see Fig. 16-32). During this time no external potential is applied, and thus no cathodic current flows. It represents the time period over which the wafer is exposed to the plating electrolyte at an uncontrolled (floating) potential. If the wafer is not polarized during this time, copper corrosion and cuprous oxide dissolution can occur.[40] To avoid the possibility of corrosion during the initial immersion period, the wafer may instead be introduced into the bath with an immediate small current flowing (or with a very-small cathodic potential being applied). In this way these corrosion reactions can be reduced or reversed. Immersing the wafers while applying a small cathodic potential is applied is thus referred to as *cathodic protection.*[33]

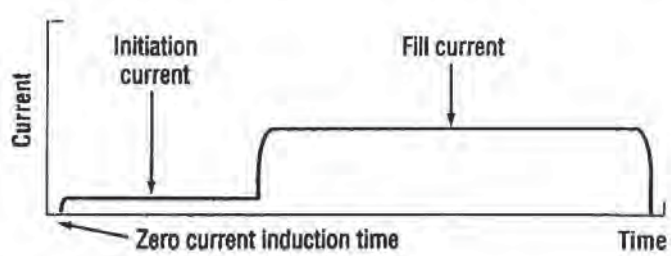


Fig. 16-32 Example of a two-step dc plating-waveform with three key features identified.[33]

After the induction time has passed, an "initiation current" is applied to the wafer (see again Fig. 16-32). During this time the current level is small, the deposition rate is slow, and the deposition occurs conformally. Thus, the seed-layer thickens uniformly during this period (allowing it to become continuous if a discontinuity in its coverage had occurred). In some cases, a thicker Cu seed-layer is needed to support the nucleation and high current density required in the subsequent fill step.

At the conclusion of the initiation-current stage, the "fill-step" stage is performed (Fig. 16-32). Since the damascene recesses are typically about 0.5-μm deep, and the Cu deposition-rate during the electrofilling stage of the plating process is ~1.0-μm/min, the fill-step lasts 20-40-sec, depending on bath conditions and feature size. Smaller features tend to fill earlier because they develop the conditions necessary for bottom-up fill (as will be described in the next sections). Since the larger features (i.e., with aspect-ratios much smaller than unity) fill more slowly, the copper layer must typically be deposited to a thickness somewhat greater than that of the damascene dielectric film stack. This issue will be considered in more detail later.

16.5.2.2 Additives in Plating Baths for Damascene Cu Interconnects: As noted earlier, the most important challenge for depositing Cu-films by plating for damascene applications is to completely fill vias, holes, trenches, and their combinations without voids or seams. For such defect-free filling, a higher deposition-rate along the sides and the bottom of the feature is needed than on the flat, top-wafer surface. As early as 1990 at IBM, it was discovered that plating from certain electrolytic solutions that contain additives leads to this kind of "bottom-up" filling. Since that time, work has continued to understand the role of such additives in plating solutions that will give the best filling results.

Additives to electroplating baths were originally developed to enhance the brightness and hardness of metallic deposits. Both of these attributes can be related to decreased grain-size in the deposits and reduction (or leveling) of the topography over rough surfaces. When the Cu-plating for submicron IC interconnects was being developed it was also observed that without additives the grain-size of the Cu was large (roughly 1-μm) and the film surface was rough. Additives led to a much finer grain-size (<1000-Å) and a smooth, highly reflective surface that had significantly less topography than the underlying substrate. From that work it was surmised that perhaps additional additives could be found that would also permit the damascene recesses to be filled without voids. It was discovered that a number of different additives (i.e., four or more)

need to be added to the plating solution to give the best filling results. (It also appears that the effects of these multiple additives are interactive.) Here such additives and their characteristics are described. In the next section a model is given for how these additives allow recesses to be filled from the "bottom-up."

The plating baths, as formulated by a number of specialty suppliers, include low concentrations (in the millimolar or micromolar range) of a variety of organic agents (generically referred to as *additives*) which serve to modify the properties of the deposited films as compared to results otherwise obtained from additive-free copper-sulfate/acid solutions. The manufacturing processes generally employ Cu plating-solutions purchased commercially, and the identity of the additives is proprietary. The examples of the various additives listed in this section come from the patent literature, as well as from various research articles that describe the additives being investigated. At the outset of the discussion the various classes of plating-bath additives are described. These classes include: suppressors, accelerators, and levelers (which, as will be noted, are also referred to by other names).

Accelerators are additives that speed or enhance deposition of the Cu during electroplating. Accelerators adsorb strongly on seed surfaces, where they also compete with suppressors for surface adsorption sites. Accelerators are usually unsaturated small organic molecules containing a polar sulfur, oxygen, or nitrogen functional group. In addition to increasing the Cu deposition-rate, they promote dense nucleation (and consequently the growth of films with fine grains). As a result, accelerators are also referred to as *brighteners* (i.e., because they cause the Cu-film to have a smooth, well-textured [i.e., bright] finish). Accelerators are added to plating baths in low concentration-levels (1-25 ppm). Examples of accelerators reported in the literature include: bis(3-sulfopropyl)disulfide (SPS);[41] sulfonated acetylthiourea;[42] 3-mercapto-1-propanesulfonate (MPSA);[33] and dibenzyl-dithio-carbammate.[43]

Suppressors (also called *inhibitors*, *carriers*, *surfactants or wetting-agents*) are plating-bath additives that reduce the Cu plating rate. Suppressors are usually present in the plating bath at higher concentrations (200-2000-ppm), so that their concentration at the interface is not strongly dependent on their rate of mass-transfer or diffusion to the wafer surface.

The suppressors are generally polymeric surfactants (with 1500 molecular-weight polyethylene glycol [PEG] reportedly being the most widely-used material for this purpose).[33] The suppressor molecules slow down the deposition-rate of Cu by adsorbing on the wafer surface, where they form a monolayer which offers a diffusion barrier to the cupric ions. In addition, they enhance the

cathodic polarization needed for fine-grain structure. In order for the polyethylene glycol to act as an effective suppressor, however, chlorine ions must also be added to the bath (in the form of HCl), and thus the chloride ion Cl^- can be considered a co-suppressor. In fact, HCl is the only non-organic additive in plating solutions.[33]

The role of chloride ions should be discussed in more detail. Chloride ions are believed to adsorb on the wafer surface, where they attract PEG molecules, and cause them to be more strongly adsorbed there as well. In fact, it has been observed that low chloride concentration leads to weak or negligible PEG adsorption.[44] This effect results in poor suppression of current at the wafer surface, and therefore the deposition on the wafer surface is not suppressed (which impairs the desirable condition of a differential deposition-rate between the top surface and inside the recesses that assists the complete filling of recesses). On the other hand, as the Cl^- concentration is allowed to increase to the appropriate level, good suppression of Cu deposition on the wafer surface is obtained. The levels of Cl^- within the recesses, however, might not be sufficiently high to maintain a high level of PEG adsorption, allowing accelerator molecules to be adsorbed on those surface instead. Thus, the conditions for good "bottom-up" filling are not disrupted. But too high a concentration of Cl^- concentration can interfere with "bottom-up" filling, because Cl^- can compete successfully with the accelerator molecules for surface sites in the recesses, and subsequently attract suppressing PEG molecules within the recess.

Levelers are plating-bath additives used to reduce surface roughness and to smooth the topography of the plated-film. They perform this role by locally reducing the Cu deposition-rate (i.e., by adsorbing on surface sites, blocking them from serving as locations where cupric ions can plate). Hence, levelers can also be considered as kin to suppressor additives. However, unlike suppressors, levelers are added to plating baths only in low concentrations (i.e., 1-25 ppm, comparable to the accelerator concentration). Hence, unlike suppressors, the concentration of levelers at the interface is mass-transport dependent and the large size of the leveler molecules also impedes their migration into trenches. In these ways, isolated locations (such as the insides of recesses, where mass-transport is limited) have fewer leveler species adsorbed on their surfaces. Thus, these regions experience less deposition-reduction effects caused by leveler adsorption than do the top, flat-surface regions of the wafer.

On the other hand, protruding-surfaces on wafer flat areas, or trench corners (to which mass-transport by diffusion or surface-migration is more efficient), experience a greater suppression of the deposition-rate. That is, the number of

leveler molecules adsorbed on wafer surfaces is continually being depleted during the plating process – by incorporation into the film or by electrolytic decomposition. The suppression of plating at protrusions on the wafer flat-areas and the upper corners of the trenches is maintained by constant replenishment of the leveler species that block surface sites (provided the leveler is present at the correct concentration). The suppression of the growth of protrusions on the wafer surface results in a more *level* film surface on the top-surface of the wafer (hence the name *leveler*). The suppression of deposition on the corners of the trenches allows the tops of the recesses to remain open while the "bottom-up" filling proceeds to completion. Examples of leveler additives listed in the literature are Janus Green B (JGB) a kind of dye,[45] and quatenary ammonium salt (QAS).[43]

For Cu-plating in dual-damascene applications, the composition and concentration of accelerators and suppressors are selected such that the accelerator surface-concentration dominates that of suppressors on the interior surfaces of trenches and vias. Local deposition-rates are thus suppressed on the flat surfaces on top of the wafer relative to the insides of recessed features, leading to the desired "bottom-up" deposition and void-free metal filling.

As a result, when these various additives are correctly balanced in the plating bath solution, it is possible to get a correct fill without voids and seeds. However, high precision is required to balance the roles of these materials. This topic is addressed in Sect. 16.5.2.4, where the issues of managing plating-bath chemistries are covered.

It should also be noted that in addition to void-free filling of recesses by Cu layers, it is also desirable to end up with a smooth (not rough) and topography-free (i.e., level) film after plating. This will allow a CMP process without an extensive overpolish time (i.e., that would be needed to get rid of the high spots that accompany rough and non-planar films) to be used. If an extensive overpolish time is required, this will lead to more severe dishing & erosion problems. Adding levelers to the plating bath and employing reverse-pulse plating waveforms are measures used to try and planarize Cu-layer topography.

16.5.2.3 Models of How Additives in Plating Baths Impact "Bottom-Up" Filling: A model that describes the effects of the plating-additives on the "bottom-up" filling of damascene recesses was published by Reid in 2000.[33] Reid's model is based on a large volume of experimental work, and it proposes that the mechanism for "bottom-up" fill is primarily due to the accumulation of *accelerator species* within damascene features. It supercedes a model by

Andricacos in 1998 that held that the "bottom-up" filling was driven primarily by the establishment of a gradient of *suppressor polymers* in the recesses.[46]

Before presenting the mechanisms that Reid proposes are responsible for "bottom-up" recess-filling, a few preliminary remarks are in order. First it has been observed by others that if the co-suppressors PEG and Cl^- are the only additives present in a plating bath, feature filling is poor. If PEG and Cl^- and an accelerator (e.g., SPS) are the additives present, better filling is seen to occur. If all three additive types (i.e., suppressor, accelerator and leveler) are present, the best filling results are obtained.[47] Furthermore, the concentrations in the bath must be correctly balanced to obtain the best filling effects. This implies that the effects of the three types of additive are interactive, as is also proposed in Reid's model.

Figure 16-33 shows the possible ways for a profile of plated copper to evolve during plating. In conformal plating, a deposit of equal thickness at all points of a

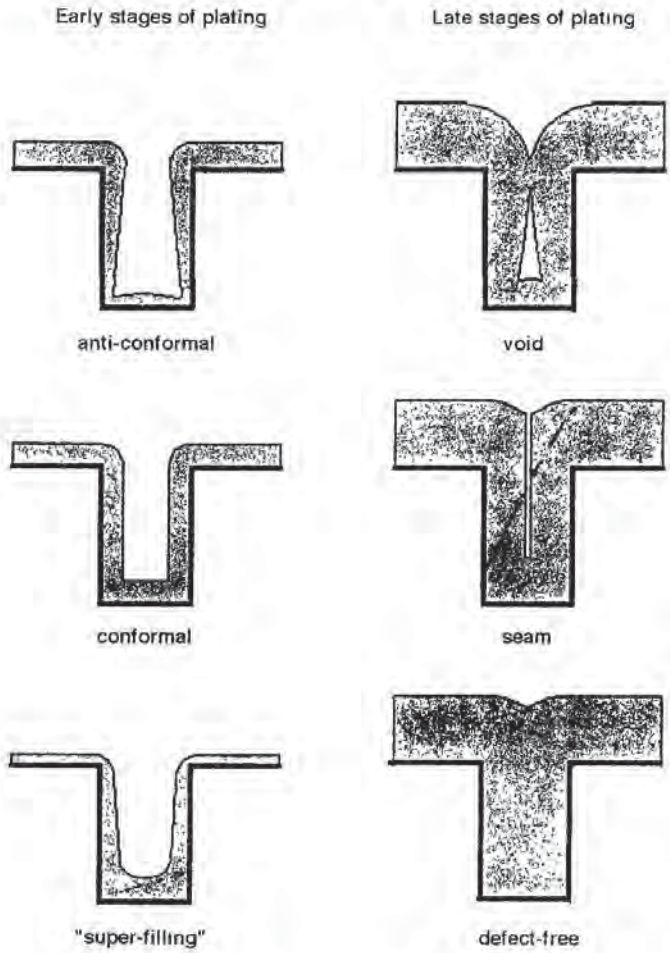


Fig. 16-33 Types of profile evolution in damascene plating.

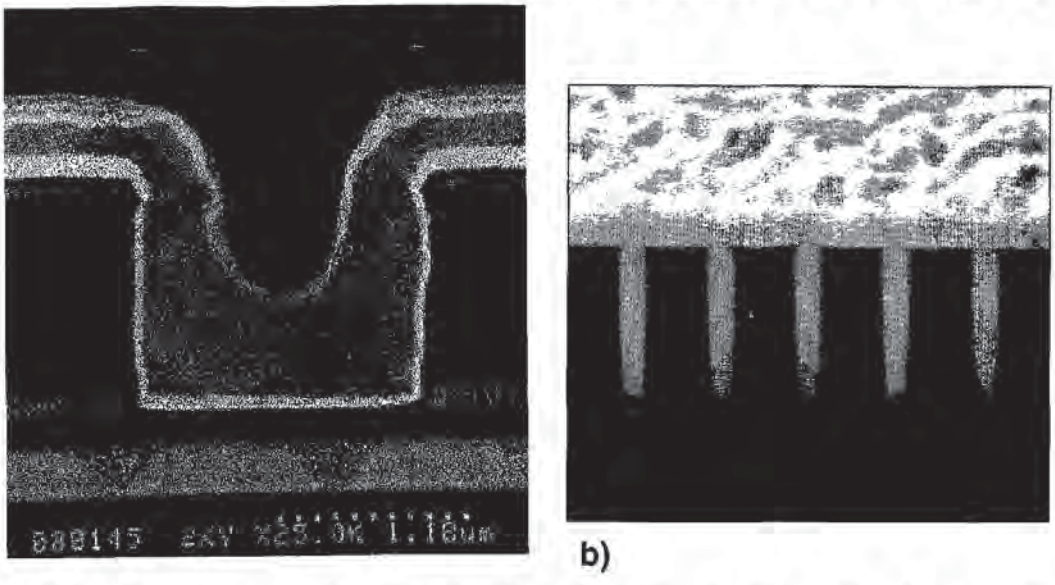


Fig. 16-34 a) Cross-section of a partially-filled line showing the profile of electroplated copper that exhibits the "bottom-up" filling phenomena.[48] b) Vias completely filled with Cu.

feature leads to the creation of a seam. If the shape of the feature is re-entrant, a void is formed. Subconformal plating also leads to void formation, even in straight-walled features. Subconformal plating occurs when substantial depletion of the cupric ions in the plating solution leads to significant concentration overpotentials, which in turn, cause the current to flow preferentially to more accessible locations outside of the feature. Thus, for defect-free filling, an increasing deposition-rate along the sides and bottom of the feature is desired ("bottom-up" filling). Fig. 16-34 shows a SEM of partially-filled line showing the profile of electroplated copper that exhibits such a "bottom-up" filling phenomenon.[48] Figure 16-35 shows SEMs of the time-evolution of filling a trench with a Cu-layer in a "bottom-up" manner.[49]

Seed 10sec 20sec 30sec 40sec

Fig. 16-35 SEMs of how "bottom-up" filling of Cu damascene recesses occurs versus time.[49]

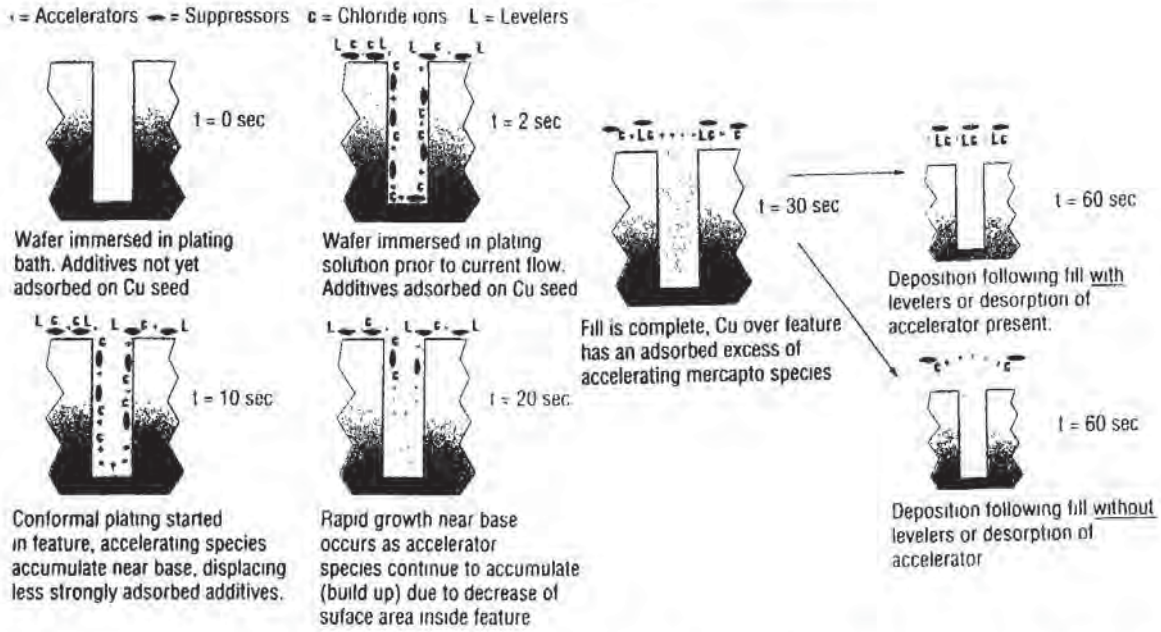


Fig. 16-36 Illustration of additive adsorption behavior during plating. A mechanism for the establishment and propagation of "bottom-up" fill is suggested. By permission of Solid State Technology. Published by PennWell.[33]

Reid's model of the sequence of events that accompanies "bottom-up" filling during Cu-plating is shown using Fig. 16-36. It begins by assuming that when a wafer is initially immersed in the plating bath (t = 0 in Fig. 16-36), that no additives are adsorbed on the Cu seed. However, within a few seconds (i.e., t = 2 sec in Fig. 16-36) both the suppressor and accelerator additives have been adsorbed on all areas of the wafer (including the insides of recesses) at their equilibrium levels. Thus, when the plating process is initiated by applying an external voltage to the cathode, the initial currents on all surfaces should be approximately equivalent on all surfaces. This leads to a deposition-rate that is constant everywhere. This perception is supported by the observed conformal deposition seen in the first 5-10 sec of a filling process (see also Fig. 16-35b - 10 sec). As was shown in Fig. 16-32, the plating current is kept low during this time (initiation current), to keep this conformal deposition thin.

After some time (which depends on current density, chemical concentrations, and feature size - e.g., t = 10 sec in Fig. 16-36), two phenomena are thought to begin to contribute to turn the fill process from a *conformal* filling-mode to a "*bottom-up*" filling-mode. First, the accelerator molecules start to accumulate at higher concentrations at locations near the bottom of narrow recesses. The increase in accelerator concentration near a recess bottom occurs because the surface area within the recess decreases as it fills (even if the fill is conformal),

and the accelerator molecules are neither incorporated in the depositing Cu nor are they desorbed into solution. (Recall from Sect. 16.5.2.2 that accelerator species adsorb strongly on seed-layer surfaces.) Meanwhile the PEG and Cl^- species are held less tightly on the seed-layer surface, and so they are displaced by the accelerator molecules and desorb into the solution. Thus, with a higher concentration of accelerator molecules in the areas of geometric concentration, the current-density (and the Cu-deposition-rate) is increased (t = 20 sec in Fig. 16-36).

The concentration of accelerator species in the solution must remain within an appropriate range. Too much accelerator in a bath disrupts fill because the accumulation of accelerating species also begins to take place on the top wafer surface between the recesses, and the differential deposition-rate with respect to the bottom of recesses is lost.

16.5.2.4 Electroplating Bath Control: Copper plating-baths are complex mixtures of chemicals, whose compositions contain various components that must be maintained at correct concentration levels. This is a challenging requirement because the composition of the bath changes as the plating process proceeds. The most dynamic ingredients of electroplating solutions are the organic additives. During normal electroplating the organic chemicals may be consumed in stoichiometric reactions (or they may break down in a variety of oxidative side reactions, some of which are non-stoichiometric). In any event, for consistent performance of the plating-bath, the original concentrations of these organics must be maintained, and their breakdown products must be removed. Even a small imbalance between components of the additives can cause defects in the filling of the trenches and/or degradation of the properties of the electroplated copper. As higher aspect-ratio-recesses are encountered, the ability to fill them properly will thus increase the importance of electrolyte management systems. (It should be noted that the bath solutions themselves are supplied by specialty-chemical vendors, such as Shipley Ronal.)

To enable the plating tools to be used in a high-volume production environment, the complex plating-bath chemistries have to be continuously monitored and controlled. Rigorous analysis of the plating bath chemistry has to be performed to determine how the bath composition changes with time as a consequence of plating, and then appropriate measures to counteract these changes must be taken. Such real-time analysis and feedback control of electrolyte are key to operating plating processes in a manufacturing mode. A self-adjusting, self-monitoring electrolyte is necessary to ensure precise control

of the plating chemistry to guarantee repeatable lot-to-lot fill. This has to be done on a large number of plating tools in a wafer fab that may be producing 20,000 wafers per month (with six or more levels of copper interconnect).

In some cases a separate, standalone, closed-loop analysis-and-dosing-system for multiple plating tools is used. In other cases the tool is designed with an on-board closed-loop electrolyte management system (e.g., as is done in the Applied Materials Electra ECP Deposition System™).[50] In the Electra tool, the bath management system measures (and then doses) the bath on-board at the system level, enabling precise control of suppressor, accelerator, leveler, copper, and acid concentrations. The system has a 200-liter tank with filtration on-board and six dosing channels. If the monitoring unit detects that, for example, suppressor x is under-concentrated, it immediately calculates how much is needed to dose the tank, and then does it. Feedback is on the order of minutes, rather than hours.

One method for monitoring the electroplating bath is a technique called *cyclic voltametric stripping* (CVS). The CVS principle has been widely used in the PCB industry, and was subsequently implemented for monitoring the electrolyte baths for IC Cu-plating. In the CVS method, a Cu film is deposited on an inert electrode and then this film is stripped by anodic dissolution. During stripping, the current is integrated over time to quantify the electric charge required for complete film dissolution. This charge is directly related to the molar quantity of the metal stripped (and thus to the amount initially deposited). From this information, calibration curves can be generated that provide reasonably accurate quantification of the total additive concentration in a plating bath. The stripping charge is monitored instead of the deposition charge because it is less sensitive to changing electrode surface states and impurity currents. Monitoring a process that proceeds to a well-defined endpoint also has inherent advantages.

The small plating cells used for plating Cu onto silicon wafers create very dynamic changes in chemical component activity, and this has generated a demand for a continuous, on-line, closed-loop analytical system. ECI Technology (Rutherford, N.J.) has developed such a CVS system for monitoring Cu-plating processes for silicon fabrication,[51] the Quali-Line QLC-5000.™ The CVS bath controller samples multiple plating tanks as well as a standard solution and then outputs the results.

The main limitation of CVS is its sensitivity to "matrix effects." Many bath components and their breakdown products display convoluted electrochemical interactions, so that the stripping-charge response is ambiguous if several components simultaneously change concentration. Thus, it is difficult to precisely correlate observed changes of electrochemical activity to variations in

individual bath components over extended times. These attributes make CVS less than ideal if the user's goal is individual monitoring of each bath component. However, under conditions where the principal requirement is to detect and correct changes in one or two electrochemically active components that have a rapid rate of consumption compared to others, the CVS method may be adequate for a closed-loop control system. In addition, CVS can provide rapid measurements with low-hardware investment, and little added waste-disposal burden.[52]

Another more elaborate plating-bath monitoring technology involves metal-free and ion liquid chromatography (also termed *high performance liquid chromatography* [HPLC] and *ion chromatography* [IC]). This method works on the principle of separating each of the individual components in the bath prior to detecting and quantifying them. It can provide information on the concentration and proportional balances of components in the plating solutions, as well as information on contaminants and degradation products.[53] A bath monitoring HPLC system for IC Cu-plating applications is being developed by Dionex Corp.[63] A short-coming of the chromatography methods include waste generation and the fact that the time required to perform the analyses can be long. It appears that a workable approach may be one in which both CVS and chromatography are integrated into a hierarchical method that exploits their relative strengths and minimizes their shortcomings.

When it has been determined that a plating bath needs to be adjusted (or replaced), several strategies can be employed. The simplest (and crudest) approach is to dump the bath when the plating results no longer meet the required specifications (and this is associated with a condition where the organic contaminant level exceeds a specified value). This technique is referred to as *batch dump,* or *bleed-and-dump-to-drain.* The level of contaminants in the bath is determined by correlating the Cu deposition tool throughput (and its related current-density) to the concentration of organic contaminants produced by breakdown of the organic additives. The increase in contaminant concentration is correlated to the amount of charge passed through the plating bath, and this relationship is expressed in units of *mg/amp-hr* (see Fig. 16-37). Thus, if this quantity is known (and the maximum acceptable contaminant-level is specified), the length time that a bath can be used before dumping is known. However, this method generates large quantities of waste that must be treated due to the copper and acid content. There is also no control (in either the general, or statistical sense), over the bath chemistry between dumps.

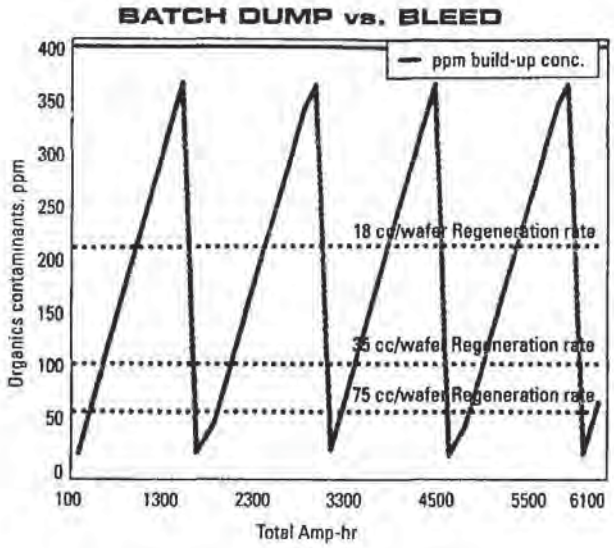


Fig. 16-37 "Batch dump" control versus "Bleed" control (0.3 amp-hr/wafer used to plate 1-μm thickness).[54] By permission of Solid State Technology. Published by PennWell.[33]

In a more refined technique, some fraction (typically about 10%) of the bath is removed daily, and it is replaced with new electrolyte solution. This is called the *bleed-and-feed* method. By analyzing a sample of the removed bath solution (e.g., with CVS), the concentration of additives in the new solution added to the bath can be adjusted to keep the total additive concentration within specified limits. However, as shown in Fig. 16-37, only a higher bleed-and-feed flow-rate can actively control the bath contaminant build-up that adversely impacts the bottom-up filling mechanisms. In addition, the bleed-and-feed method generates about the same amount of waste over time as the batch-dump method. Finally, while it does remove some of the contaminants that arise from breakdown of the organic additives, it does not completely remove them. It only dilutes them somewhat to a steady-state concentration. These drawbacks have led to a new approach to managing bath chemistry, referred to as a *remove-and-reconstitute* technique.

In this closed-loop method, the bath chemistry is continuously regenerated by stripping all organics (active and contaminant) from the recirculating bath. Then new organic additives (with the original concentration), are added back in. The bath solution is removed with flow-rates that are high enough to stabilize the concentration of contaminants at low levels. This flow rate is adjusted automatically, based on such inputs from the process tool as: amp-hours; wafer throughput; tool status, etc. The organic components are removed from the electrolyte by filtration, followed by their destruction using oxidizing agents

combined with heat and UV-light exposure. The organics are photochemically decomposed to carbon dioxide by exposure to the UV light - a clean process that involves no direct contact with the process fluid.

Process stabilization of both by-product and active organics are the benefits of this remove-and-reconstitute approach. The cost of consumables is also greatly reduced as only the organic additives are being removed (so only the organic additives need to be replaced). By using a closed-loop system, costly treatment of waste copper and acid is eliminated. A system in which this process is carried out is built by BOC Edwards. They call it the CuBIS™ (Copper Bath Integrated System), and it is shown in Fig. 16-38.[54] Its centralized monitoring system can simultaneously track five plating tools (from different equipment manufacturers).

16.5.2.5 Pulsed Plating: Utilizing pulsed-current waveforms (see Fig. 16-39b) during plating (instead of a dc-current) is a technique that complements the use of additives to obtain complete Cu filling of recessed features without voids. By periodically ceasing the current-flow, the plating reaction at the surface is halted in that time interval. The Cu filling process is improved for the following reason:

During electroplating a diffusion boundary layer is established between the bulk of the electrolyte solution and the wafer surface. In this boundary layer the Cu concentration trails off towards the wafer surface (since cupric ions are plated

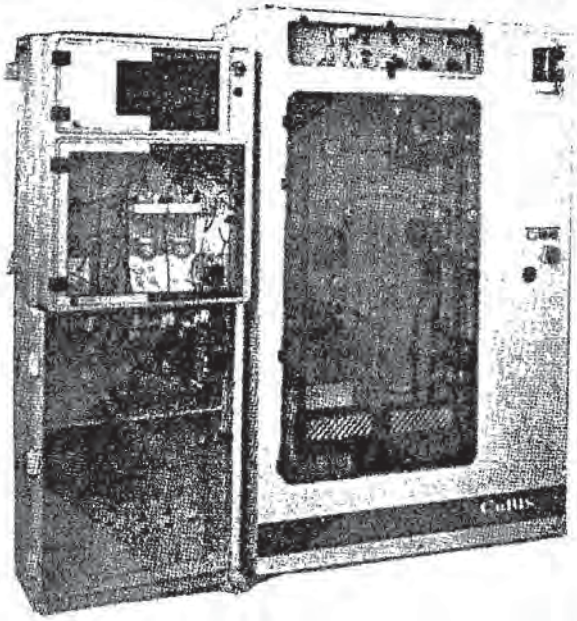


Fig. 16-38 Chemistry management is moving away from costly bleed-and-dump-to-drain approaches to bleed-and-feed. BOC's CuBIS Autorator uses a "remove-and-reconstitute" technique, which recycles the bleed stream, replenishing the bath at a rate automatically determined by plating conditions and by-product formantion. Courtesy of BOC Edwards.[54]

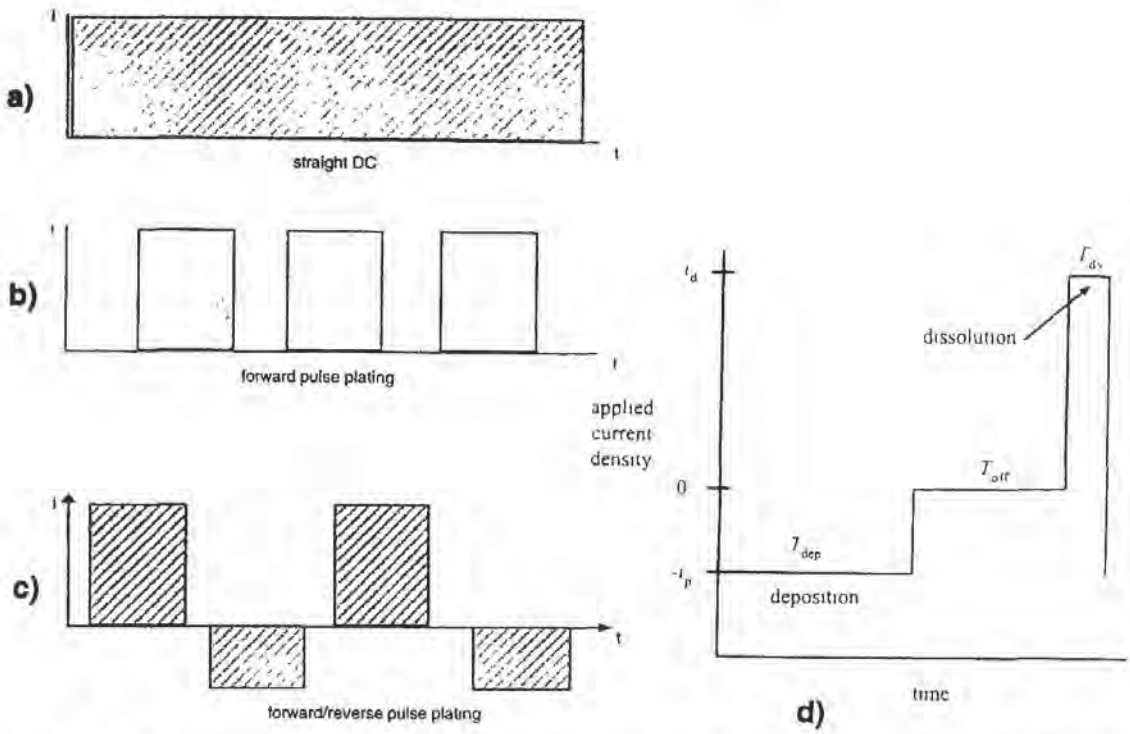


Fig. 16-39 a) dc current plating waveform; b) pulsed plating waveform; c) reversed-pulse-plating waveform; d) Example of reverse-pulse-plating waveform with optimized current amplitudes and pulse durations.[57]

out of the solution onto wafer surface). This boundary-layer is typically several microns thick. For a boundary-layer thickness that is larger than the pattern dimension, when the plating process reaches a steady-state condition, the copper-ion density is higher at the top-edges of trenches than at the bottom, Thus, for a dc-current-plating-process, a higher deposition rate is expected at the top of the trenches than at the bottom - and plating in this manner can lead to void formation.

However, by using pulsed-mode current, the concentration of cupric-ions depleted deep in the damascene recesses by the plating reaction can be restored to a higher level by Cu-ion diffusion to the bottom of the recess during such "rest-periods." This allows the deposition-rate at the bottom of the recess to equal the deposition-rate at the top when the current is restored during the next pulse of the waveform. This type of plating process is thus called *pulse-plating*. With an optimally shaped voltage pulse (both in amplitude and temporal shape), Cu filling of the recesses can be significantly improved.

Not only can the dc plating-current waveform be replaced with a pulse-waveform, but the polarity of the pulses can also be periodically reversed (Fig.

16-39c). The effect of reversing the polarity is to cause the Cu-film to undergo dissolution during the time polarity is reversed. Under the proper waveform conditions, the dissolution occurs more selectively at the top-corners of the trenches, thus allowing the trenches to remain open during the deposition-part of the plating waveform. Figure 16-39d shows an example of pulse-reverse waveform.[57] In one report, the application of periodic polarity reversal, together with adequately formulated and dosed surface-active additives allowed high aspect-ration via/trench filling capability. [58] One report observed that using small pulse periods gave better filling characteristics inside the trench. Using a small duty cycle and current density along with small pulse period appeared to give the best results.[59]

16.5.2.6 Copper Thickness Variation Within a Wafer After Electroplating: The copper topography across a wafer after the completion of a conventional electroplating process is not planar. Such within-wafer non-planarity is due to several effects. First, as discussed in Sect. 16.5.1, the higher current-density at the edge of the wafer next to the ring electrodes causes the Cu deposition-rate to be higher there than at the wafer-center. Thus, there is a buildup of copper thicker than at the center. One of the significant issues of achieving tight dishing and erosion specs after Cu-CMP is that these thicker Cu-regions require extra polishing time to get rid of them. This tends to increase dishing and erosion on other areas of the wafer.

Second, topography variations are caused by the feature-size-dependence of the filling process that is a characteristic of conventional electroplating. For example, the additives present in the electroplating baths used to enhance "bottom-up" filling of recesses with Cu can cause copper mounds to grow above regions containing dense arrays of narrow features (Fig. 16-40a). This occurs because the concentration of additives which accelerate the Cu-deposition rates in the recesses remain adsorbed on the top of the copper layer after the recesses

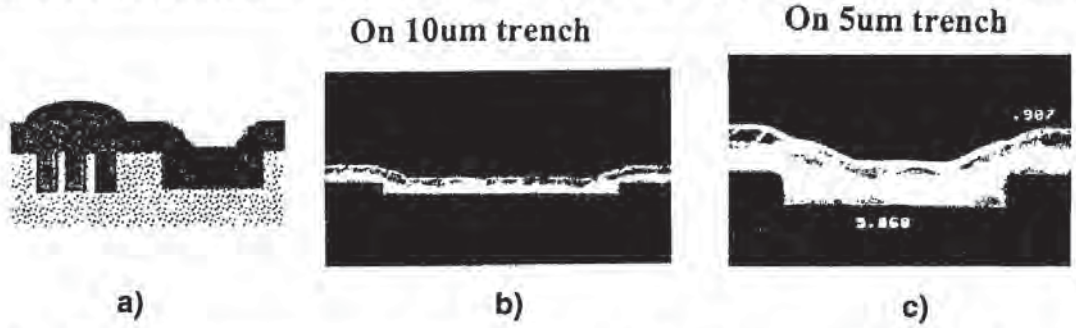


Fig. 16-40 a) Topography of a Cu-layer after plating into damascene recesses of varying widths; b) SEM of Cu plating into 10-μm-wide trench; c) into a 5-μm-wide trench.[61]

filling has been completed in those areas. This accelerates copper growth with respect to other areas of the wafer. If plating is done using electroltye solutions in which no additives are present to inhibit this effect, the copper layer over dense features can be twice as thick as the copper layer on wafer regions with no recesses. This reflects a continuation of copper growth beyond the time of filling completion, and the phenomenon is sometimes referred to as *overplating* (or *overburdening*, see also Fig. 16-36, t = 30 sec, and t = 60 sec).[60] The presence of mounds of excess copper in such regions again requires additional CMP over-polish. As a result, levelers are added to the plating bath (and reverse-pulsed waveforms are also used) to suppress the degree of such overburdening.

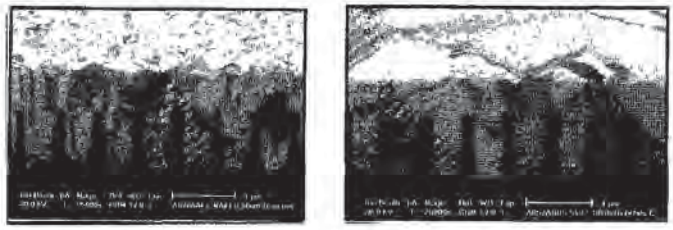
On the other hand, wide features do not fill as rapidly with Cu as narrow ones. Thus, there are steps in the copper layer at the edge of wide features. Figure 16-40a also shows such a step at the edge of a wide recess. Figures 16-40b and 16-40c show SEMs of Cu layers plated onto wide recesses, again showing the topography that results from a slower filling of wide recesses by plating relative that at which narrower recesses are filled.[61]

In summary, the topography that results from conventional electroplating processes exacerbates the problems of dishing and erosion that occur in a Cu-CMP process. Modifications to the plating process (such as those described in Sect. 16.5.4) have been proposed to alleviate this difficulty.

16.5.3 Post-Electroplating Cu Annealing and Recrystallization

When work began on copper-electroplating for IC interconnects, it was discovered that Cu-films are unstable after being deposited by electroplating, in that they self-anneal at room temperature (with the transient film-changes occurring over a period of hours to days). Furthermore, the transformation time is a strong function of film thickness. Thinner films take substantially longer to transform than do thicker films. In addition, the Cu seed-layer thickness also appears to play a role in the time and the degree to which annealing reduces the resistivity of the plated Cu-films. Greater resistivity reductions were observed as the plated films self-annealed on thinner Cu seed-layers than on thicker ones.[62]

In any case, if these variables are not controlled, each plated wafer headed for CMP may be different, depending on how much time has elapsed before it reaches the CMP step (a period that can vary depending on load size or tool selection). This can lead to wide distribution in electromigration behavior due to grain-size differences. To prevent such lack of control in plated-Cu-film characteristics, a post-ECP anneal at an elevated temperature was instituted. Such



a) No Anneal b) Integrated Anneal

Fig. 16-41 Comparison of grain size in damascene trenches: a) without; and b) with anneal.

post-plating anneals have since become a standard part of the Cu-deposition sequence.

The annealing process causes several changes in the properties of the as-plated Cu-films. First, grain-growth and strong (111)-texture is observed after 400°C annealing (Fig. 16-41). The as-plated grain-size of 1000 Å increases to several microns.[77] The increase in grain-size is significant because the film resistivity is also a strong function of grain-size. (Thin films with larger grains generally have a smaller resistivity than do those with smaller grains. This is because in films with large grains there are fewer grain boundaries – which cause carrier scattering, and thus degrade conductivity.) Thus, annealing of plated-Cu films also reduces their resistivity by up to 20%.[50]

Furthermore, annealing before CMP stabilizes both the Cu-grains and the Cu film-density (i.e., they no longer undergo changes with time at room-temperature). The result of such stabilization is not only a more controllable (and repeatable) Cu-CMP polishing-rate, but this rate also tends to be somewhat higher (by about 20-30%).[64] However, the temperature and time-duration of the annealing process can have an impact on the reliability of the Cu lines, and this must be considered when specifying the annealing conditions (as is discussed in more detail in Sect. 16.8.2).

To avoid having to raise the temperature of the Cu annealing process beyond the point where it makes no further improvements, studies of changes in the sheet resistance versus anneal-temperature and time were conducted. In one study it was found that a temperature of 200°C for 30 seconds would adequately reduce the resistivity and improve the Cu CMP removal-rate (Fig. 16-42). Thus, by designing a resistively-heated-pedestal-based annealing chamber within an electroplating tool enclosure, an annealing process can be integrated into the plating system. A chill-plate is also used in this arrangement to quickly cool the wafer to 50°C after annealing before exposing it to atmosphere (to keep the hot copper from oxidizing, as it would do if it were allowed to cool in air). The wafer

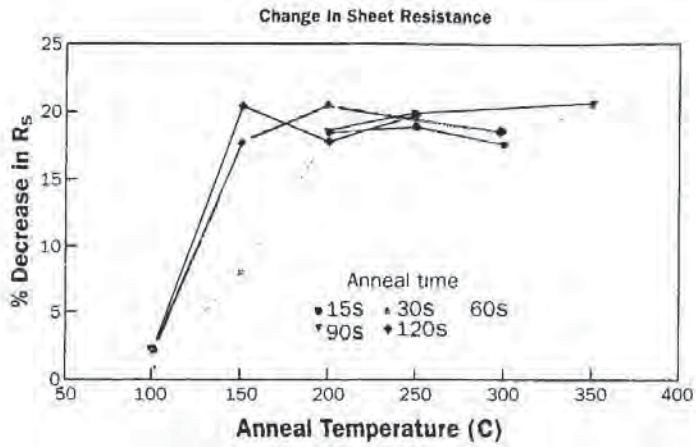


Fig. 16-42 Sheet resistance of Cu film as a function of anneal time and temperature after electroplating.[50]

is actually moved close to the chill plate (i.e., proximity cooling is used). To prevent the copper film from oxidizing during annealing, the ambient in the annealing chamber is maintained with < 5-ppm oxygen.

The Cu self-annealing effect can be explained as a recrystallization and purification process.[65] That is, an as-deposited plated-Cu-film is highly defective and the resistivity of the as-deposited film is high. The defects in the film are likely to be impurity inclusions caused by additives in the baths. (The large-grained deposits from additive-free baths do not undergo this recrystallization.) The inclusion of impurities at grain boundaries from the additives or their electrolyte by-products would be expected to cause pinning that would suppress grain growth. The as-deposited electroplated Cu film is not stable because of this high defect density. The film tends to reduce the defect level by recrystallization. During recrystallization, new grains are formed with fewer defects. These grains grow larger by consuming defective grains, leaving defects mainly in the grain boundaries and film interfaces. The stress in electroplated copper also changes from compressive-stress to tensile-stress after self-annealing. This is the macro evidence of film contraction caused by defect reduction.

16.5.4 ElectroChemical Mechanical Deposition (ECMD™)

As noted in Sect. 16.5.2.2, the Cu electroplating deposition-rate within recessed regions of a wafer exhibits a feature-size-dependence. That is, the Cu-deposition-rate is higher on areas of the wafer where there is a high-density of narrow, recessed damascene-features (and the plating process continues beyond the point

where the recess is filled). This results in mounding of the copper to a local thickness above those regions that is greater than in the flat regions devoid of recessed features (overburdening). In wide recessed-features, the deposition-rate is close to that on the flat-areas devoid of features, and hence a downward step can occur in the copper film when going from a flat area adjacent to a wide-recessed area. This has several detrimental consequences, especially with respect to the CMP process. That is, the thickness of the plated film must be increased to ensure that the wide recesses are completely filled. Thus, the process time of the CMP to polish the thicker Cu-film and the overburdened areas must be longer (which reduces the CMP throughput). There is also apt to be more Cu dishing in the wider-recessed areas. This problem would be overcome if the Cu could be deposited so that its surface after plating was globally planar. While techniques such as the use of leveler additives and pulsed plating can reportedly reduce the non-planarity to some degree, further improvement in the global planarity is still being pursued.

A novel process and deposition tool has been introduced by NuTool Inc. which seeks to address this issue directly. That is, in a process they call *electrochemical mechanical deposition* (ECMD™), as a copper layer is deposited in their tool (NuTool 2000™), a polishing pad is in physical contact with the wafer. This mechanical polishing coupled with the NuTool process chemistry simultaneously deposits copper and removes it. A differential growth rate between Cu deposition on the wafer flat areas and Cu deposition in the features is obtained. The speed, pressure, and mechanical path of the pad can all be controlled with software, eliminating the common problems of polishing copper, such as dishing and erosion.[66]

The ECMD process solves the problem of *excess-overburdening* (i.e., the buildup of excess copper over small densely arrayed features) and the downward steps that occur at the edges of wide recessed-features, by providing *aspect-ratio-independent filling* of features. Because the copper surface is not only globally planar but it is thinner in the field area than in a conventional Cu electroplating deposition process, the ECMD technique permits the CMP polish time to be reduced.

The tool and process were introduced in 2000, and thus information about its use in production is not available at the time of this book's publication. Some observers have commented that the ECMD process combines electroplating with some form of CMP on the wafer. Whether this combination of phenomena can be made to work simultaneously in a manufacturing environment will have to be demonstrated.

16.5.5 Electroless-Plating of Copper

Copper films can also be deposited by an electroless plating process, and this technology is already used in electronic packaging. Some work has also been done to develop Cu electroless plating processes for IC interconnect films. However, while this method has not gained the acceptance of electrolytic electroplating for forming Cu films, it is also briefly described here.

An *electroless* process involves the formation of a thin-film from an electrolytic solution without externally applied voltage. The deposition is due to an electrochemical reaction among the metal ions, reducing-agent, complexing-agents, and pH-adjusters on catalytic surfaces. The chemical process involves a CuO_4 and formaldehyde reduction:[67]

$$Cu^{2+} + 2HCHO + 4OH^- \rightarrow Cu^0(\text{solid}) + 2H_2O(\textit{liquid}) + H_2(\textit{gas}) \qquad \textbf{(16.7)}$$

An electroless Cu plating process for ICs was described in 1993 to give films with resistivities of 1.9 $\mu\Omega$-cm, close to that of bulk-Cu (1.7 $\mu\Omega$-cm).[68] Later work demonstrated filling of vias with aspect ratios of greater than 4:1 onto diffusion-barrier films of TiN.[69]

Although potentially a low-cost process because of its batch nature, electroless plating lost ground to electrolytic plating because of concerns due to hydrogen evolution, complexity of process control, low deposition rates, and potentially adverse environmental impact. However, it is possible that electroless plating will offer significant advantages for future wiring structures with improvements in sophistication and understanding. For example, some think that electroless plating may be used to deposit the Cu seed-layer at the 0.7-μm technology node.

16.5.6 CVD of Copper

While electroplating is the dominant method used to deposit Cu films for IC interconnects, work has been done on CVD-Cu deposition methods as well. One reason why interest remains in Cu-CVD processes is that it becomes increasingly difficult to deposit a uniform, conformal Cu seed-layer in the vias and trenches as their aspect-ratio continues to increase. At some point, it may not be possible to deposit a Cu-PVD-layer with sufficient thickness and/or continuity into such narrow features. A more conformal CVD-process could potentially produce a better Cu seed-layer in such high-aspect-ratio features. Thus, CVD-Cu technology approaches are briefly described here. (It should be noted however, that a copper PVD-process which deposits a very-thin nucleation layer will still be still needed before the Cu-CVD process.)

Organo-metallic sources are the most widely used precursors of CVD copper. These include Copper(II) {bis-hexa-fluoro-acetyl-acetonate copper} [$Cu^{II}(hfac)_2$] and Copper(I) {hexa-fluoro-acetyl-acetonatoL copper} or [$Cu^{I}(hfac)L$], where L is a neutral ligand weakly bonded to the Cu. One such ligand that has been used is vinyl-tri-methyl-silane (or *vtms*). $Cu^{II}(hfac)_2$ is a solid at room temperatures and must be dissolved in isopropyl alcohol in order to form a liquid precursor that can be delivered as a vapor (with hydrogen used as the carrier-gas). High quality Cu-films with low resistivity can be formed by the hydrogen reduction of $Cu^{II}(hfac)_2$. However, to get the lowest-resistivity Cu-films, the deposition temperature must be between 350–450°C. Since Cu is likely to be used with thermally-fragile low-*k* dielectrics, such high deposition-temperatures are undesirable. A low-pressure plasma process has reportedly been developed which allows the deposition temperature to be reduced to about 170°C, and which produces films with resistivities of 2.2 $\mu\Omega$-cm.

The $Cu^{I}(hfac)L$ precursor (where the L = vtms) is commercially available as a product called Cupra Select,™ developed by Schumacher.[70] It is a liquid at room temperature and is fed into the process chamber by direct-liquid-injection (i.e., the liquid is pumped to a vaporizer and then injected). This delivery method is needed for such precursors as $Cu^{I}(hfac)$-vtms, which decompose after long periods of heating in a bubbler. Low-resistivity Cu films can be formed at deposition temperatures of 150°C. The Cu is then deposited through a disproportionation mechanism:

$$2Cu^{I}(hfac)\text{-vtms}\ (gas) \rightarrow Cu^{0}(solid) + Cu^{II}(hfac)_2\ (gas) + 2\text{vtms}\ (gas) \qquad \textbf{(16.8)}$$

Both the $Cu^{II}(hfac)_2$ and the vtms ligand are stable compounds and readily desorb from the surface at the deposition temperature, leaving behind a Cu film relatively free of residues. Since the reaction is reversible, vtms can be used to dry clean the deposition chamber. By removing the Cu deposited on the parts inside the chamber, particle contamination by the film's cracking and flaking can be prevented. However, an issue that must also be addressed with CVD-Cu is wafer-backside Cu-deposition.

16.6 WET-ETCHING AND ELECTROPOLISHING OF CU FILMS

Work has also been carried out to develop processes that would replace (or shorten the process time) of Cu-CMP. Two basic approaches have been pursued: **1**) chemical *spin-etch planarization* (SEP) - in which the Cu film is etched with wet-chemicals using a special spin-processing tool; and **2**) electrochemically removing the Cu film with a process called *electropolishing*.

16.6.1 Spin-Etch Planarization of Cu Films

A SEP process was jointly developed by SEZ and Honeywell.[71] The SEP process removes layers of Cu material at a controlled rate by exposure to a reactive chemical solution while the substrate is spinning. Its goal is to remove the copper overfill material after a plating process with the same planarization results as CMP (but with no risk of damage to the low-*k* materials in the structure), and at much lower cost than CMP. Damage to the low-*k* is avoided and low-erosion of the dielectric is also achieved because there is no mechanical downforce as occurs in CMP.

During SEP the wafer is suspended horizontally on a nitrogen cushion above a rotating chuck (utilizing the Bernoulli principle). The substrate is held in place laterally with locating pins about the wafer perimeter. As the chuck and wafers are spun, wet-etchants are dispensed onto the wafer from a radially oscillating nozzle. An appropriate etching solution and spinning of the wafer result in a planar final surface (with the simultaneous radial and tangential etchant flow greatly enhancing planarization over simpler static etch processes).[72] DI water and nitrogen are then applied to the wafer to achieve rapid cleaning and drying. Etch rates of copper layers can range from 500-2000-nm/min, depending on the chemistry selected, and almost infinite selectivity exists with respect to etching of the underlying Ta and TaN barrier-layers.

By 2000, SEP was still in an early stage of development. However, it was demonstrated that the SEP process could provide a high degree of planarization for small features (0.35-0.5-μm-wide), and work was proceeding to improve the planarization of larger features in the 5-100-μm range. One way that SEP may become more practical is if a short CMP process (with a small downforce) could be used to knock off the large mounds of excess overburden present on parts of the wafer where high densities of narrow features are present. This would make the surface substantially more planar, making the SEP process more effective.

16.6.2 Electropolishing of Cu Films

Electropolishing of the overfill material after Cu electroplating is another process that has been pursued to eliminate or shorten the Cu CMP process. That is, after the electroplating step is completed, the current flow can be reversed, and the Cu film will then de-plate. The idea is to use such de-plating to remove the Cu overburden while leaving the Cu in the damascene recesses. Since reverse electroplating will remove Cu uniformly across the wafer, at first glance the concept appears feasible. However, it proves not to be practical as long as the

problem of aspect-ratio-dependent filling-effects occur during the initial electroplating process (see Sect. 16.5.2.6). That is, the non-uniform topography of conventional electroplating processes will result in overpolishing in the wide trench-regions and under-polishing in the circuit regions where there are dense-arrays of small-features. However, with the advent of a globally-planar Cu-deposition-process such as described in Sect. 16.5.4, electropolishing is once again being investigated.

In 2001 a Cu-electropolishing process was described in which the Cu-CMP step was either eliminated or significantly shortened.[61] A globally-planarized Cu-film was then deposited (such as was described in Sect. 16.5.4). With a globally planarized Cu film, the electropolishing can remove copper across the wafer without thinning the metal in wide trenches. In the Cu-CMP-free process that was described in Ref. 61, the Cu-overburden was electroplolished down to the barrier-layer. The barrier-layer was then removed by dry-etching with a fluorine-based plasma (that does not etch the exposed Cu remaining in the trenches). The wafer was then cleaned with brush scrubbing (Fig. 16-43). In the CMP-less process, the Cu-overburden was partially-removed by electropolishing and the remainder by conventional CMP. Less dishing could be achieved with the CMP-less process. A smooth Cu surface and highly (111) texture was also obtained by selecting the proper current density during the electropolish step.

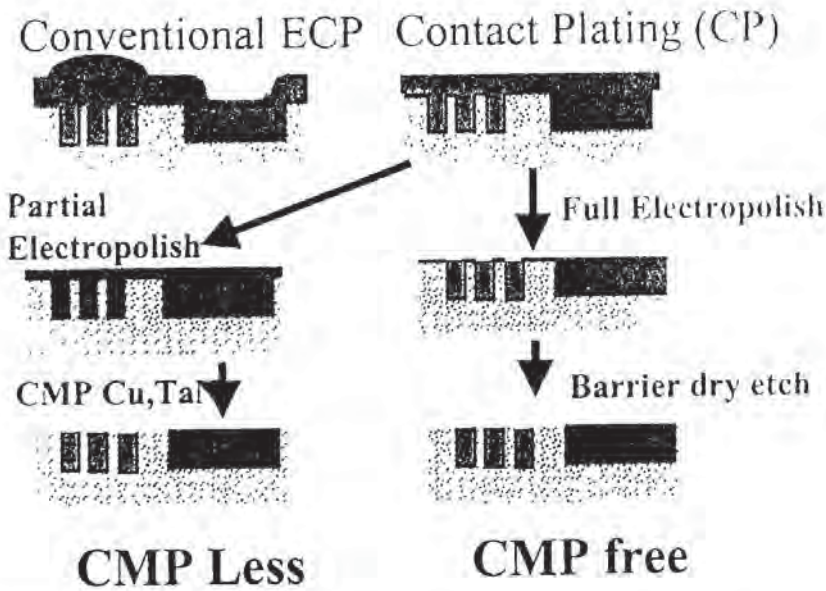


Fig. 16-43 Schematic diagram of CMP-less and CMP-free process flows by using a process that produced planar-Cu films after the plating process.[61]

A tool designed for precise electropolishing was introduced by ACM Research Inc. They refer to the process as *stress-free polishing* (SFP), and tool is called the ACM Ultra SFP.™ It is claimed that the SFP Ultra can polish Cu supported by ultra-low-*k* dielectrics (i.e., with a *k*-value less than 1.8).

16.7 CONTAMINATION CONTROL IN COPPER TECHNOLOGY

In Section 16.1 the issue of copper-contamination was introduced. Also briefly listed were the on-chip lines-of-defense and Cu-manufacturing protocols developed by wafer fabs to guard against this occurrence. Here additional information is provided about methods used to control copper-contamination in wafer manufacturing environments.

16.7.1 Sources of Copper Cross-Contamination in a Wafer Fab

In a completed device with a dual-damascene interconnect (and during many stages of the wafer manufacturing sequence), the embedded copper lines and vias are fully encapsulated with barrier-layers to prevent Cu out-diffusion into the surrounding dielectric and silicon areas. In those processes the likelihood of copper contaminating either other parts of the chip, or the wafer-fab environment, are small. However, in several process steps, Cu is exposed or is present outside of these sealed boundary areas (e.g., during those steps that occur from Cu-deposition to Cu-CMP). The most obvious risk of Cu-contamination occurs when large open areas of Cu are present on the wafer, or when Cu-containing chemicals or waste products - such as electroplating solutions or Cu-CMP slurry - are present. Another critical mode of Cu-contamination results from the high-energy bombardment of exposed Cu surfaces during plasma processing (e.g., via-open etch, and resist-strip). The following wafer processing steps (in roughly descending order of importance), can thus be considered to carry the highest risk of spreading Cu contamination - either into the deeper layers of an individual wafer or from wafer-to-wafer: **a**) Cu-CMP; **b**) Cu-deposition (including PVD seed-layer-deposition and electroplating); **c**) post-plating anneal: **d**) cap diffusion-barrier layer deposition; and **e**) via opening.[73]

During Cu-seed-layer deposition, electroplating, and post-plating anneal processes, the front side of the wafer surface is almost completely covered with a blanket Cu-film (and some Cu may find its way to the bevel and wafer backside during one or more of these steps). Therefore, cleaning of the wafer backside and bevel at certain critical steps during this stage may be necessary to prevent the spread of Cu particles from wafer-to-wafer by way of wafer-handling equipment (see Sect. 16.8.3). A barrier layer should also ideally extend over the whole wafer

surface, including around the bevel and on the backside to prevent Cu from diffusing into the wafer. This could be accomplished by using a wafer frontside barrier-layer (typically the conductive barrier-layer deposited before Cu), which overlaps a diffusion-barrier layer present on the wafer backside (e.g., CVD-SiN). Thus, the wafer bevel would also be completely covered by one or both of these barrier-layers. In many cases, the backside SiN diffusion-barrier-layer is not present. The backside and bevel cleaning is even more important in such cases. In some cases, if there is no backside diffusion-barrier layer, a silicon etch is performed after the backside and bevel cleaning step.[74] Its purpose is to remove a thin layer of silicon from the wafer backside that contains any copper that was deposited by the previous processes.

As noted above, contamination from copper can arise from tools and equipment involved in the deposition and handling of wafers. For example, a deposition tool that coats wafers with copper may cause it to be deposited on the bevel of the wafer. This wafer with copper on its bevel may be sent to a metrology tool equipped with a wafer handler that manipulates the edges of the wafers. (Such metrology tools are commonly shared among various process steps because manufacturers generally find that the acquisition of dedicated metrology equipment for copper processing is cost-prohibitive. These tools may include in-line SEMs for critical-dimension measurement, film-thickness monitors, and optical defect inspection devices.) The metrology-tool wafer-handler is now contaminated with copper, and can then cross-contaminate other wafers (for example, those that are on their way to an etch tool). The etcher thus eventually becomes contaminated with copper, and this contamination can spread throughout the fab (accumulating in plasma process chambers, wet benches, and lithography steppers). Contamination can also be spread by way of the wafer backside, as many wafer-handlers and robots hold and lift wafers by their backsides.

Wafer-handling by transport in cassettes is another likely source of copper cross-contamination. If copper is left on the wafer bevel as it exits a process tool, the carrier will invariably be contaminated with copper. Great care must thus be taken to either limit the use of wafer carriers to a specified area or to switch to a clean carrier once the copper is removed from the bevel. Wafer carriers may also need to be cleaned more frequently than otherwise required just for particle control. Furthermore, to prevent wafer-handlers and wafer-carriers from being contaminated by Cu particles on the wafer edge, it is preferable to maintain a sufficient edge exclusion of the Cu seed-layer or electroplated film. However, a full-faced seed-layer is typically required to allow electroplating with an edge-exclusion region of less than 4-mm. If dedicated cassettes are used to move the

wafers from the PVD-tool to the plating tool, and a cleaning step that removes the Cu from the bevel (and wafer backside) after electroplating is used, this problem can be circumvented.

Another source of possible copper cross-contamination is wafer breakage. Although the incidence of wafer breakage in processing tools has dramatically declined in recent years, it still occasionally happens. Thus, protocols for cleaning tools in which a wafer that contains copper has broken, are crucial to preventing factory-wide cross-contamination. A decontamination plan is required for each area and tool, which mandates appropriate cleaning methods and wipedowns in the immediate area in which the breakage occurred. However, there is no easy test for demonstrating the cleanliness of a tool after such breakage and cleanup, short of analyzing a test-wafer for copper-contamination.

Copper can reach the wafer bevel or backside during a deposition process. However, these surfaces can be protected by clamping and sealing the wafer hermetically during the plating operation so that only the face of the wafer is exposed during the process as required. The SABRE Electrofill™ tool from Novellus Systems uses a clamping method known as a *clamshell* to prevent the wafer backsides from being exposed to copper-containing solutions during the electroplating process. Surface analysis over a period of time during which 100,000 wafers were processed through a SABRE tool showed that a consistently low copper concentration of $< 10^{11}$ atoms/cm^2 were present (which was similar to the copper concentrations on control-wafers that did not undergo the plating process).[75]

The plating tool from Applied Materials (Electra™) uses a different approach. It contains a separate backside- and bevel-cleaning station integrated into the tool to treat each wafer after the electroplating step such that any copper that is deposited is removed (see Sect. 16.8.3 for more details).

16.7.2 Effects of Copper-Cross Contamination at the Back-End-of-Line (BEOL)

The concern for copper cross-contamination at the front-end-of-line (FEOL) stages of wafer processing is that the copper can diffuse into the active device regions and cause degradation of the gate-oxide-integrity or *pn*-junction leakage. The method of ensuring that copper-contamination is not occurring in the FEOL bays of a wafer fab is to monitor the MOS-C characteristics of wafers passing through the process line (much in the same way that is also done to safeguard against other forms of metal contamination - e.g., sodium).

However, the concerns at the BEOL phase of the wafer processing sequence are different from those feared at FEOL. That is, the solid solubility of Cu at

BEOL processing temperatures is relatively low, so not much Cu is expected to be incorporated into the silicon substrate from Cu on the wafer surface as long as the process temperature does not exceed 400°C. A test at SEMATECH took wafers with Cu plated on the backside, and put them into a furnace at 400°C.[76] Subsequent tests for leakage and threshold-voltage-shift showed no deviation from control wafers. Apparently the gettering mechanisms that protect devices from other contaminants can also handle levels of copper-contamination from such an event. As a result, worries about Cu entering the Si wafer at BEOL are probably somewhat exaggerated. On the other hand, the concern that copper will diffuse into the interlevel dielectric and cause leakage during BEOL processing is more real. The failure due to such a degradation of interconnect-leakage from copper contamination could also be one that develops slowly during the life of a part.

16.7.3 Cu Removal from the Wafer Bevel/Edge and Backside

Isolating Cu production from the rest of a wafer fab's manufacturing area is one approach to control copper contamination. But, many fabs share such critical and sophisticated tools as metrology and lithography equipment. Thus, such tools must accept Cu-processed wafers but it must be ensured that no contamination transfers to non-Cu wafers. While backside hermetic sealing and clamp rings are used to provide electrical contact and to mask the wafers exclusion zone from Cu deposition, they may not be 100% effective in preventing Cu deposition in the exclusion zone and on the wafer backside. This condition is further exacerbated by trends that minimize the exclusion zone to 3-mm (and even 2-mm), effectively putting the deposited Cu blanket onto the beveled edge of the wafer (Fig. 16-44a). Furthermore, since CMP cannot remove copper from the bevel and

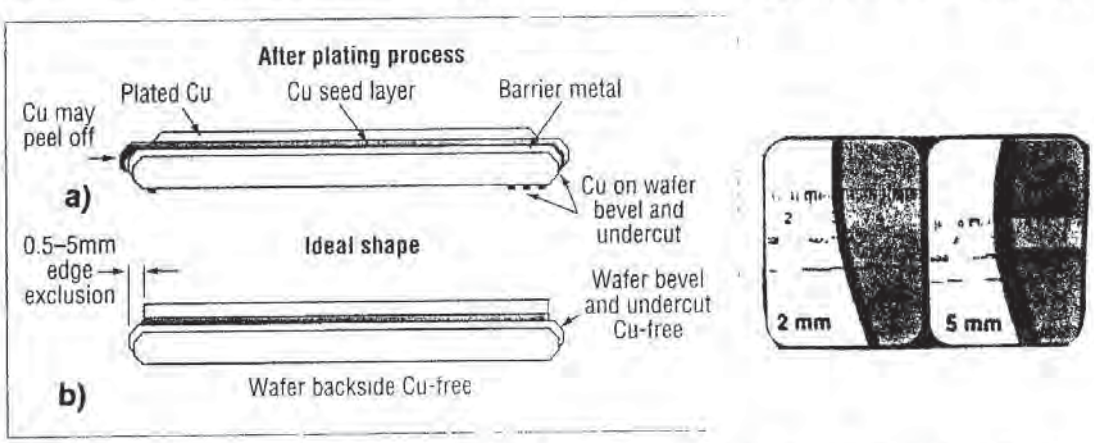


Fig. 16-44 a)Full coverage electrochemical Cu plating; b) The ideal Cu condition on the wafer after SPCE. By permission of Solid State Technology. Published by PennWell.[74]

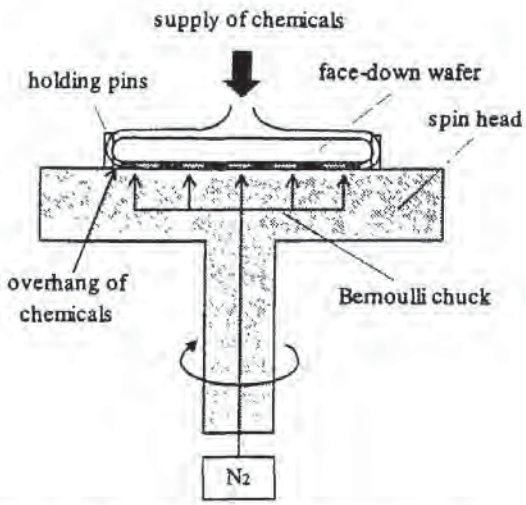


Fig. 16-45 Schematic diagram of the single-wafer cleaning system with a Bernoulli chuck.

backside, after a few layers, Cu-peeling (and resulting Cu cross-contamination) due to film buildup may occur.

The approach used to overcome this problem is to remove any copper that may have accumulated on the wafer-backside, bevel/edge, and exclusion-zone with a spin-etching process. Such a process is carried out immediately after the electroplating step is completed, and may be conducted either on a standalone spin-processor or on spin-processor that is integrated into the platform of the elctroplating tool.

A *standalone, single-wafer spin-cleaning-system* for backside Cu removal has been developed by SEZ Inc. They call their technology *spin-process contamination elimination* (SPCE™). During SPCE the wafer is suspended horizontally and frontside-down on a nitrogen cushion above a rotating chuck, utilizing the Bernoulli principle (Fig. 16-45). The substrate is held in place lateral with locating pins about the wafer perimeter. As the chuck and wafers are spun, the wafer is lifted about 1-mm. Wet-etchants are dispensed onto the wafer backside from a radially oscillating nozzle (e.g., modified HNO_3 chemicals are used for Cu removal), and the N_2 flow protects the entire front of the wafer (except the edge) from the chemicals. The degree of wraparound of chemicals onto the front of the wafer is a function of the N_2 flow-rate, the rotation speed of the chuck, and the viscosity and composition of the chemicals. This enables contamination and film removal from the back, edge/bevel, and front of the wafer without damaging the devices and without the use of masking materials on the frontside of the wafer. The width of the exclusion ring is tunable from 0.5-5-

Fig. 16-46 Edge-clean chambers in the Applied Materials Electra electroplating tool. (Courtesy of Applied Materials)

mm.[74] DI-water and nitrogen are applied to the wafer for rapid rinsing and drying. Fig. 16-44b shows ideal Cu coverage on a wafer after an SPCE process.

A backside and edge *Cu-removal spin processor* has also been *integrated* into the Electra™ electroplating tool of Applied Materials. After the electroplating process, the wafer is moved to the cleaning chamber, where it is loaded face down by a robot onto the self-centering wafer hoop. A wafer chuck holds each wafer, which is then lowered into a cavity with three chemical channels below and three above the wafer (Fig. 16-46). While the wafer is rotated, a DI-water rinse first rinses the electrolyte from the wafer surface. As the wafer is spun dry at high rotation speeds, the chemical dispensing arm moves into position to release its etching/cleaning chemical precisely at the edge of the wafer. Three sets of nozzles (120 degrees apart) enable simultaneous chemical dispensing for very short edge clean times. While the chemicals remove any edge and backside copper, DI-water is sprayed on the front side. By rotating the wafer and balancing the flows, it is possible to control how much material from the backside overwraps, either on the side or the bevel, or just above the bevel, or whether its kept from coming to the front side at all. Figure 16-47 shows the programmable edge exclusion with this edge clean process.[50]

An integrated bevel and backside cleaning process is also offered in the Novellus SABRE™ electroplating system. In this approach, the Cu is removed

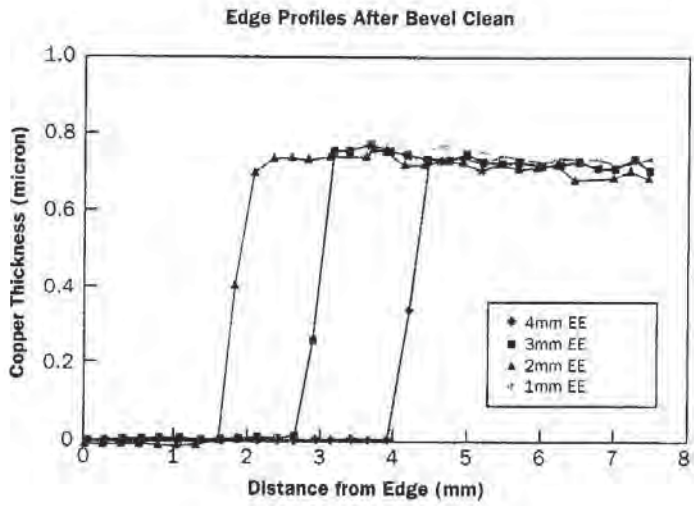


Fig. 16-47 Programmable edge exclusion with the applied Materials Electra™ edge-clean process. (Courtesy of Applied Materials)

from the bevel after the Cu seed-layer is deposited (i.e., prior to the electroplating process). The removal is carried out in the cleaning station of the tool.[78]

16.8 RELIABILITY OF COPPER INTERCONNECTS

As described in Sect. 16.1, copper lines offer the benefit of improved reliability over Al lines, primarily due to their superior electromigration lifetimes. However, the issue of copper interconnect reliability has other aspects as well, and some of these are described in this section.

16.8.1 Reliability of Copper Interconnects: "Missing-Metal" Defects

One Cu reliability issue involves post-CMP defects in narrow lines, which are referred to as "missing-metal" defects (Fig. 16-48). Such defects occur as a result

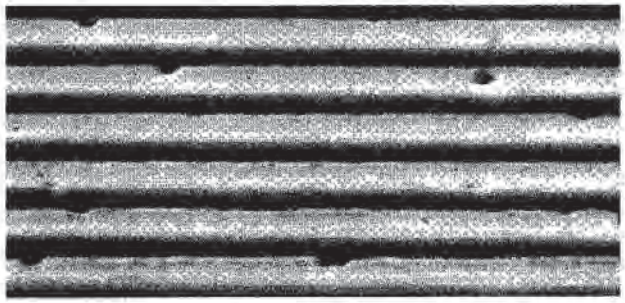


Fig. 16-48 Example of "missing-metal"-type defects. These defects arise from grain pull-out or corrosion and are exposed during the CMP process.[39] Reprinted with permission of Semiconductor International.

of corrosion or *grain-pullout* of lines exposed to a CMP-process. While the mechanism for these defects is poorly understood, it appears that their occurrence is influenced by a number of factors, including: plating-chemistry; plating-waveform; composition of the barrier-layer; and thermal-treatment. The latter effect appears to be most significant, and is thus discussed further here.[39]

Copper-lines are annealed after electrodeposition with the Cu overburden still in place. High thermal-excursions can cause large stress in the Cu films. That is, as the temperature is increased, the thermal expansion of the copper is greater than that of the surrounding dielectric material. This Cu expansion thus induces compressive-stress in the copper film that causes the film to re-crystallize and relax through dislocation motion. However, upon cooling the copper contracts and goes into tensile stress that is much higher under ambient temperature conditions than in the as-deposited film, and such stressed crystalline-films are prone to grain-pullout during CMP.

To reduce the incidence of defects related to thermal treatment it is necessary to minimize the temperature excursion of the post-deposition-anneal process (i.e., while the Cu overburden remains in place). Temperatures should be kept below the Cu plastic-flow limits (~200°C) so the copper can expand and contract elastically. Figure 16-49a shows the sensitivity of via-chain yield to the post-electroplating annealing temperature. Some have said that controlling the defects related to the copper process is perhaps the most important reliability issue facing the drive to achieve higher yields for copper in production.[39]

16.8.2 Reliability of Copper Interconnects: Plated vs. CVD Cu Films

Another reliability aspect observed in copper interconnects is that electroplated copper is more reliable than CVD-Cu with respect to electromigration failures.

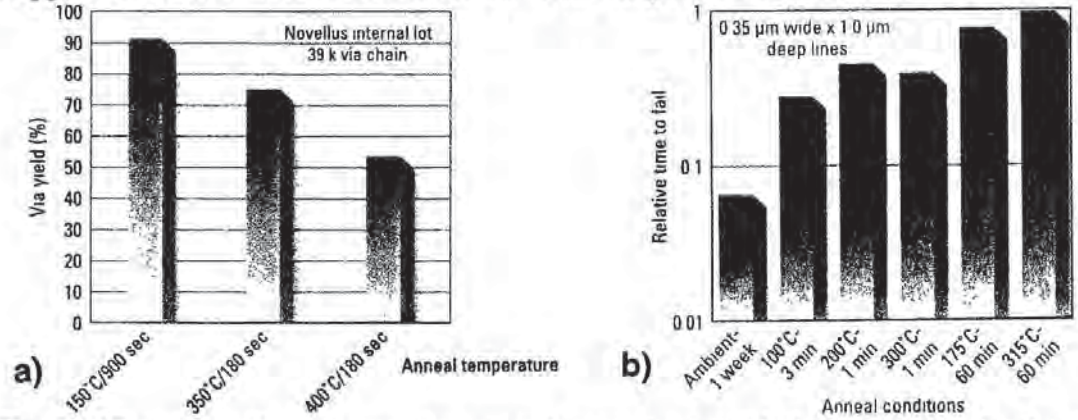


Fig. 16-49 a) The effect of post-plate anneal temperature with the copper overburden in place on via-chain yield.[39] b) Electromigration lifetimes for narrow lines (0.35-μm) with various pre-CMP anneals.[39] Reprinted with permission of Semiconductor International.

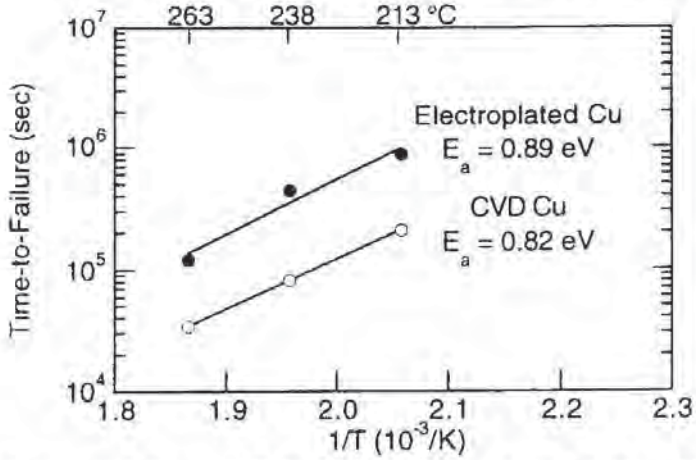


Fig. 16-50 Plot of time-to-failure of CVD-Cu and electroplated-Cu lines.[80] (© IEEE 1998)

As shown in Fig. 16-50, this is especially true for deep-submicron Cu linewidths. (The 0.4-μm-thick Cu-lines in Fig. 16-50 were tested for electromigration behavior after deposition, annealing [at 400°C for one hour], and CMP.[80]) Copper-lines deposited by electroplating exhibit longer lifetimes under electromigration-stressing than do CVD-Cu-lines because CVD-Cu has a smaller as-deposited grain size. In the narrow trenches of deep-submicron dual-damascene interconnects, electroplated-Cu has a bamboo grain-structure, which is conducive to superior electromigration behavior (whereas CVD-Cu has smaller grains after annealing than Cu deposited by electroplating, as can be seen in Fig. 16-51).[80,81]

As far as the electroplated-Cu-lines themselves, their electromigration reliability is impacted by the line-width and post-plating anneal-cycle. Wide lines anneal fully at the lowest anneal-temperatures, and when fully annealed they

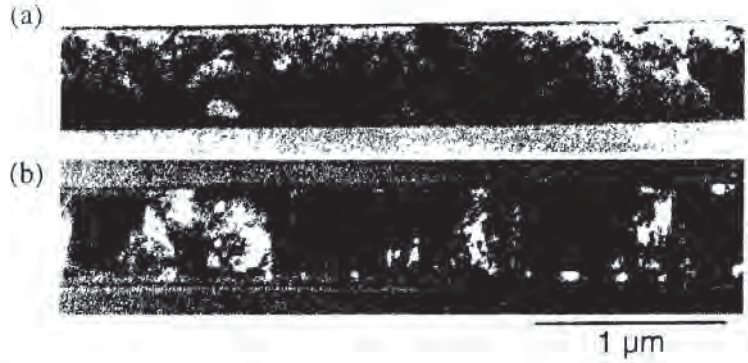


Fig. 16-51 Plan-view TEM micrographs of Cu lines in trenches after annealing: a) CVD-Cu; and b) electroplated Cu. (© IEEE 1998)

exhibit the longest electromigration lifetimes. Narrower linewidths require a higher-temperature anneal-cycle to achieve the same reliability behavior (see Fig. 16-49b, which shows the electromigration lifetimes of narrow copper-lines versus anneal-time and temperatures).[39] However, higher-temperature annealing cycles lead to greater "missing-metal" defect levels in narrow Cu-lines. Thus, a tradeoff must be made between deteriorating defect-performance and improved electromigration-performance as the anneal-temperature is increased.[39]

It was also reported that by incorporating a small amount of magnesium into the copper, various characteristics of the Cu interconnect were improved. That is, by forming a CuMg/Cu/CuMg stack, it was observed that the Mg diffuses through the copper and aggregates on the Cu surfaces. At the interface between the Cu seed-layer and the TiN barrier-layer this Mg improves the adhesion of copper to the TiN. At the top surface of the Cu-layers, the Mg forms a self-limiting oxide that hinders copper oxidation. Electromigration characteristics of such Cu/Mg stacked layers showed no difference relative to pure copper layers.[79]

16.9 ENVIRONMENT, HEALTH, AND SAFETY ISSUES OF COPPER TECHNOLOGY

The implementation of copper technology in IC fabrication introduces new chemistries, tools, and waste streams into the manufacturing arena. Before copper processes are put into production, it is important to address the *environment, health, and safety issues* (EHS) involved with them. Copper brings five new technologies to wafer fabrication, and their EHS impacts are discussed here: barrier-layer deposition; copper seed-layer deposition; Cu-fill by electroplating; copper CMP; and copper wafer reclaim.[82]

The first two of these processes, *barrier-layer deposition* and *Cu seed-layer deposition* are currently PVD processes which use solid sources, and hence do not involve any special EHS considerations. *Electrolytic plating for Cu fill*, however, is a new technology for the semiconductor industry, which also involves new chemistries, tools, and wastes. Nonetheless, commercially available electroplating chemistries used in the printed-circuit wiring board (PWB) industry have been evaluated and found to have no particular hazards or worker exposure issues. That is, all materials are TSCA listed (Toxic Substance Control Act). The primary concern is the two waste streams generated by the process: rinse water and a concentrated bath.

Copper CMP involves the use of a slurry that may or may not contain any chemicals that are environmentally hazardous. However, the process effluent is a potential environmental hazard, insofar as the it contains all the copper removed from the wafer by the CMP process. Development and manufacturing fabs

generate a large number of *test wafers that are reclaimed.* When these have a copper film, they cannot be reclaimed using existing methods. Nevertheless, relatively environmentally friendly techniques have been developed for this purpose (e.g., ammonium persulfate/sulfuric acid),[83] which is also compatible with electroplating waste. Nevertheless, the wafer reclaim process, like the electroplating process, generates the same two waste streams.

Thus, the two key steps in a copper dual-damascene structure – electroplating and CMP – are both wet-chemical processes. They use large amounts of water and create large amounts of acid and heavy-metal waste. They require large quantities of slurries, plating solution, and other liquid feedstocks. Bulk chemical distribution systems and waste-water treatment facilities for these materials can be built into new fabs. Accommodating them in an existing fab is more difficult. Typical fab delivery systems are designed around gases and DI-water, not slurries and plating chemicals.

16.9.1 Copper Waste Handling

The liquid chemical wastes from the various copper process steps described above must be evaluated for their toxic substance concentrations, and treated appropriately. It has been determined that the rinse water from the copper plating and wafer reclaim process ordinarily contains relatively low-levels of copper and contribute only minor increases in the total copper concentration of the industrial waste-water discharge. However, copper CMP contributes more than 80% of the discharged copper on a mass basis, and is likely to require treatment before being discharged to the industrial waste-water.

16.9.1.1 Handling Concentrated Waste from Plating and Wafer Reclaim: The liquid chemical wastes and slurries containing concentrated copper must be treated to remove the copper. A process similar to the electroplating process (called *electrowinning)* is one method for treating the concentrated plating baths and wafer reclaim wastes. That is, copper is reduced and plated out of solution at the cathode, and water is oxidized (split) to form oxygen at the anode. This process is capable of reducing the copper concentration in these waste liquids to levels below the current concentration based discharge limit for *publicly owned treatment works* (POTW). While, the time to reach such limits with the electrowinning process is 20-40 hours, it is still a cost-effective method and it does not generate other waste streams (e.g., sludge).

16.9.1.2 Handling Copper CMP Effluents: The treatment of the Cu-CMP effluent is done in another way. The primary goal of such treatment is to remove the

copper from the effluent. Recycling of the water is a secondary goal. In many CMP effluents the copper is entirely soluble and is not incorporated into the abrasive particles of the slurry residue. Thus, the treatment first involves microfiltering the effluent to remove the nonhazardous abrasive solids (which are then discharged into the fabs industrial wastewater and ultimately to the POTW). Next the water containing the slurry chemicals and copper is treated. The slurry oxidizer (e.g., H_2O_2) is removed by appropriate chemical addition. Then the copper can be removed by several different methods:

1. An ion exchange process can be employed, using cation-exchange canisters. These require periodic on-site or off-site regeneration (which again involves an electrowinning procedure). Such a treatment scheme can achieve very high levels of copper removal from the relatively dilute CMP effluent.

2. Coagulation and microfiltration is another method that can effectively reduce the copper content to less than 0.1 ppm.[83]

3. To insure copper removal to sub-0.1 ppm levels due to stringent POTW discharge requirements, it may be necessary to use water-soluble heavy-metal removal agents. These materials typically contain sulfide functionality, which bonds strongly to transition metals and forms insoluble precipitants.[84]

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