**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

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| ADVANCED INTEGRATED CIRCUIT PROCESS LLC, | § | |
| | § | |
| Plaintiff, | § | Case No. 2:24-cv-000730-JRG |
| | § | (Lead Case) |
| v. | § | |
| | § | |
| UNITED MICROELECTRONICS CORPORATION | § | |
| | § | |
| Defendant, | § | |

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|---|---|---|
| | § | |
| TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED | § | Case No. 2:24-cv-00623-JRG |
| | § | (Member Case) |
| Defendant. | § | |

**DEFENDANT UNITED MICROELECTRONICS CORPORATION'S INVALIDITY CONTENTIONS**

## I. INTRODUCTION

Pursuant to Rule 3-3 of the Local Patent Rules of the Eastern District of Texas and the Court's Third Amended Docket Control Order (Dkt. 83), Defendant United Microelectronics Corporation ("Defendant") provides its invalidity contentions demonstrating the invalidity of the patent claims asserted by Plaintiff Advanced Integrated Circuit Process LLC ("Plaintiff") in its Infringement Contentions for U.S. Patent No. 7,579,227 (the "'227 Patent"), U.S. Patent No. 7,923,764 (the "'764 Patent"), United States Patent No. 8,198,686 (the "'686 Patent"), United States Patent No. 8,253,180 (the "'180 Patent"), United States Patent No. 8,587,076 (the "'076 Patent"), United States Patent No. 8,796,779 (the "'779 Patent"), and United States Patent No. 8,907,425 (the "'425 Patent") (collectively, the "Asserted Patents").

The asserted claims of the Asserted Patents are as follows (collectively, the "Asserted Claims"):

| Asserted Patent | Asserted Claims |
|---|---|
| 7,579,227 | 1, 2, 7, 8, and 14 |
| 7,923,764 | 1, 2, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, and 19 |
| 8,198,686 | 25, 26, 27, 28, 31, and 35 |
| 8,253,180 | 1, 2, 3, 5, 6, 11, 13, 14, 16, 17, 18, 19, 21, and 22 |
| 8,587,076 | 1, 2, 3, 6, 7, 8, 10, 11, 12, and 13 |
| 8,796,779 | 1, 2, 7, 12, and 13 |
| 8,907,425 | 1, 3, 4, 7, 8, and 11 |

Defendant hereby provides its invalidity contentions as to the Asserted Claims. Defendant reserves the right to serve amended invalidity contentions in the event that Plaintiff amends its infringement contentions.

## II. RESERVATIONS

### A. General Reservations

Consistent with P.R. 3-6, Defendant reserves the right to amend these Invalidity Contentions. The information and documents that Defendant produces are provisional and subject

to further revision. Defendant reserves the right to amend or supplement these disclosures and the subsequent document production should Plaintiff: 1) provide any information that it failed to provide in its P.R. 3-1 and 3-2 disclosures; 2) amend its P.R. 3-1 or 3-2 disclosures in any way; or 3) attempt to rely upon any information at trial, in a hearing, or during a deposition which it failed to provide in its P.R. 3-1 and 3-2 disclosures.

The information provided shall not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Nothing contained in these Invalidity Contentions should be understood or deemed to be an express or implied admission or contention with respect to the proper construction of any terms in the asserted claim, or with respect to the alleged infringement of that claim.

**B. Ongoing Discovery**

Furthermore, because only limited discovery has occurred, Defendant reserves the right to revise, amend, and/or supplement the information provided herein, including identifying, charting, and relying on additional references, should Defendant's further search and analysis yield additional information or references, consistent with this Court's Patent Local Rules and the Federal Rules of Civil Procedure. Discovery is ongoing, and Defendant's prior art investigation and third-party discovery is therefore not yet complete. Defendant reserves the right to present additional items of prior art located during the course of discovery or further investigation.

**C. Claim Constructions**

Defendant reserves the right to revise its ultimate contentions concerning the invalidity of the Asserted Claims, which may change depending upon any findings as to the priority date of those claims, and/or positions that Plaintiff or expert witnesses may take concerning infringement and/or invalidity issues. Defendant does not waive the right to contest any claim constructions or to take positions during claim construction proceedings that have yet to occur that may be

inconsistent with the invalidity contentions herein. Consequently, Defendant also reserves the right to amend or supplement these invalidity contentions in the event that the claims are construed differently at some point in the future.

Defendant's invalidity contentions are not adoptions or admissions by Defendant as to the accuracy of Plaintiff's allegations, admissions, or positions, or of this Court's prior claim constructions. Accordingly, these contentions are made in the alternative, are not necessarily intended to be consistent with each other, and should not be otherwise construed. Defendant expressly reserves the right to take positions with respect to future claim construction or infringement issues that are inconsistent with, or even contradictory to, the claim construction or infringement positions expressed or implied in the invalidity contentions set forth herein.

**D. Plaintiff's Infringement Contentions**

Plaintiff's disclosures under P.R. 3-1 and 3-2 are deficient. For example, Plaintiff has charted just two products and contends, without sufficient support, that the two charted products are exemplary of every product UMC makes using its 22nm and 28nm processes. Because such deficiencies may lead to further grounds for invalidity once Plaintiff has fully disclosed its infringement theories for all Accused Products, Defendant specifically reserves the right to modify, amend, or supplement these contentions as Plaintiff modifies, amends, or supplements its disclosures under P.R. 3-1, 3-2 and/or 3-6, and/or produces documents in discovery.

**E. The Intrinsic Record**

Defendant further reserves the right to rely upon applicable industry standards and prior art cited in the file histories of the Asserted Patents and any related U.S. and foreign patent applications as invalidating references or to show the state of the art. Defendant further intends to rely on the patent applicant's admissions concerning the scope of the prior art relevant to the Asserted Patents found in, inter alia: the patent prosecution history for the Asserted Patents and

any related patents and/or patent applications, reissue applications or reexaminations; any deposition testimony of the named patent applicant on the asserted patent; and the papers filed and any evidence submitted by Plaintiff in connection with this litigation as well as prior litigation and PTAB proceedings.

### F. Contextual Evidence

Defendant's claim charts cite to particular teachings and disclosures of the prior art as applied to features of the Asserted Claims. However, persons having ordinary skill in the art generally may view an item of prior art in the context of his or her experience and training, other publications, literature, products, and understanding. As such, the cited portions are only examples, and Defendant reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation or the claimed subject matter as a whole. Defendant further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony, including expert testimony, to establish bases for combinations of certain cited references that render the Asserted Claims obvious. The references discussed in the claim charts may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame. The suggested obviousness combinations are provided in the alternative to anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory, nor are they admissions that obviousness is not to be tested against the prior art as a whole.

### G. Priority Date

Defendant reserves the right to present additional items of prior art or further support for current prior art should discovery or further investigation show that any one of the Asserted Claims

is not entitled to the priority date of any priority application, for example JP 2005-227457 filed on August 5, 2005. For example, discovery may show that the Asserted Claims are not entitled to the benefit of the filing date of the priority application or any earlier date because, at the time of filing the Japanese application, the applicant failed to enable or adequately describe the subject matter of the Asserted Claims.

## III. INVALIDITY

Based on Plaintiff's Infringement Contentions, Defendant identifies the following items of prior art that anticipate or render obvious the Asserted Claims of the Asserted Patents. Defendant fully incorporates by reference the Invalidity and Ineligibility Contentions served by Co-Defendant Taiwan Semiconductor Manufacturing Company Limited in this Action. Defendant further fully incorporates by reference all docket entries and exhibits to the Petitions for *Inter Partes* Review filed by Co-Defendant Taiwan Semiconductor Manufacturing Company Limited against Plaintiff, namely IPR2025-00683, IPR2025-00682, IPR2025-00828, IPR2025-00829, IPR2025-00830, IPR2025-00831, and IPR2025-00832. Defendant further identifies the prior art referenced in Section IV below.

### A. State of the Art

The core concepts claimed in the Asserted Patents are not new or novel. Long before the priority dates of the Asserted Patents, the semiconductor industry had already disclosed each of the core concepts of the Asserted Patents, e.g. that using high-k gate dielectrics, like hafnium oxide, provided significant benefits as gate widths decreased and transistor sizes shrunk, that dual metal gates formed by a replacement gate process was especially beneficial for use with a high-k gate dielectric, that stress introduced in the channel of both P and N type transistors improved channel mobility, and that numerous different sidewall structures could provide benefits, including the alleged four-layer sidewall asserted against the UMC accused product. For example, the

Symposium on VLSI Technology was first organized in 1981 and provides an annual event for the "world's top technologists to engage in an open exchange of ideas" through the "presentation of high-quality papers [which] has made it possible for attendees to learn about new directions in the development of VLSI technology."[1] The following non-exhaustive list of presentations and papers given at the 2002-2004 VLSI Symposiums evidence the state of the art and the knowledge of a person of ordinary skill prior to the priority dates of the Asserted Patents.

| Primary Author or Publisher | Reference | Prior Art Date |
|---|---|---|
| Rim et al. | "Mobility Enhancement in Strained Si NMOSFETs with HfO2 Gate Dielectrics" ("Rim-2002") | June 11-13, 2002 |
| Onishi et al. | "Effects of High-Temperature Forming Gas Anneal on HfO2 MOSFET Performance" ("Onishi-2002") | June 11-13, 2002 |
| Samavedam et al. | "Metal Gate MOSFETs with HfO2 Gate Dielectric" ("Samavedam-2002") | June 11-13, 2002 |
| Harada et al. | "Specific Structural Factors Influencing on Reliability of CVD-HfO2" ("Harada-2002") | June 11-13, 2002 |
| Pidin et al. | "Low Standby Power CMOS with HfOz Gate Oxide for 100-nm Generation" ("Pidin-2002") | June 11-13, 2002 |
| Lee et al. | "Self-Aligned Ultra Thin HfO2 CMOS Transistors with High Quality CVD TaN Gate Electrode" ("Lee-2002") | June 11-13, 2002 |
| Lu et al. | "Improved Performance of Ultra-Thin HfO2 CMOSFETs Using Poly-SiGe Gate" ("Lu-2002") | June 11-13, 2002 |
| Wilk et al. | "Improved Film Growth and Flatband Voltage (Control of ALD HfO2 and Hf-AI-O with n+ poly-Si Gates using Chemical Oxides and Optimized Post-Annealing" ("Wilk-2002") | June 11-13, 2002 |
| Watanabe et al. | "Design Guideline of HfSiON Gate Dielectrics for 65 nm CMOS Generation" ("Watanabe-2003") | June 10-12, 2003 |
| Tsai et al. | "Comparison of sub 1 nm TiN/HfO2 with Poly-Si/HfO2 gate stacks using scaled chemical oxide interface" ("Tsai-2003") | June 10-12, 2003 |
| Kerber et al. | "Direct Measurement of the Inversion Charge in MOSFETs: Application to Mobility Extraction in Alternative Gate Dielectrics" ("Kerber-2003") | June 10-12, 2003 |

[1] https://archive.vlsisymposium.org/04web/about.html (last visited April 1, 2025)

| Primary Author or Publisher | Reference | Prior Art Date |
|---|---|---|
| Morioka et al. | "High mobility MISFET with low trapped charge in HfSiO films" ("Morioka-2003") | June 10-12, 2003 |
| Kim et al. | "Conventional poly-Si gate MOS-transistors with a novel, ultra-thin Hf-oxide layer" ("Kim-2003") | June 10-12, 2003 |
| Ryu et al. | "Fully Working 1.10µm^2 Embedded 6T-SRAM Technology with High-k Gate Dielectric Device for Ultra Low Power Applications" ("Ryu-2004") | June 15-17, 2004 |
| Weber et al. | "55nm high mobility SiGe(:C) pMOSFETs with HfO2 gate dielectric and TiN metal gate for advanced CMOS" ("Weber-2004") | June 15-17, 2004 |
| Chidambaram et al. | "35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS" ("Chidambaram-2004") | June 15-17, 2004 |
| Mistry et al. | "Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology" ("Mistry-2004") | June 15-17, 2004 |
| Chen et al. | "Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application" ("Chen-2004") | June 15-17, 2004 |

### B. The '227, '764, '180, and '076 Patents

The claim charts found below identify where each element of the Asserted Claims is found in the given prior art. Defendant fully incorporates by reference the Petition for *Inter Partes* Review No. IPR2025-00828 and the Declaration of Dr. Jack Lee in Support of IPR Petition (Ex-1003) thereto, the Petition for *Inter Partes* Review No. IPR2025-00829 and the Declaration of Dr. Jack Lee in Support of IPR Petition (Ex-1003) thereto, the Petition for *Inter Partes* Review No. IPR2025-00830 and the Declaration of Dr. Jack Lee in Support of IPR Petition (Ex-1003) thereto, and the Petition for *Inter Partes* Review No. IPR2025-00831 and the Declaration of Dr. Jack Lee in Support of IPR Petition (Ex-1003) thereto. Defendant reserves the right to revise its claim charts to rely on any of these references to prove the invalidity of the Asserted Claims in a manner consistent with the Federal Rules of Civil Procedure, the Court's Local Rules, the Local Patent Rules and this Court's Orders.

### 1. Prior Art Patents and Patent Applications

| Reference | Exhibit | Prior Art Date |
|---|---|---|
| U.S. Pat. App. Pub. No. 2005/0093084 to Wang et al. ("Wang '084") | 227A1, 764A1, 180A1, 076A1 | October 31, 2003 |
| U.S. Pat. App. Pub. No. 2004/0227185 to Matsumoto et al. ("Matsumoto '185") | 227A2, 764A2, 180A2, 076A2 | January 12, 2004 |
| U.S. Pat. App. Pub. No. 2004/0224471 to Clevenger et al. ("Clevenger") | 227A3, 764A3, 180A3, 076A3 | December 23, 2002 |
| PCT Patent App. Pub. No. WO2005/041307 to Anezaki ("Anezaki") | 227A4, 764A4, 180A4, 076A4 | October 23 2003 |
| U.S. Patent No. 6,348,390 to Wu ("Wu '390") | 227A5, 764A5, 180A5, 076A5 | February 19, 2002 |
| U.S. Pat. No. 4,963,502 to Teng et al. ("Teng") | 227B, 764B, 180B, 076B | October 16, 1990 |
| U.S. Pat. App. Pub. No. 2005/0081781 to Lin et al. ("Lin '781") | 227B, 764B, 180B, 076B | October 17, 2003 |
| U.S. Pat. App. Pub. No. 2004/0150066 to Inoue et al. ("Inoue") | 227B, 764B, 180B, 076B | December 18, 2003 |
| U.S. Pat. App. Pub. No. 2004/0169221 to Ko et al. ("Ko") | 227B, 764B, 180B, 076B | October 30, 2003 |
| PCT Patent App. Pub. No. W02004/017418 to Sakai et al. ("Sakai '481") | 227B, 764B, 180B, 076B | February 26, 2004 |
| U.S. Pat. No. 5,134,451 to Katoh ("Katoh") | 227B, 764B, 180B, 076B | July 28, 1992 |
| U.S. Pat. No. 6,727,148 to Setton ("Setton") | 227B, 764B, 180B, 076B | April 27, 2004 |
| U.S. Pat. No. 6,833,296 to Yugami et al. ("Yugami") | 227B, 764B, 180B, 076B | December 7, 2001 |
| U.S. Pat. App. Pub. No. 2002/0063299 to Kamata et al. ("Kamata") | 227B, 764B, 180B, 076B | May 30, 2002 |
| U.S. Pat. App. Pub. No. 2004/0070037 to Takayanagi ("Takayanagi") | 227B, 764B, 180B, 076B | April 15, 2004 |
| U.S. Pat. No. 6,368,907 to Doi et al. ("Doi") | 227B, 764B, 180B, 076B | April 9, 2002 |
| U.S. Pat. App. Pub. No. 2003/0222303 to Fukuda et al. ("Fukuda") | 227B, 764B, 180B, 076B | December 4, 2003 |

### 2. Prior Art Non-Patents and Patent Applications

| Primary Author or Publisher | Reference | Exhibit | Prior Art Date |
|---|---|---|---|
| Kim, et al. | Conventional n-channel MOSFET devices using single layer $HfO_2$ and $ZrO_2$ as high-k | 227A6, 764A6, 180A6, 076A6 | December 2-5, 2001 |

| Primary Author or Publisher | Reference | Exhibit | Prior Art Date |
|---|---|---|---|
| | gate dielectrics with polysilicon gate electrode ("Kim-2001") | | |
| Jung, et al. | A Highly Manufacturable MIPS (Metal Inserted Poly-Si Stack) Technology with Novel Threshold Voltage Control ("Jung-2005") | 227A7, 764A7, 180A7, 076A7 | June 14-16, 2005 |
| Rotondaro, et al. | Advanced CMOS Transistors with a Novel HfSiON Gate Dielectric ("Rotondaro-2002") | 227B, 764B, 180B, 076B | June 11-13, 2002 |

### 3. Prior Art from *Inter Partes* Review Nos. IPR2025-00828, IPR2025-00829, IPR2025-00830, and IPR2025-00831.

| IPR Ex. No. | Reference |
|---|---|
| 1009 | U.S. Publication 2003/0025135 to Matsumoto, et al. ("Matsumoto '135") |
| 1010 | JP2003-258241 to Kajiyama ("JP-Kajiyama") |
| 1011 | Certified Translation of JP2003-258241 to Kajiyama ("Kajiyama") |
| 1012 | U.S. Publication 2006/0131672 to Wang, et al. ("Wang '672") |
| 1013 | U.S. Publication 2005/0051856 to Ono, et al. ("Ono") |
| 1018 | Wilk, G. D., et al., "High-k gate dielectrics: Current status and materials properties considerations," Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-75, May 15, 2001 ("Wilk-2001") |
| 1019 | U.S. Publication 2005/0045938 to Mutou, et al. ("Mutou") |
| 1023 | U.S. Patent 6,306,712 to Rodder, et al. ("Rodder") |
| 1024 | Sim, J. H., et al., "Effects of ALD HfO2 thickness on charge trapping and mobility," Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 ("Sim") |
| 1025 | U.S. Publication 2004/0110352 to Bu, et al. ("Bu") |
| 1027 | U.S. Publication 2002/0063299 to Kamata, et al. (Kamata) |
| 1028 | U.S. Publication 2006/0091432 to Guha, et al. ("Guha '432") |
| 1029 | Koyama, M., et al., "Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics," Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 ("Koyama-2002") |
| 1030 | U.S. Patent 6,664,577 to Takayanagi ("Takayanagi") |
| 1031 | U.S. Patent 6,911,695 to Ahmed, et al. ("Ahmed") |
| 1032 | Houssa, M., "High-κ Gate Dielectrics" (CRC Press 1st Ed. 2003) ("Houssa-2003") |

| IPR Ex. No. | Reference |
|---|---|
| 1033 | Plummer, J., et al., "Silicon VLSI Technology: Fundamentals, Practice and Modeling" (Prentice Hall 2000) ("Plummer") |
| 1034 | Wolf, S., "Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology" (Lattice 2002) ("Wolf-2002-1034") |
| 1037 | Lee, S. J., et al. "High Quality Ultra Thin CVD HfO2 Gate Stack with Poly-Si Gate Electrode," Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 ("Lee-2000") |
| 1038 | Campbell, "The Science and Engineering of Microelectronic Fabrication", Second Edition (2001) ("Campbell") |
| 1040 | JP2005-064190 to Ono with certified translation ("JP-Ono") |
| 1041 | N. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Third Edition (Pearson/Addison Wesley, 2005) ("Weste") |
| 1042 | U.S. Patent 7,807,990 to Koyama, et al. ("Koyama '990") |
| 1045 | U.S. Publication 2005/0093084 to Wang, et al. (Wang '084) |
| 1048 | U.S. Patent 6,504,214 to Yu, et al. ("Yu '214") |
| 1049 | Lee, B.H., et al., "Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 ("Lee-1999") |
| 1050 | U.S. Publication 2005/0040479 to Koldiaev, et al. ("Koldiaev") |
| 1051 | U.S. Publication 2005/0139932 to Cho, et al. ("Cho") |
| 1052 | Albertin, K.F., et al., "Study of PECVD SiOxNy films dielectric properties with different nitrogen concentration utilizing MOS capacitors," Microelectronic Engineering, Vol. 77, pp. 144-49 (2005) ("Albertin") |

### 4. Identification of Obviousness Combinations Pursuant to P.R. 3-3 (b) and (c)

Based upon Defendant's present understanding of the Asserted Claims, those claims are invalid as obvious in view of the following combination of prior art references. In *KSR International Co. v. Teleflex Inc.*, 500 U.S. 398 (2007), the U.S. Supreme Court rejected the Federal Circuit's rigid "teaching, suggestion, or motivation" requirement in favor of a flexible, functional approach in which an explicit finding of a "motivation" to combine prior art references is not required to establish obviousness. The Supreme Court held that it is sufficient that a combination of elements was "obvious to try" holding that, "[w]hen there is a design need or

market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known option within his or her technical grasp." *Id.* at 402; *see also Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (explaining that when the "combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient," there exists a motivation to combine prior art references even when there is no explicit suggestion in the references themselves "[b]ecause the desire to enhance commercial opportunities by improving a product or process is universal—and even commonsensical"); *LeapFrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157 (Fed. Cir. 2007) (applying KSR and holding that "one of ordinary skill in the art of children's learning toys would have found it obvious to combine the Bevan device with the SSR to update it using modern electronic components in order to gain the commonly understood benefits of such adaption, such as decreased size, increased reliability, simplified operation, and reduced cost").

The Asserted Claims are rendered obvious by the references identified in the attached claim charts, either alone or in the combinations with other prior art references as identified below or in the attached claim charts. The tables above identify prior art that anticipates each asserted claim.

Those tables, the prior art claim charts found in Exhibits 227A1-A7, 227B, 764A1-A7, 764B, 180A1-A7, 180B, 076A1-A7, & 076B, and the table below identifies prior art that by itself, or in combination with other art and/or the knowledge of one skilled in the art, renders the asserted claims obvious.

Defendant contends that all claims that are anticipated by a particular reference are also rendered obvious by that same reference alone, or in combination with the other references, discussed below. Defendant further contends that one of ordinary skill in the art, at the time of the

alleged invention of the Asserted ’227, ’764, ’180, and ’076 Patent Claims, would have been motivated to combine the references disclosed herein in such a way to reach the alleged inventions. The teaching, suggestion, or motivation to combine these references, although not required, is explicitly or implicitly found in one or more of the following: the knowledge or common sense of one of ordinary skill in the art; the prior art references themselves and/or the prior art as a whole, including interrelated teachings of multiple prior art references; the subject matter acknowledged as prior art in the ’227, ’764, ’180, and ’076 Patents; the nature of the problem to be solved and the existence of similar improvements in similar applications; design incentives and other market forces, including the advantages of creating a superior and more desirable product and the effects of demands known to the design community or present in the marketplace; the ability to implement the alleged invention as a predictable variation of the prior art; improvements in similar devices; the interrelated teachings of multiple prior art references; any needs or problems known in the field addressed by the ’227, ’764, ’180, and ’076 Patents; and the number of identified, predictable solutions to the problem addressed by these patents. In addition, the simultaneous (and/or prior) inventions described above, and elsewhere in these contentions, is evidence that motivation to combine the concepts described in the various prior art references did, in fact, exist, and they were, in fact, combined. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary. A person of ordinary skill would have access to the materials found in the cited and attached exhibits and would have at least the ordinary creativity and skill to combine the attached references in ways not explicitly recited above. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary,

| Primary Reference | In Combination With One or More Of |
|---|---|
| Wang ’084 | Clevenger, Matsumoto ’185, Anezaki, Kim-2001, Jung-2005, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| Matsumoto ’185 | Wang ’084, Clevenger, Anezaki, Kim-2001, Jung-2005, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| Clevenger | Wang ’084, Matsumoto ’185, Anezaki, Kim-2001, Jung-2005, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Kamata, Takayanagi, Doi, Fukuda, Sim, Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481, Yugami |
| Anezaki | Wang ’084, Clevenger, Matsumoto ’185, Kim-2001, Jung-2005, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami,Kamata, Takayanagi, Doi, Fukuda, Sim, Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| Wu ’390 | Wang ’084, Clevenger, Matsumoto ’185, Anezaki, Kim-2001, Jung-2005, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| 2001 IEDM Paper by Kim et al. (Kim-2001) | Wang ’084, Clevenger, Matsumoto ’185, Anezaki, Jung-2005, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| 2005 VLSI Paper by Jung et al. (Jung-2005) | Wang ’084, Clevenger, Matsumoto ’185, Anezaki, Kim-2001, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |

| Primary Reference | In Combination With One or More Of |
|---|---|
| Kamata | Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Guha ’432, Wang ’084, Clevenger, Matsumoto ’185, Anezaki, Kim-2001, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Takayanagi, Doi, Fukuda, Sim, Jung-2005, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| Guha ’432 | Matsumoto ’135, Yu ’214, Koyama-2002, Ono, Wang ’084, Clevenger, Matsumoto ’185, Anezaki, Kim-2001, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Jung-2005, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| Matsumoto ’135 | Yu ’214, Koyama-2002, Ono, Guha ’432, Wang ’084, Clevenger, Matsumoto ’185, Anezaki, Kim-2001, Inoue, Rotondaro-2002, Teng, Lin ’781, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Jung-2005, Wilk-2001, Mutou, Bu, Kajiyama, Sakai ’481 |
| Kajiyama | Yu ’214, Koyama-2002, Ono, Guha ’432, Wang ’084, Clevenger, Matsumoto ’185, Anezaki, Kim-2001, Inoue, Rotondaro-2002, Teng, Lin ’781, Matsumoto ’135, Setton, Yugami, Kamata, Takayanagi, Doi, Fukuda, Sim, Jung-2005, Wilk-2001, Mutou, Bu, Sakai ’481 |

Defendant hereby identifies additional motivation and reasons to combine the cited art: One of ordinary skill in the art would be motivated to combine these references in the above combinations for at least the following reasons. One of skill in the art would have been motivated to combine these references, because these references relate to common objectives and subject matter. The use of high-k gate dielectrics was a well-understood concept to improve performance of small transistors. *See, e.g.*, 2002 VLSI Symposium Paper 2.1 by Rim et al. (Rim-2002) (“Strained Si NFETs with high-K dielectrics exhibit significantly enhanced NFET mobility, even over the universal mobility of the SiO2/bulk Si devices, and hold the promise for the best trade-off between mobility and gate leakage reduction, which is especially attractive for low power, high performance CMOS technology.”); 2002 VLSI Symposium Paper 3.1 by Onishi et al. (Onishi-

2002) ("High-temperature FG annealing improved channel carrier mobility as well as subthreshold slopes in both N and PMOSFET with HfO2 gate dielectrics. These features are advantageous in achieving large on current while suppressing off current, and give more flexibility in Vt adjustment."); 2002 VLSI Symposium Paper 3.4 by Pidin et al. (Pidin-2002) ("55-nm CMOS with 3-nm HfO2 gate dielectric was fabricated using conventional process flow with high-temperature anneal of ≥1OOO°C and cobalt silicide. Gate current reduction of more than 3 orders of magnitude was achieved and low off-state current devices were obtained demonstrating very promising characteristics of HfO2 for low standby current applications."); 2002 VLSI Symposium Paper 9.1 by Lee et al. (Lee-2002) ("Compared with PVD TaN devices, the CVD TaN/HfO2 devices exhibit lower leakage current and CV hysteresis, superior interface properties, higher tranaconductance, and superior effective electron and hole mobility."); 2004 VLSI Symposium Paper 5.1 by Ryu et al. (Ryu-2004) ("In this paper, for the first time, we have demonstrated 1.10µm^2 embedded SRAM chip with high-k gate dielectric for ultra low power applications."); 2004 VLSI Symposium Paper 5.3 by Weber et al. (Weber-2004) ("For the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length. SiGe(:C) surface channel pMOSFETs with HfO2 gate dielectric exhibit a 10^4 gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal Si02/Si reference.").

Beyond these VLSI Symposium papers, the prior art MOSFETs and MISFETs devices also disclosed using a high dielectric constant gate insulating film, as recited in the Asserted Claims. *See, e.g.*, Wang '084 at [0023] ("Exemplars of appropriate and preferred high-k materials include . . . HfO2."); Lin '781 at [0003] ("As the gate length in transistors shrinks in order to keep pace with demands for improved performance, the thickness of the gate electrode and the gate dielectric

layer are following a trend toward thinner films. Shrinking device dimensions force a thinner gate dielectric layer in order to maintain an adequate capacitance between the gate electrode and the channel region. A traditional gate dielectric layer consisting of silicon oxide with a dielectric constant (k) of about 4 is being replaced by a high k dielectric layer with a k value of 10 or greater in order to reduce gate leakage current associated with an ultra thin $SiO_2$ layer."); 2005 VLSI Symposium Paper by Jung et al. (Jung-2005) at Conclusion ("Therefore maximum operating voltages above 1.0V are obtained for an extrapolated 10-years lifetime in both poly-Si and MIPS gates with HfSiO/AlOx as a gate dielectric."); Fukuda at [0192] ("Films of high dielectric constants, such as tantalum oxide, alumina, hafnium oxide, etc. may be used. These films can increase the field Strength than Silicon nitride film, and the writing characteristics can be improved.").

A person of ordinary skill in the art would have also been motivated to modify a prior art reference or semiconductor device, or combine the device with one or more of the above prior art references, to use hafnium as the material for the high dielectric constant gate insulating film. It was well known in the art, at the time of the alleged invention, that using a high dielectric constant gate insulating film such as one made of hafnium would prevent gate leakage between the gate electrode and the channel region, among other benefits. *See* Wang '084 at [0004]; Lin '781 at [0003].

Further, the Asserted Claims of the '227, '764, '180, and '076 Patents contain merely a duplication of concepts known in the prior art and have no patentable significance given that no unexpected results occur (i.e., the patentee merely combines known prior art elements according to known methods to yield predictable results). For example, the prior art references of record describe using not only hafnium in the gate dielectric, but also the benefits of using an interfacial

layer underneath the hafnium gate dielectric and above the substrate, for example SiO2. *See, e.g.*, 2002 VLSI Symposium Paper 2.1 by Rim et al. (Rim-2002) (discloses using HfOx on interfacial layer of oxynitride); 2002 VLSI Symposium Paper 3.3 by Harada et al. (Harada-2002) ("Interfacial layer near Si substrate with lower k where the gate electric field is high enough [3] is a key region to discuss the reliability, i.e., Tbd, β."); 2002 VLSI Symposium Paper 9.3 by Lu et al. (Lu-2002) (discloses using HfO2 on interfacial layer of nitride); 2002 VLSI Symposium Paper 9.4 by Wilk et al. (Wilk-2002) ("[T]hermal Si02 and SiOxNy, underlayers, which are typically used for high-K gate stacks . . ."); *id.* ("Chemical oxides were demonstrated to afford better control than thermal oxides/oxynitrides for achieving predictable, high-quality growth of ALD HfO2 films with low fixed charge. The appropriate combination of chemical oxide and post-annealing minimizes both fixed charge and interfacial oxide growth in ALD HfO2, and should be applicable to most high-k materials."); 2003 VLSI Symposium Paper 3A-2 by Watanabe et al. (Watanabe-2003) ("CMOSFETs with HfSiON gate dielectrics were fabricated using advanced dual gate CMOSFET process as shown in Fig. 1. HfSiO with various CHf and target Tphy were deposited by MOCVD, some on ultra thin SiO2 interfacial layer (IL)."); 2003 VLSI Symposium Paper 3A-3 by Tsai et al. (Tsai-2003) ("Chemical oxide scaling by modulating ozone concentration is used to produce SiOx interfaces with thickness as low as 0.3 nm for HfO2 dielectrics."); 2003 VLSI Symposium Paper 12A-1 by Kerber et al. (Kerber-2003) ("The mobility for the SiO2/HfO2 dual layer gate stacks is shown in Fig. 11."); 2003 VLSI Symposium Paper 12A-4 by Morioka et al. (Morioka-2003) ("The N-ch MISFETs with a HfSiO gate insulator film were fabricated. MOCVD-HfSiO films were grown on SiO2 (1nm-thick) film, formed by rapid thermal oxidation (RTO)."); 2003 VLSI Symposium Paper 12A-5 by Kim et al. (Kim-2003) ("Conventional NMOS and PMOS transistors with poly-Si gate were successfully fabricated using a novel Hf-oxide as a gate-dielectric. A

modified spacer formation scheme using a nitride layer was successfully implemented suppressing sub-SiOx layer thickening.”).

The prior art MOSFETs and MISFETs devices further disclose using a high dielectric constant gate insulating film on top of a buffer insulating film made of silicon dioxide, as recited in the Asserted Claims. *See, e.g.*, Wang ’084 at [0048] (“A layer of the high-k material of the gate dielectric 126, which may reside atop a buffer interface layer 127, is then deposited on the upper, free surface of the substrate.”); 2001 IEDM Paper to Kim et al. (Kim-2001) at Fig. 4; *id.* (“TEM micrograph of ZrO2/Poly gate stack showing 4.8nm ZrO2 sandwiched between two interfacial layers of 1.1nm each.”); Lin ’781 at [0004] (“In some cases, an ultra thin interfacial layer of less than 10 Angstroms consisting of SiO2, silicon nitride or silicon oxynitride is formed on the substrate before depositing the high k dielectric layer. The interfacial layer is used to passivate dangling bonds on the substrate surface and to prevent charge/traps in the high k dielectric layer from contacting the channel region.”); Lin ’781, at [0017] (“In a second embodiment, an interfacial layer is formed on the substrate prior to deposition of a high k gate dielectric layer and a gate layer. The interfacial layer is preferably less than 10 Angstroms thick and is comprised of SiO2, silicon nitride, or silicon oxynitride.”); Teng, at [7:36-43] (“A protective layer 26 (e.g. 2000 A of TEOS oxide, but alternatively there may be advantages to using nitride or a nitride/oxide layer structure for this layer) is deposited over the polysilicon layer 24, to protect it from later etch steps. A resist layer 28 is then patterned to define the predetermined pattern for the polysilicon layer 24 (which will provide not only gates but also gate-level interconnects).”); Katoh at [4:20-31] (“The silicon oxide film 15 shown in FIG. 2(b) is formed between the tantalum oxide film 16 and the silicon substrate 11 in order to eliminate the limitation on the temperature. This silicon oxide 15 is formed in a thickness of from 5 to 10 angstroms at the time of the anodization.”); Setton at [Abstract]

("The device includes (a) an interfacial layer formed on the substrate; (b) a high dielectric constant layer covering the interfacial layer . . . wherein the interfacial layer separates the high dielectric constant layer from the substrate."); *id.* at [3:28-55] ("The interfacial layer serves to prevent reaction of Ta2O5 in layer 110 with the silicon substrate. The interfacial layer will have a thickness that is sufficient to prevent reaction between the high dielectric constant layer and the silicon substrate and the thickness typically ranges from about 1 nm to 5 nm and preferably about 1 nm to 2 nm."); Kamata, at [0054] ("It is desired that a SiOx (0<x 2) layer or the layer containing N is interposed between the gate insulating film and the silicon substrate or between the gate insulating film and the gate electrode of poly silicon.").

Thus, a person of ordinary skill in the art would have been motivated to modify the semiconductor device or combine the device with one or more of the above prior art references to use a buffer insulating layer made of silicon dioxide in between the high dielectric constant gate insulating film and substrate. For example, it was known in the art, at the time of the alleged invention, that using a buffer insulating layer specifically made of silicon dioxide between the high dielectric constant gate insulating film and substrate would prevent reaction of the high dielectric constant gate insulating film with the substrate and improve transistor performance. *See* Setton, at [Abstract]; Lin '781, at [0017]; Teng, at [7:36-43]; Katoh at [4:20-31]; Kamata, at [0054].

Not only were high-k gate dielectrics well known and well understood in the art, but the various structures in the Asserted Claims of the '227, '764, '180, and '076 Patents were also well known. Wang '084, for example, teaches that significant benefits can be found by extending the high-k gate dielectric out to a predetermined distance from underneath the gate electrode, toward the sidewall. Wang '084 at [0043] ("Peripheral portions 200 of a high-k gate dielectric 126 extend or protrude outwardly or laterally away from and beyond a gate electrode 124 of a gate 122. As

will be described in more detail below, this structure (the high-k gate dielectric and its extending portions 200) is highly etch-resistant and prevents damage during various process steps, such as pre-epitaxy cleaning and HF treatment (oxide removal), selective etching, and epitaxial processes. This protective function of the extending portions 200 of the gate dielectric 126 ameliorates or prevents gate-electrode-to-source-extension 124-to-148 bridging and gate-electrode-to-drain-extension 124-to-150 bridging and consequent leakage currents. The extending portions 200 of the gate dielectric 126 thus act as a protective barrier, particularly between the lower edge of the gate electrode 126 and the proximate portions of source and drain upper extensions 148 and 150, during processing and fabrication of the device 100."); *id.* at [0044] ("As noted above, the protruding extension 200 of the gate dielectric 126 prevents bridging between the gate electrode 126 and the extensions 148 and 150. The extensions 148 and 150 not only extend under the protruding portions 200 of the gate dielectric 126 but also extend partially beneath the gate electrode 124."); *id.* at [0053] ("It has been found that devices having the protruding extensions 200 of the gate dielectric 126 prevent leakage currents and bridging between the gate electrode 124 and the source/drain extensions 148/150. Accordingly, the presence of the protruding extensions 200 has been found to ameliorate the short channel effect and to increase the reliability and robustness of MOSFETs having epitaxially formed extensions 148 and 150. It is theorized that the extensions 200 protect the geometry between the lower edge of the gate electrode 124 and the extensions 148 and 150 by resisting and protecting against the deleterious effects on this geometry of the etching procedures used to produce the recesses 138 a and 138 b and the effects of the epitaxy procedures used to produce the extensions 148 and 150. This protection has been found to result in no bridging from the gate electrode 124 to the source/drain extensions 148/150 and low leakage currents in completed MOSFETs having oxide-based gate dielectrics. It is theorized that prior art techniques

using only a liner/spacer 30/32 on the sides of the gate 22 and not having the protruding portions 200 permit etching and/or epitaxy procedures to attack the edges of the gate dielectric 26, ultimately resulting in lowered electrical resistance and elevated leakage current."). *See also* Clevenger at [0030] ("FIG. 3 illustrates the conversion of the gate insulator 25 to a highly conductive metallic material 90 in regions not blocked by the protective cap formed by the gate electrode 30 and sidewall spacers 50. Furthermore, a deep high doping implant source/drain region 60 is also shown embedded in the substrate 10. The conversion preferably consists of a thermal annealing process in a reducing ambient such as H2, and/or an annealing process in a vacuum to drive the oxygen out of the metal oxide film, i.e., to reduce the metal oxide. This process minimizes the overlap capacitance of the device 1."); *id.* at [0031] ("The overlap capacitance is best illustrated in FIGS. 3-6, where it is seen that the portions of the high- k dielectric 25 extending under the spacers 50 (both sides) creates an overlap in the capacitance, thereby slowing the switching effects of the device 1. In other words, if a metal were formed beneath the spacers, a capacitor structure would exist that would slow the speed at which the transistor switched. Theoretically, the overlap capacitance can be eliminated by removing all excess high-k dielectric material 25 from underneath the spacers 50, thus only having the high-k dielectric positioned underneath the gate electrode 30. However, this could possibly lead to the metallic film 90 coming into contact with the gate electrode 30, which would cause device failure. Thus, the high-k dielectric material 25 is extended below the spacers 50 as a factor of safety. However, contrary to conventional devices, the present invention reduces the overlap capacitance in the device 1 by controlling the metal conversion step (conversion of high-k dielectric material 25 to the metal oxide 90) very precisely with the cap (spacers 50 and gate 30). Thus, since the positions of the metallic and insulating portions of the layer 25 are self-aligned and precisely controlled with the cap (spacers 50 and gate

30), a capacitor is not created under the spacers 50 and overlap capacitance is avoided."); *id.* at Figs. 2-3; Teng at Fig. 6; Lin '781 at Fig. 9; Inoue at [0084] ("As a result of over etching to form the gate electrodes, the first gate insulation film 11 and the second gate insulation film 21 are made somewhat thinner except for the area underneath the gate electrodes."); Setton at Fig. 1F; Takayanagi at [0062] ("Instead of removing the unnecessary part of the Hf silicate film 5 a as explained with reference to FIG. 7, gate insulation film 23 is deposited on the whole surface of the substrate 1 as shown in FIG. 9 followed by an etching process to leave gate side-walls 23 a and 23 b on the sides of the gate electrode 6 a as is shown in FIG. 10. In this case, the Hf silicate film 5 a may be removed, but the parts that lie beneath the gate sidewalls 23 a and 23 b, may be left as is illustrated in FIG. 10.").

In particular, the prior art understood the benefits of not only extending the high-k gate film beyond the gate electrode, but it also understood that decreasing the thickness of the high-k gate film for portions underneath the sidewall provided additional benefits. For example, Takayanagi disclosed that a thicker high-k gate film under the gate electrode redistributes the electric field to the center of the gate insulating film and minimizes field concentration at the edges of the gate electrode. Takanayagi at [0065] ("In the MOSFET of FIG. 2, manufactured by the second embodiment descried with reference to FIGS. 5 to 10, the lines of electric force become dense at the center part of the gate insulating film 5 a and sparse at the edges of the film 5 a in the channel length direction when the gate voltage is applied between the gate electrode 6 a and the source/ drain regions 7 a and 7 b. Hence, the electric field is distributed to be intense at the center part of the gate insulating film 5 a. The electric field can therefore be prevented from concentrating at the edges of the gate electrode 6 a."); *see also* Inoue at [0083]-[0084] ("Then, an etching operation, Such as RIE (reactive ion etching), is performed to produce the pattern of the gate

electrode shape to form the first gate electrode 12 on the first gate insulation film 11 in the first transistor fabrication area R1 . . . As a result of over etching to form the gate electrodes, the first gate insulation film 11 and the Second gate insulation film 21 are made Somewhat thinner except for the area underneath the gate electrodes."); *id.* at [0089] ("In this way, first inner sidewall insulation film 14 is formed on both sides of the first gate electrode 12 in the first transistor fabrication area R1, and second inner sidewall insulation film 25 is formed at least on part of the Second gate insulation film 21 and on both sides of the Second gate electrode 22 in the Second transistor fabrication area R2."); Kajiyama at [0029] ("First, as shown in Fig. 1(A), . . . reactive sputtering is performed on the metal target consisting of Zr in the atmosphere of a mixture of argon gas and oxygen gas to form a ZrO2 film 2 on the Si substrate 1 that becomes a high dielectric gate insulating film, for example, at a thickness of about 5 nm. . . . and then a resist film (not shown) is RIEd to the mask to form a gate electrode 3 on the ZrO2 film 2. At this time, the ZrO2 film 2 of the base film is also etched to reduce the film as in the conventional case. Also, etch damage causes damage to the surface of ZrO2 film 2. After removing the resist membrane, gate electrode 3 is ion-implanted with, for example, arsenic to the mask to form an n-type L DD diffusion layer 4 on the surface of Si substrate 1."); *id.* at Fig. 1(A)-1(B); *id.* at [0030] ("Next, as shown in Fig. 1(B), after depositing a ZrO2 film that is reactive sputtering and becomes an insulating film over the gate electrode 3 at a film thickness of, for example, about 20 to 100 nm, RIE is performed on this ZrO2 film to form a first sidewall 5 consisting of a ZrO2 film on the side of the gate electrode 3.").

Further, a person of ordinary skill in the art would have been motivated to decrease the thickness of the high-k gate film to under 2 nm, as the prior art had already recognized benefits of making high-k gate films that small. Sim, for example, teaches that reducing the thickness of $HfO_2$ to below 20 angstroms enhances mobility and reduces charge trapping. Sim at pg. 221 ("Scaling

the physical thickness of the HfO2 dielectric to below 20Å causes less charge trapping and higher mobility."); *id.* at pg. 219 ("Even within 100µs, a 33Å HfO2 sample shows significant current reduction while a 18Å HfO2 sample is free from transient charging within the detection limits.").

Therefore, a person of ordinary skill in the art at the time of the alleged invention would have been further motivated to modify the high-k gate film identified in the cited references to extend the high-k gate film from the side surface of the gate electrode to a predetermined distance toward the sidewall and to also decrease the thickness of the film to under 2 nm because the cited references are directed at solving similar problems related to the high-k film, with similar, well-known solutions in predictable ways.

Long before the invention of the '227, '764, '180, and '076 Patents, the prior art taught a variety of sidewall structures. *See, e.g.*, Wang '084 at [0038] ("Sidewall spacers 32 on the liner 31 define the locations between the spacers 32 and the isolation regions 14 where the source 18 and the drain 20 will be formed by epitaxy. The spacers 32 may be an oxide, such as silicon oxide; a nitride, such as silicon nitride; or a composite spacer, such as oxide/nitride, nitride/oxide, oxide/nitride/oxide, or nitride/oxide/nitride"); Bu at [0026] ("In the illustrated embodiment, the layers formed on the outer surface of gate stack 20 and sidewall spacers 22 include a first sidewall-forming layer 40, a second sidewall-forming layer 42, and a third sidewall-forming layer 44."); *id.* at Fig. E; Kajiyama at Fig. 1(D); Matsumoto '185 at Fig. 32; *id.* at [0119] ("The sidewalls 41 are formed on the bottoms of the recesses 14 and in contact with the side surfaces of the sidewalls 9. The sidewalls 42 are formed on the bottoms of the recesses 14 in contact with side surfaces of the element isolation insulating films 5."). As one of several purposes, sidewalls may be used for "[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge" to optimize the amount of overlap between the

source/drain and the gate edge, which optimizes transistor performance. *See* Wolf-2002-1034 at 217. To the extent the prior art references do not disclose the exact claimed sidewall structures in the ’227, ’764, ’180, and ’076 Patents, these limitations would nevertheless be obvious to implement as a routine, trivial, and non-novel optimization of transistor performance. Using well-known techniques to create these different sidewall structures, to achieve well-known and understood benefits using routine manufacturing steps, was well within the knowledge and skill of a person of ordinary skill in the art prior to the invention of the ’227, ’764, ’180, and ’076 Patents.

As one example, claim 15 of the ’764 Patent requires two insulating sidewalls, where the second insulating sidewall has a triple layer structure, with a first oxide film, a nitride film, and a second oxide film. A person of ordinary skill in the art would have been motivated to apply a triple layer sidewall structure to other semiconductor devices, for example containing only one nitride sidewall, in light of the known benefits of sidewalls with such structures, such as preventing stress-induced degradation at oxide-nitride interfaces, mitigating dopant clustering in source/drain regions/extensions, and allowing independent control of spacer dimensions to optimize device scaling. *See* Koldiaev at [0005]-[0006], [0036]-[0043]; *id.* at Figs. 3-4; *see also* Bu at [0026] (noting that “film properties of sidewall-forming layers 40 and 42 may minimize dopant loss from source drain extension region 32 to first sidewall forming layer 40. Accordingly, parasitic resistance may be lowered.”).

Additional evidence that there would have been a motivation to combine the prior art references identified above pursuant to P.R. 3-3(a) includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution

encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art. For example, the prior art references are directed to solving the same problem. Thus, a skilled artisan seeking to solve this problem, would have looked to these cited references alone or in combination. Accordingly, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art, (4) the prior art as of the priority date is generally within the same field of endeavor, or (5) the predictable results obtained in combining the different elements of the prior art.

To the extent Plaintiff contends that any reference contains multiple distinct embodiments, it would be obvious to combine element of the distinct embodiments. A person would be motivated to make such a combination because the elements are found in the same reference and the reference as a whole is directed to the same topic or topics.

Numerous prior art references, including those identified above pursuant to P.R. 3-3(a), reflect common knowledge and the state, scope and content of the prior art before the priority dates of the Asserted Patents. *See Graham v. John Deere Co.*, 383 U.S. 1, 35-36 (1966).

Defendant is not aware of any secondary considerations supporting non-obviousness of the Asserted Claims of the ’227, ’764, ’180, and ’076 Patents. To the extent Plaintiff seeks to introduce any alleged secondary considerations in the future, Defendant reserves the right to respond at that time.

For at least the reasons described herein as well as in the exemplary combinations and the prior art claim charts found at Exhibits 227A1-A7, 227B, 764A1-A7, 764B, 180A1-A7, 180B,

076A1-A7, and 076B, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those identified above. As such, Defendant's inclusion of exemplary combinations, in view of the factors and motivations identified in the preceding paragraph, does not preclude Defendant from identifying other invalidating combinations as appropriate, or the prior art as a whole.

### C. The '686 Patent

The claim charts found below identify where each element of the Asserted Claims is found in the given prior art. Defendant fully incorporates by reference the Petition for *Inter Partes* Review No. IPR2025-00682 and the Declaration of Dr. Scott E. Thompson (Ex-1003) thereto. Defendant reserves the right to revise its claim charts to rely on any of these references to prove the invalidity of the Asserted Claims in a manner consistent with the Federal Rules of Civil Procedure, the Court's Local Rules, the Local Patent Rules and this Court's Orders.

#### 1. Prior Art Patents and Patent Applications

| Reference | Exhibit | Prior Art Date |
|---|---|---|
| U.S. Pat. App. Pub. No. 2007/0066077 to Akasaka et al. ("Akasaka '077") | 686A1 | September 20, 2006 |
| U.S. Pat. App. Pub. No. 2007/0215950 to Aoyama ("Aoyama") | 686A2 | March 19, 2007 |
| U.S. Pat. No. 7,138,323 to Kavalieros et al. ("Kavalieros '323") | 686A3 | November 21, 2006 |
| U.S. Pat. App. Pub. No. 2007/0099414 to Frohberg et al. ("Frohberg") | 686B | July 5, 2006 |
| U.S. Pat. App. Pub. No. 2007/0190767 to Nakamura et al. ("Nakamura") | 686B | February 9, 2007 |

#### 2. Prior Art Non-Patent Publications

| Primary Author or Publisher | Reference | Exhibit | Prior Art Date |
|---|---|---|---|
| Mayuzumi et al. | Extreme High-Performance n- and p-MOSFETs Boosted by Dual-Metal/High-k Gate Damascene Process using Top-Cut | 686A4 | December 10-12, 2007 |

| Primary Author or Publisher | Reference | Exhibit | Prior Art Date |
|---|---|---|---|
| | Dual Stress Liners on (100) Substrates ("Mayuzumi-2007") | | |

### 3. Prior Use or Offer for Sale

| Product | Exhibit | Date Available |
|---|---|---|
| Products Manufactured using Intel's 45nm Process | 686A5 | November 2007 |

### 4. Prior Art from *Inter Partes* Review No. IPR2025-00682

| IPR Ex. No. | Reference |
|---|---|
| Ex-1005 | U.S. Pat. Pub. No. 2007/0215950 A1 to Aoyama (Aoyama). |
| Ex-1006 | U.S. Pat. Pub. No. 2007/0235823 A1 to Hsu et al. ("Hsu '823"). |
| Ex-1007 | U.S. Patent No. 6,171,910 B2 to Hobbs et al. ("Hobbs"). |
| Ex-1008 | U.S. Pat. Pub. No. 2007/0066077 A1 to Akasaka et al. (Akasaka '077). |
| Ex-1009 | S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) (excerpted) ("Sze-1981"). |
| Ex-1010 | J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000) (excerpted) (Plummer). |
| Ex-1011 | M. Baklanov et al., *Dielectric Films for Advanced Microelectronics* (2007) (excerpted) ("Baklanov"). |
| Ex-1012 | International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) ("ITRS: FEP"). |
| Ex-1013 | International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures (2007 ed.) ("ITRS: PIDS"). |
| Ex-1014 | U.S. Pat. Pub. No. 2006/0081939 A1 to Akasaka et al. ("Akasaka '939") |
| Ex-1015 | U.S. Pat. Pub. No. 2006/0022277 A1 to Kavalieros et al. ("Kavalieros '277") |
| Ex-1016 | K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007). ("Mistry-2007") |
| Ex-1017 | K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007). ("Mistry-2007-2") |

| IPR Ex. No. | Reference |
|---|---|
| Ex-1018 | U.S. Patent No. 6,881,631 B2 to Saito et al. ("Saito '631"). |
| Ex-1019 | U.S. Patent No. 7,812,414 B2 to Hou et al. ("Hou"). |
| Ex-1020 | U.S. Pat. Pub. No. 2005/0258468 A1 to Colombo et al. ("Colombo") |
| Ex-1021 | U.S. Patent No. 6,849,511 B2 to Iriyama et al. ("Iriyama") |
| Ex-1022 | U.S. Pat. Pub. No. 2002/0037615 A1 to Matsuo. ("Matsuo") |
| Ex-1023 | S.E. Thompson et al., "A 90-nm Logic Technology Featuring Strained Silicon," IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004). ("Thompson-2004") |
| Ex-1024 | Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007). ("Sun-2007"). |
| Ex-1025 | D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-77 (2005) ("James-2005"). |
| Ex-1026 | U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al. ("Murthy '151") |
| Ex-1027 | U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al. ("Bohr") |
| Ex-1028 | P. Morin et al., "Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007) ("Morin-2007"). |
| Ex-1029 | U.S. Pat. Pub. No. 2005/0170104 A1 to Jung et al. ("Jung '104") |
| Ex-1030 | Y.C. Liu et al., "Single Stress Liner for Both NMOS and PMOS Current Enhancement By a Novel Ultimate Spacer Process," Technical Digest of the 2005 IEEE International Electron Devices Meeting (IEDM), pp. 836-39 (Dec. 2005) ("Liu-2005"). |
| Ex-1031 | U.S. Pat. Pub. No. 2008/0145984 A1 to Ke et al. ("Ke") |
| Ex-1032 | P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 $\mu m^2$ SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) ("Bai-2004"). |
| Ex-1033 | Westlinder et al., "On the Thermal Stability of Atomic Layer Deposited TiN as Gate Electrode in MOS Devices," IEEE Electron Device Letters, vol. 24, no. 9, pp. 550-552 (Sept. 2003) ("Westlinder-2003"). |
| Ex-1034 | U.S. Pat. Pub. No. 2007/0105317 A1 to Nakajima ("Nakajima"). |
| Ex-1035 | G. Eneman et al., "Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study," IEEE Transactions on Electron Devices, vol. 54, no. 6, pp. 1446-53 (June 2007) ("Eneman-2007"). |
| Ex-1036 | M. Quirk & J. Serda, *Semiconductor Manufacturing Technology*, Ch. 12: Metallization (2001) (excerpted) ("Quirk-2001"). |
| Ex-1037 | U.S. Patent No. 7,785,952 B2 to Chang et al. ("Chang"). |
| Ex-1038 | U.S. Patent No. 8,536,660 B2 to Hsu et al. ("Hsu '660"). |

| IPR Ex. No. | Reference |
|---|---|
| Ex-1039 | U.S. Patent Pub. No. 2005/0048754 A1 to Yeh et al. ("Yeh"). |
| Ex-1040 | U.S. Patent Pub. No. 2006/0001106 A1 to Metz et al. ("Metz"). |
| Ex-1041 | U.S. Patent No. 8,486,789 B2 to Okazaki et al. ("Okazaki"). |

### 5. Identification of Obviousness Combinations Pursuant to P.R. 3-3 (b) and (c)

Based upon Defendant's present understanding of the Asserted Claims, those claims are invalid as obvious in view of the following combination of prior art references. In *KSR International Co. v. Teleflex Inc.*, 500 U.S. 398 (2007), the U.S. Supreme Court rejected the Federal Circuit's rigid "teaching, suggestion, or motivation" requirement in favor of a flexible, functional approach in which an explicit finding of a "motivation" to combine prior art references is not required to establish obviousness. The Supreme Court held that it is sufficient that a combination of elements was "obvious to try" holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known option within his or her technical grasp." *Id.* at 402; *see also Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (explaining that when the "combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient," there exists a motivation to combine prior art references even when there is no explicit suggestion in the references themselves "[b]ecause the desire to enhance commercial opportunities by improving a product or process is universal—and even commonsensical"); *LeapFrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157 (Fed. Cir. 2007) (applying KSR and holding that "one of ordinary skill in the art of children's learning toys would have found it obvious to combine the Bevan device with the SSR to update it using

modern electronic components in order to gain the commonly understood benefits of such adaption, such as decreased size, increased reliability, simplified operation, and reduced cost").

The Asserted Claims are rendered obvious by the references identified in the attached claim charts, either alone or in the combinations with other prior art references as identified below or in the attached claim charts. The tables above identify prior art that anticipates each asserted claim.

Those tables, the prior art claim charts found at Exhibits 686A1-A5 and 686B, and the table below identifies prior art that by itself, or in combination with other art and/or the knowledge of one skilled in the art, renders the asserted claims obvious.

Defendant contends that all claims that are anticipated by a particular reference are also rendered obvious by that same reference alone, or in combination with the other references, discussed below. Defendant further contends that one of ordinary skill in the art, at the time of the alleged invention of the Asserted '686 Patent Claims, would have been motivated to combine the references disclosed herein in such a way to reach the alleged inventions. The teaching, suggestion, or motivation to combine these references, although not required, is explicitly or implicitly found in one or more of the following: the knowledge or common sense of one of ordinary skill in the art; the prior art references themselves and/or the prior art as a whole, including interrelated teachings of multiple prior art references; the subject matter acknowledged as prior art in the '686 Patent; the nature of the problem to be solved and the existence of similar improvements in similar applications; design incentives and other market forces, including the advantages of creating a superior and more desirable product and the effects of demands known to the design community or present in the marketplace; the ability to implement the alleged invention as a predictable variation of the prior art; improvements in similar devices; the interrelated teachings of multiple prior art references; any needs or problems known in the field addressed by the '686 Patent; and

the number of identified, predictable solutions to the problem addressed by these patents. In addition, the simultaneous (and/or prior) inventions described above, and elsewhere in these contentions, is evidence that motivation to combine the concepts described in the various prior art references did, in fact, exist, and they were, in fact, combined. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary. A person of ordinary skill would have access to the materials found in the cited and attached exhibits and would have at least the ordinary creativity and skill to combine the attached references in ways not explicitly recited above. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary,

| Primary Reference | In Combination With One or More Of |
|---|---|
| Akasaka ’077 | Aoyama, Kavalieros ’323, Frohberg, Nakamura, Mayuzumi-2007, Intel 45nm Process, Hsu ’823, Jung ’104, Murthy ’151, Morin-2007 |
| Aoyama | Akasaka ’077, Kavalieros ’323, Frohberg, Nakamura, Mayuzumi-2007, Intel 45nm Process, Hsu ’823, Jung ’104, Murthy ’151, Morin-2007 |
| Kavalieros ’323 | Akasaka ’077, Aoyama, Frohberg, Nakamura, Mayuzumi-2007, Intel 45nm Process, Hsu ’823, Jung ’104, Murthy ’151, Morin-2007 |
| Frohberg | Akasaka ’077, Aoyama, Kavalieros ’323, Nakamura, Mayuzumi-2007, Intel 45nm Process, Hsu ’823, Jung ’104, Murthy ’151, Morin-2007 |
| Nakamura | Akasaka ’077, Aoyama, Kavalieros ’323, Frohberg, Mayuzumi-2007, Intel 45nm Process, Hsu ’823, Jung ’104, Murthy ’151, Morin-2007 |
| Mayuzumi-2007 | Akasaka ’077, Aoyama, Kavalieros ’323, Frohberg, Nakamura, Intel 45nm Process, Hsu ’823, Jung ’104, Murthy ’151, Morin-2007 |
| Intel 45nm Process | Akasaka ’077, Aoyama, Kavalieros ’323, Frohberg, Nakamura, Mayuzumi-2007, Hsu ’823, Jung ’104, Murthy ’151, Morin-2007 |

Defendant hereby identifies additional motivation and reasons to combine the cited art: One of ordinary skill in the art would be motivated to combine these references in the above combinations for at least the following reasons. One of skill in the art would have been motivated to combine these references, because these references relate to common objectives and subject matter. It was well known prior to the invention of the ’686 Patent the dual metal gates in PMOS and NMOS transistors on high-k gate dielectrics provided significant benefits as gate thicknesses became smaller and smaller. *See e.g.*, 2002 VLSI Symposium Paper 3.2 by Samavedam et al. (Samavedam-2002) (“Metal gates will eliminate gate depletion and address other issues like boron penetration and increased gate resistance, which will be aggravated as the poly gate thickness is scaled down.”); *id.* (“We have successfully fabricated and characterized HfO2 n-MOSFETs with TaSiN and PVD TIN gates and p-MOSFETs with CVD and PVD TiN gates using a conventional CMOS process. Metal-gated HfO2 n-MOSFETs show a 10^4X gate leakage reduction compared to poly/SiO2 devices. Reasonable Ion/Ioff performance and reliability were observed in PVD TiN/HfO2 PMOS.”); 2002 VLSI Symposium Paper VLSI 9.1 by Lee et al. (Lee-2002) (“As CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns. Therefore, metal gate electrodes are being explored to replace the polysilicon gate.”); 2004 VLSI Symposium Paper 5.3 by Weber et al. (Weber-2004) (“For the first time, MOS transistors with compressively strained SiGe(:C) channel, metal gate and high-k dielectric are demonstrated down to 55nm gate length. SiGe(:C) surface channel pMOSFETs with HfO2 gate dielectric exhibit a 10^4 gate leakage reduction and a 65% mobility enhancement at high transverse effective field (1MV/cm) when compared to the universal SiO2/Si reference.”).

In particular, the prior art of record also describes the benefits provided by dual metal gates on top of high k dielectrics. *See e.g.*, Kavalieros ’323 at 1:20-27 (“Because such a high-k dielectric

layer may not be compatible with polysilicon, it may be desirable to use metal gate electrodes in devices that include high-k gate dielectrics. When making a CMOS device that includes metal gate electrodes, it may be necessary to make the NMOS and PMOS gate electrodes from different materials. A replacement gate process may be used to form gate electrodes from different metals."); Aoyama at [0006] ("For example, a CMOSFET for the 45 nm technology node or beyond requires performance, equivalent to that of a gate dielectric film with an equivalent oxide thickness of 1.3 nm or less. However, it is difficult to achieve such performance by thinning a silicon oxide film or silicon oxynitride film. For this reason, there has been proposed a method, thinning a gate dielectric film while suppressing an increase in leakage current, by adopting, as the gate dielectric film, a metal dielectric film with a higher permittivity than a silicon oxide film or silicon oxynitride film (high-permittivity gate dielectric film). Examples of the metal dielectric film include a metal oxide film, metal oxynitride film, metal silicate film, metal silicon oxynitride film, and the like."); *id.* at [0009] ("For this reason, there has been proposed a method, suppressing a shift in the threshold voltage of a PMOSFET and increasing the inversion capacitance of the PMOSFET, by adopting a metal gate electrode as a gate electrode of a CMOSFET when a high-permittivity gate dielectric film is adopted as a gate dielectric film of the CMOSFET."); Akasaka '077 at [0005] ("In recent years, owing to the demands of increased miniaturization, CMOS (Complementary Metal Oxide Semiconductor) transistors comprising MISFETs having a dual metal gate structure have attracted attentions."); Mayuzumi-2007 at Introduction ("Metal/high-k gate stacks have been recently investigated for Tinv scaling and gate-leakage-current reduction. The gate-last damascene process having band-edge work-function dual-metal is one of the great candidates to achieve high-performance MOSFETs.").

Therefore, a person of ordinary skill in the art at the time of the alleged invention would have been motivated to modify the dual metal gate structures identified in the references above with other structures found in other references disclosing dual metal gate structures. The references are directed at solving similar problems with similar, well-known solutions in predictable ways.

It was also well known prior to the invention of the ’686 Patent that a stress-inducing silicon nitride film over the p- and n- channel regions improve electron mobility. *See e.g.*, Hsu ’823 at [0002] (“The performance of a MOS device can be enhanced through a stressed-surface channel.”); *id.* at [0039] (“the performance of PMOS devices can be easily improved . . . , while the performance of NMOS devices is relatively difficult to improve”); Murthy ’151 at [0005] (“For n-MOS devices, carrier mobility (i.e. electron mobility) is enhanced by generating a tensile strain in the transistor’s channel region.”); Liu-2005 at 1-2 (“[T]he same tensile capping layer (stress: 1GPa; thickness: 700A) was applied to both [the] USP and tensile-CESL process[es] . . . . Significant drive current enhancement of both N/PMOS is achieved with insertion of this USP in standard CMOS flow.”); *id.* at Tbls. I-II, Figs. 1-7; Thompson-2004 (“A tensile silicon nitride-capping layer is used to introduce tensile strain into the n-type MOSFET and enhance electron mobility by 20%.”); *id.* (“Contrary to hole mobility enhancement with stress, the theoretical understanding for electron mobility enhancement for bi-axial and uniaxial tensile stress is well developed.”); *id.* at Fig. 5(c); Jung ’104 (“Table V shows the deposition conditions for silicon nitride films which were deposited under conditions which provided tensile stress films.”); *id.* at Tbl. V.

It was further well known in the prior art that stress-inducing silicon nitride film may be a contact etch stop layer. *See e.g.*, Morin-2007 (“As a result, in these technologies, process induced

stress engineering is dedicated to electron mobility enhancement, so by using tensile nitride as CESL.");;; Bohr at [0038]-[0039]; *id.* at Fig. 6.

Further, before the invention of the '686 Patent, the state of the art had already disclosed using both compressive and tensile stress contact etch stop layers (CESLs) over the PMOS and NMOS devices to induce the desired strain. *See e.g.*, James at 2,4; Morin-2007 at 355-56, 367; Hsu '823 at [0003]; Jung '104 at Abstract; *id.* at [0090] ("[A] stress-tuned silicon nitride film can be deposited . . . to provide an etch stop layer"). CESL's were commonly made of silicon nitride before the invention of the '686 Patent. *See e.g.*, Hsu '823 [0003]; Ke at [0003] ("A commonly used method for applying stress to the channel region is forming a stressed contact etch stop layer (CESL) on a MOS device."); Jung '104 at [0090] ("In addition to being deposited as part of a structure to control electron mobility, . . . a stress-tuned silicon nitride film can be deposited for other purposes in various steps in the fabrication process, for example (and not by way of limitation), to provide an etch stop layer . . . , as well as to enhance channel mobility in various portions of the device structure."); Morin-2007 at 355-56. The CESL may provide tensile stress, compressive stress, or no stress, depending on how it is formed. *See e.g.*, Jung '104 at [0017]; *id.* at [0090]; *id.* at [0099]-[0100]; *id.* at [0131]-[0132]; *id.* at Tbls. IV-V, VII and Fig. 15.

A person of ordinary skill in the art at the time of the alleged invention would have been motivated to modify the silicon nitride etch stopper films, for example as taught by Aoyama, Akasaka '077, and other cited references, to cause a stress in the channel region, as disclosed in the prior art, to improve the electron mobility of the device. A person of ordinary skill in the art would have reasonably expected success by modifying the silicon nitride etch stopper films to cause a stress in the gate length direction because the references are directed at the same structure,

the silicon nitride etch stop layer, and solve similar problems with similar, well-known solutions in predictable ways.

Additional evidence that there would have been a motivation to combine the prior art references identified above pursuant to P.R. 3-3(a) includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art. For example, the prior art references are directed to solving the same problem. Thus, a skilled artisan seeking to solve this problem, would have looked to these cited references alone or in combination. Accordingly, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art, (4) the prior art as of the priority date is generally within the same field of endeavor, or (5) the predictable results obtained in combining the different elements of the prior art.

To the extent Plaintiff contends that any reference contains multiple distinct embodiments, it would be obvious to combine element of the distinct embodiments. A person would be motivated to make such a combination because the elements are found in the same reference and the reference as a whole is directed to the same topic or topics.

Numerous prior art references, including those identified above pursuant to P.R. 3-3(a), reflect common knowledge and the state, scope and content of the prior art before the priority dates of the Asserted Patents. *See Graham v. John Deere Co.*, 383 U.S. 1, 35-36 (1966).

Defendant is not aware of any secondary considerations supporting non-obviousness of the Asserted Claims of the ’686 Patent. To the extent Plaintiff seeks to introduce any alleged secondary considerations in the future, Defendant reserves the right to respond at that time.

For at least the reasons described herein as well as in the exemplary combinations and the prior art claim charts found at Exhibits 686A1-A5 and 686B, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those identified above. As such, Defendant’s inclusion of exemplary combinations, in view of the factors and motivations identified in the preceding paragraph, does not preclude Defendant from identifying other invalidating combinations as appropriate, or the prior art as a whole.

### D. The ’779 Patent

The claim charts found below identify where each element of the Asserted Claims is found in the given prior art. Defendant fully incorporates by reference the Petition for *Inter Partes* Review No. IPR2025-00832 and the Declaration of Jakub Kedzierski, Ph.D. (Ex-1003) thereto. Defendant reserves the right to revise its claim charts to rely on any of these references to prove the invalidity of the Asserted Claims in a manner consistent with the Federal Rules of Civil Procedure, the Court’s Local Rules, the Local Patent Rules and this Court’s Orders.

#### 1. Prior Art Patents and Patent Applications

| Reference | Exhibit. | Prior Art Date |
|---|---|---|
| U.S. Pat. App. Pub. No. 2005/0014352 to Torii et al. (“Torii”) | 779A1 | January 20, 2005 |
| U.S. Pat. App. Pub. No. 2010/0167482 to Mori et al. (“Mori”) | 779A2 | December 23, 2009 |
| U.S. Pat. App. Pub. No. 2004/0188769 to Tsuno (“Tsuno”) | 779B | September 30, 2004 |
| U.S. Pat. App. Pub. No. 2009/0039445 to Wu (“Wu ’445”) | 779B | February 12, 2009 |
| U.S. Pat. No. 6,946,709 to Yang (“Yang”) | 779B | September 20, 2005 |

| Reference | Exhibit. | Prior Art Date |
|---|---|---|
| U.S. Pat. No. 7,335,561 to Sakai ("Sakai '561") | 779B | February 26, 2008 |
| U.S. Pat. No. 6,787,421 to Gilmer et al. ("Gilmer") | 779B | September 7, 2004 |
| U.S. Pat. No. 8,349,695 to Scheiper et al. ("Scheiper") | 779B | August 2, 2010 |
| Japanese Patent App. Pub. No. JP2006/060155 to Yasuhira et al. ("Yasuhira") | 779B | March 2, 2006 |
| Japanese Patent App. Pub. No. JP2003/100896 to Fujiwara et al. ("Fujiwara") | 779B | April 4, 2003 |

### 2. Prior Art from *Inter Partes* Review No. IPR2025-00832

| IPR Ex. No. | Reference |
|---|---|
| 1005 | U.S. Patent 6,881,657 to Torii, et al. (Torii) |
| 1006 | U.S. Patent Publication 2010/0258878 to Mise, et al. ("Mise") |
| 1007 | U.S. Patent 8,114,739 to Chowdhury, et al. ("Chowdhury") |
| 1008 | U.S. Patent 6,693,333 to Yu ("Yu '333") |
| 1009 | U.S. Patent 6,787,421 to Gilmer, et al. (Gilmer) |
| 1010 | U.S. Patent 7,382,023 to Chen ("Chen '023") |
| 1011 | Van Zant, "Microchip Fabrication" (Fifth Edition, 2004) ("Van Zant-2004") |
| 1012 | Weste, "CMOS VLSI Design: A Circuits and Systems Perspective" (Third Edition, 2005) (Weste) |
| 1013 | Houssa, M., "High-k Dielectrics" to Houssa (IOP Publishing Ltd. 2004) ("Houssa-2004") |
| 1014 | Wolf, "Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology" (2002) ("Wolf-2002-1014") |
| 1015 | Plummer, J., et al., "Silicon VLSI Technology: Fundamentals, Practice and Modeling" (Prentice Hall 2000) (Plummer) |
| 1016 | "International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures" (2007 Edition) (ITRS: PIDS) |
| 1017 | Campbell, "The Science and Engineering of Microelectronic Fabrication" (Second Edition, 2001) (Campbell) |
| 1018 | Chau, "Advanced Metal Gate/High-K Dielectric Stacks" ("Chau") |
| 1019 | Guha, et al. "Examination of flatband and threshold voltage tuning of HfO2/TiN field effect transistors by dielectric cap layers", Applied Physics Letters (March 1, 2007) ("Guha-2007") |
| 1020 | H.-J. Li and M. Gardner, "Dual high-k gate dielectric with poly gate electrode: HfSiON on nMOS and Al2O3 capping layer on pMOS," IEEE Electron Device Lett., vol. 26, no. 7, pp. 441-443, 2005. ("Li/Gardner") |
| 1021 | U.S. Patent 7,807,990 to Koyama (Koyama '990) |
| 1022 | U.S. Publication 2006/0244035 to Bojarczuk, JR, et al. ("Bojarczuk") |

| IPR Ex. No. | Reference |
|---|---|
| 1023 | "Semiconductor Devices: Physics and Technology" by Sze (Second Edition, 2002) ("Sze-2002") |
| 1024 | Lee, S. J., et al. "High Quality Ultra Thin CVD HfO2 Gate Stack with Poly-Si Gate Electrode," Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (Lee-2000) |
| 1025 | Lee, B.H., et al., "Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (Lee-1999) |
| 1026 | U.S. Patent 7,709,331 to Karve, et al. ("Karve") |
| 1027 | U.S. Patent 8,017,469 to Luo, et al. ("Luo") |
| 1029 | Wolf, "Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET" (1995) ("Wolf-3") |
| 1030 | Translated Excerpts from File History of JP2010-205599 |
| 1031 | U.S. Patent 8,384,160 to Onishi, et al. ("Onishi '160") |
| 1032 | "An Adjustable Work Function Technology Using Mo Gate for CMOS Devices", Lin, et al., IEEE Electron Device Letters, Vol. 23, No. 1, January 2002 ("Lin-2002") |
| 1033 | "Dual Work Function Metal Gate CMOS Transistors by Ni-Ti Interdiffusion", Polishchuk, et al., IEEE Electron Device Letters, Vol. 23, No. 4, April 2002 ("Polishchuk-2002") |

### 3. Identification of Obviousness Combinations Pursuant to P.R. 3-3 (b) and (c)

Based upon Defendant's present understanding of the Asserted Claims, those claims are invalid as obvious in view of the following combination of prior art references. In *KSR International Co. v. Teleflex Inc.*, 500 U.S. 398 (2007), the U.S. Supreme Court rejected the Federal Circuit's rigid "teaching, suggestion, or motivation" requirement in favor of a flexible, functional approach in which an explicit finding of a "motivation" to combine prior art references is not required to establish obviousness. The Supreme Court held that it is sufficient that a combination of elements was "obvious to try" holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known option within his or her technical grasp." *Id.* at 402; *see also Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d

1356, 1368 (Fed. Cir. 2006) (explaining that when the "combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient," there exists a motivation to combine prior art references even when there is no explicit suggestion in the references themselves "[b]ecause the desire to enhance commercial opportunities by improving a product or process is universal—and even commonsensical"); *LeapFrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157 (Fed. Cir. 2007) (applying KSR and holding that "one of ordinary skill in the art of children's learning toys would have found it obvious to combine the Bevan device with the SSR to update it using modern electronic components in order to gain the commonly understood benefits of such adaption, such as decreased size, increased reliability, simplified operation, and reduced cost").

The Asserted Claims are rendered obvious by the references identified in the attached claim charts, either alone or in the combinations with other prior art references as identified below or in the attached claim charts. The tables above identify prior art that anticipates each asserted claim.

Those tables, the prior art claim charts found at Exhibits 779A1-A2 and 779B, or in combination with other art and/or the knowledge of one skilled in the art, renders the asserted claims obvious.

Defendant contends that all claims that are anticipated by a particular reference are also rendered obvious by that same reference alone, or in combination with the other references, discussed below. Defendant further contends that one of ordinary skill in the art, at the time of the alleged invention of the Asserted '779 Patent Claims, would have been motivated to combine the references disclosed herein in such a way to reach the alleged inventions. The teaching, suggestion, or motivation to combine these references, although not required, is explicitly or implicitly found in one or more of the following: the knowledge or common sense of one of ordinary skill in the

art; the prior art references themselves and/or the prior art as a whole, including interrelated teachings of multiple prior art references; the subject matter acknowledged as prior art in the ’779 Patent; the nature of the problem to be solved and the existence of similar improvements in similar applications; design incentives and other market forces, including the advantages of creating a superior and more desirable product and the effects of demands known to the design community or present in the marketplace; the ability to implement the alleged invention as a predictable variation of the prior art; improvements in similar devices; the interrelated teachings of multiple prior art references; any needs or problems known in the field addressed by the ’779 Patent; and the number of identified, predictable solutions to the problem addressed by these patents. In addition, the simultaneous (and/or prior) inventions described above, and elsewhere in these contentions, is evidence that motivation to combine the concepts described in the various prior art references did, in fact, exist, and they were, in fact, combined. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary. A person of ordinary skill would have access to the materials found in the cited and attached exhibits and would have at least the ordinary creativity and skill to combine the attached references in ways not explicitly recited above. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary,

| Primary Reference | In Combination With One or More Of |
|---|---|
| Torii | Mori, Wu ’445, Tsuno, Yang, Chen ’023, Sakai ’561, Gilmer, Yasuhira, Fujiwara, Scheiper |
| Mori | Torii, Wu ’445, Tsuno, Yang, Chen ’023, Sakai ’561, Gilmer, Yasuhira, Fujiwara, Scheiper |
| Sakai ’561 | Mori, Torii, Wu ’445, Tsuno, Yang, Chen ’023, Gilmer, Yasuhira, Fujiwara, Scheiper |
| Gilmer | Mori, Torii, Wu ’445, Tsuno, Yang, Chen ’023, Sakai ’561, Yasuhira, Fujiwara, Scheiper |

| Primary Reference | In Combination With One or More Of |
|---|---|
| Yasuhira | Mori, Torii, Wu ’445, Tsuno, Yang, Chen ’023, Sakai ’561, Gilmer, Fujiwara, Scheiper |
| Fujiwara | Mori, Torii, Wu ’445, Tsuno, Yang, Chen ’023, Sakai ’561, Gilmer, Yasuhira, Scheiper |
| Scheiper | Mori, Torii, Wu ’445, Tsuno, Yang, Chen ’023, Sakai ’561, Gilmer, Yasuhira, Fujiwara, |

Defendant hereby identifies additional motivation and reasons to combine the Torii sidewall structures with the remaining primary references: One of ordinary skill in the art would be motivated to combine the Torii reference for at least the following reasons. One of skill in the art would have been motivated to combine these references, because these references relate to common objectives and subject matter. The identified prior art references relate to common objectives and share commonalities in terms of their general subject matter as well as the types of equipment, products, and approaches used, including their descriptions of semiconductor devices (e.g., field-effect transistors, such as MOSFETs and MISFETs, CMOS, and I/O circuits). *See, e.g.*, Torii at [0019-0020]; Mori at [0009]; Gilmer 1:13-32; Sakai ’561 at 1:16-31; Fujiwara at [0001]; Wu ’445 at [0016]; Tsuno at [0003]; Yang at [Abstract].

Further, the Asserted Claims of the ’779 Patent contains merely a duplication of concepts known in the prior art and have no patentable significance given that no unexpected results occur (i.e., the patentee merely combines known prior art elements according to known methods to yield predictable results). For example, the prior art references describe well-known semiconductor devices (e.g., field-effect transistors, such as MOSFETs and MISFETs), their structures and fabrication processes, including the common use of multi-layer gate insulating films of different thicknesses, high dielectric constant insulating films, sidewalls, the process of forming films of various thicknesses, the formation of active regions, and the process of refining films (such as anisotropic etching). *See, e.g.*, Torii at [0034-0039]; Mori at [0099-0105]; *id.* at [0111]; Gilmer at

1:13-32; *id.* at 2:315-34; Sakai ’561 at 1:16-31; *id.* at 2:33-53; Fujiwara at [0001]; Yasuhira (“The present invention relates to a semiconductor device and a method of manufacturing the same, and more specifically, an insulated gate field effect transistor having a plurality of types of gate insulating films made of a high dielectric constant insulating film (High-k film) formed on the semiconductor device (MISFET) and a method for forming the same on a semiconductor substrate.”).

Further, the prior art of record confirms that it was well-known to form sidewalls using various sidewall processing techniques. The prior art of records discloses various sidewall structures in its semiconductor devices. *See, e.g.*, Torii at [0037] (“On the sidewalls of each gate electrode 32 and the underlying gate insulating film, side wall spacers 36 and 38 are formed.”), [0034-0039]; Mori at [0111] (“Sidewall insulating films 20 are formed on sidewalls of the gate structures 16 using a sidewall processing technique.”); *id.* at [0052-0054]; Fujiwara at Fig. 11; Yasuhira (“Then, a sidewall insulating film 10 made of a silicon oxide film or a silicon nitride film is formed by a well-known method”); Sakai ’561 at 3:4-8 (“forming a first side wall insulation film on the side wall of the first conductive piece and a second side wall insulation film on the side wall of the second conductive piece by anisotropic etching the third insulation film”).

In particular, it was well known prior to the invention of the ’779 Patent that having transistors of different work functions on a single chip, known as system on chip (SOC) devices, is advantageous because it provided greater functionality in the single device and ease of manufacturing. *See e.g.*, ’779 Patent at 3:41-45 (“Accordingly, in a semiconductor integrated circuit device requiring two or more threshold voltages, gate structures having different work functions need to be formed in a single chip in order to maximize a transistor driving force at each threshold voltage.”); Torii at [0004] (“Therefore, an integrated-circuit device referred to as SoC

(System on chip) that can individually realize functions conventionally realized using a plurality of element has been widely used."); Wu '445 at [0003] ("With increasing demands for embedded memory type structures, mixed-signal circuits, and system on chip (SOC) IC design, it has become necessary to form multiple transistor structures on a single die to achieve integrated functioning of the different transistor structures."); Wu '445 at [0005] ("In addition, there is an increasing demand for integrating mixed signal (i.e., digital/analog) functions on a single chip, e.g., system on chip (SOC devices, thereby requiring the formation of different types of transistors.). Forming different gate structures to achieve different work functions on a single chip requires too many steps, which in turn, increases production costs. *See e.g.*, '779 Patent at 4:55-64 ("To achieve the object, the inventors of the present application studied methods for forming gate structures (a gate structure includes a stack of a gate insulating film and a gate electrode) having different work functions. . . . However, these methods were found not to be practical because they consisted of significantly increased number of steps."); Wu '445 at [0007] ("Methods for dealing with the different processing requirements in forming different types of transistors (i.e. analog and digital) on a single chip, e.g., SOC devices, have focused on separate processes carried out for each type of transistor. Such prior art approaches lead to higher costs and process incompatibility which detrimentally impacts the performance and reliability of both transistor types.").

Further, the prior art demonstrates that it was well known prior to the invention of the '779 Patent that different thicknesses of gate insulating films can achieve those different work functions. *See e.g.*, '779 Patent at 4:65-5:3 ("As a result of further studies, the inventors have found the following. Thus, gate structures are allowed to have different work functions by increasing the thickness of an interface layer constituting the lowest layer of a gate insulating film by means of selective oxidation which is performed after formation of the gate structures."); Torii at [0007]

("When a logic circuit portion and a peripheral circuit portion are formed in a semiconductor device, the gate insulating films of the different thickness require to be formed in these circuit portions on a Substrate. One of the methods for forming gate insulating films of different thickness is as follows:"); *id.* at [0011]-[0012] ("Therefore, in order to produce finer elements and reduce power consumption, the use of a high-dielectric constant film (hereafter referred to as high-k film) as a gate insulating film has been studied. The high-k film can be formed thicker than the silicon oxide film, while maintaining the effective film thickness that determines the transistor current Sufficiently thin, and can inhibit the increase of power consumption. As such an SoC, there has been proposed a semiconductor device that uses a high-k film as the gate insulating film of an MISFET (metal insulator semiconductor field effect transistor) for the logic circuit, and a thick silicon oxide film and a high-k film as the gate insulating film for the peripheral circuit."); *id.* at Fig. 9; Mori at [Abstract] ("The method forms two types of field-effect transistors including gate insulating films having different film thickness in a first region and a second region on a silicon Substrate, respectively"); *id.* at [0009] ("According to a first aspect of the invention, there is provided a method of manufacturing a semiconductor device in which two types of field-effect transistors that include gate insulating films having different film thickness are formed in a first region and a second region on a silicon substrate, respectively, and that includes the following."); *id.* at Fig. 10; *id.* at [0068] ("By varying the film thicknesses of gate insulating films, MOSFETs that differ in operating voltage can be obtained. For example, it is considered that three types of MOSFETs that include gate insulating films having different film thickness are formed on a semiconductor substrate by this multi-oxide process."); *id.* at [0070]-[0071] ("The MOSFET in the LV region is suitable for low power consumption and high-speed operation. . . . On the other hand, the MOSFET in the MV region is suitable for applications in which the operating voltage

and the drive current are large. Based on such characteristics of the MOSFETs, the HV region includes, for example, an interface unit with an outer circuit, and the LV region includes, for example, a core unit of an LSI."); Gilmer at [Abstract] ("A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22)."); Wu '445 at [0021] ("In an important aspect of the invention, the SiO, layer formed over the gate structures are formed to have a differential thickness. For example, in the embodiment shown, SiO, layer portion 20B, grown over the area subjected to the fluorine ion implant including gate structure 12B, is formed have a relatively greater thickness compared to SiO, layer portion 20A grown over the photoresist covered area including gate structure 12A. The differential thickness is advantageously formed as a result of the oxide growth rate enhancing fluorine ion implantation over the gate structure 12B and adjacent Substrate portions.").

Even further, the prior art of record also describes the benefits provided by high-k dielectric films on top of the gate insulating films of different thicknesses. *See e.g.*, Torii at [0019] ("Each of the first gate insulating film and the Second gate insulating film includes a Silicon oxynitride film and a high-dielectric constant film. The equivalent-oxide thickness of the first gate insulating film is thicker than the equivalent-oxide thickness of the Second gate insulating film. The high dielectric-constant film in the first gate insulating film has the same thickness as the high-dielectric-constant film in the second gate insulating film."); Mori at Fig. 1O; Gilmer at 2:14-17 ("The present invention integrates a high-k dielectric material, preferably a metal oxide, in a dual gate process sequence using a single metal oxide deposition to form multiple gate dielectric Stacks

of differing thicknesses."); Wu '445 at [0012] ("In a first embodiment, the method includes providing a semiconductor Substrate including at least two gate structures; growing a silicon oxide layer having a respective differential thickness over the at least two gate structures: forming a dielectric layer on the silicon oxide layer having an etching selectivity with respect to the silicon oxide layer;") *id.* at [0018] ("It will be appreciated that the high-K dielectric layer may include a lowermost interfacial layer formed on the semiconductor substrate such as an oxide or oxynitride (not shown).")

Defendant hereby identifies additional motivation and reasons to combine the cited references with the insulating sidewall spacers of differential thicknesses as disclosed in Wu '445. First, one of skill in the art would have been motivated to combine Wu '445 with the cited references, because these references relate to common objectives, namely, optimization of transistors of different functions on SOC devices. *See e.g.*, Mori at [0069]-[0070]; *id.* at Fig. 1O; Torii at Fig. 9; *id.* at [0014] ("In such SoC carrying an MISFET for LOP, an MISFET for LSTP, and an MISFET for a high withstand Voltage in one chip, the thickness of the gate insulating films in these MISFETS is different from each other."); Wu '445 at [0003] ("With increasing demands for embedded memory type structures, mixed-signal circuits, and system on chip (SOC) IC design, it has become necessary to form multiple transistor structures on a single die to achieve integrated functioning of the different transistor structures. For example, transistors with different structures and functions typically operate under different current and voltage parameters requiring different LDD widths and depths for the various transistors."); *id.* at [0005] ("In addition, there is an increasing demand for integrating mixed signal (i.e., digital/analog) functions on a single chip, e.g., system on chip (SOC devices, thereby requiring the formation of different types of transistors. Problematically, transistors for analog circuits have significantly different operating and

processing requirements compared to transistors for digital or logic circuits."); *id.* at [0012] ("In a first embodiment, the method includes providing a semiconductor Substrate including at least two gate structures; growing a silicon oxide layer having a respective differential thickness over the at least two gate structures: forming a dielectric layer on the silicon oxide layer having an etching selectivity with respect to the silicon oxide layer; forming offset spacers having a differential thickness including the dielectric layer and the silicon oxide layer adjacent either side of the at least two respective gate structures; and, carrying out anion implant process adjacent the offset spacers to form doped regions in the semiconductor substrate forming at least two MOSFET devices."). This is the same problem the '779 Patent is aimed to solving. *See* '779 Patent at 3:41-45 ("Accordingly, in a semiconductor integrated circuit device requiring two or more threshold voltages, gate structures having different work functions need to be formed in a single chip in order to maximize a transistor driving force at each threshold voltage."); *id.* at 6:39-43 ("Therefore, the present disclosure is useful as a semiconductor device having a CMIS structure including a plurality of MIS transistors different in threshold voltage (Vth), and for fabricating the semiconductor device.")

It was well known prior to the invention of the '779 Patent that differing the thicknesses of the insulating sidewall spacers provided significant benefits to SOC devices. *See e.g.*,Wu '445 at [0003]; *id.* at [0007] ("Methods for dealing with the different processing requirements in forming different types of transistors (i.e. analog and digital) on a single chip, e.g., SOC devices, have focused on separate processes carried out for each type of transistor. Such prior art approaches lead to higher costs and process incompatibility which detrimentally impacts the performance and reliability of both transistor types."); *id.* at [0008] ("There is therefore a need in the semiconductor device integrated circuit manufacturing art for an improved mixed signal device and method for

forming the same such that digital and analog CMOS devices may be more effectively individually optimized for performance and reliability in parallel production processes, including forming system on chip (SOC) devices."); *id.* at [0009] ("It is therefore an object of the present invention to provide an improved mixed signal device and methods for forming the same Such that digital and analog CMOS devices may be more effectively individually optimized for performance and reliability in parallel production processes, including forming system on chip (SOC) devices, as well as overcoming other shortcomings of the prior art."); *id.* at [0012] ("growing a silicon oxide layer having a respective differential thickness over the at least two gate structures"); *id.* at [0026] ("It will additionally be appreciated that the MOSFET devices formed comprising the differential width offset spacers form MOSFET devices having operationally distinguishable characteristics, e.g., drive current, Voltage threshold (VT), short channel effects (SCE), and the like."); *id.* at [0029] ("It will additionally be appreciated that the dual off set spacer widths may be used to form logic and SRAM devices, for example the relatively thicker offset spacer width forming a portion of SRAM transistors and the relatively thinner offset spacer widths forming a portion of logic transistors. In addition, dual spacer widths may be used to form an NMOS SRAM cell transistor (relatively thicker offset spacer width) and a PMOS SRAM cell transistor (relatively thinner offset spacer width)."); *id.* at [0031] ("Thus, MOSFET devices having differentially wide offset spacers and associated ion implanted (doped) regions forming operationally distinguishable devices and a method for forming the same has been presented such that a cost effective way for forming respective ion implants to form doped regions adjacent gate structures can be accomplished with a minimal number of steps and be optimized for formation of different MOSFET devices in parallel. For example, analog/digital, logic/SRAM, and SRAM PMOS/NMOS MOSFET devices may be formed in parallel processes with a reduced number of processing steps on a single chip,

including in a system on chip (SOC) implementation. Advantageously, analog devices having a thicker offset spacer width may be formed with doped regions optimized for Voltage threshold matching and Voltage gain while the thinner offset spacer width may be formed with doped regions being optimized for reducing SCE effects and increasing drive current.”).

Therefore, a person of ordinary skill in the art at the time of the alleged invention would have been motivated to modify the gate insulating film structures identified in the cited references with other insulating sidewall spacer structure disclosed in Wu ’445. The references are directed at solving similar problems with similar, well-known solutions in predictable ways.

Additional evidence that there would have been a motivation to combine the prior art references identified above pursuant to P.R. 3-3(a) includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art. For example, the prior art references are directed to solving the same problem. Thus, a skilled artisan seeking to solve this problem, would have looked to these cited references alone or in combination. Accordingly, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art, (4) the prior art as of the priority date is generally within the same field of endeavor, or (5) the predictable results obtained in combining the different elements of the prior art.

To the extent Plaintiff contends that any reference contains multiple distinct embodiments, it would be obvious to combine element of the distinct embodiments. A person would be motivated to make such a combination because the elements are found in the same reference and the reference as a whole is directed to the same topic or topics.

Numerous prior art references, including those identified above pursuant to P.R. 3-3(a), reflect common knowledge and the state, scope and content of the prior art before the priority dates of the Asserted Patents. *See Graham v. John Deere Co.*, 383 U.S. 1, 35-36 (1966).

Defendant is not aware of any secondary considerations supporting non-obviousness of the Asserted Claims of the '779 Patent. To the extent Plaintiff seeks to introduce any alleged secondary considerations in the future, Defendant reserves the right to respond at that time.

For at least the reasons described herein as well as in the exemplary combinations and the prior art claim charts found at Exhibits 779A1-A2 and 779B, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those identified above. As such, Defendant's inclusion of exemplary combinations, in view of the factors and motivations identified in the preceding paragraph, does not preclude Defendant from identifying other invalidating combinations as appropriate, or the prior art as a whole.

**E. The '425 Patent**

The claim charts found below identify where each element of the Asserted Claims is found in the given prior art. Defendant fully incorporates by reference the Petition for *Inter Partes* Review No. IPR2025-00683 and the Declaration of Scott E. Thompson, Ph.D. (Ex-1003) thereto. Defendant reserves the right to revise its claim charts to rely on any of these references to prove the invalidity of the Asserted Claims in a manner consistent with the Federal Rules of Civil Procedure, the Court's Local Rules, the Local Patent Rules and this Court's Orders.

### 1. Prior Art Patents and Patent Applications

| Reference | Exhibit | Prior Art Date |
|---|---|---|
| U.S. Pat. App. Pub. No. 2009/0032844 to Ogura et al. ("Ogura") | 425A1 | July 29, 2008 |
| U.S. Pat. App. Pub. No. 2009/0085123 to Sato ("Sato") | 425A2 | September 16, 2008 |
| U.S. Pat. App. Pub. No. 2007/0126036 to Ohta et al. ("Ohta") | 425A3 | June 7, 2007 |
| U.S. Pat. App. Pub. No. 2006/0202278 to Shima et al. ("Shima") | 425A4 | September 14, 2006 |
| U.S. Pat. App. Pub. No. 2009/0242995 to Suzuki et al. ("Suzuki '995") | 425B | June 11, 2009 |
| U.S. Pat. No. 6,720,601 to Terauchi et al. ("Terauchi") | 425B | April 13, 2004 |
| U.S. Pat. App. Pub. No. 2009/0246922 to Wu et al. ("Wu '922") | 425B | March 27, 2008 |
| U.S. Pat. App. Pub. No. 2007/0249069 to Alvarez et al. ("Alvarez") | 425B | October 25, 2007 |

### 2. Prior Use or Offer for Sale

| Product | Exhibit/Bates No. | Date Available |
|---|---|---|
| Products Manufactured using Intel's 65nm Process ("Intel 65nm Process") | 425A5 | January 2006 |
| Products Manufactured using UMC's 40nm Process ("UMC's 40nm Process")[2] | 425A6 | February 2009 |
| Products Manufactured using Intel's 90nm Process ("Intel 90nm Process") | 425B | August 2002 |

### 3. Prior Art from *Inter Partes* Review No. IPR2025-00683

| IPR Ex. No. | Reference |
|---|---|
| Ex-1005 | U.S. Pat. Pub. No. 2009/0246922 A1 to Wu et al. (Wu '922). |
| Ex-1006 | U.S. Pat. Pub. No. 2007/0249069 A1 to Alvarez et al. (Alvarez). |
| Ex-1007 | S. Wolf, *Silicon Processing for the VLSI Era: Volume 4—Deep-Submicron Process Technology* (2002) (excerpted) ("Wolf-2002-1007"). |
| Ex-1008 | U.S. Pat. Pub. No. 2005/0112817 A1 to Cheng et al. ("Cheng '817"). |
| Ex-1009 | U.S. Pat. Pub. No. 2007/0034906 A1 to Wang et al. ("Wang '906"). |
| Ex-1010 | U.S. Pat. Pub. No. 2008/0029825 A1 to Saito et al. ("Saito '825"). |
| Ex-1011 | U.S. Pat. Pub. No. 2005/0285203 A1 to Fukutome et al. ("Fukutome"). |

[2] Documents related to products manufactured using UMC's 40nm Process are being produced as Sensitive Technical Information in accordance with Section 11 of the Protective Order (Dkt. 71).

| IPR Ex. No. | Reference |
|---|---|
| Ex-1012 | D. James, "2004 – The Year of 90-nm: A Review of 90 nm Devices," 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (2005) (James-2005). |
| Ex-1013 | S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) (excerpted). ("Sze-1981") |
| Ex-1014 | J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000) (excerpted) (Plummer) |
| Ex-1015 | S.E. Thompson et al., "A 90-nm Logic Technology Featuring Strained Silicon," IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004). (Thompson-2004) |
| Ex-1016 | Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) (May 2007) (Sun-2007). |
| Ex-1017 | T. Ghani et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," Technical Digest of the 2003 IEEE International Electron Devices Meeting ("IEDM"), pp. 978-80 (Dec. 10, 2003) ("Ghani-2003"). |
| Ex-1018 | U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al. (Bohr) |
| Ex-1019 | U.S. Pat. Pub. No. 2006/0286729 A1 to Kavalieros et al. ("Kavalieros '729") |
| Ex-1020 | U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al. ("Murthy '151") |
| Ex-1021 | U.S. Pat. Pub. No. 2011/0042729 A1 to Chen et al. ("Chen '729") |
| Ex-1022 | P. Morin et al., "Extensive Study of the Correlation between ContactEtch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-69 (2007) (Morin-2007). |
| Ex-1023 | U.S. Pat. Pub. No. 2007/0235823 A1 to Hsu et al. (Hsu '823) |
| Ex-1024 | U.S. Pat. Pub. No. 2005/0170104 A1 to Jung et al. ("Jung '104") |
| Ex-1025 | U.S. Pat. Pub. No. 2008/0145984 A1 to Ke et al. (Ke '984) |
| Ex-1026 | P. Bai et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 $\mu m^2$ SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) (Bai-2004). |
| Ex-1027 | K. Mistry et al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007). ("Mistry-2007") |
| Ex-1028 | S. Natarajan et al., "A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171$\mu m^2$ SRAM Cell Size in a 291Mb Array," Technical Digest of the of the 2008 IEEE International Electron Devices Meeting (IEDM), pp. 1-3 (Dec. 2008) ("Natarajan-2008") |
| Ex-1029 | U.S. Pat. Pub. No. 2004/0262784 A1 to Doris et al. ("Doris") |

| IPR Ex. No. | Reference |
|---|---|
| Ex-1030 | U.S. Pat. No. 6,797,556 B2 to Murthy et al. ("Murthy '556") |
| Ex-1031 | U.S. Pat. Pub. No. 2007/0134870 A1 to Lee et al. ("Lee '870") |
| Ex-1032 | U.S. Pat. Pub. No. 2005/0260810 A1 to Cheng et al. ("Cheng '810") |
| Ex-1033 | U.S. Pat. Pub. No. 2009/0020820 A1 to Baik et al. ("Baik"). |
| Ex-1034 | U.S. Pat. Pub. No. 2008/0293207 A1 to Koutny et al. ("Koutny"). |
| Ex-1035 | U.S. Pat. Pub. No. 2010/0075476 A1 to Miyashita. ("Miyashita"). |
| Ex-1039 | S. Thompson et al., "Source/Drain Extension Scaling for 0.1µm and Below Channel Length MOSFETS," Digest of Technical Papers for the 1998 Symposium on VLSI Technology, pp. 132-33 (1998) ("Thompson-1998"). |
| Ex-1040 | D.M. Fleetwood et al., *Defects in Microelectronic Materials and Devices* (2008) ("Fleetwood-2008"). |
| Ex-1041 | U.S. Pat. Pub. No. 2006/0246641 A1 to Kammler et al. ("Kammler"). |
| Ex-1042 | U.S. Pat. Pub. No. 2007/0228482 A1 to Wei et al. ("Wei"). |
| Ex-1043 | U.S. Pat. Pub. No. 2008/0203486 A1 to Wiatr et al. ("Wiatr"). |
| Ex-1044 | U.S. Pat. Pub. No. 2009/0242995 A1 to Suzuki et al. (Suzuki '995). |
| Ex-1045 | U.S. Pat. Pub. No. 2007/0090465 A1 to Suzuki et al. ("Suzuki '465"). |
| Ex-1046 | A. Pavlov & M. Sachdev, *CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test* (2008) (excerpted) ("Pavlov-2008"). |
| Ex-1047 | U.S. Pat. Pub. No. 2007/0023832 A1 to Matsui ("Matsui"). |
| Ex-1048 | M. Ishida et al., "A Novel 6T-SRAM Cell Technology Designed with Rectangular Patterns Scalable Beyond 0.18 µm Generation and Desirable for Ultra High Speed Operation," Proceedings of the 1998 International Electron Devices Meeting (IEDM), pp. 201-04 (1998) ("Ishida-1998"). |
| Ex-1049 | D. Balobas & N. Konofaos, "Design and Evaluation of 6T SRAM Layout Designs at Modern Nanoscale CMOS Processes," 4th International Conference on Modern Circuits and System Technologies (2015) ("Balobas-2015"). |
| Ex-1050 | U.S. Pat. Pub. No. 2011/0074498 A1 to Thompson et al. ("Thompson '498"). |

### 4. Identification of Obviousness Combinations Pursuant to P.R. 3-3 (b) and (c)

Based upon Defendant's present understanding of the Asserted Claims, those claims are invalid as obvious in view of the following combination of prior art references. In *KSR International Co. v. Teleflex Inc.*, 500 U.S. 398 (2007), the U.S. Supreme Court rejected the Federal Circuit's rigid "teaching, suggestion, or motivation" requirement in favor of a flexible, functional approach in which an explicit finding of a "motivation" to combine prior art references

is not required to establish obviousness. The Supreme Court held that it is sufficient that a combination of elements was "obvious to try" holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known option within his or her technical grasp." *Id.* at 402; *see also Dystar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (explaining that when the "combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient," there exists a motivation to combine prior art references even when there is no explicit suggestion in the references themselves "[b]ecause the desire to enhance commercial opportunities by improving a product or process is universal—and even commonsensical"); *LeapFrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157 (Fed. Cir. 2007) (applying KSR and holding that "one of ordinary skill in the art of children's learning toys would have found it obvious to combine the Bevan device with the SSR to update it using modern electronic components in order to gain the commonly understood benefits of such adaption, such as decreased size, increased reliability, simplified operation, and reduced cost").

The Asserted Claims are rendered obvious by the references identified in the attached claim charts, either alone or in the combinations with other prior art references as identified below or in the attached claim charts. The tables above identify prior art that anticipates each asserted claim.

Those tables, the prior art claim charts found at Exhibits 425A1-A6 and 425B, and the table below identifies prior art that by itself, or in combination with other art and/or the knowledge of one skilled in the art, renders the asserted claims obvious.

Defendant contends that all claims that are anticipated by a particular reference are also rendered obvious by that same reference alone, or in combination with the other references,

discussed below. Defendant further contends that one of ordinary skill in the art, at the time of the alleged invention of the Asserted ’425 Patent Claims, would have been motivated to combine the references disclosed herein in such a way to reach the alleged inventions. The teaching, suggestion, or motivation to combine these references, although not required, is explicitly or implicitly found in one or more of the following: the knowledge or common sense of one of ordinary skill in the art; the prior art references themselves and/or the prior art as a whole, including interrelated teachings of multiple prior art references; the subject matter acknowledged as prior art in the ’425 Patent; the nature of the problem to be solved and the existence of similar improvements in similar applications; design incentives and other market forces, including the advantages of creating a superior and more desirable product and the effects of demands known to the design community or present in the marketplace; the ability to implement the alleged invention as a predictable variation of the prior art; improvements in similar devices; the interrelated teachings of multiple prior art references; any needs or problems known in the field addressed by the ’425 Patent; and the number of identified, predictable solutions to the problem addressed by these patents. In addition, the simultaneous (and/or prior) inventions described above, and elsewhere in these contentions, is evidence that motivation to combine the concepts described in the various prior art references did, in fact, exist, and they were, in fact, combined. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary. A person of ordinary skill would have access to the materials found in the cited and attached exhibits and would have at least the ordinary creativity and skill to combine the attached references in ways not explicitly recited above. The combinations evidencing teachings, suggestions, and/or motivations to combine the prior art references in a way that renders the asserted claims obvious are merely exemplary,

| Primary Reference | In Combination With One or More Of |
|---|---|
| Shima | Sato, Ohta, Ogura, Intel 65nm Process, Intel 90nm Process, Terauchi, Suzuki ’995, Wu ’922, Alvarez, UMC 40nm Process, Wolf-2002-1007, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005 |
| Ohta | Sato, Ogura, Intel 65nm Process, Intel 90nm Process, Shima, Terauchi, Suzuki ’995, Wu ’922, Alvarez, UMC 40nm Process, Wolf-2002-1007, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005 |
| Intel 65nm Process | Sato, Ohta, Ogura, Shima, Terauchi, Suzuki ’995, Wu ’922, UMC 40nm Process, Wolf-2002-1007, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005, Intel 90nm Process, Alvarez |
| Ogura | Ohta, Intel 65nm Process, Intel 90nm Process, Shima, Terauchi, Suzuki ’995, Wu ’922, Alvarez, UMC 40nm Process, Wolf-2002-1007, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005 |
| Sato | Ogura, Ohta, Intel 65nm Process, Intel 90nm Process, Shima, Suzuki ’995, Wu ’922, Alvarez, UMC 40nm Process, Wolf-2002-1007, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005 |
| UMC 40nm Process | Sato, Ohta, Ogura, Intel 65nm Process, Intel 90nm Process, Shima, Terauchi, Suzuki ’995, Wu ’922, Alvarez, Wolf-2002-1007, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005, |
| Intel 90nm Process | Sato, Ohta, Intel 65nm Process, Shima, Terauchi, Suzuki ’995, Wu ’922, Alvarez, UMC 40nm Process, Wolf-2002-1007, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005, |
| Wu ’922 | Alvarez, Wolf-2002-1007, Ogura, Ohta, Intel 65nm Process, Intel 90nm Process, Shima, Sato, Suzuki ’995, UMC 40nm Process, Wang ’906, Cheng ’817, Saito ’825, Fukutome, James-2005, Terauchi |
| Cheng ’817 | Wolf-2002-1007, Ogura, Ohta, Intel 65nm Process, Intel 90nm Process, Shima, Sato, Suzuki ’995, UMC 40nm Process, Wu ’922, Alvarez, Wang ’906, Saito ’825, Fukutome, James-2005, Terauchi |

| Primary Reference | In Combination With One or More Of |
|---|---|
| Saito ’825 | Fukutome, James-2005, Ogura, Ohta, Intel 65nm Process, Intel 90nm Process, Shima, Sato, Suzuki ’995, UMC 40nm Process, Wu ’922, Alvarez, Wang ’906, Cheng ’817, Terauchi, Wolf-2002-1007 |

Defendant hereby identifies additional motivation and reasons to combine the cited art: One of ordinary skill in the art would be motivated to combine these references in the above combinations for at least the following reasons. One of skill in the art would have been motivated to combine these references, because these references relate to common objectives and subject matter. The identified prior art references relate to common objectives and share commonalities in terms of their general subject matter as well as the types of equipment, products, and approaches used, including their descriptions of semiconductor devices (e.g., field-effect transistors, such as MOSFETs and MISFETs). *See e.g.*, Shima at [0080]; Ogura at [0003]; Intel Core Duo 52300 (“Yonah”) at Sections 4.6-4.8; Ohta at [0010]-[0011]; Sato at [0003]; Terauchi at [2:32-50]; Suzuki ’995 at [0001]-[0004]; Thompson-2004 at Abstract, Introduction; Wu ’922 at [0004].

Further, the Asserted Claims of the ’425 Patents contain merely a duplication of concepts known in the prior art and have no patentable significance given that no unexpected results occur (i.e., the patentee merely combines known prior art elements according to known methods to yield predictable results). For example, the state of the art had already disclosed that stress inducing components like SiGe source/drains and SiN layers formed on top of P and N transistors could provide channel benefits as transistors continued to decrease in size. *See e.g.*, 2004 VLSI Symposium Paper 6.1 by Chidambaram et al. (Chidambaram-2004) (“A highly compressive SiGe layer, in close proximity to the channel, results in large hole mobility improvements. HRTEM based lattice parameter extractions confirm the compressive strain in the channel.”); 2004 VLSI Symposium Paper 6.2 by Mistry et al. (“Mistry-2004”) (“Uniaxial strained silicon has been

implemented in a high volume manufacturing 90nm logic technology for the first time, with impressive performance results and improved power scaling.”).

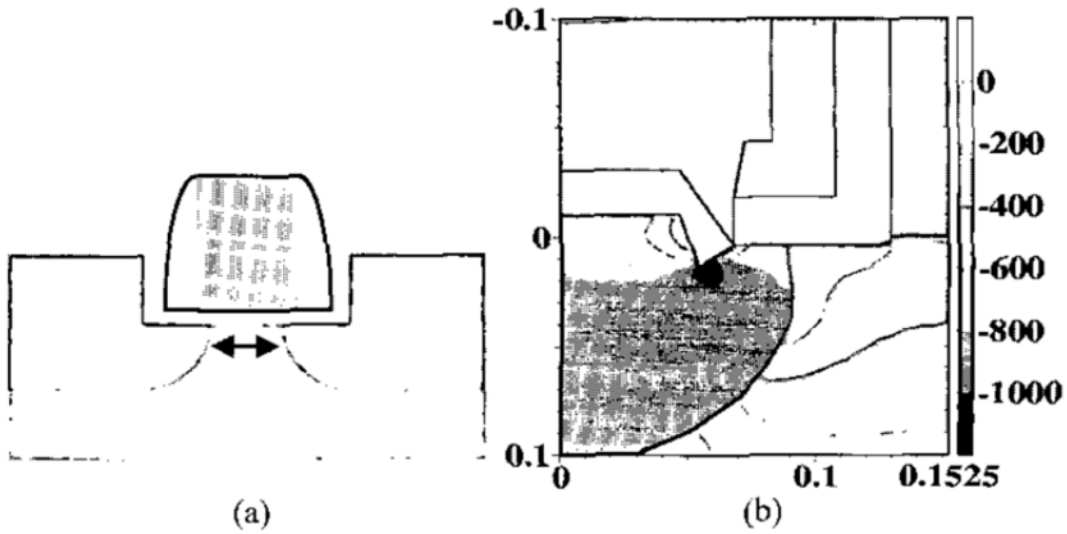


Fig. 2 (a) Epitaxial S/D Transistor structure. (b) Stress simulations: the resulting stress is dominantly uniaxial along the [110] current flow direction X and Y-axes show dimensions in μm. Contours show stress in MPa.

2004 VLSI Symposium Paper 6.5 by Chen et al. (Chen-2004) (“An advanced stress memorization technique (SMT) for device performance enhancement is presented. A high-tensile nitride layer is selectively deposited on the n+ poly-Si gate electrode as a stressor with poly amorphorization implantation in advance. And, this high-tensile nitride capping layer will be removed after the poly and S/D activation procedures. The stress modulation effect was found to be enhanced and memorized to affect the channel stress underneath the re-crystallized poly-Si gate electrode after this nitride layer removal. More than 15% current drivability improvement was obtained on NMOS without any cost of PMOS degradation. The driving current improvement through the PAI, tensile ACL and ACL thickness effects clearly illustrate that the stress memorization effect is achieved by this temporary stress promoter. Compared to the complicated strain substrate OT selective epi SiGe process, this SMT approach shows the benefits of low cost and low risk of reliability.”); *id.* (“In this paper, we proposed a novel stress memorized technique

(SMT) to improve the device performance without PMOS degradation. A high tensile nitride capping layer acts as a temporary stressor to effectively modulate the channel stress. The stress effect is then enhanced and memorized by well-controlled poly amorphorization and re-crystallization procedures. This high tensile nitride capping layer will be removed after the annealing step. Therefore, a much thicker capping layer can be used to increase the stress level without any process limitation to impact the subsequent gap filling process steps."); *id.* ("After the silicide formation, the low temperature, high-tensile Nitride film is deposited as Contact-Etch-Stop-Layer (SIN-CESL) to add up the stress effect. Finally, the metallization is done for device characterization.").

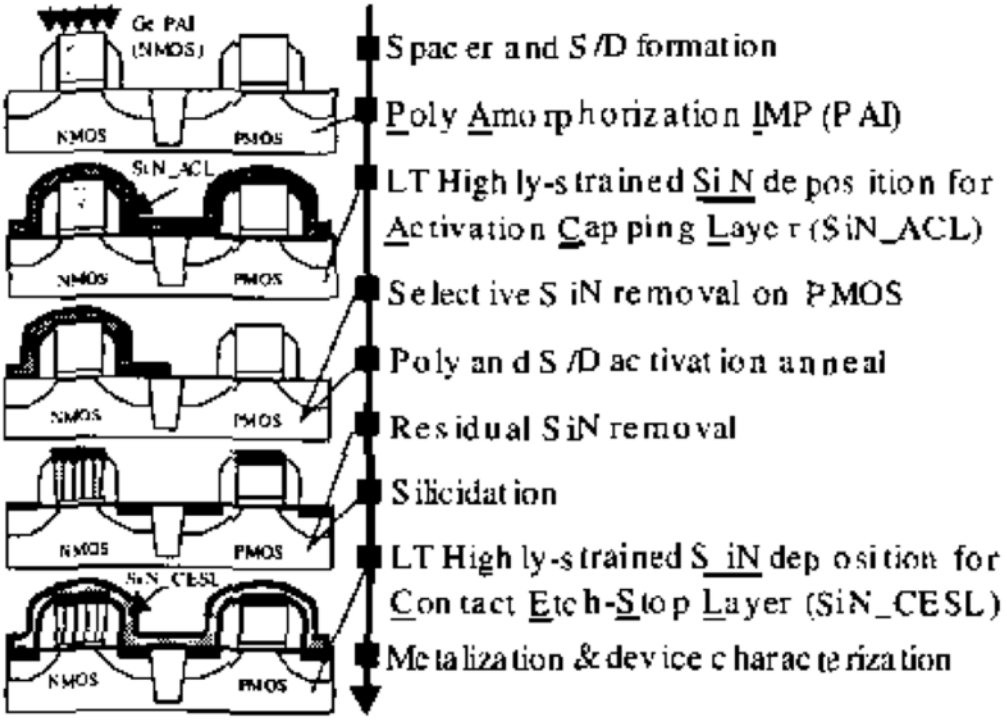


Fig.1 Process sequence of Stress Memorization Technique (SMT).

Further, the prior art references of record describe well-known semiconductor devices (e.g., field-effect transistors, such as MOSFETs and MISFETs), their structures and fabrication processes, including the common gate structure, a gate dielectric layer, sidewall structures, and

trenching then growing epitaxial silicon germanium (SiGe) in the source drain regions of a PMOS device, and the use of stress-inducing films over the NMOS and PMOS devices. *See, e.g.,* Shima at [0069], [0080], [0097]-[0098], [0059]-[0065],[0082]-[0083], and Figs. 3, 12, and 13; Ogura at [0003], [0019]-[0022] and Fig. 1I; Yonah at Sections 4.6-4.8; Ohta at [0010]-[0011], [0040]-[0045], and Fig. 10B; Sato at [0115], [0126], and Figs. 2C, 6A; Terauchi at [2:32-50] and Fig. 5; Suzuki '995 at [0001]-[0004], [0057]-[0058] and Fig. 2(c); Thompson-2004 at Fig. 2; Wu '922 at [0004].

In particular, the prior art of record confirms that it was well-known to deposit a compressive or tensile stress-inducing film over the NMOS and PMOS devices to induce a desired strain on the NMOS and/or PMOS device. *See, e.g.*, Shima at [0069] ("On the other hand, the CMOS device . . . includes a compressive stressor film . . . typically of SiN and accumulating a tensile stress therein in correspondence to the device region"); *id.* at [0097]-[0098] ("Further, in the present embodiment, it is possible to cover the p-channel MOS transistor . . . by the tensile stressor film formed on the device region . . . in place of the foregoing compressive stressor film . . . and decrease the thickness of the tensile stressor film . . . selectively in correspondence to the device region"); Ogura at [0005]-[0008]; Yonah at Section 4.6; Ohta at [0040]-[0045]; Sato at [0126]; Thompson-2004 at Abstract ("A tensile silicon nitride-capping layer is used to introduce tensile strain into the n-type MOSFET and enhance electron mobility by 20%."); *id.* ("Contrary to hole mobility enhancement with stress, the theoretical understanding for electron mobility enhancement for bi-axial and uniaxial tensile stress is well developed."); *id.* at Fig. 5; Wu '922 at [0005] ("The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor.")

Depending on how the stress-inducing film is formed, it may provide tensile stress or compressive stress. *See e.g.*, Ohta at [0041] ("the influence from the stressor film upon the stresses applied on an NMOS transistor (corresponding to a first field effect transistor according to the invention) and a PMOS transistor (corresponding to second field effect transistor according to the invention) is controlled by controlling the respective gate heights mainly of the NMOS transistor and the PMOS transistor."); Shima at Fig. 4 and [0069]; Wu '922 at [0005] ("The process-induced strain based method is performed with several unique processes to form a strained thin film upon a surface of the MOS transistor that exert tensile stress or compressive stress upon the MOS transistor."). Stress on the devices in the channel region has a long history and was well know before January 2010, as the '425 Patent itself acknowledges. *See* '425 Patent at 1:15-2:62 ("A distortion technique of enhancing the drive capability of a MISFET (hereinafter referred to as a 'MIS transistor') by applying a stress to the channel region of the MIS transistor has been employed to improve the performance of a semiconductor integrated circuit device."). *See also* Thompson-2004 ("Contrary to hole mobility enhancement with stress, the theoretical understanding for electron mobility enhancement for bi-axial and uniaxial tensile stress is well developed."). The tensile stress was well known to improve electron mobility in the channel region of the NMOS device. *See e.g.*, Shima at [0039]; Ohta at [0003] ("It is generally known that an NMOS semiconductor device gets improvement of an electron mobility due to a stress acting in a direction of stretching (a direction in which an interval between atoms structuring a crystal expands) within a plane parallel with a substrate of the semiconductor device."); Ogura at [0004] ("The electron mobility in an n-channel MOS (nMOS) transistor can be improved by applying tensile stress to the channel region."); Yonah at Section 4.6 ("PMD 1 (silicon nitride) applies tensile strain to the NMOS channel. For minimum pitch NMOS transistors, this tensile strain

reportedly gives a 20% mobility gain over Intel's 90 nm process, and a 40% mobility gain over unstrained silicon.").

Therefore, a person of ordinary skill in the art the time of the alleged invention would have been motivated to modify the prior art include a tensile stress-inducing film over the NMOS and PMOS devices, as taught by the prior art.

Further the prior art of record confirms that it was well-known to form stress-relief layers. In the case of a PMOS device with SiGe regions, the tensile stress-inducing film offsets at least some of the compressive stress the SiGe applies to the channel region, thereby reducing improvements in the device's performance. *See e.g.*, Shima at Fig. 4; Ogura at [0010] ("However, in the CMOS semiconductor devices having a Si Ge mixed crystal in the source/drain of the pMOS transistor and the silicon nitride film of tensile stress formed over the pMOS transistor, many contact failures have occurred."). It was well known in the art that the tensile stress on the PMOS can be further reduced by forming a stress-relief layer. *See e.g.*, Lee '870 at [0020], [0046]-[0067] ("a stress film over stress relief film and the second type MOS transistor whereby the stress film improves the second type MOS transistor performance and whereby the stress relief film reduces the strain from the stress film."); Wu '922 at [0005]; Alvarez at [0049] ("However, due to the presence of the first material or stress-controlling material 226 in the second region 232 and the third region 242, the stress-increasing material 216 has less of an impact of the stress 248 in the channel regions of the transistors 222 b, 224 b, 222 c, and 224 c in the second region 232 and the third region 242."); Murthy '556 at 9:27-29 ("Oxide layer 322 buffers the large stress inherent silicon nitride layer 324 and provides an etch step for silicon nitride layer 324 during a Subsequent Spacer etch."); Doris at [0042] ("The stress level along with the thickness of the film also defines a neutral buffer layer between the compressive spacer and the tensile etch stop layer. Thickness

optimization of this film allows the compressive spacer for the pFET to have maximum influence on the pFET channel mobility and minimizes the influence of the tensile barrier etch stop layer 340."); Cheng '810 at [0030] ("Alternatively, the oxide buffer layer 26 may be formed over the PMOS device but not removed prior to forming a tensile stress dielectric layer over both the NMOS and PMOS devices followed by the thinning process.").

Therefore, a person of ordinary skill in the art at the time of the alleged invention would have been motivated to modify the PMOS device to include a stress-relief film in order to mitigate the tensile stress on the device, as taught by the prior art.

Additional evidence that there would have been a motivation to combine the prior art references identified above pursuant to P.R. 3-3(a) includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art. For example, the prior art references are directed to solving the same problem. Thus, a skilled artisan seeking to solve this problem, would have looked to these cited references alone or in combination. Accordingly, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved, (2) the express, implied and inherent teachings of the prior art, (3) the knowledge of persons of ordinary skill in the art, (4) the prior art as of the priority date is generally within the same field of endeavor, or (5) the predictable results obtained in combining the different elements of the prior art.

To the extent Plaintiff contends that any reference contains multiple distinct embodiments, it would be obvious to combine element of the distinct embodiments. A person would be motivated to make such a combination because the elements are found in the same reference and the reference as a whole is directed to the same topic or topics.

Numerous prior art references, including those identified above pursuant to P.R. 3-3(a), reflect common knowledge and the state, scope and content of the prior art before the priority dates of the Asserted Patents. *See Graham v. John Deere Co.*, 383 U.S. 1, 35-36 (1966).

Defendant is not aware of any secondary considerations supporting non-obviousness of the Asserted Claims of the '425 Patent. To the extent Plaintiff seeks to introduce any alleged secondary considerations in the future, Defendant reserves the right to respond at that time.

For at least the reasons described herein as well as in the exemplary combinations and the prior art claim charts found at Exhibits 425A1-A6 and 425B, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those identified above. As such, Defendant's inclusion of exemplary combinations, in view of the factors and motivations identified in the preceding paragraph, does not preclude Defendant from identifying other invalidating combinations as appropriate, or the prior art as a whole.

## IV. PRIOR ART DOCUMENT PRODUCTION

Defendant is producing prior art under P.R. 3-4 concurrent with these contentions, including at PRIOR_ART_UMC_00000001 through PRIOR_ART_UMC_00032152. Additionally, documents related to products manufactured using UMC's 40nm Process are being produced as Sensitive Technical Information in accordance with Section 11 of the Protective Order (Dkt. 71).

## V. TECHNICAL DOCUMENT PRODUCTION

Defendant has diligently collected technical documents sufficient to show the operation of the accused products and are producing them under P.R. 3-4 concurrent with these contentions.

Defendant will make documents available according to the Sensitive Technical Information procedures under the protective order on a standalone computer at the offices of Troutman Pepper Locke LLP or at another location selected by Defendant.

Dated: May 1, 2025

Respectfully submitted,

*/s/ Mark Hannemann*
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**COUNSEL FOR DEFENDANT UNITED MICROELECTRONICS CORPORATION**

## CERTIFICATE OF SERVICE

I hereby certify that on May 1, 2025, the foregoing document was served via e-mail on all counsel of record for Plaintiff.

*/s/ Ryan E. Dornberger*
Ryan E. Dornberger