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(54) TRANSISTORS OF SEMICONDUCTOR DEVICES AND METHODS OF FABRICATING THE SAME

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(57) **ABSTRACT**

Transistors and methods of fabricating transistors are disclosed. A disclosed method comprises forming an inversion epitaxial layer on a silicon substrate; forming a hard mask on the inversion epitaxial layer; depositing a silicon epitaxial layer over the inversion epitaxial layer; forming a trench through the silicon epitaxial layer by removing the hard mask; forming reverse spacers on the sidewalls of the trench by filling the trench with an insulating layer and etching the insulating layer; forming a gate electrode over the reverse spacers; forming pocket-well regions and LDD regions in the silicon substrate by performing ion implantations; forming spacers on the sidewalls of the gate electrode; forming source and drain regions in the silicon substrate by performing an ion implantation; and forming a silicide layer on the gate electrode and the source and drain regions.

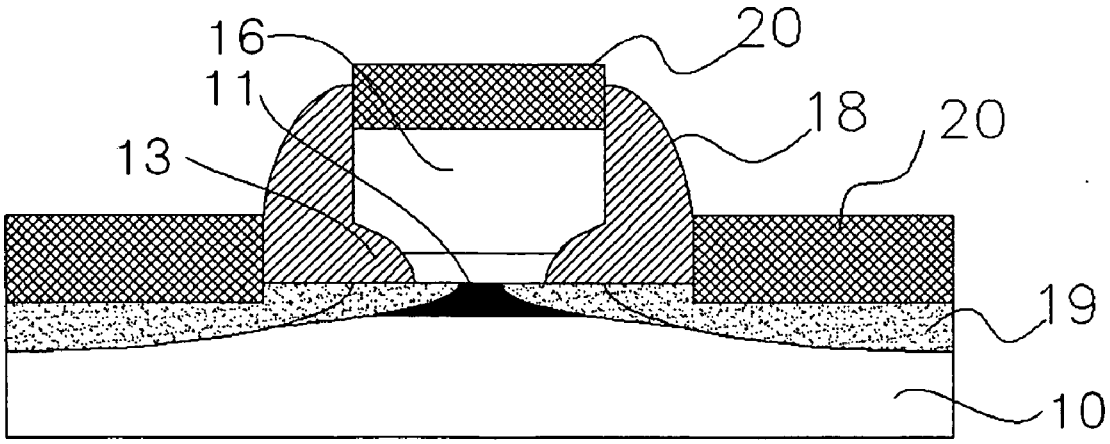


Fig. 1 (PRIOR ART)

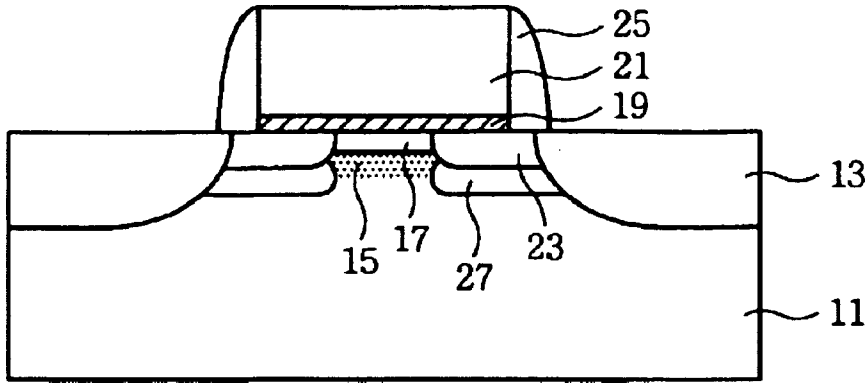


Fig. 2a

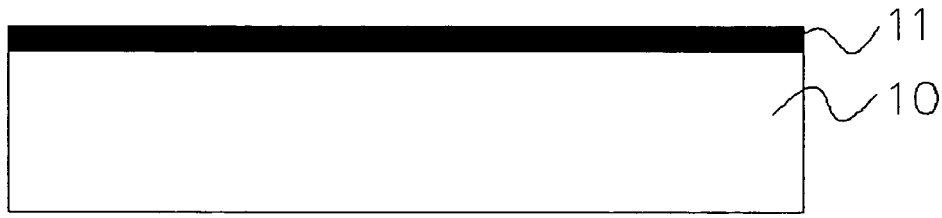


Fig. 2b

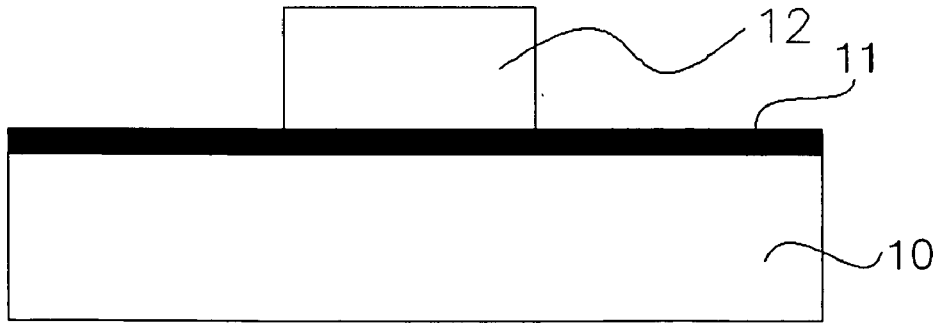


Fig. 2c

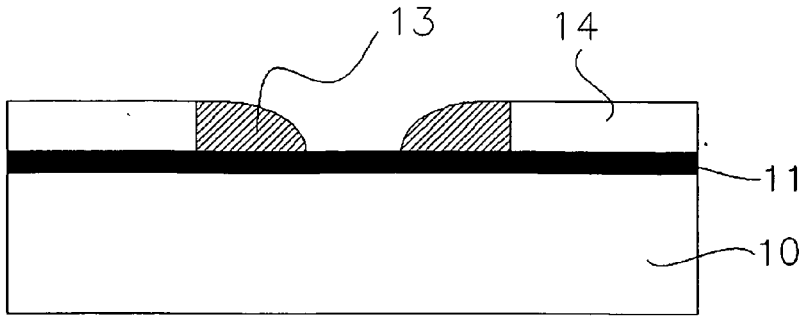


Fig. 2d

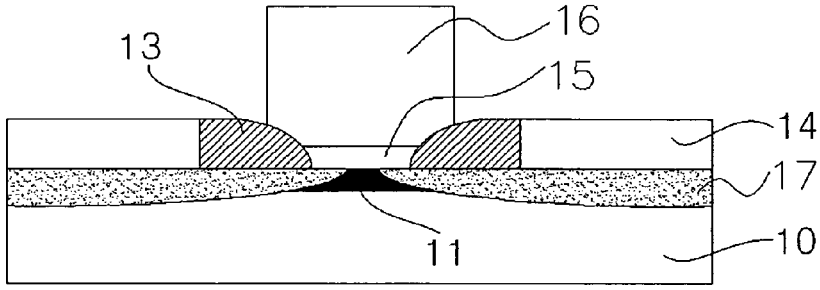
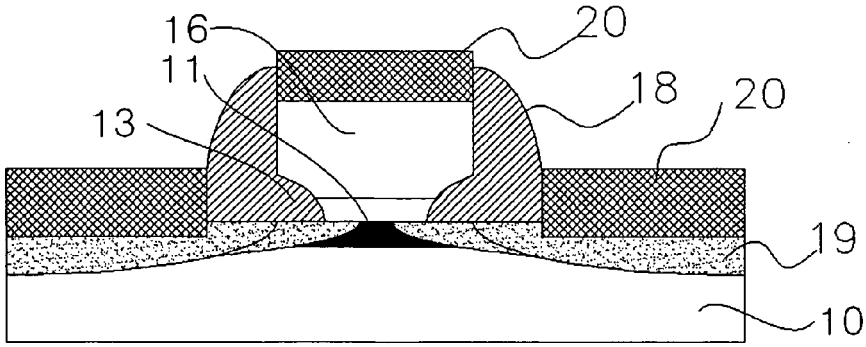


Fig. 2e



TRANSISTORS OF SEMICONDUCTOR DEVICES AND METHODS OF FABRICATING THE SAME

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to transistors of semiconductor devices and methods of fabricating the same.

BACKGROUND

[0002] In a metal-oxide-semiconductor (MOS) transistor such as a MOS field-effect-transistor (MOSFET), electric current flows through a surface region under a gate electrode and a gate oxide when an electric field is applied to the source and drain junction regions while a gate charge is applied. The surface region through which the electric current flows is known as a channel. The characteristics of a MOSFET are determined by a dopant concentration in the channel. More specifically, it is very important to precisely dope impurities into the channel region because device characteristics such as the threshold voltage of the transistor and the drain current are subject to the dopant concentration.

[0003] Conventional channel doping is achieved by performing well ion implantation, channel ion implantation, or threshold ion implantation. Channel structures formed by such ion implantation include a flat channel in which a dopant concentration is uniform through the whole region of the channel, a buried channel which is formed at a predetermined distance from the top surface of a semiconductor substrate, and a retrograde channel which has a vertically increasing doping profile from the top surface of the channel. Retrograde channels are widely used for high performance microprocessors requiring a channel length less than 0.2 μm. In such a context, the retrograde channel is generally formed by heavy ion implantation using indium (In), arsenic (As), or antimony (Sb). The retrograde channel is suitable for high performance MOSFET devices with high driving current characteristics because a low dopant concentration in its surface increases the surface mobility of an electric current.

[0004] As the degree of integration of a semiconductor device increase, the channel length is shortened, and a very thin channel is required. However, conventional ion implantation technology cannot achieve a retrograde channel less than 50 nm in depth. To solve such a problem, an epitaxial channel has been suggested. However, the epitaxial channel has not achieved an improvement in the current on-off characteristics because it is difficult to control the loss and diffusion of the channel dopants due to an epitaxial layer formation process and a later thermal treatment process.

[0005] The most ideal channel doping method may embody a δ-doped epitaxial channel. However, according to the reported findings, both doped and undoped epitaxial layers cannot be made into a δ-doped epitaxial channel less than 30 nm in depth because of later dopant diffusion.

[0006] To solve such a problem, a method for preventing diffusion of dopants in a δ-doped layer has been suggested in Lee and Lee, *Laser Thermal Annealed SSR Well Prior to Epi-Channel Growth (LASPE) for 70 nm nFET*, IEDM 2000. The suggested method performs channel doping by using an ultra-low energy ion implantation and an instant laser annealing. According to the suggested method, the instant laser annealing controls the diffusion and loss of dopants during a selective epitaxial growth.

[0007] However, the laser power for the laser annealing may cause partial melting of the silicon substrate surface, thereby deteriorating the surface roughness and causing crystal defects. Therefore, the laser annealing method is not applicable to practical semiconductor device manufacturing processes.

[0008] **FIG. 1** is a cross-sectional view of a conventional transistor having a super steep retrograde (SSR) epitaxial channel. Although conventional transistor fabrication technology has reduced the depth of the channel by forming a retrograde channel **17** as shown in **FIG. 1**, it has failed to substantially reduce the length of the channel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **FIG. 1** is a cross-sectional view of a conventional transistor having an SSR epitaxial channel.

[0010] **FIGS. 2***a* through **2***e* are cross-sectional views illustrating an example process of fabricating a transistor of a semiconductor device having an SSR epitaxial channel and reverse spacers performed in accordance with the teachings of the present invention.

DETAILED DESCRIPTION

[0011] **FIGS. 2***a* through **2***e* are cross-sectional views illustrating an example process of fabricating a transistor of a semiconductor device having an SSR epitaxial channel and reverse spacers. Referring to **FIG. 2***a*, an inversion epitaxial layer **11** is formed over a silicon substrate **10**. The inversion epitaxial layer **11** is used as an SSR epitaxial channel.

[0012] Referring to **FIG. 2***b*, a hard mask **12** is formed on the inversion epitaxial layer **11**. The hard mask **12** covers an area for reverse spacers to be formed by a later unit process.

[0013] Referring to **FIG. 2***c*, a silicon epitaxial layer **14** is formed over the inversion epitaxial layer **11**, but not on the area covered by the hard mask. The hard mask is then removed to form a trench through the silicon epitaxial layer **14**. The trench is filled with an insulating layer. The insulating layer is then dry-etched to form reverse spacers **13** on the sidewalls of the trench. In the illustrated example process, the width of the trench is smaller than the width of a gate electrode to be formed by a later unit process. The insulating layer is preferably a single layer of tetra ethyl ortho silicate (TEOS) or a multi-layer of TEOS-SiN-TEOS.

[0014] Referring to **FIG. 2***d*, an oxide layer and a polysilicon layer are sequentially deposited over the structure of **FIG. 2***c*. Some portion(s) of the oxide layer and the polysilicon layer are removed by using a dry etching process to complete a gate oxide **15** and a gate electrode **16**. The gate electrode **16** is positioned above the inversion epitaxial layer between the reverse spacers. In the illustrated example process, the width of the gate electrode **16** is smaller than the width of the trench, but larger than the space between the reverse spacers **13**. The length of a channel under the gate electrode **16** is defined as the length of the SSR epitaxial channel **11** between the reverse spacers **13**. By forming the reverse spacers **13** on the area for the gate electrode **16**, the illustrated example process can considerably reduce the length of the channel compared to a conventional process

which forms a channel having the same length as the gate electrode. Therefore, the illustrated example process is applicable to a fabrication process for a less than 90 nm transistor.

[0015] Next, pocket-well regions (not shown) and lightly doped drain (LDD) regions **17** are formed in the silicon substrate **10** by performing a first ion implantation process. Generally, conventional technology must implant low energy ions in order to form a shallow junction to prevent a leakage current of the junction area. However, the illustrated example process can form a shallow junction even when high energy ions are implanted because the silicon epitaxial layer **14** and the reverse spacers **13** on the inversion epitaxial layer **11** function as a buffer layer during the first ion implantation.

[0016] Referring to **FIG. 2***e*, an insulating layer is deposited over the structure of **FIG. 2***d*. An etching process is performed to form gate spacers **18** on the sidewalls of the gate electrode **16**. A second ion implantation process is then performed using the gate electrode **16** and the gate spacers **18** as a mask to form deep source and drain regions **19** in the silicon substrate **10**. Particularly, the illustrated example process may form elevated source and drain regions because the second ion implantation process may implant ions into the silicon epitaxial layer **14** on the source and drain regions **19**. Moreover, because the silicon epitaxial layer **14** functions as a buffer layer during the second ion implantation process, the described example process achieves the shallow junction necessary for a nanometer scale transistor design, thereby obviating the problem of parasitic capacitance due to the formation of the shallow junction. Subsequently, a silicide layer **20** is respectively formed on the gate electrode **16** and on the source drain regions **19** by using a known unit process.

[0017] Consequently, a MOS transistor comprising an inversion epitaxial layer as an SSR epitaxial channel and elevated source and drain regions is completed. In detail, as shown in **FIG. 2***e*, after an inversion epitaxial layer is formed on a semiconductor substrate, a trench is placed over the inversion epitaxial layer and reverse spacers are positioned on the sidewalls of the trench. After a gate electrode is positioned above the inversion epitaxial layer between the reverse spacers, gate spacers are placed on the sidewalls of the gate electrode. Pocket-well regions are formed under opposite sides of the gate electrode in the silicon substrate, and LDD regions are positioned adjacent the upper part of the pocket-well regions and the inversion epitaxial layer over the pocket-well regions. Source and drain regions, (which have a larger thickness than the LDD regions), are positioned adjacent the LDD regions in the silicon substrate. A silicide layer is positioned on the gate electrode and through the silicon epitaxial layer on the source and drain regions, respectively.

[0018] From the foregoing, persons of ordinary skill in the art will appreciate that the disclosed methods of fabricating a transistor of a semiconductor device simplify the manufacturing process and reduce production costs because they use an existing gate fabrication process. In other words, by depositing a silicon epitaxial layer before source and drain regions are formed in a silicon substrate and performing ion implantation processes, the disclosed methods simplify the manufacturing process in comparison with a conventional selective epitaxial growth process requiring an additional ion implantation process.

[0019] From the foregoing, persons of ordinary skill in the art will further appreciate that, by forming an SSR epitaxial channel, a silicon epitaxial layer, and reverse spacers, the disclosed methods of fabricating a transistor of a semiconductor device reduce parasitic capacitance and a junction leakage current of a nanometer scale MOS transistors.

[0020] It is noted that this patent claims priority from Korean Patent Application Serial Number 10-2003-0102038, which was filed on Dec. 31, 2003, and is hereby incorporated by reference in its entirety.

[0021] Although certain example methods, apparatus and articles of manufacture have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.

What is claimed is:

1. A transistor comprising:

an inversion epitaxial layer on a silicon substrate;

a trench over the inversion epitaxial layer;

reverse spacers on sidewalls of the trench;

a gate electrode above the inversion epitaxial layer between the reverse spacers;

spacers on the sidewalls of the gate electrode;

pocket-well regions under opposite sides of the gate electrode;

LDD regions positioned adjacent respective ones of the pocket-well regions;

source and drain regions positioned adjacent the LDD regions, the source and drain regions having a larger thickness than the LDD regions; and

a silicide layer positioned on the gate electrode and the source and drain regions.

2. A transistor as defined by claim 1, wherein the inversion epitaxial layer is used as an SSR epitaxial channel.

3. A transistor as defined by claim 1, wherein a gate channel is located under the gate electrode, the gate channel having a length defined by a length of the inversion epitaxial layer exposed between the reverse spacers.

4. A transistor as defined by claim 1, wherein the gate electrode has a width smaller than the trench and larger than a space between the reverse spacers.

5. A transistor as defined by claim 1, wherein the source and drain regions are elevated source and drain regions.

6. A method of fabricating a transistor comprising:

forming an inversion epitaxial layer on a silicon substrate;

forming a hard mask on the inversion epitaxial layer;

forming a silicon epitaxial layer over the inversion epitaxial layer;

removing the hard mask to form a trench through the silicon epitaxial layer;

filling the trench with an insulating layer;

etching the insulating layer to form reverse spacers on sidewalls of the trench;

forming a gate electrode over the reverse spacers, the gate electrode being positioned above the inversion epitaxial layer between the reverse spacers;

performing ion implantation using the gate electrode as a mask to form pocket-well regions and LDD regions;

forming spacers on sidewalls of the gate electrode;

performing ion implantation using the gate electrode and the spacers as a mask to form source/drain regions; and

forming a silicide layer on the gate electrode and the source and drain regions.

7. A method as defined by claim 6, wherein the reverse spacers are formed by a dry etching process.

8. A method as defined by claim 6, wherein the reverse spacers are formed of a single layer of TEOS or a multi-layer of TEOS-SiN-TEOS.

9. A method as defined by claim 6, wherein the source and drain regions are elevated source and drain regions.

10. A method as defined by claim 6, wherein the silicide layer on the source and drain regions is formed through the silicon epitaxial layer on the source and drain regions

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