

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,
Patent Owner.

IPR2025-00829

U.S. Patent 7,923,764

**DECLARATION OF JACK LEE, PH.D. IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT 7,923,764**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 7,923,764 to Hirase, et al. (“the ’764 patent”)
1002	File History of U.S. Patent 7,923,764 (“’764 File History”)
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from JP File History
1006	U.S. Patent 7,579,227 to Hirase, et al. (“the ’227 patent”)
1009	U.S. Publication 2003/0025135 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1012	U.S. Publication 2006/0131672 to Wang, et al. (“Wang”)
1013	U.S. Publication 2005/0051856 to Ono, et al. (“Ono”)
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”)
1019	U.S. Publication 2005/0045938 to Mutou, et al. (“Mutou”)
1023	U.S. Patent 6,306,712 to Rodder, et al. (“Rodder”)
1024	Sim, J. H., et al., “Effects of ALD HfO ₂ thickness on charge trapping and mobility,” Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 (“Sim”)
1025	U.S. Publication 2004/0110352 to Bu, et al. (“Bu”)

Exhibit	Description
1029	Koyama, M., et al., “Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics,” Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 (“Koyama”)
1032	Houssa, M., “High-κ Gate Dielectrics” (CRC Press 1st Ed. 2003) (“Houssa”)
1033	TSMC-1033, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1034	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf”)
1037	Lee, S. J., et al. “High Quality Ultra Thin CVD HfO ₂ Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1038	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1040	JP2005-064190 to Ono with certified translation (“JP-Ono”)
1041	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1049	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1050	U.S. Publication 2005/0040479 to Koldiaev, et al. (“Koldiaev”)
1051	U.S. Publication 2005/0139932 to Cho, et al. (“Cho”)

Exhibit	Description
1052	Albertin, K.F., et al., “Study of PECVD SiO _x N _y films dielectric properties with different nitrogen concentration utilizing MOS capacitors,” Microelectronic Engineering, Vol. 77, pp. 144-49 (2005)

I, Dr. Jack Lee, declare as follows:

1. I have been retained on behalf of Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner” or “TSMC”) as a technical expert witness in connection with the petition for *Inter Partes* Review (“Petition”) of U.S. Patent 7,923,764 to Hirase (“the ’764 patent”). It is my understanding that the ’764 patent is currently assigned to Advanced Integrated Circuit Process LLC (“Patent Owner”).

2. I have been asked by Petitioner to offer opinions regarding the ’764 patent, including the patentability of the claims in view of certain prior art references and the knowledge of a person of ordinary skill in the art. I have also been asked to provide my technical opinions on how concepts in the ’764 patent specification relate to claim limitations of the ’764 patent. This declaration sets forth the opinions I have reached to date regarding these matters.

3. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

4. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the

substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '764 patent.

I. Qualifications

5. I am an expert in the field of semiconductor process technology and semiconductor design. I have over 40 years of first-hand experience as a researcher, educator, and consultant in this field.

6. In formulating my opinions, I have relied on my knowledge, training, and experience in the relevant field, which I will summarize briefly. A more detailed summary of my background, education, experience, and publications is set forth in my curriculum vitae ("CV"), which is provided as TSMC-1004.

7. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley ("UC Berkeley").

8. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

9. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

10. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

11. My current research and teaching interests encompass high-K gate dielectrics and gate electrodes, semiconductor devices, fabrication processes, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, semiconductor memory applications, and alternative channel materials.

12. I have been invited to give talks, teach short courses and participate in panel discussions at numerous conferences specifically on the topic of high-K gate dielectrics and gate electrodes. This includes prestigious conferences such as the Symposium on VLSI Technology, the IEEE International Electron Devices Meeting, and other global forums. My research group at The University of Texas at Austin is recognized as a pioneer in developing hafnium-based high-K materials for nanoscale MOSFETs applications. I have extensive experience in this field, with numerous publications in journals and conference proceedings on the topics of HfO₂, HfSiON, hafnium silicate, interfacial layers, and dielectric reliability.

13. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

14. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 book and book chapters on semiconductor technologies. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g. inventor recognition and best paper awards.

15. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to

silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

16. I have served in various technology consulting and business advisor roles. For example, I have been teaching short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

II. Materials Considered

17. The '764 patent is a division of the application leading to U.S. Patent No. 7,579,227 (the “'227 patent”). In reaching the opinions provided herein, I have considered the '764 patent, its U.S. prosecution history, the '227 patent and its U.S. prosecution history, the prosecution history of the foreign priority application (JP 2005-227457), and the references cited in my Declaration or Attachment A hereto.

18. I have also relied upon my own education, training, research, knowledge, and personal and professional experience in the field and have also considered the viewpoint of a person of ordinary skill in the art at the time of the '764 patent's priority date. As explained below, I am familiar with the level of

skill of a person of ordinary skill in the art regarding the technology at issue as of that time frame.

19. In general, I have been asked to cite to the specification of a patent or patent publication using the following formats: (Patent, Col:Line Number(s)) or (Patent, Paragraph Number(s)). For example, the citation (TSMC-1001, 1:1-10) points to the '764 patent specification at column 1, lines 1-10. Also, for convenience, I have been asked to use italics to denote limitations from the challenged claims. Unless otherwise noted, all emphasis added.

III. Understanding of Relevant Legal Principles

20. I am not a lawyer, and I will not provide any legal opinions. Although I am not a lawyer, I have been advised certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

A. Patent Validity

21. I understand that the prior art to the '764 patent includes patents and printed publications in the relevant art that (1) were published more than a year before the effective U.S. filing date of the application leading to the '227 patent (July 24, 2006), or (2) otherwise predate the '227 patent's foreign priority date (August 5, 2005), both of which I have been instructed to assume for purposes of my analysis that the '764 patent can claim the benefit of. I further understand that,

for purposes of this proceeding in the United States Patent Trial and Appeal Board, only patents and documents that have the legal status of a “printed publication” may be relied on as prior art.

22. I understand that a patent claim is anticipated if a single prior art document describes every element of the claim such that a person of ordinary skill in the art (“POSITA”) could practice the claimed method without undue experimentation.

23. I understand that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art. I further understand that in analyzing the obviousness of a claim, the following factors may be taken into account: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art; and (4) any so called “secondary considerations” of non-obviousness, if they are present. I am not aware of any evidence of secondary considerations of non-obviousness relevant to the ’764 patent. I reserve the right to supplement this Declaration if Patent Owner (“PO”) introduces evidence of secondary considerations of non-obviousness.

24. I understand that to prove that prior art or a combination of prior art renders a patent obvious, it is necessary to:

- (1) identify the particular references that, singly or in combination, make the patent obvious;

- (2) specifically identify which elements of the patent claim appear in each of the asserted references; and
- (3) explain why a person of ordinary skill in the art would have combined the references, and how they would have done so, to create the inventions claimed in the patent. I further understand that exemplary rationales that may support a conclusion of obviousness include:
 - combining prior art elements according to known methods to yield predictable results;
 - simple substitution of one known element for another to obtain predictable results;
 - use of known technique(s) to improve similar devices (methods or products) in the same way;
 - applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
 - “obvious to try” – choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
 - known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a person of ordinary skill in the art; and

- some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. I understand that anticipation or obviousness may be by express disclosure in the prior art. I also understand that a patent claim is invalid if it is anticipated or obvious in view of the prior art, and that a claim can be unpatentable even if all of the requirements of the claim cannot be found in a single prior-art reference. For example, I also understand that if the prior art references does not expressly set forth a particular claim element, the prior art may still anticipate or render obvious a patent claim if that element is “inherent” in its disclosure—that is, if it is necessarily found in the reference. A property is inherent even if a POSITA would not have appreciated that property as of the date of that prior art.

26. I understand that invalidity of a claim requires that the claim be anticipated or obvious from the perspective of a person of ordinary skill in the art at the time the invention was made. To that end, I understand that in considering obviousness, hindsight reasoning derived from the patent-at-issue may not be used.

27. I understand that some claims are independent, and that these claims are complete by themselves. Other claims refer to these independent claims and are “dependent” from those independent claims. The dependent claims include all of

the limitations of the claims on which they depend. Moreover, although I understand that preambles are not ordinarily treated as claim limitations, but for my declaration only, have been asked to complete my analysis as if the preambles were deemed limiting.

B. Claim Construction

28. I understand that “claim construction” is the process of determining a patent claim’s meaning. I understand the claim construction standard used in IPRs seeks to give claim terms their plain and ordinary meaning to a POSITA at the time of the claimed invention in view of the claims, specification, and prosecution history. I also understand that if the patent applicant gave a term a special meaning in the specification or during prosecution, then the special meaning should be used.

29. In my declaration, I apply the above understanding. In my view, no claim terms require explicit construction in this proceeding to resolve patentability of the claims.

C. Level of Ordinary Skill in the Art

30. I understand that certain issues relating to the validity of a patent must be judged from the perspective of a person of ordinary skill in the relevant art, as I discuss below. I have been asked to define the level of a “person of ordinary skill in the art” or “POSITA” at the time the alleged invention as claimed was made (which as discussed above, I have assumed to be August 5, 2005, for the ’764

patent). In deciding the level of ordinary skill, I have considered the following factors, which I have been informed are relevant to the determination of ordinary skill in the art.

- levels of education and experience of persons working in the field;
- types of problems encountered in the art;
- prior art solutions to these problems;
- rapidity with which innovations are made; and
- sophistication of the technology.

31. In my opinion, a POSITA at the time of the alleged invention of the '764 patent would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

32. My opinions regarding the level of ordinary skill in the art are based on, among other things, my experience conceiving, patenting, and prototyping novel technology for semiconductor devices and semiconductor fabrication processes. Although my qualifications and experience exceed those of the hypothetical person having ordinary skill in the art, my analysis and opinions

regarding the '764 patent have been based on the perspective of a person of ordinary skill in the art as of August 5, 2005.

IV. '764 Patent – Technical Background and Overview

33. The '764 patent, titled “Semiconductor Device and Method for Fabricating the Same,” to Junji Hirase, et al., was filed on July 20, 2009, as a divisional of the '227 patent, filed on July 24, 2006. The '227 patent claims priority to JP Application 2005-227457, filed on August 5, 2005. Solely for purposes of this IPR, I have been asked to assume August 5, 2005 as the earliest priority date claimed on the face of the '764 patent. However, my opinions set forth herein would not change if the priority date was determined to be July 24, 2006.

34. At a high level, the '764 patent relates to metal insulator semiconductor field-effect transistors (MISFETs) having a high dielectric constant (high-k) gate insulating film that (1) extends from under the gate electrode to under an insulating sidewall structure and (2) is high-k film thicker under the gate electrode than under the sidewall structure. (TSMC-1001, 1:15-21, 2:6-17, 2:35-44.) I will discuss these concepts, which were known in the art before the filing of the '764 patent, in greater detail below.

A. Technical Background

35. A semiconductor device is an electronic component that exploits the properties of semiconductor materials such as silicon, germanium, gallium arsenide, etc. Many types of semiconductor devices exist including, for example, diodes, metal-insulator-semiconductor (MIS) transistors (e.g., field effect transistors (FETs)), and memory devices, to name a few. (*See, e.g.*, TSMC-1033, 33-41.) In this Declaration, I will focus primarily on FET devices, and more particularly on MISFET devices which are described in further detail below.

1. MISFET/MOSFET

36. A metal-insulator-semiconductor field effect transistor (MISFET), also referred to as a metal-oxide-semiconductor field effect transistor (MOSFET) when the insulator is an oxide, is a common type of semiconductor device. Because most insulators traditionally used in FETs are oxides, it is common to use the terms MISFET and MOSFET interchangeably in the art. A typical MISFET device is a three-terminal structure with an input, referred to as the source, an output, referred to as the drain, and a control terminal, referred to as the gate electrode. (*See, e.g.*, TSMC-1033, 36.) Further to these terminals, the MISFET includes a gate insulating layer that electrically isolates the conductive gate electrode from a silicon substrate in which the source and the drain terminals are formed. (*See* TSMC-1041, 8 (MISFET “generally includes a stack of the

conducting gate, an insulating layer, and the silicon wafer, also called the substrate, body or bulk.”.) In principle, the MISFET operates as a current switch, conducting current in an area between the source and drain regions, referred to as the “channel” or the “channel region”, when an appropriate voltage is applied to the gate electrode. (TSMC-1041, 9) The gate electrode modulates the electric field across the insulator, controlling the behavior of the device, hence the term field-effect transistor or FET. (TSMC-1041, 9.)

37. When appropriate voltage is applied to the gate electrode, a conducting path of minority carriers forms the channel between the source and the drain, and current can flow between the source and the drain via the formed channel. (TSMC-1041, 9.) When the MISFET is conducting current, it is in the “ON” state. Once the voltage is removed from the gate, the channel disappears, and ideally there is no current flow between the source and the drain regions. In this non-conductive state, the MISFET is in the “OFF” state. (TSMC-1041, 9.)

38. MISFETs are fabricated on silicon wafers that serve as the **substrate**. The substrate provides both mechanical support and an electrical common point. (TSMC-1041, 23.) The substrate can be doped with impurities, known as dopants, to modulate its conductivity and influence the electrical behavior of the transistors built on it. (TSMC-1041, 7.) For example, doping the silicon substrate (or selective regions of the substrate) with boron (a Group III dopant) increases the number of

holes (positive doping or p-type) when it replaces a silicon atom in the silicon crystal lattice, while doping the silicon substrate (or selective regions of the substrate) with arsenic (a Group V dopant) increases the number of free *electrons* (negative doping or n-type) when it replaces a silicon atom in the silicon crystal lattice. (TSMC-1041, 7; TSMC-1033, 17.) “The electrons or holes are introduced on a one for one basis by the dopants.” (TSMC-1033, 17.) “[T]o the extent that we can control the doping concentration accurately, we can precisely control the free electron and hole concentrations and therefore the conductivity of the silicon.” (TSMC-1033, 17.)

39. Once implanted, dopants or impurities need to be **activated** via one or more anneal processes, which also intend to repair any damage introduced to the silicon crystal lattice by the implant process. (TSMC-1033, 81-82.) Accordingly, the terms n-type and p-type dopants, as customarily used in the art, indicate activated dopants—i.e., dopants that can act as a donor or acceptor of electrons and contribute to the conductivity of a doped region.

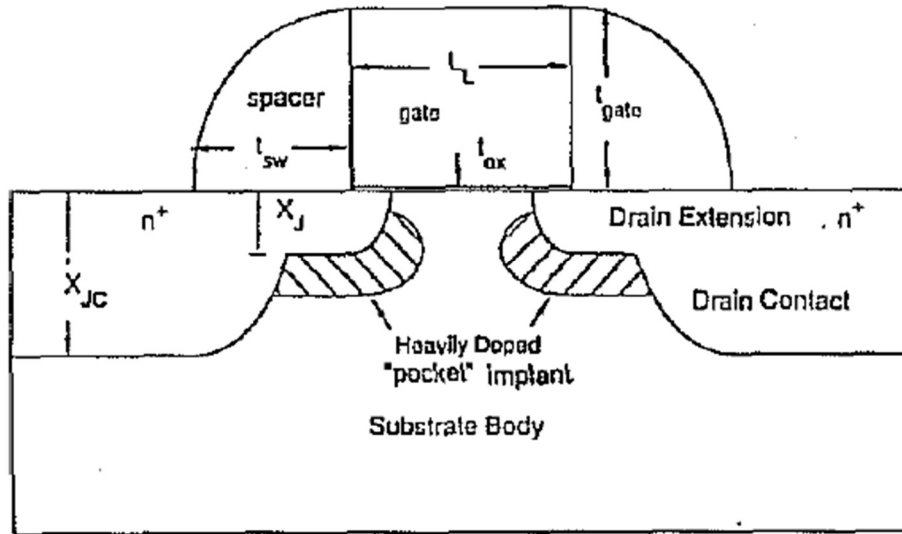
40. **Doped regions**—including wells, source/drain regions, and channel regions—are created in the substrate through a selective doping process known as ion implantation. (TSMC-1033, 375.) The source and drain regions, which are physically equivalent and therefore interchangeable, are formed by implanting dopants (either n-type or p-type) into the silicon substrate on either side of the gate

electrode. (TSMC-1041, 8.) These regions are intentionally heavily doped to improve the conductivity and facilitate current flow when the transistor is in the ON state. The formation of these regions is critical for defining the transistor's electrical characteristics.

41. In aggressively scaled MISFET devices, source and drain regions may include **source/drain extension (or SDE) regions**. SDE regions may be lightly doped extension regions, known in the art as Lightly Doped Drain (LDD), or heavily doped extension regions, known in the art as Highly Doped Drain (HDD) extension. (TSMC-1033, 77; TSMC-1023, 2:61-62, 3:65-67.) SDE regions provide a graded doping profile between the source/drain regions and the channel region that suppresses short channel effects by ensuring a gradual transition in the electric field between the source/drain and the channel. (TSMC-1033, 77-78.) “[M]odest reductions in the field strength obtained through the [SDE regions] can make a significant difference in device reliability. (TSMC-1033, 78.) Oftentimes, gate sidewall spacers are employed to control the position the leading edges of the SDE regions relative to the sidewall edges of gate electrode during the implant process. (TSMC-1033, 78.)

42. To further mitigate the short channel effects in aggressively scaled MISFET devices manifested by the presence of leakage current between the source and drain regions (known as punchthrough), **pocket implants** (also known as **halo**

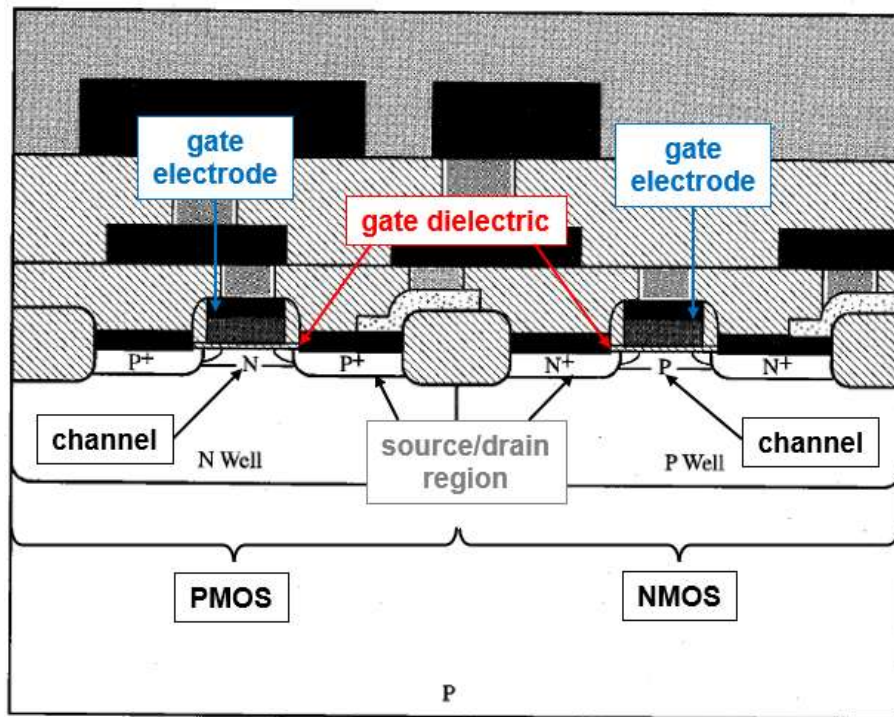
implants) are introduced just below the active channel and adjacent to the source/drain, as shown in Figure 5-27 below. (TSMC-1034, 219-20.)



Wolf, Figure 5-27

43. The dopant type of the pocket implants is **opposite** to that of the source/drain and SDE implants—i.e., the pocket implants have the **same** conductivity type with the well in which the source/drain and SDE regions are formed (*see* discussion below). (TSMC-1034, 219.) Thus, if the source/drain and SDE implants are p-type, the pocket implants are n-type, and vice versa. “Precise control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements.” (TSMC-1034, 219.)

44. MISFETs with n-type source/drain regions are referred to as **NMOS**, and MISFETs with p-type source/drain regions are referred to as **PMOS**. (TSMC-1033, 13, Figure 1-11.)



Plummer, Figure 1-11

45. In modern complementary metal-oxide-semiconductor (CMOS) technology, NMOS and PMOS are fabricated and integrated onto the same wafer. (TSMC-1033, 52 (“Modern CMOS chips integrate millions of active devices (and NMOS and PMOS) side by side in a common silicon substrate.”)) Each NMOS and PMOS transistor is formed over doped wells of opposite conductivity type. “These wells tailor the substrate doping locally to provide optimum device characteristics. The well doping affects device characteristics such as the MOS transistor threshold voltage and the I-V characteristics and PN junction capacitances” (TSMC-1033, 60.) For example, as shown in Figure 1-11 above, PMOS transistors are formed over an n-type well (N-well) and NMOS transistors

are formed over a p-type well (P-well). The N and P wells are created in the substrate, which in this case is a p-type substrate, through selective doping (i.e., by selectively masking areas not intended to receive a particular dopant). (*See, e.g.*, TSMC-1033, 60-63.) This arrangement of the CMOS technology enables the creation of high-performance, energy-efficient logic circuits.

2. Gate Insulating Film

a. Materials

46. A common feature of a FET is the gate insulator (also referred to as gate dielectric or gate insulating film), which electrically isolates the gate electrode from the semiconductor channel. (TSMC-1033, 288.) For decades prior to the '764 patent, silicon dioxide (SiO₂) was the primary material used for gate dielectrics in MOSFETs. (TSMC-1033, 53 (“SiO₂ is essentially a perfect insulator and provides the needed [electrical] isolation.”); TSMC-1032, 3-4.) However, as gate dielectric layers continued to shrink in thickness (e.g., below 1.5 nm), the use of SiO₂ became untenable, because the amount of gate-to-channel tunneling leakage current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON and OFF states of the FET. (TSMC-1034, 4-5, *see also* TSMC-1032, 5.)

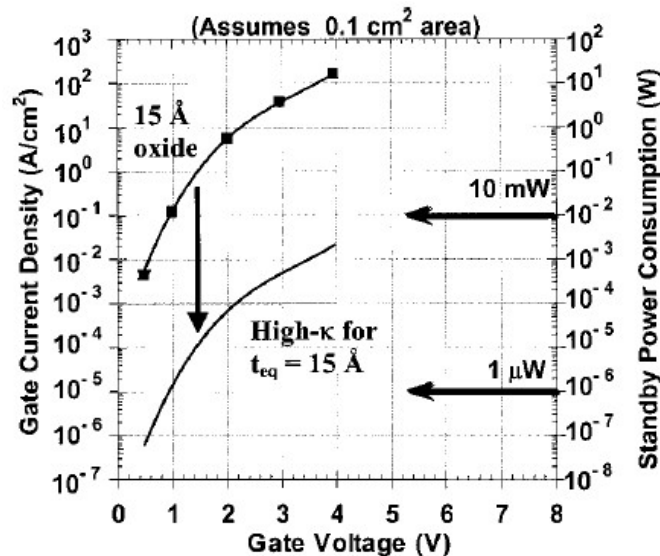
47. A metal-insulator-semiconductor structure behaves like a parallel plate capacitor with a capacitance, $C = \frac{A \epsilon_r \epsilon_0}{t_{ox}}$, where A is the capacitor plate area,

ϵ_r is the relative dielectric constant of the gate insulator (e.g., SiO_2), ϵ_0 is the permittivity of free space, and t_{ox} is the thickness of the gate insulator (e.g., SiO_2). (TSMC-1032, 8.) From the capacitance equation above, it is becoming apparent that decreasing the gate insulator thickness, t_{ox} , increases the capacitance, C , for the same gate voltage applied to the gate electrode. (TSMC-1032, 8.) However, as discussed above, the thickness of SiO_2 cannot be reduced indefinitely to increase or even sustain the same capacitance. Thus, “[a]n alternative way of increasing the capacitance is to use an insulator [a gate insulator] with a higher relative dielectric constant than SiO_2 [...]” (TSMC-1032, 8-9.) And because the dielectric would have a higher dielectric constant (i.e., a higher k value), this high- k dielectric could be thicker than SiO_2 and still achieve the same or higher capacitance value. This means that (i) the high- k would not suffer from the leakage current issues of SiO_2 , and (ii) the transistors can continue to scale. The term equivalent oxide thickness, t_{eq} , is used in the art in connection to high- k dielectrics, and is defined as the equivalent physical thickness of “the SiO_2 layer that would be required to achieve the same capacitance density as the high- k material in consideration.” (TSMC-1032, 9.)

48. High- k dielectrics, like Hf-based oxides, tantalum oxide (Ta_2O_5), or zirconium oxide (ZrO_2), were considered as potential candidates to replace SiO_2 and to address the challenges faced by SiO_2 . (TSMC-1034, 146.) Hafnium oxide

(HfO₂), in particular, became the material of choice due to its optimal dielectric constant (not too high or too low), thermal stability, and scalability. (TSMC-1049, 134.)

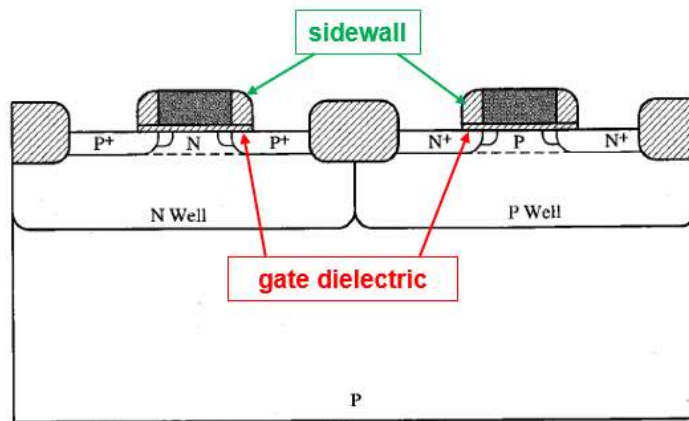
49. It was already known by 2005 that high-k materials substantially reduce the amount of leakage current compared to SiO₂ for the same equivalent oxide thickness and, thus, improve the semiconductor device's energy efficiency and reliability. (TSMC-1018, 5250, Figure 5 (below); Wolf 146-47.)



Wilk, Figure 5

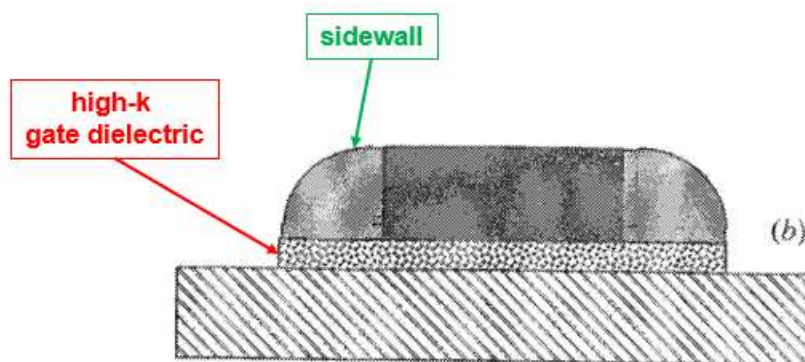
b. Extended Gate Insulating Films

50. Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under the gate sidewalls. For example, Plummer depicts a CMOS device having an extended gate dielectric in both the NMOS and PMOS transistors. (TSMC-1033, 82-83.)



Plummer, Figure 2-34

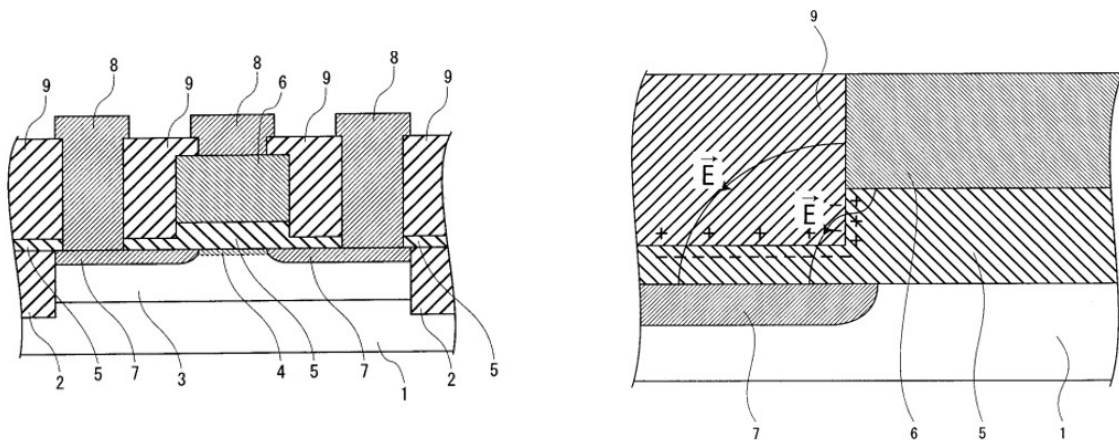
51. Houssa, which provides a MOSFET that uses a high-k material (e.g., HfO_2) as the gate dielectric material, explains that extending the gate dielectric under the sidewall spacers offers a process integration benefit—i.e., it relaxes the etch selectivity requirements between the high-k dielectric material and the silicon substrate. (TSMC-1032, 510; Figure 5.1.9(b).)



Houssa, Figure 5.1.9(b)

52. JP Publication 2005-064190 by Ono, et al. (“JP-Ono”¹; TSMC-1040), filed two years before the earliest priority date of the ’764 patent, discusses various benefits of extending a high-k gate dielectric beyond the gate edges. For example, JP-Ono explains that differing dielectric constants creates a concentration of electric field lines at the gate edge. (TSMC-1040, ¶ 6.)

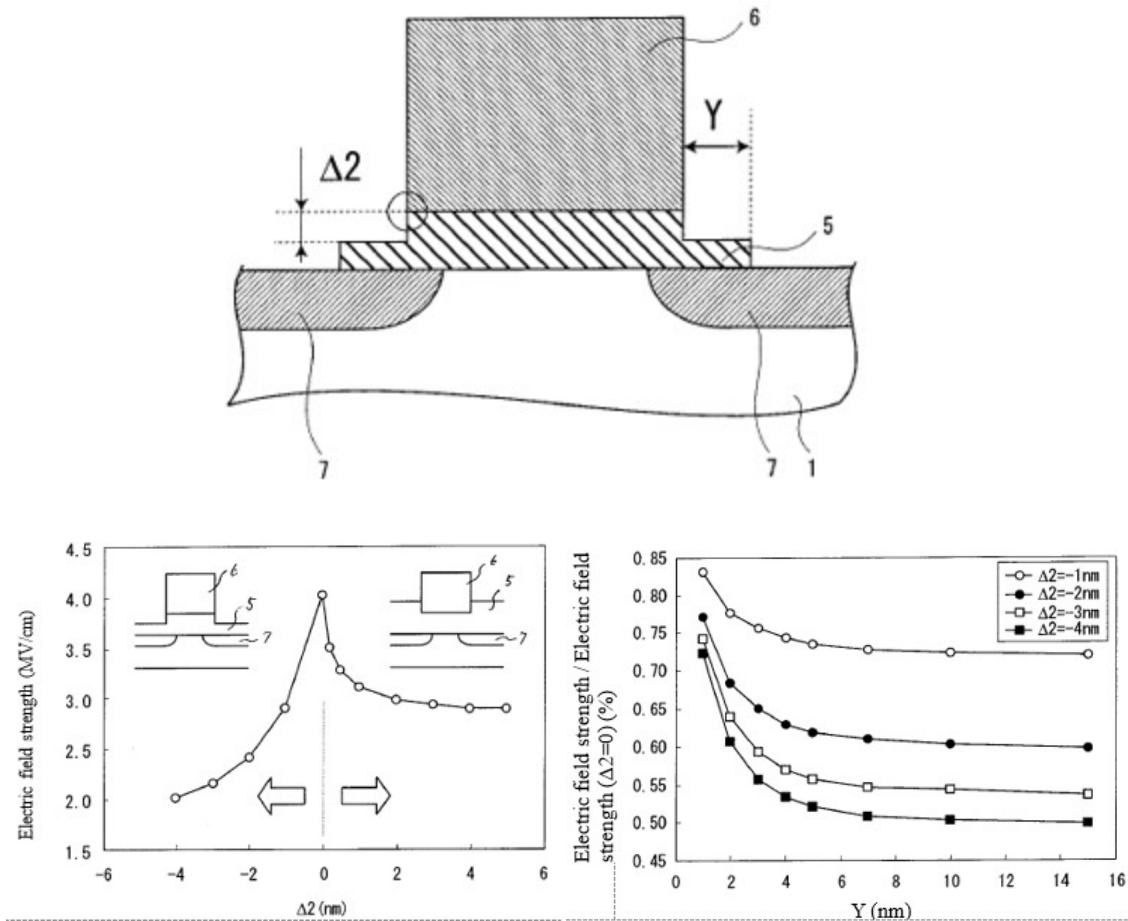
53. JP-Ono demonstrates that an extended gate dielectric mitigates field crowding at the gate electrode corners. (TSMC-1040, Abstract.) JP-Ono details how extending the gate dielectric to a thinner layer over the source/drain region minimizes the electric field, reinforcing the high-k dielectric’s performance under the sidewall structure. (TSMC-1040, ¶¶29-32, Figures 1-2 (below).)



JP-Ono, Figures 1 (left), 2 (right)

¹ A certified translation of JP-Ono is included with TSMC-1040.

54. JP-Ono examines how adjusting both the thickness reduction of the gate dielectric outside the gate electrode (Δt) and the extension length the gate dielectric from the lower gate electrode corners (Y) affects electric field distribution. Figure 4 (bottom-left) shows that when the thickness of the gate dielectric over the source/drain region matches its thickness under the gate, the electric field is at its highest intensity. (TSMC-1040, ¶34.) As the gate dielectric over the source/drain region becomes thinner, the electric field weakens, which favors a thinner dielectric in that area. (TSMC-1040, ¶35.) Figure 24 (bottom-right) further demonstrates that the electric field is reduced as the length of the gate dielectric extends farther from the lower gate electrode corner, i.e., as Y increases. (TSMC-1040, ¶87.)



JP-Ono, Figures 3 (top), 4 (bottom-left), 24 (bottom-right)

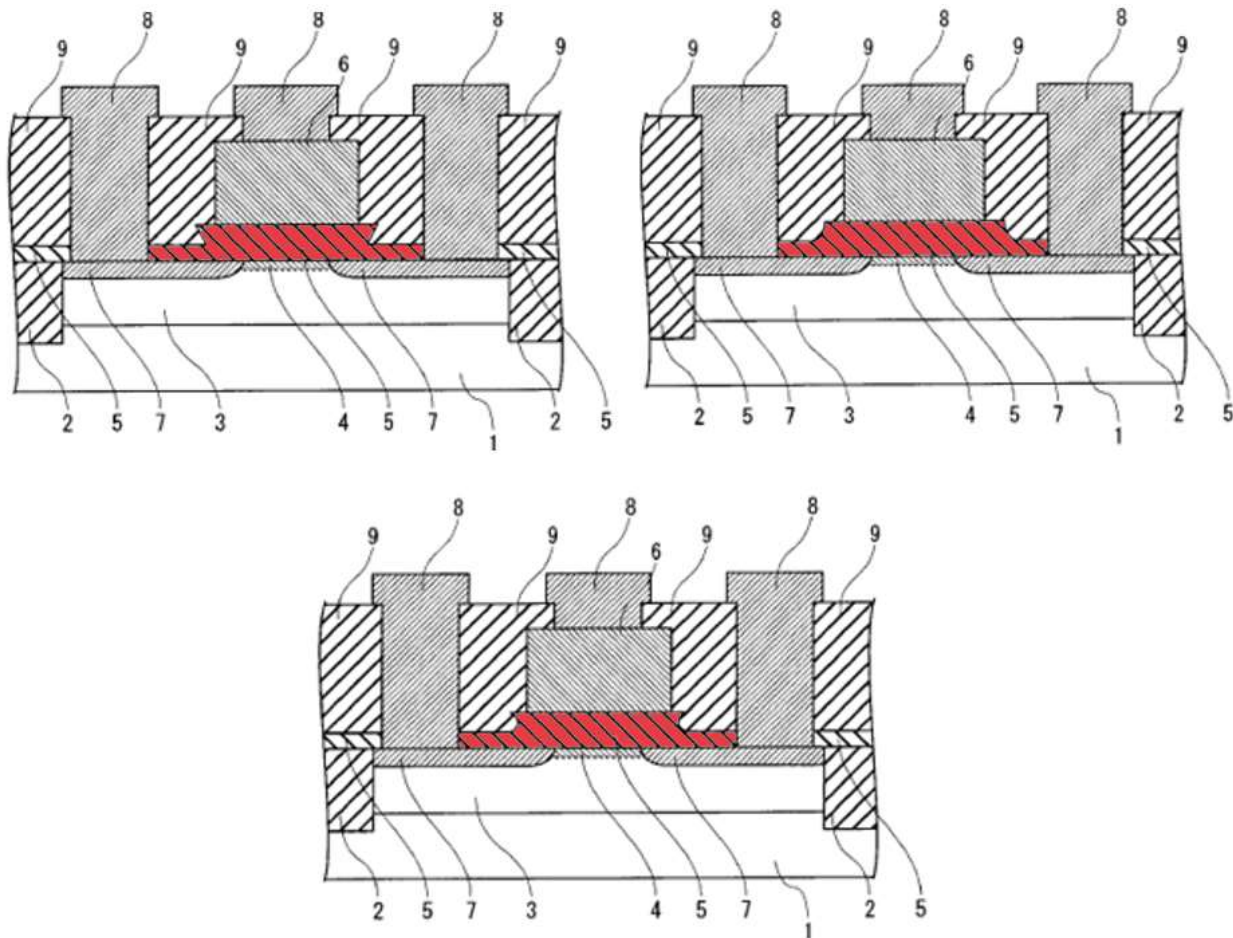
55. JP-Ono also describes the same improvements are achieved in a FET having a gate sidewall formed of silicon nitride or silicon oxide, such as that illustrated in Figure 23 below. (TSMC-1040, ¶83.)

15...シリサイド層

c. Varying the Location and Shape of the End of Gate Insulating Film

57. In Figures 36-44, JP-Ono illustrates various example shapes for the end of the gate insulating film (shaded red). (See, e.g., TSMC-1040, Figures 38,

41-42 (below).) JP-Ono explains that modifying the end shape allows for “optimization” of parasitic resistance and parasitic capacitance. (TSMC-1040, ¶108.) Although these figures are depicted without sidewall 10, JP-Ono describes that sidewall 10 may be included in the device, placing the gate dielectric end shape beneath the sidewall. (See TSMC-1040, ¶103.)



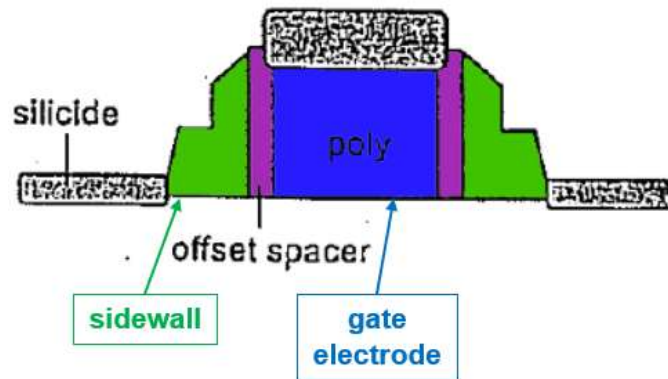
JP-Ono, Figures 38 (top-left), 41 (top-right), 42 (bottom)

3. Sidewalls/Spacers

58. Another common feature of the MISFET are the gate spacers or sidewalls, which are single layer or multilayer vertical insulating structures formed on or proximate to the side surfaces of a gate electrode. The terms “spacer,” “sidewall spacer,” and “sidewall” are sometimes used interchangeably in the art. Spacers/sidewalls (hereafter, spacers) serve a variety of purposes. For example, spacers are used to define the position of source/drain implants relative to the SDE implants, the gate electrode, and the channel region. (*See, e.g.*, TSMC-1032, 511; TSMC-1041, 122; TSMC-1034, 9, 217, 219.) Additionally, spacers can provide electrical isolation to the gate electrode by preventing shorts between silicided portions of the source/drain regions and the gate electrode. (TSMC-1033, 742.) This is because, spacers are made of a dielectric material such as SiO_2 and/or silicon nitride (Si_3N_4). (TSMC-1032, 511.) Spacers may also help control the gate width along the gate length direction. (TSMC-1051, ¶¶13-14, Figs. 2c, 2d.)

59. As a non-limiting example, spacers may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” so as to achieve the optimal amount of overlap between the SDE and the gate edge. (TSMC-1034, 217.) As shown in Wolf’s Figure 5-25 below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...),” with offset-spacer width “varied

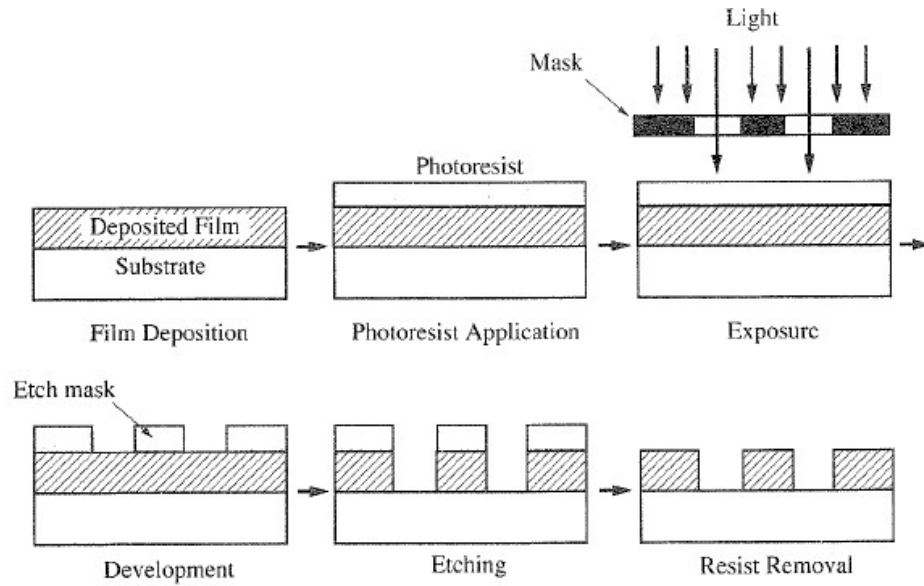
from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. (TSMC-1034, 217.)



Wolf, Figure 5-25

4. Etching Properties

60. In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. (TSMC-1033, 609-11.) The desired pattern is often defined by placing an etch mask over areas of the substrate to be protected from the etch process (e.g., by depositing and patterning an etch mask layer), subjecting both masked and unmasked portions to the etching chemistry so that unmasked areas are etched, and removing the etch mask when the etch process is complete. (TSMC-1033, 609-10, Figure 10-1 (below).) Gate electrodes and high-k gate insulating films are some examples of MISFET features formed by one or more combinations of deposition and etching processes.



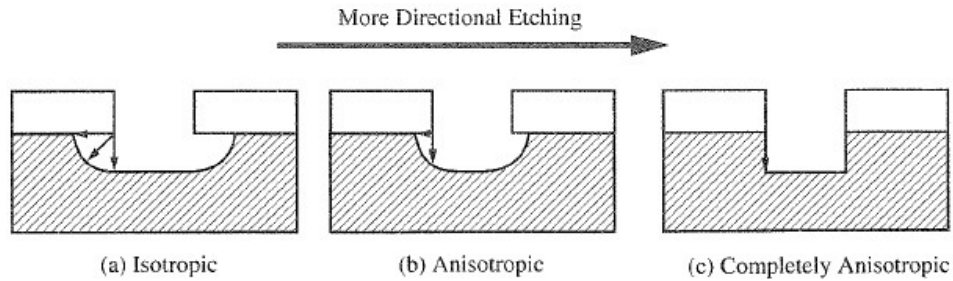
Plummer, Figure 10-1

61. Etching can be performed in a “wet” or “dry” environment. (TSMC-1033, 609, 612-37.) More specifically, wet etching uses liquid etchants (e.g., hydrofluoric acid, HF), whereas dry etching uses gas-phase etchants in a plasma. (TSMC-1033, 609, 612.) In wet etching, the wafers are immersed in an etching bath filled with an etchant solution and the exposed materials are etched mostly by a chemical process. (TSMC-1033, 609.) In dry etching, the wafers are exposed to the etching plasma where the materials are etched by a combination of chemical and physical processes. (TSMC-1033, 609.)

62. Depending on the etching chemistry used, the etch process parameters, and the etching selectivity between the materials being etched and those not etched, etching processes can develop different relative etch rates in different directions. (TSMC-1033, 609-11.) For example, the more physical an

etch process is (e.g., ion bombardment or sputtering), the more directional and less selective tends to be. (TSMC-1033, 611.) “On the other hand, the more chemical an etch process is, the more selective and the less directional it generally is.” (TSMC-1033, 611.) Directionality is often desirable because it “maintains lithographically defined feature sizes as they are transferred by etching into underlying films.” (TSMC-1033, 611.)

63. Isotropic etching is direction independent (i.e., the etch rate is similar in all directions) and can result in a semicircular etch profile as shown in Figure 10-3(a) below. Most wet chemical etchants etch isotropically. (TSMC-1033, 610-13.) On the other hand, anisotropic etching is more direction dependent and results in little or no etching in the lateral direction. (TSMC-1033, 611, Figure 10-3(b), (c) (below).) For example, anisotropic etching can have substantially higher etch rate in the vertical direction than in the lateral direction. However, for anisotropic etching, the amount of lateral etching may vary, such that the etched surface may be curved or sloped (TSMC-1033, Figure 10-3(b)) to completely vertical (TSMC-1033, Figure 10-3(c)).

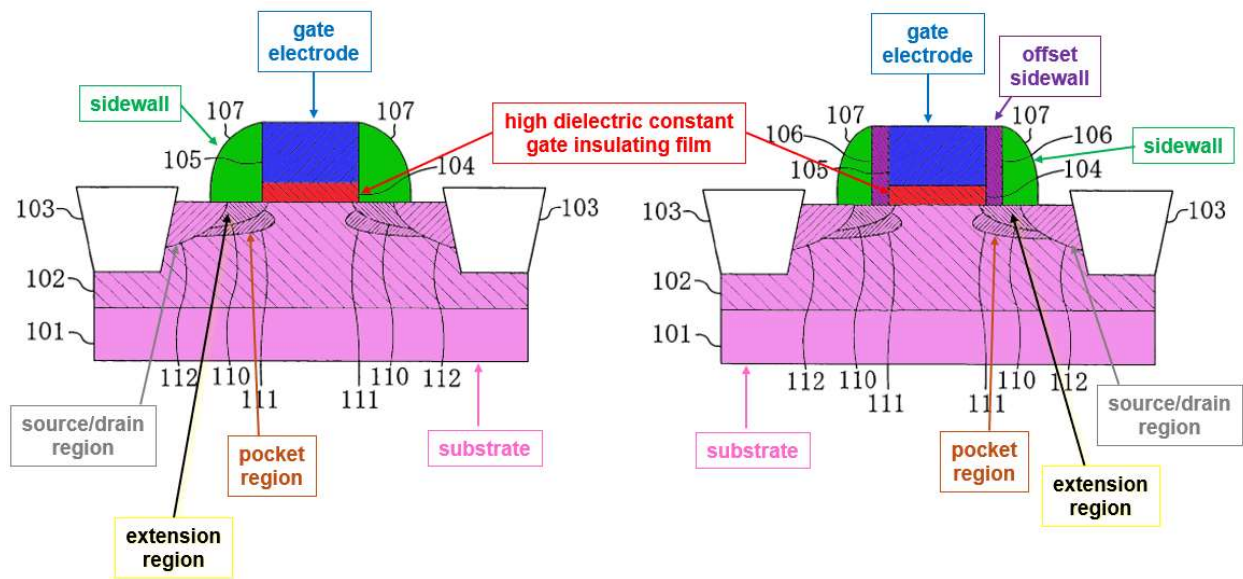


Plummer, Figure 10-3

B. Applicant Admitted Prior Art (“AAPA”)

64. As discussed above, semiconductor devices, such as MISFETs, existed for decades prior to the filing of the '764 patent. The '764 patent does not purport to invent the limitations of most of its claims, including, for example, high dielectric constant gate insulating film formed on a substrate, a gate electrode formed on the gate insulating film, or the use of insulating sidewalls. Rather, the '764 patent claims are directed to specific arrangements of gate insulating films and insulating sidewalls (which, as I will explain later in relation to the prior art grounds, were also well known).

65. For example, the '764 patent recognized that semiconductor devices using “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film already existed prior to its filing in 2005. (TSMC-1001, 1:23-31.) The '764 patent illustrates and describes two exemplary prior art devices in relation to Figures 16A and 16B.



'764 Patent, Fig. 16A (annotated left), '764 Patent, Fig. 16B (annotated right)

66. As shown above in Figures 16A and 16B, prior art devices included gate electrode 105 (shaded blue) “on a region of a well 102” surrounded by a shallow trench isolation (STI) 103 which served “as an active region” of substrate 101 (shaded pink). (TSMC-1001, 1:39-40.) A high dielectric constant (referred to herein as “high-k”) gate insulating film 104 (shaded red) lies between gate electrode 105 and the active region. (TSMC-1001, 1:43-44.) Each of these devices had insulating sidewalls (107 in Figure 16A; 106 and 107 in Figure 16B) formed on each side surface of the gate electrode.

C. '764 Patent Overview

67. According to the '764 patent, in prior art devices such as those shown in Figures 16A and 16B, the “side end portions” of the high-k film “are in direct contact with sidewalls,” which caused the reliability of the gate insulating film to

degrade. (TSMC-1001, 1:61-2:5.) The '764 patent purports to solve this problem by extending the high-k film at least partially under the insulating sidewalls.

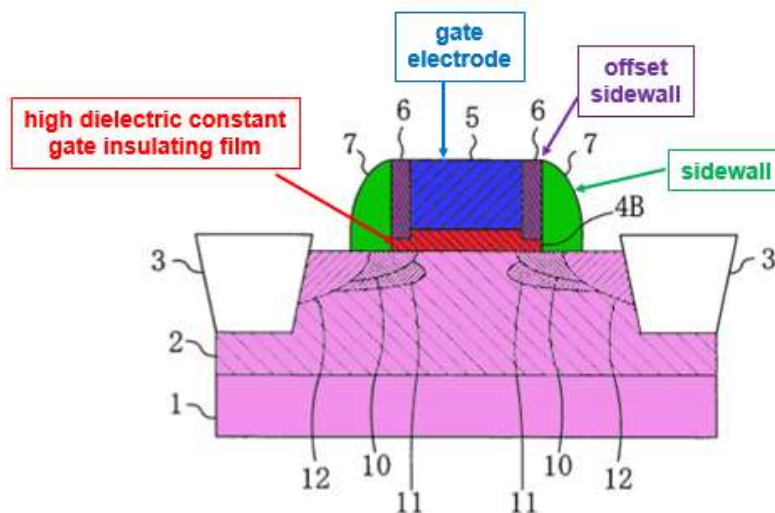
68. The '764 patent discloses several exemplary embodiments wherein the high-k gate insulating film extends at least partially under the insulating sidewall and is thinner under the insulating sidewall than under the gate electrode. This includes devices with a single sidewall (such as the first and fourth embodiments) and devices with double sidewalls (such as the second and third embodiments), as well as minor modifications thereof. The '764 patent's claims are specifically directed to double sidewall devices.

69. For example, independent claim 1 recites:

[1P]	1. A semiconductor device comprising:
[1A]	a high dielectric constant gate insulating film formed on an active region in a substrate;
[1B]	a gate electrode formed on the high dielectric constant gate insulating film;
[1C]	a first insulating sidewall formed on each side surface of the gate electrode; and
[1D]	a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween,

[1E]	wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and
[1F]	part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

70. Figure 2 of the '764 patent, which corresponds to the second embodiment of the '764 patent, illustrates an exemplary device covered by claim 1.

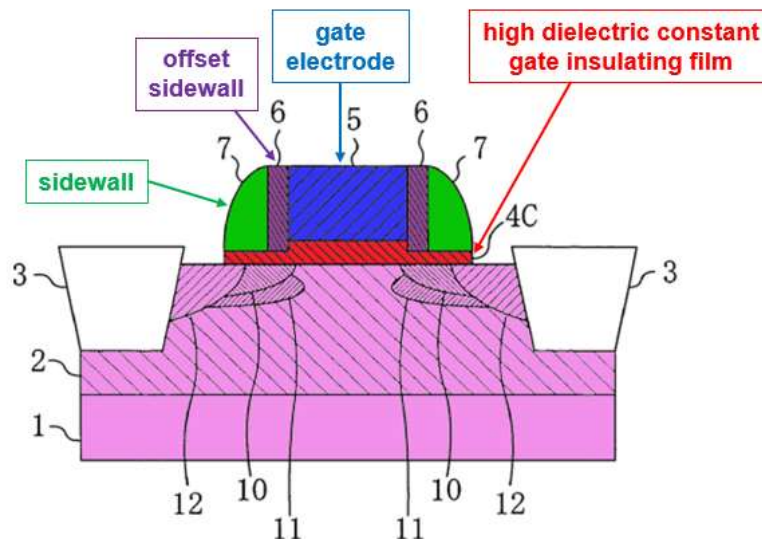


'764 Patent, Fig. 2 (annotated)

71. As can be seen in Figure 2, the high-k gate insulating film (shaded red) extends under first, or inner, sidewall 6 (shaded purple) and has a smaller thickness under inner sidewall 6 than under gate electrode 5 (shaded blue). This arrangement also satisfies the limitations of dependent claim 2, which recites “[t]he

semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall” because the high-k gate insulating film does not extend under the second sidewall 7 (shaded green).

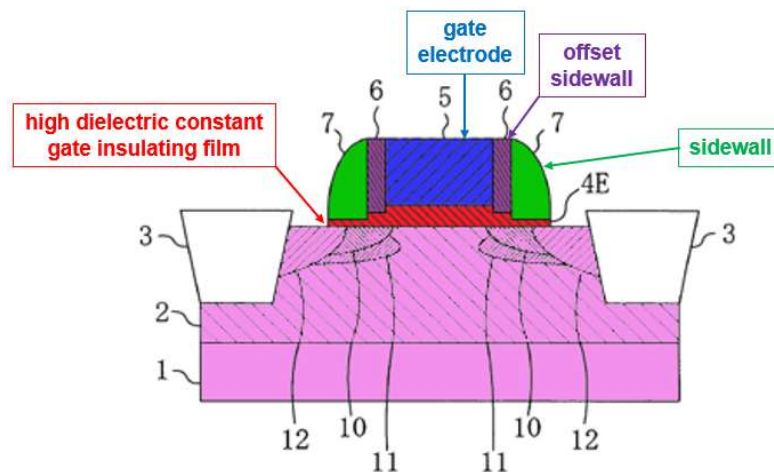
72. Figure 3, which shows a modification of the second embodiment of the '764 patent, illustrates another exemplary device covered by claim 1. Here, the high-k gate insulating film (shaded red) extends under both the first sidewall 6 (shaded purple) second sidewall 7 (shaded green), and has a smaller thickness under the sidewalls 6 and 7 than under gate electrode 5 (shaded blue).



'764 Patent, Fig. 3 (annotated)

73. Figure 5 of the '764 patent, which corresponds to the third embodiment of the '764 patent device (Figure 5 below), illustrates another exemplary device covered by claim 1. Here, the high-k gate insulating film (shaded

(TSMC-1001, 10:53-62).



'764 Patent, Fig. 5 (annotated)

D. Prosecution History

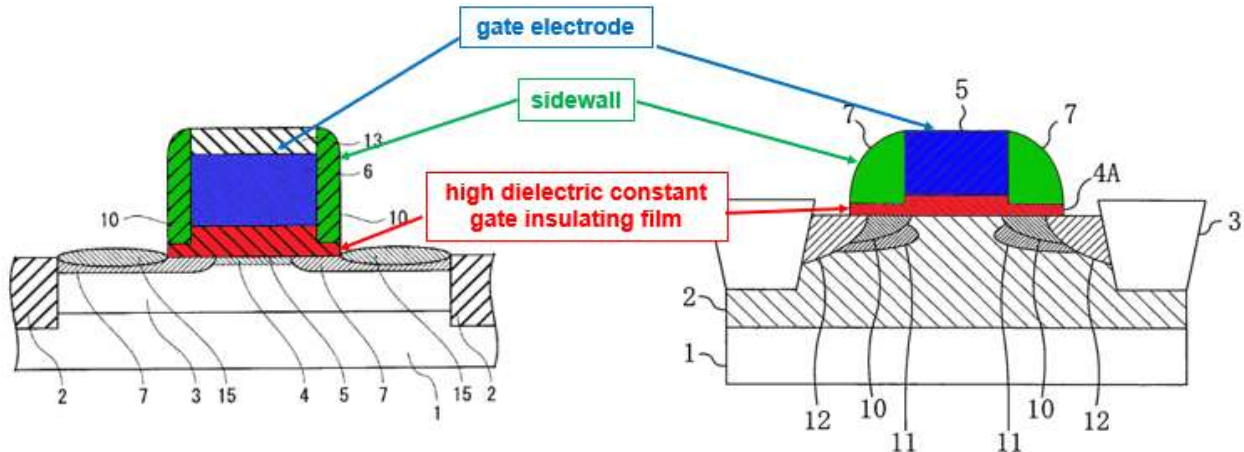
1. U.S. Prosecution of the '764 Patent

74. The U.S. application leading to the '764 patent was filed with one independent claim corresponding to issued claim 1. The Examiner rejected this claim as anticipated by U.S. Patent 6,992,358 to Hieda ("Hieda"). (TSMC-1002, 122-23.) Applicant did not amend the claims, but rather successfully argued that the Examiner misapplied Hieda. (TSMC-1002, 142-44, 159.)

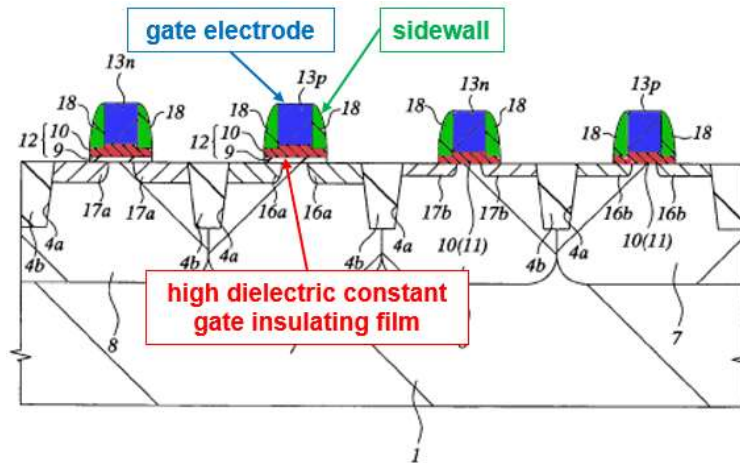
2. Japanese Prosecution

75. I have also reviewed a translated version of the prosecution history for the Japanese application that the '227 and '764 patents claim priority to.

76. The Japanese priority application was filed with the same single-sidewall device claim originally filed with the '227 application. (TSMC-1005, 1.) On September 16, 2011 (after the '764 patent issued in the United States), the Japanese Examiner found this claim scope unpatentable, citing JP2005-064190 to Ono ("Ono '190") and WO2004/017418 to Sakai, et al. ("Sakai"). (TSMC-1005, 52-55). As shown in Figure 23 of Ono and Figure 25 of Sakai, these references both teach a high-k gate insulating film that extends past the gate electrode under the insulating sidewall, and has a smaller thickness under the sidewall than under the gate electrode, like e.g., the '764 patent's single sidewall embodiments. (TSMC-1001, Figure 1.)



Ono '190, Fig. 23 (annotated left); '764 Patent, Fig. 1 (annotated right)

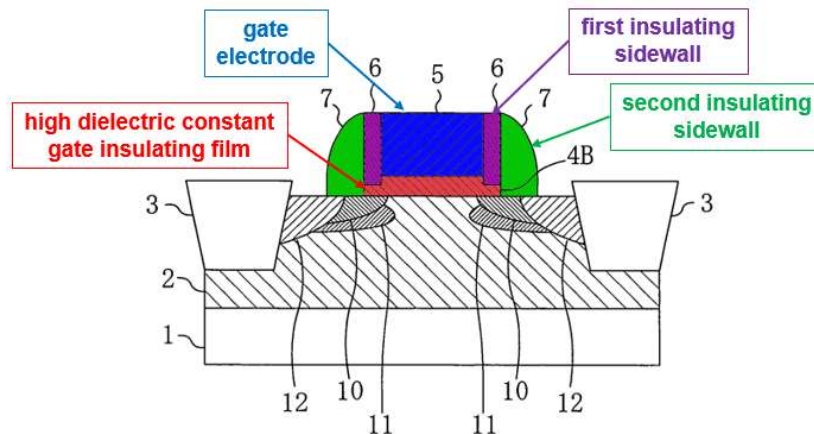


Sakai, Figure 25 (annotated)

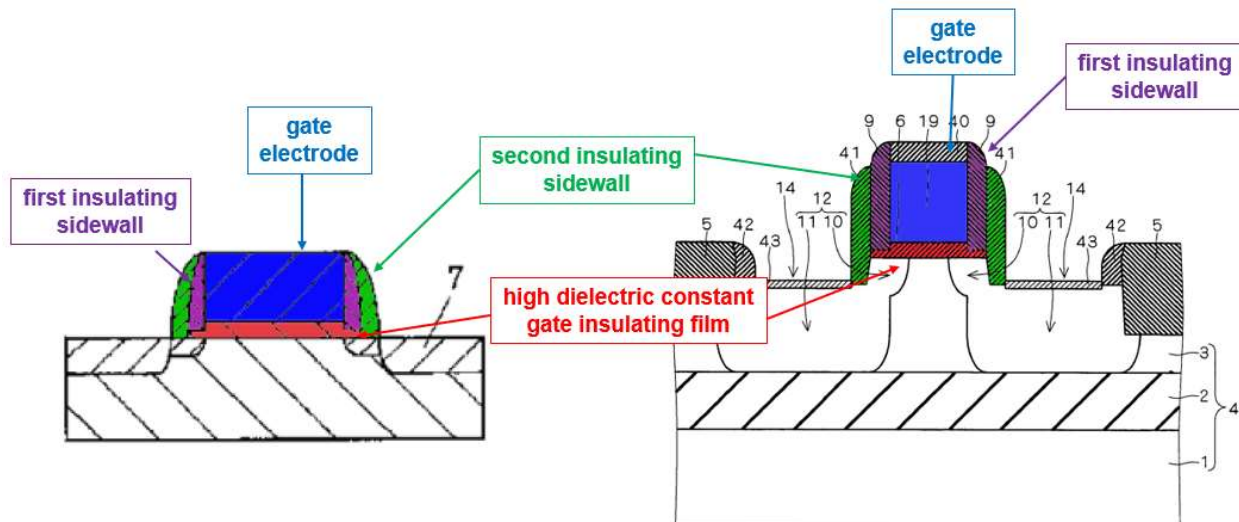
77. In response, Applicant narrowed the Japanese claim to recite (1) a *double* sidewall structure with a high-k film having a smaller thickness under a first sidewall than under the gate electrode and (2) extension and source/drain regions. (TSMC-1005, 56.) The Japanese Examiner then rejected the amended claim based on both JP 2003-258241 to Kajiyama (“JP-Kajiyama” (TSMC-1010)) and JP 2004-241755 to Matsumoto (“JP-Matsumoto”). (TSMC-1005, 64-65.) As

shown in Figure 1(D) of JP-Kajiyama and Figure 33 of JP-Matsumoto, both of these references teach the same basic structure as the '764 patent's Figure 2.

(TSMC-1005, 64-65; *compare* TSMC-1001, Figure 2.)



'764 Patent, Figure 2 (annotated)



**JP-Kajiyama, Fig. 1(D) (annotated left);
JP-Matsumoto, Fig. 33 (annotated right)**

78. In response to that rejection, Applicant further narrowed the claim to recite that the thickness of the high-k gate insulating film under the second

sidewall is smaller than the thickness under the first sidewall which is smaller than the thickness under the gate electrode, an arrangement that corresponds to the '764 patent's third embodiment. (TSMC-1005, 18.) The JP Examiner allowed the claim based on this amendment. (TSMC-1005, 20.)

79. In my opinion, based on this prosecution history, the applicant acquiesced during the co-pending Japanese prosecution that devices corresponding to the '764 patent's issued claim 1 were known in the art before the '764 patent.

V. GROUND 1: Matsumoto Renders Claims 1, 4-5, and 14-21 Obvious.

A. Overview of Matsumoto

80. Matsumoto, titled "Semiconductor Device and Method for Manufacturing Same," to Takuji Matsumoto, et al. ("Matsumoto"; TSMC-1009) was filed on July 11, 2002, claiming priority to a JP application filed on July 17, 2001, and was published on February 6, 2003.

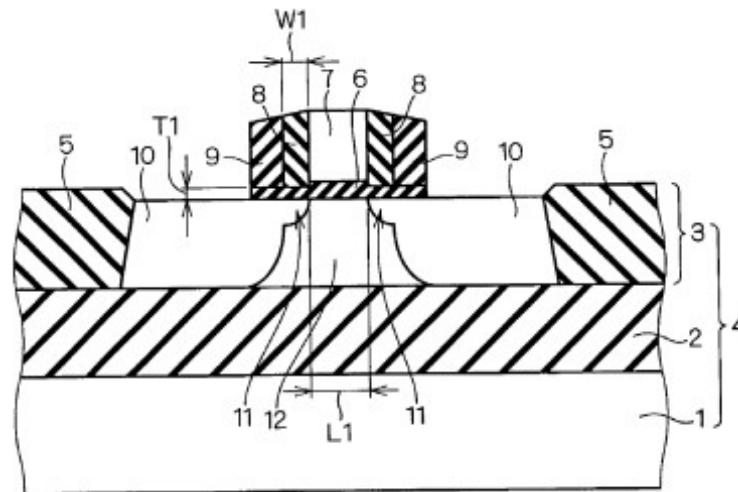
81. Similar to the '764 patent, Matsumoto relates "to a semiconductor device" and more specifically to an improved MOSFET (Metal Oxide Semiconductor Field Effect Transistor), and methods for manufacturing the same. (TSMC-1009, Abstract, ¶2.) Matsumoto discloses several illustrative embodiments, and optional modifications of those embodiments, of a semiconductor device having a gate electrode, insulating sidewalls on the side of the gate electrode, and a gate insulating film that extends from under the gate

electrode to the under the insulating sidewalls.² According to Matsumoto, the “increased base width of a parasitic bipolar transistor reduces the gain of the

² Although Matsumoto discloses several embodiments and modifications, many of the fabrication steps are discussed in relation to the first embodiment. (*See, e.g.*, TSMC-1009, ¶123 (“The remaining structure of the semiconductor device according to the second preferred embodiment is similar to the corresponding structure of the above-stated semiconductor device according to the first preferred embodiment shown in FIG. 1.”), 137 (“Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment....”).) Moreover, Matsumoto repeatedly explains, and a POSITA would have thus understood, that the teachings of one embodiment (or modification thereof) could be readily applied to other embodiments. (*See, e.g.*, TSMC-1009, 140 (“The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments.”), 141 (“The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments.”), 143 (“The technique of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment.”).)

parasitic bipolar transistor, thereby to suppress malfunctions and operating characteristic variations of the MOSFET. Additionally, a decreased amount of overlap between the gate electrode and the extensions as viewed in plan suppresses a gate overlap capacitance to achieve the increase in operating speed and the reduction in power consumption.” (TSMC-1009, ¶15.)

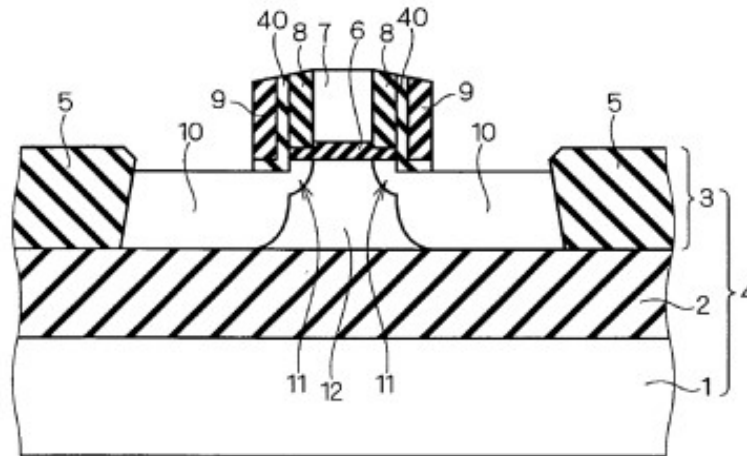
82. In my opinion, the first and fourth embodiments of Matsumoto, at a minimum, render claims 1, 4-5, and 14-21 of the '764 patent obvious. As shown in Figure 1 below, Matsumoto's first embodiment has a gate insulating film 6 extends from under the gate electrode 7 to under both sidewalls 8 and 9, just like Figure 3 of the '764 patent. (See TSMC-1009, ¶103.)



Matsumoto, Fig. 1

83. As shown in Figure 22 below, Matsumoto's fourth embodiment includes a gate insulating film 6 extending from under the gate electrode 7 to under

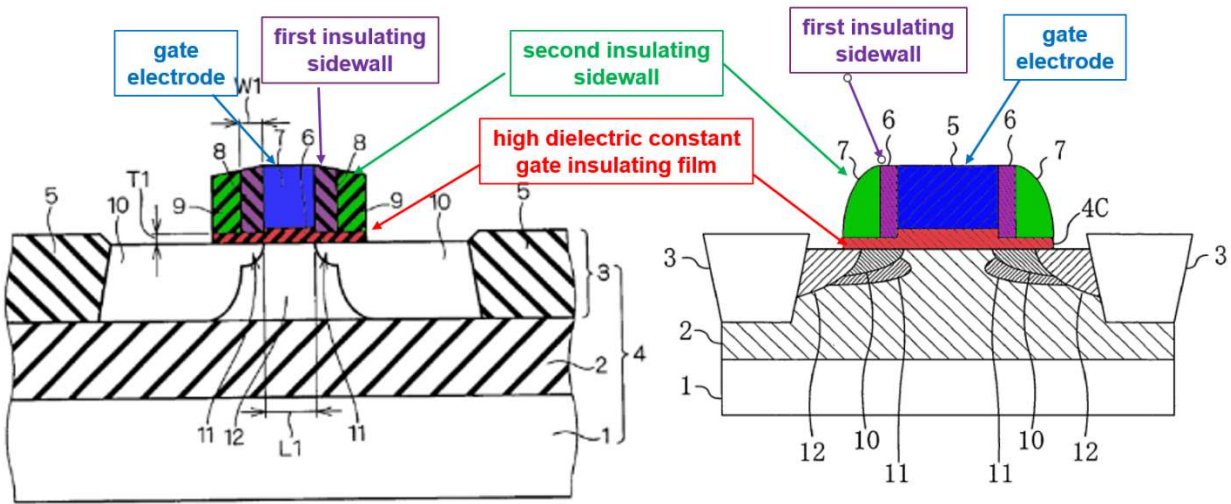
only the sidewall film 8, comparable to Figure 2 of the '764 patent. (*See* TSMC-1009, ¶¶138-140.)



Matsumoto, Fig. 22

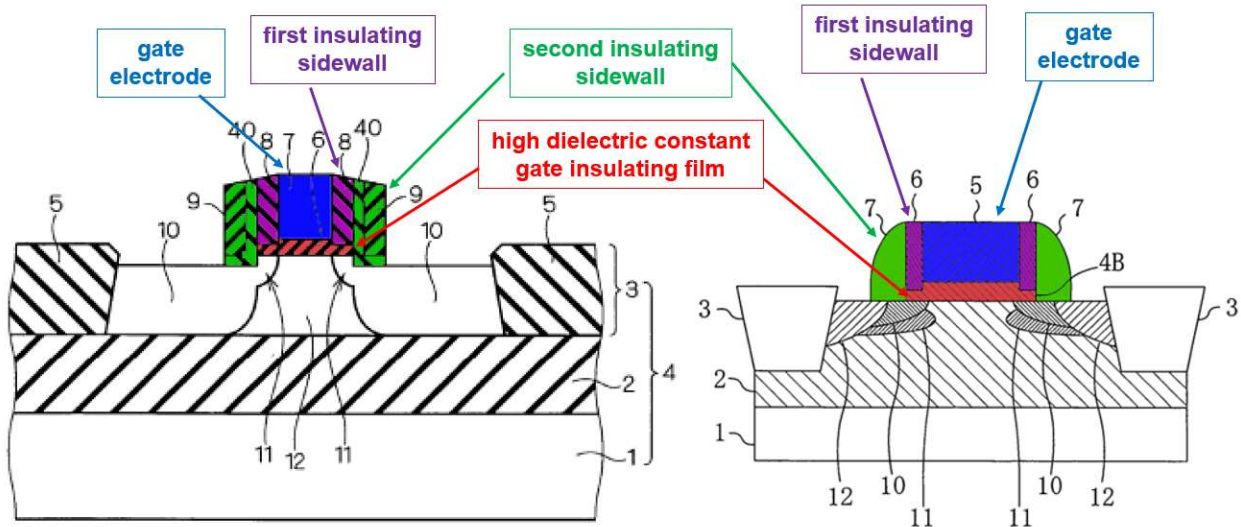
B. Independent Claim 1

84. In my opinion, the semiconductor devices of Matsumoto's first and fourth embodiments render claim 1 obvious. The similarity between Matsumoto's first embodiment and the '764 patent can be seen in the side-by-side figures from Matsumoto (left) and the '764 patent (right), below.



Matsumoto, Fig. 1 (annotated left); '764 Patent, Fig. 3 (annotated right)

85. The similarity between Matsumoto's fourth embodiment and the '764 patent also can be seen in the side-by-side figures from Matsumoto (left) and the '764 patent (right), below.



**Matsumoto, Fig. 22 (annotated left);
'764 Patent, Fig. 2 (annotated right)**

1. Preamble

[1P] *A semiconductor device comprising:*

86. Matsumoto's first embodiment and fourth embodiments are each a "*semiconductor device*," such as shown in Figures 1 and 22 of Matsumoto, above. Matsumoto is entitled "Semiconductor device and method of manufacturing same," and discloses that "[t]he present invention relates to **a semiconductor device**." (See, e.g., TSMC-1009, ¶¶2, 102, 137; see also TSMC-1009, Abstract ("A semiconductor device").)

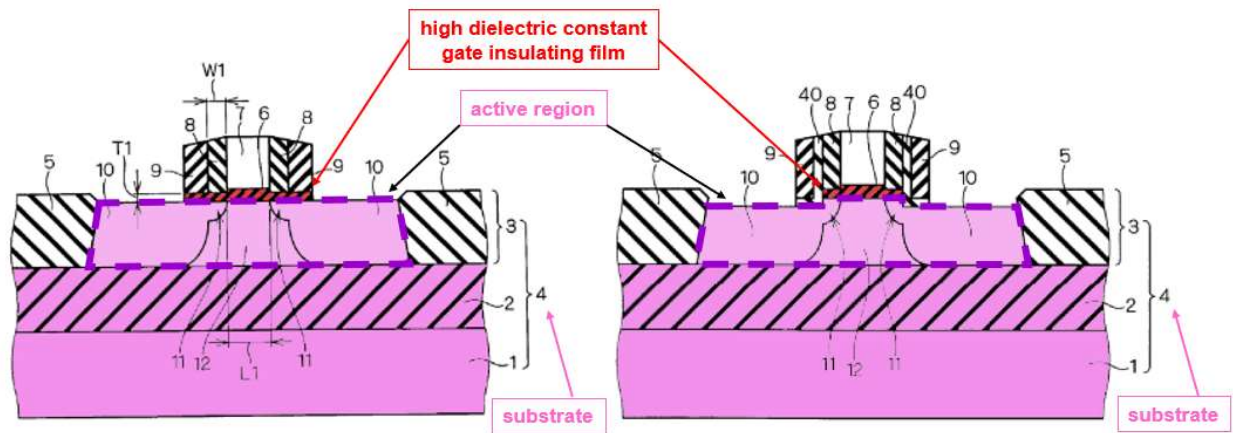
2. Limitation [1A]

[1A] *a high dielectric constant gate insulating film formed on an active region in a substrate*

87. Matsumoto's first and fourth embodiments each includes "*a high dielectric constant gate insulating film formed on an active region in a substrate*" [1A].

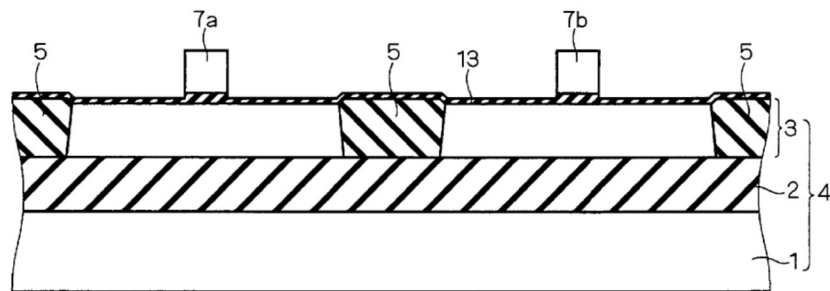
88. Matsumoto discloses that these embodiments include a substrate, disclosing that its device has a multi-layer SOI **substrate 4** (shaded pink) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3 "stacked in the order named." (TSMC-1009, ¶102; see also TSMC-1009, ¶137 (relating process steps of first embodiment through forming gate electrode to fourth embodiment), ¶140 (relating fourth embodiment to first embodiment).)

89. Matsumoto discloses that these embodiments include *an active region* in a substrate, explaining that, for example, “isolating insulation film 5 extends from the upper surface of the silicon layer 3 to the upper surface of the BOX layer 2,” and that the “MOSFET is formed in a **device region** defined by the isolating insulation film 5.” (TSMC-1009, ¶¶102-03.) The device region, identified by isolation regions, is an “*active region in a substrate*” and includes source/drain regions 10. (TSMC-1009, ¶¶103-05, 139). This is consistent with the disclosure of the ’764 patent, which confirms that the boundaries of an “*active region*” are defined by isolation structures. (See TSMC-1001, 1:39-40 (“The region of the well 102 surrounded by the STI serves as an **active region** of a substrate 101”), 7:30-47 (active region includes source/drain regions surrounded by STI isolation structures).) The *active region* (outlined in magenta) *in a substrate* (shaded pink) is shown in Figures 1 (first embodiment) and 22 (fourth embodiment) of Matsumoto, below.



Matsumoto, Figs. 1 (annotated left) and 22 (annotated right)

90. A POSITA would have understood Matsumoto's film 6 to be the claimed gate insulating film. (TSMC-1009, ¶103 (referring to film 6 as a "gate insulation film").) In both the first and fourth embodiments of Matsumoto, "silicon oxide film 6 is formed partially on the upper surface of the silicon layer 3" in the device region and gate electrode 7 "is formed partially on the silicon oxide film 6." (TSMC-1009, ¶103 (first embodiment), ¶137 (in fourth embodiment, "gate electrode 7 is formed by the process described in the first embodiment").) This is done by forming film 13 on the substrate, as shown in Figure 4, below.



Matsumoto, Fig. 4

91. After one or more sidewalls are formed, film 13 is etched to form film 6. (See TSMC-1009, ¶107, Figure 1, 9-10, ¶114 (first embodiment); TSMC-1009, ¶138, Figures 18-19, 22 (fourth embodiment).)

92. Although Matsumoto uses silicon oxide as its illustrative embodiment, and does not use the words “high dielectric constant” to describe its gate insulating film, a POSITA would have nevertheless understood Matsumoto to disclose the use of a high dielectric constant gate insulating film. At a minimum, a POSITA would have considered it obvious. This is because Matsumoto teaches that “[a] silicon oxynitride film, a metal oxide film such as Al_2O_3 or a ferroelectric film such as Ta_2O_5 and BST may be formed in place of the silicon oxide film 13.” (TSMC-1009, ¶107). Al_2O_3 , Ta_2O_5 , and BST are, and were understood to be, high-k dielectrics. (See TSMC-1018 (Wilk), Table I (identifying Al_2O_3 , Ta_2O_5 as high-k dielectrics).) The ’764 patent itself acknowledges this, explaining that it was known to use, “as a gate insulating film of a MISFET, a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more.” (TSMC-1001, 1:23-31). Al_2O_3 is an example of an “Al based oxide” as recited by the ’764 patent, and Ta_2O_5 and BST are also understood to have dielectric constants greater than 10.

93. A POSITA would have been motivated to use a high-k dielectric in the first and fourth embodiment devices, such as those disclosed by Matsumoto or

otherwise known in the art, to address the well-documented issues with silicon dioxide gate dielectrics in ultra-large-scale integration devices having scaled down features. (See TSMC-1032, 3-12; TSMC-1034, 4-5, 146-47.)

94. Thus, in both the first and fourth embodiments of Matsumoto, film 6 is formed between the substrate's active region and gate electrode, and constitutes "*a high dielectric constant gate insulating film formed on an active region in a substrate*" [1A].

3. Limitation [1B]

[1B] <i>a gate electrode formed on the high dielectric constant gate insulating film</i>
--

95. Matsumoto's first and fourth embodiments are semiconductor devices that include "*a gate electrode formed on the high dielectric constant gate insulating film*" [1B].

96. In both embodiments, "**gate electrode 7** made of polysilicon **is formed partially**" on high-k gate insulating film 6. (TSMC-1009, ¶103 (first embodiment), ¶107 (describing formation of high-k insulating film and gate electrode), ¶¶137-138 (fourth embodiment).) In both cases, gate electrode 7 (shaded blue) is formed over the high dielectric constant gate insulating film 6 (shaded red), as shown in Figures 1 and 22 of Matsumoto, below.



Matsumoto, Figs. 1 (annotated left), 22 (annotated right)

4. Limitations [1C]-[1D]

[1C] a first insulating sidewall formed on each side surface of the gate electrode; and

[1D] a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween

97. In my opinion, Matsumoto’s first and fourth embodiments disclose “a *first insulating sidewall formed on each side surface of the gate electrode*” [1C] and “a *second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween*” [1D].

98. Both Matsumoto's first and fourth embodiments have an insulating sidewall that comprises first and second insulating sidewalls.

99. In Matsumoto’s first embodiment, “silicon nitride film 9 is formed on each side surface of the gate electrode 7, with a silicon oxide film 8 therebetween.” (TSMC-1009, ¶103.) A POSITA would have understood film 8 to be the claimed

first insulating sidewall and film 9 to be the claimed second insulating sidewall.

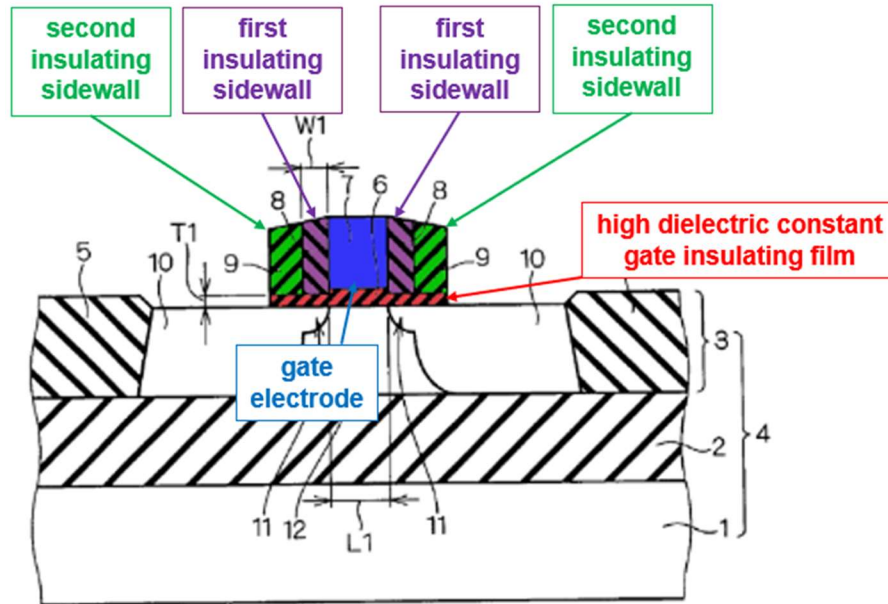
Matsumoto expressly refers to film 9 as a “sidewall insulation film.” (TSMC-1009, ¶114 (describing nitride films 9a/9b “serving as **sidewall** insulation films”).)

Matsumoto, however, does not refer to film 8 as a sidewall. A POSITA would nevertheless have understood film 8 to also be a sidewall. (TSMC-1009, ¶¶104, 110.) A POSITA also would have known that silicon oxide and silicon nitride are both insulators, and thus films 8 and 9 are insulating sidewalls. (*See* TSMC-1009, ¶110 (“This forms silicon oxide films 8a and 8b on the side surfaces of the gate electrodes 7a and 7b.”); TSMC-1009, ¶114 (“This forms silicon nitride films 9a and 9b serving as sidewall insulation films on the outer side surfaces of the silicon oxide films 8a and 8b.”); TSMC-1009, claim 1 (“a pair of second insulation films having respective inner side surfaces in contact with side surfaces of said gate electrode and respective outer side surfaces out of contact with said side surfaces of said gate electrode, with said gate electrode disposed between said pair of second insulation films”).)

100. As illustrated below, in Matsumoto’s first embodiment, film 8 (shaded purple) is “*a first insulating sidewall formed on³ each side surface of the gate*

³ The ’764 patent uses the term “*formed on*” generally to refer to location and does not require contact. (*See, e.g.*, TSMC-1001, 1:37-39, 7:33-37). For

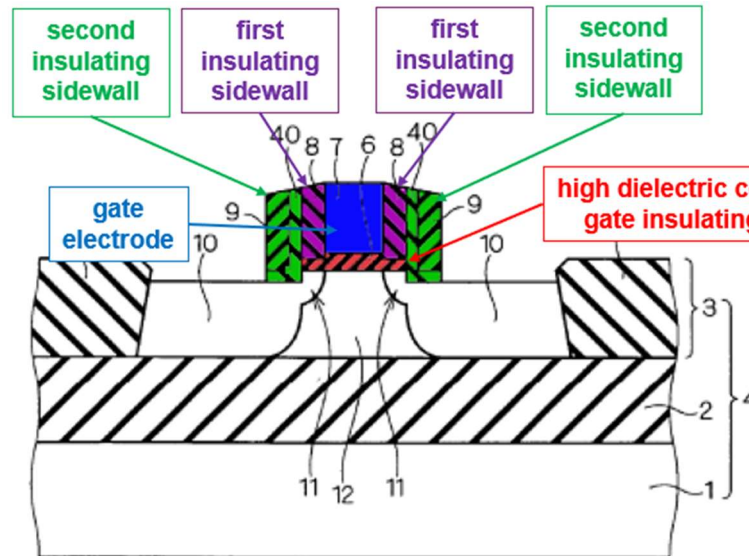
electrode” [1C] and film 9 (shaded green) being the “second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween” [1D].



Matsumoto, Fig. 1 (annotated)

example, claim 1 recites “a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween.” (TSMC-1001, claim 1.) The second insulating sidewall is still “formed on the side surface of the gate electrode” even though “the first insulating sidewall [is] interposed therebetween,” meaning that the second insulating does not directly contact the gate electrode.

101. In the fourth embodiment, silicon oxide film 40 and silicon nitride film 9 are formed “on the outer side surfaces of” film 8. (See TSMC-1009, ¶139.) This is shown in Figure 22 below.



Matsumoto, Fig. 22 (annotated)

102. As shown in Figure 22, in Matsumoto’s fourth embodiment, film 8 (shaded purple) is “a first insulating sidewall formed on each side surface of the gate electrode” [1C] and film 9 (shaded green) alone, film 40 (shaded green) alone or their combination⁴ is “a second insulating sidewall formed on said each side

⁴ The ’764 patent uses the term “insulating sidewall” broadly to refer to a single component (6:4-5), a collective structure of two components (3:22-28), and a component having multiple layers (20:66-21:8). Moreover, Figure 23 of Matsumoto shows a modification of Matsumoto’s fourth embodiment. (TSMC-

surface of the gate electrode with the first insulating sidewall interposed therebetween” [1D], consistent with the disclosures of the ’764 patent.

5. Limitations [1E]-[1F]

[1E] *wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall; and*

[1F] *part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode*

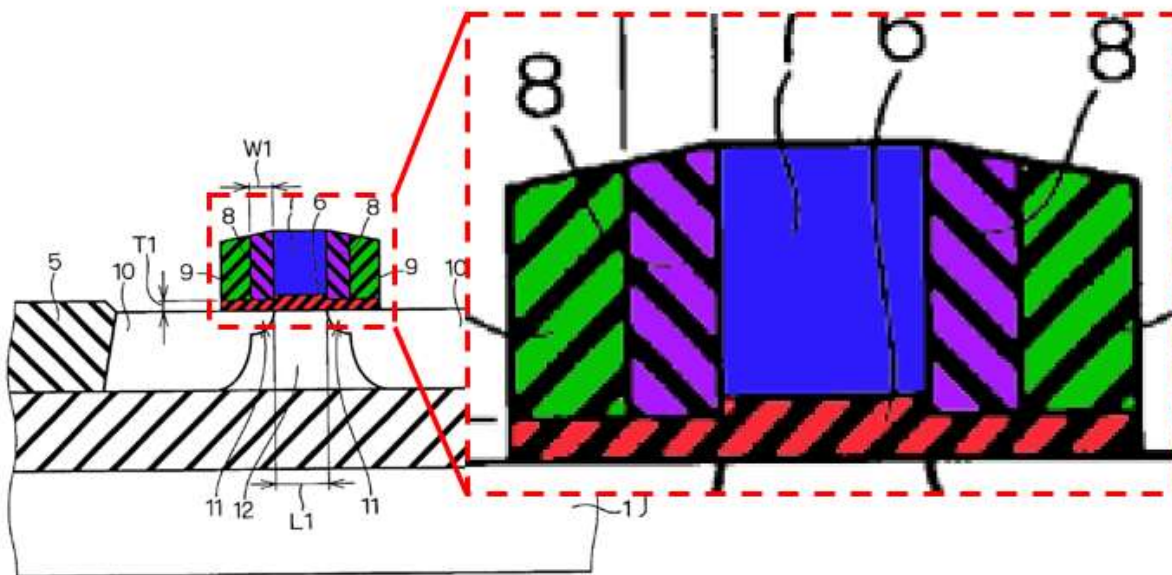
103. Limitation [1E] recites “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode **to under the first insulating sidewall***” and limitation [1F] recites “*part of the high dielectric constant gate insulating film located **under the first insulating sidewall** has a*

1009, ¶141 (“FIG. 23 is a sectional view showing a first modification of the method of manufacturing the semiconductor device according to the fourth preferred embodiment. ... The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments.”).) In Figure 23, film 9 replaces films 40 and 9 of Figure 22. (See TSMC-1009, Figs. 22-23.) From this, a POSITA would have understood that films 40 and 9 in Figure 22 can also be considered the claimed second insulating sidewall.

smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.”

104. These limitations focus on the dimensions (e.g., width and thickness) of the gate insulating film in relation to the gate electrode and insulating sidewalls. Matsumoto’s first and fourth embodiments both disclose these limitations.

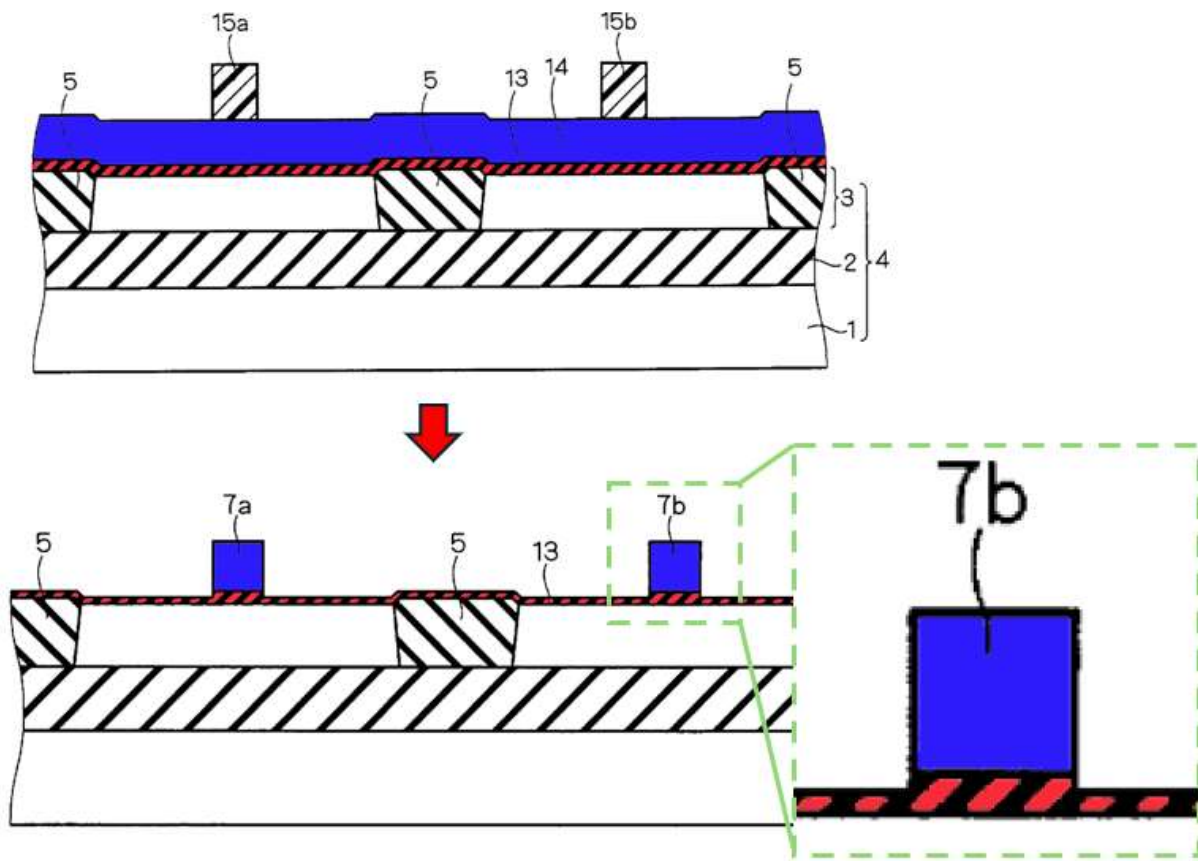
105. **First Embodiment.** In Matsumoto’s first embodiment, the gate insulating film 6 (shaded red) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode 7 to under film 8. Film 8 (shaded purple) is the claimed “*first insulating sidewall.*” This is shown in Figure 1 below.



Matsumoto, Fig. 1 (annotated and enlarged)

106. Figure 1 also shows that gate insulating film 6 is thinner under film 8 (*“first insulating sidewall”*), than it is under the gate electrode 7 (shaded blue).

107. The larger thickness of the gate insulating film under the gate electrode compared to under the first insulating sidewall is a result of Matsumoto’s fabrication process. As shown in the Figure 3 below, dielectric film 13 (shaded red) is formed on the substrate and polysilicon film 14 (shaded blue) is formed on high-k dielectric film 13. (*See* TSMC-1009, ¶107, Figure 3.) The etching process used to form the gate electrodes (7a and 7b) **“slightly etches the upper surface of”** film 13. This “slight etching” of film 13 in the areas not covered by the gate electrode result in the dielectric film having a larger thickness under the gate electrode than in the areas not under the gate electrode. (*See* TSMC-1009, ¶108, Figure 4.)

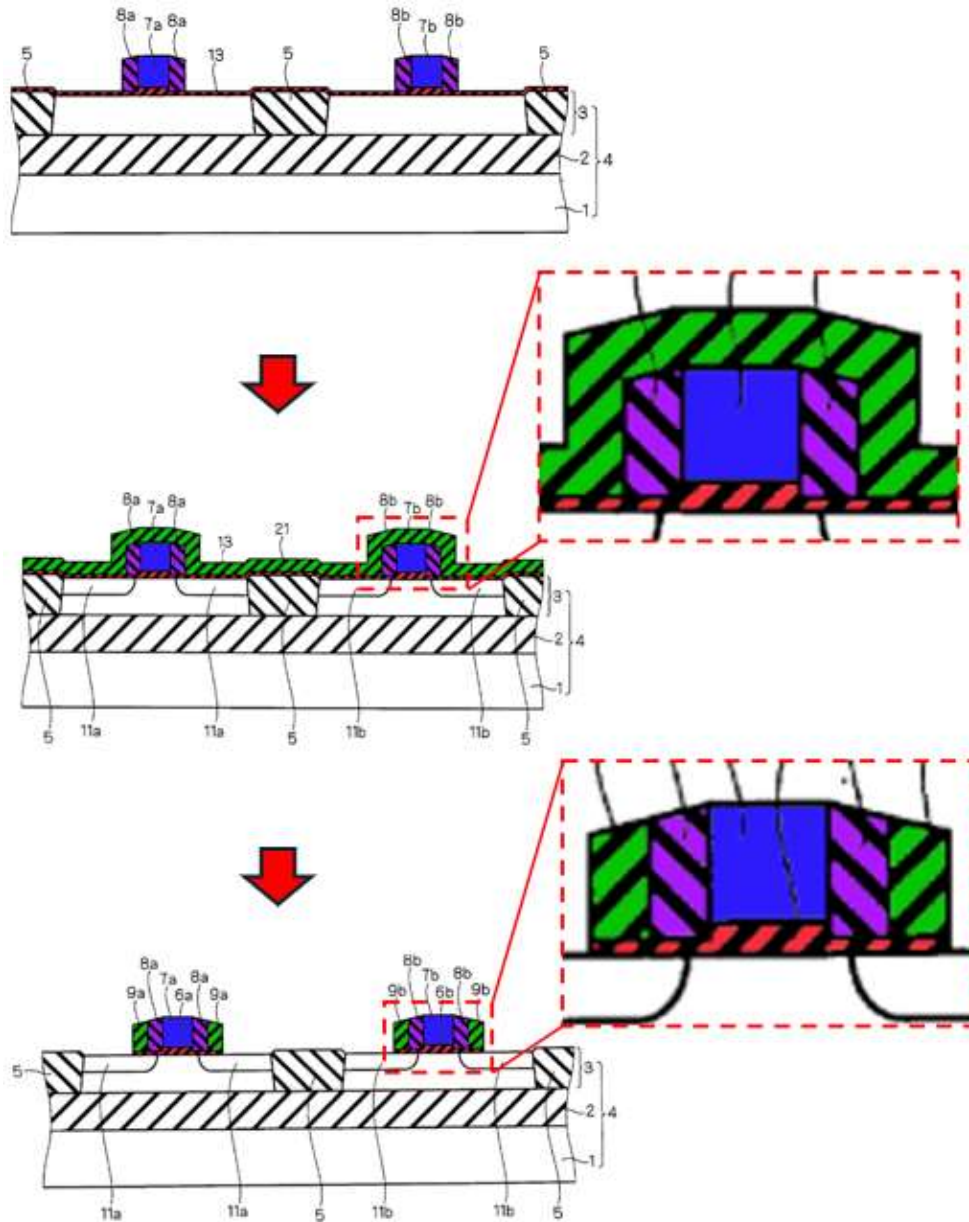


Matsumoto, Figs. 3 (annotated top) and 4 (annotated and enlarged, bottom)

108. Similarly, Matsumoto's manufacturing process confirms that gate insulating film 6 is "*continuously formed so as to extend from under the gate electrode to under the first insulating sidewall.*" As shown in Figures 3-4, above, the dielectric film 13 that forms the gate insulating film is formed continuously as one layer. After formation of the gate electrode and sidewalls 8a/8b (the "*first insulating sidewall,*" shaded purple), silicon nitride film 21 is "*formed on the entire top surface*" of the intermediate structure as shown in Figures 6 and 9 below. (TSMC-1009, ¶¶109-110, 114, Figs. 6, 9.) Film 21 and film 13 are then etched

“until the upper surface of the silicon layer 3 is exposed”, forming sidewalls 9a/9b (the “*second insulating sidewall*,” shaded green). (TSMC-1009, ¶114, Fig. 10.)

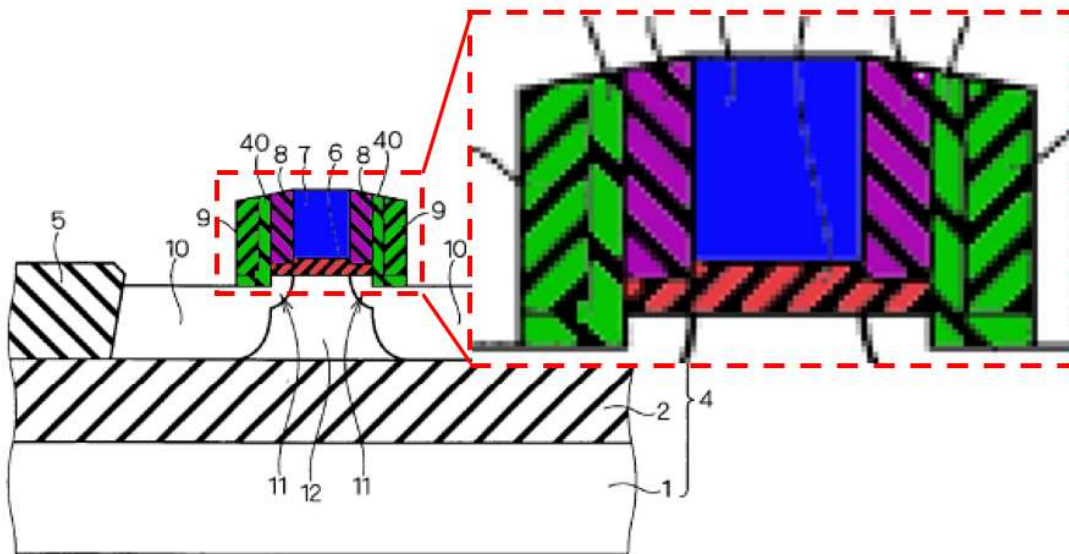
After this etching, the dielectric film (shaded red) remains under only the gate electrode and first and second sidewalls.



Matsumoto, Figs. 6 (top), 9 (middle), 10 (bottom) (annotated with enlargements)

109. Through this process, the gate insulating film 6 is “*continuously formed so as to extend from under the gate electrode to under the first insulating sidewall*,” because gate insulating film 6 is formed by etching film 13, which was continuously formed, in the areas not covered by sidewall insulating films 8 and 9.

110. **Fourth Embodiment.** In Matsumoto’s fourth embodiment, gate insulating film 6 (shaded red) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under only film 8, but not under films 9 and 40. Film 8 (shaded purple) is the claimed “*first insulating sidewall*.” This is shown in Figure 22 below.



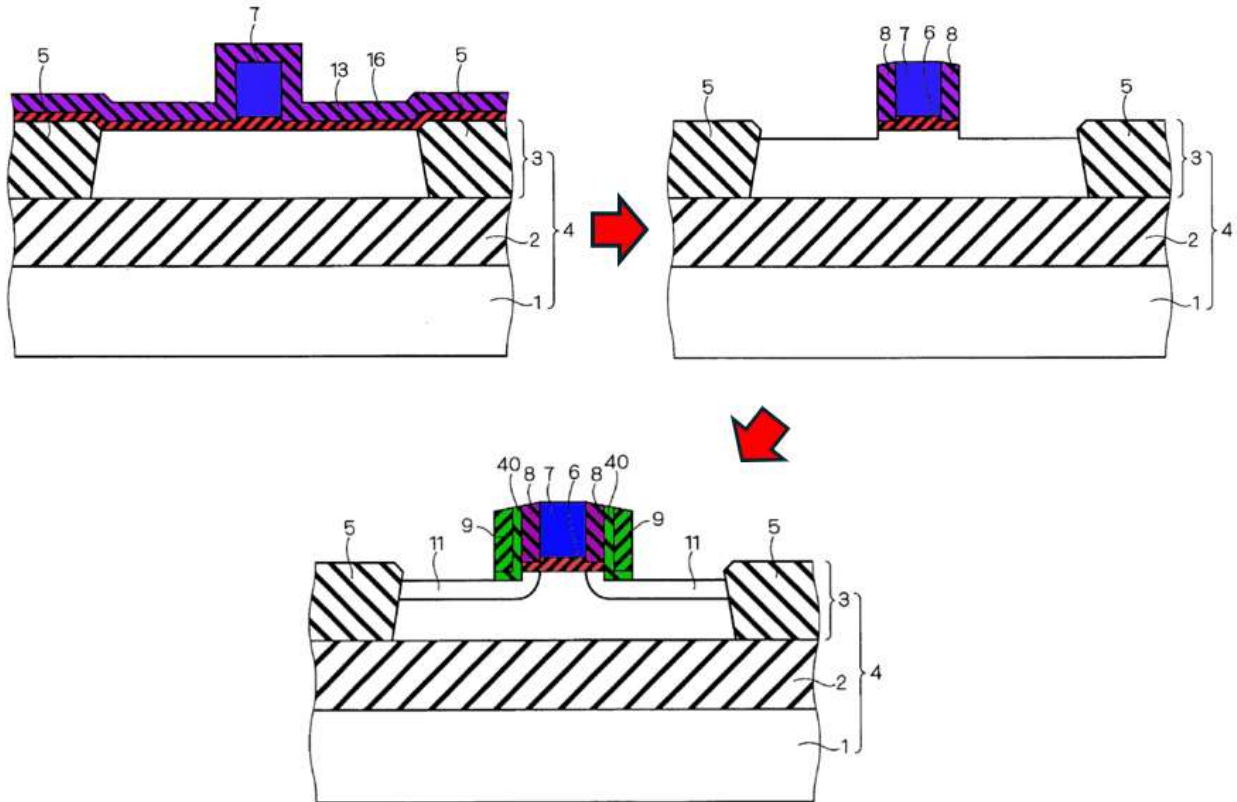
Matsumoto, Fig. 22 (annotated and enlarged)

111. Figure 22 also shows that gate insulating film 6 is thinner under film 8 (“*first insulating sidewall*”; shaded purple) than it is under the gate electrode 7 (shaded blue).

112. Once again, Matsumoto's fabrication process confirms the presence of these features in Matsumoto's fourth embodiment. "[G]ate electrode 7 is formed by the process described in the first preferred embodiment, and thereafter the silicon oxide film 16 is formed on the entire top surface of the resultant structure by a CVD process." (See TSMC-1009, ¶¶137, 108.) As discussed above with regard to the first embodiment, this process "**slightly etches the upper surface of**" film 13. (See TSMC-1009, ¶108.) The "slight etching" of film 13 in the areas not covered by the gate electrode result in the dielectric film having a larger thickness under the gate electrode than in the areas not under the gate electrode. (See also TSMC-1009, Figs. 3-4, annotated above.)

113. Similarly, Matsumoto's manufacturing process confirms that gate insulating film 6 is "*continuously formed so as to extend from under the gate electrode to under the first insulating sidewall.*" As shown in Figures 3-4, annotated above, the dielectric film 13 that forms the gate insulating film is formed continuously as one layer. After formation of the gate electrode, sidewalls 8 are formed. (TSMC-1009, ¶138.) The etching process that forms sidewalls 8 ("*the first insulating sidewall*"; shaded purple) "is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16." (TSMC-1009, ¶138.) This process is shown in Figures 18-19, below. As shown in Figure 19, the high-k dielectric film (shaded red) remains only under the gate and first

sidewall. Film 40 and film 9 (alone or in combination the “*second insulating sidewall*” (shaded green)) are then formed on the outer side surfaces of film 8, as shown in Figure 21, below. (TSMC-1009, ¶139.)



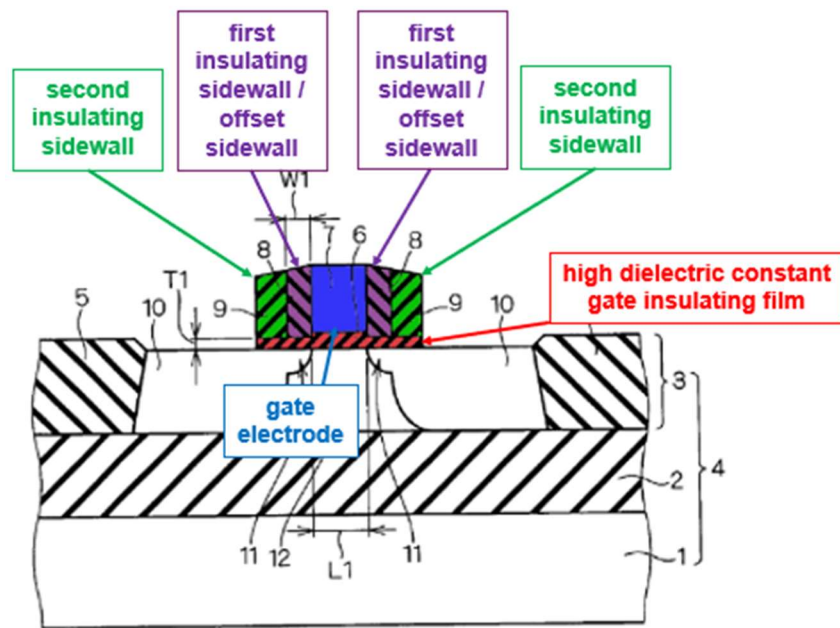
Matsumoto, Figs. 18 (top-left), 19 (top-right), and 21 (bottom) (annotated)

114. Through this process, the gate insulating film 6 is “*continuously formed so as to extend from under the gate electrode to under the first insulating sidewall,*” because gate insulating film 6 is formed by etching film 13, which was continuously formed, in the areas not covered by sidewall insulating films 8.

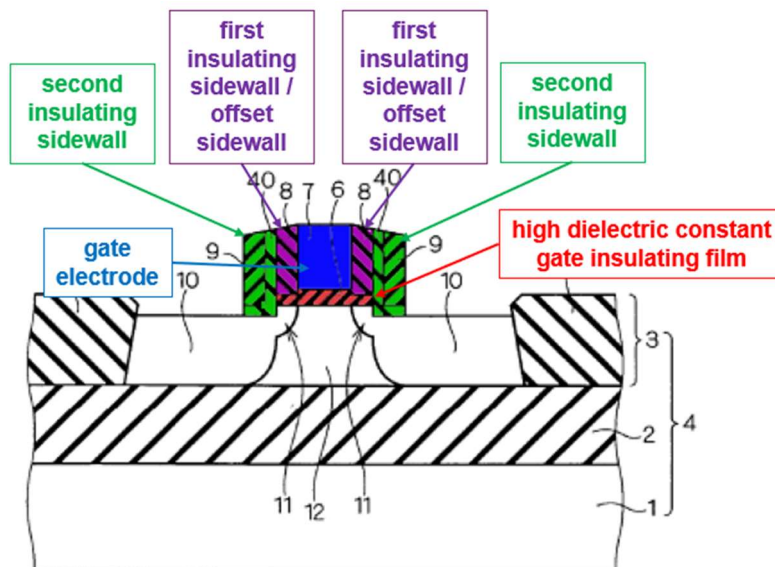
C. Dependent Claim 4

[4] <i>The semiconductor device of claim 1, wherein the first insulating sidewall is an offset sidewall.</i>
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115. Matsumoto's first and fourth embodiments each discloses this limitation. As explained above, in Matsumoto's first and fourth embodiments, film 8 is the "*first insulating sidewall*." Matsumoto expressly refers to film 8, which is located between gate electrode 7 and the "*second insulating sidewall*", as an "**offset** insulation film." (TSMC-1009, ¶155 ("The relationship between the width W1 of the **silicon oxide film 8 serving as an offset insulation film** ..."), ¶157 ("FIG. 28 is a graph of the **width W1 of the offset insulation film** versus the delay time t_{pd} ...), Figure 1 (below, showing width W1)). Matsumoto's film 8 (shaded purple) is also formed on the sidewalls of the gate electrode (shaded blue). Accordingly, in Matsumoto's first and fourth embodiment devices, film 8 "*is an offset sidewall*" [4]. (See also TSMC-1001, 7:37-41 (referring to the inner sidewall as an offset sidewall), Figure 2; TSMC-1034, Figure 5-25.)



Matsumoto, Fig. 1 (annotated)



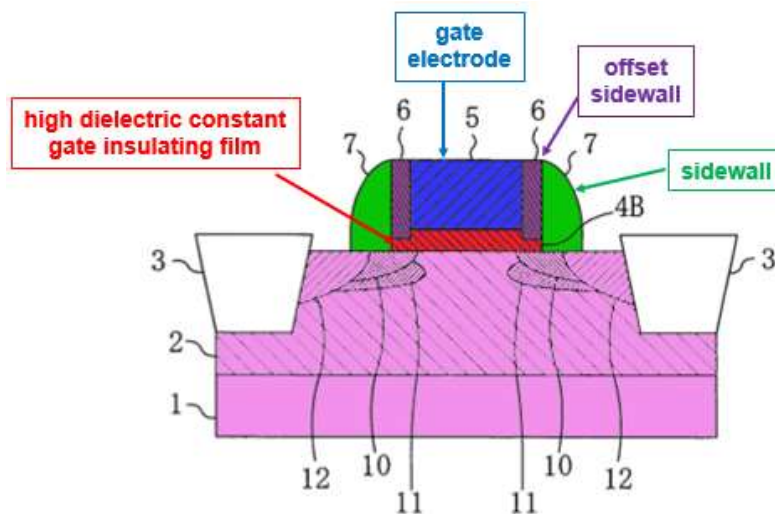
Matsumoto, Fig. 22 (annotated)

D. Dependent Claim 5

[5] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.*

116. Matsumoto's fourth embodiment discloses this limitation.

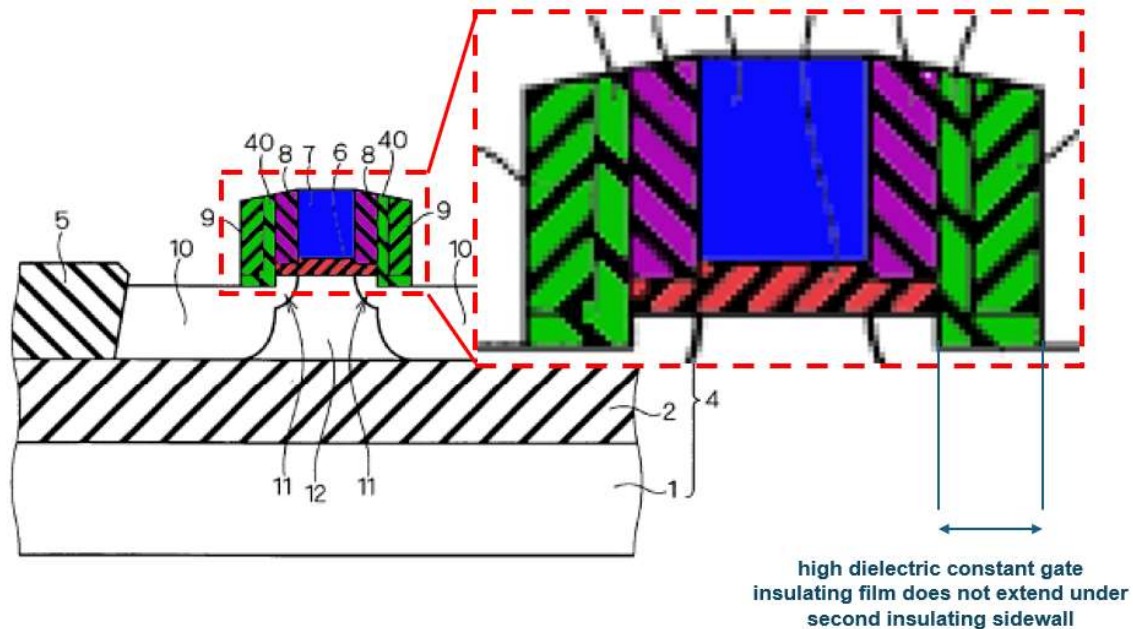
117. As explained above in my overview of the '764 patent, Figure 2 of the '764 patent illustrates an embodiment that satisfies the limitations of dependent claim 2. As can be seen in Figure 2, the high-k gate insulating film (shaded red) extends under first, or inner, sidewall 6 (shaded purple) and has a smaller thickness under inner sidewall 6 than under gate electrode 5 (shaded blue), but does not extend under the second sidewall 7 (shaded green).



'764 Patent, Fig. 2 (annotated)

118. Matsumoto's fourth embodiment discloses a similar structure. As shown in Figure 22 of Matsumoto, below, and discussed above with regard to

limitations [1E]-[1F], the gate insulating film 6 of Matsumoto's fourth embodiment (shaded red) extends only under the film 8 ("*first insulating sidewall*") but not under films 40 and 9 (alone or collectively the "*second insulating sidewall*").



Matsumoto, Fig. 22 (annotated and enlarged)

119. Thus, Matsumoto's fourth embodiment device discloses the additional limitation of claim 5.

E. Dependent Claim 14

[14] *The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film.*

120. Matsumoto's fourth embodiment teaches this limitation.

121. As discussed above with regard limitations [1C]-[1D], **silicon nitride** film 9 and **silicon oxide** film 40 are collectively the "*second insulating sidewall*."

This is shown, for example, in Figure 22 of Matsumoto. A POSITA would have understood these two films to be “layers” of the collective sidewall structure, consistent with the disclosures of ’764 patent.⁵ Silicon nitride film 9 is an example of an nitride film, and silicon oxide film 40 is an example of an oxide film, as claimed. For these reasons, Matsumoto’s fourth embodiment discloses “*the second insulating sidewall has a double layer structure including an oxide film and a nitride film*” [14].

F. Dependent Claim 15

[15] <i>The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.</i>
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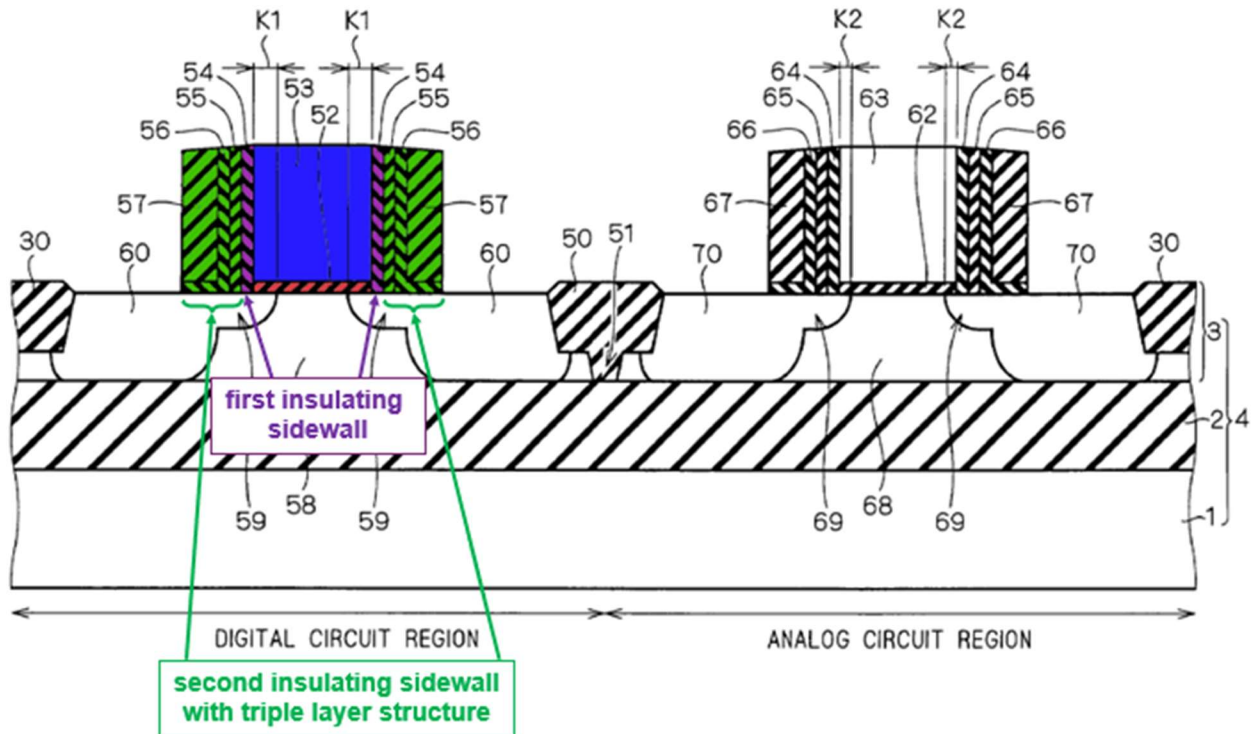
⁵ For example, the ’764 patent states:

In each of the first through eighth embodiments, a single layer structure of a SiN film has been used as an example of the sidewall 7. However, instead of the single layer structure of a SiN film, for example, a double layer structure of a combination of an oxide film (SiO₂ film) and a nitride film (SiN film) (for example, including a SiO₂ layer as an lower layer and a SiN film as an upper layer), a triple layer structure (for example including an SiO₂ film as a lower layer, a SiN film as a middle layer and a SiO₂ film as an upper layer) or the like may be used.

(TSMC-1001, 20:66-21:8.)

122. Matsumoto renders obvious this limitation. As discussed above with regard to claim 14, in its fourth embodiment (Figure 22), Matsumoto already discloses a second insulating sidewall with a double layer structure including an oxide film and a nitride film.

123. In addition, Matsumoto also discloses a digital FET, isolated from analog device regions, that includes additional layers. For example, the device shown in Matsumoto's Figure 29 below includes silicon oxide film 54 (*"first insulating sidewall"*; shaded purple) "formed in contact with each side surface of the gate electrode 53." (TSMC-1009, ¶¶160, 162, Figure 29 (below).) Film 54 functions as an "offset insulation film." (TSMC-1009, ¶162.) Beyond this layer, "[a] silicon oxide film 55 is formed outside the silicon oxide film 54", followed by a structure containing "a silicon oxide film 56 and a silicon nitride film 57" (TSMC-1009, ¶162.) A POSITA would have considered this structure comprising films 55, 56, and 57 to be a second insulating sidewall with a triple layer structure. More specifically, silicon oxide film 55 (*"a first oxide film"*), silicon oxide film 56 (*"a second oxide film"*), and silicon nitride film 57 (*"a nitride film"*) form a "second insulating sidewall" with "a triple layer structure including a first oxide film, a nitride film and a second oxide film."



Matsumoto, Fig. 29 (annotated)

124. Although the gate insulating film in Figure 29, above, does not extend under the insulating sidewalls, such a modification would have been obvious to a POSITA in light of the disclosures regarding at least Matsumoto's fourth embodiment. For example, it would have been obvious to a POSITA to modify Matsumoto's fourth embodiment device by adding an additional oxide layer to the existing second insulating sidewall, which includes silicon nitride film 9 and silicon oxide film 40, as disclosed in Matsumoto's sixth embodiment shown in Figure 29. Indeed, Matsumoto explicitly teaches that "[t]he structure according to the sixth preferred embodiment is applicable to the semiconductor device of any one of the first to fifth preferred embodiments." (TSMC-1009, ¶159.)

G. Dependent Claims 16-17

[16] *The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.*

[17] *The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.*

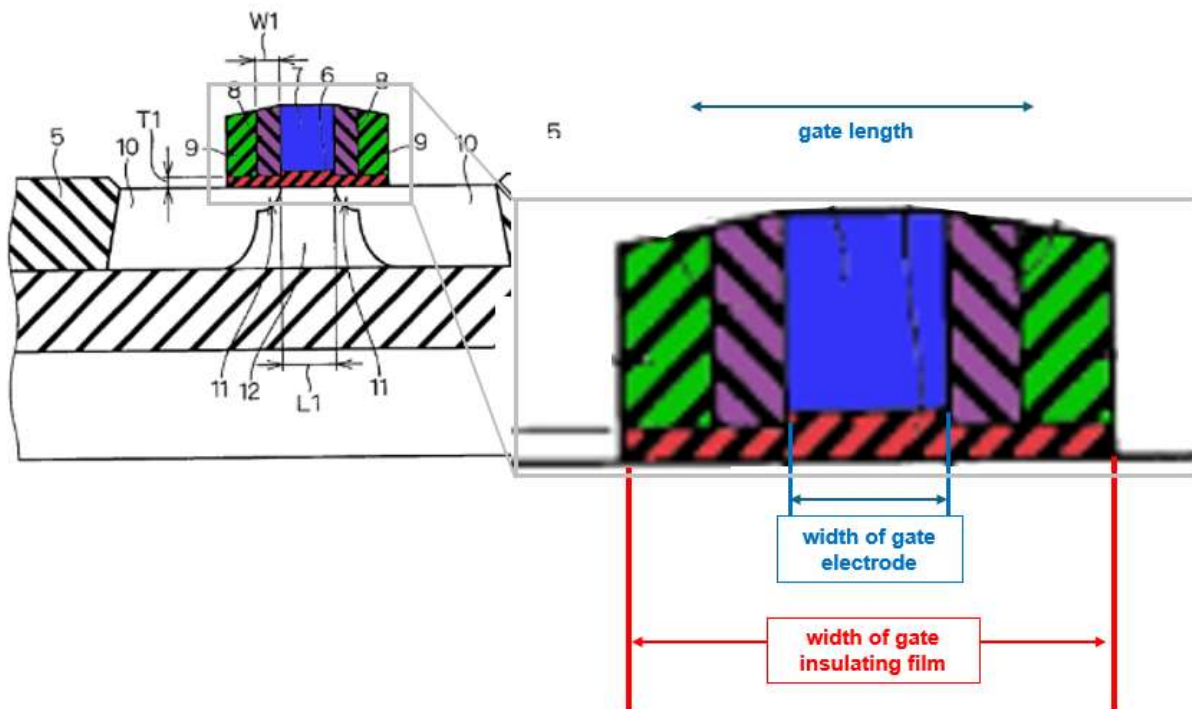
125. These claims address the width of the gate insulating film relative to the gate electrode. Matsumoto's first and fourth embodiments each teaches the limitations of claims 16 and 17.

126. Matsumoto's first and fourth embodiments teach "*a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length*" [16]⁶ and "*a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*" [17] because, as I explained above with regard to limitation [1E], the high-k gate insulating film 6 in Matsumoto's first and fourth embodiments extends from under the gate to

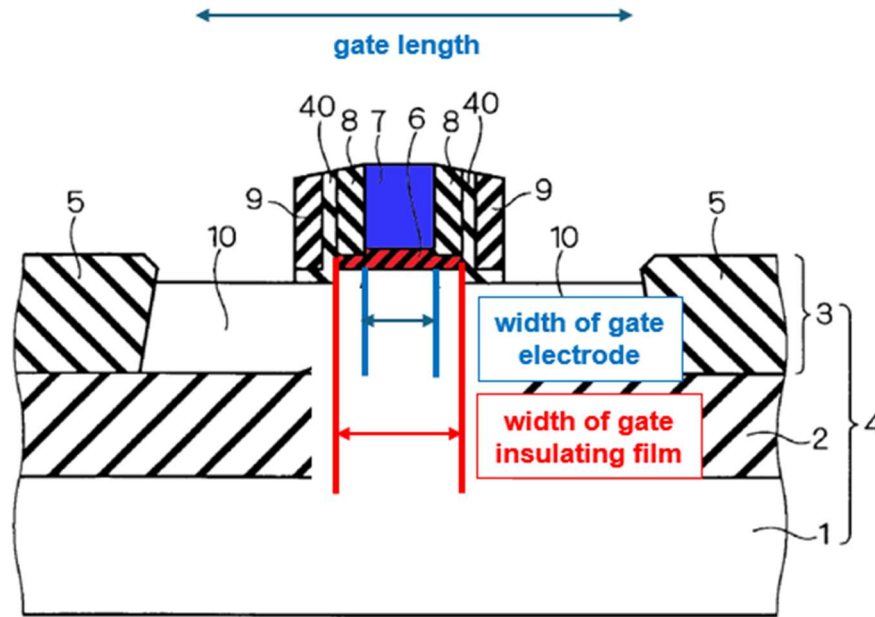
⁶ The '764 patent uses the term "along the gate length" to refer to a direction, specifically from the source region to the drain region.

under the first insulating sidewall 8, which is formed on the sidewalls of the gate electrode 7. This is shown in Figures 1 and 22, below.

127. As can be seen in Figures 1 and 22, the width of Matsumoto's gate electrode 7 is constant across its entire height. In both figures, the width of the high-k gate insulating film 6 (shaded red), including at film 6's bottom surface, is larger than the width of the gate electrode 7 (shaded blue), including at gate electrode 7's bottom surface. The fabrication processes of both embodiments, discussed above with regard to limitations [1E]-[1F], confirm the structures shown in Figures 1 and 22.



Matsumoto, Fig. 1 (annotated and enlarged)



Matsumoto, Fig. 22 (annotated)

H. Dependent Claims 18-19

[18] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.*

[19] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.*

128. These claims relate to the dielectric constant of the gate insulating film. Matsumoto's first and fourth embodiments disclose this limitation because the dielectric constants of materials disclosed by Matsumoto for the gate insulating film and the second insulating sidewall are inherent to those materials. Even if that were not found to be the case, then at a minimum, using knowledge of a POSITA, as reflected in AAPA, Matsumoto renders the limitations of claims 18-19 obvious.

129. The “*relative dielectric constant*” is an inherent property of a material. Indeed, the ’764 patent admits that a “high dielectric constant film formed of a Hf based oxide, Al based oxide or the like [] **has a relative dielectric constant of 10 or more**, instead of an SiO₂ based insulating film having a **relative dielectric constant of about 4.**” (TSMC-1001, 1:28-31.) Matsumoto teaches that “Ta₂O₅” is one example of a material that can be used to form the gate insulating film. (TSMC-1009, ¶107.) The dielectric constant for Ta₂O₅ is known to be 26, which is greater than 10. (TSMC-1018, Table I.) This alone meets the limitation of claim 18.

130. As discussed above with regard limitations [1C]-[1D], in Matsumoto’s first and fourth embodiments, sidewall film 9 is comprised of silicon nitride (Si₃N₄). Although the dielectric constant of silicon nitride is not explicitly mentioned in the ’764 patent, the dielectric constant of Si₃N₄ is and was well-known to a POSITA to be approximately 7. (See TSMC-1018, Table 1; TSMC-1052, Figure 4 (Si₃N₄ has dielectric constant of 7.2).) Because Matsumoto’s sidewall film 9 is comprised of silicon nitride (Si₃N₄), which has a dielectric constant of 7, and Ta₂O₅ has a dielectric constant greater than 10 (see TSMC-1009, ¶¶114, 139; TSMC-1018, Table I), Matsumoto’s first and fourth embodiments disclose “*the high dielectric constant gate insulating film has a larger relative*

dielectric constant than that of the second insulating sidewall” as recited by claim 19.

I. Dependent Claim 20

<p>[20] <i>The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed to have a convex cross-sectional shape.</i></p>

131. Matsumoto’s first and fourth embodiments each disclose this limitation, consistent with the disclosures of the ’764 patent.

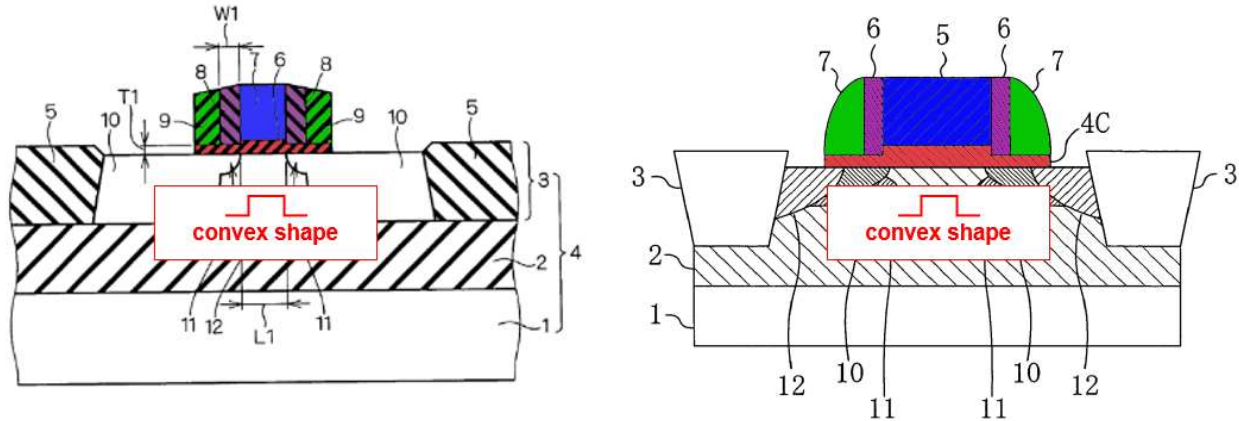
132. The ’764 patent discusses forming gate insulating film to have a convex cross-sectional shape:

It is a second feature of this [second] embodiment that the thickness of the part of the high dielectric constant gate insulating film 4B located under the offset sidewall 6 is smaller than a thickness of the part of the high dielectric constant film 4B located under the gate electrode 5. **That is, the gate insulating film 4B is formed so as to have a convex shape.**

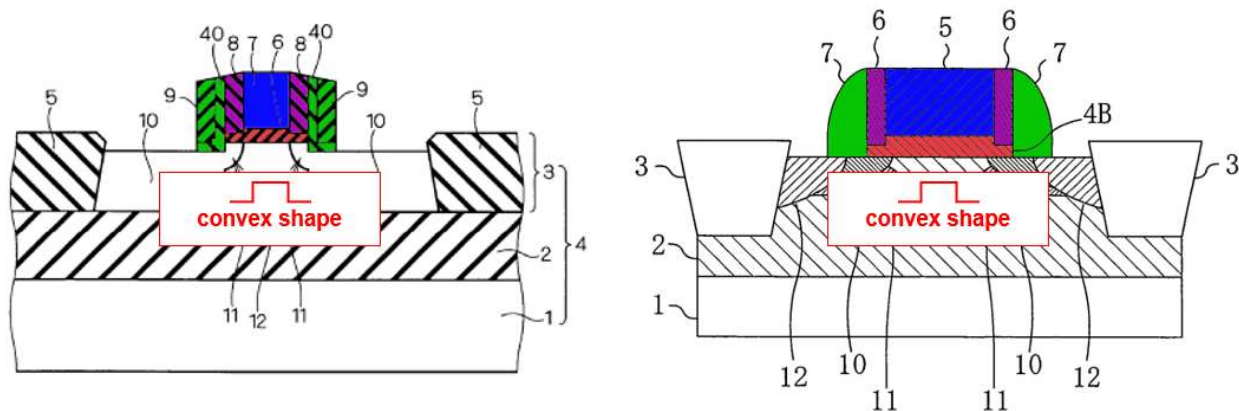
(TSMC-1001, 7:54-59; *see also* TSMC-1001, 8:62-67.)

133. Matsumoto discloses a gate insulating film having similar shape. Specifically, the part of gate insulating film 6 under first and second insulating sidewalls 8, 9 in Matsumoto’s first embodiment (Figure 1) and under first insulating sidewall 8 in Matsumoto’s fourth embodiment (Figure 22) has a smaller thickness than the part of gate insulating film 6 under gate electrode 5. This forms

a gate insulating film 6 having a convex shape, consistent with the disclosures of the '764 patent. This is shown in the figures below.



Matsumoto, Fig. 1 (left); '764 Patent, Fig. 3 (right) (annotated)



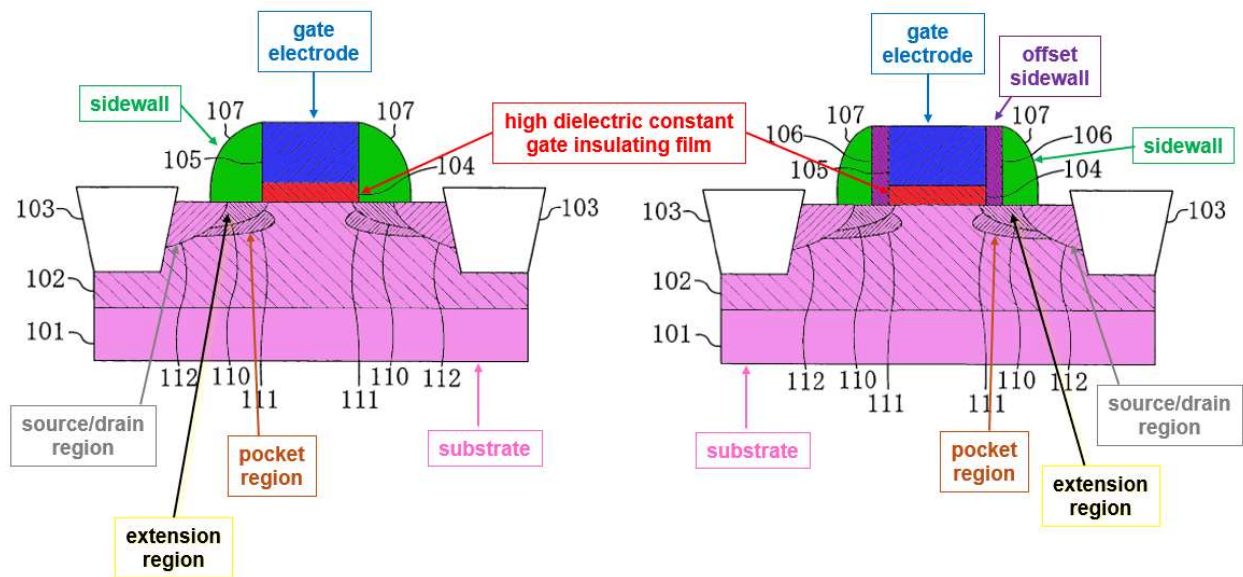
Matsumoto, Fig. 22 (left); '764 Patent, Fig. 2 (right) (annotated)

J. Dependent Claim 21

[21] *The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film is not in contact with the first insulating sidewall.*

134. Matsumoto's first and fourth embodiments each teaches this limitation, consistent with the disclosures of the '764 patent.

135. The '764 patent explains that “in a structure of a known MISFET using a high dielectric constant gate insulating film, side end portions of the high dielectric constant gate insulating film are in direct contact with sidewalls.” (TSMC-1001, 1:61-64.) Examples of such devices are shown in Figures 16A and 16B, below. As can be seen in these figures, the side end of the gate insulating film (shaded red) contact side surfaces of the insulating sidewalls.



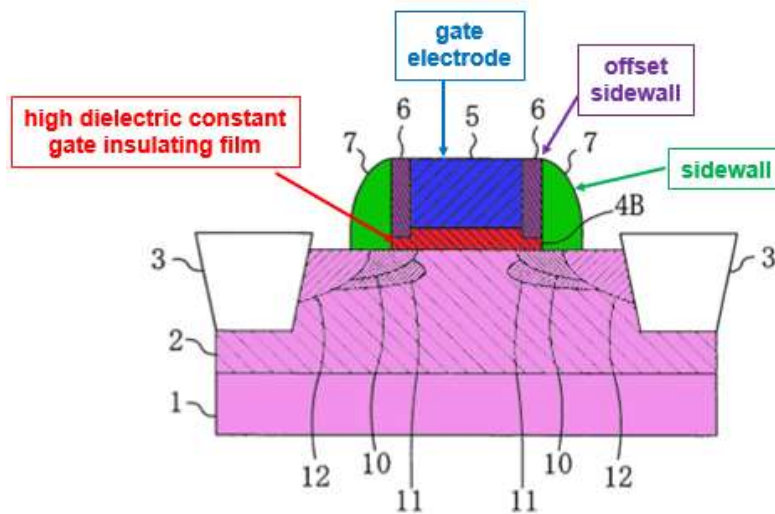
'764 Patent, Fig. 16A (annotated left), Fig. 16B (annotated right)

136. The '764 patent then discloses that in contrast to the prior art devices, its structure is such that “a high dielectric constant gate insulating film is **kept remaining under sidewalls to prevent end portions of the high dielectric constant gate insulating film from being in contact with the sidewalls.**” (TSMC-1001, 2:12-16; *see also* TSMC-1001, 4:39-48 (“According to the present invention, a high dielectric constant gate insulating film is continuously formed so

as to extend from under a gate electrode to under a sidewall. In other words, continuity of the high dielectric constant gate insulating film at a gate end portion is maintained. Thus, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film at the gate end portion, caused by a side end portion of the high dielectric constant gate insulating film being in direct contact with a sidewall film, can be suppressed.”.)

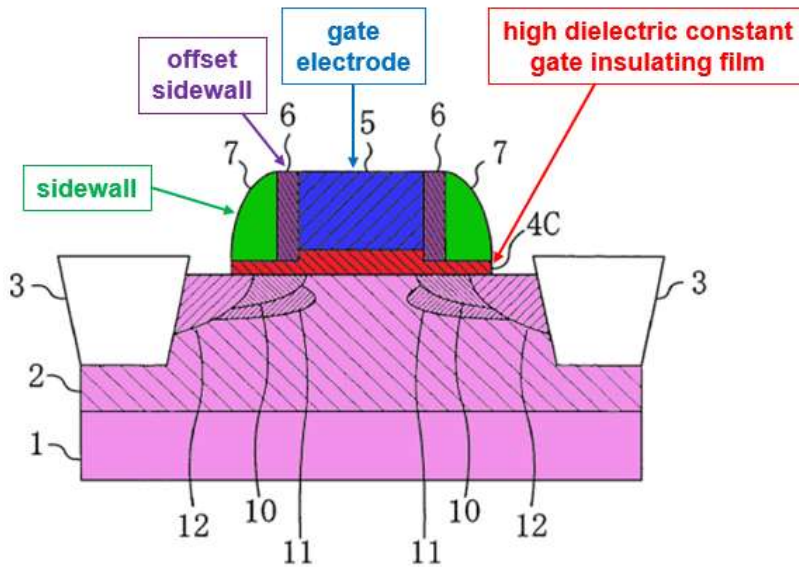
137. Figure 2 of the '764 patent, which corresponds to the second embodiment of the '764 patent, illustrates an exemplary device in which “each side end portion of the high dielectric constant gate insulating film 4B is not in contact with the offset sidewall 6 and continuity of the high dielectric constant gate insulating film 4B at an end portion of the gate electrode 5 is maintained.” (TSMC-1001, 7:60-64.) As shown below, the end of the gate insulating film does not contact the side of the first, or offset, sidewall.⁷ Rather, the gate insulating film extends under the first insulating sidewall.

⁷ A POSITA would have understood from this discussion that the side of the gate insulating film disposed under the gate electrode is not the “side **end** portion” of the gate insulating film, as recited by claim 21. Rather, that term refers to the outer side ends of the gate insulating film.



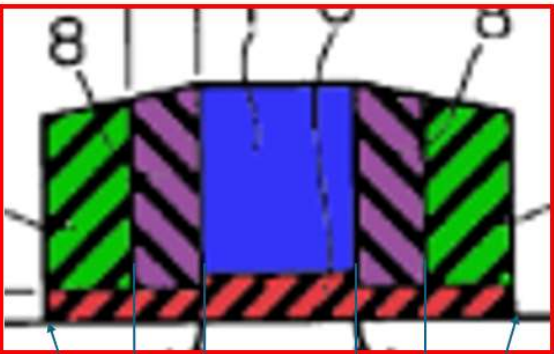
'764 Patent, Fig. 2 (annotated)

138. Figure 3, which shows a modification of the second embodiment of the '764 patent, illustrates another exemplary device in which “each side end portion of the high dielectric constant gate insulating film 4C is not in contact with the sidewall 7 and continuity of the high dielectric constant gate insulating film 4C at an end portion of the gate electrode 5 is maintained.” (TSMC-1001, 9:5-9; *see also* TSMC-1001, 9:60-64, 10:67-11:3 (similar disclosures as to the embodiments of Figures 4 and 5).)

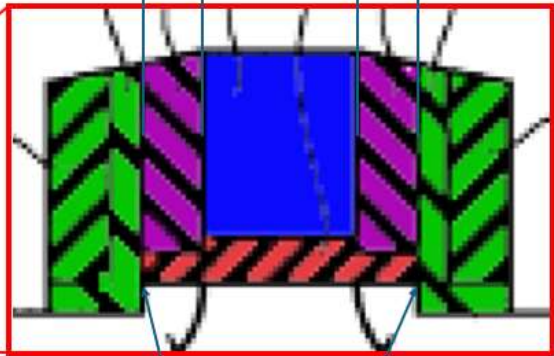


'764 Patent, Fig. 3 (annotated)

139. As discussed above with regard to limitation [1E], in both the first and fourth embodiments of Matsumoto, gate insulating film 6 also extends from under gate electrode 7 to under film 8 (the “*first insulating sidewall*”). In the first embodiment, gate insulating film 6 further extends under films 40 and 9. Because film 6 is completely under film 8 in both embodiments, its side end cannot contact sidewall film 8, as that phrase is used in the ’764 patent.



Matsumoto, Fig. 1 (annotated and enlarged)



Matsumoto, Fig. 22 (annotated and enlarged)

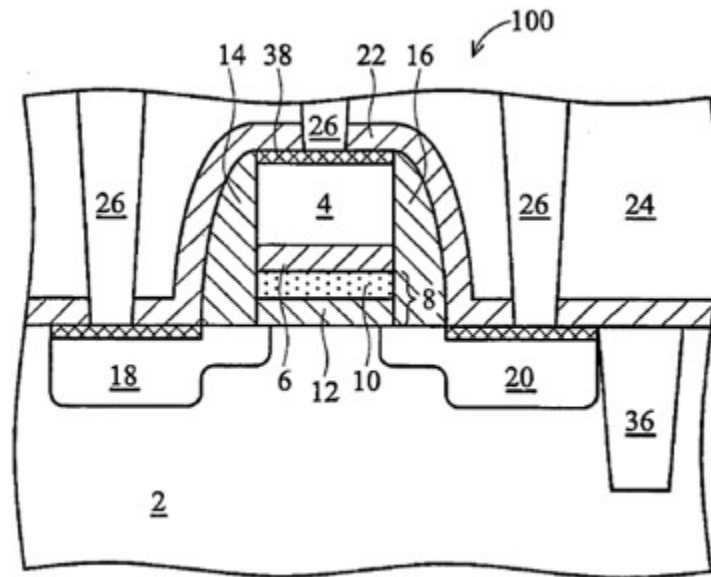
VI. GROUND 2: Matsumoto in View of Wang Renders Claims 2-3, 6-7, and 11 Obvious.

140. As discussed above with regard to Ground 1, Matsumoto discloses, or at least renders obvious, every limitation of claim 1. To the extent Matsumoto is found not to disclose the additional limitations of claims 2-3, 6-7, and 11, Wang, discussed below, does. A POSITA would have been motivated to combine these references, thereby rendering claims 2-3, 6-7, and 11 obvious.

A. Overview of Wang

141. U.S. Publication 2006/0131672, titled “Nitrogen Treatment to Improve High-k Gate Dielectrics,” to Wang, et al. (“Wang”; TSMC-1012), was filed April 27, 2005. Wang “relates generally to semiconductor devices and methods of manufacturing same.” (TSMC-1012, ¶2.) More particularly, Wang relates to an improved transistor (e.g., MOSFET) having a nitrogen containing, high-k gate dielectric, and an underlying dielectric layer having a nitrogen containing portion in contact with the high-k dielectric and a non-nitrogen containing portion (e.g., oxide) that is in contact with the substrate. (TSMC-1012, Abstract, ¶2.) Wang is therefore in the same field as Matsumoto and the ’764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).)

142. An example of Wang's transistor is shown in Figure 3, below. As shown in Figure 3 of Wang, transistor 100 includes a gate stack with high-k dielectric layer 6 and underlying dielectric layer 8 comprising a nitrided portion 10 and a non-nitrided/substantially nitride-free portion 12. (TSMC-1012, ¶¶22, 24, 48.)



Wang, Fig. 3

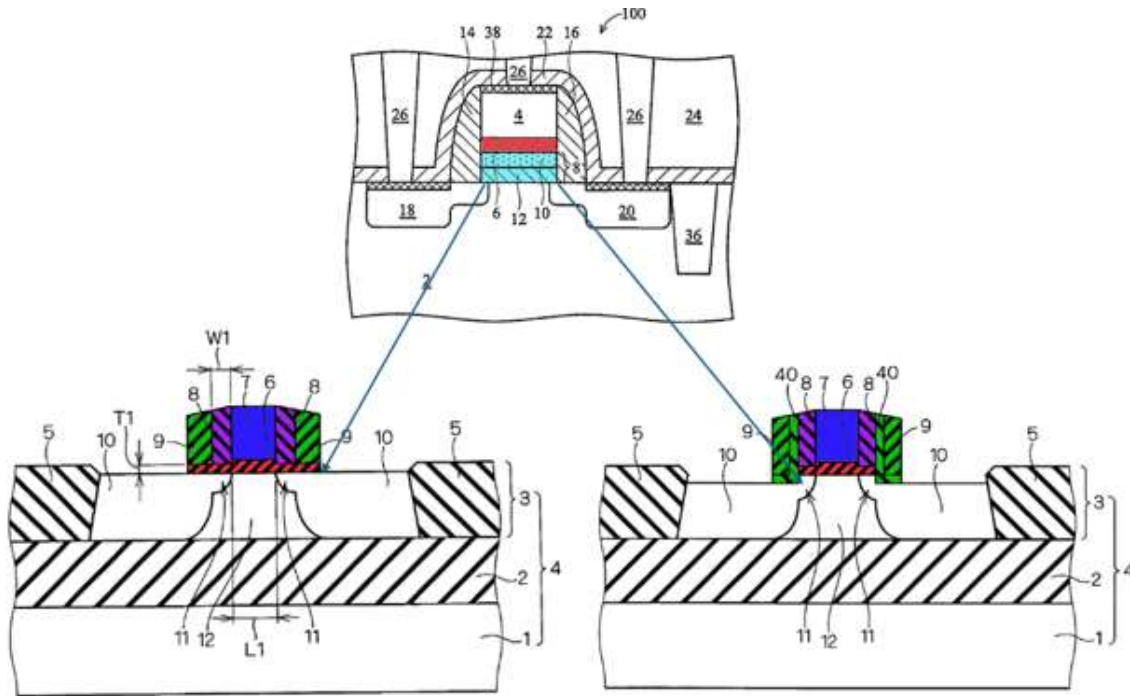
143. Wang presents a list of options for forming its high-k gate dielectric including Hf-based dielectrics (e.g., HfO₂, HfSiO, HfON, or HfSiON). (TSMC-1012, ¶9.)

B. Dependent Claims 2-3

[2] *The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.*

[3] *The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.*

144. A POSITA would have known to combine Wang and Matsumoto by applying Wang's teachings regarding use of an underlying dielectric layer as a buffer layer between a high-k dielectric and silicon substrate to Matsumoto's first and fourth embodiment semiconductor devices. Such a device, for example, would have taken the underlying dielectric layer 8 (shaded aqua) located between the substrate 2 and high-k gate dielectric 6 (shaded red) in Wang, and placed that underlying dielectric between the substrate and high-k dielectric (shaded red) of Matsumoto's first embodiment (Figure 1) and fourth embodiment (Figure 22) devices. In the combination, the resulting device is, for example, Matsumoto's transistor, with Wang's underlying dielectric 8 situated between the Matsumoto's substrate and high-k gate insulating film 6.



**Wang, Fig. 3 (top);
Matsumoto, Figs. 1 (bottom-left) and 22 (bottom-right) (annotated)**

145. Wang discloses that underlying dielectric 8 is “preferably formed of silicon oxide” and “has a first, nitrided portion 10 that is in contact with high-k dielectric layer 6 and a second non-nitrided, or substantially nitrogen-free, portion 12 that is in contact with the underlying substrate 2.” (TSMC-1012, ¶48.) A POSITA would have understood that underlying dielectric 8 is used as a “*buffer insulating film*,” as required by claim 2. Indeed, the background of the invention provides the context for Wang’s teachings as providing an improved and optimal buffer between “undesirable interactions between high-k dielectrics and the underlying semiconductor material.” (TSMC-1012, ¶3; *see also* TSMC-1012, ¶¶4-6).

146. A POSITA would have understood that underlying dielectric 8 includes a “*silicon oxide film*” (e.g., in non-nitrided portion 12, and in nitrided oxide portion 10), as required by claim 3. (*See also* TSMC-1038, 88-89 (describing use of “nitrided oxides” including SiO_xN_y).)

147. For these reasons, it is my opinion that the combination of Wang with Matsumoto’s first and fourth embodiments Wang renders claims 2-3 obvious.

148. **Motivation to Combine.** A POSITA would have been motivated to combine Matsumoto and Wang as discussed above. Wang explicitly states the motivation, explaining that it was well known in the art (even before Wang) that the use of silicon oxide as a buffer layer between the high-k gate dielectric and the substrate was “typical.” According to Wang, “[d]ue to the undesirable interactions between high-k dielectrics and the underlying semiconductor material (usually silicon, germanium, silicon germanium, and the like) to degrade carrier mobility, a thin silicon oxide layer is typically employed as part of the gate dielectric even when a high-k gate dielectric is employed.” (TSMC-1012, ¶3.) This aligns with the description of the buffer insulating film in the ’764 patent, which states that by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed.” (TSMC-1001, 12:9-18)

149. A POSITA would have been further motivated to combine Matsumoto and Wang, because Wang’s teachings can be used along with Matsumoto’s to

further Matsumoto's goals. More specifically, one objective of Matsumoto is "to provide a semiconductor device which achieves reductions in malfunctions and operating characteristic variations." (TSMC-1009, ¶13.) Wang explains that "underlying dielectric layer 8 advantageously provides higher mobility and higher reliability for the high-k peripheral (or I/O) device." (TSMC-1012, ¶28.) Based on these disclosures of Wang and Matsumoto, a POSITA would have been motivated to use Wang's buffer insulating layer to improve carrier mobility, and thereby performance and reliability, of semiconductor devices such as the MOSFETs disclosed by both Wang and Matsumoto.

150. In my opinion, combining Wang's buffer layer with Matsumoto's high-k film in the manner described above would have been a straightforward use of a known technique (forming Wang's buffer insulating layer) to improve similar devices (Matsumoto's transistor using a high-k gate insulating film) in the same way (improving carrier mobility in high-k transistor designs).

151. Wang discloses the use of well-known and established methods for forming the underlying dielectric: "Preferably, the underlying dielectric layer 8 is a thermally grown oxide formed by subjecting substrate 2 to an oxygen ambient." (TSMC-1012, ¶22.) Wang also teaches that deposition of the high-k dielectric layers "may be performed by conventional methods including remote plasma CVD (RPCVD), plasma enhanced CVD (PECVD), atomic layer deposition (ALD),

MOCVD, MBE, PVD, sputtering or other methods known in the art.” (TSMC-1012, ¶24.) Matsumoto similarly discloses the use of well-known and existing techniques for forming the gate dielectric, including using CVD for dielectric film deposition (TSMC-1009, ¶107.)

152. To go further, Matsumoto discloses forming a layer of silicon oxide above the substrate, with other high-k dielectrics as alternative gate insulating films. (TSMC-1009, ¶107.) A POSITA wanting to include a buffer layer between the substrate and the high-k gate dielectric (which Wang states was “typical” in the art) would have simply applied Matsumoto’s (or Wang’s) disclosure of forming a silicon oxide layer along with (and before) Matsumoto’s (or Wang’s) disclosure regarding using other high-k materials for the gate dielectric. Wang’s teachings for nitriding part of the underlying gate dielectric would then be applied, followed by Matsumoto’s remaining steps of forming the insulating sidewalls.

153. In my opinion, in light of the disclosures above, a POSITA would have had a reasonable expectation of success in combining Matsumoto and Wang in the manner discussed above, and the results of the combination would have been predictable.

C. Dependent Claims 6-7

[6] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.*

[7] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a HfSiON film.*

154. Claim 6 depends from claim 1, and recites “*The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide*” [6]. Claim 7 depends from claim 1, and recites “*The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a HfSiON film*” [7].

155. Although Matsumoto discloses exemplary high-k dielectrics for use in its device, it does not explicitly disclose its high-k film “*is formed of a Hf based oxide*” [6] or “*formed of a HfSiON film*” [7]. Wang does. A POSITA would have combined these references by utilizing a Hf based oxide, such as HfO₂, or a nitrided Hf based oxide, such as HfSiON, as the gate dielectric in Matsumoto’s device (or the combined Matsumoto-Wang device). In my opinion, such a combination of Matsumoto with Wang renders Claims 6-7 obvious.

156. More specifically, Matsumoto teaches that high-k materials such as “a metal oxide film such as Al₂O₃ or a ferroelectric film such as Ta₂O₅ and BST” can be used as a gate insulating film. (TSMC-1009, ¶107.) Wang teaches the use of similar high-k dielectrics, including “**HfSiON**, amorphous **HfSiON**, Ta₂O₅, TiO₂,

Al₂O₃, ZrO₂, **HfO₂**, Y₂O₃, La₂O₃, aluminates, silicates, **HfAlO_x**, TiO₂, PbTiO₃, BaTiO₃, SrTiO₃, and PbZrO₃, and combinations thereof.” (TSMC-1012, ¶12; *see also* TSMC-1012, ¶¶ 9, 25.)⁸

157. Matsumoto and Wang both explicitly list Al₂O₃ and Ta₂O₅ as exemplary high-k gate dielectrics, and Wang’s disclosure of **HfO₂**, for example, is consistent with Matsumoto’s disclosure of “a metal oxide film such as...”

158. **Motivation to Combine.** A POSITA would have been motivated to use a Hf-based oxide as a high-k gate insulating film, as taught by Wang, in the semiconductor devices of Matsumoto’s first and fourth embodiments. By 2005,

⁸ In addition to HfO₂, materials such as HfON (hafnium oxynitride), HfSiO (hafnium silicate), and HfSiON (hafnium-silicon oxynitride) are also considered hafnium-based oxides because they contain hafnium oxide as a key component. HfSiO is a combination of hafnium oxide and silicon dioxide, forming a silicate, which enhances thermal stability and process compatibility. HfSiON is an evolution of HfSiO with the addition of nitrogen, further improving its resistance to oxygen diffusion and enhancing its thermal stability. Even though these materials contain other elements like silicon and nitrogen, they are still considered hafnium-based oxides because the core dielectric properties stem from the presence of hafnium oxide.

i.e., the earliest priority date of the '764 patent, a POSITA would have been motivated to select HfO_2 as a high-k gate insulating film, as hafnium-based dielectrics (e.g., HfO_2) had already become a popular high-k dielectric in advanced semiconductor manufacturing due to the many known benefits. For example, HfO_2 was known to have superior thermal stability and band gap alignment. (*See, e.g.*, TSMC-1037, 2.4.1 (“Recently, HfO_2 films have emerged as the most promising gate dielectric material for sub 100nm technology due to its superior thermal stability with poly-Si and reasonable band alignment”); TSMC-1032, 207 (HfO_2 “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 134 (“Excellent dielectric properties such as high dielectric constant, low leakage current, good thermal stability, negligible dispersion and excellent reliability were demonstrated. These results suggest that HfO_2 is a promising material for the future gate dielectric application.”).) HfO_2 also could be scaled down to a smaller EOT. (TSMC-1032, 207.)

159. A POSITA would have also been motivated to use HfSiON to further enhance operation because nitrogen incorporation was found to improve thermal stability and electrical characteristics of HfSiON , including by enhancing the dielectric constant of the film. (*See* TSMC-1029, 849.)

160. In light of the foregoing, of the high-k materials disclosed by Wang and Matsumoto, a POSITA would have been motivated to choose (1) a hafnium-based oxide as the high-k gate insulating film, thereby rendering claim 6 obvious, and/or (2) HfSiON as the high-k gate insulating film, thereby rendering claim 7 obvious.

D. Dependent Claim 11

<p>[11] <i>The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.</i></p>

161. The combination of Matsumoto's first and fourth embodiments with Wang discloses claim 11.

162. Wang discloses that the high-k dielectric layer 6 "is preferably less than about 50 Å to maintain low gate leakage and thin equivalent oxide thickness (EOT)." (TSMC-1012, ¶26). For an exemplary HfSiON gate insulating layer, the film "was deposited to a thickness of about 5 to 50 Angstroms and having an equivalent oxide thickness (EOT) of less than about 2.0 nanometers." (TSMC-1012, ¶34.) Wang also specifically claims a device "wherein the high-k dielectric has a thickness from about 5 to 50 Å." (TSMC-1012, claim 3.) A POSITA would have been motivated to use thinner gate insulating films, as taught by Wang, consistent with the goals of miniaturizing semiconductor devices.

163. In the combined device of Matsumoto and Wang, the thickness of the high-k gate insulating film at its side ends would also range from about less than 5 Angstroms to less than 50 Angstroms since the thickness of the layer is smaller under sidewall 8 than under the gate electrode 7. The range of 5 to 50 Å is equivalent to 0.5 to 5 nm, and thus Wang's preferred range includes thicknesses less than 2 nm, as recited by claim 11. Put another way, the thickness of 2 nm (20 Angstroms) falls within the range of thicknesses disclosed by Wang.

164. I am informed and understand that, where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness, and it becomes the patentee's burden to present evidence of teaching away, unexpected results or criticality, or other pertinent objective indicia indicating that the overlapping range would not have been obvious in light of that prior art." Based on my review of the intrinsic record, there is no discussion, evidence, or justification for the selection of 2 nm as the thickness of the gate insulating film. Thus, the combination of Matsumoto and Wang renders obvious that "*each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*" [11].

VII. GROUND 3: Matsumoto in View of Wang and Sim Renders Claim 11 Obvious.

[11] *The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.*

165. Should an argument be made that the combination of Matsumoto and Wang does not render claim 11 obvious, the combination of Matsumoto, Wang, and Sim renders the claim obvious. Sim, titled “Effects of ALD HfO₂ Thickness on Charge Trapping and Mobility,” was published on June 17, 2005. Sim’s study related to the use of high-k dielectrics used in semiconductor devices. (TSMC-1024, Abstract (“Scaling the physical thickness of the HfO₂ dielectric causes less charge trapping and higher mobility.”).) Sim is therefore in the same field as Matsumoto, Wang, and the ’764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”); TSMC-1012, ¶2.)

166. Sim explicitly describes use of a gate insulating film having a thickness 2nm or less. Specifically, Sim explains that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low

mobility and charge trapping have been identified.” (TSMC-1024, 218.) Sim’s authors set out to examine and address these drawbacks by testing films of different thickness, and “systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility.” They found that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.” (*Id.*) Specifically, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å causes less charge trapping and higher mobility.” (TSMC-1024, 221.) 20Å is equal to 2 nm, as recited by claim 11. This is especially true since the thickness of the high-k film is even smaller under sidewall 8 than under the gate electrode 7. Thus, the devices resulting from the combination of Matsumoto’s first or fourth embodiments with Wang and Sim provides that “*each side portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*” [11].

167. **Motivation to Combine.** Wang discloses use of HfO₂ as an example of a high-k gate dielectric (TSMC-1012, ¶12), the same film studied in Sim. Wang also discloses a preferred thickness that includes the ideal range disclosed by Sim. A POSITA would have been motivated to apply Sim’s findings regarding ideal thicknesses of a HfO₂ gate insulating film (namely, a thickness of 20Å (2 nm) or less) to the combined devices of Matsumoto’s first and fourth embodiments and Wang.

168. Sim itself explains why such a combination would have been desired. According to Sim, reducing the thickness of HfO_2 to below $20\text{\AA}$ enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (TSMC-1024, 221) Sim's teaching are consistent with Wang's goal of using a thickness of "preferably less than about $50\text{\AA}$ to maintain low gate leakage and thin equivalent oxide thickness (EOT)." (TSMC-1012, ¶26.)

169. The aforementioned combination would have been nothing more than the use of a known technique (Sim's HfO_2 dielectric layer with less than $20\text{\AA}$ thickness) to improve similar devices (the Matsumoto/Wang's semiconductor device having a high-k dielectric layer that is 5 to $50\text{\AA}$ thick), in the same way. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218.)

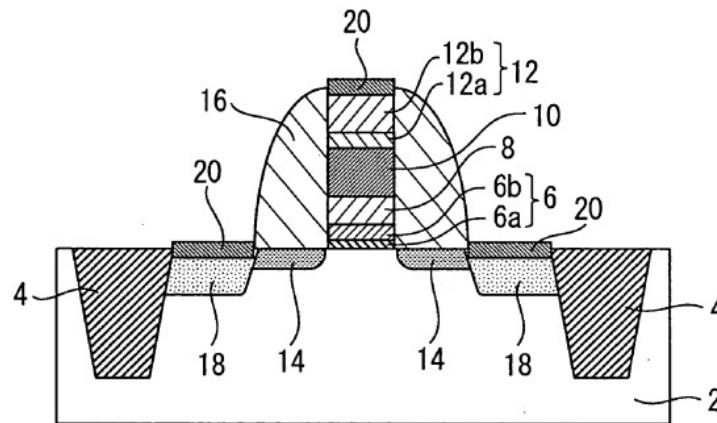
VIII. GROUND 4: Matsumoto in view of Mutou Renders Claims 2-3 Obvious.

170. As discussed above with regard to Ground 1, Matsumoto discloses, or at least renders obvious, every limitation of claim 1. To the extent Matsumoto is found not to disclose the additional limitations of claims 2-3, Mutou, discussed below, does. A POSITA would have been motivated to combine these references, thereby rendering claims 2-3 obvious.

A. Overview of Mutou

171. U.S. Publication 2005/0045938, titled “Semiconductor Device with Silicon-Germanium Gate Electrode and Method for Manufacturing Thereof,” to Akiyoshi Mutou, et al. (“Mutou”; TSMC-1019), was filed August 26, 2004, claiming priority to a JP application filed August 29, 2003, and published on March 3, 2005. As its title suggests, Mutou relates to semiconductor devices, including, specifically MOSFETS. (TSMC-1019, Abstract, ¶¶2, 4.) Mutou is therefore in the same field as Matsumoto and the ’764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).)

172. Mutou’s first embodiment is shown in Figure 1 below. As shown in Figure 1, Mutou’s transistor includes a silicon substrate 2, a gate dielectric film 6 comprising underlying interfacial layer 6a and high-k dielectric film 6b, and a gate electrode comprising a seed Si film 8, a SiGe film 10, a lower cap Si film 12 a, an upper cap Si film 12 b and a silicide layer 20. (TSMC-1019, ¶¶40-41, 44.)



Mutou, Fig. 1

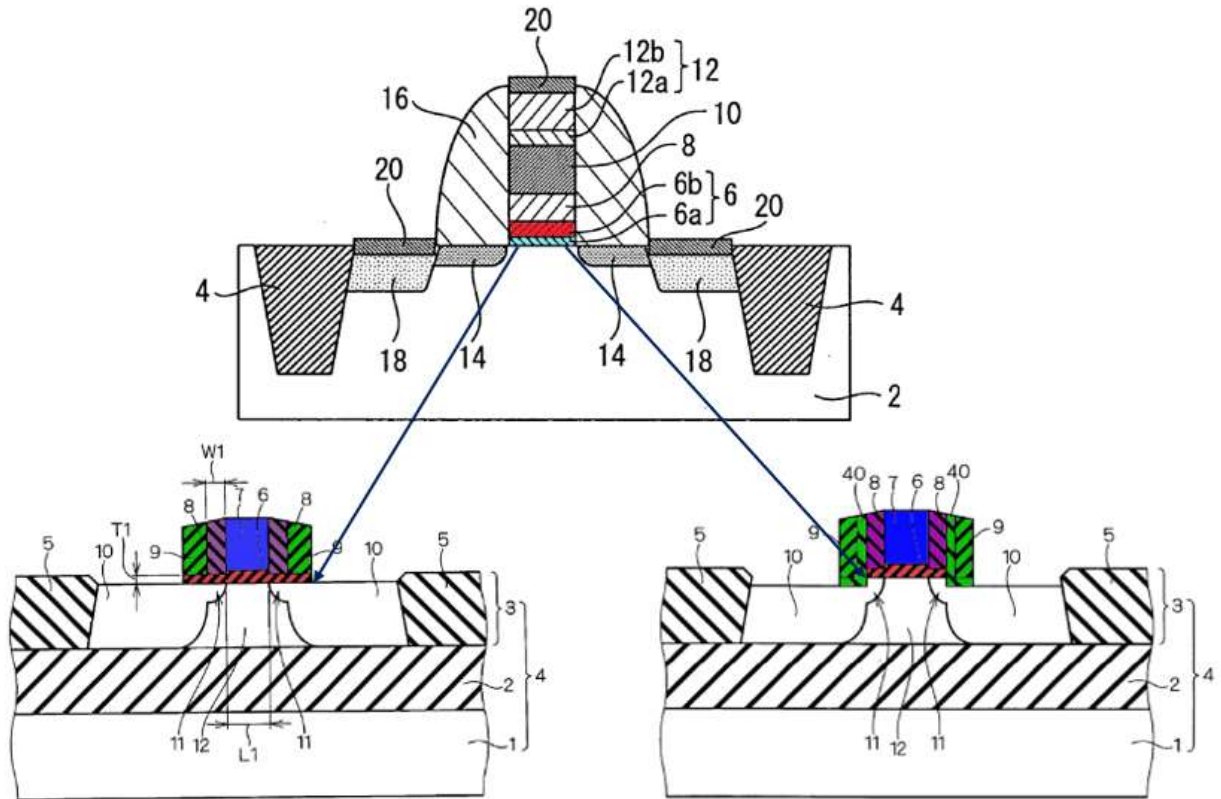
B. Dependent Claims 2-3

[2] *The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.*

[3] *The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.*

173. A POSITA would have known to combine Mutou and Matsumoto by applying Mutou's teachings regarding use of a buffer layer between a high-k dielectric and silicon substrate to Matsumoto's first and fourth embodiment semiconductor devices. Such a device, for example, would have taken the underlying interfacial layer 6a (shaded aqua) located between the substrate 2 and high-k gate dielectric 6b (shaded red) in Mutou, and placed that underlying interfacial layer between the substrate and high-k dielectric (shaded red) of Matsumoto's first embodiment (Figure 1) and fourth embodiment (Figure 22)

devices. In the combination, the resulting device is, for example, Matsumoto's transistor, with Mutou's underlying interfacial layer situated between the Matsumoto's substrate and high-k gate insulating film 6, such as shown below.



**Mutou, Fig. 1 (top);
Matsumoto, Figs. 1 (bottom-left) and 22 (bottom-right) (annotated)**

174. Mutou teaches that, “[o]n the substrate 2 in the element regions, a gate dielectric film 6 is formed.” (TSMC-1019, ¶41.) Gate dielectric film 6 includes “an underlying interfacial layer 6a formed on the silicon substrate 2; and high-k dielectric film 6b formed on the underlying interfacial layer 6a and having higher dielectric constant than the underlying interfacial layer 6a.” (TSMC-1019, ¶41.)

175. Underlying interfacial layer 6a may be, “for example, a SiO₂ film, a Si₃N₄ film, or a SiON film (hereafter collectively referred to as ‘SiO₂ film of the like’),” and acts to “inhibit interfacial reaction between the silicon substrate 2 and the high-k dielectric film 6b.” (TSMC-1019, ¶42.) A POSITA would have understood from this disclosure that Mutou’s interfacial layer 6a serves as a buffer layer between the substrate and the high-k gate insulating film, as required by claim 2, and that it is formed of silicon oxide, as required by claim 3. Thus, the combination of Matsumoto’s first and fourth embodiments with Mutou renders claims 2 and 3 obvious.

176. **Motivation to Combine.** In my opinion, a POSITA would have been motivated to combine Mutou and Matsumoto in the manner above. Mutou provides express motivation, teaching that “[t]he underlying interfacial layer 6a is acted to inhibit interfacial reaction between the silicon substrate 2 and the high-k dielectric film 6b.” (TSMC-1019, ¶42.) Inhibiting such reactions between the substrate and the high-k film decreases degradation of the high-k film and, thus, improves performance of the device. (*See also* TSMC-1001, 12:12-22 (by using a buffer insulating film, “deterioration of an interface between a substrate and a gate insulating film can be suppressed”).) This use of a buffer layer is also what Wang described as “typical.” Mutou’s interfacial layer furthers Matsumoto’s goal “to provide a semiconductor device which achieves reductions in malfunctions and

operating characteristic variations.” (TSMC-1009, ¶13.) Specifically, based on these disclosures in Mutou and Matsumoto, a POSITA would have been motivated to use Mutou’s underlying interfacial layer to inhibit interfacial reaction between the substrate and the high-k film and improve performance of Matsumoto’s semiconductor devices.

177. In my opinion, combining Mutou with Matsumoto’s first and fourth embodiments would have required nothing more than the use of a known technique (Mutou’s underlying interfacial layer) to improve similar devices (Matsumoto’s transistor using a high-k gate insulating film) in the same way (forming an underlying interfacial layer prior to forming the high-k dielectric film) and the application of a known technique (Mutou’s underlying interfacial layer) to a known device (Matsumoto’s transistor using a high-k gate insulating film) ready for improvement.

178. Mutou discloses the use of well-known processes to form its underlying interfacial layer: “Next, ... a SiO₂ film or the like ... is formed as an underlying interfacial layer 6a on the silicon substrate 2 using a method such as thermal oxidation (or thermal nitriding or thermal oxynitriding) or plasma oxidation (or plasma nitriding or plasma oxynitriding).” (TSMC-1019, ¶53.) Mutou also discloses that that deposition of the high-k dielectric film may be done “using an ALD (atomic layer deposition) method or an MOCVD (metal organic

chemical vapor deposition) method.” (TSMC-1019, ¶54.) Matsumoto similarly discloses the high-k gate insulating film is deposited using a CVD process. (TSMC-1009, ¶107.)

179. To go further, a POSITA seeking to utilize an underlying interfacial layer underlying the high-k dielectric would have utilized the teachings of Mutou and Matsumoto in succession. Matsumoto already discloses forming a layer of silicon oxide above the substrate, with other high-k dielectrics as alternative gate insulating films. (TSMC-1009, ¶107.) A POSITA wanting to include a buffer layer of silicon oxide between the substrate and the high-k gate dielectric (such as disclosed by Mutou) would have simply applied Matsumoto’s (or Mutou’s) disclosure of forming a silicon oxide layer along with (and before) Matsumoto’s (or Mutou’s) disclosure regarding using other high-k materials for the gate dielectric. Matsumoto’s remaining steps of forming the gate electrode and insulating sidewalls could then be performed.

180. In my opinion, in light of the disclosures above, a POSITA would have had a reasonable expectation of success in combining Matsumoto and Mutou in the manner discussed above, and the results of the combination would have been predictable.

IX. GROUND 5: Matsumoto in View of Ono Renders Claims 6, 10, 12, and 13 Obvious.

181. As discussed above with regard to Ground 1, Matsumoto discloses, or at least renders obvious, every limitation of claim 1. To the extent Matsumoto is found not to disclose the additional limitations of claims 6, 10, 12, and 13, Ono, discussed below, does. A POSITA would have been motivated to combine these references, thereby rendering claims 6, 10, 12, and 13 obvious.

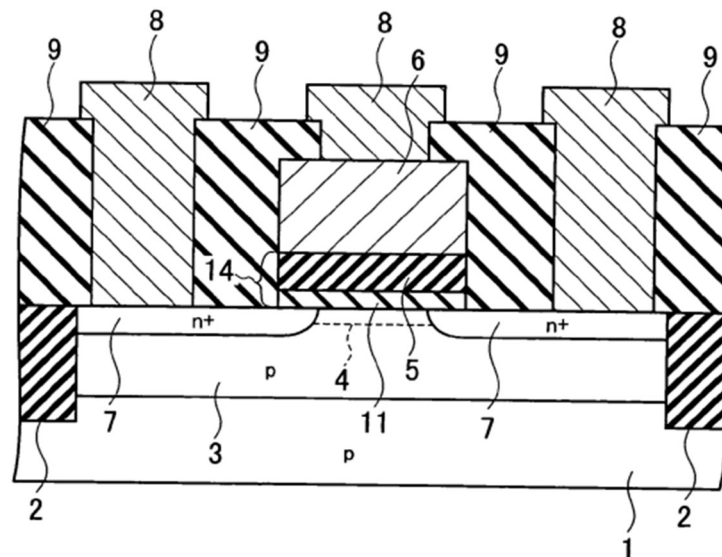
A. Overview of Ono

182. U.S. Publication 2005/0051856, titled “Semiconductor Device,” to Mizuki Ono, et al. (“Ono”; TSMC-1013), was filed July 2, 2004, claiming priority to a JP application filed September 4, 2003, and published on March 10, 2005. As its title suggests, Ono relates to semiconductor devices, including, specifically field effect transistors. (TSMC-1013, Abstract, ¶¶3-7.) Ono is therefore in the same field as Matsumoto and the ’764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).)

183. Ono discloses two base embodiments of a semiconductor device with multiple modifications applicable to each. Both embodiments include a semiconductor substrate, source and drain regions arranged at the surface of the semiconductor substrate, a gate insulator film on the substrate, and a gate electrode

on the gate insulator film. (TSMC-1013, ¶¶8-9.) In this Declaration, I will focus on Ono's second embodiment and the modifications thereto.

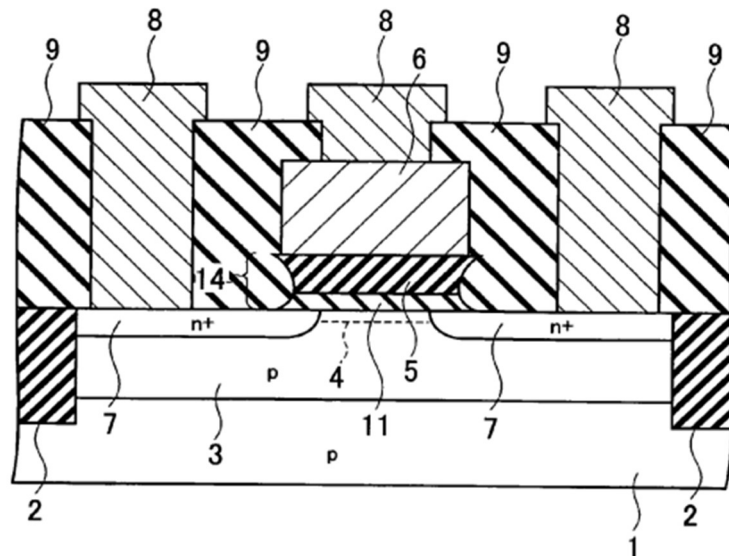
184. An example of Ono's second embodiment is illustrated in Figure 77, below. As shown in this figure, Ono's semiconductor device includes a gate stack comprising gate insulator film 11 and gate insulator film 5 made of "HfO₂ film." (TSMC-1013, ¶¶207, 209, Figure 77.) Gate electrode 6 is formed on gate insulator film 5, as shown in Figure 77 below, and can be provided with gate sidewalls. (TSMC-1013, ¶¶207, 181 (in the first embodiment, "gate sidewalls are not mentioned; however, sidewalls may be provided to the gate electrode"), 210 ("Various modifications as described in the first embodiment are also possible with this [second] embodiment, and the same effects may be obtained.").)



Ono, Fig. 77

185. Ono further discloses that the length of the gate insulating film and the shape of the side surfaces of the gate insulating film can be modified using known techniques to adjust and optimize the electrical performance of the device. (TSMC-1013, ¶216; *see also* TSMC-1013, ¶200.) For example, “the sidewalls of the gate insulator film may curve.” (TSMC-1013, ¶216.)

186. Ono provides several examples of its second embodiment where the length of the gate insulating film is varied in relation to the gate electrode (Figures 86-91), several examples where the sidewall of the gate insulating film is “slanted” (Figures 92-103), and several examples of gate insulator films with curved end portions (Figures 104-123). (TSMC-1013, ¶216.) One such example of a curved end portion is shown in Figure 108, although a POSITA would have understood that other structures are equally applicable.



Ono, Fig. 108

B. Dependent Claim 6

[6] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.*

187. Ono teaches that its gate insulator film 5 is made of a “HfO₂ film.” (TSMC-1013, ¶209.) A POSITA would have combined Ono with Matsumoto by utilizing a Hf based oxide, such as HfO₂, as the gate dielectric in the devices of Matsumoto’s first and fourth embodiments, thereby rendering claim 6 obvious.

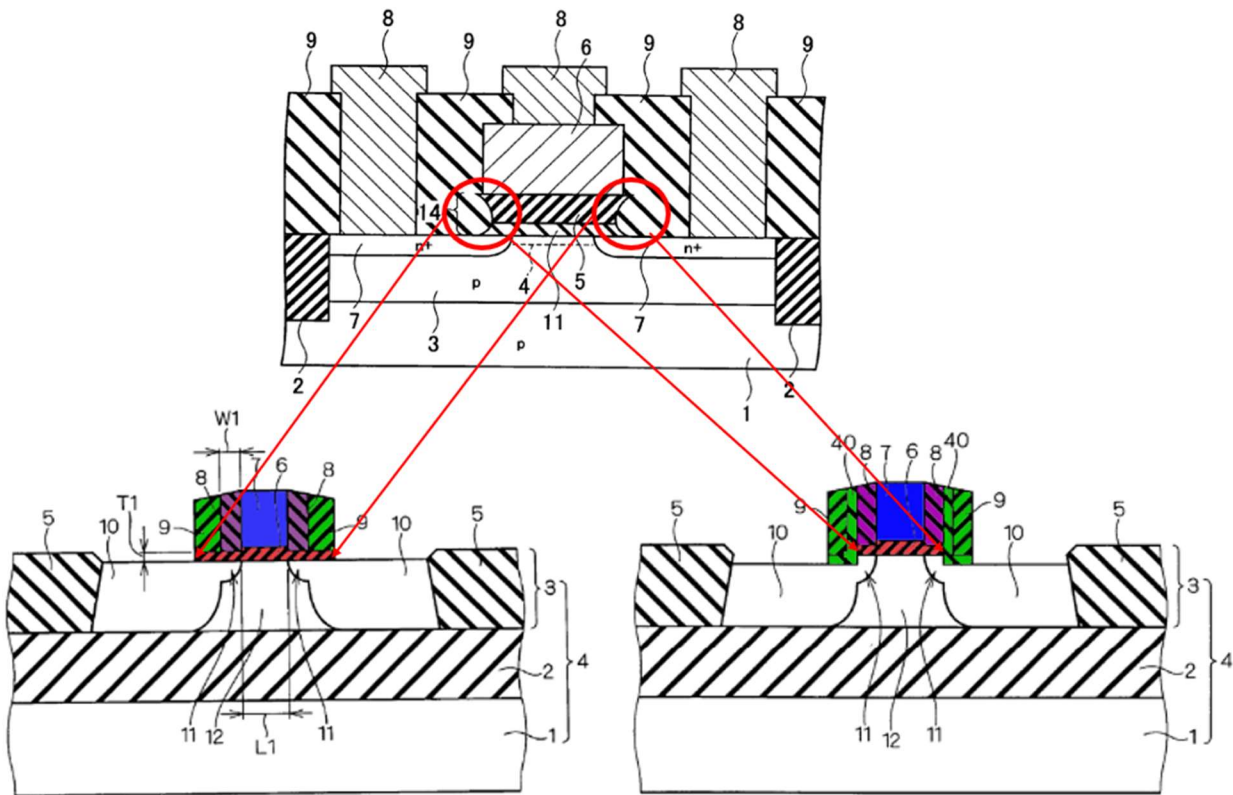
188. A POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer, as taught by Ono, in Matsumoto’s first and fourth embodiments for the reasons discussed above with regard to Matsumoto and Wang, i.e., because HfO₂ was already commonly used in the industry due to its many known benefits. (TSMC-1037, 2.4.1 (“Recently, HfO₂ films have emerged as the most promising gate dielectric material for sub 100nm technology due to its superior thermal stability with poly-Si and reasonable band alignment”); TSMC-1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 134 (“Excellent dielectric properties such as high dielectric constant, low leakage current, good thermal stability, negligible dispersion and excellent reliability were demonstrated. These results suggest that HfO₂ is a promising material for the future gate dielectric application.”).)

189. The semiconductor devices resulting from the combination of Ono and Matsumoto's first and fourth embodiments would utilize HfO_2 as gate insulating film 6, thereby satisfying the limitation of a "*high dielectric constant gate insulating film is formed of a Hf based oxide*" [6].

C. Dependent Claim 10

[10] <i>The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.</i>
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190. A POSITA would have known to combine Ono and Matsumoto by applying Ono's teaching of curving the end portion of a gate insulating film (circled below in Figure 108) to the ends of gate insulating film 6 of Matsumoto's first and fourth embodiments, such as illustrated below.



**Ono, Fig. 108 (top);
Matsumoto, Figs. 1 (bottom-left) and 22 (bottom-right) (annotated)**

191. In the devices resulting from combining Matsumoto’s first and fourth embodiments with Ono, the end portion of Matsumoto’s gate insulating film 6 has a semicircular shape such as taught by Ono and illustrated in Ono’s Figure 108. Such devices provide that “*the high dielectric constant gate insulating film includes a notch at a side end portion*” [10], consistent with the disclosure of the ’764 patent and as shown in Figure 7 of the ’764 patent, below.⁹

⁹ See, e.g., TSMC-1001, Fig. 7 (depicting notch 20 having a semicircular shape), 8:35-40 (“As shown in FIG. 7, this modified example is different from the



'764 Patent, Fig. 7 (annotated and enlarged)

192. **Motivation to Combine.** A POSITA would have been motivated to combine Ono and Matsumoto in the manner described above. Ono expressly suggests the combination, teaching that using curved side surfaces for the gate insulating film “reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel

second embodiment is that part of a high dielectric constant gate insulating film 4B located under each side end portion of the offset sidewall 6, i.e., a side portion of the high dielectric constant gate insulating film 4B is removed in a notch shape, so that a notch 20 is provided”).

region” and therefore provides “an advantage of optimization.” (TSMC-1013, ¶216; *see also* TSMC-1013, ¶200 (noting, for first embodiment, that by using curved side surfaces, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”).

193. Ono’s curved sidewall can be applied to gate insulating films that “overhang” the gate electrode as well, since it was understood that by extending the gate insulating film past the gate electrode, “the capacitive coupling between the source/drain regions 7 and the gate electrode 6 is strengthened, therefore advantages of reducing the resistance of the source/drain regions 7, controlling the parasitic capacitance as well as allowing high-speed operations are obtained.” (TSMC-1013, ¶¶215-16.)

194. Ono’s teachings to adjust the length of the gate insulating film and the shape of the end of the gate insulating film (e.g., to be curved) align with Matsumoto’s goals of reducing overlap capacitance, improving speed, and lowering power consumption by minimizing the overlap between the gate electrode and the extension regions. (TSMC-1009, ¶47.) A POSITA would have been further motivated to curve the end of Matsumoto’s gate insulating film to enhance controllability of the gate and to optimize parasitic resistance and parasitic capacitance, which improves device performance. (*See* TSMC-1040, ¶108.)

195. Applying Ono's teachings to Matsumoto's first and fourth embodiments would have been nothing more than applying a known technique (Ono's curved sidewalls for a gate insulating film) to improve similar devices (Matsumoto's transistor using a high-k gate insulating film) in the same way (modifying the dielectric layer to control capacitance). For example, Matsumoto and Ono both disclose forming high-k gate insulating films that extend under the gate electrode and the insulating sidewall using conventional techniques. (TSMC-1009, ¶114; Ono ¶167.) Given the use of known techniques, applying the teachings of Ono to Matsumoto would have been within the skills of a POSITA. A POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable.

D. Dependent Claims 12-13

[12] *The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode.*

[13] *The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall.*

196. In the combination of Matsumoto's fourth embodiment (Figure 22) and Ono, a notch is formed at each side end of Matsumoto's gate insulating film 6 located under the first insulating sidewall film 8, as described above with regard to

claim 10. In this arrangement, the end of the gate insulating film no longer extends completely under the first insulating sidewall, but rather contains a portion that curves inward from the side end surface of the first insulating sidewall towards the gate electrode. Additionally, the notch's semicircular shape (as taught by Ono) and the distance which the semicircular shape extends inward toward the gate electrode are set based on specific process parameters. A POSITA would understand such parameters, relating to the deposition and etch processes, to include, for example, etch rate, duration, pressure, gas composition, and material selectivity. By using the same process parameters, a POSITA would be able to recreate the same end shape of the gate insulating film (e.g., a semicircle as shown in Ono's Figure 108), such that the end and its distance relative to other components on the device are fixed or predetermined. Accordingly, the side end surface of the gate insulating film in the combined device of Matsumoto's fourth embodiment and Ono is *"located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode"* and *"located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall,"* as recited by claims 12 and 13, respectively, consistent with the disclosure of the '764 patent. (TSMC-1001, 21:26-30 ("side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5").)

X. GROUND 6: Matsumoto in View of Rodder Renders Claims 8-9 Obvious.

[8] *The semiconductor device of claim 1*

[8A] *wherein an extension region of a first conductivity type is formed in each of parts of the active region located under the first insulating sidewall and the second insulating sidewall, and*

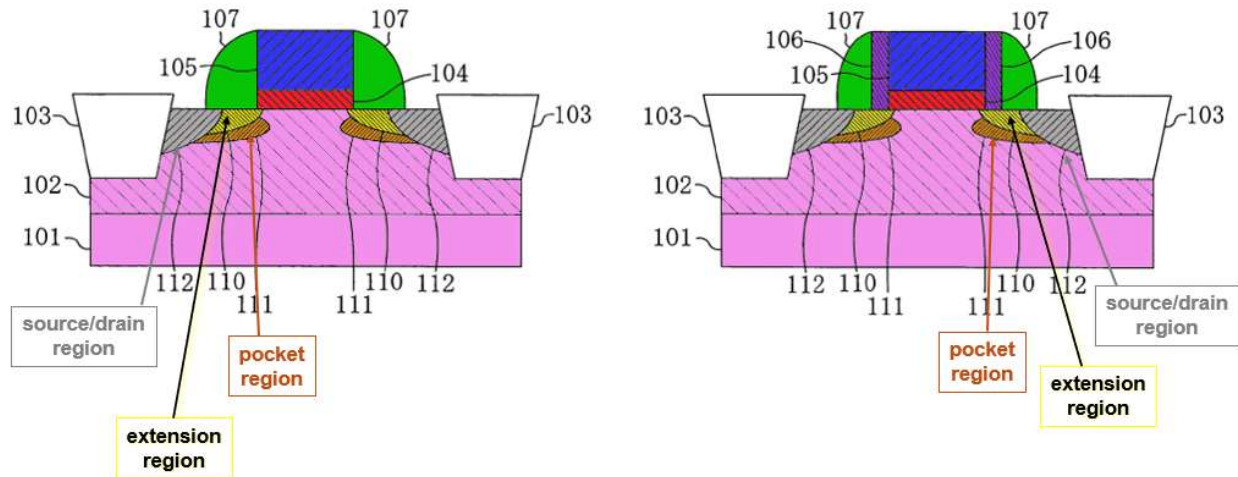
[8B] *a pocket region of a second conductivity type is formed in part of the active region located under the extension region.*

[9] *The semiconductor device of claim 8, wherein each of source/drain regions of a first conductivity type is formed in part of the active region located in an external side to the extension region and the pocket region when viewed from the gate electrode.*

197. The limitations recited by claims 8-9 were well-known and common in semiconductor devices prior to the '764 patent. The '764 patent admits as such, presenting the claimed subject matter almost verbatim in its background section when describing two prior art devices, illustrated in Figures 16A and 16B below:

A pocket region 111 is formed in part of the well 102 located under the extension region 110. Source/drain regions 112 are formed so that each of the source/drain regions 112 is provided in parts of the well 102 located at the external side to the extension region 110 and the pocket region 111 when viewed from the gate electrode 105.

(TSMC-1001, 1:45-51.)



'764 Patent, Figs. 16A (left) and 16B (right) (annotated)

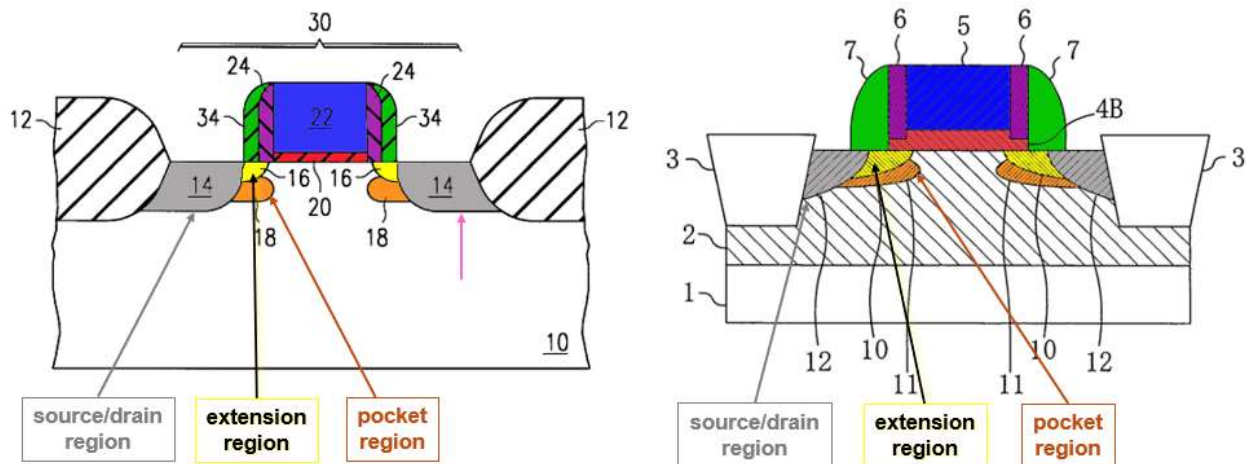
198. In light of this disclosure, Matsumoto alone, in view of Applicant's Admitted Art, renders claims 8-9 obvious. However, to the extent more is required, Rodder, discussed below, discloses these features too.

B. Overview of Rodder

199. U.S. Patent 6,306,712, titled "Sidewall Process and Method of Implantation for Improved CMOS with Benefit of Low CGD, Improved Doping Profiles, and Insensitivity to Chemical Processing" to Rodder, et al. ("Rodder"; TSMC-1023), was filed on December 3, 1998, and issued October 23, 2001.

200. Rodder discloses a transistor, which is a semiconductor device, and method for forming a transistor. (TSMC-1023, Abstract). Rodder is therefore in the same field as Matsumoto and the '764 patent. (TSMC-1001, 1:15-16 ("The present invention relates to a semiconductor device and a method for fabricating the semiconductor device."); TSMC-1009, ¶2 ("The present invention relates to a

semiconductor device and a method of manufacturing the same.”.) Rodder’s transistor is located on a substrate having “highly doped regions (n-type) 16 commonly referred to as drain extensions” and “[p]ocket regions 18 ... doped oppositely to drain extension regions 16.” (TSMC-1023, 2:61-3:1.) Rodder’s substrate also includes “deep source/drain regions 14.” (TSMC-1023, 2:62-63.) Rodder’s source/drain regions (shaded gray), drain extension regions (shaded yellow), and pocket regions (shaded orange) are shown in Figure 1, below.



Rodder, Fig. 1 (left); '764 Patent, Fig. 2 (right) (annotated)

201. As shown in the side-by-side figures above, Rodder’s Figure 1 has the same structure, including placement of the extension regions, pocket regions, and source/drain regions, as Figure 2 (as well as 16A and 16B) of the '764 patent. (See also TSMC-1001, Figures 16A-B.)

C. Dependent Claims 8-9

202. Matsumoto discloses that its first embodiment includes extensions 11 (shaded yellow) located under sidewall film 8 (the “*first insulating sidewall*”) “in the upper surface of the silicon layer 3” (part of the “*active region*” of the substrate). (TSMC-1009, ¶¶111 (“Next, n-type ions 18 such as As, P and Sb are implanted under conditions of 1×10^{13} to $1 \times 10^{15} \text{ cm}^{-2}$ to form extensions 11a in the silicon layer 3 in the future NMOSFET region.”), 113 (“Next, p-type ions 20 such as B, BF_2 and In are implanted under conditions of 1×10^{12} to $1 \times 10^{14} \text{ cm}^{-2}$ to form extensions 11b in the silicon layer 3 in the future PMOSFET region.”).) The intermediate steps for forming extensions 11 are shown, for example, in Figures 7-10 of Matsumoto.

203. Matsumoto’s substrate further includes source/drain regions, (shaded grey in Figure 1 below) which are formed in silicon layer 3 after the formation of sidewall film 9 (the “*second insulating sidewall*”). (TSMC-1009, ¶¶115 (“Then, using the photoresist 22 as an implant mask, n-type ions 23 such as As, P and Sb are implanted under conditions of 1×10^{14} to $1 \times 10^{16} \text{ cm}^{-2}$ to form source/drain regions 10a in the silicon layer 3 in the future NMOSFET region.”), 116 (“Then, using the photoresist 24 as an implant mask, p-type ions 25 such as B, BF_2 and In are implanted under conditions of 1×10^{14} to $1 \times 10^{16} \text{ cm}^{-2}$ to form source/drain

regions 10*b* in the silicon layer 3 in the future PMOSFET region.”.) These steps are shown in Figures 11-12.

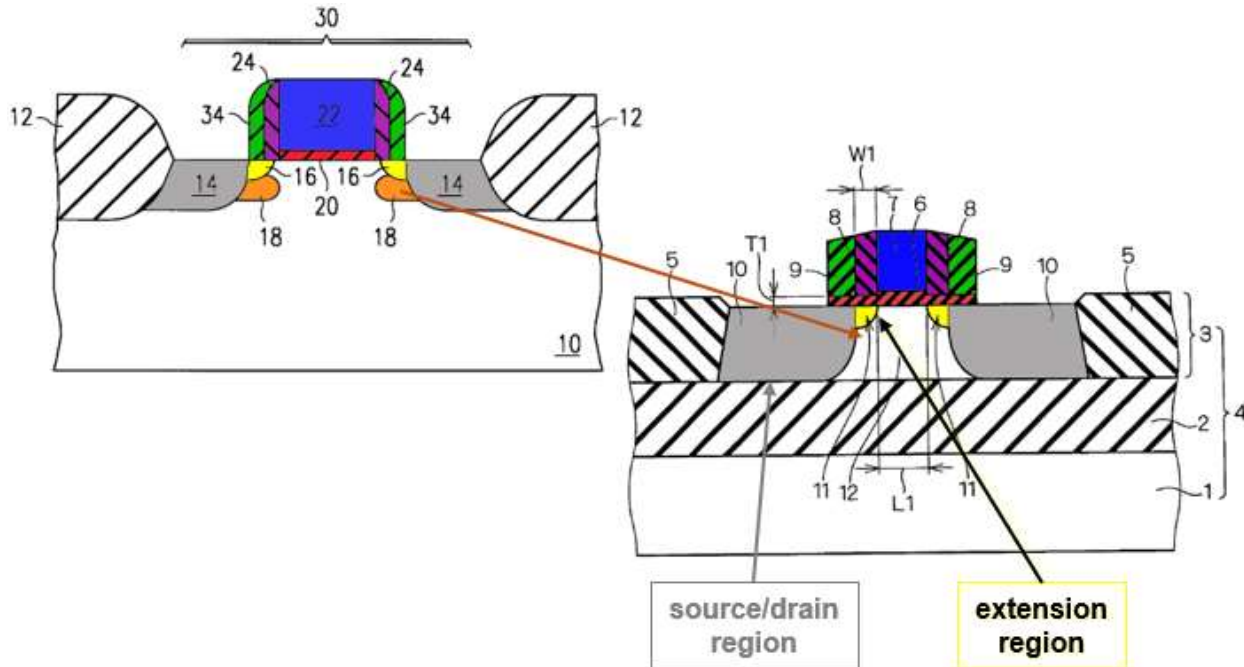
204. Matsumoto discloses that, for an NMOS device, p-type ions are implanted in the pocket region, and n-type ions are implanted in the extensions and the source/drain regions. (TSMC-1009, ¶¶111 (“Then, using the photoresist 17 as an implant mask, ions of p-type impurity such as B, BF₂ and In are implanted under conditions of 1×10^{12} to 1×10^{14} cm⁻² to form a pocket region (not shown) in the silicon layer 3 in a future NMOSFET region. The pocket region is formed to suppress a short channel effect resulting from device size reduction.”), 115.) Similarly, for a PMOS device, n-type ions are implanted in the pocket region, and p-type ions are implanted in the extensions and the source/drain regions. (TSMC-1009, ¶¶113, 116.)

205. Matsumoto does not explicitly show the extension region extending beyond sidewall film 8, but a POSITA would have understood the extension regions would remain at least partially under film 9 after creation of the source/drain regions, consistent with the ’764 patent’s description of the prior art, and also as taught by Rodder. (TSMC-1001, 1:45-51; TSMC-1023, 2:61-3:1; *see also* TSMC-1038, 463.) Matsumoto therefore teaches or at least suggests “*an extension region of a first conductivity type is formed in each of parts of the active region located under the first insulating sidewall and the second insulating*

sidewall” [8A] and “*each of source/drain regions of a first conductivity type is formed in part of the active region ...*” [9].

206. Matsumoto states that the pocket regions are not shown in its figures, but discloses methods to control where they are formed. (TSMC-1009, ¶¶112 (“Alternatively, a silicon oxide film having a predetermined thickness may be formed on the entire top surface of the resultant structure by a CVD process before forming the photoresist 17 and after the structure shown in FIG. 6 is provided, thereby to control where to form the pocket region and the extensions 11*a* in the silicon layer 3.”), 113 (“As stated above, where to form the pocket region and the extensions 11*b* in the silicon layer 3 may be controlled.”).)

207. To the extent Matsumoto does not explicitly describe the location of its pocket regions (because Matsumoto says the pocket regions are not shown in its figures), Rodder provides an explicit disclosure. For example, Rodder describes “*pocket regions*” having “opposite conductivity to” the conductivity of the extensions and placed under its extensions. (TSMC-1023, 4:35-36.) Rodder also explicitly discloses and shows that its source/drain regions are located external to the extensions and pocket regions, when viewed from the gate electrode. (*See, e.g.*, TSMC-1023, Figure 1.) A POSITA would have been motivated to combine Rodder’s teaching regarding the placement of “*pocket regions*” with Matsumoto’s first embodiment device, as shown below.



Rodder, Fig. 1 (left); Matsumoto, Fig. 1 (right) (annotated)

208. A POSITA would have combined Matsumoto's disclosure with Rodder's, resulting in a device where Matsumoto's pocket regions, which are of an opposite conductivity to the extensions and source/drain regions, are formed under the extensions such that the source/drain regions are external to the pocket regions, as explicitly taught by Rodder. Accordingly, the combination of Matsumoto's first embodiment and Rodder provides the remaining limitations of claims 8 and 9: "*a pocket region of a second conductivity type is formed in part of the active region located under the extension region*" [8B] and "*each of source/drain regions ... located in an external side to the extension region and the pocket region when*

viewed from the gate electrode” [9]. Thus, the combination of Matsumoto (first embodiment) and Rodder renders claims 8-9 obvious.

209. **Motivation to Combine.** A POSITA would have been motivated to combine Matsumoto and Rodder as set forth above because the benefits of pocket regions, and where to form them, was well-known in the art, as acknowledged by Matsumoto, Rodder, and the '764 patent itself. For example, Rodder describes well-understood benefits of “*pocket regions*” such as “reduc[ing] the threshold voltage (V_t) rolloff, reduc[ing] the nominal V_t , and thus improv[ing] the nominal drive current.” (TSMC-1023, 1:22-25; *see also* TSMC-1038, 463-64 (describing pocket implants which “reduce short-channel effects by shielding the channel from the deep source/drain diffusion”).) Matsumoto also notes that pocket regions “suppress a short channel effect resulting from device size reduction.” (TSMC-1009, ¶111.)

210. Combining Matsumoto with Rodder would have been nothing more than the use of a known technique (Rodder’s formation of pocket regions below extension regions and outside of source/drain regions) to improve similar devices (Matsumoto’s transistors having source/drain regions, extension regions, and pocket regions) in the same way (ion implantation). A POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable, because both Matsumoto and Rodder use known ion implantation

processes for forming doped regions, including pocket regions, extension regions, and source/drain regions. (TSMC-1009, ¶¶111, 113; TSMC-1023, 4:21-62; TSMC-1038, 463-64 (describing techniques for forming pocket implants).)

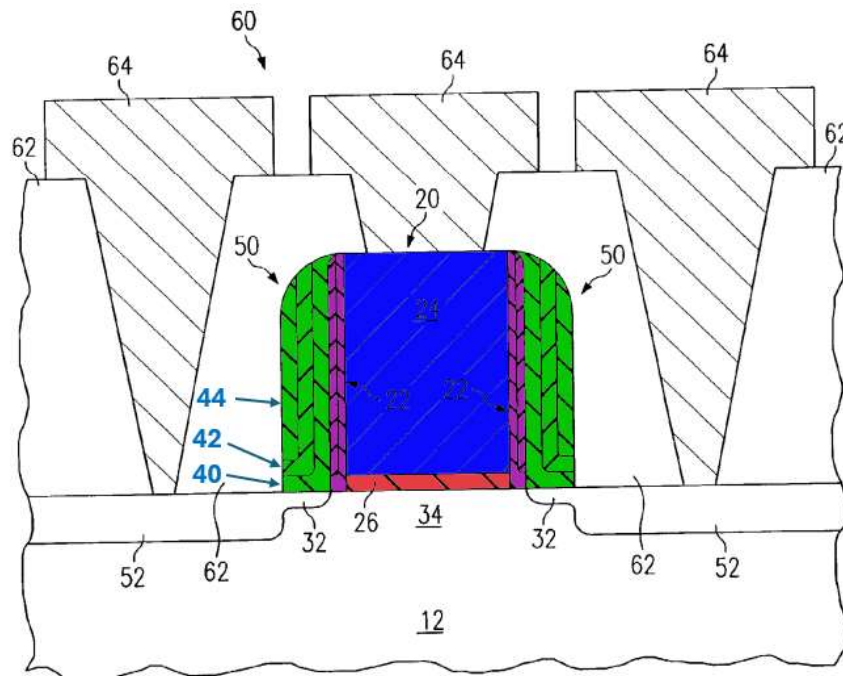
XI. GROUND 7: Matsumoto in View of Bu Renders Claim 15 Obvious.

[15] *The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.*

211. As explained above, Matsumoto renders claim 15 obvious because Matsumoto discloses both embodiments with a triple layer second sidewall and embodiments where the gate insulating film extends under at least the first insulating sidewall. However, should it be found that Matsumoto alone does not render claim 15 obvious, Matsumoto in view of Bu does.

212. U.S. Publication 2004/0110352 to Bu, et al. (“Bu”; TSMC-1025), was filed on December 10, 2002, and published on June 10, 2004. Bu discloses a method of forming a semiconductor device that includes forming one or more sidewall spacer layers on the outer surface of a gate stack. (TSMC-1025, Abstract). Bu is therefore in the same field as Matsumoto and the ’764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).) Bu’s transistor includes a gate stack 20 comprising gate conductor 24

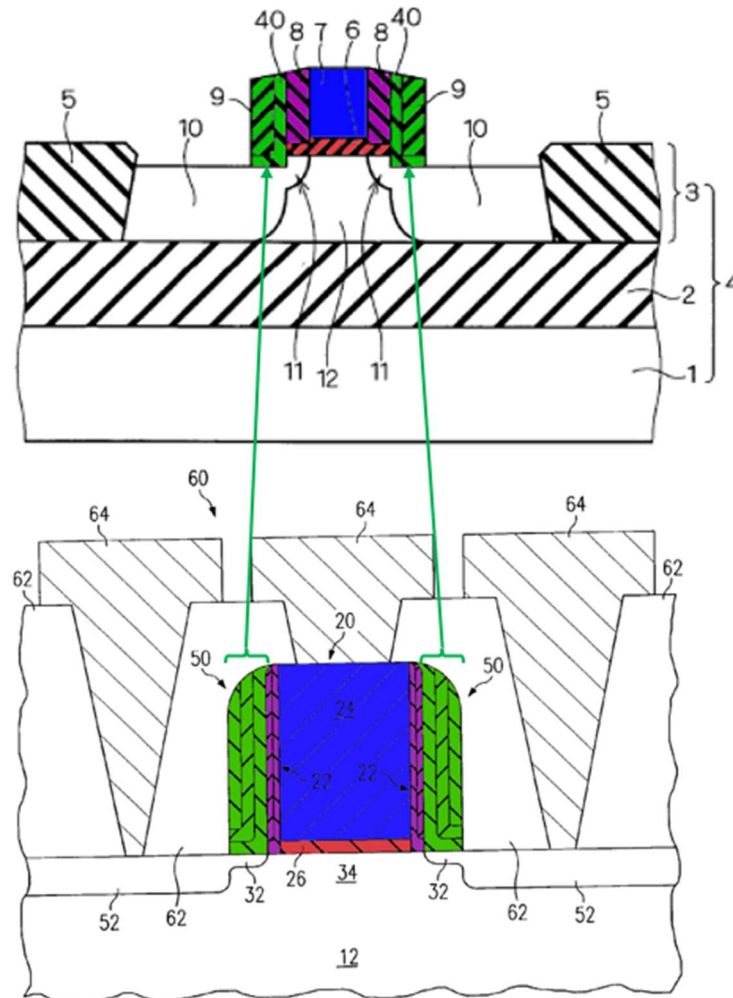
(shaded blue) and gate insulator 26 (shaded red), and sidewall spacers 22 (the “*first insulating sidewall*,” shaded purple). (TSMC-1025, ¶42, Figure 1E (below).) Bu’s transistor further includes an outer sidewall (the “*second insulating sidewall*,” shaded green) formed on sidewall spacers 22. The outer sidewall has a triple-layer “ONO” structure with a first sidewall-forming layer 40 comprised of “**oxide**”; a second sidewall-forming layer 42 comprised of “**nitride**”; and third sidewall-forming layer 44 comprised of “**oxide**.” (TSMC-1025, ¶¶26-27, 30, 35, 43, Figure 1E.) This is shown, for example, in Figure 1E of Bu, below.



Bu, Fig. 1E (annotated)

213. Matsumoto’s fourth embodiment, shown in Figure 22 below, already includes an inner “first sidewall” 8 and an double-layer outer “second sidewall”

comprised of oxide film 40 and nitride film 9. In my opinion, a POSITA would have known to implement Bu's triple-layer ONO sidewall structure with Matsumoto's fourth embodiment device by adding an additional oxide layer to Matsumoto's second sidewall (shaded green in Figure 22), as taught by Bu (shaded green in Figure 1E). The device resulting from such a combination of Matsumoto with Bu would include *"the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film"* [15].



Matsumoto, Fig. 22 (top) (annotated); Bu, Fig. 1E (bottom) (annotated)

214. **Motivation to Combine.** A POSITA would be motivated to combine Matsumoto with Bu in the manner described above. For example, a POSITA would have utilized Bu's triple-layer ONO sidewall structure with Matsumoto's device given the well-known benefits of ONO structures such as preventing stress-induced degradation at oxide-nitride interfaces and allowing independent control of spacer dimensions to optimize device scaling. (*See* TSMC-1050, ¶¶5-6, Figure 4.) Bu itself notes some of the benefits of using different materials in the sidewall structure: "film properties of sidewall-forming layers 40 and 42 may minimize dopant loss from source drain extension region 32 to first sidewall-forming layer 40. Accordingly, parasitic resistance may be lowered." (TSMC-1025, ¶26.) A POSITA would have been motivated to make the combination to obtain these benefits and improve device performance and reliability.

215. Combining Bu and Matsumoto in this manner would have been nothing more than the use of a known technique (Bu's triple-layer outer sidewall) to improve similar devices (Matsumoto's fourth embodiment transistor having a double-layer outer sidewall) in the same manner (depositing a layer of materials before etching, much like Matsumoto's formation of layers 9 and 40). A POSITA would have had a reasonable expectation of success in the combination, and the results would have been predictable, because both Matsumoto and Bu disclose

forming sidewall layers using standard deposition and etching techniques, making the application of Bu's triple layer structure to Matsumoto's design straightforward. (See TSMC-1009, ¶¶139, 162, Figure 29; TSMC-1025, ¶¶27, 30, 35, 38.)

XII. GROUND 8: Matsumoto in View of Wilk Renders Claims 18-19 Obvious.

[18] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.*

[19] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.*

216. As explained above, Matsumoto's first and fourth embodiments already disclose this limitation because the dielectric constants of materials disclosed by Matsumoto for both the gate insulating film and the second insulating sidewall are inherent to those materials. Even if it were not found to be the case, then Matsumoto in light of the knowledge of a POSITA, at a minimum, renders the limitations of claims 18-19 obvious. If this were also not found to be the case, and an explicit disclosure of dielectric constants were deemed necessary, then Wilk provides such a disclosure. The combination of Matsumoto and Wilk thus renders claims 18-19 obvious too.

217. "High-k Gate Dielectrics: Current Status and Materials Properties considerations" to Wilk, et al. ("Wilk"; TSMC-1018) was published in 2001. Wilk

describes a study of high-k dielectric candidates for use “as potential replacements for SiO₂ as the gate dielectric material for sub-0.1 μm CMOS technology.”

(TSMC-1018, Abstract.) Wilk therefore relates to semiconductor devices, which is the same field as Matsumoto and the '764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).) Table I of Wilk provides a “Comparison of relevant properties for high-k candidates,” including dielectric constants for those materials:

TABLE I. Comparison of relevant properties for high- κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).

^bMono.=monoclinic.

^cTetrag.=tetragonal.

Wilk, Table I

218. A POSITA wanting to understand the dielectric constants for high-k materials disclosed by Matsumoto would have been motivated to look to any

number of references that listed those values. Wilk is one such reference, and is specifically directed to high-k materials for gate dielectric applications. Wilk lists relevant properties of materials discussed in Matsumoto, allowing a POSITA to, for example, ensure that the gate insulating film had a optimally high dielectric constant.

219. As but one example, Matsumoto teaches use of Ta_2O_5 as the gate insulating film. (TSMC-1009, ¶107.) Wilk discloses that the dielectric constant for Ta_2O_5 is 26, which is greater than 10, as required by claim 18. (TSMC-1018, Table I.) Matsumoto also discloses that the second sidewall 9 is formed of silicon nitride (Si_3N_4), which Wilk discloses has a dielectric constant of 7. (TSMC-1009, ¶¶114, 139; TSMC-1018, Table I; TSMC-1052, Figure 4.) The dielectric constant for Ta_2O_5 is 26, which is also greater than 7, the dielectric constant of the second insulating sidewall 9.

220. Thus, in the devices resulting from the combination of Matsumoto and Wilk, “*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*” [18] and “*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*” [19].

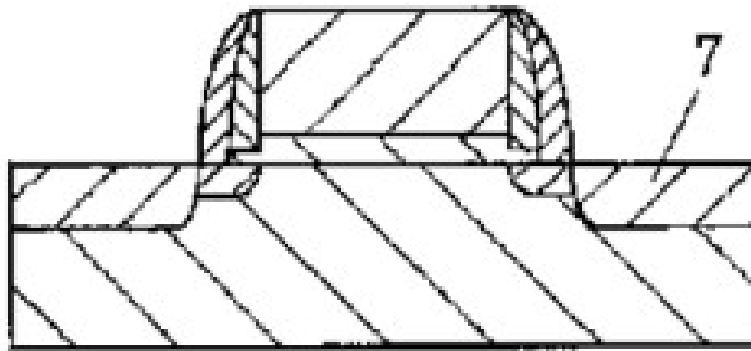
XIII. GROUND 9: Kajiyama Anticipates Claims 1, 5, 16-17, and 21.

A. Overview of Kajiyama

221. JP2003-258241 to Kajiyama (“JP-Kajiyama”; TSMC-1010), published September 12, 2003. For the purposes of my analysis, I was provided with, and conducted my analysis, using a certified translation of JP-Kajiyama. For the sake of clarity, I refer to that translation, TSMC-1011, as “Kajiyama”.

222. Kajiyama is entitled “Semiconductor Device and Manufacturing Method Thereof.” As its title suggest, Kajiyama is directed to semiconductor devices, “in particular to insulating gate type field effect transistors having a gate dielectric film (high dielectric constant material).” (TSMC-1011, ¶1.)

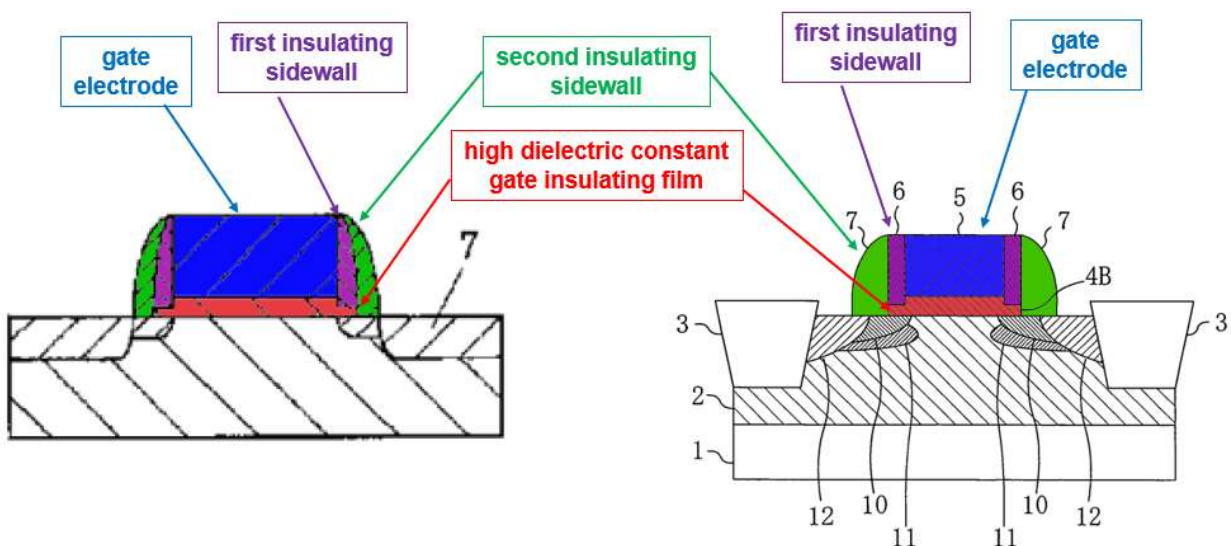
223. Kajiyama’s first embodiment is illustrated in Figure 1(D) below. As shown in Figure 1(D), Kajiyama’s semiconductor device includes a gate electrode surrounded by double sidewalls. A gate insulating film extends from under the gate electrode to under only the first sidewall, and is thicker under the gate electrode than under the first sidewall. (TSMC-1011, ¶28.)



Kajiya, Fig. 1(D)

B. Independent Claim 1

224. The semiconductor device of Kajiya's first embodiment anticipates claim 1. To illustrate this point, I have provided a side-by-side comparison of figures from Kajiya (left) and the '764 patent (right) below.



Kajiya, Fig. 1(D) (annotated); '764 Patent, Fig. 2 (annotated)

1. Preamble

[1P] *A semiconductor device comprising:*

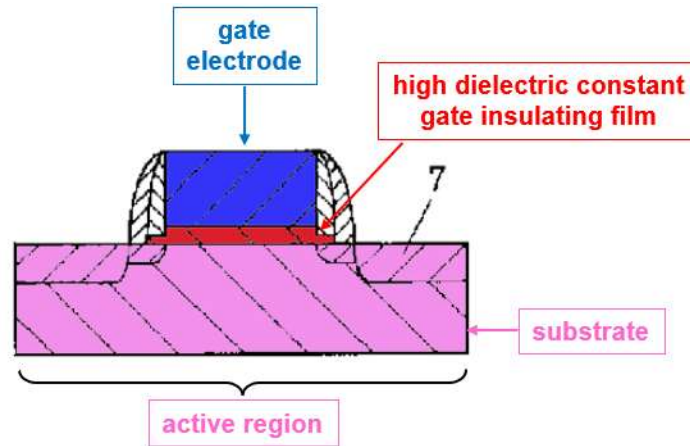
225. Kajiyama's first embodiment is a "*semiconductor device.*" Kajiyama discloses that "[t]he present invention relates to semiconductor devices." (TSMC-1011, ¶1; *see also* TSMC-1011, ¶27 ("Fig. 1 is a cross-sectional view illustrating a manufacturing process of a semiconductor device that functions as an n-type MOSFET according to a first embodiment of the present invention.").)

2. Limitation [1A]

[1A] *a high dielectric constant gate insulating film formed on an active region in a substrate*

226. Kajiyama's first embodiment includes "*a high dielectric constant gate insulating film formed on an active region in a substrate*" [1A].

227. For example, Kajiyama discloses that its device has a "p-type Si **substrate**" (shaded pink) with an "element separation layer (not shown) on the Si substrate 1." (TSMC-1011, ¶¶28-29, Figure 1(D).)



Kajiyama, Fig. 1(D) (annotated)

228. The “*active region*” of Kajiyama’s device is defined by the element separation layer, which a POSITA would have recognized to be equivalent to the ’764 patent’s STI (shallow trench isolation). (TSMC-1011, ¶¶5, 29; TSMC-1001, 7:30-47 (showing active region with source/drain regions surrounded by STI structures 3).) Within the region defined by Kajiyama’s element separation layer, an n-type LDD diffusion layer 4 is formed “on the surface of Si substrate 1” and, in a subsequent process step, an n⁺ source drain diffusion layer 7 is formed on the substrate. (TSMC-1011, ¶¶29, 32, Figs 1(A), 1(D).) Thus, consistent with the disclosures of the ’764 patent, Kajiyama’s first embodiment device has “*an active region in a substrate.*”

229. Kajiyama discloses a high dielectric constant gate insulating film formed on the active region of the substrate. For example, Kajiyama discloses that: “the semiconductor device of the present invention ... comprises a gate insulating

film consisting of a high dielectric film formed on a semiconductor substrate.”

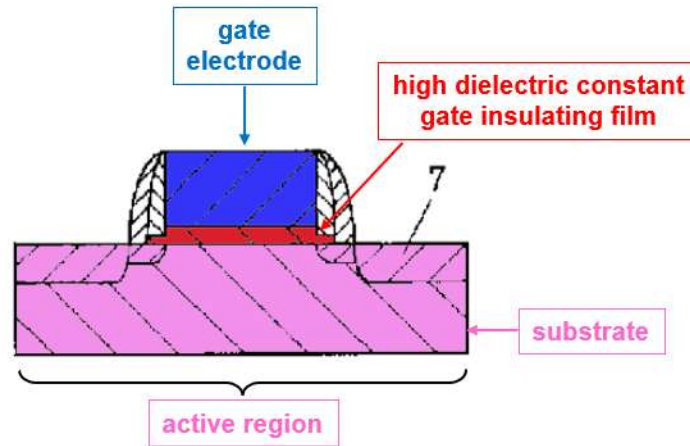
(TSMC-1011, ¶14, Fig. 1(D); *see also* TSMC-1011, ¶28.) Kajiyama also refers to its high-k gate insulating film as ZrO₂ film 2. (TSMC-1011, ¶29.) ZrO₂ is a high-k dielectric. (TSMC-1018, Table I (ZrO₂ has a dielectric constant of 25).)

230. As shown in Figure 1(D), the high-k film (shaded red) is formed on the substrate within the element separation layer and is therefore “*a high dielectric constant gate insulating film formed on an active region in a substrate.*” (TSMC-1011, ¶29.)

3. Limitation [1B]

[1B] <i>a gate electrode formed on the high dielectric constant gate insulating film</i>
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231. Kajiyama’s first embodiment device also includes “*a gate electrode formed on the high dielectric constant gate insulating film*” [1B]. For example, Kajiyama discloses that: “the semiconductor device of the present invention ... comprises ... a gate electrode consisting of a conductive film formed on a gate insulating film.” (TSMC-1011, ¶14, Fig. 1(D).) Gate electrode 3 (shaded blue) is shown on the gate insulating film (shaded red) in Figure 1(D), below.



Kajiyama, Fig. 1(D) (annotated)

4. Limitations [1C]-[1D]

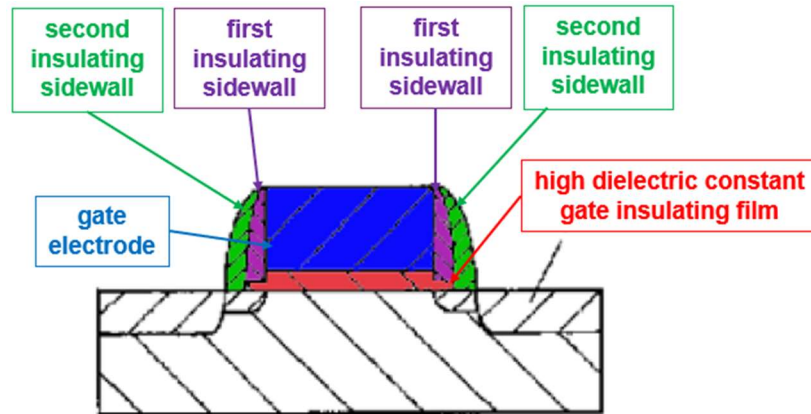
[1C] *a first insulating sidewall formed on each side surface of the gate electrode; and*

[1D] *a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween*

232. Kajiyama's first embodiment device discloses "*a first insulating sidewall formed on each side surface of the gate electrode*" [1C] and "*a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween*" [1D].

233. For example, Kajiyama discloses that "the semiconductor device of the present invention ... comprises ... a first sidewall consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall consisting of an oxidizing resistant film formed to cover the first sidewall." (TSMC-1011, ¶14, Fig.

1(D).) Kajiyama's first sidewall (shaded purple) and second sidewall (shaded green) are shown in Figure 1(D).



Kajiyama, Fig. 1(D) (annotated)

234. Kajiyama discloses that its first sidewall 5 “consist[s] of ZrO_2 film (insulation film).” (TSMC-1011, ¶28.) Kajiyama’s first sidewall 5 is therefore “a first insulating sidewall formed on each side surface of the gate electrode” [1C].

235. As shown above in Figure 1(D), Kajiyama’s second sidewall is also formed on the side surface of the gate electrode, with first sidewall 6 situated between the gate electrode and the second sidewall. (TSMC-1011, ¶28.) Second sidewall 6 is a silicon nitride film 6 (referred to as Si_3N_4 film), which is also understood to be an insulating material. (TSMC-1011, ¶28.) Kajiyama’s second sidewall and is therefore “a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween” [1D].

5. Limitations [1E]-[1F]

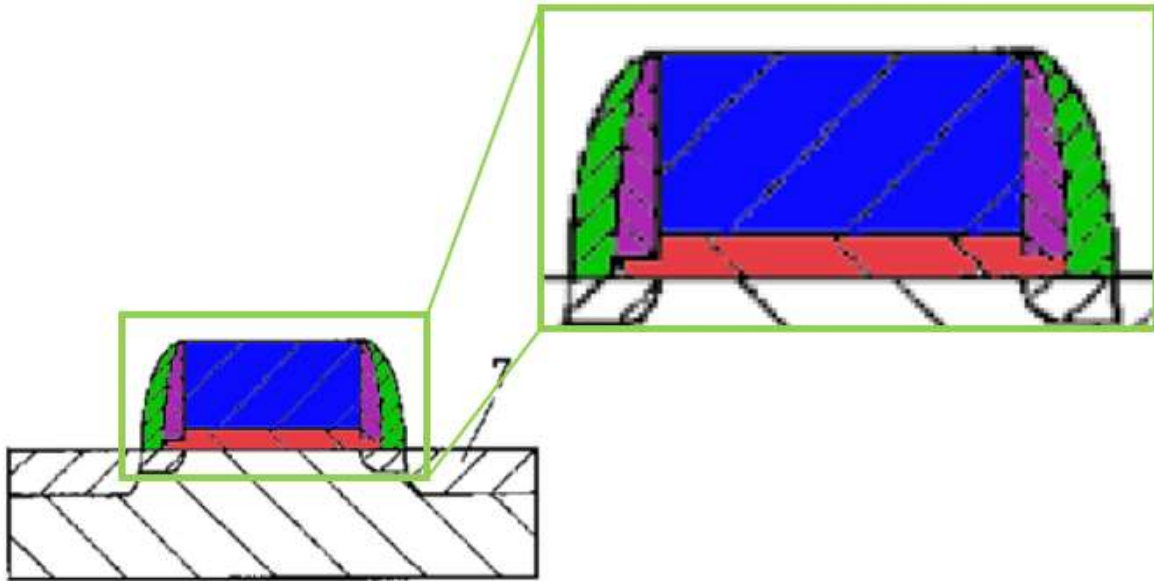
[1E] *wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall; and*

[1F] *part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode*

236. Limitation [1E] recites “*the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode **to under the first insulating sidewall***” and limitation [1F] recites “*part of the high dielectric constant gate insulating film located **under the first insulating sidewall** has a **smaller thickness** than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.*”

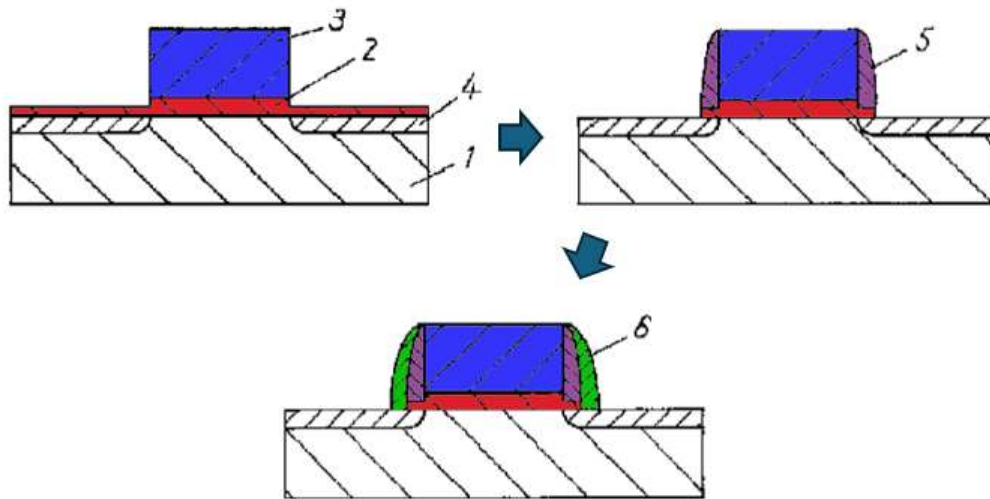
237. These limitations focus on the dimensions (e.g., width and thickness) of the gate insulating film in relation to the gate electrode and insulating sidewalls. In my opinion, Kajiyama discloses these limitations.

238. As shown Kajiyama’s Figure 1(D), the high-k film 2 (shaded red) is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode to under first sidewall 5 (the “*first insulating sidewall*,” shaded purple). The high-k film is thinner under sidewall 5 (the “*first insulating sidewall*”) than it is under the gate electrode (shaded blue). Kajiyama’s device therefore discloses limitations [1E]-[1F].



Kajiyama, Fig. 1(D) (annotated and enlarged)

239. Kajiyama’s fabrication process confirms this. During fabrication of Kajiyama’s device, an n-type polySi film is deposited on high-k film 2 and etched “to form a gate electrode 3.” (TSMC-1011, ¶29.) As part of that process, high-k film 2 “is also etched to reduce the film.” (TSMC-1011, ¶29.) As a result of this process, the thickness of high-k film 2 is larger under the gate electrode than in the areas surrounding the gate electrode. This is shown in Figure 1(A), below.



Kajiyama, Figs. 1(A) (top-left), 1(B) (top-right), and 1(C) (bottom) (annotated)

240. After forming the gate electrode 3 (shaded blue) and partially etching the insulating film (shaded red), first sidewall 5 (shaded purple) is formed on the side of gate electrode 3 and over the thinner portion of the high-k film. (TSMC-1011, ¶30.) This is shown in Figure 1(B), above.

241. Next, the high-k film 2 is then etched “to remove all.” (TSMC-1011, ¶30.) That is, the high-k film outside the outer edge of sidewall 5 is etched down to the substrate and completely removed, leaving only the portions of the film covered by the gate electrode and first insulating sidewall. Then, second sidewall 6 (shaded green) is formed “to cover the first sidewall 5 provided on the sidewall of the gate electrode 3.” (TSMC-1011, ¶31.) This is shown in Figure 1(C) of Kajiyama, above. As shown in Figure 1(C) above, a portion of the high-k dielectric

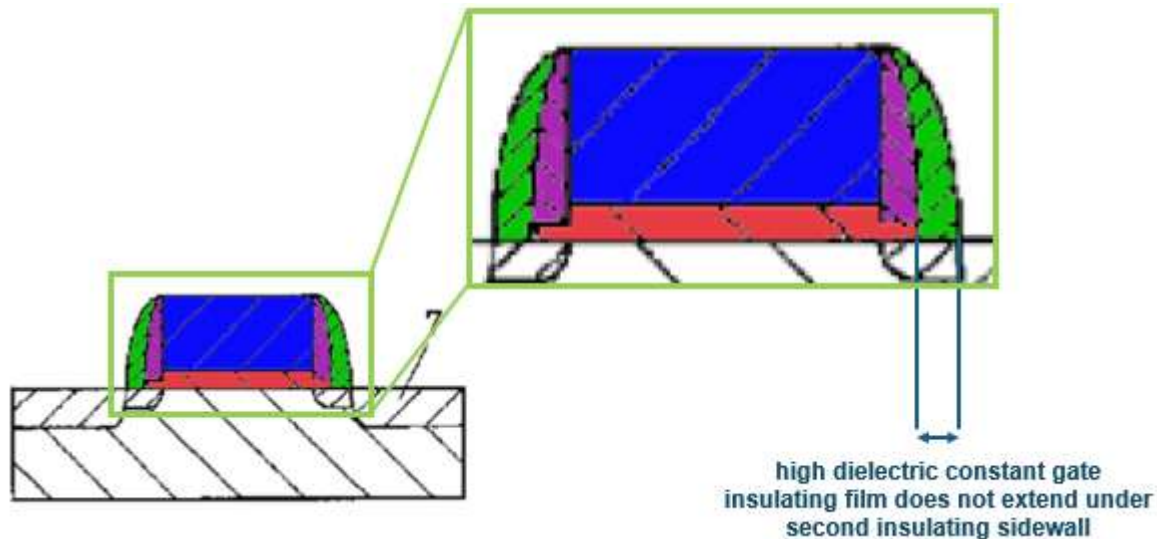
film (shaded red) remains under the gate electrode and first sidewall 5 (shaded purple) but does not extend under sidewall 6 (shaded green).

C. Dependent Claim 5

[5] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.*

242. Kajiya's first embodiment discloses this limitation.

243. As shown in Figure 1(D) below, high-k dielectric film 2 (shaded red) is formed so as to be located only under gate electrode 3 (shaded blue) and first sidewall 5 (shaded purple). It is not located under sidewall 6 (the “*second insulating sidewall*,” shaded green).



Kajiya, Fig. 1(D) (annotated and enlarged)

244. As discussed above, the fabrication process confirms the structure illustrated in Figure 1(D). As part of this process, the high-k film outside the outer

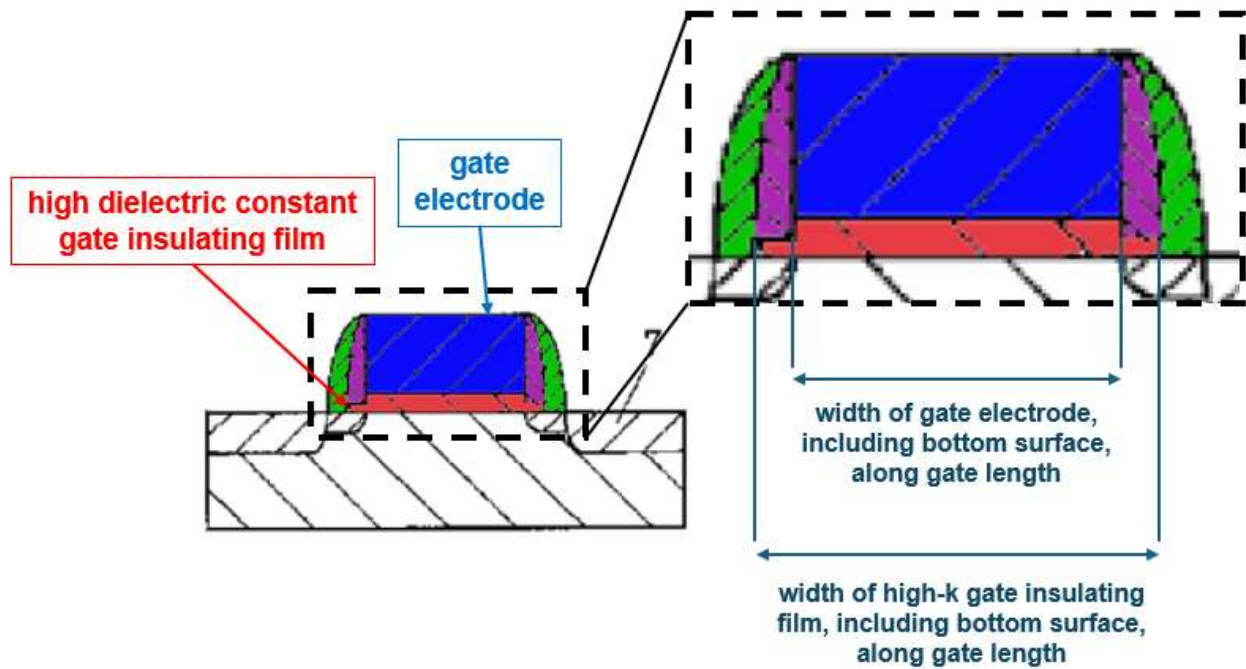
edge of sidewall 5 is etched down to the substrate and completely removed, leaving only the portions of the film covered by the gate electrode and first insulating sidewall, before the second insulating sidewall is formed. (See TSMC-1011, ¶¶30-31.)

D. Dependent Claims 16-17

[16] *The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.*

[17] *The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.*

245. These claims address the width of the gate insulating film relative to the gate electrode. Kajiyama's first embodiment discloses these limitations. As discussed above with regard to limitation [1E], Kajiyama's high dielectric gate insulating film 2 in extends from under the gate electrode to under the first insulating sidewall. This can be seen in Figure 1(D), below. As shown below, the width of high-k gate insulating film 2 (shaded red) along the gate length (which is also the same as the width of the bottom surface of high-k gate insulating film 2) is larger than the width of the gate electrode 3 (shaded blue) along the gate length (which is also the same as the width of the bottom surface of the gate electrode). Kajiyama thus discloses both the limitations of claims 16 and 17.



Kajiyama, Fig. 1(D) (annotated and enlarged)

E. Dependent Claim 21

[21] *The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film is not in contact with the first insulating sidewall.*

246. Kajiyama's first embodiment teaches this limitation, consistent with the disclosures of the '764 patent.

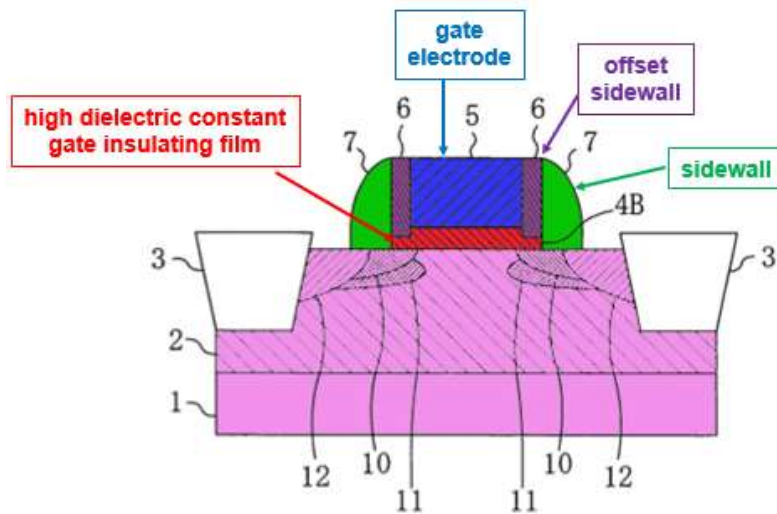
247. As discussed above with regard to Matsumoto and claim 21, a POSITA reading the '764 patent would have understood from the disclosures of the '764 patent that this limitation is met when the end of the gate insulating film

does not contact the side of the first, or offset, sidewall,¹⁰ but rather, the gate insulating film extends under the first insulating sidewall. (*See, e.g.*, TSMC-1001, 2:12-16 (“a high dielectric constant gate insulating film is **kept remaining under sidewalls to prevent end portions of the high dielectric constant gate insulating film from being in contact with the sidewalls.**”), 4:39-48 (“According to the present invention, a high dielectric constant gate insulating film is continuously formed so as to extend from under a gate electrode to under a sidewall. In other words, continuity of the high dielectric constant gate insulating film at a gate end portion is maintained. Thus, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film at the gate end portion, caused by a side end portion of the high dielectric constant gate insulating film being in direct contact with a sidewall film, can be suppressed.”); *see also* TSMC-1001, Figs. 2, 3, 16A, 16B.)

248. Figure 2 of the '764 patent, which corresponds to the second embodiment of the '764 patent, illustrates an exemplary device in which “each side

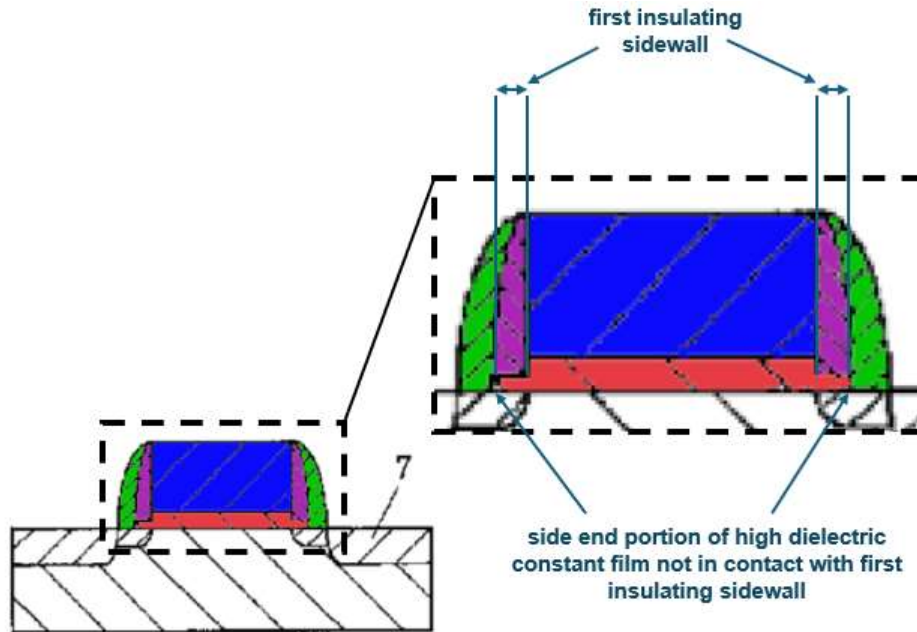
¹⁰ A POSITA would have understood from this discussion that the side of the gate insulating film disposed under the gate electrode is not the “side **end** portion” of the gate insulating film, as recited by claim 21. Rather, that term refers to the outer side ends of the gate insulating film.

end portion of the high dielectric constant gate insulating film 4B is not in contact with the offset sidewall 6 and continuity of the high dielectric constant gate insulating film 4B at an end portion of the gate electrode 5 is maintained.” (TSMC-1001, 7:60-64.)



'764 Patent, Fig. 2 (annotated)

249. As discussed above with regard to limitation [1E], in Kajiyama's first embodiment, the gate insulating film 2 (shaded red) extends from beneath the gate electrode 3 (shaded blue) to under the first sidewall 5 (shaded purple) and ends at the second sidewall 6 (shaded green). The side end portion of film 2 therefore is not in contact with sidewall 5, as that phrase is used in the '764 patent. This is shown in Kajiyama Figure 1(D), below, which also resembles the arrangement of Figure 2 of the '764 patent, shown above.



Kajiyama, Figure 1(D) with enlargement

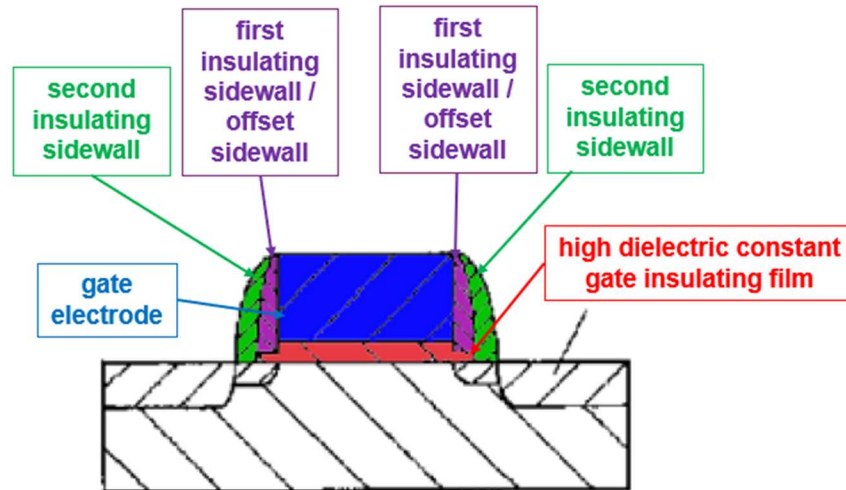
XIV. GROUND 10: Kajiyama Renders Claims 4, 6, and 18-20 Obvious.

A. Dependent Claim 4

[4] *The semiconductor device of claim 1, wherein the first insulating sidewall is an offset sidewall.*

250. Kajiyama's first embodiment, at a minimum, renders this limitation obvious. As discussed above with regard to limitation [1C], in Kajiyama's first embodiment, first sidewall 5 is the "*first insulating sidewall*." Kajiyama does not explicitly refer to first sidewall 5 as an "offset" sidewall, but a POSITA would have understood that first sidewall 5, located between gate electrode 3 and second sidewall 6, to be an offset sidewall, consistent with the disclosures of the '764 patent specification. For example, the '764 patent refers to an inner sidewall as an

offset sidewall: “An insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween.” (TSMC-1001, 7:37-39, Figure 2.) Kajiyama’s first sidewall 5 meets the same description. (See also TSMC-1034, 216-17, Figure 5-25.)



Kajiyama, Fig. 1(D) (annotated)

B. Dependent Claim 6

[6] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.*

251. Kajiyama’s teachings offer flexibility regarding high-k dielectric materials, initially describing a ZrO_2 film as the gate insulating film in the first embodiment. Kajiyama also states that “other high dielectric films, such as a **HfO_2 film**, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention” (TSMC-1011, ¶45), indicating that the use of alternative high-k materials, including HfO_2 , was within the scope of the invention. To the extent this

is not found to be an explicit disclosure of a gate insulating film “*formed of a Hf based oxide*,” it would have been obvious. In light of Kajiyama’s suggestion to use other high dielectric constant films such as HfO₂ as a viable substitute for ZrO₂, a POSITA would have been motivated to select HfO₂. Furthermore, the rationale established above regarding Matsumoto in view of Wang demonstrates that a POSITA would find HfO₂ an advantageous high-k choice, rendering claim 6 obvious in light of Kajiyama.

C. Dependent Claims 18-19

[18] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.*

[19] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.*

252. Kajiyama’s first embodiment discloses this limitation because the dielectric constants of materials disclosed by Kajiyama for the gate insulating film and the second insulating sidewall are inherent to those materials. Even if that were not found to be the case, then at a minimum, using knowledge of a POSITA, as reflected in AAPA, Kajiyama renders the limitations of claims 18-19 obvious.

253. The “*relative dielectric constant*” is an inherent property of a material. Indeed, the ’764 patent admits that a “high dielectric constant film formed of a Hf based oxide, Al based oxide or the like [] **has a relative dielectric constant of 10**

or more, instead of an SiO₂ based insulating film having a **relative dielectric constant of about 4.**” (TSMC-1001, 1:28-31.) Kajiyama teaches that, in addition to ZrO₂ “other high dielectric films, such as a HfO₂ film, a Ta₂O₅ film, or a Al₂O₃ film, can be used instead to obtain the effects of the invention.” (TSMC-1011, ¶45.) ZrO₂ has a dielectric constant of 25, HfO₂ has a dielectric constant of 25, and Ta₂O₅ has a dielectric constant of 26, all of which are greater than 10. (TSMC-1018, Table I.) Kajiyama thus teaches claim 18.

254. Kajiyama also discloses that the second sidewall 6 is comprised of silicon nitride (Si₃N₄), which is known to have a dielectric constant of approximately 7. (TSMC-1011, ¶28; TSMC-1018, Table I.) While Kajiyama itself does not expressly disclose the relative dielectric constants of the listed materials, the dielectric constant is a material property and, therefore, the dielectric constants for ZrO₂, HfO₂, Ta₂O₅, and Si₃N₄ are necessarily present in Kajiyama, and would have been understood by a POSITA reading Kajiyama. Because Kajiyama’s second sidewall 6 is comprised of silicon nitride (Si₃N₄), which has a dielectric constant of 7, and Kajiyama’s high-k gate insulating film can be a number of materials with a dielectric constant greater than 20, Kajiyama discloses “*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*” as recited by claim 19.

D. Dependent Claim 20

[20] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed to have a convex cross-sectional shape.*

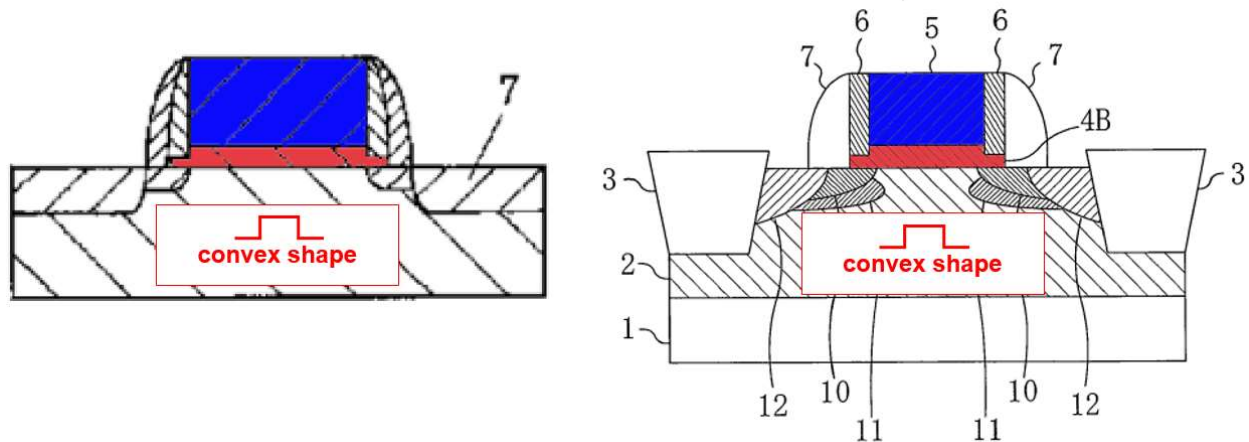
255. Kajiyama's first embodiment discloses this limitation, consistent with the disclosures of the '764 patent.

256. The '764 patent discusses forming gate insulating film to have a convex cross-sectional shape:

It is a second feature of this [second] embodiment that the thickness of the part of the high dielectric constant gate insulating film 4B located under the offset sidewall 6 is smaller than a thickness of the part of the high dielectric constant film 4B located under the gate electrode 5. **That is, the gate insulating film 4B is formed so as to have a convex shape.**

(TSMC-1001, 7:54-59; *see also* TSMC-1001, 8:62-67.)

257. Kajiyama discloses a similar structure. As discussed above with regard to limitation [1F], in Kajiyama's first embodiment device, the part of the gate insulating film that is under the first insulating sidewall has a smaller thickness than the part of the gate insulating film under the gate electrode. This forms a gate insulating film having a generally convex cross-sectional shape, consistent with the disclosure of the '764 patent. (TSMC-1001, 7:54-59 (describing the gate insulating film 4B as having "**a convex shape**").) This is shown in the figures below.



Kajiyama, Fig. 1(D) (left); '764 Patent, Fig. 2 (right) (annotated)

II. GROUND 11: Kajiyama in View of Wang Renders Claims 7 and 11 Obvious.

258. As discussed above with regard to Ground 9, Kajiyama discloses every limitation of claim 1. To the extent Kajiyama is found not to disclose the additional limitations of claims 7 and 11, Wang does. A POSITA would have been motivated to combine these references, thereby rendering claims 7 and 11 obvious. As I noted above, Wang relates to semiconductor devices (TSMC-1012, ¶2), so it is in the same field as Kajiyama and the '764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1011, ¶1 (“The present invention relates to semiconductor devices.”).)

A. Dependent Claim 7

[7] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a HfSiON film.*

259. Kajiyama's teachings offer flexibility regarding high-k dielectric materials, initially describing a ZrO₂ film as the exemplary gate insulating film in the first embodiment, but also stating that "**other high dielectric films, such as a HfO₂ film, ... can be used instead.**" (TSMC-1011, ¶45.) Wang teaches the use of similar high-k dielectrics, including, specifically, "**HfSiON**, amorphous **HfSiON**, Ta₂O₅, TiO₂, Al₂O₃, ZrO₂, **HfO₂**, Y₂O₃, La₂O₃, aluminates, silicates, **HfAlO_x**, TiO₂, PbTiO₃, BaTiO₃, SrTiO₃, and PbZrO₃, and combinations thereof." (TSMC-1012, ¶12; *see also* TSMC-1012, ¶¶ 9, 25.)

260. Kajiyama already discloses the use of HfO₂ as the high-k gate dielectric. As explained above with regard to Ground 2, Hf-based dielectrics (e.g., HfO₂ and **HfSiON**) such as disclosed by Wang (TSMC-1012, ¶¶9, 25) were already recognized as a leading material for high-k gate dielectrics prior to 2005. (TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 134.) A POSITA would have been motivated to use HfSiON to enhance operation of Kajiyama's device because nitrogen incorporation was found to improve thermal stability and electrical characteristics of HfSiON, including by enhancing the dielectric constant of the film. (TSMC-1029, 849.)

B. Dependent Claim 11

<p>[11] <i>The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.</i></p>

261. The combination of Kajiyama with Wang discloses this limitation.

262. Wang discloses that the high-k dielectric layer 6 “is preferably less than about 50 Å to maintain low gate leakage and thin equivalent oxide thickness (EOT).” (TSMC-1012, ¶26.) For an exemplary HfSiON gate insulating layer, the film “was deposited to a thickness of about 5 to 50 Angstroms and having an equivalent oxide thickness (EOT) of less than about 2.0 nanometers.” (TSMC-1012, ¶34.) Wang also specifically claims a device “wherein the high-k dielectric has a thickness from about 5 to 50 Å.” (TSMC-1012, claim 3). A POSITA would have been motivated to use thinner gate insulating films, as taught by Wang, consistent with the goals of miniaturizing semiconductor devices.

263. In the combined device of Kajiyama and Wang, the thickness of the high-k gate insulating film at its side ends would also range from about less than 5 Angstroms to less than 50 Angstroms since the thickness of the layer is smaller under first sidewall 5 than under the gate electrode. The range of 5 to 50 Å is equivalent to 0.5 to 5 nm, and thus Wang’s preferred range includes thicknesses less than 2 nm, as recited by claim 11. Put another way, the thickness of 2 nm (20 Angstroms) falls within the range of thicknesses disclosed by Wang.

264. I am informed and understand that where a claimed range overlaps with a range disclosed in the prior art, there is a presumption of obviousness, and it becomes the patentee's burden to present evidence of teaching away, unexpected results or criticality, or other pertinent objective indicia indicating that the overlapping range would not have been obvious in light of that prior art." Based on my review of the intrinsic record, there is no discussion, evidence, or justification for the selection of 2 nm as the thickness of the gate insulating film. Thus, the combination of Kajiyama and Wang renders obvious that "*each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*" [11].

III. GROUND 12: Kajiyama in View of Sim Renders Claim 11 Obvious.

[11] <i>The semiconductor device of claim 1, wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less.</i>
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265. Should an argument be made that the combination of Kajiyama and Wang does not render claim 11 obvious, Sim provides this feature as discussed in Ground 3, above. The combination of Kajiyama and Sim thus also renders claim 11 obvious. As I noted above, Sim relates to semiconductor devices (TSMC-1024, Abstract), so it is in the same field as Kajiyama and the '764 patent. (TSMC-1001, 1:15-16 ("The present invention relates to a semiconductor device and a method

for fabricating the semiconductor device.”); TSMC-1011, ¶1 (“The present invention relates to semiconductor devices.”).)

266. As explained above, Sim explicitly describes use of a HfO₂ gate insulating film having a thickness 2 nm or less. Specifically, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20Å causes less charge trapping and higher mobility.” (TSMC-1024, 221.) 20Å is equal to 2 nm, as recited by claim 11.

267. Kajiyama discloses use of HfO₂ as a high-k gate dielectric (TSMC-1011, ¶45), the same film studied in Sim. A POSITA would have been motivated to apply Sim’s teachings in the device of Kajiyama’s first embodiment to form a HfO₂ gate insulating film with a thickness of 20Å (2 nm) or less. This is especially true since the thickness of the high-k film is even smaller under first sidewall 5 than under the gate electrode. Thus, the device resulting from the combination of Kajiyama and Sim provides that “*each side portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less*” [11].

268. **Motivation to Combine.** A POSITA would have been motivated to combine Kajiyama and Sim in the manner described above. Kajiyama discloses use of HfO₂ as an example of a high-k gate dielectric (TSMC-1011, ¶145, the same film studied in Sim. A POSITA would have been motivated to apply Sim’s

findings regarding ideal thicknesses of a HfO₂ gate insulating film (namely, a thickness of 20Å (2 nm) or less) to Kajiyama's semiconductor device.

269. Sim itself explains why such a combination would have been desired. According to Sim, reducing the thickness of HfO₂ to below 20Å enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (TSMC-1024, 221) The aforementioned combination would have been nothing more than the use of a known technique (Sim's HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices (the Kajiyama's semiconductor device having a HfO₂ high-k gate dielectric layer), in the same way. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218.)

IV. GROUND 13: Kajiyama in View of Rodder Renders Claims 8-9 Obvious.

[8] *The semiconductor device of claim 1*

[8A] *wherein an extension region of a first conductivity type is formed in each of parts of the active region located under the first insulating sidewall and the second insulating sidewall, and*

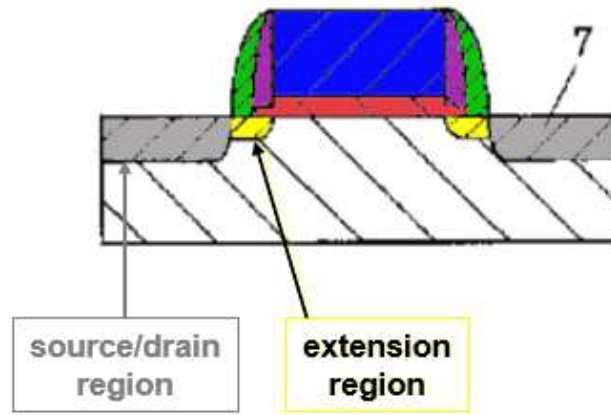
[8B] *a pocket region of a second conductivity type is formed in part of the active region located under the extension region.*

[9] *The semiconductor device of claim 8, wherein each of source/drain regions of a first conductivity type is formed in part of the active region located in an external side to the extension region and the pocket region when viewed from the gate electrode.*

270. As explained above with regard to Ground 6, the limitations recited by claims 8-9 were well-known and common in semiconductor devices prior to the '764 patent. The '764 patent admits as much, presenting the claimed subject matter almost verbatim in its background section when describing two prior art devices, illustrated in Figures 16A, 16B. (TSMC-1001, 1:45-51; Figs. 16A, 16B).

271. Kajiyama discloses a device having an **n-type** LDD diffusion layer 4 (“*extension region*”) (shaded yellow) located under first sidewalls 5 and second sidewalls 6 and “on the surface of Si substrate 1” (part of the “*active region*” of the substrate). (TSMC-1011, ¶29, Figure 1(D).) Kajiyama also discloses that its device further includes “an **n⁺** source drain diffusion layer 7” formed after first and second sidewalls 5, 6. (TSMC-1011, ¶32.) Kajiyama therefore teaches “*an extension*

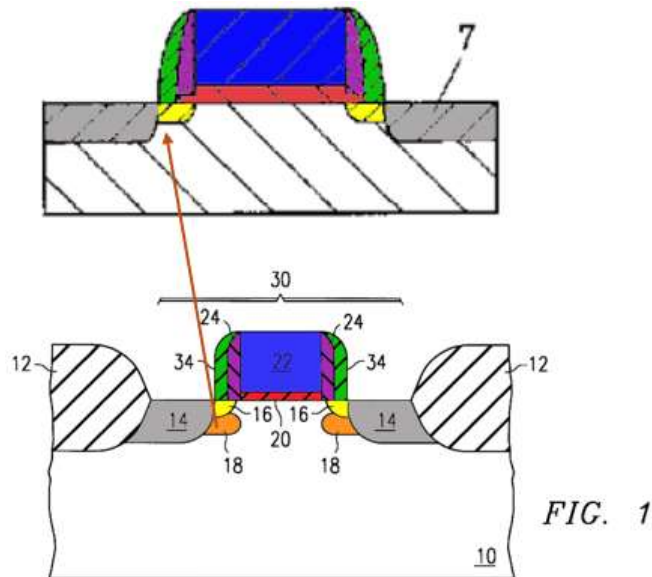
region of a first conductivity type is formed in each of parts of the active region located under the first insulating sidewall and the second insulating sidewall” [8A] and “each of source/drain regions of a first conductivity type is formed in part of the active region ...” [9].



Kajiyama, Fig. 1(D)

272. Kajiyama, however, does not explicitly disclose the use of “*pocket regions*”, a feature admitted by the ’764 patent to have been known in the prior art. (TSMC-1001, 1:45-51, Figures 16A-16B.) Rodder does. As I noted above, Rodder relates to semiconductor devices (TSMC-1023, Abstract), so it is in the same field as Kajiyama and the ’764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1011, ¶1 (“The present invention relates to semiconductor devices.”).) For example, Rodder discloses “*pocket regions*” having “opposite conductivity to” the conductivity of the extensions. (TSMC-1023, 4:35-36.) A

POSITA would have been motivated to combine Rodder's teachings regarding the placement of pocket regions below the extension region and external to the source/drain regions in Kajiyama's first embodiment device, as illustrated below. Such a combination would have included *a pocket region of a second conductivity type is formed in part of the active region located under the extension region* [8B], thereby satisfying the remainder of claims 8-9.



Kajiyama, Fig. 1(D) (top); Rodder, Fig. 1 (bottom) (annotated)

273. **Motivation to Combine.** A POSITA would have been motivated combined Kajiyama and Rodder, resulting in a device where pocket regions of an opposite conductivity to the extensions and source/drain regions are formed under the extensions such that the source/drain regions are external to the pocket regions, as explicitly taught by Rodder. As explained above with regard to Ground 6, a POSITA would have been motivated to combine the references in this manner

bination to obtain the benefits of pocket regions described by Rodder, including “reduc[ing] the threshold voltage (V_t) rolloff, reduc[ing] the nominal V_t , and thus improv[ing] the nominal drive current.” (TSMC-1023, 1:22-25; *see also* TSMC-1038, 463-64 (describing pocket implants which “reduce short-channel effects by shielding the channel from the deep source/drain diffusion”).)

274. Such a combination would have been also nothing more than the use of a known technique (Rodder’s formation of pocket regions below extension regions and outside of source/drain regions) to improve similar devices (Kajiyama’s transistor including extensions regions and source/drain regions) in the same way (ion implantation). A POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable, because both Kajiyama and Rodder use known ion implantation processes for forming doped regions in the semiconductor substrate. (TSMC-1011, ¶¶29, 32; TSMC-1023, 4:21-62; TSMC-1038, 463-64 (describing techniques for forming pocket implants).)

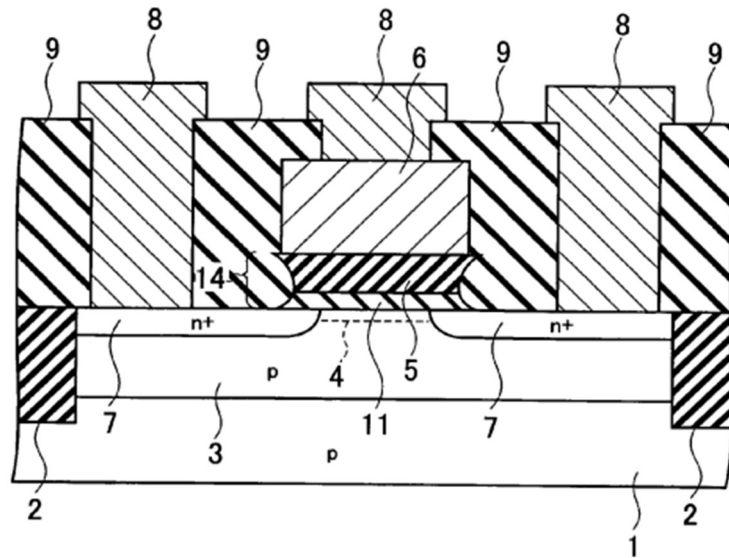
XV. GROUND 14: Kajiyama in View of Ono Renders Claims 10, 12, and 13 Obvious.

A. Dependent Claim 10

<p>[10] <i>The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.</i></p>

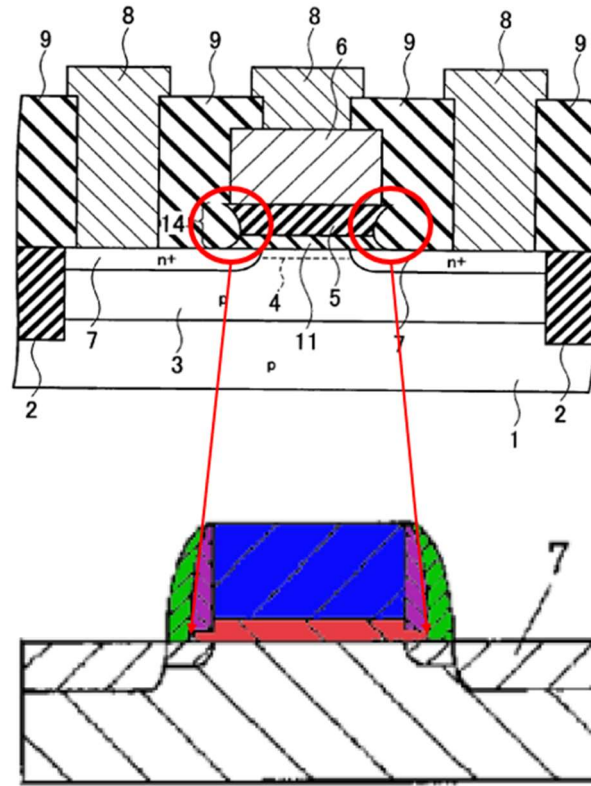
275. The combination of Kajiyama and Ono discloses this limitation. As I noted above, Ono relates to semiconductor devices (TSMC-1013, ¶¶3-7), so it is in the same field as Kajiyama and the '764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1011, ¶1 (“The present invention relates to semiconductor devices.”).)

276. As explained above with regard to the combination of Matsumoto and Ono, Ono discloses that the gate insulating film can be modified to have different lengths (such as overhanging the gate electrode), and that “the sidewalls of the gate insulator film may curve .” (TSMC-1013, ¶¶215-216.) This is shown, for example, in Figure 108 of Ono, below.



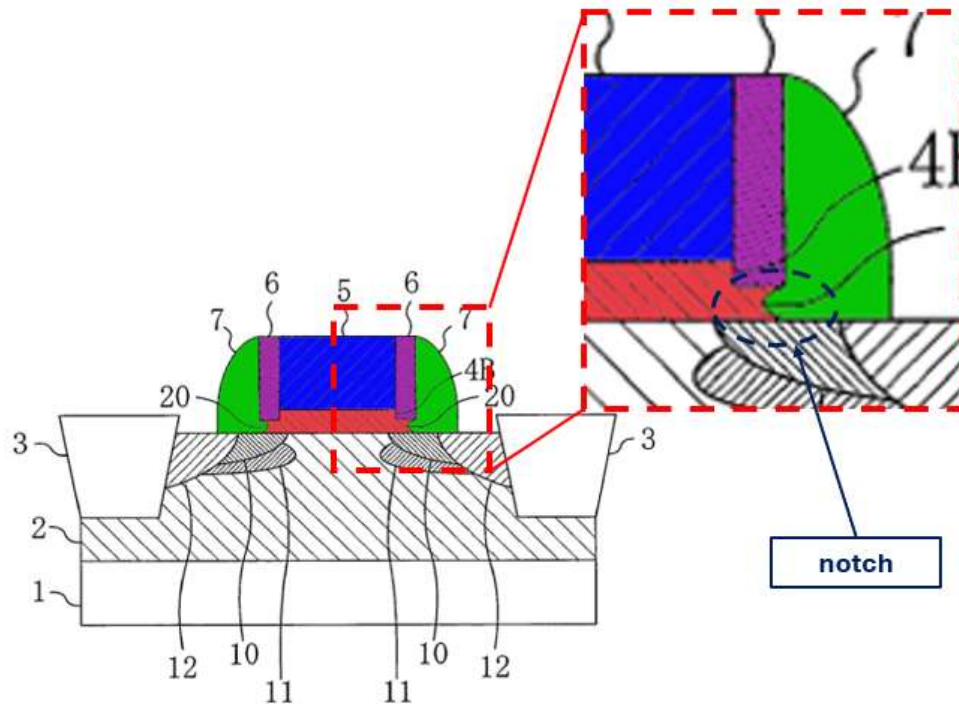
Ono, Fig. 108

277. A POSITA would have been motivated to apply Ono's teaching of curving the end portion of a gate insulating film (circled in Figure 108 below) to Kajiyama's high-k dielectric (shaded red in Figure 1(D) below).



Ono, Fig. 108 (top); Kajiyama, Fig. 1(D) (bottom) (annotated)

278. When Ono and Kajiyama are combined in this manner, the end portion of Kajiyama's gate insulating film has a semicircular shape, as taught by Ono in, e.g., Figure 108. The resulting device includes "*high dielectric constant gate insulating film includes a notch at a side end portion,*" consistent with the disclosure of the '764 patent, and as claimed by claim 10. (See, e.g., TSMC-1001, 8: 35-40 (referring to notch 20 of Figure 7), Figure 7 (below, depicting notch 20 having a semicircular shape).)



'764 Patent, Figure 7 with enlargement

279. **Motivation to Combine.** A POSITA would have been motivated to combine Kajiyama and Ono in this manner. As discussed above with regard to the combination of Matsumoto and Ono, Ono expressly suggests the combination, as discussed above with regard to the combination of Ono and Matsumoto. (TSMC-1013, ¶¶200, 215-216.) Based on Ono's teaching that "the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted," resulting in "an advantage of optimization" with its curved side surfaces, a POSITA would have been motivated to apply that teaching to improve performance of Kajiyama's first embodiment device, further optimizing the electrical capacitance between the gate electrode and the source/drain regions. This

is especially true because it was understood, as recognized by Ono, that by extending the gate insulating film past the gate electrode (as is the case with Kajiyama), “the capacitive coupling between the source/drain regions 7 and the gate electrode 6 is strengthened, therefore advantages of reducing the resistance of the source/drain regions 7, controlling the parasitic capacitance as well as allowing high-speed operations are obtained.” (TSMC-1013, ¶¶200, 215-216).

280. Applying Ono’s teachings to Kajiyama would have been nothing more than the use of a known technique (Ono’s use of curved sidewalls for a gate insulating film) to improve similar devices (Kajiyama’s device using a high-k gate insulating film) in the same way (modifying the dielectric layer to control capacitance). For example, Kajiyama and Ono both use conventional techniques to form high-k gate insulating films that extend under the gate electrode and the insulating sidewall. (TSMC-1011, ¶29; TSMC-1013, ¶167.) Because the processes used are well understood, applying the teachings of Ono to Kajiyama would have been within the skills of a POSITA. A POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable.

B. Dependent Claims 12-13

[12] *The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode.*

[13] *The semiconductor device of claim 1, wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall.*

281. In the combination of Kajiyama and Ono, a notch is formed at each side end of Kajiyama's gate insulating film 2 located under the first sidewall 5, as discussed above with regard to claim 10. In this arrangement, the end of the gate insulating film no longer extends completely under the first insulating sidewall, but rather contains a portion that curves inward from the side end surface of the first insulating sidewall towards the gate electrode. Further, as discussed in Ground 5 above with respect to claims 12-13, the notch's semicircular shape and the distance which the semicircular shape extends inward toward the gate electrode are set by specific process parameters and, thus, are fixed or predetermined. Accordingly, in the combination of Kajiyama and Ono, the gate insulating film's side surface is "*located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode*" [12] and "*located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall*" [13], consistent with the disclosure of the '764 patent. (TSMC-1001, 21:26-30

(“side surface ... may be located at a predetermined distance from a side end surface of the sidewall 7 or the offset sidewall 6 toward the gate electrode 5”).)

V. GROUND 15: Kajiyama in View of Bu Renders Claims 14-15 Obvious.

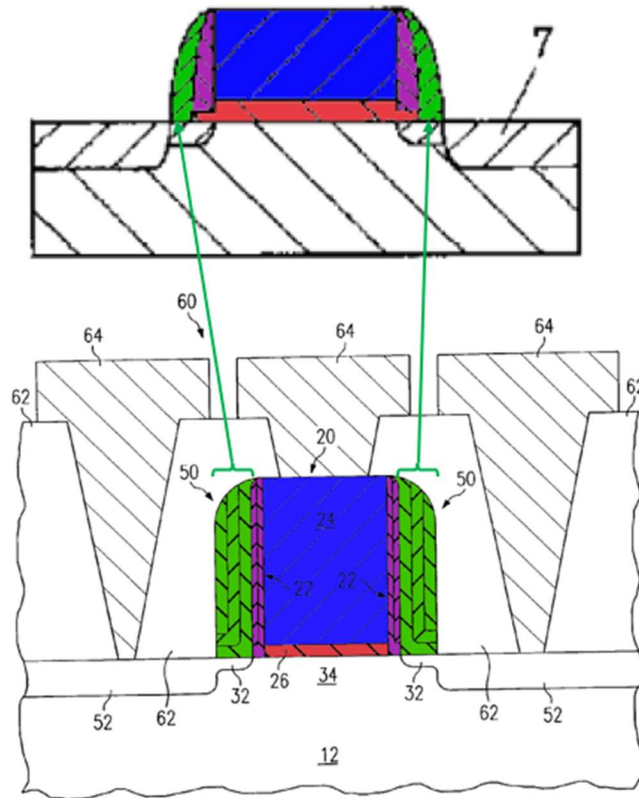
282. Claim 14 depends from claim 1 and recites “*The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film*” [14]. Claim 15 depends from claim 1, and recites “*The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*” [15]. In my opinion, the combination of Kajiyama and Bu render these limitations obvious.

283. As described above with regard to ground 7, Bu teaches an outer sidewall structure having three layers: namely, a first sidewall-forming layer 40 comprising an oxide, a second sidewall-forming layer 42 comprising a nitride, and a third sidewall-forming layer 44 comprising an oxide. (TSMC-1025, ¶¶26-27, 30, 35, 42-43.) As I noted above, Bu relates to semiconductor devices (TSMC-1025, Abstract), so it is in the same field as Kajiyama and the ’764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1011, ¶1 (“The present invention relates to semiconductor devices.”).)

A. Dependent Claim 15

[15] *The semiconductor device of claim 1, wherein the second insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film.*

284. In Kajiyama's first embodiment, the second sidewall 6 is a silicon nitride film ("*a nitride film*"). (TSMC-1011, ¶28.) In my opinion, a POSITA would have known to use Bu's triple-layer ONO sidewall structure with Kajiyama's first embodiment device by forming Kajiyama's second sidewall 6 (shaded green in Figure 1(D) below) with two additional silicon oxide layers to create a triple-layer ONO sidewall structure (shaded green in Figure 1E below) as taught and shown in Figure 1E of Bu. The resulting device would include a "*second insulating sidewall ha[ving] a triple layer structure including a first oxide film, a nitride film and a second oxide film*" [15].



Kajiyama, Fig. 1(D) (top); Bu, Fig. 1E (bottom) (annotated)

285. **Motivation to combine.** A POSITA would have been motivated to apply Bu's teaching of a triple-layer ONO sidewall structure to Kajiyama's semiconductor device in light of the known benefits of sidewalls with ONO structures such as preventing stress-induced degradation at oxide-nitride interfaces, mitigating dopant clustering in source/drain extensions, and allowing independent control of spacer dimensions to optimize device scaling. (See TSMC-1050, ¶¶5-6, 36-43, Figure 4.). Bu itself notes some of the benefits of using different materials in the sidewall structure: "film properties of sidewall-forming layers 40 and 42 may minimize dopant loss from source drain extension region 32 to first sidewall-

forming layer 40. Accordingly, parasitic resistance may be lowered.” (TSMC-1025, ¶26.) A POSITA would have been motivated to make the combination to obtain these benefits and improve device performance and reliability.

286. Combining Bu and Kajiyama in this manner would have been nothing more than the use of a known technique (Bu’s triple-layer outer sidewall) to improve similar devices (Kajiyama’s transistor having a first and second sidewall) in the same manner (depositing a layer of materials before etching). A POSITA would have had a reasonable expectation of success in the combination, and the results would have been predictable, because both Kajiyama and Bu disclose forming sidewall layers using standard deposition and etching techniques, making the application of Bu’s triple layer structure to Kajiyama’s design straightforward. (See TSMC-1011, ¶¶30-31, Figure 29; TSMC-1025, ¶¶27, 30, 35, 38.)

B. Dependent Claim 14

[14] <i>The semiconductor device of claim 1, wherein the second insulating sidewall has a double layer structure including an oxide film and a nitride film.</i>
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287. A POSITA reading Bu would have understood that forming the second sidewall with multiple layers was advantageous and provided many known benefits discussed above. That said, a POSITA applying Bu to Kajiyama also would have understood that three layers, as taught by Bu’s exemplary embodiment, was not strictly required. Rather, the number of layers could be varied based on the

desired characteristics of the device. For example, Bu states that “it is generally recognized that the film properties associated with third sidewall-forming layer may be less critical to transistor performance than the film properties associated with first and second sidewall-forming layers 40 and 42.” (TSMC-1025, ¶36.)

288. Thus, in addition to forming a second sidewall with three layers, a POSITA would have also recognized that the second sidewall could be formed with a two layers including an oxide film and a nitride film (for example, as taught by Matsumoto’s Figure 22 embodiment). Such an arrangement would have resulted in a device where “*the second insulating sidewall has a double layer structure including an oxide film and a nitride film*” [14].

289. A POSITA would have known to apply Bu’s teachings to form Kajiyama’s second sidewall 6 (formed of nitride) with a single additional silicon oxide layer to create a double-layer sidewall structure. A POSITA would have been motivated to apply Bu in this way to obtain the benefits of Bu’s multi-layer sidewall (e.g., minimize dopant loss and lower parasitic resistance (TSMC-1025, ¶26)). Depending on the device and desired characteristics, a POSITA would have known that it was possible to use fewer than three (i.e., two) layers to achieve similar benefits taught by Bu, and if two layers were found to be sufficient, would have been motivated to forego an extra layer, for example, to save on material costs, reduce complexity, or avoid subjecting the device to additional thermal load

(see, e.g., TSMC-1025, ¶29). In light of these considerations, a POSITA would also have been motivated to implement Bu's teachings into Kajiyama's device to form a double-layer sidewall structure.

290. For the same reasons discussed above with regard to a triple-layer sidewall, the combination of Kajiyama and Bu to include a double-layer sidewall structure is nothing more than the use of a known technique to improve similar devices in the same way. A POSITA would have had a reasonable expectation of success in the combination, and the results would have been predictable.

VI. GROUND 16: Kajiyama in View of Wilk Renders Claims 18-19 Obvious.

[18] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.*

[19] *The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall.*

291. As explained above, it is my opinion that Kajiyama already discloses this limitation because the dielectric constants of materials disclosed by Kajiyama for both the gate insulating film and the second insulating sidewall are inherent to those materials. Even if it were not found to be the case, then Kajiyama in light of the knowledge of a POSITA, at a minimum, renders the limitations of claims 18-19 obvious. If this were also not found to be the case, and an explicit disclosure of

dielectric constants were deemed necessary, then Wilk provides such a disclosure.

The combination of Kajiyama and Wilk thus renders claims 18-19 obvious too.

292. As I noted above, Wilk relates to semiconductor devices (TSMC-1018, Abstract), so it is in the same field as Kajiyama and the '764 patent. (TSMC-1001, 1:15-16 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1011, ¶1 (“The present invention relates to semiconductor devices.”).) As noted in Ground 8, Table I of Wilk provides a “Comparison of relevant properties for high-k candidates,” including dielectric constants for those materials:

TABLE I. Comparison of relevant properties for high- κ candidates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO ₂	3.9	8.9	3.2	Amorphous
Si ₃ N ₄	7	5.1	2	Amorphous
Al ₂ O ₃	9	8.7	2.8 ^a	Amorphous
Y ₂ O ₃	15	5.6	2.3 ^a	Cubic
La ₂ O ₃	30	4.3	2.3 ^a	Hexagonal, cubic
Ta ₂ O ₅	26	4.5	1–1.5	Orthorhombic
TiO ₂	80	3.5	1.2	Tetrag. ^c (rutile, anatase)
HfO ₂	25	5.7	1.5 ^a	Mono. ^b , tetrag. ^c , cubic
ZrO ₂	25	7.8	1.4 ^a	Mono. ^b , tetrag. ^c , cubic

^aCalculated by Robertson (See Ref. 153).

^bMono.=monoclinic.

^cTetrag.=tetragonal.

Wilk, Table I

293. A POSITA wanting to understand the dielectric constants for high-k materials disclosed by Kajiyama would have been motivated to look to any number

of references that listed those values. Wilk is one such reference, and is specifically directed to high-k materials for gate dielectric applications. Wilk lists relevant properties of materials discussed in Kajiyama, allowing a POSITA to, for example, ensure that the gate insulating film had a optimally high dielectric constant.

294. Kajiyama teaches that, in addition to ZrO_2 , “other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention.” (TSMC-1011, ¶45.) Wilk’s Table I discloses, for example, that ZrO_2 has a dielectric constant of 25, HfO_2 has a dielectric constant of 25, and Ta_2O_5 has a dielectric constant of 26. (TSMC-1018, Table I.) All of these values are greater than 10, as required by claim 18.

295. Kajiyama discloses that the second sidewall 6 is comprised of silicon nitride (Si_3N_4). (TSMC-1011, ¶28). Table I of Wilk discloses Si_3N_4 has a dielectric constant of 7. (TSMC-1018, Table I.). The dielectric constants of ZrO_2 , HfO_2 , and Ta_2O_5 are also greater than 7, as required by claim 19.

296. Thus, in the devices resulting from the combination of Kajiyama and Wilk, “*the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more*” [18] and “*the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the second insulating sidewall*” [19].

XVI. Conclusion

297. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 15th day of April, 2025, in Austin, Texas.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Jack Lee", followed by a period.

Jack Lee, Ph.D.