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Effects of ALD HfO_2 thickness on charge trapping and mobility

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Abstract

The effects of HfO_2 thickness on charge trapping and mobility were investigated. The impact of fast transient electron trapping on DC measurements results in underestimating channel carrier mobility. Scaling the physical thickness of the HfO_2 dielectric causes less charge trapping and higher mobility. A HfO_2-based high-k solution requires fine-tuning the thickness of the high-k film to maintain a balance between electron trapping in thicker films and increased leakage current in thinner films.

Keywords: charge trapping; mobility; high-k

1. Introduction

Hafnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology [1-2], but several drawbacks such as low mobility and charge trapping have been identified [3-7]. Even though several process modifications such as nitridation and silicate formation have been proposed to overcome the limitations of high-k dielectrics, the effect of these changes has not been investigated systematically [8-11]. Recently, the reduction of transient charge trapping was proposed as a way to improve the quality of high-k dielectrics [3]. Transient charging, which is generally not observed in SiO_2, complicates the evaluation of the properties of high-k gate stacks because the mobility of the high-k device is usually underestimated when DC I_d-V_g curves are used for mobility extractions. To overcome the limitations of this conventional methodology, a pulsed I_d-V_g method has been proposed to extract close to intrinsic channel mobility of high-k gate transistors [6-7, 12-14]. Using this new understanding and new methodologies, we have systematically evaluated the effects of high-k film thickness on charge trapping and channel carrier mobility and demonstrated that scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics.

2. Experimental

To investigate the effects of high-k thickness, transistor gate stacks were fabricated with 20–40Å thick atomic layer deposition (ALD) HfO_2 films. The gate electrode was 10nm ALD TiN with a 150nm polysilicon capping layer. Equivalent oxide thickness

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(EOT) and mobility values were extracted from the capacitance-voltage (C-V) and current-voltage (I-V) data using the North Caroline State University (NCSU) model. For mobility extraction, both DC and pulsed I_d-V_g data were used [12]. Pulse rise/fall and width times were varied to evaluate the effects of charge trapping on channel mobility. For the charge trapping study, threshold voltage shifts and drain current changes were estimated from the pulsed I_d-V_g measurements. I-V characteristics were measured on 10×1μm (WxL) field-effect transistors (FETs). The physical thickness of the HfO_2 and interfacial sub-oxide layer were verified by transmission electron microscopy (TEM) measurements.

3. Results and Discussion

Raw C-V data show capacitance scaling with physical thicknesses of 18Å, 25Å, and 33Å as estimated by TEM measurements (Fig. 1), which correlate well with the extracted EOT values of 9.5Å, 10.6Å, and 11.8Å, respectively (Fig. 2).

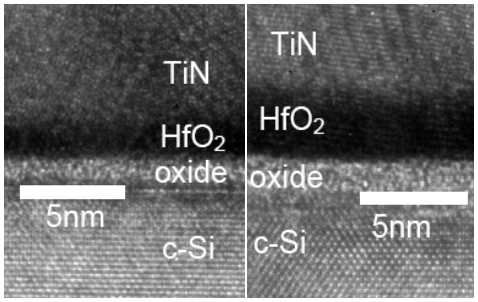

Figure. 1: TEM images of the HfO_2 gate stacks of 18Å and 33Å physical thickness.

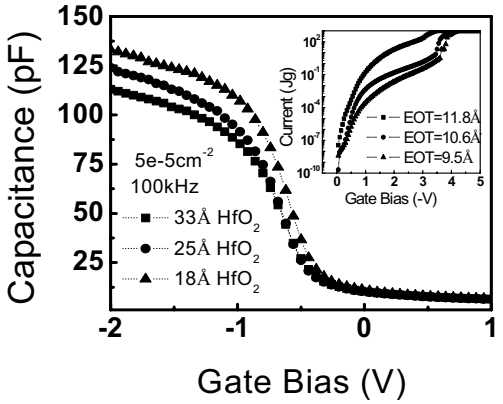

Figure. 2: C-V and gate leakage current (inserted) data for the studied dielectric films.

In all stacks, the effective k value of the nitride high-k film is about 24. The EOT of the interfacial layer is estimated as ~ 6.5Å due to the greater k value of the interfacial oxide layer [13]. Gate leakage current also scales with the physical thickness of HfO_2 (inset of Fig. 2). The gate leakage current values measured in this study roughly match historical data in the literature and our own work, indicating these samples are very close to typical HfO_2 dielectrics (Fig. 3).

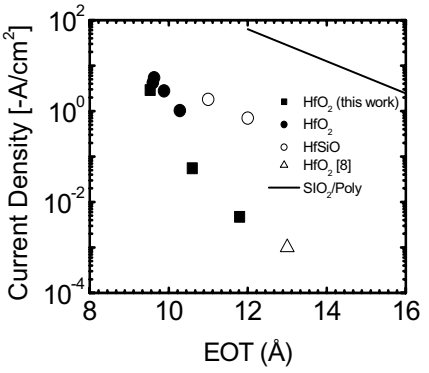

Figure. 3: Current density vs. EOT data for the HfO_2 gate stacks studied in this work and published data at V_{fb}-1V.

To examine fast charge trapping effects, the time dependence of the drain current induced by the 1.4V, 100μs width pulse (applied to the drain current and to NMOS with various HfO_2 thicknesses) was monitored (Fig. 4). In this plot, the reduction in time-dependent drain current is primarily due to the charge trapping-induced V_{th} shift. Even within 100μs, a 33Å HfO_2 sample shows significant current reduction while a 18Å HfO_2 sample is free from transient charging within the detection limits.

Effective mobility values extracted from DC and pulsed I_d-V_g measurements are plotted in Fig. 5. DC mobility decreases as the HfO_2 becomes thicker. This result can be interpreted using different models. For example, a fixed charge theory attributes this result to increased bulk charge with thicker HfO_2 samples. A phonon scattering theory attributes it to a greater contribution from phonon scattering. However, neither model can explain the dependence of the reduced drain current on time, which is the signature of a dynamic charging process. The

dynamic analysis of I_d (V_g) hysteresis was proposed in high-k dielectric devices [15].

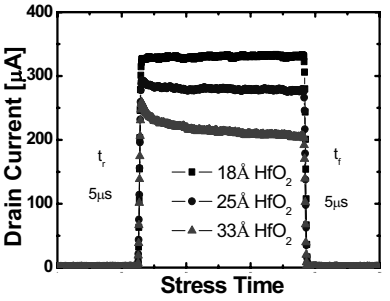

Figure. 4: Variation of the drain current during the pulsed I_d-V_g measurements (pulse width [PW]= 100μs).

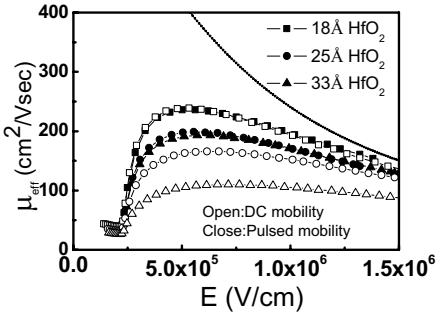

Figure. 5: Mobility vs. effective electrical field dependencies for different HfO_2 film thicknesses extracted from DC and pulsed I_d-V_g measurement.

HfO_2 thickness	18Å	25Å	33Å
EOT(Å)	9.5	10.6	11.8
Jg (A/cm^2) (at V_{fb}-1V)	2.88	5.5 e-2	4.7 e-4
DC/Pulse mobility (1MV/cm)	194/ 197	153/ 171	105/ 170
Peak Nit (x10^{10}cm^{-2})	2.9	2	2

Table 1: Electrical characteristics of the studied high-k stacks.

Mobility values extracted from the pulsed I_d-V_g dependencies are much higher than the DC mobility for 25Å and 33Å HfO_2 samples; for the 18Å sample, the difference between DC mobility and pulsed mobility is minimal. Also, the mobility value of the 18Å sample is very close to universal mobility [14]. Table. 1 summarizes the electrical characteristics of the studied gate stack. It is interesting to note that the mobility values for the pulse (which is free from the effect of charge trapping) are higher for thinner dielectric films. Since the interface state density is similar in all high-k samples (Table. 1), the interface quality of these HfO_2 stacks is not the main reason for the higher mobility of the 18Å sample.

The transient charging model can explain these results in a systematic way. Fast electron trapping can effectively increase the magnitude of the threshold voltage during the DC measurements of the drain current, resulting in overestimation of the inversion charge and, subsequently, underestimation of intrinsic channel carrier mobility [4].

The dependence of drain current on pulse magnitude shows less charge trapping when the applied gate voltage and HfO_2 thickness decrease (Fig. 6). The thinnest HfO_2 film does not exhibit a reduction in drain current at any of the applied voltages, indicating no appreciable charge trapping exists in the microsecond pulse time range.

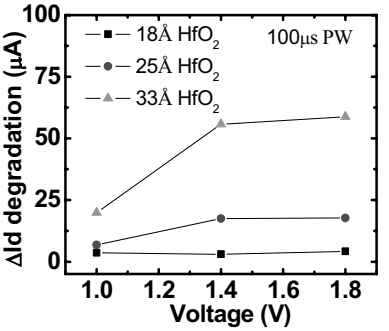

Figure. 6: Drain current reduction vs. amplitude of the 100μs pulse.

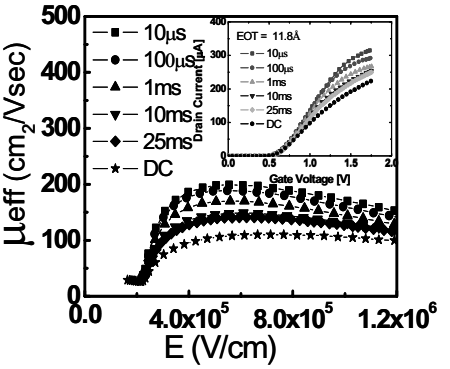

Figure. 7: Channel mobility of the 33Å gate stack extracted from the pulsed I-V data of different pulse rise time.

The charge trapping effect also depends on charging time. As can be seen in the insert in Fig. 7, I_{dlin} (at V_g=1.8V V_d=0.05V) is a function of pulse rise time indicating that charge trapping occurs on a time scale of less than 10μs. Channel mobility of the 33Å gate stack follows the pulsed I-V data of different pulse rise time.

The ratio of the pulsed I_d-V_g and DC drain currents in the linear regime shows a significant gain with thicker HfO_2 (Fig. 8). On the other hand, the gain in the18Å HfO_2 sample is less than 1%, pointing to a similar charge trapping effect caused by the fast pulse and DC I_d-V_g measurements. The 18Å HfO_2 stack demonstrated less V_{th} shift under DC constant voltage stress than did thicker films (Fig. 9). Since the electric field in the thin film during the stress was higher than in thicker films by 2MV/cm, one may conclude that thinner films demonstrate better device stability with respect to charge trapping.

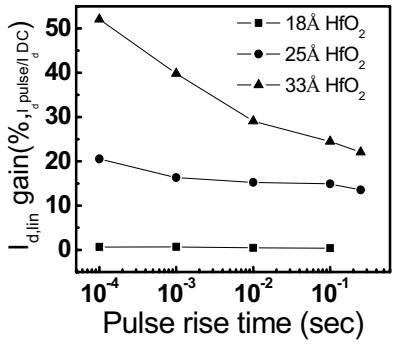

Figure. 8: Ratio of the pulse and DC drain currents in the linear regime vs. pulse width time.

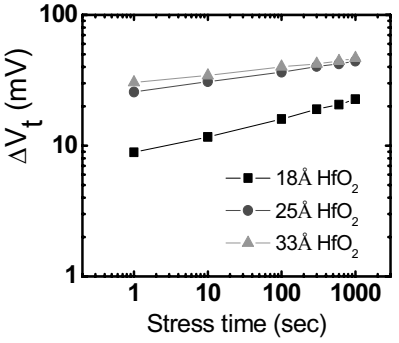

Figure. 9: Under the same constant voltage stress condition (Vg=1.8V), 18Å HfO_2 device show less threshold voltage shift.

The threshold voltage shift in thin film devices during constant voltage stress (CVS) indicates that charge traps still exist in thinner films although their effect on V_{th} shift is much less. Therefore, the HfO_2-based high-k solution requires fine-tuning the thickness of the high-k film to maintain a balance between electron trapping in thicker films and increased leakage current in thinner films. Plasma treatments, surface nitridation, and other processing techniques can be used to further reduce charge trapping in thin high-k dielectric gate stacks to improve device stability.

4. Summary

The effects of HfO_2 thickness on charge trapping and mobility were investigated. The impact of fast transient electron trapping on DC measurements results in underestimating channel carrier mobility. Scaling the physical thickness of the HfO_2 dielectric to below 20Å causes less charge trapping and higher mobility.

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