IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

ADVANCED INTEGRATED CIRCUIT PROCESS LLC, **Plaintiff,** **v.** **UNITED MICROELECTRONICS CORPORATION,** **Defendant.**	Case No.: 2:24-cv-00730-JRG (Lead Case)
ADVANCED INTEGRATED CIRCUIT PROCESS LLC, **Plaintiff,** **v.** **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LIMITED,** **Defendant.**	Civil Action No.: 2:24-cv-623 (Member Case)

DEFENDANT TSMC'S
INVALIDITY CONTENTIONS

Pursuant to Local Patent Rules ("P.R.") 3-3, and 3-4 Defendant Taiwan Semiconductor Manufacturing Company Limited ("TSMC" or "Defendant") hereby serves its Invalidity Contentions and accompanying document production on Plaintiff Advanced Integrated Circuit Process LLC ("AICP" or "Plaintiff"). TSMC contends that each of the claims asserted by AICP is invalid under at least 35 U.S.C. §§ 102, 103, and/or 112.

I. GENERAL STATEMENT AND RESERVATION OF RIGHTS

A. General Reservation of Rights

These Contentions, along with the information and documents that TSMC produces herewith, are based on information currently available to TSMC and subject to further revision. Consistent with the Patent Rules, TSMC reserves the right to amend these Contentions should AICP: (1) provide any information that it failed to provide in its P.R. 3-1 and 3-2 disclosures or otherwise properly produce; (2) amend its P.R. 3-1 and 3-2 disclosures in any way; or (3) attempt to rely upon any information during claim construction proceedings, at trial, in a hearing, or during a deposition that it failed to provide in its P.R. 3-1 and 3-2 disclosures or otherwise properly produce. TSMC further reserves the right to amend these Contentions based on claim construction positions taken by AICP and/or construction of claim terms adopted by the Court. Moreover, TSMC further reserves the right to amend these contentions based on further discovery or Court rulings (or any other related reason). This includes, for instance, the issuance of subpoenas to third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed below and/or additional prior art. These third parties may include, without limitation, any relevant authors, inventors, developers, designers, corporate designees with knowledge, or assignees. TSMC provides these Contentions, as well as the accompanying production of documents, for the sole purpose of complying with P.R. 3-3 and 3-4 and the Standing Order.

B. Asserted Claims

In this case, and based on AICP's P.R. 3-1 Infringement Contentions, served on January 7, 2025 and February 5, 2025, AICP has asserted that TSMC infringes the following claims ("Asserted Claims") of U.S. Patent Nos. 7,579,227 (the "'227 Patent"), 7,923,764 (the "'764 Patent"), 8,198,686 (the "'686 Patent"), 8,253,180 (the "'180 Patent"), 8,587,076 (the "'076 Patent"), 8,796,779 (the "'779 Patent"), and 8,907,425 (the "'425 Patent") (collectively, the "Patents-In-Suit" or "Asserted Patents").

- '227 patent: claims 1, 2, 7, 8, and 14
- '764 patent: claims 1, 2, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, and 19
- '686 patent: claims 25, 26, 27, 28, 29, 31, 34, and 35
- '180 patent: claims 1, 2, 3, 5, 6, 11, 13, 14, 16, 17, 18, 19, 21, and 22
- '076 patent: claims 1, 2, 3, 6, 7, 8, 10, 11, 12, and 13
- '779 patent: claims 1, 12, 13, 14, and 15
- '425 patent: claims 1, 3, 4, 5, 7, and 11

TSMC's Invalidity Contentions address only those claims asserted in AICP's Infringement Contentions, and claims upon which these claims depend. To the extent that the Court or the Patent Rules permit AICP to assert additional claims against TSMC, TSMC reserves the right to disclose new or supplemental contentions regarding such claims.

C. AICP's P.R. 3-1 and 3-2 Disclosures

TSMC provides these Contentions consistent with the schedule set forth in the Court's April 9, 2025 Order (ECF No. 83) but do so without waiving any right to receive from AICP full, complete and detailed infringement disclosures as required under P.R. 3-1 and 3-2. TSMC's compliance with the schedule currently in place should not be viewed as a waiver of its right to seek relief regarding the deficiencies in AICP's disclosures.

AICP's Infringement Contentions are deficient in numerous respects. AICP's Infringement Contentions lack the specificity required under P.R. 3-1 as would be necessary to fairly provide TSMC notice of AICP's theories, including without limitation: (1) AICP fails to provide claim charts for each Accused Product—AICP accuses 141 products but provides only 8 claim charts—or support, with specificity and supporting documentary or declaratory evidence, its assertions that there are no material differences between the Accused Instrumentalities that affect its infringement theories for the uncharted products; and (2) AICP fails to identify where each element of each asserted claim is found within each Accused Instrumentality. In particular, AICP accuses 23 different FinFET node processes from 3nm to 16nm using one claim chart of a 5nm node product even though each node process forms products differently.

TSMC further specifically reserves the right to modify, amend, or supplement its Contentions should AICP be permitted to further modify, amend, or supplement its P.R. 3-1 and 3-2 disclosures or produce documents responsive to TSMC's discovery requests.

D. Priority Applications / Priority Date of Asserted Claims

TSMC's Contentions, including but not limited to identification of prior art, rely in part on AICP's contention that the Patents-in-Suit are entitled to claim priority to the following applications:

- '227 patent: Japanese Patent Application No. 2005-227457, filed August 5, 2005
- '764 patent: Japanese Patent Application No. 2005-227457, filed August 5, 2005
- '686 patent: Japanese Patent Application No. 2008-064435, filed March 13, 2008
- '180 patent: Japanese Patent Application No. 2005-227457, filed August 5, 2005
- '076 patent: Japanese Patent Application No. 2005-227457, filed August 5, 2005
- '779 patent: Japanese Patent Application No. 2010-205599, filed September 14, 2010
- '425 patent: Japanese Patent Application No. 2010-002225, filed January 7, 2010

TSMC reserves the right to challenge any of the above alleged priority claims and reserves the right to amend these Contentions to the extent that AICP is permitted to claim priority to an earlier application, assert an earlier conception or reduction to practice date than the priority application filing date, changes its alleged priority dates, or if the Court determines that any of the Patents-in-Suit are not entitled to claim priority to the earlier applications as asserted by AICP.

E. Claim Construction

Claim construction proceedings for this action have not yet occurred. Accordingly, TSMC reserves the right to modify, amend, and/or supplement its Contentions in accordance with P.R. 3-6 following claim construction rulings from this Court, or to the extent permitted by this Court. TSMC also reserves the right to modify, amend, and/or supplement its Contentions upon AICP's alteration/clarification of any asserted claim constructions, including as adopted by AICP in its Infringement Contentions or any amendment thereto.

TSMC's Contentions are based in part on its present understanding of AICP's Infringement Contentions. In some instances, AICP's Infringement Contentions contradict the teachings of the Patents-In-Suit, contradict the meaning of the claim terms as would have been understood by a person of ordinary skill in the art, are internally inconsistent, and/or are vague and conclusory concerning how the claim limitations supposedly read on the Accused Instrumentalities or activities. As a result, TSMC is currently unable to fully discern AICP's position regarding the construction of the patent claim limitations or terms. To the extent that AICP supplements or amends its Infringement Contentions, TSMC reserves the right to modify, amend, and/or supplement these Contentions.

TSMC's Contentions do not represent its agreement or view as to the meaning of any claim term contained therein. To the extent that TSMC asserts that prior art is anticipatory or renders obvious claims based on the construction apparently applied by AICP to the Asserted Claims,

TSMC's Contentions are not—and should not be interpreted as—adoptions or admissions as to the accuracy of that scope or construction.

Nothing in TSMC's Contentions should be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Nor should anything contained herein be understood or deemed to be an express or implied admission or contention with respect to the proper construction of any terms in any asserted claim, or with respect to the alleged infringement of that claim.

Unless otherwise stated herein, TSMC takes no position on any matter of claim construction in these Contentions. TSMC reserves the right to propose any claim construction it considers appropriate and to contest any claim construction it considers inappropriate. TSMC also reserves the right to argue that certain claim terms, phrases, and elements are indefinite, lack written description, are not enabled and/or are otherwise invalid under 35 U.S.C. § 112.

Because of the uncertainty of claim construction, TSMC reserves the right to further supplement or modify the positions and information in these Contentions, including, without limitation, the prior art and grounds of invalidity set forth herein, after the Asserted Claims have been construed, in accordance with the Patent Rules and the Court's Orders.

F. Ongoing Discovery and Disclosures

Discovery in this case and TSMC's investigation, including TSMC's search for prior art, are ongoing. Some of the relevant prior art and other information is in the possession of third parties, and TSMC is in the process of seeking discovery related to such prior art. For example, TSMC intends to subpoena or otherwise seek discovery from third parties regarding at least the following prior art systems, including Intel Penryn 45nm processors, Intel Presler 65nm processors, Intel Xeon E5410 processors, Intel QX9650 processors, Intel Pentium D 920 processors, and Altera Stratix IV FPGAs, in addition to other systems that may be related to the

Patents-In-Suit and printed publication references disclosed in these Contentions. TSMC expressly reserves the right to amend or modify these Contentions based on additional information obtained through continued formal discovery or other means pursuant to Fed. R. Civ. P. 26(e).

TSMC further reserves the right to revise, amend, or supplement these Contentions, including by identifying, charting, and relying on additional information, references, systems, and devices, should TSMC's further search and analysis yield additional information, references, systems, or devices, consistent with the Local Patent Rules and the Federal Rules of Civil Procedure. In addition, TSMC reserves the right to supplement, amend, and/or alter the positions taken and information disclosed in these Contentions including, without limitation, the prior art and grounds of invalidity set forth herein under 35 U.S.C. §§ 102, 103 or 112, to take into account information or defenses that may come to light as a result of TSMC's discovery efforts; additional information obtained as to the priority date(s) of the asserted claims; testimony or documents produced by a party or non-party; and positions that AICP may take concerning infringement or invalidity issues. For example, TSMC may seek further discovery from third parties believed to have knowledge, documentation, or corroborating evidence concerning prior art references, including prior art listed in the Exhibits hereto. Such third parties may include, without limitation, the authors, inventors, assignees, owners, or developers of the references and technologies listed in these disclosures.

TSMC further reserve the right to rely upon prior art cited in the file histories of the Patents-In-Suit and related patent applications, including post-issuance proceedings, as invalidating references or to show the state of the art. TSMC further reserves the right to rely upon additional prior art to show the state of the art. TSMC further intends to rely on inventor admissions, and admissions by AICP and others providing testimony on behalf of AICP (e.g., experts), concerning

the scope of the prior art relevant to the Patents-In-Suit found in, *inter alia*: the patent prosecution history for the Patents-In-Suit and any related patents or patent applications, including post-issuance proceedings; any deposition testimony of the named inventors on the Patents-In-Suit; and the papers filed and any evidence submitted by AICP in connection with this litigation, prior litigations, and other proceedings involving the Patents-in-Suit. For example, IPR2025-00828 covering the Asserted Claims of the ’227 patent, IPR2025-00829 covering the Asserted Claims of the ’764 patent, IPR2025-00682 covering the Asserted Claims of the ’686 patent, IPR2025-00830 covering the Asserted Claims of the ’180 patent, IPR2025-00831 covering the Asserted Claims of the ’076 patent, IPR2025-00832 covering the Asserted Claims of the ’779 patent, and IPR2025-00683 covering the Asserted Claims of the ’425 patent and any other IPRs to be filed against any of the Asserted Claims of the Patents-In-Suit. Those proceedings are part of the file histories of the Patents-in-Suit and AICP should be estopped from taking contrary positions in this Court to positions it takes before the Patent Trial and Appeal Board. TSMC incorporates by reference the relevant testimony of any fact witnesses who are deposed, provide declarations, or otherwise testify in this lawsuit. TSMC also incorporates by reference the reports and testimony of any expert witnesses regarding invalidity of the Patents-In-Suit, either here or at the Patent Trial and Appeal Board.

II. INVALIDITY CONTENTIONS

A. Invalidity Contentions Pursuant to P.R. 3-3(a)

Pursuant to P.R. 3-3(a), and as detailed below and in the attached Exhibits, TSMC contends that the Asserted Claims of the Patents-In-Suit are invalid as anticipated and/or obvious, either expressly or inherently as understood by a person having ordinary skill in the art, under 35 U.S.C. §§ 102 and 103 over at least the following prior art. To the extent that any prior art listed herein is not identified as prior art that anticipates and/or renders obvious an Asserted Claim, TSMC intends

to rely on the reference as background and as evidence of the state of the art at the time of AICP's alleged invention.

In addition to the references identified below, the prior art references systems identified below and the "References Cited" on the face of the Patents-In-Suit may render obvious, alone or in combination with any other reference cited herein, the asserted claim of the Patents-In-Suit; provide background and context pertinent to the teachings and interpretation of the prior art referenced by the claim charts identified below; and may also be indicative of the relevant state of the art and/or the knowledge of one of ordinary skill in the art at the time of inventions of the Patents-In-Suit, such that it demonstrates, for example, the lack of invention between the asserted claim and the prior art as well as teachings, suggestions and motivations to combine. The prior art is exemplary only and is not in any way intended to limit the scope of what one of ordinary skill in the art would have understood at the time of the alleged invention.

Furthermore, along with the references disclosed in these Contentions, the exhibits thereto, the Patents-In-Suit and their prosecution history, and the common sense and understanding of those in the relevant field at the time of the alleged invention, invalidity may be demonstrated by the live testimony of relevant witnesses, who will be identified in accordance with the case schedule and as discovery in this matter proceeds. Such witnesses may be used, among other purposes, to discuss issues of prior art systems, prior art references, and the knowledge of one of ordinary skill in the art at the time of the alleged invention. As noted above, TSMC intends to seek third party discovery regarding certain prior art systems, in addition to other systems that may be related to the Patents-In-Suit and printed publication references disclosed in these Contentions.

TSMC reserves the right to rely upon additional prior art, information, testimony, and/or knowledge to demonstrate what one of ordinary skill in the art would have understood prior to the date of the alleged invention of the asserted claim of the Patents-In-Suit.

1. '227 Patent Prior Art

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
227-01	U.S. Patent Pub. 2003/0025135 ("Matsumoto 135")	Takuji Matsumoto, Hirokazu Sayama, Shigenobu Maeda, Toshiaki Iwamatsu, Kazunobu Ota	July 11, 2002	Feb. 6, 2003
227-02	JP2003-258241 ("JP-Kajiyama")	Masaoki Kajiyama	Mar. 5, 2002	Sept. 12, 2003
227-03	U.S. Patent Pub. 2004/0227185 ("Matsumoto 185")	Takuji Matsumoto, Takashi Ipposhi, Toshiaki Iwamatsu, Yuuichi Hirano	Jan. 12, 2004	Nov. 18, 2004
227-04	U.S. Patent Pub. 2006/0091432 ("Guha")	Supratik Guha, Hussein Hanafi, Rajarao Jammy, Paul Solomon	Nov. 2, 2004	May 4, 2006
227-05	"Investigation of Poly-Si/HfO2 Gate Stacks in a Self-aligned 70nm MOS Process Flow" ("Kubicek")	Stefan Kubicek et al.	N/A	Sept. 2003
227-06	U.S. Patent No. 6,917,072 ("Noguchi")	Mitsuhiro Noguchi, Akira Goda	Mar. 24, 2003	July 12, 2005
227-07	JP2005-064190 ("JP-Ono")	Tamashiro Ono, Akira Nishiyama	Aug. 11, 2003	Mar. 10, 2005
227-08	U.S. Patent No. 6,632,729 ("Paton")	Eric Paton	June 7, 2002	Oct. 14, 2003
227-09	U.S. Patent No. 6,168,958 ("Gardner")	Mark Gardner, H. Jim Fulford, Charles E. May	Aug. 7, 1998	Jan. 2, 2001

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
227-10	U.S. Patent Pub. 2005/0051856 ("Ono")	Mizuki Ono, Takamitsu Ishihara	July 2, 2004	Mar. 10, 2005
227-11	U.S. Patent Pub. 2005/0093084 ("Wang 084")	Chih-Hao Wang, Shang-Chih Chen, Yen-Ping Wang, Hsien-Kuang Chiu, Liang-Gi Yao, Chenming Hu	June 19, 2004	May 5, 2005
227-12	U.S. Patent No. 7,585,735 ("Mathew")	Leo Mathew, Yang Du, Bich-Yen Nguyen, Voon-Yew Thean	Feb. 1, 2005	Sept. 8, 2009
227-13	"Effects of ALD HfO2 Thickness on Charge Trapping and Mobility" to Sim ("Sim")	J.H. Sim et al.	N/A	June 17, 2005
227-13	"High-k Gate Dielectrics: Current Status and Materials Properties Considerations" ("Wilk")	G.D. Wilk et al.	N/A	May 15, 2001
227-13	U.S. Patent 6,504,214 ("Yu")	Bin Yu, Qi Xiang	Jan. 11, 2002	Jan. 7, 2003
227-13	"Impact of Hf Concentration on Performance and Reliability for HfSiON-CMOSFET" ("Watanabe 2004")	Takeshi Watanabe et al.	N/A	Dec. 15, 2004
227-13	"Design Guideline of HfSiON Gate Dielectrics for 65 nm CMOS Generation" ("Watanabe 2003")	Takeshi Watanabe et al.	N/A	June 12, 2003
227-13	"Ultrathin Hafnium Oxide with Low Leakage and Excellent	Byoung Hun Lee et al.	N/A	Dec. 8, 1999

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Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
	Reliability for Alternative Gate Dielectric Application" ("Lee 1999")			
227-13	"High Quality Ultra Thin CVD HfO2 Gate Stack with Poly-Si Gate Electrode" ("Lee 2000")	S.J. Lee	N/A	Dec. 13, 2000
227-13	U.S. Patent Pub. 2005/0280105 ("Andreoni")	Wanda Andreoni, Alessandro Callegari, Eduard Cartier, Alessandro Curioni, Christopher D'Emic, Evengi Gousev, Michael Gribelyuk, Paul Jamison, Rajarao Jammy, Dianne Lacey, Fenton McFeely, Vijay Narayanan, Carlo Pignedoli, Joseph Shepard, Sufi Zafar	June 22, 2004	Dec. 22, 2004
227-13	"Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology" ("Wolf")	Stanley Wolf	N/A	2002
227-13	"High-k Dielectrics" ("Houssa")	Michel Houssa	N/A	2004
227-13	"Silicon VLSI Technology: Fundamentals, Practice and Modeling" ("Plummer")	James D. Plummer	N/A	2000

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
227-13	U.S. Patent Pub. 2005/0045938 ("Mutou")	Akiyoshi Mutou, Hiroshi Ohji	Aug. 26, 2004	Mar. 3, 2005
227-13	U.S. Patent Pub. 2006/0131672 ("Wang 672")	Chih-Hao Wang, Ta-Wei Wang, Shang-Chih Chen, Ching-Wei Tsai	Apr. 27, 2005	June 22, 2006
227-13	U.S. Patent Pub. 2004/0110352 ("Bu")	Haowen Bu, Amitabh Jain, Wayne Bather, Stephanie Butler	Dec. 10, 2002	June 10, 2004
227-13	U.S. Patent No. 6,911,695 ("Ahmed")	Shafqat Ahmed, Henry Chao, DerChang Kau	Sept. 19, 2002	June 28, 2005
227-13	U.S. Patent 6,818,516 ("Lo")	Wai Lo, Hong Lin, Shiqun Gu, James R. B. Elmer	July 29, 2003	Nov. 16, 2004
227-13	U.S. Patent 6,617,209 ("Chau 209")	Robert Chau, Reza Arghavani, Mark Doczy	Feb. 22, 2002	Sept. 9, 2003
227-13	U.S. Patent 6,617,210 ("Chau 210")	Robert Chau, Reza Arghavani	May 31, 2002	Sept. 9, 2003
227-13	U.S. Patent 6,787,440 ("Parker")	Christopher G. Parker, Markus Kuhn, Ying Zhou, Scott A. Hareland, Suman Datta, Nick Lindert, Robert S. Chau, Timothy E. Glassman, Matthew V. Metz, Sunit Tyagi	Dec. 10, 2002	Sept. 7, 2004

2. ’764 Patent Prior Art

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
764-01	U.S. Patent Pub. 2003/0025135 (“Matsumoto 135”)	Takuji Matsumoto, Hirokazu Sayama, Shigenobu Maeda, Toshiaki Iwamatsu, Kazunobu Ota	July 11, 2002	Feb. 6, 2003
764-02	JP2003-258241 (“JP-Kajiyama”)	Masaoki Kajiyama	Mar. 5, 2002	Sept. 12, 2003
764-03	U.S. Patent Pub. 2004/0227185 (“Matsumoto 185”)	Takuji Matsumoto, Takashi Ipposhi, Toshiaki Iwamatsu, Yuuichi Hirano	Jan. 12, 2004	Nov. 18, 2004
764-04	U.S. Patent Pub. 2006/0091432 (“Guha”)	Supratik Guha, Hussein Hanafi, Rajarao Jammy, Paul Solomon	Nov. 2, 2004	May 4, 2006
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764-07	JP2005-064190 (“JP-Ono”)	Tamashiro Ono, Akira Nishiyama	Aug. 11, 2003	Mar. 10, 2005
764-08	U.S. Patent No. 6,632,729 (“Paton”)	Eric Paton	June 7, 2002	Oct. 14, 2003

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764-09	U.S. Patent No. 6,168,958 ("Gardner")	Mark Gardner, H. Jim Fulford, Charles E. May	Aug. 7, 1998	Jan. 2, 2001
764-10	U.S. Patent Pub. 2005/0051856 ("Ono")	Mizuki Ono, Takamitsu Ishihara	July 2, 2004	Mar. 10, 2005
764-11	U.S. Patent Pub. 2005/0093084 ("Wang 084")	Chih-Hao Wang, Shang-Chih Chen, Yen-Ping Wang, Hsien-Kuang Chiu, Liang-Gi Yao, Chenming Hu	June 19, 2004	May 5, 2005
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764-13	"High-k Gate Dielectrics: Current Status and Materials Properties Considerations" ("Wilk")	G.D. Wilk et al.	N/A	May 15, 2001
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764-13	"High Quality Ultra Thin CVD HfO2 Gate Stack with Poly-Si Gate Electrode" ("Lee 2000")	S.J. Lee	N/A	Dec. 13, 2000
764-13	U.S. Patent Pub. 2005/0280105 ("Andreoni")	Wanda Andreoni, Alessandro Callegari, Eduard Cartier, Alessandro Curioni, Christopher D'Emic, Evengi Gousev, Michael Gribelyuk, Paul Jamison, Rajarao Jammy, Dianne Lacey, Fenton McFeely, Vijay Narayanan, Carlo Pignedoli, Joseph Shepard, Sufi Zafar	June 22, 2004	Dec. 22, 2004
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764-13	"High-k Dielectrics" ("Houssa")	Michel Houssa	N/A	2004

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764-13	U.S. Patent Pub. 2005/0045938 ("Mutou")	Akiyoshi Mutou, Hiroshi Ohji	Aug. 26, 2004	Mar. 3, 2005
764-13	U.S. Patent Pub. 2006/0131672 ("Wang 672")	Chih-Hao Wang, Ta-Wei Wang, Shang-Chih Chen, Ching-Wei Tsai	Apr. 27, 2005	June 22, 2006
764-13	U.S. Patent Pub. 2004/0110352 ("Bu")	Haowen Bu, Amitabh Jain, Wayne Bather, Stephanie Butler	Dec. 10, 2002	June 10, 2004
764-13	U.S. Patent No. 6,911,695 ("Ahmed")	Shafqat Ahmed, Henry Chao, DerChang Kau	Sept. 19, 2002	June 28, 2005
227-13	U.S. Patent 6,818,516 ("Lo")	Wai Lo, Hong Lin, Shiqun Gu, James R. B. Elmer	July 29, 2003	Nov. 16, 2004
227-13	U.S. Patent 6,617,209 ("Chau 209")	Robert Chau, Reza Arghavani, Mark Doczy	Feb. 22, 2002	Sept. 9, 2003
227-13	U.S. Patent 6,617,210 ("Chau 210")	Robert Chau, Reza Arghavani	May 31, 2002	Sept. 9, 2003
227-13	U.S. Patent 6,787,440 ("Parker")	Christopher G. Parker, Markus Kuhn, Ying Zhou, Scott A. Hareland, Suman Datta,	Dec. 10, 2002	Sept. 7, 2004

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
		Nick Lindert, Robert S. Chau, Timothy E. Glassman, Matthew V. Metz, Sunit Tyagi		

3. ’686 Patent Prior Art

Charted Prior Art Patents / Published Applications / Publications				
Exhibit Chart(s)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
686-01	“A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” Technical Digest of the 2007 IEEE Electron Devices Meeting (“IEDM”), pp. 247-250 (“Mistry2007 article”)	K. Mistry et al.	N/A	Dec. 11, 2007
686-01	“A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” Slides Presented at 2007 IEEE Electron Devices Meeting (“IEDM”), pp. 1-37 (“Mistry2007 presentation”)	K. Mistry et al.	N/A	Dec. 11, 2007

Charted Prior Art Patents / Published Applications / Publications				
Exhibit Chart(s)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
686-02	U.S. Pat. Pub. No. 2007/0066077 ("Akasaka077")	Akasaka et al.	Sept. 20, 2006	Mar. 22, 2007
686-03	U.S. Pat. Pub. No. 2006/0081939 ("Akasaka939")	Akasaka et al.	Sept. 9, 2005	Apr. 20, 2006
686-04	U.S. Pat. Pub. No. 2007/0215950 ("Aoyama950")	Aoyama	Mar. 19, 2007	Sept. 20, 2007
686-05	U.S. Pat. Pub. No. 2007/0138559 ("Bohr559")	Bohr	Dec. 16, 2005	June 21, 2007
686-06	U.S. Pat. Pub. No. 2006/0022277 ("Kavalieros277")	Kavalieros et al.	July 28, 2004	Feb. 2, 2006
686-07	U.S. Pat. No. 8,486,789 ("Okazaki 89")	Okazaki	Feb. 14, 2008	July 16, 2013
686-08	U.S. Pat. No. 8,536,660 ("Hsu660")	Hsu et al.	Mar. 12, 2008	Sept. 17, 2013
686-09	U.S. Pat. Pub. 2007/0249069 ("Alvarez 069")	Alvarez et al.	Apr. 25, 2006	Oct. 25, 2007
686-09	"A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting ("IEDM"), pp. 657-660 ("Bai article")	P. Bai et al.	N/A	Dec. 2004
686-09	"The Invention of Uniaxial Strained Silicon Transistors at Intel," pp. 1-4 ("Bohrarticle")	M. Bohr	N/A	Jan. 2007
686-09	U.S. Pat. Pub. 2004/0262683 ("Bohr683")	Bohr et al.	June 27, 2003	Dec. 30, 2004

Charted Prior Art Patents / Published Applications / Publications				
Exhibit Chart(s)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
686-09	U.S. Pat. No. 7,812,414 ("Hou414")	Hou et al.	Jan. 23, 2007	Oct. 12, 2010
686-09	U.S. Pat. Pub. 2007/0235823 ("Hsu823")	Hsu et al.	Mar. 30, 2006	Oct. 11, 2007
686-09	"2004 – The Year of 90-nm: A Review of 90 nm Devices," Proceedings of the 2005 IEEE / SEMI Advanced Semiconductor Manufacturing Conference ("ASMC"), pp. 72-77 ("James 90nm article")	D. James,	N/A	Apr. 12, 2005
686-09	U.S. Pat. Pub. 2005/0170104 ("Jung104")	Jung et al.	Jan. 29, 2004	Aug. 4, 2005
686-09	U.S. Pat. Pub. 2006/0286729 ("Kavalieros729")	Kavalieros et al.	June 21, 2006	Dec. 21, 2006
686-09	U.S. Pat. Pub. 2008/0145984 ("Ke984")	Ke et al.	Dec. 18, 2006	June 19, 2008
686-09	U.S. Pat. Pub. 2006/0148151 ("Murthy151")	Murthy et al.	Jan. 4, 2005	July 6, 2006
686-09	U.S. Pat. No. 6,949,482 ("Murthy482")	Murthy et al.	Dec. 8, 2003	Sept. 27, 2005
686-09	U.S. Pat. Pub. 2007/0105317 ("Nakajima317")	Nakajima	Mar. 20, 2006	May 10, 2007
686-09	U.S. Pat. No. 7,977,751 ("Nagaoka751")	Nagaoka et al.	Feb. 5, 2008	July 12, 2011
686-09	"A Logic Nanotechnology Featuring Strained-Silicon," IEEE Electron Device Letters, vol. 25, no. 4, pp. 191-193 ("Thompson Apr2004 article")	S.E. Thompson et al.	N/A	April 2004

Charted Prior Art Patents / Published Applications / Publications				
Exhibit Chart(s)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
686-09	"A 90-nm Logic Technology Featuring Strained-Silicon," IEEE Transactions on Electron Devices, vol. 51, no. 11, pp. 1790-1797 ("Thompson Nov2004 article")	S.E. Thompson et al.	N/A	Nov. 2004
686-09	U.S. Pat. No. 7,629,273 ("Yu273")	Yu et al.	Sept. 19, 2006	Dec. 8, 2009

Charted Prior Art Systems			
Exhibit (Chart)	**Item(s) Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/ Entity and Abbreviation**
686-01	Intel Xeon E5410 *See generally, e.g.*, D. James, "High-k/Metal Gates in Leading Edge Silicon Devices," Proceedings of the 2012 SEMI Advanced Semiconductor Manufacturing Conference ("ASMC"), pp. 346-353 (May 17, 2012) (*hereinafter* "James HKMG article"); D. James, "From Strain to High-K/Metal Gate—the 65–45 nm Transition," Proceedings of the 2008 IEEE/SEMI Advanced Semiconductor Manufacturing Conference ("ASMC"), pp. 76-81 (May 7, 2008) (*hereinafter* "James 65/45 article"); Mistry 2007 article; Mistry 2007 presentation. Intel Core 2 Extreme QX9650 *See generally, e.g.*, Semiconductor Insights, "Logic Detailed Structural Analysis with Gate Dielectric Analysis of the Intel 45nm QX9650 Penryn Processor," Report ID# 1107-18979-O-4DL-20 (Dec. 5, 2007) (*hereinafter* "QX9650_Report"); Mistry 2007 article; Mistry 2007 presentation.	At least by Nov. 11, 2007 Newegg.com had purchased at least one Intel Xeon E5410 and listed it for resale on its website by Nov. 28, 2007.[1] Newegg.com had purchased at least one Intel Core 2 Extreme QX9650 and listed it on its website for resale by Nov. 14, 2007).[2]	Intel_686_Products Intel Corp. made and publicized the claimed invention of the '686 patent in the U.S. before the alleged invention date,[3] and then sold products like the Xeon E5410 and Core 2 Extreme QX9650 that embody the claimed invention in the U.S. before the alleged invention date.

[1] *See, e.g.*, https://web.archive.org/web/20071128142237/http://www newegg.com:80/Product/Product.aspx?Item=N82E16819117149.
[2] *See, e.g.*, https://web.archive.org/web/20071114055447/http://www newegg.com:80/Product/Product.aspx?Item=N82E16819115035.
[3] *See generally, e.g.*, Mistry2007 article; Mistry2007 presentation. *See also, e.g.*, "Intel® 45nm Transistor Technology," https://web.archive.org/web/20070208005508/http://www.intel.com/pressroom/kits/45nm/index.htm (archived Feb. 8, 2007); "Intel's Transistor Technology Breakthrough Represents Biggest Change to Computer Chips In 40 Years," https://web.archive.org/web/20070207224401/http://www.intel.com/pressroom/archive/releases/20070128comp htm (archived Feb. 7, 2007); "Intel First to Demonstrate Working 45nm Chips," https://web.archive.org/web/20070208060210/http://www.intel.com/pressroom/archive/releases/20060125comp.htm (archived Feb. 8, 2007).

In addition, TSMC reserves the right to rely upon at least the following additional prior art to demonstrate the state of the art at the time of the alleged invention the ’686 patent.

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
M. Baklanov et al., *Dielectric Films for Advanced Microelectronics* (2007) (“Baklanov”)	N/A	Mar. 19, 2007
G. Eneman et al., “Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study,” IEEE Transactions on Electron Devices, vol. 54, no. 6, pp. 1446-1453 (“Eneman article”)	N/A	June 2007
International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) (“ITRS 2007 FEP”)	N/A	Aug. 21, 2007
International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures (2007 ed.) (“ITRS 2007 PIDS”)	N/A	Aug. 21, 2007
U.S. Pat. No. 9,299,704 to Ji et al. (“Ji704”).	Sept. 17, 2014	Mar. 29, 2016
Y.C. Liu et al., “Single Stress Liner for Both NMOS and PMOS Current Enhancement By a Novel Ultimate Spacer Process,” Technical Digest of the 2005 IEEE International Electron Devices Meeting (IEDM), pp. 836-839 (“Liu article”)	N/A	Dec. 2005
H.B. Michaelson, “The Work Function of the Elements and Its Periodicity,” Journal of Applied Physics, vol. 48, pp. 4729-4733 (“Michaelson article”)	N/A	Nov. 1, 1977
P. Morin et al., “Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS,” ECS Transactions, vol. 6, no. 3, pp. 355-369 (“Morin article”)	N/A	May 10, 2006
M. Quirk & J. Serda, *Semiconductor Manufacturing Technology* (2001) (“Quirk & Serda”)	N/A	Nov. 19, 2000
J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000) (“Plummer”)	N/A	At least Dec. 31, 2000

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
S.C. Song et al., "Highly Manufacturable 45nm LSTP CMOSFETs Using Novel Dual High-k and Dual Metal Gate CMOS Integration," Digest of Technical Papers, 2006 IEEE Symposium on VLSI Technology	N/A	June 15, 2006
Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) ("Sun article")	N/A	May 2007
S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) ("Sze")	N/A	Sept. 30, 1981
U.S. Pat. No. 6,563,178 to Moriwaki et al. ("Moriwaki178")	Mar. 28, 2001	May 13, 2003
U.S. Pat. No. 6,849,511 to Iriyama et al. ("Iriyama511")	Apr. 7, 2004	Feb. 1, 2005
U.S. Pat. No. 6,881,631 to Saito et al. ("Saito631")	Nov. 5, 2003	Apr. 19, 2005
U.S. Pat. No. 7,153,784 to Brask et al. ("Brask784")	Apr. 20, 2004	Dec. 26, 2006
U.S. Pat. Pub. No. 2002/0037615 to Matsuo ("Matsuo615")	Sept. 25, 2001	Mar. 28, 2002
U.S. Pat. Pub. No. 2005/0064663 to Saito ("Saito663")	Dec. 18, 2003	Mar. 24, 2005
U.S. Pat. Pub. No. 2005/0250258 to Metz et al. ("Metz258")	May 4, 2004	Nov. 10, 2005
U.S. Pat. Pub. No. 2005/0258468 to Colombo et al. ("Colombo468")	July 13, 2004	Nov. 24, 2005
U.S. Pat. Pub. No. 2008/0111167 to Yamaguchi ("Yamaguchi167")	June 18, 2007	May 15, 2008
Westlinder et al., "On the Thermal Stability of Atomic Layer Deposited TiN as Gate Electrode in MOS Devices," IEEE Electron Device Letters, vol. 24, no. 9, pp. 550-552 ("Westlinder article")	N/A	Sept. 2003
Z.B. Zhang et al., "Integration of Dual Metal Gate CMOS with TaSiN (NMOS) and Ru (PMOS) Gate Electrodes on HfO_2 Gate Dielectric," Digest of Technical Papers, 2005 IEEE Symposium on VLSI Technology, pp. 50-51 ("Zhang article")	N/A	June 16, 2005

4. ’180 Patent Prior Art

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
180-01	U.S. Pub. 2002/0063299 (“Kamata”)	Yoshiki Kamata, Akira Nishiyama	Nov. 28, 2001	May 30, 2002
180-02	U.S. Patent Pub. 2006/0091432 (“Guha”)	Supratik Guha, Hussein Hanafi, Rajarao Jammy, Paul Solomon	Nov. 2, 2004	May 4, 2006
180-03	U.S. Patent Pub. 2003/0025135 (“Matsumoto 135”)	Takuji Matsumoto, Hirokazu Sayama, Shigenobu Maeda, Toshiaki Iwamatsu, Kazunobu Ota	July 11, 2002	Feb. 6, 2003
180-04	U.S. Patent No. 6,251,763 (“Inumiya 763”)	Seiji Inumiya, Katsuhiko Hieda, Tetsuo Matsuda, Yoshio Ozawa	June 29, 1998	June 26, 2001
180-05	U.S. Patent No. 6,054,355 (“Inumiya 355”)	Seiji Inumiya, Tomohiro Saito, Atsushi Yagishita, Katsuhiko Hieda, Toshihiko Iinuma	June 29, 1998	Apr. 25, 2000
180-06	U.S. Patent No. 6,346,732 (“Mizushima”)	Ichiro Mizushima, Yuichiro Mitani, Shigeru Kambayashi, Kiyotaka Miyano	May 11, 2000	Feb. 12, 2002

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
180-07	"Investigation of Poly-Si/HfO2 Gate Stacks in a Self-aligned 70nm MOS Process Flow" ("Kubicek")	Stefan Kubicek et al.	N/A	Sept. 2003
180-08	"50-nm Fully Depleted SOI CMOS Technology with HfO2 Gate Dielectric and TiN Gate" ("Vandooren")	Anne Vandooren et al.	N/A	Dec. 2003
180-09	JP2004-356576 ("Sasaki")	Takaoki Sasaki, Takeshi Maeda	May 30, 2003	Dec. 16, 2004
180-10	JP2005-064190 ("JP-Ono")	Tamashiro Ono, Akira Nishiyama	Aug. 11, 2003	Mar. 10, 2005
180-11	U.S. Patent Pub. 2004/0227185 ("Matsumoto 185")	Takuji Matsumoto, Takashi Ipposhi, Toshiaki Iwamatsu, Yuuichi Hirano	Jan. 12, 2004	Nov. 18, 2004
180-12	U. S. Patent No. 6,933,189 ("Clevenger")	Lawrence Clevenger, Louis Hsu, Carl Radens, Joseph Shepard, Jr.	June 16, 2004	Aug. 23, 2005
180-13	U.S. Patent Pub. 2005/0093084 ("Wang 084")	Chih-Hao Wang, Shang-Chih Chen, Yen-Ping Wang, Hsien-Kuang Chiu, Liang-Gi Yao, Chenming Hu	June 19, 2004	May 5, 2005
180-14	U.S. Patent Pub. 2005/0051856 ("Ono")	Mizuki Ono, Takamitsu Ishihara	July 2, 2004	Mar. 10, 2005

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
180-15	"Effects of ALD HfO2 Thickness on Charge Trapping and Mobility" to Sim ("Sim")	J.H. Sim et al.	N/A	June 17, 2005
180-15	"High-k Gate Dielectrics: Current Status and Materials Properties Considerations" ("Wilk")	G.D. Wilk et al.	N/A	May 15, 2001
180-15	U.S. Patent 6,504,214 ("Yu")	Bin Yu, Qi Xiang	Jan. 11, 2002	Jan. 7, 2003
180-15	"Impact of Hf Concentration on Performance and Reliability for HfSiON-CMOSFET" ("Watanabe 2004")	Takeshi Watanabe et al.	N/A	Dec. 15, 2004
180-15	"Design Guideline of HfSiON Gate Dielectrics for 65 nm CMOS Generation" ("Watanabe 2003")	Takeshi Watanabe et al.	N/A	June 12, 2003
180-15	"Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application" ("Lee 1999")	Byoung Hun Lee et al.	N/A	Dec. 8, 1999
180-15	"High Quality Ultra Thin CVD HfO2 Gate Stack with Poly-Si Gate Electrode" ("Lee 2000")	S.J. Lee	N/A	Dec. 13, 2000
180-15	U.S. Patent Pub. 2005/0280105 ("Andreoni")	Wanda Andreoni, Alessandro Callegari, Eduard Cartier, Alessandro Curioni, Christopher D'Emic,	June 22, 2004	Dec. 22, 2004

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
		Evengi Gousev, Michael Gribelyuk, Paul Jamison, Rajarao Jammy, Dianne Lacey, Fenton McFeely, Vijay Narayanan, Carlo Pignedoli, Joseph Shepard, Sufi Zafar		
180-15	"Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology" ("Wolf")	Stanley Wolf	N/A	2002
180-15	"High-k Dielectrics" ("Houssa")	Michel Houssa	N/A	2004
180-15	"Silicon VLSI Technology: Fundamentals, Practice and Modeling" ("Plummer")	James D. Plummer	N/A	2000
180-15	U.S. Patent Pub. 2005/0045938 ("Mutou")	Akiyoshi Mutou, Hiroshi Ohji	Aug. 26, 2004	Mar. 3, 2005
180-15	U.S. Patent Pub. 2006/0131672 ("Wang 672")	Chih-Hao Wang, Ta-Wei Wang, Shang-Chih Chen, Ching-Wei Tsai	Apr. 27, 2005	June 22, 2006
180-15	U.S. Patent Pub. 2004/0110352 ("Bu")	Haowen Bu, Amitabh Jain, Wayne Bather, Stephanie Butler	Dec. 10, 2002	June 10, 2004

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
180-15	U.S. Patent No. 6,911,695 ("Ahmed")	Shafqat Ahmed, Henry Chao, DerChang Kau	Sept. 19, 2002	June 28, 2005

5. '076 Patent Prior Art

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
076-01	U.S. Pub. 2002/0063299 ("Kamata")	Yoshiki Kamata, Akira Nishiyama	Nov. 28, 2001	May 30, 2002
076-02	U.S. Patent Pub. 2006/0091432 ("Guha")	Supratik Guha, Hussein Hanafi, Rajarao Jammy, Paul Solomon	Nov. 2, 2004	May 4, 2006
076-03	U.S. Patent Pub. 2003/0025135 ("Matsumoto 135")	Takuji Matsumoto, Hirokazu Sayama, Shigenobu Maeda, Toshiaki Iwamatsu, Kazunobu Ota	July 11, 2002	Feb. 6, 2003
076-04	U.S. Patent No. 6,251,763 ("Inumiya 763")	Seiji Inumiya, Katsuhiko Hieda, Tetsuo Matsuda, Yoshio Ozawa	June 29, 1998	June 26, 2001
076-05	U.S. Patent No. 6,054,355 ("Inumiya 355")	Seiji Inumiya, Tomohiro Saito, Atsushi Yagishita, Katsuhiko	June 29, 1998	Apr. 25, 2000

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
		Hieda, Toshihiko Iinuma		
076-06	U.S. Patent No. 6,346,732 (“Mizushima”)	Ichiro Mizushima, Yuichiro Mitani, Shigeru Kambayashi, Kiyotaka Miyano	May 11, 2000	Feb. 12, 2002
076-07	“Investigation of Poly-Si/HfO2 Gate Stacks in a Self-aligned 70nm MOS Process Flow” (“Kubicek”)	Stefan Kubicek et al.	N/A	Sept. 2003
076-08	“50-nm Fully Depleted SOI CMOS Technology with HfO2 Gate Dielectric and TiN Gate” (“Vandooren”)	Anne Vandooren et al.	N/A	Dec. 2003
076-09	JP2004-356576 (“Sasaki”)	Takaoki Sasaki, Takeshi Maeda	May 30, 2003	Dec. 16, 2004
076-10	JP2005-064190 (“JP-Ono”)	Tamashiro Ono, Akira Nishiyama	Aug. 11, 2003	Mar. 10, 2005
076-11	U.S. Patent Pub. 2004/0227185 (“Matsumoto 185”)	Takuji Matsumoto, Takashi Ipposhi, Toshiaki Iwamatsu, Yuuichi Hirano	Jan. 12, 2004	Nov. 18, 2004
076-12	U. S. Patent No. 6,933,189 (“Clevenger”)	Lawrence Clevenger, Louis Hsu, Carl Radens, Joseph Shepard, Jr.	June 16, 2004	Aug. 23, 2005

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
076-13	U.S. Patent Pub. 2005/0093084 ("Wang 084")	Chih-Hao Wang, Shang-Chih Chen, Yen-Ping Wang, Hsien-Kuang Chiu, Liang-Gi Yao, Chenming Hu	June 19, 2004	May 5, 2005
076-14	U.S. Patent Pub. 2005/0051856 ("Ono")	Mizuki Ono, Takamitsu Ishihara	July 2, 2004	Mar. 10, 2005
076-15	"Effects of ALD HfO2 Thickness on Charge Trapping and Mobility" to Sim ("Sim")	J.H. Sim et al.	N/A	June 17, 2005
076-15	"High-k Gate Dielectrics: Current Status and Materials Properties Considerations" ("Wilk")	G.D. Wilk et al.	N/A	May 15, 2001
076-15	U.S. Patent 6,504,214 ("Yu")	Bin Yu, Qi Xiang	Jan. 11, 2002	Jan. 7, 2003
076-15	"Impact of Hf Concentration on Performance and Reliability for HfSiON-CMOSFET" ("Watanabe 2004")	Takeshi Watanabe et al.	N/A	Dec. 15, 2004
076-15	"Design Guideline of HfSiON Gate Dielectrics for 65 nm CMOS Generation" ("Watanabe 2003")	Takeshi Watanabe et al.	N/A	June 12, 2003
076-15	"Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application" ("Lee 1999")	Byoung Hun Lee et al.	N/A	Dec. 8, 1999
076-15	"High Quality Ultra Thin CVD HfO2 Gate Stack	S.J. Lee	N/A	Dec. 13, 2000

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
	with Poly-Si Gate Electrode" ("Lee 2000")			
076-15	U.S. Patent Pub. 2005/0280105 ("Andreoni")	Wanda Andreoni, Alessandro Callegari, Eduard Cartier, Alessandro Curioni, Christopher D'Emic, Evengi Gousev, Michael Gribelyuk, Paul Jamison, Rajarao Jammy, Dianne Lacey, Fenton McFeely, Vijay Narayanan, Carlo Pignedoli, Joseph Shepard, Sufi Zafar	June 22, 2004	Dec. 22, 2004
076-15	"Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology" ("Wolf")	Stanley Wolf	N/A	2002
076-15	"High-k Dielectrics" ("Houssa")	Michel Houssa	N/A	2004
076-15	"Silicon VLSI Technology: Fundamentals, Practice and Modeling" ("Plummer")	James D. Plummer	N/A	2000
076-15	U.S. Patent Pub. 2005/0045938 ("Mutou")	Akiyoshi Mutou, Hiroshi Ohji	Aug. 26, 2004	Mar. 3, 2005

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Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
076-15	U.S. Patent Pub. 2006/0131672 ("Wang 672")	Chih-Hao Wang, Ta-Wei Wang, Shang-Chih Chen, Ching-Wei Tsai	Apr. 27, 2005	June 22, 2006
076-15	U.S. Patent Pub. 2004/0110352 ("Bu")	Haowen Bu, Amitabh Jain, Wayne Bather, Stephanie Butler	Dec. 10, 2002	June 10, 2004
076-15	U.S. Patent No. 6,911,695 ("Ahmed")	Shafqat Ahmed, Henry Chao, DerChang Kau	Sept. 19, 2002	June 28, 2005

6. '779 Patent Prior Art

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
779-01	U.S. Patent No. 6,787,421 ("Gilmer")	David C. Gilmer Christopher C. Hobbs Hsing-Huang Tseng	Aug. 15, 2002	Sept. 4, 2004
779-02	U.S. Patent No. 8,114,739 ("Chowdhury")	Murshed M. Chowdhury James K. Schaeffer	Sept. 28, 2009	Feb. 14, 2012
779-03	U.S. Patent No. 6,881,657 ("Torii")	Kazuyoshi Torii Riichirou Mitsuhashi Atsushi Horiuchi	July 13, 2004	Apr. 19, 2005
779-04	U.S. Patent No. 7,354,830 ("Lin")	Chun-Chieh Lin Wen-Chin Lee Chenming Hu Shang-Chih Chen Chih-Hao Wang Fu-Liaog Yang Yee-Chia Yeo	Mar. 16, 2006	Apr. 8, 2008

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
779-05	U.S. Patent No. 8,008,143 ("Hsu")	Kuang-Yuan Hsu Da-Yuan Lee Wei-Yang Lee Hun-Jan Tao	Dec. 30, 2009	Aug. 30, 2011
779-06	U.S. Patent Pub. 2010/0270621 ("Iwamoto")	Toshiyuki Iwamoto Gen Tsutsui	Apr. 20, 2010	Oct. 28, 2010
779-07	U.S. Patent No. 7,087,494 ("Suzuki")	Tatsuya Suzuki Hidemitsu Aoki	Oct. 16, 2003	Aug. 8, 2006
779-08	Japan Patent Pub. 2004079606 ("Irino")	Kiyoshi Irino Yusuke Morizaki Yoshihiro Sugita	Aug. 12, 2002	Mar. 11, 2004
779-09	Japan Patent Pub. 2003100896A ("Fujiwara")	Ikuo Fujiwara Akira Nishiyama	Sept. 25, 2001	Apr. 4, 2003
779-10	U.S. Patent No. 6,953,727 ("Hori")	Mitsuaki Hori	Aug. 21, 2003	Oct. 11, 2005
779-11	U.S. Patent No. 8,106,455 ("Greene")	Brian J. Greene Michael P. Chudzik Shu-Jen Han William K. Henson Yue Liang Edward P. Maciejewski Myung-Hee Na Edward J. Nowak Xiaojun Yu	Apr. 30, 2009	Jan. 31, 2012
779-12	U.S. Patent Pub. 2007/0052037 ("Luan")	Hongfa Luan	May 15, 2006	Mar. 8, 2007
779-14	U.S. Patent No. 7,382,023 ("Chen")	Hao-Yu Chen Chang-Yun Chang Di-Hong Lee Fu-Liang Yang	Mar. 29, 2005	June 3, 2008
779-15	U.S. Patent No. 6,693,333 ("Yu")	Bin Yu	May 1, 2001	Feb. 17, 2004
779-16	U.S. Patent No. 7,564,108 ("Wang")	Chih-Hao Wang Ta-Wei Wang Shang-Chih Chen Ching-Wei Tsai	Apr. 27, 2005	July 21, 2009

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
779-17	Applicant Admitted Prior Art ("AAPA")			
779-17	U.S. Patent No. 7,144,784 ("Min")	Byoung W. Min Nigel G. Cave Venkat R. Kolagunta Omar Zia Sinan Goktepeli	July 29, 2004	Dec. 5, 2006
779-17	U.S. Patent No. 8,252,649 ("Stahrenberg")	Knut Stahrenberg Jin-Ping Han	Dec. 22, 2008	Aug. 28, 2012
779-17	U.S. Patent No. 8,384,160 ("Onishi")	Kazuhiro Onishi Kazuhiro Tsukamoto	Nov. 30, 2009	Feb. 26, 2013
779-17	U.S. Patent No. 10,424,517 ("Tseng")	Joshua Tseng Yasutoshi Okuno Lars-Ake Ragnarsson Tom Schram Stefan Kubicek Thomas Y. Hoffman Naohisa Sengoku	June 13, 2016	Sept. 24, 2019
779-17	U.S. Patent Publication 2008/0128822 to Koyama ("Koyama")	Masato Koyama Yoshinori Tsuchiya Yuuichi Kamimuta Reika Ichihara Katsuyuki Sekine	May 24, 2007	June 5, 2008
779-17	U.S. Patent Pub. 2010/0258878 ("Mise")	Nobuyuki Mise Takahisa Eimori	Nov. 26, 2008	Oct. 14, 2010
779-17	U.S. Patent Pub. 2011/0068413 ("Liaw")	Jhon-Jhy Liaw	July 1, 2010	Mar. 24, 2011
779-17	"Advanced Gate Materials and Processes for sub-70nm CMOS Technology" ("Ranade-Thesis")	Pushkar Sharad Ranade	N/A	2002
779-17	"An Investigation of the Work Function of Metal Gate Electrodes for Advanced CMOS Applications" ("Wong-Thesis")	Gloria Man Ting Wong	N/A	2008

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
779-17	"A Cost-Effective LOP/LSTP Integrated CMOS Platform Utilizing Multi-Thickness SiON Gate Dielectrics with Hafnium for 45-nm Node" ("Tsutsui")	Gen Tsutsui Shinya Maruyama Tomohisa Abe Hidetatsu Nakamura Tadashi Fukase	N/A	2007
779-17	"A Novel Approach for Integration of Dual Metal Gate Process Using Ultra Thin Aluminum Nitride Buffer Layer" ("Park")	Chang Seo Park Byung Jin Cho Du An Yan N. Balasubramanian Dim-Lee Kwong	N/A	June 2003
779-17	"CMOS VLSI Design: A Circuits and Systems Perspective, Third Edition ("Weste")	Neil H.E. Weste David Harris	N/A	2005
779-17	"Development of an Innovative Fabrication Method for nMOS to pMOS Tunable Single Metal Gate/High-k Insulator Devices for Multiple Threshold Voltage Applications" ("Burham-Thesis")	Cynthia Faye Burham	N/A	2009
779-17	"High-k Gate Dielectrics" to Houssa (IOP Publishing Ltd. 2004) ("Houssa")	Michel Houssa	N/A	2004
779-17	"Integration of ALD AlN Work Function Tuning Layers" ("Lu")	Chi-Pei Lu Mathias Schmidt Heinrich D. B. Gottlob Heinrich Kurz	N/A	Apr. 2010
779-17	"International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures" (2007 Edition) ("ITRS")	N/A	N/A	2007

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
779-17	"Metal gate work function engineering using AlNx interfacial layers" ("Alshareef")	H. N. Alshareef H. F. Luan K. Choi H. R. Harris H. C. Wen M. A. Quevedo-Lopez P. Majhi B. H. Lee	N/A	Mar. 2006
779-17	"Semiconductor Devices: Physics and Technology" by Sze (Second Edition, 2002) ("Sze")	S. M. Sze	N/A	2002
779-17	"Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology" to Wolf ("Wolf")	Stanley Wolf	N/A	2002
779-17	"Silicon VLSI Technology: Fundamentals, Practice and Modeling" (Prentice Hall 2000) ("Plummer")	James D. Plummer Michael D. Deal Peter B. Griffin	N/A	2000
779-17	"Three-Layer Laminated Metal Gate Electrodes With Tunable Work Functions for CMOS Applications" ("Bai")	W. P. Bai S. H. Bae H. C. Wen S. Mathew L. K. Bera N. Balasubramanian N. Yamada M. F. Li	N/A	April 2005
779-17	"Tungsten work function engineering for dual metal gate nano-CMOS" ("Efavi")	J.K. Efavi T. Mollenhauer T. Wahlbrink H.D.B. Gottlob M.C. Lemme H. Kurz	N/A	July 2005
779-17	"Work Function Tunability of Refractory Metal Nitrides by Lanthanum or Aluminum	Xin Peng Wang Andy Eu-Jin Lim Hong Yu Yu Ming-Fu Li	N/A	November 2007

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
	Doping for Advanced CMOS Devices" ("Wang-Paper")	Chi Ren Wei-Yip Loh Chun Xiang Zhu Albert Chin Alastair David Trigg Yee-Chia Yeo Serge Biesemans Guo-Qiang Lo Dim-Lee Kwong		
779-17	U.S. Patent Publication 2009/0068807 to Karve, et al. ("Karve")	Gauri V. Karve Srikanth B. Samavedam William J. Taylor, Jr	Sept. 7, 2007	March 12, 2009

Charted Prior Art Systems			
Exhibit (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
779-13	Intel Core 2 Extreme QX9650 Processor *See generally, e.g.*, Semiconductor Insights, "Logic Detailed Structural Analysis with Gate Dielectric Analysis of the Intel 45nm QX9650 Penryn Processor," Report ID# 1107-18979-O-4DL-20 (Dec. 5, 2007) ("QX9650 Report");	At least by Nov. 11, 2007 Newegg.com had purchased at least one Intel Core 2 Extreme QX9650 and listed it on its website for resale by Nov. 14, 2007).[4]	Intel ("Intel QX9650") Intel Corp. made and publicized the claimed invention of the '779 patent in the U.S. before the alleged invention date,[5] and then sold products like the Core 2 Extreme QX9650 that embody the claimed invention in the U.S. before the alleged invention date.

[4] *See, e.g.*, https://web.archive.org/web/20071114055447/http://www newegg.com:80/Product/Product.aspx?Item=N82E16819115035.

[5] *See generally, e.g.*, Mistry2007 article; Mistry2007 presentation. *See also, e.g.*, "Intel® 45nm Transistor Technology," https://web.archive.org/web/20070208005508/http://www.intel.com/pressroom/kits/45nm/index.htm (archived Feb. 8, 2007); "Intel's Transistor Technology Breakthrough Represents Biggest Change to Computer Chips In 40 Years," https://web.archive.org/web/20070207224401/http://www.intel.com/pressroom/archive/

Charted Prior Art Systems			
Exhibit (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
	Mistry 2007 article; Mistry 2007 presentation.		

In addition, TSMC reserves the right to rely upon at least the following additional prior art to demonstrate the state of the art at the time of the alleged invention the ’779 patent.

Additional Prior Art			
Reference	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
U.S. Patent No. 7,709,902 (“Doris”)	Bruce B. Doris Young-Hee Kim Barry P. Linder Vijay Narayanan Vamsi K. Paruchuri	Sept. 16, 2008	May 4, 2010
U.S. Patent Pub. 2010/0258878 (“Mise”)	Nobuyuki Mise Takahisa Eimori	Nov. 26, 2008	Oct. 14, 2010
U.S. Patent No. 8,865,539 (“Chen 539”)	Hao-Yu Chen Chang-Yun Chang Di-Hong Lee Fu-Liang Yang	Mar. 29, 2005	Oct. 21, 2014
U.S. Patent Pub. 2008/0122011 (“Wu”)	Shien-Yang Wu	Nov. 3, 2006	May 29, 2008
U.S. Patent Pub. 2010/0038692 (“Chuang”)	Harry Chuang Mong Song Liang Wen-Chih Yang Chien-Liang Chen Chii-Horng Li	Aug. 14, 2008	Feb. 18, 2010
U.S. Patent Pub. 2009/0221105 (“Hishiki”)	Masanobu Hishiki Yaichiro Miura Hiroshi Kawashima Katsuhiro Mitsuda	Feb. 26, 2009	Sept. 3, 2009
U.S. Patent Pub. 2010/0276753 (“Greene 753”)	Brian J. Greene Michael P. Chudzik Shu-Jen Han	Apr. 30. 2009	Nov. 4, 2010

releases/20070128comp htm (archived Feb. 7, 2007); “Intel First to Demonstrate Working 45nm Chips,” https://web.archive.org/web/20070208060210/http://www.intel.com/pressroom/archive/releases/20060125comp.htm (archived Feb. 8, 2007).

Additional Prior Art			
Reference	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
	William K. Henson Yue Liang Edward P. Maciejewski Myung-Hee Na Edward J. Nowak Xiaojun Yu		
U.S. Patent No. 7,745,278 ("Bojarczuk Patent")	Nestor A. Bojarczuk, Jr. Cyril Cabral, Jr. Eduard A. Cartier Matthew W. Copel Martin M. Frank Evgeni P. Gousev Supratik Guha Rajarao Jammy Vijay Narayanan Vamsi K. Paruchuri	Sept. 16, 2008	June 29, 2010
U.S. Patent Pub. 2006/0244035 ("Bojarczuk Publication")	Nestor Bojarczuk Michael Chudzik Matthew Copel Supratik Guha Rajarao Jammy Vijay Narayanan Vamsi Paruchuri	Apr. 29, 2005	Nov. 2, 2006
"An Integratable Dual Metal Gate CMOS Process Using an Ultrathin Aluminum Nitride Buffer Layer" ("Park-May-2003")	Chang Seo Park Byung Jin Cho Dim-Lee Kwong	N/A	May 2003
"2003 Symposium on VLSI Technology, Digest of Technical Papers" ("VLSI Symposium")	N/A	N/A	June 10-12, 2003
"Statistical Simulation of Metal-Gate Work-function Fluctuation in High-k/Metal-Gate Devices" ("Yu Article")	Chia-Hui Yu Ming-Hung Han Hui-Wen Cheng Zhong-Cheng Su Yiming Li Hiroshi Watanabe	N/A	Sept. 6-8, 2010
"Threshold Voltage Control in Al0.72Ga0.28N/AIN/GaN	Guowang Li Tom Zimmermann Yu Cao	N/A	Sept. 2010

Additional Prior Art			
Reference	**Inventor(s)/Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
HEMTs by Work-Function Engineering" ("Li")	Chuanxin Lian Xiu Xing Ronghua Wang Patrick Fay Huili Grace Xing Debdeep Jena		
"The Science and Engineering of Microelectronic Fabrication" (Second Edition, 2001) ("Campbell")	Stephen A. Campbell	N/A	2001

7. '425 Patent Prior Art

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
425-01	"A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell," Technical Digest of the 2004 IEEE International Electron Devices Meeting ("IEDM"), pp. 657-660 ("Bai article")	Bai et al.	N/A	Dec. 2004

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
425-01	"From Strain to High-K/Metal Gate—the 65–45 nm Transition," Proceedings of the 2008 IEEE/SEMI Advanced Semiconductor Manufacturing Conference ("ASMC"), pp. 76-81 ("James 65/45 article")	D. James	N/A	May 7, 2008
425-01	"An Advanced Low Power, High Performance, Strained Channel 65nm Technology," Technical Digest of the 2005 IEEE Electron Devices Meeting ("IEDM"), pp. 245-247 ("Tyagi article")	S. Tyagi et al.	N/A	Dec. 5, 2005
425-03	U.S. Pat. Pub. 2009/0020820 ("Baik820")	Baik et al.	June 13, 2008	Jan. 22, 2009
425-04	U.S. Pat. Pub. 2004/0262683 ("Bohr683")	Bohr et al.	June 27, 2003	Dec. 30, 2004
425-05	U.S. Pat. Pub. 2007/0200179 ("Chen179")	Chen et al.	Feb. 24, 2006	Aug. 30, 2007
425-06	U.S. Pat. Pub. 2011/0042729 ("Chen729")	Chen et al.	Aug. 21, 2009	Feb. 24, 2011
425-07	U.S. Pat. Pub. 2005/0260810 ("Cheng810")	Cheng et al.	May 21, 2004	Nov. 24, 2005
425-08	U.S. Pat. Pub. 2005/0112817 ("Cheng817")	Cheng et al.	Aug. 11, 2004	May 26, 2005

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
425-09	U.S. Pat. Pub. 2004/0262784 ("Doris784")	Doris et al.	June 30, 2003	Dec. 20, 2004
425-10	U.S. Pat. Pub. 2006/0151776 ("Hatada776")	Hatada et al.	May 19, 2005	July 13, 2006
425-11	U.S. Pat. Pub. 2007/0235823 ("Hsu823")	Hsu et al.	Mar. 30, 2006	Oct. 11, 2007
425-12	"2004 – The Year of 90-nm: A Review of 90 nm Devices," Proceedings of the 2005 IEEE / SEMI Advanced Semiconductor Manufacturing Conference ("ASMC"), pp. 72-77 ("James 90nm article")	James	N/A	Apr. 12, 2005
425-13	U.S. Pat. Pub. 2008/0145984 ("Ke984")	Ke et al.	Dec. 18, 2006	June 19, 2008
425-14	U.S. Pat. Pub. 2007/0134870 ("Lee870")	Lee et al.	Dec. 12, 2005	June 14, 2007
425-15	U.S. Pat. Pub. 2009/0032844 ("Ogura844")	Ogura et al.	July 29, 2008	Feb. 5, 2009
425-16	U.S. Pat. Pub. 2008/0029825 ("Saito825")	Saito et al.	Aug. 2, 2007	Feb. 7, 2008
425-17	U.S. Pat. Pub. 2006/0138398 ("Shimamune398")	Shimamune et al.	Apr. 18, 2005	June 29, 2006
425-18	U.S. Pat. Pub. 2007/0034906 ("Wang906")	Wang et al.	Dec. 27, 2005	Feb. 15, 2007
425-19	U.S. Pat. Pub. 2009/0246922 ("Wu922")	Wu et al.	Mar. 27, 2008	Oct. 1, 2009

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
425-20	U.S. Pat. Pub. 2007/0200170 ("Yamasaki170")	Yamasaki et al.	Feb. 14, 2007	Aug. 30, 2007
425-21	U.S. Pat. Pub. 2007/0249069 ("Alvarez069")	Alvarez et al.	Apr. 25, 2006	Oct. 25, 2007
425-21	U.S. Pat. Pub. 2007/0018205 ("Chidambarrao205")	Chidambarrao et al.	July 21, 2005	Jan. 25, 2007
425-21	U.S. Pat. No. 7,816,243 ("Chuang243")	Chuang et al.	Feb. 18, 2009	Oct. 19, 2010
425-21	U.S. Pat. Pub. 2009/0065807 ("Fujimoto807")	Fujimoto	Aug. 29, 2008	Mar. 12, 2009
425-21	U.S. Pat. Pub. 2005/0285203 ("Fukutome203")	Fukutome et al.	Dec. 13, 2004	Dec. 29, 2005
425-21	U.S. Pat. Pub. 2005/0170104 ("Jung104")	Jung et al.	Jan. 29, 2004	Aug. 4, 2005
425-21	U.S. Pat. Pub. 2006/0286729 ("Kavalieros729")	Kavalieros et al.	June 21, 2006	Dec. 21, 2006
425-21	"Mobility Improvement for 45nm Node by Combination of Optimized Stress Control and Channel Orientation Design," Technical Digest of the 2004 IEEE International Electron Devices Meeting ("IEDM"), pp. 217-220 ("Komoda article")	Komoda et al.,	N/A	Dec. 15, 2004
425-21	U.S. Pat. Pub. 2008/0293207 ("Koutny207")	Koutny, Jr. et al.	May 22, 2008	Nov. 27, 2007
425-21	U.S. Pat. Pub. 2008/0070360 ("Kwon360")	Kwon et al.	Sept. 19, 2006	Mar. 20, 2008

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
425-21	"Single Stress Liner for Both NMOS and PMOS Current Enhancement by a Novel Ultimate Spacer Process," Technical Digest of the 2005 IEEE International Electron Devices Meeting ("IEDM"), pp. 836-839 ("Liu article")	C. Liu et al.,	N/A	Dec. 5, 2005
425-21	U.S. Pat. Pub. 2005/0218455 ("Maeda455")	Maeda et al.	Feb. 28, 2005	Oct. 6, 2005
425-21	"A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Technical Digest of the 2007 IEEE Electron Devices Meeting ("IEDM"), pp. 247-250 ("Mistry2007 article")	K. Mistry et al.,	N/A	Dec. 11, 2007

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
425-21	"A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Slides Presented at 2007 IEEE Electron Devices Meeting ("IEDM"), pp. 1-37 ("Mistry 2007 presentation")	K. Mistry et al.,	N/A	Dec. 11, 2007
425-21	U.S. Pat. Pub. 2010/0075476 ("Miyashita476")	Miyashita	Aug. 20, 2009	Mar. 25, 2010
425-21	U.S. Pat. No. 6,949,482 ("Murthy482")	Murthy et al.	Dec. 8, 2003	Sept. 27, 2005
425-21	U.S. Pat. No. 6,797,556 ("Murthy556")	Murthy et al.	Jan. 7, 2003	Sept. 28, 2004
425-21	"A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171μm^2 SRAM Cell Size in a 291Mb Array," Technical Digest of the of the 2008 IEEE International Electron Devices Meeting ("IEDM"), pp. 1-3 ("Natarajan article")	S. Natarajan et al.	N/A	Dec. 2008
425-21	U.S. Pat. Pub. 2007/0231893 ("Shifren983")	Shifren et al.	Mar. 31, 2006	Oct. 4, 2007

Charted Prior Art Patents / Published Applications / Publications				
Exhibit (Chart)	**Reference**	**Inventor(s) / Author(s)**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
425-21	"A Logic Nanotechnology Featuring Strained-Silicon," IEEE Electron Device Letters, vol. 25, no. 4, pp. 191-193 ("Thompson Apr2004 article")	S.E. Thompson et al.	N/A	April 2004
425-21	"A 90-nm Logic Technology Featuring Strained-Silicon," IEEE Transactions on Electron Devices, vol. 51, no. 11, pp. 1790-1797 ("Thompson Nov2004 article")	S.E. Thompson et al.	N/A	Nov. 2004
425-21	"Record-High Performance 32 nm Node pMOSFET with Advanced Two-Step Recessed SiGe-S/D and Stress Liner Technology," Proceedings of the 2007 IEEE Symposium on VLSI Technology, pp. 48-49 ("Yasutake article")	N. Yasutake et al.	N/A	June 14, 2007

Charted Prior Art Systems			
Exhibit (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
425-01	Intel Pentium D 920 *See generally , e.g.*, Chipworks, "Intel D920 (Presler 65 nm node) 2.8 GHz Dual Core Microprocessor: Structural Analysis," Report ID# SAR-0602-801 (Feb. 17, 2006) (*hereinafter* "D920_Report"); Bai article; Tyagi article; James 65/45 article.	At least by Jan. 16, 2006 Newegg.com had purchased at least one Intel Pentium D 920 and listed it for resale on its website by Oct. 11, 2007.[6]	Intel_425_Product Intel Corp. made and publicized the claimed invention of the '425 patent in the U.S. before the alleged invention date,[7] and then sold products like the Pentium D 920 that embody the claimed invention in the U.S. before the alleged invention date.
425-02	Altera Stratix IV FPGA (e.g., EP4SGX23) *See generally, e.g.*, Chipworks, "Altera Stratix IV TSMC 40 nm Technology Generation: Structural Analysis with TEM Analysis of the I/O Transistor," Report ID# SAR-0902-802 (July 22, 2009) (*hereinafter* "StratixIV_Report"); D. James, "A Trip Down TSMC Memory Lane – Part 2," TechInsights Blog (Jan. 5, 2023) (*hereinafter* "James TSMC article").[8]	At least by Q2 2008[9]	Altera_425_Products

[6] *See, e.g.*, https://web.archive.org/web/20071128142237/http://www newegg.com:80/Product/Product.aspx?Item=N82E16819117149.
[7] *See generally, e.g.*, Bai article; Tyagi article. *See also, e.g.*, "Intel Drives Moore's Law Forward With 65 Nanometer Process Technology," https://web.archive.org/web/20040831235824/http://www.intel.com/pressroom/archive/releases/20040830net.htm (archived Aug. 31, 2004).
[8] *Available at* https://www.techinsights.com/blog/trip-down-tsmc-memory-lane-part-2.
[9] *See, e.g.*, Altera, "Leveraging the 40-nm Process Node to Deliver the World's Most Advanced Custom Logic Devices," https://web.archive.org/web/20091128021000/http://www.altera.com:80/literature/wp/wp-01058-stratix-iv-40nm-process-node-custom-logic-devices.pdf at 1 (archived Nov. 28, 2009) (stating that "Altera announces the world's first 40-nm FPGAs, the Stratix IV device family, and first 40-nm HardCopy IV ASICs" in "Q2 2008"); "Altera Product Catalog," https://web.archive.org/web/20081220145857/http://www.altera.com/literature/sg/product-catalog.pdf at 21-23 (archived Dec. 20, 2008); "Overview of the Stratix IV FPGA Family," https://web.archive.org/web/20090107192206/http://www.altera.com:80/products/devices/stratix-fpgas/stratix-iv/overview/stxiv-overview html (archived Jan. 7, 2009).

In addition, TSMC reserves the right to rely upon at least the following additional prior art to demonstrate the state of the art at the time of the alleged invention the ’425 patent.

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
D. Balobas & N. Konofaos, “Design and Evaluation of 6T SRAM Layout Designs at Modern Nanoscale CMOS Processes,” Proceedings of the 4th International Conference on Modern Circuits and Systems Technologies, (“Balobas article”)	N/A	2015
M. Bohr, “The Invention of Uniaxial Strained Silicon Transistors at Intel,” pp. 1-4 (“Bohr article”)	N/A	Jan. 2007
G. Eneman et al., “Scalability of Stress Induced by Contact-Etch-Stop Layers: A Simulation Study,” IEEE Transactions on Electron Devices, vol. 54, no. 6, pp. 1446-53 (“Eneman article”)	N/A	June 2007
D.M. Fleetwood et al., *Defects in Microelectronic Materials and Devices* (2008) (“Fleetwood”)	N/A	Nov. 19. 2008
T. Ghani et al., “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors,” Technical Digest of the 2003 IEEE International Electron Devices Meeting (“IEDM”), pp. 11.6.1 through 11.6.3. (“Ghani article”)	N/A	Dec. 10, 2003
International Technology Roadmap for Semiconductors: Front End Processes (2007 ed.) (“ITRS_2007_FEP”)	N/A	Aug. 21, 2007
International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures (2007 ed.) (“ITRS_2007_PIDS”)	N/A	Aug. 21, 2007
M. Ishida et al., “A Novel 6T-SRAM Cell Technology Designed with Rectangular Patterns Scalable Beyond 0.18 µm Generation and Desirable for Ultra High Speed Operation,” Technical Digest of the 1998 International Electron Devices Meeting (“IEDM”), pp. 201-204 (“Ishida article”)	N/A	Dec. 9, 1998

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
U.S. Pat. Pub. No. 2006/0246641 to Kammler et al. ("Kammler 641")	Nov. 29, 2005	Nov. 2, 2006
Y.C. Liu et al., "Single Stress Liner for Both NMOS and PMOS Current Enhancement By a Novel Ultimate Spacer Process," Technical Digest of the 2005 IEEE International Electron Devices Meeting (IEDM), pp. 836-839 ("Liu article")	N/A	Dec. 2005
Z. Luo et al., "Design of High Performance PFETs with Strained Si Channel and Laser Anneal," Technical Digest of the 2005 IEEE International Electron Devices Meeting ("IEDM"), pp. 489-492. ("Luo article")	N/A	Dec. 5, 2005
U.S. Pat. Pub. No. 2007/0023832 to Matsui ("Matsui 832")	July 21, 2006	Feb. 1, 2007
P. Morin et al., "Extensive Study of the Correlation between Contact Etch Stop Nitride Material Properties and Negative Bias Temperature Instabilities Measured in pMOSFETS," ECS Transactions, vol. 6, no. 3, pp. 355-369 ("Morin article")	N/A	May 10, 2006
U.S. Pat. No. 6,621,131 to Murthy et al. ("Murthy 131")	Nov. 1, 2001	Sept. 16, 2003
M. Quirk & J. Serda, *Semiconductor Manufacturing Technology* (2001) ("Quirk & Serda")	N/A	Nov. 19, 2000
A. Pavlov & M. Sachdev, *CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test* (2008) ("Pavlov")	N/A	June 21, 2008
J.D. Plummer et al., *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (2000) ("Plummer")	N/A	At least Dec. 31, 2000
Y. Sun et al., "Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 101, Art. No. 104503 (22 pages) ("Sun article")	N/A	May 2007
U.S. Pat. Pub. No. 2007/0090465 to Suzuki et al. ("Suzuki 465")	June 20, 2006	Apr. 26, 2007
U.S. Pat. Pub. No. 2009/0242995 to Suzuki et al. ("Suzuki 995")	June 11, 2009	Oct. 1, 2009

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
S.M. Sze, *Physics of Semiconductor Devices* (2d ed. 1981) ("Sze")	N/A	Sept. 30, 1981
U.S. Pat. Pub. No. 2011/0074498 to Thompson et al. ("Thompson 498")	Feb. 18, 2010	Mar. 31, 2011
S. Thompson et al., "Source/Drain Extension Scaling for 0.1µm and Below Channel Length MOSFETS," Digest of Technical Papers for the 1998 Symposium on VLSI Technology, pp. 132-133 (1998) ("Thompson1998 article")	N/A	June 11, 1998
U.S. Pat. Pub. No. 2007/0228482 to Wei et al. ("Wei 482")	Nov. 9, 2006	Oct. 4, 2007
U.S. Pat. Pub. No. 2008/0203486 to Wiatr et al. ("Waitr 486")	Oct. 3, 2007	Aug. 28, 2008
S. Wolf, *Silicon Processing for the VLSI Era: Volume 4—Deep-Submicron Process Technology* ("Wolf")	N/A	May 2002

B. Invalidity Contentions Pursuant To P.R. 3-3(b)-(c)

Subject to TSMC's reservations of rights, and with respect to each asserted claim of AICP's Infringement Contentions, TSMC provides the following information required by P.R. 3-3(b) and (c).

1. Claim Charts

As set forth in Exhibits 227-01 through 227-13; 764-01 through 764-13; 686-01 through 686-09; 180-01 through 180-15; 076-01 through 076-15; 779-01 through 779-17; and 425-01 through 425-21, and below, each of the charted references, and any products, devices, or processes used in the prior art that embody the subject matter disclosed in the references, invalidates one or more Asserted Claims of the Patents-in-Suit. To the extent any Exhibit concerns or refers to the operation, function, structure, or use of a product, system, or method, TSMC's contentions are based on information and belief.

While TSMC has identified at least one citation per element or limitation for each reference identified in the attached Exhibits, each and every disclosure of the same element or limitation in the same reference is not necessarily identified. TSMC cites exemplary relevant portions of identified references, even where a reference may contain additional disclosure for a particular claim element or limitation, and reserves all rights to rely on other portions of the identified references to support its claims and/or defenses. Any reference to a figure in cited text incorporates by reference the figure itself, and any citation to a figure incorporates by reference any description of that figure in a reference. Similarly, any reference to a cited part or portion of a document encompasses all figures and text within the cited page or portion. Additionally, many of the prior art references are related to, or counterparts of, patent applications and issued patents that contain substantially the same subject matter (e.g., published U.S. patent applications, issued U.S. patents, and foreign applications or issued patents). Any citation to or quotation from any of these patent applications or patents, therefore, should be understood as encompassing any parallel citation to the same subject matter in other related or corresponding applications or patents. Supporting citations in the Invalidity Charts are representative and do not necessarily represent every location where a particular claim element may be found in the prior art reference. TSMC reserves the right to rely on additional, or different, portions of the prior art other than those specifically cited, and to supplement and/or amend these Invalidity Charts.

As noted above, these Invalidity Charts are based on TSMC's understanding of the claim constructions applied by AICP, even though TSMC does not necessarily agree with those constructions and reserves the right to dispute them. To the extent any limitation is deemed not to be met exactly by a prior art reference, TSMC contends that the difference would have been obvious to a person of ordinary skill in the art and within the knowledge of one skilled in the art

at the time of the alleged invention, so that the claimed invention would have been obvious both in light of the single reference alone and/or in light of combined references. TSMC does not admit or concede that the element is not expressly or inherently disclosed by the reference at issue.

Much of the art identified in the attached Invalidity Charts reflects common knowledge and the state of the art at the time of the earliest filing date of the Patents-in-Suit. TSMC may rely on additional citations, references, expert testimony, fact testimony and other corroborating evidence, and other material to provide context and background illustrating the knowledge of a person of ordinary skill in the art at the time of the claimed inventions and/or to aid in understanding the cited portions of the references and/or cited features of the systems. TSMC may also rely on expert testimony explaining relevant portions of references, relevant hardware or software products or systems, and other discovery regarding these subject matters. Additionally, TSMC may rely on other portions of any prior art reference, whether or not identified in the Invalidity Charts, particularly those produced in TSMC's accompanying production, for purposes of explaining the background, general technical subject area, and the knowledge of a person of ordinary skill in the art. In addition, TSMC may rely on any portions of the prior art references that are identified in petitions for *inter partes* review or reexamination for the Patents-in-Suit and/or related patents, as well as any obviousness combinations identified in those documents.

2. Anticipation and Single Reference Obviousness

As set forth in the attached Exhibits and below, the following references anticipate one or more of the Asserted Claims of the Patents-in-Suit by expressly or inherently disclosing each and every limitation of that claim. To the extent AICP contends that any of these references do not expressly or inherently disclose any limitation of any claim, they nevertheless anticipate because a POSITA would at once envisage the claimed arrangement or combination of claim elements. To the extent that AICP contends that any of these references do not anticipate any asserted claim,

TSMC further contends each reference renders the asserted claim obvious either in view of the reference alone or in combination with other references and/or the knowledge of a person of ordinary skill in the art. A corresponding claim chart for each reference is attached hereto as indicated in the "Exh. No." column.

Exh. No	**Prior Art Reference**[10]	**Patents and Claims**
227-01	Matsumoto 135	'227 patent, claims 1, 2, 7, 8, 14
227-02	JP-Kajiyama	'227 patent, claims 1, 2, 7, 8, 14
227-03	Matsumoto 185	'227 patent, claims 1, 2, 7, 8, 14
227-04	Guha	'227 patent, claims 1, 2, 7, 8, 14
227-05	Kubicek	'227 patent, claims 1, 2, 7, 8, 14
227-06	Noguchi	'227 patent, claims 1, 2, 7, 8, 14
227-07	JP-Ono	'227 patent, claims 1, 2, 7, 8, 14
227-08	Paton	'227 patent, claims 1, 2, 7, 8, 14
227-09	Gardner	'227 patent, claims 1, 2, 7, 8, 14
227-10	Ono	'227 patent, claims 1, 2, 7, 8, 14
227-11	Wang 084	'227 patent, claims 1, 2, 7, 8, 14
227-12	Mathew	'227 patent, claims 1, 2, 7, 8, 14
764-01	Matsumoto 135	'764 patent, claims 1-6, 11-19
764-02	JP-Kajiyama	'764 patent, claims 1-6, 11-19
764-03	Matsumoto 185	'764 patent, claims 1-6, 11-19
764-04	Guha	'764 patent, claims 1-6, 11-19
764-05	Kubicek	'764 patent, claims 1-6, 11-19
764-06	Noguchi	'764 patent, claims 1-6, 11-19
764-07	JP-Ono	'764 patent, claims 1-6, 11-19
764-08	Paton	'764 patent, claims 1-6, 11-19
764-09	Gardner	'764 patent, claims 1-6, 11-19
764-10	Ono	'764 patent, claims 1-6, 11-19
764-11	Wang 084	'764 patent, claims 1-6, 11-19
764-12	Mathew	'764 patent, claims 1-6, 11-19
686-01	Intel 686 Products	'686 patent, claims 25-29, 31, 34, 35
686-02	Akasaka 077	'686 patent, claims 25-29, 31, 34, 35
686-03	Akasaka 939	'686 patent, claims 25-29, 31, 34, 35
686-04	Aoyama 950	'686 patent, claims 25-28, 31, 34, 35
686-05	Bohr 559	'686 patent, claims 25-27, 29, 31, 34, 35
686-06	Kavalieros 277	'686 patent, claims 25-28, 31, 34, 35
686-07	Okazaki 789	'686 patent, claims 25-29, 31, 34, 35
686-08	Hsu 660	'686 patent, claims 25-29, 31, 34, 35

[10] To the extent third party discovery shows other prior art systems are anticipatory, TSMC reserves the right to amend these Contentions to specifically identify other anticipatory systems.

Exh. No	Prior Art Reference[10]	Patents and Claims
180-01	Kamata	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-02	Guha	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-03	Matsumoto 135	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-04	Inumiya 763	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-05	Inumiya 355	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-06	Mizushima	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-07	Kubicek	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-08	Vandooren	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-09	Sasaki	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-10	JP-Ono	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-11	Matsumoto 185	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-12	Clevenger	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-13	Wang 084	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
180-14	Ono	’180 patent, claims 1-3, 5, 6, 11, 13, 14, 16-19, 21, 22
076-01	Kamata	’076 patent, claims 1-3, 6-8, 10-13
076-02	Guha	’076 patent, claims 1-3, 6-8, 10-13
076-03	Matsumoto 135	’076 patent, claims 1-3, 6-8, 10-13
076-04	Inumiya 763	’076 patent, claims 1-3, 6-8, 10-13
076-05	Inumiya 355	’076 patent, claims 1-3, 6-8, 10-13
076-06	Mizushima	’076 patent, claims 1-3, 6-8, 10-13
076-07	Kubicek	’076 patent, claims 1-3, 6-8, 10-13
076-08	Vandooren	’076 patent, claims 1-3, 6-8, 10-13
076-09	Sasaki	’076 patent, claims 1-3, 6-8, 10-13
076-10	JP-Ono	’076 patent, claims 1-3, 6-8, 10-13
076-11	Matsumoto 185	’076 patent, claims 1-3, 6-8, 10-13
076-12	Clevenger	’076 patent, claims 1-3, 6-8, 10-13
076-13	Wang 084	’076 patent, claims 1-3, 6-8, 10-13
076-14	Ono	’076 patent, claims 1-3, 6-8, 10-13
779-01	Gilmer	’779 patent, claims 1, 12-15

Exh. No	Prior Art Reference[10]	Patents and Claims
779-02	Chowdhury	’779 patent, claims 1, 12-15
779-03	Torii	’779 patent, claims 1, 12-15
779-04	Lin	’779 patent, claims 1, 12-15
779-05	Hsu	’779 patent, claims 1, 12-15
779-06	Iwamoto	’779 patent, claims 1, 12-15
779-07	Suzuki	’779 patent, claims 1, 12-15
779-08	Irino	’779 patent, claims 1, 12-15
779-09	Fujiwara	’779 patent, claims 1, 12-15
779-10	Hori	’779 patent, claims 1, 12-15
779-11	Greene	’779 patent, claims 1, 12-15
779-12	Luan	’779 patent, claims 1, 12-15
779-13	Intel QX9650	’779 patent, claims 1, 12-15
779-14	Chen	’779 patent, claims 1, 12-15
779-15	Yu	’779 patent, claims 1, 12-15
779-16	Wang	’779 patent, claims 1, 12-15
425-01	Intel 425 Product	’425 patent, claims 1, 3-5, 7, 11
425-02	Altera 425 Products	’425 patent, claims 1, 3-5, 7, 11
425-03	Baik 820	’425 patent, claims 1, 3-5, 7, 11
425-04	Bohr 683	’425 patent, claims 1, 3-5, 7, 11
425-05	Chen 179	’425 patent, claims 1, 3-5, 7, 11
425-06	Chen 729	’425 patent, claims 1, 3-5, 7, 11
425-07	Cheng 810	’425 patent, claims 1, 3-5, 7, 11
425-08	Cheng 817	’425 patent, claims 1, 3-5, 7, 11
425-09	Doris 784	’425 patent, claims 1, 3-5, 7, 11
425-10	Hatada 776	’425 patent, claims 1, 3-5, 7, 11
425-11	Hsu 823	’425 patent, claims 1, 3-5, 7, 11
425-12	James 90nm article	’425 patent, claims 1, 3-5, 7, 11
425-13	Ke 984	’425 patent, claims 1, 3-5, 7, 11
425-14	Lee 870	’425 patent, claims 1, 3-5, 7, 11
425-15	Ogura 844	’425 patent, claims 1, 3-5, 7, 11
425-16	Saito 825	’425 patent, claims 1, 3-5, 7, 11
425-17	Shimamune 398	’425 patent, claims 1, 3-5, 7, 11
425-18	Wang 906	’425 patent, claims 1, 3-5, 7, 11
425-19	Wu 922	’425 patent, claims 1, 3-5, 7, 11
425-20	Yamasaki 170	’425 patent, claims 1, 3-5, 7, 11

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case Nos. IPR2025-00682, IPR2025-00683, IPR2025-00828, IPR2025-00829, IPR2025-00830, IPR2025-00831, and IPR2025-00832 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the Patents-in-Suit.

3. Obviousness

As further set forth in the attached Exhibits and below, each of the charted references, and any products, devices, or processes used in the prior art that embody the subject matter disclosed in the references, anticipates and/or renders obvious one or more Asserted Claims of the Patents-in-Suit. Each of the combinations of prior art references described or identified in Claim Charts and below renders the Asserted Claims of the Patents-in-Suit invalid under 35 U.S.C. § 103 for obviousness. Each prior art reference may be combined with one or more other prior art references to render obvious the Asserted Claims, as explained in more detail below. The disclosures of these references also may be combined with information known to persons skilled in the art at the time of the alleged invention and understood and supplemented in view of the common sense of persons skilled in the art at the time of the alleged invention, including any statements in the intrinsic record of the Patents-in-Suit and related applications.

TSMC expressly intends to combine one or more prior art references identified in the attached Exhibits with each other to address any further contentions from AICP that a particular prior art reference supposedly lacks one or more elements of an Asserted Claim. In other words, TSMC contends that each charted prior art reference can be combined with each other charted prior art reference (individually or in combination) to the extent the prior art reference lacks or does not explicitly disclose an element or feature of an Asserted Claim. The obviousness combinations described below are not to be construed to suggest that any reference included in the combinations is not anticipatory. Further, to the extent that AICP contends that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, TSMC reserves the right to identify other prior art references that, when combined with the anticipatory prior art, would render the claims obvious despite an allegedly missing limitation.

To the extent not explicitly disclosed by the prior art, the Asserted Claims of the Patents-in-Suit are nothing more than a combination of standard, conventional elements already existing and well-known at the time of the purported invention, combined according to known methods to achieve predictable results.

All of the following rationales support a finding of obviousness here:

(a) Combining prior art elements according to known methods to yield predictable results;

(b) Simple substitution of one known element for another to obtain predictable results;

(c) Use of known technique to improve similar devices (methods, or products) in the same way;

(d) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(e) "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(f) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

(g) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

TSMC further contends that the prior art identified in these Contentions is evidence of simultaneous or near-simultaneous independent invention by others of the alleged invention as recited in one or more of the Asserted Claims. TSMC reserves its right to rely on the simultaneous or near-simultaneous independent invention by others as further evidence of the obviousness of the Asserted Claims.

Each limitation of the Asserted Claims was well known to those of ordinary skill in the art before the filing dates of the application to which the Patents-in-Suit claim priority, as detailed below and in the attached charts.

The elements recited in the Asserted Claims are mere combinations and modifications of these well-known elements. A person of ordinary skill in the art would be able, and motivated, to improve the existing technology in the same or similar manner by combining or modifying the individual elements that were already known in the art to yield predictable results.

a. The ’227 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below, and in Exhibits 227-01 through 227-13 would have rendered obvious one or more Asserted Claims of the ’227 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits 227-01 through 227-13, TSMC contends that all asserted claims are rendered obvious by Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, or Mathew alone, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 227-01 through 227-13 and Herein)[11]:
227-01	Matsumoto 135	One or more of Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-02	Kajiyama	One or more of Matsumoto 135, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-03	Matsumoto 185	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-04	Guha	One or more of Matsumoto 135, Kajiyama, Noguchi, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-05	Kubicek	Matsumoto 135, Kajiyama, Noguchi, Guha, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-06	Noguchi	One or more of Matsumoto 135, Kajiyama, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-07	JP-Ono	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe 2004, Watanabe 2003,

[11] To the extent any reference is cited in Exhibits 227-01 to 227-13, but not referenced here, any omission was unintentional and TSMC intends to rely on its identification of any such combinations in Exhibits 227-01 to 227-13.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 227-01 through 227-13 and Herein) [11]:
		Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-08	Paton	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-09	Gardner	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-10	Ono	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-11	Wang 084	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
227-12	Mathew	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’227 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’227 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with

any other of the references in Exhibits 227-01 through 227-13 and/or with a POSITA's general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits 227-01 through 227-13, including for the reasons described below. A POSITA at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the '227 patent relates to a semiconductor device comprising a high dielectric constant gate insulating film formed on an active region in a substrate. The asserted claims recite elements that were conventional in manufacturing transistors well before the priority date of the '227 patent (alleged to be August 5, 2005). A semiconductor device comprising a high dielectric constant gate insulating film formed on an active region in a substrate was well-known prior to the '227 patent. *See, e.g.*, '227 patent, 1:26-52, 5:43-44, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; '227 patent file history, 2008-11-12 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0014], [0015]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102], [0103], [0105], [0107], [0137]-[0138], [0140], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kajiyama at Title, Summary, claims 1, 5, 8, ¶¶ [0001], [0002], [0005], [0013]-[0015], [0027]-[0029], [0045], Figures 1(A)-(D); Noguchi at Title, Abstract, 1:14-17, 3:50-52, 4:35-39, 4:40-52, 4:53-57, 5:23-28, 13:11-15, 13:16-21, Figures 1, 6; Guha at Title, Abstract, ¶¶ [0001], [0021], [0022], [0023], [0026], [0037], [0038], [0043], Figures 10-12, claims 1, 3, 13; Kubicek at Abstract, 1, 2, 4, Figure 1; Paton

at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, claims 1, 8, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], claims 1, 7, Figures 3-6, 33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], claim 1, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Title, Abstract, ¶¶ [0002], [0007]-[0011], [0020]-[0022], [0047]-[0048], [0054]-[0055], claim 1, Figures 2, 5F; Ono at Title, Abstract, ¶¶ [0003], [0007], [0008], [0158], [0160], [0166], claims 1, 8, 13, Figure 4; Mathew at Abstract, 1:7-10, 1:35-2:10, 3:17-40, 4:6-8, 4:15-34, claim 1, Figures 20, 21; Yu at Title, 1:6-10, 1:14-17, 1:17-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004 at Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003 at Title, 19, Figures 1, 11; Lee_2000 at Title, 2.4.1, 2.4.2, Figures 1, 12; Lee_1999 at Title, 6.1.1; Andreoni at Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055], [0056], [0057], Figures 1, 2A, 2B, 2C; Wolf at 145-146, Figures 1-2, 5-25; Wang 672 at Title, Abstract, ¶¶ [0002], [0008], [0009], [0010]-[0012], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044], [0045], [0047], [0048], [0050]-[0052], claim 15, Figure 3; Ahmed at 5:40-61; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4, 5, Figures 1-11; Houssa at 8, 9, 510.

A gate electrode formed on the high dielectric constant gate insulating film was also well-known prior to the ’227 patent. *See, e.g.*, ’227 patent, 1:26-52, 5:43-44, Figures 16A-16B; ’227 patent file history, 2008-11-12 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 10, 13, ¶¶ [0103], [0107]-[0108], [0137]-[0138], Figures 1-4, 10, 13, 19-26; Kajiyama at claims 1, 5, ¶¶ [0014], [0028]-[0029], Figures 1(A)-(D); Noguchi at 4:40-52, 5:6-10, 5:29-43, Figures 1, 6; Guha at ¶¶ [0041], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at

Abstract, 2, Figure 1; Paton at Abstract, 7:31-63, claim 1, Figures 1-5; Matsumoto 185 at ¶¶ [0038], [0046], [0048]-[0049], Figure 33, claim 7; JP-Ono at Abstract, ¶¶ [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0042]-[0043], claim 1, Figures 1-3, 6-10, 19-22, 23; Gardner at Abstract, 2:20-30, 3:39-4:21, 6:19-30, claims 1-3, 10, Figures 1-4, 7; Wang 084 at Abstract, ¶¶ [0008]-[0011], [0020]-[0022], [0024], [0043], [0047]-[0048], [0054]-[0055], claim 1, Figures 2, 5F; Ono at ¶¶ [0160], [0167], claim 1; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:35-56, claim 1, Figures 20, 21; Yu at 3:1-7, Figure 1, Watanabe_2004 at Figures 2, 5, 6; Watanabe_2003 at Figures 1, 11; Andreoni at Abstract, ¶¶ [0028], [0046], [0051], [0057], Figures 1, 2A-2C; Wolf at Figure 1-2, 5-25; Wang 672 at ¶¶ [0011], [0044], [0048], [0051], [0054], Figure 3.

An insulating sidewall formed on each side surface of the gate electrode was also well-known prior to the ’227 patent. *See, e.g.*, ’227 patent, 1:26-52, 5:43-44, Figures 16A-16B; ’227 patent file history, 2008-11-12 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at [Solution method], claims 1, 8, ¶¶ [0014], [0028], [0030], [0031], [0033], [0047], Figures 1(A)-(D); Noguchi at 4:64-5:10, 5:11-14, 6:6-18, 7:21-28, 8:56-64, 9:45-50, 13:25-32, 13:59-61, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0040], [0043]-[0045], Figures 3-6, 10-12, claim 1; Kubicek at 2, Figure 1; Paton at 4:39-57, 7:64-8:11, claim 15, Figures 1-5; Matsumoto 185 at ¶¶ 38, 44, 119-120, Figures 32-33, claim 7; JP-Ono at ¶¶ [0033], [0078]-[0079], [0083]-[0084], claim 3, Figures 19-22, 23; Gardner at 4:26-45, 6:19-30, Figures 3 and 7; Wang 084 at ¶¶ [0010], [0011], [0044], [0049]-[0050], [0055]-[0056]; Ono at ¶ [0181]; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:50-5:47, 6:22-41, 7:5-31, claims 1, 3, Figures 20, 21; Yu at 4:3-9, 4:22-27, 6:49-60, 7:31-39, Figure 1; Watanabe_2004 at 507, Figures 1, 2, 4-6; Watanabe_2003 at 19, Figures 1, 11; Andreoni at 56,

Figures 2A-2C; Wolf at 217, Figure 5-25; Houssa at 510, 511; Wang 672 discloses at ¶ [0049], Figure 3; Mutou at ¶¶ [0047], [0076]-[0077], [0095]-[0096], [0103], [0116], claim 10, Figure 1; Bu at ¶¶ [0019]-[0022], [0026], [0027], [0030], [0035]-[0038], claims 1-2, 5, 9, 15-17, 21, Figure 1D; Ahmed at 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, claims 1, 3-7.

The high dielectric constant gate insulating film continuously formed so as to extend from under the gate electrode to under the insulating sidewall was also well-known prior to the '227 patent. *See, e.g.*, '227 patent file history, 2008-11-12 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0107]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 2, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Ono at ¶¶ [0199], [0215], Figures 13, 80; Mathew at 5:62-6:7, 7:5-31, Figures 11, 17, 20, 21; Houssa at 510; Plummer at 82, 83. By the 2005 priority date of the '227 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the

gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figs. 1-4.)

At least part of the high dielectric constant gate insulating film located under the insulating sidewall having a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode was also well-known prior to the ’227 patent. *See, e.g.*, ’227 patent file history, 2008-11-12 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 10, 11, 13, 14, ¶¶ [0002], [0013]-[0014], [0015]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102]-[0105], [0107]-[0108], [0109-0110], [0114], [0137]-[0141], [0143], [0167], Figures 1-4, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Ono at ¶¶ [0181], [0200], [0202], [0215-0216], Figure 43, 53, 57, 95, 104, 108; Mathew at Figures 20, 21. By the 2005 priority date of the ’227 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figs. 1-4.)

The insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween was also well-known prior to the ’227 patent. *See, e.g.*, ’227 patent, 1:26-52, 5:43-44, Figures 16A-16B; Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at [Solution method], claims 1, 8, ¶¶ [0014], [0028], [0030], [0031], [0033], [0047], Figures 1(A)-(D); Noguchi at 4:64-5:10, 5:11-14, 6:6-18, 7:21-28, 8:56-64, 9:45-50, 13:25-32, 13:59-61, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0040], [0043]-[0045], Figures 3-6, 10-12, claim 1; Kubicek at 1, Figure 1; Paton at 4:39-57, 7:64-8:11, claim 15, Figures 1-5; Matsumoto 185 at ¶¶ [0038], [0044], [0119]-[0120], Figures 32-33, claim 7; JP-Ono at ¶¶ [0033], [0078]-[0079], [0083]-[0084], claim 3, Figures 19-22, 23; Gardner at 4:26-45, 6:19-30, Figures 3 and 7; Wang 084 at ¶¶ [0010], [0011], [0044], [0049]-[0050], [0055]-[0056]; Ono at ¶ [0181]; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:50-5:47, 6:22-41, 7:5-31, claims 1, 3, Figures 20, 21; Yu at 4:3-9, 4:22-27, 6:49-60, 7:31-39, Figure 1; Watanabe_2004 at 507, Figures 1, 2, 4-6; Watanabe_2003 at 19, Figures 1, 11; Andreoni at 56, Figures 2A-2C; Wolf at 217, Figure 5-25; Houssa at 510, 511; Wang 672 at ¶ [0049], Figure 3; Mutou at ¶¶ [0047], [0076]-[0077], [0095]-[0096], [0103], [0116], claim 10, Figure 1; Bu at ¶¶ [0019]-[0022], [0026], [0027], [0030], [0035]-[0038], claims 1-2, 5, 9, 15-17, 21, Figure 1D; Ahmed at 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, claims 1, 3-7.

The high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall was also well-known prior to the ’227 patent. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-

10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Ono at ¶¶ [0199], [0215], Figure 13; Mathew at 5:62-6:7, 7:5-31, Figures 11, 17, 20, 21; Houssa at 510; Plummer at 82, 83. By the 2005 priority date of the ’227 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figs. 1-4.)

Part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode was also well-known prior to the ’227 patent. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1;

Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Ono at ¶¶ [0181], [0199], [0200], [0202], [0215-0216], Figures 13, 43, 53, 57; Mathew at Figures 20, 21.

The high dielectric constant gate insulating film formed so as not to be located under the second insulating sidewall was also well-known prior to the ’227 patent. *See, e.g.*, ’227 patent, 1:26-52, 5:43-44, Figures 16A-16B; Matsumoto 135 at ¶¶ [0137]-[0141], 143, Figures 19-26; Kajiyama at ¶¶ 29-31, Figures 1(A)-(D); Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1; Matsumoto 185 at Title, Abstract, ¶¶ 1, 10, 11, 12, 38, 42-45, 119-120, claims 1, 7, Figures 3-6, 32-33; Gardner at 4:26-45, 6:19-30, Figures 3 and 7; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Ono at ¶¶ [0181], [0199], [0200], [0202], [0215-0216], Figures 13, 43, 53, 57; Mathew at Figures 20, 21.

A buffer insulating film between the substrate and the high dielectric constant gate insulating film was also well-known prior to the ’227 patent. *See, e.g.*, Guha at ¶¶ [0037], [0043], Figure 12, claim 11; Kubicek at 2, Figure 1; Wang 084 at ¶¶ [0032], [0034], [0048], [0055], claim 2, Figures 2, 5F; Ono at ¶ [0160], Figure 4; Yu at 3:59-4:2, 6:29-33, Figure 1; Sim at 219, Figure 1; Watanabe_2004 at 510, Figure 5; Watanabe_2003 at 19, Figures 1-4, 11; Houssa at 8-9; Andreoni at ¶¶ [0001], [0008], [0010], [0028], [0032]-[0035], [0040], [0049], [0056], [0057],

Figure 1, 2A-2C; Wang 672 at Abstract, ¶¶ [0002], [0003], [0008], [0009], [0011], [0022]-[0024], [0027], [0028], [0041], [0043], [0044], [0048], claim 15, Figure 3; Mutou at Abstract, ¶¶ [0020], [0041], [0042], [0053]-[0055], [0110]-[0112], claims 1, 10, 12, 19, 20, Figures 1-11; Lo at 3:34-37, 3:45-48, Fig. 7; Parker at 1:20-26, 1:33-42, 2:30-3:6, claims 1-3, 11.

The buffer insulating film being a silicon oxide film or a silicon oxynitride film was also well-known prior to the ’227 patent. *See, e.g.*, Guha at ¶ [0037], Figure 12; Kubicek at 2; Ono at ¶ [0160], Figure 4; Yu at 4:56-67; Watanabe_2004 at 510, Figure 5, Watanabe_2003 at 19; Houssa at 8, 9; Andreoni at ¶¶ [0001], [0008]; Wang 672 at ¶ [0048]; Mutou at ¶¶ [0042], [0053], [0110]; Lo at 3:40-43, 3:45-48, claim 8. By the 2005 priority date of the ’227 patent, a POSITA would have been motivated to include a buffer insulating film between the substrate and the high dielectric constant gate insulating film in a semiconductor device in light of the known benefits of a buffer insulating film, including, for example, suppressing the “deterioration of an interface between a substrate and a gate insulating film” caused by chemical interactions between the high-k material and the silicon substrate. (’227 patent, 12:9-15; *see also, e.g.*, Wang 672, ¶ [0003].) It was also known that a buffer insulating film between the substrate and the high-k gate insulating film improves carrier mobility and provides higher device reliability. (*See, e.g.*, Wang 672, ¶ [0028].) By the 2005 priority date of the ’227 patent, a POSITA would also have been motivated to use a silicon oxide film or a silicon oxynitride film as a buffer insulating film. For example, silicon oxide had already been used for decades in the semiconductor industry; a POSITA therefore would have been very familiar with its properties and the processes for depositing silicon oxide on a device. Furthermore, a POSITA would have known that silicon oxide or silicon oxynitride is a better-suited material for interfacing with the silicon substrate than a high-k material used for the gate insulating film.

The high dielectric constant gate insulating film formed of a Hf based oxide was also well-known prior to the ’227 patent. *See, e.g.*, Kajiyama at ¶ 45; Guha at ¶¶ [0038], [0043]; Kubicek at Title, Abstract, 2, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, claims 1, 8, Figures 1-5; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Wang 084 at ¶¶ [0023], [0035], claim 6; Ono at ¶ [0166], claim 8; Mathew at 4:15-25; Yu at 3:14-33; Sim at 218; Watanabe_2004 at Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003 at Title, 19, Figures 1, 11; Lee_1999 at 6.1.1; Lee_2000 at Title, 2.4.1, 2.4.2, Figures 1, 12; Houssa at 8, 9; Andreoni at ¶¶ [0037], [0039]; Wang 672 at Abstract, ¶¶ [0009], [0012], [0025], [0034], [0045], claim 23; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4-5; Lo at 3:50-60; Chau 209 at 2:6-14; Chau 210 at 2:9-23; Parker at 2:50-60, claim 4. By the 2005 priority date of the ’227 patent, a POSITA would have been motivated to use a Hf-based oxide, e.g., HfO2, as the material for a gate insulating film in a semiconductor device. By that time, as semiconductor devices continued to shrink in size, the industry had already been searching for high-k material replacements for SiO2 as the gate insulating film. A POSITA would have known that Hf based oxides, such as HfO2, have a high dielectric constant (25 for HfO2). (*See, e.g.*, Wilk, Table I.) Moreover, based on research and studies that had been conducted over the years, a POSITA would have known by the 2005 priority date of the ’227 patent that HfO2 has multiple known benefits, including, for example, superior thermal stability, reasonable band alignment, and ability to scale down to a smaller EOT. (*See, e.g.*, Lee-2000, 2.4.1; Houssa, 207; Lee-1999, 6.1.2.)

Additional motivations to combine may be found in the ’227 patent invalidity charts.

In sum, by the time the application for the ’227 patent was filed, it was well known to design a semiconductor device as claimed at least because all the above was well known in the art before the ’227 patent, and a POSITA would have known that any and/or all the above techniques could be combined to fabricate a semiconductor device with a high dielectric constant gate insulating film formed on an active region in a substrate, a gate electrode formed on the high dielectric constant gate insulating film, an insulating sidewall formed on each side surface of the gate electrode, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode. This is especially true here because all of the references disclose a semiconductor device with sidewalled transistors even if they do not disclose every aspect of a semiconductor device design. As such, a POSITA would have logically and predictably consulted all of the references together to design a complete semiconductor device with the claimed sidewalled transistors. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known semiconductor device designs to create different semiconductor devices

with the claimed sidewalled transistors. Because all of these techniques were already known in the art for use in fabrication of semiconductor devices, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a semiconductor device, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits 227-01 through 227-13, a POSITA would have been motivated to combine any of the references identified as prior art to the ’227 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar semiconductor device designs with sidewalled transistors (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Matsumoto 135 at Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0014], [0015]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102], [0103], [0105], [0107], [0137]-[0138], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kajiyama at Title, Summary, claims 1, 5, 8, ¶¶ [0001], [0002], [0005], [0013]-[0015], [0027]-[0029], [0045], Figures 1(A)-(D); Noguchi at Title, Abstract, 1:14-17, 3:50-52, 4:35-39, 4:40-52, 4:53-57, 5:23-28, 13:11-15, 13:16-21, Figures 1, 6; Guha at Title, Abstract, ¶¶ [0001], [0021], [0022], [0023], [0026], [0037], [0038], [0043], Figures 10-12, claims 1, 3, 13; Kubicek at Abstract, 1, 4, Figure 1;

Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, claims 1, 8, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], claims 1, 7, Figures 3-6, 33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], claim 1, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Title, Abstract, ¶¶ [0002], [0007]-[0011], [0020]-[0022], [0047]-[0048], [0054]-[0055], claim 1, Figures 2, 5F; Ono at Title, Abstract, ¶¶ [0003], [0007], [0008], [0158], [0160], [0166], claims 1, 8, 13, Figure 4; Mathew at Abstract, 1:7-10, 1:35-2:10, 3:17-40, 4:6-8, 4:15-34, claim 1, Figures 20, 21; Yu at Title, 1:6-10, 1:14-17, 1:17-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004 at Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003 at Title, 19, Figures 1, 11; Lee_2000 at Title, 2.4.1, 2.4.2, Figures 1, 12; Lee_1999 at Title, 6.1.1; Andreoni at Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055], [0056], [0057], Figures 1, 2A, 2B, 2C; Wolf at 145-146, Figures 1-2, 5-25; Wang 672 at Title, Abstract, ¶¶ [0002], [0008], [0009], [0010]-[0012], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044], [0045], [0047], [0048], [0050]-[0052], claim 15, Figure 3; Ahmed at 5:40-61; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4, 5, Figures 1-11; Houssa at 8, 9, 510.

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, a high dielectric constant gate insulating film continuously formed so as to extend from under the gate electrode to under the insulating sidewall—to other references that relate to semiconductor device designs generally because all references teach designing transistors with particular technical specifications suitable for different purposes in semiconductor devices, and it would have been a trivial exercise to consult the references that

taught more specific semiconductor device designs to fill in less specific disclosures in other references. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ 1, 10, 11, 12, 38, 42-45, 119-120, claims 1, 7, Figures 3-6, 32-33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Ono at ¶¶ [0199], [0215], Figure 13; Mathew at 5:62-6:7, 7:5-31, Figures 11, 17, 20, 21; Houssa at 510; Plummer at 82, 83.

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular semiconductor device with the teachings regarding other materials, components, and configurations used in other semiconductor devices for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques for designing semiconductor devices existed. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose:

fabricating a semiconductor device with sidewalled transistors. This is thus a combination of prior art elements (*e.g.*, a high dielectric constant gate insulating film formed on an active region in a substrate, a gate electrode formed on the high dielectric constant gate insulating film, an insulating sidewall formed on each side surface of the gate electrode, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of semiconductor fabrication were all well-known at the time. Implementing the combination and

any necessary modifications would have been routine and within the scope of the prior art references' teachings.

Additional obviousness combinations of the references identified here are possible, and TSMC may rely on such combination(s) in this litigation. In particular, TSMC is currently unaware of AICP's allegations with respect to the level of skill in the art and the qualifications of a POSITA. TSMC is also unaware of the extent, if any, to which AICP may contend that limitations of the claims at issue are not disclosed in the prior art identified by TSMC as anticipatory, and the extent to which AICP will contend that elements not disclosed in the asserted patent specifications would have been known to a POSITA. And TSMC does not yet know how the Court will construe terms in the asserted claim. TSMC is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. TSMC reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case No. IPR2025-00828 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the '227 patent.

b. The '764 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant's Admitted Prior Art, and/or the additional prior art references discussed below, and in Exhibits 764-01 through 764-13 would have rendered obvious one or more Asserted Claims of the '764 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would

have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits 764-01 through 764-13, TSMC contends that all asserted claims are rendered obvious by Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, or Mathew alone, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exh. No.	**Primary Reference**	**In Combination With One or More of the Following (As Described in Exhibits 764-01 through 764-13 and Herein)** [12]**:**
764-01	Matsumoto 135	One or more of Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-02	Kajiyama	One or more of Matsumoto 135, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-03	Matsumoto 185	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe 2004, Watanabe 2003, Lee 1999,

[12] To the extent any reference is cited in Exhibits 764-01 to 764-13, but not referenced here, any omission was unintentional and TSMC intends to rely on its identification of any such combinations in Exhibits 764-01 to 764-13.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 764-01 through 764-13 and Herein) [12]:
		Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-04	Guha	One or more of Matsumoto 135, Kajiyama, Noguchi, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-05	Kubicek	Matsumoto 135, Kajiyama, Noguchi, Guha, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-06	Noguchi	One or more of Matsumoto 135, Kajiyama, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-07	JP-Ono	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-08	Paton	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-09	Gardner	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Wang 084, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-10	Ono	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe 2003, Lee 1999, Lee 2000, Andreoni, Wolf,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 764-01 through 764-13 and Herein) [12]:
		Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-11	Wang 084	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Ono, Mathew, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker
764-12	Mathew	Matsumoto 135, Kajiyama, Noguchi, Guha, Kubicek, Paton, Matsumoto 185, JP-Ono, Gardner, Wang 084, Ono, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang 672, Bu, Ahmed, Lo, Chau 209, Chau 210, and Parker

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’764 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’764 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits 764-01 through 764-13 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits 764-01 through 764-13, including for the reasons described below. A POSITA at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’764 patent relates to a semiconductor device comprising a high dielectric constant gate insulating film formed on an active region in a substrate. The asserted

claims recite elements that were conventional in manufacturing transistors well before the priority date of the ’764 patent (alleged to be August 5, 2005). A semiconductor device comprising a high dielectric constant gate insulating film formed on an active region in a substrate was well-known prior to the ’764 patent. *See, e.g.*, ’764 patent, 1:32-57, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’764 patent file history, 2010-08-03 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0014], [0015]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102], [0103], [0105], [0107], [0137]-[0138], [0140], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kajiyama at Title, Summary, claims 1, 5, 8, ¶¶ [0001], [0002], [0005], [0013]-[0015], [0027]-[0029], [0045], Figures 1(A)-(D); Noguchi at Title, Abstract, 1:14-17, 3:50-52, 4:35-39, 4:40-52, 4:53-57, 5:23-28, 13:11-15, 13:16-21, Figures 1, 6; Guha at Title, Abstract, ¶¶ [0001], [0021], [0022], [0023], [0026], [0037], [0038], [0043], Figures 10-12, claims 1, 3, 13; Kubicek at Abstract, 1, 2, 4, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, claims 1, 8, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], claims 1, 7, Figures 3-6, 33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], claim 1, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Title, Abstract, ¶¶ [0002], [0007]-[0011], [0020]-[0022], [0047]-[0048], [0054]-[0055], claim 1, Figures 2, 5F; Ono at Title, Abstract, ¶¶ [0003], [0007], [0008], [0158], [0160], [0166], claims 1, 8, 13, Figure 4; Mathew at Abstract, 1:7-10, 1:35-2:10, 3:17-40, 4:6-8, 4:15-34, claim 1, Figures 20, 21; Yu at Title, 1:6-10, 1:14-17, 1:17-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004 at Title, Abstract, 507,

Figures 2, 5, 21; Watanabe_2003 at Title, 19, Figures 1, 11; Lee_2000 at Title, 2.4.1, 2.4.2, Figures 1, 12; Lee_1999 at Title, 6.1.1; Andreoni at Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055], [0056], [0057], Figures 1, 2A, 2B, 2C; Wolf at 145-146, Figures 1-2, 5-25; Wang 672 at Title, Abstract, ¶¶ [0002], [0008], [0009], [0010]-[0012], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044], [0045], [0047], [0048], [0050]-[0052], claim 15, Figure 3; Ahmed at 5:40-61; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4, 5, Figures 1-11; Houssa at 8, 9, 510.

A gate electrode formed on the high dielectric constant gate insulating film was also well-known prior to the ’764 patent. *See, e.g.*, ’764 patent, 1:32-57, 5:48-49, Figures 16A-16B; ’764 patent file history, 2010-08-03 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 10, 13, ¶¶ [0103], [0107]-[0108], [0137]-[0138], Figures 1-4, 10, 13, 19-26; Kajiyama at claims 1, 5, ¶¶ [0014], [0028]-[0029], Figures 1(A)-(D); Noguchi at 4:40-52, 5:6-10, 5:29-43, Figures 1, 6; Guha at ¶¶ [0041], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at Abstract, 2, Figure 1; Paton at Abstract, 7:31-63, claim 1, Figures 1-5; Matsumoto 185 at ¶¶ [0038], [0046], [0048]-[0049], Figure 33, claim 7; JP-Ono at Abstract, ¶¶ [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0042]-[0043], claim 1, Figures 1-3, 6-10, 19-22, 23; Gardner at Abstract, 2:20-30, 3:39-4:21, 6:19-30, claims 1-3, 10, Figures 1-4, 7; Wang 084 at Abstract, ¶¶ [0008]-[0011], [0020]-[0022], [0024], [0043], [0047]-[0048], [0054]-[0055], claim 1, Figures 2, 5F; Ono at ¶¶ [0160], [0167], claim 1; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:35-56, claim 1, Figures 20, 21; Yu at 3:1-7, Figure 1, Watanabe_2004 at Figures 2, 5, 6; Watanabe_2003 at Figures 1, 11; Andreoni at Abstract, ¶¶ [0028], [0046], [0051], [0057], Figures 1, 2A-2C; Wolf at Figure 1-2, 5-25; Wang 672 at ¶¶ [0011], [0044], [0048], [0051], [0054], Figure 3.

A first insulating sidewall formed on each side surface of the gate electrode was also well-known prior to the ’764 patent. *See, e.g.*, ’764 patent, 1:32-57, 5:48-49, Figures 16A-16B; ’764 patent file history, 2010-08-03 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at [Solution method], claims 1, 8, ¶¶ [0014], [0028], [0030], [0047], Figures 1(A)-(B); Noguchi at 4:64-5:10, 5:11-14, 6:6-18, 7:21-28, 8:56-64, 9:45-50, 13:25-32, 13:59-61, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0040], [0043]-[0045], Figures 3-6, 10-12, claim 1; Kubicek at 2, Figure 1; Paton at 4:39-57, 7:64-8:11, claim 15, Figures 1-5; Matsumoto 185 at ¶¶ [0038], [0044], [0119]-[0120], Figures 32-33, claim 7; JP-Ono at ¶¶ [0033], [0078]-[0079], [0083]-[0084], claim 3, Figures 19-22, 23; Gardner at 4:26-45, 6:19-30, Figures 3, 7; Wang 084 at ¶¶ [0010], [0011], [0044], [0049]-[0050], [0055]-[0056]; Ono at ¶ [0181]; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:50-5:47, 6:22-41, 7:5-31, claims 1, 3, Figures 20, 21; Yu at 4:3-9, 4:22-27, 6:49-60, 7:31-39, Figure 1; Watanabe_2004 at 507, Figures 1, 2, 4-6; Watanabe_2003 at 19, Figures 1, 11; Andreoni at 56, Figures 2A-2C; Wolf at 217, Figure 5-25; Houssa at 510, 511; Wang 672 discloses at ¶ [0049], Figure 3; Mutou at ¶¶ [0047], [0076]-[0077], [0095]-[0096], [0103], [0116], claims 10, 12, 19, 20, Figure 1; Bu at ¶¶ [0019]-[0022], [0026], [0027], [0030], [0035]-[0038], claims 1-2, 5, 9, 15-17, 21, Figure 1D; Ahmed at 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, claims 1, 3-7, Figure 3, 5E, 5F.

A second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween was also well-known prior to the ’764 patent. *See, e.g.*, ’764 patent, 1:32-57, 5:48-49, Figures 16A-16B; ’764 patent file history, 2010-08-03 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143],

Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at [Solution method], claims 1, 8, ¶¶ [0014], [0028], [0029], [0031], [0033], Figures 1(A)-(C); Noguchi at 4:64-5:10, 5:11-14, 6:6-18, 7:21-28, 8:56-64, 9:45-50, 13:25-32, 13:59-61, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0040], [0043]-[0045], Figures 3-6, 10-12, claim 1; Kubicek at 1, Figure 1; Paton at 4:39-57, 7:64-8:11, claim 15, Figures 1-5; Matsumoto 185 at ¶¶ [0038], [0044], [0119]-[0120], Figures 32-33, claim 7; JP-Ono at ¶¶ [0033], [0078]-[0079], [0083]-[0084], claim 3, Figures 19-22, 23; Gardner at 4:26-45, 6:19-30, Figures 3, 7; Wang 084 at ¶¶ [0010], [0011], [0044], [0049]-[0050], [0055]-[0056]; Ono at [0181]; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:50-5:47, 6:22-41, 7:5-31, claims 1, 3, Figures 20, 21; Yu at 4:3-9, 4:22-27, 6:49-60, 7:31-39, Figure 1; Watanabe_2004 at 507, Figures 1, 2, 4-6; Watanabe_2003 at 19, Figures 1, 11; Andreoni at 56, Figures 2A-2C; Wolf at 217, Figure 5-25; Houssa at 510, 511; Wang 672 discloses at ¶ [0049], Figure 3; Mutou at ¶¶ [0047], [0076]-[0077], [0095]-[0096], [0103], [0116], claims 10, 12, 19, 20, Figure 1; Bu at ¶¶ [0019]-[0022], [0026], [0027], [0030], [0035]-[0038], claims 1-2, 5, 9, 15-17, 21, Figure 1D; Ahmed at 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, claims 1, 3-7, Figure 3, 5E, 5F.

The high dielectric constant gate insulating film continuously formed so as to extend from under the gate electrode to under the insulating sidewall was also well-known prior to the ’764 patent. *See, e.g.*, ’764 patent file history, 2010-08-03 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0107]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 2, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012],

[0038], [0042-45], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Ono at ¶¶ [0199], [0215], Figures 13, 80; Mathew at 5:62-6:7, 7:5-31, Figures 11, 17, 20, 21; Houssa at 510; Plummer at 82, 83. By the 2005 priority date of the ’764 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (*See, e.g.*, JP-Ono, ¶¶ [0029]-[0035], Figs. 1-4.)

Part of the high dielectric constant gate insulating film located under the first insulating sidewall having a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode was also well-known prior to the ’764 patent. *See, e.g.*, ’764 patent file history, 2010-08-03 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 10, 11, 13, 14, ¶¶ [0002], [0013]-[0014], [0015]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102]-[0105], [0107]-[0108], [0109]-[0110], [0114], [0137]-[0141], [0143], [0167], Figures 1-4, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012],

[0038], [0042]-[0045], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Ono at ¶¶ [0181], [0200], [0202], [0215-0216], Figure 43, 53, 57, 95, 104, 108; Mathew at Figures 20, 21. By the 2005 priority date of the ’764 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (*See, e.g.*, JP-Ono, ¶¶ [[0029]-[0035], Figs. 1-4.)

A buffer insulating film between the substrate and the high dielectric constant gate insulating film was also well-known prior to the ’764 patent. *See, e.g.*, Guha at ¶¶ [0037], [0043], Figure 12, claim 11; Kubicek at 2, Figure 1; Wang 084 at ¶¶ [0032], [0034], [0048], [0055], claim 2, Figures 2, 5F; Ono at ¶ [0160], Figure 4; Yu at 3:59-4:2, 6:29-33, Figure 1; Sim at 219, Figure 1; Watanabe_2004 at 510, Figure 5; Watanabe_2003 at 19, Figures 1-4, 11; Houssa at 8-9; Andreoni at ¶¶ [0001], [0008], [0010], [0028], [0032]-[0035], [0040], [0049], [0056], [0057], Figure 1, 2A-2C; Wang 672 at Abstract, ¶¶ [0002], [0003], [0008], [0009], [0011], [0022]-[0024], [0027], [0028], [0041], [0043], [0044], [0048], claim 15, Figure 3; Mutou at Abstract, ¶¶ [0020], [0041], [0042], [0053]-[0055], [0110]-[0112], claims 1, 10, 12, 19, 20, Figures 1-11; Lo at 3:34-37, 3:45-48, Fig. 7; Parker at 1:20-26, 1:33-42, 2:30-3:6, claims 1-3, 11.

The buffer insulating film being a silicon oxide film was also well-known prior to the ’764 patent. *See, e.g.*, Guha at ¶ [0037], Figure 12; Kubicek at 2; Ono at ¶ [0160], Figure 4; Yu at 4:56-67; Watanabe_2004 at 510, Figure 5, Watanabe_2003 at 19; Houssa at 8, 9; Andreoni at ¶¶ [0001],

[0008]; Wang 672 at ¶ [0048]; Mutou at ¶¶ [0042], [0053], [0110]; Lo at 3:45-48; Parker at 3:40-43, claim 8. By the 2005 priority date of the ’764 patent, a POSITA would have been motivated to include a buffer insulating film between the substrate and the high dielectric constant gate insulating film in a semiconductor device in light of the known benefits of a buffer insulating film, including, for example, suppressing the “deterioration of an interface between a substrate and a gate insulating film” caused by chemical interactions between the high-k material and the silicon substrate. (’764 patent, 12:9-18; *see also, e.g.*, Wang 672, ¶ [0003].) It was also known that a buffer insulating film between the substrate and the high-k gate insulating film improves carrier mobility and provides higher device reliability. (*See, e.g.*, Wang 672, ¶ [0028].) By the 2005 priority date of the ’764 patent, a POSITA would also have been motivated to use a silicon oxide film as a buffer insulating film. For example, silicon oxide had already been used for decades in the semiconductor industry; a POSITA therefore would have been very familiar with its properties and the processes for depositing silicon oxide on a device. Furthermore, a POSITA would have known that silicon oxide is a better-suited material for interfacing with the silicon substrate than a high-k material used for the gate insulating film.

The first insulating sidewall being an offset sidewall was also well-known prior to the ’764 patent. *See, e.g.*, ’764 patent, 1:32-57, 5:48-49, Figures 16A-16B; ’764 patent file history, 2010-08-03 Non-Final Rejection at 2-3; *see also, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0155], [0157], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at [Solution method], claims 1, 8, ¶¶ [0014], [0028], [0030], [0047], Figures 1(A)-(B); Noguchi at 4:64-5:10, 5:11-14, 6:6-18, 7:21-28, 8:56-64, 9:45-50, 13:25-32, 13:59-61, Figures 1, 6; Guha at ¶¶ [0028], [0034], [0035], [0040], [0043]-[0045], Figures 3-6, 10-12, claim 1; Kubicek at 1, Figure 1; Matsumoto 185 at ¶¶ [0038], [0044],

[0119]-[0120], Figures 32-33, claim 7; Wang 084 at ¶¶ [0010], [0011], [0044], [0049]-[0050], [0055]-[0056]; Ono at ¶ [0181]; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:50-5:47, 6:22-41, 7:5-31, claims 1, 3, Figures 20, 21; Yu at 4:3-9, 4:22-27, 6:49-60, 7:31-39, Figure 1; Watanabe_2004 at 507, Figures 1, 2, 4-6; Watanabe_2003 at 19, Figures 1, 11; Andreoni at 56, Figures 2A-2C; Wolf at 217, Figure 5-25; Houssa at 510, 511; Wang 672 discloses at ¶ [0049], Figure 3; Mutou at ¶¶ [0047], [0076]-[0077], [0095]-[0096], [0103], [0116], claims 10, 12, 19, 20, Figures 1-11; Bu at ¶¶ [0019]-[0022], [0026], [0027], [0030], [0035]-[0038], claims 1-2, 5, 9, 15-17, 21, Figure 1D; Ahmed at 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, claims 1, 3-7, Figures 3, 5E, 5F.

The high dielectric constant gate insulating film formed so as not to be located under the second insulating sidewall was also well-known prior to the ’764 patent. *See, e.g.*, ’764 patent, 1:32-57, 5:48-49, Figures 16A-16B; Matsumoto 135 at ¶¶ [0137]-[0141], 143, Figures 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Guha at ¶¶ [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; Gardner at 4:26-45, 6:19-30, Figures 3 and 7; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Ono at ¶¶ [0181], [0199], [0200], [0202], [0215-0216], Figures 13, 43, 53, 57; Mathew at Figures 20, 21.

The high dielectric constant gate insulating film formed of a Hf based oxide was also well-known prior to the ’764 patent. *See, e.g.*, Kajiyama at ¶ [0045]; Guha at ¶¶ [0038], [0043]; Kubicek at Title, Abstract, 2, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, claims 1, 8, Figures 1-5; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Wang 084 at ¶¶ [0023], [0035], claim 6; Ono at ¶ [0166], claim 8;

Mathew at 4:15-25; Yu at 3:14-33; Sim at 218; Watanabe_2004 at Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003 at Title, 19, Figures 1, 11; Lee_1999 at 6.1.1; Lee_2000 at Title, 2.4.1, 2.4.2, Figures 1, 12; Houssa at 8, 9; Andreoni at ¶¶ [0037], [0039]; Wang 672 at Abstract, ¶¶ [0009], [0012], [0025], [0034], [0045], claim 23; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4-5; Lo at 3:50-60; Chau 209 at 2:6-14; Chau 210 at 2:9-23; Parker 2:50-60, claim 4. By the 2005 priority date of the ’764 patent, a POSITA would have been motivated to use a Hf-based oxide, e.g., HfO2, as the material for a gate insulating film in a semiconductor device. By that time, as semiconductor devices continued to shrink in size, the industry had already been searching for high-k material replacements for SiO2 as the gate insulating film. A POSITA would have known that Hf based oxides, such as HfO2, have a high dielectric constant (25 for HfO2). (See, e.g., Wilk, Table I.) Moreover, based on research and studies that had been conducted over the years, a POSITA would have known by the 2005 priority date of the ’764 patent that HfO2 has multiple known benefits, including, for example, superior thermal stability, reasonable band alignment, and ability to scale down to a smaller EOT. (*See, e.g.*, Lee-2000, 2.4.1; Houssa, 207; Lee-1999, 6.1.2.)

Each side end portion of the high dielectric constant gate insulating film having a thickness of 2 nm or less was also well-known prior to the ’764 patent. *See, e.g.*, Mathew at 4:14-15, Figures 20, 21; Sim at 218-221; Wang ’672 at ¶¶ [0026], [0034], claim 6; Lo at 3:50-60; Chau 209 at 2:21-35, claims 10, 17; Chau 210 at 2:24-39; claims 1, 8; Parker at 1:20-26, 3:6-11, claims 4, 12. By the 2005 priority date of the ’764 patent, a POSITA would have been motivated to reduce the thickness of a high-k gate insulating film made of, e.g., HfO2, to 2 nm or less, as it was known that reducing the thickness of HfO_2 to below 20Å (2 nm) enhances mobility and reduces charge

trapping, key issues in ensuring the performance and scalability of semiconductor devices. (Sim, 219, 221.)

A side surface of the high dielectric constant gate insulating film located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode was also well-known prior to the ’764 patent. *See, e.g.*, Guha at ¶¶ [0035], [0040], [0043]-[045], Figure 1, claims 1, 13; Kubicek at 1, Figure 1; JP-Ono at Abstract, ¶¶ [0013], [0018]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083], [0084], claims 1, 3, Figures 1, 2, 6-10, 19-23; Ono at ¶¶ [0181], [0199], [0215], Figure 13; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], 20-22, 44, 47-50, 54-56, Figures 2, 5F; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:50-5:47, 5:62-6:7, 6:22-41, 7:5-31, claims 1, 3, Figures 11, 17, 20, 21.

A side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall was also well-known prior to the ’764 patent. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 10, 11, 13, ¶¶ [0032], [0034], [0038], [0064], [0102]-[0104], [0105], [0107], [0109], [0110], [0114], [0137]-[0141], [0167], Figures 1, 2, 4, 10, 13, 19-26; Matsumoto 185 at Abstract, ¶¶ [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32, 33, claim 7; Guha at ¶¶ [0035], [0040], [0043]-[045], Figure 1, claims 1, 13; Kubicek at 1, Figure 1; JP-Ono at Abstract, ¶¶ [0013], [0018]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083], [0084], claims 1, 3, Figures 1, 2, 6-10, 19-23; Gardner at Title, Abstract, 2:20-30, 3:39-4:21, 4:26-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-4, 7; Ono at Abstract, ¶¶ [0008], [0158], [0160], [0181], [0199], [0215], Figures 4, 13, claim 8; Wang 084 at Title, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], claim 1, Figures 2, 5F; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:6-8, 4:15-34, 4:50-5:47, 5:62-6:7, 6:22-41, 7:5-31, claims 1, 3, Figures 11, 17, 20, 21.

The second insulating sidewall having a double layer structure including an oxide film and a nitride film was also well-known prior to the ’764 patent. *See, e.g.*, Matsumoto 135 at Abstract, ¶¶ [0034], [0038], [0040], [0064], [0103], [0104], [0109], [0110], [0114], [0137]-[0141], [0143]; Figures 1-2, 5-6, 9-10, 13, 19-26, claims 1, 11, 13, 14; Wang 084 at ¶ [0038]; Mathew at 4:50-5:47, 6:22-41, 7:5-31, Figures 20, 21; Bu at ¶¶ [0019]-[0022], [0026], [0027], [0030], [0035]-[0038], claims 1, 2, 5, 9, 15-17, 21, Figure 1D; Ahmed at 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, claims 1, 3-7.

The second insulating sidewall having a triple layer structure including a first oxide film, a nitride film and a second oxide film was also well-known prior to the ’764 patent. *See, e.g.*, Bu at ¶¶ [0019]-[0022], [0026], [0027], [0030], [0035]-[0038], claims 1, 2, 5, 9, 15-17, 21, Figure 1D; Matsumoto 135 at Abstract, ¶¶ [0034], [0038], [0040], [0064], [0103], [0104], [0109], [0110], [0114], [0137]-[0141], [0143], [0159]-[0164], [0166]-[0174]; Figures 1-2, 5-6, 9-10, 13, 19-26, 29-35, claims 1, 11, 13, 14; Wang ’084 at ¶ [0038]; Mathew at 4:50-5:47, 6:22-41, 7:5-31, Figures 20, 21.

A width of the high dielectric constant gate insulating film along a gate length being larger than a width of the gate electrode along the gate length was also well-known prior to the ’764 patent. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], 143, Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Matsumoto 185 at Abstract, ¶¶ [0011], [0012], [0038], [0042]-[0046], [0048], [0049], Figures 3-6, 33, claim 7; Guha at ¶¶ [0040], [0041], [0043]-[0045], [0047], Figure 12; Kubicek at 1, Figure 1; Noguchi at 4:35-39, 4:40-52, 4:53-57, 5:6-10, 5:23-43, Figures 1, 6; JP-Ono at Abstract, ¶¶ [0013], [0018]-[0022], [0023]-[0037], [0041]-[0044], [0060], [0076]-[0080], Figures 1-3, 6-10, 19-23, claim 1; Paton at Abstract , 1:56-

2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, Figures 1-5, claims 1, 8; Gardner at Abstract, 2:20-30, 3:39-4:21, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-4, 7; Ono at ¶¶ [0199], [0215], Figure 13; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[005]6, Figures 2, 5F; Mathew at 5:62-6:7, 7:5-31, Figures 11, 17, 20, 21; Houssa at 510; Plummer at 82-83.

A width of a bottom surface of the high dielectric constant gate insulating film along a gate length being larger than a width of a bottom surface of the gate electrode along the gate length was also well-known prior to the ’764 patent. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Matsumoto 185 at Abstract, ¶¶ [0011], [0012], [0038], [0042]-[0046], [0048], [0049], Figures 3-6, 33, claim 7; Guha at ¶¶ [0040], [0041], [0043]-[0045], [0047], Figure 12; Kubicek at 1, Figure 1; Noguchi at 4:35-39, 4:40-52, 4:53-57, 5:6-10, 5:23-43, Figures 1, 6; JP-Ono at Abstract, ¶¶ [0013], [0018]-[0022], [0023]-[0037], [0041]-[0044], [0060], [0076]-[0080], Figures 1-3, 6-10, 19-23, claim 1; Paton at Abstract , 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, Figures 1-5, claims 1, 8; Gardner at Abstract, 2:20-30, 3:39-4:21, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-4, 7; Ono at ¶¶ [0199], [0215], Figure 13; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Mathew at 5:62-6:7, 7:5-31, Figures 11, 17, 20, 21; Houssa at 510; Plummer at 82-83. By the 2005 priority date of the ’764 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the

gate electrode, that improve device performance and reliability. (*See, e.g.*, JP-Ono, ¶¶ [0029]-[0035], Figs. 1-4.)

The high dielectric constant gate insulating film having a relative dielectric constant of 10 or more was also well-known prior to the ’764 patent. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 10, 13, 14, ¶¶ [0032], [0102], [0103], [0105], [0107], [0137], [0138], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kajiyama at ¶ [0045]; Matsumoto 185 at Abstract, ¶¶ [0011], [0012], [0038], [0042]-[0045], Figures 3-6, 33, claim 7; Guha at ¶¶ [0038], [0043], claims 1, 3; Kubicek at Title, Abstract, 1, 4, Figure 1; Noguchi at 4:35-39, 4:40-52, 4:53-57, 5:23-28, Figures 1, 6; JP-Ono at Abstract, ¶¶ [0013], [0018]-[0032], [0041]-[0044], [0060], [0076]-[0080], claim 1, Figures 1-3, 6-10, 19-23; Paton at 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, claim 8, Figures 1-5; Gardner at Abstract, 2:20-30, 3:39-4:21, 4:41-64, 5:5-16, 6:19-30, claim 1-3, 10, Figures 1-4, 7; Ono at ¶ [0166], claims 1, 8; Wang ’084 at ¶ 35; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:6-8, 4:15-34, claim 1, Figures 20, 21; Yu at 3:15-33, 5:19-44; Wilk at 5254; Watanabe_2004 at Title, Abstract, 507, Figure 2; Watanabe_2003 at Title, 19, Figures 1, 11; Lee_1999 at 6.1.1; Wolf at 145, 146; Houssa at 8-9; Wang 672 at Abstract, ¶¶ [0009], [0012], [0025], [0034], [0045], claim 23; Ahmed at 5:40-61, 9:39-57; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4, 5; Lo at 3:50-60. By the 2005 priority date of the ’764 patent, a POSITA would have been motivated to use a high dielectric constant material to form the gate insulating film of a semiconductor device. For decades prior to the ’764 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. (*See, e.g.*, Plummer, 53; Houssa, 3-4.) As gate dielectrics continued to shrink in thickness (*e.g.*, below 1.5 nm), use of SiO2 became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON/OFF

states of the FET. (*See, e.g.*, Wolf, 4-5.) High-k gate dielectrics, like Hf-based oxides, Ta2O5, or ZrO2, replaced SiO_2 to address these challenges. (*See, e.g.*, Wolf, 146.) For example, it was known by the 2005 priority date of the ’764 patent that, as compared to SiO2, high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. (Wilk, 5250, Figure 5; Wolf, 146-47.)

The high dielectric constant gate insulating film having a larger relative dielectric constant than that of the second insulating sidewall was also well-known prior to the ’764 patent. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 10, 11, 13, 14, ¶¶ [0032], [0034], [0038], [0040], [0064], [0102]-[0104], [0105], [0107], [0109], [0110], [0114], [0137]-[0141], [0143], [0159]-[0164], [0166]-[0174], Figures 1, 2, 4-6, 9, 10, 13-15, 18-26, 29-35; Kajiyama at ¶¶ [0028], [0031], [0045]; Matsumoto 185 at Abstract, ¶¶ [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32, 33, claim 7; Guha at ¶¶ [0028], [0038], [0043], claims 1, 3; Kubicek at Title, Abstract, 1, 4, Figure 1; Noguchi at 4:35-39, 4:40-52, 4:53-5:10, 5:11-14, 5:23-28, 6:6-18, 7:21-28, 8:56-64, 9:45-50, 13:25-32, 13:59-61, Figures 1, 6; Wang ’084 at ¶¶ [0023], [0035], [0038], claim 6; Mathew at Abstract, 1:35-2:10, 3:17-40, 4:6-8, 4:15-34, 4:50-5:47, 6:22-41, 7:5-31, claims 1, 3, Figures 20, 21; Yu at 3:34-42; Wilk at 5254; Watanabe_2004 at Title, Abstract, 507, Figure 2; Watanabe_2003 at Title, 19, Figures 1, 11; Houssa at 8-9; Wang 672 at Abstract, ¶¶ [0009], [0012], [0025], [0034], [0045], claim 23; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4, 5.

Additional motivations to combine may be found in the ’764 patent invalidity charts.

In sum, by the time the application for the ’764 patent was filed, it was well known to design a semiconductor device as claimed at least because all the above was well known in the art before the ’764 patent, and a POSITA would have known that any and/or all the above techniques

could be combined to fabricate a semiconductor device with a high dielectric constant gate insulating film formed on an active region in a substrate, a gate electrode formed on the high dielectric constant gate insulating film, a first insulating sidewall formed on each side surface of the gate electrode, a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode. This is especially true here because all of the references disclose a semiconductor device with sidewalled transistors even if they do not disclose every aspect of a semiconductor device design. As such, a POSITA would have logically and predictably consulted all of the references together to design a complete semiconductor device with the claimed sidewalled transistors. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known semiconductor device designs to create different semiconductor devices with the claimed sidewalled transistors. Because all of these techniques were already known in the art for use in fabrication of semiconductor devices, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a

semiconductor device, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits 764-01 through 764-13, a POSITA would have been motivated to combine any of the references identified as prior art to the ’764 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar semiconductor device designs with sidewalled transistors (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Matsumoto 135 at Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0014], [0015]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102], [0103], [0105], [0107], [0137]-[0138], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kajiyama at Title, Summary, claims 1, 5, 8, ¶¶ [0001], [0002], [0005], [0013]-[0015], [0027]-[0029], [0045], Figures 1(A)-(D); Noguchi at Title, Abstract, 1:14-17, 3:50-52, 4:35-39, 4:40-52, 4:53-57, 5:23-28, 13:11-15, 13:16-21, Figures 1, 6; Guha at Title, Abstract, ¶¶ [0001], [0021], [0022], [0023], [0026], [0037], [0038], [0043], Figures 10-12, claims 1, 3, 13; Kubicek at Abstract, 1, 4, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 6:20-29, 6:52-7:25, 7:31-63, claims 1, 8, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], claims 1, 7, Figures 3-6, 33; JP-Ono at Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], claim 1, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Title, Abstract, ¶¶ [0002], [0007]-[0011], [0020]-[0022], [0047]-[0048], [0054]-[0055], claim 1, Figures 2, 5F; Ono at Title, Abstract, ¶¶ [0003], [0007], [0008], [0158], [0160], [0166], claims 1, 8, 13, Figure 4; Mathew at Abstract, 1:7-10, 1:35-

2:10, 3:17-40, 4:6-8, 4:15-34, claim 1, Figures 20, 21; Yu at Title, 1:6-10, 1:14-17, 1:17-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004 at Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003 at Title, 19, Figures 1, 11; Lee_2000 at Title, 2.4.1, 2.4.2, Figures 1, 12; Lee_1999 at Title, 6.1.1; Andreoni at Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055], [0056], [0057], Figures 1, 2A, 2B, 2C; Wolf at 145-146, Figures 1-2, 5-25; Wang 672 at Title, Abstract, ¶¶ [0002], [0008], [0009], [0010]-[0012], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044], [0045], [0047], [0048], [0050]-[0052], claim 15, Figure 3; Ahmed at 5:40-61; Mutou at ¶¶ [0006], [0007], [0042], [0043], [0054], [0055], [0072], [0080], [0111], [0112], claims 1, 4, 5, Figures 1-11; Houssa at 8, 9, 510.

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, a high dielectric constant gate insulating film continuously formed so as to extend from under the gate electrode to under the insulating sidewall—to other references that relate to semiconductor device designs generally because all references teach designing transistors with particular technical specifications suitable different purposes in semiconductor devices, and it would have been a trivial exercise to consult the references that taught more specific semiconductor device designs to fill in less specific disclosures in other references. *See, e.g.*, Matsumoto 135 at Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kajiyama at ¶¶ [0029]-[0031], Figures 1(A)-(D); Noguchi at 4:35-39, 13:33-39, 14:20-30, Figures 1, 6; Guha at [0028], [0034], [0035], [0043]-[0045], Figures 10-12, claims 1, 13; Kubicek at 1, Figure 1; Paton at Abstract, 1:7-12, 1:56-2:13, 3:63-4:13, 4:39-57, 6:20-29, 6:52-7:25, 7:31-63, 7:64-8:11, claims 1, 8, 15, Figures 1-5; Matsumoto 185 at Title, Abstract, ¶¶ [0001], [0010], [0011], [0012], [0038], [0042]-[0045], [0119]-[0120], claims 1, 7, Figures 3-6, 32-33; JP-Ono at

Title, Abstract, ¶¶ [0001], [0013], [0018]-[0022], [0023]-[0032], [0033]-[0037], [0041]-[0044], [0060], [0076]-[0080], [0083]-[0084], claims 1, 3, Figures 1-3, 6-10, 19-22, 23; Gardner at Title, Abstract, 1:7-10, 2:12-14, 2:20-30, 3:22-26, 3:39-4:21, 4:26-45, 4:41-64, 5:5-16, 6:19-30, claims 1-3, 10, Figures 1-7; Wang 084 at Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Ono at ¶¶ [0199], [0215], Figure 13; Mathew at 5:62-6:7, 7:5-31, Figures 11, 17, 20, 21; Houssa at 510; Plummer at 82, 83.

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular semiconductor device with the teachings regarding other materials, components, and configurations used in other semiconductor devices for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques for designing semiconductor devices existed. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: fabricating a semiconductor device with sidewalled transistors. This is thus a combination of prior art elements (*e.g.*, a high dielectric constant gate insulating film formed on an active region in a substrate, a gate electrode formed on the high dielectric constant gate insulating film, a first insulating sidewall formed on each side surface of the gate electrode, a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller

thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of semiconductor fabrication were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

Additional obviousness combinations of the references identified here are possible, and TSMC may rely on such combination(s) in this litigation. In particular, TSMC is currently unaware of AICP's allegations with respect to the level of skill in the art and the qualifications of a POSITA. TSMC is also unaware of the extent, if any, to which AICP may contend that limitations of the claims at issue are not disclosed in the prior art identified by TSMC as anticipatory, and the extent to which AICP will contend that elements not disclosed in the asserted patent specifications would have been known to a POSITA. And TSMC does not yet know how the Court will construe terms in the asserted claim. TSMC is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. TSMC reserves the

right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case No. IPR2025-00829 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the ’764 patent.

c. The ’686 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below, and in Exhibits 686-01 through 686-09 would have rendered obvious one or more Asserted Claims of the ’686 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits 686-01 through 686-09, TSMC contends that all asserted claims are rendered obvious by Intel_686_Products, Akasaka077, Akasaka939, Aoyama950, Bohr559, Hsu660, Kavalieros277, and Okazaki789 alone or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 686-01 through 686-09 and Herein)[13]:
686-01	Intel_686_Products	Akasaka077, Akasaka939, Alvarez069, Aoyama950, Bai article, Bohr article, Bohr559, Bohr683, Hou414, Hsu660, Hsu823, James 90nm article, Jung104, Kavalieros277, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Okazaki789, Thompson Apr2004 article, Thompson Nov2004 article, Yu273
686-02	Akasaka077	Akasaka939, Alvarez069, Aoyama950, Bai article, Bohr article, Bohr559, Bohr683, Hou414, Hsu660, Hsu823, Intel_686_Products, James 90nm article, Jung104, Kavalieros277, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Okazaki789, Thompson Apr2004 article, Thompson Nov2004 article, Yu273
686-03	Akasaka939	Akasaka077, Alvarez069, Aoyama950, Bai article, Bohr article, Bohr559, Bohr683, Hou414, Hsu660, Hsu823, Intel_686_Products, James 90nm article, Jung104, Kavalieros277, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Okazaki789, Thompson Apr2004 article, Thompson Nov2004 article, Yu273
686-04	Aoyama950	Akasaka077, Akasaka939, Alvarez069, Bai article, Bohr article, Bohr559, Bohr683, Hou414, Hsu660, Hsu823, Intel_686_Products, James 90nm article, Jung104, Kavalieros277, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Okazaki789, Thompson Apr2004 article, Thompson Nov2004 article, Yu273
686-05	Bohr559	Akasaka077, Akasaka939, Alvarez069, Aoyama950, Bai article, Bohr article, Bohr683, Hou414, Hsu660, Hsu823, Intel_686_Products, James 90nm article, Jung104, Kavalieros277, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Okazaki789, Thompson Apr2004 article, Thompson Nov2004 article, Yu273

[13] To the extent any reference is cited in Exhibits 686-01 through 686-09, but not referenced here, any omission was unintentional and TSMC intends to rely on its identification of any such combinations in Exhibits 686-01 through 686-09.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 686-01 through 686-09 and Herein)[13]:
686-06	Kavalieros277	Akasaka077, Akasaka939, Alvarez069, Aoyama950, Bai article, Bohr article, Bohr559, Bohr683, Hou414, Hsu660, Hsu823, Intel_686_Products, James 90nm article, Jung104, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Okazaki789, Thompson Apr2004 article, Thompson Nov2004 article, Yu273
686-07	Okazaki789	Akasaka077, Akasaka939, Alvarez069, Aoyama950, Bai article, Bohr article, Bohr559, Bohr683, Hou414, Hsu660, Hsu823, Intel_686_Products, James 90nm article, Jung104, Kavalieros277, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Thompson Apr2004 article, Thompson Nov2004 article, Yu273
686-08	Hsu660	Akasaka077, Akasaka939, Alvarez069, Aoyama950, Bai article, Bohr article, Bohr559, Bohr683, Hou414, Hsu823, Intel_686_Products, James 90nm article, Jung104, Kavalieros277, Kavalieros729, Ke984, Mistry2007 article, Mistry2007 presentation, Murthy151, Murthy482, Nagaoka751, Nakajima317, Okazaki789, Thompson Apr2004 article, Thompson Nov2004 article, Yu273

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’686 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’686 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits 686-01 through 686-09 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits 686-01 through 686-09, including for the reasons described below. A POSITA at the time of filing of the asserted patents would also have understood the references listed above,

alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’686 patent relates to Metal Insulator Semiconductor Field Effect Transistors (“MISFETs”)[14] with high-k insulating films and metal gate electrodes (also known as high-k/metal-gate, or “HKMG,” transistors). The asserted claims recite elements that were conventional in HKMG MISFETs long before the earliest available priority date listed on the face of the ’686 patent (March 13, 2008). A first gate insulating film formed on a first active region in a semiconductor substrate, *see, e.g.*, ’686 patent at 11:25-12:7, 16:16-22, 17:31-18:24, 18:51-53, 19:25-41, 21:18-24, 22:33-41, 23:11-15, 24:4-65, 25:21-27, 26:14-27, 26:65-27:20, 27:27-48, 28:3-9, 29:16-40, FIGS. 1B-5C, 6B-12, was well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62, 2:1-3:4, 3:29-4:26, 5:12-21, FIGS. 13-16; Zhang article at 50, Figs. 1-4 (incorporated by reference in the ’686 patent); Song article at 1, Figs. 1(a), 1(b), 4 (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 247-50, Figs. 2, 5, 6 (same); Mistry2007 presentation at 3-5, 14, 15a-15j, 16, 19, 35 (same); QX9650_Report, at 2, 14-15, 24-28, 43-56, 67-68, 70-74, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.14 through 2.3.1.27, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6, 2.4.2 (same); Aoyama950, at Abstract, ¶ [0003], ¶ [0006], ¶¶ [0008]-[0031], ¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶¶ [0115]-[0117], ¶ [0119], FIGS. 5, 6D-6Q; Akasaka077 ¶ [0003], ¶ [0006],¶ [0072], ¶ [0075], ¶¶ [0082]-[0083], ¶¶ [0087]-[0088], FIGS. 19-26; Akasaka939, at Title, Abstract, ¶¶ [0002]-[0006], ¶¶ [0008]-[0009], ¶¶ [0011]-[0021], ¶ [0037], ¶¶ [0039]-[0059], ¶¶ [0061]-[0066], ¶¶ [0069]-[0070], ¶¶ [0072]-[0073], ¶¶ [0080]-[0096], TBL. 1, FIGS. 1-15;

[14] MISFETs are also referred to sometimes as Metal Oxide Semiconductor Field Effect Transistors (“MOSFETs”).

Bohr559 ¶¶ [0002]-[0003], ¶ [0008], ¶¶ [0016]-[0019], ¶ [0022], ¶¶ [0024]-[0027], ¶¶ [0029]-[0032], ¶¶ [0035]-[0043], ¶ [0050], ¶ [0053], FIGS. 1-10; Kavalieros277 ¶¶ [0002]-[0003], ¶¶ [0007]-[0011], ¶¶ [0013]-[0018], ¶¶ [0025]-[0026], ¶¶ [0034]-[0037], ¶¶ [0042]-[0043], FIGS. 1A-1R; Okazaki789, at Abstract, 1:44-51, 1:58-65, 2:15-24, 2:44-64, 3:3-19, 3:25-40, 6:8-51, 7:23-46, 8:48-58, 9:35-10:67, 12:63-13:29, 14:24-30, 14:56-15:21, 16:4-17, 16:57-63, FIGS. 1C-1I, 2C-2I, 3A-5B; Hsu660, at Abstract, 1:35-54, 2:32-38, 2:47-4:40, 5:9-46, 6:10-7:8, 7:64-8:2, 8:26-34, FIGS. 1-11; Hsu823, ¶¶ [0013]-[0014], ¶ [0028], FIGS. 1-2B, 4-15B; Jung104, ¶ [0008], ¶¶ [0035]-[0037], ¶ [0079], ¶ [0084], ¶ [0105], FIGS. 1A-1C; Yu273, 3:10-34, FIGS. 2-7; Saito663, at Abstract, ¶ [0005], ¶¶ [0008]-[0038], ¶¶ [0050]-[0053], ¶¶ [0055]-[0056], ¶¶ [0058]-[0059], ¶¶ [0061]-[0062], ¶ [0064], ¶ [0067], ¶ [0071], ¶¶ [0073]-[0078], ¶ [0080], ¶¶ [0083]-[0084], ¶ [0086], ¶¶ [0089]-[0090], ¶¶ [0092]-[0095], ¶¶ [0097]-[0100], ¶¶ [0103]-[0105], ¶¶ [0109]-[0112], ¶¶ [0115]-[0124], ¶¶ [0127]-[0130], ¶ [0133], FIGS. 1A-1F, 2E-2I, 3-5, 6A-6G, 7-9; Iriyama511, 1:41-2:65, 3:51-56, 3:59-5:4, 7:31-44, 9:29-54, 11:55-60, 12:20-30, 13:1-5, FIGS. 1B-1C, 8B-13B, 8C-13C, 15B-20B, 15C-20C, 25A-25B, 26; Nakajima317, at Abstract, ¶¶ [0010]-[0015], ¶ [0100], ¶ [0107], ¶ [0117], ¶ [0125], ¶ [0155], ¶ [0179], ¶ [0190], ¶ [0198], ¶ [0214], ¶ [0227], ¶ [0236], ¶ [0255], ¶ [0268], ¶ [0277], ¶ [0295], ¶ [0307], ¶¶ [0340]-[0341], ¶ [0355], ¶ [0364], ¶¶ [0389]-[0390], ¶ [0403], ¶ [0436], ¶ [0447], ¶ [0465], FIGS. 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶¶ [0006]-[0007], ¶¶ [0009]-[0011], ¶ [0013], ¶¶ [0020]-[0026], ¶¶ [0040]-[0041], ¶¶ [0043]-[0044], ¶¶ [0047]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 2:35-3:15, 10:5-15, 11:43-46, 11:67-12:5, 12:63-13:6, 13:8-16, 13:33-36, FIGS. 3A-3D, 4A-4H; Hou414, 2:31-3:57, 4:19-5:11, 5:64-6:3, 6:23-28, FIGS. 1-13; Matsuo615, at Abstract, ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0009]-[0014], ¶ [0018], ¶ [0024], ¶¶ [0027]-[0028], ¶¶ [0034]-[0035], ¶ [0039], ¶¶ [0046]-

[0047], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Title, Abstract, 1:8-10, 1:14-21, 1:32-48, 2:4-12, 2:19-42, 4:17-5:32, 7:5-12, 8:56-9:3, FIGS. 1C-1F, 2C-2F; Kavalieros729, ¶¶ [0018]-[0019], ¶ [0027]-[0028], ¶ [0039], ¶ [0046], FIGS. 1-14; Ke984, ¶ [0016], FIGS. 3-10; Murthy151, ¶¶ [0022]-[0023], ¶ [0028]-[0029], ¶¶ [0031]-[0038], ¶ [0049], ¶ [0073], ¶ [0075], ¶ [0079], ¶¶ [0081]-[0084], ¶ [0086], ¶ [0088], ¶¶ [0091]-[0092], ¶ [0094], ¶¶ [0124]-[0125], FIGS. 1-12; Bohr683, at Abstract, ¶¶ [0012]-[0017], ¶¶ [0030]-[0031], ¶ [0043], FIGS. 1-6; Nagaoka751, at Abstract, 1:22-55, 2:25-64, 3:32-54, 4:40-5:60, 6:1-8:3, 9:21-10:22, 11:19-40, 12:31-54, 13:46-14:3, 14:10-49, 14:64-16:5, 16:15-28, 16:50-17:17, 17:63-18:25, 19:34-54, 20:65-21:3, 21:8-22:3, 22:15-30, 22:44-23:4, 23:32-24:27, 25:14-39, FIGS. 1D-6H; Moriwaki178, 15:42-47, 16:24-31, 17:60-67, 18:35-42, 19:25-28, 19:54-61, 20:49-52, 21:7-17, 21:64-22:4, 22:58-61, 23:27-38, 23:49-52, 24:17-28, 25:17-24, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Alvarez069, ¶ [0039], FIGS. 5-11; Murthy482, 3:47-4:38, FIGS. 1a-1c; Metz258, Abstract, ¶ [0002], ¶¶ [0004]-[0005], ¶ [0009], ¶¶ [0022]-[0029], ¶ [0049], FIGS. 1c-1i; Colombo468, Abstract, ¶¶ [0004]-[0011], ¶ [0022], ¶¶ [0025]-[0026], ¶[0028], ¶ [0047], ¶ [0055], FIGS. 1-10; Thompson Nov2004 article, at 1790-96, Figs. 2, 5; Thompson Apr2004 article, at 191-93, Fig. 1; Morin article, at 355-58, Figs. 1, 2.

A first gate electrode including a second metal film formed on the first gate insulating film, *see, e.g.*, ’686 patent at 15:64-16:22, 16:55-60, 17:10-18:41, 18:54-66, 19:31-40, 21:7-24, 21:61-67, 22:1-19, 22:33-41, 23:11-24, 24:46-65, 25:21-27, 26:7-27, 26:65-27:6, 27:49-60, FIGS. 1B-12, was also well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62, 2:1-5, 2:23-3:4, 3:29-4:26, 5:12-21, FIGS. 13-16; Zhang article at 50, Figs. 1-4 (incorporated by reference in the ’686 patent); Song article at 1, Figs. 1(a)-4 (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing

Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 247-50, Figs. 2, 5, 6 (same); Mistry2007 presentation at 4, 5, 7, 8, 14, 15e-15j, 16, 19, 35 (same); QX9650_Report, at 2, 14-15, 24-28, 43-56, 67-68, 70-74, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.14 through 2.3.1.27, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6, 2.4.2 (same); Aoyama950, at Abstract, ¶ [0003], ¶¶ [0007]-[0031], ¶¶ [0098], ¶¶ [0118]-[0119], FIGS. 5, 6P-6Q; Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0082]-[0088], FIGS. 19-26; Akasaka939, at Abstract, ¶¶ [0005]-[0006], ¶¶ [0008]-[0009], ¶¶ [0014]-[0021], ¶ [0037], ¶¶ [0039]-[0041], ¶¶ [0049]-[0051], ¶¶ [0053]-[0054], ¶¶ [0056]-[0066], ¶¶ [0068]-[0070], ¶ [0074], ¶¶ [0076]-[0079], ¶¶ [0084]-[0086], ¶¶ [0088]-[0089], ¶¶ [0091]-[0092], FIGS. 8, 10-13; Bohr559 ¶ [0002], ¶¶ [0009]-[0014], ¶ [0018], ¶ [0021], ¶¶ [0023]-[0026], ¶¶ [0028]-[0030], ¶¶ [0034]-[0036], ¶¶ [0040]-[0045], ¶ [0047], ¶¶ [0050]-[0054], FIGS. 5-10; Kavalieros277, at Abstract, ¶¶ [0001]-[0004], ¶¶ [0029]-[0040], ¶ [0042], ¶ [0044], FIGS. 1I-1R; Okazaki789, at Abstract, 1:18-2:40, 2:44-3:45, 4:55-5:44, 5:6-6:16, 6:8-58, 7:23-67, 8:58-9:29, 9:35-42, 10:33-67, 11:1-16, 11:46-12:15, 12:63-13:3, 13:30-52, 13:60-14:17, 14:24-50, 14:56-15:28, 15:37-45, 16:4-17, 16:34-42, 16:52-63, FIGS. 1E-1I, 2E-2I, 3A-5B; Hsu660, 1:23-45, 1:55-67, 2:1-7, 5:47-8:34, FIGS. 2-11; Saito663, at Abstract, ¶ [0003], ¶¶ [0005]-[0007], ¶¶ [0010]-[0038], ¶ [0055], ¶¶ [0058]-[0062], ¶¶ [0069]-[0070], ¶¶ [0073]-[0078], ¶¶ [0086]-[0087], ¶¶ [0089]-[0095], ¶¶ [0098]-[0106], ¶¶ [0110]-[0116], ¶ [0118], ¶¶ [0121]-[0122], ¶¶ [0124]-[0128], ¶ [0130], ¶ [0132], FIGS. 1C-1F, 2F-2I, 3-5, 6D-6G, 7-9; Iriyama511, at Abstract, 1:16-19, 1:41-2:65, 3:51-56, 3:59-5:4, 7:35-52, 7:59-65, 9:33-54, 9:64-10:36, 12:33-47, 12:52-67, 13:6-9, 13:20-28, FIGS. 1B-1C, 8B-13B, 8C-13C, 15B-15C, 17B-20B, 17C-20C, 25A-25B, 26; Nakajima317, at Abstract, ¶ [0003], ¶¶ [0005]-[0008], ¶¶ [0010]-[0015], ¶¶ [0099]-[0104], ¶¶ [0106]-[0114], ¶¶ [0116]-[0122], ¶¶ [0124]-[0132], ¶¶ [0139]-[0144], ¶¶ [0155]-[0159], ¶ [0168], ¶ [0178], ¶¶ [0190]-[0191], ¶ [0203],

¶ [0213], ¶¶ [0227]-[0229], ¶ [0244], ¶ [0254], ¶¶ [0268]-[0270], ¶ [0284], ¶ [0294], ¶¶ [0307]-[0309], ¶ [0331], ¶¶ [0337]-[0339], ¶¶ [0355]-[0357], ¶ [0367], ¶ [0380], ¶¶ [0386]-[0388], ¶ [0399], ¶¶ [0402]-[0407], ¶ [0424], ¶ [0435], ¶ [0443], ¶¶ [0446]-[0450], ¶¶ [0454]-[0458], ¶ [0464], FIGS. 1-11, 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0007]-[0013], ¶¶ [0025]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 1:15-18, 2:35-3:15, 7:42-9:50, 9:53-10:2, 10:5-13:6, 13:8-41, FIGS. 3A-3D, 4A-4H; Hou414, at Abstract, 2:31-3:57, 4:19-5:11, 7:4-21, FIGS. 1-13; Matsuo615, at Abstract, ¶ [0003], ¶¶ [0005]-[0008], ¶¶ [0015]-[0025], ¶¶ [0027]-[0028], ¶¶ [0036]-[0053], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Abstract, 1:22-31, 2:1-12, 6:16-44, 7:21-57, 8:56-9:3, FIGS. 1E-1F, 2E-2F; Kavalieros729, ¶ [0046], FIG. 14; Nagaoka751, 1:56-67, 2:42-64, 5:21-60, 6:1-56, 7:26-8:3, 11:19-40, 12:55-13:32, 13:46-14:3, 14:64-15:11, 15:51-16:5, 16:30-17:17, 20:12-64, 21:8-42, 21:54-22:30, 22:53-23:21, 23:46-24:27, FIGS. 1J-1P, 2C, 3D, 4C-5E, 6B-6H; Moriwaki178, 15:48-60, 16:19-31, 17:46-67, 18:44-50, 19:30-41, 19:54-61, 20:66-21:17, 22:5-11, 22:26-30, 22:62-23:7, 23:27-38, 23:66-24:12, 24:17-28, 25:26-32, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Metz258, Abstract, ¶¶ [0003]-[0005], ¶ [0009], ¶¶ [0032]-[0036], ¶ [0049], FIGS. 1h-1i; Colombo468, Abstract, ¶¶ [0002]-[0003], ¶¶ [0006]-[0007], ¶¶ [0009]-[0012], ¶¶ [0018]-[0019], ¶ [0022], ¶¶ [0024]-[0055], FIGS. 2-10.

First sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative, *see, e.g.*, ’686 patent at 12:8-17, 12:44-63, 14:46-50, 17:52-18:24, 28:10-15, FIGS. 1D-6A, 7A-8C, 10A-11C, were also well-known before the ’686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346, Figs. 2, 3 (same); Mistry2007 article at 248, Figs. 5, 6 (same); Mistry2007 presentation at 15a-15j, 16, 19 (same); QX9650_Report, at 2, 14-15,

24-28, 43-56, 67-68, 70-74, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.14 through 2.3.1.27, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6, 2.4.2 (same); Aoyama950, ¶ [0054], ¶ [0086], ¶ [0111], FIGS. 5, 6I-6Q; Akasaka077 ¶ [0005], ¶ [0007], ¶ [0073], ¶¶ [0084]-[0087], FIGS. 16-26; Akasaka939 ¶¶ [0008]-[0009], ¶¶ [0069]-[0070], ¶ [0077], ¶ [0086], ¶¶ [0088]-[0089], FIGS. 10, 11B-13; Bohr559 ¶ [0018], ¶ [0021], ¶¶ [0025]-[0026], ¶ [0030], ¶ [0041], ¶ [0043], FIGS. 1-10; Kavalieros277 ¶ [0003], ¶¶ [0019]-[0023], ¶ [0027], ¶ [0029], ¶ [0040], FIGS. 1E-1R; Okazaki789, 1:66-2:5, 2:15-20, 4:19-44, 8:58-9:12, 9:52-10:12, 10:57-67, 11:6-15, 12:19-25, 13:10-20, 13:42-52, 14:31-37, 14:65-15:6, 15:21-28, 15:49-55, 16:18-26, FIGS. 1A-5B; Hsu660, 2:1-38, 3:48-4:34, 6:19-23, FIGS. 4-11; Hsu823, at Abstract, ¶ [0008], ¶¶ [0010]-[0011], ¶¶ [0013]-[0015], ¶ [0028], ¶¶ [0024]-[0026], ¶¶ [0030]-[0033], ¶ [0035], ¶ [0037], ¶¶ [0041]-[0042], FIGS. 1-2B, 5-15B; Jung104, ¶¶ [0035]-[0037], ¶ [0079], ¶ [0084], ¶¶ [0089]-[0090], ¶ [0105], FIGS. 1A-1C; Yu273, 3:10-58, FIGS. 3-7; Saito663, at Abstract, ¶¶ [0107]-[0112], FIGS. 2B-2I, 3-5, 6A-6G, 7-9; Iriyama511, 1:41-2:20, 7:17-52, 8:32-58, FIGS. 1B, 3B-13B, 15B-20B, 24A-24C, 25A-25B; Nakajima317, ¶ [0152], ¶ [0157], ¶ [0170], ¶ [0187], ¶ [0192], ¶ [0205], ¶ [0224], ¶ [0230], ¶ [0246], ¶ [0265], ¶ [0271], ¶ [0286], ¶ [0304], ¶ [0310], ¶ [0320], ¶ [0322], ¶ [0352], ¶ [0358], ¶ [0368], ¶ [0370], ¶ [0400], ¶ [0405], ¶ [0415], ¶ [0444], ¶ [0448], FIGS. 14-15, 19-20, 22-23, 27-28, 30-31, 35-36, 38-39, 43-44, 46-47, 50-53, 55-56, 59-62, 64-65, 68-73, 75-79; Saito631, 10:5-13:6, FIGS. 4B-4H; Hou414, 1:57-2:22, 3:33-53, 5:12-40, FIGS. 3-13; Matsuo615, ¶ [0009], ¶¶ [0011]-[0012], ¶ [0034], FIGS. 1A-1I, 3A-3J; Brask784, at Abstract, 1:22-31, 2:19-31, 2:43-60, 4:17-33, 7:21-57, FIGS. 1A-1F, 2A-2F; Kavalieros729, ¶ [0018], ¶ [0023], ¶¶ [0027]-[0028], ¶ [0046], FIGS. 2-14; Ke984, ¶ [0018], FIGS. 4-10; Murthy151, ¶ [0007], ¶ [0022], ¶¶ [0031]-[0033], ¶ [0038], ¶ [0070], ¶ [0073], ¶¶ [0075]-[0076], ¶ [0084], ¶ [0088], ¶¶ [0091]-[0092], ¶ [0094], ¶ [0097], ¶¶ [0124]-[0125], FIGS. 1-12; Bohr683, ¶ [0017], ¶ [0038],

FIGS. 2-6; Nagaoka751, 2:30-40, 2:49-64, 8:34-9:20, 10:34-51, 12:31-42, 13:33-45, 14:15-49, 16:50-17:17, 22:15-30, FIGS. 1A-6H; Moriwaki178, 15:17-21, 17:24-28, 19:21-24, 20:45-49, 22:54-57, 23:45-49, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Alvarez069, ¶ [0040], FIGS. 5-11; Murthy482, 3:47-4:38, FIGS. 1a-1c; Metz258, ¶¶ [0010]-[0012], ¶ [0021], FIGS. 1a-1i; Colombo468, ¶ [0054], FIGS. 9-10.

A silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers, *see, e.g.*, '686 patent at 14:51-15:30, 17:19-30, 17:50-18:24, 18:42-50, 28:10-29:15, FIGS. 3D-6A, 7A-8C, 10A-11C, was also well-known before the '686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 248, Figs. 5, 6 (same); Mistry2007 presentation at 16, 19 (same); QX9650_Report, at 2, 14-15, 26-28, 43-44, 65-67, 70-72, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1.14, 2.3.1.15, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); Aoyama950, ¶ [0054], ¶ [0056], ¶ [0086], ¶ [0088], ¶¶ [0100]-[0101], ¶¶ [0111]-[0113], FIGS. 5, 6I-6Q; Akasaka077 ¶ [0007], ¶¶ [0072]-[0074], ¶¶ [0084]-[0087], FIGS. 16-26; Akasaka939, at Abstract, ¶ [0003], ¶¶ [0006]-[0010], ¶ [0040], ¶¶ [0069]-[0071], ¶¶ [0077]-[0079], ¶ [0086], FIGS. 10, 11B-13; Bohr559 ¶ [0018], ¶ [0021], ¶¶ [0025]-[0026], ¶¶ [0030]-[0032], ¶ [0034], ¶ [0037], ¶ [0039], ¶ [0041], ¶ [0043], FIGS. 1-10; Kavalieros277, at Abstract, ¶ [0003], ¶¶ [0019]-[0025], ¶ [0027], ¶ [0029], ¶ [0037], ¶ [0040], ¶ [0043], ¶¶ [0045]-[0046], FIGS. 1G-1R; Okazaki789, at Abstract, 1:58-2:5, 2:30-40, 3:3-40, 3:55-4:44, 6:52-7:30, 7:59-67, 8:1-11, 8:48-10:3, 11:6-26, 11:46-52, 12:6-15, 12:19-13:20, 13:38-52, 14:1-17, 14:24-50, 14:56-64, 15:49-65, 16:4-17, TBLS. 1-2, FIGS. 1A-5B; Hsu660, 2:1-38, 5:37-38, 6:19-37, 7:64-8:2, FIGS. 4-11; Hsu823, at

Abstract, ¶¶ [0002]-[0003], ¶¶ [0005]-[0006], ¶ [0008], ¶¶ [0012]-[0015], ¶ [0019], ¶¶ [0024]-[0026], ¶ [0028], ¶ [0032], ¶¶ [0035]-[0038], ¶ [0040], ¶ [0043], FIGS. 3, 10-13; Jung104, at Title, Abstract, ¶ [0001], ¶¶ [0010]-[0065], ¶¶ [0075]-[0133], TABLES I-VII, FIGS. 1A-2, 4A-15; Yu273, at Title, Abstract, 1:30-6:64, FIGS. 6-7; Nakajima317, ¶ [0304], ¶ [0310], ¶¶ [0326]-[0328], ¶ [0352], ¶ [0358], ¶¶ [0374]-[0376], FIGS. 46-47, 5153, 55-56, 60-62; Hou414, 3:33-57, 6:51-7:3, FIG. 13; Kavalieros729, ¶ [0018], ¶ [0026], ¶ [0046], FIGS. 6-14; Ke984, at Abstract, ¶ [0003], ¶ [0027], ¶ [0030], ¶ [0031], FIGS. 8-10; Bohr683, ¶¶ [0038]-[0039], ¶¶ [0048]-[0049], FIG. 6; Nagaoka751, 2:30-40, 3:32-4:39, 8:34-9:20, 12:31-42, 13:33-45, 14:15-49, 17:63-18:25, 24:33-36, 24:44-25:5, 25:24-39, FIGS. 1A-6H; Alvarez069, Abstract, ¶¶ [0047]-[0055], ¶¶ [0059]-[0064], ¶¶ [0073]-[0081], FIGS. 9-11; James 90nm article, at 2, Figure 5; Bohr article, at 2, Figures 1-2; Eneman article, at 1446-52, Table I, Figs. 2-4, 6, 8-10; Bai article, at 657, Fig. 3.

A second gate insulating film formed on a second active region in a semiconductor substrate, *see, e.g.*, ’686 patent at 11:25-12:7, 16:16-22, 17:31-18:24, 18:51-53, 19:25-41, 21:18-24, 22:33-41, 23:11-15, 25:21-27, 26:65-27:6, 27:39-48, 28:3-9, 29:16-40, FIGS. 1B-5C, 6B-12, was well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62, 2:1-3:4, 3:29-4:26, 5:12-21, FIGS. 13-16; Zhang article at 50, Figs. 1-4 (incorporated by reference in the ’686 patent); Song article at 1, Figs. 1(a), 4 (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 247-50, Figs. 2, 5, 6 (same); Mistry2007 presentation at 3-5, 14, 15a-15j, 16, 19, 35 (same); QX9650_Report, at 2, 14-15, 24-28, 30-40, 63-64, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.2.8, 2.3.2.9 (same); Aoyama950, at Abstract, ¶ [0003], ¶ [0006],

¶¶ [0008]-[0031], ¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶¶ [0115]-[0117], ¶ [0119], FIGS. 5, 6D-6Q; Akasaka077 ¶ [0003], ¶ [0006], ¶ [0072], ¶ [0075], ¶¶ [0082]-[0083], ¶¶ [0087]-[0088], FIGS. 19-26; Akasaka939, at Title, Abstract, ¶¶ [0002]-[0006], ¶¶ [0008]-[0009], ¶¶ [0011]-[0021], ¶ [0037], ¶¶ [0039]-[0059], ¶¶ [0061]-[0066], ¶¶ [0069]-[0070], ¶¶ [0072]-[0073], ¶¶ [0080]-[0096], TBL. 1, FIGS. 1-15; Bohr559 ¶¶ [0002]-[0003], ¶ [0005], ¶¶ [0016]-[0021], ¶ [0024], ¶ [0031], ¶ [0033], ¶¶ [0036]-[0043], ¶ [0046], ¶ [0048], ¶ [0050], ¶ [0053], FIGS. 1-10; Kavalieros277 ¶¶ [0002]-[0003], ¶¶ [0007]-[0011], ¶¶ [0013]-[0018], ¶¶ [0025]-[0026], ¶¶ [0034]-[0037], ¶¶ [0042]-[0043], FIGS. 1A-1R; Okazaki789, at Abstract, 1:44-51, 1:58-65, 2:15-24, 2:44-64, 3:3-19, 3:25-40, 6:8-51, 7:23-46, 8:48-58, 9:35-10:67, 12:63-13:29, 14:24-30, 14:56-15:21, 16:4-17, 16:52-63, FIGS. 1C-1I, 2C-2I, 3A-5B; Hsu660, at Abstract, 1:35-54, 2:32-38, 2:47-4:40, 5:9-46, 6:10-7:8, 7:64-8:2, 8:26-34, FIGS. 1-11; Hsu823, ¶¶ [0013]-[0014], ¶ [0028], FIGS. 1-2B, 4-15B; Jung104, ¶ [0008], ¶¶ [0035]-[0037], ¶ [0079], ¶ [0084], ¶ [0105], FIGS. 1A-1C; Yu273, 3:10-34, FIGS. 2-7; Saito663, at Abstract, ¶ [0005], ¶¶ [0008]-[0038], ¶¶ [0050]-[0053], ¶¶ [0055]-[0056], ¶¶ [0058]-[0059], ¶¶ [0061]-[0062], ¶ [0064], ¶ [0067], ¶ [0071], ¶¶ [0073]-[0078], ¶ [0080], ¶¶ [0083]-[0084], ¶ [0086], ¶¶ [0089]-[0090], ¶¶ [0092]-[0095], ¶¶ [0097]-[0100], ¶¶ [0103]-[0105], ¶¶ [0109]-[0112], ¶¶ [0115]-[0124], ¶¶ [0127]-[0130], ¶ [0133], FIGS. 1A-1F, 2E-2I, 3-5, 6A-6G, 7-9; Iriyama511, 1:41-2:65, 3:51-56, 3:59-5:4, 7:8-22, 9:5-8, 9:14-19, 12:11-13, 13:1-5, FIGS. 1A, 1C, 5A-13A, 5C-13C, 15A-20A, 15C-20C, 25A-25B, 26; Nakajima317, at Abstract, ¶¶ [0010]-[0015], ¶ [0100], ¶ [0107], ¶ [0117], ¶ [0125], ¶ [0150], ¶ [0163], ¶ [0179], ¶ [0185], ¶ [0198], ¶ [0214], ¶ [0222], ¶ [0236], ¶ [0255], ¶ [0263], ¶ [0277], ¶ [0295], ¶ [0302], ¶¶ [0340]-[0341], ¶ [0350], ¶ [0364], ¶¶ [0389]-[0390], ¶ [0399], ¶ [0436], ¶ [0443], ¶ [0465], FIGS. 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶¶ [0006]-[0007], ¶¶ [0009]-[0011], ¶ [0013],

¶¶ [0020]-[0026], ¶¶ [0040]-[0041], ¶¶ [0043]-[0044], ¶¶ [0047]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 2:35-3:15, 10:5-15, 11:43-46, 11:67-12:5, 12:63-13:6, 13:8-16, 13:33-36, FIGS. 3A-3D, 4A-4H; Hou414, 2:31-3:57, 4:19-5:11, 5:64-6:36, FIGS. 1-13; Matsuo615, at Abstract, ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0009]-[0014], ¶ [0018], ¶ [0024], ¶¶ [0027]-[0028], ¶¶ [0034]-[0035], ¶ [0039], ¶¶ [0046]-[0047], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Title, Abstract, 1:8-10, 1:14-21, 1:32-48, 2:4-12, 2:19-42, 4:17-5:32, 7:5-12, 8:56-9:3, FIGS. 1C-1F, 2C-2F; Kavalieros729, ¶¶ [0032]-[0036], ¶ [0039], FIGS. 10-13; Ke984, ¶ [0016], FIGS. 3-10; Murthy151, ¶¶ [0022]-[0023], ¶¶ [0028]-[0029], ¶¶ [0031]-[0038], ¶ [0049], ¶ [0073], ¶ [0075], ¶ [0079], ¶¶ [0081]-[0084], ¶ [0086], ¶ [0088], ¶¶ [0091]-[0092], ¶ [0094], ¶¶ [0124]-[0125], FIGS. 1-12; Bohr683, at Abstract, ¶¶ [0012]-[0017], ¶¶ [0030]-[0031], ¶ [0043], FIGS. 1-6; Nagaoka751, at Abstract, 1:22-55, 2:25-64, 3:32-54, 4:40-5:67, 6:1-8:3, 9:21-10:33, 11:3-48, 12:31-54, 13:46-14:3, 14:10-49, 14:64-16:5, 16:15-28, 16:50-17:17, 17:63-18:25, 19:34-54, 20:65-21:3, 21:8-22:3, 22:15-30, 22:44-23:4, 23:32-24:27, 25:14-39, FIGS. 1D-6H; Moriwaki178, 15:42-47, 16:24-31, 17:54-67, 18:35-42, 19:25-28, 19:54-61, 20:49-52, 21:7-17, 21:64-22:4, 22:58-61, 23:27-38, 23:49-52, 24:17-28, 25:17-24, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Alvarez069, ¶ [0039], FIGS. 5-11; Murthy482, 3:47-4:38, 5:14-23, FIGS. 1a-1c, 2-3, 4a-4c, 8; Metz258, Abstract, ¶ [0002], ¶¶ [0004]-[0005], ¶ [0009], ¶¶ [0022]-[0029], ¶ [0049], FIGS. 1c-1i; Colombo468, Abstract, ¶¶ [0004]-[0011], ¶ [0022], ¶¶ [0025]-[0026], ¶[0028], ¶ [0047], ¶ [0055], FIGS. 1-10.

A second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film, *see, e.g.*, ’686 patent at 11:38-12:7, 15:64-16:60, 17:10-18:41, 19:31-40, 21:7-45, 21:61-67, 22:1-19, 22:33-64, 23:17-25, 25:21-57, 26:7-12, 26:65-27:6, 27:20-26, 27:49-28:9, FIGS. 1B-12, was also well-known before the ’686

patent, *see, e.g.*, *id.* at 1:14-62, 2:1-5, 2:23-3:4, 3:29-4:26, 5:12-21, FIGS. 13-16; Zhang article at 50, Figs. 1-4 (incorporated by reference in the '686 patent); Song article at 1, Figs. 1(a)-4 (same). The prior art is replete with teachings that confirm this admission in the '686 patent. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 247-50, Figs. 2, 5, 6 (same); Mistry2007 presentation at 4, 5, 7, 8, 14, 15e-15j, 16, 19, 35 (same); QX9650_Report, at 2, 14-15, 24-28, 30-40, 63-64, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.2.8, 2.3.2.9 (same); Aoyama950, at Abstract, ¶ [0003], ¶¶ [0007]-[0031], ¶¶ [0098], ¶¶ [0107]-[0109], ¶¶ [0113]-[0117], ¶ [0119], ¶ [0121], FIGS. 5, 6E-6Q; Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0076]-[0077], ¶¶ [0080]-[0088], FIGS. 19-26; Akasaka939, at Abstract, ¶¶ [0005]-[0006], ¶¶ [0008]-[0009], ¶¶ [0014]-[0021], ¶ [0037], ¶¶ [0039]-[0041], ¶¶ [0049]-[0051], ¶¶ [0053]-[0054], ¶¶ [0056]-[0066], ¶¶ [0068]-[0070], ¶ [0074], ¶¶ [0076]-[0079], ¶¶ [0084]-[0086], ¶¶ [0088]-[0092], FIGS. 8, 10-13; Bohr559 ¶ [0002], ¶¶ [0009]-[0014], ¶ [0018], ¶ [0021], ¶¶ [0023]-[0026], ¶¶ [0028]-[0030], ¶¶ [0034]-[0036], ¶¶ [0040]-[0045], ¶¶ [0047]-[0048], ¶¶ [0050]-[0054], FIGS. 5-10; Kavalieros277, at Abstract, ¶¶ [0001]-[0004], ¶¶ [0029]-[0040], ¶¶ [0042]-[0044], FIGS. 1L-1R; Okazaki789, at Abstract, 1:18-2:40, 2:44-3:45, 4:55-5:44, 5:6-6:16, 6:8-58, 7:23-67, 8:58-9:29, 9:35-42, 10:33-67, 11:1-16, 11:46-12:15, 12:63-13:3, 13:30-52, 13:60-14:17, 14:24-50, 14:56-15:28, 15:37-45, 16:4-17, 16:34-42, 16:52-63, FIGS. 1E-1I, 2E-2I, 3A-5B; Hsu660, 1:23-45, 1:55-67, 2:1-7, 5:47-8:34, FIGS. 2-11; Saito663, at Abstract, ¶ [0003], ¶¶ [0005]-[0007], ¶¶ [0010]-[0038], ¶¶ [0058]-[0062], ¶¶ [0073]-[0078], ¶¶ [0089]-[0095], ¶¶ [0098]-[0106], ¶¶ [0110]-[0116], ¶¶ [0118], ¶¶ [0121]-[0122], ¶¶ [0124]-[0128], ¶ [0130], ¶ [0132], FIGS. 1E-1F, 2H-2I, 3-5, 6F-6G, 7-9; Iriyama511, at Abstract, 1:16-19, 1:41-2:65, 3:51-56, 3:59-5:4, 7:12-30, 7:59-65, 9:9-22, 9:64-10:35, 11:24-33, 12:33-36, 12:52-67, 13:6-19,

FIGS. 1A, 1C, 5A-13A, 5C-13C, 15A-20A, 15C-20C, 25A-25B, 26; Nakajima317, at Abstract, ¶ [0003], ¶¶ [0005]-[0008], ¶¶ [0010]-[0015], ¶¶ [0099]-[0104], ¶¶ [0106]-[0114], ¶¶ [0116]-[0122], ¶¶ [0124]-[0132], ¶¶ [0139]-[0144], ¶¶ [0150]-[0151], ¶ [0168], ¶ [0177], ¶¶ [0185]-[0186], ¶ [0203], ¶ [0212], ¶¶ [0222]-[0223], ¶ [0244], ¶ [0253], ¶¶ [0263]-[0264], ¶ [0284], ¶ [0293], ¶¶ [0302]-[0303], ¶ [0319], ¶¶ [0337]-[0339], ¶¶ [0350]-[0351], ¶ [0367], ¶¶ [0386]-[0388], ¶ [0399], ¶ [0424], ¶ [0434], ¶ [0443], ¶ [0464], FIGS. 1-11, 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0007]-[0013], ¶¶ [0025]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 1:15-18, 2:35-3:15, 7:42-9:50, 9:53-10:2, 10:5-13:6, 13:8-41, FIGS. 3A-3D, 4A-4H; ou414, at Abstract, 2:31-3:57, 6:4-41, 7:4-21, FIGS. 8-13; Matsuo615, at Abstract, ¶ [0003], ¶¶ [0005]-[0008], ¶¶ [0015]-[0025], ¶¶ [0027]-[0028], ¶¶ [0036]-[0053], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Abstract, 1:22-31, 2:1-12, 5:42-6:44, 7:5-57, 8:56-9:3, FIGS. 1E-1F, 2E-2F; Kavalieros729, at Abstract, ¶¶ [0037]-[0041], ¶ [0045], FIGS. 11-13; Nagaoka751, 1:56-67, 2:42-64, 5:21-67, 6:1-56, 7:26-8:3, 11:3-40, 12:55-13:32, 13:46-14:3, 14:64-15:11, 15:51-16:5, 16:30-17:17, 20:12-64, 21:8-42, 21:54-22:30, 22:53-23:21, 23:46-24:27, 25:14-23, FIGS. 1J-1P, 2C, 3D, 4C-5E, 6B-6H; Moriwaki178, 16:9-16, 16:24-31, 17:34-45, 18:51-57, 19:45-61, 20:54-65, 21:7-17, 22:12-25, 23:9-21, 23:31-38, 23:54-65, 24:21-27, 25:33-40, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Metz258, Abstract, ¶¶ [0003] [0005], ¶ [0009], ¶¶ [0030]-[0036], ¶ [0049], FIGS. 1g-1i; Colombo468, Abstract, ¶¶ [0002]-[0003], ¶¶ [0006]-[0007], ¶¶ [0009]-[0012], ¶¶ [0018]-[0019], ¶ [0022], ¶¶ [0024]-[0055], FIGS. 2-10.

Second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative, *see, e.g.*, ’686 patent at 12:8-17, 12:44-63, 14:46-50, 17:52-18:24, 28:10-15, FIGS. 1D-6A, 7A-8C, 10A-11C, were also well-known before the ’686 patent.

The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346, Figs. 2, 3 (same); Mistry2007 article at 248, Figs. 5, 6 (same); Mistry2007 presentation at 15a-15j, 16, 19 (same); QX9650_Report, at 2, 14-15, 24-28, 30-39, 63-64, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.10, 2.3.2.8, 2.3.2.9 (same); Aoyama950, ¶ [0054], ¶ [0086], ¶ [0111], FIGS. 5, 6I-6Q; Akasaka077 ¶ [0005], ¶ [0007], ¶ [0073], ¶¶ [0084]-[0087], FIGS. 16-26; Akasaka939 ¶¶ [0008]-[0009], ¶¶ [0069]-[0070], ¶ [0077], ¶ [0086], ¶¶ [0088]-[0089], FIGS. 10, 11B-13; Bohr559 ¶ [0018], ¶ [0021], ¶¶ [0025]-[0026], ¶ [0030], ¶ [0041], ¶ [0043], FIGS. 1-10; Kavalieros277 ¶ [0003], ¶¶ [0019]-[0023], ¶ [0027], ¶ [0029], ¶ [0040], FIGS. 1E-1R; Okazaki789, 1:66-2:5, 2:15-20, 4:19-44, 8:58-9:12, 9:52-10:12, 10:57-67, 11:6-15, 12:19-25, 13:10-20, 13:42-52, 14:31-37, 14:65-15:6, 15:21-28, 15:49-55, 16:18-26, 16:52-62, FIGS. 1A-5B; Hsu660, 2:1-38, 3:48-4:34, 6:19-23, FIGS. 4-11; Hsu823, at Abstract, ¶[0008], ¶¶ [0010]-[0011], ¶¶ [0013]-[0015], ¶ [0028], ¶¶ [0024]-[0026], ¶¶ [0030]-[0033], ¶ [0035], ¶ [0037], ¶¶ [0041]-[0042], FIGS. 1-2B, 5-15B; Jung104, ¶¶ [0035]-[0037], ¶ [0079], ¶ [0084], ¶¶ [0089]-[0090], ¶ [0105], FIGS. 1A-1C; Yu273, 3:10-58, FIGS. 3-7; Saito663, at Abstract, ¶¶ [0107]-[0112], FIGS. 2B-2I, 3-5, 6A-6G, 7-9; Iriyama511, 1:41-2:20, 7:17-52, 8:32-58, FIGS. 1A, 3A-13A, 15A-20A, 24A-24C, 25A-25B; Nakajima317, ¶ [0152], ¶ [0157], ¶ [0170], ¶ [0187], ¶ [0192], ¶ [0205], ¶ [0224], ¶ [0230], ¶ [0246], ¶ [0265], ¶ [0271], ¶ [0286], ¶ [0304], ¶ [0310], ¶ [0320], ¶ [0322], ¶ [0352], ¶ [0358], ¶ [0368], ¶ [0370], ¶ [0400], ¶ [0405], ¶ [0415], ¶ [0444], ¶ [0448], FIGS. 14-15, 19-20, 22-23, 27-28, 30-31, 35-36, 38-39, 43-44, 46-47, 50-53, 55-56, 59-62, 64-65, 68-73, 75-79; Saito631, 10:5-13:6, FIGS. 4B-4H; Hou414, 1:57-2:22, 3:33-53, 5:12-40, FIGS. 3-13; Matsuo615, ¶ [0009], ¶¶ [0011]-[0012], ¶ [0034], FIGS. 1A-1I, 3A-3J; Brask784, at Abstract, 1:22-31, 2:19-31, 2:43-60, 4:17-33, 7:21-57, FIGS. 1A-1F, 2A-2F; Kavalieros729, ¶ [0023], ¶ [0028],

FIGS. 2-13; Ke984, ¶ [0018], FIGS. 4-10; Murthy151, ¶ [0007], ¶ [0022], ¶¶ [0031]-[0033], ¶ [0038], ¶ [0070], ¶ [0073], ¶¶ [0075]-[0076], ¶ [0084], ¶ [0088], ¶¶ [0091]-[0092], ¶ [0094], ¶ [0097], ¶¶ [0124]-[0125], FIGS. 1-12; Bohr683, ¶ [0017], ¶ [0038], FIGS. 2-6; Nagaoka751, 2:30-40, 2:49-64, 5:21-67, 8:34-9:20, 10:34-51, 11:3-18, 12:31-42, 13:15-45, 14:15-49, 16:36-17:17, 20:12-38, 22:15-30, 25:14-23, FIGS. 1A-6H; Moriwaki178, 15:17-21, 17:24-28, 19:21-24, 20:45-49, 22:54-57, 23:45-49, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Alvarez069, ¶ [0040], FIGS. 5-11; Alvarez069, ¶ [0040], FIGS. 5-11; Murthy482, 3:47-5:13, FIGS. 1a-1c, 2-3, 4a-4c, 8; Metz258, ¶¶ [0010]-[0012], ¶ [0021], FIGS. 1a-1i; Colombo468, ¶ [0054], FIGS. 9-10.

A silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers, *see, e.g.*, ’686 patent at 14:51-15:30, 17:19-30, 17:50-18:24, 18:42-50, 28:10-29:15, FIGS. 3D-6A, 7A-8C, 10A-11C, was also well-known before the ’686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 248, Figs. 5, 6 (same); Mistry2007 presentation at 16, 19 (same); QX9650_Report, at 2, 14-15, 26-28, 30-32, 43-44, 63, 65-67, 70-72, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1.2, 2.3.1.3, 2.3.1.14, 2.3.1.15, 2.3.2.8, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); Aoyama950, ¶ [0054], ¶ [0056], ¶ [0086], ¶ [0088], ¶ [0099], ¶ [0101], ¶¶ [0111]-[0113], FIGS. 5, 6I-6Q; Akasaka077 ¶ [0007], ¶¶ [0072]-[0074], ¶¶ [0084]-[0087], FIGS. 16-26; Akasaka939, at Abstract, ¶ [0003], ¶¶ [0006]-[0010], ¶ [0040], ¶¶ [0069]-[0071], ¶¶ [0077]-[0079], ¶ [0086], FIGS. 10, 11B-13; Bohr559 ¶ [0018], ¶ [0021], ¶¶ [0025]-[0026], ¶¶ [0030]-[0032], ¶ [0034], ¶ [0037], ¶ [0039], ¶ [0041], ¶ [0043], FIGS. 1-10; Kavalieros277, at Abstract, ¶ [0003], ¶¶ [0019]-[0025], ¶ [0027], ¶ [0029], ¶ [0037], ¶ [0040],

¶ [0043], ¶¶ [0045]-[0046], FIGS. 1G-1R; Okazaki789, at Abstract, 1:58-2:5, 2:30-40, 3:3-40, 3:55-4:44, 6:52-7:30, 7:59-67, 8:1-11, 8:48-10:3, 11:6-26, 11:46-52, 12:6-15, 12:19-13:20, 13:38-52, 14:1-17, 14:24-50, 14:56-64, 15:49-65, 16:4-17, 16:52-63, TBLS. 1-2, FIGS. 1A-5B; Hsu660, 2:1-38, 5:37-38, 6:19-37, 7:64-8:2, 8:35-41, FIGS. 4-11; Hsu823, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0005]-[0006], ¶ [0008], ¶¶ [0012]-[0015], ¶ [0019], ¶¶ [0024]-[0026], ¶ [0028], ¶ [0032], ¶ [0035]-[0038], ¶ [0040], ¶ [0043], FIGS. 3, 10-13; Jung104, at Title, Abstract, ¶ [0001], ¶¶ [0010]-[0065], ¶¶ [0075]-[0133], TABLES I-VII, FIGS. 1A-2, 4A-15; Yu273, at Title, Abstract, 1:30-6:64, FIGS. 6-7; Nakajima317, ¶ [0304], ¶ [0310], ¶¶ [0326]-[0328], ¶ [0352], ¶ [0358], ¶¶ [0374]-[0376], FIGS. 46-47, 5153, 55-56, 60-62; Hou414, 3:33-57, 6:51-7:3, FIG. 13; Kavalieros729, ¶ [0026], FIGS. 6-12; Ke984, at Abstract, ¶ [0003], ¶ [0027], ¶ [0030], ¶ [0031], FIGS. 8-10; Bohr683, ¶¶ [0038]-[0039], ¶¶ [0048]-[0049], FIG. 6; Nagaoka751, 2:30-40, 3:32-4:39, 5:21-67, 8:34-9:20, 11:3-18, 12:31-42, 13:15-45, 14:15-49, 16:36-49, 17:63-18:25, 20:12-38, 24:33-36, 24:44-25:5, 25:14-39, FIGS. 1A-6H; Alvarez069, Abstract, ¶¶ [0047]-[0055], ¶¶ [0059]-[0064], ¶¶ [0073]-[0081], FIGS. 9-11; Eneman article, at 1446-52, Table I, Figs. 2-4, 6, 8-10; Morin article, at 355-58, Figs. 1, 2.

The first and second metal films being made of different metal materials, *see, e.g.*, ’686 patent at Abstract, 11:38-55, 15:64-16:9, 18:25-33, 19:25-41, 21:25-45, 22:42-53, 23:11-27, 25:28-57, FIGS. 4A-12, was also well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62, 2:23-29, 2:49-60, 3:29-36, 3:42-50, 5:12-21, FIGS. 13-14E, 16; Zhang article at 50, Figs. 1, 2, 4 (incorporated by reference in the ’686 patent); Song article at 1, Figs. 1(a)-4 (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79, Figs. 5-7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 1-3 (same); Mistry2007 article at 248, Figs. 2, 5, 6 (same); Mistry2007 presentation at 5, 14, 15e-15j,

16, 18, 19 (same); QX9650_Report, at 2, 14-15, 24-28, 30-40, 43-56, 63-64, 67-68, 70-74, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.1.14 through 2.3.1.27, 2.3.2.8, 2.3.2.9, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6, 2.4.2 (same); Aoyama950, at Abstract, ¶ [0003], ¶¶ [0009]-[0011], ¶¶ [0065]-[0066], ¶ [0098], ¶ [0107], ¶ [0109], ¶¶ [0115]-[0119], ¶ [0121], FIGS. 6, 6E-6Q; Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0076]-[0077], ¶¶ [0080]-[0088], FIGS. 19-26; Akasaka939, at Abstract, ¶¶ [0005]-[0006], ¶¶ [0008]-[0009], ¶¶ [0014]-[0021], ¶ [0037], ¶¶ [0039]-[0041], ¶¶ [0049]-[0051], ¶¶ [0053]-[0054], ¶¶ [0056]-[0066], ¶¶ [0068]-[0070], ¶ [0074], ¶ [0076]-[0079], ¶¶ [0084]-[0086], ¶¶ [0088]-[0092], FIGS. 8, 10-13; Bohr559 ¶ [0002], ¶¶ [0009]-[0014], ¶ [0018], ¶ [0021], ¶¶ [0023]-[0026], ¶¶ [0028]-[0030], ¶¶ [0034]-[0036], ¶¶ [0040]-[0045], ¶¶ [0047]-[0048], ¶¶ [0050]-[0054], FIGS. 5-10; Kavalieros277, at Abstract, ¶¶ [0001]-[0004], ¶¶ [0029]-[0040], ¶¶ [0042]-[0044], FIGS. 1I-1R; Okazaki789, at Abstract, 1:18-2:40, 2:44-3:45, 4:55-5:44, 5:6-6:16, 6:8-58, 7:23-67, 8:58-9:29, 9:35-42, 10:33-67, 11:1-16, 11:46-12:15, 12:63-13:3, 13:30-52, 13:60-14:17, 14:24-50, 14:56-15:28, 15:37-45, 16:4-17, 16:34-42, 16:52-63, FIGS. 1E-1I, 2E-2I, 3A-5B; Hsu660, 1:23-45, 1:55-67, 2:1-7, 5:47-8:34, FIGS. 2-11; Saito663, at Abstract, ¶ [0003], ¶¶ [0017]-[0018], ¶¶ [0027]-[0028], ¶¶ [0037]-[0038], ¶¶ [0058]-[0062], ¶¶ [0073]-[0078], ¶ [0089], ¶ [0091], ¶¶ [0093]-[0095], ¶¶ [0099]-[0103], ¶¶ [0111]-[0115], ¶ [0118], ¶¶ [0123]-[0127], ¶ [0130], ¶ [0132], FIGS. 1E-1F, 2H-2I, 3-5, 6F-6G, 7-9; Iriyama511, at Abstract, 2:29-65, 3:51-56, 3:59-5:4, 7:12-52, 7:59-65, 9:9-54, 9:64-10:36, 12:52-67, 13:6-28, FIGS. 1A-1C, 8A-13C, 15A-20C, 26; Nakajima317, at Abstract, ¶ [0003], ¶¶ [0005]-[0008], ¶¶ [0010]-[0015], ¶¶ [0099]-[0104], ¶¶ [0106]-[0114], ¶¶ [0116]-[0122], ¶¶ [0124]-[0132], ¶¶ [0139]-[0144], ¶¶ [0150]-[0151], ¶¶ [0155]-[0159], ¶ [0168], ¶¶ [0177]-[0178], ¶¶ [0185]-[0186], ¶¶ [0190]-[0191], ¶ [0203], ¶¶ [0212]-[0213], ¶¶ [0222]-[0223], ¶¶ [0227]-[0229], ¶ [0244], ¶¶ [0253]-[0254], ¶¶ [0263]-

[0264], ¶ [0268] ¶ [0270], ¶ [0284], ¶¶ [0293]-[0294], ¶¶ [0302]-[0303], ¶¶ [0307]-[0309], ¶ [0319], ¶ [0331], ¶¶ [0337]-[0339], ¶¶ [0350]-[0351], ¶¶ [0355]-[0357], ¶ [0367], ¶ [0380], ¶¶ [0386]-[0388], ¶ [0399], ¶ [0424], ¶¶ [0434]-[0435], ¶ [0443], ¶¶ [0446]-[0450], ¶¶ [0454]-[0458], ¶ [0464], FIGS. 1-11, 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶ [0009], ¶ [0011], ¶¶ [0026]-[0027], ¶ [0041], ¶ [0044], ¶¶ [0047]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 1:15-18, 2:35-3:15, 7:42-9:50, 9:53-10:2, 10:5-13:6, 13:8-41, FIGS. 3A-3D, 4A-4H; Hou414, at Abstract, 2:31-3:57, 4:19-5:11, 6:4-41, 7:4-21, FIGS. 1-13; Matsuo615, at Abstract, ¶ [0003], ¶¶ [0005]-[0008], ¶¶ [0015]-[0025], ¶¶ [0027]-[0028], ¶¶ [0036]-[0053], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Abstract, 1:22-31, 2:1-12, 5:42-6:44, 7:5-57, 8:56-9:3, FIGS. 1E-1F, 2E-2F; Nagaoka751, 13:15-32, 16:36-17:17, 20:12-38, 21:8-23, 22:5-30, 22:53-23:4, 23:44-24:27, FIGS. 1J-1P, 2C, 3D, 4C-5E, 6B-6H; Moriwaki178, 3:32-4:17, 4:28-5:13, 5:24-6:4, 6:17-64, 7:9-57, 8:1-11, 15:51-60, 16:9-16, 16:24-54, 17:34-18:23, 18:44-57, 19:30-20:17, 20:31-34, 20:54-21:40, 21:55-59, 22:5-32, 22:62-23:22, 23:30-37, 23:54-24:12, 24:21-53, 24:66-25:16, 25:26-40, Abstract, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Metz258, Abstract, ¶¶ [0003]-[0005], ¶ [0009], ¶¶ [0030]-[0036], ¶ [0049], FIGS. 1f-1i; Colombo468, Abstract, ¶¶ [0002]-[0003], ¶¶ [0006]-[0007], ¶¶ [0009]-[0012], ¶¶ [0018]-[0019], ¶ [0022], ¶¶ [0024]-[0055], FIGS. 2-10.

The silicon nitride film not being formed on any of upper surfaces of the first and second gate electrodes, *see, e.g.*, ’686 patent at 14:51-15:30, 18:42-50, FIGS. 3D-6A, 7A-8C, 10A-11C, was also well-known before the ’686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 248, Figs. 5, 6 (same); Mistry2007 presentation at 16, 19 (same); QX9650_Report, at 2, 28, 30-31, 43-44, 63, 65-67, 70-

72, 76, Figs. 2.3.1.2, 2.3.1.3, 2.3.1.14, 2.3.1.15, 2.3.2.8, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); Aoyama950 ¶¶ [0113]-[0119], FIGS. 5, 6K-6Q; Akasaka077 ¶¶ [0072]-[0074], ¶ [0087], FIGS. 16-26; Akasaka939 ¶ [0010], ¶ [0071], ¶¶ [0078]-[0079], ¶ [0086], FIGS. 10, 11B-13; Bohr559 ¶ [0018], ¶ [0021], ¶¶ [0025]-[0026], ¶¶ [0030]-[0032], ¶ [0034], ¶ [0037], ¶ [0039], ¶ [0041], ¶ [0043], FIGS. 1-10; Kavalieros277 ¶ [0022], ¶¶ [0027]-[0035], ¶ [0037], ¶ [0043], ¶¶ [0045]-[0046], FIGS. 1G-1R; Okazaki789, 3:55-4:44, 8:1-11, 12:19-13:20, 13:38-52, 14:1-17, 15:49-65, 16:4-17, TBLS. 1-2, FIGS. 2A-2I, 4A-4B; Hsu660, 2:1-38, 5:37-38, 6:19-37, 7:64-8:2, 8:35-41, FIGS. 4-11; Nakajima317, ¶ [0327], ¶ [0375], FIGS. 46-47, 5153, 55-56, 60-62; Kavalieros729, ¶ [0026], ¶ [0046], FIG. 12; Nagaoka751, 1:22-67, 2:19-3:28, 6:57-7:11, 8:34-9:20, 11:3-40, 13:33-45, 14:15-15:11, 16:30-17:17, 17:63-18:25, FIGS. 1B-6H.

The silicon nitride film causing a first stress in a gate length direction of a channel region in the first active region, *see, e.g.*, ’686 patent at 28:10-29:15, FIGS. 3D-6A, 7A-8C, 10A-11C, was also well-known before the ’686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); QX9650_Report, at 15, 27-28, 30-32, 43-44, 63, 65-67, 70-72, 76, 119, Figs. 2.3.1.2, 2.3.1.3, 2.3.1.14, 2.3.1.15, 2.3.2.8, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); James 65/45 article, at 79-80, Figs. 6, 7; James HKMG article, at 346-47, Figs. 2, 3; Mistry2007 article, at 248, Figs. 5, 6; Mistry2007 presentation, at 16, 19; James 90nm article, at 2-5, Figs. 5-6, 8-9, 10, 11-12; Hsu660, at 2:8-13, 5:37-38, 6:19-37, 7:64-8:2, 8:35-41, FIGS. 4-11; Okazaki789, at 8:1-7, 12:23-29, 14:13-17, 15:49-65, FIGS. 2I, 4B; Nagaoka751, at 2:37-40, 3:32-41, 3:55-66, 4:15-20, 4:23-33, 8:52-56, 9:15-20, 13:41-45, 14:46-48, 17:67-18:5, 24:34-36, 24:49-59, 25:32-39, FIGS. 1O, 5D, 6H; Bohr559, at Abstract, ¶¶[0001]-[0003], ¶ [0016], ¶ [0018], ¶ [0021], ¶¶ [0025]-[0026], ¶¶ [0030]-[0032], ¶ [0034], ¶¶ [0036]-[0037],

¶ [0039], ¶ [0041], ¶ [0043], ¶ [0047], ¶ [0050], ¶ [0053], FIGS. 1-10; Bohr683, at Title, Abstract, ¶ [0009], ¶¶ [0038]-[0041], ¶¶ [0048]-[0049], FIGS. 6, 8; Bohr article, at Title, 1-3, Figs. 1, 2; Hou414, at 1:65-2:3, 3:33-57, 6:54-7:3, FIG. 13; Hsu823, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0005]-[0006], ¶ [0008], ¶¶ [0012]-[0015], ¶ [0019], ¶¶ [0024]-[0027], ¶¶ [0036]-[0040], ¶ [0043], FIGS. 3, 10-13; Yu273, at Title, Abstract, 1:6-2:60, 3:5-9, 3:59-4:7, 4:17-6:64, FIGS. 6-9; Jung104, at Title, Abstract, ¶ [0001], ¶¶ [0010]-[0065], ¶ [0071], ¶¶ [0075]-[0133], TABLES III-VII, FIGS. 1A-2, 4A-15; Kavalieros729, ¶ [0001], ¶ [0026], ¶¶ [0044]-[0046], FIG. 14; Ke984, at Abstract, ¶¶ [0001]-[0009], ¶ [0015], ¶ [0020], ¶ [0022], ¶ [0027], ¶¶ [0030]-[0032], FIGS. 8-10; Alvarez069, at Abstract, ¶[0001], ¶¶ [0005]-[0008], ¶¶ [0013]-[0016], ¶¶ [0019]-[0020], ¶¶ [0022]-[0027], ¶ [0031], ¶¶ [0033]-[0035], ¶ [0037], ¶ [0043], ¶¶ [0047]-[0082], TBL. I, FIGS. 4, 9-11; ITRS_2007_PIDS, at 27; ITRS_2007_FEP, at 2-3, 19-20, 29-30, Tbl. FEP1, Fig. FEP4; Thompson Apr2004 article, at 191-93, Table 1, Fig. 1; Thompson Nov2004 article, at 1790-96, Figs. 2, 5-6, 8, 12, 13; Sun article, at 1-2, 10, 14-16, 20-21, Figs. 5-7; Eneman article, at 1446-52, Table I, Figs. 2-4, 6, 8-10; Liu article, at 836-37, Figs. 1-7; Morin article, at 355-361, 367, Tbl. I, Figs. 1, 2, 8, 15, 17; Bai article, at 657, Figs. 3, 4.

The first metal film having a thickness smaller than that of the second metal film, *see, e.g.*, ’686 patent at 11:50-55, 18:34-41, FIGS. 4B-5C, 6B-12, was also well-known before the ’686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 347, Figs. 2, 3 (same); Mistry2007 article at Fig. 6 (same); Mistry2007 presentation at 16, 19 (same); QX9650_Report, at 14-15, 24-28, 30-40, 43-56, 63-64, 67-68, 70-74, 76, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.1.14 through 2.3.1.27, 2.3.2.8, 2.3.2.9, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6, 2.4.2 (same); Aoyama950 ¶ [0098], ¶¶ [0113]-[0119], FIGS. 5, 6D, 6K-6Q; Akasaka077

¶ [0046], ¶¶ [0053]-[0054], ¶ [0077], ¶¶ [0085]-[0086], FIGS. 19-26; Akasaka939 ¶¶ [0073]-[0074], ¶ [0076], ¶¶ [0082]-[0084], ¶¶ [0086]-[0090], FIGS. 10-12; Bohr559 ¶ [0002], ¶¶ [0009]-[0014], ¶ [0018], ¶ [0021], ¶¶ [0023]-[0026], ¶¶ [0028]-[0030], ¶¶ [0034]-[0036], ¶¶ [0040]-[0045], ¶ [0047], ¶¶ [0050]-[0054], FIGS. 5-10; Kavalieros277 ¶ [0011], ¶¶ [0029]-[0040], ¶¶ [0042]-[0044], FIGS. 1I-1R; Okazaki789, at Abstract, 1:18-2:40, 2:44-3:45, 4:55-5:44, 5:6-6:16, 6:8-58, 7:23-67, 8:58-9:29, 9:35-42, 10:33-67, 11:1-16, 11:46-12:15, 12:63-13:3, 13:30-52, 13:60-14:17, 14:24-50, 14:56-15:28, 15:37-45, 16:4-17, 16:34-42, 16:52-63, FIGS. 1E-1I, 2E-2I, 3A-5B; Hsu660, 1:23-45, 1:55-67, 2:1-7, 5:47-8:34, FIGS. 2-11; Hou414, at Abstract, 2:31-3:57, 4:19-5:11, 6:4-41, 7:4-21, FIGS. 1-13; Matsuo615, at Abstract, ¶ [0009], ¶ [0015], ¶¶ [0024]-[0025], ¶¶ [0034]-[0036], ¶ [0041], ¶¶ [0049]-[0051], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Nagaoka751, 12:33-13:32, 15:12-28, 16:30-17:17, FIGS. 1J-1P, 2C, 3D, 4C-5E, 6B-6H; Moriwaki178, 20:54-21:17, FIG. 4D; Colombo468, Abstract, ¶ [0030], ¶ [0038], ¶ [0041], ¶ [0043], ¶ [0049], FIGS. 4-10.

The first and second metal films having different work functions, *see, e.g.*, ’686 patent at Abstract, 11:38-55, 15:64-16:9, 18:25-33, FIGS. 4A-12, was also well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62, 2:23-29, 2:49-60, 3:29-36, 3:42-50, 5:12-21, FIGS. 13-14E, 16; Zhang article at 50, Figs. 1, 2, 4 (incorporated by reference in the ’686 patent); Song article at 1, Figs. 1(a)-4 (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 247-49, Figs. 2, 5, 6 (same); Mistry2007 presentation at 5, 14, 15e-15j, 16, 18, 19 (same); QX9650_Report, at 2, 14-15, 24-28, 30-40, 43-56, 63-64, 67-68, 70-74, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.1.14 through 2.3.1.27, 2.3.2.8, 2.3.2.9, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6,

2.4.2 (same); Aoyama950, at Abstract, ¶ [0003], ¶¶ [0007]-[0012], ¶ [0098], ¶ [0107], ¶ [0109], ¶¶ [0115]-[0119], ¶ [0121], FIGS. 6, 6E-6Q; Akasaka077 ¶ [0003], ¶¶ [0005]-[0006], ¶¶ [0076]-[0077], ¶¶ [0080]-[0088], FIGS. 19-26; Akasaka939 ¶ [0015], ¶¶ [0053]-[0054], ¶¶ [0060]-[0062], ¶ [0064], ¶¶ [0073]-[0074], ¶ [0083], ¶ [0086], ¶¶ [0089]-[0090], FIGS. 10, 12; Bohr559 ¶ [0022], ¶ [0027], ¶ [0038], ¶¶ [0040]-[0043], ¶¶ [0045]-[0048]; Kavalieros277 ¶¶ [0036]-[0039], ¶ [0044], FIGS. 1I-1R; Okazaki789, at Abstract, 1:18-2:40, 2:44-3:45, 4:55-5:44, 5:6-6:16, 6:8-58, 7:23-67, 8:58-9:29, 9:35-42, 10:33-67, 11:1-16, 11:46-12:15, 12:63-13:3, 13:30-52, 13:60-14:17, 14:24-50, 14:56-15:28, 15:37-45, 16:4-17, 16:34-42, 16:52-63, FIGS. 1E-1I, 2E-2I, 3A-5B; Hsu660, 1:23-45, 1:55-67, 2:1-7, 5:47-8:34, FIGS. 2-11; Saito663, at Abstract, ¶ [0003], ¶¶ [0017]-[0018], ¶¶ [0027]-[0028], ¶¶ [0037]-[0038], ¶¶ [0058]-[0062], ¶¶ [0073]-[0078], ¶ [0089], ¶ [0091], ¶¶ [0093]-[0095], ¶ [0103], ¶¶ [0114]-[0115], ¶ [0121], ¶¶ [0126]-[0127], ¶ [0134], FIGS. 1E-1F, 2H-2I, 3-5, 6F-6G, 7-9; Iriyama511, at Abstract, 2:29-65, 3:51-56, 3:59-5:4, 7:12-52, 7:59-65, 9:9-54, 9:64-10:36, 12:52-67, 13:6-28, FIGS. 1A-1C, 8A-13C, 15A-20C, 26; Nakajima317, at Abstract, ¶ [0003], ¶¶ [0006]-[0008], ¶¶ [0010]-[0015], ¶¶ [0099]-[0104], ¶¶ [0106]-[0114], ¶¶ [0116]-[0122], ¶¶ [0124]-[0132], ¶¶ [0137]-[0144], ¶ [0146], ¶ [0162], ¶¶ [0177]-[0178], ¶¶ [0181]-[0182], ¶ [0197], ¶¶ [0212]-[0213], ¶¶ [0216]-[0217], ¶ [0235], ¶¶ [0253]-[0254], ¶¶ [0257]-[0258], ¶ [0276], ¶¶ [0293]-[0294], ¶¶ [0297]-[0298], ¶ [0315], ¶ [0317], ¶ [0331], ¶¶ [0337]-[0339], ¶¶ [0342]-[0343], ¶ [0363], ¶ [0365], ¶ [0380], ¶¶ [0386]-[0388], ¶¶ [0391]-[0392], ¶ [0394], ¶ [0410], ¶¶ [0423]-[0425], ¶¶ [0434]-[0435], ¶ [0438], ¶¶ [0453]-[0455], ¶ [0464], ¶ [0467], FIGS. 1-11, 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶ [0009], ¶ [0011], ¶¶ [0026]-[0027], ¶ [0041], ¶ [0044], ¶¶ [0047]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 1:15-18, 2:35-3:15, 7:42-9:50, 9:53-10:2, 10:5-13:6, 13:8-41, FIGS. 3A-3D, 4A-4H; Hou414, at

Abstract, 2:31-3:57, 4:19-5:11, 6:4-41, 7:4-21, FIGS. 1-13; Matsuo615, at Abstract, ¶ [0007], ¶ [0015], ¶ [0019], ¶ [0021], ¶¶ [0024]-[0026], ¶ [0036], ¶ [0042], ¶ [0045], ¶ [0049], ¶ [0053], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Abstract, 1:22-31, 2:1-12, 5:42-6:44, 7:5-57, 8:56-9:3, FIGs. 1E-1F, 2E-2F; Nagaoka751, 13:15-32, 16:36-17:17, 20:12-38, 21:8-23, 22:5-30, FIGS. 1J-1P, 2C, 3D, 4C-5E, 6B-6H; Moriwaki178, 3:66-4:17, 4:62-5:13, 5:53-6:4, 6:46-64, 7:41-57, 15:51-60, 16:9-16, 16:24-54, 17:34-18:23, 18:44-57, 19:30-20:17, 20:54-21:40, 22:5-32, 22:62-23:22, 23:30-37, 23:54-24:12, 24:21-53, 24:66-25:16, 25:26-40, Abstract, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Metz258, ¶ [0030], ¶ [0033], ¶ [0049], FIGS. 1f-1i; Colombo468, Abstract, ¶ [0003], ¶¶ [0006]-[0008], ¶¶ [0010]-[0012], ¶ [0018], ¶¶ [0020]-[0022], ¶ [0024], ¶ [0027], ¶ [0033], ¶ [0036], ¶¶ [0039]-[0056], FIGS. 2-10; Westlinder article, at 550-552.

The silicon nitride film having a thickness smaller than that of the first gate electrode, *see, e.g.*, ’686 patent at 11:38-55, 14:51-54, 18:42-50, FIGS. 3D-5C, 7A-8C, 10A-11C, was also well-known before the ’686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 248, Fig. 6 (same); Mistry2007 presentation at 16, 19 (same); QX9650_Report, at 14-15, 26-28, 30-32, 43-44, 63, 65-67, 70-72, 76, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1.2, 2.3.1.3, 2.3.1.14, 2.3.1.15, 2.3.2.8, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); Aoyama950 Abstract, ¶ [0003], ¶¶ [0007]-[0031], ¶¶ [0098], ¶¶ [0113]-[0119], FIGS. 5, 6K-6Q; Akasaka077 ¶¶ [0072]-[0074], ¶ [0087], FIGS. 16-26; Akasaka939 ¶ [0010], ¶ [0071], ¶¶ [0073]-[0074], ¶ [0076], ¶¶ [0078]-[0079], ¶¶ [0082]-[0084], ¶¶ [0086]-[0090], FIGS. 10-12; Kavalieros277 ¶ [0011], ¶¶ [0022]-[0029], ¶¶ [0037]-[0039], ¶¶ [0043]-[0045], FIGS. 1G-1R; Okazaki789, 3:55-4:44, 8:1-11, 12:19-13:20, 13:38-52, 14:1-17, 15:49-65, 16:4-17, 17:6-10, TBLS. 1-2, FIGS. 2A-2I, 4A-4B; Hsu660, 1:23-45, 1:55-67, 2:1-7, 5:47-8:34,

FIGS. 2-11; Hsu823, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0005]-[0006], ¶ [0008], ¶¶ [0012]-[0015], ¶ [0019], ¶¶ [0024]-[0026], ¶ [0028], ¶¶ [0036]-[0038], ¶ [0040], ¶¶ [0042]-[0043], FIGS. 3, 10-13; Jung104, at Abstract, ¶ [0016], ¶ [0018], ¶ [0029], ¶ [0031], ¶ [0076], ¶ [0077], ¶ [0102], TABLES I-II, FIGS. 1B-1C, 7B; Yu273, 4:17-36, FIGS. 6-7; Nakajima317, ¶ [0304], ¶¶ [0307]-[0308], ¶ [0317], ¶ [0326], ¶ [0352], ¶¶ [0355]-[0356], ¶ [0358], ¶ [0365], ¶ [0374], FIGS. 46-47, 5153, 55-56, 60-62; Nagaoka751, 2:25-3:14, 13:33-14:56, 16:50-17:17, 17:63-18:25, FIGS. 1B-6H; James 90nm article, at Figs. 1-3, 5-6, 8-12; James HKMG article, at Figs. 2, 3 (same); Thompson Nov2004 article, at Figs. 2, 4; Morin article, at Fig. 1.

The conductive film being made of the second metal film, *see, e.g.*, ’686 patent at 6:14-15, 15:64-16:22, 16:55-60, 17:39-47, 17:50-18:41, FIGS. 5A-5C, 6B, was also well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62; Zhang article at 50, Figs. 1, 2, 4 (incorporated by reference in the ’686 patent); Song article at 1, Fig. 1(b) (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 248, Figs. 5, 6 (same); Mistry2007 presentation at 15e-15j, 16, 19 (same); QX9650_Report, at 2, 14-15, 24-28, 30-40, 43-56, 63-64, 67-68, 70-74, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.1.14 through 2.3.1.27, 2.3.2.8, 2.3.2.9, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6, 2.4.2 (same); Akasaka077 ¶¶ [0084]-[0088], FIGS. 25, 26; Akasaka939 ¶¶ [0068]-[0070], ¶ [0074], ¶¶ [0076]-[0079], ¶¶ [0084]-[0086], ¶¶ [0088]-[0090], FIGS. 10-12; Bohr559 ¶¶ [0047]-[0049], FIGS. 5-10; Hsu660, 7:34-63, FIGS. 8-11; Iriyama511, 7:35-39, 7:59-65, 9:34-45, 9:64-65, 9:64-10:36, 11:28-33, 11:64-65, 12:33-36, 12:52-67, 13:6-32, FIGS. 1A-1C, 8A-13C, 15A-20C, 26; Nakajima317, ¶¶ [0107]-[0114], ¶¶[0117]-[0121], ¶¶ [0125]-[0132], ¶¶ [0140]-[0144], ¶¶ [0150]-[0151], ¶¶ [0155]-[0159], ¶ [0168],

¶¶ [0177]-[0178], ¶¶ [0185]-[0186], ¶¶ [0190]-[0191], ¶ [0203], ¶¶ [0212]-[0213], ¶¶ [0222]-[0223], ¶¶ [0227]-[0229], ¶ [0244], ¶¶ [0253]-[0254], ¶¶ [0263]-[0264], ¶ [0268] ¶ [0270], ¶ [0284], ¶¶ [0293]-[0294], ¶ [0319], ¶ [0331], ¶¶ [0337]-[0339], ¶¶ [0350]-[0351], ¶¶ [0355]-[0357], ¶ [0367], ¶ [0380], ¶¶ [0386]-[0388], ¶ [0399], ¶ [0424], ¶¶ [0434]-[0435], ¶ [0443], ¶¶ [0446]-[0450], ¶¶ [0454]-[0458], ¶ [0464], FIGS. 4-8, 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶ [0009], ¶ [0011], ¶¶ [0026]-[0033], ¶ [0041], ¶ [0044], ¶¶ [0047]-[0048], FIGS. 2D-2G, 4A-4D; Matsuo615, at Abstract, ¶¶ [0020]-[0025], ¶¶ [0027]-[0028], ¶¶ [0043]-[0052], FIGS. 1I, FIGS. 2A-2B, 3J, 4A-4B; Brask784, at Abstract, 2:1-12, 6:19-44, 7:21-57, 8:56-9:3, FIGS. 1E-1F, 2E-2F; Nagaoka751, 8:3-21, 11:3-48, 13:15-13:32, 16:30-17:17, 20:12-38, 21:8-42, 22:15-30, 22:53-23:21, 23:46-24:27, 25:14-23, FIGS. 1J-1P, 2C, 3D, 4C-5E, 6B-6H; Metz258, Abstract, ¶ [0009], ¶¶ [0032]-[0036], ¶ [0049], FIGS. 1f-1i; Colombo468, ¶¶ [0041]-[0045], ¶ [0049], FIGS. 5-10.

The first and second gate insulating films being made of the same insulating material, *see, e.g.*, ’686 patent at 11:25-12:7, 16:16-22, 17:31-18:24, 18:51-53, 19:25-41, 20:49-51, 21:18-24, 22:33-41, 23:11-15, 29:16-40, FIGS. 1B-5C, 6B-9, was well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62, 2:1-3:4, FIG. 13; Zhang article at 50, Figs. 1-4 (incorporated by reference in the ’686 patent); Song article at 1, Fig. 1(b) (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 247-48, Figs. 2, 5, 6 (same); Mistry2007 presentation at 15a-15j, 16 (same); QX9650_Report, at 2, 14-15, 24-28, 30-40, 43-56, 63-64, 67-68, 70-74, 76, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.1.14 through 2.3.1.27, 2.3.2.8, 2.3.2.9, 2.3.2.11, 2.3.2.12, 2.3.3.2 through 2.3.3.6, 2.4.2 (same); Aoyama950, at Abstract, ¶ [0003], ¶ [0006], ¶¶ [0008]-[0031],

¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶¶ [0115]-[0117], ¶ [0119], FIGS. 5, 6D-6Q; Akasaka077 ¶ [0003], ¶ [0006], ¶ [0075], ¶¶ [0082]-[0083], ¶¶ [0087]-[0088], FIGS. 19-26; Akasaka939 ¶¶ [0069]-[0070], ¶¶ [0072]-[0073], ¶¶ [0080]-[0090], FIGS. 10-12; Bohr559 ¶¶ [0002]-[0003], ¶ [0005], ¶ [0008], ¶¶ [0016]-[0022], ¶¶ [0024]-[0027], ¶¶ [0029]-[0033], ¶¶ [0035]-[0043], ¶ [0046], ¶ [0048], ¶ [0050], ¶ [0053], FIGS. 1-10; Kavalieros277 ¶¶ [0002]-[0003], ¶¶ [0007]-[0011], ¶¶ [0013]-[0018], ¶¶ [0025]-[0026], ¶¶ [0034]-[0037], ¶¶ [0042]-[0043], FIGS. 1A-1R; Okazaki789, at Abstract, 1:44-51, 1:58-65, 2:15-24, 2:44-64, 3:3-19, 3:25-40, 6:8-51, 7:23-46, 8:48-58, 9:35-10:67, 12:63-13:29, 14:24-30, 14:56-15:21, 16:4-17, 16:57-63, 17:6-10, FIGS. 1C-1I, 2C-2I, 3A-5B; Jung104, ¶ [0008], ¶¶ [0035]-[0037], ¶ [0079], ¶ [0084], ¶ [0105], FIGS. 1A-1C; Jung104, ¶ [0008], ¶¶ [0035]-[0037], ¶ [0079], ¶ [0084], ¶ [0105], FIGS. 1A-1C; Saito663, at Abstract, ¶ [0005], ¶¶ [0008]-[0038], ¶¶ [0050]-[0053], ¶¶ [0055]-[0056], ¶¶ [0058]-[0059], ¶¶ [0061]-[0062], ¶ [0064], ¶ [0067], ¶ [0071], ¶¶ [0073]-[0078], ¶ [0080], ¶¶ [0083]-[0084], ¶ [0086], ¶¶ [0089]-[0090], ¶¶ [0092]-[0095], ¶¶ [0097]-[0100], ¶¶ [0103]-[0105], ¶¶ [0109]-[0112], ¶¶ [0115]-[0124], ¶¶ [0127]-[0130], ¶ [0133], FIGS. 1A-1F, 2E-2I, 3-5, 6A-6G, 7-9; Iriyama511, 7:8-11, 7:30-34, 9:5-8, 9:14-19, 9:29-33, 11:55-60, 12:11-13, 13:1-5, FIGS. 1A-1C, 5A-13C, 15A-20C, 25A-25B, 26; Nakajima317, at Abstract, ¶¶ [0010]-[0015], ¶ [0100], ¶ [0107], ¶ [0117], ¶ [0125], ¶ [0150], ¶ [0163], ¶ [0179], ¶ [0185], ¶ [0198], ¶ [0214], ¶ [0222], ¶ [0236], ¶ [0255], ¶ [0263], ¶ [0277], ¶ [0295], ¶ [0302], ¶¶ [0340]-[0341], ¶ [0350], ¶ [0364], ¶¶ [0389]-[0390], ¶ [0399], ¶ [0436], ¶ [0443], ¶ [0465], FIGS. 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶¶ [0006]-[0007], ¶¶ [0009]-[0011], ¶ [0013], ¶¶ [0020]-[0026], ¶¶ [0040]-[0041], ¶¶ [0043]-[0044], ¶¶ [0047]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 2:35-3:15, 10:5-15, 11:43-46, 11:67-12:5, 12:63-13:6, 13:8-16, 13:33-36, FIGS. 3A-3D, 4A-4H; Hou414, 2:31-3:57, 4:19-5:11,

5:64-6:36, FIGS. 1-13; Matsuo615, at Abstract, ¶¶ [0005]-[0006], ¶[0014], ¶ [0018], ¶ [0024], ¶¶ [0027]-[0028], ¶ [0035], ¶ [0039], ¶¶ [0046]-[0047], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Title, Abstract, 1:8-10, 1:14-21, 1:32-48, 2:4-12, 2:19-42, 4:17-5:32, 7:5-12, 8:56-9:3, FIGS. 1C-1F, 2C-2F; Bohr683, at Abstract, ¶ [0014], ¶ [0038], FIGS. 1-6; Nagaoka751, 9:65-10:22, 11:3-18, 12:31-42, FIGS. 1D-6H; Moriwaki178, 15:42-47, 16:24-31, 17:60-67, 18:35-42, 19:25-28, 19:54-61, 20:49-52, 21:10-17, 21:64-22:4, 22:58-61, 23:30-38, 23:49-52, 24:21-28, 25:17-24, FIGS. 1H, 2D, 3D, 4D, 5F, 6F; Alvarez069, ¶ [0039], FIGS. 5-11; Murthy482, 3:47-4:38, FIGS. 1a-1c; Metz258, Abstract, ¶ [0002], ¶¶ [0004]-[0005], ¶ [0009], ¶¶ [0022]-[0029], ¶ [0049], FIGS. 1c-1i; Colombo468, Abstract, ¶¶ [0004]-[0011], ¶ [0022], ¶¶ [0025]-[0026], ¶[0028], ¶ [0047], ¶ [0055], FIGS. 1-10.

Source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region, *see, e.g.*, ’686 patent at 13:12-45, 18:4-24, 19:54-20:20, 23:28-33, 28:63-29:15, FIGS. 2C-5C, 7A-8C, 10A-11C, were also well-known before the ’686 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, James 65/45 article at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 346-47, Figs. 2, 3 (same); Mistry2007 article at 248-49, Figs. 5, 6 (same); Mistry2007 presentation at 14, 15a-15j, 16, 19, 35 (same); QX9650_Report, at 2, 14-15, 19-20, 26-28, 30-32, 41-42, 60, 62-63, 77, 79, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.2.2, 2.2.3, 2.3.1.2, 2.3.1.3, 2.3.1.12, 2.3.1.13, 2.3.2.5, 2.3.2.7, 2.3.2.8, 2.4.4, 2.4.5 (same); Hsu823 ¶ [0002], ¶ [0028], ¶¶ [0031]-[0033], ¶ [0035], ¶¶ [0037]-[0039], ¶ [0041], FIGS. 5-14; Ke984, at Abstract, ¶¶ [0001]-[0009], ¶ [0021], FIG. 5B; Hsu660, at 4:35-40, 5:3-9, 6:19-31, 8:35-41, FIGS. 4-11; Bohr559, at Abstract, ¶¶ [0001]-[0003], ¶¶ [0015]-[0016], ¶ [0018], ¶¶ [0020]-[0021], ¶ [0024], ¶ [0031], ¶¶ [0036]-[0037], ¶ [0039],

¶ [0050], ¶ [0053], FIGS. 1-10; Bohr683, at Title, Abstract, ¶¶ [0022]-[0039], ¶ [0041], ¶¶ [0043]-[0050], FIGS. 3-6, 8; Bohr article, at 1-3, Figs. 1, 2; Hou414, at 4:19-23, 5:12-40, FIGS. 3-13; Hsu823, ¶ [0002], ¶ [0028], ¶¶ [0031]-[0033], ¶ [0035], ¶¶ [0037]-[0039], ¶ [0041], FIGS. 5-14; Murthy151, at Abstract, ¶ [0005], ¶ [0021], ¶¶ [0034]-[0035], ¶¶ [0040]-[0041], ¶¶ [0046]-[0048], ¶ [0057], ¶ [0060], ¶¶ [0063]-[0074], ¶¶ [0081]-[0082], ¶ [0085], ¶ [0102], ¶¶ [0115]-[0117], ¶¶ [0122]-[0125], FIGS. 2-12; Murthy482, Abstract, 1:41-2:15, 4:39-7:10, 8:6-9:63, FIGS. 2-8; Kavalieros729, at Title, Abstract, ¶¶ [0001]-[0002], ¶¶ [0024]-[0025], ¶ [0040], ¶ [0043], FIGS. 4-13; Kavalieros277 ¶ [0007], ¶¶ [0023]-[0025], ¶ [0027]; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶ [0006], ¶ [0016], ¶¶ [0020]-[0021], ¶ [0023], ¶ [0032], FIG. 10; ITRS_2007_PIDS, at 16, 26, 27, 56, Tbl. PIDS1a, PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, Figs. PIDS5, PIDS10; ITRS_2007_FEP, at 1-3, 10-13, 16, 17, 19-20, 29, 33 n.1, 35, 58-59, Tbl. FEP1, Figs. FEP1-FEP5; James 90nm article, at 2-3, Fig. 6; Thompson Apr2004 article, at 191-93, Fig. 1; Thompson Nov2004 article, at 1790-96, Figs. 2-5, 9-11, 13; Sun article, at 1-4, 7-16, 21, Figs. 5-8, 11, 12; Bai article, at 657, Fig. 4.

The first and second gate insulating films including a high-k film made of a metal oxide having a relative dielectric constant of 10 or more, *see, e.g.*, ’686 patent at 6:62-65, 11:25-37, 29:16-40, was well-known before the ’686 patent, *see, e.g.*, *id.* at 1:14-62; Zhang article at 50, Figs. 1-4 (incorporated by reference in the ’686 patent); Song article at 1, Figs. 1(a), 1(b), 4 (same). The prior art is replete with teachings that confirm this admission in the ’686 patent. *See, e.g.*, James 65/45 article at 79, Figs. 6, 7 (describing Intel_686_Products); James HKMG article at 347, Figs. 2, 3 (same); Mistry2007 article at 247-48, Figs. 2, 5, 6 (same); Mistry2007 presentation at 4, 5, 7, 8, 14, 15a-15j, 16, 25, 35 (same); QX9650_Report, at 2, 14-15, 24-28, 30-40, 43-56, 64, 68, 73-74, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1, 2.3.2, 2.3.1.2 through 2.3.1.11, 2.3.1.14 through

2.3.1.27, 2.3.2.9, 2.3.2.12, 2.3.3.4 through 2.3.3.6 (same); Aoyama950, at Abstract, ¶ [0003], ¶ [0006], ¶¶ [0008]-[0031], ¶¶ [0098], ¶¶ [0106]-[0107], ¶ [0110], ¶ [0117], FIGS. 5, 6D-6Q; Akasaka077 ¶ [0006], ¶ [0044], ¶ [0051], ¶ [0075], ¶¶ [0087]-[0088], FIGS. 19-26; Akasaka939 ¶ [0004], ¶¶ [0069]-[0070], ¶¶ [0072]-[0073], ¶¶ [0080]-[0090], FIGS. 10-12; Bohr559 ¶¶ [0002]-[0003], ¶ [0005], ¶ [0008], ¶¶ [0016]-[0022], ¶¶ [0024]-[0027], ¶¶ [0029]-[0033], ¶¶ [0035]-[0043], ¶ [0046], ¶ [0048], ¶ [0050], ¶ [0053], FIGS. 1-10; Okazaki789, at Abstract, 1:44-51, 1:58-65, 2:15-24, 2:44-64, 3:3-19, 3:25-40, 6:8-51, 7:23-46, 8:48-58, 9:35-10:67, 12:63-13:29, 14:24-30, 14:56-15:21, 16:4-17, 16:57-63, FIGS. 1C-1I, 2C-2I, 3A-5B; Hsu660, at Abstract, 1:35-54, 2:32-38, 2:47-4:40, 5:9-46, 6:10-7:8, 7:64-8:2, 8:26-34, FIGS. 1-11; Saito663, ¶ [0052], ¶¶ [0097]-[0098], ¶ [0105], ¶¶ [0109]-[0110], ¶ [0117], ¶ [0119], ¶ [0121], ¶ [0129], ¶ [0133], FIGS. 1A-1F, 2E-2I, 3-5, 6A-6G, 7-9; Iriyama511, 7:8-11, 7:30-34, 9:5-8, 9:14-19, 9:29-33, 11:55-60, 12:11-13, 13:1-5, FIGS. 1A-1C, 5A-13C, 15A-20C, 25A-25B, 26; Nakajima317, at Abstract, ¶¶ [0010]-[0015], ¶ [0100], ¶ [0107], ¶ [0117], ¶ [0125], ¶ [0150], ¶ [0163], ¶ [0179], ¶ [0185], ¶ [0198], ¶ [0214], ¶ [0222], ¶ [0236], ¶ [0255], ¶ [0263], ¶ [0277], ¶ [0295], ¶ [0302], ¶¶ [0340]-[0341], ¶ [0350], ¶ [0364], ¶¶ [0389]-[0390], ¶ [0399], ¶ [0436], ¶ [0443], ¶ [0465], FIGS. 14, 16-20, 22, 24-28, 30, 32-36, 38, 40-44, 46, 48-53, 55, 57-62, 64, 66-73, 75, 77-79; Yamaguchi167, at Abstract, ¶¶ [0006]-[0007], ¶¶ [0009]-[0011], ¶ [0013], ¶¶ [0020]-[0026], ¶¶ [0040]-[0041], ¶¶ [0043]-[0044], ¶¶ [0047]-[0048], FIGS. 2D-2G, 4A-4D; Saito631, at Abstract, 2:35-3:15, 10:5-15, 11:43-46, 11:67-12:5, 12:63-13:6, 13:8-16, 13:33-36, FIGS. 3A-3D, 4A-4H; Hou414, 2:31-3:57, 4:19-5:11, 5:64-6:36, FIGS. 1-13; Matsuo615, at Abstract, ¶ [0005], ¶ [0014], ¶ [0018], ¶ [0035], ¶ [0039], FIGS. 1A-1I, FIGS. 2A-2B, 3A-3J, 4A-4B; Brask784, at Title, Abstract, 1:8-10, 1:14-21, 1:32-48, 2:4-12, 2:19-42, 4:17-5:32, 7:5-12, 8:56-9:3, FIGS. 1C-1F, 2C-2F; Murthy151, ¶ [0028], ¶ [0073], FIGS. 1-12; Nagaoka751, 1:22-55, 2:42-47, 9:65-10:22, 11:3-18, 12:31-54,

15:12-22, FIGS. 1D-6H; Moriwaki178, 15:42-47, 16:24-31, 17:60-67, 18:35-42, 19:25-28, 19:54-61, 20:49-52, 21:10-17, 21:64-22:4, 22:58-61, 23:30-38, 23:49-52, 24:21-28, 25:17-24; Akasaka939 ¶¶ [0003]-[0004]; Baklanov, at xiii; Colombo468 ¶ [0025]; ITRS_2007_FEP, at 2, 20; ITRS_2007_PIDS, at 1, 6, 8, 27, Fig. PIDS5; Kavalieros277 ¶¶ [0002]-[0003], ¶¶ [0007]-[0011], ¶¶ [0013]-[0018], ¶¶ [0025]-[0026], ¶¶ [0034]-[0037], ¶¶ [0042]-[0043], FIGS. 1A-1R; Kavalieros729, ¶¶ [0032]-[0036], ¶ [0039], ¶ [0045], FIGS. 10-13; Ji704, at 8:27-31; Yu273, at 3:21-34; Alvarez069, ¶ [0039], FIGS. 5-11; Metz258, Abstract, ¶ [0002], ¶¶ [0004]-[0005], ¶ [0009], ¶¶ [0022]-[0029], ¶ [0049], FIGS. 1c-1i; Colombo468, Abstract, ¶¶ [0004]-[0011], ¶ [0022], ¶¶ [0025]-[0026], ¶[0028], ¶ [0047], ¶ [0055], FIGS. 1-10.

In sum, by the time the application for the ’686 patent was filed, HKMG MISFETs as claimed were well known because all the above was well known in the art before the earliest listed priority date for the ’686 patent, and a POSITA would have found it obvious to combine any and/or all the above features to create a semiconductor device comprising: a first MIS transistor; and a second MIS transistor, wherein: the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate; a first gate electrode including a second metal film formed on the first gate insulating film; first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers, the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate; a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film; second sidewall spacers formed on side surfaces of the second gate electrode, the second

sidewall spacers being insulative; and the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers, the first and second metal films are made of different metal materials, the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region, including such a semiconductor device (1) wherein the first metal film has a thickness smaller than that of the second metal film; (2) wherein the first and second metal films have different work functions; (3) wherein the silicon nitride film has a thickness smaller than that of the first gate electrode; (4) wherein the conductive film is made of the second metal film; (5) wherein the first and second gate insulating films are made of the same insulating material; (6) wherein the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more; or (7) further comprising: source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.

A POSITA would have logically and predictably consulted all of the references together to design a HKMG MISFET. Further, the general background knowledge described above would have provided the basis for combining any number of known MISFET design features together. All these MISFET design features were already known in the art, and a POSITA would have expected that combining any or all of these features to yield predictable results, would have found it obvious to substitute one known feature for another to obtain predictable results, would have found it obvious to use known techniques to improve similar devices in the same way, would have found it obvious to apply a known technique to a known device that was ready for improvement

to yield predictable results, would have found it obvious to try different combinations of device features because the techniques were known alternatives, would have found it obvious to try improving a semiconductor device, and would have reasonably expected to succeed because all these features were already known and combined previously in various ways. With respect to the prior art references in Exhibits 686-01 through 686-09, a POSITA would have been motivated to combine any of the references identified as prior art to the ’686 patent and would have reasonably expected to succeed for the reasons provided above and for additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar MISFET device structures within relevant timeframes, and the teachings of any one reference are applicable to other references in the same field.

Second, a POSITA would have been motivated to combine teachings from references that disclose certain specific features—e.g., high-k gate dielectrics, metal gate electrodes, epitaxial SiGe source/drain regions, and/or stress-inducing silicon nitride contact etch-stop layers (“CESLs”) (including CESLs that are thinner than the gate electrodes and that have been planarized to the top of the gate electrodes)—with teachings from other references that relate to similar MISFETs because all such references identified herein for the ’686 patent teach contemporaneously well-known and mutually compatible features of MISFETs, including high-k gate dielectrics, metal gate electrodes, epitaxial SiGe source/drain regions, and stress-inducing silicon nitride CESLs. Moreover, well-known contemporaneous commercial embodiments (not to mention a litany of research articles, patents, and other disclosures) demonstrate a reasonable likelihood of success in doing so. *See generally, e.g.*, Mistry2007 article; Mistry2007 presentation; James 65/45 article; James 90nm article; Bai article; Tyagi article; Thompson Nov2004 article; Thompson Apr2004 article.

A POSITA would have also been motivated and reasonably expected to succeed when attempting to replace and/or combine a reference's exact set of materials, components, or configurations in a particular MISFET device structure with other materials, components, and configurations used in similar MISFET device structures for all the reasons provided above and below. Such modifications would have been a simple addition or substitution of one known element to yield predictable results because such features were already well known in the art. The addition or substitution of one component, material, or configuration would not have materially changed the principle of operation for any reference in such a combination of teachings because the constituent references use similar device features for similar purposes: designing and making MISFETs, including HKMG MISFETs.

A POSITA would have found it obvious to combine such prior-art features (e.g., high-k gate dielectrics, metal gate electrodes, epitaxial SiGe source/drain regions, and/or CESLs) according to known methods to yield predictable results.[15] A POSITA would have been motivated to combine these teachings, and to make related additions or substitutions, because all of these MISFET device structures, materials, and configurations were widely known and used in compatible and synergistic ways. Accordingly, a POSITA would have reasonably expected to succeed given the considerations discussed above, the similarities in teachings, and because the claimed components and configurations of such MISFET devices were well known at the time. Implementing any of the identified combinations and any necessary modifications would have involved no more than routine trial and error based on the teachings in the prior art.

[15] A POSITA would have understood that these were all suitable design choices and also would have understood the benefits and tradeoffs of each design choice. There would have been no unexpected results from any particular combination of these design choices.

As one example, to the extent that any of Akasaka077, Akasaka939, Aoyama950, Bohr559, Hsu660, Kavalieros277, or Okazaki789 do not disclose that "the silicon nitride film has a thickness smaller than that of the first gate electrode," as claimed, a POSITA would have found it obvious based on their disclosures alone.

First, their respective gate electrodes are planarized to the tops of the gate electrodes, such that the silicon nitride film must be thinner than gate electrodes so long as their respective interlayer dielectric layers are thicker than their respective gate dielectric films. A POSITA would have expected any interlayer dielectric layer to be thicker than the gate dielectric film. *See, e.g.*, Nakajima317, ¶ [0317], ¶ [0326], FIG. 52. A POSITA would have known the thickness of a gate dielectric film is negligible compared to the height of the gate electrode. *See, e.g.*, James 90nm article, at Figs. 1-3, 5-6, 8-12; Mistry2007 article, at Fig. 6 (describing Intel_686_Products); Mistry2007 presentation, at 16, 19 (same); James 65/45 article, at Figs. 6, 7 (same); James HKMG article, at Figs. 2, 3 (same); QX9650_Report, at 14-15, 26-28, 30-32, 43-44, 63, 65-67, 70-72, 76, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1.2, 2.3.1.3, 2.3.1.14, 2.3.1.15, 2.3.2.8, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); Thompson Nov2004 article, at Figs. 2, 4; Morin article, at Fig. 1; Akasaka077, at FIG. 26; Akasaka939, at FIGS. 12, 13; Aoyama950, at FIG. 5; Hsu660, at FIG. 10; Okazaki, at FIGS. 2I, 4B; Nagaoka751, at FIG. 1O; Kavalieros277, at FIG. 1R; Bohr559, at FIG. 8. The gate dielectric is famously very thin to maximize capacitance. *See, e.g.*, Baklanov, at xiii. Interlayer dielectrics, on the other hand, require low capacitance and are much thicker: "gate and interlayer (ILD) dielectric films" have "opposing requirements" in that regard. *Id.*

Second, when "there are a finite number of identified, predictable solutions, a [POSITA] has good reason to pursue the known options within his or her technical grasp." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007). Because the silicon nitride films in Akasaka077,

Akasaka939, Aoyama950, Bohr559, Hsu660, Intel_686_Products, Kavalieros277, and Okazaki789 have been planarized to the tops of the gate electrodes, a POSITA would have recognized a design need to form the silicon nitride film and the inter-layer dielectric layer in a limited space between the substrate surface and the top of the gate electrodes. There are only two "identified, predictable solutions": the silicon nitride film is either thinner than the gate electrode, or it is not.[16] *See Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020) (holding that two is a "finite number of identified, predictable solutions"); *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2009) (holding the same for three options). Of those options, a silicon nitride film that is thinner than the gate electrode was known (in fact, expected) and therefore within the technical grasp of a POSITA and obvious. *See, e.g.*, Mistry2007 article, at Fig. 6 (describing Intel_686_Products); Mistry2007 presentation, at 16, 19 (same); James 65/45 article, at Figs. 6, 7 (same); James HKMG article, at Figs. 2, 3 (same); QX9650_Report, at 14-15, 26-28, 30-32, 43-44, 63, 65-67, 70-72, 76, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1.2, 2.3.1.3, 2.3.1.14, 2.3.1.15, 2.3.2.8, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); James 90nm article, at Figs. 1-3, 5-6, 8-12; Morin article, at Fig. 1; Thompson Nov2004 article, at Fig. 2.

Third, a POSITA would have understood that silicon nitride etch stop ("CESL") films like the ones in Akasaka077, Akasaka939, Aoyama950, Bohr559, Hsu660, Intel_686_Products, Kavalieros277, and Okazaki789 "ha[ve] a typical thickness of 20 nm" or so—much less than their respective gate electrode thicknesses. Eneman article, at 1446; *see also, e.g.*, Nakajima317 ¶ [0317], ¶ [0326], FIG. 52. A POSITA thus would have found it obvious to make the CESL film thinner than the gate electrode. *See Pfizer Inc. v. Sano*[fi] *Pasteur Inc.*, 94 F.4th 1341, 1348 (Fed. Cir.

[16] At most, there are only three options: the silicon nitride film is thinner than the gate electrode, thicker than the gate electrode, or the same thickness as the gate electrode. Whether there can be said to be two vs. three options is immaterial here.

2024) (finding obviousness where "techniques and conditions were routine such that a [POSITA] would have understood the claimed [property] to be 'typical'").

Fourth, where claimed "dimensions were known to be result-effective variables," "it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Applied Materials*, 692 F.3d 1289, 1295 (Fed. Cir. 2012) (quoted source omitted). Such dimensions are only patentable if they produce a "new and unexpected result" that differs in kind, not degree, from the prior art. *Id.* at 1297; *see also In re Geisler*, 116 F.3d 1465, 1469-70 (Fed. Cir. 1997). Here, the silicon nitride CESL film thickness was known to affect stress. *See generally, e.g.*, Eneman article; Hsu823 ¶ 0019], ¶¶ [0024]-[0027], FIG. 3. Implementing the CESL film to be thinner than the gate electrode, as claimed, would have yielded no unexpected results, as the relationship between silicon nitride film thickness and stress was known and predictable. *See generally, e.g.*, Eneman article; Hsu823 ¶ 0019], ¶¶ [0024]-[0027], FIG. 3.

Additionally, to the extent that any of Akasaka077, Akasaka939, Aoyama950, Bohr559, Hsu660, Kavalieros277, or Okazaki789 do not disclose that "the silicon nitride film has a thickness smaller than that of the first gate electrode," as claimed, a POSITA would have found it obvious to combine it with, e.g., Intel_686_Products, Nakajima317, James 90nm article, Mistry2007 article, Mistry2007 presentation (same), and/or Thompson Nov2004 article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a silicon nitride film, and a POSITA would have been motivated to consult references that disclose known options for its thickness relative to the gate electrodes. *See, e.g.*, Nakajima317, ¶ [0317], ¶ [0326], FIG. 52; James 90nm article, at Figs. 1-3, 5-6, 8-12; Mistry2007 article, at Fig. 6 (describing Intel_686_Products); Mistry2007 presentation, at 16, 19 (same); James 65/45 article, at Figs. 6, 7 (same); James HKMG article, at Figs. 2, 3 (same); QX9650_Report, at 14-15, 26-28,

30-32, 43-44, 63, 65-67, 70-72, 76, Tbls. 4.0.1, 4.0.2, Figs. 2.3.1.2, 2.3.1.3, 2.3.1.14, 2.3.1.15, 2.3.2.8, 2.3.2.10, 2.3.2.11, 2.3.3.2 through 2.3.3.4, 2.4.2 (same); Thompson Nov2004 article, at Figs. 2, 4; Morin article, at Fig. 1.

As another example, to the extent that any of Akasaka077, Akasaka939, Aoyama950, Intel_686_Products, or Kavalieros277 do not disclose that "the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region," as claimed, a POSITA would have found it obvious to combine it with, e.g., Hsu660, Okazaki789, Bohr559, Bohr683, Bohr article, Hou414, Hsu823, Yu273, Jung104, Kavalieros729, Ke984, Alvarez069, James 90nm article, Thompson Apr2004 article, Thompson Nov2004 article, Eneman article, and/or Bai article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for improving the electron mobility and accompanying device performance in HKMG MISFETs. *See, e.g.*, James 65/45 article, at 79-80, Figs. 6, 7; James HKMG article, at 346-47, Figs. 2, 3; Mistry2007 article, at 248, Figs. 5, 6; Mistry2007 presentation, at 16, 19; James 90nm article, at 2-5, Figs. 5-6, 8-9, 10, 11-12; Hsu660, at 2:8-13, 5:37-38, 6:19-37, 7:64-8:2, 8:35-41, FIGS. 4-11; Okazaki789, at 8:1-7, 12:23-29, 14:13-17, 15:49-65, FIGS. 2I, 4B; Nagaoka751, at 2:37-40, 3:32-41, 3:55-66, 4:15-20, 4:23-33, 8:52-56, 9:15-20, 13:41-45, 14:46-48, 17:67-18:5, 24:34-36, 24:49-59, 25:32-39, FIGS. 1O, 5D, 6H; Bohr559, at Abstract, ¶¶[0001]-[0003], ¶ [0016], ¶ [0018], ¶ [0021], ¶¶ [0025]-[0026], ¶¶ [0030]-[0032], ¶ [0034], ¶¶ [0036]-[0037], ¶ [0039], ¶ [0041], ¶ [0043], ¶ [0047], ¶ [0050], ¶ [0053], FIGS. 1-10; Bohr683, at Title, Abstract, ¶ [0009], ¶¶ [0038]-[0041], ¶¶ [0048]-[0049], FIGS. 6, 8; Bohr article, at Title, 1-3, Figs. 1, 2; Hou414, at 1:65-2:3, 6:54-7:3, FIG. 13; ; Hsu823, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0005]-[0006], ¶ [0008], ¶¶ [0012]-[0015], ¶ [0019], ¶¶ [0024]-[0027], ¶¶ [0036]-[0040],

¶ [0043], FIGS. 3, 10-13; Yu273, at Title, Abstract, 1:6-2:39, 2:47-60, 3:5-9, 4:17-59, 5:10-64, FIGS. 7-9; Jung104, at Title, Abstract, ¶ [0001], ¶¶ [0010]-[0065], ¶ [0071], ¶¶ [0075]-[0133], TABLES III-VII, FIGS. 1A-2, 4A-15; Kavalieros729, ¶ [0001], ¶ [0026], FIG. 14; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0005]-[0009], ¶ [0015], ¶ [0020], ¶ [0022], ¶ [0027], ¶ [0030], ¶ [0032], FIG. 10; Alvarez069, at Abstract, ¶[0001], ¶¶ [0005]-[0008], ¶¶ [0013]-[0016], ¶¶ [0019]-[0020], ¶¶ [0022]-[0027], ¶ [0031], ¶¶ [0033]-[0035], ¶ [0037], ¶ [0043], ¶¶ [0047]-[0082], TBL. I, FIGS. 4, 9-11; ITRS_2007_PIDS, at 27; ITRS_2007_FEP, at 2-3, 19-20, 29-30, Tbl. FEP1, Fig. FEP4; Thompson Apr2004 article, at 191-93, Fig. 1; Thompson Nov2004 article, at 1790-96, Figs. 2, 5, 12, 13; Sun article, at 1-2, 10, 16, 20-21, Figs. 5-7; Eneman article, at 1446-51, Tbls. I, II, Figs. 2-4, 8, 9; Liu article, at 836-37, Figs. 1-7; Morin article, at 355-58, 362, 367, Tbl. I, Figs. 1, 2; Bai article, at 657, Figs. 3, 4.

As another example, to the extent that any of Akasaka077, Akasaka939, Aoyama950, Kavalieros277, or Okazaki789 do not disclose the claimed "source/drain regions formed in the second active region laterally outside the second sidewall spacers, wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region," a POSITA would have found it obvious to combine it with, e.g., Intel_686_Products, Hsu660, Bohr559, Bohr683, Bohr article, Hou414, Hsu823, Murthy151, Murthy482, Kavalieros277, Kavalieros729, Ke984, James 90nm article, Thompson Apr2004 article, Thompson Nov2004 article, and/or Bai article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for improving the hole mobility and accompanying device performance in MISFETs, including HKMG MISFETs. *See, e.g.*, James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_686_Products); James HKMG article, at 346-47, Figs. 2, 3 (same);

Mistry2007 article, at 248-49, Figs. 5, 6 (same); Mistry2007 presentation, at 14, 15a-15j, 16, 19, 35 (same); QX9650_Report, at 2, 14-15, 19-20, 26-28, 30-32, 41-42, 60, 62-63, 77, 79, 118-19, Tbls. 4.0.1, 4.0.2, Figs. 2.2.2, 2.2.3, 2.3.1.2, 2.3.1.3, 2.3.1.12, 2.3.1.13, 2.3.2.5, 2.3.2.7, 2.3.2.8, 2.4.4, 2.4.5 (same); Hsu660, at 4:35-40, 5:3-9, 6:19-31, 8:35-41, FIGS. 4-11; Bohr559, at Abstract, ¶¶ [0001]-[0003], ¶ [0016], ¶¶ [0020]-[0021], ¶ [0034], ¶¶ [0036]-[0037], ¶ [0039], ¶ [0050], ¶ [0053], FIG. 8; Bohr683, at Title, Abstract, ¶¶ [0022]-[0035], ¶ [0039], ¶ [0041], ¶¶ [0043]-[0046], ¶ [0050], FIGS. 3-6, 8; Bohr article, at 1-3, Figs. 1, 2; Hou414, at 4:19-23, 5:24-40; Hsu823, ¶ [0002], ¶ [0028], ¶¶ [0031]-[0033], ¶ [0035], ¶¶ [0037]-[0039], ¶ [0041], FIGS. 5-14; Murthy151, ¶ [0005], ¶ [0021], ¶¶ [0046]-[0048], ¶¶ [0063]-[0074], ¶ [0102], ¶ [0125], FIGS. 2-4; Murthy482, 1:41-2:15, 4:39-7:10, 8:6-9:63, FIGS. 2-8; Kavalieros729, at Abstract, ¶¶ [0001]-[0002], ¶¶ [0024]-[0025], ¶ [0043], FIGS. 4-13; Kavalieros277 ¶ [0007], ¶ [0027]; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶ [0006], ¶ [0016], ¶¶ [0020]-[0021], ¶ [0023], ¶ [0032], FIG. 10; ITRS_2007_PIDS, at 16, 26, 27, 56, Tbls. PIDS1a, PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, Figs. PIDS5, PIDS10; ITRS_2007_FEP, at 1-3, 10-13, 16, 17, 19-20, 29, 33 n.1, 35, 58-59, Tbl. FEP1, Figs. FEP1-FEP5; James 90nm article, at 73-74, Fig. 6; Thompson Apr2004 article, at 191-93, Fig. 1; Thompson Nov2004 article, at 1790-96, Figs. 2-7, 10, 13; Sun article, at 1-4, 7-16, 21, Figs. 5-8, 11, 12; Bai article, at 657, Fig. 4.

As another example, to the extent that any of Akasaka077, Aoyama950, Bohr559, Hsu660, Intel_686_Products, or Okazaki789 do not disclose that "the first and second gate insulating films include a high-k film made of a metal oxide having a relative dielectric constant of 10 or more," as claimed, a POSITA would have found it obvious to combine it with, e.g., Akasaka939, Bohr559, Kavalieros277, Mistry2007 article, Mistry2007 presentation, Ji704, and/or Yu273, thereby resulting in a combination that includes this claimed feature, because each of Akasaka077,

Aoyama950, Bohr559, Hsu660, Intel_686_Products, Kavalieros277, and Okazaki789 discloses certain high-k materials for use in their respective gate insulating films, and these references confirm the values of their respective relative dielectric constants and the benefit of using films with such a property. *See, e.g.*, Akasaka939 ¶¶ [0003]-[0004]; Baklanov, at xiii; Colombo468 ¶ [0025]; ITRS_2007_FEP, at 2, 20; ITRS_2007_PIDS, at 1, 6, 8, 27, Fig. PIDS5; Kavalieros277 ¶ [0002], ¶[0008]; Kavalieros729 ¶ [0032]; Mistry2007 article, at 247-48, Fig. 6; Mistry2007 presentation, at 17; Ji704, at 8:27-31; Yu273, at 3:21-34.

Additional obviousness combinations of the references identified here are possible, and TSMC may rely on such combination(s) in this litigation. In particular, TSMC is currently unaware of Plaintiff's allegations with respect to the level of skill in the art and the qualifications of a POSITA. TSMC is also unaware of the extent, if any, to which Plaintiff may contend that limitations of the claims at issue are not disclosed in the prior art identified by TSMC as anticipatory, and the extent to which Plaintiff will contend that features not disclosed in the asserted patent specifications would have been known to a POSITA. And TSMC does not yet know how the Court will construe terms in the asserted claim. TSMC is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. TSMC reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case No. IPR2025-00682 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the '686 patent.

d. The ’180 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below, and in Exhibits 180-01 through 180-15 would have rendered obvious one or more Asserted Claims of the ’180 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits 180-01 through 180-15, TSMC contends that all asserted claims are rendered obvious by Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, or Wang ’084 and Yu alone, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 180-01 through 180-15 and Herein) [17]:
180-01	Kamata	One or more of Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-02	Guha	One or more of Kamata, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-03	Matsumoto135	One or more of Kamata, Guha, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-04	Kubicek	One or more of Kamata, Guha, Matsumoto 135, Sasaki, JP-Ono, Matsumoto-185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-05	Sasaki	Kamata, Guha, Matsumoto 135, Kubicek, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-06	JP-Ono	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe 2004, Watanabe 2003, Lee 1999, Lee 2000,

[17] To the extent any reference is cited in Exhibits 180-01 to 180-15, but not referenced here, any omission was unintentional and TSMC intends to rely on its identification of any such combinations in Exhibits 180-01 to 180-15.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 180-01 through 180-15 and Herein) [17]:
		Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-07	Matsumoto 185	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-08	Mizushima	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-09	Inumiya 763	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Vandooren, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-10	Vandooren	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-11	Inumiya 355	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-12	Clevenger	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 180-01 through 180-15 and Herein) [17]:
		Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-13	Ono	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
180-14	Wang ’084	Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Mizushima, Inumiya 763, Vandooren, Inumiya 355, Clevenger, Ono, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’180 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’180 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits 180-01 through 180-15 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits 180-01 through 180-15, including for the reasons described below. A POSITA at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’180 patent relates to a semiconductor device comprising a high dielectric constant gate insulating film formed on an active region in a substrate. The asserted claims recite elements that were conventional in manufacturing transistors well before the priority date of the ’180 patent (alleged to be August 5, 2005). A semiconductor device comprising a high dielectric constant gate insulating film formed on an active region in a substrate was well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, Title, Abstract, ¶¶ [0003], [0008]-[0010], [0032], [0036], [0050], [0052]-[0053], [0056], [0068], [0073], [0093]-[0094], [0099]-[0100], Figures 1B(j), 5(c), 10(b); Guha, Title, Abstract, claims 1, 3, 13, ¶¶ [0001], [0021]-[0023], [0026], [0037]-[0038], [0043], Figures 10-12; Matsumoto 135, Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102-103], [0105], [0107], [0137]-[0138], [0140], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kubicek, Abstract, 1, 4, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claim 1, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], Figures 1-3, 6-10, 19-23; Matsumoto 185, Title, Abstract, claims 1, 7, ¶¶ [0001], [0010]-[0012], [0038], [0042]-[0045], Figures 3-6, 33; Mizushima, Title, Abstract, claims 3, 1:14-29, 4:15-26, 17:26-56, Figures 13A-13L; Inumiya 763, Title, Abstract, 1:5-6, 3:45-49, 4:15-22, 14:17-20, 19:43-49, 20:11-19, Figures 10G, 10I; Vandooren, Abstract, 324, 325, Figures 1-2; Inumiya 355, Title, Abstract, 1:6-9, 5:29-37, 7:45-49, 10:54-56, 12:43-45, 15:63-16:8, 16:25-34, 33:55-64, 34:29-46, Figures 9E, 9G-9I, 50G-50I; Clevenger at Abstract, claims 1, 3, 4, 1:12-15, 1:17-28, 1:54-2:3, 3:40-46, 3:58-5:2, Figures 1-8; Ono, Title, Abstract,

claim 1, 8, 13, ¶¶ [0003], [0007], [0008], [0158], [0160], [0166], Figures 4, 9; Wang ’084, Title, Abstract, claims 1, ¶¶ [0002], [0007]-[0011], [0020]-[0022], [0029]-[0039], [0040], [0044], [0047]-[0048], [0054]-[0055], Figures 2, 5F; Yu, Title, 1:6-10, 1:14-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004, Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003, Title, 19, Figures 1, 11; Lee_2000, Title, 2.4.1, 2.4.2, Figures 1, 12; Andreoni, Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055]-[0057], Figures 1, 2A-2C; Wolf, 145-146, Figures 1-2, 5-25; Wang ’672, Title, Abstract, claim 15, ¶¶ [0002], [0008]-[0012], [0015], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044]-[0045], [0047]-[0048], [0050]-[0052], Figure 3; Lee_1999, Title, 6.1.1; Ahmed, 5:40-61; Mutou, claims 1, 4-5, ¶¶ [0006]-[0007], [0042]-[0043], [0054]-[0055], [0072], [0080], [0111]-[0112], Figures 1-11; Houssa, 8-9, 510.

A gate electrode formed on the high dielectric constant gate insulating film was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, claim 1, ¶¶ [0008]-[0011], [0050], Figures 1A(a)-(c), 1B(j), 5(c), 10(b); Guha, claims 1, 13, ¶¶ [0041], [0043]-[0045], Figures 10-12; Matsumoto 135, Abstract, claims 1, 10, 13, ¶¶ [0103], [0107]-[0108], [0137]-[0138], Figures 1-4, 10, 13, 19-26; Kubicek, Abstract, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0028]-[0029], [0039]-[0050], [0063]-[0064], [0068]-[0077], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claim 1, ¶¶ [0013], [0018]-[0022], [0033]-[0037], [0042]-[0043], Figures 1-3, 6-10, 19-23; Matsumoto 185, claims 1, 7, ¶¶ [0038], [0046], [0048]-[0049], Figure 33; Mizushima, claim 3, 17:56-18:3, Figures 13A-13K; Inumiya 763, 20:11-19, Figures 10G, 10I; Vandooren, 324, Figures 1-2; Inumiya 355, 16:25-34, 34:29-46,

Figures 9G-9I, 50G-50I; Clevenger, Abstract, claim 1, 3:58-5:2, Figures 1-6; Ono, claim 1, ¶¶ [0160], [0167]; Wang ’084, Abstract, claim 1, ¶¶ [0008]-[0011], [0020]-[0022], [0024], [0029]-[0040], [0043]-[0044], [0047]-[0048], [0054]-[0055], Figures 2, 5F; Yu, 3:1-7, Figure 1; Watanabe_2004, Figures 2, 5-6; Watanabe_2003, Figures 1, 11; Andreoni, Abstract, ¶¶ [0028], [0046], [0051], [0057], Figure 1, 2A-2C; Wolf, Figures 1-2, 5-25; Wang ’672, ¶¶ [0011], [0044], [0048], [0051], [0054], Figure 3.

An insulating sidewall formed on each side surface of the gate electrode was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0008]-[0016], [0050], [0052], [0057]-[0058], [0074], Figures 1B(j), 5(c), 10(b); Guha, claim 1, ¶¶ [0028], [0034]-[0035], [0040], [0043]-[0045], Figures 3-6, 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [00143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, ¶¶ [0028], [0056], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono, claim 3, ¶¶ [0033], [0078]-[0079], [0083]-[0084], Figures 19-23; Matsumoto 185, claims 1, 7, ¶¶ [0038], [0044], [0119]-[0120], Figures 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, Abstract, 4:15-34, 19:52-65, 20:22-33, Figures 10A-10G, 10I, 50F-50I; Vandooren, 324, 326, Figures 2, 12; Inumiya 355, 15:63-16:24, 16:27-34, 34:24-46, Figures 9E-9I; Clevenger, 4:26-45, Figures 1-6; Ono, ¶ 181; Wang ’084, ¶¶ [0010]-[0011], [0029]-[0039], [0040], [0044], [0049]-[0050], [0055]-[0056]; Yu, 4:3-9, 4:22-27, 6:49-60, 7:31-39, Figure 1; Watanabe_2004, 507, Figures 1-2, 4-6; Watanabe_2003, 19, Figures 1, 11; Andreoni, 56, Figures 2A-2C; Wolf, 217, 5-

25; Houssa, 510-511; Wang ’672, ¶¶ [0049], Figure 3; Mutou, claims 10, 12, 19, 20, ¶¶ [0047], [0076]-[0077], [0095]-[0096], [0103], [0116], Figures 1-11.

A high dielectric constant gate insulating film continuously formed so as to extend from under the gate electrode to under the insulating sidewall was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0050], [0056], [0093], Figure 1A(f), 1B(g), 1B(j), 5(c), 10(b); Guha, claims 1, 13, ¶¶ [0028], [0034]-[0035], [0043]-[0044], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0107]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Vandooren, 324, Figures 1-2; Inumiya 355, 16:27-34, 34:24-46, Figures 9G-9I, 50F-50I; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0199], [0215], Figures 13, 80; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Houssa, 510; Plummer, 82-83. By the 2005 priority date of the ’180 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for

example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figures 1-4.)

An end of the high dielectric constant gate insulating film under the insulating sidewall located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0050], [0056], [0093], Figures 1A(f), 1B(g), 1B(j), 5(c), 10(b); Guha, claims 1, 13, ¶¶ [0028], [0034]-[0035], [0043]-[0044], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Vandooren, 324, Figures 1-2; Inumiya 355, 16:27-34, Figures 9G-9I, 50F-50I; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0200], [0215], Figures 57, 108; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Kajiyama, ¶¶ [0029]-[0031], Figures 1(A)-(D).

A buffer insulating film between the substrate and the high dielectric constant gate insulating film was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-

49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶ [0054]; Guha, claims 1, 11, ¶¶ [0037], [0043], Figure 12; Kubicek, 1, Figure 1; Sasaki, ¶¶ [0028]-[0030], [0035]-[0038], [0050], [0056], [0063]-[0064], [0068], [0072], [0074], [0080], Figures 1, 3-14, 16-19; Inumiya 763, 20:11-19, Figures 10G, 10I; Vandooren, Figures 1-2; Ono, ¶ [0160], Figure 4; Wang ’084, claim 2, ¶¶ [0029]-[0039], [0040], [0044], [0048], [0055], Figures 2, 5F; Yu, 3:59-4:2, 6:29-33, Figure 1; Sim, 219, Figure 1; Watanabe_2004, 510, Figure 5, Watanabe_2003, 19, Figures 1-4, 11; Houssa, 8-9; Andreoni, ¶¶ [0001], [0008], [0010], [0028], [0032]-[0035], [0040], [0049], [0056], [0057], Figures 1, 2A-2C; Wang ’672, Abstract, claim 15, ¶¶ [0002]-[0003], [0008]-[0009], [0011], [0022]-[0024], [0027]-[0028], [0041], [0043]-[0044], [0048], Figure 3; Mutou, Abstract, claims 1, 10, 12, 19, 20, ¶¶ [0020], [0041]-[0042], [0053]-[0055], [0110]-[0112], Figures 1-11; Lo, 3:34-37, 3:45-48, Figure 7; Parker, claims 1-3, 11, 1:20-26, 1:33-42, 2:30-3:6. By the 2005 priority date of the ’180 patent, a POSITA would have been motivated to include a buffer insulating film between the substrate and the high dielectric constant gate insulating film in a semiconductor device in light of the known benefits of a buffer insulating film, including, for example, suppressing the “deterioration of an interface between a substrate and a gate insulating film” caused by chemical interactions between the high-k material and the silicon substrate. (’180 patent, 11:66-12:5; see also, e.g., Wang ’672, ¶ [0003].) It was also known that a buffer insulating film between the substrate and the high-k gate insulating film improves carrier mobility and provides higher device reliability. (See, e.g., Wang ’672, ¶ [0028].) By the 2005 priority date of the ’180 patent, a POSITA would also have been motivated to use a silicon oxide film as a buffer insulating film. For example, silicon oxide had already been used for decades in the semiconductor

industry; a POSITA therefore would have been very familiar with its properties and the processes for depositing silicon oxide on a device. Furthermore, a POSITA would have known that silicon oxide is a better-suited material for interfacing with the silicon substrate than a high-k material used for the gate insulating film.

A buffer insulating film that is a silicon oxide film was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶ [0054]; Guha, ¶ [0037], Figure 12; Kubicek, 1, Figure 1; Sasaki, ¶¶ [0028]-[0030], [0035]-[0038], [0050], [0056], [0063]-[0064], [0068], [0072], [0074], [0080], Figures 1, 3-14, 16-19; Inumiya 763, 20:11-19; Vandooren, Figures 1-2; Ono, ¶ 160, Figure 4; Wang ’084, claim 2, ¶¶ [0029]-[0039], [0040], [0044], [0048], [0055], Figures 2, 5F; Yu, 3:59-4:2, 4:56-67, 6:29-33, Figure 1; Watanabe_2004, 510, Figure 5; Watanabe_2003, 19, Figures 1-4, 11; Houssa, 8-9; Andreoni, ¶¶ [0001], [0008], [0010], [0028], [0032]-[0035], [0040], [0049], [0056], [0057], Figures 1, 2A-2C; Wang ’672, Abstract, claim 15, ¶¶ [0002]-[0003], [0008]-[0009], [0011], [0022]-[0024], [0027]-[0028], [0041], [0043]-[0044], [0048], Figure 3; Mutou, Abstract, claims 1, 10, 12, 19, 20, ¶¶ [0020], [0041]-[0042], [0053]-[0055], [0110]-[0112], Figures 1-11; Sim, 219, Figure 1; Lo, 3:45-48; Parker, claims 1, 8, 3:40-43.

A smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall that is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file

history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0018], [0050], [0056], [0085], [0093], Figures 1A(f), 1B(g), 1B(j), 5(c), 10(b); Guha, ¶¶ [0043]-[0044], Figure 12; Matsumoto 135, Abstract, claims 1, 10, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0107]-[0110], [0114], [0137]-[0141], [0143], Figures 1-6, 9-10, 13, 19-26; Kubicek, Figure 1; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Vandooren, Abstract, 324, Figures 1-2; Ono, ¶¶ [0181], [0200], [0215]-[0216], Figures 43, 53, 57, 95, 104, 108; Watanabe_2004, Figure 5. By the 2005 priority date of the ’180 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figures 1-4.)

A high dielectric constant gate insulating film formed of a Hf based oxide was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0052]-[0053]; Guha, ¶¶ [0038], [0043]; Kubicek, Title, Abstract, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claim 1, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], Figures 1-3, 6-10, 19-23; Vandooren, Title, Abstract, 324, Figures 1-2; Clevenger, Abstract, claims 1, 3, 4, 1:17-28, 3:58-5:2, Figures 1-6; Ono, claims 1, 8, ¶ [0166]; Wang ’084, claim 6, ¶¶ [0023], [0029]-[0039], [0040],

[0044]; Yu, 3:14-33; Sim, 218; Watanabe_2004, Title, Abstract, 507, Figures 2, 21; Watanabe_2003, Title, 19, Figures 1, 11; Lee_1999, 6.1.1; Lee_2000, Title, 2.4.1, 2.4.2, Figures 1, 12; Houssa, 8-9; Andreoni, ¶¶ [0037], [0039]; Wang '672, Abstract, ¶¶ [0009], [0012], [0023], [0025], [0034], [0045]; Mutou, claims 1, 4-5, ¶¶ [0006]-[0007], [0042]-[0043], [0054]-[0055], [0072], [0080], [0111]-[0112]; Lo, 3:50-60; Chau '209, 2:6-14; Chau '210, 2:9-23; Parker, claim 4, 2:50-60. By the 2005 priority date of the '180 patent, a POSITA would have been motivated to use a Hf-based oxide, e.g., HfO2, as the material for a gate insulating film in a semiconductor device. By that time, as semiconductor devices continued to shrink in size, the industry had already been searching for high-k material replacements for SiO2 as the gate insulating film. A POSITA would have known that Hf based oxides, such as HfO2, have a high dielectric constant (25 for HfO2). (See, e.g., Wilk, Table I.) Moreover, based on research and studies that had been conducted over the years, a POSITA would have known by the 2005 priority date of the '180 patent that HfO2 has multiple known benefits, including, for example, superior thermal stability, reasonable band alignment, and ability to scale down to a smaller EOT. (See, e.g., Lee-2000, 2.4.1; Houssa, 207; Lee-1999, 6.1.2.)

A part of the high dielectric constant gate insulating film located under the insulating sidewall having a thickness of 2 nm or less was also well-known prior to the '180 patent. *See, e.g.*, '180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; '180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kubicek, 1, Figure 1; Sasaki, ¶ [0037]; Sim, 218-221; Wang '672, claims 1, 6, ¶¶ [0026], [0034]; Lo, 3:50-60; Chau '209, claims 10, 17, 2:21-35; Chau '210, claims 1, 8, 2:24-39; Parker, claims 4, 12, 1:20-26, 3:6-11. By the 2005 priority date of the '180 patent, a POSITA would have been motivated to reduce

the thickness of a high-k gate insulating film made of, e.g., HfO2, to 2 nm or less, as it was known that reducing the thickness of HfO_2 to below 20Å (2 nm) enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (Sim, 219, 221.)

An end of the high dielectric constant gate insulating film located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ¶¶ 50, 56, 93, Figures 1A(f), 1B(g), 1B(j), 5(c), 10(b); ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Guha, claims 1, 13, ¶¶ [0035], [0040], [0043]-[0045], Figure 12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Vandooren, 324, Figures 1-2; Inumiya 355, 16:27-34, Figures 9G, 9H, 9I; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0181], [0199], [0215], Figures 13, 80; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2-5F; Kajiyama, ¶¶ [0029]-[0031], Figures 1(A)-(D).

An insulating sidewall having a double layer structure including an oxide film and a nitride film was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0016], [0050], [0056], [0058], [0093], Figures 1A(f), 1B(g), 1B(j), 5(c), 10(b); Guha, claim 1, ¶¶ [0028], [0034]-[0035], [0040], [0043]-[0045], Figures 3-6, 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Matsumoto 185, claims 1, 7, ¶¶ [0038], [0044], [0119]-[0120], Figures 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, Abstract, 4:15-34, 19:52-65, 20:22-33, Figures 10A-10I; Vandooren, 324, 326, Figures 2, 12; Inumiya 355, 15:63-16:24, 16:27-34, Figures 9E-9I, 50F-50I; Wang ’084, ¶¶ [0029]-[0039], [0040], [0044]; Yu, 4:3-27, Figure 1; Watanabe_2004, 507, Figure 2; Wang ’672, ¶ [0049]; Bu, claims 1-2, 5, 9, 15-17, 21, ¶¶ [0019]-[0022], [0026]-[0027], [0030], [0035]-[0038], Figure 1D; Ahmed, claims 1, 3-7, 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, Figures 3, 5E-5F. By the 2005 priority date of the ’180 patent, a POSITA would have been motivated to form an insulating sidewall in a semiconductor device with a double layer structure that includes an oxide film and a nitride film. A POSITA would have known, for example, that using oxide and nitride films in insulating sidewall structures, e.g., in an ONO structure, provided known benefits including allowing independent control of spacer dimensions which optimizes device scaling. (See, e.g., U.S. Publication 2005/0040479, ¶¶ [0005]-[0006], Figure 4.) Additionally, a POSITA would have known by the 2005 priority date of the ’180 patent that forming a sidewall structure with different

layers of oxide and nitride films can help with minimizing dopant loss from the source/drain region, thereby lowering parasitic resistance in the semiconductor device. (See, e.g., Bu, ¶ [0025].)

A width of the high dielectric constant gate insulating film along a gate length that is larger than a width of the gate electrode along the gate length was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata ¶¶ [0050], [0056], [0068], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0040]-[0041], [0043]-[0045], [0047], Figure 12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Vandooren, 324, Figures 1-2; Inumiya 355, 16:27-34, Figures 9G, 9H, 9I; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0181], [0199], [0215], Figure 13; Wang ’084, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Houssa, 510; Plummer, 82-83; Kajiyama, ¶¶ [0029]-[0031], Figures 1(A)-(D). By the 2005 priority date of the ’180 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example,

minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figs. 1-4.)

A width of a bottom surface of the high dielectric constant gate insulating film along a gate length that is larger than a width of a bottom surface of the gate electrode along the gate length was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0050], [0056], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0040]-[0041], [0043]-[0045], [0047], Figure 12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Vandooren, 324, Figures 1-2; Inumiya 355, 16:27-34, Figures 9G, 9H, 9I; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0181], [0199], [0215], Figure 13; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Houssa, 510; Plummer, 82-83; Kajiyama, ¶¶ [0029]-[0031], Figures 1(A)-(D).

A high dielectric constant gate insulating film having a relative dielectric constant of 10 or more was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance

and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0052]-[0053]; Guha, claim 1, ¶¶ [0038], [0043]; Matsumoto 135, Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102]-[0103], [0105], [0107], [0137]-[0138], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kubicek, Title, Abstract, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claim 1, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], Figures 3-6, 33; Mizushima, 17:33-56, Figures 13A-13K; Inumiya 763, 4:15-22, 14:17-20, 19:43-49, 20:11-19, Figures 10G, 10I; Vandooren, Title, Abstract, 324, Figures 1-2; Inumiya 355, 5:29-37, 15:63-16:8, 16:25-34, Figures 9E, 9G, 9H, 9I; Clevenger, Abstract, claims 1, 3, 4, 1:17-28, 3:58-5:2, Figures 1-6; Ono, claims 1, 8, ¶ [0166]; Wang ’084, ¶¶ [0029]-[0039], [0040], [0044]; Yu, 3:15-33, 5:19-44; Wilk, 5254; Watanabe_2004, Title, Abstract, 507, Figure 2; Watanabe_2003, Title, 19, Figures 1, 11; Lee_1999, 6.1.1; Wolf, 145-146; Houssa, 8-9; Wang ’672, Abstract, claim 23, ¶¶ [0009], [0012], [0025], [0034], [0045]; Ahmed, 5:40-61, 9:39-57; Mutou, claims 1, 4-5, ¶¶ [0006]-[0007], [0042]-[0043], [0054]-[0055], [0072], [0080], [0111]-[0112]; Lo, 3:50-60. By the 2005 priority date of the ’180 patent, a POSITA would have been motivated to use a high dielectric constant material to form the gate insulating film of a semiconductor device. For decades prior to the ’180 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. (See, e.g., Plummer, 53; Houssa, 3-4.) As gate dielectrics continued to shrink in thickness (e.g., below 1.5 nm), use of SiO2 became untenable, because the amount of gate-to-channel tunneling leakage-current passing through the gate dielectric prevents the gate electrode from effectively controlling

the ON/OFF states of the FET. (See, e.g., Wolf, 4-5.) High-k gate dielectrics, like Hf-based oxides, Ta2O5, or ZrO2, replaced SiO_2 to address these challenges. (See, e.g., Wolf, 146.) For example, it was known by the 2005 priority date of the ’180 patent that, as compared to SiO2, high-k materials significantly reduce the amount of leakage current and, thus, improve energy efficiency. (Wilk, 5250, Figure 5; Wolf, 146-47.)

A high dielectric constant gate insulating film having a larger relative dielectric constant than that of the insulating sidewall was also well-known prior to the ’180 patent. *See, e.g.*, ’180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0050], [0052]-[0053], [0058]; Guha, claims 1, 3, ¶¶ [0028], [0038], [0040], [0043]; Matsumoto 135, Title, Abstract, claims 1, 10-11, 13-14, ¶¶ [0002], [0013]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102]-[0105], [0107], [0109]-[0110], [0114], [0137]-[0141], [0143], [0167], Figures 1-2, 4-6, 9-10, 13, 19-26; Kubicek, Title, Abstract, 1, 4, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Mizushima, claims 14, 18, 17:33-56, 18:4-30, Figures 13A-13K; Inumiya 763, Abstract, 4:15-34, 14:17-20, 19:43-49, 19:52-65, 20:11-19, 20:22-33, Figures 10A-10G, 10I; Vandooren, Title, Abstract, 324, 326, Figures 1-2, 12; Inumiya 355, 5:29-37, 15:63-16:24, 16:25-34, Figures 9E-9I; Clevenger, Abstract, claims 1, 3, 4, 1:17-28, 3:58-5:2, Figures 1-6; ; Wang ’084, claim 6, ¶¶ [0023], [0029]-[0039], [0040], [0044]; Yu, 1:17-29, 2:48-52, 2:63-67,

3:1-7, 3:14-33, 4:3-27, 5:19-44, 6:49-60, 7:31-39, Figure 1; Watanabe_2004, Title, Abstract, 507, Figures 1-2, 4-6, 21; Watanabe_2003, Title, 19, Figures 1, 11; Lee_1999, Title, 6.1.1; Lee_2000, Title, 2.4.1, 2.4.2, Figures 1, 12; Andreoni, Title, ¶¶ [0001], [0008], [0010], [0028], [0037], [0039], [0049], [0056]-[0057], Figures 1, 2A-2C; Wolf, 145-146, 217, Figure 5-25; Houssa, 8-9, 510-511; Wang '672, Title, Abstract, claims 15, 23, ¶¶ [0002], [0008]-[0009], [0011]-[0012], [0020]-[0026], [0034], [0041], [0044]-[0045], [0047]-[0052], Figure 3; Mutou, claims 1, 4-5, 10, 12, 19, 20, ¶¶ [0006]-[0007], [0042]-[0043], [0047], [0054]-[0055], [0072], [0076]-[0077], [0080], [0095]-[0096], [0103], [0111]-[0112], [0116], Figures 1-11; Ahmed, claims 1, 3-7, 5:40-61, 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, Figures 3, 5E-5F; Sim, 218; Bu, claims 1-2, 5, 9, 15-17, 21, ¶¶ [0019]-[0022], [0026]-[0027], [0030], [0035]-[0038], Figure 1D; Wilk, 5254.

An end of the high dielectric constant gate insulating film located under the insulating sidewall having a tapered surface was also well-known prior to the '180 patent. *See, e.g.*, '180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; '180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0018], [0050], [0056], [0085], [0093], Figures 1A(f), 1B(g), 1B(j), 5(c), 10(b); Guha, ¶¶ [0043]-[0044], Figure 12; Kubicek, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figures 1-14, 16-19; Vandooren, Abstract, 324, Figures 1-2; Ono, ¶¶ [0181], [0200], [0215]-[0216], Figures 43, 53, 57, 95, 104, 108; Watanabe_2004, Figure 5.

A high dielectric constant gate insulating film located under the insulating sidewall having a thickness which becomes smaller toward the end thereof was also well-known prior to the '180 patent. *See, e.g.*, '180 patent, 1:24-60, 5:48-49, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS

technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’180 patent file history, 2011-09-09 Non-Final Rejection at 2-6, 2012-01-12 Final Rejection at 2-6; Kamata, ¶¶ [0018], [0050], [0056], [0085], [0093], Figures 1A(f), 1B(g), 1B(j), 5(c), 10(b); Guha, ¶¶ [0043]-[0044], Figure 12; Kubicek, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figures 1-14, 16-19; Vandooren, Abstract, 324, Figures 1-2; Ono, ¶¶ [0181], [0200], [0215]-[0216], Figures 43, 53, 57; Watanabe_2004, Figure 5.

Additional motivations to combine may be found in the ’180 patent invalidity charts.

In sum, by the time the application for the ’180 patent was filed, it was well known to design a semiconductor device as claimed at least because all the above was well known in the art before the ’180 patent, and a POSITA would have known that any and/or all the above techniques could be combined to fabricate a semiconductor device with a high dielectric constant gate insulating film formed on an active region in a substrate, a gate electrode formed on the high dielectric constant gate insulating film, an insulating sidewall formed on each side surface of the gate electrode, and wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode. This is especially true here because all of the references disclose a semiconductor device with sidewalled transistors even if they do not disclose every aspect of a semiconductor device design. As such, a POSITA would have logically and predictably consulted all of the references together to design a complete semiconductor device with the claimed sidewalled transistors. Furthermore, the general background knowledge described above and below would have provided the basis for

combining any number of known semiconductor device designs to create different semiconductor devices with the claimed sidewalled transistors. Because all of these techniques were already known in the art for use in fabrication of semiconductor devices, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a semiconductor device, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits 180-01 through 180-15, a POSITA would have been motivated to combine any of the references identified as prior art to the ’180 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar semiconductor device designs with sidewalled transistors (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Kamata, Title, Abstract, ¶¶ [0003], [0008]-[0010], [0032], [0036], [0050], [0052]-[0053], [0056], [0068], [0073], [0093]-[0094], [0099]-[0100], Figures 1B(j), 5(c), 10(b); Guha, Title, Abstract, claims 1, 3, 13, ¶¶ [0001], [0021]-[0023], [0026], [0037]-[0038], [0043], Figures 10-12; Matsumoto 135, Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102-103], [0105], [0107], [0137]-[0138], [0140], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kubicek, Abstract, 1, 4, Figure 1;

Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claim 1, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], Figures 1-3, 6-10, 19-23; Matsumoto 185, Title, Abstract, claims 1, 7, ¶¶ [0001], [0010]-[0012], [0038], [0042]-[0045], Figures 3-6, 33; Mizushima, Title, Abstract, claims 3, 1:14-29, 4:15-26, 17:26-56, Figures 13A-13L; Inumiya 763, Title, Abstract, 1:5-6, 3:45-49, 4:15-22, 14:17-20, 19:43-49, 20:11-19, Figures 10G, 10I; Vandooren, Abstract, 324, 325, Figures 1-2; Inumiya 355, Title, Abstract, 1:6-9, 5:29-37, 7:45-49, 10:54-56, 12:43-45, 15:63-16:8, 16:25-34, 33:55-64, 34:29-46, Figures 9E, 9G-9I, 50G-50I; Clevenger at Abstract, claims 1, 3, 4, 1:12-15, 1:17-28, 1:54-2:3, 3:40-46, 3:58-5:2, Figures 1-8; Ono, Title, Abstract, claim 1, 8, 13, ¶¶ [0003], [0007], [0008], [0158], [0160], [0166], Figures 4, 9; Wang ’084, Title, Abstract, claims 1, ¶¶ [0002], [0007]-[0011], [0020]-[0022], [0029]-[0039], [0040], [0044], [0047]-[0048], [0054]-[0055], Figures 2, 5F; Yu, Title, 1:6-10, 1:14-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004, Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003, Title, 19, Figures 1, 11; Lee_2000, Title, 2.4.1, 2.4.2, Figures 1, 12; Andreoni, Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055]-[0057], Figures 1, 2A-2C; Wolf, 145-146, Figures 1-2, 5-25; Wang ’672, Title, Abstract, claim 15, ¶¶ [0002], [0008]-[0012], [0015], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044]-[0045], [0047]-[0048], [0050]-[0052], Figure 3; Lee_1999, Title, 6.1.1; Ahmed, 5:40-61; Mutou, claims 1, 4-5, ¶¶ [0006]-[0007], [0042]-[0043], [0054]-[0055], [0072], [0080], [0111]-[0112], Figures 1-11; Houssa, 8-9, 510.

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, a high dielectric constant gate insulating film continuously formed so as to extend from under the gate electrode to under the insulating

sidewall—to other references that relate to semiconductor device designs generally because all references teach designing transistors with particular technical specifications suitable for different purposes in semiconductor devices, and it would have been a trivial exercise to consult the references that taught more specific semiconductor device designs to fill in less specific disclosures in other references. *See, e.g.*, Kamata, ¶¶ [0050], [0056], [0093], Figure 1A(f), 1B(g), 1B(j), 5(c), 10(b); Guha, claims 1, 13, ¶¶ [0028], [0034]-[0035], [0043]-[0044], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0107]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], 1:54-2:3, Figures 1-14, 16-19; JP-Ono, Title, Abstract, claims 1, 3, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0045], [0119]-[0120], Figures 3-6, 32-33; Mizushima, claims 3, 18:4-30, Figures 13A-13K; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Vandooren, 324, Figures 1-2; Inumiya 355, 16:27-34, 34:24-46, Figures 9G-9I, 50F-50I; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0199], [0215], Figures 13, 80; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Houssa, 510; Plummer, 82-83.

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference’s exact set of materials, components, or configurations in a particular semiconductor with the teachings regarding other materials, components, and configurations used in other semiconductor device for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques for

designing semiconductor devices existed. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: fabricating a semiconductor device with sidewalled transistors. This is thus a combination of prior art elements (*e.g.*, a high dielectric constant gate insulating film formed on an active region in a substrate, a gate electrode formed on the high dielectric constant gate insulating film, a insulating sidewall formed on each side surface of the gate electrode, and wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of semiconductor fabrication were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

Additional obviousness combinations of the references identified here are possible, and TSMC may rely on such combination(s) in this litigation. In particular, TSMC is currently

unaware of AICP's allegations with respect to the level of skill in the art and the qualifications of a POSITA. TSMC is also unaware of the extent, if any, to which AICP may contend that limitations of the claims at issue are not disclosed in the prior art identified by TSMC as anticipatory, and the extent to which AICP will contend that elements not disclosed in the asserted patent specifications would have been known to a POSITA. And TSMC does not yet know how the Court will construe terms in the asserted claim. TSMC is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. TSMC reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case No. IPR2025-00830 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the '180 patent.

e. The '076 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant's Admitted Prior Art, and/or the additional prior art references discussed below, and in Exhibits 076-01 through 076-15 would have rendered obvious one or more Asserted Claims of the '076 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results;

(e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits 076-01 through 076-15, TSMC contends that all asserted claims are rendered obvious by Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, or Wang ’084 and Yu alone, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exh. No.	**Primary Reference**	**In Combination With One or More of the Following (As Described in Exhibits 076-01 through 076-15 and Herein)** [18]**:**
076-01	Kamata	One or more of Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-02	Guha	One or more of Kamata, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-03	Matsumoto 135	One or more of Kamata, Guha, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 764, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-04	Kubicek	One or more of Kamata, Guha, Matsumoto 135, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya

[18] To the extent any reference is cited in Exhibits 076-01 to 076-15, but not referenced here, any omission was unintentional and TSMC intends to rely on its identification of any such combinations in Exhibits 076-01 to 076-15.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 076-01 through 076-15 and Herein) [18]:
		355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-05	Sasaki	One or more of Kamata, Guha, Matsumoto 135, Kubicek, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-06	JP-Ono	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-07	Matsumoto 185	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-08	Vandooren	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-09	Inumiya 763	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 355, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-10	Inumiya 355	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Mizushima, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 076-01 through 076-15 and Herein) [18]:
		Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-11	Mizushima	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Clevenger, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-12	Clevenger	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Ono, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-13	Ono	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Wang ’084, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker
076-14	Wang ’084	One or more of Kamata, Guha, Matsumoto 135, Kubicek, Sasaki, JP-Ono, Matsumoto 185, Vandooren, Inumiya 763, Inumiya 355, Mizushima, Clevenger, Ono, Yu, Sim, Wilk, Watanabe_2004, Watanabe_2003, Lee_1999, Lee_2000, Andreoni, Wolf, Houssa, Plummer, Mutou, Wang ’672, Bu, Ahmed, Kajiyama, Lo, Chau ’209, Chau ’210, and Parker

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’076 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’076 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits 076-01 through 076-15 and/or with a POSITA’s general

knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits 076-01 through 076-15, including for the reasons described below. A POSITA at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’076 patent relates to a semiconductor device comprising a gate insulating film formed on an active region in a substrate and including Hf. The asserted claims recite elements that were conventional in in manufacturing transistors well before the priority date of the ’076 patent (alleged to be August 5, 2005). A semiconductor device comprising a gate insulating film formed on an active region in a substrate and including Hf was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, Title, Abstract, ¶¶ [003], [0008]-[0010], [0032], [0036], [0050], [0052]-[0053], [0056], [0068], [0073], [0093]-[0094], [0099]-[0100], Figures 1B(j), 5(c), 10(b); Guha, Title, Abstract, claims 1, 13, ¶¶ [0001], [0021]-[0023], [0026], [0037]-[0038], [0043], Figures 10-12; Matsumoto 135, Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102]-[0103], [0105], [0107], [0137]-[0138], [0140], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kubicek, Abstract, 1, 4, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figure 1, 3-14, 16-19; JP-Ono, Title, Abstract, claim 1, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044],

[0076]-[0080], Figures 1-3, 6-10, 19-23; Matsumoto 185, Title, Abstract, claims 1, 7, ¶¶ [0001], [0010], [0011]-[0012], [0038], [0042]-[0045], Figures 3-6, 33; Vandooren, Title, Abstract, 324, 325, Figures 1-2; Inumiya 763, Title, Abstract, 1:5-6, 3:45-49, 4:15-22, 14:17-20, 19:43-49, 20:11-19, Figures 10G, 10I; Inumiya 355, Title, Abstract, 1:6-9, 5:29-37, 7:45-49, 12:43-45, 15:23-29, 15:63-16:8, 16:25-34, 33:55-64, 34:29-46, Figures 9E, 9G-9I, 50G-50I; Mizushima, Title, Abstract, claim 3, 1:14-29, 4:15-26, 17:26-56, Figures 13A-13L; Clevenger, Abstract, claims 1, 3, 4, 1:12-15, 1:17-28, 1:54-2:3, 3:40-46, 3:58-5:2, Figures 1-8; Ono, Title, Abstract, claims 1, 8, 13, ¶¶ [0003], [0007]-[0008], [0158], [0160], [0166], Figure 4; Wang ’084, Title, Abstract, claims 1, 6, ¶¶ [0002], [0007]-[0011], [0020]-[0023], [0029]-[0039], [0040], [0044], [0047]-[0048], [0054]-[0055], Figures 2, 5F; Yu, 1:6-10, 1:14-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004, Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003, Title, 19, Figures 1, 11; Lee_2000, Title, 2.4.1, 2.4.2, Figures 1, 12; Andreoni, Title, Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055]-[0057], Figures 1, 2A-2C; Wolf, 145-146, Figures 1-2, 5-25; Wang ’672, Abstract, claims 15, 23, ¶¶ [0002], [0008]-[0012], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044]-[0045], [0047]-[0048], [0050]-[0052], Figure 3; Sim, 218; Lee_1999, Title, 6.1.1; Ahmed, 5:40-61, 9:39-57; Mutou, claims 1, 4-5, ¶¶ [0006]-[0007], [0042]-[0043], [0054]-[0055], [0072], [0080], [0111]-[0112], Figures 1-11; Houssa, 8-9, 510.

A gate electrode formed on the gate insulating film was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, claim 1, ¶¶ [0008]-[0011], [0050], Figures 1A(a)-(c), 1B(j), 5(c), 10(b); Guha, claims 1, 13, ¶¶ [0041], [0043]-[0045], Figures

10-12; Matsumoto 135, Abstract, claims 1, 10, 13, ¶¶ [0103], [0107]-[0108], [0137]-[0138], Figures 1-4, 10, 13, 19-26; Kubicek, Abstract, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0028]-[0029], [0039]-[0050], [0063]-[0064], [0068]-[0077], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claim 1, ¶¶ [0013], [0018]-[0037], [0042]-[0043], Figures 1-3, 6-10, 19-23; Matsumoto 185, claims 1, 7, ¶¶ [0038], [0046], [0048]-[0049], Figure 33; Vandooren, 324, Figures 1-2; Inumiya 763, 20:11-19, Figures 10G, 10I; Inumiya 355, 16:25-34, 33:55-64, 34:29-46, Figures 9G-9I, 50G-50I; Mizushima, claim 3, 17:56-18:3, Figures 13A-13K; Clevenger, Abstract, claim 1, 3:58-5:2, Figures 1-6; Ono, claim 1, ¶¶ [0160], [0167]; Wang ’084, Abstract, claim 1, ¶¶ [0008]-[0011], [0020]-[0022], [0024], [0029]-[0039], [0040], [0043]-[0044], [0047]-[0048], [0054]-[0055], Figures 2, 5F; Yu, 3:1-7, Figure 1; Watanabe_2004, Figures 2, 5-6; Watanabe_2003, Figures 1, 11; Andreoni, Abstract, ¶¶ [0028], [0046], [0051], [0057], Figures 1, 2A-2C; Wolf, Figures 1-2, 2-25; Wang ’672, ¶¶ [0011], [0044], [0048], [0051], [0054], Figure 3.

An insulating sidewall formed on each side surface of the gate electrode was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0008]-[0016], [0050], [0052], [0057]-[0058], [0074], Figures 1B(j), 5(c), 10(b); Guha, claim 1, ¶¶ [0028], [0034], [0035], [0040], [0043]-[0045], Figures 3-6, 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, ¶¶ [0028], [0056], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono, claim 3, ¶¶ [0033], [0078]-[0079], [0083]-[0084], Figures 19-23; Matsumoto 185, claims 1, 7, ¶¶ [0038], [0044], [0119]-[0120], Figures 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, Abstract, 4:15-34, 19:52-65, 20:22-33, Figures 10A-10G,

10I; Inumiya 355, 15:63-16:24, 16:27-34, 34:24-46, Figures 9E-9I, 50F-50I; Mizushima, 18:4-30, Figures 13A-13K; Clevenger, 4:26-45, Figures 1-6; Ono, ¶ [0181]; Wang ’084, ¶¶ [0010]-[0011], [0029]-[0039], [0040], [0044], [0049]-[0050], [0055]-[0056]; Yu, 4:3-9, 4:22-27, 6:49-60, 7:31-39, Figure 1; Watanabe_2004, 507, Figures 1-2, 4-6; Watanabe_2003, 19, Figures 1, 11; Andreoni, 56, 2A-2C; Wolf, 217, Figure 5-25; Houssa, 510-511; Wang ’672, ¶ [0049], Figure 3; Mutou, claims 10, 12, 19, 20, ¶¶ [0047], [0076]-[0077], [0095]-[0096], [0103], [0116], Figures 1-11.

A width of the gate insulating film along a gate length that is larger than a width of the gate electrode along the gate length was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0050], [0056], [0068], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0040]-[0041], [0043]-[0045], [0047], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0107]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claims 1, 3, ¶¶ [0013], [0018]-[0037], [0041]-[0043], [0060], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0046], [0048]-[0049], [0119]-[0120], Figures 3-6, 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Inumiya 355, 16:27-34, 34:24-46, Figures 9G-9I, 50F-50I; Mizushima, 18:4-30, Figures 13A-13K; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0199], [0215], Figures 13, 80; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Houssa, 510; Plummer, 82-83. By the 2005 priority date of the ’076 patent, a POSITA would have

known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figures 1-4.)

An end of the gate insulating film under the insulating sidewall that is retracted from an outer end of the insulating sidewall toward the gate electrode was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0050], [0056], [0068], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0043]-[0045], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26, Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claims 1, 3, ¶¶ [0013], [0018]-[0037], [0041]-[0043], [0060], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0046], [0048]-[0049], [0119]-[0120], Figures 3-6, 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Inumiya 355, 16:27-34, Figures 9G-9I, 50F-50I; Mizushima, 18:4-30, Figures 13A-13K; Clevenger, Abstract, claims 1, 3, 4, 1:17-28, 3:58-5:2, Figures 1-6; Ono, ¶¶ [0200], [0202], [0215]-[0216], Figure 43, 53, 57, 95, 104, 108; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Kajiyama, ¶¶ [0029]-[0031], Figures 1(A)-(D).

A buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶ [0054]; Guha, claims 1, 11, ¶¶ [0037], [0043], Figures 10-12; Kubicek, 1, Figure 1; Sasaki, ¶¶ [0028]-[0030], [0035]-[0038], [0050], [0056], [0063]-[0064], [0068], [0072], [0074], [0080], Figures 1, 3-14, 16-19; Vandooren, Figures 1-2; Inumiya 763, 13:16-27, 20:11-19, Figures 10G, 10I; Ono, ¶¶ [0160], Figure 4; Wang ’084, claim 2, ¶¶ [0032], [0029]-[0039], [0040], [0044], [0048], [0055], Figures 2, 5F; Yu, 3:59-4:2, 4:56-67, 6:29-33, Figure 1; Sim, 219, Figure 1; Watanabe_2004, 510, Figure 5; Watanabe_2003, 19, Figures 1-4, 11; Houssa, 8-9; Andreoni, ¶¶ [0001], [0008], [0010], [0028], [0032]-[0035], [0040], [0049], [0056]-[0057], Figure 1, 2A-2C; Wang ’672, Abstract, claim 15, ¶¶ [0002]-[0003], [0008]-[0009], [0011], [0022]-[0024], [0027]-[0028], [0041], [0043]-[0044], [0048], Figure 3; Mutou, Abstract, claims 1, 10, 12, 19, 20, ¶¶ [0020], [0041]-[0042], [0053]-[0055], [0110]-[0112], Figures 1-11. By the 2005 priority date of the ’076 patent, a POSITA would have been motivated to include a buffer insulating film between the substrate and the high dielectric constant gate insulating film in a semiconductor device in light of the known benefits of a buffer insulating film, including, for example, suppressing the “deterioration of an interface between a substrate and a gate insulating film” caused by chemical interactions between the high-k material and the silicon substrate. (’076 patent, 12:17-23; see also, e.g., Wang 672, ¶ [0003].) It was also known that a buffer insulating film between the substrate and the high-k gate insulating film improves carrier mobility and provides higher device reliability. (See, e.g., Wang 672, ¶ [0028].) By the 2005 priority date of the ’076 patent, a POSITA would also have been motivated to use a silicon oxide film as a buffer

insulating film. For example, silicon oxide had already been used for decades in the semiconductor industry; a POSITA therefore would have been very familiar with its properties and the processes for depositing silicon oxide on a device. Furthermore, a POSITA would have known that silicon oxide is a better-suited material for interfacing with the silicon substrate than a high-k material used for the gate insulating film.

A gate insulating film that is formed of a Hf based oxide was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0052]-[0053]; Guha, ¶¶ [0038], [0043]; Kubicek, Title, Abstract, 1, Figure 1; Sasaki, Abstract, claim 1 ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claim 1, ¶¶ [0013], [0018]-[0037], [0041]-[0044], [0060], [0076]-[0080], Figures 1-3, 6-10, 19-23; Vandooren, Title, Abstract, 324, Figures 1-2; Clevenger, Abstract, claims 1, 3, 4, 1:17-28, 3:58-5:2, Figures 1-6; Ono, claims 1, 8, ¶¶ [0166]; Wang ’084, claim 6, ¶¶ [0023], [0029]-[0039], [0040], [0044]; Yu, 3:14-33; Sim, 218; Watanabe_2004, Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003, Title, 19, Figures 1, 11; Lee_1999, 6.1.1; Lee_2000, Title, 2.4.1, 2.4.2, Figures 1, 12; Houssa, 8-9; Andreoni, ¶¶ [0037], [0039]; Wang ’672, Abstract, claim 23, ¶¶ [0009], [0012], [0025], [0034], [0045]; Mutou, claims 1, 4-5, ¶¶ [0006]-[0007], [0042]-[0043], [0054]-[0055], [007]2, [0080], [0111]-[0112].

A part of the gate insulating film located under the insulating film located under the insulating sidewall has a thickness of 2 nm or less was also well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076

patent file history, 2013-04-12 Non-Final Rejection at 2-7; Sasaki, ¶ 37; Sim, 218-221; Wang ’672, claim 6, ¶¶ [0026], [0034]; Lo, 3:50-60; Chau ’209, claims 10, 17, 2:21-35; Chau ’210, claims 1, 8, 2:24-39; Parker, claims 4, 12, 3:6-11. By the 2005 priority date of the ’076 patent, a POSITA would have been motivated to reduce the thickness of a high-k gate insulating film made of, e.g., HfO2, to 2 nm or less, as it was known that reducing the thickness of HfO_2 to below 20Å (2 nm) enhances mobility and reduces charge trapping, key issues in ensuring the performance and scalability of semiconductor devices. (Sim, 219, 221.)

An end of the gate insulating film that protrudes from a side end of the gate electrode toward the insulating sidewall was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0050], [0056], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0040]-[0041], [0043]-[0045], [0047], Figures 10-12; Matsumoto 135, Title, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claims 1, 3, ¶¶ [0013], [0018]-[0037], [0041]-[0043], [0060], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0046], [0048]-[0049], [0119]-[0120], Figures 3-6, 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, Abstract, 4:15-34, 19:52-65, 20:22-33, Figures 10A-10G, 10I; Inumiya 355, 15:63-16:24, 16:27-34, Figures 9E-9I, 50F-50I; Mizushima, 18:4-30, Figures 13A-13K; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0181], [0199], [0215], Figures 13, 80; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-

[0050], [0054]-[0056], Figures 2, 5F; Houssa, 510; Plummer, 82-83; Kajiyama, ¶¶ [0029]-[0031], Figures 1(A)-(D). By the 2005 priority date of the ’076 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figures 1-4.)

An insulating sidewall that has a double layer structure including an oxide film and a nitride film was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0008]-[0016], [0050], [0052], [0057]-[0058], [0074], Figures 1B(j), 5(c), 10(b); Guha, claim 1, ¶¶ [0028], [0034], [0035], [0040], [0043]-[0045], Figures 3-6, 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Matsumoto 185, claims 1, 7, ¶¶ [0038], [0044], [0119]-[0120], Figures 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, Abstract, 4:15-34, 19:52-65, 20:22-33, Figures 10A-10G, 10I; Inumiya 355, 15:63-16:24, 16:27-34, Figures 9E-9I, 50F-50I; Mizushima, 18:4-30, Figures 13A-13K; Wang ’084, ¶¶ [0029]-[0039], [0040], [0044]; Yu, 4:3-27, Figure 1; Watanabe_2004, 507, Figure 2; Wang ’672, ¶ [0049]; Bu, claims 1-2, 5, 9, 15-17, 21, ¶¶ [0019]-[0022], [0026]-[0027], [0030], [0035]-[0038], Figure 1D; Ahmed, claims 1, 3-7, 6:29-33, 7:29-63, 9:20-62, 10:55-64, 12:59-13:66, Figures 3, 5E-5F. By the 2005 priority date of the ’076 patent, a POSITA would have been motivated to form an insulating sidewall in a semiconductor device with a double layer structure that includes an oxide film and a nitride film. A POSITA would have known, for example,

that using oxide and nitride films in insulating sidewall structures, e.g., in an ONO structure, provided known benefits including allowing independent control of spacer dimensions which optimizes device scaling. (See, e.g., U.S. Publication 2005/0040479, ¶¶ [0005]-[0006], Figure 4.) Additionally, a POSITA would have known by the 2005 priority date of the ’076 patent that forming a sidewall structure with different layers of oxide and nitride films can help with minimizing dopant loss from the source/drain region, thereby lowering parasitic resistance in the semiconductor device. (See, e.g., Bu, ¶ [0025].)

A width of a bottom surface of the gate insulating film along a gate length that is larger than a width of a bottom surface of the gate electrode along the gate length was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0050], [0056], [0068], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0040]-[0041], [0043]-[0045], [0047], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claims 1, 3, ¶¶ [0013], [0018]-[0037], [0041]-[0043], [0060], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0046], [0048]-[0049], [0119]-[0120], Figures 3-6, 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Inumiya 355, 16:27-34, Figures 9G, 9H, 9I; Mizushima, 18:4-30, Figures 13A-13K; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0181], [0199], [0215], Figure 13; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050],

[0054]-[0056], Figures 2, 5F; Houssa, 510; Plummer 82-83. By the 2005 priority date of the ’076 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figures 1-4.)

An end of the gate insulating film located under the insulating sidewall that has a tapered surface was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0018], [0050], [0056], [0085], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0043]-[0044], Figures 10-12; Kubicek, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], Figures 1, 3-14, 16-19; Ono, ¶¶ [0181], [0200], [0202], [0215]-[0216], Figure 43, 53, 57, 95, 104, 108; Watanabe_2004, Figure 5.

A gate insulating film located under the insulating sidewall that has a thickness which becomes smaller toward the end thereof was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0018], [0050], [0056], [0085], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0043]-[0044], Figures 10-12; Kubicek, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[007]7, Figures 1, 3-14, 16-19; Ono, ¶¶ [0181], [0200], [0202], [0215]-[0216], Figure 43, 53, 57; Watanabe_2004, Figure 5.

A width of the gate insulating film along a gate length that is larger than a width of part of the gate electrode in a middle position in height along the gate length was well-known prior to the ’076 patent. *See, e.g.*, ’076 patent, 1:25-60, 5:53-54, Figures 16A-16B; Ken Watanabe, HfSiON-CMOS technology for achieving high performance and high reliability, Semi. Forum Japan, 2005; ’076 patent file history, 2013-04-12 Non-Final Rejection at 2-7; Kamata, ¶¶ [0050], [0056], [0068], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0040]-[0041], [0043]-[0045], [0047], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26; Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono, Abstract, claims 1, 3, ¶¶ [0013], [0018]-[0037], [0041]-[0043], [0060], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0046], [0048]-[0049], [0119]-[0120], Figures 3-6, 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Inumiya 355, 16:27-34, Figures 9G, 9H, 9I; Mizushima, 18:4-30, Figures 13A-13K; Clevenger, 16:27-34, Figures 1-6; Ono, ¶¶ [0181], [0199], [0215], Figures 13, 57, 80, 108; Wang ’084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Houssa 510; Plummer 82-83. By the 2005 priority date of the ’076 patent, a POSITA would have known that extending a thinner layer of the high-k gate insulating film beyond the edges of the gate electrode to under the insulating sidewall provides known benefits, including, for example, minimizing electric field concentration at the edges of the gate electrode, that improve device performance and reliability. (See, e.g., JP-Ono, ¶¶ [0029]-[0035], Figures 1-4.)

Additional motivations to combine may be found in the ’076 patent invalidity charts.

In sum, by the time the application for the ’076 patent was filed, it was well known to design a semiconductor device as claimed at least because all the above was well known in the art before the ’076 patent, and a POSITA would have known that any and/or all the above techniques could be combined to fabricate a semiconductor device comprising a gate insulating film formed on an active region in a substrate and including Hf, a gate electrode formed on the gate insulating film, a insulating sidewall formed on each side surface of the gate electrode, and wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode. This is especially true here because all of the references disclose a semiconductor device with sidewalled transistors even if they do not disclose every aspect of a semiconductor device design. As such, a POSITA would have logically and predictably consulted all of the references together to design a complete semiconductor device with the claimed sidewalled transistors. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known semiconductor device designs to create different semiconductor devices with the claimed sidewalled transistors. Because all of these techniques were already known in the art for use in fabrication of semiconductor devices, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a

semiconductor device, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits 076-01 through 076-15, a POSITA would have been motivated to combine any of the references identified as prior art to the ’076 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar semiconductor device designs with sidewalled transistors (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Kamata, Title, Abstract, ¶¶ [003], [0008]-[0010], [0032], [0036], [0050], [0052]-[0053], [0056], [0068], [0073], [0093]-[0094], [0099]-[0100], Figures 1B(j), 5(c), 10(b); Guha, Title, Abstract, claims 1, 13, ¶¶ [0001], [0021]-[0023], [0026], [0037]-[0038], [0043], Figures 10-12; Matsumoto 135, Title, Abstract, claims 1, 10, 13, ¶¶ [0002], [0013]-[0046], [0060], [0062], [0064], [0068]-[0069], [0077], [0079]-[0082], [0085]-[0086], [0102]-[0103], [0105], [0107], [0137]-[0138], [0140], [0167], Figures 1, 2, 4, 10, 13, 19-26; Kubicek, Abstract, 1, 4, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0001], [0020], [0028]-[0029], [0033]-[0050], [0063]-[0064], [0068]-[0077], 1:54-2:3, Figure 1, 3-14, 16-19; JP-Ono, Title, Abstract, claim 1, ¶¶ [0001], [0013], [0018]-[0037], [0041]-[0044], [0076]-[0080], Figures 1-3, 6-10, 19-23; Matsumoto 185, Title, Abstract, claims 1, 7, ¶¶ [0001], [0010], [0011]-[0012], [0038], [0042]-[0045], Figures 3-6, 33; Vandooren, Title, Abstract, 324, 325, Figures 1-2; Inumiya 763, Title, Abstract, 1:5-6, 3:45-49, 4:15-22, 14:17-20, 19:43-49, 20:11-19, Figures 10G, 10I; Inumiya 355, Title, Abstract, 1:6-9, 5:29-37, 7:45-49, 12:43-45, 15:23-29, 15:63-16:8, 16:25-34, 33:55-64, 34:29-46, Figures 9E, 9G-9I, 50G-50I; Mizushima, Title, Abstract, claim 3, 1:14-29, 4:15-26, 17:26-56, Figures 13A-13L; Clevenger, Abstract, claims 1, 3, 4, 1:12-15, 1:17-28, 1:54-2:3, 3:40-46, 3:58-5:2, Figures 1-8;

Ono, Title, Abstract, claims 1, 8, 13, ¶¶ [0003], [0007]-[0008], [0158], [0160], [0166], Figure 4; Wang ’084, Title, Abstract, claims 1, 6, ¶¶ [0002], [0007]-[0011], [0020]-[0023], [0029]-[0039], [0040], [0044], [0047]-[0048], [0054]-[0055], Figures 2, 5F; Yu, 1:6-10, 1:14-29, 2:11-14, 2:28-34, 2:48-52, 2:63-67, 3:1-7, 3:14-33, Figure 1; Watanabe_2004, Title, Abstract, 507, Figures 2, 5, 21; Watanabe_2003, Title, 19, Figures 1, 11; Lee_2000, Title, 2.4.1, 2.4.2, Figures 1, 12; Andreoni, Title, Abstract, ¶¶ [0001], [0008], [0010], [0012], [0017], [0019], [0028], [0037], [0039], [0049], [0055]-[0057], Figures 1, 2A-2C; Wolf, 145-146, Figures 1-2, 5-25; Wang ’672, Abstract, claims 15, 23, ¶¶ [0002], [0008]-[0012], [0020]-[0022], [0024]-[0026], [0034], [0041], [0044]-[0045], [0047]-[0048], [0050]-[0052], Figure 3; Sim, 218; Lee_1999, Title, 6.1.1; Ahmed, 5:40-61, 9:39-57; Mutou, claims 1, 4-5, ¶¶ [0006]-[0007], [0042]-[0043], [0054]-[0055], [0072], [0080], [0111]-[0112], Figures 1-11; Houssa, 8-9, 510.

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, an end of the gate insulating film under the insulating sidewall retracted from an outer end of the insulating sidewall toward the gate electrode—to other references that relate to semiconductor device designs generally because all references teach designing transistors with particular technical specifications suitable for different purposes in semiconductor devices, and it would have been a trivial exercise to consult the references that taught more specific semiconductor device designs to fill in less specific disclosures in other references. *See, e.g.*, Kamata, ¶¶ [0050], [0056], [0068], [0093], Figures 1B(j), 5(c), 10(b); Guha, ¶¶ [0043]-[0045], Figures 10-12; Matsumoto 135, Abstract, claims 1, 11, 13, 14, ¶¶ [0034], [0038], [0040], [0064], [0103]-[0104], [0109]-[0110], [0114], [0137]-[0141], [0143], Figures 1-2, 5-6, 9-10, 13, 19-26, Kubicek, 1, Figure 1; Sasaki, Abstract, claim 1, ¶¶ [0020], [0028]-[0029], [0033]-[0050], [0056], [0063]-[0064], [0068]-[0077], [0079]-[0080], Figures 1, 3-14, 16-19; JP-Ono,

Abstract, claims 1, 3, ¶¶ [0013], [0018]-[0037], [0041]-[0043], [0060], [0076]-[0080], [0083]-[0084], Figures 1-3, 6-10, 19-23; Matsumoto 185, Abstract, claims 1, 7, ¶¶ [0011]-[0012], [0038], [0042]-[0046], [0048]-[0049], [0119]-[0120], Figures 3-6, 32-33; Vandooren, 324, 326, Figures 2, 12; Inumiya 763, 20:11-19, 20:34-49, Figures 10G, 10I; Inumiya 355, 16:27-34, Figures 9G-9I, 50F-50I; Mizushima, 18:4-30, Figures 13A-13K; Clevenger, Abstract, claims 1, 3, 4, 1:17-28, 3:58-5:2, Figures 1-6; Ono, ¶¶ [0200], [0202], [0215]-[0216], Figure 43, 53, 57, 95, 104, 108; Wang '084, Abstract, ¶¶ [0002], [0008]-[0011], [0020]-[0022], [0044], [0047]-[0050], [0054]-[0056], Figures 2, 5F; Kajiyama, ¶¶ [0029]-[0031], Figures 1(A)-(D).

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular semiconductor device with the teachings regarding other materials, components, and configurations used in other semiconductor devices for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques for designing semiconductor devices existed. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: fabricating a semiconductor device with sidewalled transistors. This is thus a combination of prior art elements (*e.g.*, a semiconductor device comprising a gate insulating film formed on an active region in a substrate and including Hf, a gate electrode formed on the gate insulating film, a insulating sidewall formed on each side surface of the gate electrode, and wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and an end of the gate insulating film under the insulating sidewall is retracted from an

outer end of the insulating sidewall toward the gate electrode.) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of semiconductor fabrication were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

Additional obviousness combinations of the references identified here are possible, and TSMC may rely on such combination(s) in this litigation. In particular, TSMC is currently unaware of AICP's allegations with respect to the level of skill in the art and the qualifications of a POSITA. TSMC is also unaware of the extent, if any, to which AICP may contend that limitations of the claims at issue are not disclosed in the prior art identified by TSMC as anticipatory, and the extent to which AICP will contend that elements not disclosed in the asserted patent specifications would have been known to a POSITA. And TSMC does not yet know how the Court will construe terms in the asserted claim. TSMC is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. TSMC reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case No. IPR2025-00831 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the ’076 patent.

f. The ’779 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below or referenced herein, and in Exhibits 779-01 through 779-17 would have rendered obvious one or more Asserted Claims of the ’779 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits 779-01 through 779-17, TSMC contends that all asserted claims are rendered obvious by Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, and/or AAPA alone, or in combination with other references, including the references identified above in Section II.A.6 and those identified below and/or discussed in the attached exhibits 779-01 through 779-17.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 779-01 through 779-18 and Herein) [19]:
779-01	Gilmer	One or more of Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-02	Chowdhury	One or more of Gilmer, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-03	Torii	One or more of Gilmer, Chowdhury, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-04	Lin	One or more of Gilmer, Chowdhury, Torii, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-05	Hsu	One or more of Gilmer, Chowdhury, Torii, Lin, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-06	Iwamoto	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis,

[19] To the extent any reference is cited in Exhibits 779-01 to 779-17, but not referenced here, any omission was unintentional and Defendant intends to rely on its identification of any such combinations in Exhibits 779-01 to 779-17.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 779-01 through 779-18 and Herein) [19]:
		Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-07	Suzuki	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-08	Irino	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-09	Fujiwara	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-10	Hori	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-11	Greene	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-12	Luan	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 779-01 through 779-18 and Herein) [19]:
		Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-13	Intel QX9650	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-14	Chen	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-15	Yu	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-16	Wang	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve
779-17	Applicant Admitted Prior Art (AAPA)	One or more of Gilmer, Chowdhury, Torii, Lin, Hsu, Iwamoto, Suzuki, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’779 patent, it would have been obvious to a POSITA at the

time of the alleged invention of the ’779 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits 779-01 through 779-17 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits 779-01 through 779-17, including for the reasons described below. A POSITA at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’779 patent relates to a semiconductor device comprising a first MIS transistor and a second MIS transistor of the same conductivity type formed on an identical semiconductor substrate. The asserted claims recite elements that were conventional in manufacturing transistors well before the priority date of the ’779 patent (alleged to be September 14, 2010). A semiconductor device with two MIS transistors of the same conductivity type on an identical semiconductor substrate was well-known prior to the ’779 patent. *See, e.g.*, ’779 patent file history, 2013-08-29 Non-Final Rejection at 3-4; *see also, e.g.*, Gilmer at 1:7-10, 1:14-50, 1:57-61, 2:36-46, 2:46-48, :58-65, 3:9-12, 3:44-47, 4:35-40, 4:43-47, Figure 4, Abstract, claims 1, 14; Chowdhury at Title, 1:7-9, 1:16-38, 1:59-62, 2:10-29, 2:30-38, 2:55-58, 3:4-6, 3:21-32, 3:38-4:3, 9:35-65, Figure 8, claim 14; Torii at Abstract, 1:9-14, 1:16-39, 2:51-65, 3:54-61, 3:62-65, 4:10-14, 4:30-32, 4:58-60, 4:61-67, 5:1-4, 6:14-18, 7:6-12, 10:39-42, Figure 1, claims 1, 9; Lin at Title, 1:29-32, 3:26-40, 5:42-59, 6:17-24, 6:25-28, 6:35-49, 6:50-62, 6:63-7:4, 8:21-23, 9:19-22, 9:27-29, 9:38-45, Figures 2, 3, 5C; Hsu at Title, 1:22-25, 1:46-54, 1:62-64, 2:55-3:3, 3:12-28, 3:29-48,

3:49-61, 3:62-4:17, 4:18-47, 6:63-63, 7:1-29, 10:40-55, Figure 2K; Iwamoto at Title, Abstract, ¶¶ [0003], [0012], [0015], [0017], [0018], [0019], [0021]-[0052], [0054], [0055], [0056], [0057], [0058], [0059], [0063], [0064], [0065], [0066], [0073], [0074], [0075], [0076], [0081], [0082], [0086], [0087], [0088], [0089], [0101]-[0104], claim 1, Figures 1, 2A, 3, 4; Suzuki at Title, 1:12-19, 1:21-29, 2:55-61, 3:45-59, 5:53-64, 5:65-6:2, 7:23-28, 7:35-49, 7:50-52, 8:30-35, 8:39-44, 8:45-64, 8:65-9:10, 9:11-18, 9:36-43, 9:44-58, 9:59-65, 9:66-10:4, 10:22-27, Abstract, Figure 1D, 2E, 3B, 3D, 4C; Irino at Title, ¶¶ [0001], [0020], [0035]-[0036], [0038]-[0041], [0047]-[0049], [0051]-[0061], [0065]-[0066], [0074], Figures 4(d), 5(f), 5(h), 6(i), 6(j), 6(k), 6(l), claim 1; Fujiwara at Title, [Summary], [Solution means], ¶¶ [0001], [0012]-[0014], [0026], [0028], [0054]-[0060], [0063], [0093], Figures 11, 17-20, 22, 27, 33, claims 1, 5-7; Hori at Title, Abstract, 1:16-19, 3:29-31, 3:54-59, 7:54-8:6, 8:25-38, 8:42-57, Figures 4A, 4B, 4C, 4F, 4G; Greene at 1:7-10, 1:63-65, 2:7-42, 3:50-5:5, 5:31-36, 5:48-7:39, 7:61-9:59, 11:10-43, 11:44-13:8, Figures 1-12, claims 1, 6, 10, 17; Luan at Title, Abstract, ¶¶ [0002], [0014]-[0015], [0018], [0021]-[0024], [0037]-[0042], [0044]-[0050], [0054]-[0055], [0067]-[0069], [0071]-[0072], [0074]-[0080], [0091], [0094], [0096], [0098], [0100], [0102], [0105]-[0106], [0108]-[0109], [0112]-[0114], Figures 1-4, 8, 13-19, claims 1, 7, 13, 17; Intel QX9650 at pages 1, 2, 8, 9, 14, 16, 17, 25, 26, 39, 40, 60, 62, 63, 64, 118; Chen at 1:12-14, 1:18-26, 3:6-19, 3:34-60, 4:30-33, 4:34-48, 4:49-57, 8:27-42, 8:50-63, 9:9-20, claims 14, 31; Yu at 1:27-31, 2:30-33, 4:18-24, 5:4-12, 5:14-15, 6:10-24, 6:25-41, Figure 1; Wang at 1:11-18, 2:18-25, 2:40-42, 2:53-54, 3:57-4:3, 6:28-32, 6:56-7:11, 7:29-31, 7:40-45, 8:43-62, Figures 2, claim 14; AAPA at 1:46-60, Fig. 13; Weste at Fig. 1.8; Wolf at Fig. 1-2; Plummer at iii, 52; Sze at Title, Fig. 14; ITRS at 7; Koyama at Title, Abstract, 1:14-15, 3:14-15, 3:45-46, 4:19-20, 5:41-43, 5:46-48, 5:51-53, 12:24-34, 12:37-42, 12:49-13:2, 16:33-34, 16:38-42, 20:24-30, Fig. 9, Fig. 16, claims 1, 8, 15; Mise at [0002], [0005], [0070], [0096], [0097],

[0108], Fig. 11; Onishi at 1:39-42, 1:58-61, 2:16-19, 4:27-29, 4:50-55; Liaw at [0003], [0016], [0059]; Stahrenberg at Title, Abstract, 2:51-54, 3:22-25, 3;40-52, 11:27-36, Fig. 2; Park at Fig. 1(d); Efavi at 433; Lu at 92; Min at Title, Abstract, 1:7-9, 1:50-54, 2:27-36, 2:50-57, 6:43-49, 7:18-21, Fig. 9, claim 18; Tseng at Title, Abstract, 1:18-22, 2:25-34, 3:33-37, 3:59-62, 4:9-13, 7:41-45, 8:49-51, 9:33-36, 14:49-52, 14:65-15:2, 15:14-20, 18:56-62; Karve at [0002], [0007]-[0014], [0017], [0019], [0027], Fig. 8; Tsutsui at Abstract, Introduction, Device Structure and Transistor Characteristics, Fig. 1, Fig. 3, Common Channel Dosage for Core and I/O Tr.

A first MIS transistor including a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film, and a second MIS transistor including a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film, was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 2:43-46, 2:46-55, 3:9-33, 3:44-4:7, 4:35-43, 4:43-47, Figure 4, Abstract, claims 1, 7-8, 14; Chowdhury at 3:4-6, 3:19-32; 4:56-5:14, 5:19-29, 5:35-6:3, 6:26-41, 6:42-48, 6:54-57, 7:8-14, 7:21-49, 8:44-66, 9:3-34, 9:35-65, Figure 8, Abstract; Torii at 4:1-4, 5:1-4, 5:5-13, 5:14-18, 5:33-41, 5:42-49, 5:62-6:6, 6:14-23, 6:24-27, 6:55-63, 6:66-7:5, 7:6-22, 8:14-23, 9:32-38, 10:34-38, 12:13-21, Figures 1, 3, 8, claim 1; Lin at 6:17-24, 6:50-62, 8:21-23, 8:49-63, 9:4-7, 9:7-16, 9:19-22, 9:22-27, 9:27-29, 9:29-45, Figure 3, 4A, 5A, 5B, 5C; Hsu at 1:22-33, 1:34-45, 1:46-61, 1:62-2:14, 3:12-20, 3:49-61, 4:18-47, 6:63-63, 7:1-29, 8:18-34, 8:35-59, 8:60-63, 9:14-24, 9:25-44, 9:56-10:6, 10:7-25, 10:26-39, Figures 1, 2H, 2I, 2J, 2K; Iwamoto at ¶¶ [0018], [0055], [0056], [0057], [0060], [0061], [0063], [0067], [0068], [0074], [0075], [0076], [0077], [0078], [0079], [0081], [0082], [0084], [0086], [0087], [0091], [0093], [0094], [0101], [0102], [0103], 0104], [0105], [0111], claim 1, Figures 2A, 4, 5A, 5B, 5D, 6A, 6B, 6D, 9A, 9B, 9D, 14, 15; Suzuki at Abstract, 3:45-59, 5:53-64, 5:65-6:2,

8:39-44, 8:45-64, 8:65-9:10, 9:11-18, 9:36-43, 9:44-58, Figures 1D, 2B, 2D, 2E, 3B; Irino at ¶¶ [0035]-[0036], [0038]-[0041], [0053]-[0060], Figures 5(f), 5(h), 6(i), 6(j), 6(k); Fujiwara at ¶¶ [0008], [0016]-[0019], [0021]-[0022], [0024], [0026], [0028], [0034]-[0038], [0041], [0043]-[0049], [0063]-[0069], [0083]-[0087], [0089]-[0091], Figures 5, 8-9, 11, 16-18, 26, 30-35; Hori at 7:57-8:6, 8:25-38, 8:42-57, Figures 4A, 4B, 4C, 4F, 4G; Greene at 4:56-5:5, 5:31-36, 5:48-7:39, 7:61-8:50, 11:10-12:15, Figures 2-8, 10-12, claims 1, 6, 10, 17; Luan at ¶¶ [0038]-[0039], [0041]-[0042], [0044]-[0050], [0054]-[0055], [0068]-[0069], [0071]-[0072], [0074]-[0076], [0078]-[0079], [0096], [0098], [0100], [0105], [0112]-[0113], Figures 1-5, 8, 13-19, claim 17; Intel QX9650 at 2, 14, 16, 18, 19, 20, 22, 25, 26, 29, 30, 31, 33-34, 35-36, 37-38, 40, 60, 62, 63, 64, 112, 118; Chen at 3:6-19, 4:34-48, 4:49-57, 6:46-53, 7:1-8, 7:9-19, 7:35-42, 7:43-8:3, 8:10-26, 8:26-42, Fig. 2e, Fig. 3e, Fig.3g , Fig. 3h, claims 14, 24; Yu at 5:10-12, 5:14-15, 6:3-41, 7:1-14, 7:23-30, 7:41-46, 7:58-62, 8:1-34, Figures 1, 2, 4, 5; Wang 3:57-4:3, 6:28-32, 6:56-7:11, 7:29-31, Figure 2; AAPA at 1:61-2:31; Weste at Fig. 1.8; Wolf at Fig. 1-2; Plummer at 52-53, Fig. 2-33; Koyama at 12:37-38, 12:49-13:2, 16:33-34, 16:39-42, 17:5-45, Fig. 9, Fig. 22; Mise at [0071], [0072], Fig. 1; Onishi at Fig. 1, 4:37-42, 4:43-49; Liaw at [0050], [0059]; Stahrenberg at 4:19-37, Fig. 2; Park at 149, Fig. 1(d); Min at 2:27-36, 6:43-39, 3:60-4:22, 4:52-61; Tseng at 2:30-36, 2:41-53, 3:37-55, 8:55-67, 9:13-29, 9:37-55, 10:4-14, 10:63-11:51; Karve at [0019], [0021], [0023], [0024], [0025], [0026], [0027], Fig. 3, Fig. 5, Fig. 6, Fig. 7, Fig. 8; Tsutsui at Abstract, Device Structure and Transistor Characteristics, Fig. 1.

A first gate insulating film including a first interface layer being in contact with the semiconductor substrate with a first high dielectric constant insulating film formed on the first interface layer, and a second gate insulating film including a second interface layer being in contact with the semiconductor substrate with a second high dielectric constant insulating film formed on

the second interface layer, was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 2:46-55, 3:9-33, 3:44-4:7, Abstract, 4:43-47, Figure 4, claims 1, 14; Chowdhury at 4:56-5:14, 5:35-6:3, 6:26-41, 8:44-66, 9:3-34, 9:35-65, Figure 8, Abstract; Torii at 2:28-49, 4:1-4, 5:14-29, 5:33-41, 6:28-65, 6:66-7:5, 8:14-23, 9:32-38, Figures 1, 6, 8, claim 1; Lin at 2:3-14, 7:30-8:1, 8:34-48, 7:23-30, 8:49-63, 9:4-7, 9:19-22, 9:22-27, 9:27-29; Figure 4A, Figure 5A, 5B; Hsu at 2:43-49, 3:12-20, 8:18-34, 8:35-59, 8:60-63, 9:14-24, 9:25-44, 9:56-10:6, Figures 1, 2H, 2I, 2J, 2K; Iwamoto at ¶¶ [0018], [0055], [0056], [0060], [0074], [0076], [0101], [0102], [0103], [0105], Figures 2A, 5A, 5B; Suzuki at Abstract, 3:45-59, 5:53-64, 5:65-6:2, 8:39-44, 8:45-64, 8:65-9:10, 9:11-18, 9:36-43, 9:44-58, 9:44-58, Figures 1D, 2B, 2D, 2E, 3A, 3B; Irino at ¶¶ [0016], [0023], [0035]-[0041], [0045], [0055]-[0058], [0064]-[0065], [0068], [0072], Figures 5(g), 5(h), 6(i), 6(k); Fujiwara at ¶¶ [0008], [0021]-[0022], [0032], [0034], [0037]-[0038], [0043], [0045], [0047]-[0048], [0067]-[0068], [0083], [0085]-[0086], [0090], Figures 8, 16-18, 26, 30-35; Hori at 7:57-8:6, 8:25-38, 8:42-57, 9:35-36, Figures 4A, 4B, 4C, 4F, 4G; Greene at 4:56-5:30; Luan at ¶¶ [0041]-[0042], [0044]; Intel QX9650 at 1, 2, 14, 25, 26, 33-34, 37-38, 40, 64, 112, 118; Chen at 7:9-19; Wang at 2:53-61, 4:4-5:33, 5:62-67, 6:56-7:11, 7:29-31, Figures 1a, 1b, 2, claims 14, 15, 22; AAPA at 2:16-24; Koyama at 12:49-13:2, 17:5-14, Figs. 1, 4, 5, 17, 30, 31; Stahrenberg at 4:19-24, 4:52-57, 5:51-59, Fig. 2; Min at 3:60-4:22; Tseng at 10:4-24; Karve at [0021], [0024], Fig. 3, Fig. 6.

The first interface layer having a thickness larger than that of the second interface layer was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 1:14-32, 2:46-55, 2:60-65, 3:17-21, 3:44-45, Abstract, Figure 4, claims 1, 14; Chowdhury at 1:32-38, 3:52-58, 5:56-6:3, 7:50-8:9, 9:35-50, 9:63-65, Figure 8; Torii at 1:9-14, 1:41-2:14, 2:35-49, 2:66-3:8, 4:4-6, 5:14-29, 5:62-6:3, 12:13-21, Figure 1, claim 1; Lin at 3:26-40, 9:18-45, Figures 5A, 5B, 5C; Hsu at 1:22-33, 1:34-45, 1:46-61, 1:62-2:14, 2:34-37, 3:16-20, 4:18-47, 8:18-34, 8:35-59, 8:60-63, 9:14-24, 9:25-44,

Figures 2H, 2I, 2J; Iwamoto at Abstract, ¶¶ [0017], [0018], [0060], [0067], [0074], [0075], [0076], [0081], [0101]-[0116], claim 1; Suzuki at Abstract, 1:22-30, 5:53-64, 5:65-6:2, 7:35-49, 8:39-44, 9:11-18, 9:29-33, 9:36-43, 10:22-27, 13:41-44, Figures 2E, 4C; Irino at ¶¶ [0001], [0020], [0047], [0055], [0058], [0065], [0074], Figure 6(i), claim 1; Fujiwara at [Solution means], ¶¶ [0016]-[0017], claim 1; Hori at Abstract, 1:16-19, 7:62-8:6, 8:25-38, Figures 4B, 4C, 4F, claim 1; Greene at 4:59-5:3, 5:64-6:20, 6:54-7:31, 11:10-43; Luan at ¶¶ [0041]-[0042], [0044]; Intel QX9650 at 40, 64, 112; Chen at 7:20-34, 8:43-49, Fig. 3b, Fig. 3h; Wang at 2:50-52, 6:49-51, 6:67-7:3, claim 14; Wolf at 121; Stahrenberg at 5:5-10.

Each of the first interface layer and the second interface layer made of a silicon dioxide film or a silicon oxynitride film was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 2:46-55, 2:67-3:6, 3:10-14, Figure 4, Abstract, claims 2-3, 15; Chowdhury at 4:56-5:7, 5:54-6:25; Torii at 5:14-29, 6:28-65, 8:14-23, 8:24-40, 9:32-38, claim 1; Lin at 2:3-14, 7:23-30, 8:34-48, 8:51-56, 9:19-22, 9:22-27, Figures 4A, 5A; Hsu at 9:14-24, Figure 2J; Iwamoto at ¶¶ [0060], [0067], [0074], [0075], [0076]; Suzuki at 2:12-21, 4:4-20, 9:4-18, 12:60-63, 13:12-15, 13:21-24, 13:41-44; Irino at [0035]-[0036], [0038]-[0041], [0070]; Fujiwara at ¶¶ [0008], [0021], [0023], [0032], [0038], [0043], [0068], [0086], [0090], Figures 17, 26, 33-35; Hori at 7:62-65, 8:25-38, Figures 4B, 4F; Greene at 4:59-5:3; Luan at ¶¶ [0041], [0044]; Intel QX9650 at 1, 2, 14, 25, 26, 37-38, 40, 118; Chen at 7:9-19; Yu at 7:11-14; Wang at Abstract, 1:11-18, 2:26-33, 2:38-39, 2:53-61, 4:4-20, 4:59-5:10, 6:56-7:11, 7:63-67, Figures 1a, 1b, 2, claim 14; AAPA at 2:16-24; Koyama at 8:4-14, 13:53-57; Stahrenberg at 4:57-59; Min at 4:14-22; Tseng at 10:4-14.

Each of the first and second high dielectric constant insulating films containing hafnium or zirconium was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 3:47-54, claims 4, 17; Chowdhury at 6:26-41; Torii at 5:33-36, 10:9-33; Lin at 2:3-14, 7:30-8:1, 9:4-7, 9:27-29,

Figures 5B, 5C; Hsu at 9:64-10:12, Figure 2K; Iwamoto at ¶¶ [0060], [0067], [0074], [0075], [0076]; Suzuki at 6:8-15, 6:16-34, 7:35-49, 9:44-58; Irino at ¶¶ [0016], [0023], [0037], [0045], [0055]-[0058], [0064], [0068], Figures 5(h), 6(i); Fujiwara at ¶ [0032]; Greene at 5:13-30; Luan at ¶ [0041]; Intel QX9650 at 2, 10, 14, 25, 26, 33-34, 37-38, 40, 64, 112, 118; Chen at 7:9-19; Wang at Abstract, 2:33-38, 3:4-8, 4:32-52, 5:62-65, 7:32-34, claims 6, 13, 22; AAPA at 2:16-24; Houssa at 8-9, 510; Wolf at 145-146; Koyama at 2:58-63, 6:25-37, 6:47-50, 12:49-13:2, 17:5-45; Mise at [0003]; Liaw at [0059]; Stahrenberg at 5:61-64; Min at 1:13-35, 4:5-11; Tseng at 10:15-24; Karve at [0024].

The first and second high dielectric constant insulating films equal in thickness was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 3:54-4:7, Figure 4, Abstract, claims 1, 14; Chowdhury at 6:26-7:28, Figures 6, 8; Torii at 4:6-9, 5:33-37, 6:66-7:5, 12:13-21, Figure 1, claim 1; Lin at 9:4-16, 9:27-29, Figures 5B, 5C; Hsu at 9:14-24, 9:25-30, 9:56-10:12, Figures 1, 2J, 2K; Iwamoto at ¶¶ [0060], [0067], [0074], [0075], [0076], [0078], Figures 14, 15; Suzuki at 9:36-43, 9:44-58, 9:59-65, 9:66-10:4, 10:22-27, Figures 2E, 3B, 3D, 4C; Irino at ¶¶ [0016], [0023], [0035]-[0041], [0045], [0055]-[0058], [0064]-[0065], [0068], [0072], Figures 5(f)-6(k); Fujiwara at ¶¶ [0008], [0021]-[0022], [0032], [0034], [0037]-[0038], [0043], [0045], [0047]-[0048], [0067]-[0068], [0083], [0085]-[0086], [0090], Figures 8, 16-18, 26, 30-35; Greene at 5:26-30, Figures 9, 12, claim 2, 11; Luan at ¶¶ [0041], [0044], [0068], [0078], [0098], [0100], [0105], Figures 1, 5, 8, 14, 16-19, claim 17; Intel QX9650 at 40, 64, 112; Wang at 4:55-58, 5:62-65, 7:29-31, Figure 2, claim 14; Koyama at 13:51-64, 16:38-42; Onishi at 2:41-53, 2:61-63; Liaw at [0021]-[0022], [0054], claim 1; Stahrenberg at 10:62-68, Fig. 8; Min at 3:60-66, 4:21-33, Fig. 4, Fig. 9; Karve at [0026], Fig. 6.

The first and second gate electrodes made of an identical material was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 4:35-43, 4:43-47, Figure 4, claims 7-8, 14; Chowdhury at 6:54-7:28, 9:50-65, Figures 6, 8; Torii at 7:6-22, 10:34-38, Figures 1, 8; Lin at 9:7-16, 9:27-29, Figure 5C; Lin at 3:26-40, 9:18-45, Figures 5A, 5B, 5C; Hsu at 10:7-25, 10:26-39; Iwamoto at ¶¶ [0061], [0068], [0074], [0075], [0076], [0078], [0082], [0091]; Suzuki at 9:44-58, 9:59-65, 9:66-10:4, Figures 3B, 3D, 4C; Irino at ¶¶ [0059]-[0060], Figures 6(j), 6(k); Fujiwara at ¶¶ [0022], [0033], [0043], [0048], [0069], [0086], [0091], Figures 9, 17-18, 33; Hori at 8:42-50, Figure 4G; Greene at 7:32-39, Figures 7, 9, 12; Luan at ¶¶ [0045]-[0050], [0054]-[0055], [0069], [0071]-[0072], [0074]-[0076], [0078]-[0079], [0100], [0102], [0105]-[0106], Figures 2-5, 8, 13-19, claim 17; Intel QX9650 at 2, 15, 25, 26, 33-34, 37-38, 40, 118; Yu at 7:23-30, 7:41-46, 7:58-62, 8:1-22, Figures 1, 2, 3, 4, 5; Wang at 7:59-63; Koyama at 12:49-59, 13:32-34, 16:38-42, 16:54-61; Mise at [0156], [0145]-[0146], [0072], Fig. 11; Onishi at Fig. 1, 4:37-49, 5:39-51; Liaw at [0020]; Stahrenberg at 10:15-20; Min at 6:1-4, 6:10-49 Fig. 8, Fig. 9; Karve at [0025], [0026], Fig. 7; Tsutsui at Abstract, Fig. 1.

An effective work function of the first MIS transistor higher than an effective work function of the second MIS transistor, as described in the specification, was also well-known prior to the ’779 patent. *See, e.g.*, Gilmer at 2:46-55, 2:60-65, 3:9-33, 3:44-4:7, Abstract; Chowdhury at 1:32-38, 3:38-58, 4:56-5:14, 5:19-29, 5:35-6:3, 6:26-41, 6:42-48, 7:50-8:9, 9:35-50, 9:63-65, Figure 8; Torii at 1:9-14, 4:1-6, 5:14-29, 5:33-41, 5:62-6:6, 6:55-63, 6:66-7:5, 8:14-23, 9:32-28, 12:13-21; Hsu at 1:22-33, 1:34-45, 1:46-61, 1:62-2:14, 2:34-37, 3:16-20, 4:18-47, 8:18-34, 8:35-59, 8:60-63, 9:14-24, 9:25-44, 9:56-64, Figures 2H, 2I, 2J, 2K; Iwamoto at Abstract, ¶¶ [0017], [0018], [0060], [0067], [0074], [0075], [0076], [0081], [0101]-[0116], claim 1; Suzuki at Abstract, 1:22-30, 5:53-64, 5:65-6:2, 7:35-49, 8:39-44, 9:11-18, 9:29-33, 9:36-43, 10:22-27, 13:41-44,

Figures 2E, 4C; Irino at ¶¶ [0001], [0020], [0047], [0055], [0058], [0065], [0074], Figure 6(i), claim 1; Fujiwara at [Solution means], ¶¶ [0016]-[0017], claim 1; Hori at Abstract, 1:16-19, 7:62-8:6, 8:25-38, Figures 4B, 4C, 4F, claim 1; Greene at 5:31-36, 10:33-48, 10:61-11:9, 13:9-30, 13:38-52; Luan at ¶¶ [0021]-[0022], [0045], [0053], [0066]-[0067], [0069], [0071], [0075]-[0078], [0080], [0086]-[0087], [0089], [0103]-[0104], [0106]-[0107], [0109], [0112]-[0113]; Intel QX9650 at 40, 64, 112; Chen at 1:12-14, 1:18-32, 1:36-56, 1:63-2:54, 7:43-8:49, claims 14, 31; Yu at Abstract, 4:9-17, 5:51-54, 5:61-67, 6:1-3, 7:1-5, 7:63-67, claims 1, 7; Wang at 2:50-52, 6:49-51, 6:67-7:3, claim 14; AAPA at 2:24-27; Koyama at 16:54-61, Fig. 28; Mise at Fig. 11, [0153], [0195]; Onishi at 6:14-37, 8:36-53; Liaw at [0019], [0050]; Stahrenberg at 5:6-18, 6:10-19; Park at 124, Fig. 7; Lu at Fig. 4; Tseng at 15:3-12, Fig. 10, 15:56-63, 15:64-67, Fig. 11, 16:47-54, 16:54-17:3; Fig. 12, 17:8-31; Fig. 13; Karve at [0019]; Alshareef at Abstract, 112114-1, 112114-2, 112114-3, Fig. 3, Fig. 5; Bai at 231, 232, 233, Fig. 1, Fig. 2; Wang-Paper at 2871, 2872, 2873, 2875, Table 1, Fig. 2, Fig. 3, Fig. 7, Fig. 8, Fig. 9, Fig. 10, Fig. 11; Tsutsui at Introduction, Common Channel Dosage for Core and I/O Tr., Fig. 10; Burham-Thesis at 33-55; Ranade-Thesis at 37-58; Wong-Thesis at 8-32.

In sum, by the time the application for the ’779 patent was filed, it was well known to design a semiconductor device as claimed at least because all the above was well known in the art before the ’779 patent, and a POSITA would have known that any and/or all the above techniques could be combined to fabricate a semiconductor device with a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate, wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film, the second MIS transistor includes a second gate insulating film formed on a second active region

in the semiconductor substrate and a second gate electrode formed on the second gate insulating film, the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer, the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer, the first interface layer has a thickness larger than that of the second interface layer, and each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film. This is especially true here because all the references disclose a semiconductor device with MIS transistors even if they do not disclose every aspect of a semiconductor device design. As such, a POSITA would have logically and predictably consulted all the references together to design a complete semiconductor device with the claimed MIS transistors. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known semiconductor device designs to create different semiconductor devices with the claimed MIS transistors. Because all of these techniques were already known in the art for use in fabrication of semiconductor devices, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a semiconductor device, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior

art references in Exhibits 779-01 through 779-17, a POSITA would have been motivated to combine any of the references identified as prior art to the ’779 patent for these reasons provided above and the additional reasons provided below.

For example, a person of ordinary skill in the art (POSITA) would have been motivated to form transistors of the same-conductivity type on a common substrate due to the well-known and understood benefits of process simplification, cost reduction, and yield improvement in semiconductor fabrication. To that end, a POSITA would have been motivated to combine any of the references with, for example but not limited to, Gilmer, Torii, Chowdhury, Hsu, Lin, Suzuki, Iwamoto, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, or Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve. Specifically, a POSITA would know that forming transistors of the same conductivity type on a substrate streamlines the fabrication process by reducing process complexity and improving manufacturing efficiency. For example, the number of mask steps required is reduced which reduces defectivity and fabrication errors and lowers production costs by reducing the need for additional processing steps or materials. Additionally, a POSITA would have been motivated to allow for the formation of transistors with different electrical characteristics (e.g., I/O transistors, low power transistors, low standby power transistors) which can be tailored for different applications within the circuit, while simultaneously achieving layout uniformity, device matching, and performance consistency, all of which are desirable in many circuit applications. A POSITA would have considered the combination a matter of routine optimization to consolidate transistor types to reduce process and performance variability, simplify isolation requirements, and enhance electrical characteristics such as threshold voltage matching

and channel mobility uniformity. Forming the same-type of transistors on a common substrate is a straightforward design choice that flows logically from already established design goals and benefits—namely, reliability, reproducibility, and efficiency. Further, the result is a predictable improvement in manufacturability and cost-effectiveness, naturally leading engineers to pursue such optimization using familiar elements and methodologies.

Further, the prior art references identified above and the accompanying invalidity claim charts teach similar semiconductor device designs with MIS transistors (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Gilmer at 1:7-10, 1:57-61, 2:36-46, 2:58-65, 3:9-12, 3:44-47, 4:35-40, 4:43-47, Figure 4, Abstract, claims 1, 14; Chowdhury at Title, 1:7-9, 1:16-38, 1:59-62, 2:10-29, 2:30-38, 2:55-58, 3:4-6, 3:21-32, 3:38-4:3, 9:35-65, Figure 8; Torii at Abstract, 1:9-14, 1:16-39, 2:51-65, 3:54-61, 3:62-65, 4:30-32, 4:58-60, 4:61-67, 5:1-4, 6:14-18, 10:39-42, Figure 1, claims 1, 9; Lin at Title, 1:29-32, 3:26-40, 5:42-59, 6:17-24, 6:25-28, 6:35-49, 6:50-62, 6:63-7:4, 8:21-23, 9:19-22, 9:27-29, 9:38-45, Figures 2, 3, 5C; Hsu at Title, 1:22-25, 1:46-54, 1:62-64, 2:55-3:3, 3:12-28, 3:29-48, 3:49-61, 3:62-4:17, 4:18-47, 6:63-63, 7:1-29, 10:40-55, Figure 2K; Iwamoto at Title, Abstract, ¶¶ [0003], [0012], [0015], [0017], [0018], [0019], [0021]-[0052], [0054], [0055], [0056], [0057], [0058], [0059], [0063], [0064], [0065], [0066], [0073], [0074], [0075], [0076], [0081], [0082], [0086], [0087], [0088], [0089], [0101]-[0104], claim 1, Figures 1, 2A, 3, 4; Suzuki at Title, 1:12-19, 1:21-29, 2:55-61, 3:45-59, 5:53-64, 5:65-6:2, 7:23-28, 7:35-49, 7:50-52, 8:30-35, 8:39-44, 8:45-64, 8:65-9:10, 9:11-18, 9:36-43, 9:44-58, 9:59-65, 9:66-10:4, 10:22-27, Abstract, Figure 1D, 2E, 3B, 3D, 4C; Irino at Title, ¶¶ [0001], [0020], [0035]-[0036], [0038]-[0041], [0047]-[0049], [0051]-[0061], [0065]-[0066], [0074], Figures 4(d), 5(f), 5(h), 6(i), 6(j), 6(k), 6(l), claim 1; Fujiwara at Title, [Summary], [Solution means], ¶¶ [0001], [0012]-[0014],

[0026], [0028], [0054]-[0060], [0063], [0093], Figures 11, 17-20, 22, 27, 33, claims 1, 5-7; Hori at Title, Abstract, 1:16-19, 3:29-31, 3:54-59, 7:54-8:6, 8:25-38, 8:42-57, Figures 4A, 4B, 4C, 4F, 4G; Greene at 1:7-10, 1:63-65, 2:7-42, 3:50-5:5, 5:31-36, 5:48-7:39, 7:61-9:59, 11:10-43, 11:44-13:8, Figures 1-12, claims 1, 6, 10, 17; Luan at Title, Abstract, ¶¶ [0002], [0014]-[0015], [0018], [0021]-[0024], [0037]-[0042], [0044]-[0050], [0054]-[0055], [0067]-[0069], [0071]-[0072], [0074]-[0080], [0091], [0094], [0096], [0098], [0100], [0102], [0105]-[0106], [0108]-[0109], [0112]-[0114], Figures 1-4, 8, 13-19, claims 1, 7, 13, 17; Intel QX9650 at pages 1, 2, 8, 9, 14, 16, 17, 25, 26, 39, 40, 60, 62, 63, 64, 118; Chen at 1:12-14, 1:18-26, 3:6-19, 3:34-60, 4:30-33, 4:34-48, 4:49-57, 8:27-42, 8:50-63, 9:9-20, claims 14, 31; Yu at 1:27-31, 2:30-33, 4:18-24, 5:4-12, 5:14-15, 6:10-24, 6:25-41, Figure 1; Wang at 1:11-18, 2:18-25, 2:40-42, 2:53-54, 3:57-4:3, 6:28-32, 6:56-7:11, 7:29-31, 7:40-45, 8:43-62, Figures 2, claim 14; AAPA at 1:46-60, Fig. 13; Weste at Fig. 1.8; Wolf at Fig. 1-2; Plummer at iii, 52; Sze at Title, Fig. 14; ITRS at 7; Koyama at Title, Abstract, 1:14-15, 3:14-15, 3:45-46, 4:19-20, 5:41-43, 5:46-48, 5:51-53, 12:24-34, 12:37-42, 12:49-13:2, 16:33-34, 16:38-42, 20:24-30, Fig. 9, Fig. 16, claims 1, 8, 15; Mise at [0002], [0005], [0070], [0096], [0097], [0108], Fig. 11; Onishi at 1:39-42, 1:58-61, 2:16-19, 4:27-29, 4:50-55; Liaw at [0003], [0016], [0059]; Stahrenberg at Title, Abstract, 2:51-54, 3:22-25, 3;40-52, 11:27-36, Fig. 2; Park at Fig. 1(d); Efavi at 433; Lu at 92; Min at Title, Abstract, 1:7-9, 1:50-54, 2:27-36, 2:50-57, 6:43-49, 7:18-21, Fig. 9, claim 18; Tseng at Title, Abstract, 1:18-22, 2:25-34, 3:33-37, 3:59-62, 4:9-13, 7:41-45, 8:49-51, 9:33-36, 14:49-52, 14:65-15:2, 15:14-20, 18:56-62; Karve at [0002], [0007]-[0014], [0017], [0019], [0027], Fig. 8; Tsutsui at Abstract, Introduction, Device Structure and Transistor Characteristics, Fig. 1, Fig. 3, Common Channel Dosage for Core and I/O Tr.

Additionally, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, identical conductivity type on an identical semiconductor substrate, a gate insulating film formed on a first active region in the semiconductor substrate and a gate electrode formed on the gate insulating film, an interface layer being in contact with the semiconductor substrate and a high dielectric constant insulating film formed on the interface layer, interface layers of different thicknesses, and interface layers made of silicon dioxide or silicon oxynitride films—to other references that relate to semiconductor device designs generally because all references teach designing transistors with particular technical specifications suitable different purposes in semiconductor devices, and it would have been a trivial exercise to consult the references that taught more specific semiconductor device designs to fill in less specific disclosures in other references. *See, e.g.*, Gilmer at Abstract; Chowdhury at Abstract; Torii at Abstract; Lin at Abstract, 1:29-32; Hsu at Abstract, 1:7-2:14; Iwamoto at Abstract; Suzuki at 1:12-19; Irino at Abstract, ¶ [0001]; Fujiwara at Abstract, ¶¶ [0001], [0013]-[0015]; Hori at Abstract, 1:16-19; Greene at Abstract, 1:7-10, 1:63-3:4; Luan at Abstract, ¶¶ [0002], [0014]-[0016]; Intel QX9650 at page 1; Chen at Abstract; Yu at Abstract, 1:27-31, 4:9-44; Wang at Abstract, 1:11-18; AAPA at Title, Abstract; Weste at Title, 5-7; Wolf at Title, Preface; Plummer at 7-12; Sze at Title, 431-433; ITRS at 1; Koyama at Title, Abstract; Mise at Title, Abstract; Onishi at Title, Abstract; Liaw at Abstract; Stahrenberg at Title, Abstract; Park at Abstract; Efavi at Introduction; Lu at Abstract, Introduction; Min at Title, Abstract; Tseng at Title, Abstract; Karve at Abstract; Tsutsui at Abstract, Introduction.

As another example, a POSITA would have been motivated to tune the gate electrode work function for individual transistors to control and keep the threshold voltage (Vth) in the desired range, a key parameter that directly impacts power consumption, switching speed, and overall

circuit functionality. To that end, a POSITA would have been motivated to combine any of the references with, for example but not limited to, Gilmer, Torii, Chowdhury, Hsu, Lin, Suzuki, Iwamoto, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, or Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve. It was well-known that as transistor dimensions scale down, conventional methods for threshold voltage adjustment become less effective and introduce variability, motivating use of gate electrode work function engineering to fine tune Vth of individual transistors. Techniques for tuning work function including changing the material in the metal gate electrode (e.g., selecting different metals with inherent work function values), incorporating cap layers that, e.g., that modify the effective work function through dipole interactions or interface dipole engineering, and adjusting the equivalent oxide thickness (EOT) of the gate dielectric, which can affect the degree of Fermi level pinning and thereby shift the apparent work function were well-known in the art demonstrating a POSITA would have had a reasonable likelihood of success in the combination and the combination results would have been predictable. The combination, and the selection of a particular work function engineering technique, would be a matter of routine engineering design choice, based on tradeoffs between, e.g., thermal budget, process integration, reliability, and material compatibility. Moreover, the methods to achieve the combination were known and routinely used. Each technique was well-documented in the literature and widely practiced in the semiconductor industry by the priority date of the ’779 patent. Their individual and combined effects on transistor performance, including threshold voltage modulation, interface quality improvement, and defect mitigation, were well documented. Published results demonstrated that these techniques could be reliably implemented across both

NMOS and PMOS devices, including in differentiated applications such as core and I/O transistors. Given this state of the art, a POSITA would have recognized these techniques as complementary and interchangeable, and would have reasonably expected that combining them would yield predictable, beneficial results. The goal—adjusting threshold voltage to meet design and performance specifications—was a routine engineering objective, and the methods available were proven and readily adaptable.

A POSITA would also have been motivated to implement cap layers in the gate stacks of transistors to modulate the effective work function and control threshold voltage of transistors. To that end, a POSITA would have been motivated to combine any of the references with, for example but not limited to, Gilmer, Torii, Chowdhury, Hsu, Lin, Suzuki, Iwamoto, Irino, Fujiwara, Hori, Greene, Luan, Intel QX9650, Chen, Yu, Wang, AAPA, or Min, Stahrenberg, Onishi, Tseng, Koyama, Mise, Liaw, Ranade-Thesis, Wong-Thesis, Tsutsui, Park, Weste, Burham-Thesis, Houssa, Lu, ITRS, Alshareef, Sze, Wolf, Plummer, Bai, Efavi, Wang-Paper, and Karve. Specifically, a POSITA can independently tune the threshold voltages of devices, allowing for greater flexibility in CMOS design, particularly as device scaling reduces the tolerance for doping-based work function adjustments. A POSITA would have further been motivated to implement cap layers, particularly in transistors having metal gate electrodes and high-k gate dielectrics to reduce interface defects that otherwise degrade carrier mobility and increase threshold voltage variability and improve compatibility at the interface between the gate electrode and the gate dielectric, helping to mitigate chemical or structural incompatibilities that can arise during thermal processing. The ’779 patent further acknowledges the motivation to use cap layers in this manner in its admitted prior art. (’779 patent, 2:24-27.)

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular semiconductor device with the teachings regarding other materials, components, and configurations used in other semiconductor devices for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques for designing semiconductor devices existed. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: fabricating a semiconductor device with MIS transistors. This motivation would conclude in a combination of prior art elements (*e.g.*, identical conductivity type on an identical semiconductor substrate, a gate insulating film formed on a first active region in the semiconductor substrate and a gate electrode formed on the gate insulating film, an interface layer being in contact with the semiconductor substrate and a high dielectric constant insulating film formed on the interface layer, interface layers of different thicknesses, and interface layers made of silicon dioxide or silicon oxynitride films) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of

semiconductor device fabrication were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

Additional obviousness combinations of the references identified here are possible, and TSMC may rely on such combination(s) in this litigation. In particular, TSMC is currently unaware of AICP's allegations with respect to the level of skill in the art and the qualifications of a POSITA. TSMC is also unaware of the extent, if any, to which AICP may contend that limitations of the claims at issue are not disclosed in the prior art identified by TSMC as anticipatory, and the extent to which AICP will contend that elements not disclosed in the asserted patent specifications would have been known to a POSITA. And TSMC does not yet know how the Court will construe terms in the asserted claim. TSMC is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. TSMC reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case No. IPR2025-00832 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the '779 patent.

g. The '425 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant's Admitted Prior Art, and/or the additional prior art references discussed below, and in Exhibits 425-01 through 425-21 would have rendered obvious one or more Asserted Claims of the '425 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a

reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits 425-01 through 425-21, TSMC contends that all asserted claims are rendered obvious by Intel_425_Product, TSMC_425_Product, James 90nm article, Wu922, Cheng817, Saito825, Ogura844, Cheng810, Lee870, Baik820, Wang906, Bohr683, Chen729, Doris784, Hsu823, Ke984, Yamasaki170, Hatada776, Chen179, and Shimamune398 alone or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exh. No.	**Primary Reference**	**In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:**
425-01	Intel_425_Product	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article,

[20] To the extent any reference is cited in Exhibits 425-01 through 425-21, but not referenced here, any omission was unintentional and TSMC intends to rely on its identification of any such combinations in Exhibits 425-01 through 425-21.

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:
		Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-02	TSMC_425_Product	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-03	Baik820	One or more of Alvarez069, Bai article, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-04	Bohr683	One or more of Alvarez069, Bai article, Baik820, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:
		Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-05	Chen179	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-06	Chen729	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-07	Cheng810	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:
		Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-08	Cheng817	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-09	Doris784	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-10	Hatada776	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:
		presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-11	Hsu823	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-12	James 90nm article	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-13	Ke984	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:
		Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-14	Lee870	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-15	Ogura844	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-16	Saito825	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation,

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:
		Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-17	Shimamune398	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yamasaki170, Yasutake article
425-18	Wang906	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wu922, Yamasaki170, Yasutake article
425-19	Wu922	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan

Primary Exh. No.	Primary Reference	In Combination With One or More of the Following (As Described in Exhibits 425-01 through 425-21 and Herein)[20]:
		article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Yamasaki170, Yasutake article
425-20	Yamasaki170	One or more of Alvarez069, Bai article, Baik820, Bohr683, Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Chuang243, Doris784, Fischer208, Fukutome203, Fujimoto807, Hatada776, Hsu823, Intel_425_Product, James 65/45 article, James 90nm article, Jung104, Kavalieros729, Ke984, Komoda article, Koutny207, Kwon360, Lee870, Liu article, Maeda845, Mistry2007 article, Mistry2007 presentation, Miyashita476, Murthy482, Murthy556, Natarajan article, Ogura844, Saito825, Shifren983, Shimamune398, Thompson Apr2004 article, Thompson Nov2004 article, TSMC_425_Product, Tyagi article, Wang906, Wu922, Yasutake article

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’425 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’425 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits 425-01 through 425-21 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits 425-01 through 425-21, including for the reasons described below. A POSITA at the time of filing of the asserted patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’425 patent relates to strain-engineered Semiconductor Field Effect Transistors (“MISFETs”).[21] The asserted claims recite elements that were conventional in strain-engineered MISFETs well before the earliest available priority date listed on the face of the ’425 patent (January 7, 2010). A first MIS transistor with a first gate insulating film formed on a first active region in a semiconductor substrate, *see, e.g.*, ’425 patent at 8:42-37, 14:24-42, 17:33-67, FIGS. 1A-7B, was well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:1-6, 2:61-62, FIGS. 8A-10C; Murthy131, at 2:40-44, FIGS. 1-6 (incorporated by reference in the ’425 patent); Ghani article, at 978, Figs. 1, 4, 5 (same); Luo article, at 489-90, Figs. 1, 2, 8, 14 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-38, 4-42 through 4-52, 4-56, 5-10 through 5-14, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.10, 4.5.11, 4.6.1 through 4.6.7, 4.6.11, 5.3.3 through 5.3.7, 6.2.4 through 6.2.6 (describing Intel_425_Product); Stratix_IV_Report, 3-66, 3-68; James TSMC article; Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Baik820, ¶ [0004], ¶ [0011], ¶ [0013], ¶¶ [0024]-[0026], ¶ [0033], FIGS. 1A-1I, 4A-5E; Bohr683, at Abstract, ¶ [0002], ¶¶ [0004]-[0031], ¶ [0033], ¶ [0036], ¶¶ [0038]-[0041], ¶¶ [0043]-[0046], ¶ [0050], FIGS. 1-8; Chen179, at Abstract, ¶¶ [0002]-[0004], ¶¶ [0006]-[0007], ¶ [0016], ¶¶ [0018]-[0021], FIGS. 1A-1D; Chen729, ¶ [0001], ¶ [0012], ¶ [0014], ¶¶ [0018]-[0021], ¶ [0023], FIGS. 1-6; Cheng810, ¶¶ [0015]-[0016], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0056]-[0058], ¶¶ [0072]-[0073], FIGS. 4j, 5i; Doris784, ¶ [0019], ¶ [0036], FIGS. 14, 15; Hatada776, ¶ [0089], ¶ [0090], ¶ [0135], ¶ [0147], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶[0028], FIGS. 7B, 11A, 13; James 90nm Article, at 73-74, 76, FIG. 6; Ke984, ¶ [0016], FIG. 10; Lee870, ¶ [0044], FIGS.

[21] MISFETs are also referred to sometimes as Metal Oxide Semiconductor Field Effect Transistors (“MOSFETs”).

4, 5; Ogura844, ¶ [0021], ¶¶ [0058]-[0061]; FIGS. 4A-4B, 1I, 1M; Saito825, ¶ [0051], ¶ [0124], FIGS. 12, 21; Shimamune398, at Abstract, ¶ [0028], ¶ [0033], ¶ [0039], ¶ [0074], ¶ [0111], ¶ [0152], FIGS. 3, 8E; Wang906, ¶ [0024], FIG. 16; Wu922, ¶ [0017], ¶ [0038], FIGS. 7, 14; Yamasaki170, ¶ [0056], ¶ [0058], FIGS. 31A-31B; Sun article, at 16, 19-20; Quirk & Serda, at FIGS. 12.1, 12.4-12.5, 12.9-12.10, 12.12-12.14; Morin article, at 355-356, 358, 366-367, Fig. 1; Bohr article, Figs. 1, 2; ITRS_2007_PIDS, at 1, 2, 4, 6-8, 15-16, 25-27, Tbls. PIDS1a, PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, PIDS3d, Figs. PIDS2, PIDS3, PIDS4, PIDS5; ITRS_2007_FEP, at 2, 5, 10, 12-13, 16, 19-20, 26-32, 35, 37-38, Tbls. FEP4a, FEP4b, Figs. FEP1, FEP4, FEP5; Alvarez069, ¶ [0020], ¶ [0039], ¶ [0040], ¶ [0063], FIGS. 5-11; Chidambarrao205, ¶ [0041]-[0046], FIG. 4F; Chuang243, 3:55-64, 5:1-14, 6:10-32, FIG. 1I; Fischer208, ¶ [0006], ¶ [0031], ¶ [0036], ¶ [0040], ¶ [0041], ¶ [0047], ¶ [0048], ¶ [0058], ¶ [0078], ¶ [0082], ¶ [0090], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 7A-7C, 8; Fujimoto807, Abstract, ¶ [0081], ¶ [0058], FIGS. 1A-10D; Fukutome203, Abstract, ¶ [0013], ¶ [0015], ¶ [0018], ¶ [0028], ¶ [0029], ¶ [0079], ¶ [0086], ¶ [0148], ¶ [0156], ¶ [0159], ¶ [0163], ¶ [0173], ¶ [0184], ¶ [0209], ¶ [0211], ¶ [0215], ¶ [0226], ¶ [0229], ¶ [0233], ¶ [0239], ¶ [0239], FIGS. 5A-14B, 16. Jung104, ¶¶ [0002]-[0016], ¶¶ [0035]-[0037], ¶ [0079], FIGS. 1A-1C. Kavalieros729, Abstract, ¶¶ [0032]-[0036], ¶ [0045], FIG. 13; Koutny207, ¶¶ [0069]-[0074], FIG. 6A; Kwon360, ¶ [0017], Fig. 3(c), Fig. 4; Maeda455, ¶¶ [0003]-[0009], ¶¶ [0011]-[0020], ¶ [0062], ¶¶ [0078]-[0087], ¶ [0092], ¶ [0097], ¶¶ [0102]-[0110], FIGS. 9, 10, 21-27; Mistry2007 article, 247-250, Figs. 2, 5, 6; Mistry2007 Presentation, 4, 5, 14, 15a-15j, 16-19, 21-35; Miyashita476, ¶ [0020], FIGS. 1D-5I, 5H, 5I; Murthy482, 3:47-4:3, FIG. 4c; Murthy556, Abstract, 1:30-64, 2:4-5, 3:16-5:15, 5:46-6:21, 7:11-52, FIGS. 1-15; Natarajan article, 1-3, Fig. 2; Shifren983, ¶ [0014].FIGS. 6, 7.

A first MIS transistor with a first gate electrode formed on the first gate insulating film, *see, e.g.*, ’425 patent at 9:15-37, 11:49-51, 13:20-39, 14:24-42, 17:33-67, 18:54-56, FIGS. 1A-7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:1-6, 2:61-62, FIGS. 8A-10C; Murthy131, at 2:45-60, 3:1-4:8, FIGS. 1-6 (incorporated by reference in the ’425 patent); Ghani article, at 978, Figs. 1, 4, 5 (same); Luo article, at 489-90, Figs. 1, 2, 8, 14 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-38 through 4-40, 4-42 through 4-52, 4-56, 5-10 through 5-14, 6-11, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.10 through 4.5.12, 4.6.1 through 4.6.7, 4.6.11, 5.3.3 through 5.3.7, 6.2.1, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Stratix_IV_Report, 3-65, 3-68; James TSMC article; Baik820, ¶ [0006], ¶ [0024], ¶ [0035], ¶ [0037], ¶ [0039], ¶ [0052], ¶ [0054], ¶ [0056], FIGS. 1A-1I, 4A-5E; Bohr683, ¶ [0004], ¶ [0008], ¶ [0012], ¶¶ [0014]-[0017], ¶¶ [0019]-[0020], ¶¶ [0022]-[0023], ¶¶ [0030]-[0032], ¶¶ [0036]-[0037], ¶ [0040], ¶ [0043], ¶ [0045], ¶ [0047], FIGS. 1-8; Chen179, ¶ [0002], ¶ [0007], ¶ [0020], ¶ [0022], ¶ [0024], FIGS. 1A-1D; Chen729, ¶ [0001], ¶¶ [0012]-[0013], ¶ [0018], ¶ [0023], FIGS. 1-6; Cheng810, ¶ [0015], ¶ [0017], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0056]-[0058], ¶¶ [0072]-[0073], FIGS. 4j, 5i; Doris784, ¶ [0019], ¶ [0036], FIGS. 14, 15; Hatada776, Abstract, ¶ [0027], ¶ [0035], ¶¶ [0038]-[0040], ¶ [0044], ¶¶[0046]-[0048], ¶¶ [0053]-[0056], ¶ [0058], ¶ [0061], ¶ [0062], ¶¶ [0064]-[0067], ¶ [0089], ¶ [0091], ¶ [0094], ¶¶ [0124]-[0125], ¶¶ [0130]-[0133], ¶ [0135], ¶¶ [0138]-[0143], ¶¶ [0147]-[0153], ¶¶ [0158]-[0159], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶[0028], FIGS. 7B, 11A, 13; James 90nm Article, at 73-74, 76, FIG. 6; Ke984, ¶ [0016], FIG. 10; Lee870, ¶ [0044], FIGS. 4, 5; ; Ogura844, ¶ [0021], ¶¶ [0058]-[0061]; FIGS. 4A-4B, 1I, 1M; Saito825, ¶

[0051], ¶ [0066], ¶ [0093], ¶ [0124], FIGS. 12, 21; Shimamune398, at Abstract, ¶ [0028], ¶ [0033], ¶ [0039], ¶ [0075], ¶ [0111], ¶ [0152], FIGS. 3, 8E; Wang906, ¶ [0024], FIG. 16; Wu922, ¶ [0017], ¶ [0038], FIGS. 7, 14; Yamasaki170, ¶¶ [0056]-[0058], ¶¶ [0065]-[0066], FIGS. 31A-31B; Sun article, at 14, 19-20; Quirk & Serda, at 309-312, FIGS. 12.1, 12.4-12.5, 12.9-12.10, 12.12-12.14; Morin article, Figs. 1, 2, 6, 20; Bohr article, Figs. 1, 2; ITRS_2007_PIDS, at 1, 2, 4, 6-8, 15-16, 25-27, Tbls. PIDS1a, PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, PIDS3d, Figs. PIDS2, PIDS3, PIDS4, PIDS5; ITRS_2007_FEP, at 2, 3, 12-13, 16-17, 19-20, 26-38, Tbls. FEP1, FEP2a, FEP2b, FEP3a, FEP3b, FEP4a, FEP4b, Figs. FEP1, FEP4, FEP5; Alvarez069, ¶ [0020], ¶ [0039], ¶ [0040], ¶ [0063], FIGS. 5-9-11; Chidambarrao205, ¶ [0041], ¶¶ [0046]-[0050], FIG. 4F; Chuang243, 4:57-67, 5:1-14, 6:10-32, FIG. 1I; Fischer208, ¶ [0036], ¶ [0037], ¶ [0040], ¶¶ [0058]-[0066], ¶ [0070], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 7A-7C, 8; Fujimoto807, Abstract, ¶ [0022], ¶ [0023], ¶¶ [0027]-[0037], ¶ [0037], ¶¶ [0059]-[0068], ¶¶ [0081]-[0093], FIGS. 1A-10D; Fukutome203, Abstract, ¶ [0013], ¶ [0014], ¶ [0018], ¶ [0020], ¶ [0021], ¶ [0079], ¶ [0081], ¶¶ [0083]-[0087], ¶ [0091], ¶ [0094], ¶ [0103], ¶ [0122], ¶ [0125], ¶ [0129], ¶ [0134], ¶ [0139], ¶ [0142], ¶ [¶ [0157], ¶ [0158], ¶ [00169], ¶ [0172], ¶ [0180], ¶ [0181], ¶ [0185], ¶ [0186], ¶ [0195], ¶ [0196], ¶¶ [0218]-[0223], , FIGS. 5B-10, 11B-12D, 13C-17; Jung104, ¶¶ [0002]-[0016], ¶¶ [0035]-[0037], ¶ [0079], FIGS. 1A-1C; Kavalieros729, Abstract, ¶¶ [0037]-[0041] ¶ [0045], FIG. 13; Koutny207, ¶ [0017], ¶ [0084], ¶ [0101], FIG. 6A; Kwon360, ¶ [0017], ¶ [0019], ¶ [0020], Fig. 3(c), 4; Maeda455, ¶¶ [0003]-[0009], ¶¶ [0011]-[0020], ¶ [0062], ¶¶ [0078]-[0087], ¶ [0092], ¶ [0095], ¶ [0097], ¶ [0098], ¶¶ [0102]-[0110], FIGS. 9, 10, 21-27; Mistry2007 article, 247-250, Figs. 2, 5, 6; Mistry2007 Presentation, 4, 5, 7, 10, 14, 5a-15j, 16, 19; Miyashita476, ¶ [0025], ¶ [0027], ¶ [0033], ¶ [0038], ¶ [0046], ¶ [0048], ¶ [0051], ¶ [0052], ¶ [0058], ¶ [0059], ¶¶ [0069]-[0073], ¶ [0079], ¶ [0093], FIGS. 1E-5I; Murthy482, 3:47-4:3, FIG. 4c; Murthy556, Abstract, 1:30-64, 2:4-5,3:16-4:67, 5:63-

8:22, 9:45-10:11, 10:42-55, FIGS. 1-15; Natarajan article, 1-3, Fig. 2; Shifren983, ¶ [0014], FIGS. 6, 7; Yasutake article, 48 49, Figs. 1, 5, 9, 11.

A first MIS transistor with a first sidewall spacer formed on a side surface of the first gate electrode, *see, e.g.*, '425 patent at 10:17-40, 12:13-29, 14:24-42, 15:40-51, 18:44-53, 19:5-22, FIGS. 1B-7B, was also well-known before the '425 patent, *see, e.g.*, *id.* at 1:15-56, 2:14-22, 2:61-62, FIGS. 8B-10C; Murthy131, at 2:61-67, FIGS. 2-6 (incorporated by reference in the '425 patent); Ghani article, at 978, Figs. 1, 4, 5 (same); Luo article, at 489-90, Figs. 1, 2, 6, 8, 14 (same). The prior art is replete with teachings that confirm this admission in the '425 patent. *See, e.g.*, D920_Report, at 4-38 through 4-40, 4-42 through 4-52, 4-54 through 4-57, 5-10 through 5-14, 6-14 through 6-16, 8-2, Tbls. 4.6.1, 8.1.3, Figs. 4.5.10 through 4.5.12, 4.6.1 through 4.6.7, 4.6.9 through 4.6.11, 4.7.1, 5.3.3 through 5.3.7, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Stratix_IV_Report, 3-65, 3-68; James TSMC article; Baik820, ¶ [0026], ¶ [0042], FIGS. 1B-1I, 4A-5E; Bohr683, ¶ [0005], ¶ [0008], ¶ [0012], ¶¶ [0014]-[0017], ¶¶ [0019]-[0023], ¶¶ [0030]-[0032], ¶¶ [0036]-[0037], ¶ [0040], ¶ [0043], ¶ [0045], ¶ [0047], FIGS. 2-8; Chen179, ¶ [0002], ¶ [0004], ¶ [0007], ¶ [0020], ¶ [0022], ¶ [0024], FIGS. 1A-1D; Chen729, ¶ [0001], ¶ [0004], ¶¶ [0014]-[0016], ¶¶ [0018]-[0019], ¶¶ [0020]-[0022], FIGS. 1-6; Cheng810, ¶ [0019], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0061]-[0062], ¶¶ [0076]-[0077], FIGS. 4j, 5i; Doris784, ¶ [0019], ¶ [0036], ¶ [0038], ¶ [0050], FIGS. 14, 15; Hatada776, Abstract, ¶ [0027], ¶ [0035], ¶ [0039], ¶ [0047], ¶¶ [0091]-[0092], ¶ [0135], ¶ [0140], ¶ [0154], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶¶ [0030]-[0031], ¶ [0035], ¶ [0041], FIGS. 7B, 11A, 13; James 90nm Article, at 73-74, 76, FIG. 6; Ke984, ¶ [0018], FIG. 10; Lee870, ¶ [0044], FIGS. 4, 5; Ogura844, ¶ [0022], ¶¶ [0058]-[0061];

FIGS. 4A-4B, 1I, 1M; Saito825, ¶ [0051], ¶ [0070], ¶¶ [0095]-[0097], ¶ [0124], FIGS. 12, 21; Shimamune398, at Abstract, ¶ [0028], ¶¶ [0075]-[0076], ¶ [0112], ¶¶ [0121]-[0122], FIGS. 3, 8E; Wang906, ¶ [0039], FIG. 16; Wu922, ¶ [0017]-[0018], ¶ [0024], ¶ [0028], ¶¶ [0038]-[0039], ¶ [0043], FIGS. 7, 14; Yamasaki170, ¶ [0065], FIGS. 31A-31B; Quirk & Serda, at 311-312, FIGS. 12.1, 12.4-12.5, 12.9-12.10, 12.12-12.14; Morin article, Figs. 1, 2, 20; Bohr article, Fig. 2; ITRS_2007_FEP, at 20, 27, 30, 34, 38, Tbls. FEP4a, FEP4b, Fig. FEP1; Alvarez069, ¶ [0021], ¶ [0040], ¶ [0041], ¶ [0063], FIGS. 5-11; Chidambarrao205, ¶ [0041], ¶ [0050], ¶ [0051], ¶ [0054], ¶ [0055], FIG. 4F; Chuang243, 2:27-31, 3:10-12, 5:15-6:32, FIG. 1I; See also Fischer208, ¶ [0036], ¶ [0049], ¶ [0060], ¶ [0066], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5C, 7A-7C, 8; Fujimoto807, Abstract, ¶¶ [0022]-[0025], ¶ [0031], ¶ [0032], ¶ [0034], ¶ [0035], ¶ [0037], ¶ [0044], ¶¶ [0058]-[0067], ¶ [0073], ¶¶ [0081]-[0093], FIGS. 1B-4C, 5B-7C, 8B-10D; Fukutome203, ¶ [0018], ¶ [0036], ¶ [0084], ¶ [0086], ¶ [0087], ¶ [0094], ¶ [0095], ¶ [0113], ¶ [0114], ¶ [0134], ¶ [0136], ¶ [0137], ¶ [0169], ¶ [0180], FIGS. 5C-10, 11C-12D, 13C-14B, 16; Jung104, ¶¶ [0002]-[0016], ¶¶ [0035]-[0037], ¶ [0079], FIGS. 1A-1C; Kavalieros729, ¶ [0023], ¶ [0028], FIG. 13; Koutny207, ¶ [0018], ¶ [0019], ¶ [0020], ¶ [0085], ¶ [0089], ¶ [0099], FIGS. 3I, 3J, 6A; Kwon360, ¶ [0017], Fig. 3(c); Liu article, 836-839, Fig. 1; Maeda455, ¶¶ [0003]-[0009], ¶¶ [0011]-[0020], ¶ [0062], ¶¶ [0078]-[0087], ¶ [0092], ¶ [0097], ¶¶ [0102]-[0110], FIGS. 9, 10, 21-27; Mistry2007 Presentation, 15a-15j, 16, 19; Miyashita476, ¶ [0027], ¶ [0028], ¶¶ [0038]-[0040], ¶ [0043], ¶ [0046], ¶ [0048], ¶ [0052], ¶ [0054], FIGS. 1J-5I; Murthy482, 3:47-4:3, Fig. 4c; Murthy556, Abstract, 1:30-64, 2:6-23, 3:16-54, 4:34-67, 6:22-7:16, 7:53-8:22, 9:10-10:55, FIGS. 1, 2, 4-15; Natarajan article, 1-3, Fig. 2; Shifren983, ¶ [0014], FIGS 6, 7; Thompson Apr2004 article, 191-193, Fig. 1; Thompson Nov2004 article, 1790-1797, Fig. 2, 4-6; Yasutake article, 48 49, Figs. 1, 5, 9, 11.

A first MIS transistor with a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, *see, e.g.*, '425 patent at 4:33-37, 10:65-11:48, 12:35-54, 13:20-39, 14:24-51, 15:55-62, 16:12-25, 16:63-17:33, FIGS. 2B-7B, was also well-known before the '425 patent, *see, e.g.*, *id.* at 1:15-56, 2:28-36, 2:61-62, FIGS. 8C-10C; Murthy131, at 3:28-4:44, FIGS. 5, 6 (incorporated by reference in the '425 patent); Ghani article, at 978, Figs. 1, 4 (same); Luo article, at 489-90, Figs. 1, 2, 6, 8, 14 (same). The prior art is replete with teachings that confirm this admission in the '425 patent, including under Plaintiff's apparent understanding of the claims. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-39 through 4-40, 4-42, 4-46 through 4-48, 4-53, 4-56, 4-60 through 4-61, 5-12 through 5-13, 6-12 through 6-16, Tbls. 1.6.1, 4.6.1, Figs. 4.5.11, 4.5.12, 4.6.3, 4.6.4, 4.6.8, 4.6.11, 4.8.1, 5.3.5, 5.3.6, 6.2.2 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 65/45 article, at 79-80, Fig. 6 (describing Intel_E5410); Stratix_IV_Report, 3-65, 3-68; James TSMC article; Cheng810 ¶ [0014], ¶ [0018], ¶¶ [0020]-[0021], ¶ [0030], FIGS. 1D-1F; Doris784, ¶ [0029], ¶ [0031], ¶ [0038], ¶ [0051], FIGS. 14, 15; Lee870, ¶ [0037], ¶ [0044], FIGS. 4, 5; Saito825, ¶ [0051], ¶ [0055], [0078]-[0079], ¶¶ [0099]-[0101], ¶¶ [0116]-[0119], ¶ [0124], FIGS. 12, 21; D920_Report, at 1-6, 1-8, 4-39 through 4-40, 4-42, 4-46 through 4-48, 4-53, 4-56, 4-60 through 4-61, 5-12 through 5-13, 6-12 through 6-16, Tbls. 1.6.1, 4.6.1, Figs. 4.5.11, 4.5.12, 4.6.3, 4.6.4, 4.6.8, 4.6.11, 4.8.1, 5.3.5, 5.3.6, 6.2.2 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); James TSMC article, at 8-9, Fig. 17 (describing

TSMC_425_Product); Mistry2007 article, at 248-49, Figs. 5, 6; Mistry2007 presentation, at 14, 15a-15j, 16, 19, 35; Baik820, at Title, Abstract, ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0027]-[0032], ¶¶ [0034]-[0040], ¶¶ [0042]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶ [0056], ¶ [0058], FIGS. 1C-1I, 4A-5F; Bohr683, at Title, Abstract, ¶¶ [0006]-[0007], ¶ [0011], ¶¶ [0022]-[0036], ¶ [0039], ¶ [0041], ¶¶ [0043]-[0046], ¶ [0050], FIGS. 3-8; Bohr article, at 1-3, Figs. 1, 2; Chen179, at Title, Abstract, ¶ [0001], ¶¶ [0002]-[0005], ¶¶ [0006]-[0007], ¶ [0013], ¶¶ [0016]- [0017], ¶ [0019], ¶¶ [0021]-[0023], FIGS. 1A-1D; Chen729, at Abstract, ¶ [0001], ¶ [0002], ¶ [0004], ¶ [0006], ¶ [0009], ¶ [0014], ¶¶ [0018]-[0022], FIGS. 1-6; Cheng817, ¶¶ [0002]-[0003], ¶¶ [0022]-[0023], ¶ [0033]-[0037], ¶ [0044], ¶ [0046], ¶ [0052], ¶ [0056], ¶ [0060], ¶¶ [0063]-[0065], ¶¶ [0068]-[0069], ¶ [0072], ¶ [0075], ¶¶ [0079]-[0080], ¶ [0083], ¶¶ [0093]-[0094], ¶ [0101], FIGS. 1, 2, 3e-3n, 4d-4j, 5d-5i, 6d-6i, 7; Chidambarrao205, at Abstract, ¶¶ [0003]-[0004], ¶¶ [0053]-[0061], FIGS. 1-3, 4C-4F; Chuang243, at 2:32-34, 3:13-15, 5:28-6:23, FIGS. 1H-1I; Fischer208, ¶¶ [0004]-[0007], ¶ [0014], ¶ [0015], ¶¶ [0022]-[0024], ¶¶ [0030]-[0034], ¶ [0037], ¶ [0040], ¶¶ [0046]-[0048], ¶¶ [0060]-[0066], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5C, 7A-7C, 8; Fujimoto807, at Abstract, ¶¶ [0013]-[0018], ¶¶ [0064]-[0074], ¶¶ [0087]-[0092], FIGS. 2C-4C, 6C-7C, 9D-10D; Fukutome203, at Abstract, ¶¶ [0004]-[0019], ¶¶ [0054]-[0055], ¶ [0074], ¶¶ [0085]-[0104], ¶¶ [0110]-[0111], ¶ [0115], ¶¶ [0121]-[0126], ¶¶ [0138]-[0146], ¶¶ [0157]-[0162], ¶¶ [0168]-[0177], ¶¶ [0185]-[0191], ¶¶ [0199]-[0201], ¶ [0206], ¶ [0240], ¶¶ [0248]-[0249], FIGS. 5D-5G, 8A-8C, 9C-9D, 11D-11E, 12C-12D, 13D-13E, 14A-14B, 16; Hatada776, at Abstract, ¶¶ [0004]-[0019], ¶ [0027], ¶ [0035], ¶ [0038], ¶¶ [0045]-[0046], ¶ [0050], ¶¶ [0057]-[0058], ¶ [0061], ¶¶ [0069]-[0070], ¶ [0089], ¶ [0094], ¶¶ [0097]-[0113], ¶¶ [0118]-[0121], ¶¶ [0128]-[0133], ¶¶ [0137]-[0138], ¶ [0141], ¶ [0145], ¶ [0150], ¶¶ [0156]-[0157], ¶ [0172], FIGS. 1, 2C-3, 4E-4F, 5E-5F, 6G-6I, 7F-8; Hsu823, ¶ [0002],

¶¶ [0028]-[0029], ¶¶ [0032]-[0035], ¶¶ [0038]-[0039], FIGS. 7A, 7B, 11A, 13; Maeda455, ¶¶ [0002]-[0005], ¶ [0018], ¶ [0029], ¶ [0042], ¶ [0048], ¶ [0102], ¶¶ [0105]-[0109], FIGS. 23-27; Miyashita476, ¶¶ [0048]-[0051], ¶¶ [0058]-[0061], ¶¶ [0078]-[0079], FIGS. 1S-1Y, 3A-3D, 5A-5I; Murthy482, 1:41-2:15, 4:39-7:10, 8:6-9:63, FIGS. 2-8; Murthy556, at 4:34-67, 6:60-9:9, 9:58-11:30, FIGS. 2, 6-14; Kavalieros729, at Abstract, ¶¶ [0001]-[0002], ¶¶ [0024]-[0025], ¶ [0043], FIGS. 4-13; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶ [0006], ¶¶ [0016]-[0017], ¶¶ [0019]-[0021], ¶ [0023], ¶ [0026], ¶ [0032], FIG. 10; Kwon360, at Abstract, ¶¶ [0001]-[0009], ¶¶ [0015]-[0024], Figs. 1-4; Ogura844, at Abstract, ¶¶ [0004]-[0011], ¶¶ [0020]-[0031], ¶¶ [0053]-[0055], ¶¶[0058]-[0061], FIGS. 1E-1M, 3A-4B; Shifren983, at Abstract, ¶¶ [0002]-[0003], ¶ [0011], ¶¶ [0015]-[0020], ¶¶ [0024]-[0026], FIGS. 2-7; Shimamune398 at Abstract, ¶¶ [0004]-[0013], ¶¶ [0019]-[0025], ¶¶ [0029]-[0032], ¶¶ [0034]-[0038], ¶ [0040], ¶¶ [0043]-[0147], ¶¶ [0157]-[0164], FIGS. 1-7, 8C-10C, 12A-14C; Wang906, at Abstract, ¶¶ [0002]-[0008], ¶ [0011], ¶ [0013], ¶ [0017], ¶ [0027], ¶¶ [0029]-[0032], ¶ [0038], ¶¶ [0040]-[0042], FIGS. 7-16; Wu922, at Abstract, ¶ [0005], ¶ [0009], ¶¶ [0017]-[0018], ¶¶ [0020]-[0021], ¶ [0024], ¶ [0029], ¶ [0031], ¶¶ [0035]-[0036], ¶¶ [0039]-[0041], ¶[0043], ¶ [0048], ¶ [0050], ¶¶ [0054]-[0058], FIGS. 3-8, 11-15; Yamasaki170, at Abstract, ¶¶ [0002]-[0010], ¶ [0013], ¶ [0016], ¶¶ [0035]-[0036], ¶¶ [0040]-[0047], ¶ [0054], ¶¶ [0058]-[0062], ¶ [0064], ¶¶ [0066]-[0082], ¶¶ [0085]-[0089], ¶¶ [0091]-[0092], ¶ [0095], ¶¶ [0099]-[0100], FIGS. 2A, 6A-19, 23A-43; ITRS_2007_PIDS, at 16, 26, 27, 56, Tbl. PIDS1a, PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, Figs. PIDS5, PIDS10; ITRS_2007_FEP, at 1-3, 10-13, 16, 17, 19-20, 29, 33 n.1, 35, 58-59, Tbl. FEP1, Figs. FEP1-FEP5; James 90nm article, at 73-74, 76, Figs. 6, 7; Thompson Apr2004 article, at 191-93, Fig. 1; Thompson Nov2004 article, at 1790-96, Figs. 2-7, 10, 13; Sun article, at 1-4, 7-16, 21, Figs. 5-8, 11, 12; Yasutake article, at 48, Figs. 1, 5, 6, 9-11; Natarajan article, at 1, Fig. 2.

A first MIS transistor with a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, which causes a second stress opposite to the first stress, *see, e.g.*, ’425 patent at 4:33-37, 13:66-14:9, 14:24-42, 16:26-30, 18:61-67, 19:10-39, FIGS. 6B, 7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:57-62, 3:5-9, FIG. 10C; Ghani article, at 978, Figs. 5, 6 (incorporated by reference in the ’425 patent); Luo article, at 489, Figs. 1, 2, 14 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-7, 4-16 through 4-17, 4-36, 4-38 through 4-41, 4-43 through 4-48, 4-53 through 4-58, 5-9 through 5-13, 6-9 through 6-10, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.3.1, 8.2.1, Figs. 4.3.9, 4.3.10, 4.5.8, 4.5.10 through 4.5.13, 4.6.1 through 4.6.4, 4.6.8 through 4.6.11, 4.7.1, 4.7.2, 5.3.2 through 5.3.6, 6.1.10, 6.1.11, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Stratix_IV_Report, 3-65, 3-67, 3-68, 3-71; James TSMC article; Baik820 ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0024]-[0033], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶¶ [0056]-[0058], FIGS. 1H-1I, 5E-5F; Bohr683, at Title, Abstract, ¶¶ [0006]-[0007], ¶ [0009], ¶ [0011], ¶¶ [0022]-[0036], ¶¶ [0038]-[0041], ¶¶ [0043]-[0048], ¶ [0050], FIGS. 6, 8; Chen179, at Title, Abstract, ¶¶ [0002]-[0004], ¶¶ [0006]-[0007], ¶ [0013], ¶ [0016], ¶¶ [0019]-[0025], FIGS. 1A-1D; Chen729 ¶ [0001], ¶ [0002], ¶ [0004], ¶ [0006], ¶ [0009], ¶ [0014], ¶¶ [0018]-[0023], FIGS. 1-6; Cheng810 Abstract, ¶¶ [0001]-[0002], ¶ [0009], ¶ [0013], ¶¶ [0024]-[0030], ¶ [0032], FIGS. 1D-1F; Cheng817, ¶¶ [0002]-[0003], ¶ [0030], ¶ [0070], ¶ [0084], FIGS. 4j, 5i; Doris784, ¶ [0005], ¶ [0008], ¶ [0013], ¶ [0029], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 14, 15; Hsu823, ¶ [0003], ¶¶ [0013]-[0014], ¶ [0024], ¶¶ [0036]-[0037], FIGS. 7B, 11A, 13;

James 90nm Article, at 73-74, 76, FIG. 6; Ke984, at Abstract, ¶ [0003], ¶¶ [0005]-[0006], ¶ [0030], FIG. 10; Lee870, at Abstract, ¶ [0002], ¶¶ [0016]-[0022], ¶¶ [0028]-[0030], ¶¶ [0037]-[0038], ¶¶ [0049]-[0051], ¶¶ [0054]-[0058], ¶¶ [0060]-[0064], ¶ [0067], ¶ [0069], FIGS. 4, 5; Ogura844, ¶ [0033], ¶¶[0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, ¶[0080], ¶ [0120], FIGS. 12, 21; Wu922, ¶ [0005], ¶ [0025], ¶ [0036], ¶ [0044], FIGS. 7, 14; Yamasaki170, ¶ [0013], ¶ [0016], ¶ [0067], FIGS. 31A-31B; Morin article, at Abstract, 355-358, 360-361, 364-367, Tbl. I, Figs. 1, 2, 8, 9, 15, 17, 20; Bohr article, at 1-3, Fig. 1; ITRS_2007_PIDS, at 27; ITRS_2007_FEP, at 1, 29-30, Figs. FEP4, FEP5; Alvarez069, Abstract, ¶ [0001], ¶¶ [0007]-[0009], ¶¶ [0020]-[0035], ¶ [0043], ¶¶ [0047]-[0055], ¶ [0057], ¶ [0058], ¶ [0059], ¶¶ [0061]-[0070], ¶ [0073]-[0074], ¶¶ [0080]-[0083], TBL 1, FIGS. 1, 4, 9-13; Chidambarrao205, ¶ [0003], ¶ [0061]; Chuang243, 1:47-50, 2:32-38, 3:13-18, 3:23-27, 5:28-38, 5:46-6:9, 6:15-23, 6:58-61, FIGS. 1H, 1I; Fischer208, ¶ [0034], ¶ [0038], ¶ [0067], ¶ [0099], FIGS. 1, 5F-5I, 7E, 8; Fukutome203, ¶ [0106], ¶ [0107], FIG. 5G; see generally Jung104; see also Jung104, Abstract, ¶ [0002], ¶ [0007], ¶¶ [0012]-[0014], ¶¶ [0016]-[0018], ¶ [0029], ¶ [0035], ¶ [0036], ¶¶ [0048]-[0063], ¶ [0079], ¶ [0083], ¶ [0084], ¶ [0089], ¶ [0090], ¶ [0092], ¶ [0094], ¶ [0099], ¶¶ [0102]-[0130], TBLS. IV-VI, FIGS. 1B, 1C, 2, 4A-14B; Kavalieros729, ¶ [0042], FIG. 13; Komoda article, 217-220, Tbl. 1, Figs. 2, 3, 17; Koutny207, ¶ [0028], ¶ [0036], ¶ [0107], ¶ [0108], FIG. 6A; Liu article, 836-839, Tbls. I, II, Figs. 1-7; Maeda455, ¶ [0006], ¶ [0016], ¶ [0020], ¶ [0027], ¶¶ [0034]-[0038], ¶¶ [0042]-[0045], ¶¶ [0049]-[0050], ¶¶ [0083]-[0091], ¶¶ [0102]-[0109], FIGS. 9, 10, 23-27; Mistry2007 article, 247-250, Figs. 5, 6; Mistry2007 Presentation, 16, 19; Miyashita476, ¶ [0080]; Thompson Apr2004 article, 191-193, Fig. 1; Thompson Nov2004 article, 1790-1797, Fig. 2, 3(c), 5(c), 12.

A first MIS transistor with an uppermost surface of the silicon compound layer being located higher than a surface of the semiconductor substrate located directly under the first gate

electrode, *see, e.g.*, ’425 patent at 3:38-46, 11:23-26, 13:20-39, 14:45-51, 15:55-62, 16:12-25, 16:63-17:3, FIGS. 2C-7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56; Ghani article, at 978, Figs. 1, 4 (incorporated by reference in the ’425 patent); Luo article, at 489-90, Figs. 1, 2, 8, 10 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent, including under Plaintiff’s apparent understanding of the claims. *See, e.g.*, D920_Report, at 4-39 through 4-40, 4-46 through 4-48, 4-56, 5-13, 6-13 through 6-16, Figs. 4.5.11, 4.5.12, 4.6.3, 4.6.4, 4.6.11, 5.3.6, 6.2.3 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 65/45 article, at 79-80, Fig. 6 (describing Intel_E5410); Baik820, at Title, Abstract, ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0027]-[0032], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶ [0056], ¶ [0058], FIGS. 1C-1I, 4A-5E; Bohr683, at Title, Abstract, ¶¶ [0007]-[0008], ¶ [0011], ¶¶ [0024]-[0026], ¶¶ [0033]-[0037], ¶ [0039], ¶¶ [0043]-[0044], ¶¶ [0046]-[0047], ¶ [0050], FIGS. 4-8; Chen179 ¶¶ [0002]-[0004], ¶ [0007], ¶¶ [0016]-[0025], FIGS. 1A-1D; Chen729 ¶ [0001], ¶¶ [0020]-[0022], FIGS. 1, 5, 6; Cheng810 ¶ [0021], ¶ [0030], FIGS. 1D-1F; Cheng817, at Abstract, ¶ [0022], ¶ [0029], ¶¶ [0033]-[0037], ¶ [0044], ¶ [0054], ¶ [0065], ¶ [0069], ¶ [0080], ¶¶ [0083]-[0084], FIGS. 4j, 5i; Doris784, ¶ [0029], ¶ [0031], ¶ [0038], ¶ [0051], FIGS. 14, 15; Hatada776, ¶ [0103], ¶ [0109], ¶ [0120], ¶ [0132], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶¶ [0032]-[0035], FIGS. 7B, 11A, 13; James 90nm Article, at 73-74, 76, FIG. 6; Ke984, ¶ [0019], ¶ [0021], ¶ [0023], ¶ [0026], FIGS. 5B, 10; Lee870, ¶ [0044], FIGS. 4, 5; Ogura844, ¶ [0011], ¶ [0026], ¶ [0028], ¶ [0031], ¶¶[0058]-[0061], FIGS. 1I, 1M, 4A-4B; Shimamune398, at Abstract, ¶ [0031], ¶ [0045], ¶ [0049], ¶ [0053], ¶ [0081], ¶ [0125], ¶¶ [0127]-[0129], FIGS. 3, 8E; Wang906, ¶ [0031], ¶ [0040], FIG. 16; Wu922, ¶ [0017], ¶ [0021], ¶ [0024], ¶ [0031], ¶ [0036], ¶ [0041], ¶ [0043], ¶ [0050], ¶ [0055], FIGS. 7, 8, 14, 15;

Yamasaki170, at Abstract, ¶ [0013], ¶ [0016], ¶¶ [0053]-[0054], ¶¶ [0058]-[0062], ¶ [0064], ¶¶ [0066]-[0068], FIGS. 31A-31B; Bohr article, at 1-3, Figs. 1, 2; ITRS_2007_FEP, at 30, 32, Figs. FEP1, FEP4a, FEP4b, FEP5; Chuang243, 2:32-34, 2:39-56, 3:13-15, 5:28-6:9, 6:10-32, FIG. 1H, 1I; Fischer208, ¶¶ [0004]-[0007], ¶ [0014], ¶ [0015], ¶¶ [0022]-[0024], ¶¶ [0030]-[0034], ¶ [0037], ¶ [0040], ¶¶ [0046]-[0048], ¶¶ [0060]-[0066], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5C, 7A-7C, 8; Fujimoto807, Abstract, ¶¶ [0013]-[0018], ¶ [0021], ¶ [0022], ¶ [0025]-[0045], ¶¶ [0058]-[0075], ¶¶ [0080]-[0097], FIGS. 2C-4C, 6C-7C, 9D-10D; Fukutome203, Abstract, ¶¶ [0004]-[0019], ¶¶ [0054]-[0055], ¶ [0074], ¶ [0083], ¶¶ [0085]-[0104], ¶¶ [0109]-[0111], ¶ [0115], ¶¶ [0121]-[0126], ¶¶ [0137]-[0146], ¶¶ [0157]-[0162], ¶ [0164], ¶¶ [0168]-[0177], ¶¶ [0185]-[0191], ¶¶ [0199]-[0201], ¶ [0206], ¶ [0240], ¶¶ [0248]-[0249], FIGS. 5D-5G, 8A-8C, 9C-9D, 11D-11E, 12C-12D, 13D-14B, 16; Kavalieros729, Abstract, ¶ [0001], ¶ [0016], ¶ [0024], ¶ [0025], ¶ [0040], ¶ [0043], FIG. 13; Kwon360, Abstract, ¶ [0001], ¶¶ [0006]-[0009], ¶ [0015], ¶ [0018], ¶ [0022], ¶ [0024], Figs. 1, 3(c), 4; Mistry2007 article, 247-250, Figs. 5, 6; Mistry2007 Presentation, 7, 14, 15a-15j, 16-19, 21-35; Miyashita476, ¶ [0018], ¶ [0026], ¶ [0033], ¶¶ [0036]-[0038], ¶¶ [0043]-[0051], ¶¶ [0058]-[0062], ¶¶ [0071]-[0073], ¶¶ [0078]-[0083], ¶¶ [0090]-[0093], FIGS. 1U-1Y, 3A-3D, 5A-5I; Murthy482, 5:34-7:10, FIGS. 3, 4a-4c, 8; Murthy556, Abstract, 1:52-64, 2:15-17, 2:58-3:29, 3:55-4:67, 6:60-9:9, 9:58-11:30, FIGS. 2, 6-15; Natarajan article. 1-3, Fig. 2; Shifren983, Abstract, ¶¶ [0001]-[0003], ¶ [0011], ¶¶ [0015]-[0017], ¶ [0024], ¶ [0025], FIGS. 3-7; Thompson Apr2004, 191-193, Fig. 1; Thompson Nov2004 article, 1790-1797, Figs. 2-5; Yasutake article, 48 49, Figs. 1, 5, 6, 9-11.

A first MIS transistor with a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer, *see, e.g.*, ’425 patent at Abstract, 3:38-58, 4:33-37, 12:59-13:19, 14:43-15:5, 15:52-16:11, FIGS. 5A-7B, was also well-known before the ’425 patent.

The prior art is replete with teachings that confirm this, including under Plaintiff's apparent understanding of the claims. *See, e.g.*, D920_Report, at 4-39, 4-46, 4-53, 4-56, 5-13, 6-14 through 6-16, Figs. 4.5.11, 4.6.3, 4.6.8, 4.6.11, 5.3.6, 6.2.4 through 6.2.6 (describing Intel_425_Product);[22] Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 90nm article, at Fig. 6; Stratix_IV_Report, 3-65, 3-68; James TSMC article; Baik820, at Title, Abstract, ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0027]-[0032], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶ [0056], ¶ [0058], FIGS. 1C-1I, 4A-5E; Bohr683, at Abstract, ¶ [0005], ¶ [0007], ¶ [0011], ¶ [0017], ¶¶ [0021]-[0037], ¶¶ [0030]-[0031], ¶ [0040], ¶¶ [0043]-[0048], ¶ [0050], FIGS. 4-8; Chen179 ¶¶ [0003]-[0004], ¶ [0017], ¶¶ [0021]-[0022], FIGS. 1A-1D; Chen729 ¶[0001], ¶ [0004], ¶[0014]-[0016], ¶¶ [0018]-[0022], FIGS. 1-6; Cheng810 ¶¶ [0021]-[0022], ¶ [0025], ¶ [0030], ¶ [0032], FIGS. 1D-1F; Cheng817, ¶ [0061], ¶ [0063], ¶ [0069], ¶ [0078], ¶ [0083], FIGS. 4j, 5i; Doris784, ¶ [0021], ¶¶ [0024]-[0025], ¶ [0029], ¶ [0031], ¶¶ [0036]-[0038], ¶¶ [0042]-[0043], ¶¶ [0045]-[0046], ¶¶ [0048]-[0049], ¶ [0051], FIGS. 6, 9, 10, 14, 15; Hsu823, ¶ [0025], ¶ [0032], ¶¶ [0034]-[0035], FIGS. 7B, 11A, 13; Ke984, ¶¶ [0005]-[0006], ¶ [0023], ¶ [0026], FIG. 10; Lee870, at Abstract, ¶¶ [0016]-[0022], ¶¶ [0028]-[0029], ¶¶ [0037]-[0038], ¶ [0044], ¶¶ [0046]-[0053], ¶ [0058], ¶ [0064], ¶ [0067], FIGS. 4, 5; Ogura844, ¶ [0011], ¶¶ [0031]-[0032], ¶¶[0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, at Abstract, ¶¶ [0074]-[0076], ¶¶ [0078]-[0079], ¶¶ [0104]-[0105], ¶¶ [0107]-[0114], ¶¶ [0116]-[0119], ¶ [0124], FIGS. 12, 21; Kwon360, Abstract, ¶ [0007], ¶ [0008], ¶ [0009], ¶ [0014], ¶ [0015], ¶¶ [0022]-[0024], Fig. 3(c), 4; Alvarez069, Abstract, ¶¶ [0001]-[0008], ¶ [0009], ¶¶ [0013]-[0016], ¶ [0018], ¶ [0019], ¶¶ [0022]-[0032], ¶ [0037], ¶¶ [0042]-[0045], ¶¶ [0047]-

[22] Under Plaintiff's apparent interpretation of the claim language, any silicon oxide film under the stress insulating film would appear to qualify as a "stress-relief film." *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 21. Although TSMC disagrees with such a broad proposition, Intel_425_Product appears to include such a layer.

[0050], ¶¶ [0052]-[0061], ¶¶ [0063]-[00810], TBL. 1, FIGS. 1-4, 9-13; Koutny207, ¶ [0036], ¶ [0088]-[0090], ¶ [0106], ¶ [0107], ¶ [0108], FIG. 6A.

A first MIS transistor with the first stress-relief film being formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, *see, e.g.*, '425 patent at Abstract, 12:59-13:19, 14:43-15:5, 15:52-16:11, FIGS. 5A-7B, was also well-known before the '425 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, D920_Report, at 4-39, 4-46, 4-53, 4-56, 5-13, 6-14 through 6-16, Figs. 4.5.11, 4.6.3, 4.6.8, 4.6.11, 5.3.6, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 90nm article, at Fig. 6; Stratix_IV_Report, 3-68; James TSMC article; Baik820, at Title, Abstract, ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0026]-[0032], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶ [0056], ¶ [0058], FIGS. 1C-1I, 4A-5E; Bohr683 ¶¶ [0004]-[0005], ¶ [0008], ¶ [0012], ¶¶ [0014]-[0017], ¶¶ [0019]-[0023], ¶¶ [0030]-[0032], ¶¶ [0036]-[0037], ¶ [0040], ¶ [0043], ¶ [0045], ¶ [0047], FIGS. 1-8; Chen179 ¶¶ [0002]-[0003], ¶ [0007], ¶ [0017], ¶¶ [0020]-[0022], ¶ [0024], FIGS. 1A-1D; Chen729 ¶[0001], ¶ [0004], ¶[0012]-[0016], ¶¶ [0018]-[0023], FIGS. 1-6; Cheng810 ¶ [0022], ¶ [0025], ¶ [0030], ¶ [0032], FIGS. 1D-1F; Cheng817, ¶ [0061], ¶ [0063], ¶ [0078], FIGS. 4j, 5i; Doris784, ¶ [0021], ¶¶ [0024]-[0025], ¶¶ [0036]-[0037], ¶¶ [0042]-[0043], ¶¶ [0045]-[0046], ¶¶ [0048]-[0049], FIGS. 6, 9, 10, 14, 15; Hsu823, ¶ [0025], ¶ [0032], FIGS. 7B, 11A, 13; Ke984, ¶¶ [0005]-[0006], ¶ [0027], FIG. 10; Lee870, at Abstract, ¶¶ [0016]-[0022], ¶¶ [0028]-[0029], ¶¶ [0037]-[0038], ¶¶ [0046]-[0053], ¶ [0058], ¶ [0064], ¶ [0067], FIGS. 4, 5; Ogura844, ¶ [0032], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, at Abstract, ¶¶ [0074]-[0076], ¶¶ [0104]-[0105], ¶¶ [0107]-[0114], FIGS. 12, 21; Alvarez069, Abstract, ¶¶ [0001]-[0008], ¶ [0009], ¶¶ [0013]-[0016], ¶ [0018], ¶ [0019], ¶¶ [0022]-[0032], ¶ [0037], ¶¶ [0042]-[0045], ¶¶

[0047]-[0050], ¶¶ [0052]-[0061], ¶¶ [0063]-[00810], TBL. 1, FIGS. 1-4, 9-13; Koutny207, ¶ [0036], ¶ [0088]-[0090], ¶ [0106], ¶ [0107], ¶ [0108], FIG. 6A; Kwon360, Abstract, ¶ [0007], ¶ [0008], ¶ [0009], ¶ [0014], ¶ [0015], ¶¶ [0022]-[0024] , Fig. 3(c), 4.

A first MIS transistor with the first stress-relief film not being in direct contact with the side surface of the first gate electrode, *see, e.g.*, '425 patent at 12:59-13:19, 14:55-15:5, 15:52-65, FIGS. 5A-7B, was also well-known before the '425 patent. The prior art is replete with teachings that confirm this. *See, e.g.*, D920_Report, at 4-39, 4-46, 4-53, 4-56, 5-13, 6-14 through 6-16, Figs. 4.5.11, 4.6.3, 4.6.8, 4.6.11, 5.3.6, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 90nm article, at Fig. 6; Stratix_IV_Report, 3-68; James TSMC article; Baik820, at Title, Abstract, ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0027]-[0032], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶ [0056], ¶ [0058], FIGS. 1C-1I, 4A-5E; Bohr683 ¶ [0004], ¶ [0008], ¶ [0012], ¶¶ [0014]-[0017], ¶¶ [0019]-[0020], ¶¶ [0022]-[0023], ¶¶ [0030]-[0032], ¶¶ [0036]-[0037], ¶ [0040], ¶ [0043], ¶ [0045], ¶ [0047], FIGS. 1-8; Chen179 ¶ [0002], ¶ [0007], ¶ [0020], ¶ [0022], ¶ [0024], FIGS. 1A-1D; Chen729 ¶¶ [0012]-[0013], ¶ [0023], FIGS. 1-6; Cheng810 ¶ [0022], ¶ [0025], ¶ [0030], ¶ [0032], FIGS. 1D-1F; Cheng817, ¶ [0061], ¶ [0063], ¶ [0078], FIGS. 4j, 5i; Doris784, ¶ [0021], ¶¶ [0024]-[0025], ¶¶ [0036]-[0037], ¶¶ [0042]-[0043], ¶¶ [0045]-[0046], ¶¶ [0048]-[0049], FIGS. 6, 9, 10, 14, 15; Hsu823, ¶ [0025], ¶ [0032], FIGS. 7B, 11A, 13; Ke984, ¶¶ [0005]-[0006], ¶ [0027], FIG. 10; Lee870, at Abstract, ¶¶ [0016]-[0022], ¶¶ [0028]-[0029], ¶¶ [0037]-[0038], ¶¶ [0046]-[0053], ¶ [0058], ¶ [0064], ¶ [0067], FIGS. 4, 5; Ogura844, ¶ [0032], ¶¶[0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, at Abstract, ¶¶ [0074]-[0076], ¶¶ [0104]-[0105], ¶¶ [0107]-[0114], FIGS. 12, 21; Alvarez069, Abstract, ¶¶ [0001]-[0008], ¶ [0009], ¶¶ [0013]-[0016], ¶ [0018], ¶ [0019], ¶¶ [0022]-[0032], ¶ [0037], ¶¶ [0042]-

[0045], ¶¶ [0047]-[0050], ¶¶ [0052]-[0061], ¶¶ [0063]-[00810], TBL. 1, FIGS. 1-4, 9-13; Koutny207, ¶ [0036], ¶ [0088]-[0090], ¶ [0106], ¶ [0107], ¶ [0108], FIG. 6A; Kwon360, Abstract, ¶ [0007], ¶ [0008], ¶ [0009], ¶ [0014], ¶ [0015], ¶¶ [0022]-[0024] , Fig. 3(c), 4.

A first MIS transistor with a first silicide layer formed on the first gate electrode and a second silicide layer formed on the first source/drain region which includes the silicon compound layer, *see, e.g.*, '425 patent at 4:10-14, 13:20-39, 13:58-65, 14:24-42, 18:1-8, 18:54-60, FIGS. 6A-6B, 7B, was also well-known before the '425 patent, *see, e.g.*, *id.* at 1:15-56, 2:52-56, 2:61-62, FIGS. 10B, 10C; Ghani article, at 978, Figs. 1, 4 (incorporated by reference in the '425 patent); Luo article, at 489-90, Figs. 1, 2, 14 (same). The prior art is replete with teachings that confirm this admission in the '425 patent, including under Plaintiff's apparent understanding of the claims. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-38 through 4-40, 4-42 through 4-49, 4-53, 4-56, 5-10 through 5-13, 6-11, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.10 through 4.5.12, 4.5.11, 4.6.1 through 4.6.4, 4.6.8, 4.6.11, 5.3.3 through 5.3.6, 6.2.1, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); Stratix_IV_Report, 3-65, 3-68; James TSMC article; Chen729 ¶ [0001], ¶¶ [0012]-[0013], ¶¶ [0018]-[0024], FIGS. 1, 5, 6; Wu922, ¶ [0017], ¶ [0024], ¶ [0036], ¶ [0043], ¶ [0055], FIGS. 7, 14; Alvarez069 ¶¶ [0029]-[0032], ¶[0037], ¶¶ [0044]-[0046], ¶¶ [0063]-[0064], ¶ [0068], ¶ [0073], FIGS. 3, 4, 8-10; Baik820, ¶ [0008], ¶¶ [0028]-[0032], ¶¶ [0038]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0055]-[0058], FIGS. 1H-1I, 5E-5F; Bohr683, at Title, Abstract, ¶ [0004], ¶¶ [0007]-[0008], ¶¶ [0011]-[0012], ¶¶ [0014]-[0017], ¶¶ [0019]-[0020], ¶¶ [0022]-[0038], ¶ [0040], ¶¶ [0043]-[0048], ¶ [0050], FIGS. 1-8; Chen179, ¶¶ [0002]-[0004], ¶ [0007]-[0011], ¶¶ [0016]-[0017], ¶¶ [0020]-[0025], ¶¶ [0027]-[0028], ¶¶ [0031]-[0034], ¶¶ [0039]-[0040], FIGS. 1A-2G, 3D-3E; Cheng810 ¶¶ [0003]-[0004], ¶ [0017],

¶ [0021], ¶¶ [0029]-[0031], FIGS. 1A-1F; Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7; Doris784 ¶ [0029], ¶ [0031], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 1, 2, 14, 15; Fujimoto807 ¶ [0017], ¶ [0031], ¶ [0068], ¶ [0074], ¶ [0091], FIGS. 3C, 4B-4C, 7C, 10D; Fukutome203 ¶¶ [0103]-[0104], ¶ [0107], ¶¶ [0125]-[0126], ¶ [0130], FIGS. 5F-5G, 8C; Hatada776 ¶ [0109], ¶¶ [0120]-[0121], ¶ [0132], ¶ [0171], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823 ¶¶ [0034]-[0035], ¶¶ [0040]-[0041], FIGS. 8-13; Ke984, at Title, ¶ [0023], ¶ [0026], ¶¶ [0028]-[0029], FIGS. 7-10; Kwon360, at Abstract, ¶¶ [0001]-[0003], ¶¶ [0006]-[0009], ¶ [0011], ¶¶ [0014]-[0016], ¶ [0019], ¶¶ [0022]-[0024], Figs. 1, 2(e), 3(c), 4; Lee870 ¶ [0037], ¶¶ [0044]-[0045], FIGS. 1-6; Maeda455 ¶¶ [0005]-[0006], ¶ [0017], ¶ [0028], ¶ [0039], ¶ [0046], ¶ [0079], ¶ [0083], ¶ [0087], ¶ [0095], ¶¶ [0097]-[0101], ¶ [0107], ¶ [0110], FIGS. 1, 6-13, 16-20, 25-32; Miyashita476 ¶ [0079], FIGS. 5A-5H; Murthy482, at Abstract, 2:39-41, 2:66-3:13, 4:32-38, 7:11-9:63, FIGS. 4a-4c, 5-8; Murthy556, at 2:31-33, 2:37-41, 3:30-46, 8:52-55, 9:38-43, 9:58-11:15, FIGS. 2, 11-15; Ogura844, at Abstract, ¶ [0009], ¶ [0011], ¶ [0031], ¶ [0038], ¶¶ [0054]-[0055], ¶¶ [0058]-[0061], FIGS. 1G-1M, 3A-4B; Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0116]-[0120], ¶¶ [0122]-[0124], FIGS. 3, 8-12, 20-21; Shifren983, at Abstract, ¶ [0002], ¶ [0009], ¶ [0011], ¶ [0019], ¶¶ [0024]-[0026], FIGS. 6, 7; Shimamune398 ¶ [0020], ¶¶ [0024]-[0025], ¶ [0053], ¶ [0081], ¶ [0088], ¶ [0120], ¶ [0125], ¶¶ [0128]-[0130], ¶ [0143], ¶ [01], FIGS. 2, 3, 8E; Wang906 ¶ [0024], ¶ [0040], FIGS. 16; Yamasaki170 ¶ [0008], ¶¶ [0040]-[0041], ¶¶ [0046]-[0047], ¶¶ [0050]-[0051], ¶¶ [0066]-[0068], ¶¶ [0073]-[0074], ¶¶ [0077]-[0079], ¶ [0082], ¶ [0097], FIGS. 12A-12B, 30A-31B, 39A-40B, 41A-42B; ITRS_2007_FEP, at 1, 4, 9, 16, 21, 22, 25, 27-30, 34, Figs. FEP1; ITRS_2007_PIDS, at 16, 26; James 90nm article, at 73-74, 76, Figs. 5, 6; D920_Report, at 1-6, 1-8, 4-38 through 4-40, 4-42

through 4-49, 4-53, 4-56, 5-10 through 5-13, 6-11, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.10 through 4.5.12, 4.5.11, 4.6.1 through 4.6.4, 4.6.8, 4.6.11, 5.3.3 through 5.3.6, 6.2.1, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); Tyagi article, at 245, Figs. 1, 2 (same); James TSMC article, at 8, Fig. 17 (describing TSMC_425_Product); Quirk & Serda, at 303, 308, 309-12, 321-22, 331, Tbl. 12.4, Figs. 12.9 through 12.13; Morin article, Fig. 1.

A first MIS transistor with the first stress-relief film being formed on a side surface of the silicon compound layer, *see, e.g.*, '425 patent at 12:59-13:19, 14:51-54, FIGS. 5A-7B, was also well-known before the '425 patent. The prior art is replete with teachings that confirm this, including under Plaintiff's apparent understanding of the claims. *See, e.g.*, D920_Report, at 4-39, 4-46, 4-53, 4-56, 5-13, 6-14 through 6-16, Figs. 4.5.11, 4.6.3, 4.6.8, 4.6.11, 5.3.6, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 90nm article, at Fig. 6; Stratix_IV_Report, 3-68; James TSMC article; Baik820, at Title, Abstract, ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0027]-[0032], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶ [0056], ¶ [0058], FIGS. 1C-1I, 4A-5E; Bohr683, at Title, Abstract, ¶ [0007], ¶ [0011], ¶¶ [0024]-[0037], ¶ [0039], ¶¶ [0043]-[0048], ¶ [0050], FIGS. 4-8; Chen179 ¶ [0003], ¶ [0017], ¶¶ [0021]-[0022], FIGS. 1A-1D; Chen729 ¶ [0001], ¶¶ [0020]-[0021], FIGS. 1, 5, 6; Cheng810, ¶ [0021], ¶ [0022], ¶ [0025], ¶ [0030], ¶ [0032], FIGS. 1D-1F; Cheng817, ¶ [0061], ¶ [0063], ¶ [0069], ¶ [0078], ¶ [0083], FIGS. 4j, 5i; Doris784 ¶ [0029], ¶ [0031], ¶ [0038], ¶ [0051]; Hsu823, ¶¶ [0034]-[0035], FIGS. 11A, 13; Ke984, ¶¶ [0005]-[0006], ¶ [0027], FIG. 10; Lee870, ¶ [0044], FIGS. 4, 5; Ogura844, ¶ [0011], ¶ [0031], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, at Abstract, ¶¶ [0074]-[0076], ¶¶ [0104]-[0105], ¶¶ [0107]-[0114], ¶ [0124], FIGS. 12,

21; Alvarez069, ¶¶ [0029]-[0032], ¶ [0037], ¶¶ [0044]-[0046], ¶ [0063], ¶ [0064], ¶ [0068], ¶ [0073], FIGS. 3, 4, 8, 10; Chidambarrao205, ¶ [0058], FIG. 4F; Fischer208, ¶ [0037], ¶ [0040], ¶¶ [0062]-[0065], ¶¶ [0100]-[0102], FIGS. 1, 5E, 7A-7C, 8; Fujimoto807, ¶ [0017], ¶ [0031], ¶ [0068], ¶ [0074], ¶ [0091], FIGS. 3C, 4B, 7C, 10D; Fukutome203, ¶ [0103], ¶ [0125], ¶ [0130], FIGS. 5F, 5G, 8C; Jung104, ¶ [0035], ¶ [0079], FIGS. 1A-1C; Kavalieros729, ¶ [0042], FIG. 13; Kwon360, Abstract, ¶¶ [0001]-[0003], ¶¶ [0007]-[0009], ¶ [0014], ¶ [0015], ¶ [0022], ¶ [0024], FIGS. 3(c), 4; Maeda455, ¶¶ [0005]-[0006], ¶ [0017], ¶ [0028], ¶ [0039], ¶ [0079], ¶¶ [0083]-[0091], ¶¶ [0102]-[0109], FIGS. 9, 10, 23-27; Mistry2007 article, 247-250, Figs. 5, 6; Mistry2007 Presentation. 16, 19; Miyashita476, ¶ [0079], FIGS. 5A-5I; Murthy482, Abstract, 1:14-2:20, 2:66-5:33, 5:31-6:30, 6:60-9:63, FIGS. 2-4b, 8; Murthy556, 3:30-46, 9:31-43, 9:58-11:15, FIGS. 2, 11-15; Shifren983, Abstract, ¶ [0002], ¶ [0009], ¶ [0011], ¶¶ [0017]-[0019], ¶ [0024], ¶ [0025], FIGS. 6, 7; Thompson Nov2004 article, 1790-1797, Figs. 3, 5; Yasutake article, 48 49, Figs. 1, 9.

A first MIS transistor with the first sidewall spacer including an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer, *see, e.g.*, ’425 patent at 10:17-40, 15:40-51, FIGS. 1B-6B; *cf. also id.* at 18:44-53, 19:5-22, FIGS. 7A-7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:14-22, 2:61-62, FIGS. 8B-10C; Ghani article, at 978, Figs. 1, 4, 5 (incorporated by reference in the ’425 patent); Luo article, at 489-90, Figs. 1, 2, 8, 14 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 4-38 through 4-40, 4-43 through 4-49, 4-54 through 4-56, 5-10 through 5-13, 6-14, Figs. 4.5.10 through 4.5.12, 4.6.1 through 4.6.4, 4.6.9 through 4.6.11, 5.3.3 through 5.3.6, 6.2.4 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same);

Stratix_IV_Report, 3-68; James TSMC article; Bohr683 ¶ [0005], ¶ [0017], ¶ [0021], ¶¶ [0030]-[0031], ¶ [0040], ¶ [0043], FIGS. 2-8; Ogura844, ¶ [0022], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Baik820 ¶ [0026], ¶ [0042], FIGS. 1B-1I, 4A-5F; Chen179 ¶ [0002], ¶ [0004], ¶ [0007], ¶ [0020], ¶ [0022], ¶ [0024], ¶ [0027], ¶ [0036], FIGS. 1A-3E; Chen729 ¶ [0001], ¶ [0004], ¶¶ [0012]-[0016], ¶¶ [0018]-[0022], FIGS. 1-6; Cheng810 ¶¶ [0019]-[0020], ¶ [0030], FIGS. 1A-1F; Cheng817, at Abstract, ¶ [0017], ¶¶ [0020]-[0021], ¶ [0023], ¶ [0025], ¶ [0027], ¶ [0035], ¶¶ [0043]-[0045], ¶¶ [0048]-[0050], ¶ [0054], ¶¶ [0061]-[0064], ¶ [0066], ¶¶ [0076]-[0079], ¶ [0081], ¶¶ [0090]-[0093], ¶ [0095], ¶ [0097], ¶ 0099], ¶ [0101], claims 33, 42, FIGS. 1, 2, 3b-3n, 4b-4j, 5b-5i, 6b-6i, 7; Chidambarrao205, at Abstract, ¶¶ [0005]-[0009], ¶ [0012], ¶ [0015], ¶¶ [0020]-[0023], ¶ [0030], ¶ [0041], ¶¶ [0050]-[0055], ¶¶ [0060]-[0061], FIGS. 2, 3, 4B-4F; Fischer208, ¶ [0036], ¶ [0049], ¶ [0060], ¶ [0066], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5C, 7A-7C, 8; Fujimoto807, at Abstract, ¶¶ 0006]-[0008], ¶ [0013], ¶ [0016], ¶¶ [0022]-[0025], ¶¶ [0031]-[0032], ¶¶ [0034]-[0035], ¶ [0037], ¶¶ [0042]-[0044], ¶¶ [0058]-[0061], ¶ [0063], ¶¶ [0066]-[0067], ¶ [0073], ¶[0076], ¶¶ [0081]-[0084], ¶ [0087], ¶¶ [0089]-[0090], FIGS. 1B-3C, 5B-7C, 8B-10D; Hatada776, at Abstract, ¶¶ [0007]-[0009], ¶ [0037], ¶ [0039], ¶¶ [0047]-[0048], ¶ [0091]-[0099], ¶¶ [0106]-[0109], ¶¶ [0111]-[0112], ¶ [0116], ¶¶ [0120]-[0121], ¶¶ [0124]-[0127], ¶ [0130], ¶ [0132], ¶¶ [0135]-[0145], ¶¶ [0149]-[0170], ¶ [0175], FIGS. 2B-2F, 3, 4B-4F, 5B-5F, 6E-6I, 7D-7H, 8-12; Jung104 ¶ [0035], ¶ [0079], ¶ [0090], FIGS. 1A-1C; Ke984 ¶ [0018], ¶ [0021], FIGS. 4-10; Kwon360 ¶ [0005], ¶ [0017], ¶ [0024], Figs. 2(a), 2(b), 2(d)-3(c); Lee870 ¶¶ [0044]-[0045], FIGS. 1-6; Murthy556, at Abstract, 1:37-42, 1:54-55, 2:6-11, 2:21-23, 3:22-54, 4:43-46, 6:22-7:16, 7:53-63, 8:10-22, 9:10-57, 10:28-31, 10:42-55, FIGS. 2, 8-15; Shimamune398, at Abstract, ¶ [0008], ¶ [0010], ¶¶ [0075]-[0076], ¶¶ [0096]-[0097], ¶ [0107], ¶¶ [0112]-[0114], ¶ [0118], ¶¶ [0121]-[0122], ¶ [0130], ¶ [0143], ¶ [0159], ¶ [0165], FIGS. 3-5D,

8B-9; Wang906 ¶ [0026], ¶¶ [0029]-[0031], ¶¶ [0033]-[0036], ¶ [0039], FIGS. 5-11, 15, 16; Wu922 ¶¶ [0017]-[0018], ¶¶ [0022]-[0025], ¶ [0028], ¶ [0034], ¶¶ [0037]-[0039], ¶¶ [0042]-[0044], ¶ [0047], ¶ [0053], ¶¶ [0057]-[0058], FIGS. 1-4, 7-12, 14, 15; Yamasaki170 ¶ [0039], ¶¶ [0057]-[0058], ¶ [0065], FIGS. 11A-12B, 22A-27B, 29A-31B, 39A-41B; James 90nm article, at 72-76, Figs. 1-3, 5, 6, 8, 9, 10(a), 10(b), 11, 12; D920_Report, at 4-38 through 4-40, 4-43 through 4-49, 4-54 through 4-56, 5-10 through 5-13, 6-14, Figs. 4.5.10 through 4.5.12, 4.6.1 through 4.6.4, 4.6.9 through 4.6.11, 5.3.3 through 5.3.6, 6.2.4 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76-79, Figs. 1(c), 2(a)-2(c), 3(a)-3(c), 4(a)-4(c); Thompson Apr2004 article, at 191, Fig. 1; Thompson Nov2004 article, at 1791, Figs. 2, 4; Bohr article, at 3, Fig. 2; Morin article, at 355-56, 366, Figs. 1, 2, 20; James TSMC article, at 8, Fig. 17 (describing TSMC_425_Product[23]).

The first MIS transistor being a p-type MIS transistor, *see, e.g.*, ’425 patent at 4:29-32, 8:62-9:14, 9:54-10:16, 11:10-22, 11:28-48, 12:42-58, 13:20-39, 14:24-42, 17:4-20, 18:9-12, FIGS. 1A-7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:1-13, 2:32-36, 2:43-51, 2:61-62, FIGS. 8A-10C; Murthy131, at 2:1-15, 2:52-60, 3:1-27, 3:40-48, 3:65-4:8, FIG. 6 (incorporated by reference in the ’425 patent); Ghani article, at 978, Figs. 1, 4 (same); Luo article, at 489-90, Figs. 1, 2, 8, 14 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-39 through 4-40, 4-42, 4-46 through 4-48, 4-53, 4-56, 4-60 through 4-61, 5-12 through 5-13, 6-12 through 6-16, 8-3,

[23] Under Plaintiff’s apparent interpretation of the claim language, the claimed “L shape” may include a “J” shape. *See* AICP’s P.R. 3-1 Disclosures, Ex. H, at 28. Although TSMC disagrees with such an interpretation, combinations involving TSMC_425_Product would satisfy this claim feature if applied since the pFET sidewalls spacers in TSMC_425_Product resemble the pFET sidewall spacers in the accused products analyzed in AICP’s infringement contentions.

Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.11, 4.5.12, 4.6.3, 4.6.4, 4.6.8, 4.6.11, 4.8.1, 5.3.5, 5.3.6, 6.2.2 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 65/45 article, at 79-80, Fig. 6 (describing Intel_E5410); Stratix_IV_Report, 3-68; James TSMC article; Baik820, at Abstract, ¶¶ [0004]-[0009], ¶¶ [0010]-[0013], ¶¶ [0023]-[0058], FIGS. 1A-1I, 4A-5E; Bohr683, at Title, Abstract, ¶ [0002], ¶¶ [0004]-[0011], ¶ [0012]-[0013], ¶¶ [0015]-[0041], ¶¶ [0043]-[0050], FIGS. 1-8; Chen179, at Title, Abstract, ¶ [0001], ¶¶ [0002]-[0005], ¶¶ [0006]-[0007], ¶¶ [0016]-[0017], ¶¶ [0019]-[0022], FIGS. 1A-1D; Chen729, at Abstract, ¶ [0001], ¶¶ [0002]-[0003], ¶ [0009], ¶ [0012], ¶ [0014], ¶¶ [0016]-[0023], FIGS. 1-6; Cheng810 Abstract, ¶ [0001], ¶¶ [0007]-[0009], ¶ [0011], ¶¶ [0013]-[0014], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0033]-[0037], ¶ [0056], ¶ [0060], ¶ [0065], ¶ [0068], ¶ [0070], ¶ [0072], ¶ [0075], ¶ [0080], FIGS. 4j, 5i; Doris784, Abstract, ¶ [0002], ¶¶ [0009]-[0014], ¶ [0031], ¶¶ [0036]-[0052], FIGS. 4-15; Hatada776, at Abstract, ¶ [0017], ¶ [0025], ¶ [0027], ¶ [0033], ¶ [0035], ¶ [0038], ¶¶ [0045]-[0046], ¶ [0050], ¶¶ [0057]-[0058], ¶ [0061], ¶¶ [0088]-[0089], ¶ [0094], ¶¶ [0101]-[0106], ¶ [0110], ¶¶ [0112]-[0113], ¶ [0119], ¶¶ [0128]-[0129], ¶ [0131], ¶¶ [0137]-[0138], ¶ [0150], ¶ [0152], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶¶ [0028]-[0029], ¶¶ [0032]-[0033], ¶ [0039], FIGS. 7B, 11A, 13; James 90nm article, at 73-74, 76, Fig. 6; Ke984, at Abstract, ¶¶ [0005]-[0006], ¶¶ [0016]-[0017], ¶¶ [0019]-[0021], FIG. 10; Lee870, at Abstract, ¶ [0002], ¶¶ [0016]-[0020], ¶ [0026], ¶ [0036], ¶ [0040], ¶¶ [0042]-[0044], FIGS. 4, 5; Ogura844, ¶¶ [0020]-[0021], ¶¶ [0023]-[0027], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, ¶ [0051], ¶ [0057], ¶¶ [0062]-[0063], ¶ [0066], FIGS. 12, 21; Shimamune398, at Abstract, ¶ [0007], ¶ [0029], ¶ [0037], ¶ [0040], ¶¶ [0073]-[0167], FIGS. 3, 4A-8E, 9; Wang906, at Abstract, ¶ [0011], ¶ [0023], ¶ [0027], ¶¶ [0030]-[0032], ¶¶ [0037]-[0038], ¶ [0041], FIG. 16; Wu922, at Abstract, ¶ [0017], ¶ [0021], ¶¶ [0026]-[0027],

¶ [0031], ¶ [0038], ¶ [0041], ¶¶ [0045]-[0046], ¶ [0050], ¶ [0057], FIGS. 7, 14; Yamasaki170, ¶ [0054], ¶¶ 0058]-[0062], ¶ [0064], ¶¶ [0067]-[0068], FIGS. 31A-31B; Stratix_IV_Report, 3-68; James TSMC article; Alvarez069, ¶ [0025], ¶ [0038], ¶ [0042], ¶ [0043], ¶¶ [0046]-[0053], ¶ [0059], ¶ [0063], ¶¶ [0065]-[0067], ¶ [0076], FIGS. 5-11; Chidambarrao205, Abstract, ¶ [0001], ¶¶ [0012]-[0025], ¶¶ [0030]-[0034], ¶ [0041], FIG. 4F; Chuang243, Abstract, 1:51-67, 2:39-56, 3:13-15, 3:40-54, 5:15-6:32, FIGS. 1A-1I; Fischer208, ¶¶ [0004]-[0007], ¶¶ [0022]-[0027], ¶¶ [0030]-[0048], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 7A-7C, 8; Fujimoto807, Abstract, ¶¶ [0022]-[0045], ¶¶ [0058]-[0063], ¶¶ [0064]-[0075], ¶¶ [0080]-[0097]; Fukutome203, Abstract, ¶¶ [0004]-[0019], ¶¶ [0054]-[0055], ¶ [0074], ¶ [0083], ¶¶ [0085]-[0104], ¶¶ [0109]-[0111], ¶ [0115], ¶¶ [0121]-[0126], ¶¶ [0137]-[0146], ¶¶ [0157]-[0162], ¶ [0164], ¶¶ [0168]-[0177], ¶¶ [0185]-[0191], ¶¶ [0199]-[0201], ¶ [0206], ¶ [0240], ¶¶ [0248]-[0249], FIGS. 5D-5G, 8A-8C, 9C-9D, 11D-11E, 12C-12D, 13D-14B, 16; Jung104, ¶ [0002], ¶ [0006], ¶ [0007], ¶ [0009], ¶ [0035], ¶ [0079], ¶ [0084], ¶ [0105], FIGS. 1A-1C; Kavalieros729, Abstract, ¶ [0001], ¶ [0016], ¶ [0018], ¶ [0021], ¶ [0024], ¶ [0025], ¶ [0040], ¶ [0043], FIG. 13; Komoda article, 217-220, Figs. 2, 3; Koutny207, ¶ [0002], ¶ [0028], ¶ [0035], ¶ [0046], ¶ [0083], ¶ [0086], ¶ [0094], ¶ [0099], ¶¶ [0106]-[0108], FIG. 6A; Kwon360, Abstract, ¶ [0001], ¶¶ [0004]-[0009], ¶ [0013], ¶¶ [0015]-[0017], ¶¶ [0018]-[0024], Figs. 3(c), 4; Liu article, 836-839, Figs. 2-18; Maeda455, Abstract, ¶¶ [0002]-[0020], ¶ [0062], ¶¶ [0083]-[0091], ¶¶ [0102]-[0109], FIGS. 9, 10, 21-27; Mistry2007 article, 247-250, Figs. 5, 6; Mistry2007 Presentation, 15a-15j, 16-19, 21-26; Miyashita476, ¶ [0014], ¶ [0015], ¶ [0018], ¶ [0022], ¶ [0026], ¶¶ [0033]-[0038], ¶¶ [0043]-[0051], ¶¶ [0058]-[0062], ¶¶ [0071]-[0073], ¶¶ [0078]-[0083], ¶¶ [0090]-[0093], FIGS. 1A-5I; Murthy482, Abstract, 1:14-2:20, 2:66-9:63, FIGS. 2-8; Murthy556, 1:6-2:43, 2:47-12:10, FIGS. 1-15; Natarajan article, 1-3, Figs. 2-8; Shifren983, ¶¶ [0001]-[0003], ¶ [0011], ¶¶ [0015]-[0020], ¶ [0024], ¶ [0025], FIGS. 2-7;

Thompson Apr2004 article, 191-193, Tbl. 1, Figs. 1-3; Thompson Nov2004 article, 1790-1797, Figs. 2, 5(c), 6, 8, 9, 12, 13; Yasutake article, 48 49, Fig. 1-15.

The first stress being a compressive stress, *see, e.g.*, '425 patent at 4:29-32, 11:20-22, 14:43-45, 16:12-25, 17:21-32, was also well-known before the '425 patent, *see, e.g.*, *id.* at 1:15-56, 2:32-36, 2:61-62; Murthy131, at 3:40-59, 4:9-29, FIG. 7 (incorporated by reference in the '425 patent); Ghani article, at 978, Figs. 1, 4 (same); Luo article, at 489-90, Figs. 6, 10 (same). The prior art is replete with teachings that confirm this admission in the '425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-39 through 4-40, 4-42, 4-46 through 4-48, 4-53, 4-56, 5-12 through 5-13, 6-12 through 6-16, Tbls. 1.6.1, 4.6.1, Figs. 4.5.11, 4.5.12, 4.6.3, 4.6.4, 4.6.8, 4.6.11, 5.3.5, 5.3.6, 6.2.2 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 65/45 article, at 76, 79-80, Fig. 6 (describing Intel_E5410); Stratix_IV_Report, 3-65; James TSMC article; Baik820, at Title, Abstract, ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0027]-[0032], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶ [0056], ¶ [0058], FIGS. 1C-1I, 4A-5E; Bohr683 ¶¶ [0024]-[0026], ¶ [0028], ¶ [0035], ¶ [0039], ¶ [0041], ¶¶ [0044]-[0046], ¶ [0048], FIGS. 4-8; Chen179, at Abstract, ¶¶ [0003]-[0004], ¶¶ [0021]-[0022], FIGS. 1A-1D; Chen729 ¶ [0001], ¶ [0006], ¶ [0009], ¶¶ [0020]-[0021], FIGS. 1, 5, 6; Cheng810 ¶ [0014], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶ [0002], ¶ [0022], ¶ [0044], ¶ [0065], ¶ [0069], ¶ [0080], ¶ [0083], FIGS. 4j, 5i; Hatada776, at Abstract, ¶ [0006], ¶ [0018], ¶ [0027], ¶ [0035], ¶ [0038], ¶¶ [0045]-[0046], ¶¶ [0057]-[0058], ¶¶ [0101]-[0104], ¶ [0106], ¶¶ [0112]-[0113], ¶ [0119], ¶ [0131], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶¶ [0032]-[0033], ¶ [0039], FIGS. 7B, 11A, 13; James 90nm article, at 73-74, 76, Fig. 6; Ke984, ¶ [0003], ¶¶ [0019]-[0021], FIG. 10; Lee870, ¶ [0044], FIGS. 4, 5; Ogura844, ¶ [0005], ¶¶ [0007]-[0008], ¶¶ [0020]-[0021], ¶¶ [0024]-[0029], ¶¶ [0058]-[0061],

FIGS. 1I, 1M, 4A-4B; Shimamune398, at Abstract, ¶ [0007], ¶¶ [0011]-[0013], ¶¶ [0031]-[0032], ¶¶ [0037]-[0038], ¶¶ [0043]-[0045], ¶ [0052], ¶¶ [0076]-[0077], ¶¶ [0084]-[0085], ¶ [0097], ¶¶ [0117]-[0118], ¶¶ [0126]-[0129], ¶ [0135], ¶ [0137], ¶ [0141], FIGS. 3, 8E; Wang906, ¶¶ [0004]-[0005], ¶ [0011], ¶¶ [0030]-[0032], FIG. 16; Wu922, ¶ [0005], ¶ [0009], ¶ [0021], ¶ [0031], ¶ [0041], ¶ [0050], FIGS. 7, 8, 14, 15; Yamasaki170, ¶ [0003], ¶¶ 0059]-[0062], ¶ [0064], ¶¶ [0067]-[0068], FIGS. 31A-31B; Sun article, at Abstract, 1-16; Bohr article, at 1-3, Figs. 1, 2; Chidambarrao205, Abstract, ¶ [0003], ¶ [0004], ¶ [0012], ¶ [0053]-[0055], ¶¶ [0056]-[0061], FIGS. 1-3, 4C-4F; Chuang243, Abstract, 1:51-67, 2:32-56, 3:13-15, 5:28-6:32, FIG. 1H, 1I; Fischer208, ¶¶ [0004]-[0007], ¶ [0014], ¶ [0015], ¶¶ [0022]-[0024], ¶¶ [0030]-[0034], ¶ [0037], ¶ [0040], ¶¶ [0046]-[0048], ¶¶ [0060]-[0066], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5C, 7A-7C, 8; Fujimoto807, Abstract, ¶¶ [0013]-[0018], ¶¶ [0021]-[0045], ¶¶ [005]-[0075], ¶¶ [0080]-[0097], FIGS. 2C-4C, 6C-7C, 9D-10D; Fukutome203, Abstract, ¶¶ [0004]-[0019], ¶¶ [0054]-[0055], ¶ [0074], ¶ [0083], ¶¶ [0085]-[0104], ¶¶ [0109]-[0111], ¶ [0115], ¶¶ [0121]-[0126], ¶¶ [0137]-[0146], ¶ [0148], ¶¶ [0157]-[0162], ¶ [0164], ¶¶ [0168]-[0177], ¶¶ [0185]-[0191], ¶¶ [0199]-[0201], ¶ [0206], ¶ [0240], ¶¶ [0248]-[0249], FIGS. 5D-5G, 8A-8C, 9C-9D, 11D-11E, 12C-12D, 13D-14B, 16; Jung104, ¶ [0002], ¶ [0006], ¶ [0007], ¶ [0009], ¶ [0035], ¶ [0079], ¶ [0084], ¶ [0105], FIGS. 1A-1C; Kavalieros729, Abstract, ¶ [0001], ¶ [0016], ¶ [0024], ¶ [0025], ¶ [0040], ¶ [0043], FIG. 13; Kwon360, ¶ [0002], ¶ [0003], ¶¶ [0001]-¶ [0009], ¶ [0011], ¶ [0013], ¶¶ [0015]-[0024], Figs. 1-4; Maeda455, ¶¶ [0011]-[0020], ¶ [0029], ¶ [0042], ¶ [0048], ¶¶ [0083]-[0091], ¶¶ [0102]-[0109], FIGS. 9, 10, 23-27; Mistry2007 article, 247-250, Figs. 5, 6; Mistry2007 Presentation, 7, 14, 15a-15j, 16-19, 21-35; Miyashita476, ¶ [0018], ¶ [0026], ¶ [0033], ¶¶ [0036]-[0038], ¶¶ [0043]-[0051], ¶¶ [0058]-[0062], ¶¶ [0071]-[0073], ¶¶ [0078]-[0083], ¶¶ [0090]-[0093], FIGS. 1U-1Y, 3A-3D, 5A-5I; Murthy482, Abstract, 1:41-2:4, 4:4-6:49, 6:60-7:10, FIGS. 2-8;

Murthy556, Abstract, 1:52-64, 2:15-17, 2:58-3:29, 3:55-4:67, 6:60-9:9, 9:58-11:30, FIGS. 2, 6-15; Natarajan article, 1-3, Fig. 2; Shifren983, Abstract, ¶¶ [0001]-[0003], ¶ [0011], ¶¶ [0015]-[0020], ¶ [0024], FIGS. 2-7; Thompson Apr2004 article, 191-193, Tbl. 1, Figs. 1-3; Thompson Nov2004 article, 1790-1797, Figs. 2-7, 10, 13; Yasutake article, 48 49, Fig. 1.

The second stress being a tensile stress, *see, e.g.*, '425 patent at 4:29-32, 13:66-14:3, 16:26-30, 19:25-34, was also well-known before the '425 patent, *see, e.g.*, *id.* at 1:15-56, 2:58-62; Ghani article, at 978, Figs. 5, 6 (incorporated by reference in the '425 patent). The prior art is replete with teachings that confirm this admission in the '425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-7, 4-16 through 4-17, 4-36, 4-38 through 4-41, 4-43 through 4-48, 4-53 through 4-58, 5-9 through 5-13, 6-9 through 6-10, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.3.1, 8.2.1, Figs. 4.3.9, 4.3.10, 4.5.8, 4.5.10 through 4.5.13, 4.6.1 through 4.6.4, 4.6.8 through 4.6.11, 4.7.1, 4.7.2, 5.3.2 through 5.3.6, 6.1.10, 6.1.11, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 76, 79-80, Figs. 6, 7 (describing Intel_E5410); Baik820 ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0024]-[0033], ¶¶ [0034]-[0040], ¶¶ [0043]-[0046], ¶ [0049], ¶¶ [0051]-[0054], ¶¶ [0056]-[0058], FIGS. 1H-1I, 5E-5F; Bohr683 ¶ [0039], ¶ [0041], ¶ [0045], ¶ [0048], FIGS. 6, 8; Chen179, at Title, Abstract, ¶¶ [0002]-[0004], ¶¶ [0006]-[0007], ¶ [0013], ¶ [0016], ¶¶ [0019]-[0025], FIGS. 1A-1D; Chen729 ¶ [0023], FIG. 6; Cheng810 Abstract, ¶ [0001], ¶ [0013], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0002]-[0003], ¶ [0030], ¶ [0070], ¶ [0084], FIGS. 4j, 5i; Doris784, ¶ [0005], ¶ [0008], ¶ [0013], ¶ [0029], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 14, 15; Hsu823, ¶ [0003], ¶¶ [0036]-[0037], FIGS. 7B, 11A, 13; James 90nm article, at 73-74, 76, Fig. 6; Ke984, ¶ [0003], ¶ [0030], FIG. 10; Lee870, at Abstract, ¶¶ [0021]-[0022], ¶¶ [0028]-[0030], ¶ [0038], ¶ [0049], ¶ [0051], ¶ [0057], ¶¶ [0060]-[0064], ¶ [0067], FIGS. 4, 5; Ogura844,

¶ [0033], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Wu922, ¶ [0005], ¶ [0025], ¶ [0036], ¶ [0044], FIGS. 7, 14; Yamasaki170, ¶ [0013], ¶ [0016], ¶ [0067], FIGS. 31A-31B; Sun article, at 1-16; Bohr article, at 1-3, Figs. 1, 2; ITRS_2007_FEP, at 10; Alvarez069, Abstract, ¶ [0020], ¶ [0022], ¶ [0025], ¶ [0033], ¶¶ [0047]-[0055], ¶ [0059], ¶¶ [0061]-[0063], ¶ [0065], ¶ [0066], ¶ [0069], Tbl. 1, FIGS. 1, 4, 6-13; Chuang243, 1:47-50, 2:32-38, 3:13-18, 3:23-27, 5:28-38, 5:58-6:9, 6:15-23, 6:58-61, FIGS. 1H, 1I; Fischer208, ¶ [0034], ¶ [0038], ¶ [0067], ¶ [0099], FIGS. 1, 5F-5I, 7E, 8; see generally Jung104; see also Jung104, Abstract, ¶ [0002], ¶ [0007], ¶¶ [0012]-[0014], ¶¶ [0016]-[0018], ¶ [0029], ¶ [0035], ¶ [0036], ¶¶ [0048]-[0063], ¶ [0079], ¶ [0083], ¶ [0084], ¶ [0089], ¶ [0090], ¶ [0092],¶ [0094], ¶ [0099], ¶¶ [0102]-[0130], TBLS. IV-VI, FIG. 1B, 1C, 2, 4A-14B; Komoda article, 217-220, Tbl. 1, Fig2. 2, 3, 17; Koutny207, ¶ [0028], ¶ [0036], ¶ [0107], ¶ [0108], FIG. 6A; Liu article, 836-839, Tbls. I, II, Figs. 1-7; Maeda455, ¶¶ [0006], ¶ [0016], ¶ [0020], ¶ [0027], ¶¶ [0034]-[0038], ¶¶ [0042]-[0045], ¶¶ [0049]-[0050], ¶¶ [0083]-[0091], ¶¶ [0102]-[0109], FIGS. 9, 10, 23-27; Mistry2007 article, 247-250, Figs. 5, 6; Mistry2007 Presentation, 16, 19; Miyashita476, ¶ [0080]; Thompson Apr2004 article, 191-193, Fig. 1; Thompson Nov2004 article, 1790-1797, Figs. 2, 5, 12.

A second MIS transistor with a second gate insulating film formed on a second active region in the semiconductor substrate, *see, e.g.*, ’425 patent at 8:42-37, 15:6-23, 17:33-67, FIGS. 1A-7B, was well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:1-6, 2:61-62, FIGS. 8A-10C; Ghani article, at 978, Figs. 1, 4, 5 (incorporated by reference in the ’425 patent); Luo article, at 489-90, Fig. 1 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-38, 4-42 through 4-52, 4-56, 5-10 through 5-14, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.10, 4.5.11, 4.6.1 through 4.6.7, 4.6.11, 5.3.3 through 5.3.7, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai

article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Stratix_IV_Report, 3-66, 3-70; James TSMC article; Baik820 ¶ [0004], ¶ [0011], ¶ [0013], ¶¶ [0024]-[0026], ¶ [0033], FIGS. 1A-1I, 4A-5E; Bohr683, at Abstract, ¶ [0002], ¶¶ [0004]-[0011], ¶¶ [0012]-[0031], ¶ [0033], ¶ [0036], ¶¶ [0038]-[0041], ¶¶ [0043]-[0046], ¶ [0050], FIGS. 1-8; Chen179, at Abstract, ¶¶ [0002]-[0004], ¶¶ [0006]-[0007], ¶ [0016], ¶¶ [0018]-[0021], FIGS. 1A-1D; Chen729 ¶ [0001], ¶ [0012], ¶ [0014], ¶¶ [0017]-[0023], FIGS. 1-6; Cheng810 ¶¶ [0015]-[0016], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0056]-[0058], ¶¶ [0072]-[0073], FIGS. 4j, 5i; Doris784, ¶ [0019], ¶ [0036], FIGS. 14, 15; Hatada776, ¶¶ [0089]-[0090], ¶ [0135], ¶ [0147], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶ [0028], FIGS. 7B, 11A, 13; James 90nm article, at 73, Fig. 5; Ke984, ¶ [0016], FIG. 10; Lee870, ¶ [0045], FIGS. 4, 5; Ogura844, ¶ [0021], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, ¶ [0051], ¶ [0124], FIGS. 12, 21; Wang906, ¶ [0024], FIG. 16; Wu922, ¶ [0017], ¶ [0038], FIGS. 7, 14; Yamasaki170, ¶ [0056], ¶ [0058], FIGS. 31A-31B; Sun article, at 16, 19-20; Quirk & Serda, at 311-312, FIGS. 12.1, 12.12-12.14; Bohr article, at 1-3, Figs. 1, 2; ITRS_2007_PIDS, at 6, 14-16, 24-27, Tbls. PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, PIDS3d, Figs. PIDS2, PIDS3, PIDS4, PIDS5; ITRS_2007_FEP, at 2, 5, 10, 12-13, 16, 19-20, 26-32, 35, 37-38, Tbls. FEP4a, FEP4b, Figs. FEP1, FEP4, FEP5; Alvarez069, ¶ [0020], ¶ [0039], ¶ [0040], ¶ [0063], FIGS. 5-11; Chuang243, 3:55-64, 5:1-14, 6:10-32, FIG. 1I; Fischer208, ¶¶ [0004]-[0007], ¶ [0031], ¶ [0036], ¶ [0040], ¶ [0041], ¶ [0047], ¶ [0048], ¶ [0058], ¶ [0078], ¶ [0082], ¶ [0090], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5A-5I, 8; Fujimoto807, Abstract, ¶ [0058], ¶ [0081], FIGS. 1A-10D; Jung104, ¶¶ [0002]-[0016], ¶¶ [0035]-[0037], ¶ [0079], FIGS. 1A-1C; Kavalieros729, ¶ [0017], ¶ [0046], FIG. 14; Koutny207, ¶¶ [0069]-[0074], FIG. 6A; Kwon360, ¶ [0017], Figs. 3(c), 4; Maeda455, ¶¶ [0003]-[0009], ¶¶ [0011]-[0020], ¶ [0062], ¶¶

[0078]-[0087], ¶ [0092], ¶ [0097], ¶¶ [0102]-[0110], FIGS. 9, 10, 21-27; Mistry2007 article, 247-250, Figs. 2, 5; Mistry2007 Presentation, 4, 5, 14, 15a-15j, 17-35; Miyashita476, ¶ [0020], FIGS. 1D-5F5I; Murthy482, 4:32-34; Murthy556, 5:16-23-28, 11:45-12:8; Natarajan article, 1-3; Shifren983, ¶ [0014], FIGS. 6, 7.

A second MIS transistor with a second gate electrode formed on the second gate insulating film, *see, e.g.*, '425 patent at 9:15-37, 11:54-59, 13:20-39, 15:6-23, 17:33-67, 18:54-56, FIGS. 1A-7B, was also well-known before the '425 patent, *see, e.g.*, *id.* at 1:15-56, 2:1-6, 2:61-62, FIGS. 8A-10C; Ghani article, at 978, Figs. 1, 4, 5 (incorporated by reference in the '425 patent); Luo article, at 489-90, Fig. 1 (same). The prior art is replete with teachings that confirm this admission in the '425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-38 through 4-40, 4-42 through 4-52, 4-56, 5-10 through 5-14, 6-11, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.10 through 4.5.12, 4.6.1 through 4.6.7, 4.6.11, 5.3.3 through 5.3.7, 6.2.1, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Stratix_IV_Report, 3-70; James TSMC article; Baik820 ¶ [0006], ¶ [0024], ¶ [0035], ¶ [0037], ¶ [0039], ¶ [0052], ¶ [0054], ¶ [0056], FIGS. 1A-1I, 4A-5E; Bohr683 ¶ [0004], ¶ [0008], ¶ [0012], ¶¶ [0014]-[0017], ¶¶ [0019]-[0020], ¶¶ [0022]-[0023], ¶¶ [0030]-[0032], ¶¶ [0036]-[0037], ¶ [0040], ¶ [0043], ¶ [0045], ¶ [0047], FIGS. 1-8; Chen179 ¶ [0002], ¶ [0007], ¶ [0020], ¶ [0022], ¶ [0024], FIGS. 1A-1D; Chen729 ¶ [0001], ¶¶ [0012]-[0013], ¶ [0018], ¶ [0023], FIGS. 1-6; Cheng810 ¶ [0015], ¶ [0017], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0056]-[0058], ¶¶ [0072]-[0073], FIGS. 4j, 5i; Doris784, ¶ [0019], ¶ [0036], FIGS. 14, 15; Hatada776, Abstract, ¶ [0026], ¶ [0034], ¶¶ [0038]-[0039], ¶ [0044], ¶¶ [0046]-[0048], ¶ [0052], ¶ [0058], ¶ [0060], ¶ [0062], ¶ [0063], ¶ [0089], ¶ [0091], ¶ [0093], ¶¶ [0124]-

[0125], ¶ [0127], ¶ [0135], ¶¶ [0138]-[0143], ¶ [0147], ¶ [0149], ¶ [0151], ¶ [0153], ¶ [0158], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶ [0028], FIGS. 7B, 11A, 13; James 90nm article, at 73, Fig. 5; Ke984, ¶ [0016], FIG. 10; Lee870, ¶ [0045], FIGS. 4, 5; Ogura844, ¶ [0021], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, ¶ [0051], ¶ [0066], ¶ [0093], ¶ [0124], FIGS. 12, 21; Wang906, ¶ [0024], FIG. 16; Wu922, ¶ [0017], ¶ [0038], FIGS. 7, 14; Yamasaki170, ¶¶ [0056]-[0058], ¶¶ [0065]-[0066], FIGS. 31A-31B; Sun article, at 16, 19-20; Quirk & Serda, at 311-312, FIGS. 12.1, 12.12-12.14; Bohr article, at 1-3, Figs. 1, 2; ITRS_2007_PIDS, at 6, 14-16, 24-27, Tbls. PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, PIDS3d, Figs. PIDS2, PIDS3, PIDS4, PIDS5; ITRS_2007_FEP, at 2, 3, 12-13, 16-17, 19-20, 26-38, Tbls. FEP1, FEP2a, FEP2b, FEP3a, FEP3b, FEP4a, FEP4b, Figs. FEP1, FEP4, FEP5; Alvarez069, ¶ [0020], ¶ [0039], ¶ [0040], ¶ [0063], FIGS. 5-11; Chuang243, 4:57-67, 5:1-14, 6:10-32, FIGS. 1A-1I; Fischer208, ¶ [0036], ¶ [0037], ¶ [0040], ¶¶ [0058]-[0066], ¶ [0070], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5A-5I, 8; Fujimoto807, Abstract, ¶ [0022], ¶ [0023], ¶¶ [0027]-[0037], ¶ [0037], ¶¶ [0058]-[0068], ¶¶ [0081]-[0093], FIGS. 1A-10D; Jung104, ¶¶ [0002]-[0016], ¶¶ [0035]-[0037], ¶ [0079], FIGS. 1A-1C; Kavalieros729, ¶ [0001], ¶ [0017], ¶ [0046], FIG. 14; Koutny207, ¶ [0017], ¶ [0084], ¶ [0099], ¶ [0101], FIG. 6A; Kwon360, ¶ [0017], ¶ [0019], ¶ [0020], Figs. 3(c), 4; Liu article, 836-839, Figs. 1, 3, 6, 7; Maeda455, ¶¶ [0003]-[0009], ¶¶ [0011]-[0020], ¶ [0062], ¶¶ [0078]-[0087], ¶ [0092], ¶ [0095], ¶ [0097], ¶ [0098], ¶¶ [0102]-[0110], FIGS. 9, 10, 21-27; Mistry2007 article, 247-250, Figs. 2, 5; Mistry2007 Presentation, 4, 5, 7, 10, 14, 15a-15j; Miyashita476, ¶ [0025], ¶ [0027], ¶ [0033], ¶ [0038], ¶ [0046], ¶ [0048], ¶ [0051], ¶ [0052], ¶ [0058], ¶ [0059], ¶¶ [0069]-[0073], ¶ [0079], ¶ [0093], FIGS. 1E-5I; Murthy482, 4:32-34; Murthy556, 5:16-23-28, 11:45-12:8; Natarajan article, 1-3; Shifren983, ¶ [0014], FIGS. 6, 7.

A second MIS transistor with a second sidewall spacer formed on a side surface of the second gate electrode, *see, e.g.*, ’425 patent at 10:17-40, 12:13-29, 15:6-23, 15:40-51, 18:44-53, 19:5-22, FIGS. 1B-7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:14-22, 2:61-62, FIGS. 8B-10C; Ghani article, at 978, Figs. 1, 4, 5 (incorporated by reference in the ’425 patent); Luo article, at 489-90, Fig. 1 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 4-38 through 4-40, 4-42 through 4-52, 4-54 through 4-57, 5-10 through 5-14, 6-14 through 6-16, 8-2, Tbls. 4.6.1, 8.1.3, Figs. 4.5.10 through 4.5.12, 4.6.1 through 4.6.7, 4.6.9 through 4.6.11, 4.7.1, 5.3.3 through 5.3.7, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Stratix_IV_Report, 3-70; James TSMC article; Baik820 ¶ [0026], ¶ [0042], FIGS. 1B-1I, 4A-5E; Bohr683 ¶ [0005], ¶ [0008], ¶ [0012], ¶¶ [0014]-[0017], ¶¶ [0019]-[0023], ¶¶ [0030]-[0032], ¶¶ [0036]-[0037], ¶ [0040], ¶ [0043], ¶ [0045], ¶ [0047], FIGS. 2-8; Chen179 ¶ [0002], ¶ [0004], ¶ [0007], ¶ [0020], ¶ [0022], ¶ [0024], FIGS. 1A-1D; Chen729 ¶ [0001], ¶ [0004], ¶¶ [0014]-[0016], ¶¶ [0018]-[0019], ¶¶ [0020]-[0022], FIGS. 1-6; Cheng810 ¶ [0019], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0061]-[0062], ¶¶ [0076]-[0077], FIGS. 4j, 5i; Doris784, ¶ [0019], ¶ [0028], ¶ [0036], ¶ [0038], ¶ [0050], FIGS. 14, 15; Hatada776, Abstract, ¶ [0026], ¶ [0034], ¶ [0039], ¶ [0041], ¶ [0047], ¶¶ [0091]-[0092], ¶ [0135], ¶ [0140], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶¶ [0030]-[0031], ¶ [0035], ¶ [0041], FIGS. 7B, 11A, 13; James 90nm article, at 73, Fig. 5; Ke984, ¶ [0018], FIG. 10; Lee870, ¶ [0045], FIGS. 4, 5; Ogura844, ¶ [0022], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, ¶ [0051], ¶ [0070], ¶¶ [0095]-[0097], ¶ [0124], FIGS. 12, 21; Wang906, ¶ [0039], FIG. 16; Wu922, ¶¶ [0017]-[0018], ¶ [0024], ¶ [0028], ¶¶ [0038]-[0039], ¶ [0043], FIGS. 7, 14; Yamasaki170, ¶ [0065], FIGS. 31A-

31B; Quirk & Serda, at 311-312, FIGS. 12.1, 12.12-12.14; Bohr article, Fig. 2; ITRS_2007_FEP, at 20, 27, 30, 34, 38, Tbls. FEP4a, FEP4b, Fig. FEP1; Alvarez069, ¶ [0021], ¶ [0040], ¶ [0041], ¶ [0063], FIGS. 5-11; Chuang243, 2:27-31, 3:10-12, 5:15-6:32, FIGS. 1G-1I; Fischer208, ¶ [0036], ¶ [0049], ¶ [0060], ¶ [0066], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5A-5I, 8; Fujimoto807, Abstract, ¶¶ [0022]-[0025], ¶ [0031], ¶ [0032], ¶ [0034], ¶ [0035], ¶ [0037], ¶ [0044], ¶¶ [0058]-[0067], ¶ [0073], ¶¶ [0081]-[0093], FIGS. 1B-4C, 5B-7C, 8B-10D; Jung104, ¶¶ [0002]-[0016], ¶¶ [0035]-[0037], ¶ [0079], FIGS. 1A-1C; Kavalieros729, ¶ [0001], ¶ [0017], ¶ [0023], ¶ [0046], FIG. 14; Koutny207, ¶¶ [0018]-[0020], ¶ [0085], ¶ [0089], ¶ [0099], FIGS. 3I, 3J, 6A; Kwon360, ¶ [0017], Fig. 3(c); Liu article, 836-839, Figs. 1, 3, 6, 7; Maeda455, ¶¶ [0003]-[0009], ¶¶ [0011]-[0020], ¶ [0062], ¶¶ [0078]-[0087], ¶ [0092], ¶ [0097], ¶¶ [0102]-[0110], FIGS. 9, 10, 21-27; Mistry2007 Presentation, 15a-15j; Miyashita476, ¶ [0027], ¶ [0028], ¶ [0038], ¶ [0040], ¶ [0046], ¶ [0052], ¶ [0054], FIGS. 1J-5I; Murthy482, 4:32-34; Murthy556, 5:16-28, 11:45-12:8; Natarajan article, 1-3, Fig. 2; Shifren983, ¶ [0014], FIGS. 6, 7; Thompson Apr2004 article, 191-193, Fig. 1; Thompson Nov2004 article, 1790-1797, Fig. 2.

A second MIS transistor with a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, *see, e.g.*, ’425 patent at 4:53-65, 10:41-60, 12:29-49, 13:20-58, 15:6-23, FIGS. 1A-7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:23-27, 2:61-62, FIGS. 8A-10C; Ghani article, at 978, Fig. 5 (incorporated by reference in the ’425 patent); Luo article, at 489-90, Fig. 1 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent, including under Plaintiff’s apparent understanding of the claims. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-38, 4-42 through 4-45, 4-54 through 4-55, 4-57 through 4-58, 4-60 through 4-63, 5-8 through 5-11, Tbls. 1.6.1, 4.6.1, Figs. 4.5.10, 4.6.1, 4.6.2, 4.6.9, 4.6.10, 4.7.1, 4.7.2, 4.8.1 through

4.8.3, 5.3.1 through 5.3.4, 6.2.2 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 3 (same); Tyagi article, at 245, Fig. 1 (same); James 65/45 article, at 76, Fig. 1(a) (same); James 65/45 article, at 79-80, Fig. 7 (describing Intel_E5410); Stratix_IV_Report, 3-70; James TSMC article; Baik820 ¶¶ [0004]-[0006], ¶¶ [0009]-[0013], ¶ [0023], ¶¶ [0025]-[0027], ¶¶ [0033]-[0035], ¶ [0039], ¶ [0042], ¶¶ [0050]-[0052], ¶¶ [0055]-[0057], FIGS. 1A-1I, 5A-5F; Bohr683 ¶¶ [0004]-[0005], ¶ [0008], ¶¶ [0012]-[0013], ¶ [0015], ¶¶ [0018]-[0021], ¶¶ [0036]-[0037], FIGS. 1-8; Chen179, at Abstract, ¶¶ [0002]-[0004], ¶¶ [0006]-[0007], ¶ [0016], ¶¶ [0019]-[0023], FIGS. 1A-1D; Chen729 ¶ [0012], ¶ [0014], ¶ [0017], ¶¶ [0019]-[0023], FIG. 6; Cheng810 ¶ [0014], ¶ [0018], ¶ [0020], ¶ [0030], FIGS. 1D-1F; Cheng817, ¶¶ [0033]-[0037], ¶ [0056], ¶ [0060], ¶ [0066], ¶ [0072], ¶ [0075], ¶ [0081], FIGS. 4j, 5i; Doris784, ¶ [0029], ¶ [0038], FIGS. 14, 15; Hatada776, ¶ [0026], ¶ [0034], ¶ [0042], ¶ [0049], ¶ [0089], ¶ [0093], ¶¶ [0107]-[0108], ¶¶ [0126]-[0127], ¶¶ [0138]-[0139], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823, ¶ [0029], ¶ [0032], FIGS. 7B, 11A, 13; James 90nm article, at 73, Fig. 5; Ke984, ¶ [0017], ¶¶ [0019]-[0021], FIG. 10; Lee870, ¶ [0045], FIGS. 4, 5; Ogura844, ¶¶ [0020]-[0021], ¶ [0023], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, ¶¶ [0070]-[0071], ¶ [0124], FIGS. 12, 21; Wang906, ¶ [0023], ¶¶ [0038]-[0039], FIG. 16; Wu922, ¶¶ [0023]-[0024], ¶ [0033], ¶ [0035], ¶ [0039], ¶¶ [0042]-[0043], ¶ [0048], ¶ [0052], ¶ [0054], FIGS. 7, 8, 14, 15; Yamasaki170, ¶ [0054], ¶ [0058], ¶¶ [0063]-[0064], ¶ [0067], FIGS. 31A-31B; Sun article, at 16; Quirk & Serda, at 311-312, FIGS. 12.1, 12.12-12.14; Bohr article, at 1-3, Fig. 2; ITRS_2007_PIDS, at 6, 14-16, 24-27, Tbls. PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, PIDS3d; ITRS_2007_FEP, at 26-27, 30, 32-34, Tbls. FEP4a, FEP4b, Figs. FEP1, FEP3; Alvarez069, ¶¶ [0020]-[0022], ¶ [0041], ¶ [0042], ¶ [0066], FIGS. 8-11; Chuang243, Abstract, 1:51-67, 2:39-56, 3:40-42, 3:49-54, 5:15-38, 5:58-6:32, FIGS. 1G-1I; Fischer208, See also Fischer208, ¶¶ [0004]-[0007], ¶ [0014], ¶ [0015], ¶¶ [0022]-[0024], ¶¶ [0030]-[0034], ¶

[0037], ¶ [0040], ¶¶ [0046]-[0048], ¶¶ [0060]-[0066], ¶¶ [0093]-[0096], ¶¶ [0100]-[0102], FIGS. 1, 5A-5I, 8; Fujimoto807, Abstract, ¶ [0002], ¶ [0003], ¶ [0022], ¶ [0035], ¶ [0058], ¶ [0060], ¶ [0081], ¶ [0083], FIGS. 1A-10D; Jung104, ¶¶ [0002]-[0016], ¶¶ [0035]-[0037], ¶ [0079], FIGS. 1A-1C; Kavalieros729, ¶ [0001], ¶ [0017], ¶ [0026], ¶ [0046], FIG. 14; Komoda article, 217-220, Tbl. 1, Figs. 2, 3, 17; Koutny207, ¶ [0035], ¶ [0048], ¶ [0049], ¶ [0083], ¶ [0086], ¶ [0087], ¶ [0094], ¶ [0099], FIG. 6A; Kwon360, Abstract, ¶ [0007], ¶ [0008], ¶ [0016], ¶ [0017], ¶ [0021], Figs. 3(c); Liu article, 836-839, Figs. 1, 3, 4, 6-9; Maeda455, ¶¶ [0011]-[0020], ¶ [0029], ¶ [0042], ¶ [0048], ¶ [0079], ¶¶ [0083]-[0091], ¶¶ [0102]-[0109], FIGS. 9, 10, 23-27; Mistry2007 article, 247-250, Figs. 5, 7, 8, 11, 13, 15; Mistry2007 Presentation, 15a-15j, 17, 18, 20, 22, 26; Miyashita476, Abstract, ¶ [0014], ¶ [0015], ¶ [0017], ¶ [0021], ¶¶ [0026]-[0033], ¶¶ [0038]-[0048], ¶¶ [0054]-[0057], ¶ [0061], ¶ [0062], ¶¶ [0078]-[0093], FIGS. 5G-5I; Murthy482, 4:32-34; Murthy556, 5:16-2, 11:45-12:8; Natarajan article, 1-3, Figs. 3, 4, 7, 9, 10; Shifren983, Abstract, ¶¶ [0001]-[0003], ¶ [0011], ¶¶ [0015]-[0021], ¶ [0024], ¶ [0025], FIGS. 2-7; Thompson Apr2004 article,. 191-193, Fig. 1; Thompson Nov2004 article, 1790-1797, FIG. 2.

A second MIS transistor with the stress insulating film being formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region, *see, e.g.*, ’425 patent at 4:53-65, 13:66-14:9, 15:6-23, 16:26-30, 18:61-67, 19:10-39, FIGS. 6B, 7B, was also well-known before the ’425 patent, *see, e.g.*, *id.* at 1:15-56, 2:57-62, 3:5-9, FIG. 10C; Ghani article, at 978, Figs. 5, 6 (incorporated by reference in the ’425 patent); Luo article, at 489, Figs. 1, 2 (same). The prior art is replete with teachings that confirm this admission in the ’425 patent. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-7, 4-16 through 4-17, 4-36, 4-38 through 4-41, 4-43 through 4-48, 4-53 through 4-58, 5-9 through 5-13, 6-9 through 6-10, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.3.1, 8.2.1, Figs. 4.3.9, 4.3.10, 4.5.8, 4.5.10 through 4.5.13, 4.6.1 through

4.6.4, 4.6.8 through 4.6.11, 4.7.1, 4.7.2, 5.3.2 through 5.3.6, 6.1.10, 6.1.11, 6.2.4 through 6.2.6 (describing Intel_425_Product); Stratix_IV_Report, 3-70; James TSMC article; Bai article, at 657-58, Figs. 3, 4 (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); Baik820 ¶¶ [0001]-[0009], ¶¶ [0010]-[0013], ¶¶ [0023]-[0040], ¶¶ [0042]-[0046], ¶¶ [0049]-[0058], FIGS. 1H-1I, 5E-5F; Bohr683, at Title, Abstract, ¶¶ [0006]-[0007], ¶ [0009], ¶ [0011], ¶¶ [0022]-[0036], ¶¶ [0038]-[0041], ¶¶ [0043]-[0048], ¶ [0050], FIGS. 6, 8; Chen179, at Title, Abstract, ¶¶ [0002]-[0004], ¶¶ [0006]-[0007], ¶ [0013], ¶ [0016], ¶¶ [0019]-[0025], FIGS. 1A-1D; Chen729 ¶[0001], ¶ [0006], ¶ [0009], ¶¶ [0022]-[0023], FIG. 6; Cheng810 Abstract, ¶¶ [0001]-[0002], ¶ [0009], ¶ [0013], ¶¶ [0024]-[0030], ¶ [0032], FIGS. 1D-1F; Cheng817, ¶¶ [0002]-[0003], ¶ [0030], ¶ [0070], ¶ [0084], FIGS. 4j, 5i; Doris784, ¶ [0005], ¶ [0008], ¶ [0013], ¶ [0029], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 14, 15; Hsu823, ¶ [0003], ¶¶ [0013]-[0014], ¶ [0024], ¶¶ [0036]-[0037], FIGS. 7B, 11A, 13; James 90nm article, at 73, Fig. 5; Ke984, ¶ [0030], FIG. 10; Lee870, at Abstract, ¶ [0002], ¶¶ [0016]-[0022], ¶¶ [0028]-[0030], ¶¶ [0037]-[0038], ¶¶ [0049]-[0051], ¶¶ [0054]-[0058], ¶¶ [0060]-[0064], ¶ [0067], ¶ [0069], FIGS. 4, 5; Ogura844, ¶ [0033], ¶¶ [0058]-[0061], FIGS. 1I, 1M, 4A-4B; Saito825, ¶ [0080], ¶ [0120], ¶ [0124], FIGS. 12, 21; Wu922, ¶ [0005], ¶ [0025], ¶ [0036], ¶ [0044], FIGS. 7, 14; Yamasaki170, ¶ [0013], ¶ [0016], ¶ [0067], FIGS. 31A-31B; Morin article, at 355-356, 358, 360-361, 367, Tbl. I, Figs. 1, 2, 8, 20; Bohr article, at 1-3, Figs. 1, 2; ITRS_2007_PIDS, at 27; ITRS_2007_FEP, at 1, 29-30, Figs. FEP4, FEP5; Alvarez069, Abstract, ¶ [0001], ¶¶ [0007]-[0009], ¶¶ [0020]-[0035], ¶ [0043], ¶¶ [0047]-[0055], ¶¶ [0057]-[0059] ¶¶ [0061]-[0070], ¶ [0073]-[0074], ¶¶ [0080]-[0083], TBL 1, FIGS. 1, 4, 9-13; Chuang243, 1:47-50, 2:35-38, 3:16-18, 3:23-27, 5:28-38, 5:46-6:9, 6:15-23, 6:58-61, FIG. 1I; Fischer208, ¶ [0034], ¶ [0038], ¶ [0067], ¶ [0099], FIGS. 1, 5F-5I, 7E, 8; see generally Jung104;

see also Jung104, Abstract, ¶ [0002], ¶ [0007], ¶¶ [0012]-[0014], ¶¶ [0016]-[0018], ¶ [0029], ¶ [0035], ¶ [0036], ¶¶ [0048]-[0063], ¶ [0070], ¶ [0083], ¶ [0084], ¶ [0089], ¶ [0090], ¶ [0092], ¶ [0094], ¶ [0099], ¶¶ [0102]-[0130], TBLS. IV-VI, FIG. 1C, 2, 4A-14B; Kavalieros729, ¶ [0001], ¶ [0017], ¶ [0026], ¶ [0046]; FIG. 14; Komoda article, 217-220, Tbl. 1, Figs. 2, 3, 17; Koutny207, ¶ [0028], ¶ [0036], ¶ [0107], ¶ [0108], FIG. 6A; Liu article, 836-839, Tbls. I, II, Figs. 1-7; Maeda455, ¶¶ [0006], ¶ [0020], ¶ [0027], ¶¶ [0034]-[0038], ¶¶ [0042]-[0045], ¶¶ [0049]-[0050], ¶¶ [0083]-[0091], ¶¶ [0102]-[0109], FIGS. 9, 10, 23-27; Thompson Apr2004 article, 191-193, Fig. 1; Thompson Nov2004 article, 1790-179, Figs. 2, 5, 12, 13.

In sum, by the time the application for the ’425 patent was filed, strain-engineered MISFETs as claimed were well known because all the above was well known in the art before the earliest listed priority date for the ’425 patent, and a POSITA would have found it obvious to combine any and/or all of the above features to create a semiconductor device, comprising: a first MIS transistor, wherein: the first MIS transistor includes: a first gate insulating film formed on a first active region in a semiconductor substrate, a first gate electrode formed on the first gate insulating film, a first sidewall spacer formed on a side surface of the first gate electrode, a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region, and a stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress, an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode, a first stress-relief film is formed in a space between the silicon compound layer and the first

sidewall spacer, the first stress-relief film is formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and the first stress-relief film is not in direct contact with the side surface of the first gate electrode, including such a semiconductor device (1) further comprising: a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer, (2) wherein the first stress-relief film is formed on a side surface of the silicon compound layer, (3) wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer, (4) wherein the first MIS transistor is a p-type MIS transistor, the first stress is a compressive stress, and the second stress is a tensile stress, or (5) further comprising: a second MIS transistor, wherein: the second MIS transistor includes: a second gate insulating film formed on a second active region in the semiconductor substrate, a second gate electrode formed on the second gate insulating film, a second sidewall spacer formed on a side surface of the second gate electrode, a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer, and the stress insulating film formed on the second active region to cover the second gate electrode, the second sidewall spacer, and the second source/drain region.

A POSITA would have logically and predictably consulted all the references together to design a strain-engineered MISFET. Further, the general background knowledge described above and below would have provided the basis for combining any number of known MOSFET design features together. All these MOSFET design features were already known in the art, and a POSITA would have expected that combining any or all of these features to yield predictable results, would have found it obvious to substitute one known feature for another to obtain predictable results,

would have found it obvious to use known techniques to improve similar devices in the same way, would have found it obvious to apply a known technique to a known device that was ready for improvement to yield predictable results, would have found it obvious to try different combinations of device features because the techniques were known alternatives, would have found it obvious to try improving a semiconductor device, and would have reasonably expected to succeed because all these features were already known and combined previously in various ways. With respect to the prior art references in Exhibits 425-01 through 425-21, a POSITA would have been motivated to combine any of the references identified as prior art to the ’425 patent and would have reasonably expected to succeed for the reasons provided above and for additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar MISFET device structures within relevant timeframes, and the teachings of any one reference are applicable to other references in the same field.

Second, a POSITA would have been motivated to combine teachings from references that disclose certain specific features—e.g., epitaxial SiGe pMIS source/drain regions that extend above the substrate surface, stress insulating films (e.g., tensile contact etch stop layers, also known as CESLs) covering both nMIS and pMIS transistors, stress-relief films to alleviate stress caused by a stress insulating film, silicide source/drain and gate contact layers, and/or inner and outer sidewall spacers (including inner sidewall spacers with an L-shaped cross-section)—with teachings from other references that relate to similar MISFETs because all such references identified herein for the ’425 patent teach contemporaneously well-known and mutually compatible features of MISFETs, including epitaxial SiGe pMIS source/drain regions that extend above the substrate surface, stress insulating films (e.g., tensile contact etch stop layers, also known

as CESLs) covering both nMIS and pMIS transistors, stress-relief films to alleviate stress caused by a stress insulating film, silicide source/drain and gate contact layers, and/or inner and outer sidewall spacers (including inner sidewall spacers with an L-shaped cross-section). Moreover, well-known contemporaneous commercial embodiments (not to mention a litany of research articles, patents, and other disclosures) demonstrate a reasonable likelihood of success in doing so. *See, e.g.*, Mistry2007 article; Mistry2007 presentation; James 65/45 article; James 90nm article; D920_Report; Bai article; Tyagi article; Thompson Nov2004 article; Thompson Apr2004 article; James TSMC article; Natarajan article.

A POSITA would have also been motivated and reasonably expected to succeed when attempting to replace and/or combine a reference's exact set of materials, components, or configurations in a particular MOSFET device structure with other materials, components, and configurations used in similar MOSFET device structures for all the reasons provided above and below. Such modifications would have been a simple addition or substitution of one known element to yield predictable results because such features were already well known in the art. The addition or substitution of one component, material, or configuration would not have materially changed the principle of operation for any reference in such a combination of teachings because the constituent references use similar device features for similar purposes: designing and making MISFETs, including strain-engineered MISFETs.

A POSITA would have found it obvious to combine such prior-art features (e.g., epitaxial SiGe pMIS source/drain regions that extend above the substrate surface, stress insulating films (e.g., tensile contact etch stop layers, also known as CESLs) covering both nMIS and pMIS transistors, stress-relief films to alleviate stress caused by a stress insulating film, silicide source/drain and gate contact layers, and/or inner and outer sidewall spacers (including inner

sidewall spacers with an L-shaped cross-section)) according to known methods to yield predictable results.[24] A POSITA would have been motivated to combine these teachings, and to make related additions or substitutions, because all of these MISFET device structures, materials, and configurations were widely known and used. Accordingly, a POSITA would have reasonably expected to succeed given the considerations discussed above, the similarities in teachings, and because the claimed components and configurations of MISFET devices were well known at the time. Implementing any of the identified combinations and any necessary modifications would have involved no more than routine trial and error based on the teachings in the prior art.

As one example, to the extent that any of Cheng810, Doris784, Lee870, or Saito825 do not disclose the claimed "first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer, and which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region," a POSITA would have found it obvious to combine it with, e.g., Intel_425_Product, TSMC_425_Product, Baik820, Bohr683, Chen179, Chen729, Cheng817, Chidambarrao205, Chuang243, Fischer208, Fujimoto807, Fukutome203, Hatada776, Hsu823, Maeda455, Miyashita476, Murthy482, Murthy556, Kavalieros729, Ke984, Kwon360, Ogura844, Shifren983, Shimamune398, Wang906, Wu922, Yamasaki170, James 90nm article, James 65/45 article, Mistry2007 article, Mistry2007 presentation, Thompson Apr2004 article, Thompson Nov2004 article, Yasutake article, Tyagi article, Natarajan article, and/or Bai article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that

[24] A POSITA would have understood that these were all suitable design choices and also would have understood the benefits and tradeoffs of each design choice. There would have been no unexpected results from any particular combination of these design choices.

disclose known options for improving the hole mobility and accompanying device performance in p-type MISFETs. *See, e.g.*, D920_Report, at 1-6, 1-8, 4-39 through 4-40, 4-42, 4-46 through 4-48, 4-53, 4-56, 4-60 through 4-61, 5-12 through 5-13, 6-12 through 6-16, Tbls. 1.6.1, 4.6.1, Figs. 4.5.11, 4.5.12, 4.6.3, 4.6.4, 4.6.8, 4.6.11, 4.8.1, 5.3.5, 5.3.6, 6.2.2 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); James 65/45 article, at 79-80, Figs. 6, 7 (describing Intel_E5410); James TSMC article, at 8-9, Fig. 17 (describing TSMC_425_Product); Mistry2007 article, at 248-49, Figs. 5, 6; Mistry2007 presentation, at 14, 15a-15j, 16, 19, 35; Baik820, at Abstract, ¶¶ [0008]-[0013], ¶¶ [0028]-[0032], ¶¶ [0042]-[0046], ¶ [0049], FIGS. 1C-1I, 4A-5F; Bohr683, at Title, Abstract, ¶¶ [0022]-[0035], ¶ [0039], ¶ [0041], ¶¶ [0043]-[0046], ¶ [0050], FIGS. 3-6, 8; Bohr article, at 1-3, Figs. 1, 2; Chen179 ¶¶ [0021]-[0022], FIGS. 1A-1D; Chen729, at Abstract, ¶ [0014], ¶¶ [0019]-[0022], FIGS. 1, 5, 6; Cheng817, ¶¶ [0002]-[0003], ¶¶ [0022]-[0023], ¶ [0036], ¶ [0044], ¶ [0046], ¶ [0052], ¶¶ [0064]-[0065], ¶ [0069], ¶¶ [0079]-[0080], ¶ [0083], ¶¶ [0093]-[0094], ¶ [0101], FIGS. 1, 2, 3e-3n, 4d-4j, 5d-5i, 6d-6i, 7; Chidambarrao205, at Abstract, ¶¶ [0003]-[0004], ¶¶ [0053]-[0061], FIGS. 1-3, 4C-4F; Chuang243, at 2:32-34, 3:13-15, 5:28-6:23, FIGS. 1H-1I; Fujimoto807, at Abstract, ¶¶ [0013]-[0018], ¶¶ [0064]-[0074], ¶¶ [0087]-[0092], FIGS. 2C-4C, 6C-7C, 9D-10D; Fukutome203, at Abstract, ¶¶ [0004]-[0019], ¶¶ [0054]-[0055], ¶ [0074], ¶¶ [0085]-[0104], ¶¶ [0110]-[0111], ¶ [0115], ¶¶ [0121]-[0126], ¶¶ [0138]-[0146], ¶¶ [0157]-[0162], ¶¶ [0168]-[0177], ¶¶ [0185]-[0191], ¶¶ [0199]-[0201], ¶ [0206], ¶ [0240], ¶¶ [0248]-[0249], FIGS. 5D-5G, 8A-8C, 9C-9D, 11D-11E, 12C-12D, 13D-13E, 14A-14B, 16; Hatada776, at Abstract, ¶¶ [0004]-[0019], ¶¶ [0069]-[0070], ¶¶ [0097]-[0113], ¶¶ [0118]-[0121], ¶¶ [0130]-[0133], ¶ [0141], ¶ [0145], ¶¶ [0156]-[0157], ¶ [0172], FIGS. 1, 2C-3, 4E-4F, 5E-5F, 6G-6I, 7F-8; Hsu823, ¶ [0002], ¶ [0028],

¶¶ [0032]-[0033], ¶¶ [0038]-[0039], FIGS. 7A, 7B, 11A, 13; Maeda455, ¶¶ [0002]-[0005], ¶ [0018], ¶ [0029], ¶ [0042], ¶ [0048], ¶ [0102], ¶¶ [0105]-[0109], FIGS. 23-27; Miyashita476, ¶¶ [0048]-[0051], ¶¶ [0058]-[0061], ¶¶ [0078]-[0079], FIGS. 1S-1Y, 3A-3D, 5A-5I; Murthy482, 1:41-2:15, 4:39-7:10, 8:6-9:63, FIGS. 2-8; Murthy556, at 4:34-67, 6:60-9:9, 9:58-11:30, FIGS. 2, 6-14; Kavalieros729, at Abstract, ¶¶ [0001]-[0002], ¶¶ [0024]-[0025], ¶ [0043], FIGS. 4-13; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶ [0006], ¶ [0016], ¶¶ [0020]-[0021], ¶ [0023], ¶ [0032], FIG. 10; Kwon360, at Abstract, ¶¶ [0001]-[0009], ¶¶ [0015]-[0024], Figs. 1-4; Ogura844, at Abstract, ¶¶ [0004]-[0011], ¶¶ [0023]-[0031], ¶¶ [0053]-[0055], FIGS. 1E-1M, 3A-4B; Shifren983, at Abstract, ¶¶ [0002]-[0003], ¶ [0011], ¶¶ [0015]-[0020], ¶¶ [0024]-[0026], FIGS. 2-7; Shimamune398 at Abstract, ¶¶ [0004]-[0013], ¶¶ [0019]-[0025], ¶¶ [0078]-[0147], ¶¶ [0157]-[0164], FIGS. 1-7, 8C-10C, 12A-14C; Wang906, ¶¶ [0002]-[0008], ¶ [0011], ¶ [0017], ¶ [0027], ¶¶ [0029]-[0032], ¶¶ [0040]-[0042], FIGS. 7-16; Wu922, at Abstract, ¶ [0005], ¶ [0009], ¶¶ [0020]-[0021], ¶ [0031], ¶¶ [0040]-[0041], ¶ [0050], ¶¶ [0056]-[0058], FIGS. 3-8, 11-15; Yamasaki170, at Abstract, ¶¶ [0002]-[0010], ¶¶ [0035]-[0036], ¶¶ [0040]-[0047], ¶¶ [0058]-[0062], ¶ [0066], ¶¶ [0068]-[0082], ¶¶ [0085]-[0089], ¶¶ [0091]-[0092], ¶ [0095], ¶¶ [0099]-[0100], FIGS. 2A, 6A-19, 23A-43; ITRS_2007_PIDS, at 16, 26, 27, 56, Tbl. PIDS1a, PIDS2a, PIDS2b, PIDS3a, PIDS3b, PIDS3c, Figs. PIDS5, PIDS10; ITRS_2007_FEP, at 1-3, 10-13, 16, 17, 19-20, 29, 33 n.1, 35, 58-59, Tbl. FEP1, Figs. FEP1-FEP5; James 90nm article, at 73-74, Fig. 6; Thompson Apr2004 article, at 191-93, Fig. 1; Thompson Nov2004 article, at 1790-96, Figs. 2-7, 10, 13; Sun article, at 1-4, 7-16, 21, Figs. 5-8, 11, 12; Yasutake article, at 48, Figs. 1, 5, 6, 9-11; Natarajan article, at 1, Fig. 2.

Further, to the extent that any of Cheng810, Doris784, Lee870, or Saito825 do not disclose "a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the

first source/drain region which includes the silicon compound layer," as claimed, a POSITA would have found it obvious for the same reasons to combine it with, e.g., Alvarez069, Baik820, Bohr683, Chen179, Cheng810, Cheng817, Chuang243, Doris784, Hsu823, Jung104, Ke984, Lee870, Ogura844, James 90nm article, Komoda article, Liu article, and/or Thompson Nov2004 article, thereby resulting in a combination that includes this claimed feature.

As another example, to the extent that any of Intel_425_Product, TSMC_425_Product, Chen729, Cheng810, Hatada776, Saito825, Shimamune398, Wang906, Wu922, or Yamasaki170 do not disclose the claimed "stress insulating film which is formed on the first active region to cover the first gate electrode, the first sidewall spacer, and the first source/drain region, and which causes a second stress opposite to the first stress," a POSITA would have found it obvious to combine it with, e.g., Alvarez069, Baik820, Bohr683, Chen179, Cheng810, Cheng817, Chuang243, Doris784, Fischer208, Hsu823, Jung104, Ke984, Lee870, Ogura844, James 90nm article, Komoda article, Liu article, and/or Thompson Nov2004 article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for improving the electron mobility and accompanying device performance in n-type MISFETs. *See, e.g.*, Alvarez069, at Abstract, ¶ [0001], ¶¶ [0007]-[0009], ¶ [0018], ¶¶ [0020]-[0035], ¶¶ [0047]-[0055], ¶¶ [0057]-[0070], ¶¶ [0073]-[0074], ¶¶ [0080]-[0083], TBL 1, FIGS. 1, 4, 9-13; Baik820, at Abstract, ¶¶ [0001]-[0010], ¶¶ [0029]-[0032], ¶ [0039], ¶¶ [0043]-[0049], ¶¶ [0056]-[0057], FIGS. 1F-1I, 5C-5F; Bohr683, at Abstract, ¶ [0002], ¶¶ [0024]-[0039], ¶¶ [0043]-[0050], FIGS. 4-6, 8; Chen179, at Abstract, ¶¶ [0002]-[0006], ¶¶ [0009]-[0011], ¶ [0013], ¶ [0015], ¶ [0019], ¶¶ [0021]-[0023], ¶ [0035], ¶¶ [0037]-[0039], FIGS. 1A-1D, 3D-3E; Cheng810, at Abstract, ¶¶ [0001]-[0010], ¶ [0013], ¶¶ [0024]-[0030], ¶ [0032], FIGS. 1D-1F, 2;

Cheng817, ¶¶ [0002]-[0003], ¶¶ [0022]-[0023], ¶ [0030], ¶ [0036], ¶ [0044], ¶ [0052], ¶ [0065], ¶ [0070], ¶ [0080], ¶ [0084], ¶ [0094], ¶¶ [0098]-[0099], ¶ [0101], Figs. 1, 3n, 4j, 5i, 6i, 7; Chuang243, at 1:47-50, 2:32-38, 3:13-18, 3:23-27, 5:28-38, 5:46-57, 6:3-9, 6:15-23, 6:58-61, , FIGS. 1H-1I; Doris784, at Abstract, ¶¶ [0005]-[0013], ¶¶ [0016]-[0017], ¶¶ [0029]-[0030], ¶¶ [0032]-[0035], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 1, 2, 3(b), 14, 15; Hsu823, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0023]-[0026], ¶¶ [0032]-[0034], ¶¶ [0036]-[0039], FIGS. 3, 7B, 10-13; Jung104, at Abstract, ¶ [0036], ¶ [0090], ¶¶[0099]-[0100], ¶¶ [0104]-[0130], TBLS. IV-VI, FIGS. 1B-1C, 8A, 10A, 11A, 12A, 13A, 14A, 15; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0020]-[0021], ¶ [0027], ¶¶ [0030]-[0031], FIGS. 8-10; Koutny207, ¶¶ [0107]-[0108], ¶ [0110], FIG. 6A; Lee870, at Abstract, ¶¶ [0001]-[0015], ¶¶ [0021]-[0022], ¶¶ [0028]-[0038], ¶ [0043], ¶¶ [0054]-[0064], ¶¶ [0066]-[0067], FIGS. 4, 5; Ogura844, at Abstract, ¶¶ [0004]-[0009], ¶ [0026], ¶ [0033], ¶¶ [0053]-[0055], FIGS. 1I-1M, 3A-4B; James 90nm article, at 73-74, Figs. 5, 6; Komoda article, at 217-18, Tbl. 1, Figs. 2, 17; Liu article, at 836-37, Tbls. I, II, Figs. 1-7; Morin article, at 355-56, 358, 361, Tbl. 1, Figs. 1, 2, 8, 9; Thompson Nov2004 article, at 1790-96, Figs. 2, 5(c), 6, 8, 9, 12, 13.

As another example, to the extent that any of Intel_425_Product, TSMC_425_Product, Chen729, Cheng810, Hatada776, Saito825, Shimamune398, Wang906, or Wu922 do not disclose that "the stress insulating film formed on the second active region . . . cover[s] the second gate electrode, the second sidewall spacer, and the second source/drain region," as claimed, a POSITA would have found it obvious to combine it with, e.g., Alvarez069, Baik820, Bohr683, Chen179, Cheng810, Cheng817, Chuang243, Doris784, Fischer208, Hsu823, Ke984, Lee870, Ogura844, Yamasaki170, James 90nm article, Komoda article, Liu article, and/or Thompson Nov2004 article, thereby resulting in a combination that includes this claimed feature, because the constituent

references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for improving the electron mobility and accompanying device performance in n-type MISFETs. *See, e.g.*, Alvarez069, at Abstract, ¶ [0001], ¶¶ [0007]-[0009], ¶ [0018], ¶¶ [0020]-[0035], ¶¶ [0047]-[0055], ¶¶ [0057]-[0070], ¶¶ [0073]-[0074], ¶¶ [0080]-[0083], TBL 1, FIGS. 1, 4, 9-13; Baik820, at Abstract, ¶¶ [0001]-[0010], ¶¶ [0029]-[0032], ¶ [0039], ¶¶ [0043]-[0049], ¶¶ [0056]-[0057], FIGS. 1F-1I, 5C-5F; Bohr683, at Abstract, ¶ [0002], ¶¶ [0024]-[0039], ¶¶ [0043]-[0050], FIGS. 4-6, 8; Chen179, at Abstract, ¶¶ [0002]-[0006], ¶¶ [0009]-[0011], ¶ [0013], ¶ [0015], ¶ [0019], ¶¶ [0021]-[0023], ¶ [0035], ¶¶ [0037]-[0039], FIGS. 1A-1D, 3D-3E; Cheng810, at Abstract, ¶¶ [0001]-[0010], ¶ [0013], ¶¶ [0024]-[0030], ¶ [0032], FIGS. 1D-1F, 2; Cheng817, ¶¶ [0002]-[0003], ¶¶ [0022]-[0023], ¶ [0030], ¶ [0036], ¶ [0044], ¶ [0052], ¶ [0065], ¶ [0070], ¶ [0080], ¶ [0084], ¶ [0094], ¶¶ [0098]-[0099], ¶ [0101], Figs. 1, 3n, 4j, 5i, 6i, 7; Chuang243, at 1:47-50, 2:32-38, 3:13-18, 3:23-27, 5:28-38, 5:46-57, 6:3-9, 6:15-23, 6:58-61, , FIGS. 1H-1I; Doris784, at Abstract, ¶¶ [0005]-[0013], ¶¶ [0016]-[0017], ¶¶ [0029]-[0030], ¶¶ [0032]-[0035], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 1, 2, 3(b), 14, 15; Hsu823, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0023]-[0026], ¶¶ [0032]-[0034], ¶¶ [0036]-[0039], FIGS. 3, 7B, 10-13; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0020]-[0021], ¶ [0027], ¶¶ [0030]-[0031], FIGS. 8-10; Koutny207, ¶¶ [0107]-[0108], ¶ [0110], FIG. 6A; Lee870, at Abstract, ¶¶ [0001]-[0015], ¶¶ [0021]-[0022], ¶¶ [0028]-[0038], ¶ [0043], ¶¶ [0054]-[0064], ¶¶ [0066]-[0067], FIGS. 4, 5; Yamasaki170 ¶ [0067], FIGS. 31A-31B; Ogura844, at Abstract, ¶¶ [0004]-[0009], ¶ [0026], ¶ [0033], ¶¶ [0053]-[0055], FIGS. 1I-1M, 3A-4B; James 90nm article, at 73-74, Figs. 5, 6; Komoda article, at 217-18, Tbl. 1, Figs. 2, 17; Liu article, at 836-37, Tbls. I, II, Figs. 1-7; Morin article, at 355-56, 358, 361, Tbl. 1, Figs. 1, 2, 8, 9; Thompson Nov2004 article, at 1790-96, Figs. 2, 5(c), 6, 8, 9, 12, 13.

As another example, to the extent that any of Intel_425_Product, TSMC_425_Product, Chen729, Cheng810, Hatada776, Saito825, Shimamune398, Wang906, Wu922, Yamasaki170 do not disclose that "the first MIS transistor is a p-type MIS transistor, the first stress is a compressive stress, and the second stress is a tensile stress," as claimed, a POSITA would have found it obvious to combine it with, e.g., Alvarez069, Baik820, Bohr683, Chen179, Cheng810, Cheng817, Chuang243, Doris784, Fischer208, Hsu823, James 90nm article, Jung104, Ke984, Lee870, Ogura844, Komoda article, Liu article, and/or Thompson Nov2004 article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for improving the electron mobility and accompanying device performance in n-type MISFETs. *See, e.g.*, Alvarez069, at Abstract, ¶ [0001], ¶¶ [0007]-[0009], ¶ [0018], ¶¶ [0020]-[0035], ¶¶ [0047]-[0055], ¶¶ [0057]-[0070], ¶¶ [0073]-[0074], ¶¶ [0080]-[0083], TBL 1, FIGS. 1, 4, 9-13; Baik820, at Abstract, ¶¶ [0001]-[0010], ¶¶ [0029]-[0032], ¶ [0039], ¶¶ [0043]-[0049], ¶¶ [0056]-[0057], FIGS. 1F-1I, 5C-5F; Bohr683, at Abstract, ¶ [0002], ¶¶ [0024]-[0039], ¶¶ [0043]-[0050], FIGS. 4-6, 8; Chen179, at Abstract, ¶¶ [0002]-[0006], ¶¶ [0009]-[0011], ¶ [0013], ¶ [0015], ¶ [0019], ¶¶ [0021]-[0023], ¶ [0035], ¶¶ [0037]-[0039], FIGS. 1A-1D, 3D-3E; Cheng810, at Abstract, ¶¶ [0001]-[0010], ¶ [0013], ¶¶ [0024]-[0030], ¶ [0032], FIGS. 1D-1F, 2; Cheng817, ¶¶ [0002]-[0003], ¶¶ [0022]-[0023], ¶ [0030], ¶ [0036], ¶ [0044], ¶ [0052], ¶ [0065], ¶ [0070], ¶ [0080], ¶ [0084], ¶ [0094], ¶¶ [0098]-[0099], ¶ [0101], Figs. 1, 3n, 4j, 5i, 6i, 7; Chuang243, at 1:47-50, 2:32-38, 3:13-18, 3:23-27, 5:28-38, 5:46-57, 6:3-9, 6:15-23, 6:58-61, , FIGS. 1H-1I; Doris784, at Abstract, ¶¶ [0005]-[0013], ¶¶ [0016]-[0017], ¶¶ [0029]-[0030], ¶¶ [0032]-[0035], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 1, 2, 3(b), 14, 15; Hsu823, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0023]-[0026], ¶¶ [0032]-[0034], ¶¶ [0036]-[0039], FIGS. 3, 7B, 10-13;

Jung104, at Abstract, ¶ [0036], ¶ [0090], ¶¶[0099]-[0100], ¶¶ [0104]-[0130], TBLS. IV-VI, FIGS. 1B-1C, 8A, 10A, 11A, 12A, 13A, 14A, 15; Ke984, at Abstract, ¶¶ [0002]-[0003], ¶¶ [0020]-[0021], ¶ [0027], ¶¶ [0030]-[0031], FIGS. 8-10; Koutny207, ¶¶ [0107]-[0108], ¶ [0110], FIG. 6A; Lee870, at Abstract, ¶¶ [0001]-[0015], ¶¶ [0021]-[0022], ¶¶ [0028]-[0038], ¶ [0043], ¶¶ [0054]-[0064], ¶¶ [0066]-[0067], FIGS. 4, 5; Ogura844, at Abstract, ¶¶ [0004]-[0009], ¶ [0026], ¶ [0033], ¶¶ [0053]-[0055], FIGS. 1I-1M, 3A-4B; James 90nm article, at 73-74, Figs. 5, 6; Komoda article, at 217-18, Tbl. 1, Figs. 2, 17; Liu article, at 836-37, Tbls. I, II, Figs. 1-7; Morin article, at 355-56, 358, 361, Tbl. 1, Figs. 1, 2, 8, 9; Thompson Nov2004 article, at 1790-96, Figs. 2, 5(c), 6, 8, 9, 12, 13.

As another example, to the extent that any of Cheng810, Doris784, Hatada776, Hsu823, Ke984, Lee870, or Saito825 do not disclose "an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode," as claimed, a POSITA would have found it obvious to combine it with, e.g., Intel_425_Product, TSMC_425_Product, Baik820, Bohr683, Chen179, Chen729, Cheng817, Chuang243, Fujimoto807, Fischer208, Fukutome203, Miyashita476, Murthy482, Murthy556, Kavalieros729, Kwon360, Ogura844, Shifren983, Shimamune398, Wang906, Wu922, Yamasaki170, James 90nm article, James 65/45 article, Mistry2007 article, Mistry2007 presentation, Thompson Apr2004 article, Thompson Nov2004 article, Yasutake article, Tyagi article, Natarajan article, and/or Bai article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for improving the hole mobility and accompanying device performance in p-type MISFETs by implementing epitaxial SiGe source/drain regions. *See, e.g.*, D920_Report, at 4-39 through 4-40, 4-46 through 4-48, 4-56,

5-13, 6-13 through 6-16, Figs. 4.5.11, 4.5.12, 4.6.3, 4.6.4, 4.6.11, 5.3.6, 6.2.3 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Fig. 4 (same); Tyagi article, at 245, Fig. 2 (same); James 65/45 article, at 76, Fig. 1(b) (same); James 65/45 article, at 79-80, Fig. 6 (describing Intel_E5410); James TSMC article, at 8-9, Fig. 17 (describing TSMC_425_Product); Mistry2007 article, at 248-49, Fig. 6; Mistry2007 presentation, at 15b-15j, 16, 19; Baik820 ¶¶ [0028]-[0032], ¶¶ [0042]-[0046], ¶ [0049], FIGS. 1D-1I, 4B-5F; Bohr683, at Title, Abstract, ¶¶ [0022]-[0035], ¶ [0039], ¶ [0041], ¶¶ [0043]-[0046], ¶ [0050], FIGS. 3-6, 8; Bohr article, at 1-3, Figs. 1, 2; Chen179 ¶¶ [0021]-[0022], FIGS. 1A-1D; Chen729 ¶¶ [0020]-[0022], FIG. 6; Cheng817, ¶ [0022], ¶ [0036], ¶ [0044], ¶ [0052], ¶ [0065], ¶ [0069], ¶ [0080], ¶ [0083], ¶ [0094], ¶ [0101], FIGS. 1, 2, 3f-3n, 4e-4j, 5e-5i, 6e-6i, 7; Chuang243, at 2:32-34, 3:13-15, 5:28-6:23, FIGS. 1H-1I; Fujimoto807 ¶¶ [0014]-[0017], ¶ [0065], ¶ [0068], ¶¶ [0071]-[0074], ¶ [0088], ¶ [0091], FIGS. 2D-4C, 6D-7C, 10A-10D; Fukutome203 ¶¶ [0097]-[0104], ¶¶ [0110]-[0111], ¶ [0115], ¶¶ [0124]-[0126], ¶¶ [0144]-[0146], ¶¶ [0158]-[0162], ¶¶ [0175]-[0177], ¶¶ [0186]-[0191], ¶¶ [0199]-[0201], ¶ [0206], ¶ [0240], FIGS. 5E-5G, 8B-8C, 9D, 11E, 12D, 13E, 14B, 16; Miyashita476, ¶¶ [0050]-[0051], ¶ [0061], ¶ [0079], FIGS. 1U-1Y, 3A-3D, 5A-5I; Murthy482, 5:34-6:30, FIGS. 3, 4, 8; Murthy556, at 3:4-14, 3:47-49, 4:34-67, 7:64-8:22, 8:59-9:9, 9:58-11:30, FIGS. 2, 7-14; Kavalieros729, at Title, Abstract, ¶ [0025], ¶ [0040], ¶ [0043], FIGS. 5-13; Kwon360 ¶¶ [0007]-[0009], ¶¶ [0015]-[0024], Figs. 1-4; Ogura844 ¶ [0011], ¶¶ [0026]-[0031], ¶¶ [0053]-[0055], FIGS. 1F-1M, 3A-4B; Shifren983 ¶ [0011], ¶¶ [0016]-[0020], ¶¶ [0024]-[0026], FIGS. 3-7; Shimamune398 at Abstract, ¶¶ [0019]-[0020], ¶ [0031], ¶ [0049], ¶ [0053], ¶¶ [0156]-[0161], FIGS. 1-4, 8D-9, 12C, 13B, 13C, 14C; Wang906, ¶ [0011], ¶ [0027], ¶¶ [0030]-[0031], ¶¶ [0040]-[0042], FIGS. 9-16; Wu922 ¶ [0021], ¶ [0041], FIGS. 4-7, 12-14; Yamasaki170 ¶ [0007], ¶ [0036], ¶¶ [0040]-[0041], ¶¶ [0045]-[0047], ¶ [0053], ¶¶ [0060]-[0062], ¶ [0066],

¶ [0068], ¶¶ [0072]-[0077], ¶¶ [0079]-[0082], ¶¶ [0085]-[0089], ¶ [0099], FIGS. 2A, 7A-12B, 15-16, 25A-31B, 34-35, 38A-41B; James 90nm article, at 73-74, Fig. 6; Thompson Apr2004 article, at 191-93, Fig. 1; Thompson Nov2004 article, at 1790-91, Figs. 2-5; Yasutake article, at 48, Figs. 1, 5, 6, 9-11; Natarajan article, at 1, Fig. 2.

As another example, to the extent that any of Intel_425_Product, TSMC_425_Product, Baik820, Bohr683, Chen179, Chen729, Hatada776, Hsu823, James 90nm article, Ogura844, Shimamune398, Wang906, Wu922, or Yamasaki170 do not disclose "a first stress-relief film [being] formed in a space between the silicon compound layer and the first sidewall spacer, the first stress-relief film [being] formed on the side surface of the first gate electrode with the first sidewall spacer interposed therebetween, and the first stress-relief film [being] not in direct contact with the side surface of the first gate electrode," as claimed, a POSITA would have found it obvious to combine it with, e.g., Alvarez069, Cheng810, Cheng817, Doris784, Lee870, Ke984, Koutny207, Kwon360, and/or Saito825, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for buffering strain from a tensile CESL film formed over a p-type MISFET to improve device performance. *See, e.g.*, Alvarez069, at Abstract, ¶ [0001]-[0009], ¶¶ [0018]-[0019], ¶¶ [0022]-[0032], ¶¶ [0034]-[0037], ¶¶ [0042]-[0045], ¶¶ [0047]-[0082], TBL. 1, FIGS. 1-4, 9-13; Cheng810 ¶¶ [0001]-[0008], ¶ [0013], ¶¶ [0022]-[0030], ¶ [0032], FIGS. 1B-1F, 2; Cheng817 ¶¶ [0002]-[0003], ¶ [0030], ¶ [0061], ¶¶ [0063]-[0064], ¶ [0066], ¶ [0070], ¶ [0078], ¶ [0081], ¶ [0084], ¶ [0099], ¶ [0101], FIGS. 4j, 5i, 7; Doris784, at Abstract, ¶¶ [0002]-[0013], ¶¶ [0031]-[0038], FIGS. 1, 2, 3(b), 6-15; Lee870, at Title, Abstract, ¶¶ [0001]-[0007], ¶ [0016], ¶ [0024], ¶¶ [0028]-[0038], ¶¶ [0042]-[0043], ¶¶ [0046]-[0058], ¶¶ [0061]-[0064], ¶¶ [0066]-[0067], FIGS. 2-6; Ke984, at Abstract,

¶ [0003], ¶ [0005], ¶¶ [0007]-[0009], ¶ [0014], ¶ [0027], ¶¶ [0030]-[0031], FIGS. 8-10; Koutny207 ¶¶ [0106]-[0108], FIG. 6A; Saito825 ¶¶ [0074]-[0076], ¶ [0078], ¶¶ [0082]-[0084], ¶ [0104]-[0119], ¶¶ [0125]-[0126], FIGS. 3, 6-12, 18-21. Moreover, a POSITA would have understood that when such a stress-relief film (like the ones Alvarez069, Cheng810, Cheng817, Doris784, Lee870, Ke984, Koutny207, and Saito825 disclose) is applied over the epitaxial source/drain regions of Intel_425_Product, TSMC_425_Product, Baik820, Bohr683, Chen179, Chen729, Hatada776, Hsu823, James 90nm article, Ogura844, Shimamune398, Wang906, Wu922, or Yamasaki170, then the resulting structure would satisfy this claimed feature because the stress-relief film would form in a space between the silicon compound layer and the gate sidewall spacers (e.g., an actual space created by facets of the silicon compound layer or another space formed during the principle reference's process flow, or simply by covering the silicon compound layer and gate sidewall spacers[25]).

As another example, to the extent that any of Intel_425_Product, TSMC_425_Product, Baik820, Bohr683, Chen179, Chen729, Hatada776, Hsu823, James 90nm article, Ogura844, Shimamune398, Wang906, Wu922, or Yamasaki170 do not disclose that "the first stress-relief film is formed on a side surface of the silicon compound layer," as claimed, a POSITA would have found it obvious to combine it with, e.g., Alvarez069, Cheng810, Cheng817, Doris784, Lee870, Ke984, Koutny207, Kwon360, and/or Saito825, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for buffering strain

[25] Under Plaintiff's apparent interpretation of the claim language, the claimed "first stress-relief film . . . formed space between the silicon compound layer and the first sidewall spacer" need not be formed in a "space" at all, and a silicon oxide buffer layer located underneath the stress insulating film satisfies the claim language. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 21. Although TSMC disagrees with such an interpretation, combinations involving Bohr683, Chen179, Hsu823, or Wang906 as the principle reference would satisfy this claim feature if applied.

from a tensile CESL film formed over a p-type MISFET to improve device performance. *See, e.g.*, Alvarez069, at Abstract, ¶ [0001]-[0009], ¶¶ [0018]-[0019], ¶¶ [0022]-[0032], ¶¶ [0034]-[0037], ¶¶ [0042]-[0045], ¶¶ [0047]-[0082], TBL. 1, FIGS. 1-4, 9-13; Cheng810 ¶¶ [0001]-[0008], ¶ [0013], ¶¶ [0022]-[0030], ¶ [0032], FIGS. 1B-1F, 2; Cheng817 ¶¶ [0002]-[0003], ¶ [0030], ¶ [0061], ¶¶ [0063]-[0064], ¶ [0066], ¶ [0070], ¶ [0078], ¶ [0081], ¶ [0084], ¶ [0099], ¶ [0101], FIGS. 4j, 5i, 7; Doris784, at Abstract, ¶¶ [0002]-[0013], ¶¶ [0031]-[0038], FIGS. 1, 2, 3(b), 6-15; Lee870, at Title, Abstract, ¶¶ [0001]-[0007], ¶ [0016], ¶ [0024], ¶¶ [0028]-[0038], ¶¶ [0042]-[0043], ¶¶ [0046]-[0058], ¶¶ [0061]-[0064], ¶¶ [0066]-[0067], FIGS. 2-6; Ke984, at Abstract, ¶ [0003], ¶ [0005], ¶¶ [0007]-[0009], ¶ [0014], ¶ [0027], ¶¶ [0030]-[0031], FIGS. 8-10; Koutny207 ¶¶ [0106]-[0108], FIG. 6A; Saito825 ¶¶ [0074]-[0076], ¶ [0078], ¶¶ [0082]-[0084], ¶ [0104]-[0119], ¶¶ [0125]-[0126], FIGS. 3, 6-12, 18-21. Moreover, a POSITA would have understood that when such a stress-relief film (like the ones Alvarez069, Cheng810, Cheng817, Doris784, Lee870, Ke984, Koutny207, and Saito825 disclose) is applied over the epitaxial source/drain regions of Intel_425_Product, TSMC_425_Product, Baik820, Bohr683, Chen179, Chen729, Hatada776, Hsu823, James 90nm article, Ogura844, Shimamune398, Wang906, Wu922, or Yamasaki170, then the resulting structure would satisfy this claimed feature because the stress-relief film would form on a side surface of the compound silicon layer (e.g., the actual side surfaces of the silicon compound layer, or simply by covering the silicon compound layer[26]).

As another example, to the extent that either Chen729 or Wu922 does not disclose "a first silicide layer formed on the first gate electrode; and a second silicide layer formed on the first source/drain region which includes the silicon compound layer," as claimed, a POSITA would have

[26] Under Plaintiff's apparent interpretation of the claim language, the claimed "side surface of the silicon compound layer" may include an upper surface. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 25, 26. Although TSMC disagrees with such an interpretation, combinations involving Bohr683, Chen179, Hsu823, or Wang906 as the principle reference would satisfy this claim feature if applied.

found it obvious to combine it with, e.g., Intel_425_Product, TSMC_425_Product, Alvarez069, Baik820, Bohr683, Chen179, Cheng810, Cheng817, Doris784, Fischer208, Fujimoto807, Fukutome203, Hatada776, Hsu823, Ke984, Kwon360, Lee870, Maeda455, Miyashita476, Murthy482, Murthy556, Ogura844, Saito825, Shifren983, Shimamune398, Wang906, Yamasaki170, James 90nm article, Bai article, James 65/45 article, and/or Tyagi article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for reducing gate and source/drain contact resistance. *See, e.g.*, Alvarez069 ¶¶ [0029]-[0032], ¶[0037], ¶¶ [0044]-[0046], ¶¶ [0063]-[0064], ¶ [0068], ¶ [0073], FIGS. 3, 4, 8-10; Baik820 ¶¶ [0038]-[0040], ¶¶ [0055]-[0056], ¶ [0058], FIGS. 1H-1I, 5E-5F; Bohr683 ¶¶ [0036]-[0038], ¶ [0040], ¶ [0047], FIGS. 5-8; Chen179 ¶¶ [0007]-[0011], ¶¶ [0022]-[0025], ¶¶ [0027]-[0028], ¶¶ [0031]-[0034], ¶¶ [0039]-[0040], FIGS. 1A-2G, 3D-3E; Cheng810 ¶¶ [0003]-[0004], ¶ [0017], ¶ [0021], ¶ [0029], ¶ [0031], FIGS. 1A-1F; Cheng817 ¶ [0003], ¶ [0019], ¶ [0041], ¶ [0052], ¶ [0058], ¶ [0069], ¶ [0073], ¶ [0083], ¶ [0087], ¶ [0097], ¶ [0099], ¶ [0101], FIGS. 1, 2, 3n, 4i-4j, 5h-5i, 6h-6i, 7; Doris784 ¶ [0029], ¶ [0031], ¶ [0038], ¶ [0042], ¶ [0051], FIGS. 1, 2, 14, 15; Fujimoto807 ¶ [0017], ¶ [0031], ¶ [0068], ¶ [0074], ¶ [0091], FIGS. 3C, 4B-4C, 7C, 10D; Fukutome203 ¶¶ [0103]-[0104], ¶ [0107], ¶¶ [0125]-[0126], ¶ [0130], FIGS. 5F-5G, 8C; Hatada776 ¶ [0109], ¶¶ [0120]-[0121], ¶ [0132], ¶ [0171], FIGS. 2F, 4F, 5F, 6I, 7H; Hsu823 ¶¶ [0034]-[0035], ¶¶ [0040]-[0041], FIGS. 8-13; Ke984, at Title, ¶ [0023], ¶ [0026], ¶¶ [0028]-[0029], FIGS. 7-10; Kwon360, at Abstract, ¶¶ [0001]-[0003], ¶¶ [0006]-[0009], ¶ [0011], ¶¶ [0014]-[0016], ¶ [0019], ¶¶ [0022]-[0024], Figs. 1, 2(e), 3(c), 4; Lee870 ¶ [0037], ¶¶ [0044]-[0045], FIGS. 1-6; Maeda455 ¶¶ [0005]-[0006], ¶ [0017], ¶ [0028], ¶ [0039], ¶ [0046], ¶ [0079], ¶ [0083], ¶ [0087], ¶ [0095], ¶¶ [0097]-[0101], ¶ [0107], ¶ [0110], FIGS. 1, 6-13, 16-20,

25-32; Miyashita476 ¶ [0079], FIGS. 5A-5H; Murthy482, at Abstract, 2:39-41, 2:66-3:13, 4:32-38, 7:11-9:63, FIGS. 4a-4c, 5-8; Murthy556, at 2:31-33, 2:37-41, 3:30-46, 8:52-55, 9:38-43, 9:58-11:15, FIGS. 2, 11-15; Ogura844, at Abstract, ¶ [0009], ¶ [0011], ¶ [0031], ¶ [0038], ¶¶ [0054]-[0055], ¶ [0058], FIGS. 1G-1M, 3A-4B; Saito825 ¶ [0024], ¶ [0026], ¶ [0055], ¶¶ [0077]-[0084], ¶ [0104], ¶ [0107], ¶¶ [0117]-[0120], ¶¶ [0122]-[0123], FIGS. 3, 8-12, 20-21; Shifren983, at Abstract, ¶ [0002], ¶ [0009], ¶ [0011], ¶ [0019], ¶¶ [0024]-[0026], FIGS. 6, 7; Shimamune398 ¶ [0020], ¶¶ [0024]-[0025], ¶ [0081], ¶ [0088], ¶ [0120], ¶ [0125], ¶¶ [0128]-[0130], ¶ [0143], ¶ [01], FIGS. 2, 3, 8E; Wang906 ¶ [0024], ¶ [0040], FIGS. 16; Yamasaki170 ¶ [0008], ¶¶ [0040]-[0041], ¶¶ [0046]-[0047], ¶¶ [0050]-[0051], ¶¶ [0066]-[0068], ¶¶ [0073]-[0074], ¶¶ [0077]-[0079], ¶ [0082], ¶ [0097], FIGS. 12A-12B, 30A-31B, 39A-40B, 41A-42B; ITRS_2007_FEP, at 1, 4, 9, 16, 21, 22, 25, 27-30, 34, Figs. FEP1; ITRS_2007_PIDS, at 16, 26; James 90nm article, at 73-74, Figs. 5, 6; D920_Report, at 1-6, 1-8, 4-38 through 4-40, 4-42 through 4-49, 4-53, 4-56, 5-10 through 5-13, 6-11, 6-14 through 6-16, 8-3, Tbls. 1.6.1, 4.6.1, 8.2.1, Figs. 4.5.10 through 4.5.12, 4.5.11, 4.6.1 through 4.6.4, 4.6.8, 4.6.11, 5.3.3 through 5.3.6, 6.2.1, 6.2.4 through 6.2.6 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); Tyagi article, at 245, Figs. 1, 2 (same); James TSMC article, at 8, Fig. 17 (describing TSMC_425_Product); Quirk & Serda, at 303, 308, 309-12, 321-22, 331, Tbl. 12.4, Figs. 12.9 through 12.13.

As another example, to the extent that any of Bohr683, Doris784, Hsu823, Ogura844, or Saito825 do not disclose that "the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape, and an outer sidewall spacer formed on the inner sidewall spacer," as claimed, a POSITA would have found it obvious to combine it with, e.g., Intel_425_Product, TSMC_425_Product, Baik820,

Chen179, Chen729, Cheng810, Cheng817, Chidambarrao205, Fujimoto807, Hatada776, Jung104, Ke984, Kwon360, Lee870, Murthy556, Shimamune398, Wang906, Wu922, Yamasaki170, James 90nm article, Bai article, James 65/45 article, Tyagi article, Thompson Apr2004 article, and/or Thompson Nov2004 article, thereby resulting in a combination that includes this claimed feature, because the constituent references disclose such a feature, and a POSITA would have been motivated to consult references that disclose known options for controlling the doing profiles of source/drain regions to attain desired operating properties and to avoid short-channel effects and current leakage, as well as to control the amount of stress transfer from the CESL to the channel and to minimize voids in the CESL and inter-layer dielectric ("ILD") films. *See, e.g.*, Baik820 ¶ [0026], ¶ [0042], FIGS. 1B-1I, 4A-5F; Chen179 ¶ [0022], ¶ [0027], ¶ [0036], FIGS. 1A-3E; Chen729 ¶ [0001], ¶ [0004], ¶¶ [0014]-[0016], ¶¶ [0018]-[0022], FIGS. 4-6; Cheng810 ¶¶ [0019]-[0020], FIGS. 1A-1F; Cheng817, at Abstract, ¶ [0017], ¶¶ [0020]-[0021], ¶ [0023], ¶ [0025], ¶ [0027], ¶ [0035], ¶¶ [0043]-[0045], ¶¶ [0048]-[0050], ¶ [0054], ¶¶ [0061]-[0064], ¶ [0066], ¶¶ [0076]-[0079], ¶ [0081], ¶¶ [0090]-[0093], ¶ [0095], ¶ [0097], ¶ 0099], ¶ [0101], FIGS. 1, 2, 3b-3n, 4b-4j, 5b-5i, 6b-6i, 7; Chidambarrao205, at Abstract, ¶¶ [0005]-[0009], ¶ [0012], ¶ [0015], ¶¶ [0020]-[0023], ¶ [0030], ¶ [0041], ¶¶ [0050]-[0055], ¶¶ [0060]-[0061], FIGS. 2, 3, 4B-4F; Fujimoto807, at Abstract, ¶¶ 0006]-[0008], ¶ [0013], ¶ [0016], ¶¶ [0022]-[0025], ¶¶ [0031]-[0032], ¶¶ [0034]-[0035], ¶ [0037], ¶¶ [0042]-[0044], ¶¶ [0058]-[0061], ¶ [0063], ¶¶ [0066]-[0067], ¶ [0073], ¶[0076], ¶¶ [0081]-[0084], ¶ [0087], ¶¶ [0089]-[0090], FIGS. 1B-3C, 5B-7C, 8B-10D; Hatada776, at Abstract, ¶¶ [0007]-[0009], ¶¶ [0091]-[0099], ¶¶ [0106]-[0108], ¶ [0111]-[0112], ¶ [0116], ¶ [0121], ¶¶ [0124]-[0127], ¶ [0130], ¶¶ [0135]-[0145], ¶¶ [0149]-[0170], ¶ [0175], FIGS. 2B-2F, 3, 4B-4F, 5B-5F, 6E-6I, 7D-7H, 8-12; Jung104 ¶ [0035], ¶ [0079], ¶ [0090], FIGS. 1A-1C; Ke984 ¶ [0018], ¶ [0021], FIGS. 4-10; Kwon360 ¶ [0005], ¶ [0017],

¶ [0024], Figs. 2(a), 2(b), 2(d)-3(c); Lee870 ¶¶ [0044]-[0045], FIGS. 1-6; Murthy556, at Abstract, 1:37-42, 1:54-55, 2:6-11, 2:21-23, 3:22-54, 4:43-46, 6:22-7:16, 7:53-63, 8:10-22, 9:10-57, 10:28-31, 10:42-55, FIGS. 2, 8-15; Shimamune398, at Abstract, ¶ [0008], ¶ [0010], ¶¶ [0075]-[0076], ¶¶ [0096]-[0097], ¶ [0107], ¶¶ [0112]-[0114], ¶ [0118], ¶¶ [0121]-[0122], ¶ [0130], ¶ [0143], ¶ [0159], ¶ [0165], FIGS. 3-5D, 8B-9; Wang906 ¶ [0026], ¶¶ [0029]-[0031], ¶¶ [0033]-[0036], ¶ [0039], FIGS. 5-11, 15, 16; Wu922 ¶¶ [0017]-[0018], ¶¶ [0022]-[0025], ¶ [0028], ¶ [0034], ¶ [0037], ¶ [0039], ¶¶ [0042]-[0044], ¶ [0047], ¶ [0053], ¶¶ [0057]-[0058], FIGS. 1-4, 7-12, 14, 15; Yamasaki170 ¶ [0039], ¶¶ [0057]-[0058], ¶ [0065], ¶ [00], FIGS. 11A-12B, 22A-27B, 29A-31B, 39A-41B; James 90nm article, at 72-76, Figs. 1-3, 5, 6, 8, 9, 10(a), 10(b), 11, 12; D920_Report, at 4-38 through 4-40, 4-43 through 4-49, 4-54 through 4-56, 5-10 through 5-13, 6-14, Figs. 4.5.10 through 4.5.12, 4.6.1 through 4.6.4, 4.6.9 through 4.6.11, 5.3.3 through 5.3.6, 6.2.4 (describing Intel_425_Product); Bai article, at 657-58, Figs. 3, 4 (same); James 65/45 article, at 76, Figs. 1(a), 1(b) (same); Tyagi article, at 245, Figs. 1, 2 (same); James 65/45 article, at 76-79, Figs. 1(c), 2(a)-2(c), 3(a)-3(c), 4(a)-4(c); Thompson Apr2004 article, at 191, Fig. 1; Thompson Nov2004 article, at 1791, Figs. 2, 4; Bohr article, at 3, Fig. 2; Morin article, at 355-56, 366, Figs. 1, 2, 20; James TSMC article, at 8, Fig. 17 (describing TSMC_425_Product[27]).

Additional obviousness combinations of the references identified here are possible, and TSMC may rely on such combination(s) in this litigation. In particular, TSMC is currently unaware of Plaintiff's allegations with respect to the level of skill in the art and the qualifications of a POSITA. TSMC is also unaware of the extent, if any, to which Plaintiff may contend that

[27] Under Plaintiff's apparent interpretation of the claim language, the claimed "L shape" may include a "J" shape. *See* AICP's P.R. 3-1 Disclosures, Ex. H, at 28. Although TSMC disagrees with such an interpretation, combinations involving TSMC_425_Product would satisfy this claim feature if applied since the pFET sidewalls spacers in TSMC_425_Product resemble the pFET sidewall spacers in the accused products analyzed in AICP's infringement contentions.

limitations of the claims at issue are not disclosed in the prior art identified by TSMC as anticipatory, and the extent to which Plaintiff will contend that features not disclosed in the asserted patent specifications would have been known to a POSITA. And TSMC does not yet know how the Court will construe terms in the asserted claim. TSMC is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. TSMC reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

Additionally, TSMC incorporates by reference all positions and supporting materials it has filed in *inter partes* review Case No. IPR2025-00683 on file with the U.S. Patent Trial and Appeal Board and other IPR cases against the ’425 patent.

C. Invalidity Contentions Pursuant to P.R. 3-3(d)

Pursuant to P.R. 3-3(d), TSMC contends that certain Asserted Claims of the Patents- In-Suit are invalid under 35 U.S.C. § 112 because: (1) the claims lack adequate written description; (2) the claims are not enabled, and/or (3) the claims are indefinite. TSMC’s contentions that the following claims are invalid under 35 U.S.C. § 112 are made in the alternative and do not constitute, and should not be interpreted as, admissions regarding the construction or scope of the claims of the Patents-In-Suit, or that any of the claims of the Patents-In-Suit are not anticipated or rendered obvious by prior art. The following contentions, made pursuant to P.R. 3-3(d), are subject to revision and amendment pursuant to Federal Rule of Civil Procedure 26(e) and the Orders of record in this matter to the extent appropriate, e.g., in light of further investigation and discovery regarding the defenses, the Court’s construction of the claims at issue, and/or review and analysis of expert witnesses.

1. Enablement and Written Description

The asserted claims are invalid for failure to comply with the written description and enablement requirements because the Patents-in-Suit do not contain sufficient written description of the claimed invention and do not provide a sufficiently enabling disclosure. *See* 35 U.S.C. § 112. To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention at the time of filing the patent application. *See generally Ariad Pharm., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336 (Fed. Cir. 2010) (en banc). "To be enabling, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation." *MagSil Corp. v. Hitachi Global Storage Techs.*, 687 F.3d 1377, 1380-81 (Fed. Cir. 2012) (citation omitted). The specifications of the Patents-in-Suit do not adequately describe or enable the claimed inventions recited in the Asserted Claims.

The "enablement requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *Auto. Techs. Int'l, Inc. v. BMW of N. Am.*, 501 F.3d 1274, 1282 (Fed. Cir. 2007). A claimed invention may be invalid for lack of written description and non-enablement even if it was disclosed in the prior art: "It is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of an invention in order to constitute adequate enablement." *Genentech v. Novo Nordisk*, 108 F.3d 1361, 1366 (Fed. Cir. 1997). The patentee is "required to provide an adequate enabling disclosure in the specification; it cannot simply rely on the knowledge of a person of ordinary skill to serve as a substitute for the missing information in the specification." *Alza Corp. v. Andrx Pharms., LLC*, 603 F.3d 935, 940-41 (Fed. Cir. 2010). "A patentee who chooses broad claim language must make sure the broad claims are fully enabled." *Sitrick v. Dreamworks, LLC*, 516

F.3d 993, 999-1000 (Fed. Cir. 2008). As the Federal Circuit has explained:

> Enablement serves the dual function in the patent system of ensuring adequate disclosure of the claimed invention and of preventing claims broader than the disclosed invention. This important doctrine prevents both inadequate disclosure of an invention and overbroad claiming that might otherwise attempt to cover more than was actually invented. Thus, a patentee chooses broad claim language at the peril of losing any claim that cannot be enabled across its full scope of coverage.

Magsil Corp. and MIT v. Hitachi, 687 F.3d 1377, 1380-81 (Fed. Cir. 2012). "The specification must contain sufficient disclosure to enable an ordinarily skilled artisan to make and use the entire scope of the claimed invention at the time of filing." *Id.* at 1381-82.

TSMC contends that the specification does not provide sufficient written description and enablement for each of the claim limitations identified below, which identify grounds of invalidity for lack of enablement and written description with respect to the asserted claim and the limitations of the asserted claim, pursuant to Patent Rule 3-3(d). Where TSMC has identified a phrase as lacking written description and/or enablement, TSMC also contends that the subparts of the phrase lack written description and/or enablement within the context recited in the claim.

The following discussion includes the identification and discussion of claim terms and limitations lacking § 112 written description and enablement support. A more detailed basis for TSMC's written description and enablement defenses may be set forth in any expert report(s) on invalidity to be served by TSMC in accordance with the Court's Scheduling Order.

a. '227 Patent

Asserted claims 1, 2, 7, 8, and 14 of the '227 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the '227 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AICP in its infringement contentions:

- "wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall" (claim 1)

- "at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode" (claim 1)

- "the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween" (claim 1)

- "the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall" (claim 1)

- "part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode" (claim 1)

- "further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film" (claim 7)

- "wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film" (claim 8)

- "wherein the high dielectric constant gate insulating film is formed of a Hf based oxide" (claim 14)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the '227 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff's infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff's infringement contentions, the '227 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '227

patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

b. ’764 Patent

Asserted claims 1, 2, 3, 4, 5, 6, 11, 12, 13, 14, 15, 16, 17, 18, and 19 of the ’764 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the ’764 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AICP in its infringement contentions:

- “a second insulating sidewall formed on said each side surface of the gate electrode with the first insulating sidewall interposed therebetween” (claim 1)
- “wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall” (claim 1)
- “part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode” (claim 1)
- “further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film” (claim 2)
- “wherein the buffer insulating film is a silicon oxide film” (claim 3)
- “wherein the first insulating sidewall is an offset sidewall” (claim 4)
- “wherein the high dielectric constant gate insulating film is formed of a Hf based oxide” (claim 5)
- “wherein each side end portion of the high dielectric constant gate insulating film has a thickness of 2 nm or less” (claim 11)
- “wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the first insulating sidewall toward the gate electrode” (claim 12)
- “wherein a side surface of the high dielectric constant gate insulating film is located at a predetermined distance from a side end surface of the gate electrode toward the first insulating sidewall” (claim 13)
- “wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length” (claim 16)

- "wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length" (claim 17)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the '764 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff's infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff's infringement contentions, the '764 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '764 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

c. '686 Patent

Asserted claims 25-28 and 34 of the '686 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the '686 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AICP in its infringement contentions:

- "a first gate insulating film formed on a first active region in a semiconductor substrate;" (claim 25)
- "a first gate electrode including a second metal film formed on the first gate insulating film;" (claim 25)
- "first sidewall spacers formed on side surfaces of the first gate electrode, the first sidewall spacers being insulative; and" (claim 25)

- “a silicon nitride film formed, extending over the side surfaces of the first gate electrode on which the first sidewall spacers are formed and upper surfaces of regions located in the first active region laterally outside the first sidewall spacers,” (claim 25)

- “a second gate insulating film formed on a second active region in the semiconductor substrate;” (claim 25)

- “a second gate electrode including a first metal film formed on the second gate insulating film and a conductive film formed on the first metal film;” (claim 25)

- “second sidewall spacers formed on side surfaces of the second gate electrode, the second sidewall spacers being insulative; and” (claim 25)

- “the silicon nitride film formed, extending over the side surfaces of the second gate electrode on which the second sidewall spacers are formed and upper surfaces of regions located in the second active region laterally outside the second sidewall spacers,” (claim 25)

- “the first and second metal films are made of different metal materials,” (claim 25)

- “the silicon nitride film is not formed on any of upper surfaces of the first and second gate electrodes, and” (claim 25)

- “the silicon nitride film causes first stress in a gate length direction of a channel region in the first active region.” (claim 25)

- “the first metal film has a thickness smaller than that of the second metal film.” (claim 26)

- “the first and second metal films have different work functions.” (claim 27)

- “the silicon nitride film has a thickness smaller than that of the first gate electrode.” (claim 28)

- “source/drain regions formed in the second active region laterally outside the second sidewall spacers,” (claim 34)

- “wherein the source/drain regions include a SiGe layer which is formed in trenches provided in the second active region.” (claim 34)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the ’686 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff’s

infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff's infringement contentions, the '686 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '686 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

d. '180 Patent

Asserted claims 1, 2, 3, 5, 6, 11, 13, 14, 16, 17, 18, 19, 21, and 22 of the '180 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the '180 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AICP in its infringement contentions:

- "wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall" (claim 1)
- "an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode" (claim 1)
- "further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film" (claim 2)
- "wherein the buffer insulating film is a silicon oxide film" (claim 3)
- "wherein a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode" (claim 5)
- "wherein the high dielectric constant gate insulating film is formed of a Hf based oxide" (claim 6)
- "wherein a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less" (claim 11)

- "the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall" (claim 13)
- "the insulating sidewall has a double layer structure including an oxide film and a nitride film" (claim 14)
- "a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length" (claim 16)
- "a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length" (claim 17)
- "the end of the high dielectric constant gate insulating film located under the insulating sidewall has a tapered surface" (claim 21)
- "the high dielectric constant gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof" (claim 22)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the '180 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff's infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff's infringement contentions, the '180 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '180 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

e. '076 Patent

Asserted claims 1, 2, 3, 6, 7, 8, 10, 11, 12, and 13 of the '076 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the '076 patent fails to provide an adequate

written description or enablement of the following limitations, at least as those limitations are applied by AICP in its infringement contentions:

- "wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length" (claim 1)
- "an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode" (claim 1)
- "further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film" (claim 2)
- "wherein the gate insulating film is formed of a Hf based oxide" (claim 3)
- "wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall" (claim 7)
- "wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length" (claim 10)
- "wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface" (claim 11)
- "wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof" (claim 12)
- "wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length" (claim 13)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the '076 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff's infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff's infringement contentions, the '076 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '076

patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

f. ’779 Patent

Asserted claims 1 and 15 (including claims depending therefrom) of the ’779 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the ’779 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AICP in its infringement contentions:

- “a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate” (claim 1)
- “wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film, the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film” (claim 1)
- “the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer, the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer” (claim 1)
- “the first interface layer has a thickness larger than that of the second interface layer” (claim 1)
- “each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film” (claim 1)
- “each of the first and second high dielectric constant insulating films contains hafnium or zirconium” (claim 12)
- “the first and second high dielectric constant insulating films are equal in thickness” (claim 13)
- “the first and second gate electrodes are made of an identical material” (claim 14)
- “wherein an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor” (claim 15)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the ’779 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff’s infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff’s infringement contentions, the ’779 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff’s infringement contentions, the ’779 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

g. ’425 Patent

Asserted claims 1, 3-5, and 11 of the ’425 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the ’425 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AICP in its infringement contentions:

- “a first source/drain region of a first conductivity type which is formed in a trench provided in the first active region on a lateral side of the first sidewall spacer” (claim 1)
- “which includes a silicon compound layer causing a first stress in a gate length direction of a channel region in the first active region” (claim 1)
- “an uppermost surface of the silicon compound layer is located higher than a surface of the semiconductor substrate located directly under the first gate electrode” (claim 1)
- “a first stress-relief film is formed in a space between the silicon compound layer and the first sidewall spacer” (claim 1)
- “the first stress-relief film is not in direct contact with the side surface of the first gate electrode” (claim 1)

- “a first silicide layer formed on the first gate electrode” (claim 3)
- “a second silicide layer formed on the first source/drain region which includes the silicon compound layer” (claim 3)
- “wherein the first stress-relief film is formed on a side surface of the silicon compound layer” (claim 4)
- “wherein the first sidewall spacer includes an inner sidewall spacer which is formed on the side surface of the first gate electrode, and whose cross-section has an L shape” (claim 5)
- “a second source/drain region of a second conductivity type which is formed in the second active region on a lateral side of the second sidewall spacer” (claim 11)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the ’425 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff’s infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff’s infringement contentions, the ’425 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff’s infringement contentions, the ’425 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

TSMC reserves the right to supplement these contentions pursuant to Sections (c) and (d) of the Court’s Standing Order.

D. Document Production

Pursuant to Patent Rule 3-4, TSMC is concurrently producing the prior art identified in these Invalidity Contentions.

In addition, based on investigations to date, TSMC is making available for inspection source code, specifications, schematics, flow charts, artwork, formulas, or other documentation sufficient to show the operation of any aspects or elements of the Accused Instrumentalities identified by AICP in its P.R. 3-1(c) charts.

TSMC reserves the right to supplement these productions with additional documentation, in accordance with the Federal Rules of Civil Procedure, the Local Rules, the Court's orders and other applicable rules and statutes.

Dated: May 1, 2025

Respectfully Submitted,

/s/ Jennifer Truelove

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that counsel of record who are deemed to have consented to electronic services are being served with a copy of this document via email on May 1, 2025.

/s/ Nancy Lepore
Nancy Lepore