EXHIBIT 180-01: Invalidity of U.S. Patent No. 8,253,180 (the ’180 Patent) Based on *Kamata*

The following list illustrates certain grounds for invalidity based on:

- U.S. Publication 2002/0063299 to Kamata, et al. (“*Kamata*”), published May 30, 2002, is prior art to U.S. Patent No. 8,253,180 (the “’180 patent”) under at least pre-AIA 35 U.S.C. §102(b).

Kamata, including any material incorporated by reference into *Kamata*, anticipates at least claims 1-3, 5-6, 11, 13-14, 16-19, and 21-22 of the ’180 patent under pre-AIA 35 U.S.C. §102(b).

To the extent any limitation is found not to be expressly or inherently disclosed in *Kamata*, such a limitation would have been obvious either based on *Kamata* alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 180-02 through 180-15, because the ’180 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

In particular, any disclosures identified for each limitation of the ’180 patent in the aforementioned Exhibits may be combined with the disclosures of *Kamata* identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.[1]

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to

[1] Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

U.S. Patent No. 8,253,180	**Exemplary Disclosures Relevant to *Kamata***
Claim 1	
[1pre] A semiconductor device comprising:	*Kamata*, alone or in combination with one or more references, discloses or suggests a semiconductor device. For example: *Kamata* discloses the following at Title: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD *Kamata* discloses the following at Abstract: In the first aspect of the invention, a semiconductor device can effectively suppress the adverse short channel effect and the possible occurrence of junction leak current and has a low resistance diffusion layer to realize a short propagation delay time as a plurality of side wall films 4, 5 are formed at least in a part of the area between the gate electrode 3 and an elevated region 8 by laying a plurality of films in an appropriate order. *Kamata* discloses the following at ¶ 3: This invention relates to a semiconductor device and a method of manufacturing the same. More particularly, it relates to an MIS type semiconductor device having an elevated source/drain structure and a method of manufacturing the same. *Kamata* discloses the following at ¶ 8:

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	An first aspect of the present invention, there is provided a semiconductor device comprising: *Kamata* discloses the following at ¶ 32: FIGS. 1A and 1B are schematic cross sectional views of the first embodiment of the present invention, illustrating different steps (a) to (j) of a method of manufacturing an MIS type transistor having multilayer type side wall films and an elevated source/drain region raised vertically upwardly from the interface of the silicon substrate and the gate insulating film; *Kamata* discloses the following at ¶ 50: FIGS. 1A through 1B are schematic cross sectional views of the first embodiment of the present invention, illustrating different manufacturing steps thereof. *Kamata* discloses the following at ¶ 36: FIG. 5 shows schematic cross sectional views of the fourth embodiment of the present invention, illustrating different steps (a) to (c) of a method of manufacturing a transistor having an elevated source/drain region raised vertically upwardly from the interface of the silicon substrate and the gate insulating film and formed by means of a solid epitaxial growth process; *Kamata* discloses the following at ¶ 68, applying disclosures of first embodiment to fourth embodiment (applies throughout this claim chart):

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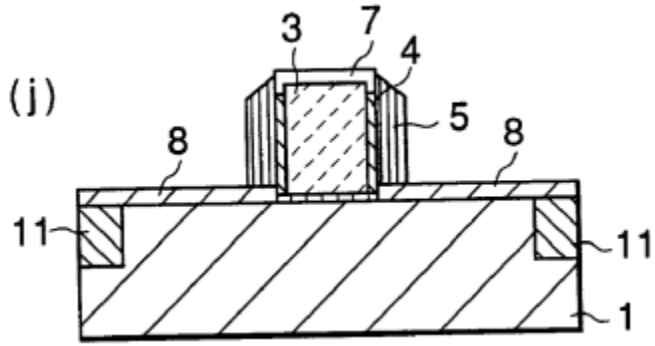
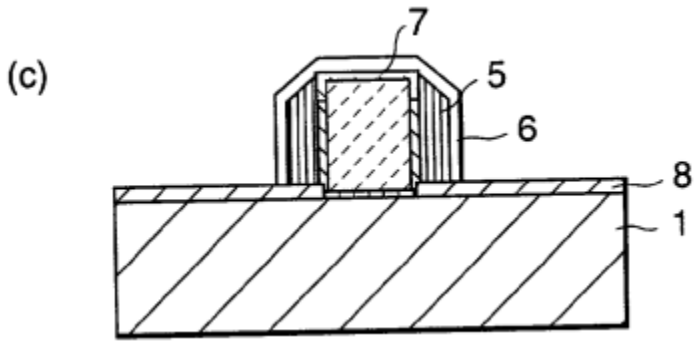
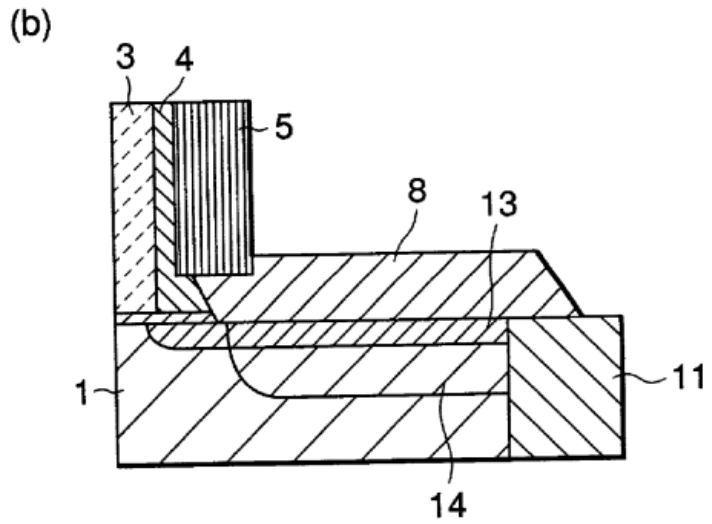
	FIGS. 5 shows the fifth embodiment of the present invention. This embodiment differs from the first embodiment only in that the first side wall film completely removed by etching in an area 4 d between the second side wall film 5 and the silicon substrate land also removed by etching in another area 4 c between the second side wall film 5 and the gate electrode 3 to reduce the film thickness if compared with the remaining part of the first side wall film. Otherwise, this embodiment is same as the first embodiment. Therefore, in FIG. 5(a) through (c), the parts that are same as or similar to those of the first embodiment are denoted respectively by the same reference symbols. *Kamata* discloses the following at ¶¶ 93-94, applying disclosures of first embodiment to ninth embodiment (applies throughout this claim chart): FIG. 10(a) and (b) shows the ninth embodiment of the present invention. Referring to the figure, a diffusion layer 14 is formed by ion implantation. After processing the gate electrode 3, an extention region 13 is formed by implanting impurities into the silicon substrate through the gate insulating film and annealing the epitaxially grown film in an ion implantation system (FIG. 10(a)). Then, as in the case of the first through eighth embodiments, a deep diffusion region 14 is formed by forming an elevated source/drain region 8 on the side wall film 5, introducing impurities into a region of the silicon substrate 1 located deeper than the extended region 13 by ion implantation and annealing the epitaxially grown layer (FIG. 10(b)). The diffusion layer formed in this wayq shows a low resistance to suppress the adverse short channel effect. In FIG. 10, the portions that are same as or similar to those FIGS. 1A through 2C are denoted respectively by the same reference symbols. In FIG. 10, reference symbol 11 denotes an element isolation zone.

	Kamata discloses the following at Figure 1B(j):  *Kamata* discloses the following at Figure 5(c):  *Kamata* discloses the following at Figure 10(b):

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	
[1A] a high dielectric constant gate insulating film formed on an active region in a substrate;	*Kamata*, alone or in combination with one or more references, discloses or suggests a high dielectric constant gate insulating film formed on an active region in a substrate. For example: *Kamata* discloses the following at ¶¶ 8-10: An first aspect of the present invention, there is provided a semiconductor device comprising: a silicon substrate; a gate insulating film formed on a surface of the silicon substrate;

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	Kamata discloses the following at ¶ 50: FIGS. 1A through 1B are schematic cross sectional views of the first embodiment of the present invention, illustrating different manufacturing steps thereof. Firstly, shallow trench isolation zones (STI) 11 are formed on a semiconductor substrate 1 made of silicon to define an element region 1 a (FIG. 1A(a)). Then, a gate electrode 3 is formed by depositing polycrystalline silicon (FIG. 1A(b)) and, after a lithography step, the gate electrode is processed by means of an anisotropic etching technique using plasma such as RIE (reactive ion etching (FIG. 1A(c)). Subsequently, the gate electrode is oxidized (to be referred to as post-gate oxidization step hereinafter) to produce a first side wall film 4 (FIG. 1A(d)). The surface layer that becomes a source region/a drain region is also oxidized in the post-gate oxidization step. Then, a silicon nitride film (Si_3N_4) 5 is deposited in a CVD (chemical vapor deposition) system (FIG. 1A(e)) and subsequently a silicon nitride film is formed only on the lateral side of the gate electrode by anisotropic etching using plasma (FIG. 1A(f)). Note that no problem arises if the gate insulating film and the silicon oxide film on the source region/drain region 8 are partly scraped off by the anisotropic etching using plasma. *Kamata* discloses the following at ¶¶ 52-53: The gate insulating film may be a silicon oxide film, a silicon nitride film, a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element. The film may be a single crystal film, a poly crystal film or an amorphous film such as TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ and Gd_2O_3. Furthermore, the film may be made of a mixture of SiO_2, TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ or Gd_2O_3, with Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr or Gd.

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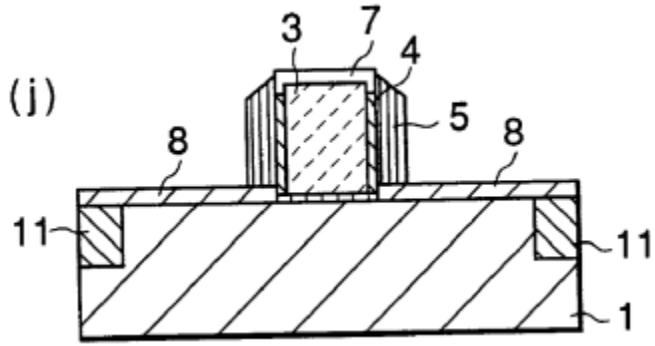
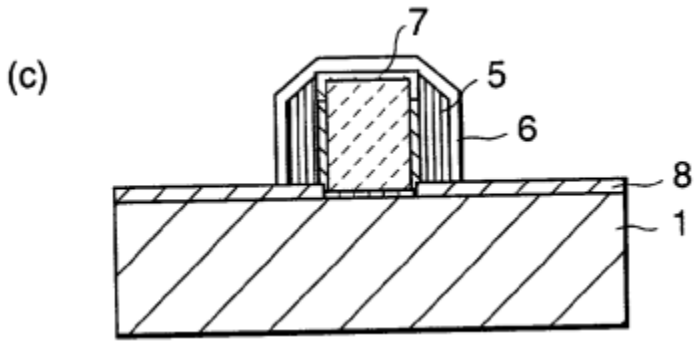
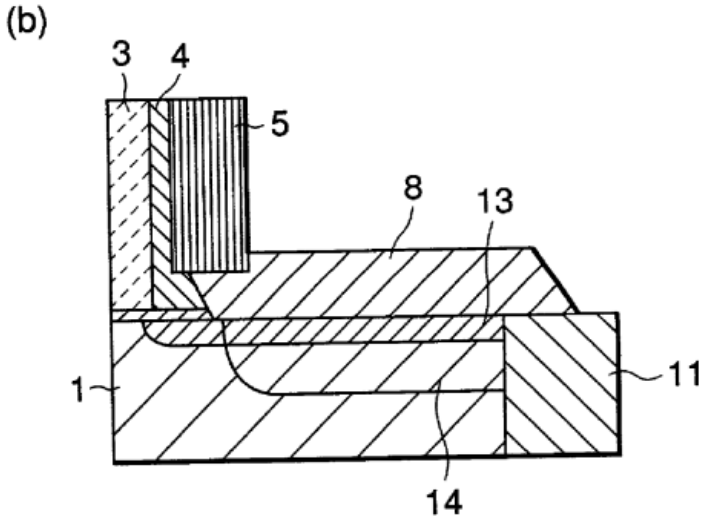
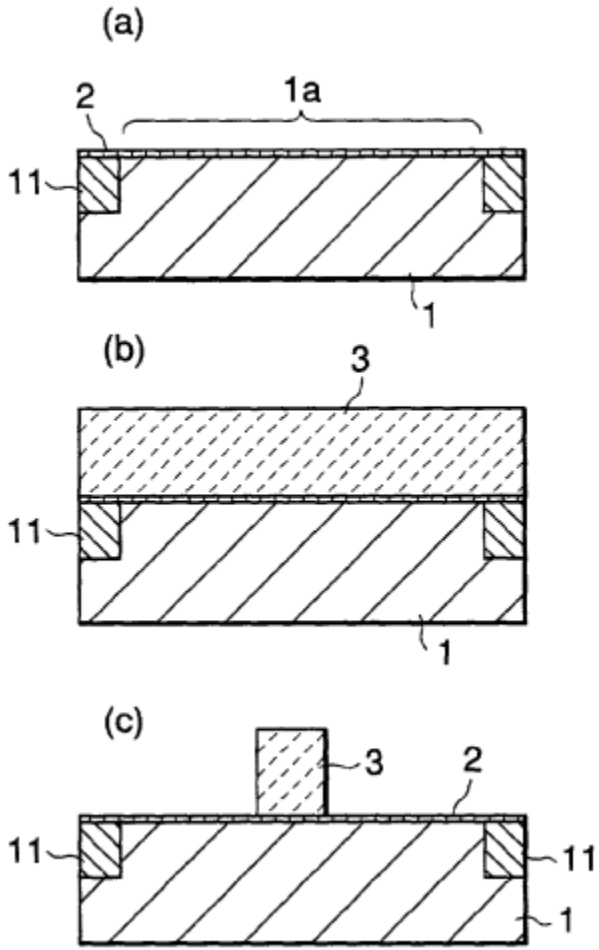
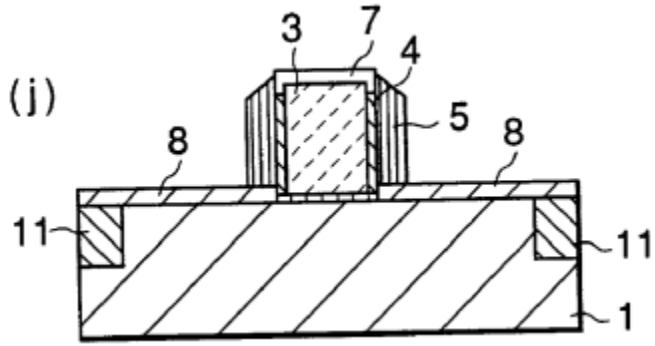
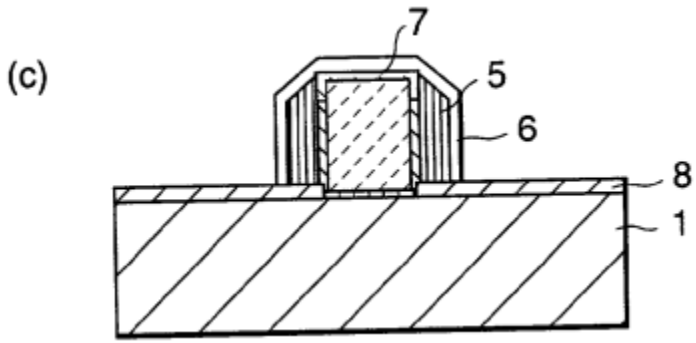
	Kamata discloses the following at ¶ 73: Note that length x in the above formula represents the distance between the end 2a of the gate insulating film 2 and the outer peripheral edge of the second side wall film 5. Otherwise, this embodiment is same as any of the above listed embodiments. *Kamata* discloses the following at ¶¶ 99-100: FIG. 12 shows the eleventh embodiment of the present invention. This embodiment differs from the tenth embodiment in that the side wall film is partly found also on the element isolation zone 11. The side wall film 5 is formed by following the steps of FIG. 1A through 1F as in the case of the first embodiment. The side wall film is made to show a large thickness and extend to or beyond the proximal end of the isolation zone 11 so that the edge 15 a of the side wall film may operate as eaves to cover the active region 1a. Then, the silicon oxide film is etched and an epitaxial growth process is conducted as in the first through sixth embodiments (FIG. 12(a)). *Kamata* discloses the following at ¶ 56: After forming the second side wall film 5 as shown in FIG. 1A(f), the silicon oxide films 2, 4 on the source/drain region 8 on the silicon substrate and on the gate electrode 3 are etched out by using dilute hydrofluoric acid (DHF). The part of the first side wall film located between the second side wall film and the silicon substrate is completely etched out in this step (FIG. 1B(g)). As a result of this etching step, a gap 10 a is produced between the surface of the silicon substrate and the end 5 a of the second side wall film 5 apart from the substrate. The film thickness of the part 4a of the first side wall film 4 is made equal to that of the remaining first side wall film.

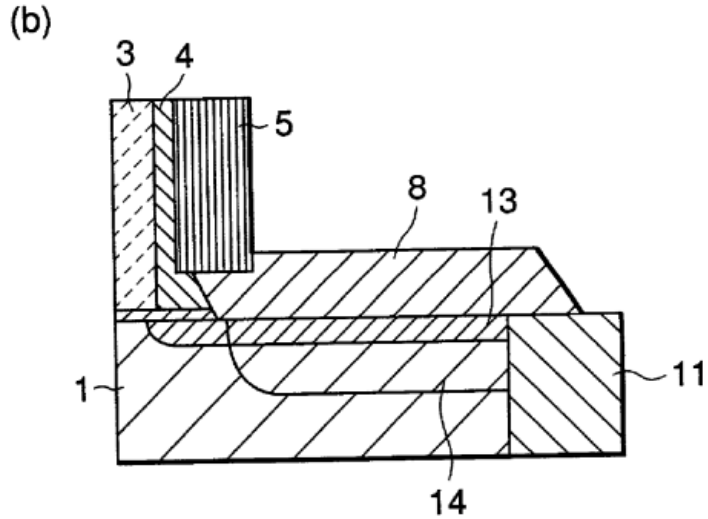
	Kamata discloses the following at Figure 1B(j):  *Kamata* discloses the following at Figure 5(c):  *Kamata* discloses the following at Figure 10(b):

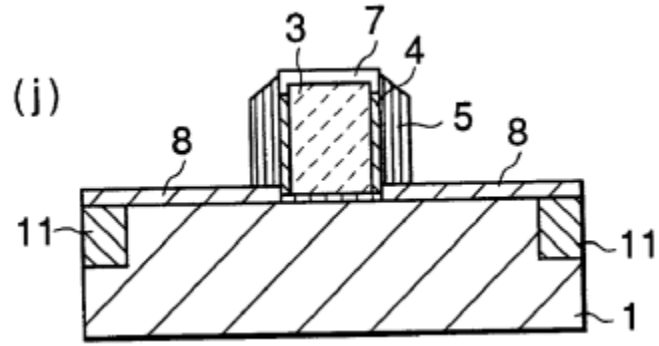
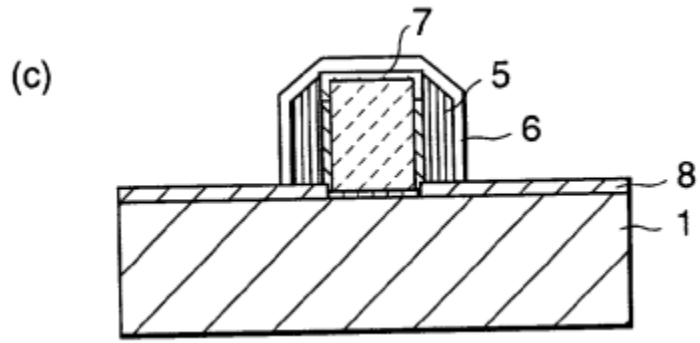
U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	
[1B] a gate electrode formed on the high dielectric constant gate insulating film;	*Kamata*, alone or in combination with one or more references, discloses or suggests a gate electrode formed on the high dielectric constant gate insulating film. For example: *Kamata* discloses the following at ¶¶ 8-11: An first aspect of the present invention, there is provided a semiconductor device comprising: a silicon substrate; a gate insulating film formed on a surface of the silicon substrate;

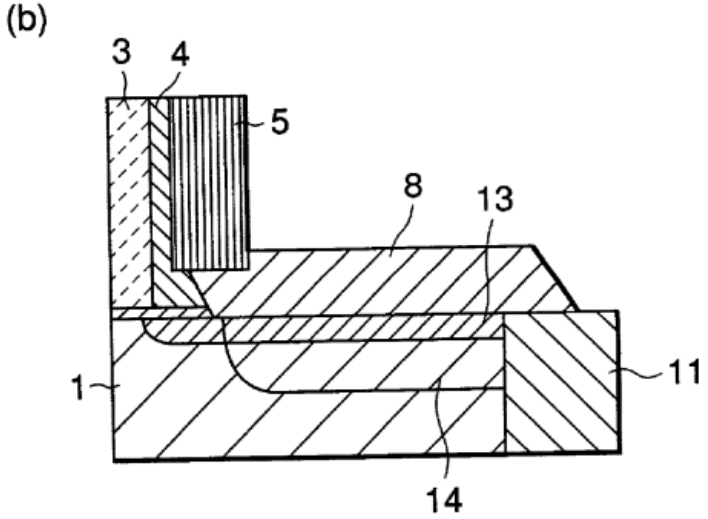
U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	a gate electrode formed on the gate insulating film; *Kamata* discloses the following at ¶ 50: Then, a gate electrode 3 is formed by depositing polycrystalline silicon (FIG. 1A(b)) and, after a lithography step, the gate electrode is processed by means of an anisotropic etching technique using plasma such as RIE (reactive ion etching (FIG. 1A(c)). *Kamata* discloses the following at claim 1: A semiconductor device comprising: a silicon substrate; a gate insulating film formed on a surface of the silicon substrate; a gate electrode formed on the gate insulating film;

	Kamata discloses the following at Figures 1A(a)-(c):  *Kamata* discloses the following at Figure 1B(j):

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	 *Kamata* discloses the following at Figure 5(c): 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	Kamata discloses the following at Figure 10(b): 
[1C] a insulating sidewall formed on each side surface of the gate electrode; and	*Kamata*, alone or in combination with one or more references, discloses or suggests a insulating sidewall formed on each side surface of the gate electrode. For example:

	Kamata discloses the following at Figure 1B(j):  *Kamata* discloses the following at Figure 5(c):  *Kamata* discloses the following at Figure 10(b):

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	 *Kamata* discloses the following at ¶¶ 8-15: An first aspect of the present invention, there is provided a semiconductor device comprising: a silicon substrate; a gate insulating film formed on a surface of the silicon substrate; a gate electrode formed on the gate insulating film; a first side wall film formed on a side surface of the gate electrode, and extending to the surface of the silicon substrate;

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	an elevated region formed by epitaxial growth of silicon on the surface of the silicon substrate; a second side wall film formed on the first side wall film, being made of different material from the first side wall film and separated from the surface of the silicon substrate by the elevated region; and a source region and a drain region formed in the silicon substrate and having a same conductive type with the elevated region. *Kamata* discloses the following at ¶ 16: A multilayer type sidewall films are formed on the respective side surfaces of the gate electrode of each MIS type element such as a transistor or a resistance by laying a number of layers that are directed toward a surface of the silicon substrate. With this arrangement, the leak current that can be generated by the tunnel phenomenon between the gate and the source or the drain is effectively suppressed. *Kamata* discloses the following at ¶ 50: Subsequently, the gate electrode is oxidized (to be referred to as post-gate oxidization step hereinafter) to produce a first side wall film 4 (FIG. 1A(d)). The surface layer that becomes a source region/a drain region is also oxidized in the post-gate oxidization step. Then, a silicon nitride film (Si_3N_4) 5 is deposited in a CVD (chemical vapor deposition) system (FIG. 1A(e)) and subsequently a silicon nitride film is formed only on the lateral side of the gate electrode by anisotropic etching using plasma (FIG. 1A(f)). *Kamata* discloses the following at ¶ 52:

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	Hereinafter, when both a post-gate oxide film (including an oxide film on the source/drain region) and a liner layer are provided, they are collectively referred to as the first side wall film and the silicon nitride film 5 at the side of the gate electrode is referred to as the second side wall film. When still another film is formed beside the silicon nitride film, these films are collectively referred to as the second side wall film. It should be noted that the second side wall film is not limited to a silicon nitride film and the silicon substrate may contain Ge. *Kamata* discloses the following at ¶ 57: If necessary, the amorphous silicon layer formed on the gate electrode 3 and the second sidewall film 5 without epitaxial growth is etched. *Kamata* discloses the following at ¶ 58: Then, the gate electrode 3 and the surface of the substrate are oxidized to produce a silicon oxide film 4 these (FIG.2A(c)) and subsequently a silicon nitride film 5 is formed there by deposition (FIG. 2A(d)). Then, the silicon nitride film is also treated by anisotropic plasma etching (FIG. 2B(e)) and the silicon oxide film 41 in the source/drain region 8 on the silicon substrate is removed by etching, using dilute hydrofluoric acid (DHF) solution. *Kamata* discloses the following at ¶ 74: FIG. 7(a) corresponds to the first embodiment and the part 4 a of the first side wall film 4 has a thickness same as the remaining part of the first sidewall film 4. The gap 10 a produced by etching a lower part of the second side wall film 5, using DHF, and located between the lower end 5 a and the silicon substrate 1 is filled as a result of solid phase epitaxial growth of the a—Si layer (which is turned into a crystalline Si layer 8 by heat treatment).

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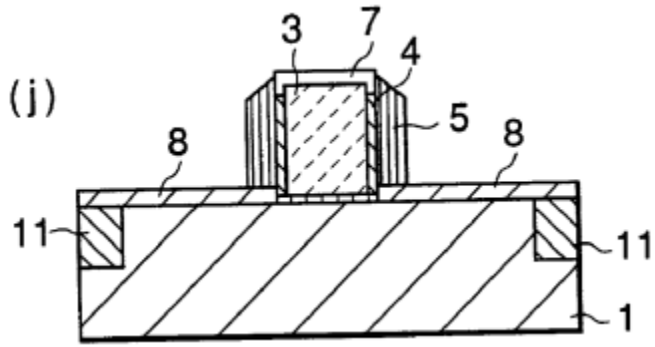
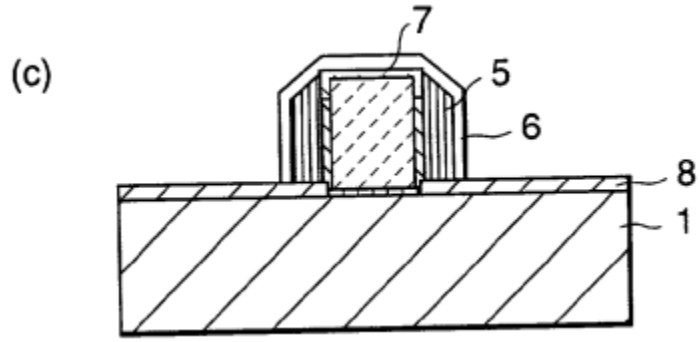
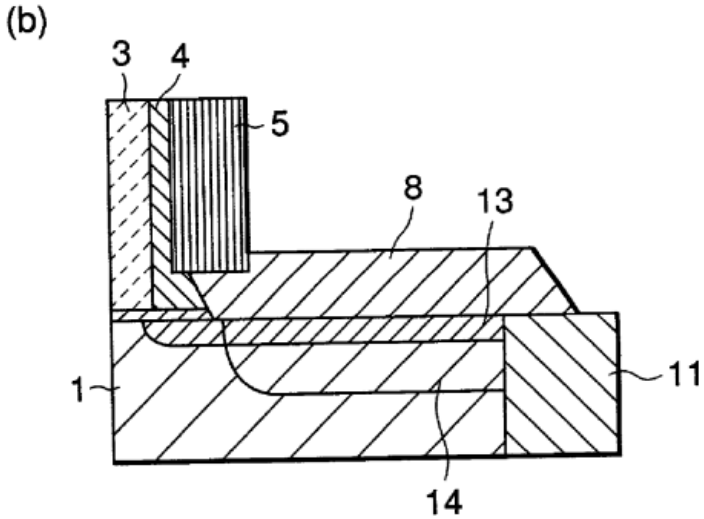
[1D] wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and	*Kamata*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall. For example: *Kamata* discloses the following at Figure 1B(j): 

	Kamata discloses the following at Figure 5(c):  *Kamata* discloses the following at Figure 10(b):  *Kamata* discloses the following at ¶ 50:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	> FIGS. 1A through 1B are schematic cross sectional views of the first embodiment of the present invention, illustrating different manufacturing steps thereof. Firstly, shallow trench isolation zones (STI) 11 are formed on a semiconductor substrate 1 made of silicon to define an element region 1 a (FIG. 1A(a)). Then, a gate electrode 3 is formed by depositing polycrystalline silicon (FIG. 1A(b)) and, after a lithography step, the gate electrode is processed by means of an anisotropic etching technique using plasma such as RIE (reactive ion etching (FIG. 1A(c)). Subsequently, the gate electrode is oxidized (to be referred to as post-gate oxidization step hereinafter) to produce a first side wall film 4 (FIG. 1A(d)). The surface layer that becomes a source region/a drain region is also oxidized in the post-gate oxidization step. Then, a silicon nitride film (Si_3N_4) 5 is deposited in a CVD (chemical vapor deposition) system (FIG. 1A(e)) and subsequently a silicon nitride film is formed only on the lateral side of the gate electrode by anisotropic etching using plasma (FIG. 1A(f)). Note that no problem arises if the gate insulating film and the silicon oxide film on the source region/drain region 8 are partly scraped off by the anisotropic etching using plasma. *Kamata* discloses the following at ¶ 56: > After forming the second side wall film 5 as shown in FIG. 1A(f), the silicon oxide films 2, 4 on the source/drain region 8 on the silicon substrate and on the gate electrode 3 are etched out by using dilute hydrofluoric acid (DHF). The part of the first side wall film located between the second side wall film and the silicon substrate is completely etched out in this step (FIG. 1B(g)). As a result of this etching step, a gap 10 a is produced between the surface of the silicon substrate and the end 5 a of the second side wall film 5 apart from the substrate. The film thickness of the part 4 a of the first side wall film 4 is made equal to that of the remaining first side wall film. *Kamata* discloses the following at Figures 1A(f) and 1B(g):

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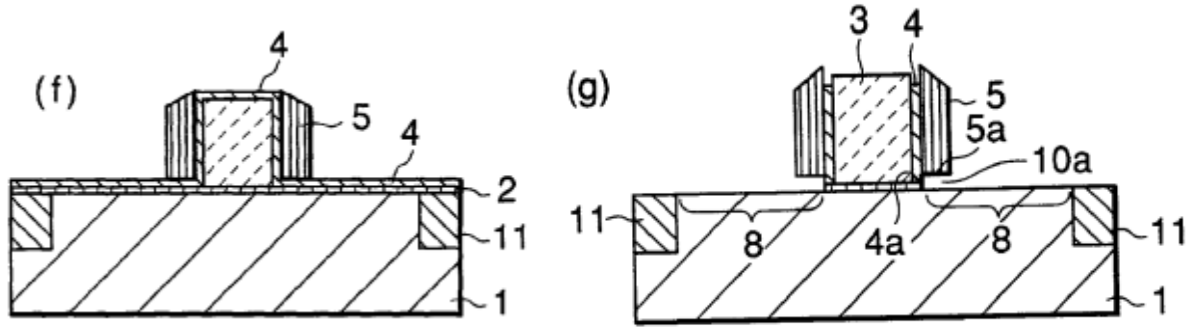
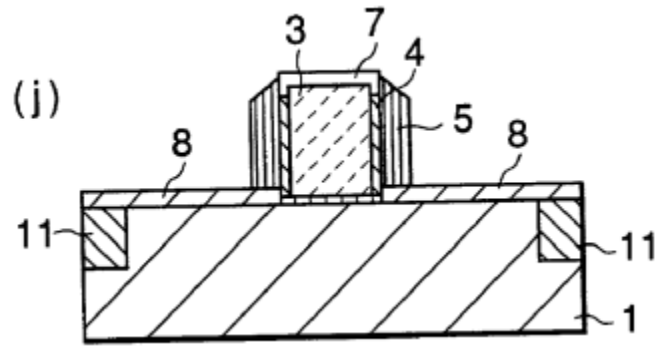
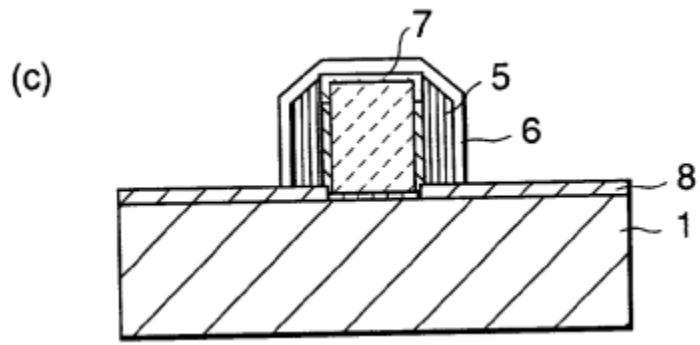
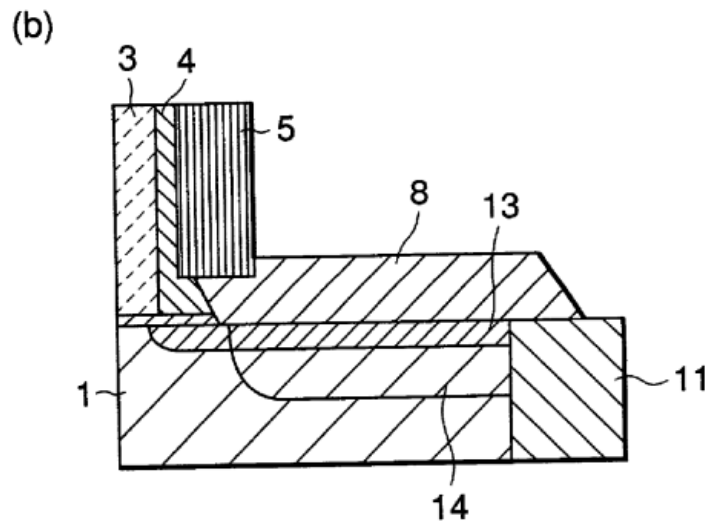
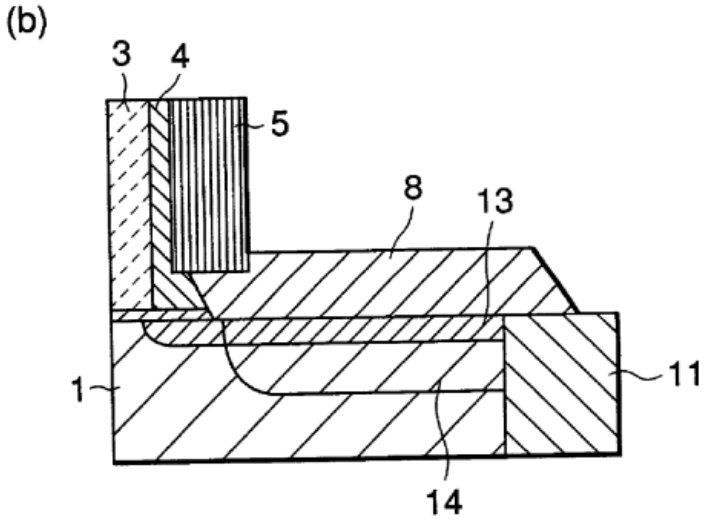
	 *Kamata* discloses the following at ¶ 93: FIG. 10(a) and (b) shows the ninth embodiment of the present invention. Referring to the figure, a diffusion layer 14 is formed by ion implantation. After processing the gate electrode 3, an extention region 13 is formed by implanting impurities into the silicon substrate through the gate insulating film and annealing the epitaxially grown film in an ion implantation system (FIG. 10(a)). Then, as in the case of the first through eighth embodiments, a deep diffusion region 14 is formed by forming an elevated source/drain region 8 on the side wall film 5, introducing impurities into a region of the silicon substrate 1 located deeper than the extended region 13 by ion implantation and annealing the epitaxially grown layer (FIG. 10(b)). The diffusion layer formed in this way shows a low resistance to suppress the adverse short channel effect.
[1E] an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end	*Kamata*, alone or in combination with one or more references, discloses or suggests an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode. For example:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
of the insulating sidewall toward the gate electrode.	*Kamata* discloses the following at Figure 1B(j):  *Kamata* discloses the following at Figure 5(c): 

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	Kamata discloses the following at Figure 10(b):  *See also* limitation [1D], *supra*.
Claim 2	
2. The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests a buffer insulating film between the substrate and the high dielectric constant gate insulating film. For example:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	Kamata discloses the following at ¶ 54: > It is desired that a SiOx (0<x≦2) layer or the layer containing N is interposed between the gate insulating film and the silicon substrate or between the gate insulating film and the gate electrode of poly silicon.
Claim 3	
3. The semiconductor device of claim 2, wherein the buffer insulating film is a silicon oxide film.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 2. *See* claim 2, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the buffer insulating film is a silicon oxide film. For example: *Kamata* discloses the following at ¶ 54: > It is desired that a SiOx (0<x≦2) layer or the layer containing N is interposed between the gate insulating film and the silicon substrate or between the gate insulating film and the gate electrode of poly silicon.
Claim 5	
5. The semiconductor device of claim 1, wherein a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating sidewall is smaller than that	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests a smallest thickness of part of the high dielectric constant gate insulating film located under the insulating

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
of part of the high dielectric constant gate insulating film located under the gate electrode.	sidewall is smaller than that of part of the high dielectric constant gate insulating film located under the gate electrode. For example: *See* limitations [1D]-[1E], *supra*. *Kamata* discloses the following at Figure 10(b):  *Kamata* discloses the following at ¶ 93:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	FIG. 10(a) and (b) shows the ninth embodiment of the present invention. Referring to the figure, a diffusion layer 14 is formed by ion implantation. After processing the gate electrode 3, an extention region 13 is formed by implanting impurities into the silicon substrate through the gate insulating film and annealing the epitaxially grown film in an ion implantation system (FIG. 10(a)). Then, as in the case of the first through eighth embodiments, a deep diffusion region 14 is formed by forming an elevated source/drain region 8 on the side wall film 5, introducing impurities into a region of the silicon substrate 1 located deeper than the extended region 13 by ion implantation and annealing the epitaxially grown layer (FIG. 10(b)). The diffusion layer formed in this way shows a low resistance to suppress the adverse short channel effect. *Kamata* discloses the following at ¶ 85: This embodiment is described according to FIG. 8(a) and (b). All the manufacturing steps of the first through sixth embodiment are applicable to this embodiment. This embodiment differs from the first through sixth embodiments in that the epitaxially grown film 8 of this embodiment that is extending onto the top surface of the element isolation zone 11 (FIG. 8(a)). As a result of a series of experiments conducted prior to the present invention, the inventor of the invention found that, when the interface of the element isolation zone 11 and the active zone 1 a is inclined toward the plane (100) from the plane (110), the epitaxially grown film 8 can be made to extend considerably onto the element isolation zone. In an experiment, the inventor of the present invention succeeded in forming a (110) facet plane and extending it laterally on the element isolation zone 11 by about 150 to 200 nm as a result of solid phase growth by conducting a rapid thermal annealing operation on a 100 nm thick a—Si layer at 680 to 700° C. for about 60 seconds. *Kamata* discloses the following at ¶ 18:

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	Both the short channel effect and the leak can be further reduced by suppressing the generation of facets in the epitaxial growth process and by filling the elevated region in the gap between the second side wall film and the silicon substrate. Generally, crystal facets having a specific facet index are formed in the epitaxial growth process to suppress the epitaxial growth in the direction of the facet. Particularly, in the case of solid phase epitaxial growth, the (110) plane grows at a rate about twice as slow as the (100) plane, whereas the (111) plane shows a growth rate twenty times as low as the (100) plane. While a silicon substrate having a (100) plane is generally used, not only a (100) plane but also a (110) plane and a (111) plane that show a low growth rate are formed in the solid phase epitaxial growth process. Similarly, in the case of vapor phase epitaxial growth, a (311) plane is apt to be formed. When the DHF process is insufficient, the epitaxially grown film produces facets due to the gate insulating film. It is believed that the amorphous silicon (to be referred to as a—Si hereinafter) deposited on the insulting film is bonded, if weakly, to atoms of the insulating film and such facets reflect the difference in the bond energy. As a result of a series of experiments conducted by the inventor of the present invention, it is found that such facets are apt to be produced more in the vicinity of a silicon oxide film than in the vicinity of a silicon nitride film. Therefore, if the gate insulating film is formed from an oxide film, facets are formed due to the oxide film but, on the other hand if an epitaxially grown facet is made to contact the lower end of the side wall film of silicon nitride film, it is possible to realize epitaxial growth on the side wall film without forming facets because of the existence of the silicon nitride film. In the case of solid phase epitaxial growth, while the etched region under the second side wall film is completely filled with amorphous silicon and hence facets are formed in the subsequent solid phase epitaxial growth process, all the amorphous silicon filling the etched region is crystallized if the solid phase epitaxial growth process is conducted thoroughly because the epitaxial growth, if slow, takes place also on the facets.
Claim 6	

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6. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film is formed of a Hf based oxide. For example: *Kamata* discloses the following at ¶¶ 52-53: > The gate insulating film may be a silicon oxide film, a silicon nitride film, a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element. > The film may be a single crystal film, a poly crystal film or an amorphous film such as TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ and Gd_2O_3. Furthermore, the film may be made of a mixture of SiO_2, TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ or Gd_2O_3, with Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr or Gd.
Claim 11	
11. The semiconductor device of claim 1, wherein a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests a part of the high dielectric constant gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.
Claim 13	

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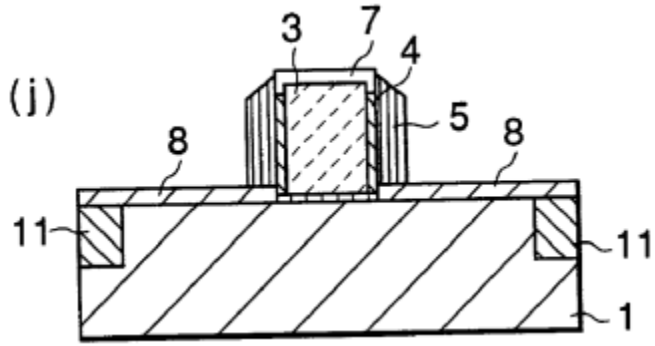
13. The semiconductor device of claim 1, wherein the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the end of the high dielectric constant gate insulating film is located at a predetermined distance from a side end of the gate electrode toward the insulating sidewall. For example: *See* limitations [1D]-[1E]. *Kamata* discloses the following at Figure 1B(j): 

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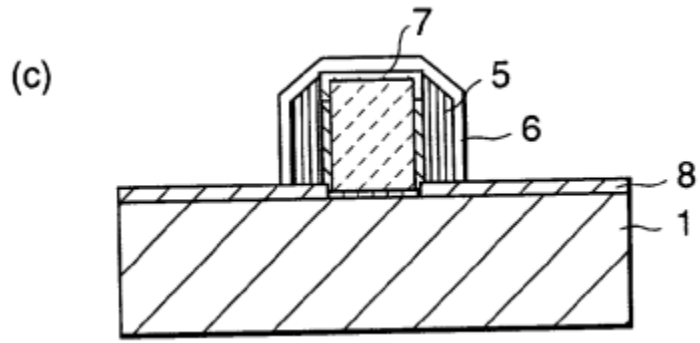
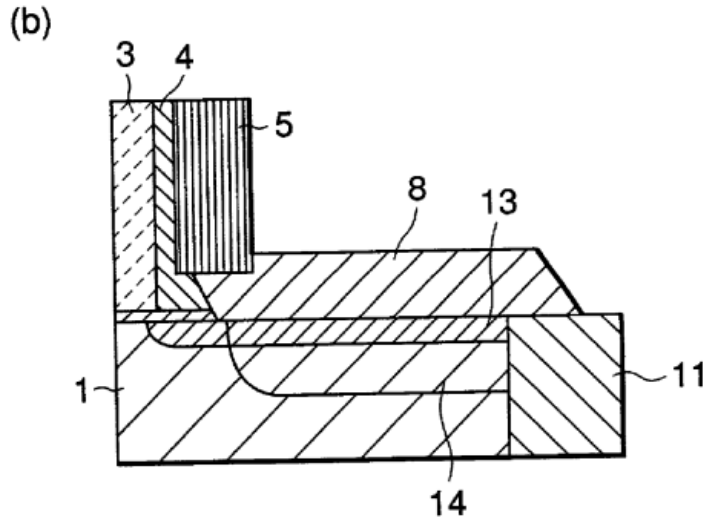
	Kamata discloses the following at Figure 5(c):  *Kamata* discloses the following at Figure 10(b): 
Claim 14	

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14. The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the insulating sidewall has a double layer structure including an oxide film and a nitride film. For example: *See* limitation [1C]. *Kamata* discloses the following at ¶ 50: > Subsequently, the gate electrode is oxidized (to be referred to as post-gate oxidization step hereinafter) to produce a first side wall film 4 (FIG. 1A(d)). The surface layer that becomes a source region/a drain region is also oxidized in the post-gate oxidization step. Then, a silicon nitride film (Si_3N_4) 5 is deposited in a CVD (chemical vapor deposition) system (FIG. 1A(e)) and subsequently a silicon nitride film is formed only on the lateral side of the gate electrode by anisotropic etching using plasma (FIG. 1A(f)). *Kamata* discloses the following at ¶ 58: > Then, the gate electrode 3 and the surface of the substrate are oxidized to produce a silicon oxide film 4 these (FIG.2A(c)) and subsequently a silicon nitride film 5 is formed there by deposition (FIG. 2A(d)). Then, the silicon nitride film is also treated by anisotropic plasma etching (FIG. 2B(e)) and the silicon oxide film 41 in the source/drain region 8 on the silicon substrate is removed by etching, using dilute hydrofluoric acid (DHF) solution. *Kamata* discloses the following at ¶ 16:

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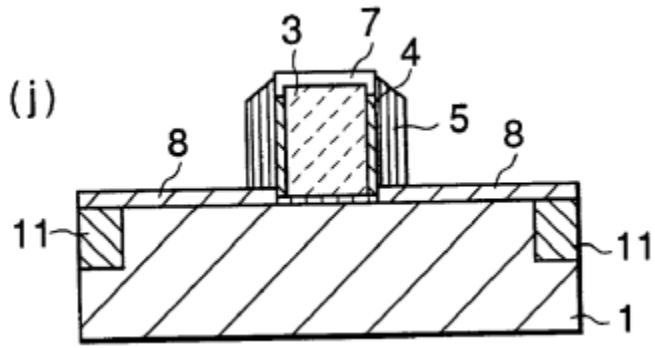
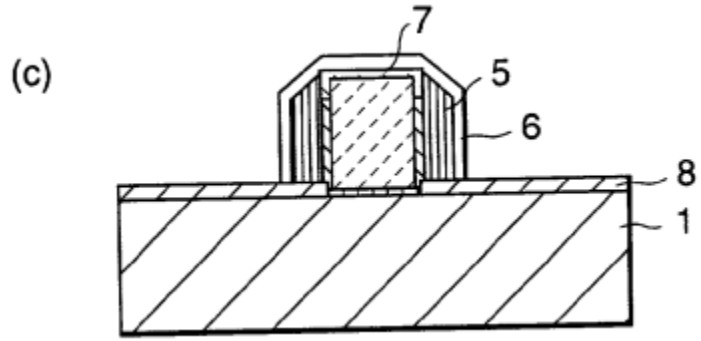
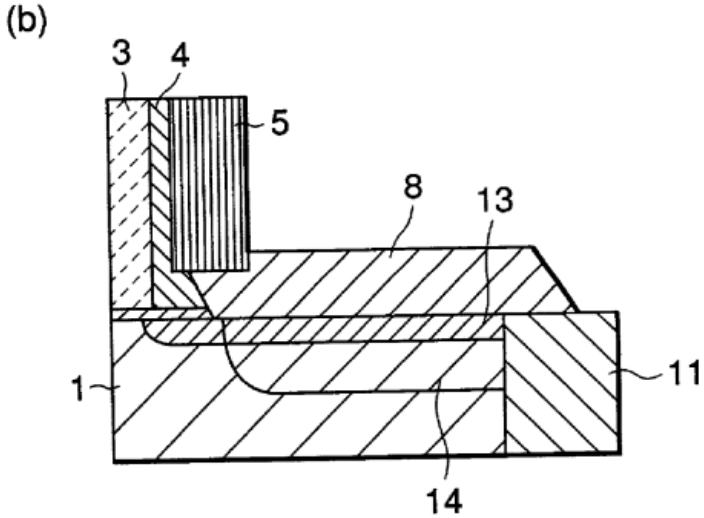
	A multilayer type sidewall films are formed on the respective side surfaces of the gate electrode of each MIS type element such as a transistor or a resistance by laying a number of layers that are directed toward a surface of the silicon substrate. With this arrangement, the leak current that can be generated by the tunnel phenomenon between the gate and the source or the drain is effectively suppressed.
Claim 16	
16. The semiconductor device of claim 1, wherein a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests a width of the high dielectric constant gate insulating film along a gate length is larger than a width of the gate electrode along the gate length. For example: *Kamata* discloses the following at Figure 1B(j): 

	Kamata discloses the following at Figure 5(c):  *Kamata* discloses the following at Figure 10(b):  *Kamata* discloses the following at ¶ 50:

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	FIGS. 1A through 1B are schematic cross sectional views of the first embodiment of the present invention, illustrating different manufacturing steps thereof. Firstly, shallow trench isolation zones (STI) 11 are formed on a semiconductor substrate 1 made of silicon to define an element region 1 a (FIG. 1A(a)). Then, a gate electrode 3 is formed by depositing polycrystalline silicon (FIG. 1A(b)) and, after a lithography step, the gate electrode is processed by means of an anisotropic etching technique using plasma such as RIE (reactive ion etching (FIG. 1A(c)). Subsequently, the gate electrode is oxidized (to be referred to as post-gate oxidization step hereinafter) to produce a first side wall film 4 (FIG. 1A(d)). The surface layer that becomes a source region/a drain region is also oxidized in the post-gate oxidization step. Then, a silicon nitride film (Si_3N_4) 5 is deposited in a CVD (chemical vapor deposition) system (FIG. 1A(e)) and subsequently a silicon nitride film is formed only on the lateral side of the gate electrode by anisotropic etching using plasma (FIG. 1A(f)). Note that no problem arises if the gate insulating film and the silicon oxide film on the source region/drain region 8 are partly scraped off by the anisotropic etching using plasma. *Kamata* discloses the following at ¶ 56: After forming the second side wall film 5 as shown in FIG. 1A(f), the silicon oxide films 2, 4 on the source/drain region 8 on the silicon substrate and on the gate electrode 3 are etched out by using dilute hydrofluoric acid (DHF). The part of the first side wall film located between the second side wall film and the silicon substrate is completely etched out in this step (FIG. 1B(g)). As a result of this etching step, a gap 10 a is produced between the surface of the silicon substrate and the end 5 a of the second side wall film 5 apart from the substrate. The film thickness of the part 4a of the first side wall film 4 is made equal to that of the remaining first side wall film.

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	Kamata discloses the following at ¶ 68: FIGS. 5 shows the fifth embodiment of the present invention. This embodiment differs from the first embodiment only in that the first side wall film completely removed by etching in an area 4 d between the second side wall film 5 and the silicon substrate land also removed by etching in another area 4 c between the second side wall film 5 and the gate electrode 3 to reduce the film thickness if compared with the remaining part of the first side wall film. Otherwise, this embodiment is same as the first embodiment. Therefore, in FIG. 5(a) through (c), the parts that are same as or similar to those of the first embodiment are denoted respectively by the same reference symbols. *Kamata* discloses the following at ¶ 93: FIG. 10(a) and (b) shows the ninth embodiment of the present invention. Referring to the figure, a diffusion layer 14 is formed by ion implantation. After processing the gate electrode 3, an extention region 13 is formed by implanting impurities into the silicon substrate through the gate insulating film and annealing the epitaxially grown film in an ion implantation system (FIG. 10(a)). Then, as in the case of the first through eighth embodiments, a deep diffusion region 14 is formed by forming an elevated source/drain region 8 on the side wall film 5, introducing impurities into a region of the silicon substrate 1 located deeper than the extended region 13 by ion implantation and annealing the epitaxially grown layer (FIG. 10(b)). The diffusion layer formed in this way shows a low resistance to suppress the adverse short channel effect.
Claim 17	
17. The semiconductor device of claim 1, wherein a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*.

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than a width of a bottom surface of the gate electrode along the gate length.	*Kamata*, alone or in combination with one or more references, discloses or suggests a width of a bottom surface of the high dielectric constant gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length. For example: *See* claim 16, *supra*.
Claim 18	
18. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film has a relative dielectric constant of 10 or more. For example: *Kamata* discloses the following at ¶¶ 52-53: > The gate insulating film may be a silicon oxide film, a silicon nitride film, a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element. > The film may be a single crystal film, a poly crystal film or an amorphous film such as TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ and Gd_2O_3. Furthermore, the film may be made of a mixture of SiO_2, TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ or Gd_2O_3, with Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr or Gd.
Claim 19	

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19. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film has a larger relative dielectric constant than that of the insulating sidewall. For example: *Kamata* discloses the following at ¶¶ 52-53: > The gate insulating film may be a silicon oxide film, a silicon nitride film, a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element. > The film may be a single crystal film, a poly crystal film or an amorphous film such as TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ and Gd_2O_3. Furthermore, the film may be made of a mixture of SiO_2, TiO_2, Ti_2O_5, BST, Si_3N_4, Al_2O_3, Y_2O_3, La_2O_3, HfO_2, ZrO_2, Pr_2O_3, $SrTiO_3$ or Gd_2O_3, with Ti, Zr, Hf, Ta, La, Al Ba, Sr, Y, Pr or Gd. *Kamata* discloses the following at ¶ 50: > Subsequently, the gate electrode is oxidized (to be referred to as post-gate oxidization step hereinafter) to produce a first side wall film 4 (FIG. 1A(d)). The surface layer that becomes a source region/a drain region is also oxidized in the post-gate oxidization step. Then, a silicon nitride film (Si_3N_4) 5 is deposited in a CVD (chemical vapor deposition) system (FIG. 1A(e)) and subsequently a silicon nitride film is formed only on the lateral side of the gate electrode by anisotropic etching using plasma (FIG. 1A(f)).

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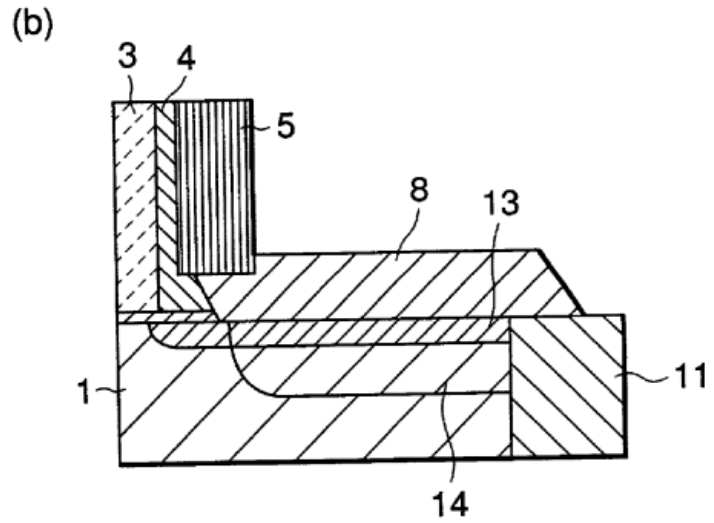
	Kamata discloses the following at ¶ 58: Then, the gate electrode 3 and the surface of the substrate are oxidized to produce a silicon oxide film 4 these (FIG.2A(c)) and subsequently a silicon nitride film 5 is formed there by deposition (FIG. 2A(d)). Then, the silicon nitride film is also treated by anisotropic plasma etching (FIG. 2B(e)) and the silicon oxide film 41 in the source/drain region 8 on the silicon substrate is removed by etching, using dilute hydrofluoric acid (DHF) solution.
Claim 21	
21. The semiconductor device of claim 1, wherein the end of the high dielectric constant gate insulating film located under the insulating sidewall has a tapered surface.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the end of the high dielectric constant gate insulating film located under the insulating sidewall has a tapered surface. For example:

	See limitations [1D]-[1E], *supra*. *Kamata* discloses the following at Figure 10(b):  *Kamata* discloses the following at ¶ 93: FIG. 10(a) and (b) shows the ninth embodiment of the present invention. Referring to the figure, a diffusion layer 14 is formed by ion implantation. After processing the gate electrode 3, an extention region 13 is formed by implanting impurities into the silicon substrate through the gate insulating film and annealing the epitaxially grown film in an ion implantation system (FIG. 10(a)). Then, as in the case of the first through eighth embodiments, a deep diffusion region 14 is formed by forming an elevated source/drain region 8 on the side wall film 5, introducing impurities into a region of the silicon substrate 1 located deeper than the extended region 13 by ion implantation and annealing the epitaxially grown layer (FIG. 10(b)). The diffusion layer formed in this way shows a low resistance to suppress the adverse short channel effect.

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	Kamata discloses the following at ¶ 85: This embodiment is described according to FIG. 8(a) and (b). All the manufacturing steps of the first through sixth embodiment are applicable to this embodiment. This embodiment differs from the first through sixth embodiments in that the epitaxially grown film 8 of this embodiment that is extending onto the top surface of the element isolation zone 11 (FIG. 8(a)). As a result of a series of experiments conducted prior to the present invention, the inventor of the invention found that, when the interface of the element isolation zone 11 and the active zone 1 a is inclined toward the plane (100) from the plane (110), the epitaxially grown film 8 can be made to extend considerably onto the element isolation zone. In an experiment, the inventor of the present invention succeeded in forming a (110) facet plane and extending it laterally on the element isolation zone 11 by about 150 to 200 nm as a result of solid phase growth by conducting a rapid thermal annealing operation on a 100 nm thick a—Si layer at 680 to 700° C. for about 60 seconds.

U.S. Patent No. 8,253,180	Exemplary Disclosures Relevant to *Kamata*
	Kamata discloses the following at ¶ 18: Both the short channel effect and the leak can be further reduced by suppressing the generation of facets in the epitaxial growth process and by filling the elevated region in the gap between the second side wall film and the silicon substrate. Generally, crystal facets having a specific facet index are formed in the epitaxial growth process to suppress the epitaxial growth in the direction of the facet. Particularly, in the case of solid phase epitaxial growth, the (110) plane grows at a rate about twice as slow as the (100) plane, whereas the (111) plane shows a growth rate twenty times as low as the (100) plane. While a silicon substrate having a (100) plane is generally used, not only a (100) plane but also a (110) plane and a (111) plane that show a low growth rate are formed in the solid phase epitaxial growth process. Similarly, in the case of vapor phase epitaxial growth, a (311) plane is apt to be formed. When the DHF process is insufficient, the epitaxially grown film produces facets due to the gate insulating film. It is believed that the amorphous silicon (to be referred to as a—Si hereinafter) deposited on the insulting film is bonded, if weakly, to atoms of the insulating film and such facets reflect the difference in the bond energy. As a result of a series of experiments conducted by the inventor of the present invention, it is found that such facets are apt to be produced more in the vicinity of a silicon oxide film than in the vicinity of a silicon nitride film. Therefore, if the gate insulating film is formed from an oxide film, facets are formed due to the oxide film but, on the other hand if an epitaxially grown facet is made to contact the lower end of the side wall film of silicon nitride film, it is possible to realize epitaxial growth on the side wall film without forming facets because of the existence of the silicon nitride film. In the case of solid phase epitaxial growth, while the etched region under the second side wall film is completely filled with amorphous silicon and hence facets are formed in the subsequent solid phase epitaxial growth process, all the amorphous silicon filling the etched region is crystallized if the solid phase epitaxial growth process is conducted thoroughly because the epitaxial growth, if slow, takes place also on the facets.
Claim 22	

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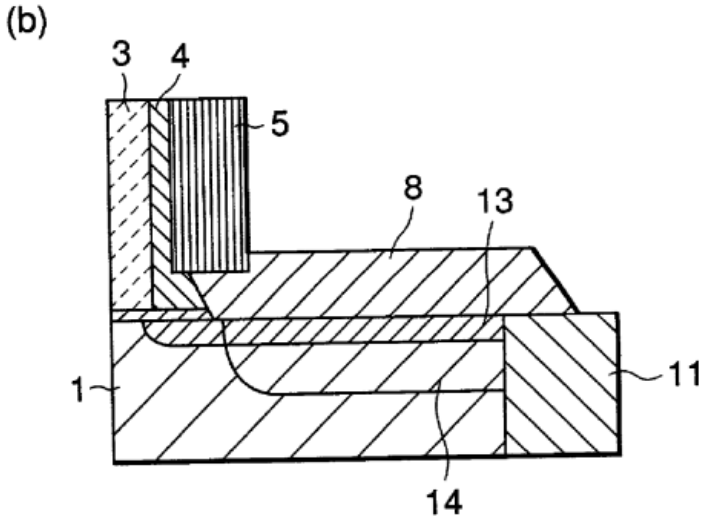
22. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.	*Kamata*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Kamata*, alone or in combination with one or more references, discloses or suggests the high dielectric constant gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof. For example: *See* limitations [1D]-[1E], *supra*. *Kamata* discloses the following at Figure 10(b): 

	Kamata discloses the following at ¶ 93: FIG. 10(a) and (b) shows the ninth embodiment of the present invention. Referring to the figure, a diffusion layer 14 is formed by ion implantation. After processing the gate electrode 3, an extention region 13 is formed by implanting impurities into the silicon substrate through the gate insulating film and annealing the epitaxially grown film in an ion implantation system (FIG. 10(a)). Then, as in the case of the first through eighth embodiments, a deep diffusion region 14 is formed by forming an elevated source/drain region 8 on the side wall film 5, introducing impurities into a region of the silicon substrate 1 located deeper than the extended region 13 by ion implantation and annealing the epitaxially grown layer (FIG. 10(b)). The diffusion layer formed in this way shows a low resistance to suppress the adverse short channel effect. *Kamata* discloses the following at ¶ 85: This embodiment is described according to FIG. 8(a) and (b). All the manufacturing steps of the first through sixth embodiment are applicable to this embodiment. This embodiment differs from the first through sixth embodiments in that the epitaxially grown film 8 of this embodiment that is extending onto the top surface of the element isolation zone 11 (FIG. 8(a)). As a result of a series of experiments conducted prior to the present invention, the inventor of the invention found that, when the interface of the element isolation zone 11 and the active zone 1 a is inclined toward the plane (100) from the plane (110), the epitaxially grown film 8 can be made to extend considerably onto the element isolation zone. In an experiment, the inventor of the present invention succeeded in forming a (110) facet plane and extending it laterally on the element isolation zone 11 by about 150 to 200 nm as a result of solid phase growth by conducting a rapid thermal annealing operation on a 100 nm thick a—Si layer at 680 to 700° C. for about 60 seconds. *Kamata* discloses the following at ¶ 18: Both the short channel effect and the leak can be further reduced by suppressing the generation of facets in the epitaxial growth process and by filling the elevated region in the gap between the second side wall film and the silicon substrate. Generally, crystal

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	facets having a specific facet index are formed in the epitaxial growth process to suppress the epitaxial growth in the direction of the facet. Particularly, in the case of solid phase epitaxial growth, the (110) plane grows at a rate about twice as slow as the (100) plane, whereas the (111) plane shows a growth rate twenty times as low as the (100) plane. While a silicon substrate having a (100) plane is generally used, not only a (100) plane but also a (110) plane and a (111) plane that show a low growth rate are formed in the solid phase epitaxial growth process. Similarly, in the case of vapor phase epitaxial growth, a (311) plane is apt to be formed. When the DHF process is insufficient, the epitaxially grown film produces facets due to the gate insulating film. It is believed that the amorphous silicon (to be referred to as a—Si hereinafter) deposited on the insulting film is bonded, if weakly, to atoms of the insulating film and such facets reflect the difference in the bond energy. As a result of a series of experiments conducted by the inventor of the present invention, it is found that such facets are apt to be produced more in the vicinity of a silicon oxide film than in the vicinity of a silicon nitride film. Therefore, if the gate insulating film is formed from an oxide film, facets are formed due to the oxide film but, on the other hand if an epitaxially grown facet is made to contact the lower end of the side wall film of silicon nitride film, it is possible to realize epitaxial growth on the side wall film without forming facets because of the existence of the silicon nitride film. In the case of solid phase epitaxial growth, while the etched region under the second side wall film is completely filled with amorphous silicon and hence facets are formed in the subsequent solid phase epitaxial growth process, all the amorphous silicon filling the etched region is crystallized if the solid phase epitaxial growth process is conducted thoroughly because the epitaxial growth, if slow, takes place also on the facets.