UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner

Case IPR2025-00830
Patent 8,253,180

PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,253,180

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EXHIBIT LIST

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EX2001	**Complaint for Patent Infringement,** Dkt. No. 1, *Advanced Integrated Circuit Process LLC v. Taiwan Semiconductor Manufacturing Company Limited,* Case No. 2:24-cv-00623, (E.D. Tex. Filed August 1, 2024)
EX2002	**Complaint for Patent Infringement,** Dkt. No. 1, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Case No. 2:24-cv-00730, (E.D. Tex. Filed September 6, 2024)
EX2003	**Consolidation Order,** Dkt. No. 12, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed December 6, 2024)
EX2004	**Docket Sheet**, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Case No. 2:24-cv-00730, (E.D. Tex.) (Printed July 7, 2025)
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EX2012	**Plaintiff's Unopposed Motion for Leave to Amend Infringement Contentions Against Defendant United Microelectronic Corporation,** Dkt. No. 64, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed March 7, 2025)
EX2013	**Defendant Taiwan Semiconductor Manufacturing Company Limited's Notice of Compliance and Service of Invalidity Contentions**, Dkt. No. 104, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 1, 2025)
EX2014	**Defendant United Microelectronic Corporation's Notice of Compliance and Service of Invalidity Contentions**, Dkt. No. 106 *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 2, 2025)
EX2015	**Scheduling Order**, Dkt. No. 28, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Case No. 2:24-cv-00730, (E.D. Tex. Filed December 11, 2024)
EX2016	**Defendant TSMC's Invalidity Contentions**, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)
EX2017	**Defendant United Microelectronics Corporation's Invalidity Contentions**, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Served May 1, 2025)
EX2018	**Declaration of Kemper Diehl**, dated July 11, 2025

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EX2019	**Protective Order**, Dkt. No. 71, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed March 20, 2025)
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EX2023	**Defendant Taiwan Semiconductor Manufacturing Company Limited's Reply in Support of its Motion to Stay Pending *Inter Partes* Review**, Dkt. No. 109, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 20, 2025)
EX2024	**Plaintiff's Opposition to Defendant Taiwan Semiconductor Manufacturing Company Limited's Motion to Stay,** Dkt. No. 108, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623, (E.D. Tex. Filed May 12, 2025)
EX2025	**Exhibit 180-01** to Defendant TSMC's Invalidity Contentions, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Served May 1, 2025)
EX2026	**Exhibit 180-02** to Defendant TSMC's Invalidity Contentions, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Served May 1, 2025)

Exhibit	Description
EX2027	**Lex Machina Time-to-Trial Statistics Report** for trials before The Honorable Rodney Gilstrap, Federal District Judge in the Eastern District of Texas, during the period from July 1, 2024 to July 1, 2025
EX2028	**Notice of Allowance** in TSMC's U.S. Patent Application Ser. No. 12/757,241 (May 24, 2012)
EX2029	RESERVED
EX2030	**Notice of Allowance** in TSMC's U.S. Patent Application Ser. No. 17/027,032 (November 24, 2023)
EX2031	**Redaction to TSMC's Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Japan,** Dkt. No. 119, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 27, 2025)
EX2032	**Exhibit A to TSMC's Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Japan,** Dkt. No. 116-1, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 20, 2025)
EX2033	**Exhibit B to TSMC's Sealed Motion for Issuance of Letter Rogatory for Nuvoton Technology Corporation – Taiwan,** Dkt. No. 114-2, *Advanced Integrated Circuit Process LLC v. United Microelectronics Corporation,* Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Filed June 20, 2025)
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EX2035	**Recorded Assignment** from Panasonic Corporation to Panasonic Semiconductor Solutions Co., Ltd. (May 21, 2020)
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EX2037	**Exhibit 180-03** to Defendant TSMC's Invalidity Contentions, *Advanced Integrated Circuit Process LLC v. United*

Exhibit	Description
	Microelectronics Corporation, Consolidated Case Nos. 2:24-cv-00730, -00623 (E.D. Tex. Served May 1, 2025)
EX2038	**Bashir, R., et al.,** "Reduction of Sidewall Defect Induced Leakage Currents by the Use of Nitrided Field Oxides in Silicon Selective Epitaxial Growth Isolation for Advanced Ultralarge Scale Integration," 18(2) J. Vac. Sci. Technol. B 695–699 (2000).

Advanced Integrated Circuit Technology, LLC ("Patent Owner") respectfully requests that the Board decline to institute *inter partes* review ("IPR") on the petition ("Petition") filed by Taiwan Semiconductor Manufacturing Company Ltd. ("Petitioner") because it fails to "show[] . . . a reasonable likelihood" that Petitioner would prevail with respect to any of the challenged claims. 35 U.S.C. § 314(a).

I. INTRODUCTION

Although the Petition's theories suffer from many infirmities, this preliminary response focuses on two flaws fatal to each of the grounds.[1] First, Petition Grounds 1-7 relying on Kamata are premised on an implied claim interpretation of U.S. Patent No. 8,253,180 ("the '180 patent"). That claim construction makes no sense given the patent's written description. Each claim in the '180 patent requires a "high dielectric constant gate insulating film" and "a[n] insulating sidewall" wherein "an end of the high dielectric constant gate insulating film under the insulating sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode." EX1001, claim 1. The specification and figures uniformly teach that

[1] Because these flaws preclude a "reasonable likelihood" of success as to all challenged claims, 35 U.S.C. § 314(a), Patent Owner need not address the Petition's other flaws. If the Board institutes IPR, Patent Owner reserves the right to address each of these flaws.

the "outer end of the insulating sidewall" corresponds to the outer end of the outermost sidewall component that is directly on the gate insulating film. The Petition attempts to fit a round peg in a square hole by relying on sidewall components in multicomponent sidewalls in Kamata that are far from the high dielectric constant gate insulating film, much less directly on it.

Second, Grounds 8-13 fail because the Petition does not prove that Guha or Matsumoto discloses "an active region ***in*** a substrate" as required by each of the '180 patent's claims. Although the Petition offers no claim construction proposal for the term "substrate," Petitioner's expert and textbook assert that it means "silicon wafer." But whereas the '180 patent teaches a transistor isolation technology that (consistent with the claims) results in the transistor's active region being "in" the silicon wafer, Guha and Matsumoto disclose a different transistor isolation technology that results in the transistor's active region being in layers that are "on," not "in," the silicon wafer. Accepting the Petition's evidence as true, the Petition cannot demonstrate that the claimed invention was known in, or obvious in view of, the asserted references.

II. BACKGROUND[2]

A. Technology Background

"Modern CMOS chips integrate millions of active devices . . . side by side in a common silicon substrate." EX1003 ¶ 45 (quoting EX1033 at 52). One such active device is a MISFET, which stands for "metal-insulator-semiconductor field effect transistor." *Id*. ¶ 36. The terms MISFET and MOSFET are interchangeable. *Id*. As exemplified by Petitioner's Weste reference Figure 1.8, EX1041 at 8 (shown below), "[a] typical MISFET device is a three-terminal structure with an input, referred to as the source, an output, referred to as the drain, and a control terminal, referred to as the gate electrode." EX1003 ¶ 36. "The source and drain regions, which are physically equivalent and therefore interchangeable, are formed by implanting dopants (either n-type or p-type) into the silicon substrate on either side of the gate electrode." *Id*. ¶ 40. "MISFETs with n-type source/drain regions are referred to as NMOS, and MISFETs with p-type source/drain regions are referred to as PMOS." *Id*. ¶ 44 (emphasis omitted).

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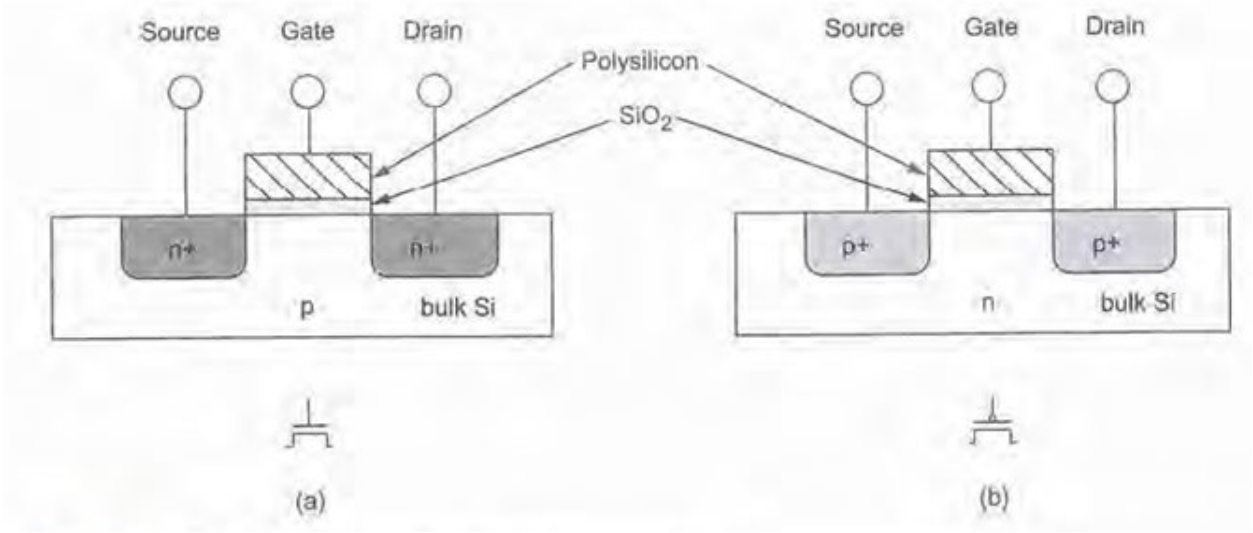
[2] Solely for purposes of demonstrating the Petition's lack of merit in this preliminary response, Patent Owner relies on the Petition's own evidence. In the event IPR is instituted, Patent Owner reserves the right to offer its own evidence, including evidence contrary to Petitioner's evidence.



Weste, Figure 1.8

As shown in Weste Figure 1.8(b) above, "a pMOS transistor requires an n-type body region" in which the transistor's source and drain are fabricated. EX1041 at 23. The CMOS fabrication process therefore typically[3] "begins with the creation of an n-well on a bare p-type silicon wafer." *Id*. at 25. More particularly, "[f]orming the n-well requires adding enough [n-type] dopants ***into the silicon substrate*** to change the substrate from p-type to n-type in the region of the well." *Id.* (emphasis added). This is accomplished "through a selective doping process known as ion implantation." EX1003 ¶ 40. In this process "dopant ions are accelerated through an electric field

[3] As will be explained *infra*, certain transistor isolation technologies perform preprocessing on the silicon wafer before this step.

and blasted ***into the substrate***." EX1041 at 25 (emphasis added).[4]

The process for forming the n-well by selectively implanting dopants into the wafer surface typically proceeds as follows. First, to define which regions of the silicon wafer are n-wells, "a protective layer of oxide [is grown] over the entire wafer" and then selectively etched using photolithography "where we want the wells." *Id*. at 25. When the ion implantation step using n-type dopants is performed, "the oxide layer prevents dopant atoms from entering the substrate where no well is intended." *Id*. However, in regions of the wafer surface that are not covered by oxide, the dopants "***enter the substrate*** and form the wells." *Id*. (emphasis added). This process is depicted graphically in Weste reference text Figure 1.36. *Id*. at 27. After the transistor's gate insulator and gate electrode have been formed, the source and drain regions can be formed in the silicon wafer (to the left and right of the gate electrode) using ion implantation, with the gate blocking the dopants from entering the channel beneath the gate. *Id*. at 28.

[4] *See also id*. at 117 ("Ion implantation involves subjecting the silicon substrate to highly energized donor or acceptor atoms. When these atoms impinge on the silicon surface, they travel below the surface of the silicon.").

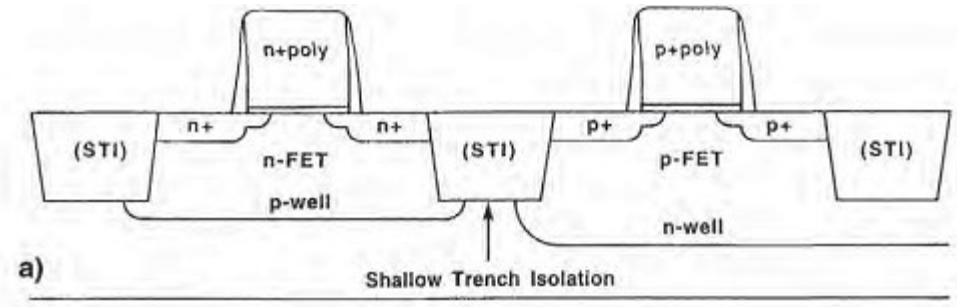
1. Transistor Isolation

Although pure crystalline silicon is a semiconductor with "bulk electrical resistance somewhere between that of a conductor and an insulator," the doping in the source and drain regions can increase their conductivity by "several orders of magnitude." *Id*. at 114. Because transistors are arranged "side by side" on the silicon wafer, EX1003 ¶ 45, to avoid undesired electrical interactions between them, "individual devices in a CMOS process need to be isolated from one another." EX1041 at 119. Moreover, because the silicon wafer is itself somewhat conductive, *id*. at 114, it can be desirable to insulate the devices from the wafer as well. As explained in detail *infra*, several techniques have been developed for electrically isolating transistors from one another and/or from the underlying silicon wafer. Importantly, and as will be described, those techniques differ in terms of whether they form the transistor's active region "in" the silicon wafer or in a layer that is deposited or grown "on" the silicon wafer surface.

a) Shallow Trench Isolation

Shallow trench isolation ("STI") is a transistor isolation approach in which "a relatively shallow trench is first etched into the Si substrate (0.3-0.5-µm deep), which is then refilled with an insulator material." EX1034 at 433. It is the isolation technology of choice "in processes at and below the 180 nm node. . . . Typical trenches in a 90 nm process can be 140 nm wide by 400 nm deep." EX1041 at 119.

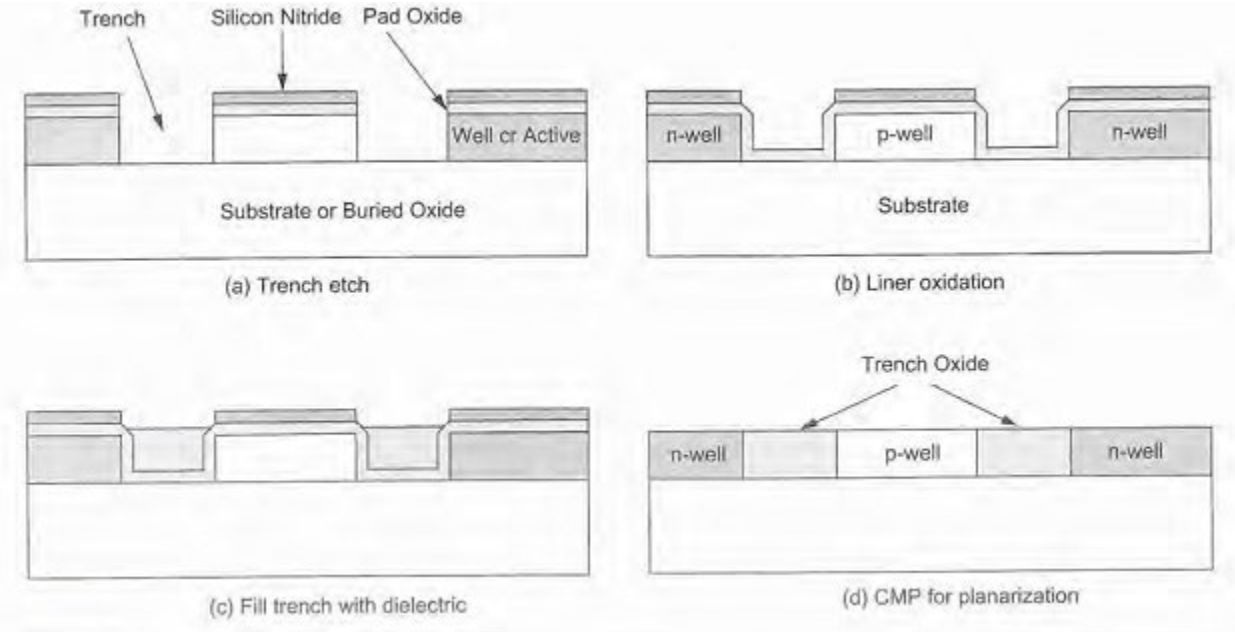
Figure 9.1(a) from Petitioner's Wolf reference textbook (below) provides a graphical representation of a cross section of pMOS and nMOS transistors fabricated using STI. EX1034 at 434. "Trench isolation [] permits nMOS and pMOS transistors to be placed closer together because the isolation provides a higher source-drain breakdown voltage." EX1041 at 119 (emphasis omitted).



Wolf, Figure 9.1(a)

As depicted in Weste Figure 3.3 (below), STI can be performed directly into the silicon wafer or in conjunction with a silicon-on-insulator process (discussed in Section II(A)(1)(b), *infra*) that employs a thin silicon layer above a buried oxide. EX1041 at 120. The STI process "starts with a pad oxide and a silicon nitride layer, which act as the masking layers." *See id.* at 119-20 (two topmost layers in Figure 3.3(a)). "Openings in the pad oxide are then used to etch into the well or substrate region (this process can also be used for source/drain diffusion)." *Id*. "A liner oxide is then grown to cover the exposed silicon." *Id*. (Figure 3.3(b)). Next, "[t]he trenches are filled with SiO_2 using CVD." *Id*. (Figure 3.3(c)). Finally, "[t]he pad oxide and nitride are removed and a *Chemical Mechanical Polishing* (CMP) step is used to

planarize the structure." *Id*. (Figure 3.3(d)).

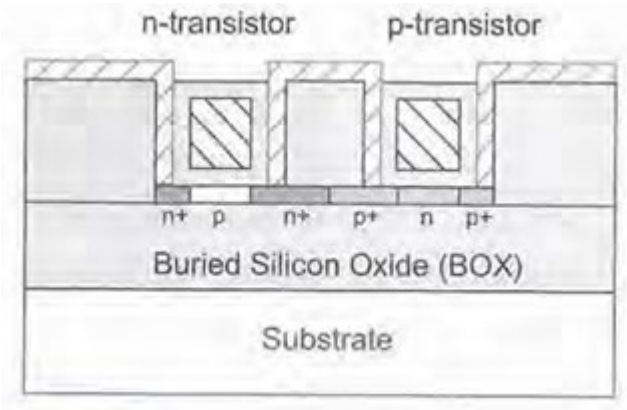


Weste, Figure 3.3

b) Silicon-On-Insulator Isolation

Silicon-on-insulator ("SOI") isolation is a "process where the transistors are fabricated on an insulator." EX1041 at 136. To accomplish this, as depicted in Figure 3.12 of Petitioner's Weste reference text (below), "a silicon substrate is used and a buried oxide (BOX) is grown ***on top of the silicon substrate***. A thin silicon layer is then grown ***on top of the buried oxide*** and this is selectively implanted to form nMOS and pMOS transistor regions. Gate, source and drain regions are then defined in a similar fashion to a bulk process." *Id*. at 137 (emphasis added and omitted). Note that, consistent with the Weste reference's description, when SOI is used, the nMOS and pMOS transistor's active regions are not "in the substrate" but rather are in the "thin

silicon layer" that is "grown on top of the buried oxide," which in turn is grown "on top of the silicon substrate." *Id*.

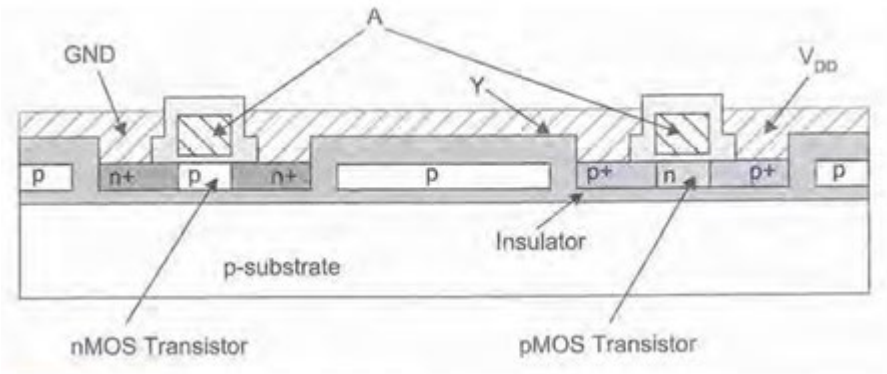


Weste, Figure 3.12

Because the foregoing process insulates the transistors from the silicon wafer below but does not provide lateral insulation between neighboring transistors located at the SOI surface, "[s]hallow trench isolation is used to surround each transistor by an oxide insulator." *Id*. at 370. As a result, "the transistor source, drain, and body are surrounded by insulating oxide rather than the conductive substrate or well (called the *bulk).*" *Id*. at 369; EX1034 at 501 (noting that, in SOI, integrated circuits are "made from single-device islands dielectrically isolated from ***the substrate*** and each other.") (emphasis added).

Weste's Figure 6.69 (below) depicts the transistor structure for a typical CMOS inverter using SOI. EX1041 at 370. Note again that the active regions of the nMOS and pMOS transistor are located in the thin silicon layer located on the insulator that is stacked on top of the substrate. Weste teaches that this approach to transistor

isolation "offers potential for higher performance and lower power consumption, but also has a higher manufacturing cost and some unusual transistor behavior that complicates circuit design." EX1041 at 369.



Weste, Figure 6.69

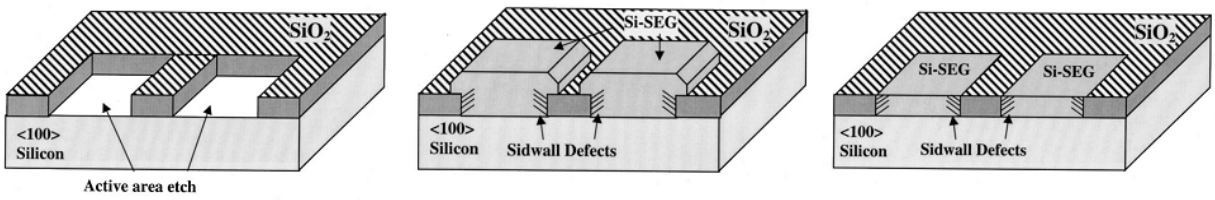
c) Selective Epitaxial Growth Isolation

Selective epitaxial[5] growth isolation ("SEGI") is an alternative to STI and SOI that affords electrical insulation between neighboring transistors through "the formation of isolated device islands." EX2038 ("Bashir")[6] at 695. Figure 4 in Bashir

[5] "Epitaxy involves growing a single-crystal film on the silicon surface." EX1041 at 117.

[6] Bashir et al., "Reduction of Sidewall Defect Induced Leakage Currents By the Use of Nitrided Field Oxides in Silicon Selective Epitaxial Growth Isolation for Advanced Ultralarge Scale Integration," J. Vac. Sci. Technol. B 18(2), pp. 695-99, March/April 2000.

"shows a typical device isolation process using selective epitaxial growth." *Id*. at 695-96. First, a film of insulating silicon dioxide is grown on the silicon wafer surface and then transistor "active regions are defined" by performing an "active area etch" of the silicon dioxide in those areas where transistors will be fabricated. *Id*. at 696 (figure caption, Figure 4a). Next, "[s]elective epitaxial growth of silicon is performed [on the exposed regions of the silicon wafer] to form the active device regions." *Id*. (figure caption, Figure 4(b)). Because "[t]he epitaxy can overgrow the insulator regions, [t]he silicon overgrowth is polished off using chemical mechanical polishing." *Id*. (figure caption, Figure 4(c)).



Bashir, Figures 4(a)-(c)

While SEGI is an alternative to STI, there are important differences. Most notably, SEGI results in active regions being "fabricated in [the] selective epitaxial silicon isolation structures." *Id*. at 699. Patent Owner is unaware of any commercially viable MISFET semiconductor device achieved through SEGI. "Defects in the near sidewall region in selective epitaxial growth of silicon have prevented its widespread use as a viable dielectric isolation technology." *Id*. at 695 (noting that the technique has not found widespread use because the epitaxial silicon "close to the sidewall

insulator can have a high defect density"). Although a method exists for addressing these high defect rates for bipolar transistors, in "the case of MOSFETs" the approach "increases the leakage between the source and drain, resulting in poor yield." *Id*.

2. High Dielectric Constant Gate Insulating Films

A "MISFET operates as a current switch, conducting current in an area between the source and drain regions, referred to as the 'channel' or the 'channel region,' when an appropriate voltage is applied to the gate electrode." EX1003 ¶ 36. The voltage on the gate electrode "modulates the electric field across the [gate] insulator." *Id*. "When [an] appropriate voltage is applied to the gate electrode, a conducting path of minority carriers [*i.e.*, holes in the case of PMOS transistors and electrons in the case of NMOS transistors] forms [in] the channel between the source and the drain, and current can flow between the source and the drain via the formed channel." *Id*. ¶ 37.

To maximize the electric field that draws minority carriers into the channel, it is desirable to maximize the capacitance of the gate insulator. For years, "silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs." *Id*. ¶ 46. The formula for the capacitance (modeling the gate insulator as a parallel plate capacitor) is:

$$C = A*\varepsilon_\tau*\varepsilon_0/t_{ox}$$

"where A is the gate insulator's area, ε_τ is the relative dielectric constant of the gate

insulator (*e.g.*, SiO_2), ε_0 is the permittivity of free space, and t_{ox} is the thickness of the gate insulator (*e.g.*, SiO_2)." *Id.* ¶ 47. Thus, the capacitance can be increased by selecting a material with a higher relative dielectric constant and/or decreasing the insulator thickness. Although the semiconductor industry initially focused on increasing the capacitance by shrinking the thickness of SiO_2 gate insulators, eventually the thickness decreased to the point where electron tunneling leakage current between the gate and channel became problematic. *Id.* ¶ 46.

Accordingly, the semiconductor industry began using high dielectric constant ("Hi-K") materials for the gate insulator because, as the above formula suggests, these materials allow the same capacitance to be achieved as SiO_2 but with a thicker film that reduces the problematic tunneling current. *Id.* ¶ 47 ("'[A]n alternative way of increasing the capacitance is to use an insulator [a gate insulator] with a higher relative dielectric constant than SiO2 […].' And because the dielectric would have a higher dielectric constant (*i.e.*, a higher k value), this high-k dielectric could be thicker than SiO_2 and still achieve the same or higher capacitance value.") (internal citation omitted).

B. The '180 Patent Invention

The '180 patent was invented and developed by Junji Hirase, Akio Sebe, Naoki Kotani, Gen Okazaki, Kazuhiko Aida, and Shinji Takeoka of Panasonic Corporation, EX1001 at 1, a leader and pioneer in the development and manufacture of electronic

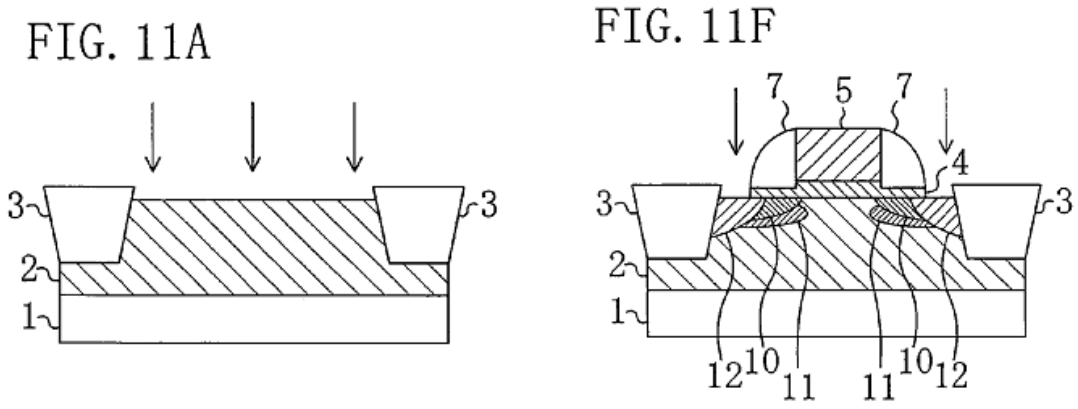
equipment including semiconductors and cameras. The patent claims priority from a foreign application filed August 5, 2005 and issued on August 28, 2012. *Id*.

The ’180 patent “relates to a structure of a MISFET (metal insulator semiconductor field-effect transistor) and a method for fabricating the MISFET and, more particularly, relates to techniques for improving the driving power and reliability of a MISFET.” EX1001 at 1:17-23. It has 22 claims, one of which—claim 1—is an independent claim. *Id*. at 21:9-22:52. Independent claim 1 recites “an active region ***in*** a substrate.” *Id*. at 21:10-11 (claim 1) (emphasis added). Thus, all claims in the ’180 patent require, directly or by dependency, this feature.

Although the ’180 patent has several points of novelty over Petitioner’s references, for purposes of this preliminary response Patent Owner will focus on its isolation technology and the relationship between its gate insulating film and sidewall structure. <u>First</u>, the ’180 patent teaches STI as its preferred transistor isolation technology. *Id*. at 5:65-66 (discussing the first embodiment); *id*. at 7:30-31 (discussing the second embodiment); *id*. at 10:21-23 (discussing the third embodiment); *id*. at 13:17-21 (discussing fifth embodiment); *id*. at 14:56-60 (discussing sixth embodiment); *id*. at 16:43-47 (discussing the seventh embodiment); *id*. at 18:22-26 (discussing the eighth embodiment). Although the term “STI” does not appear in the discussion of the fourth embodiment or modified fourth embodiment, *id*. at 11:48-13:6, Figure 9 corresponding to the fourth embodiment, *id*.

at 11:58-62, depicts STI element 3. Each of the preferred embodiments in the ’180 patent shows a finished MISFET with STI element 3 providing electrical isolation between neighboring transistors. *Id*. at Figures 1-15D.

Figures 11A and 11F (replicated below) corresponding to the ’180 patent’s fifth embodiment provides an example of how STI followed by ion implantation results in the formation of an active region ***in*** the substrate. First, as shown in Figure 11A, after “a STI 3 which is to be an isolation region is selectively formed[,] . . . B (boron) is ion implanted ***into the substrate 1*** [such that] a p-type well 2 which is to be an active region is formed.” *Id*. at 13:17-22 (emphasis added). Then, as shown in Figure 11F, after several additional processing steps, “As (arsenic) is ion implanted ***into the substrate 1*** . . . [and] n-type source/drain regions 12 are formed.” *Id*. at 13:63-14:2 (emphasis added).



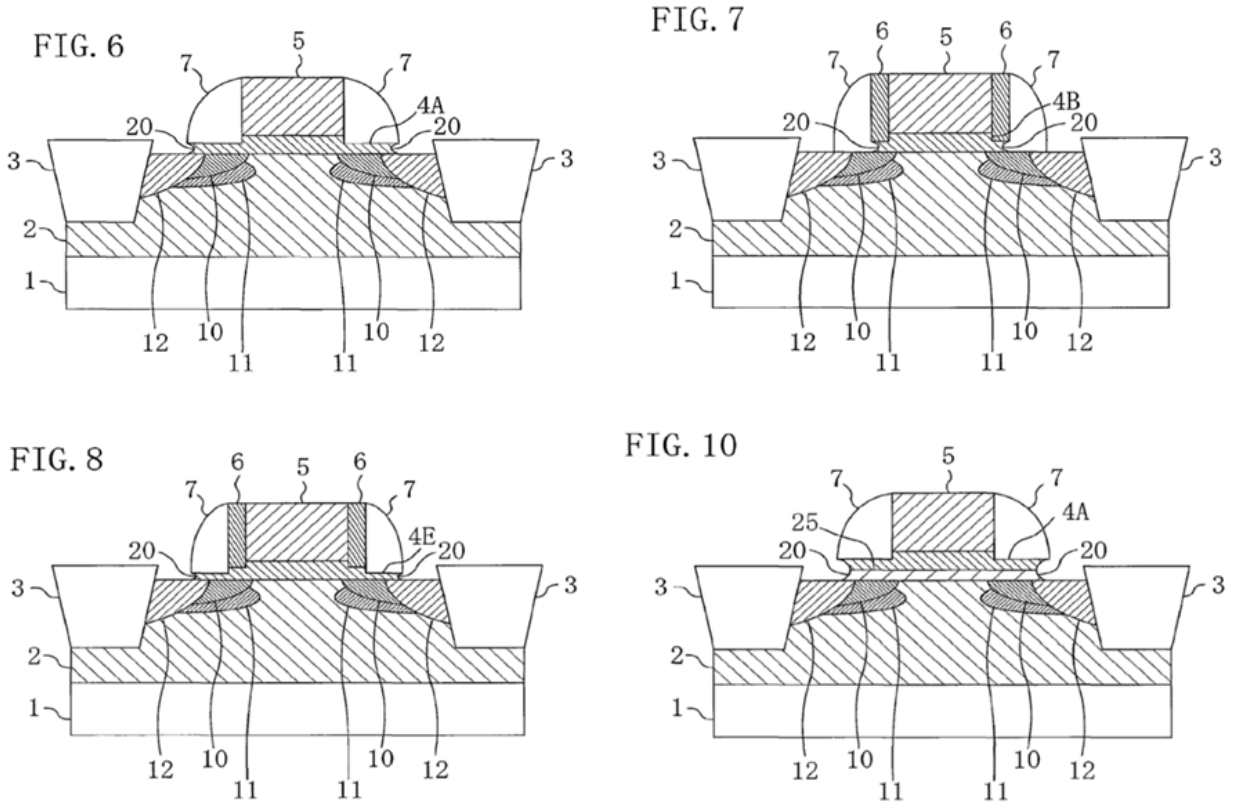
EX1001, Figures 11A and 11F

Second, the patent's inventors recognized that while Hi-K materials enable greater capacitance across the gate-channel interface, they also create new challenges. First, if the Hi-K gate insulating film terminates at the interface between the gate electrode's outer end and the SiO_2 gate sidewall's inner end (*i.e.*, "at gate electrode end part"), a "reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film" occurs and the "device characteristics of the MISFET are deteriorated and the reliability of the gate insulating film is degraded." *Id*. at 1:63-2:7. Second, the inventors also appreciated the importance of minimizing the "capacitance between a gate and a drain . . . so that adverse effects on circuit speed can be reduced." *Id*. at 4:51-54. Extending the Hi-K insulating film under the gate sidewall all the way to the source/drain electrodes increases the capacitance between the gate and source/drain electrodes. *Id.* at 6:51-57.

The inventors discovered that one technique for addressing both issues involves allowing the Hi-K gate insulating film to extend under the gate sidewall (thereby alleviating the first problem) but not all the way to its outer end (thereby alleviating the second problem). Thus, the '180 Patent claims a locational relationship between the MISFET's "high dielectric constant gate insulating film" and the "insulating sidewall formed on each side surface of the gate electrode." *Id.* at claim 1. More specifically, claim 1 (and therefore also its dependent claims) requires that "an end of the high dielectric constant gate insulating film under the insulating

sidewall is located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode. " ("the Outer End Limitation"). *Id*. at 21:9-22:52.

The '180 patent teaches four embodiments exemplifying the Outer End Limitation, and these are depicted graphically in Figures 6, 7, 8 and 10 below. In each figure, the patent refers to the portion of the gate insulating film that is recessed relative to the outer end of the insulating sidewall as notch 20. *See id.* at 7:4-9, 8:31-36, 11:37-42, 12:44-50.



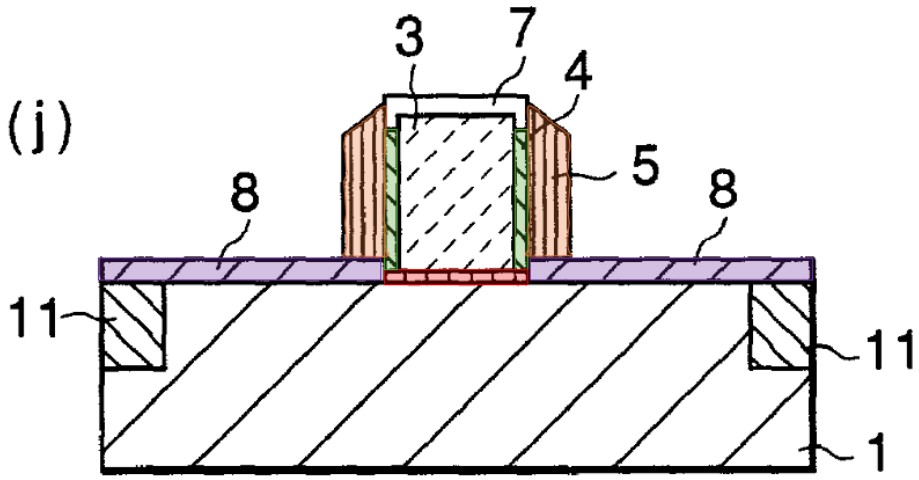
EX1001, Figures 6, 7, 8, and 10

C. Petitioner's Primary References

1. Kamata

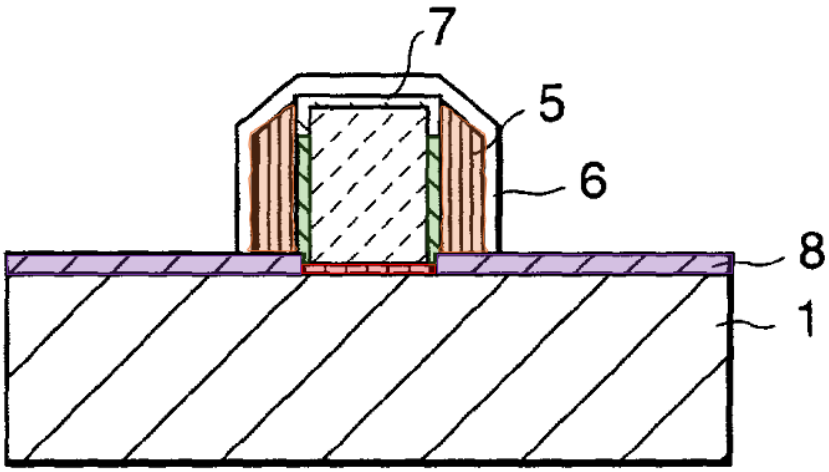
Kamata is directed to "an MIS type semiconductor device having an elevated source/drain structure and a method of manufacturing the same." EX1027 ¶ [0003]. The Petition's theories focus on Kamata's first, fourth and ninth embodiments as reflected in Figures 1B(j), 5(c), and 10(b), respectively. Petition at 18. Accordingly, Patent Owner's analysis centers on these same embodiments and figures.

Annotated Kamata Figure 1B(j) below depicts a MISFET transistor design having two sidewall components (green sidewall film 4 and orange sidewall film 5), a red gate insulating film (unnumbered), and purple elevated source drain regions 8. EX1027 ¶ [0050]. In Kamata's first embodiment, the two sidewall films have two "outer ends"—namely, the "outer end" of the green insulating film 4 and the "outer end" of the orange insulating film 5. Of these two, the "outer end" of the sidewall structure directly on the red gate insulating film is flush with the end of the orange insulating film (*i.e.*, the red gate insulating film is not recessed from the outer end of the green sidewall film 4 toward the gate electrode). Having the end of the gate insulating film flush with the end of the insulating sidewall is contrary to what the '180 patent inventors proposed and claimed, reflecting that Kamata does not teach or appreciate the significance of the '180 patent's invention.



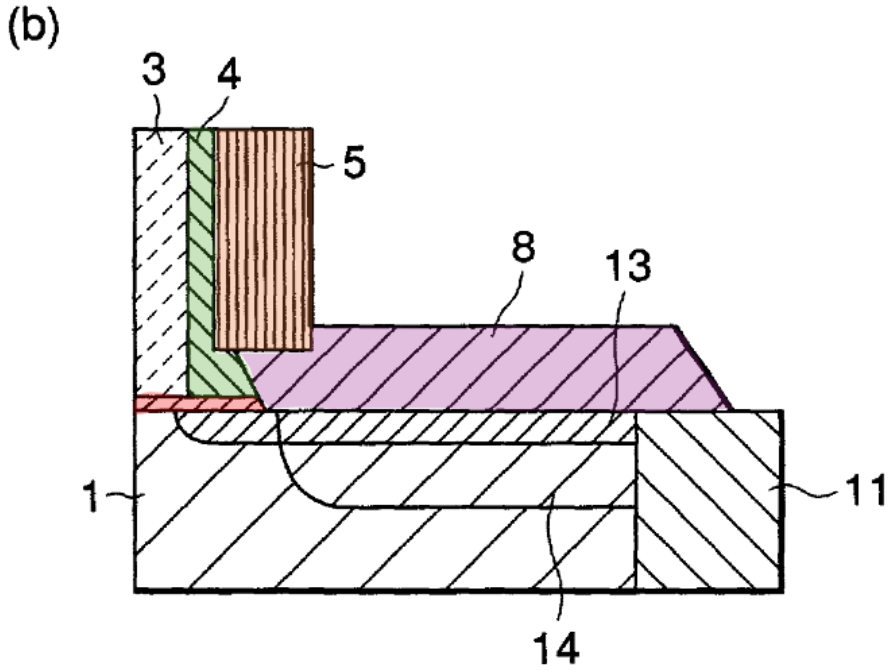
Kamata, Figure 1B(j) (annotated)

Annotated Kamata Figure 5(c) depicts a MISFET transistor design having two sidewall components (green sidewall film 4 [numbered in Figure 5(b)] and orange sidewall film 5), a red gate insulating film (unnumbered), and purple elevated source drain regions 8. EX1027 ¶¶ [0050], [0068]. In Kamata's fourth embodiment, the two sidewall films have two "outer ends"—namely, the outer end of insulating film 4 and the outer end of insulating film 5. Of these two, the outer end of the sidewall component directly on the gate insulating film is flush with the end of the insulating film (*i.e.*, the red gate insulating film is not recessed from the outer end of the green sidewall film 4 toward the gate electrode). Again, Kamata's teaching of the ends of the insulating sidewall and gate insulating film being flush is contrary to the claimed invention.



Kamata, Figure 5(c) (annotated)

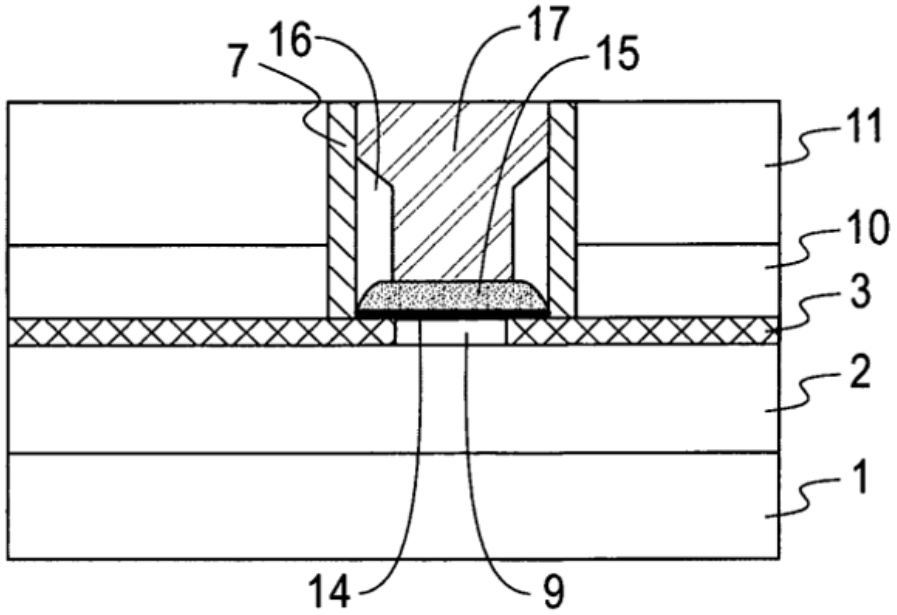
Annotated Kamata Figure 10(b) depicts a MISFET transistor design having two sidewall components (green sidewall film 4 and orange sidewall film 5), a red gate insulating film (unnumbered), and purple elevated source/drain region 8. EX1027 ¶ [0093]. Kamata's ninth embodiment has a multiplicity of outer ends of insulating film 4 and insulating film 5. The end of the red gate insulating film extends beyond the outer end of the sidewall component directly on the gate insulating film (*i.e.*, the red gate insulating film 5 is not recessed from the outer end of the green sidewall film 4 toward the gate electrode).



Kamata, Figure 10(b) (annotated)

2. Guha

Guha is directed to "a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device." EX1028 ¶ [0001]. The Petition's theories focus on Guha's Figure 12 (reproduced below) and corresponding text. Petition at 59-69. Accordingly, Patent Owner's analysis centers on this same figure.



Guha, Figure 12

Figure 12 reflects the "resulting device," EX1028 ¶ [0045], from a series of process steps. This device employs "a silicon-on-insulator (SOI) structure, where the channel layer **3** is provided over a buried oxide layer **2**," which in turn is on "substrate **1**." *Id*. ¶ [0022]. The SOI process involves "deposit[ing]" channel layer 3 on the buried oxide layer: "The channel layer **3** can be formed by a conventional ***deposition*** process including, for example, chemical vapor deposition (CVD), plasma-assisted CVD, evaporation or chemical solution deposition." *Id*. ¶ [0023] (emphasis added).

The Petition asserts that the "active region" is in channel layer 3, Petition at 60-61,[7] and Guha teaches that "[c]hannel layer **3** is disposed ***over*** substrate **1,** and

[7] Guha teaches that "source/drain extensions, also referred to as source/drain (S/D).

comprises channel **9,** source extension **3a** and drain extension **3b**," EX1028 ¶ [0046] (emphasis added). Thus, by the Petition's own admission, Guha's active region is "over substrate **1**" rather than "in substrate **1**."

3. Matsumoto

Matsumoto teaches "a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) employing an SOI (Silicon-On-Insulator) substrate and a method of manufacturing the same." EX1009 ¶ [0002]. The Petition's theories focus on Matsumoto's fourth embodiment MOSFET. Petition at 82. Matsumoto Figure 22 corresponds to the fourth embodiment. *Id*. ¶ [0137]. Accordingly, Patent Owner addresses Figure 22 and the fourth embodiment.

Matsumoto's fourth embodiment, as reflected in Figure 22 (below), uses a "multi-layer structure such that a silicon substrate **1**, a BOX layer **2** and a single-crystalline silicon layer **3** are stacked in the order named." EX1009 ¶ [0102]. The source, drain, and body region are located in silicon layer **3,** ***not*** in the silicon substrate **1**. *Id*. ¶ [0139] ("Referring to FIG. 22, the source/drain regions **10** are formed in the silicon layer **3** by an ion implantation process.").

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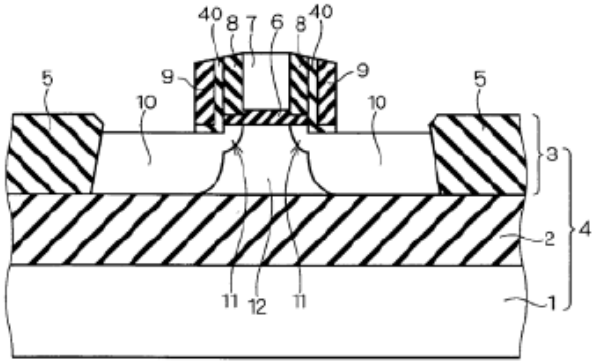
junctions, are formed by implanting dopants through the pad protection layer **4** ***into the channel layer 3***, with the dummy gate **5** acting as an implantation mask." EX1028 ¶ [0026] (emphasis added).



Matsumoto, Figure 22

D. The Level of Ordinary Skill in the Art

Petitioner asserts that a person of ordinary skill in the art ("POSA") "would have had at least a Master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education." Petition at 18 (internal citation omitted). It is unnecessary for Patent Owner to propose a competing definition at this time because, even under Petitioner's proposed definition, Petitioner has failed to demonstrate a reasonable likelihood of success on any of the challenged claims. Patent Owner reserves the right to propose a different POSA definition if the Board institutes IPR.

III. LEGAL STANDARDS

"In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (noting 35 U.S.C. § 312(a)(3) requires that petitions must identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim"). To meet this burden, "the petition must specify where ***each element of the claim*** is found in the prior art patents or printed publications relied upon." 37 C.F.R. § 42.104(b)(4) (emphasis added). And "the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The burden of persuasion on the petitioner never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Applying the foregoing substantive standards and burdens, "[t]he Director may not authorize an *inter partes* review to be instituted unless the Director determines . . . that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

IV. CLAIM CONSTRUCTION

"[A] petition ***must*** state how a challenged claim is to be construed and how each element of the construed claim is found in prior art patents or printed

publications." *Samsung Electronics Co., Ltd. v. Blaze Mobile, Inc.*, IPR2021-01569, Paper 16, at 5 (citing 37 C.F.R. §§ 42.104(b)(3)-(4)) (emphasis added). Here, Petitioner flouted that requirement by not offering any proposed constructions for any claim terms in the '180 patent. Petition at 17.

Nevertheless, Petitioner, its expert, and Weste all assert that the claim term "substrate" means "silicon wafer." First, Weste repeatedly teaches that the "silicon wafer" is "called the substrate." EX1041 at 8 ("[T]he ***silicon wafer*** [is] also called the ***substrate***, body, or bulk.") (emphasis added); *id*. at 23 ("Transistors are fabricated on thin ***silicon wafers . . . called the substrate***."). EX1041 at 23 (emphasis added). Second, Petitioner's expert also equates the terms "silicon wafer" and "substrate." EX1003 ¶ 38 ("MISFETs are fabricated on ***silicon wafers*** that serve as the ***substrate***.") (emphasis added); EX1003 (Lee Decl.) ¶ 36 (quoting the Weste reference text for the principle that the "silicon wafer [is] also called the substrate, body or bulk"). Third, in one of its sister petitions, Petitioner treats the terms "silicon wafer" and "substrate" as synonymous. *Taiwan Semiconductor Manufacturing Co., Ltd v. Advanced Integrated Circuit Process LLC*, IPR2025-00832, Paper 2 at 3 ("A metal-insulating-semiconductor transistor (MISFET or MOSFET) generally includes . . . '***the silicon wafer, also called the substrate***, body or bulk.'") (emphasis added) (quoting Weste).

Patent Owner need not formally adopt a position on the proper meaning of "substrate" in the context of the '180 patent at this time. At this stage, the relevant question is whether the Petition has met ***its burden*** of showing a "reasonable likelihood" of success under 35 U.S.C. § 314(a). Because Petitioner has not complied with its obligation under 37 C.F.R. § 42.104(b)(3) to propose a construction for "substrate" but has introduced evidence supporting the conclusion that "substrate" means "silicon wafer," Patent Owner relies on that meaning solely for purposes of rebutting the Petition's theories. In the event the Board institutes *inter partes* review on the Petition, Patent Owner reserves the right to advance and substantiate constructions for any terms in the '180 patent, including the term "substrate."

If IPR is instituted, Petitioner has no right to assert "substrate" means something other than what its expert and reference text say—namely, "silicon wafer." First, "the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *In re Magnum Oil*, 829 F.3d at 1381. Here, Petitioner waived any right to offer a different construction for substrate by not proposing any construction, Petition at 18, and then offering evidence supporting the conclusion that "substrate" means "silicon wafer." Second, even if Petitioner were now permitted to argue that "substrate" means something other than "silicon wafer," this would only highlight "Petitioner's failure to provide an interpretation in the face of claim language that is admittedly [per Petitioner]

subject to some range of interpretations." *DJI Europe B.V. v. Textron Innovations Inc.*, IPR2023-01107, Paper 14 at 7 (PTAB February 13, 2024).

With regard to the Outer End Limitation, when "a patent 'repeatedly and consistently' characterizes a claim term in a particular way, it is proper to construe the claim term in accordance with that characterization." *Wis. Alumni Research Found. v. Apple Inc.*, 905 F.3d 1341, 1351 (Fed. Cir. 2018) (quoting *GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1370 (Fed. Cir. 2016)). It was therefore incumbent upon Petitioner to consider whether the '180 patent's written description used claim terms that way. *Samsung Electronics Co., Ltd. v. Blaze Mobile, Inc.*, IPR2021-01569, Paper 16, at 5 ("[A] petition ***must*** state how a challenged claim is to be construed. . . ." (PTAB March 22, 2022) (emphasis added). Here, Petitioner flouted that requirement. Petition at 17.

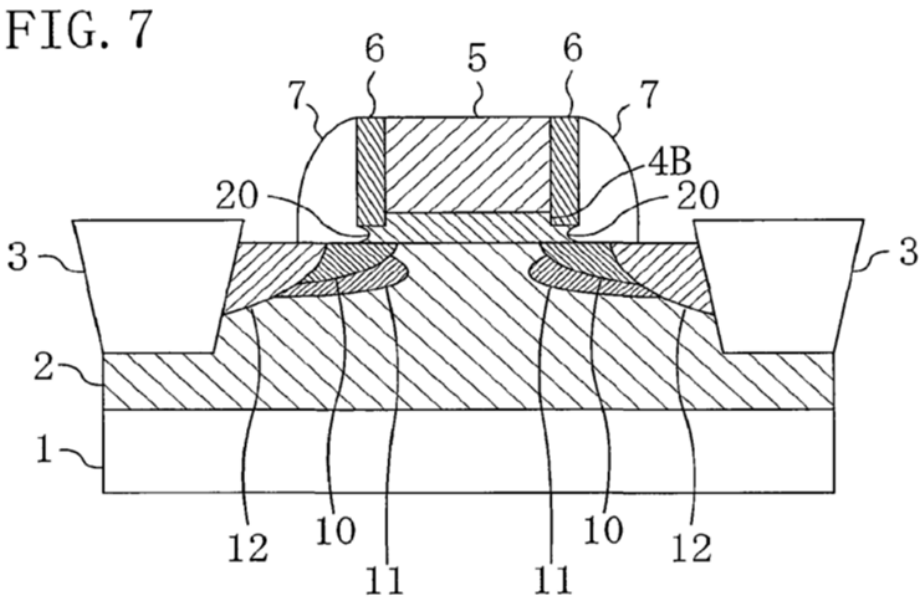
As the Petition acknowledges, the '180 patent uses the term "insulating sidewall" differently, depending on the context. Petition at 25 n.9 ("The '180 patent uses the term 'insulating sidewall' to refer to a single component (6:3-4), a collective structure of two components (3:25-30), and as a component having multiple layers (20:43-52)"). As one example of the first and second use, the '180 Patent states that "the insulating ***sidewall*** ***may include a first insulating*** ***sidewall*** formed on a side surface of the gate electrode and ***a second insulating*** ***sidewall*** formed on the side surface of the gate electrode with the first insulating sidewall interposed there

between." EX1001 at 2:58-63 (emphasis added). In this sentence, the noun "sidewall" in the terms "first insulating ***sidewall***" and "second insulating ***sidewall***" refers to ***sidewall components*** whereas the noun sidewall in the term "the insulating ***sidewall***" refers to a collective structure of two components (*i.e.*, the two referenced sidewall components).

Although the '180 patent uses the term "insulating sidewall" differently, that is not so with respect to references to the Outer End Limitation in the four exemplary embodiments. There, as explained below, the '180 patent consistently references the "outer end of the outermost sidewall component that is directly on the gate insulating film." And the patent teaches that the relevant sidewall is "in direct contact" with the gate insulating film. EX1001 at 1:63-66; 4:43-48.

First, Figure 7 and its accompanying text provide the best example. Figure 7 (reproduced below) depicts a "Modified Example of the Second Embodiment." EX1001 at 8:23-30. Although Figure 7 includes two sidewall components—namely, offset sidewall 6 and sidewall 7, the text describes the relevant locational relationship as between high dielectric constant gate insulating film 4B and ***offset sidewall 6, not sidewall 7 or the multilayer sidewall structure***: "As shown in FIG. 7, this modified example is different from the second embodiment is that part of a high dielectric constant gate insulating film 4B located under each side end portion of the ***offset sidewall 6***, i.e., a side portion of the high dielectric constant gate insulating film 4B

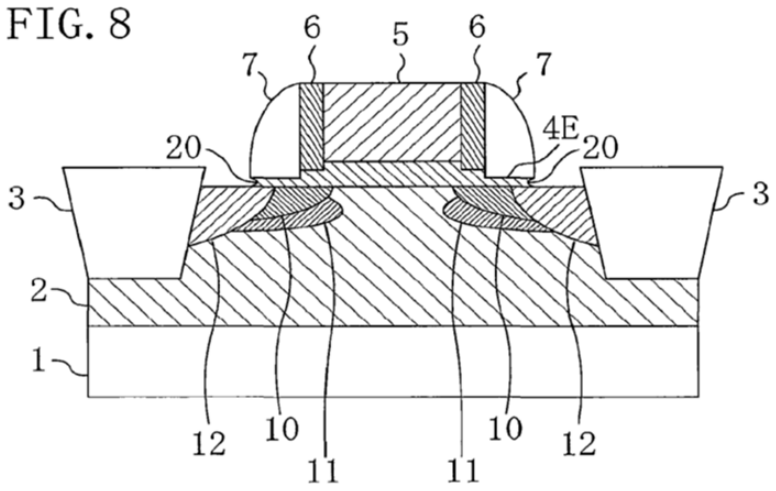
is removed in a notch shape, so that a notch 20 is provided." *Id*. at 8:31-36 (emphasis added). Thus, in this embodiment, the text identifies the relevant "outer end" as the outer end of the outermost sidewall component that is directly on the gate insulating film (*i.e.*, offset sidewall 6).



EX1001, Figure 7

Second, Figure 8 (shown below) depicts a "modified example of the third embodiment." EX1001 at 11:33-36. Figure 8 is similar to Figure 7 except that the high dielectric constant gate insulating film 4B exists under both (inner) offset sidewall 6 and (outer) sidewall 7. Importantly—and unlike the text corresponding to Figure 7—the text corresponding to Figure 8 describes the relevant locational relationship as between high dielectric constant gate insulating film 4B and ***sidewall 7, not offset sidewall 6*** as was the case for Figure 7: "As shown in FIG. 8, this

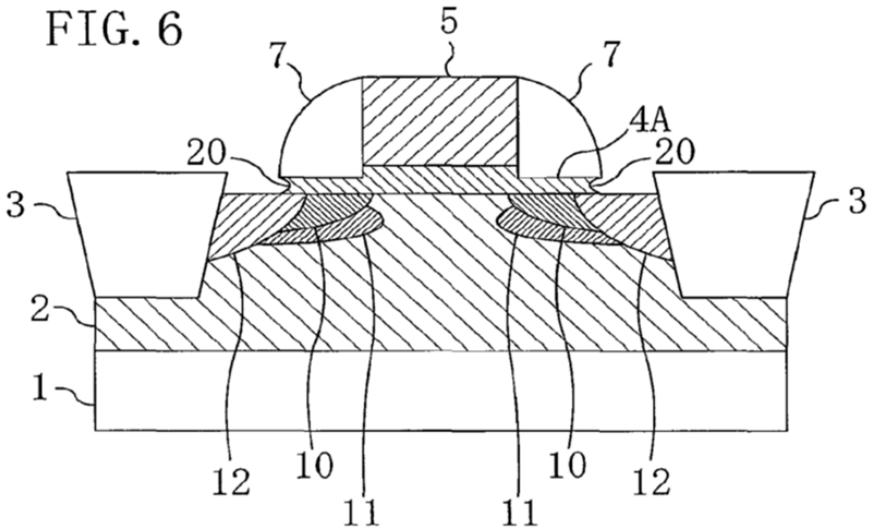
modified example is different from the first embodiment in that part of a high dielectric constant gate insulating film 4E located under each side end portion of a ***sidewall 7***, i.e., a side portion of the high dielectric constant gate insulating film 4E is removed in a notch shape, so that a notch 20 is provided." *Id*. at 11:37-42 (emphasis added). Thus, like Figure 7's text, Figure 8's text focuses on the outer end of the outermost sidewall component that is directly on the gate insulating film [*i.e.*, sidewall 7 in Figure 8 versus sidewall 6 in Figure 7].



EX1001, Figure 8

Third, Figure 6 (reproduced below) depicts a "Modified Example of the First Embodiment." *Id.* at 6:67-7:3. Figure 6 includes a single sidewall component—namely, sidewall 7—and the text describes the relevant locational relationship as between high dielectric constant gate insulating film 4B and that single sidewall component: "[T]his modified example is different from the first embodiment in that

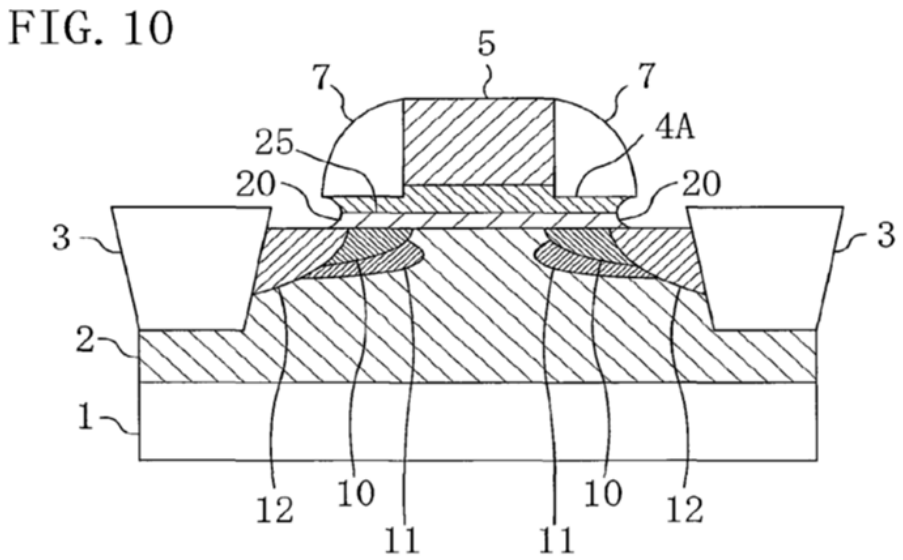
part of a high dielectric constant gate insulating film 4A located under each side end portion of a sidewall 7, i.e., a side portion of the high dielectric constant gate insulating film 4A is removed in a notch shape, so that a notch 20 is provided." *Id*. at 7:4-9. The text corresponding to Figure 6 is thus consistent with the relevant "outer end" being the outer end of the outermost sidewall component (*i.e.*, sidewall 7) that is directly on the gate insulating film.



EX1001, Figure 6

Fourth, Figure 10 (reproduced below) depicts a "modified example of the fourth embodiment." *Id*. at 12:37-43. Figure 10 includes a single sidewall component—namely, sidewall 7—and the text describes the relevant locational relationship as between high dielectric constant gate insulating film 4B and that single sidewall component: "As shown in FIG. 10, this modified example is different from the fourth embodiment in that part of a laminated insulating film of a high dielectric

constant gate insulating film 4A and a buffer insulating film 25 located under a side end portion of each sidewall 7, i.e., a side end portion of the laminated insulating film is removed in a notch shape, so that a notch 20 is provided." *Id*. at 12:44-50. This text too is consistent with the relevant "outer end" being the outer end of the outermost sidewall component [*i.e.*, sidewall 7] that is directly on the gate insulating film.



EX1001, Figure 10

Like the term "substrate," Petitioner may now seek to propose a construction for the Outer End Limitation. The Board should ignore any such proposal. First, the regulations dictate a process in which the Petitioner offers claim construction proposals in the Petition, 37 C.F.R. § 42.104(b)(3), and the Patent Owner responds to those proposals. Petitioner will be seeking to turn that process on its head if it waits for Patent Owner to propose claim constructions and then seeks to respond to those

constructions. Second, the Petition itself reflects that Patent Owner's proposed construction for the Outer End Limitation was not only entirely foreseeable, but correct. The Petition asserts that Guha teaches a multicomponent sidewall structure. Petition at 64. The Petition then asserts a theory under which the relevant "outer end" is the "outer end of spacer 16." Petition at 68. Guha's spacer 16 is the "outermost sidewall component that is directly on the gate insulating film" consistent with Patent Owner's proposed construction. *Id*. Thus, the Petition anticipated Patent Owner's proposed construction but nevertheless did not advance a specific construction.

V. ARGUMENT

The Petition fails to show a reasonable likelihood of prevailing on any claim, under any Ground. As discussed below, Petitioner fails to meet the threshold for institution on claim 1—the sole independent claim in the '180 patent—for every Ground challenging claim 1 (*i.e.*, Grounds 1, 8, and 11). Because Petitioner's other Grounds relating to the dependent claims rely on the theories presented for claim 1, the Petition's deficiencies with respect to claim 1 are fatal as to all Grounds.[8]

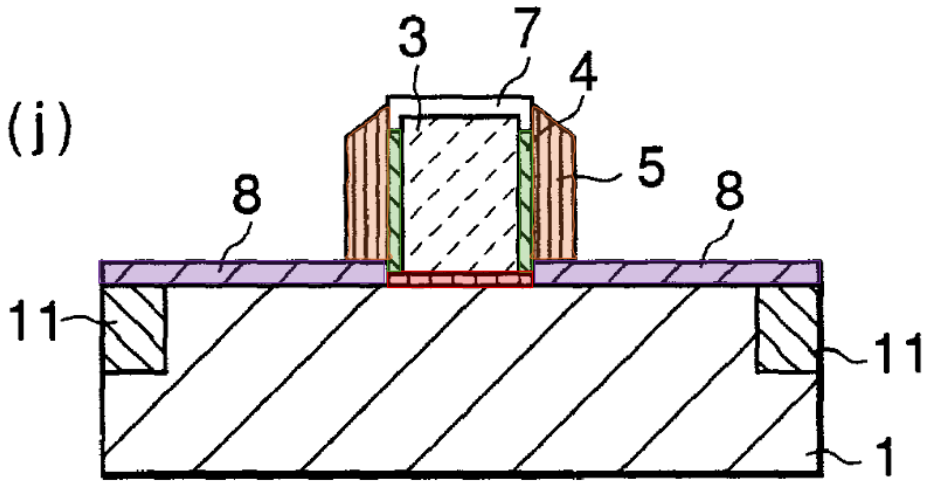
[8] Because each of the Petition's grounds fail for the reasons set forth below, Patent Owner need not address the other flaws in the Petition's theories. In the event of institution, Patent Owner reserves the right to argue each of those infirmities.

A. Grounds 1-7 Fail Because Kamata Does Not Teach the Outer End Limitation

Ground 1, and therefore also Grounds 2-7, fail because the Petition fails to show that Kamata teaches "the Outer End Limitation," which is required directly or by dependency in each claim in the '180 patent. EX1001 at 21:9-22:52. Although the Petition offers no proposed construction for the claim term "outer end of the insulating sidewall," Petition at 17, that construction is critical because each of Kamata's relevant embodiments employs a plurality of sidewall components and a plurality of outer ends. As explained in Section IV, *supra*, the term "outer end of the insulating sidewall" is properly construed to mean "outer end of the outermost sidewall component that is directly on the gate insulating film." Applying this construction, Kamata does not render obvious any of the claims in the '180 patent.

The Petition's theories focus on Kamata's first, fourth and ninth embodiments as reflected in Figures 1B(j), 5(c), and 10(b), respectively. Petition at 18. Accordingly, Patent Owner's analysis centers on these same embodiments and figures. First, annotated Kamata Figure 1B(j) depicts a MISFET transistor design having two sidewall components (green sidewall film 4 and orange sidewall film 5), a red gate insulating film (unnumbered), and purple elevated source drain regions 8. EX1027 ¶ [0050]. The relevant "outer end of the insulating sidewall"—namely, the outer end of the outermost sidewall component that is directly on the gate insulating

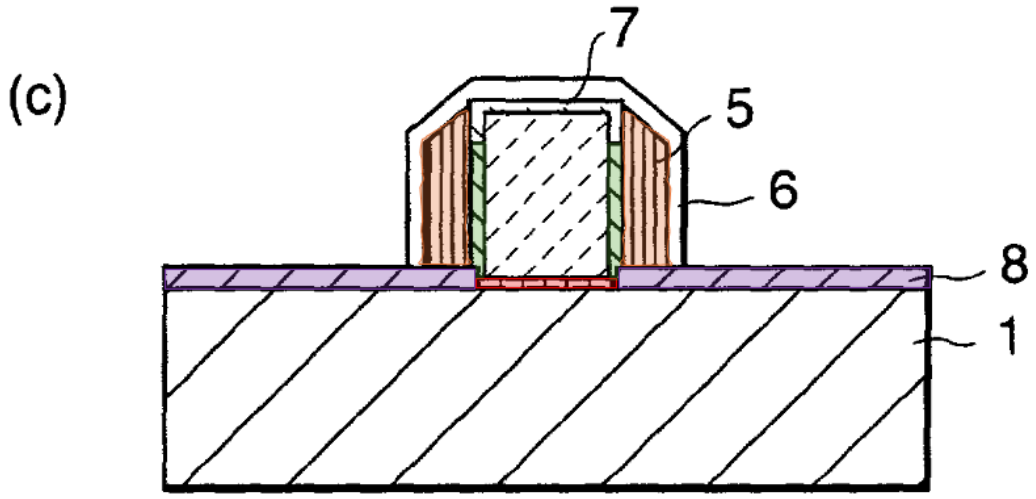
film—is the outer end of green sidewall film 4. In Kamata's first embodiment, the "end of the [] gate insulating film" is not "located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode," as required by claim 1, because the outer end of the green sidewall film 4 is flush with the end of the red gate insulating film.



Kamata, Figure 1B(j)

Second, annotated Kamata Figure 5(c) depicts a MISFET transistor design having two sidewall components (green sidewall film 4 [numbered in Figure 5(b)] and orange sidewall film 5), a red gate insulating film (unnumbered), and purple elevated source drain regions 8. EX1027 ¶¶ [0050], [0068]. The relevant "outer end of the insulating sidewall"—namely, the outer end of the outermost sidewall component that is directly on the gate insulating film—is again the outer end of green sidewall film 4 just above the red gate insulating film. In Kamata's fourth

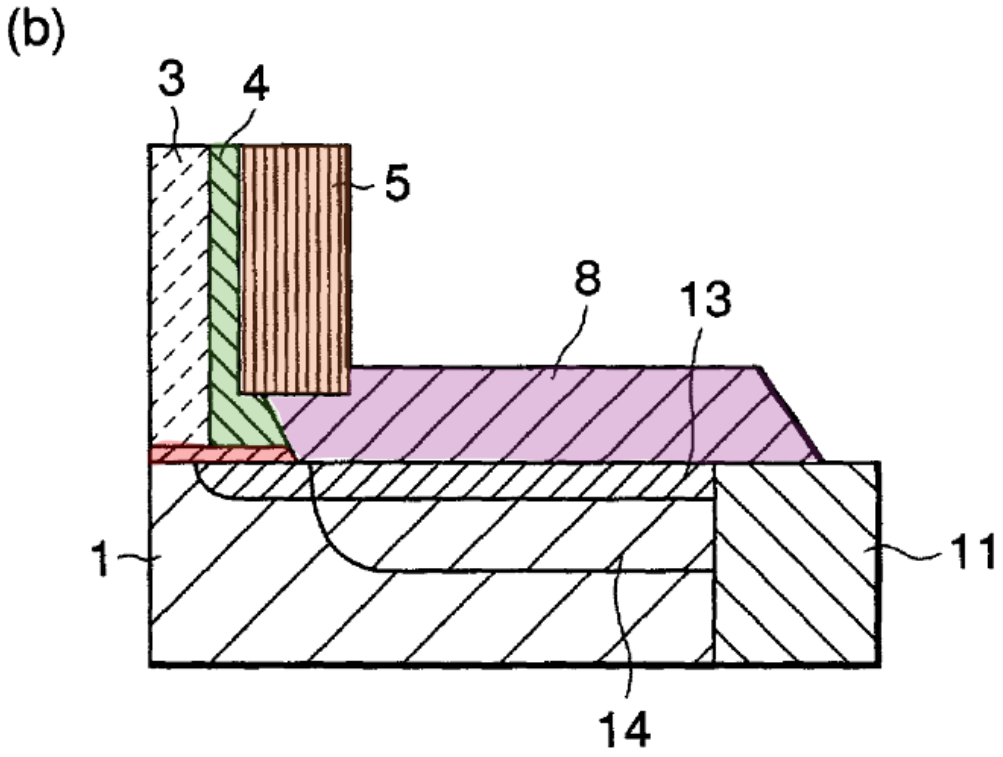
embodiment, the "end of the [] gate insulating film" is not "located at a predetermined distance from an outer end of the insulating sidewall toward the gate electrode," as required by claim 1, because the outer end of the green sidewall film 4 above the red gate insulating film is flush with the end of the red gate insulating film.



Kamata, Figure 5(c)

Third, annotated Kamata Figure 10(b) depicts a MISFET transistor design having two sidewall components (green sidewall film 4 and orange sidewall film 5), a red gate insulating film (unnumbered), and purple elevated source/drain region 8. EX1027 ¶¶ [0050], [0093]-[0094]. The relevant "outer end of the insulating sidewall"—namely, the outer end of the outermost sidewall component that is directly on the gate insulating film—is again the outer end of green sidewall film 4 just above the gate insulating film. In Kamata's ninth embodiment, the "end of the [] gate insulating film" is not "located at a predetermined distance from an outer end of

the insulating sidewall ***toward*** ***the gate electrode***," as required by claim 1, because the outer end of the red gate insulating film extends beyond the outer end of the green sidewall film 4 ***away*** ***from the gate electrode***.



Kamata, Figure 10(b)

Thus, Ground 1 fails because each of the Kamata embodiments on which the Petition relies fails to teach the "Outer End Limitation" recited directly or by dependency in each of the '180 patent claims.

Each of Grounds 2-7 fails because each relies on the evidence in Ground 1 to establish that Kamata teaches the Outer End Limitation. Petition at 42-45 (as to Ground 2, relying upon secondary reference Wang solely for its teaching of

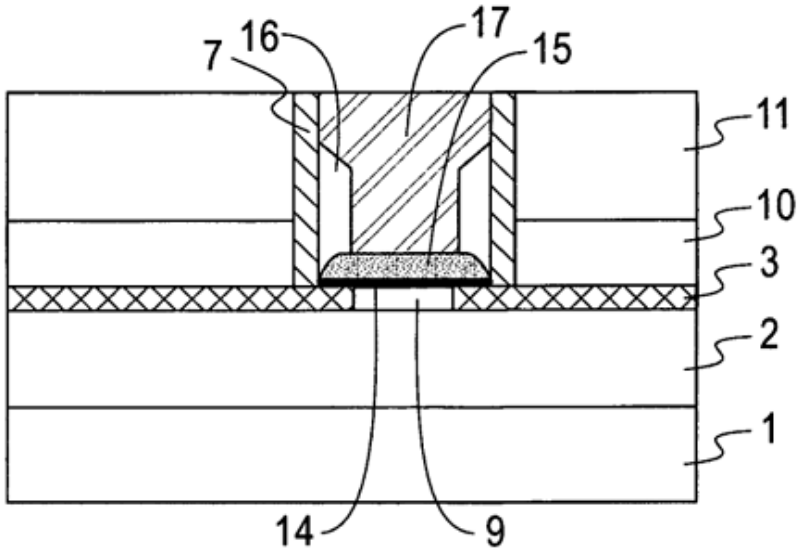
dependent claim limitations in claims 4 and 12); Petition at 45-47 (as to Ground 3, relying upon secondary reference Koyama solely for its teaching of a dependent claim limitation in claim 7); Petition at 47-52 (as to Ground 4, relying upon secondary reference Rodder solely for its teaching of dependent claim limitations in claim 8-9); Petition at 52-54 (as to Ground 5, relying upon secondary reference Sim solely for its teaching of a dependent claim limitation in claim 11); Petition at 54-56 (as to Ground 6, relying upon secondary reference Wilk solely for its teaching of dependent claim limitations in claims 18-19); Petition at 56-59 (as to Ground 7, relying upon secondary reference Takayanagi solely for its teaching of a dependent claim limitation in claim 20).

B. Grounds 8-10 Fail Because Guha Does Not Teach an "Active Region In a Substrate"

Ground 8, and therefore also Grounds 9-10, fail because, simply accepting as true Petitioner's own record, Guha does not teach "an active region in a substrate," a limitation required directly or by dependency in each claim in the '180 patent. EX1001 at 21:9-22:52. Although the Petition offers no proposed construction for the claim term "substrate," Petition at 17, Petitioner's evidence and argument support the conclusion that "substrate" means "silicon wafer." *See* Section IV, *supra*. As explained *infra*, applying this meaning, Guha does not teach forming transistor active regions "in" the substrate but rather teaches forming an SOI structure having

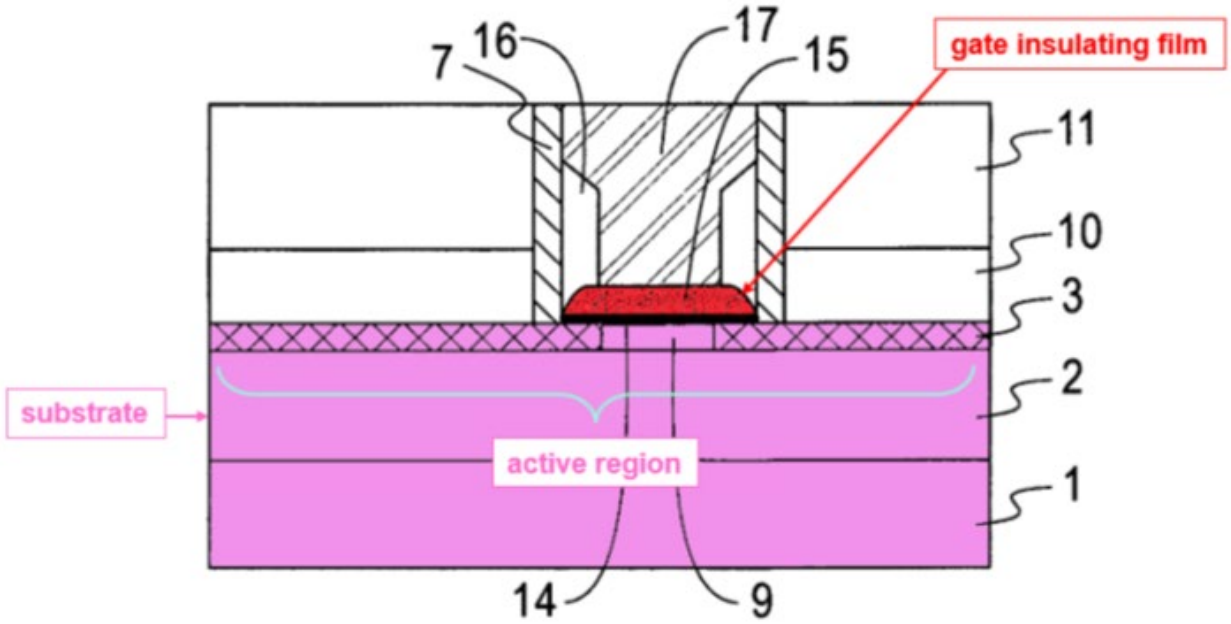
transistor active regions in "the channel layer **3** … provided over a buried oxide layer **2**" supported by "substrate **1**." EX1028 ¶ [0022]. Because Guha does not teach this claim limitation, Ground 8 fails. 37 C.F.R. § 42.104(b)(4) (requiring that the Petition identify where "***each element of the claim*** is found in the prior art patents or printed publications relied upon.") (emphasis added).

Ground 8 is predicated on "Guha's Figure 12." Petition at 59-69. That figure (reproduced below, Petition at 60) depicts a "silicon-on-insulator (SOI) structure, where the channel layer 3 is provided over a buried oxide layer 2," which is in turn located on "substrate 1." EX1028 ¶ [0022]. Guha teaches that the transistor's active region exists in channel layer 3. *Id*. ¶ [0026] ("[S]ource/drain extensions, also referred to as source/drain (S/D) junctions, are formed by implanting dopants . . . ***into the channel layer 3***. . . . A channel 9 . . . is thus defined between the S/D extensions.") (emphasis added). Importantly, "[c]hannel layer 3 is disposed ***over*** substrate 1," *id*. ¶ [0046] (emphasis added), not "in" substrate 1.



Guha, Figure 12

Rather than dispute this point, the Petition embraces it. Specifically, Petitioner's annotated version of Figure 12 (reproduced below) shows the "active region" as located in channel layer 3, which again is "disposed over substrate 1." But the Petition ignores this deficiency in Guha by labeling the entire multi-layer structure comprising elements 1-3 together as the "substrate." Petition at 61 ("A POSITA would have understood Guha's device has '*an active region in a substrate*.' (TSMC-1028, ¶22; TSMC-1003, ¶146.).").



Guha, Figure 12 (annotated by Petitioner)

But neither of the Petition's evidentiary citations supports its conclusion. First, Exhibit 1028 is the Guha reference. EX1028. The Guha reference consistently refers to the substrate as "substrate 1," and refers to the combination of layers 1-3[9] as the

[9] Guha also teaches that "[i]n other embodiments, layer 2 can be omitted." *Id*. ¶ [0022]. This is unhelpful to the Petition for multiple reasons. First, the Petition relies exclusively on Figure 12, not on some other alternative embodiment. *In re Magnum Oil*, 829 F.3d at 1381 ("[T]he Board ***must*** base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.") (emphasis added). Second, even if the Petition had relied on any embodiment in which layer 2 was omitted, the Petition fails to explain how the

"initial stacked structure." *Id*. ¶ [0021]. The term "channel layer 3" appears in twelve paragraphs of Guha and is never referred to as the substrate. *Id*. ¶¶ [0021]- [0023], [0025], [0026], [0029], [0033], [0035], [0036], [0039], [0046], [0047]. Although Guha says that "[t]he substrate may further contain active device regions, wiring regions, isolation regions or other like regions (not shown)," *id*. ¶ [0022], the relevant question is whether the particular transistor disclosed in Figure 12 has its active region in the substrate, not whether some other undefined and unidentified "devices" located elsewhere on the integrated circuit have their "active device regions" in the substrate.

Second, Petitioner's expert makes the conclusory assertion that "a POSITA would have understood that Guha's device has 'an active region in a substrate,' and that a portion of channel layer 3 forms part of that active region." EX1003 ¶ 191. But he does not square that statement with his assertions elsewhere that "substrate" is a synonym for "silicon wafer." *Id*. ¶ 38 ("MISFETs are fabricated on ***silicon wafers*** that serve as the ***substrate***.") (emphasis added); *id*. ¶ 36 (quoting the Weste reference text for the principle that the "silicon wafer [is] also called the substrate, body or bulk"). Nor does he reconcile his assertions with Guha's consistent reference to

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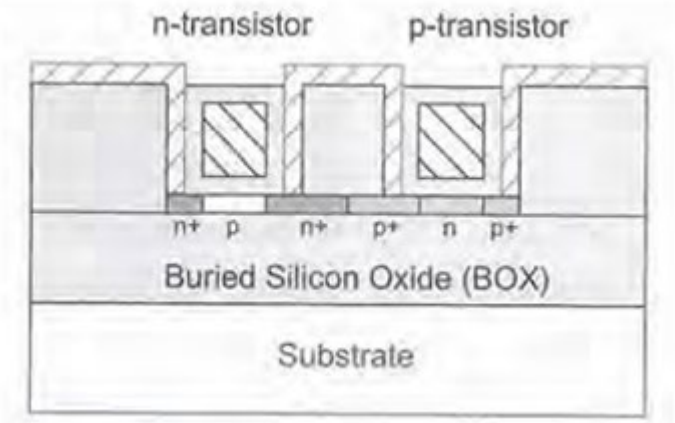
transistor's active region can be "in" the silicon wafer when it is "in" channel layer 3.

"substrate 1" as the substrate, rather than channel layer 3.

Moreover, Petitioner's Weste reference text cannot be squared with Petitioner's expert's assertions. Weste teaches that "a silicon substrate is used and a buried oxide (BOX) is grown ***on top of the silicon substrate***. A thin silicon layer is then grown ***on top of the buried oxide*** and this is selectively implanted to form nMOS and pMOS transistor regions." EX1041 at 137 (emphasis added). And, in the accompanying Figure 3.12 (below), Weste does not refer to the three-layer stack as the substrate but rather shows the "substrate" as a silicon wafer underlying the BOX and thin silicon layer. Because the Petition's evidence shows that "substrate" means "silicon wafer," and because the Petition admits that in Guha the transistor's active region is not "in" the silicon wafer but rather is in channel layer 3 that is above the silicon wafer, the Petition cannot meet its burden of showing that "***each element of the claim*** is found in the prior art patents or printed publications relied upon." 37 C.F.R. § 42.104(b)(4). Accordingly, Ground 4 does not present a "reasonable likelihood" of success as to any claim in the '180 Patent. 35 U.S.C. § 314(a).



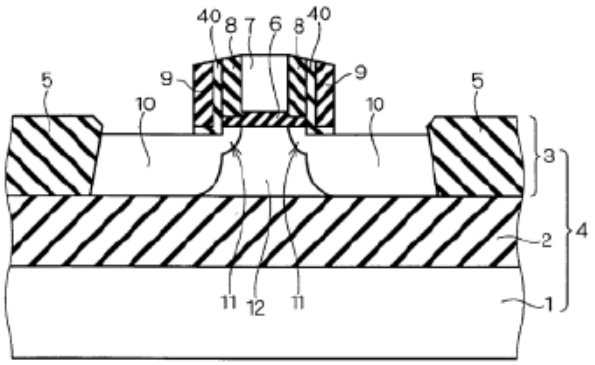
Weste, Figure 3.12

Each of Grounds 9-10 fails because each relies on the evidence in Ground 8 to establish that Guha teaches "an active region in a substrate." Petition at 79-80 (as to Ground 9, relying upon secondary reference Koyama solely for its teaching of a dependent claim limitation); Petition at 80-81 (as to Ground 10, relying upon secondary reference Sim solely for its teaching of a dependent claim limitation).

C. Grounds 11-13 Fail Because Matsumoto Does Not Teach an "Active Region In a Substrate"

Ground 11, and therefore also Grounds 12-13, fail because the Petition cannot show that Matsumoto teaches "an active region in a substrate," which is required directly or by dependency in each claim in the '180 patent. EX1001 at 21:9-22:52. Although the Petition offers no proposed construction for the claim term "substrate," Petition at 17, Petitioner's evidence and argument support the conclusion that "substrate" means "silicon wafer." *See* Section IV, *supra*. As explained *infra*,

applying this construction, Matsumoto does not teach forming transistor active regions "in" the substrate but rather teaches forming transistor active regions in a single-crystalline silicon layer that is stacked on a BOX (*i.e.*, buried oxide) layer, which is in turn stacked "on" the silicon wafer. Because Matsumoto does not teach this claim limitation, Ground 11 fails. 37 C.F.R. § 42.104(b)(4) (requiring that the Petition identify where "***each element of the claim*** is found in the prior art patents or printed publications relied upon.") (emphasis added).

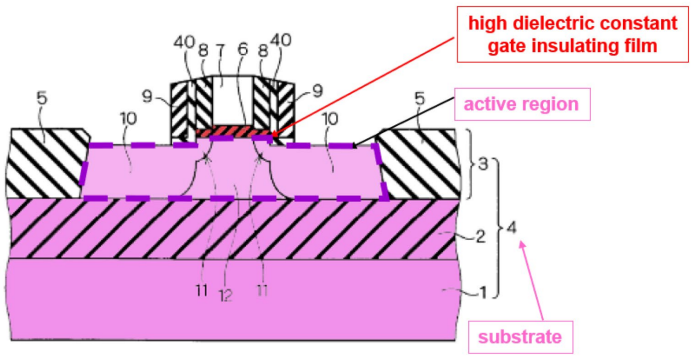


Matsumoto, Figure 22

Ground 11 is predicated on Matsumoto's fourth embodiment MOSFET, Petition at 82, which is depicted graphically in Figure 22. That figure (reproduced above) depicts a "multi-layer structure such that a silicon substrate **1**, a BOX layer **2** and a single-crystalline silicon layer **3** are stacked in the order named." EX1009 ¶ [0102]. Matsumoto teaches that the transistor's active region exists "in" single-crystalline silicon layer 3, not in silicon substrate 1. *Id.* ¶ [0105] ("A pair of

source/drain regions 10 are formed ***in the silicon layer 3***") (emphasis added); *id*. (teaching that the transistor's "body region 12" is located "between the pair of source/drain regions 10"). Figure 22, above, contains the same multi-layer structure, with the source, drain and body region located in single-crystalline silicon layer **3,** ***not*** in the silicon substrate **1**. *Id*. ¶ [0139] ("Referring to FIG. 22, the source/drain regions 10 are formed in the silicon layer 3 by an ion implantation process.").

Rather than dispute this point, the Petition embraces it. Specifically, Petitioner's annotated version of Figure 22 (reproduced below) shows the "active region" as located in single-crystalline silicon layer 3, which is "on" silicon substrate 1. Petition at 83. But the Petition ignores this deficiency in Matsumoto by labeling the entire "multi-layer structure" comprising elements 1-3 together as the "substrate." *Id.* at 82 ("The device has a multi-layer SOI substrate 4. . . .").



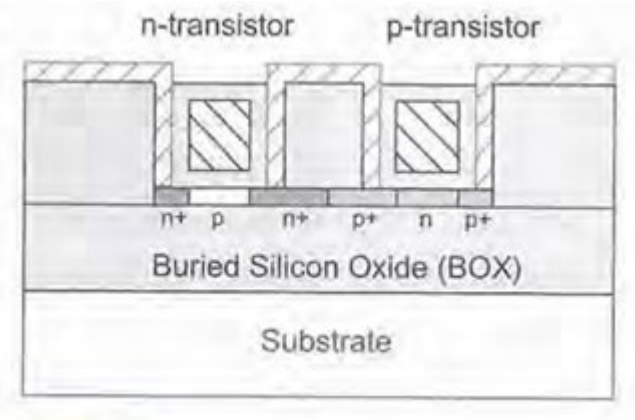
Matsumoto, Figure 22 (annotated), Petition at 83

Matsumoto also refers to the "multi-layer structure" as an "SOI substrate 4." Obviously, "SOI substrate" and "substrate" are different terms. Moreover,

Matsumoto has acted as its own lexicographer by coining the phrase "SOI substrate." Thus, Matsumoto's unique language is not relevant to the meaning of "substrate" in the '180 patent. Petitioner's own record shows that "substrate" does not mean a multi-layer SOI structure but rather means "silicon wafer." Weste repeatedly explains that the "silicon wafer" is "called the substrate." EX1041 at 8 ("[T]he ***silicon wafer*** [is] also called the ***substrate***, body, or bulk.") (emphasis added); *id*. at 23 ("Transistors are fabricated on thin ***silicon wafers . . . called the substrate***."). EX1041 at 23 (emphasis added). Moreover, Petitioner's expert also equates "silicon wafer" and "substrate." EX1003 ¶ 38 ("MISFETs are fabricated on ***silicon wafers*** that serve as the ***substrate***.") (emphasis added); EX1003 (Lee Decl.) ¶ 36 (quoting the Weste reference text for the principle that the "silicon wafer [is] also called the substrate, body or bulk"). And Petitioner itself uses "silicon wafer" and "substrate" synonymously. *Taiwan Semiconductor Manufacturing Co., Ltd v. Advanced Integrated Circuit Process LLC*, IPR2025-00832, Paper 2 at 3 ("A metal-insulating-semiconductor transistor (MISFET or MOSFET) generally includes . . . '***the silicon wafer, also called the substrate***, body or bulk.'") (emphasis added) (quoting Weste).

Indeed, Weste shows that a POSITA would not adopt Matsumoto's unique "SOI substrate" nomenclature, which is different from "substrate." Weste teaches that "a silicon substrate is used and a buried oxide (BOX) is grown ***on top of the silicon substrate***. A thin silicon layer is then grown ***on top of the buried oxide*** and this is

selectively implanted to form nMOS and pMOS transistor regions." EX1041 at 137 (emphasis added). And, in the accompanying Figure 3.12 (below), Weste does not refer to the multi-layer SOI structure as the substrate but rather describes the "substrate" as a silicon wafer underlying the BOX and thin silicon layer. Because the Petition's own evidence supports "substrate" meaning "silicon wafer," and because the Petition admits that Matsumoto's transistor active region is not "in" the silicon wafer but rather is in the single-crystalline silicon layer 3 that is above the silicon wafer, the Petition cannot meet its burden of showing that "***each element of the claim*** is found in the prior art patents or printed publications relied upon." 37 C.F.R. § 42.104(b)(4). Accordingly, Ground 1 does not present a "reasonable likelihood" of success as to any claim in the '180 Patent. 35 U.S.C. § 314(a).



Weste, Figure 3.12

Each of Grounds 12-13 fails because each relies on the evidence in Ground 8 to establish that Matsumoto teaches "an active region in a substrate." Petition at 95-

98 (as to Ground 12, relying upon secondary reference Rodder solely for its teaching of dependent claim limitations); Petition at 98-104 (as to Ground 13, relying upon secondary reference Ono solely for its teaching of a dependent claim limitation).

VI. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute IPR.

Dated: August 13, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,253,180 was served to the following counsel of record for Petitioner as follows:

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that this brief complies with the type-volume limitation of 37 C.F.R. § 42.24 because this brief contains 8,660 words.

Dated: August 13, 2025

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