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(54) DAMASCENE GATE FIELD EFFECT TRANSISTOR WITH AN INTERNAL SPACER STRUCTURE

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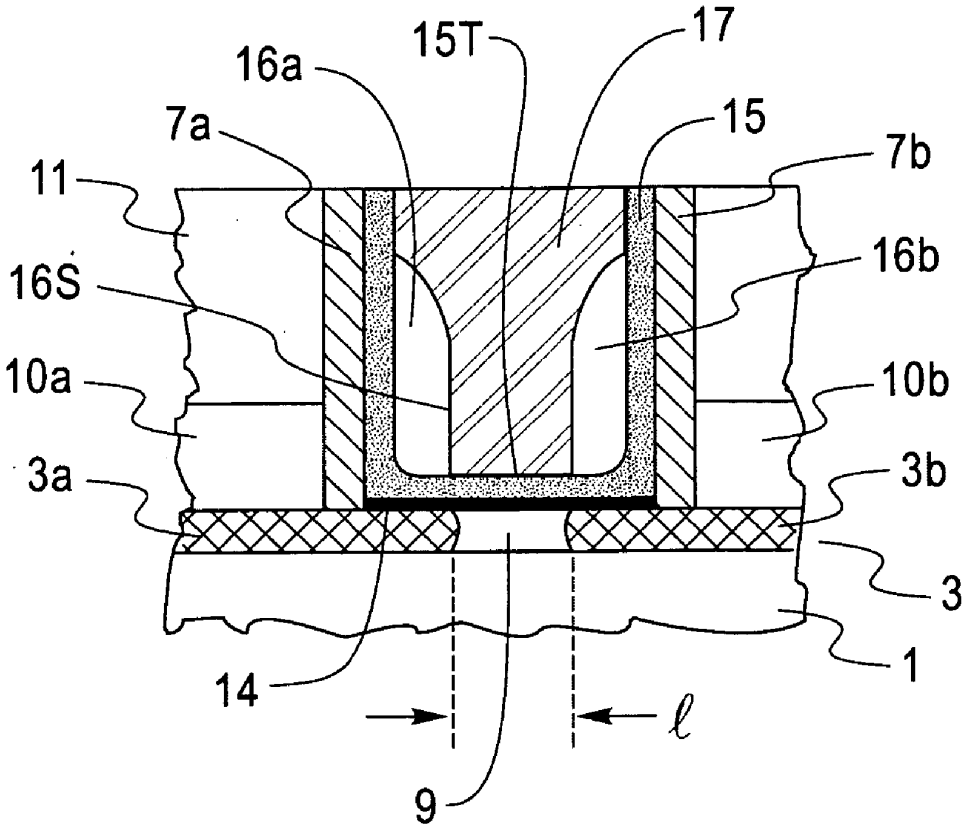
(57) **ABSTRACT**

A MOSFET is disclosed that comprises a channel between a source extension and a drain extension, a dielectric layer over the channel, a gate spacer structure formed on a peripheral portion of the dielectric layer, and a gate formed on a non-peripheral portion of the dielectric layer, with at least a lower portion of the gate surrounded by and in contact with an internal surface of the gate spacer structure, and the gate is substantially aligned at its bottom with the channel. One method of forming the MOSFET comprises forming the dielectric layer, the gate spacer structure and the gate contact inside a cavity that has been formed by removing a sacrificial gate and spacer structure.



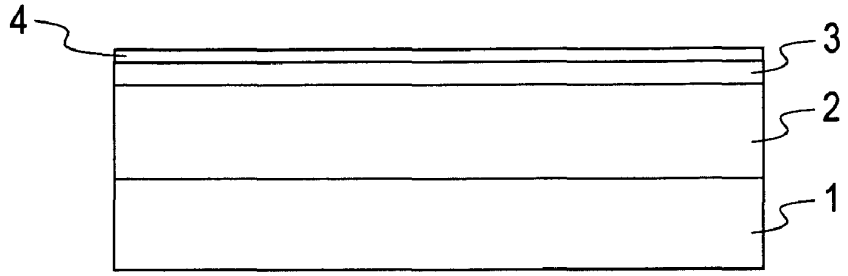


Fig. 1

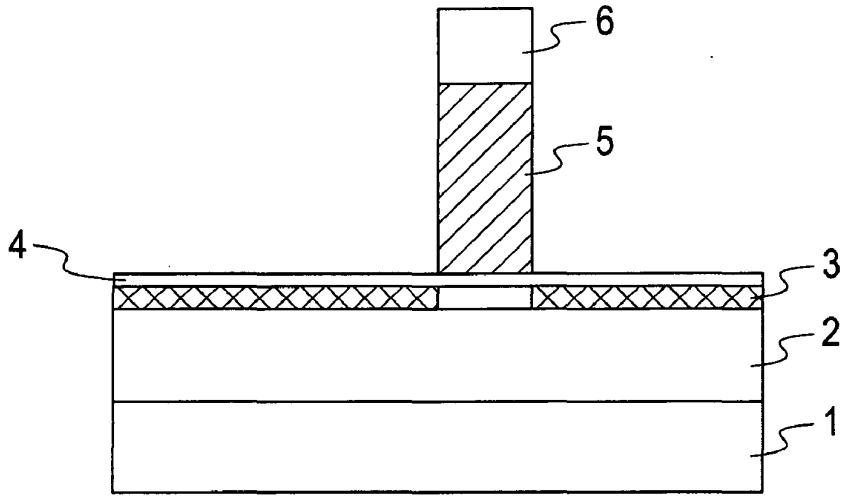


Fig. 2

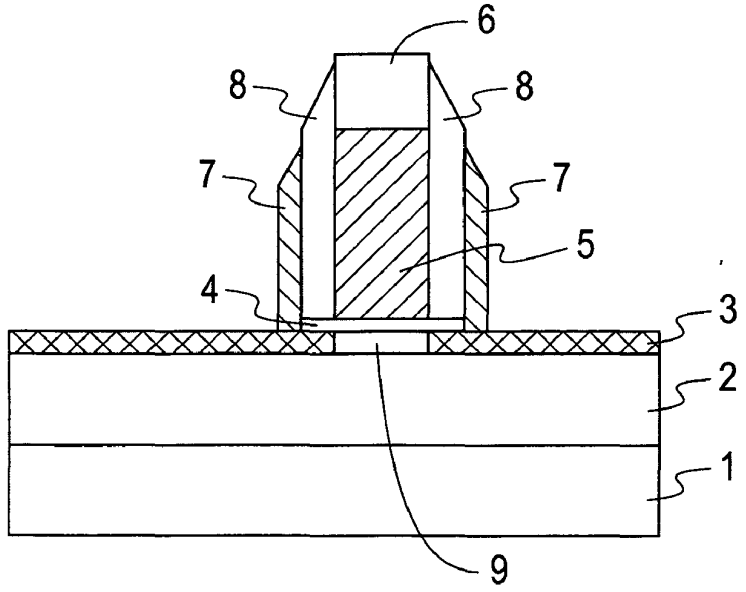


Fig. 3

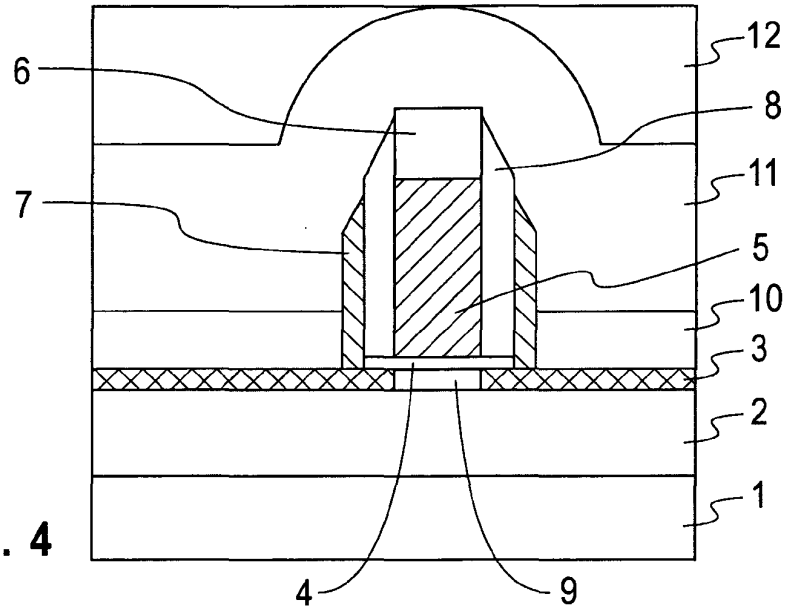


Fig. 4

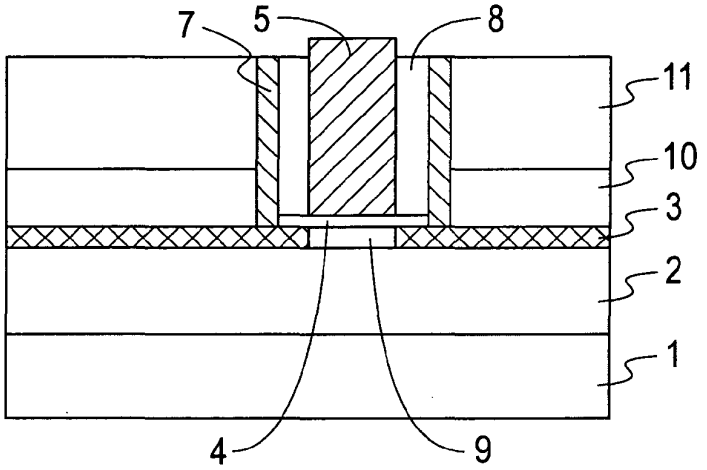


Fig. 5

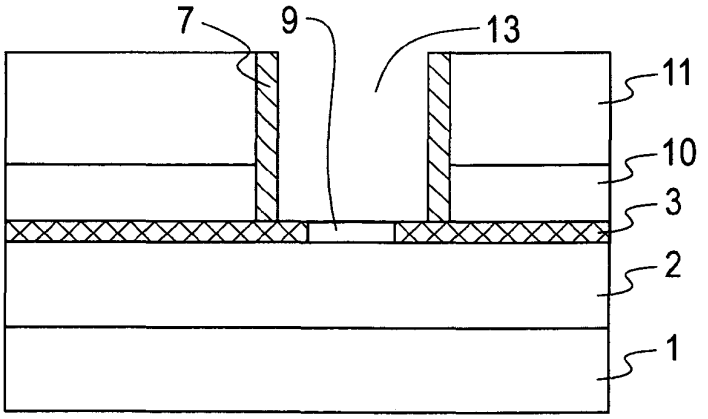


Fig. 6

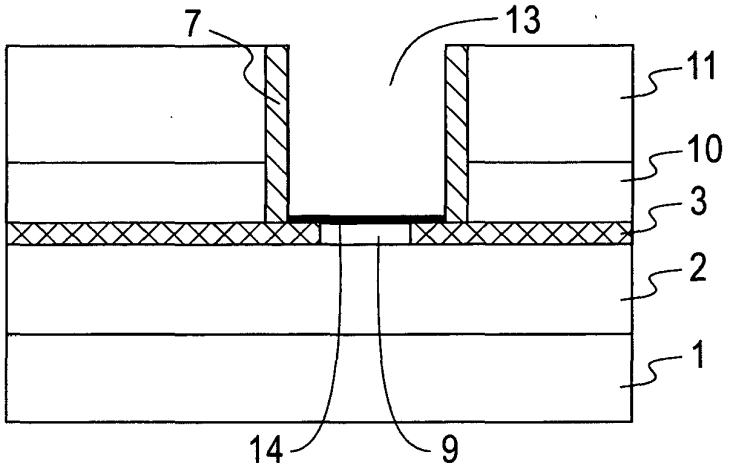


Fig. 7

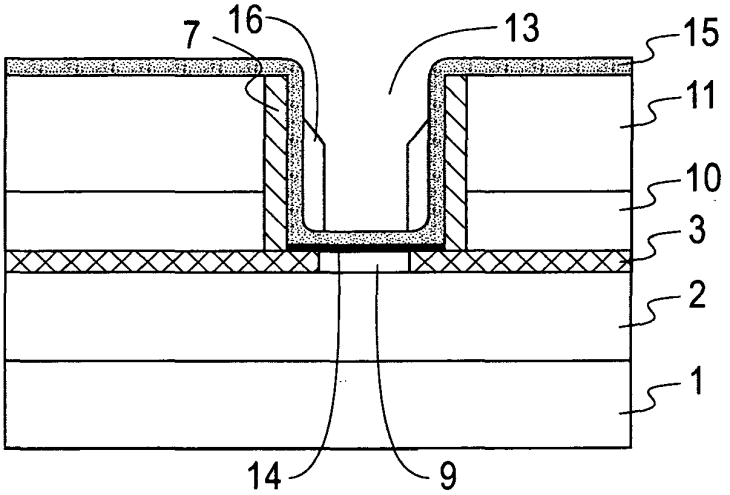


Fig. 8

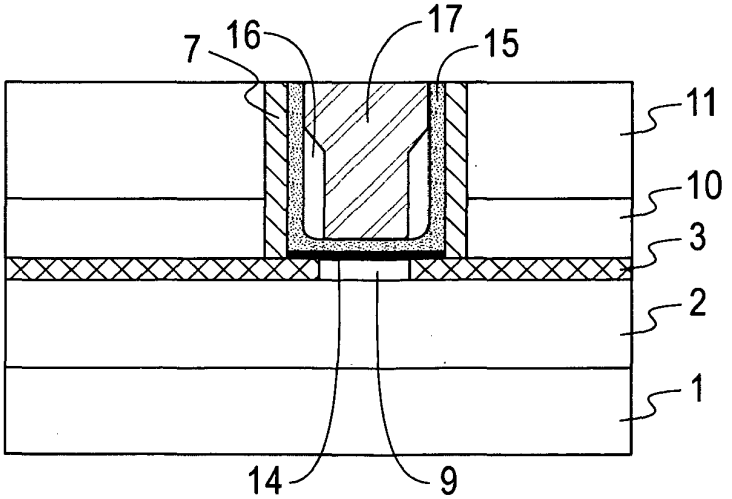


Fig. 9

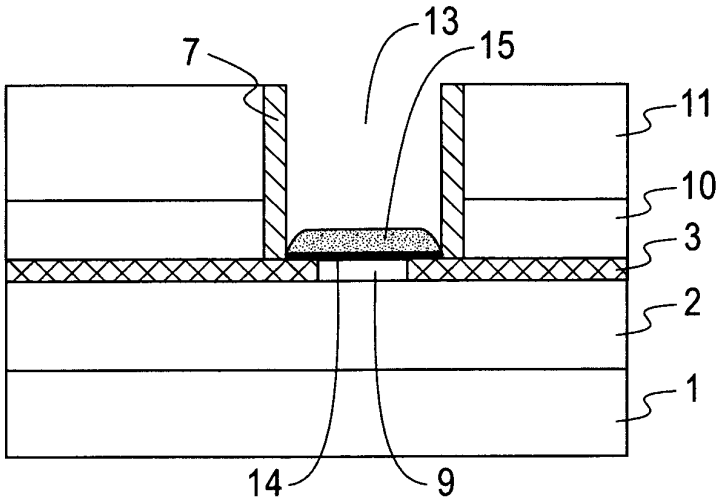


Fig. 10

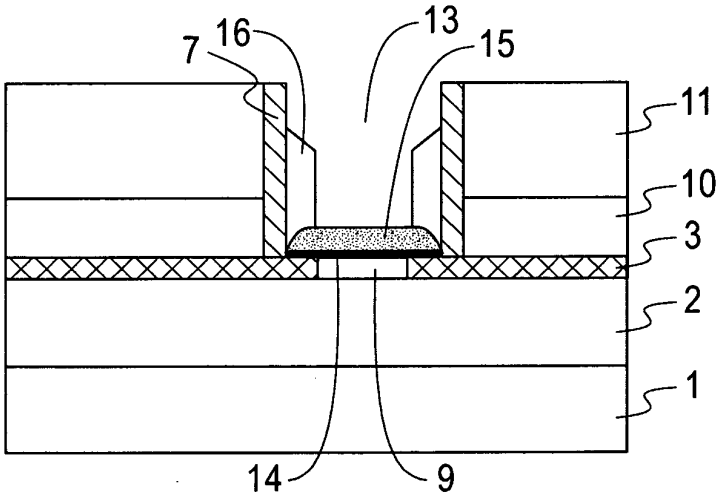


Fig. 11

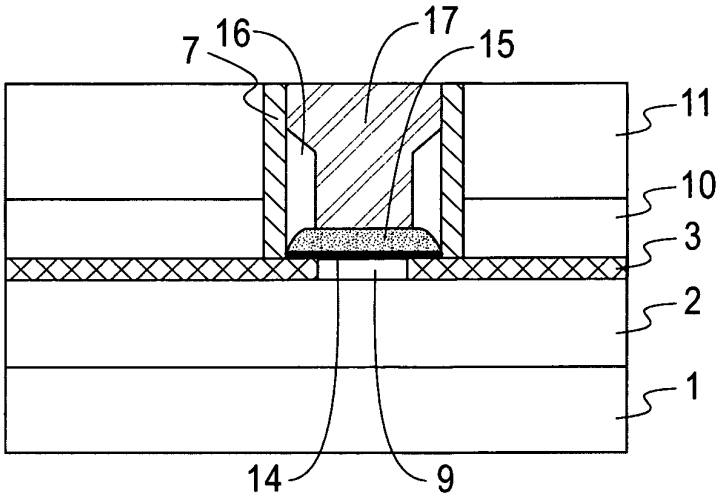
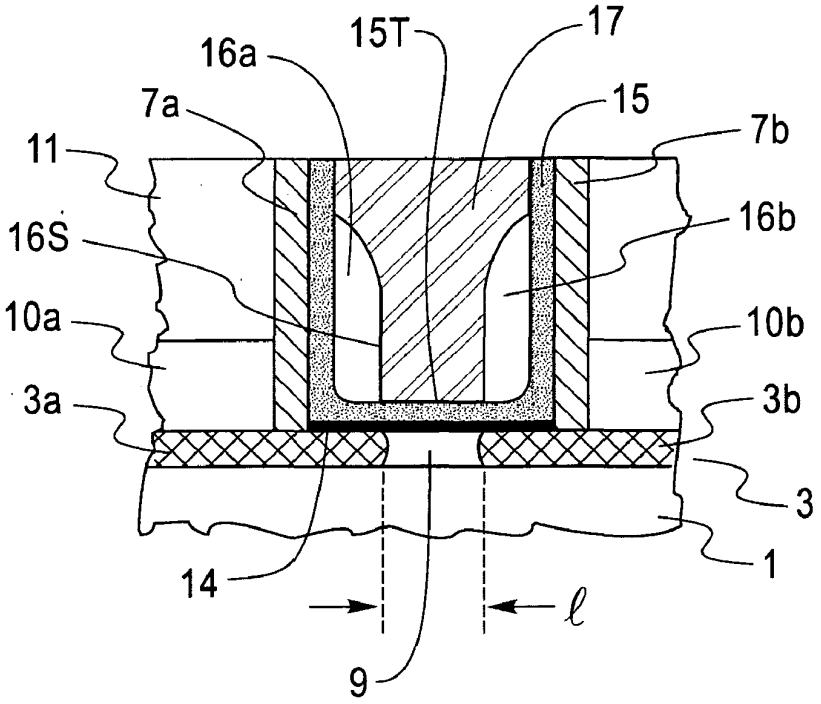


Fig. 12


15T
17
16a
7a
15
7b
11
16S
16b
10a
10b
3a
3b
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14
ℓ
9

Fig. 13

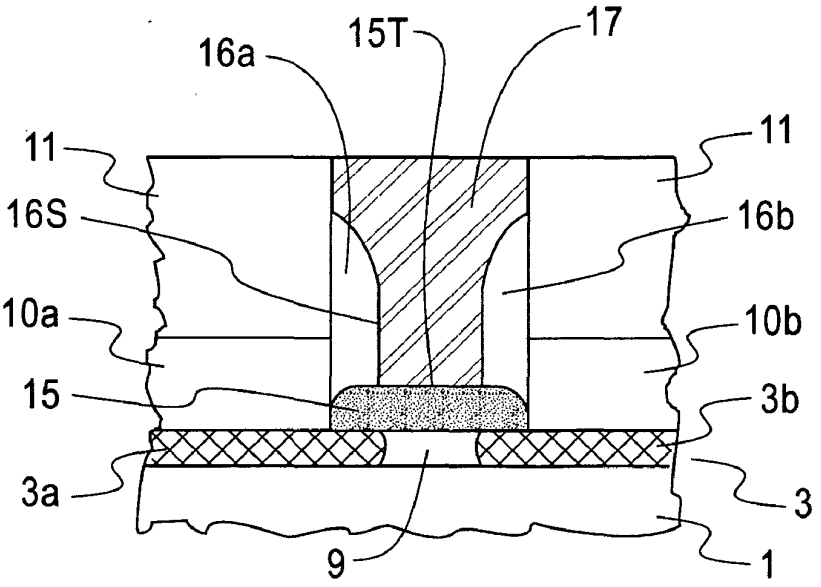
15T
17
16a
11
11
16S
16b
10a
10b
15
3b
3a
3
9
1

Fig. 14

DAMASCENE GATE FIELD EFFECT TRANSISTOR WITH AN INTERNAL SPACER STRUCTURE

FIELD OF THE INVENTION

[0001] The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device.

BACKGROUND OF THE INVENTION

[0002] In order to extend CMOS scaling, dielectrics of higher dielectric constant (Hi-K) are being investigated. For a given gate capacitance, hence charge in the channel, the Hi-K dielectric can be thicker, thus reducing tunneling leakage. To increase the gate capacitance even further, and to have a suitable work-function for thin-silicon implementation, a metal gate is desirable. These material options are frequently incompatible with conventional high-temperature front end of the line processing, so that replacement gate methods are being tried where the Hi-K dielectric and the metal are deposited in a groove formed by removing a dummy gate.

[0003] As the gate length of a field effect transistor (FET) gets shorter, the Hi-K dielectric occupies an increasing fraction of the groove. The gate itself tends to be rounded at the bottom, and as a result, only the center of the gate has full control of the channel. Furthermore, the presence of a gap between the Source/Drain (S/D) extension implant regions and the gate edge increases the on-resistance of the FET. Therefore, there is a need for alternate methods of forming a device with better overlap or alignment between the gate and S/D extensions as well as gate contact profile for improved device performance.

SUMMARY OF THE INVENTION

[0004] The invention relates to a MOSFET with improved device performance and method of fabricating the device. The MOSFET comprises a source extension, a source contact disposed on the source extension, a drain extension, a drain contact disposed on the drain extension, a channel between the source extension and the drain extension, a dielectric layer above the channel, a gate spacer structure disposed on a peripheral portion of a top surface of the dielectric layer and having an internal surface that meets the top surface of the dielectric layer at about a right angle. A gate, which is disposed over a non-peripheral portion of the top surface of the dielectric layer, has at least a lower portion surrounded by and in contact with the internal surface of the gate spacer structure. The gate is also substantially aligned at its bottom with the channel.

[0005] One method of forming the MOSFET comprises: providing a channel layer on a substrate; forming a source extension and a drain extension in the channel layer thereby defining a channel between the source and drain extensions; forming a dielectric layer over the channel; forming a gate spacer structure over a peripheral portion of a top surface of the dielectric layer, with the gate spacer structure having an internal surface with a lower portion that is substantially perpendicular to the top surface of the dielectric layer whereby a cavity is defined at its sidewall by the internal surface of the gate spacer structure and at its bottom by the dielectric layer; forming a gate contact by disposing an electrically conductive material into the cavity to contact the top surface of the dielectric layer.

DESCRIPTION OF THE DRAWINGS

[0006] Embodiments of the invention are depicted in the drawings and described in detail below by way of examples. **FIGS. 1-14** depict structures obtained during various stages of the fabrication process.

[0007] **FIG. 1** depicts a cross-sectional view of a substrate with a bottom insulator, a channel layer and a protection layer;

[0008] **FIG. 2** illustrates the formation of a dummy gate over the structure of **FIG. 1**;

[0009] **FIG. 3** illustrates the formation of a channel, dummy gate spacers and isolating spacer structure from the structure of **FIG. 2**;

[0010] **FIG. 4** illustrates a first overlayer and a second overlayer formed over the structure of **FIG. 3**;

[0011] **FIG. 5** illustrates the structure of **FIG. 4** after planarization to the dummy gate;

[0012] **FIG. 6** illustrates the structure after removing the dummy gate and dummy gate spacer;

[0013] **FIG. 7** illustrates the structure of **FIG. 6** with isolating spacers;

[0014] **FIG. 8** illustrates the formation of a dielectric layer and gate spacers;

[0015] **FIG. 9** illustrates the formation of a gate contact;

[0016] **FIGS. 10-12** illustrate an alternative process sequence of forming a dielectric layer at the bottom of a gate contact;

[0017] **FIG. 13** illustrates an enlarged cross sectional view of the device of **FIG. 9**;

[0018] **FIG. 14** illustrates a cross-sectional view of an alternative device structure.

[0019] The figures are meant for illustrative purpose and thus, not shown in real dimensions or drawn to scale.

DETAILED DESCRIPTION OF THE INVENTION

[0020] The present invention will now be described in more detail by referring to the drawings that accompany the present application. In the accompanying drawings, like reference numerals are used for describing like and corresponding elements.

[0021] **FIG. 1** shows an initial stacked structure that comprises a substrate **1** having a bottom insulator **2**, also referred to as buried oxide layer, located thereon. The initial stacked structure also includes a channel layer **3** on top of the bottom insulator **2**, and an oxide layer **4**, also referred to as pad protection layer, located atop the channel layer **3**.

[0022] The structure shown in **FIG. 1** can be manufactured from conventional materials with conventional processing steps that are well known in the art. For example, the substrate **1** may comprise any semiconducting material including, but not limited to: Si, Ge, SiGe, GaAs, InAs, InP and all other III/V semiconductor compounds, and may also

be a layered substrate comprising different semiconductor materials, e.g., Si/SiGe. The illustrative embodiment of **FIG. 1** shows a silicon-on-insulator (SOI) structure, where the channel layer **3** is provided over a buried oxide layer **2**. For embodiments with a buried oxide layer **2**, substrate **1** may also be any materials (e.g., not restricted to semiconducting) as long as it provides adequate support for layer **2**. In other embodiments, layer **2** can be omitted. The substrate may be of the n or p-type depending on the desired device to be fabricated. The substrate may further contain active device regions, wiring regions, isolation regions or other like regions (not shown). The substrate **1** may also be composed of a dielectric material such as SiO_2 and may be used as an isolation region of a memory device. In general, either layer **1** or **2** may be omitted; or the two layers may comprise any suitable materials or combinations as required by the specific device applications.

[**0023**] The channel layer **3** can comprise any semiconducting material such as Si, SiGe, SiGeC, InAs, GaAs, InP and other III/V compound semiconductors. Combinations of these semiconducting materials, strained or unstrained, are also contemplated herein. The channel layer **3** can be formed by a conventional deposition process including, for example, chemical vapor deposition (CVD), plasma-assisted CVD, evaporation or chemical solution deposition. Furthermore, the channel layer, **3**, may be formed from SOI using commercial SIMOX or SMARTCUT [Bruel et al., *Jpn. J. Appl. Phys., "Smart Cut: a new silicon on insulator material technology based on hydrogen implantation and wafer bonding,"*36 (1997) 1636-1641] processes. Typically, the channel layer **3** has a thickness of about 10 nm. It can be formed with an initial thickness between about 20 to about 100 nm, and reduced to the desired thickness thereafter.

[**0024**] The pad protection layer **4** can comprise an oxide, e.g. SiO_2, and is formed using a conventional thermal process, or may be formed by a conventional deposition process such as chemical vapor deposition (CVD), plasma-assisted CVD, sputtering, evaporation and other deposition processes. The thickness of the pad protection layer **4** may vary and is not critical to the present invention. Notwithstanding which technique is employed, the pad protection layer **4** typically has a thickness between about 2 to about 30 nm, preferably between about 5 to about 10 nm.

[**0025**] **FIG. 2** shows the result of a patterning step in which a dummy gate hard mask **6** is used to pattern a dummy gate **5**, or sacrificial gate, over the stacked structure of **FIG. 1**. This can be achieved by depositing a dummy-gate layer, e.g. comprising polysilicon, or amorphous silicon, over the structure of **FIG. 1**, followed by a dummy gate hard mask layer. After the dummy gate hard mask **6** is patterned using conventional lithography and reactive ion etching (RIE), the gate pattern is transferred to the underlying dummy gate layer by RIE. The pad protection layer **4** serves as an etch stop layer and protects the channel layer **3** during RIE patterning of the dummy gate **5**.

[**0026**] In the following step, source/drain extensions, also referred to as source/drain (S/D) junctions, are formed by implanting dopants through the pad protection layer **4** into the channel layer **3**, with the dummy gate **5** acting as an implantation mask. Following ion implantation, the S/D extensions are annealed to activate dopants. A channel **9** (see **FIG. 3**), having a predetermined channel length substantially equal to the length of the dummy gate **5**, is thus defined between the S/D extensions.

[**0027**] Dummy-gate spacers **8** are then formed adjacent to the dummy gate **5**, extending from the pad protection layer **4** up to the dummy gate hard mask **6**. The dummy-gate spacers **8** can comprise an oxide or other materials that can readily be removed in a subsequent process step. In this embodiment, the dummy gate spacers **8** are of unitary construction, e.g., are present in form of a ring that surrounds the dummy gate **5**. The dummy gate spacers **8** can be formed, for example, by first depositing a layer of suitable material over the structure shown in **FIG. 2** (after S/D formation), followed by reactive ion etching.

[**0028**] An isolating spacer structure **7** is formed flanking the dummy-gate spacers **8**. The resulting structure is depicted in **FIG. 3**. In this embodiment, the isolating spacer structure **7** is of unitary construction, e.g., present in form of a ring that surrounds the dummy gate spacer **8**. As used herein, the isolating spacer structure **7** is used to denote the isolating spacer(s), whether it is of unitary construction or not. In practice, the unitary construction is preferred because of its relative ease of fabrication. Isolating spacer structure **7** can be composed of any insulating material including, for example, an oxide, nitride, oxynitride or any combination thereof; as long as the material can be selectively etched with respect to the material of the dummy gate spacers **8**. Isolating spacer structure **7** can be formed by deposition of an insulating material and subsequent etching. A preferred material would be silicon nitride.

[**0029**] The pad protection layer **4** is then removed, e.g., by wet chemical etching with HF, at the area around the dummy gate **5** and the dummy-gate spacers **8** to expose the channel layer **3**.

[**0030**] In the following step, source/drain contacts **10** (see **FIG. 4**) are created above the source/drain extensions. This can be achieved by epitaxial growth to form the raised source/drain contacts **10** followed by implantation of a dopant such as arsenic (As) or boron (B). Thereafter the source/drain contacts **10** can be silicided. The source/drain contacts **10** are eventually composite layers with a lower silicon layer and an upper metal silicide layer.

[**0031**] Next, a first overlayer **11** e.g., an insulating layer, exemplarily comprising silicon nitride is deposited over the whole structure, followed by deposition of a second overlayer **12**, e.g. comprising oxide. The second overlayer **12** is planarized down to the first overlayer **11**, e.g. by chemical mechanical planarization (CMP). No precise time control is necessary because the first overlayer **11** acts as a planarization stop layer. The result of that step is shown in **FIG. 4**. Note that in an alternative embodiment, the first overlayer **11** may comprise an oxide and the second overlayer **12** may comprise silicon nitride. In this latter embodiment, however, CMP of the second overlayer **12** may require time control because nitride cannot be polished selectively with respect to the underlying oxide.

[**0032**] Next, the remainders of the second overlayer **12**, the nitride overlayer **11**, and the dummy gate mask **6** are etched down to the dummy gate **5**, e.g. by means of RIE. When none of the materials used provides a natural etch stop function, this step is preferably time-controlled to stop at a

desired dummy gate height. Since the RIE etch rate in polysilicon can be lower than in nitride and oxide, the dummy gate **5**, if made of polysilicon, may be a little higher than the remaining part of the first overlayer **11** and of the dummy gate spacer **8**. **FIG. 5** shows the result of this step.

[**0033**] Thereafter the dummy gate **5** is removed by etching, e.g. with potassium hydroxide (KOH). The pad protection layer **4** protects the channel layer **3** and the channel **9** from the etchant.

[**0034**] Next, the dummy gate spacer **8** is removed, e.g. using dilute HF, which also removes the pad protection layer **4**), leaving behind the structure depicted in **FIG. 6**. The first overlayer **11** and the isolating spacer structure **7** can comprise silicon nitride which is resistant to HF. Generally the isolating spacer structure **7** serves to protect the source/drain contacts **10** from the etchant used to remove the dummy gate spacer **8**. However, if the material of the S/D contacts **10** is resistant to the etchant used for removing the dummy gate spacer **8**, spacers **7** will not be necessary.

[**0035**] As shown in **FIG. 6**, the channel layer **3** and the isolating spacers **7** together define a cavity **13**. In the absence of the optional isolating spacer structure **7**, the cavity **13** will be defined at its bottom by channel layer **3** and at its sidewalls by side surfaces of S/D contacts **10** and the overlayer **11**. It can be seen that the length of channel **9** is shorter than the distance between nitride spacers **7**. In this process, the dummy gate **5** is used as a sacrificial feature to help define the channel length, while the dummy gate spacers **8** allows the cavity **13** to be defined with a bottom lateral dimension greater than the channel length. The cavity **13** is typically, but not necessarily, a high-aspect ratio aperture. The term "high-aspect ratio gate aperture" is used herein to denote a cavity **13** whose height to width ratio (H/W) is about 2 or greater.

[**0036**] At this stage, an optional sacrificial oxide layer can be grown on the channel layer **3** and channel **9** within the cavity **13** in order to produce a cleaner surface for the next step. The sacrificial oxide layer furthermore serves to make the channel **9** thinner since growth not only adds material on top of the channel **9** and channel layer **3** but also extends into the channel **9** and channel layer **3**. The sacrificial oxide layer is then removed, e.g., by selective etching, leaving behind a cleaner and thinned-down channel **9** and channel layer **3** at the bottom of the cavity **13**. This results in a "recessed" portion of the channel layer **3** that is thinner than the remaining channel layer lying outside the cavity **13**.

[**0037**] An optional gate-isolating layer **14** can then be formed at the bottom of the cavity **13**, as shown in **FIG. 7**. The gate-isolating layer **14** acts as a buffering layer between channel **9** and the dielectric material to be deposited thereon. A preferred material for the gate-isolating layer **14** is silicon oxide, which can be thermally grown, and thinned if necessary. Other materials, however, may also be suitable. This gate-isolating layer, for example, is used to prevent mobility degradation in the silicon channel that may be caused by scattering mechanisms in the dielectric layer.

[**0038**] Thereafter a dielectric layer **15**, preferably comprising a high-K dielectric material, is deposited. As shown in **FIG. 8**, the dielectric layer **15** covers the nitride overlayer **11**, the walls of the isolating spacers **7** and the gate-isolating layer **14**. A high-K material is a material that exhibits a dielectric constant of approximately above 10 or more. Examples of such materials, include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide.

[**0039**] If a gate were to be formed at this stage of the process, as typically done in conventional methods, there would be two disadvantages: First, the parasitic capacitance between the gate and the source/drain extensions in the channel layer **3** would be too high. Second, the dielectric layer, due to the nature of its deposition process exhibits rounded edges at the area where the dielectric layer transits from the plane above the gate-isolating layer **14** to the plane adjacent the isolating spacer structure **7**. These rounded edges would lead to an increased thickness of the dielectric layer **15**, between the source/drain extensions and the gate edge, resulting in diminished gate control over the channel **9**, whereby the on-resistance of the FET would increase and the sub-threshold swing would degrade. The device performance would be degraded since only the center of the gate would have full control of the channel.

[**0040**] Thus, according to the present invention, "internal" gate spacers **16**, or more generally, a gate spacer structure, is formed inside the cavity **13**, as shown in **FIG. 8**. This can be achieved, for example, by depositing a spacer material, e.g. an oxide or other suitable material, in the cavity **13** and etching the deposited material anisotropically, e.g. by RIE, such that the portion of the dielectric layer **15** above channel **9** is exposed, leaving the gate spacer structure **16** on the sidewalls of the cavity **13**. This arrangement of the gate spacer structure **16** provides a narrowing of the cavity **13** above the channel **9**. The gate spacer structure **16** has an internal surface **16**S (i.e., surface facing the interior of the cavity **13**, away from the cavity sidewalls) with a lower portion that is substantially perpendicular to the dielectric layer **15**. In other words, the internal surface **16**S contacts or meets the dielectric layer **15** at the bottom of the cavity **13** at about a right angle, although some deviation from perpendicular, e.g., smaller or larger angles, are also possible. A large re-entrant profile, however, will not be preferred. The etching process for the gate spacer structure **16** is selective with respect to dielectric layer **15**. It can be seen that the gate spacer structure **16** shown here is of unitary construction, e.g., present in form of a ring that is embedded within the cavity **13**. In principle, the gate spacer structure **16** may also be formed as two separate spacers, although it may involve a more complicated fabrication process.

[**0041**] Thereafter the cavity **13** is filled with a conductive material to form a gate **17**. This can be done by depositing the material into the cavity **13** and onto the dielectric layer **15**. For example, the conductive material may be formed from vapor phase deposition, such as tungsten or titanium nitride, or by depositing amorphous silicon and reacting it with a metal such as nickel to form a silicide, and subsequently thinning it down to the dielectric layer **15**, and possibly removing the conductive material and the dielectric layer **15** lying outside of cavity **13**, e.g., by CMP. Polysilicon may also be used, for example, either in-situ doped or doped by a conventional ion-implantation and annealing technique, as long as the annealing temperatures and conditions are compatible with the dielectric layer **15** and the second overlayer **11**. The resulting device is depicted in **FIG. 9**. Not only is channel **9** shorter than the distance between the isolating spacers **7** and is substantially aligned laterally with

the bottom of the gate **17**, but the profile of the lower portion of gate **17** at its interface to the dielectric layer **15** is also improved. Specifically, there are no rounded corners in the region where the gate spacers **16**, the dielectric layer **15** and the bottom of the gate **17** meet. Instead, the lower portion of gate **17** and the dielectric layer **15** meet at a relatively sharp "edge" as defined by the internal spacer structure **16**, and are substantially perpendicular to each other. This provides a better control from the gate **17** to the channel **9**.

[**0042**] In general, many different conductive materials can be used for gate **17**, including, for example, elemental metals such as tungsten, rhenium, tantalum, hafnium, molybdenum, aluminum, lanthanum; metal nitrides such as titanium nitride, tantalum nitride, tungsten nitride, tantalum silicon-nitride; various silicided gates (with and without dopants for threshold voltage control); and conducting metal oxides, provided that they are compatible with the desired process.

[**0043**] **FIGS. 10-12** show an alternative process sequence that can be used to form the gate with internal gate spacers. In this embodiment, the structure of **FIG. 7** is subjected to a deposition step in which the dielectric layer **15** is formed only on the gate-isolating layer **14** at the bottom of the cavity **13**. This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafiium, zirconium, aluminium, among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing a further reduction in sidewall capacitance. As shown in **FIG. 10**, the dielectric layer **15** covers only the bottom of the cavity **13**. However, the problem still exists that the edge where the dielectric layer **15** meets the isolating spacer structure **7** may not be well defined, and is rounded either upwards or downwards (e.g., similar to a cusp), which would lead to, in the first case, reduced control between the gate to be formed and the channel **9**, and in the second case a danger of a short between the gate to be formed and the channel **9**.

[**0044**] Thus, as shown in **FIG. 11**, internal gate spacer structure **16** is formed within cavity **13**, as previously described in connection with **FIG. 8**. Here the gate spacer structure **16** contacts both the dielectric layer **15** and the isolating spacer structure **7**. In other embodiments where the isolating spacer structure **7** is absent, the gate spacer structure **16** will contact the overlayer **11** instead.

[**0045**] Thereafter the cavity **13** is filled with a conductive material to form the gate **17**, as previously described. The resulting device is depicted in **FIG. 12**. Again, by means of the gate spacer structure **16**, the interface between the bottom of the gate **17** and the dielectric layer **15** is better defined and offers a better control over the channel **9**. As previously discussed, the isolating spacer structure **7** and gate isolating layer **14** are optional, and either one or both may be omitted in alternative embodiments.

[**0046**] **FIG. 13** shows an enlarged view of the device of **FIG. 9**, with different reference labels designating the source-side and drain-side elements. Channel layer **3** is disposed over substrate **1**, and comprises channel **9**, source extension **3***a* and drain extension **3***b*. Channel **9** is characterized by a channel length (1) in the lateral direction. Source contact **10***a* and drain contact **10***b* are provided to contact the source extension **3***a* and drain extension **3***b*, respectively.

[**0047**] The gate-isolating layer **14** is disposed over channel layer **3**, and dielectric layer **15** is disposed over the gate-isolating layer **14**. In other embodiments, the gate-isolating layer **14** may be omitted. In the embodiment of **FIG. 13**, dielectric layer **15** has a U-shaped cross-section, with substantially vertical sidewall portions and a horizontal portion having a top surface **15**T. The internal gate spacer structure, shown as **16***a* and **16***b*, is disposed over a peripheral area of the top surface **15**T of the dielectric layer **15**. Note that the rounded edges or profiles between the horizontal portion and vertical sidewalls of the dielectric layer **15** are covered by the internal spacer structure **16***a* and **16***b*, which has an internal surface **16**S (away from the dielectric layer **15**) whose lower portion is substantially vertical or perpendicular to the top surface **15**T of the dielectric layer **15**. In this case, the internal spacer structure **16***a* and **16***b* also contacts the vertical sidewall portions of the U-shaped dielectric layer **15**. In this embodiment, the internal surface **16**S is a curved surface, e.g., with a curved region towards the top. Other variations are also possible, depending on the specific process steps used. For example, the internal spacer **16***a* and **16***b* may also have a rectangular cross-section, e.g., by polishing or removing the upper curved region to form a horizontal portion of the internal surface.

[**0048**] The volume between spacer structure **16**a, **16**b and between the opposite sidewalls of the dielectric layer **15** is filled with a suitable gate material, resulting in gate **17** having a lower portion surrounded by the gate spacer structure **16***a*, **16***b* and an upper portion surrounded by the dielectric layer **15**. The gate **17** has a lateral dimension at its bottom that is at least equal to the channel length, and substantially aligned with channel **9** (i.e., substantially laterally aligned with the edges of the S/D extensions). In this device, the spacer structure **16***a*, **16***b* effectively confines the bottom or lower portion of gate **17** to contact a "non-peripheral" portion of the dielectric layer **15**, such that a better defined, e.g., sharper, edge between the bottom of gate **17** and the top surface **15**T of dielectric layer **15** is achieved (instead of rounded corners as obtained in conventional devices). The bottom profile of this gate contact allows improved channel control of the device.

[**0049**] As shown in **FIG. 13**, the source and drain contacts **10***a* and **10***b* are isolated from the dielectric layer **15** by means of an isolating spacer structure (shown as **7***a* on the source side and **7***b* on the drain side). As previously discussed, the use of the isolating spacer structure **7** is optional and, depending on the materials used for the source and drain contacts **10***a* and **10***b* and specific process conditions, may be omitted.

[**0050**] After this structure is formed, usual middle-end and back-end of the line processes can be done including back gate contact formation.

[**0051**] **FIG. 14** shows an alternative device structure in which the dielectric layer **15** is formed only at the bottom of the cavity **13** (see discussion in connection with **FIGS. 10-12**), and both the gate isolating layer **14** and isolating spacer **7** are omitted. In this embodiment, the gate spacer structure **16**a, **16**b is also adjacent to, and in contact with, both the source contact, the drain contact and the overlayer **11**.

[0052] Although the present invention shows the formation of one FET structure, the formation of a plurality of such FET structures on a single substrate is also contemplated.

[0053] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

[0054] Any disclosed embodiment may be combined with one or several of the other embodiments shown and/or described. This is also possible for one or more features of the embodiments.

[0055] It is understood that a person skilled in the art can modify the shown arrangements in many ways without departing from the gist of the invention which is encompassed by the subsequent claims.

1. A MOSFET comprising:

a source extension;

a source contact disposed on said source extension;

a drain extension;

a drain contact disposed on said drain extension;

a channel between said source extension and said drain extension;

a dielectric layer above said channel;

a gate spacer structure disposed on a peripheral portion of a top surface of said dielectric layer and having an internal surface that meets said top surface at about a right angle;

a gate disposed on a non-peripheral portion of said top surface of said dielectric layer and having at least a lower portion surrounded by and in contact with said internal surface of said gate spacer structure; and said gate is substantially aligned at its bottom with said channel.

2. The MOSFET of claim 1, wherein said gate spacer structure is adjacent to said source and drain contacts.

3. The MOSFET of claim 1, wherein said dielectric layer comprises a material with a dielectric constant greater than about **10**.

4. The MOSFET of claim 1, wherein said dielectric layer has a U-shaped cross-section with a vertical portion adjacent the peripheral portion of said top surface of said dielectric layer.

5. The MOSFET of claim 4, wherein an upper portion of said gate is surrounded by the vertical portion of said U-shaped dielectric layer.

6. The MOSFET of claim 1, further comprising an isolating spacer structure separating said dielectric layer from said source contact and said drain contact.

7. The MOSFET of claim 6, wherein said isolating spacer structure is of unitary construction.

8. The MOSFET of claim 1, wherein said gate further has an upper portion surrounded by an isolating spacer structure disposed between said dielectric layer and said source contact and said drain contact.

9. The MOSFET of claim 1, wherein said gate further has an upper portion surrounded by an insulating layer disposed over said source contact and said drain contact.

10. The MOSFET of claim 9, wherein said gate spacer structure is in contact with said source and drain contacts and said insulating layer.

11. The MOSFET of claim 1, further comprising a gate-isolating layer between said channel and said dielectric layer.

12. The MOSFET of claim 1, wherein said gate spacer structure is of unitary construction.

13. A method for forming a MOSFET, comprising the steps of:

a) providing a channel layer on a substrate;

b) forming a source extension and a drain extension in said channel layer thereby defining a channel between said source and drain extensions;

c) forming a dielectric layer over said channel;

d) forming a gate spacer structure over a peripheral portion of a top surface of said dielectric layer; said gate spacer structure having an internal surface with a lower portion that is substantially perpendicular to said top surface of said dielectric layer whereby a first cavity is defined at its sidewall by said internal surface of said gate spacer structure and at its bottom by said dielectric layer;

e) forming a gate contact by disposing an electrically conductive material into said first cavity to contact said top surface of said dielectric layer.

14. The method of claim 13, wherein said step (a) further comprises:

(a1) forming a sacrificial gate over said channel layer;

(a2) implanting dopants into said channel layer with said sacrificial gate acting as an implant mask;

(a3) annealing to activate said dopants thereby forming said source and drain extensions.

15. The method of claim 14, further comprising, prior to said steps (c) and (d):

f) forming a sacrificial gate spacer structure adjacent said sacrificial gate;

g) forming a source contact at said source extension and a drain contact at said drain extension;

h) forming an insulating layer on top of said source and drain contacts; and

i) removing said sacrificial gate and said sacrificial gate spacer structure to form a second cavity with a sidewall portion defined by said insulating layer and said source and drain contacts, and a bottom defined by said channel layer; wherein said gate spacer structure and said dielectric layer are formed inside said second cavity.

16. The method of claim 15, further comprising:

j) forming an isolating spacer structure on said source/drain extensions, said isolating spacer structure being adjacent to said source and drain contacts.

17. The method of claim 15, further comprising, prior to said step (c):

k) growing a sacrificial oxide layer at the bottom of said second cavity; and

l) removing said sacrificial oxide layer.

18. The method according to claim 13, further comprising forming said gate spacer structure by filling a spacer material into said first cavity and etching it anisotropically to expose said dielectric layer.

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