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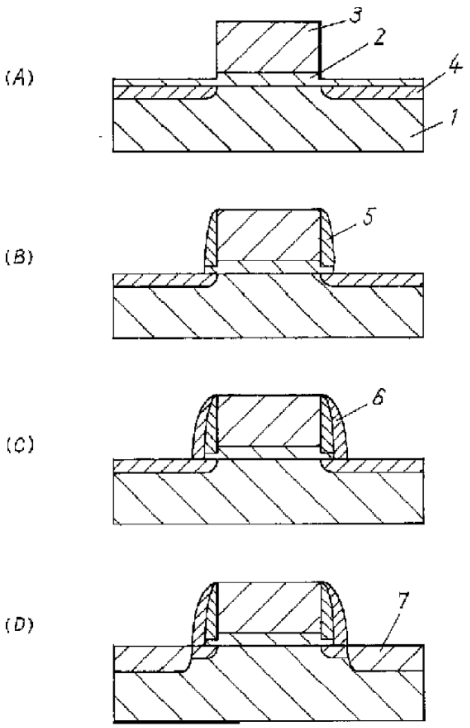
(54) [Name of invention] Semiconductor device and manufacturing method thereof

(57) [Summary]

[Task] The task aimed to be solved is to provide semiconductor devices and manufacturing methods that suppress pressure resistance defects and reliability degradation of high dielectric gate dielectric films, and prevent the reduction of high specific dielectric constants.

[Solution method] As a first sidewall consisting of a dielectric film is formed on the sidewall after the formation of a gate electrode, it is possible to suppress pressure resistance defects and reliability deterioration due to loss of the film or damage of the high dielectric gate insulating film. In addition, a second sidewall consisting of an oxidative resistant film is formed over the first sidewall, so that an ultra-thin SiO_2 film is not formed at the Si interface in a later step. This means that the high dielectric constant of the high dielectric gate dielectric film can be prevented from decreasing.



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U.S. Patent 8,587,076

[Scope of Patent Claims]

[Claim 1] In a semiconductor device that functions as a MOSFET,

A semiconductor device characterized in that it comprises a gate insulating film consisting of a high dielectric film formed on a semiconductor substrate, a gate electrode consisting of a conductive film formed on the gate insulating film, a first sidewall consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall consisting of an oxidizing resistant film formed over the first sidewall.

[Claim 2] The semiconductor device of claim 1, characterized in that the top of the first sidewall is lower than the height of the gate electrode.

[Claim 3] Semiconductor device according to claim 1 or 2, characterized in that the gate insulating film and the first sidewall consist of the same dielectric film.

[Claim 4] A semiconductor device according to any one of Claims 1 to 3, characterized in that it further comprises a cap film formed on the gate electrode comprising an oxidation resistant film.

[Claim 5] A method for manufacturing a semiconductor device that functions as a MOSFET,

comprising the steps of: (a) forming a gate insulating film made of a high dielectric film on a semiconductor substrate;

(b) forming a gate electrode made of a conductive film on the gate insulating film;

(c) forming a first sidewall made of a dielectric film on a side wall of the gate electrode;

and (d) forming a second sidewall made of an oxidation-resistant film so as to cover the first sidewall.

[Claim 6] A method of manufacturing a semiconductor device according to claim 5, characterized in that the top of the first sidewall is formed to be lower than the height of the gate electrode.

[Claim 7] A method of manufacturing a semiconductor device according to claim 5 or 6, characterized in that the gate insulating film and the first sidewall comprise the same dielectric film.

[Claim 8] In a method of manufacturing a semiconductor device that functions as a MOSFET,

comprising the steps of: (a) forming a gate insulating film made of a high dielectric film on a semiconductor substrate;

sequentially depositing a conductive film and an oxidation resistant film on the gate insulating film (b);

providing an etch mask on the oxidizing resistant film to sequentially etch the oxidizing resistant film and the conductive film to form a cap film and a gate electrode (c);

forming a first sidewall consisting only of a dielectric film on a sidewall of the gate electrode (d);

forming a second sidewall (e) consisting of an oxidation resistant film over the first sidewall.

[Claim 9] The method of manufacturing a semiconductor device according to claim 8, characterized in that the top of the second sidewall is coupled to the sidewall of the cap film.

[Claim 10] A method of manufacturing a semiconductor device according to claim 8 or 9, characterized in that the gate insulating film and the first sidewall comprise the same dielectric film.

[Detailed Description of Invention]

[0001]

[Technical field to which the invention belongs] The present invention relates to semiconductor devices and manufacturing methods thereof, and in particular to insulating gate type field effect transistors having a gate dielectric film (high dielectric constant material).

[0002]

[Prior Art] Recently, advances in semiconductor process processing technology have led to the miniaturization of insulating gate type field effect transistors (hereinafter referred to as MOSFETs) using silicon oxide films (hereinafter referred to as SiO_2 films). However, if the gate insulating film is thinned in conjunction with the proportional reduction of MOSFET, the problem is that the gate leak current increases due to tunnel current. To avoid this problem, research is being conducted on MO SFETs that have a gate insulating film (hereinafter referred to as a high dielectric gate insulating film) consisting of a high dielectric using a zirconium oxide film (hereinafter referred to as a ZrO_2 film) or the like. On the other hand, as microfabrication of the gate electrode proceeds with the reduction of the element, reactive ion etching (hereinafter referred to as RIE) that realizes anisotropy causes a loss of film or damage to the gate insulating film underlying the gate electrode. This causes poor pressure resistance and reliability degradation of the gate insulation film. To remedy this problem, conventional MOS FETs reoxidize the silicon substrate after forming the gate electrode to form a birds beak (hereinafter referred to as gate birds beak) at the bottom edge of the gate electrode. A known example of such a MOSFET having a gate bird's beak is disclosed in Japanese Patent Publication No. 6-204237.

[0003] The structure of MOSFETs with conventional gate birds beaks and their manufacturing methods are described below with reference to the drawings. Figure 4 is a cross-sectional view showing the manufacturing process of a conventional n-type MOSFET.

[0004] In Figure 4, 21 is a semiconductor substrate consisting of a p-type silicon monocrystalline (hereinafter referred to as a Si substrate), 22 is a gate insulating film consisting of a SiO_2 film, 23 is a gate electrode consisting of an n-type polycrystalline silicon film (hereinafter referred to as a polySi film), 24 is an LDD diffusion layer consisting of an n-type, 25 is a SiO_2 film consisting of a TEOS film, and 27 is a source drain diffusion layer consisting of an n^+ type.

[0005] First, as shown in Figure 4(A), after forming an element separation layer (not shown) on the Si substrate 21 consisting of a silicon monocrystalline of type p having a (100) surface, the Si substrate 21 is thermally oxidized to form a SiO_2 film 22 that becomes a gate insulating film. Subsequently, after depositing an n-type polySi film on SiO_2 film 22 by CVD method, a resist film (not shown) is RIEd onto the mask to form gate electrode

23. At this time, the SiO_2 film 22 of the base film is also etched to reduce the film. In addition, etch damage causes damage to the surface of SiO_2 film 22. After removing the resist membrane, the gate electrode 23 is ion-implanted into the mask, for example arsenic, to form an LDD diffusion layer 24 of the n type on the surface of the Si substrate 21.

[0006] Next, as shown in Figure 4(B), when the Si substrate 21 is again thermally oxidized to form a SiO_2 film 25 on the LDD diffusion layer 24, a gate birds beak is formed at the bottom edge of the gate electrode 23. In this way, the SiO_2 film 22 reduced by etching is reoxidized to a thick SiO_2 film 25. Damage to the surface of the SiO_2 film 22 is also restored by reoxidation. Therefore, it is possible to suppress pressure resistance defects and reliability deterioration of gate insulating film.

[0007] Next, after depositing a TEOS film over the gate electrode 23 by CVD method as shown in Figure 4(C), a RIE is performed on this TEOS film to form a sidewall 26 on the sidewall of the gate electrode 23.

[0008] Next, as shown in Fig. 4(D), gate electrode 23 and sidewall 26 are ionized into a mask, for example, arsenic, to form an n^+ source drain diffusion layer 27 on the surface of Si substrate 21. Finally, conventional MOSFETs are completed by sequentially forming interlayer insulation films, contact holes and metal wiring on the Si substrate 21, not shown, using well-known techniques.

[0009] As described above, by forming a gate birds beak, the increase in gate leak current is suppressed, and MOSFET is realized that does not cause pressure resistance failure or reliability deterioration.

[0010]

[Problem the invention will solve] However, while the conventional configuration can be applied to MOSFETs using SiO_2 films, it could not be applied to MOSFETs using high dielectric gate insulating films consisting of ZrO_2 films, etc. for the following reasons.

[0011] In the oxidation process of forming gate birds beak, oxidizing species (oxygen, etc.) enters the interface with the ZrO_2 film or Si substrate from the bottom edge of the gate electrode, further diffuses the interface and the film, oxidizes the Si substrate under the gate electrode, and forms a thin SiO_2 film. As a result, the gate insulating film is substantially a layered film of ZrO_2 film and thin SiO_2 film, so the specific dielectric constant of the entire gate insulating film is reduced compared to the original ZrO_2 film. For example, after forming a ZrO_2 film with a specific dielectric constant of 15 to 20 and a film thickness of 5.0 nm, a gate birds beak is formed, and a thin SiO2 film with a specific dielectric constant of 3.9 and a film thickness of 0.2 to 0.3 n m is formed at the interface. In this case, the specific dielectric constant of the entire gate insulating film is 13 to 17, and the film thickness is 5.2 to 5.3 nm. In other words, although the overall film thickness of the gate insulating film increases by only about 5%, the specific dielectric constant decreases by about 14%, resulting in a significant decrease in the current capacity of MOSFETs. In addition, since a wedge-like thick SiO_2 film is formed at the bottom edge of the gate electrode, the effective gate length changes and the threshold voltage of the MOSFET changes. As such, there was a problem that the electrical properties of MOSFETs would degrade or fluctuate if gate birds beaks were formed in MOSFETs using high dielectric gate insulating films.

[0012] Even if a gate bird's beak is not formed, if a heat treatment in an oxidizing or oxygen-containing atmosphere or deposition of an insulating film is performed after the formation of the gate electrode, an extremely thin SiO2 film is formed at the Si interface, just as in the case of forming a gate bird's beak, and the relative dielectric constant of the entire gate insulating film decreases. Therefore, there was a problem in this case as well that the electrical properties of MOSFETs using high dielectric gate dielectric film would degrade.

[0013] The present invention is made in consideration of the above problems, and is intended to provide semiconductor devices and manufacturing methods thereof that suppress pressure resistance defects and reliability degradation of high dielectric gate insulating films and prevent the reduction of high specific dielectric constants.

[0014]

[Methods for solving the problem] To achieve the above objectives, the semiconductor device of the present invention is characterized in that in a semiconductor device that functions as a MOSFET, the semiconductor device comprises a gate insulating film consisting of a high dielectric film formed on a semiconductor substrate, a gate electrode consisting of a conductive film formed on a gate insulating film, a first sidewall consisting of a dielectric film formed on a sidewall of the gate electrode, and a second sidewall consisting of an oxidizing resistant film formed to cover the first sidewall.

[0015] With this configuration, pressure resistance failure and reliability deterioration due to loss of film or damage of high dielectric gate insulating film can be suppressed. Furthermore, since an ultra-thin SiO_2 film is not formed at the Si interface in a later process, it is possible to prevent a decrease in the specific dielectric constant of the high dielectric gate insulating film.

[0016] In the semiconductor device described above, the top of the first sidewall is preferably lower than the height of the gate electrode.

[0017] In the semiconductor device described above, it is preferred that the gate insulating film and the first sidewall consist of the same dielectric film.

[0018] In the semiconductor device described above, it is preferred to further comprise a cap film consisting of an oxidation resistant film formed on a gate electrode.

[0019] The method of manufacturing the semiconductor device of the present invention is also characterized in that, in a method of manufacturing a semiconductor device that functions as a MOSFET, it comprises the steps of (a) forming a gate insulating film consisting of a high dielectric film on a semiconductor substrate, (b) forming a gate electrode consisting of a conductive

film on the gate insulating film, (c) forming a first sidewall consisting of a dielectric film on a sidewall of the gate electrode, and (d) forming a second sidewall consisting of an oxidizing resistant film over the first sidewall.

[0020] With this configuration, pressure resistance defects and reliability degradation due to loss of film or damage of high dielectric gate insulation film can be suppressed. Furthermore, since an ultra-thin SiO_2 film is not formed at the Si interface in a later process, it is possible to prevent a decrease in the specific dielectric constant of the high dielectric gate insulating film.

[0021] In the above-described method of manufacturing semiconductor devices, it is preferred that the top of the first sidewall be formed to be lower than the height of the gate electrode.

[0022] In the above semiconductor device manufacturing method, it is preferred that the gate insulating film and the first sidewall consist of the same dielectric film.

[0023] Furthermore, the method of manufacturing the semiconductor device of the present invention is characterized by the steps of (a) forming a gate insulating film consisting of a high dielectric film on a semiconductor substrate, sequentially depositing a conductive film and an oxidative resistant film on the gate insulating film (b), providing an etch mask on the oxidative resistant film to sequentially etch the oxidative film and the conductive film to form a cap film and a gate electrode (c), forming a first side wall consisting of a dielectric film only on the sidewall of the gate electrode (d), and forming a second side wall consisting of an oxidative film to cover the first side wall (e).

[0024] With this configuration, pressure resistance defects and reliability degradation due to loss of membranes and damage of high dielectric gate insulating films can be suppressed. Furthermore, since an ultra-thin SiO_2 film is not formed at the Si interface in a later process, it is possible to prevent a decrease in the specific dielectric constant of the high dielectric gate insulating film.

[0025] In the above-described method of manufacturing semiconductor devices, the top of the second sidewall is preferably coupled to the sidewall of the cap film.

[0026] In the above semiconductor device manufacturing method, it is preferred that the gate insulating film and the first sidewall consist of the same dielectric film.

[0027]

[Embodiment of the Invention] (First embodiment) The first embodiment of the invention is described below with reference to the drawings. Fig. 1 is a cross-sectional view illustrating a manufacturing process of a semiconductor device that functions as an n-type MOSFET according to a first embodiment of the present invention.

[0028] In Fig. 1, 1 is a p-type Si substrate, 2 is a high dielectric gate insulating film consisting of ZrO_2 film, 3 is a gate electrode consisting of n-type polySi film, 4 is an LDD diffusion layer consisting of n-type, 5 is a first sidewall consisting of ZrO_2 film (insulation film), 6 is a silicon nitride film (oxidation resistant film, hereinafter referred to as Si_3N_4 film), and 7 is an n^+-type source drain diffusion layer.

[0029] First, as shown in Fig. 1(A), after forming an element separation layer (not shown) on the Si substrate 1 having a (100) surface, reactive sputtering is performed on the metal target consisting of Zr in the atmosphere of a mixture of argon gas and oxygen gas to form a ZrO_2 film 2 on the Si substrate 1 that becomes a high dielectric gate insulating film, for example, at a thickness of about 5 nm. Thereafter, an n-type polySi film is deposited on the ZrO_2 film 2 by C VD method, for example at a film thickness of about 200 to 300 nm, and then a resist film (not shown) is RIEd to the mask to form a gate electrode 3 on the ZrO_2 film 2. At this time, the ZrO_2 film 2 of the base film is also etched to reduce the film as in the conventional case. Also, etch damage causes damage to the surface of ZrO_2 film 2. After removing the resist membrane, gate electrode 3 is ion-implanted with, for example, arsenic to the mask to form an n-type L DD diffusion layer 4 on the surface of Si substrate 1.

[0030] Next, as shown in Fig. 1(B), after depositing a ZrO_2 film that is reactive sputtering and becomes an insulating film over the gate electrode 3 at a film thickness of, for example, about 20 to 100 nm, RI E is performed on this ZrO_2 film to form a first sidewall 5 consisting of a ZrO_2 film on the side of the gate electrode 3. At this time, the ZrO_2 film 2 of the base film is also etched at the same time to remove all. In this way, the film loss is eliminated because the ZrO_2 film is again deposited on the ZrO_2 film 2 that has been reduced by etching at the lower edge of the gate electrode 3. In addition, damage to the surface of the ZrO_2 film 2 is restored by redeposition. Therefore, as with conventional examples of forming gate birds beaks, it is possible to suppress pressure resistance defects and reliability degradation of high dielectric gate insulating films.

[0031] Next, as shown in Fig. 1(C), after depositing a Si_3N_4 film that becomes an oxidizing resistant film over the gate electrode 3 by means of a CVD method at a film thickness of, for example, about 50 to 200 nm, a RIE is performed on the Si_3N_4 film to form a second sidewall 6 to cover the first sidewall 5 provided on the sidewall of the gate electrode 3. In this way, the sidewalls of the gate electrode 3 are covered by a second sidewall 6 consisting of a Si_3N_4 film, such that heat treatment or deposition of an insulating film in an atmosphere comprising oxidation or oxygen gas after this step does not form an ultra-thin SiO_2 film at the Si interface. Therefore, it is possible to prevent a decrease in the specific dielectric constant due to the formation of an ultra-thin SiO_2 film, which is problematic in the case of a high dielectric gate insulating film.

[0032] Next, as shown in Fig. 1(D), gate electrodes 3, first sidewalls 5 and second sidewalls 6 are ion-implanted into the mask, for example, with arsenic to form an n^+ source drain diffusion layer 7 on the surface of the Si substrate 1. Finally, the MOSFET of the first embodiment is completed by sequentially forming interlayer insulation films, contact holes and metal wiring on the Si substrate 1, not shown, using known techniques.

[0033] As described above, according to the first embodiment, a

first sidewall consisting of a ZrO_2 film is formed in the sidewall after the formation of gate electrode 3, so that pressure resistance failure and reliability deterioration due to film loss and damage of the high dielectric gate insulating film can be suppressed. Furthermore, a second sidewall 6 consisting of Si_3N_4 films is formed to cover the first sidewall 5, so that an ultra-thin SiO_2 film is not formed at the Si interface in a later step. This means that the high dielectric constant of the high dielectric gate dielectric film can be prevented from decreasing. Therefore, semiconductor devices and manufacturing methods thereof that function as MOSFETs can be realized that suppress pressure resistance defects and reliability degradation of high dielectric gate dielectric films and prevent high dielectric constant reduction.

[0034] (Variations of the first embodiment) Below, variations of the first embodiment will be described with reference to the drawings. Fig. 2 is a cross-sectional view illustrating a manufacturing process of an n-type MOSFET according to a variant of the first embodiment; The components of Fig. 2 are the same as in Fig. 1, but the shapes of the first sidewall 5 and the second sidewall 6 are different.

[0035] First, as shown in Figure 2(B), after depositing a ZrO_2 film that becomes an insulating film over the gate electrode 3, a RIE is performed on the ZrO_2 film to form a first sidewall 5 consisting of a ZrO_2 film on the side of the gate electrode 3. Here, unlike the shape of Figure 1(B), a predetermined over-etch is performed to form the top of the first sidewall 5 at least 50 nm below the height of the gate electrode 3. Again, as in Fig. 1(B), the repositioning of the ZrO_2 film at the lower edge of the gate electrode 3 also improves the film loss and damage of the ZrO_2 film 2. Therefore, it is possible to suppress pressure resistance defects and reliability degradation of high dielectric gate insulating films.

[0036] Also, as shown in Fig. 2(C), after depositing a Si_3N_4 film that becomes an oxidation-resistant film overlying the gate electrode 3, a RIE is performed on the Si_3N_4 film to form a second sidewall 6 to cover the first sidewall 5 provided on the sidewall of the gate electrode 3. Again, unlike the shape of Figure 1(C), the top of the second sidewall 6 is formed thicker by a portion of the top of the first sidewall 5 that is lower than the height of the gate electrode 3, resulting in a thickness of at least about 50 nm. Again, as in Figure 1(C), even if heat treatment or deposition of an insulating film is performed in an atmosphere comprising oxidation or oxygen gas after this step, an ultra-thin SiO_2 film is not formed at the Si interface. Therefore, it is possible to prevent a decrease in the specific dielectric constant due to the formation of ultra-thin SiO_2 films, which is a problem in the case of high dielectric gate insulating films.

[0037] As described above, according to the variant of the first embodiment, the same effect as the first embodiment is obtained, and furthermore, the top of the first sidewall 5 is formed thicker than in the first embodiment, since the top of the second sidewall 6 is lower than the height of the gate electrode 3. Thus, even if the sidewall forming step is disjointed, the sidewalls of the gate electrode 3 can reliably be covered with a second sidewall consisting of an oxidative resistant film. Therefore, since there is no formation of an ultra-thin SiO_2 film at the Si interface in a later step, it is possible to reliably prevent a decrease in the specific dielectric constant of the high dielectric gate dielectric film than in the first embodiment.

[0038] (Second embodiment) A second embodiment of the present invention is described below with reference to the drawings. Fig. 3 is a cross-sectional view illustrating a manufacturing process of a semiconductor device that functions as an n-type MOSFET according to a second embodiment of the present invention.

[0039] In Figure 3, 11 is a high dielectric gate insulating film consisting of a p-type Si substrate, 12 is a gate electrode consisting of a ZrO_2 film, 13 is a gate electrode consisting of an n-type polySi film, 14 is an n-type L DD diffusion layer, 15 is a first sidewall consisting of a ZrO_2 film (insulation film), 16 is a second sidewall consisting of a Si_3N_4 film (oxidation resistant film), 17 is a n^+-type source drain diffusion layer, and 18 is a cap film consisting of a Si_3N_4 film (oxidation resistant film).

[0040] First, as shown in Fig. 3(A), after forming an element separation layer (not shown) on the Si substrate 11 having a (100) surface, reactive sputtering is performed on the metal target consisting of Zr in the atmosphere of a mixture of argon gas and oxygen gas to form a ZrO_2 film 12 that becomes a high dielectric gate insulating film on the Si substrate 11, for example, at a film thickness of about 5 nm. Subsequently, Then, an n-type poly-Si film is deposited on the ZrO_2 film 12 by a CVD method to a thickness of, for example, about 200 to 300 nm, and then a Si3N4 film serving as an oxidation-resistant film is deposited to a thickness of, for example, about 50 to 100 nm. After that, RIE is performed using a resist film (not shown) as a mask to form a gate electrode 13 made of an n-type poly-Si film and a cap film 18 made of a Si_3N_4 film on the ZrO_2 film 12. At this time, the ZrO_2 film 12 of the base film is also etched to reduce the film. In addition, etch damage causes damage to the surface of ZrO_2 film 12. After removing the resist membrane, the gate electrode 13 is ion-implanted, for example, with arsenic, into the mask to form an L DD diffusion layer 14 of type n on the surface of the Si substrate 11.

[0041] Next, as shown in Fig. 3(B), as described above, after reactive sputtering is performed to deposit a ZrO_2 film that becomes an insulating film over the gate electrode 13 and the cap film 18, for example, at a film thickness of about 20 to 100 nm, a RIE is performed on this ZrO_2 film to form a first sidewall 15 consisting of a ZrO_2 film only on the side of the gate electrode 13. At this time, the ZrO_2 film 12 of the base film is also etched at the same time to remove all. In this way, the film loss is eliminated because the ZrO_2 film is again deposited on the ZrO2

film 12 that has been reduced by etching at the lower edge of the gate electrode 13. Damage to the surface of the ZrO_2 film 12 is also restored by repositioning. Therefore, as with conventional examples of forming gate birds beaks, it is possible to suppress pressure resistance defects and reliability degradation of high dielectric gate insulating films.

[0042] Next, as shown in Fig. 3(C), a Si_3N_4 film that becomes an oxidizing resistant film over the gate electrode 13 by means of a CVD method is deposited at a film thickness of, for example, about 50 to 200 nm, and then a RIE is performed on the Si_3N_4 film to form a second sidewall 16 to cover the first sidewall 15 provided on the sidewall of the gate electrode 13. In this way, as the sidewalls of the gate electrode 13 are covered by a second sidewall 16 consisting of a Si_3N_4 film, heat treatment or deposition of an insulating film in an atmosphere comprising oxidation or oxygen gas after this step does not form an ultra-thin SiO_2 film at the Si interface. In addition, the top surface of gate electrode 13 is also covered with a cap film 18 consisting of Si_3N_4 films, so as to prevent the diffusion of oxidized species through the grain boundaries of the polySi films that make up gate electrode 13, there is no formation of ultra-thin SiO_2 films at the Si interface. Therefore, it is possible to prevent a decrease in the specific dielectric constant due to the formation of ultra-thin SiO_2 films, which is a problem in the case of high dielectric gate insulating films.

[0043] Next, as shown in Fig. 3(D), gate electrode 13, cap membrane 18, first sidewall 15 and second sidewall 16 are ion-implanted into the mask, for example, to form an n^+ source drain diffusion layer 17 on the surface of Si substrate 11. Finally, the MOSFET of the second embodiment is completed by sequentially forming interlayer insulation films, contact holes and metal wiring on the Si substrate 11, not shown, using well-known techniques.

[0044] As described above, according to the second embodiment, a first sidewall consisting of a ZrO_2 film is formed in the sidewall after the formation of the gate electrode 13, so that pressure resistance defects and reliability deterioration due to loss of the film or damage of the high dielectric gate insulating film can be suppressed. Furthermore, because a cap film 18 consisting of Si_3N_4 film is formed over gate electrode 13 and a second sidewall 16 consisting of Si_3N_4 film is formed over first sidewall 15, an ultra-thin SiO_2 film is not formed at the Si interface in a later step. This means that the high dielectric constant of the high dielectric gate dielectric film can be prevented from decreasing. Therefore, semiconductor devices and manufacturing methods thereof that function as MOSFETs can be realized that suppress pressure resistance defects and reliability degradation of high dielectric gate dielectric films and prevent high dielectric constant reduction.

[0045] In the first to second embodiments, a ZrO_2 film was used for the high dielectric gate insulating film, but it goes without saying that other high dielectric films, such as a HfO_2 film, a Ta_2O_5 film, or a Al_2O_3 film, can be used instead to obtain the effects of the invention. Furthermore, the effects of the present invention can also be obtained by using a silicate film consisting of a high dielectric and a silicon triage compound in a high dielectric gate insulating film.

[0046] In addition, reactive sputtering was performed using a Zr target to form a ZrO_2 film that becomes a high dielectric gate insulating film, but instead, sputtering using a ZrO_2 target may be performed to form. Alternatively, CVD may be performed and formed using an organic compound of Zr, such as $C_{16}H_{26}HfO_4$, $C_{16}H_{40}N_4Zr$, and the like.

[0047] Also described using the same ZrO_2 film as the high dielectric gate insulating film on the first sidewall, but instead, the effects of the present invention can be obtained even with other dielectric films, such as TEOS films, BPSG films, or SiO N films.

[0048] Also described using a polySi film for the gate electrode, the effect of the present invention can be obtained by using another conductive film, such as W film, TiN film, WSi_2 film, etc., metal gate or silicide gate instead. Alternatively, the effects of the invention can be obtained using polymetal gate such as W/TiN/polySi films, $TiSi_2$/polySi films, and the like.

[0049]

[Effects of Invention] As explained above, according to the semiconductor device of the present invention and the manufacturing method thereof, a first sidewall consisting of dielectric film is formed on the sidewalls thereof after the formation of gate electrodes, so that pressure resistance defects and reliability degradation due to loss of membrane or damage of the high dielectric gate dielectric dielectric film can be suppressed. In addition, a second sidewall consisting of an oxidative resistant film is formed over the first sidewall, such that an ultra-thin SiO_2 film is not formed at the Si interface in a later step. This means that the high dielectric constant of the high dielectric gate dielectric film can be prevented from decreasing. Therefore, semiconductor devices and manufacturing methods thereof that function as MOSFETs can be realized that suppress pressure resistance defects and reliability degradation of high dielectric gate dielectric films and prevent high dielectric constant reduction.

[Brief Description of the Drawings]

[Figure 1] (A)-(D) shows a cross-sectional view showing the manufacturing process of the n-type MOSFET in the first embodiment of the present invention;

[Figure 2] (A)-(D) shows a cross-sectional view showing the manufacturing process of the n-type MOSFET in a variant of the first embodiment of the present invention;

[Figure 3] (A)-(D) shows a cross-sectional view showing the manufacturing process of the n-type MOSFET in a second embodiment of the present invention;

[Figure 4] (A)-(D) shows a cross-sectional view showing the manufacturing process of conventional n-type MO SFETs

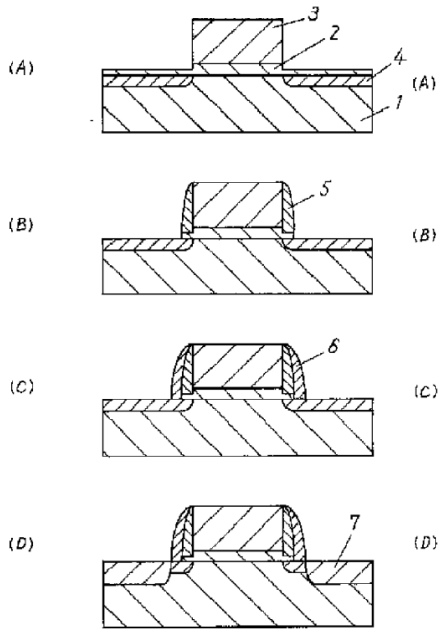
[Explanation of References]

1- and 11- p-type Si circuit packs

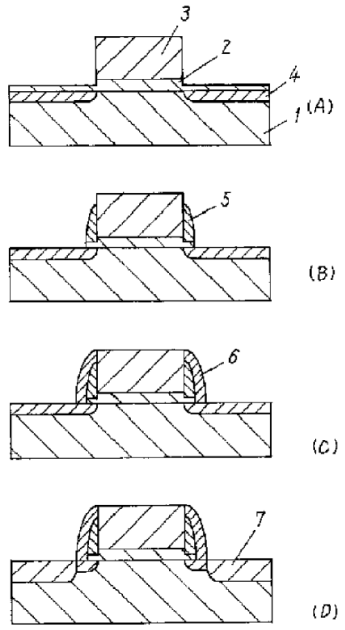
High dielectric gate insulation with 2, 12 ZrO_2 films

Gate electrode consisting of 3, 13 n polySi membranes
L DD diffusion layer of 4, 14 n type
First sidewall of 5, 15 ZrO_2 films (insulation film)
Second sidewall of 6, 16 Si_3N_4 membranes (oxidation resistant membranes)
Source drain diffusion layer of 7, 17 n^+ type
Cap membrane consisting of 18 Si_3N_4 membrane (oxidation resistant membrane)

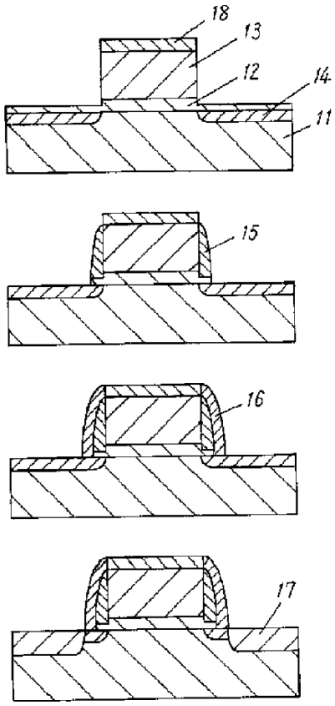
[Fig. 1]



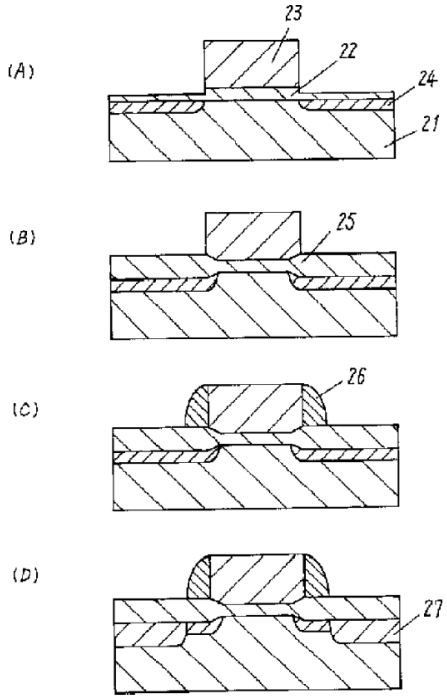
[Fig. 2]



[Fig. 3]



[Fig. 4]



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F term (reference)	5F140	AA06	AA25	BA01	BA20	BD11
		BE09	BE10	BF03	BF04	BF07
		BF08	BF10	BF11	BF18	BF20
		BF21	BF27	BG09	BG11	BG12
		BG13	BG14	BG22	BG38	BG51
		BG53	BH15	BK02	BK09	BK13

TRANSPERFECT

TRANSLATOR'S DECLARATION

I, Aeten Weaver, a translator fluent in the Japanese and English languages, as a vendor to Transperfect Translations, declare the following. The following is, to the best of my knowledge and belief, a true and correct statement that the translation of the document(s) listed below was done in a form that best reflects the intention and meaning of their original text.

1. I reviewed the Japanese-language document JP2003-258241d "JP2003-258241," submitted as TSMC-1010.

2. I prepared the English-language translation document "JP2003-258241" submitted as TSMC-1011 by reviewing and translating the Japanese-language document "JP2003-258241."

3. The English-language translation document "JP2003-258241" is, to the best of my knowledge and belief, a true and accurate English-language translation of the Japanese-language document "JP2003-258241."

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and contain no willful false statements and the like.

Executed on: April 3, 2025

[SIGNATURE]

Aeten Weaver
[NAME]