

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC,

Patent Owner.

IPR2025-00831

U.S. Patent 8,587,076

**DECLARATION OF JACK LEE, PH.D. IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT 8,587,076**

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EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 8,587,076 to Hirase et al. (“the ’076 patent”)
1002	File History of U.S. Patent 8,587,076 (“’076 File History”)
1004	CV of Dr. Jack Lee
1005	Translated Excerpts from JP File History
1006	U.S. Patent 7,579,227 to Hirase, et al. (“the ’227 patent”)
1007	U.S. Patent 7,923,764 to Hirase et al. (“the ’764 patent”)
1008	File History of U.S. Patent 8,253,180 (“’180 File History”)
1009	U.S. Publication 2003/0025135 to Matsumoto, et al. (“Matsumoto”)
1010	JP2003-258241 to Kajiyama (“JP-Kajiyama”)
1011	Certified Translation of JP2003-258241 to Kajiyama (“Kajiyama”)
1013	U.S. Publication 2005/0051856 to Ono, et al. (“Ono”)
1018	Wilk, G. D., et al., “High-k gate dielectrics: Current status and materials properties considerations,” Journal of Applied Physics, Vol. 89, No. 10, pp. 5243-5275, May 15, 2001 (“Wilk”)
1023	U.S. Patent 6,306,712 to Rodder, et al. (“Rodder”)
1024	Sim, J. H., et al., “Effects of ALD HfO ₂ thickness on charge trapping and mobility,” Microelectronic Engineering, Vol. 80, pp. 218-221, June 17, 2005 (“Sim”)
1027	U.S. Publication 2002/0063299 to Kamata, et al. (“Kamata”)
1028	U.S. Publication 2006/0091432 to Guha, et al. (“Guha”)

Exhibit	Description
1029	Koyama, M., et al., “Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics,” Digest of International Electron Devices Meeting, pp. 849-852, Dec. 8-11, 2002 (“Koyama”)
1031	U.S. Patent 6,911,695 to Ahmed, et al. (“Ahmed”)
1032	Houssa, M., “High-k Dielectrics to Houssa” (IOP Publishing Ltd. 2004) (“Houssa”)
1033	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1034	Wolf, S., “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (Lattice 2002) (“Wolf”)
1037	Lee, S. J., et al. “High quality ultra thin CVD HfO ₂ /sub 2/ gate stack with poly-Si gate electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1038	Campbell, “The Science and Engineering of Microelectronic Fabrication”, Second Edition (2001) (“Campbell”)
1040	JP2005-064190 to Ono with certified translation (“JP-Ono”)
1041	N. Weste and D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Third Edition (Pearson/Addison Wesley, 2005) (“Weste”)
1048	U.S. Patent 6,504,214 to Yu, et al. (“Yu”)
1049	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1050	U.S. Publication 2005/0040479 to Koldiaev, et al. (“Koldiaev”)
1051	U.S. Publication 2005/0139932 to Cho, et al. (“Cho”)

I, Dr. Jack Lee, declare as follows:

1. I have been retained on behalf of Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner” or “TSMC”) as a technical expert witness in connection with the petition for Inter Partes Review (“Petition”) of U.S. Patent 8,587,076 to Hirase (“the ’076 patent”). It is my understanding that the ’076 patent is currently assigned to Advanced Integrated Circuit Process LLC (“Patent Owner”).

2. I have been asked by Petitioner to offer opinions regarding the ’076 patent, including the patentability of the claims in view of certain prior art references and the knowledge of a person of ordinary skill in the art. I have also been asked to provide my technical opinions on how concepts in the ’076 patent specification relate to claim limitations of the ’076 patent. This declaration sets forth the opinions I have reached to date regarding these matters.

3. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so.

4. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the

substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '076 patent.

I. Qualifications

5. I am an expert in the field of semiconductor process technology and semiconductor design. I have over 40 years of first-hand experience as a researcher, educator, and consultant in this field.

6. In formulating my opinions, I have relied on my knowledge, training, and experience in the relevant field, which I will summarize briefly. A more detailed summary of my background, education, experience, and publications is set forth in my curriculum vitae ("CV"), which is provided as TSMC-1004.

7. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley ("UC Berkeley").

8. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

9. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

10. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

11. My current research and teaching interests encompass high-K gate dielectrics and gate electrodes, semiconductor devices, fabrication processes, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, semiconductor memory applications, and alternative channel materials.

12. I have been invited to give talks, teach short courses and participate in panel discussions at numerous conferences specifically on the topic of high-K gate dielectrics and gate electrodes. This includes prestigious conferences such as the Symposium on VLSI Technology, the IEEE International Electron Devices Meeting, and other global forums. My research group at The University of Texas at Austin is recognized as a pioneer in developing hafnium-based high-K materials for nanoscale MOSFETs applications. I have extensive experience in this field, with numerous publications in journals and conference proceedings on the topics of HfO₂, HfSiON, hafnium silicate, interfacial layers, and dielectric reliability.

13. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

14. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 book and book chapters on semiconductor technologies. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g. inventor recognition and best paper awards.

15. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to

silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

16. I have served in various technology consulting and business advisor roles. For example, I have been teaching short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

II. Materials Considered

17. The '076 patent is a division of an application leading to U.S. Patent No. 8,253,180 (“the '180 patent”), which is a division of an application leading to U.S. Patent No. 7,923,764 (the “'764 patent”), which is a division of the application leading to U.S. Patent No. 7,579,227 (the “'227 patent”). In reaching the opinions provided herein, I have considered the '076 patent, its U.S. prosecution history, the '227, '764, and '180 patents and their U.S. prosecution histories, the prosecution history of the foreign priority application (JP 2005-227457), and the references cited in my Declaration or Attachment A hereto.

18. I have also relied upon my own education, training, research, knowledge, and personal and professional experience in the field and have also considered the viewpoint of a person of ordinary skill in the art at the time of the '076 patent's priority date. As explained below, I am familiar with the level of skill of a person of ordinary skill in the art regarding the technology at issue as of that time frame.

19. In general, I have been asked to cite to the specification of a patent or patent publication using the following formats: (Patent, Col:Line Number(s)) or (Patent, Paragraph Number(s)). For example, the citation (TSMC-1001, 1:1-10) points to the '076 patent specification at column 1, lines 1-10. Also, for convenience, I have been asked to use italics to denote limitations from the challenged claims. Unless otherwise noted, all emphasis added.

III. Understanding of Relevant Legal Principles

20. I am not a lawyer, and I will not provide any legal opinions. Although I am not a lawyer, I have been advised certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims.

A. Patent Validity

21. I understand that the prior art to the '076 patent includes patents and printed publications in the relevant art that (1) were published more than a year

before the effective U.S. filing date of the application leading to the '227 patent (July 24, 2006), or (2) otherwise predate the '227 patent's foreign priority date (August 5, 2005), both of which I have been instructed to assume for purposes of my analysis that the '076 patent can claim the benefit of. I further understand that, for purposes of this proceeding in the United States Patent Trial and Appeal Board, only patents and documents that have the legal status of a "printed publication" may be relied on as prior art.

22. I understand that a patent claim is anticipated if a single prior art document describes every element of the claim such that a person of ordinary skill in the art ("POSITA") could practice the claimed method without undue experimentation.

23. I understand that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art. I further understand that in analyzing the obviousness of a claim, the following factors may be taken into account: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art; and (4) any so called "secondary considerations" of non-obviousness, if they are present. I am not aware of any evidence of secondary considerations of non-obviousness relevant to the '076 patent. I reserve the right to supplement this Declaration if Patent Owner ("PO") introduces evidence of secondary considerations of non-obviousness.

24. I understand that to prove that prior art or a combination of prior art renders a patent obvious, it is necessary to:

- (1) identify the particular references that, singly or in combination, make the patent obvious;
- (2) specifically identify which elements of the patent claim appear in each of the asserted references; and
- (3) explain why a person of ordinary skill in the art would have combined the references, and how they would have done so, to create the inventions claimed in the patent. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of known technique(s) to improve similar devices (methods or products) in the same way;
- applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- “obvious to try” – choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;

- known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a person of ordinary skill in the art; and
- some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

25. I understand that anticipation or obviousness may be by express disclosure in the prior art. I also understand that a patent claim is invalid if it is anticipated or obvious in view of the prior art, and that a claim can be unpatentable even if all of the requirements of the claim cannot be found in a single prior-art reference. For example, I also understand that if the prior art references does not expressly set forth a particular claim element, the prior art may still anticipate or render obvious a patent claim if that element is “inherent” in its disclosure—that is, if it is necessarily found in the reference. A property is inherent even if a POSITA would not have appreciated that property as of the date of that prior art.

26. I understand that invalidity of a claim requires that the claim be anticipated or obvious from the perspective of a person of ordinary skill in the art

at the time the invention was made. To that end, I understand that in considering obviousness, hindsight reasoning derived from the patent-at-issue may not be used.

27. I understand that some claims are independent, and that these claims are complete by themselves. Other claims refer to these independent claims and are “dependent” from those independent claims. The dependent claims include all of the limitations of the claims on which they depend. Moreover, although I understand that preambles are not ordinarily treated as claim limitations, but for my declaration only, have been asked to complete my analysis as if the preambles were deemed limiting.

B. Claim Construction

28. I understand that “claim construction” is the process of determining a patent claim’s meaning. I understand the claim construction standard used in IPRs seeks to give claim terms their plain and ordinary meaning to a POSITA at the time of the claimed invention in view of the claims, specification, and prosecution history. I also understand that if the patent applicant gave a term a special meaning in the specification or during prosecution, then the special meaning should be used.

29. In my declaration, I apply the above understanding. In my view, no claim terms require explicit construction in this proceeding to resolve patentability of the claims.

C. Level of Ordinary Skill in the Art

30. I understand that certain issues relating to the validity of a patent must be judged from the perspective of a person of ordinary skill in the relevant art, as I discuss below. I have been asked to define the level of a “person of ordinary skill in the art” or “POSITA” at the time the alleged invention as claimed was made (which as discussed above, I have assumed to be August 5, 2005, for the ’076 patent). In deciding the level of ordinary skill, I have considered the following factors, which I have been informed are relevant to the determination of ordinary skill in the art.

- levels of education and experience of persons working in the field;
- types of problems encountered in the art;
- prior art solutions to these problems;
- rapidity with which innovations are made; and
- sophistication of the technology.

31. In my opinion, a POSITA at the time of the alleged invention of the ’076 patent would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education.

32. My opinions regarding the level of ordinary skill in the art are based on, among other things, my experience conceiving, patenting, and prototyping novel technology for semiconductor devices and semiconductor fabrication processes. Although my qualifications and experience exceed those of the hypothetical person having ordinary skill in the art, my analysis and opinions regarding the '076 patent have been based on the perspective of a person of ordinary skill in the art as of August 5, 2005.

IV. '076 Patent – Technical Background and Overview

33. The '076 patent, titled “Semiconductor Device,” to Junji Hirase, et al., was filed on July 12, 2012, as a divisional of the '180 patent (filed March 1, 2011), which was a divisional of the '764 patent (filed on July 20, 2009), which was a divisional of the '227 patent, filed on July 24, 2006. The '227 patent claims priority to JP Application 2005-227457, filed on August 5, 2005. Solely for purposes of this IPR, I have been asked to assume August 5, 2005 as the earliest priority date claimed on the face of the '076 patent. However, my opinions set forth herein would not change if the priority date was determined to be July 24, 2006.

34. At a high level, the '076 patent relates to metal insulator semiconductor field-effect transistors (MISFETs) having a high dielectric constant (high-k) gate insulating film that extends from under the gate electrode to under an

insulating sidewall structure. (TSMC-1001, 1:18-24, 2:9-19, 2:39-46.) I will discuss this concept, which was known in the art before the filing of the '076 patent, in greater detail below.

A. Technical Background

35. A semiconductor device is an electronic component that exploits the properties of semiconductor materials such as silicon, germanium, gallium arsenide, etc. Many types of semiconductor devices exist including, for example, diodes and metal-insulator-semiconductor (MIS) transistors (e.g., field effect transistors (FETs)), to name a few. (*See, e.g.*, TSMC-1033, 33-41.) In this Declaration, I will focus primarily on FET devices, and more particularly on MISFET devices which are described in further detail below.

1. MISFET/MOSFET

36. A metal-insulator-semiconductor field effect transistor (MISFET), also referred to as a metal-oxide-semiconductor field effect transistor (MOSFET) when the insulator is an oxide, is a common type of semiconductor device. Because most insulators traditionally used in FETs are oxides, it is common to use the terms MISFET and MOSFET interchangeably in the art. A typical MISFET device is a three-terminal structure with an input, referred to as the source, an output, referred to as the drain, and a control terminal, referred to as the gate electrode. (*See, e.g.*, TSMC-1033, 36.) Further to these terminals, the MISFET

includes a gate insulating layer that electrically isolates the conductive gate electrode from a silicon substrate in which the source and the drain terminals are formed. (See, TSMC-1041, 8 (MISFET “generally includes a stack of the conducting gate, an insulating layer, and the silicon wafer, also called the substrate, body or bulk.”).) In principle, the MISFET operates as a current switch, conducting current in an area between the source and drain regions, referred to as the “channel” or the “channel region”, when an appropriate voltage is applied to the gate electrode. (TSMC-1041, 9) The gate electrode modulates the electric field across the insulator, controlling the behavior of the device, hence the term field-effect transistor or FET. (TSMC-1041, 9.)

37. When appropriate voltage is applied to the gate electrode, a conducting path of minority carriers forms the channel between the source and the drain, and current can flow between the source and the drain via the formed channel. (TSMC-1041, 9.) When the MISFET is conducting current, it is in the “ON” state. Once the voltage is removed from the gate, the channel disappears, and ideally there is no current flow between the source and the drain regions. In this non-conductive state, the MISFET is in the “OFF” state. (TSMC-1041, 9.)

38. MISFETs are fabricated on silicon wafers that serve as the **substrate**. The substrate provides both mechanical support and an electrical common point. (TSMC-1041, 23.) The substrate can be doped with impurities, known as dopants,

to modulate its conductivity and influence the electrical behavior of the transistors built on it. (TSMC-1041, 7.) For example, doping the silicon substrate (or selective regions of the substrate) with boron (a Group III dopant) increases the number of *holes* (positive doping or p-type) when it replaces a silicon atom in the silicon crystal lattice, while doping the silicon substrate (or selective regions of the substrate) with arsenic (a Group V dopant) increases the number of free *electrons* (negative doping or n-type) when it replaces a silicon atom in the silicon crystal lattice. (TSMC-1041, 7; TSMC-1033, 17.) “The electrons or holes are introduced on a one for one basis by the dopants.” (TSMC-1033, 17.) “[T]o the extent that we can control the doping concentration accurately, we can precisely control the free electron and hole concentrations and therefore the conductivity of the silicon.” (TSMC-1033, 17.)

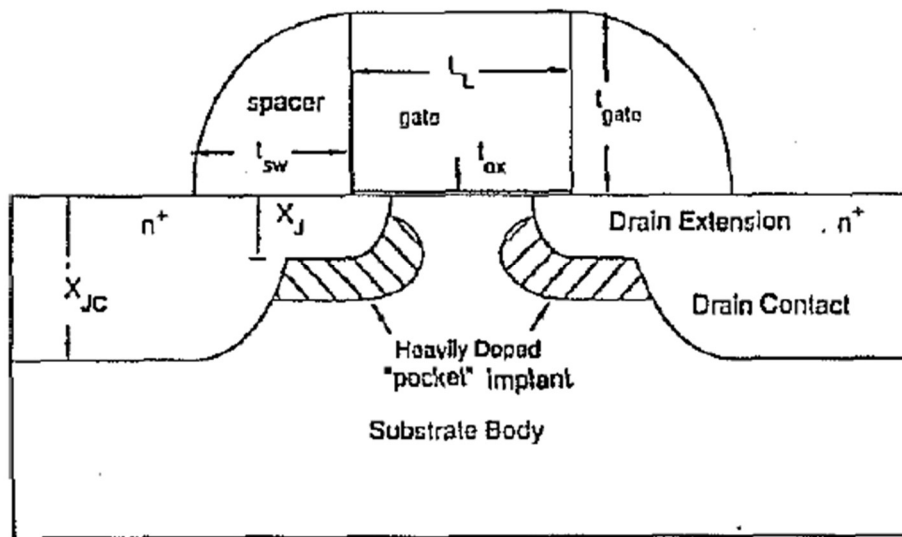
39. Once implanted, dopants or impurities need to be **activated** via one or more anneal processes, which also intend to repair any damage introduced to the silicon crystal lattice by the implant process. (TSMC-1033, 81-82.) Accordingly, the terms n-type and p-type dopants, as customarily used in the art, indicate activated dopants—i.e., dopants that can act as a donor or acceptor of electrons and contribute to the conductivity of a doped region.

40. **Doped regions**—including wells, source/drain regions, and channel regions—are created in the substrate through a selective doping process known as

ion implantation. (TSMC-1033, 375.) The source and drain regions, which are physically equivalent and therefore interchangeable, are formed by implanting dopants (either n-type or p-type) into the silicon substrate on either side of the gate electrode. (TSMC-1041, 8.) These regions are intentionally heavily doped to improve the conductivity and facilitate current flow when the transistor is in the ON state. The formation of these regions is critical for defining the transistor's electrical characteristics.

41. In aggressively scaled MISFET devices, source and drain regions may include **source/drain extension (or SDE) regions**. SDE regions may be lightly doped extension regions, known in the art as Lightly Doped Drain (LDD), or heavily doped extension regions, known in the art as Highly Doped Drain (HDD) extension. (TSMC-1033, 77; TSMC-1023, 2:61-62, 3:65-67.) SDE regions a graded doping profile between the source/drain regions and the channel region that suppresses short channel effects by ensuring a gradual transition in the electric field between the source/drain and the channel. (TSMC-1033, 77-78.) “[M]odest reductions in the field strength obtained through the [SDE regions] can make a significant difference in device reliability.” (TSMC-1033, 78.) Oftentimes, gate sidewall spacers are employed to control the position the leading edges of the SDE regions relative to the sidewall edges of gate electrode during the implant process. (TSMC-1033, 78.)

42. To further mitigate the short channel effects in aggressively scaled MISFET devices manifested by the presence of leakage current between the source and drain regions (known as punchthrough), **pocket implants** (also known as **halo implants**) are introduced just below the active channel and adjacent to the source/drain, as shown in Figure 5-27 below. (TSMC-1034, 219-20.)

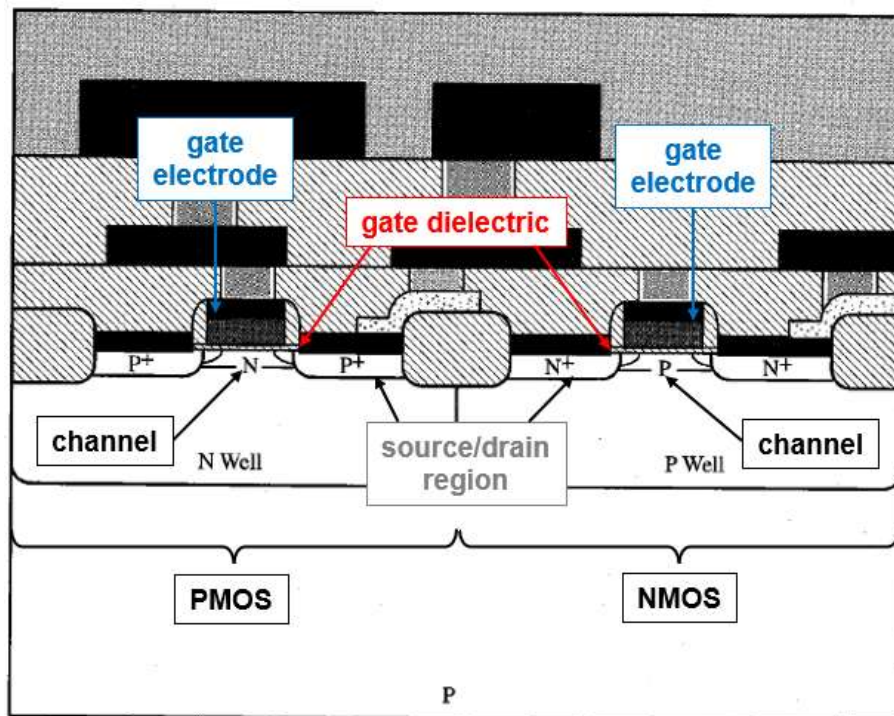


Wolf, Figure 5-27

43. The dopant type of the pocket implants is **opposite** to that of the source/drain and SDE implants—i.e., the pocket implants have the **same** conductivity type with the well in which the source/drain and SDE regions are formed (*see* discussion below). (TSMC-1034, 219.) Thus, if the source/drain and SDE implants are p-type, the pocket implants are n-type, and vice versa. “Precise

control of the placement and dose of this implant within the transistor-structure is needed to obtain the intended enhancements.” (TSMC-1034, 219.)

44. MISFETs with n-type source/drain regions are referred to as **NMOS**, and MISFETs with p-type source/drain regions are referred to as **PMOS**. (TSMC-1033, 13, Figure 1-11.)



Plummer, Figure 1-11

45. In modern complementary metal-oxide-semiconductor (CMOS) technology, NMOS and PMOS are fabricated and integrated onto the same wafer. (TSMC-1033, 52 (“Modern CMOS chips integrate millions of active devices (and NMOS and PMOS) side by side in a common silicon substrate.”)) Each NMOS and PMOS transistor is formed over doped wells of opposite conductivity type.

“These wells tailor the substrate doping locally to provide optimum device characteristics. The well doping affects device characteristics such as the MOS transistor threshold voltage and the I-V characteristics and PN junction capacitances” (TSMC-1033, 60.) For example, as shown in Figure 1-11 above, PMOS transistors are formed over an n-type well (N-well) and NMOS transistors are formed over a p-type well (P-well). The N and P wells are created in the substrate, which in this case is a p-type substrate, through selective doping (i.e., by selectively masking areas not intended to receive a particular dopant). (*See, e.g.*, TSMC-1033, 60-63.) This arrangement of the CMOS technology enables the creation of high-performance, energy-efficient logic circuits.

2. Gate Insulating Film

a. Materials

46. A common feature of a FET is the gate insulator (also referred to as gate dielectric or gate insulating film), which electrically isolates the gate electrode from the semiconductor channel. (TSMC-1033, 288.) For decades prior to the '076 patent, silicon dioxide (SiO_2) was the primary material used for gate dielectrics in MOSFETs. (TSMC-1033, 53 (“ SiO_2 is essentially a perfect insulator and provides the needed [electrical] isolation.”); TSMC-1032, 3-4.) However, as gate dielectric layers continued to shrink in thickness (e.g., below 1.5 nm), the use of SiO_2 became untenable, because the amount of gate-to-channel tunneling leakage

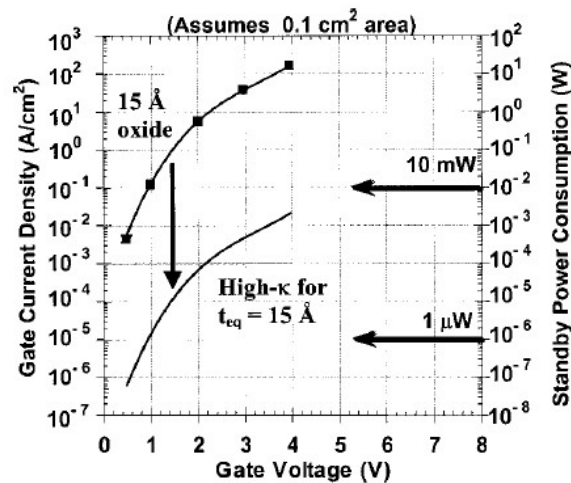
current passing through the gate dielectric prevents the gate electrode from effectively controlling the ON and OFF states of the FET. (TSMC-1034, 4-5, *see also* TSMC-1032, 5.)

47. A metal-insulator-semiconductor structure behaves like a parallel plate capacitor with a capacitance, $C = \frac{A \epsilon_r \epsilon_0}{t_{ox}}$, where A is the capacitor plate area, ϵ_r is the relative dielectric constant of the gate insulator (e.g., SiO₂), ϵ_0 is the permittivity of free space, and t_{ox} is the thickness of the gate insulator (e.g., SiO₂). (TSMC-1032, 8.) From the capacitance equation above, it is becoming apparent that decreasing the gate insulator thickness, t_{ox} , increases the capacitance, C, for the same gate voltage applied to the gate electrode. (TSMC-1032, 8.) However, as discussed above, the thickness of SiO₂ cannot be reduced indefinitely to increase or even sustain the same capacitance. Thus, “[a]n alternative way of increasing the capacitance is to use an insulator [a gate insulator] with a higher relative dielectric constant than SiO₂ [...]” (TSMC-1032, 8-9.) And because the dielectric would have a higher dielectric constant (i.e., a higher k value), this high-k dielectric could be thicker than SiO₂ and still achieve the same or higher capacitance value. This means that (i) the high-k would not suffer from the leakage current issues of SiO₂, and (ii) the transistors can continue to scale. The term equivalent oxide thickness, t_{eq} , is used in the art in connection to high-k dielectrics, and is defined as the

equivalent physical thickness of “the SiO₂ layer that would be required to achieve the same capacitance density as the high-k material in consideration.” (TSMC-1032, 9.)

48. High-k dielectrics, like Hf-based oxides, tantalum oxide (Ta₂O₅), or zirconium oxide (ZrO₂), were considered as potential candidates to replace SiO₂ and to address the challenges faced by SiO₂. (TSMC-1034, 146.) Hafnium oxide (HfO₂), in particular, became the material of choice due to its optimal dielectric constant (not too high or too low), thermal stability, and scalability. (TSMC-1049, 134.)

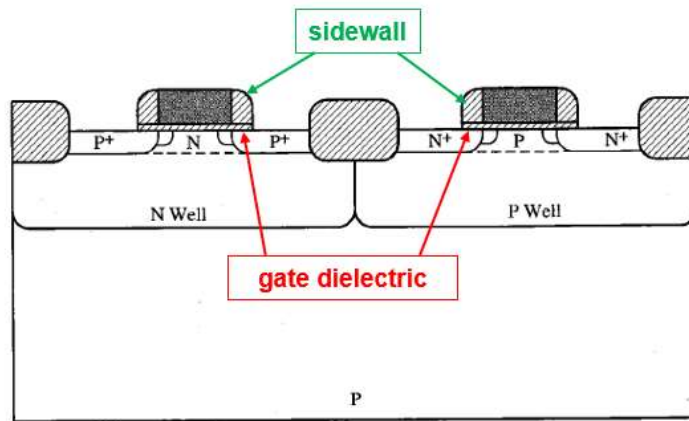
49. It was already known by 2005 that high-k materials substantially reduce the amount of leakage current compared to SiO₂ for the same equivalent oxide thickness and, thus, improve the semiconductor device’s energy efficiency and reliability. (TSMC-1018, 5250, Figure 5 (below); Wolf 146-47.)



Wilk, Figure 5

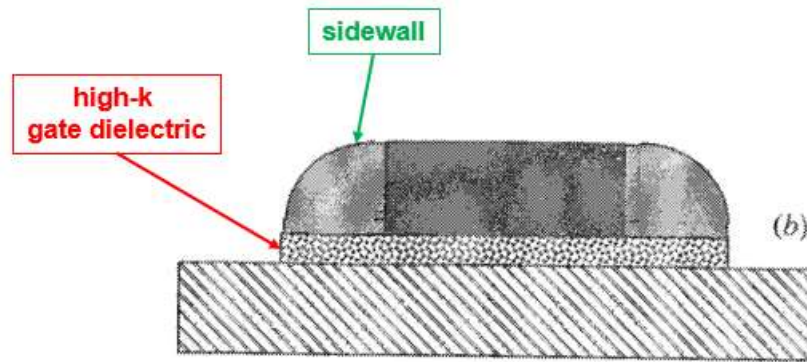
b. Extended Gate Insulating Films

50. Prior to 2005, it was common practice to extend the gate dielectric from under the gate electrode to under the gate sidewalls. For example, Plummer depicts a CMOS device having an extended gate dielectric in both the NMOS and PMOS transistors. (TSMC-1033, 82-83.)



Plummer, Figure 2-34

51. Houssa, which provides a MOSFET that uses a high-k material (e.g., HfO_2) as the gate dielectric material, explains that extending the gate dielectric under the sidewall spacers offers a process integration benefit—i.e., it relaxes the etch selectivity requirements between the high-k dielectric material and the silicon substrate. (TSMC-1032, 510; Figure 5.1.9(b).)

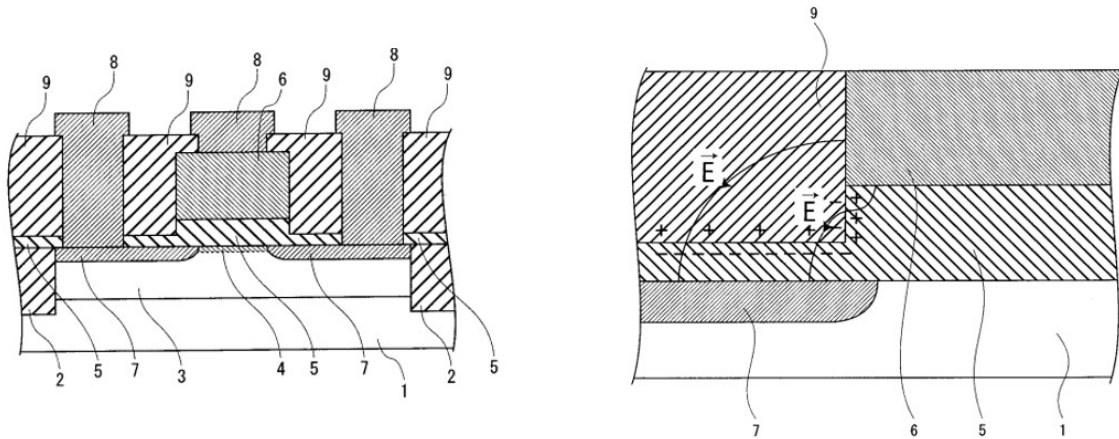


Houssa, Figure 5.1.9(b)

52. JP Publication 2005-064190 by Ono, et al. (“JP-Ono”¹; TSMC-1040), filed two years before the earliest priority date of the ’076 patent, provides a detailed discussion of motivations for extending a high-k gate dielectric beyond the gate edges. For example, JP-Ono explains that differing dielectric constants create a concentration of electric field lines at the gate edge. (TSMC-1040, ¶ 6.)

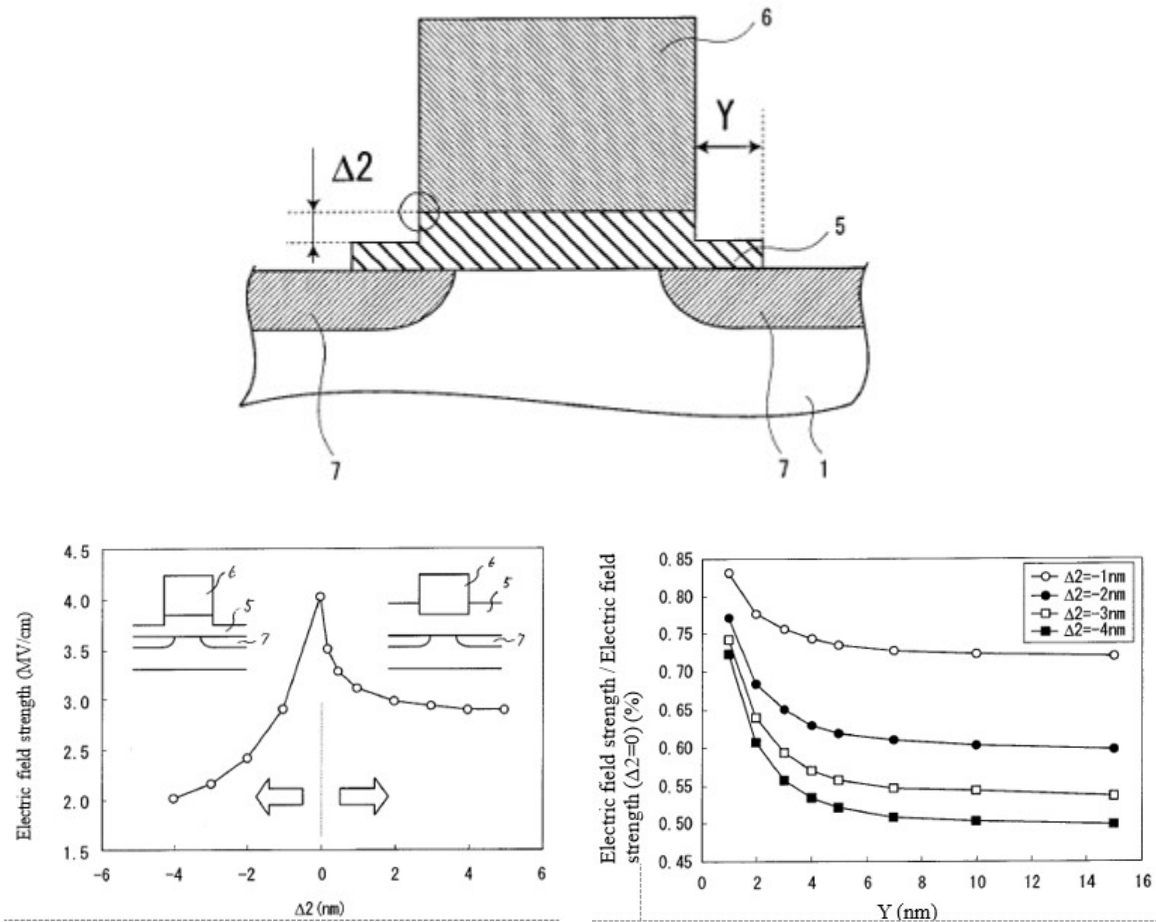
53. JP-Ono demonstrates that an extended gate dielectric mitigates field crowding at the gate electrode corners. (TSMC-1040, Abstract.) JP-Ono details how extending the gate dielectric to a thinner layer over the source/drain region minimizes the electric field, reinforcing the high-k dielectric’s performance under the sidewall structure. (TSMC-1040, ¶¶29-32, Figures 1-2 (below).)

¹ A certified translation of JP-Ono is included with TSMC-1040.



JP-Ono, Figures 1 (left), 2 (right)

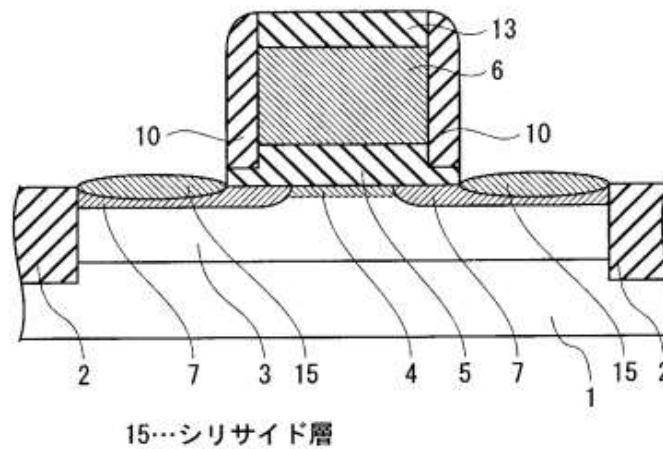
54. JP-Ono examines how adjusting both the thickness reduction of the gate dielectric outside the gate electrode ($\Delta 2$) and the extension length the gate dielectric from the lower gate electrode corners (Y) affects electric field distribution. Figure 4 (bottom-left) shows that when the thickness of the gate dielectric over the source/drain region matches its thickness under the gate, the electric field is at its highest intensity. (TSMC-1040, ¶34.) As the gate dielectric over the source/drain region becomes thinner, the electric field weakens, which favors a thinner dielectric in that area. (TSMC-1040, ¶35.) Figure 24 (bottom-right) further demonstrates that the electric field is reduced as the length of the gate dielectric extends farther from the lower gate electrode corner, i.e., as Y increases. (TSMC-1040, ¶87.)



JP-Ono, Figures 3 (top), 4 (bottom-left), 24 (bottom-right)

55. JP-Ono also describes the same improvements are achieved in a FET having a gate sidewall formed of silicon nitride or silicon oxide, such as that illustrated in Figure 23 below. (TSMC-1040, ¶83.)

【図 23】

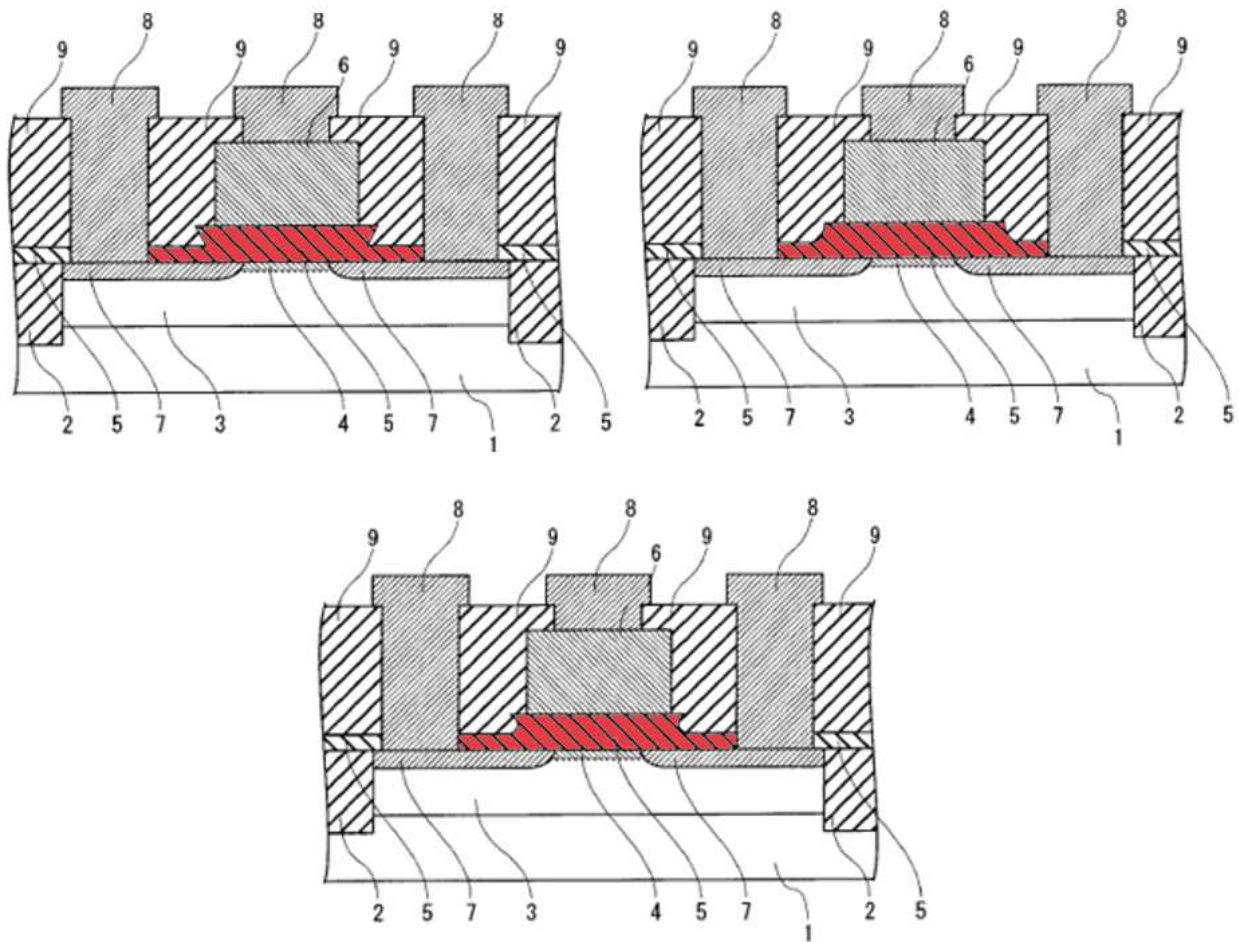


JP-Ono, Figure 23

c. Varying the Location and Shape of the End of Gate Insulating Film

56. JP-Ono also describes the benefits of varying both the location and shape of the gate dielectric ends relative to the sidewall edge to optimize device performance. For example, in reference to the embodiment shown in Figure 23 (above), JP-Ono states that “it is not essential for the side of the gate insulating film 5 to be located inside or outside of the outer surface of the gate-side wall 10.” (TSMC-1040, ¶84.) Instead, the side surface of the gate insulating film 5 can be positioned within the outer surface of gate sidewall 10. (TSMC-1040, ¶84.) Additionally, JP-Ono indicates that the gate dielectric may extend a certain distance beyond the sidewall, yielding similar performance. (TSMC-1040, ¶84.)

57. In Figures 36-44, JP-Ono illustrates various example shapes for the end of the gate insulating film (shaded red). (*See, e.g.*, TSMC-1040, Figures 38, 41-42 (below).) JP-Ono explains that modifying the end shape allows for “optimization” of parasitic resistance and parasitic capacitance. (TSMC-1040, ¶108.) Although these figures are depicted without sidewall 10, JP-Ono describes that sidewall 10 may be included in the device, placing the gate dielectric end shape beneath the sidewall. (*See* TSMC-1040, ¶103.)



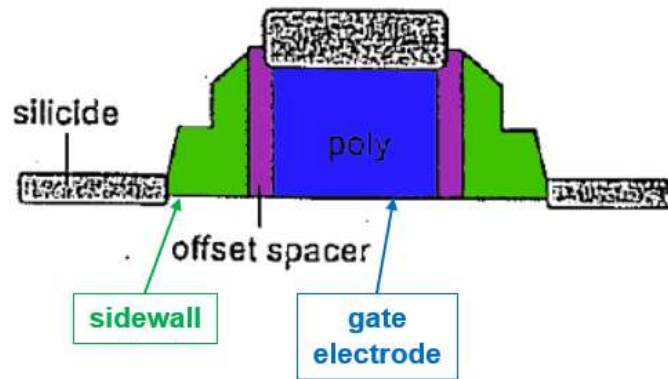
JP-Ono, Figures 38 (top-left), 41 (top-right), 42 (bottom)

3. Sidewalls/Spacers

58. Another common feature of the MISFET are the gate spacers or sidewalls, which are single layer or multilayer vertical insulating structures formed on or proximate to the side surfaces of a gate electrode. The terms “spacer,” “sidewall spacer,” and “sidewall” are sometimes used interchangeably in the art. Spacers/sidewalls (hereafter, spacers) serve a variety of purposes. For example, spacers are used to define the position of source/drain implants relative to the SDE implants, the gate electrode, and the channel region. (*See, e.g.*, TSMC-1032, 511; TSMC-1041, 122; TSMC-1034, 9, 217, 219.) Additionally, spacers can provide electrical isolation to the gate electrode by preventing shorts between silicided portions of the source/drain regions and the gate electrode. (Plummer, 742.) This is because, spacers are made of a dielectric material such as SiO_2 and/or silicon nitride (Si_3N_4). (TSMC-1032, 511.) Spacers may also help control the gate width along the gate length direction. (TSMC-1051, ¶¶13-14, Figs. 2c, 2d.)

59. As a non-limiting example, spacers may be used for “[c]ontrolling the position of the edge of the SDE [source/drain extension] region with respect to the gate edge” so as to achieve the optimal amount of overlap between the SDE and the gate edge. (TSMC-1034, 217.) As shown in Wolf’s Figure 5-25 below, “an offset-spacer is fabricated on the side of the gate after the gate-poly is etched (but before the SDE implant step is carried out ...),” with offset-spacer width “varied

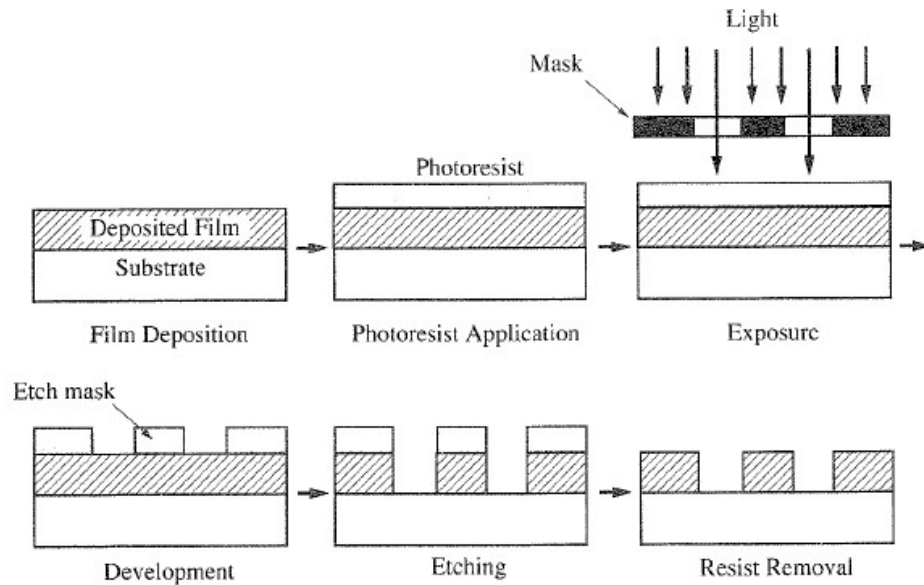
from zero (no-spacer) to some upper-bound (e.g., 50-nm)” to achieve optimum device characteristics. (TSMC-1034, 217.)



Wolf, Figure 5-25

4. Etching Properties

60. In semiconductor devices, thin films are often first deposited on the wafer surface and then selectively removed by etching to leave the desired pattern of the film. (Plummer, 609-11.) The desired pattern is often defined by placing an etch mask over areas of the substrate to be protected from the etch process (e.g., by depositing and patterning an etch mask layer), subjecting both masked and unmasked portions to the etching chemistry so that unmasked areas are etched, and removing the etch mask when the etch process is complete. (Plummer, 609-10, Figure 10-1 (below).) Gate electrodes and high-k gate insulating films are some examples of MISFET features formed by one or more combinations of deposition and etching processes.



Plummer, Figure 10-1

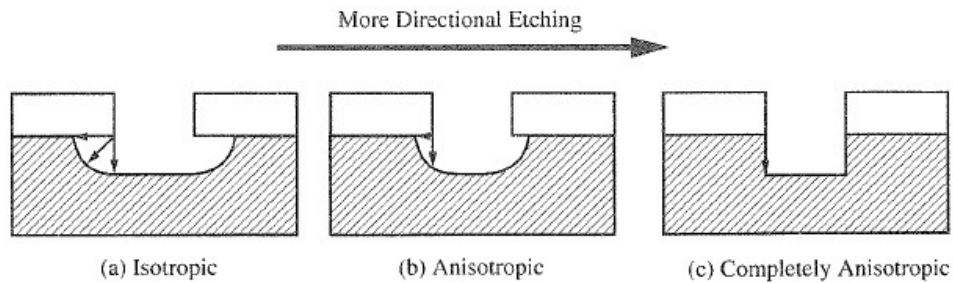
61. Etching can be performed in a “wet” or “dry” environment. (Plummer, 609, 612-37.) More specifically, wet etching uses liquid etchants (e.g., hydrofluoric acid, HF), whereas dry etching uses gas-phase etchants in a plasma. (Plummer, 609, 612.) In wet etching, the wafers are immersed in an etching bath filled with an etchant solution and the exposed materials are etched mostly by a chemical process. (Plummer, 609.) In dry etching, the wafers are exposed to the etching plasma where the materials are etched by a combination of chemical and physical processes. (Plummer, 609.)

62. Depending on the etching chemistry used, the etch process parameters, and the etching selectivity between the materials being etched and those not etched, etching processes can develop different relative etch rates in

different directions. (Plummer, 609-11.) For example, the more physical an etch process is (e.g., ion bombardment or sputtering), the more directional and less selective tends to be. (Plummer, 611.) “On the other hand, the more chemical an etch process is, the more selective and the less directional it generally is.”

(Plummer, 611.) Directionality is often desirable because it “maintains lithographically defined feature sizes as they are transferred by etching into underlying films.” (Plummer, 611.)

63. Isotropic etching is direction independent (i.e., the etch rate is similar in all directions) and can result in a semicircular etch profile as shown in Figure 10-3(a) below. Most wet chemical etchants etch isotropically. (Plummer, 610-13.) On the other hand, anisotropic etching is more direction dependent and results in little or no etching in the lateral direction. (Plummer, 611, Figure 10-3(b), (c) (below).) For example, anisotropic etching can have substantially higher etch rate in the vertical direction than in the lateral direction. However, for anisotropic etching, the amount of lateral etching may vary, such that the etched surface may be curved or sloped (Plummer, Figure 10-3(b)) to completely vertical (Plummer, Figure 10-3(c)).

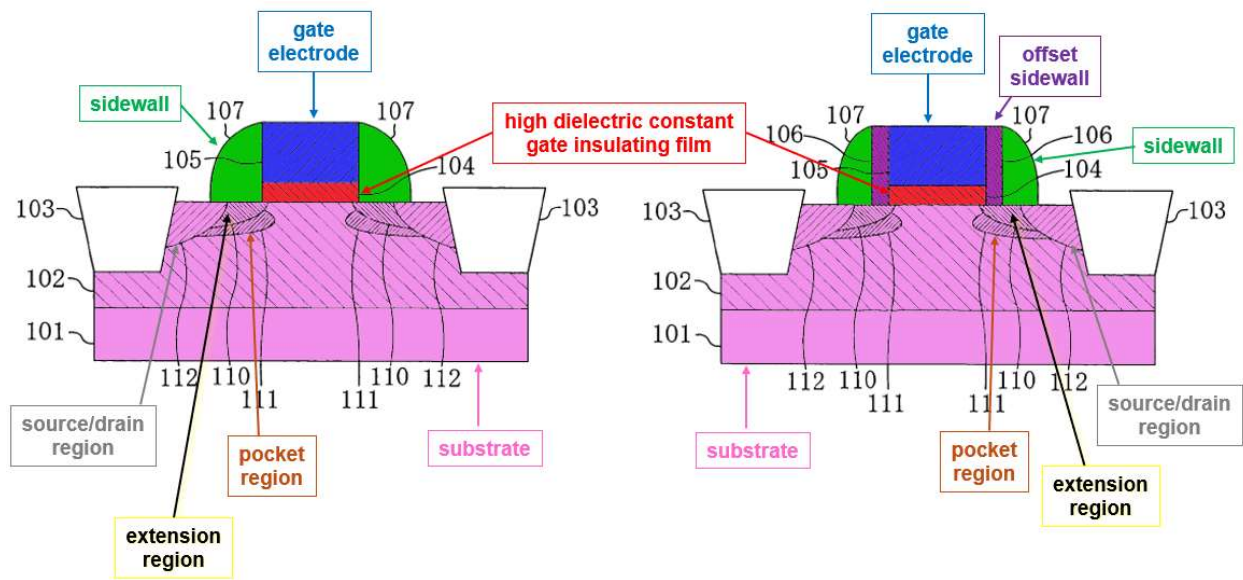


Plummer, Figure 10-3

B. Applicant Admitted Prior Art (“AAPA”)

64. As discussed above, semiconductor devices, such as MISFETs, existed for decades prior to the filing of the '076 patent. The '076 patent does not purport to invent the limitations of most of its claims, including, for example, high dielectric constant gate insulating film formed on a substrate, a gate electrode formed on the gate insulating film, or the use of insulating sidewalls. Rather, the '076 patent claims are directed to specific arrangements of gate insulating films and insulating sidewalls (which, as I will explain later in relation to the prior art grounds, were also well known).

65. For example, the '076 patent recognized that semiconductor devices using “a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like” as a gate insulating film already existed prior to its filing in 2005. (TSMC-1001, 1:26-34.) The '076 patent illustrates and describes two exemplary prior art devices in relation to Figures 16A and 16B.



'076 Patent, Fig. 16A (annotated left), '076 Patent, Fig. 16B (annotated right)

66. As shown above in Figures 16A and 16B, prior art devices included gate electrode 105 (shaded blue) “on a region of a well 102” surrounded by a shallow trench isolation (STI) 103 which served “as an active region” of substrate 101 (shaded pink). (TSMC-1001, 1:40-43.) A high dielectric constant (referred to herein as “high-k”) gate insulating film 104 (shaded red) lies between gate electrode 105 and the active region. (TSMC-1001, 1:43-45.) Each of these devices had insulating sidewalls (107 in Figure 16A; 106 and 107 in Figure 16B) formed on each side surface of the gate electrode.

C. '076 Patent Overview

67. According to the '076 patent, in prior art devices such as those shown in Figures 16A and 16B, the “side end portions” of the high-k film “are in direct contact with sidewalls,” which caused the reliability of the gate insulating film to

degrade. (TSMC-1001, 1:63-2:8.) The '076 patent purports to solve this problem by extending the high-k film at least partially under the insulating sidewalls.

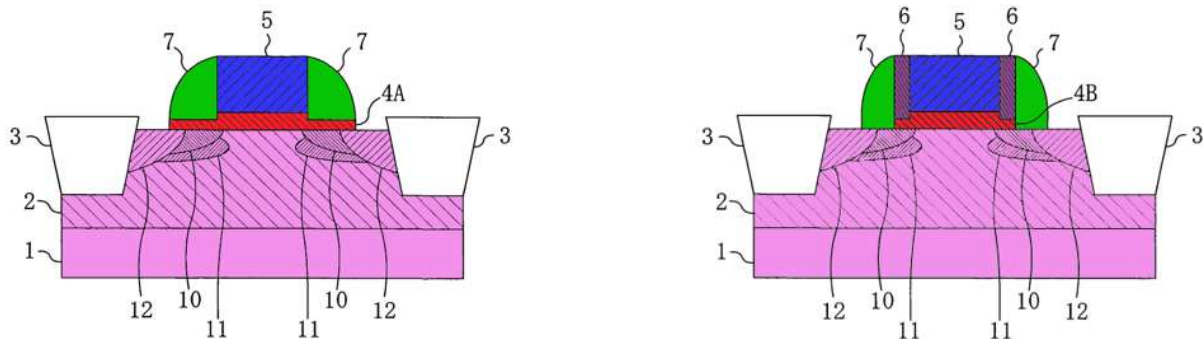
68. The '076 patent discloses several exemplary embodiments wherein the high-k gate insulating film extends at least partially under the insulating sidewall. This includes devices with a single sidewall (such as the first and fourth embodiments) and devices with double sidewalls (such as the second and third embodiments), as well as minor modifications thereof. The '076 patent's claims are specifically directed to devices wherein the gate insulating film extends under at least a portion of the insulating sidewall and an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

69. For example, independent claim 1 recites:

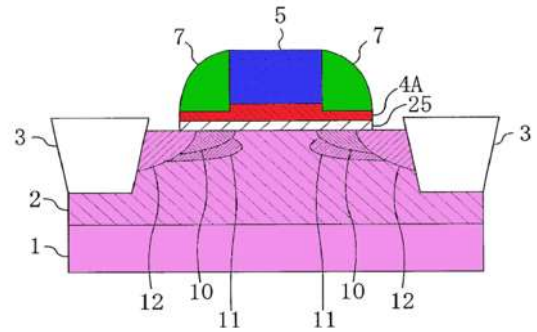
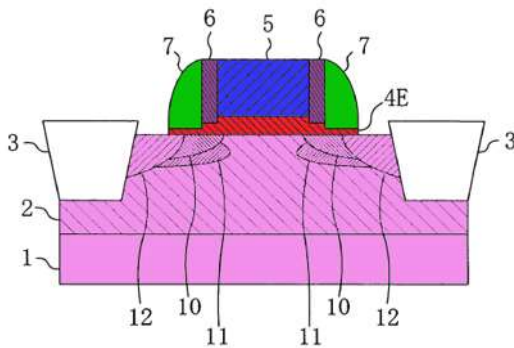
[1P]	1. A semiconductor device comprising:
[1A]	a gate insulating film formed on an active region in a substrate and including Hf;
[1B]	a gate electrode formed on the gate insulating film;
[1C]	a insulating sidewall formed on each side surface of the gate electrode; and

[1D]	wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length,
[1E]	an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

70. The '076 patent presents four semiconductor device embodiments (first-fourth embodiments) and their associated fabrication methods (fifth-eighth embodiments). In each embodiment, the high-k gate insulating film (shaded red) extends beyond the gate electrode to under the sidewall(s). (*See* TSMC-1001, Figures 1-2, 5, 9 (below).)



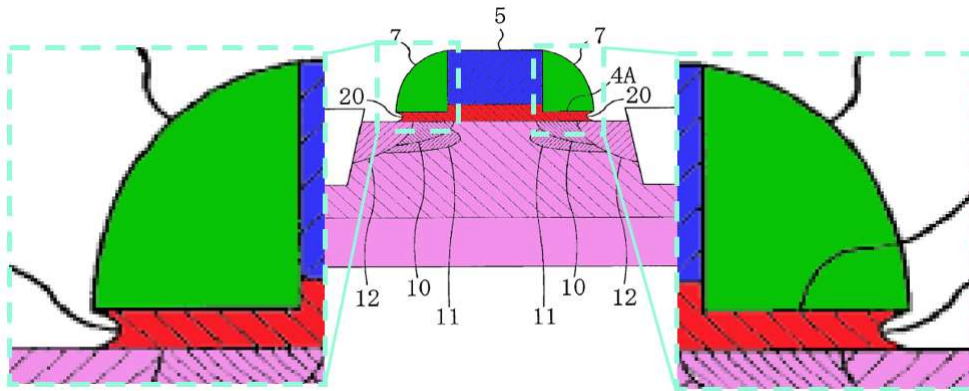
'076 Patent, Fig. 1 (First Embodiment, left) and Fig. 2 (Second Embodiment, right) (annotated)



'076 Patent, Fig. 5 (Third Embodiment, left) and Fig. 9 (Fourth Embodiment, right) (annotated)

71. As can be seen in the figures above, the embodiments differ in the number of sidewalls (one versus two) and the presence of a buffer layer under the gate insulating film (fourth embodiment). The embodiments also vary in the relative thickness of the gate insulating film under the gate electrode and sidewalls, though this difference is not relevant to most of the '076 patent's claims.

72. Each of the embodiments includes a modification in which “a side portion of the high dielectric constant gate insulating film ... is removed in a notch shape, so that a notch 20 is provided.” (TSMC-1001, 7:10-15, 14:49-56, Figure 6, 8:41-46, 16:14-21, Figure 7, 11:53-58, 18:22-28, Figure 8, 13:8-21, Figure 10.) An exemplary “notch,” applied to the first embodiment, is illustrated in Figure 6 below.



'076 Patent, Fig. 6 (annotated and enlarged)

73. The concept of changing the shape and/or location of the end of a dielectric was known, long before the '076 patent.

D. Prosecution History

1. U.S. Prosecution of the '076 Patent

74. The filed claims of the '076 patent application were rejected based on nonstatutory obviousness-type double patenting over claims 1-22 of the '180 patent (TSMC-1002, 133-34.) The Examiner also rejected the claims as unpatentable over U.S. Patent 6,992,358 to Hieda ("Hieda"). (TSMC-1002, 129-33.) Thereafter, the Applicant amended the final limitation of prosecution claim 21 (issued claim 1) as follows: "an end of the gate insulating film under the insulating sidewall is ~~located to retract~~ retracted from an outer end of the insulating sidewall toward the gate electrode." (TSMC-1002, 155.) According to the Applicant, the amendment was made "to clarify the intended subject matter." (TSMC-1002, 157.)

In response to the Examiner's rejections, the Applicant submitted a terminal disclaimer and traversed the Hieda rejection. (TSMC-1002, 157-59.) The Examiner allowed the claims. (TSMC-1002, 173-74.)

2. U.S. Prosecution of the '180 Patent

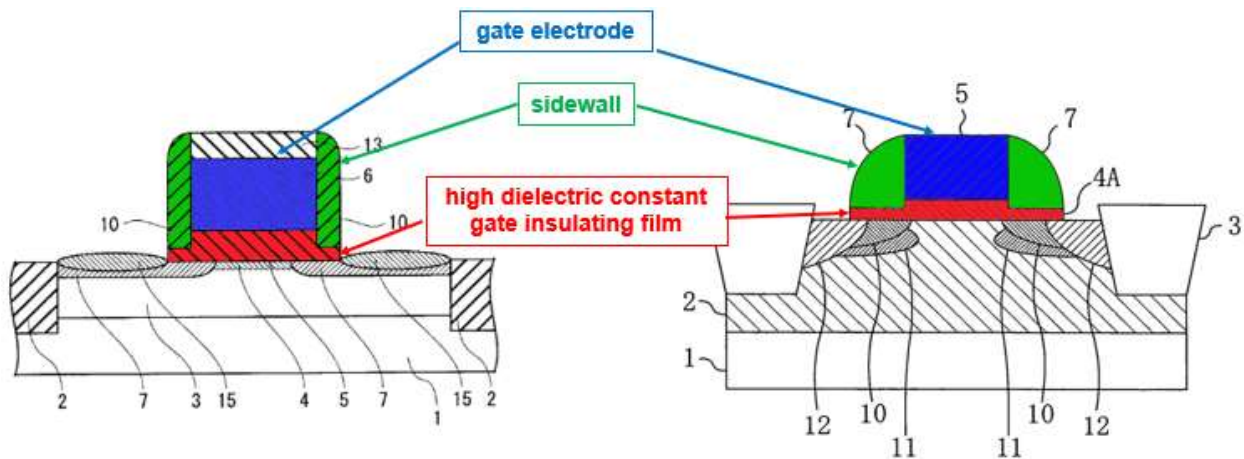
75. I also reviewed the U.S. prosecution history of the '180 patent used as the basis for the nonstatutory obviousness-type double patenting rejection. The claims of the '180 patent application, as in the '076 prosecution, were rejected as unpatentable over Hieda. (TSMC-1008, 123-27.) Applicant argued that Hieda did not disclose the "predetermined distance" limitation because "the high dielectric constant insulating [film] recited by claim 21 [issued claim 1] does not extend so far such that it is disposed beneath the outer end of the insulating sidewall It is disposed inwardly of the outer end of the insulating sidewall." (TSMC-1008, 151-52.) The Examiner allowed the claims based on the above.

3. Japanese Prosecution

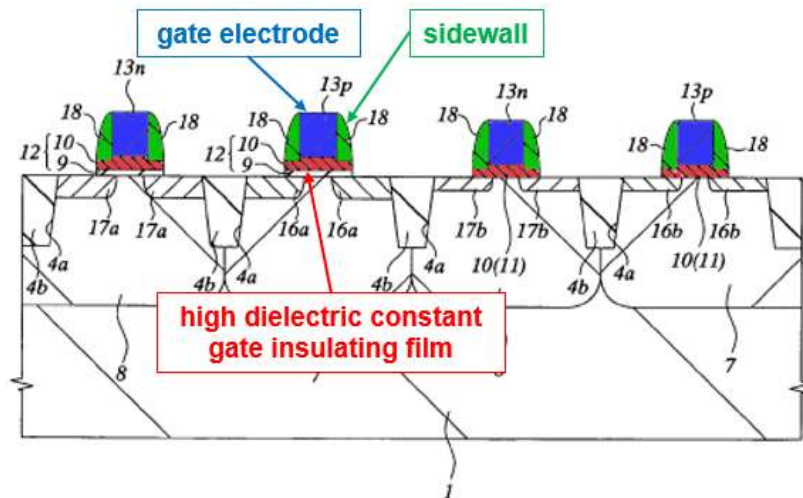
76. I have also reviewed a translated version of the prosecution history for the Japanese application that the '227, '764, '180, and '076 patents claim priority to.

77. The Japanese priority application was filed with the same single-sidewall device claim originally filed with the U.S. application. (TSMC-1005, 16.) On September 16, 2011 (before the '076 patent issued on November 19, 2013 in

the United States), the Japanese Examiner found this claim scope unpatentable, citing JP2005-064190 to Ono (“JP-Ono”) and WO2004/017418 to Sakai, et al. (“Sakai”). (TSMC-1005, 4-6.) As shown in Figure 23 of Ono and Figure 25 of Sakai, these references both teach a high-k gate insulating film that extends past the gate electrode under the insulating sidewall, and has a smaller thickness under the sidewall than under the gate electrode, like e.g., the ’076 patent’s single sidewall embodiments. (TSMC-1001, Figure 1.)



JP-Ono, Fig. 23 (annotated left); '076 Patent, Fig. 1 (annotated right)



Sakai, Figure 25 (annotated)

78. The JP-Examiner also determined JP-Ono taught the “notch” limitation of certain claims by disclosing:

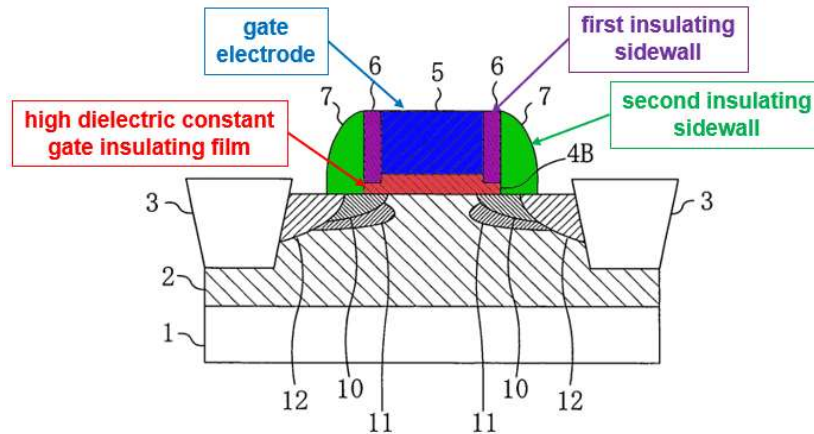
[I]n this embodiment, the side of the gate insulating film 5 is aligned with the outer surface of the gate-side wall 10. However, it is not essential for the side of the gate insulating film 5 to be located inside or

outside of the outer surface of the gate-side wall 10; similar effects can be achieved even if it is positioned differently.

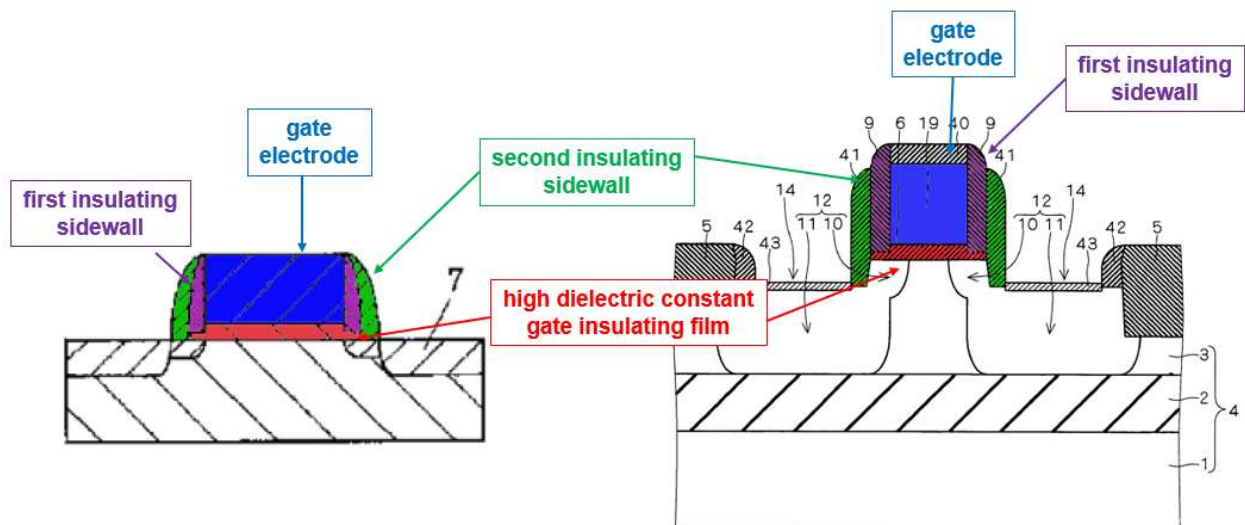
(TSMC-1040, ¶84; TSMC-1005, 5.) This disclosure from JP-Ono is also relevant to the '076 patent because it also discloses an example in which the end of the gate insulating film is retracted from the outer end of the sidewall.

79. In response, Applicant narrowed the Japanese claim to recite (1) a *double* sidewall structure with a high-k film having a smaller thickness under a first sidewall than under the gate electrode and (2) extension and source/drain regions. (TSMC-1005, 8.) The Japanese Examiner then rejected the amended claim based on both JP 2003-258241 to Kajiyama (JP-Kajiyama (TSMC-1010) and JP 2004-241755 to Matsumoto (“JP-Matsumoto”). (TSMC-1005, 14-16.) The JP-Examiner also maintained the rejection of the notch claim based on the teachings of JP-Ono. (TSMC-1005, 15.)

80. As shown in Figure 1(D) of JP-Kajiyama and Figure 33 of JP-Matsumoto, both of these references teach the same basic structure as the '076 patent's Figure 2. (TSMC-1005, 14-16; *compare* TSMC-1001, Figure 2.)



'076 Patent, Figure 2 (annotated)



JP-Kajiyama, Fig. 1(D) (annotated left);
JP-Matsumoto, Fig. 33 (annotated right)

81. In response to that rejection, Applicant further narrowed the claim to recite that the thickness of the high-k gate insulating film under the second sidewall is smaller than the thickness under the first sidewall which is smaller than the thickness under the gate electrode, an arrangement that corresponds to the '076

patent's third embodiment. (TSMC-1005, 18.) The JP Examiner allowed the claim based on this amendment. (TSMC-1005, 20.)

82. Based on this prosecution history, the applicant acquiesced during the Japanese prosecution that devices corresponding to the '076 patent's issued claim 1 were known in the art before the '076 patent. Despite the materiality of the JP notices of refusal, Applicant did not inform the U.S. Examiner of these refusals.

V. GROUND 1: Kamata Renders Claims 1-3, 5-13 Obvious.

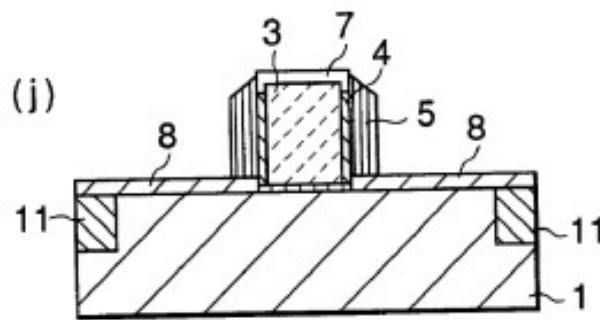
A. Overview

83. U.S. Publication 2002/0063299, titled "Semiconductor Device and Manufacturing Method," to Kamata, et al. ("Kamata"; TSMC-1027), was filed on November 28, 2001, and published May 30, 2002. Kamata discloses multiple embodiments of a semiconductor device—e.g., a MIS type transistor with a plurality of side wall films. (*See* TSMC-1027, Abstract, ¶¶3, 5, 16.) For example, Kamata discloses that manufacturing its device comprises the steps of: "forming a gate insulating film on a silicon substrate; forming a gate electrode on the gate insulating film; forming a first insulating film to cover the gate insulating film and the gate electrode; [and] forming a second insulating film on the first insulating film" (TSMC-1027, ¶¶22-30.) "The gate insulating film may be . . . a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, Hf,

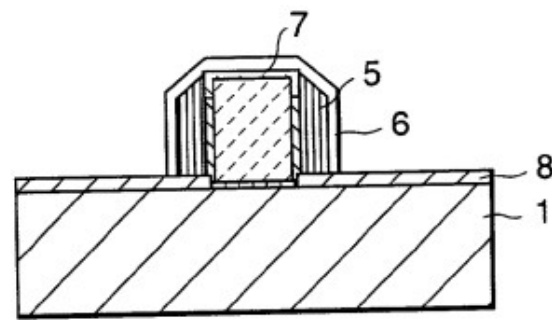
Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element.”

(TSMC-1027, ¶52.)

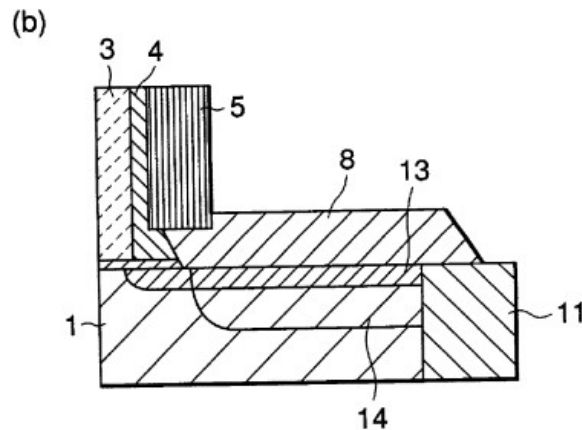
84. I have been asked to focus my analysis on the first (Figure 1B(j)), fourth (Figure 5(c)), and ninth (Figure 10(b)) embodiments, shown below, though other embodiments may invalidate the challenged claims too.



**Kamata, Figure 1B(j)
(First Embodiment)**



**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

85. As shown in the figures above, each of the illustrated embodiments includes a substrate 1, a high dielectric gate insulating film on the substrate, a gate

electrode 3 on the gate insulating film, and a sidewall structure having a first sidewall film 4 and a second sidewall film 5. (TSMC-1027, ¶¶50-61 (first embodiment), 68 (fourth embodiment), 93-94 (ninth embodiment).) In each of the above embodiments, the gate insulating film extends from under the gate electrode to under only a portion of the sidewall structure (namely, under sidewall 4 for the first and fourth embodiments, and under sidewall 4 and only a portion of sidewall 5 for the ninth embodiment). (See also TSMC-1027, ¶25 (“forming a first insulating film to cover the gate insulating film and the gate electrode”).

86. As discussed in detail below, a POSITA in 2005, working within the field of semiconductor devices, would have understood Kamata’s teachings as addressing the challenges of device scaling, particularly in managing leakage current and maintaining capacitance with shrinking gate dimensions. Kamata’s use of high-k materials and multilayer sidewall structures would have been recognized as predictable solutions to these scaling challenges, aligning with industry practices at the time. Furthermore, a POSITA would have been motivated to apply Kamata’s techniques due to their well-documented ability to enhance device performance and reliability in ultra-large-scale integration (ULSI) technologies.

B. Independent Claim 1

1. Preamble [1P]

[1P] *A semiconductor device comprising:*

87. Kamata's first, fourth, and ninth embodiments are each a "*semiconductor device*."² For example, Kamata is entitled "Semiconductor Device and Manufacturing Method" and states that "[t]his invention relates to a **semiconductor device**."³ (TSMC-1027, ¶¶3, 8; *see also* TSMC-1027, ¶¶32, 50 (first embodiment), 35, 68 (fourth embodiment), 93-94 (ninth embodiment).)

2. Limitation [1A]

[1A] *a gate insulating film formed on an active region in a substrate and including Hf;*

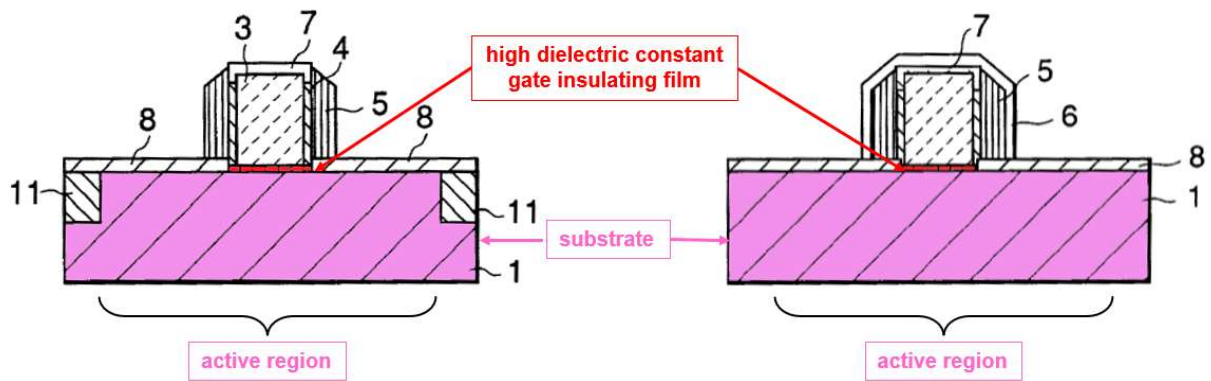
88. Kamata's first, fourth, and ninth embodiments each includes "*a gate insulating film formed on an active region in a substrate and including Hf*" [1A]. For example, Kamata discloses that each embodiment of its semiconductor device has "a semiconductor **substrate** 1 made of silicon" (*see, e.g.*, TSMC-1027, ¶50) and is manufactured by "forming a gate insulating film on a silicon **substrate**." (TSMC-1027, ¶23) (*see also* TSMC-1027, ¶¶68 ("parts [of the fourth embodiment]

² Claim language is indicated by italics throughout.

³ Unless otherwise noted, all emphasis added.

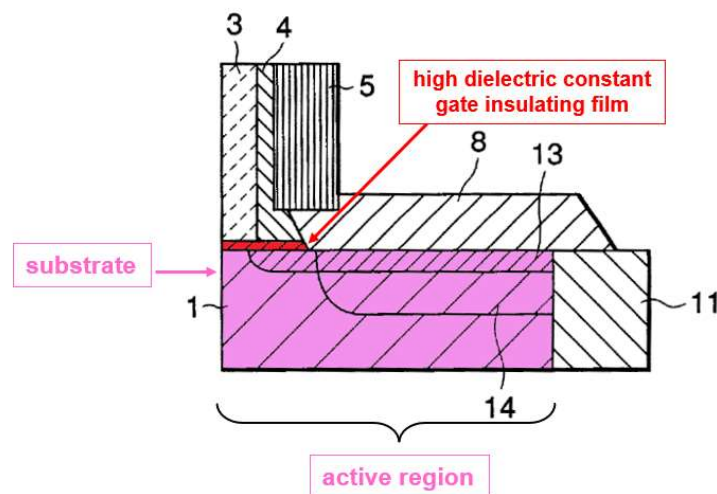
that are same as or similar to those of the first embodiment are denoted respectively by the same reference symbols”), 94 (“portions [of the ninth embodiment] that are same as or similar to those FIGS. 1A through 2C are denoted respectively by the same reference symbols”).)

89. Kamata also discloses that “shallow trench isolation zones (STI) 11 are formed on a semiconductor substrate 1 made of silicon to define an element region 1a (FIG. 1A(a)).” (TSMC-1027, ¶50; *see also* TSMC-1027, ¶¶68, 94.) A POSITA would have understood element region 1a, identified by shallow trench isolation, to be an “*active region in a substrate*,” and in fact, Kamata refers to it as such. (TSMC-1027, ¶¶99-100 (referring to “**active region 1a**” and indicating that the same or similar parts in Figures 1A through 2C are “denoted respectively by the same reference symbols”).) This is also consistent with the disclosures of the '076 patent. (*See* TSMC-1001, 1:41-43 (“region of the well 102 surrounded by the STI serves as an active region of a substrate 101”).) Kamata’s active region in a substrate is shaded pink in the annotated figures below.



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

90. Also as shown above, each embodiment of Kamata's device includes film 2 (shaded red) formed on the active region under the gate electrode extending beneath the sidewall structure. (*See, e.g., TSMC-1027, ¶¶23, 56, 68, 94*). Kamata discloses that the gate insulating film may be a high dielectric constant film:

explaining that “[t]he gate insulating film may be . . . a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, containing at least an element selected from a group of Ti, Zr, **Hf**, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element.” (TSMC-1027, ¶52). Kamata further teaches that “[t]he film may be a single crystal film, a poly crystal film or an amorphous film such as TiO₂, Ti₂O₅, BST, Si₃N₄, Al₂O₃, Y₂O₃, La₂O₃, **HfO₂**, ZrO₂, Pr₂O₃, SrTiO₃ and Gd₂O₃. Furthermore, the film may be made of a mixture of SiO₂, TiO₂, Ti₂O₅, BST, Si₃N₄, Al₂O₃, Y₂O₃, La₂O₃, **HfO₂**, ZrO₂, Pr₂O₃, SrTiO₃ or Gd₂O₃, with Ti, Zr, **Hf**, Ta, La, Al Ba, Sr, Y, Pr or Gd.” (TSMC-1027, ¶53.)

91. A POSITA would have been motivated to use a high-k material for the gate insulating film, such as those disclosed by Kamata or otherwise known in the art, to address the well-documented issues with silicon dioxide gate dielectrics in ultra-large-scale integration devices having scaled down features. (*See* TSMC-1032, 3-12; TSMC-1034, 4-5, 146-47.) Further, a POSITA would have been motivated to select HfO₂ given its known benefits, e.g., “its superior thermal stability with poly-Si and reasonable band alignment.” (TSMC-1037, 2.4.1; *see also* TSMC-1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 134 (“Excellent dielectric properties ... suggest that HfO₂ is a

promising material for the future gate dielectric application.”.) HfO₂ also could be scaled down to a smaller EOT. (See TSMC-1032, 207.)

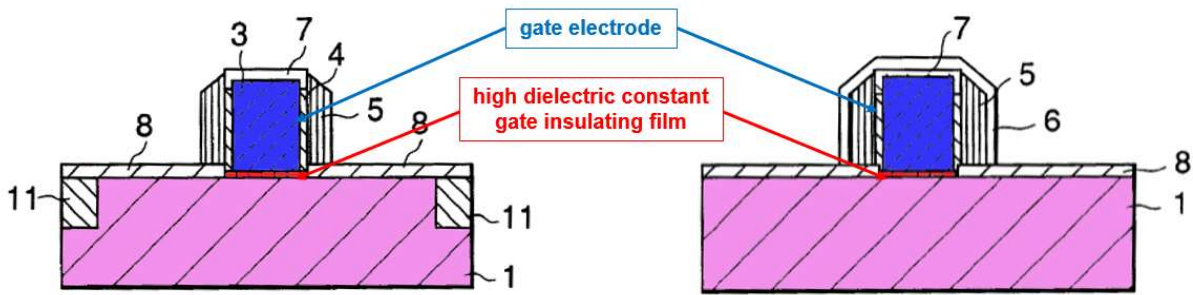
92. Thus, Kamata teaches a “*gate insulating film* [film 2] ... *including Hf.*” (See, e.g., TSMC-1027, ¶73 (referring to “gate insulating film 2”), ¶¶8-10 (teaching “present invention” device includes “a gate insulating film formed on a surface of the silicon substrate”), claim 1.)

3. Limitation [1B]

[1B] <i>a gate electrode formed on the gate insulating film;</i>
--

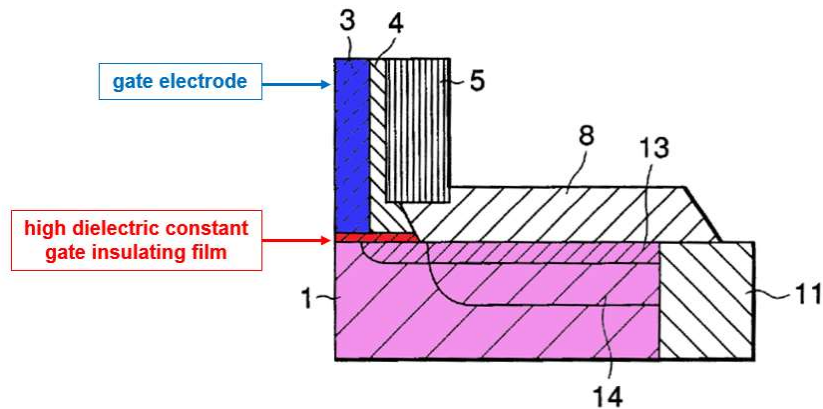
93. Kamata’s first, fourth, and ninth embodiments each teaches “*a gate electrode formed on the gate insulating film*” [1B]. For example, Kamata discloses that its manufacturing process includes “forming a gate electrode on the gate insulating film.” (TSMC-1027, ¶24; see also, e.g., TSMC-1027, ¶¶8-11, claim 1 (reciting device with “gate electrode formed on the gate insulating film”).)

94. As shown in the annotated figures below, the semiconductor device of each embodiment has a gate electrode 3 (shaded blue) formed on gate insulating film 2 (the “*gate insulating film*,” shaded red). (TSMC-1027, ¶50 (“Then, a gate electrode 3 is formed by depositing polycrystalline silicon (FIG. 1A(b)) and, after a lithography step, the gate electrode is processed by means of an anisotropic etching technique using plasma such as RIE (reactive ion etching (FIG. 1A(c)).”); see also Kamata ¶¶68, 94, Figures 1A(a)-(c).)



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

4. Limitation [1C]

[1C] *a insulating sidewall formed on each side surface of the gate electrode;
and*

95. Kamata's first, fourth, and ninth embodiments each teaches "*a insulating sidewall formed on each side surface of the gate electrode*" [1C].

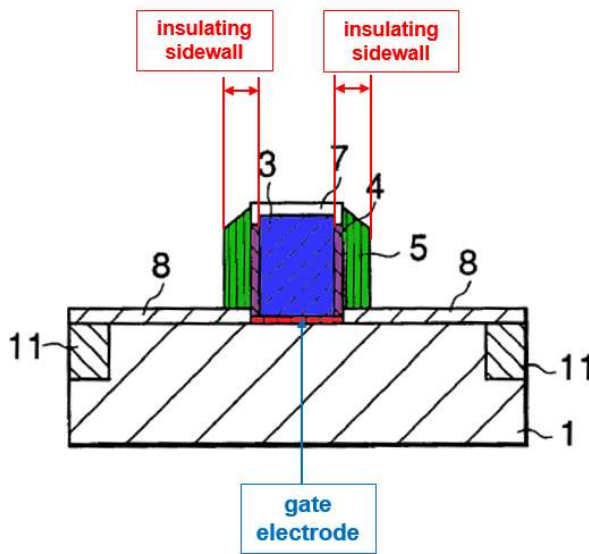
96. For example, Kamata discloses "forming a first insulating film to cover the gate insulating film and the gate electrode; forming a second insulating

film on the first insulating film [and] selectively leaving the second insulating film on a side surface of the gate electrode with the first insulating film interposed therebetween. . .” (TSMC-1027, ¶¶25-27; *see also* claim 1). Kamata refers to these insulating films as “sidewall films” 4 and 5. (*See* TSMC-1027, ¶¶57 (referring to film 5 as “sidewall film 5”), 74 (referring to film 4 as “sidewall film 4”).) In particular, film 4 is a silicon oxide film (*see, e.g.*, TSMC-1027, ¶58 (referring to “silicon oxide film 4”), and film 5 is a silicon nitride film. (*See* TSMC-1027, ¶50 (referring to “silicon nitride film (Si₃N₄) 5”).) A POSITA would have understood that silicon oxide and silicon nitride are insulators. (TSMC-1034, 9, 75; Plummer, 79-80.)

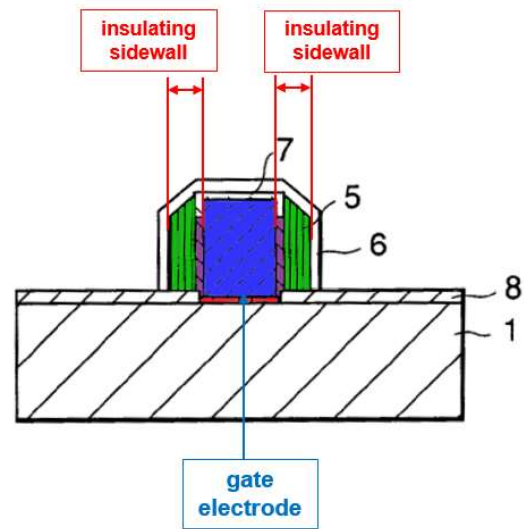
97. Sidewall 4 and sidewall 5 are collectively an “*insulating sidewall*,” consistent with the disclosure of the ’076 patent.⁴

98. Figures 1B(j) and 5(c), annotated below, show that Kamata’s first and fourth embodiment devices each includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green), which together are an insulating sidewall formed on the gate electrode’s side surfaces (shaded blue).

⁴ The ’076 patent uses the term “insulating sidewall” broadly to refer to a single component (6:9), a collective structure of two components (2:60-65), and as a component having multiple layers (21:6-15).



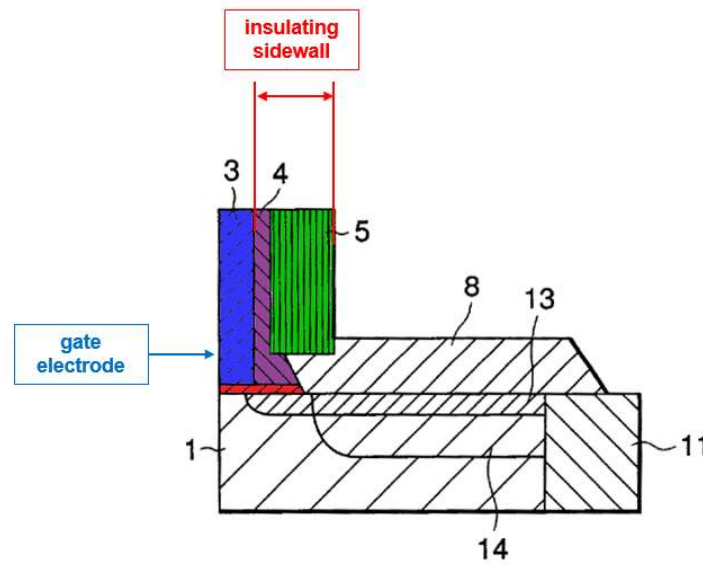
Kamata, Figure 1B(j) (First Embodiment)



Kamata, Figure 5(c)
(Fourth Embodiment)

99. Figure 10(b), annotated below, shows how Kamata's ninth embodiment device also includes sidewall film 4 (shaded purple) and sidewall film 5 (shaded green), which, like the first and fourth embodiments, together are an insulating sidewall formed on the gate electrode's side surfaces (shaded blue). (*See* TSMC-1027, ¶¶8-16, 57, 74; *see also* TSMC-1027, ¶¶50, 58, 94.⁵)

⁵ Although Figure 10(b) shows the right side of the semiconductor device of Kamata's ninth embodiment, a POSITA would have understood that the device includes a corresponding insulating sidewall on the left side surface of the gate electrode too.



**Kamata, Figure 10(b)
(Ninth Embodiment)**

5. Limitation [1D]

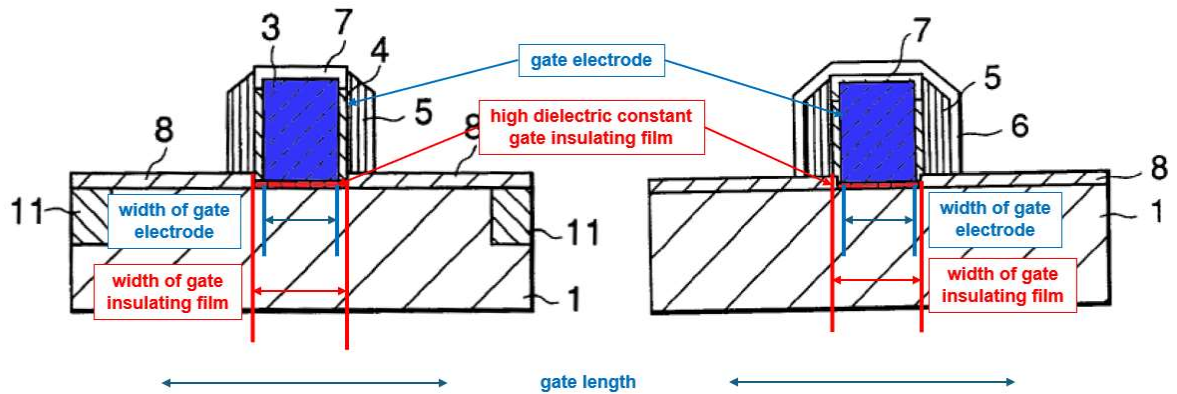
[1D] wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and

100. The devices of Kamata's first, fourth, and ninth embodiments each teaches "a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length" [1D].

101. **First and Fourth Embodiments.** In the first and fourth embodiment devices (Figures 1B(j) and 5(c)), the width along the gate length⁶ of high-k gate

⁶ The '076 patent uses the term "along the gate length" to refer to a direction, specifically from the source to the drain regions.

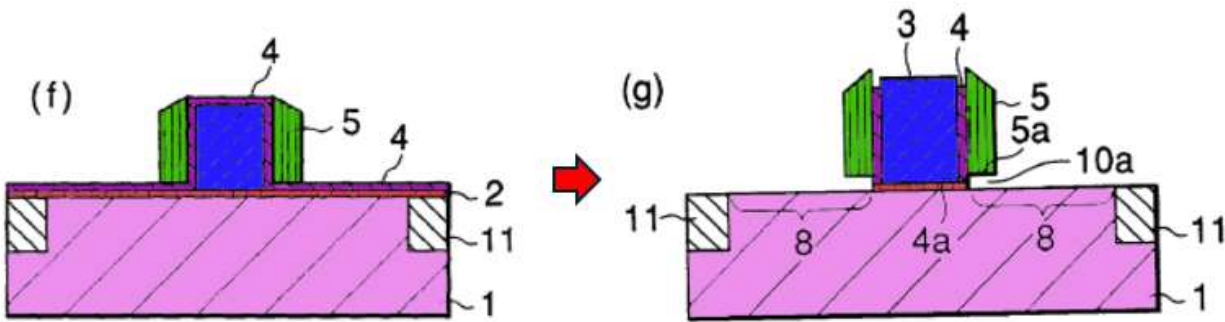
insulating film 2 (shaded red), including at its bottom surface, is larger than the width along the gate length of gate electrode 3 (shaded blue).



**Kamata, Fig. 1B(j)
(First Embodiment)**

**Kamata, Fig. 5(c)
(Fourth Embodiment)**

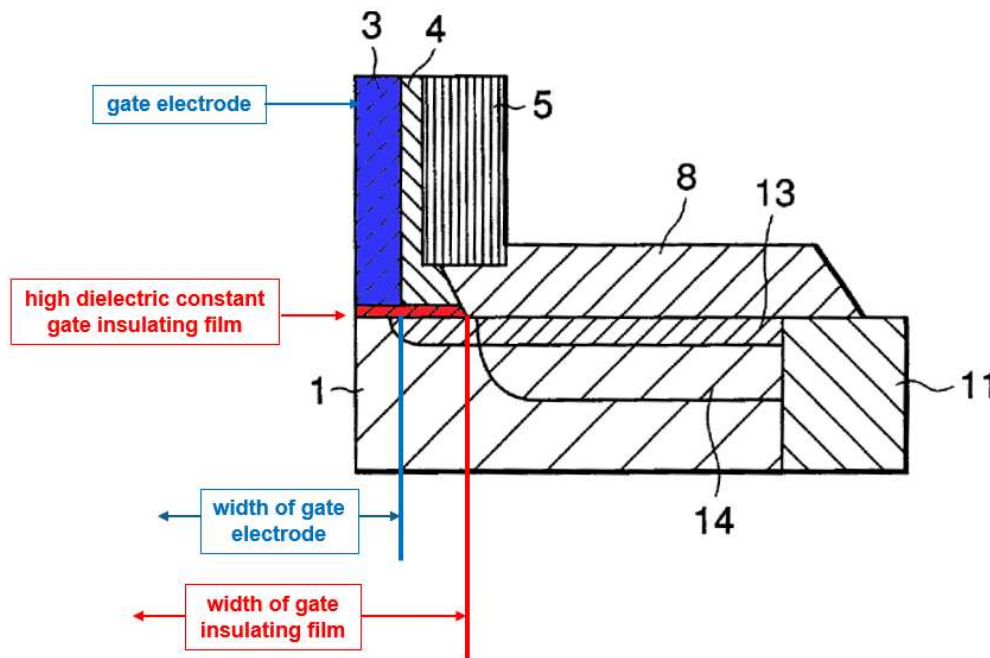
102. Kamata's manufacturing process confirms the layout of the devices depicted in Figures 1B(j) and 5(c). Specifically, gate electrode 3 and sidewall 5 are first formed on silicon oxide film 2 (sidewall 5 is also formed on silicon oxide film 4), at which point silicon oxide films 2 and 4 are etched together, resulting in gate insulating film 2 extending from beneath the gate electrode 3 to underneath sidewall 4, as shown in Figures 1A(f) and 1B(g) below. (See TSMC-1027, ¶¶50, 56 (describing formation of gate electrode 3 and sidewalls 4 and 5), 68 (fourth embodiment).)



Kamata, Fig. 1A(f) (annotated left), Fig. 1B(g) (annotated right)

103. Accordingly, Kamata's in the devices of the first and fourth embodiments "*a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length*" [1D].

104. **Ninth Embodiment.** As can be seen in Figure 10(b) below for the ninth embodiment, the high-k film 2 (shaded red) extends beyond (i.e., protrudes from) under the gate electrode 3 to under sidewall films 4 and 5. (See TSMC-1027, ¶50 (describing formation of gate electrode 3), 94 (ninth embodiment).) Although, Figure 10(b) only shows a right portion of the device of Kamata's ninth embodiment, a POSITA would have understood that the left portion has similar structure, such that the width along the gate length of high-k film 2 (shaded red), including at its bottom surface, is larger than the width along the gate length of the gate electrode (shaded blue), including at its bottom surface.



**Kamata, Fig. 10(b)
(Ninth Embodiment)**

105. Accordingly, in the device of the ninth embodiment, similar to the devices in the first and fourth embodiments, “a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length” [1D].

6. Limitation [1E]

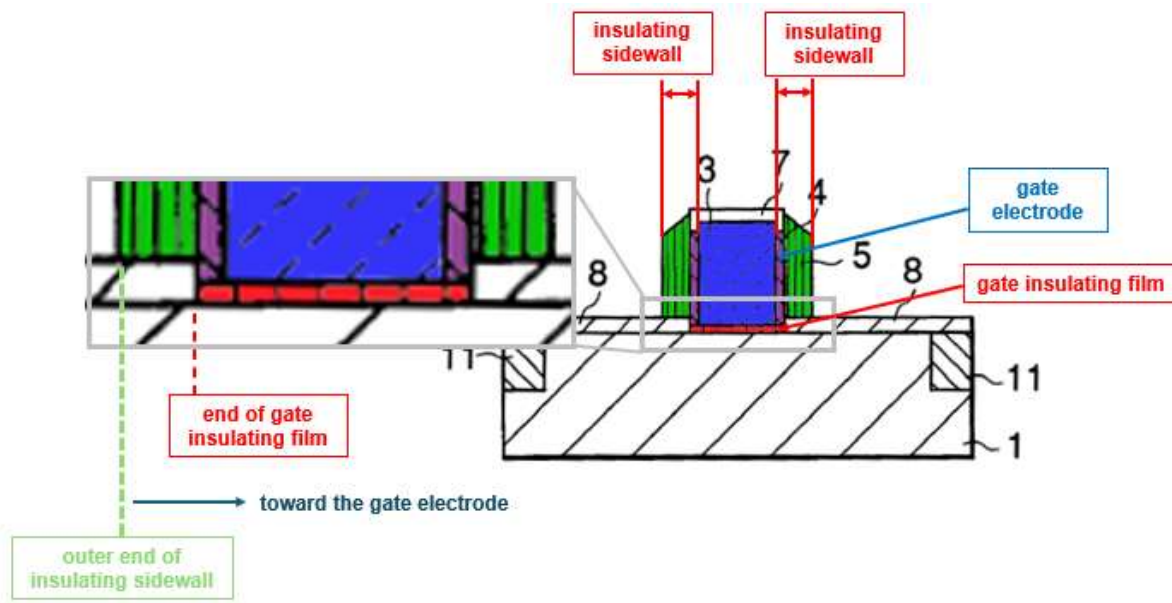
[1E] an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

106. The devices of Kamata’s first, fourth, and ninth embodiments each teaches “an end of the gate insulating film under the insulating sidewall is

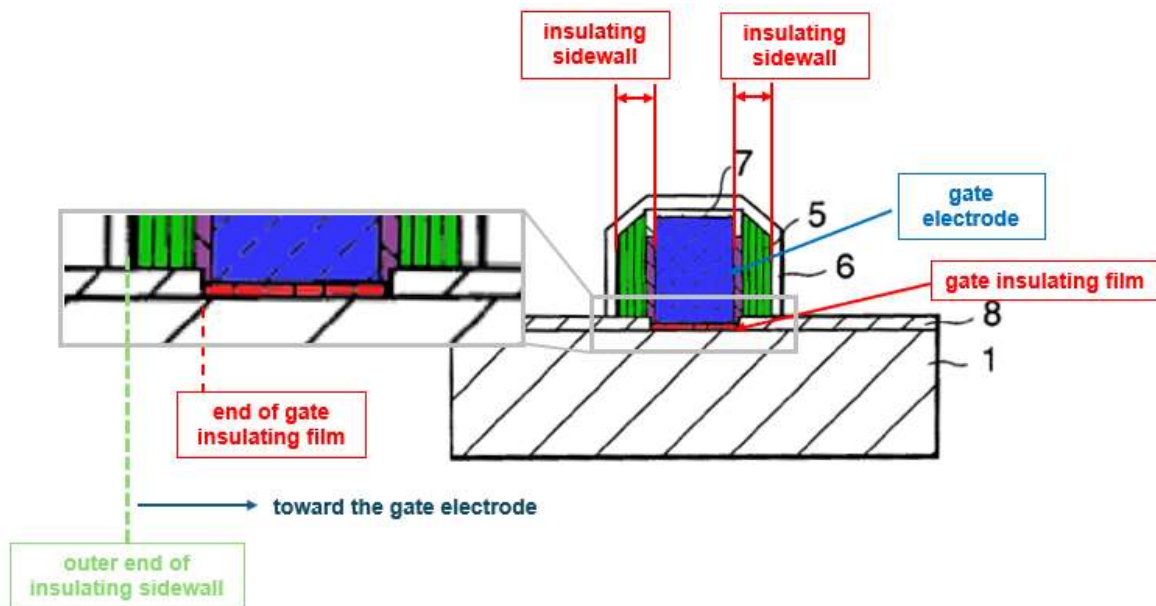
retracted from an outer end of the insulating sidewall toward the gate electrode”
[1E].

107. The term “retract” first appeared in claim 21 of the application leading to the ’076 patent (which issued as claim 1). Based on my review, the term “retract” does not appear anywhere in the ’076 patent specification or any of the other patents in the same family. I understand that, in the co-pending district court litigation, Patent Owner contends this limitation [1E] is satisfied by a gate insulating film whose end is disposed inward at a distance from the outer end of the insulating sidewall and does not require any portion of the end of the gate insulating film to be in contact with the outer end of the insulating sidewall. As discussed below, Kamata’s first, fourth, and ninth embodiments satisfy limitation [1E] at least under Patent Owner’s litigation allegation.

108. **First and Fourth Embodiments.** In Kamata’s first and fourth embodiments, shown in annotated Figures 1B(j) and 5(c) below, the high-k gate insulating film 2 is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode (shaded blue) to under insulating sidewall film 4 (shaded purple), which together with insulating sidewall film 5, forms the claimed “*insulating sidewall*.” (TSMC-1027, ¶¶50 and 56 (together describing formation of gate electrode 3 and sidewalls 4 and 5), 68 (fourth embodiment).)



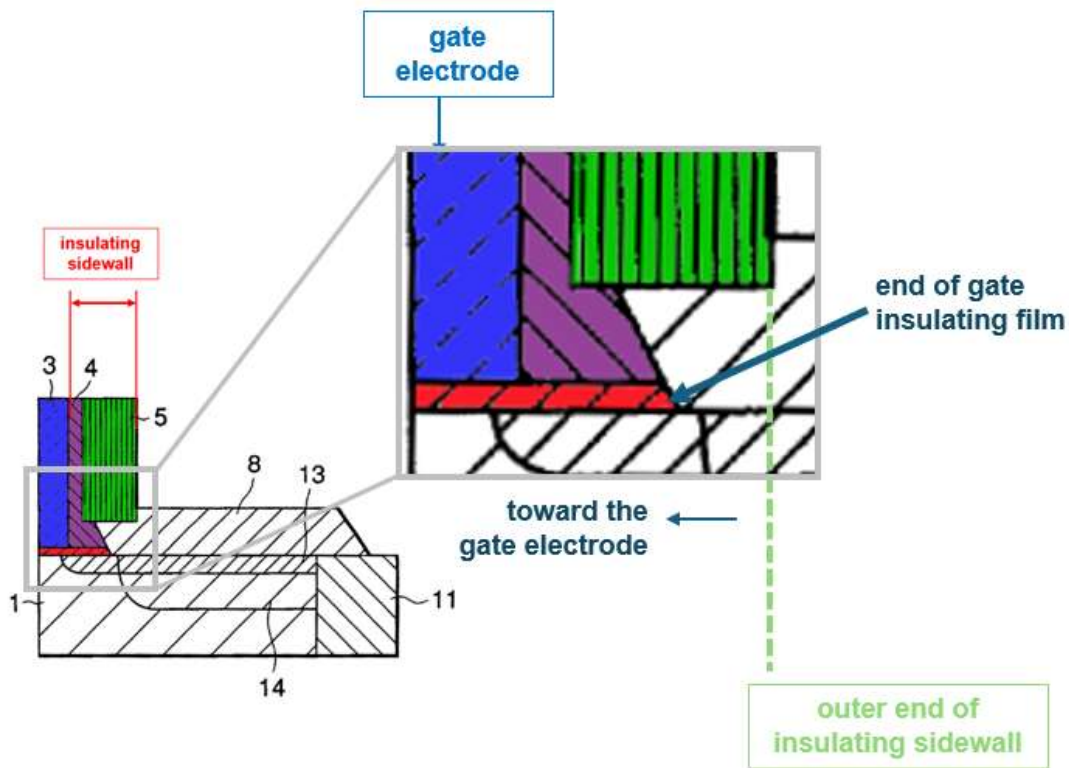
**Kamata, Fig. 1B(j) (with enlargement)
(First Embodiment)**



**Kamata, Fig. 5(c) (with enlargement)
(Fourth Embodiment)**

109. As shown in the figures above, in Kamata's first and fourth embodiments, the end of the gate insulating film is perpendicular to the substrate surface and is disposed inward from the outer end of sidewall film 5 (the outer end of the "*insulating sidewall*") toward the gate electrode. Thus, the end of the high-k gate dielectric in the first and fourth embodiments each teaches "*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode,*" at least under Patent Owner's litigation allegation discussed above.

110. **Ninth Embodiment.** Kamata's ninth embodiment meets this limitation [1E] too. For example, as shown in Figure 10(b), annotated below, the high-k gate insulating film 2 of Kamata's ninth embodiment is also an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode (shaded blue) to under sidewalls 4 (shaded purple) and 5 (shaded green), which are collectively the "*insulating sidewall*." (TSMC-1027, ¶¶50 and 56 (together describing formation of gate electrode 3 and sidewall 5), 93 (describing deep diffusion region 14 formation after sidewall film formation), 94.)



**Kamata, Fig. 10(b) (with enlargement)
(Ninth Embodiment)**

111. Also as shown in annotated Figure 10(b), although the gate insulating film extends partially under sidewall film 5, it does not extend all the way to the outer end of sidewall 5 (which is the outer end of the claimed “*insulating sidewall*”). Rather, in the ninth embodiment, the end of gate insulating film 2 (shaded red) is tapered and disposed inward from the outer end of sidewall 5 toward the gate electrode. Thus, the end of high-k gate dielectric in the ninth embodiment is “*retracted from an outer end of the insulating sidewall toward the gate electrode*” [1E], at least under Patent Owner’s litigation allegation discussed above.

C. Dependent Claim 2

[2] *The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.*

112. Kamata's first, fourth, and ninth embodiments each teaches "*a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.*"

113. For example, Kamata discloses that "[i]t is desired that a **SiO_x (0<x≤2)** layer ... is **interposed between the gate insulating film and the silicon substrate . . .**" (TSMC-1027, ¶¶54, 68 (relating fourth embodiment to first embodiment), 94 (relating ninth embodiment to first embodiment).) This SiO_x layer is a "*buffer insulating film formed of a silicon oxide film*" disposed between the substrate and high-k gate insulating film 2.

D. Dependent Claim 3

[3] *The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide.*

114. Kamata's first, fourth, and ninth embodiments each teaches "*the gate insulating film is formed of a Hf based oxide*" [3].

115. As stated above, Kamata discloses that the gate insulating film may be "a high dielectric constant film such as an oxide film with higher dielectric constant than the silicon oxide, **containing** at least an element selected from a

group of Ti, Zr, **Hf**, Ta, La, Al Ba, Sr, Y, Pr and Gd, and a silicate film containing such an element.” (TSMC-1027, ¶52). Kamata further provides a list of exemplary materials for its high-k film and teaches that “[t]he film may be . . . HfO₂” (TSMC-1027, ¶53.) HfO₂ is a “*Hf based oxide*.”

116. A POSITA would have been motivated to use a Hf-based oxide as a high-k gate insulating film, as explicitly suggested by Kamata. By 2005, i.e., the earliest priority date of the '076 patent, a POSITA would have been motivated to select HfO₂ as a high-k gate insulating film, as hafnium-based dielectrics (e.g., HfO₂) had already become a popular high-k dielectric in advanced semiconductor manufacturing due to the many known benefits. For example, HfO₂ was known to have superior thermal stability and band gap alignment. (*See, e.g.*, TSMC-1037, 2.4.1 (“Recently, HfO₂ films have emerged as the most promising gate dielectric material for sub 100 nm technology due to its superior thermal stability with poly-Si and reasonable band alignment”); TSMC-1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 134 (“Excellent dielectric properties such as high dielectric constant, low leakage current, good thermal stability, negligible dispersion and excellent reliability were demonstrated. These results suggest that HfO₂ is a promising material for the future gate dielectric

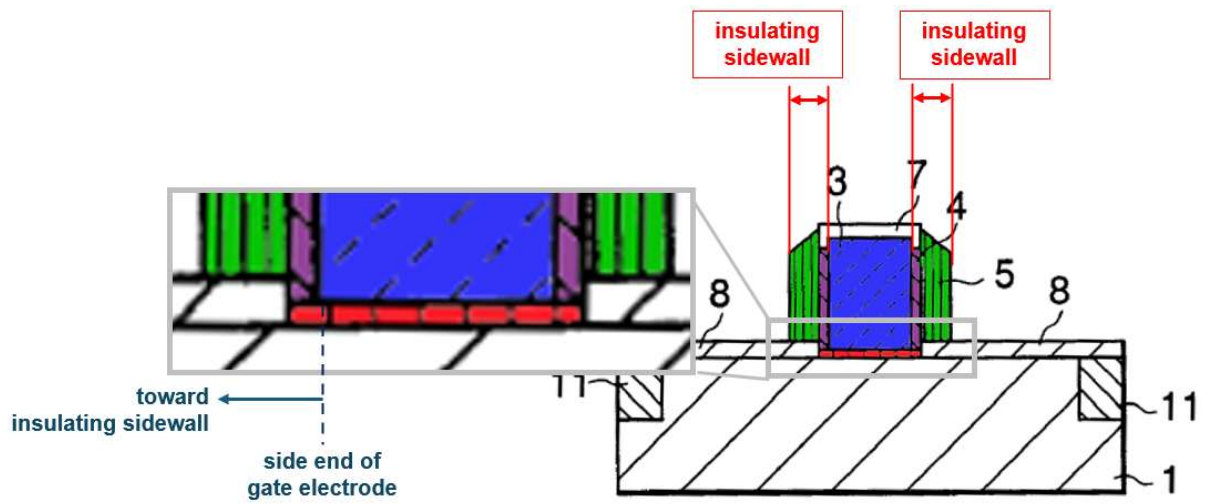
application.”.) HfO_2 also could be scaled down to a smaller EOT. (TSMC-1032, 207.)

E. Dependent Claim 7

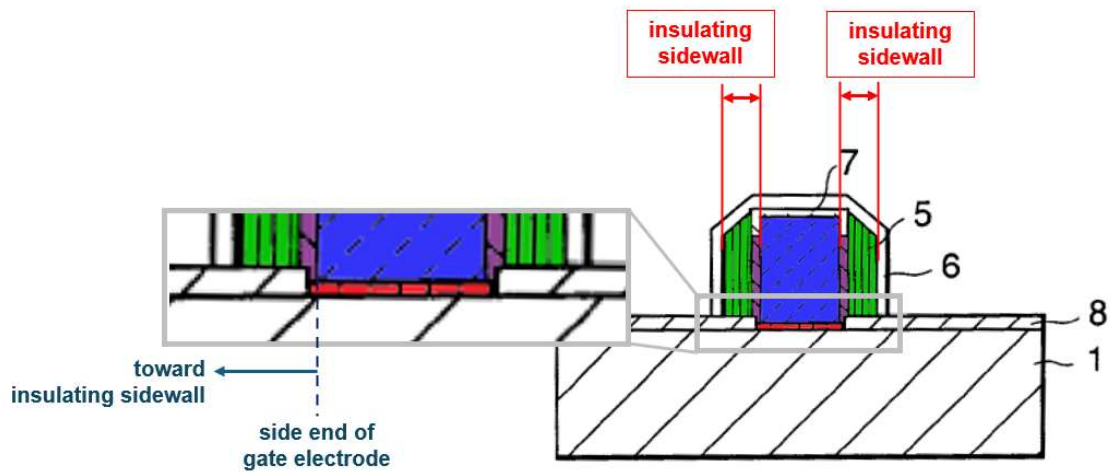
[7] *The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.*

117. Kamata’s first, fourth, and ninth embodiments each teaches “*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*” [7].

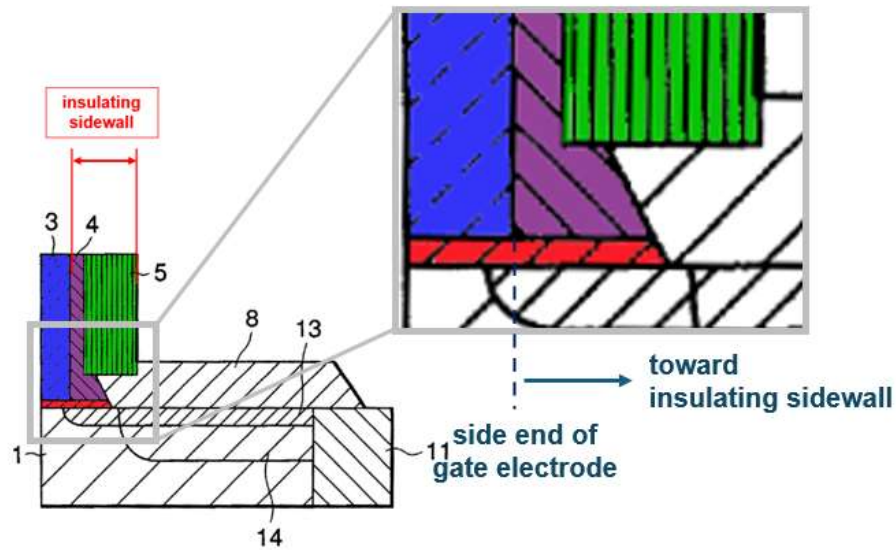
118. As discussed in connection with limitation 1[D] and shown below, in each of Kamata’s first, fourth, and ninth embodiment devices, high-k dielectric film 2 extends (protrudes outward) from under the gate electrode to under at least first sidewall 4 which is part of the “*insulating sidewall*.” Kamata’s devices therefore teach claim 7.



Kamata, Figure 1B(j) with enlargement



Kamata, Figure 5(c) with enlargement



Kamata, Figure 10(b) with enlargement

F. Dependent Claim 8

[8] *The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.*

119. Kamata’s first, fourth, and ninth embodiment devices each teaches “the insulating sidewall has a double layer structure including an oxide film and a nitride film” [8]. As discussed above with regard to limitation [1C], the “insulating sidewall” of each embodiment includes first sidewall film 4, which is an **oxide** film, and second sidewall film 5, which is a **nitride** film. (TSMC-1027, ¶¶50, 58.) A POSITA would have understood films 4 and 5 to each be a “layer” of the collective sidewall, consistent with the disclosures of the ’076 patent. (See TSMC-

1027, ¶¶16 (referring to “multilayer type sidewall films”), 50, 58; TSMC-1001, 21:6-15.)

G. Dependent Claim 9

[9] *The semiconductor device of claim 1, wherein the insulating sidewall has a triple layer structure including a first oxide film, a nitride film, and a second oxide film.*

120. Kamata’s first, fourth, and ninth embodiment devices each teaches “*the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*” [9]. As explained above with regard to claim 8, the “*insulating sidewall*” of each embodiment includes first sidewall film 4, which is an **oxide** film, and second sidewall film 5, which is a **nitride** film. (TSMC-1027, ¶¶50, 58.)

121. Kamata also discloses that a third layer may be present, by disclosing that “**a liner layer** that may be a **silicon oxide film (SiO₂)** ... may be provided before the deposition of the silicon nitride film 5.” (TSMC-1027, ¶¶51-52; *see also* Kamata ¶¶50, 68, 94.) “The liner layer is not limited to a silicon oxide film and a multilayer film made of a plurality of materials may alternatively be used for the liner layer.” (TSMC-1027, ¶51). This liner layer is a second oxide film.⁷

⁷ Claim 15 requires no specific order for the recited films.

122. It should be noted that while Kamata discloses an optional liner layer as part of its sidewall structure, a POSITA would have been motivated to include this layer for, for example, interface control and improved adhesion. This aligns with Kamata's teaching of the liner layer being a silicon oxide film (SiO_2), which forms a natural part of a triple-layer sidewall structure. Additionally, the inclusion of this liner is consistent with well-established practices in semiconductor fabrication to enhance stability and reduce device variation, making it an obvious choice for implementation.

123. Accordingly, the “*insulating sidewall*” (first and second sidewall films) of Kamata's first, fourth, and ninth embodiments has “*a triple layer structure*” comprising first silicon oxide sidewall 4 (“*a first oxide film*”), silicon oxide liner layer (“*a second oxide film*”), and Si_3N_4 second sidewall 5 (“*a first nitride film*”). A POSITA would have understood each film to be a “layer” of the collective sidewall, consistent with the disclosures of the '076 patent. (See TSMC-1027, ¶¶16 (referring to “multilayer type sidewall films”), 50, 58; TSMC-1001, 21:6-15.)

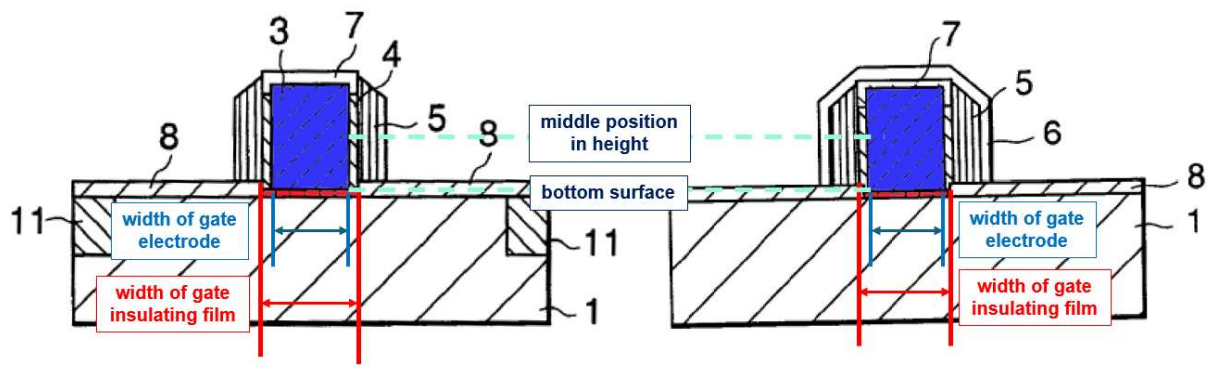
H. Dependent Claims 10 and 13

[10] *The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.*

[13] *The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.*

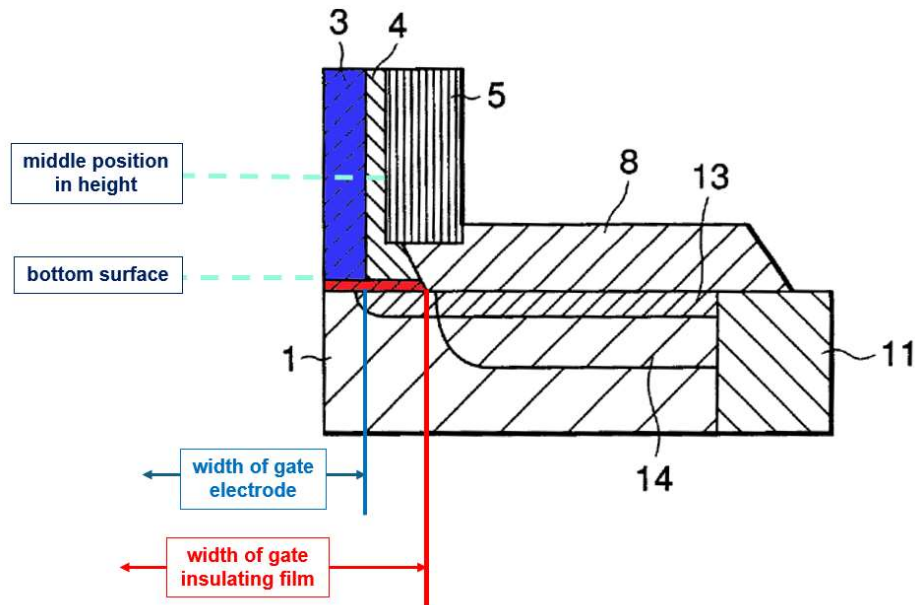
124. The devices of Kamata's first, fourth, and ninth embodiments each teaches "*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*" [10] and "*the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length*" [13].

125. As can be seen in Figures 1B(j), 5(c), and 10(b), annotated below, in each embodiment, the width of Kamata's gate electrode along the gate length is consistent across its entire height in each embodiment. Accordingly, for the same reasons discussed in connection with limitation [1D] above, the width of high-k gate insulating film 2 (shaded red), including at its bottom surface, is larger than the width of gate electrode 3 (shaded blue), including at its bottom surface and a middle position in height of the gate electrode.



**Kamata, Figures 1B(j)
(First Embodiment)**

**Kamata, Figure 5(c)
(Fourth Embodiment)**



**Kamata, Figure 10(b)
(Ninth Embodiment)**

I. Dependent Claims 11-12

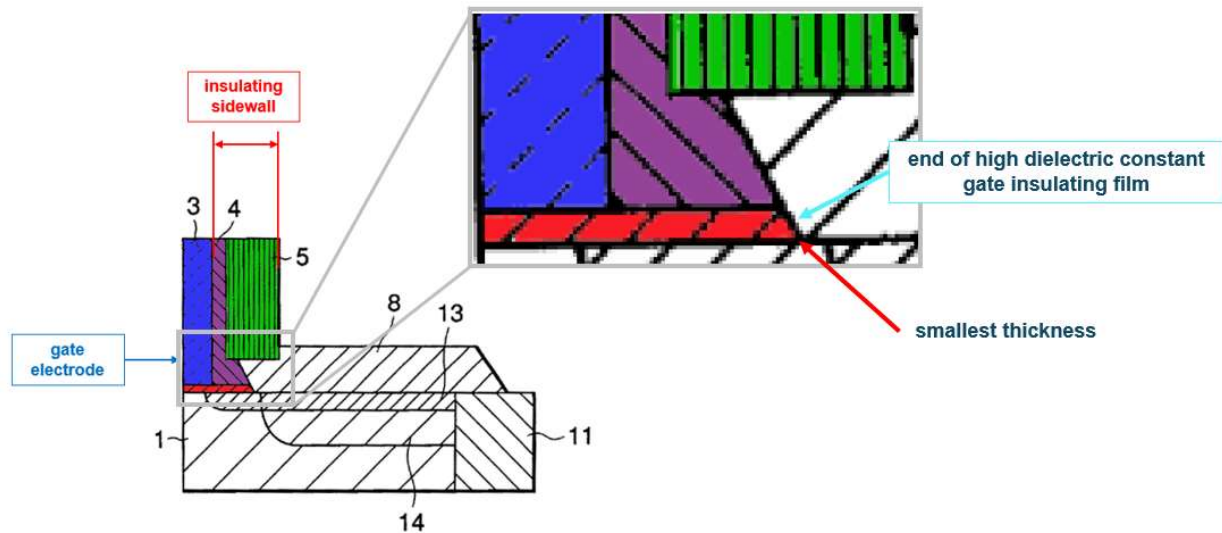
[11] *The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.*

[12] *The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.*

126. Claims 11 and 12 relate to the thickness and shape of the high gate insulating film.

127. At least Kamata's ninth embodiment discloses the limitations of claims 11 and 12.

128. As shown in Figure 10(b), annotated below, gate insulating film 2 extends from under gate electrode to under sidewall films 4 and 5 (collectively the "*insulating sidewall*"), and the end surface of gate insulating film 2, located under the "*insulating sidewall*," diminishes in thickness towards its far end, which a POSITA would understand to be a tapered surface, thus teaching claims 11 and 12. (See TSMC-1027, ¶93; see also TSMC-1027, ¶85 (describing formation of slanted surfaces in embodiment having same slanted gate dielectric and slanted epitaxially grown film 8).)



**Kamata, Fig. 10(b) (with enlargement)
(Ninth Embodiment)**

VI. GROUND 2: Combination of Kamata and Koyama Renders Claim 4 Obvious.

[4] *The semiconductor device of claim 1, wherein the gate insulating film is formed of a HfSiON film.*

129. Kamata discloses a high-k gate insulating film 2 formed of, e.g., Hf silicate. (See TSMC-1027, ¶¶52-53.) Kamata, however, does not explicitly disclose that “the gate insulating film is formed of a HfSiON film” [4]. Koyama, discussed below, discloses this limitation, and thus the combination of Kamata and Koyama renders claim 4 obvious. “Effects of Nitrogen in HfSiON Gate Dielectric on the Electrical and Thermal Characteristics” to Koyama, et al. (“Koyama”; TSMC-1029) was published in 2002. Koyama’s study relates to high-k dielectrics used in semiconductor devices; it is therefore in the same field as Kamata and the ’076

patent. (TSMC-1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1027, ¶3 (“This invention relates to a semiconductor device and a method of manufacturing the same.”).)

130. Koyama states that “Hf(Zr) silicates are considered to be prospective high-K materials due to their modest dielectric constants and good interface properties.” (TSMC-1029, 849.) Observing that a “HfSiON gate dielectric with excellent thermal stability has been proposed,” Koyama studied “the effects of nitrogen on the improved thermal stability and electrical characteristics of this dielectric.” (TSMC-1029, 849.) Out of its studies, Koyama concluded that “nitrogen [in HfSiON] enhances the dielectric constant of silicates” and “boron penetration is substantially suppressed in the HfSiON during high temperature annealing.” (TSMC-1029, 849.) Koyama’s results “strongly suggest that HfSiON is the most probable material for first generation high-K gate dielectrics.” (TSMC-1029, 850.)

131. Based on Koyama’s teachings, which were available in 2002, a POSITA reading Koyama would have been motivated to use HfSiON for its high-k a gate insulating film in place of Kamata’s Hf silicate gate insulating film. (*See* TSMC-1027, ¶¶52-53.) The devices resulting from applying Koyama’s teachings

to Kamat's first, fourth, and ninth embodiments provide devices where gate insulating film 2 "*is formed of a HfSiON film*" as recited by claim 4.

132. A POSITA would have been motivated to apply Koyama's teachings regarding use of HfSiON as a high-k gate dielectric to each of Kamata's first, fourth, and ninth embodiments. Kamata already presents Hf silicate as an option for its high-k gate dielectric. (*See* TSMC-1027, ¶52.) This suggestion would have motivated a POSITA to investigate Hf silicate options and would have led the POSITA to Koyama. As discussed above, Koyama expressly teaches that, among Hf silicates, HfSiON was the most probable high-k material in view of the benefits resulting from its incorporation of nitrogen. (TSMC-1029, 849.) A POSITA would therefore have been motivated to use HfSiON for the benefits disclosed by Koyama to improve device operation, including improved thermal stability and electrical characteristics and enhanced dielectric constant. (TSMC-1029, 849.)

133. Combining Koyama with Kamata's first, fourth, and ninth embodiments in the manner above would have been nothing more than the use of a known technique (Koyama's use of HfSiON as a gate insulating film) to improve similar devices (the transistors of Kamata's first, fourth, and ninth embodiments) in the same way. Because techniques for forming gate insulating films were well-established and formation of high-k dielectric films such as HfSiON uses these processes, a POSITA would have had a reasonable expectation of success and the

combination would have yielded predictable results. (*See also* TSMC-1032, 561-62.)

VII. GROUND 3: Combination of Kamata and Sim Renders Claim 6 Obvious.

[6] <i>The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.</i>

134. Kamata discloses use of HfO₂ as a high-k gate insulating film (*see* TSMC-1027, ¶53) but does not expressly disclose that “*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [6]. Sim provides this teaching, as discussed in greater detail below. Accordingly, the devices of the combination of Kamata (first/fourth/ninth embodiments) and Sim provide “*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [6]. Sim, titled “Effects of ALD HfO₂ thickness on charge trapping and mobility,” was published on June 17, 2005. Sim’s study related to the use of high-k dielectrics used in semiconductor devices. (TSMC-1024, Abstract (“Scaling the physical thickness of the HfO₂ dielectric causes less charge trapping and higher mobility.”).) Sim is therefore in the same field as Kamata and the ’076 patent. (TSMC-1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1027, ¶3 (“This invention relates to a semiconductor device and a method of manufacturing the same.”).)

135. Sim explicitly describes use of a gate insulating film having a thickness 2 nm or less. Specifically, Sim explains that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.” (TSMC-1024, 218.) Sim’s authors set out to examine and address these drawbacks by testing films of different thickness, and “systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility.” (TSMC-1024, 218.) They found that “scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics,” and “[e]ven within 100 μ s, a 33 $\text{\AA}$ HfO₂ sample shows significant current reduction while a 18 $\text{\AA}$ HfO₂ sample is free from transient charging within the detection limits.” (TSMC-1024, 218-219.) Specifically, Sim concluded that “[s]caling the physical thickness of the HfO₂ dielectric to below 20 $\text{\AA}$ causes less charge trapping and higher mobility.” (TSMC-1024, 221.) 20 $\text{\AA}$ is equal to 2 nm, as recited by claim 6.

136. Applying Sim’s teaching to Kamata’s first, fourth, and ninth embodiments yields devices where the high-k gate insulating film is less than 2 nm, as recited by claim 6. This is especially true for Kamata’s ninth embodiment, since the thickness of the high-k film in Kamata’s ninth embodiment device is even smaller at the ends (because the high-k film is tapered downward) than under the

gate electrode. Thus, the devices resulting from the combination of Kamata and Sim provides that “*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.*”

137. A POSITA would have been motivated to adopt Sim’s solution of forming a gate insulating film with a thickness of 20 Å (2 nm) or less to Kamata’s first, fourth, and ninth embodiments. Kamata discloses the use of hafnium oxide as an example of a high-k gate dielectric), the same film studied in Sim. Sim teaches reducing the thickness of hafnium oxide to below 20 Å enhances mobility and reduces charge trapping, which ensures the performance and scalability of semiconductor devices. (TSMC-1024, 219, 221.) Such improvements align with the continued desire to make transistors smaller and more reliable, which both Kamata and Sim emphasize as goals. (TSMC-1027, ¶5; TSMC-1024, 218.) Furthermore, the atomic layer deposition (ALD) process used in Sim for achieving thin HfO₂ films is well-established and compatible with Kamata’s fabrication methods, ensuring that the integration of Sim’s teachings would have been both feasible and expected for a POSITA. By the time of Sim’s publication (2005), ALD was a well-known and widely adopted technique for depositing high-k dielectric films like HfO₂, offering the precision and scalability required for modern semiconductor fabrication.

138. The aforementioned combination would have been nothing more than the use of a known technique (Sim's HfO₂ dielectric layer with less than 20 Å thickness) to improve similar devices (Kamata's semiconductor device having a hafnium oxide gate dielectric), in the same way. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218; TSMC-1032, 17-19.)

VIII. GROUND 4: Guha Renders Claims 1-3, 5, 7-8, 10-13 Obvious.

A. Overview of Guha

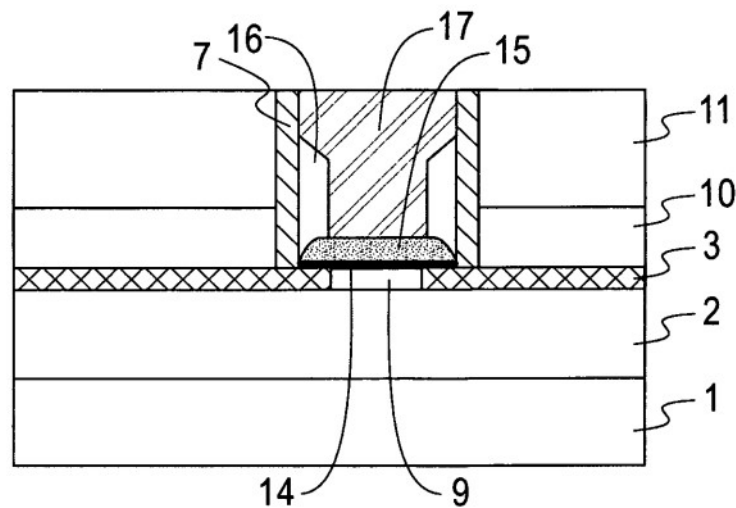
139. U.S. Publication 2006/0091432, titled "Damascene Gate Field Effect Transistor With an Internal Spacer Structure," to Supratik Guha, et al. ("Guha"; TSMC-1028) was filed on November 2, 2004, and published on May 4, 2006.

140. As its title suggests Guha is directed a semiconductor devices such as Field Effect Transistors, and methods for manufacturing the same. (*See also* TSMC-1028, ¶¶1 ("The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device."), 4 ("The invention relates to a MOSFET with improved device performance and method of fabricating the device.").)

141. The analysis herein focuses on the embodiment shown in Figure 12 of Guha, though Guha expressly discloses that its alternative processes include steps

that are common across the different embodiments (TSMC-1028, ¶42 (stating that the alternative process sequence shown in Figures 10-12 build on the structure of Figure 7; *see also* TSMC-1028, ¶54 (“Any disclosed embodiment may be combined with one or several of the other embodiments shown and/or described. This is also possible for one or more features of the embodiments.”).)

142. Guha's Figure 12 embodiment is shown below.



Guha, Figure 12

143. As shown in Figure 12, Guha's semiconductor device includes gate electrode 17 with gate spacer structure 16 and isolating spacer structure 7. (TSMC-1028, ¶¶43-45.) A gate insulating film, dielectric layer 15, is formed on a gate-isolating layer 14, both of which extend from under gate electrode 17 to under gate spacer structure 16. (TSMC-1028, ¶¶38, 43-44.) Dielectric layer 15 “preferably compris[es] a high-K dielectric material, [which] is a material that exhibits a

dielectric constant of approximately above 10 or more. Examples of such materials, include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide.” (TSMC-1028, ¶¶38, 43) “The gate-isolating layer 14 acts as a buffering layer between channel 9 and the dielectric material to be deposited thereon,” and is, for example, “used to prevent mobility degradation in the silicon channel that may be caused by scattering mechanisms in the dielectric layer.” (TSMC-1028, ¶37). As discussed in detail below, Guha’s disclosure of high-k dielectric materials and its focus on structural and material integration aligns with design principles relevant to MOSFETs, providing insights that a POSITA could apply to address the limitations of claims 1-3, 5, 7-8, and 10-13.

B. Independent Claim 1

1. Preamble [1P]

[1P] <i>A semiconductor device comprising:</i>
--

144. Guha’s Figure 12 device is a “*semiconductor device*.” For example, Guha is directed at MOSFETs, which a POSITA would have understood to be a semiconductor device. (TSMC-1028, ¶¶1 (“The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device.”), 4 (“The invention relates to a MOSFET with improved device performance and method of fabricating the device. ”).) Guha also discloses

that its device includes substrate 1 and channel layer 3 each “compris[ing] any **semiconducting material.**” (TSMC-1028, ¶¶22-23, ¶¶43-45 (relating Figure 9’s first embodiment device to Figure 12 device)).

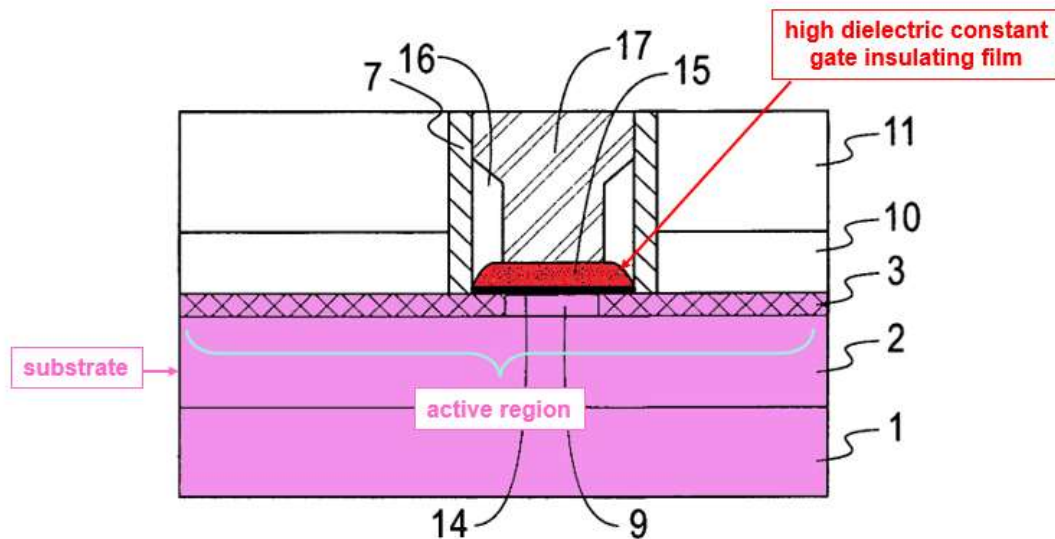
2. Limitation [1A]

<i>[1A] a gate insulating film formed on an active region in a substrate and including Hf;</i>
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145. Guha’s semiconductor device includes a high dielectric constant gate insulating film formed on an active region in a substrate. Guha discloses manufacturing “an initial stacked structure that comprises a substrate 1 having a bottom insulator 2, also referred to as buried oxide layer, located thereon. The initial stacked structure also includes a channel layer 3 on top of the bottom insulator 2, and an oxide layer 4, also referred to as pad protection layer, located atop the channel layer 3.” (TSMC-1028, ¶21). The substrate 1 “may be of the n or p-type depending on the desired device to be fabricated.” (TSMC-1028, ¶22; *see also* TSMC-1028, ¶43.)⁸ Channel layer 3 is further provided over buried oxide layer 2 which “can be omitted.” (TSMC-1028, ¶22; *see also* TSMC-1028, ¶43.) A

⁸ Paragraph 43 of Guha indicates that the embodiment of Figures 10-12 is built on the structure of Figure 7, and thus the discussion of the preceding figures applies to that of Figure 12. (Guha, ¶43).

POSITA would have understood that Guha’s substrate 1, channel layer 3, and buried oxide layer 2 (if present) are collectively “*a substrate*” (shaded pink).



Guha, Fig. 12 (annotated)

146. Guha discloses “the substrate may further contain active device regions.” (TSMC-1028, ¶22; *see also* TSMC-1028, ¶43.) “[S]ource/drain extensions, also referred to as source/drain (S/D) junctions, are formed by implanting dopants through the pad protection layer 4 into the channel layer 3, with the dummy gate 5 acting as an implantation mask. Following ion implantation, the S/D extensions are annealed to activate dopants. A channel 9 (see FIG. 3), having a predetermined channel length substantially equal to the length of the dummy gate 5, is thus defined between the S/D extensions.” (TSMC-1028, ¶26; *see also* TSMC-1028, ¶43.) Based on these disclosures, a

POSITA would have understood that Guha's device has "*an active region in a substrate*," and that a portion of channel layer 3 forms part of that active region.

147. Guha's Figure 12 device includes an optional gate-isolating layer 14 (shaded black) formed on the "*active region in a substrate*." Dielectric layer 15 (shaded red), "comprising a high-k dielectric material," is "formed only on the gate-isolating layer 14" on the active region in the substrate. (TSMC-1028, ¶¶37-38, 43.) "A high-K material is a material that exhibits a dielectric constant of approximately above 10 or more. Examples of such materials, include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide." (TSMC-1028, ¶38; *see also* TSMC-1028, ¶43 ("This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafnium [*sic*], zirconium, aluminium [*sic*], among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing a further reduction in sidewall capacitance").)

148. A POSITA would have been motivated to select hafnium-based dielectric, such as hafnium oxide or hafnium silicate, because of their known benefits as of 2005, e.g., HfO₂'s "superior thermal stability with poly-Si and reasonable band alignment," and HfSiON's "improved thermal stability and electrical characteristics." (TSMC-1037, 2.4.1; TSMC-1029, 849; *see also* TSMC-

1032, 207 (HfO₂ “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”; HfO₂ can be scaled down to a smaller EOT).) Accordingly, Guha teaches a “*gate insulating film [film 2] ... including Hf.*”

149. Based on these disclosures, a POSITA would have understood Guha’s dielectric layer 15 to be “a high dielectric constant gate insulating film formed on⁹ an active region in a substrate and including Hf.”

3. Limitation [1B]

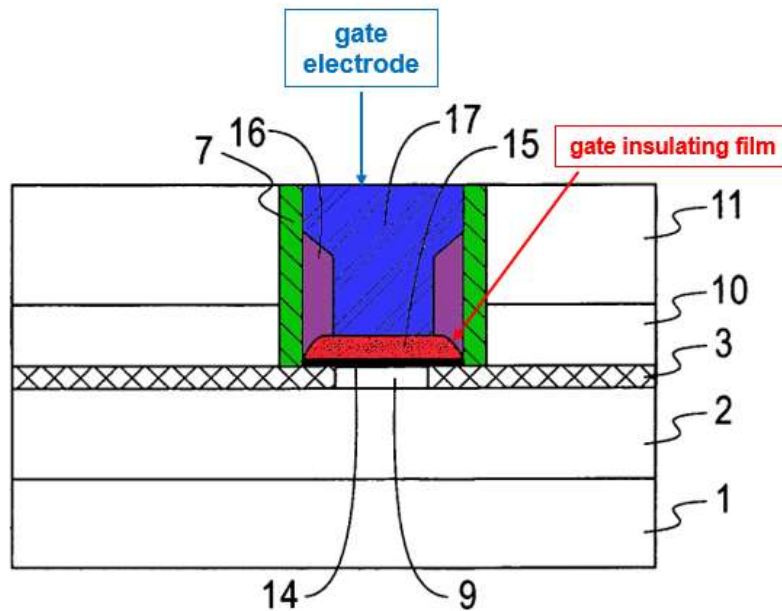
[1B] <i>a gate electrode formed on the gate insulating film;</i>
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150. Guha’s semiconductor device includes a gate electrode formed on the high dielectric constant gate insulating film. Gate electrode 17 is formed by filling cavity 13 with a conductive material. (TSMC-1028, ¶45.) “[T]he conductive material may be formed from vapor phase deposition, such as tungsten or titanium nitride, or by depositing amorphous silicon and reacting it with a metal such as nickel to form a silicide, and subsequently thinning it down to the dielectric

⁹ The ’076 patent uses the term “formed on” to indicate relative position and does not require direct contact. (*See, e.g.*, 7:42-44 (“An insulating sidewall 7 is formed on each side surface of the gate electrode 5 with an offset sidewall 6 interposed therebetween”).)

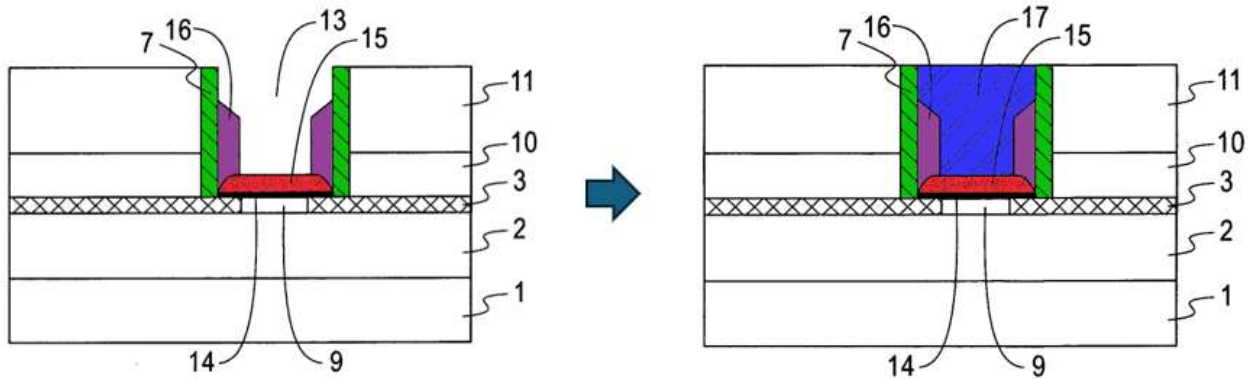
layer 15, and possibly removing the conductive material and the dielectric layer 15 lying outside of cavity 13, e.g., by CMP. Polysilicon may also be used, for example, either in-situ doped or doped by a conventional ion-implantation and annealing technique, as long as the annealing temperatures and conditions are compatible with the dielectric layer 15 and the second overlayer 11.” (TSMC-1028, ¶41). According to Guha, “by means of the gate spacer structure 16, the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9.” (TSMC-1028, ¶45.) From these disclosures, a POSITA would have understood that gate 17 is “*a gate electrode formed on the gate insulating film.*” (TSMC-1028, ¶¶41, 45).

151. Figure 12 of Guha, below, shows gate electrode 17 (shaded blue) formed on high-k dielectric layer 15 (shaded red).



Guha, Fig. 12 (annotated)

152. Guha's fabrication process confirms my description of Guha's Figure 12 device. Guha describes that cavity 13 (Figure 11 (left)) is "filled with a conductive material to form the **gate 17**" by "depositing the material into the cavity 13 and **onto the dielectric layer 15.**" (TSMC-1028, ¶¶41, 44 (associating gate formation in Figure 12 (right) with first embodiment process), 45.) This results in the formation of the gate electrode over dielectric layer 15.

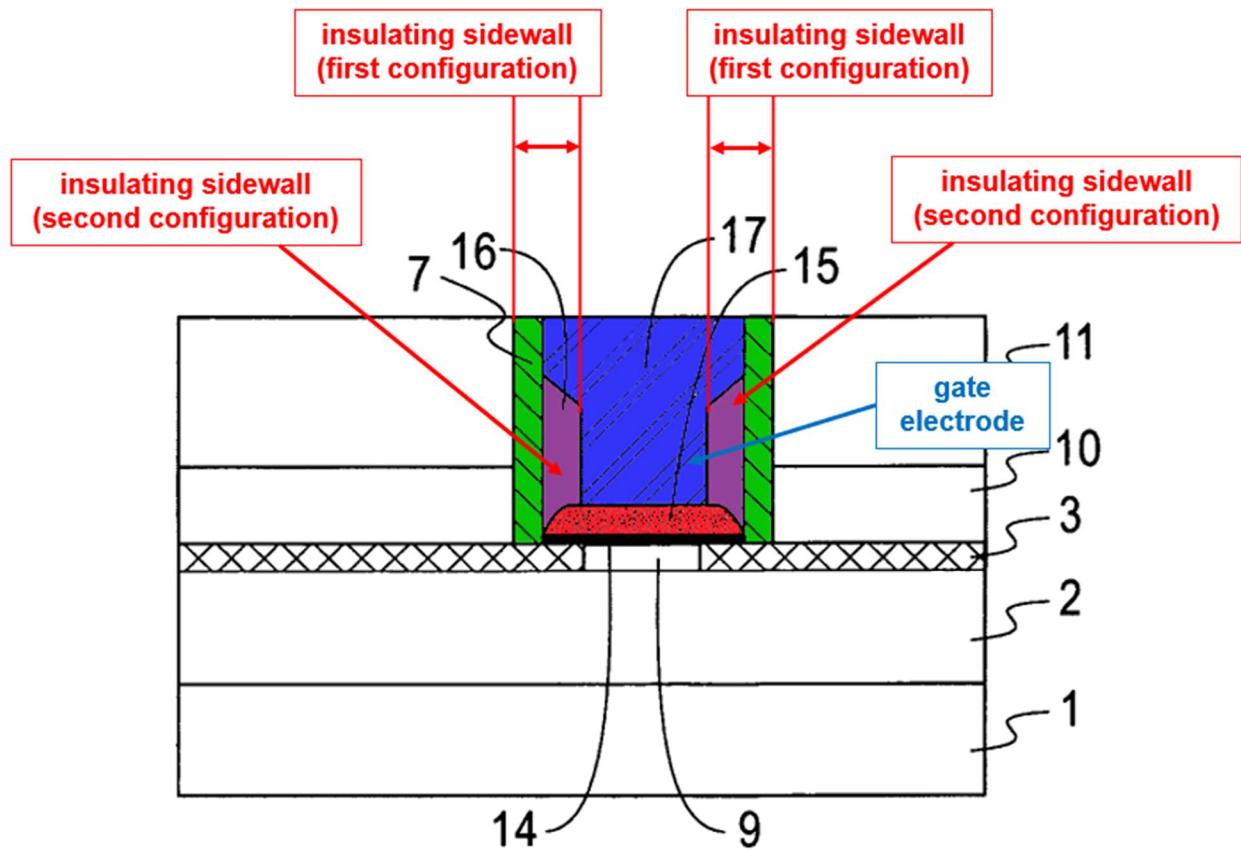


Guha, Figs. 11 (left) and 12 (right) (annotated)

4. Limitation [1C]

[1C] *a insulating sidewall formed on each side surface of the gate electrode;
and*

153. Guha's Figure 12 device includes an insulating sidewall formed on each side surface of the gate electrode. (See TSMC-1028, ¶¶28 (formation of isolating spacers 7), 44 (formation of spacers 16), 43 (associating Figure 12 device to process steps associated with Figures 1-7).) For example, Guha discloses forming a semiconductor device with gate spacers 16 (shaded purple) and isolating spacers 7 (shaded green) on the side surfaces of gate electrode 17 (shaded blue), as shown in Figure 12, below.



Guha, Fig. 12 (annotated)

154. “Isolating spacer structure 7 can be composed of any insulating material including, for example, an oxide, nitride, oxynitride or any combination thereof; as long as the material can be selectively etched with respect to the material of the dummy gate spacers 8. Isolating spacer structure 7 can be formed by deposition of an insulating material and subsequent etching. A preferred material would be silicon nitride.” (TSMC-1028, ¶¶28, 43.)

155. “[I]nternal’ gate spacers 16, or more generally, a gate spacer structure, is formed inside the cavity 13 . . . , for example, by depositing a spacer

material, e.g. an oxide or other suitable material, in the cavity 13 and etching the deposited material anisotropically, e.g. by RIE, such that the portion of the dielectric layer 15 above channel 9 is exposed, leaving the gate spacer structure 16 on the sidewalls of the cavity 13. This arrangement of the gate spacer structure 16 provides a narrowing of the cavity 13 above the channel 9.” (TSMC-1028, ¶¶40, 43.) In the embodiment of Figure 12, “the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7.” (TSMC-1028, ¶44.)

156. Although Guha refers to each of these structures as a “spacer,” a POSITA would have understood them to be “sidewalls,” as the terms “spacer” and “sidewall” are often used interchangeably in the art, as I noted above. Additionally, a POSITA would have understood Guha’s “spacers” to be “sidewalls” as used in the ’076 patent. (*See, e.g.*, TSMC-1028, ¶¶40 (describing “gate spacer structure 16 on the sidewalls of the cavity”), 44.)

157. A POSITA would have also understood both gate spacers 16 and isolating spacers 7 to be insulating sidewalls. As noted above, Guha discloses that gate spacers 16 are typically formed of “an oxide or other suitable material.” (TSMC-1028, ¶¶40, 43.) Guha further teaches that, “by means of the gate spacer structure 16, the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9.” (TSMC-1028, ¶45.) To provide such benefits, a POSITA would have understood Guha’s

gate spacers 16 to be formed of an **insulating** oxide material, such as silicon oxide, rather than a semiconductor or conductive material. This is because, if gate spacer 16 was formed of a semiconductor or conductive material, it would effectively function similar to the gate electrode (comprised of a semiconductor or conductive material), thereby eliminating the benefits disclosed in Guha. Furthermore, a POSITA would have understood that gate spacers are typically formed of an insulating oxide material. (TSMC-1034, 9, 75; Plummer, 79-80.)

158. Isolating spacers 7 are “composed of any **insulating** material including, for example, an oxide, nitride, oxynitride or any combination thereof” with the “preferred material [being] silicon nitride.” (TSMC-1028, ¶¶28.)

159. As illustrated in Figure 12, gate spacer structure 16 and isolating spacer structure 7 collectively form an “*insulating sidewall formed on each side surface of the gate electrode*” [1C], consistent with the disclosures of the '076 patent. (TSMC-1001, 2:60-65 (“insulating sidewall” includes two sidewalls).) I have been asked to analyze the claims under this first “*insulating sidewall*” configuration.

160. Alternatively, Guha also discloses that isolating structure 7 is “optional” and may “not be necessary.” (TSMC-1028, ¶¶34-35; *see also* TSMC-1028, ¶44 (“In other embodiments where the isolating spacer structure 7 is absent, the gate spacer structure 16 will contact the overlayer 11 instead.”).) In

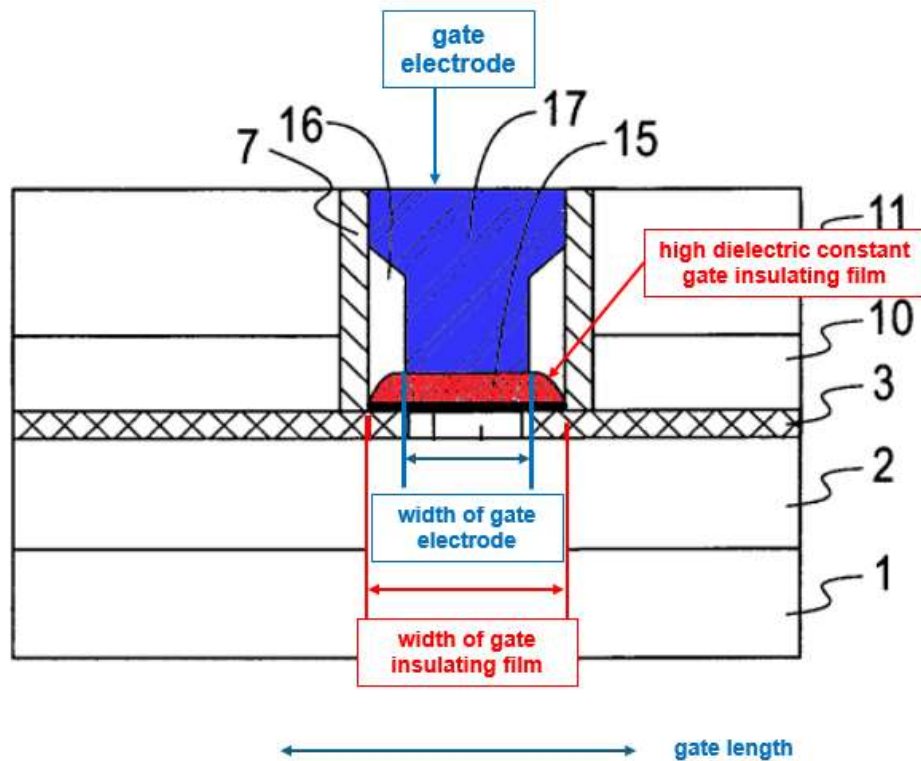
embodiments where the isolating spacer structure 7 is absent, gate spacer 16 alone is an “*insulating sidewall formed on each side surface of the gate electrode*” [1C], consistent with the disclosures of the ’076 patent. (TSMC-1001, 6:9 (“insulating sidewall” has a single component).) For purposes of this Declaration, I will treat this as the second “*insulating sidewall*” configuration.

161. Both the first and second “*insulating sidewall*” configurations meet limitation [1C].

5. Limitation [1D]

[1D] <i>wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and</i>

162. Guha teaches limitation [1D]. As shown in Figure 12, the width of dielectric layer 15 (shaded red) is larger than the width of the bottom surface and bottom portion of gate electrode 17 (shaded blue). (TSMC-1028, ¶¶41, 43-45 (describing formation of spacers 16 in the cavity followed by deposition of the gate electrode).)



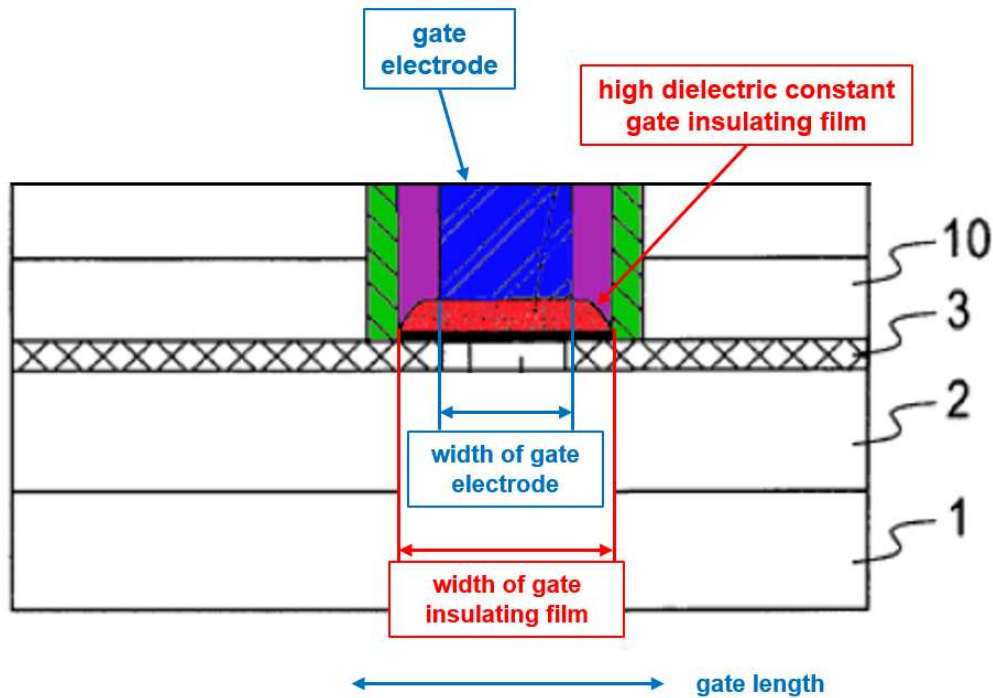
Guha, Fig. 12 (annotated)

163. Should Patent Owner attempt to argue that the width of Guha’s gate electrode at its upper portion is equal to the width of dielectric layer 15 and therefore Guha fails to disclose limitation [1D], I disagree. Nothing in the language of this limitation requires that the width of the gate electrode to be smaller than the width of the gate insulating film at all heights. To the contrary, the limitation recites broadly “*a width of the gate electrode.*” Claim 10 narrows this limitation, reciting that “*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length,*” and claim 13 also narrows this limitation, reciting “*the width of the*

gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.”

164. Even if that were not the case, Guha teaches that “internal spacer 16a and 16b may also have a rectangular cross-section, e.g., by polishing or removing the upper curved region to form a horizontal portion of the internal surface.”

(TSMC-1028, ¶47.) A POSITA would have understood that, with this teaching, the expanded upper portion of the gate electrode could be removed along with the slanted upper portion of spacers 16, resulting in a rectangular cross-section, and a gate electrode that has a uniform width from top to bottom. Put another way, in this embodiment, shown in modified Figure 12 below, the width of the gate electrode is the same at the bottom and the top, and limitation [1D] is again met.



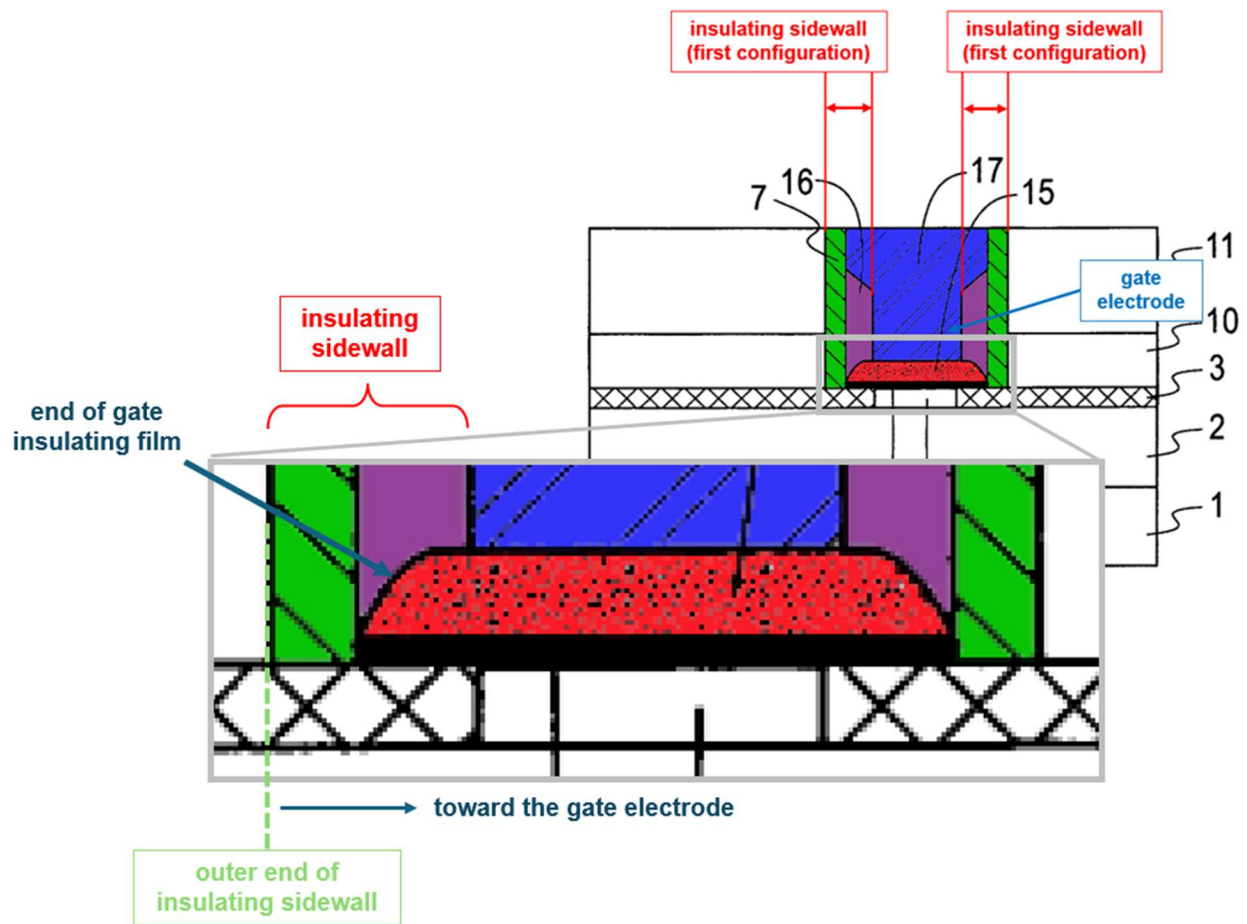
Guha, Modified Figure 12

6. Limitation [1E]

[1E] an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

165. Guha discloses limitation [1E] under both the first and second “insulating sidewall” configuration. As discussed above and shown in Figure 12, Guha’s gate insulating film (shaded red) has a rounded end that protrudes from under the gate electrode (shaded blue) to under spacers 16 (shaded purple). The rounded end of the gate insulating film is not flush with the side end of the gate electrode.

166. **First Configuration (Spacer 16 and Spacer 7).** As shown in Figure 12 below, dielectric layer 15 is an uninterrupted layer (as evidenced by the absence of gaps) that extends from under gate electrode 17 (shaded blue) to under gate spacer 16 (shaded purple), which is part of the “*insulating sidewall*” of the first configuration (gate spacer 16 and spacer 7), but not under spacer 7. This is because dielectric layer 15 is deposited at the bottom of the cavity 13 after isolating spacer 7, but before gate spacer structure 16, is formed. (TSMC-1028, ¶¶43-45 (describing formation of gate spacer 16, dielectric layer 15, and gate electrode 17).).



Guha, Fig. 12 (annotated under first configuration, and enlarged)

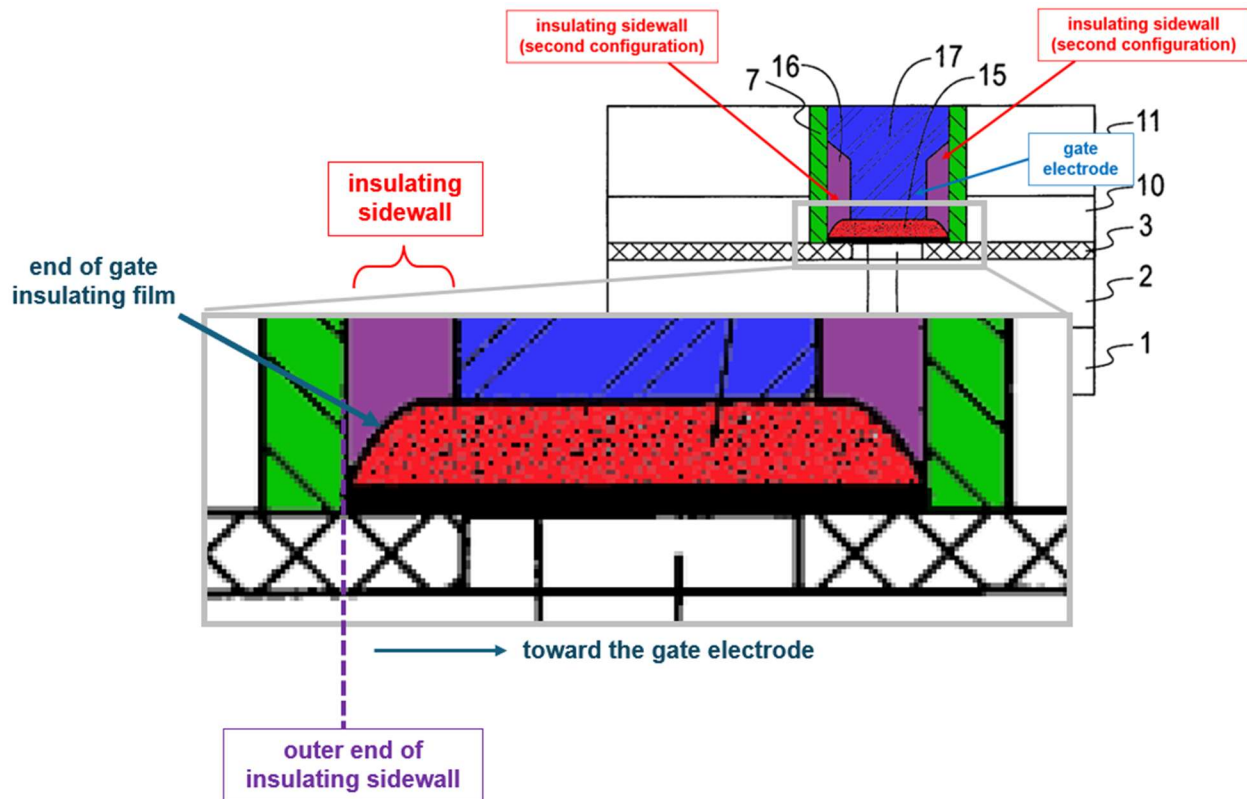
167. Also, as a result of depositing dielectric layer 15 at the bottom of the cavity 13 after isolating spacer 7, but before gate spacer structure 16, is formed, dielectric layer 15 only extends as far as inner surface of isolating spacer 7; dielectric layer 15 does not extend to the outer end of isolating spacer 7 (which is the outer end of the collective “*insulating sidewall*” structure). As shown in Figure 12 above, the end of the gate insulating film is rounded and disposed inward from the outer end of the “*insulating sidewall*” (outer end of spacer 7). Thus, the end of

dielectric layer 15 (“*gate insulating film*”) “*is retracted from an outer end of the insulating sidewall*” [1E], at least under Patent Owner’s litigation allegation discussed above. Thus, limitation [1E] is met under the first “*insulating sidewall*” configuration.

168. **Second Configuration (Spacer 16).** As explained above, Guha also discloses that spacer 7 is optional and may not be included. In such an embodiment, dielectric layer 15 is still an uninterrupted layer (as evidenced by the absence of gaps) that extends from under the gate electrode (shaded blue) to under gate spacers 16, which is the “*insulating sidewall*” of the second configuration. (See TSMC-1028, ¶¶43-45.) Thus, Guha teaches limitation [1D] under the second “*insulating sidewall*” configuration too.

169. Under the second “*insulating sidewall*” configuration, “*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*” as required by limitation [1E]. As shown below, at least part of the dielectric layer 15 does not contact the *outer* end of spacer 16 (shaded purple) (outer end of the collective “*insulating sidewall*”); rather, as shown below, the end of the gate insulating film (shaded red) contacts areas of spacer 16 other than spacer 16’s outer end. Thus, an end of dielectric layer 15 (the “*gate insulating film*”) is disposed inward from the outer end of the spacer 16 toward the gate electrode. It is therefore “*retracted from an*

outer end of the insulating sidewall toward the gate electrode” [1E], at least under Patent Owner’s litigation allegation discussed above.



Guha, Fig. 12 (annotated under second configuration, and enlarged)

C. Dependent Claim 2

[2] *The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.*

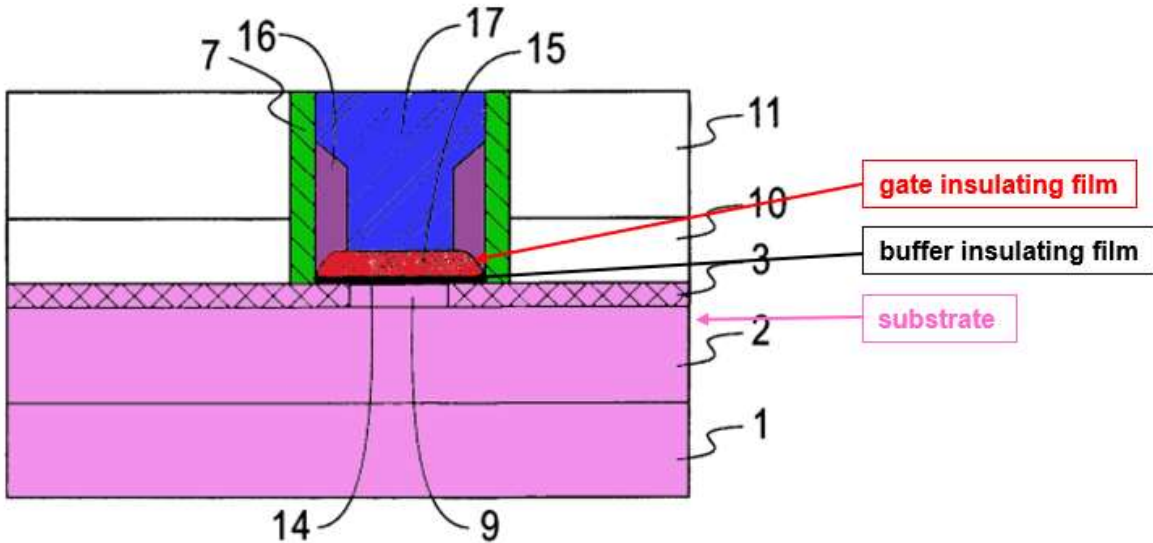
170. Guha’s semiconductor device includes a buffer insulating film between the substrate and the high dielectric constant gate insulating film. For example, Guha discloses with regard to its Figure 12 embodiment that “[i]n this

embodiment, the structure of FIG. 7 is subjected to a deposition step in which the **dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13**. This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafnium [*sic*], zirconium, aluminium [*sic*], among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing a further reduction in sidewall capacitance. As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13.” (TSMC-1028, ¶43.)

171. Guha’s gate-isolating layer 14 can be “formed at the bottom of the cavity 13,” on the substrate. (TSMC-1028, ¶37). “The gate-isolating layer 14 acts as a **buffering layer between channel 9 and the dielectric material** to be deposited thereon. **A preferred material for the gate-isolating layer 14 is silicon oxide**, which can be thermally grown, and thinned if necessary. Other materials, however, may also be suitable. This gate-isolating layer, for example, is used to prevent mobility degradation in the silicon channel that may be caused by scattering mechanisms in the dielectric layer.” (TSMC-1028, ¶37.)

172. Guha’s gate-isolating layer 14 (shaded black) is shown in Figure 12 (below). As explained above with regard to limitation [1A], channel 9 is part of the substrate (shaded pink). Gate-isolating layer 14 is therefore “*a buffer insulating*

insulating film” [2].



Guha, Fig. 12 (annotated)

D. Dependent Claim 3

[3] *The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide.*

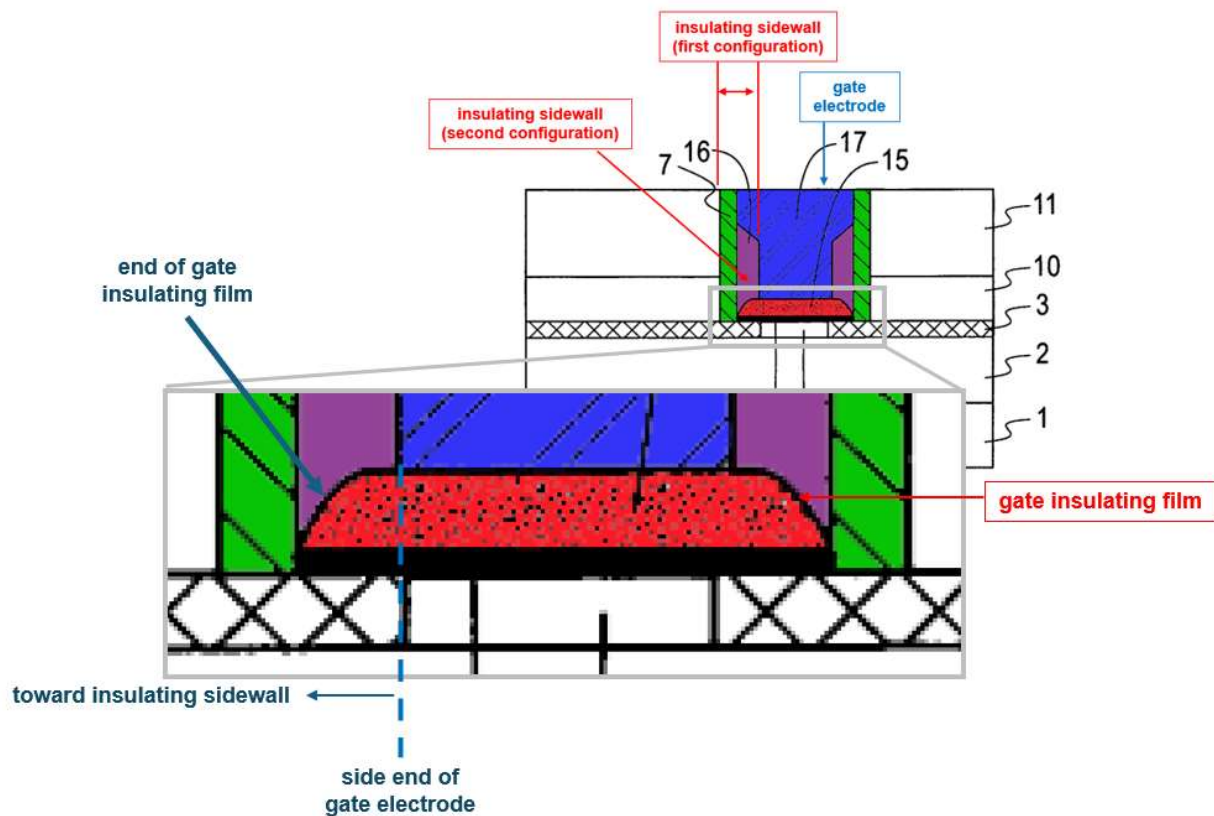
173. Guha discloses this limitation. At a minimum, Guha renders this limitation obvious. Guha specifically discloses that high-k dielectric layer 15 (“*gate insulating film*”) “preferably compris[es] a high-K dielectric material,” and that examples of such high-k materials “include, but are not limited to **hafnium oxide**, hafnium silicate, aluminum oxide or zirconium oxide.” (TSMC-1028, ¶¶38, 43.) Hafnium oxide is “*a Hf based oxide*” as recited by claim 3. A POSITA would have been motivated to select hafnium oxide from Guha’s list of exemplary

materials in light of its known benefits, including thermal stability, band alignment, and ability to scale. (TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 134.)

E. Dependent Claim 7

[7] <i>The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.</i>

174. Guha discloses the limitation of claim 7 under both the first and second “*insulating sidewall*” configurations. As discussed above and shown in Figure 12, Guha’s gate insulating film (shaded red) has a rounded end that protrudes from under the gate electrode (shaded blue) to under spacer 16 (shaded purple). The rounded end of the gate insulating film is not flush with the side end of the gate electrode.



Guha, Fig. 12 (annotated and enlarged)

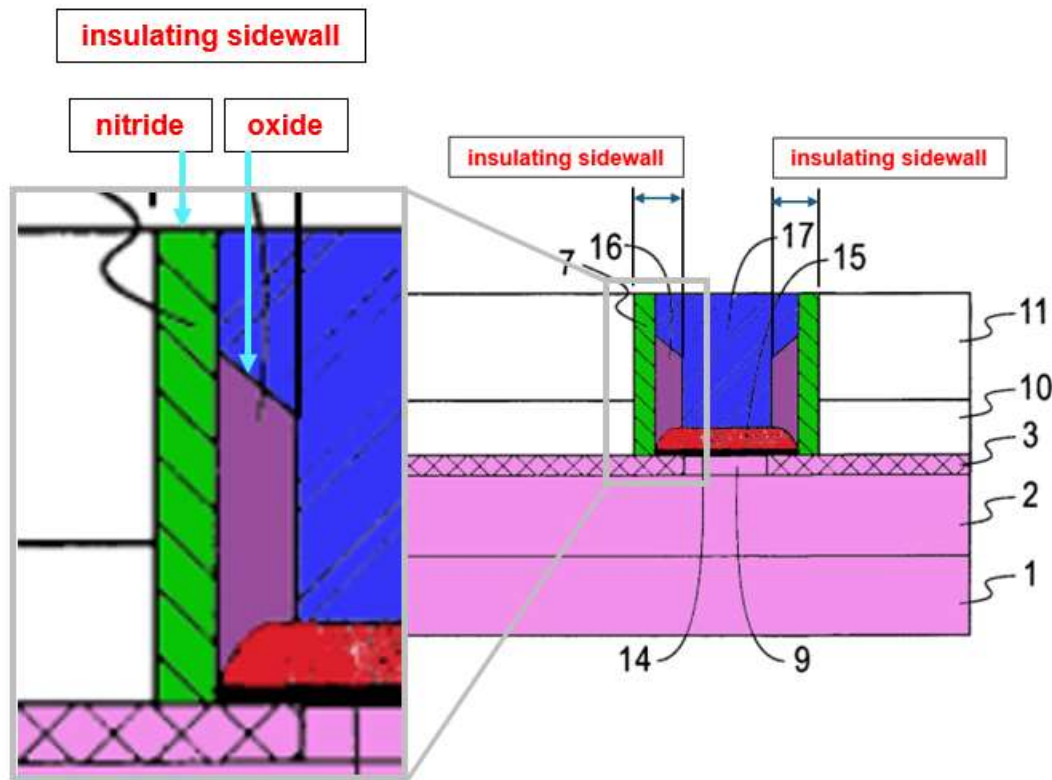
175. In such an arrangement, the end of high-k dielectric layer 15 “protrudes from a side end of the gate electrode toward the insulating sidewall” both in the first configuration (collectively spacers 16 and spacers 7) and the second configuration (spacers 16 alone).

F. Dependent Claim 8

[8] *The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.*

176. Guha discloses the limitation of claim 8, at least under the first “insulating sidewall” configuration (spacer 16 and spacer 7), because spacer 16

and 7 are two layers (a “*double layer structure*”) of the claimed insulating sidewall. This is shown in Figure 12, below.



Guha, Fig. 12 (annotated and enlarged)

177. Guha discloses that Gate spacer 16 is a “material, e.g. an **oxide** or other suitable material.” (TSMC-1028, ¶40) Gate spacer 16 is thus “*an oxide film*.”

178. Isolating spacer 7 “can be composed of any insulating material including, for example, an oxide, **nitride**, oxynitride or any combination thereof.” (TSMC-1028, ¶28.) “A preferred material would be silicon nitride.” (TSMC-1028, ¶28.) Isolating spacer 7 is thus a nitride film.

179. A POSITA would have considered gate spacer 16 and isolating spacer 7 to be “layers” (specifically, a “*double layer structure*”) of the collective sidewall structure, consistent with the disclosures of the ’076 patent. (*See, e.g.*, TSMC-1028, ¶¶28 (formation of spacers 7), 44 (formation of spacers 16); TSMC-1001, 21:6-15.)

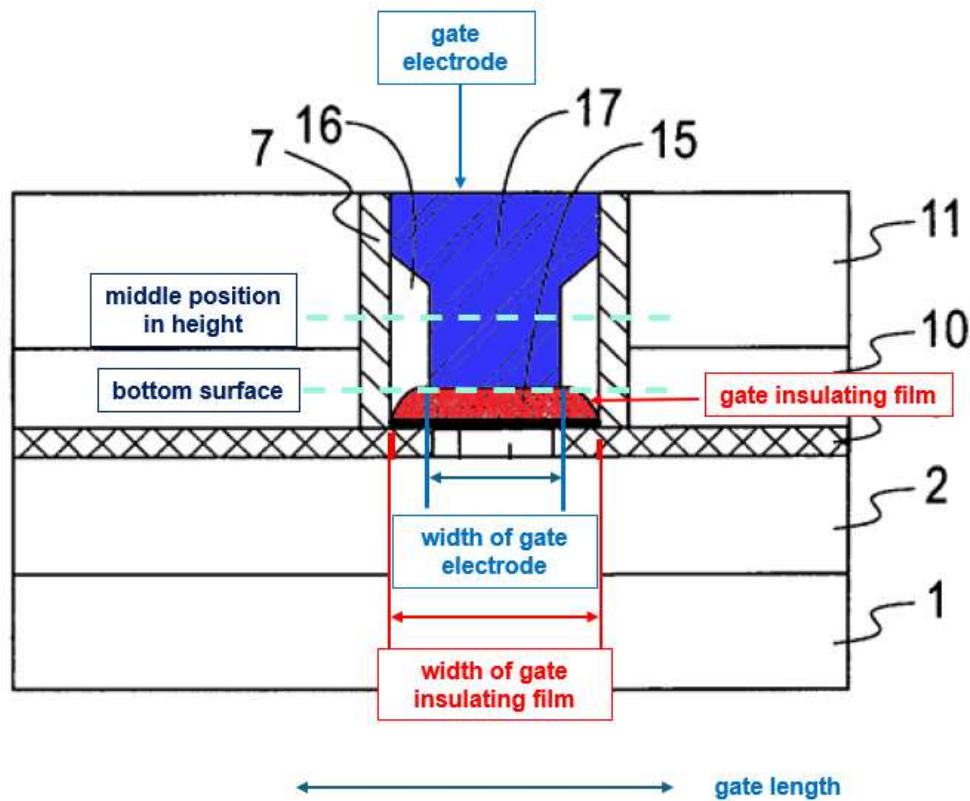
G. Dependent Claims 10 and 13

[10] *The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.*

[13] *The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.*

180. Guha discloses the limitations of claims 10 and 13. As shown in Figure 12, the width of the bottom surface of dielectric layer 15 (shaded red) is larger than the width of the bottom surface of the gate electrode (shaded blue), thereby meeting the limitation of claim 10. (TSMC-1028, ¶¶41, 43-45 (describing formation of spacers 16 in the cavity followed by deposition of the gate electrode).)

181. The width of the gate electrode is the same at its middle position as at its bottom. Therefore, the width of the dielectric layer 15 is also larger than the width of the gate electrode at its middle.



Guha, Figure 12

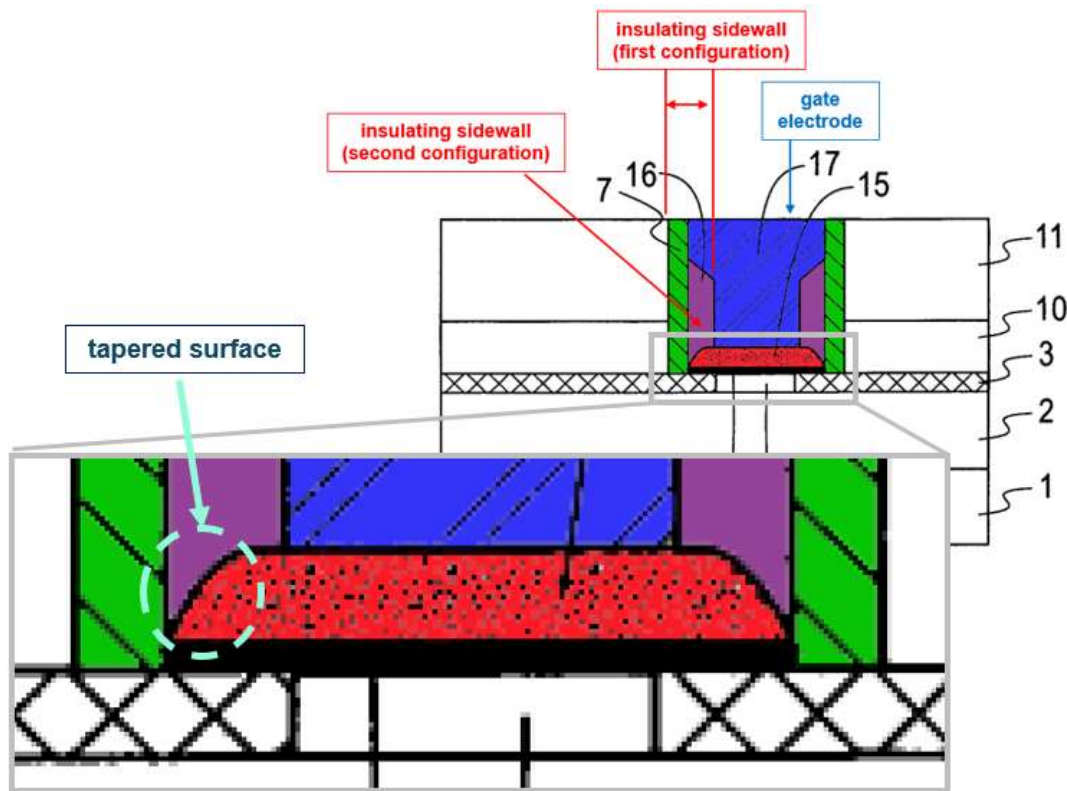
H. Dependent Claims 11-12

[11] *The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.*

[12] *The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.*

182. Guha discloses that in its device, “the edge where the dielectric layer 15 meets the isolating spacer structure 7 ... is **rounded** either upwards or **downwards** (e.g., similar to a cusp).” (TSMC-1028, ¶43.) Figure 12 shows

example of a dielectric layer that is rounded downward where it meets the isolating structure 7.



Guha, Fig. 12 (annotated and enlarged)

183. As can be seen in Figure 12, the high-k dielectric layer is rounded (or put another way, tapers) downward such that its thickness becomes smaller towards its ends, and its smallest thickness is under spacer 16 where it meets spacer 7, and its largest thickness is toward the center under the gate electrode. Under both the first and second “*insulating sidewall*” configurations, Guha teaches that the “*end of the gate insulating film located under the insulating sidewall has a tapered surface,*” as recited by claim 11, and “*has a thickness which becomes*

smaller toward the end thereof,” as recited by claim 12, because the end of the gate insulating film 15 under spacer 16 is rounded, or tapers, downward under the insulating sidewall. The tapered end portion of dielectric layer 15 is “*located under the insulating sidewall*” in the both first configuration (**spacers 16** and spacers 7 collectively) and second configuration (**spacers 16**). Accordingly, Guha teaches the limitation of claims 11 and 12.

IX. GROUND 5: Combination of Guha and Koyama Renders Claim 4 Obvious.

[4] *The semiconductor device of claim 1, wherein the gate insulating film is formed of a HfSiON film.*

184. Guha describes use of “**hafnium silicate**” as a high-k gate dielectric (TSMC-1028, ¶38) but does not expressly disclose use of “*a HfSiON film.*” Koyama provides this teaching, as discussed above with regard to Ground 2, and thus the combination of Koyama and Guha renders this claim obvious. As I noted above, Koyama’s study relates to semiconductor devices (TSMC-1029, Title); it is therefore in the same field as Guha and the ’076 patent. (TSMC-1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1028, ¶1 (“The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device.”).)

185. A POSITA would have been motivated to apply Koyama's teachings regarding use of HfSiON as a high-k gate dielectric to Guha's Figure 12 device. Guha motivates the above combination indicating that high-k dielectric materials were "not limited to" the materials on Guha's list of examples. (TSMC-1028, ¶38.) A POSITA would have known that in addition to hafnium oxide and hafnium silicate, which were explicitly listed by Guha, other materials could be used too. A POSITA would have also known that nitrided materials could also be used as high-k gate insulating films. A POSITA would thus have been motivated to investigate other hafnium silicate options and would have been led to Koyama. A POSITA would have been motivated to make the above combination to achieve the enhanced benefits of HfSiON high-k film, e.g., improved thermal stability and electrical characteristics, described by Koyama and discussed above with regard to Ground 2.

186. As discussed above with regard to Ground 2, such a combination would have been nothing more than the use of a known technique (Koyama's use of HfSiON as a high-k gate insulating film) to improve similar devices (Guha's transistor having a hafnium based high-k gate insulating film) in the same way. A POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable.

X. GROUND 6: Combination of Guha and Sim Renders Claim 6 Obvious.

[6] *The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.*

187. Guha teaches use of “hafnium oxide” as a high-k gate dielectric film (TSMC-1028, ¶38) but does not expressly disclose that the part of the gate insulating film located under the insulating sidewall has a thickness is “2 nm or less.” Sim provides this teaching, as discussed above with regard to Ground 3. Accordingly, the combination of Guha and Sim renders claim 6 obvious. As I noted above, Sim relates to semiconductor devices (TSMC-1024, Abstract), so it is in the same field as Guha and the ’076 patent. (TSMC-1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1028, ¶1 (“The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device.”).)

188. Sim, titled “Effects of ALD HfO₂ Thickness on Charge Trapping and Mobility,” was published on June 17, 2005. Sim explicitly describes use of a gate insulating film having a thickness 2 nm or less. Specifically, Sim explains that “[h]afnium-based high-k dielectrics and metal gate electrodes have been aggressively investigated to ensure continued scaling of CMOS technology, but several drawbacks such as low mobility and charge trapping have been identified.”

(TSMC-1024, 218.) Sim's authors set out to examine and address these drawbacks by testing films of different thickness, and "systematically evaluat[ing] the effects of high-k film thickness on charge trapping and channel carrier mobility." They found that "scaling the high-k dielectric is a simple, but very effective means of improving mobility and other reliability characteristics," and "[e]ven within 100 μ s, a 33Å HfO₂ sample shows significant current reduction while a 18Å HfO₂ sample is free from transient charging within the detection limits." (TSMC-1024, 218-219.) Specifically, Sim concluded that "[s]caling the physical thickness of the HfO₂ dielectric to below 20Å causes less charge trapping and higher mobility." (TSMC-1024, 221.) 20Å is equal to 2 nm, as recited by claim 6.

189. Applying Sim's teaching to Guha's yields a device where the high-k gate insulating film is less than 2 nm, as recited by claim 6. This is especially true since the thickness of the high-k film in Guha's device is even smaller at the ends (because the high-k film is rounded downward) than under the gate electrode. Thus, the devices resulting from the combination of Guha and Sim provides that "*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.*"

190. A POSITA would have been motivated to adopt Sim's solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less to Guha's Figure 12 device. Guha discloses the use of hafnium oxide as an example of a

high-k gate dielectric, the same film studied in Sim. Sim teaches reducing the thickness of hafnium oxide to below 20Å enhances mobility and reduces charge trapping, which ensures the performance and scalability of semiconductor devices. (TSMC-1024, 219, 221.) Such improvements align with the continued desire to make transistors smaller and more reliable, which both Guha and Sim emphasize as goals. (TSMC-1028, ¶2; TSMC-1024, 218.)

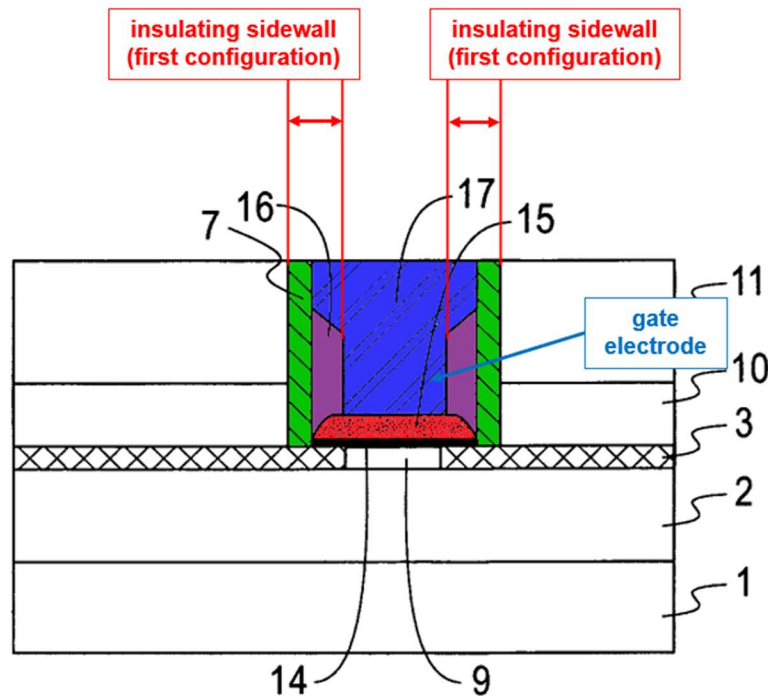
191. The aforementioned combination would have been nothing more than the use of a known technique (Sim’s HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices (Guha’s semiconductor device having a hafnium oxide gate dielectric), in the same way. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Sim uses a well-known process, atomic layer deposition (ALD), for fabricating high-k films. (TSMC-1024, 218; TSMC-1032, 17-19.)

XI. GROUND 7: Combination of Guha and Ahmed Renders Claim 9 Obvious.

[9] *The semiconductor device of claim 1, wherein the insulating sidewall has a triple layer structure including a first oxide film, a nitride film, and a second oxide film.*

192. As discussed above with regard to limitation [1C] and claim 8, Guha’s device includes gate spacer 16 and isolating spacer 7 (together the “*insulating sidewall*” in the first configuration). Guha’s insulating sidewall is shown in Figure

12, annotated below. Guha does not expressly disclose “*the insulating sidewall has a triple layer structure including a first oxide film, a nitride film and a second oxide film*” [9]. Ahmed, discussed in greater detail below, provides this teaching, such that the combination of Guha and Ahmed renders claim 9 obvious.

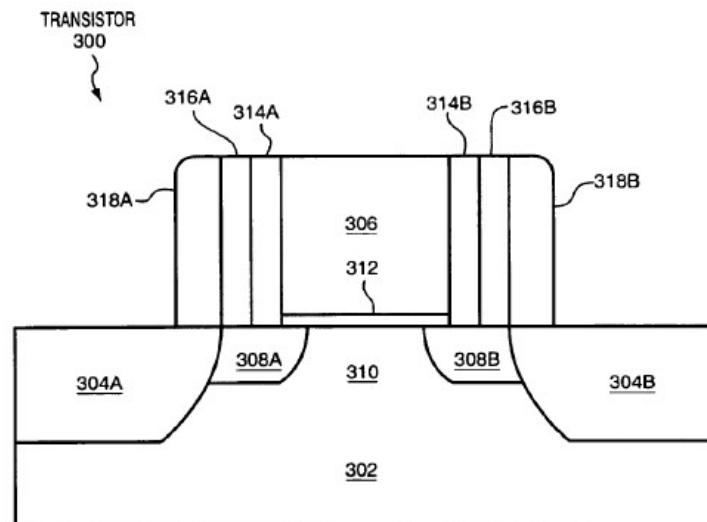


Guha, Figure 12

193. U.S. Patent 6,911,695, titled “Transistor Having Insulating Spacers on Gate Sidewalls to Reduce Overlap Between the Gate and Doped Extension Regions of the Source and Drain,” to Ahmed, et al. (“Ahmed”; TSMC-1031), was filed on September 19, 2002, and issued June 28, 2005.

194. As its title suggests, Ahmed is directed at a transistor comprising a gate, a channel beneath the gate and separate from the gate by an insulator, and

insulating spacers adjacent to the sidewalls of the gate that overlap the extension regions. (TSMC-1031, Abstract). Ahmed, directed to semiconductor devices, is in the same field as Guha and the '076 patent. (TSMC-1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1028, ¶1 (“The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device.”). An example of Ahmed’s transistor is shown in Figure 3, below.



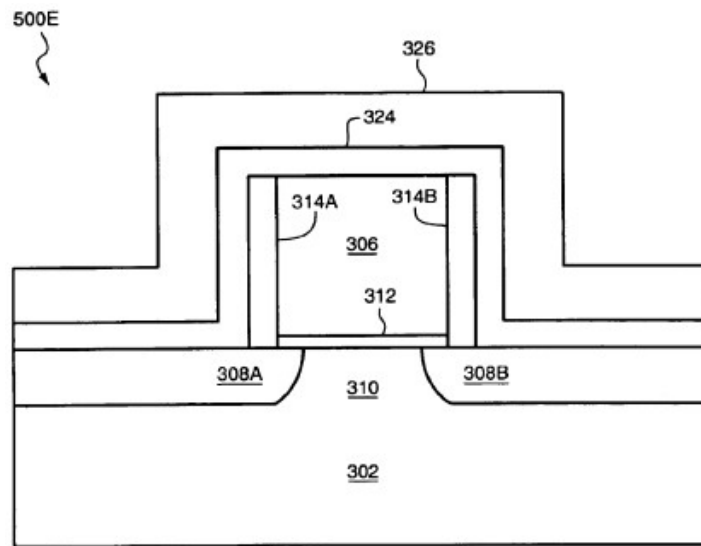
Ahmed, Figure 3

195. As can be seen in Figure 3, Ahmed’s transistor includes a triple layer sidewall: (1) insulating spacers 314A/B “adjacent and ... abutting sidewalls of the gate ... to offset the extension regions from the gate,” (2) source/drain spacers 316A/B “to offset the source/drain terminals from the gate,” and (3) source/drain

spacer liners 316A/B “disposed between and separating the source/drain spacers 318A/B and the insulating spacers 314A/B.” (TSMC-1031, 4:9-17.) Ahmed discloses examples wherein spacer 314A/B is an oxide film (TSMC-1031, 9:39-57, 10:55-60), spacer 316A/B is an oxide film (TSMC-1031, 12:59-13:6), and spacer 318A/B is a nitride film (TSMC-1031, 13:35-51, 13:61-66).

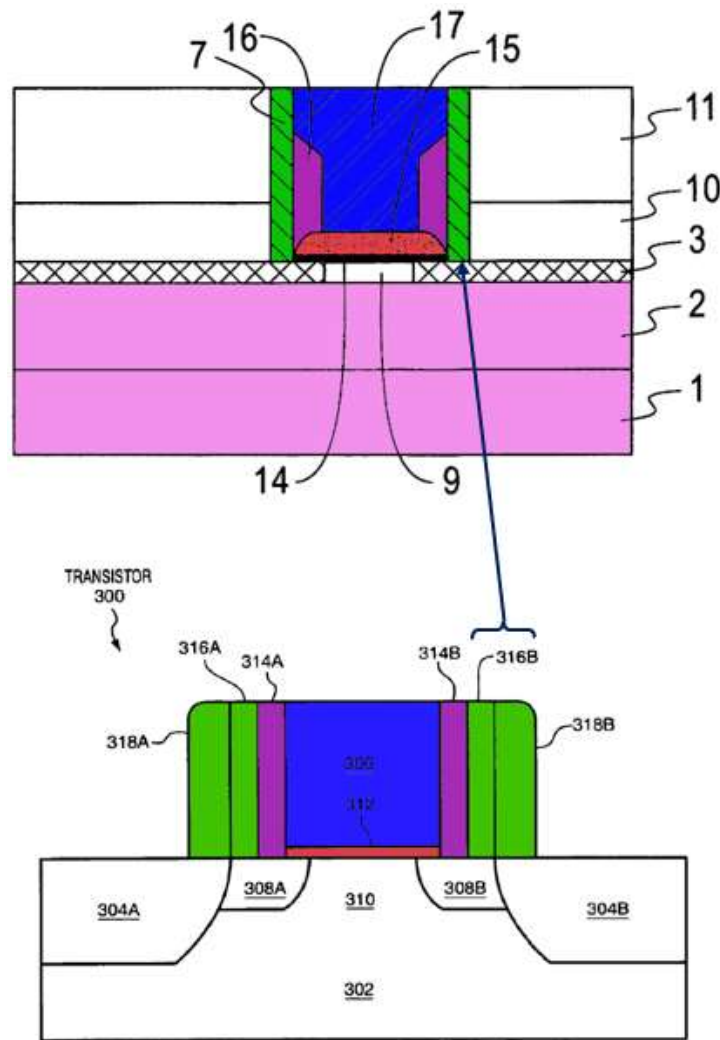
196. According to Ahmed, using a middle layer (spacer 316) in a sidewall structure provides multiple benefits, including “serv[ing] as an etch stop for a subsequent etch to form the source/drain spacers and thereby help protect the underlying materials.” (TSMC-1031, 12:53-58.) This is shown in Figure 3 (above). Figure 5E (below) also shows how layer 324 (which is etched to form spacer 316 (TSMC-1031, 13:61-66)) provides coverage for the underlying materials, including source/drain regions 308A/B.¹⁰

¹⁰ Based on the deposition of layers depicted in Figure 5E before the formation of spacers 316 and 318, a POSITA would have understood spacer 316 to be formed in an L-shape, though it is not depicted as such in Ahmed’s Figure 3.



Ahmed, Fig. 5E

197. A POSITA would have been motivated to apply Ahmed's teachings of a triple layer sidewall structure, including an intermediate oxide layer between oxide and nitride layers, to Guha's insulating sidewall structure comprising spacers 16 and 7, as shown below. Specifically, a POSITA would have been motivated to replace Guha's spacer 7 with Ahmed's spacers 316 (an oxide) and 318 (a nitride) before forming spacer 16. This combination leverages Ahmed's intermediate oxide spacer to provide both structural stability and functional benefits, such as enhanced adhesion and additional etch protection, complementing Guha's insulating sidewall design. The resulting device comprises an oxide layer (Guha's spacer 16), an oxide layer (Ahmed's spacer 316), and a nitride layer (Ahmed's spacer 318), resulting in an "insulating sidewall" with "a triple layer structure including a first oxide film, a nitride film and a second oxide film" such as illustrated below.



Guha, Fig. 12 (top); Ahmed, Fig. 3 (bottom) (annotated)

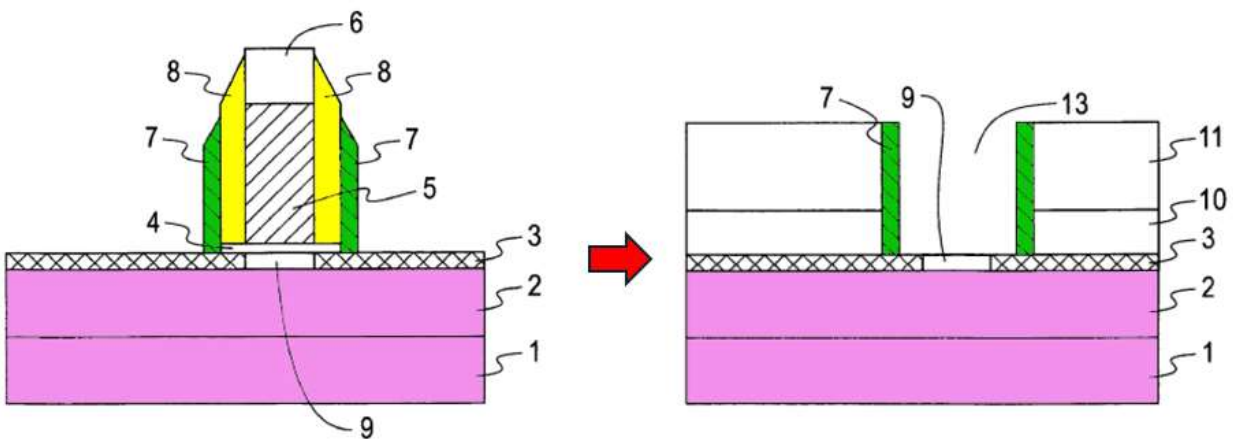
198. **Motivation to Combine.** A POSITA would have been motivated to combine Guha and Ahmed in the manner described above. Ahmed explicitly states that the oxide layer improves etch protection and adhesiveness, while the nitride layer seals and protects the gate. Guha's suggestion to use multiple insulating materials naturally aligns with Ahmed's specific implementation, making this combination logical and predictable.

199. Guha already teaches that isolating spacer 7 can include two materials: spacer 7 “can be composed of any insulating material including, for example, an oxide, nitride, oxynitride **or any combination thereof.**” (TSMC-1028, ¶28.) A POSITA would have known forming two discrete layers, as taught by Ahmed’s oxide spacer 316 and nitride spacer 318, best utilizes the distinct properties of two materials. Thus, Guha suggests using discrete layers for spacer 7’s multiple materials.

200. Guha also explains that isolating spacer 7 aids in the manufacturing process for its device. To fabricate Guha’s device, dummy spacers 8 (shaded yellow) are formed “adjacent to the dummy gate 5, extending from the pad protection layer 4 (which is an oxide (TSMC-1028, ¶24)) up to the dummy gate hard mask 6.” (TSMC-1028, ¶27, Figure 3.) Isolating spacer 7 (shaded green) is then “formed flanking the dummy-gate spacers 8.”¹¹ (TSMC-1028, ¶28.) After the source/drain contacts 10 are formed, “dummy gate 5 is removed by etching” and “dummy gate spacer 8 is removed, for example, using dilute HF, which also removes the pad protection layer 4,” leaving behind the structure of Figure 6.

¹¹ Pad protection layer 4 is partially etched before formation of isolation spacer structures 7 to arrive at the length depicted in Guha’s Figure 3. (See Guha, Figures 2, 3.)

(TSMC-1028, ¶¶33-34.) Gate-isolating layer 14, high-k dielectric layer 15, and gate spacers 16 are then formed as discussed above in Ground 4, claim 1. (TSMC-1028, ¶¶37-38, 43-44.)



Guha, Figs. 3 (left), 6 (right) (annotated)

201. Guha explains that because isolating spacer 7 is resistant to the etchant used to remove dummy-gate spacer 8, it serves “to protect the source/drain contacts 10 from the etchant used to remove the dummy gate spacer 8.” (TSMC-1028, ¶34.) A POSITA would have recognized that having isolating spacer 7 include an extra oxide layer, as taught by Ahmed, would have furthered Guha’s goal. By providing oxide spacer 316 before the outer nitride spacer (Guha’s spacer 7/Ahmed’s spacer 318), spacer 316 ensures protection of the source/drain contacts, as taught by Guha. Spacer 316 both provides an additional layer to protect the source/drain contacts and protects the outer nitride spacer from the etchant when

Guha's dummy-gate spacer 8 is removed,¹² further ensuring that the nitride layer protects the source/drain contacts during Guha's fabrication process. (TSMC-1031, 12:48-58, Figure 5E.) Providing an L-shaped oxide spacer 316 (see footnote 10, above) could further isolate Guha's outer nitride spacer 7 from the silicon substrate. This would help avoid known stresses arising at $\text{Si}_3\text{N}_4/\text{Si}$ interfaces that could induce device degradation (*see* TSMC-1050, ¶6) and also serve as an etch stop to protect Guha's underlying source/drain extensions 3a and 3b when etching a deposited nitride film to form the isolating nitride layer of Guha's spacer 7 (TSMC-1028, ¶28; TSMC-1031, 12:53-58.).

202. To go further, Ahmed also teaches that spacer 316 provides other benefits. For example, Ahmed's spacer 316 can "improve adhesiveness between the source/drain spacers and the insulating spacers" and "protect and seal the gate or gate dielectric." (TSMC-1031, 12:53-58.) In light of these known benefits and Guha's suggestion of using multiple materials (e.g., a combination of an oxide and

¹² A POSITA would have understood that in the combined device of Guha and Ahmed, different materials would be used to form spacer 316 (from Ahmed) and dummy-gate spacer 8 (from Guha) such that spacer 316 is not removed when dummy gate spacer 8 is removed. The selection of such materials would have been well within the knowledge of a POSITA by the time of the '076 patent.

a nitride) to form spacer 7, a POSITA would have been motivated to form Ahmed's spacers 316 (an oxide) and 318 (a nitride) in place of Guha's isolating spacer 7 (at least the exemplary embodiment wherein spacer 7 is only silicon nitride).

203. Applying Ahmed's triple layer spacer structure to Guha's device would have involved merely the use of a known technique (Ahmed's triple layer spacer structure) to improve similar devices (Guha's transistor, which already could include a triple-layer spacer) in the same way. A POSITA would have had a reasonable expectation of success combining Ahmed and Guha in the manner discussed above due to the predictable nature of the methods used for forming spacers in both patents. Both Guha and Ahmed use conventional methods for forming spacers involving depositing films followed by etching. (TSMC-1031, 7:45-48, 9:34-10:38, 13:7-51; TSMC-1028, ¶40.) In forming the combined structure, a POSITA would have formed Guha's isolating spacer 7 as combination of an oxide layer (equivalent to Ahmed's spacer 316, on the side surface of Guha's dummy spacer 8) and a nitride layer (equivalent to Ahmed's spacer 318, on the side surface of the first oxide layer). The process steps of Guha then proceed in the same way described above with regard to forming Guha's spacer 16, the buffer and gate insulating films, and the gate electrode. This compatibility ensures that

Ahmed's triple-layer spacer structure can integrate seamlessly into Guha's device, maintaining fabrication simplicity while achieving the desired improvements.

XII. GROUND 8: Combination of Matsumoto and Yu Renders Claims 1-3, 7-10, 13 Obvious.

A. Overview of Matsumoto

204. U.S. Publication 2003/0025135, titled "Semiconductor Device and Method for Manufacturing Same," to Takuji Matsumoto, et al. ("Matsumoto"; TSMC-1009) was filed on July 11, 2002, claiming priority to a JP application filed on July 17, 2001, and was published on February 6, 2003.

205. Similar to the '076 patent, Matsumoto relates "to a semiconductor device" and more specifically to an improved MOSFET (Metal Oxide Semiconductor Field Effect Transistor), and methods for manufacturing the same. (TSMC-1009, Abstract, ¶2.) As discussed in detail below, Matsumoto teaches a MOSFET device designed to reduce parasitic capacitance and power consumption while enhancing operating speed and device stability. These objectives closely align with those of the '076 patent.

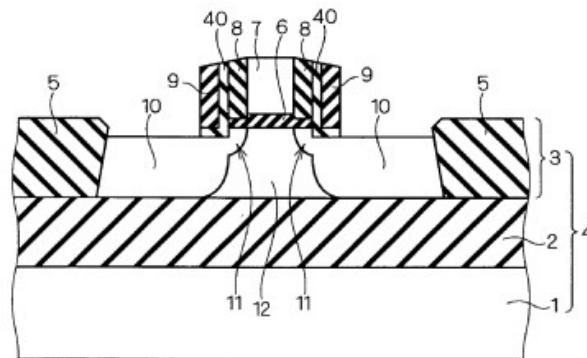
206. Matsumoto discloses several illustrative embodiments, and optional modifications of those embodiments, of a semiconductor device having a gate electrode, insulating sidewalls on the side of the gate electrode, and a gate insulating film that extends from under the gate electrode to the under the

insulating sidewalls.¹³ According to Matsumoto, the “increased base width of a parasitic bipolar transistor reduces the gain of the parasitic bipolar transistor,

¹³ Although Matsumoto discloses several embodiments and modifications, many of the fabrication steps are discussed in relation to the first embodiment. (*See, e.g.*, TSMC-1009, ¶123 (“The remaining structure of the semiconductor device according to the second preferred embodiment is similar to the corresponding structure of the above-stated semiconductor device according to the first preferred embodiment shown in FIG. 1.”), 137 (“Referring first to FIG. 18, the gate electrode 7 is formed by the process described in the first preferred embodiment....”).) Moreover, Matsumoto repeatedly explains, and a POSITA would have thus understood, that the teachings of one embodiment (or modification thereof) could be readily applied to other embodiments. (*See, e.g.*, TSMC-1009, ¶¶140 (“The technique of the fourth preferred embodiment is applicable to any one of the first to third preferred embodiments.”), 141 (“The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments.”), 143 (“The technique of the second modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments and the first modification of the fourth preferred embodiment.”).)

thereby to suppress malfunctions and operating characteristic variations of the MOSFET. Additionally, a decreased amount of overlap between the gate electrode and the extensions as viewed in plan suppresses a gate overlap capacitance to achieve the increase in operating speed and the reduction in power consumption.” (TSMC-1009, ¶15.)

207. As shown in Figure 22 below, Matsumoto's fourth embodiment includes a gate insulating film 6 extending from under the gate electrode 7 to under only the sidewall film 8. (*See* TSMC-1009, ¶¶138-140.)

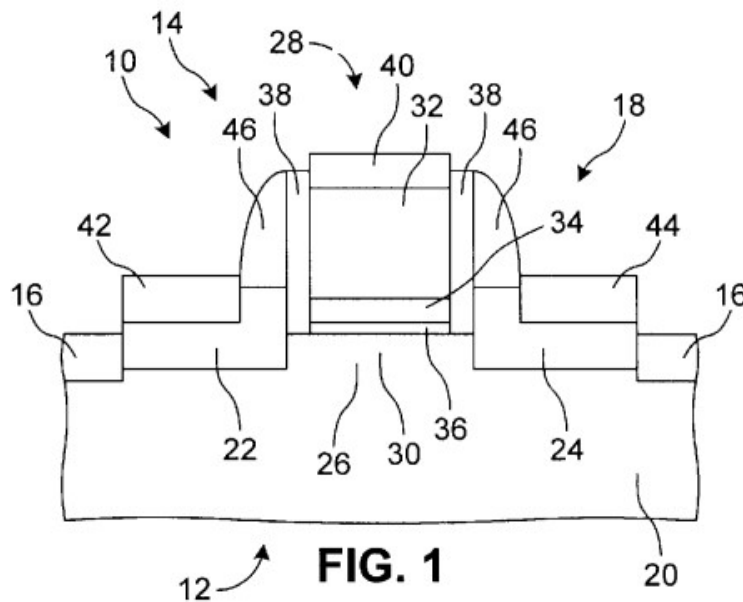


Matsumoto, Fig. 22

B. Overview of Yu

208. U.S. Patent 6,504,214, titled “MOSFET Device Having High-K Dielectric Layer,” to Bin Yu, et al. (“Yu”; TSMC-1048), was filed on January 11, 2002, and issued January 7, 2003.

209. As its title suggests, Yu discloses a MOSFET with a high-k gate dielectric separating the gate electrode from the semiconductor material. (TSMC-1048, Abstract.) An example of Yu's semiconductor device is shown below.



Yu, Fig. 1

210. Yu discloses that its semiconductor device includes buffer interface 36 between the semiconductor substrate 20 and high-k gate dielectric 34. (TSMC-1048, 3:59-62; Figure 1.) Yu's buffer interface 36 "can be a thin layer of oxide," such as "a layer of silicon oxide that is about 0.5 nm to about 0.7 nm thick." (TSMC-1048, 4:58-61; *see also* TSMC-1048, 3:62-63.) Yu discloses the benefits of having a buffer layer between the high-k gate insulating film and the substrate: "The buffer interface 36 acts to reduce diffusion and/or penetration of atoms from the high-K dielectric material into the layer of semiconductor material 20 that

could lead to a degradation in channel mobility. In addition, the buffer interface 36 may act to retard reaction of the high-K material with the layer of semiconductor material 20.” (TSMC-1048, 3:64-4:2.)

C. Motivation to Combine

211. A POSITA would have been motivated to make the combine two features of Yu with Matsumoto. Matsumoto and Yu are both directed to semiconductor devices and, thus, are in the same field as the '076 patent. (TSMC-1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”) TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”); TSMC-1048, Abstract (“A MOSFET device and method of fabrication.”).)

1. First Combination – Hafnium Based Oxide

212. First, A POSITA would have combined Yu with Matsumoto by utilizing a Hf based oxide, such as HfO₂, as the gate dielectric in Matsumoto’s device.

213. Matsumoto already provides a list of exemplary materials to use as its gate insulating film, including “a metal oxide film **such as** Al₂O₃ or a ferroelectric film such as Ta₂O₅ and BST.” (TSMC-1009, ¶107.) A POSITA would have understood these films to be high-k dielectrics. (*See, e.g.*, TSMC-1018, Table 1;

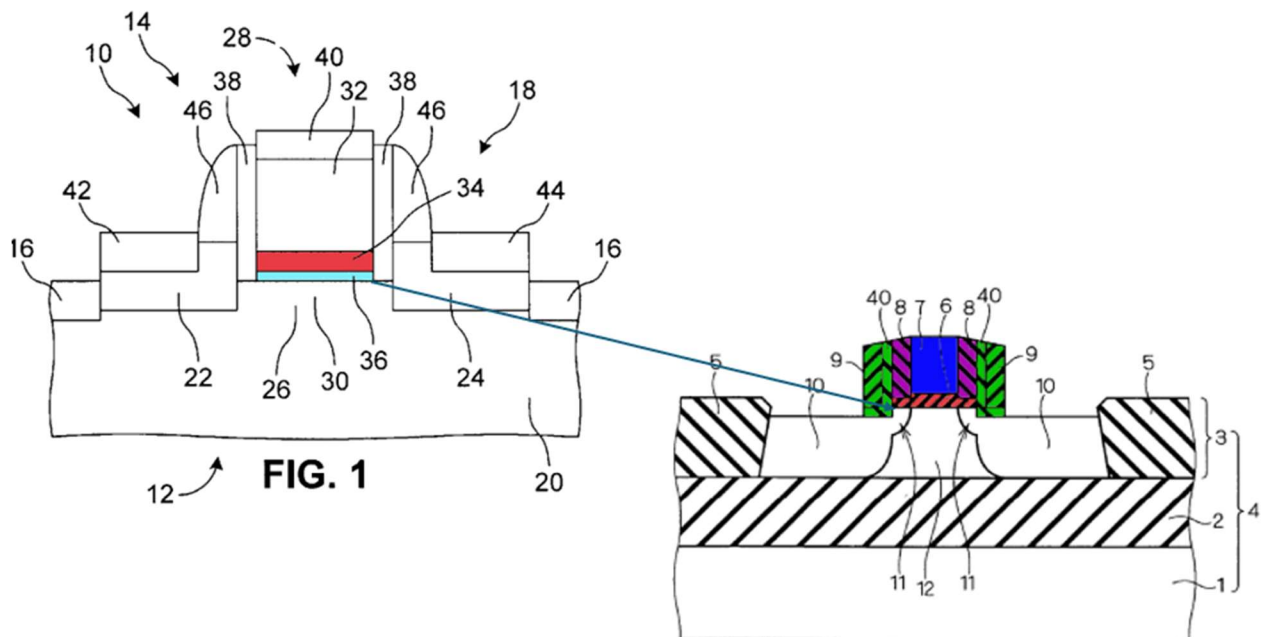
TSMC-1038, 88-89.) In addition to “aluminum oxide (e.g., Al_2O_3)” and “barium strontium titanate (BST)” as identified in Matsumoto, Yu teaches that its gate dielectric 34 may comprise “hafnium oxide (e.g., HfO_2),” which is another known high-k film. (TSMC-1048, 3:15-30; *see also* TSMC-1018, Table 1.)

214. **Motivation to Combine.** HfO_2 is a known high-k material with superior thermal stability and excellent electrical properties. Matsumoto explicitly seeks to improve the electrical characteristics of its gate insulating film, which aligns with Yu’s teaching of HfO_2 as a high-performance dielectric material. Thus, in my opinion, a POSITA would have been motivated to use a Hf-based oxide as a gate insulating layer, such as HfO_2 as taught by Yu, in Matsumoto’s device given HfO_2 ’s known benefits, e.g., “its superior thermal stability with poly-Si and reasonable band alignment.” (TSMC-1037, 2.4.1; *see also* TSMC-1032, 207 (HfO_2 “combines a high k (15–26) with a bandgap of 5.6 eV, with favourable conduction and valence band offsets with respect to Si ...”); TSMC-1049, 134 (“Excellent dielectric properties ... suggest that HfO_2 is a promising material for the future gate dielectric application.”).) HfO_2 also could be scaled down to a smaller EOT. (See TSMC-1032, 207.)

2. Second Combination – Buffer Layer

215. Second, a POSITA applying Yu's teachings to Matsumoto's device would have included a buffer interface layer between the high-k gate insulating film and the substrate, as taught by Yu.

216. For example, a POSITA would have included Yu's buffer interface 36 (shaded aqua), which "can be a layer of **silicon oxide**" (TSMC-1048, 4:58-61, 3:62-63), between the substrate and Matsumoto's high-k dielectric (shaded red) in the combined device, as illustrated below. As shown, Yu's buffer interface 36 is directly applicable to the structure of Matsumoto, fitting seamlessly between the substrate and the high-k dielectric layer, ensuring compatibility with Matsumoto's device configuration.



Yu, Fig. 1 (left); Matsumoto, Fig. 22 (right) (annotated)

217. **Motivation to Combine.** Yu's buffer layer aligns with Matsumoto's objective of reducing malfunctions and improving operational stability by mitigating adverse interactions between the high-k dielectric and the substrate. Thus, a POSITA would have been motivated to combine Matsumoto and Yu as discussed above. Yu explicitly states the motivation, teaching that the buffer interface (a) "acts to reduce diffusion and/or penetration of atoms from the high-K dielectric material into the layer of semiconductor material 20 that could lead to a degradation in channel mobility" and (b) "may act to retard reaction of the high-K material with the layer of semiconductor material 20." (TSMC-1048, 3:64-4:2; *see also* TSMC-1048, 4:65-67 ("The buffer interface material layer 62 assists in reducing integration issues that may arise when attempting form a layer of high-K material on a semiconductor layer."))

218. A POSITA would have been further motivated to combine Matsumoto and Yu, because Yu's teachings can be used along with Matsumoto's to further Matsumoto's goals. More specifically, one objective of Matsumoto is "to provide a semiconductor device which achieves reductions in malfunctions and operating characteristic variations." (TSMC-1009, ¶13.) Based on Yu's explanation of the benefits of a buffer layer, a POSITA would have been motivated to use Yu's buffer interface to improve channel mobility and performance of the combined device,

and thereby performance and reliability, of semiconductor devices such as the transistors disclosed by Matsumoto and Yu.

219. The predictable nature of Yu's buffer layer integration is further evidenced by its alignment with Matsumoto's existing process steps, such as forming a silicon oxide film via CVD or thermal oxidation. Yu explicitly teaches that a silicon oxide buffer reduces diffusion and interface defects in high-k films. (TSMC-1048, 3:64-4:2.) Given Matsumoto's disclosure of alternative high-k materials, a POSITA would have expected predictable improvements by implementing Yu's buffer design. Thus, combining Matsumoto and Yu in the manner described above would have involved nothing more than the use of a known technique (Yu's buffer interface) to improve similar devices (Matsumoto's transistor having a high-k gate dielectric) in the same way. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable because Yu provides instructions on conventional techniques to create buffer layers between the high-k gate dielectric film and the substrate. (TSMC-1048, 4:61-65 ("The buffer interface material layer 62 can be formed by a low temperature (about 500° C.) thermal oxidation process, a remote plasma deposition process, an atomic layer deposition (ALD) process or the like.").)

220. Matsumoto also discloses similar techniques for forming a layer of silicon oxide above the substrate. (TSMC-1009, ¶107 ("Next, a silicon oxide film

13 is formed entirely on the upper surface of the silicon layer 3 and the upper surface of the isolating insulation film 5 by a CVD process or a thermal oxidation process.”.) A POSITA wanting to include a buffer layer between the substrate and the high-k gate dielectric would have simply applied Matsumoto’s (or Yu’s) disclosure of forming a silicon oxide layer along with (and before) Matsumoto’s (or Yu’s) disclosure regarding using other high-k materials for the gate dielectric.

D. Independent Claim 1

1. Preamble [1P]

[1P] <i>A semiconductor device comprising:</i>
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221. The combination of Matsumoto and Yu discloses a “*semiconductor device*,” such as shown in Figure 22 of Matsumoto, above. Matsumoto is entitled “Semiconductor device and method of manufacturing same,” and discloses that “[t]he present invention relates to **a semiconductor device**.” (*See, e.g.*, TSMC-1009, ¶¶2, 102, 137; *see also* TSMC-1009, Abstract (“A semiconductor device ...”); TSMC-1048, 1:7-11.)

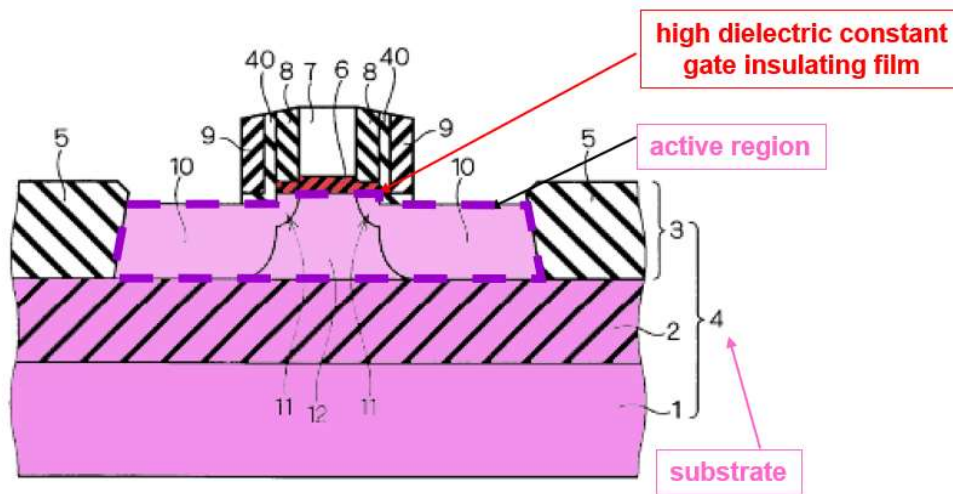
2. Limitation [1A]

[1A] <i>a gate insulating film formed on an active region in a substrate and including Hf;</i>
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222. The combination of Matsumoto and Yu provides “a gate insulating film formed on an active region in a substrate and including Hf” [1A].

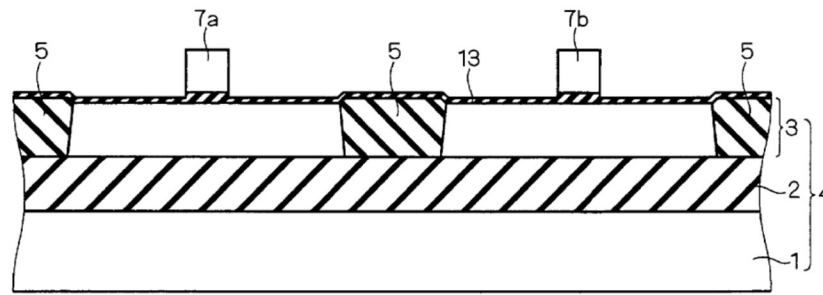
223. Matsumoto discloses a substrate, disclosing that its device has a multi-layer SOI **substrate** 4 (shaded pink) with silicon substrate 1, BOX layer 2 and single-crystalline silicon layer 3 “stacked in the order named.” (TSMC-1009, ¶102; *see also* TSMC-1009, ¶137 (relating process steps of first embodiment through forming gate electrode to fourth embodiment), ¶140 (relating fourth embodiment to first embodiment).)

224. Matsumoto also discloses *an active region* in a substrate, explaining that, for example, “isolating insulation film 5 extends from the upper surface of the silicon layer 3 to the upper surface of the BOX layer 2,” and that the “MOSFET is formed in a **device region** defined by the isolating insulation film 5.” (TSMC-1009, ¶¶102-03.) The device region, which is identified by isolation regions and includes source/drain regions 10, is an “*active region in a substrate*.” (TSMC-1009, ¶¶103-05, 139). This is consistent with the disclosure of the ’076 patent. (*See* TSMC-1001, 1:42-43 (“The region of the well 102 surrounded by the STI serves as an **active region** of a substrate 101”), 7:35-52 (active region includes source/drain regions surrounded by STI isolation structures).) The *active region* (outlined in magenta) *in a substrate* (shaded pink) is shown in Figure 22 (fourth embodiment) of Matsumoto, below.



Matsumoto, Fig. 22 (annotated)

225. A POSITA would have understood Matsumoto's film 6 to be the claimed gate insulating film. (TSMC-1009, ¶103 (referring to film 6 as a "gate insulation film").) In the fourth embodiment device of Matsumoto, "silicon oxide film 6 is formed partially on the upper surface of the silicon layer 3" in the device region and gate electrode 7 "is formed partially on the silicon oxide film 6." (TSMC-1009, ¶103 (first embodiment), ¶137 (in fourth embodiment, "gate electrode 7 is formed by the process described in the first embodiment").) This is done by forming film 13 on the substrate, as shown in Figure 4, below.



Matsumoto, Fig. 4

226. After one or more sidewalls are formed, film 13 is etched to form film 6. (See TSMC-1009, ¶138, Figures 18-19, 22.) Film 6 is therefore a “*gate insulating film formed on an active region in a substrate*” [1A].

227. As discussed above with regard to the “First Combination,” in the combination of Matsumoto and Yu, Matsumoto’s gate insulating film 6 is HfO_2 , as taught by Yu. (See also TSMC-1009, ¶107 (film 6 can be a high-k film); TSMC-1048, 3:15-30.) Accordingly, the device of the combination of Matsumoto and Yu provides “*a gate insulating film ... including Hf*” [1A].

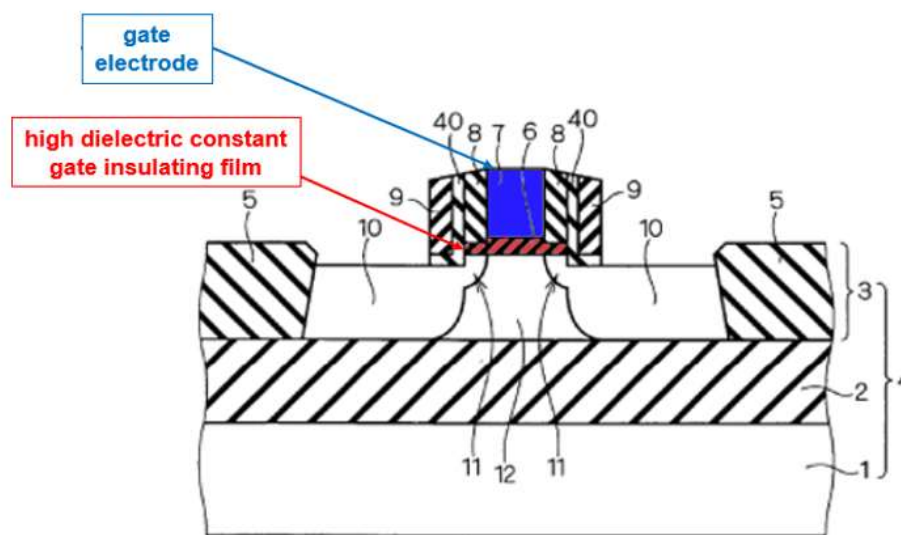
3. Limitation [1B]

[1B] <i>a gate electrode formed on the gate insulating film;</i>
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228. The combination of Matsumoto and Yu provides “*a gate electrode formed on the gate insulating film*” [1B].

229. In Matsumoto’s fourth embodiment device, “**gate electrode 7** made of polysilicon **is formed partially**” on insulating film 6. (TSMC-1009, ¶103 (first

embodiment), ¶107 (describing formation of high-k insulating film and gate electrode), ¶¶137-138 (in fourth embodiment, “gate electrode 7 is formed by the process described in the first embodiment”).) The gate electrode (shaded blue) is formed over the high dielectric constant gate insulating film (shaded red), as shown in Figure 22 of Matsumoto, below.



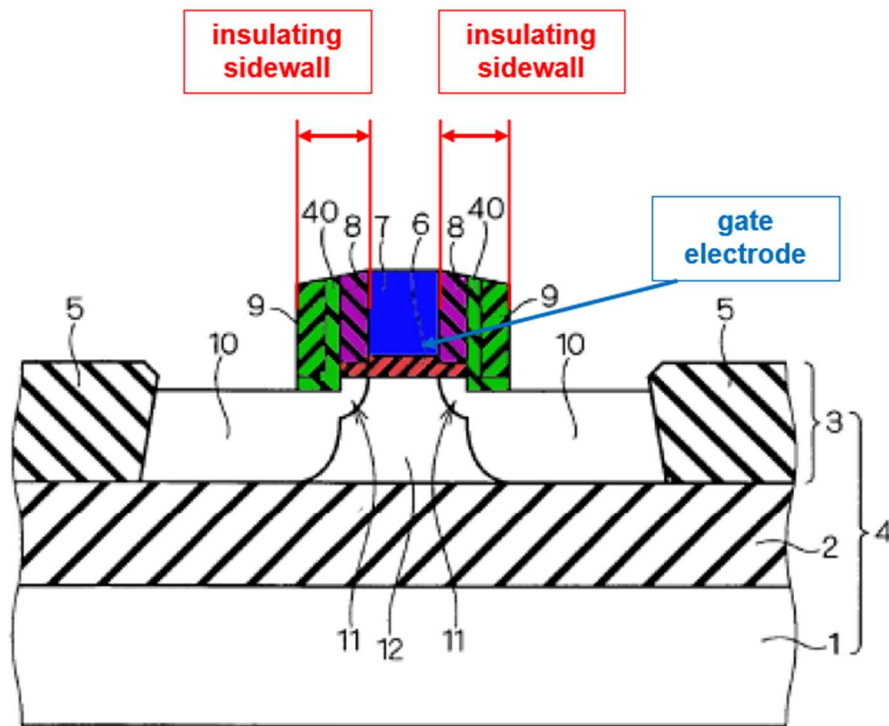
Matsumoto, Fig. 22 (annotated)

4. Limitation [1C]

[1C] *a insulating sidewall formed on each side surface of the gate electrode; and*

230. The combined Matsumoto and Yu device provides “*a insulating sidewall formed on each side surface of the gate electrode*” [1C].

231. In Matsumoto's fourth embodiment device, silicon oxide film 40 and silicon nitride film 9 are formed "on the outer side surfaces of" film 8. (See TSMC-1009, ¶139.) This is shown in Figure 22 below.



Matsumoto, Fig. 22 (annotated)

232. As shown in Figure 22, in Matsumoto's fourth embodiment, silicon oxide film 8, silicon oxide film 40, and silicon nitride film 9 are collectively "*an insulating sidewall formed on each side surface of the gate electrode*" [1C], consistent with the disclosures of the '076 patent.

233. A POSITA would have understood films 8, 40, and 9 to be the claimed insulating sidewall of limitation [1C]. Matsumoto expressly refers to film 9 as a "sidewall insulation film." (TSMC-1009, ¶114 (describing nitride films

9a/9b “serving as **sidewall** insulation films”).) Matsumoto, however, does not expressly refer to film 8 or film 40 as a sidewall. A POSITA would nevertheless have understood films 8 and 40 to be sidewalls as recited in the '076 patent.

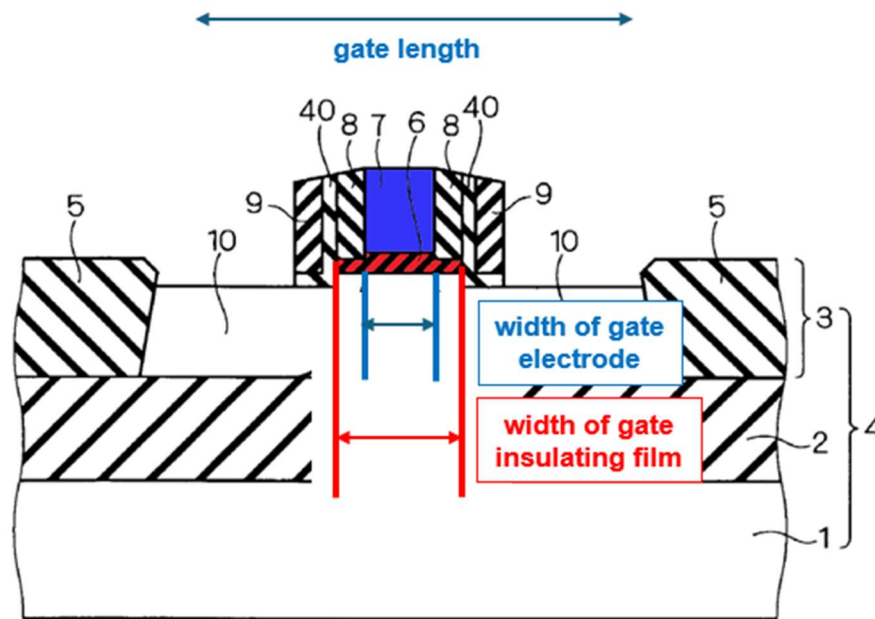
(TSMC-1009, ¶¶104, 110, 138 (“This forms the silicon oxide films 8 on the side surfaces of the gate electrode 7.”), 139 (“This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8.”), 40 (“the semiconductor device further includes a second sidewall formed on the side surface of the gate electrode, with the first sidewall therebetween”).) A POSITA also would have known that silicon oxide (for films 8 and 40) and silicon nitride (for film 9) are both insulators, and thus films 8, 40, and 9 make up the claimed “*insulating sidewall*.” Alternatively, a POSITA would have understood film 8 alone to be the claimed “*insulating sidewall*,” consistent with the disclosure of the '076 patent. (TSMC-1001, 6:9.)

5. Limitation [1D]

[1D] wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and
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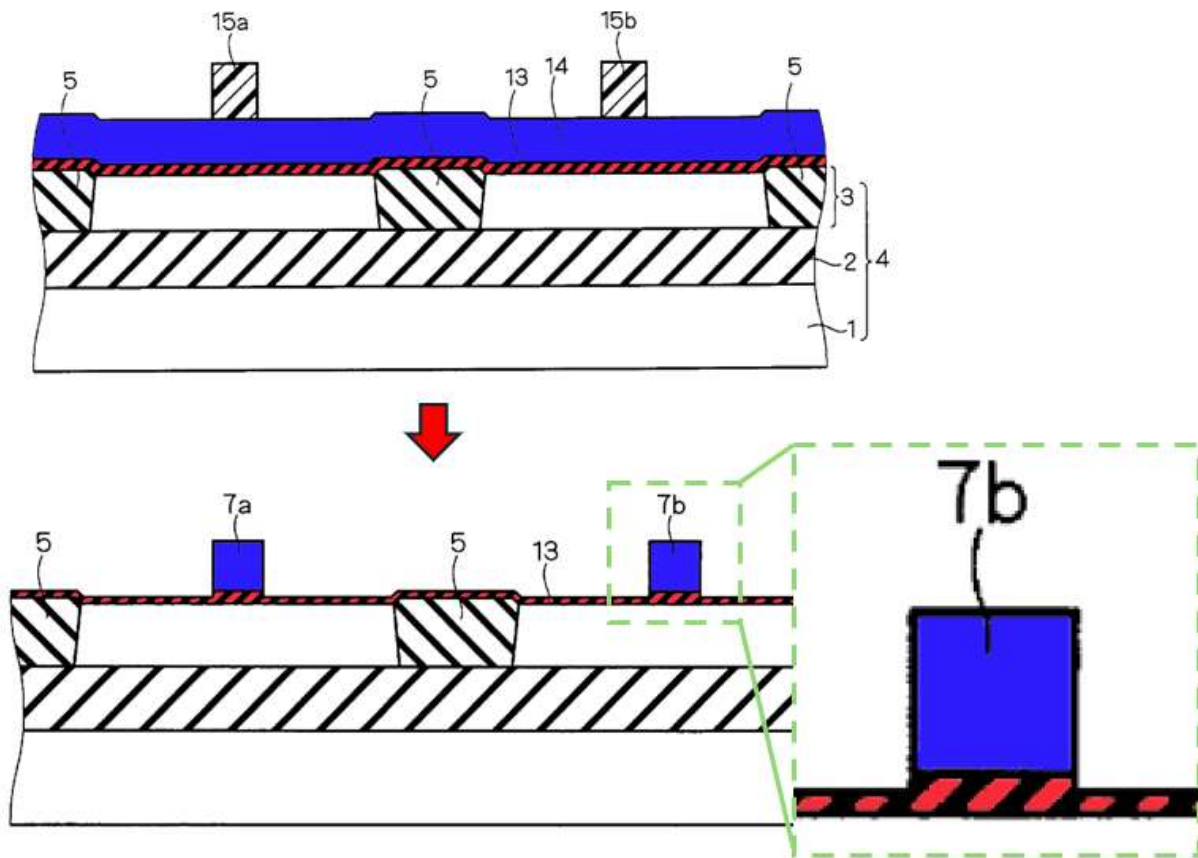
234. The combined Matsumoto and Yu device provides “*a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length*” [1D].

235. In Matsumoto's fourth embodiment device, the gate insulating film 6 (shaded red) extends from under the gate electrode 7 to under film 8 (part of the collective "*insulating sidewall*" comprising films 8, 40, and 9). Thus, the width of gate insulating film 6 (shaded red) along the gate length is larger than the width of gate electrode 7 (shaded blue). This is shown in Figure 22 below.



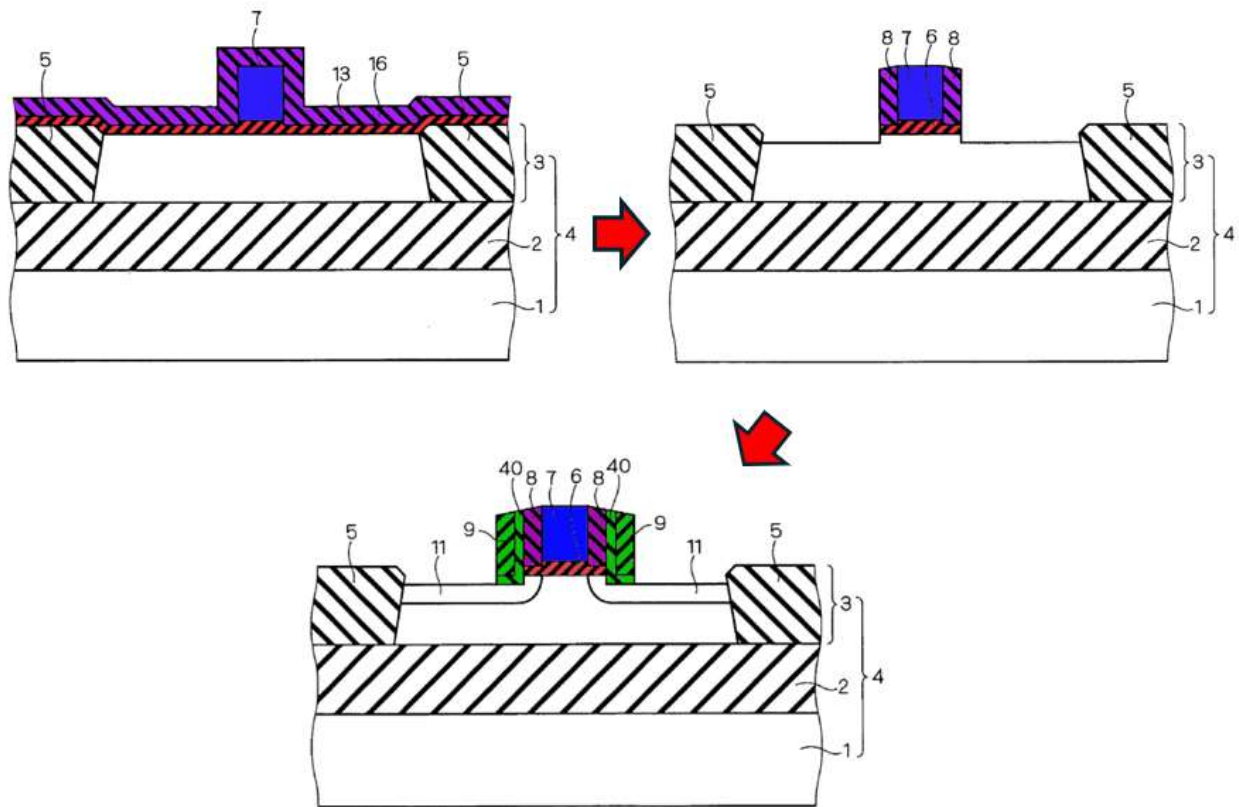
Matsumoto, Figure 22

236. Matsumoto's fabrication process confirms that the width of the gate insulating film is larger than that of the gate electrode. As shown in Figures 3-4, annotated below, the dielectric film 13 that forms the gate insulating film is formed continuously as one layer. (TSMC-1009, ¶107.)



Matsumoto, Figs. 3 (annotated top) and 4 (annotated and enlarged, bottom)

237. After formation of the gate electrode, sidewalls 8 are formed, as shown in Figures 18-19, below. (TSMC-1009, ¶138.) The etching process that forms films 8 (shaded purple) “is continued to overetch the upper surface of the silicon layer 3 exposed by the etching of the silicon oxide film 16.” (TSMC-1009, ¶138.) As shown in Figure 19, the high-k dielectric film (shaded red) remains only under the gate and sidewall film 8. Film 40 and film 9 (shaded green) are then formed on the outer side surfaces of film 8, as shown in Figure 21, below. (TSMC-1009, ¶139.)



Matsumoto, Figs. 18 (top-left), 19 (top-right), and 21 (bottom) (annotated)

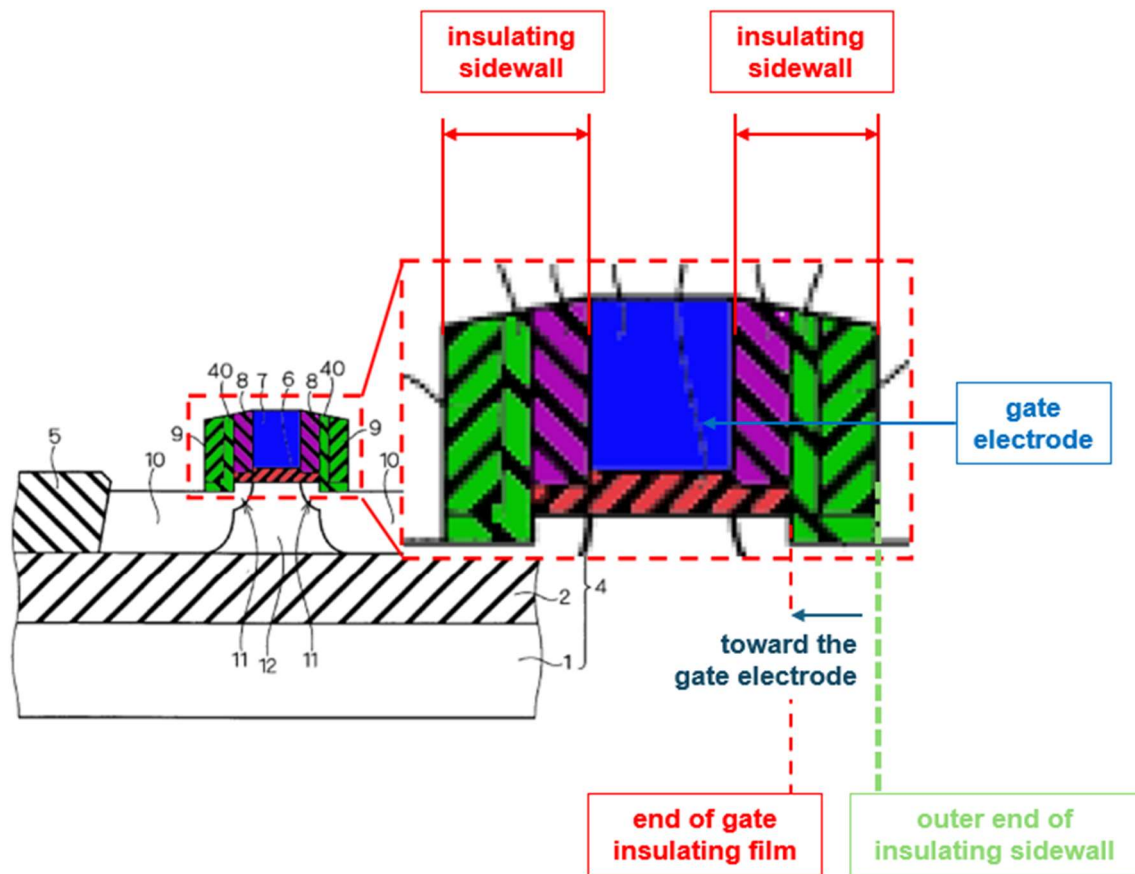
238. Because the high-k dielectric film 6 (shaded red) remains under the gate electrode 7 **and** part of the “*insulating sidewall*” (specifically, film 8) formed on the side surfaces of the gate electrode, the width of the gate insulating film is greater than the width of the gate electrode.

6. Limitation [1E]

[1E] *an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.*

239. The combined Matsumoto and Yu device includes “*an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode*” [1E].

240. As shown in Figure 22, below, the end of high-k gate insulating film 6 is perpendicular to the substrate’s surface, and disposed inward from the outer end of sidewall 9 (the outer end of the collective “*insulating sidewall*”) toward the gate electrode. Thus, the end of the gate insulating film is “*retracted from an outer end of the insulating sidewall toward the gate electrode*” [1E], at least under Patent Owner’s litigation allegation discussed above.



Matsumoto, Fig. 22 (annotated and enlarged)

E. Dependent Claim 2

[2] The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.

241. When Matsumoto and Yu are combined as described above, the combined device includes Yu's buffer interface 36, which Yu teaches "can be a layer of **silicon oxide** ... ," between the high-k dielectric and the substrate. (TSMC-1048, 4:58-61, 3:62-63.) Buffer interface 36 is therefore a "*buffer insulating film formed of a silicon oxide film.*"

F. Dependent Claim 3

[3] *The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide.*

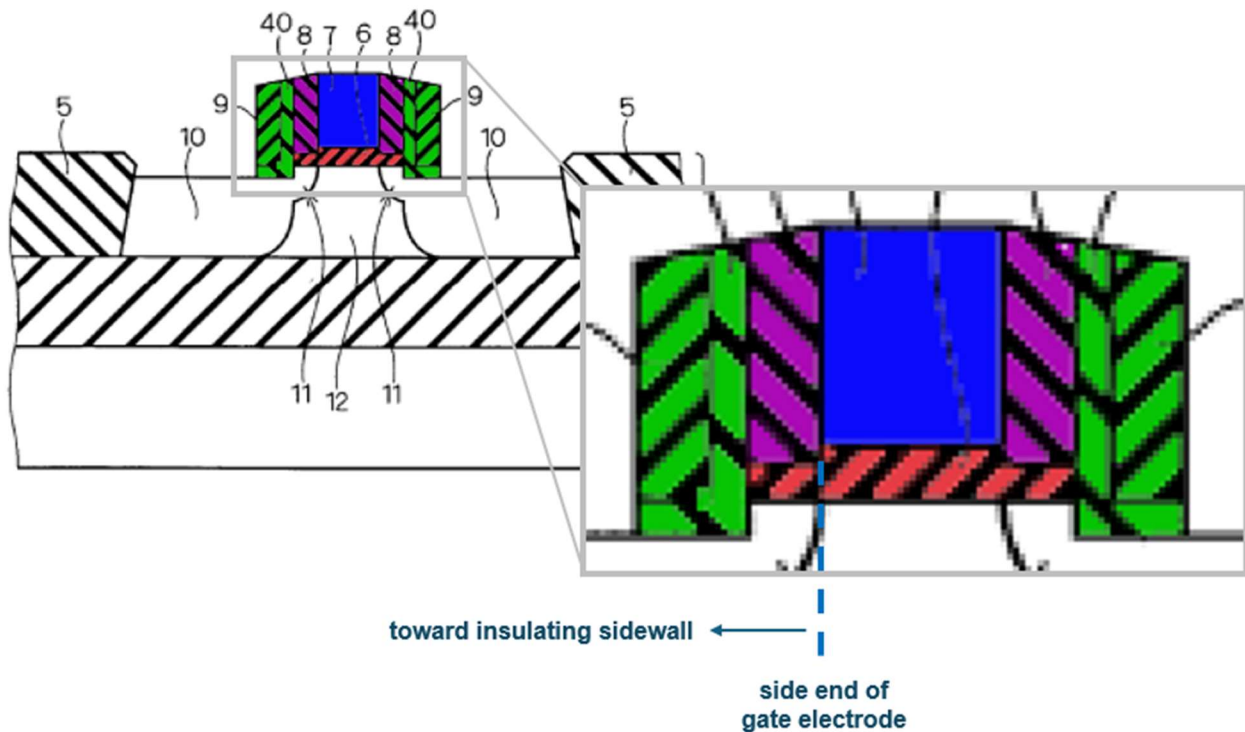
242. The combined Matsumoto and Yu device provides “*the gate insulating film is formed of a Hf based oxide*” [3]. Given Matsumoto’s explicit preference for high-k materials and the documented advantages of HfO₂, a POSITA would have viewed Yu’s teachings as a natural extension of Matsumoto’s disclosure. As discussed above with regard to limitation [1A], Yu teaches that its gate dielectric 34 may be formed of “hafnium oxide (e.g., HfO₂).” (TSMC-1048, 3:15-30.) The combination of Matsumoto and Yu thus would have resulted in a device where Matsumoto’s gate insulating film is formed of a Hf-based oxide—namely, HfO₂—as taught by Yu.

G. Dependent Claim 7

[7] *The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.*

243. The combined Matsumoto and Yu device provides “*an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall*” [7]. As discussed above with regard to limitation [1D], gate insulating film 6 (shaded red) extends (protrudes) from under the gate electrode 7 to under sidewall 8 (part of the collective “*insulating sidewall*” comprising films 8,

40, and 9). It thus “*protrudes from a side end of the gate electrode toward the insulating sidewall.*”



Matsumoto, Fig. 22 (annotated and enlarged)

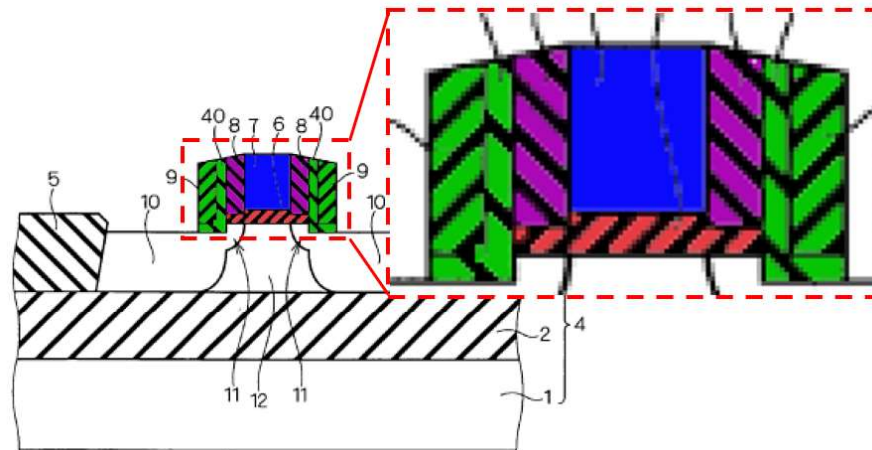
H. Dependent Claims 8-9

[8] *The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.*

[9] *The semiconductor device of claim 1, wherein the insulating sidewall has a triple layer structure including a first oxide film, a nitride film, and a second oxide film.*

244. As discussed above with regards to limitation [1C], Matsumoto’s fourth embodiment device includes an “*insulating sidewall*” comprising film 8

(shaded purple) and films 40 and 9 (together shaded green). This is shown, for example, in Figure 22 of Matsumoto.

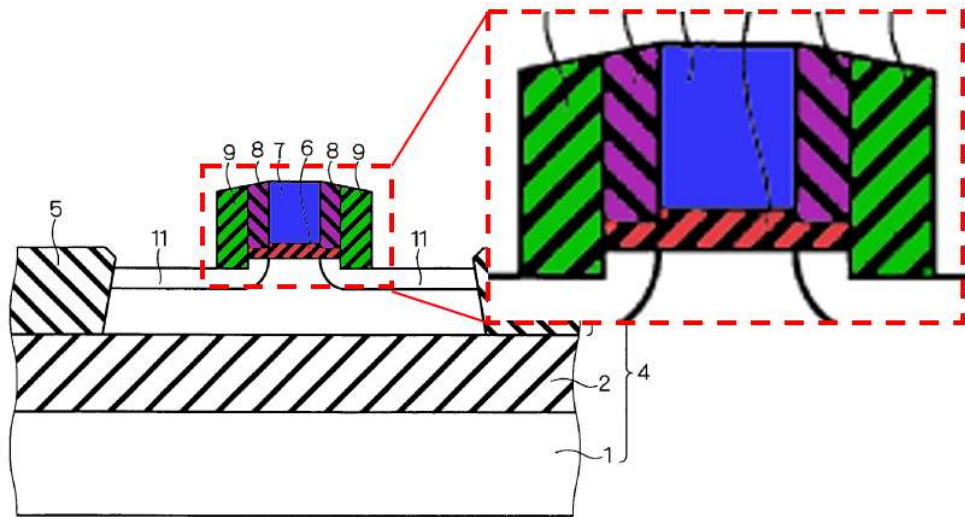


Matsumoto, Fig. 22 (annotated and enlarged)

245. Films 8 and 40, shown above, are silicon oxide and film 9 is silicon nitride. (See TSMC-1009, ¶139 (“This forms silicon oxide films 40 and the silicon nitride films 9 on the outer side surfaces of the silicon oxide films 8.”)). A POSITA would have considered each film to be a “layer” of the claimed insulating sidewall structure, consistent with the disclosures of the ’076 patent. (TSMC-1001, 21:6-15.) Matsumoto therefore teaches “*the insulating sidewall has a triple layer structure including a first oxide film [silicon oxide film 8], a nitride film [silicon nitride film 9] and a second oxide film [silicon oxide film 40],*” as recited by claim 9.

246. Claim 8 is similar to claim 9, but recites a double layer structure instead of a triple layer structure. Matsumoto discloses such an arrangement too.

For example, Matsumoto discloses a modification of the fourth embodiment that omits layer 40, such as shown in Figure 23, below.



Matsumoto, Fig. 23 (annotated and enlarged)

247. In this modification illustrated in Figure 23, after silicon oxide film 8 is formed, “silicon nitride films 9 are formed directly on the upper surface of the silicon layer 3.” (TSMC-1009, ¶141.) As before, a POSITA would have considered each film to be a “layer” of the claimed insulating sidewall structure, consistent with the disclosures of the ’076 patent. (TSMC-1001, 21:6-15.) Thus, Matsumoto’s modification to the fourth embodiment, as shown in Figure 23, discloses that “*the insulating sidewall*” (here, the collective structure of silicon oxide film 8 and

silicon nitride film 9) “*has a double layer structure including an oxide film and a nitride film,*” as recited by claim 8.¹⁴

I. Dependent Claims 10 and 13

[10] *The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.*

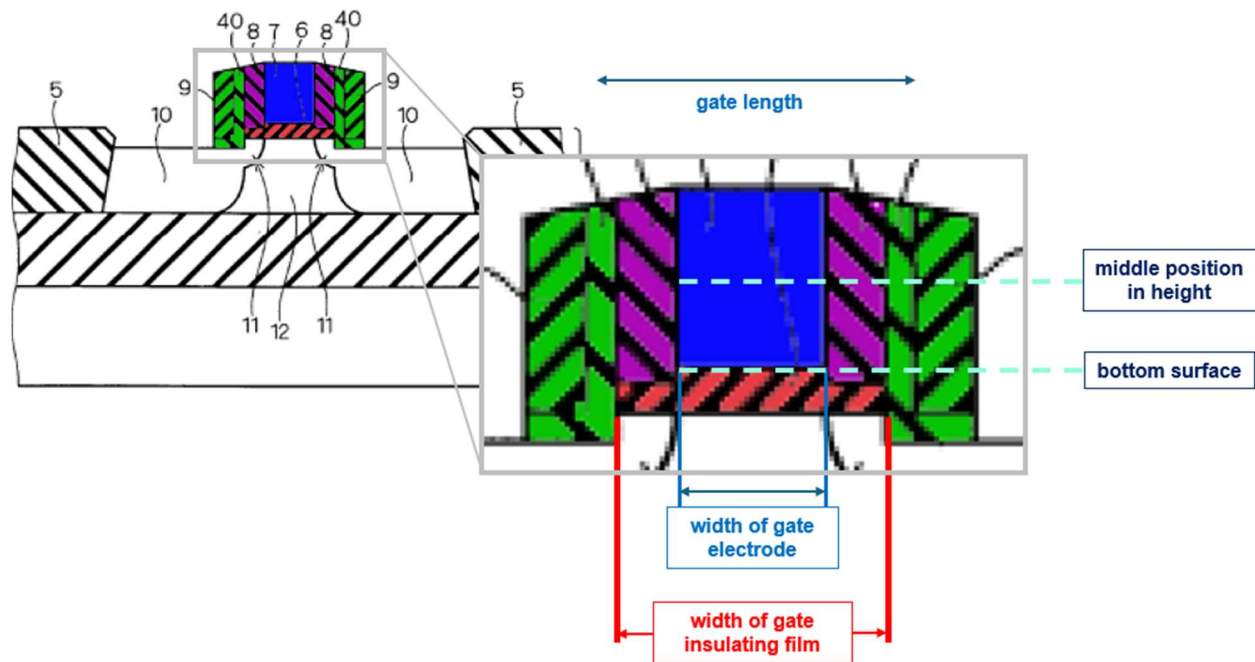
[13] *The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.*

248. The combined Matsumoto and Yu device provides that “*a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length*” [10] and “*the width*

¹⁴ Matsumoto explains this modification “is applicable to any one of the first to fourth preferred embodiment” and therefore the analysis of claim 1 in relation to Matsumoto’s fourth embodiment (Figure 22) applies equally to Figure 23. (TSMC-1009, ¶141 (“The technique of the first modification of the fourth preferred embodiment is applicable to any one of the first to fourth preferred embodiments.”).) A POSITA would have thus also understood that Matsumoto’s modification to the fourth embodiment, as shown in Figure 23, meets each limitation of claim 1.

of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length” [13].

249. As I explained above with regard to limitation [1D], the gate insulating film 6 of the combined device extends from under the gate electrode to under film 8, which is part of the collective “*insulating sidewall*” comprising films 8, 40, and 9. This can be seen in Matsumoto’s Figure 22, shown below.



Matsumoto, Fig. 22 (annotated and enlarged)

250. As can be seen in Figure 22, the width of Matsumoto’s gate electrode 7 is constant across its entire height. The width of the high-k gate insulating film 6 (shaded red), including at film 6’s bottom surface, is larger than the width of the gate electrode 7 (shaded blue), including at gate electrode 7’s bottom surface. The

fabrication process of Matsumoto's fourth embodiment, discussed above with regard to limitation [1D], confirms the structures shown in Figure 22.

XIII. GROUND 9: Combination of Matsumoto, Yu, and Sim Renders Claim 6 Obvious.

[6] *The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.*

251. The combined device of Matsumoto and Yu teaches every limitation of claim 1 but does not explicitly provide “*a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less*” [6]. As discussed above in Ground 3, Sim provides this teaching, and the combined device of Matsumoto, Yu, and Sim renders claim 6 obvious. As I noted above, Sim relates to semiconductor devices (TSMC-1024, Abstract), so it is in the same field as Matsumoto, Yu, and the '076 patent. (TSMC-1001, 1:18-19 (“The present invention relates to a semiconductor device and a method for fabricating the semiconductor device.”) TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”); TSMC-1048, Abstract (“A MOSFET device and method of fabrication.”).)

252. As discussed above with regard to the “First Combination” and limitation [1A], the combined device of Matsumoto and Yu uses a HfO₂ film as the high-k gate insulating film. Although neither Matsumoto nor Yu specifically discloses a HfO₂ film that is less than 2 nm thick, a POSITA would have

nonetheless been motivated to use a thickness of 2 nm or less in the combined device, as taught by Sim. The resulting device of the combination includes a Hf-based high-k gate dielectric having “*a thickness of 2 nm or less.*”

253. A POSITA would have been motivated to adopt Sim’s solution of forming a gate insulating film with a thickness of 20Å (2 nm) or less to the combined device of Matsumoto and Yu. Such a device already uses HfO₂ as an example of a high-k gate dielectric, which is the same film studied in Sim. Sim explicitly teaches that reducing the thickness of HfO₂ to below 20Å not only minimizes charge trapping but also enhances carrier mobility, directly addressing performance and scalability challenges in advanced semiconductor devices. (TSMC-1024, 218-19, 221.) Such improvements align with the continued desire to make transistors smaller and more reliable, which all of Matsumoto, Yu, and Sim emphasize as goals. (TSMC-1009, ¶13; TSMC-1048, 1:39-41; TSMC-1024, 218.) A POSITA would have recognized that Sim’s thinner HfO₂ film directly addresses the performance needs of the combined device of Matsumoto and Yu, including reduced leakage currents and improved device reliability, making it an obvious choice for integration.

254. The aforementioned combination would have been nothing more than the use of a known technique (Sim’s HfO₂ dielectric layer with less than 20Å thickness) to improve similar devices (the combined device of Matsumoto and Yu

having a hafnium oxide gate dielectric), in the same way (forming a high-k gate insulating film, with a smaller thickness). A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable, as Sim's use of well-established processes like atomic layer deposition (ALD) for fabricating thin HfO₂ films complements the fabrication techniques disclosed by Matsumoto and Yu, ensuring predictable and reproducible results in achieving the claimed thickness. (TSMC-1024, 218; TSMC-1032, 17-19; *see also* Matsumoto, ¶107 (disclosing that the gate insulating film is deposited "by a CVD process or a thermal oxidation process.").)

XIV. GROUND 10: Combination of Matsumoto and Koyama Renders Claims 1 and 4 Obvious.

[4] <i>The semiconductor device of claim 1, wherein the gate insulating film is formed of a HfSiON film.</i>

255. As discussed in connection with Ground 8 above, Matsumoto teaches each and every limitation of claim 1, but it does not expressly disclose "*a gate insulating film ... including Hf*" [1A] or that "*the gate insulating film is formed of a HfSiON film*" [4]. These features are taught by Koyama. As I noted above, Koyama's study relates to semiconductor devices (TSMC-1029, Title); it is therefore in the same field as Matsumoto and the '076 patent. (TSMC-1001, 1:18-19 ("The present invention relates to a semiconductor device and a method for

fabricating the semiconductor device.”) TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).)

256. In the combined device of Matsumoto’s fourth embodiment and Koyama, Matsumoto’s gate insulating film 6 comprises HfSiON, as taught by Koyama. The combination of Matsumoto and Koyama thus discloses “*a gate insulating film ... including Hf*” [1A] and that “*the gate insulating film is formed of a HfSiON film*” [4]. Accordingly, the disclosures of Matsumoto that I addressed in Ground 1, in combination with Koyama’s teaching of HfSiON as a gate insulating film, render obvious claims 1 and 4.

257. **Motivation to Combine.** As I discussed above in Ground 8, Matsumoto discloses a list of exemplary high-k films which can be used as a gate dielectric. Specifically, Matsumoto teaches that “[a] silicon oxynitride film, a metal oxide film such as Al₂O₃ or a ferroelectric film such as Ta₂O₅ and BST may be formed in place of the silicon oxide film 13.” (TSMC-1009, ¶107). Based on Matsumoto’s disclosure that the gate insulating film may be a silicon oxynitride film or a metal oxide film, a POSITA would have found it obvious to use HfSiON as the gate insulating film due to its compatibility with high-k applications and its well-known advantages, including thermal stability and reduced leakage.

258. Even if Matsumoto does not explicitly disclose HfSiON, a POSITA would have been motivated to investigate other hafnium-based options, such as

HfSiON, to use as the high-k gate insulating film. Koyama, discussed in greater detail above with regard to Ground 2, explicitly teaches the use of HfSiON as a high-k gate insulating material, providing a clear path for its integration into the Matsumoto fourth embodiment device. Thus, the combination of Koyama with Matsumoto also renders claims 1 and 4 obvious.

259. A POSITA would have been motivated to apply Koyama's teachings regarding use of HfSiON as a high-k gate dielectric to the fourth embodiment device of Matsumoto. Matsumoto motivates the combination by describing possible materials for the high-k gate insulating film that include HfSiON. A POSITA would have known that, in addition to hafnium oxide and hafnium silicate, other materials could be used too. A POSITA would have also known that nitrided materials could also be used as high-k gate insulating films. A POSITA would thus have been motivated to investigate other hafnium options and would have been led to Koyama. A POSITA would have been motivated to make the above combination to achieve the enhanced benefits of HfSiON high-k film, e.g., improved thermal stability and electrical characteristics, described by Koyama and discussed above with regard to Ground 2. Koyama emphasizes HfSiON's advantages in enhancing dielectric performance, including reducing defects at the interface and suppressing oxygen diffusion, making it an attractive candidate for

integration into Matsumoto's device, where its properties would align with Matsumoto's high-k material to improve device performance.

260. As discussed above with regard to Ground 2, such a combination would have been nothing more than the use of a known technique (Koyama's use of HfSiON as a high-k gate insulating film) to improve similar devices (Matsumoto's transistor having a high-k gate insulating film) in the same way. By leveraging Koyama's explicit guidance on HfSiON's enhanced thermal stability and its ability to minimize electron trapping, a POSITA would have had confidence in achieving the desired performance improvements in Matsumoto's fourth embodiment device. A POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable.

XV. GROUND 11: Combination of Matsumoto and Ono Renders Claims 1, 5, and 11-12 Obvious.

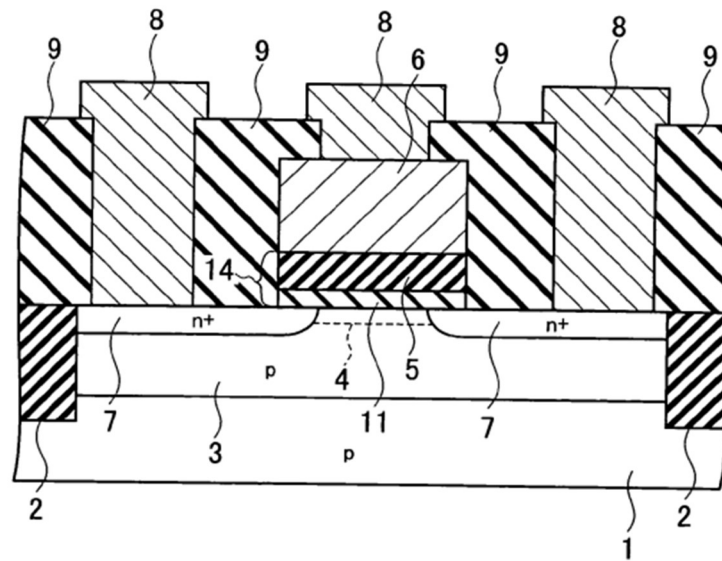
A. Overview of Ono

261. U.S. Publication 2005/0051856, titled "Semiconductor Device," to Mizuki Ono, et al. ("Ono"; TSMC-1013), was filed July 2, 2004, claiming priority to a JP application filed September 4, 2003, and published on March 10, 2005. As its name suggest, Ono relates to semiconductor devices, including, specifically field effect transistors. (TSMC-1013, Abstract, ¶¶3-7.) Ono is therefore in the same field as Matsumoto and the '076 patent. (TSMC-1001, 1:18-19 ("The present

invention relates to a semiconductor device and a method for fabricating the semiconductor device.”); TSMC-1009, ¶2 (“The present invention relates to a semiconductor device and a method of manufacturing the same.”).)

262. Ono discloses two base embodiments of a semiconductor device with multiple modifications applicable to each. Both embodiments include a semiconductor substrate, source and drain regions arranged at the surface of the semiconductor substrate, a gate insulator film on the substrate, and a gate electrode on the gate insulator film. (TSMC-1013, ¶¶8-9.) In this Declaration, I will focus on Ono’s second embodiment and the modifications thereto.

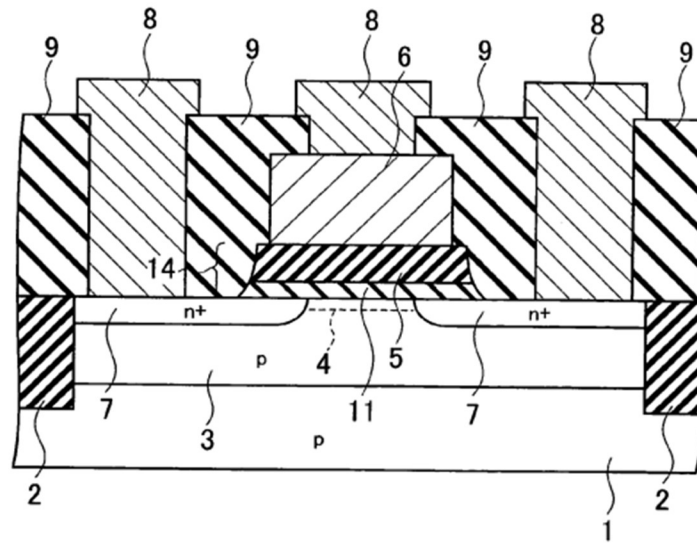
263. An example of Ono’s second embodiment is illustrated in Figure 77, below. As shown in this figure, Ono’s semiconductor device includes a gate stack comprising gate insulator film 11 and gate insulator film 5 made of “HfO₂ film.” (TSMC-1013, ¶¶207, 209, Figure 77.) Gate electrode 6 is formed on gate insulator film 5, as shown in Figure 77 below, and can be provided with gate sidewalls. (TSMC-1013, ¶¶207, 181 (in the first embodiment, “gate sidewalls are not mentioned; however, sidewalls may be provided to the gate electrode”), 210 (“Various modifications as described in the first embodiment are also possible with this [second] embodiment, and the same effects may be obtained.”).)



Ono, Fig. 77

264. Ono further discloses that the length of the gate insulating film and the shape of the side surfaces of the gate insulating film can be modified using known techniques to adjust and optimize the electrical performance of the device. (TSMC-1013, ¶216; *see also* TSMC-1013, ¶200.) For example, “the sidewalls of the gate insulator film may curve.” (TSMC-1013, ¶216.)

265. Ono provides several examples of its second embodiment where the length of the gate insulating film is varied in relation to the gate electrode (Figures 86-91), several examples where the sidewall of the gate insulating film is “slanted” (Figures 92-103), and several examples of gate insulator films with curved end portions (Figures 104-123). (TSMC-1013, ¶216.) One such example of a curved end portion is shown in Figure 107, although a POSITA would have understood that other structures are equally applicable.



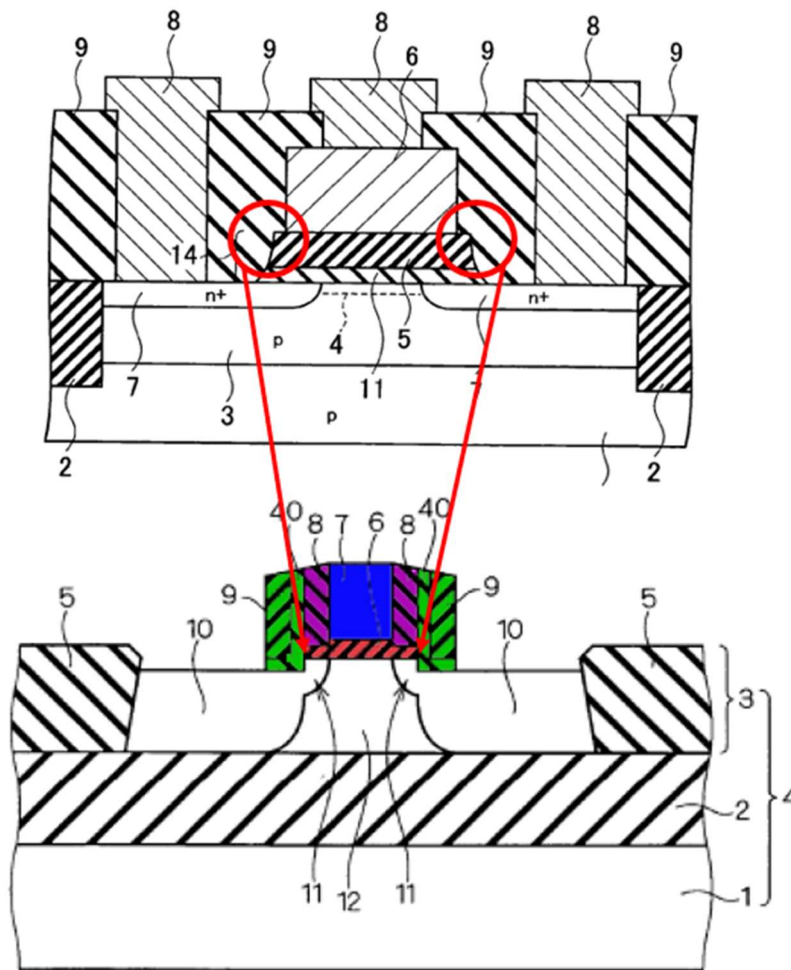
Ono, Fig. 107

B. Motivation to Combine

266. A POSITA would have been motivated to combine the teachings of Matsumoto and Ono.

267. First, a POSITA would have been motivated to select a Hf-based oxide as the gate insulating film in Matsumoto's device, as taught by Ono. (TSMC-1013, ¶209 (describing use of a "HfO₂ film").) As I have discussed previously, for example in connection with Ground 1, Ground 4, and Ground 8, a POSITA would have been motivated to select HfO₂ as a gate insulating film given its known benefits. (TSMC-1037, 2.4.1; TSMC-1032, 207; TSMC-1049, 134.)

268. Second, a POSITA would have also been motivated to apply Ono's teaching of curving the end portion of a gate insulating film to Matsumoto's device, as illustrated below.



Ono, Figure 107 (top); Matsumoto, Figure 22 (bottom)

269. It is well known, as taught by Ono, that modifying the end shape of the gate insulating film—such as curving or rounding it—optimizes electrical capacitance and improves device performance. Matsumoto explicitly seeks to reduce parasitic capacitance and enhance gate controllability, objectives that align with Ono’s demonstrated benefits of curved gate insulating film ends. Thus, a POSITA would have been motivated combine Ono and Matsumoto in the manner described above.

270. Ono expressly suggests the benefits of this combination, teaching that using curved side surfaces for the gate insulating film “reduc[es] the scattering of carriers as well as enhanc[es] the controllability of the gate electrode with respect to the potential of the channel region” and therefore provides “an advantage of optimization.” (TSMC-1013, ¶216; *see also* TSMC-1013, ¶200 (noting, for first embodiment, that by using curved side surfaces, “the electrical capacitance between the gate electrode 6 and the source/drain regions 7 may be adjusted,” resulting in “an advantage of optimization”).

271. Ono’s curved sidewall can be applied to gate insulating films that “overhang” the gate electrode as well, since it was understood that by extending the gate insulating film past the gate electrode, “the capacitive coupling between the source/drain regions 7 and the gate electrode 6 is strengthened, therefore advantages of reducing the resistance of the source/drain regions 7, controlling the parasitic capacitance as well as allowing high-speed operations are obtained.” (TSMC-1013, ¶¶215-216.)

272. Ono’s teachings to adjust the length of the gate insulating film and the shape of the end of the gate insulating film (e.g., to be slanted or curved) align with Matsumoto’s goals of reducing overlap capacitance, improving speed, and lowering power consumption by minimizing the overlap between the gate electrode and the extension regions. (TSMC-1009, ¶47.) A POSITA would have

been further motivated to curve the end of Matsumoto's gate insulating film to enhance controllability of the gate and to optimize parasitic resistance and parasitic capacitance, which improves device performance. (*See* TSMC-1040, ¶108.)

273. Applying Ono's teachings to Matsumoto's fourth embodiment would have been nothing more than applying a known technique (Ono's curved sidewalls for a gate insulating film) to improve similar devices (Matsumoto's transistor using a high-k gate insulating film) in the same way (modifying the dielectric layer to control capacitance). For example, Matsumoto and Ono both disclose forming high-k gate insulating films that extend under the gate electrode and the insulating sidewall using conventional techniques. (TSMC-1009, ¶114; TSMC-1013, ¶167.) Given the use of known techniques, applying the teachings of Ono to Matsumoto would have been within the skills of a POSITA. A POSITA would have had a reasonable expectation of success, and the results of the combination would have been predictable.

C. Claim 1

274. For the reasons I discussed in Ground 8 above, Matsumoto teaches each limitation of claim 1, except it does not expressly disclose "*a gate insulating film ... including Hf*" [1A]. In the combination of Matsumoto's fourth embodiment and Ono, Matsumoto's gate insulating film 6 comprises HfO₂, as taught by Ono.

(TSMC-1013, ¶209.) Accordingly, the combination of Matsumoto and Ono renders obvious claim 1.

D. Dependent Claims 11-12

[11] *The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.*

[12] *The semiconductor device of claim 1, wherein the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof.*

275. The combined Matsumoto and Ono device provides “*the end of the gate insulating film located under the insulating sidewall has a tapered surface*” [11] and “*the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*” [12].

276. Ono’s teaching of a curved end, in, e.g., Figure 107, results in a tapered structure with decreasing thickness towards the ends, consistent with the ’076 patent’s disclosures and figures. As discussed above, the combination of Matsumoto and Ono includes a gate insulating film with curved ends under the “*insulating sidewall*,” specifically, under sidewall film 8. When used with Matsumoto’s gate insulating film, this curved shape has a thickness that decreases toward the end of the gate insulating film, as shown below in the exemplary shape of Ono’s Figure 107. Put another way, the gate insulating film has a tapered end surface as recited by claim 11.



Ono, Fig. 107 (annotated and enlarged)

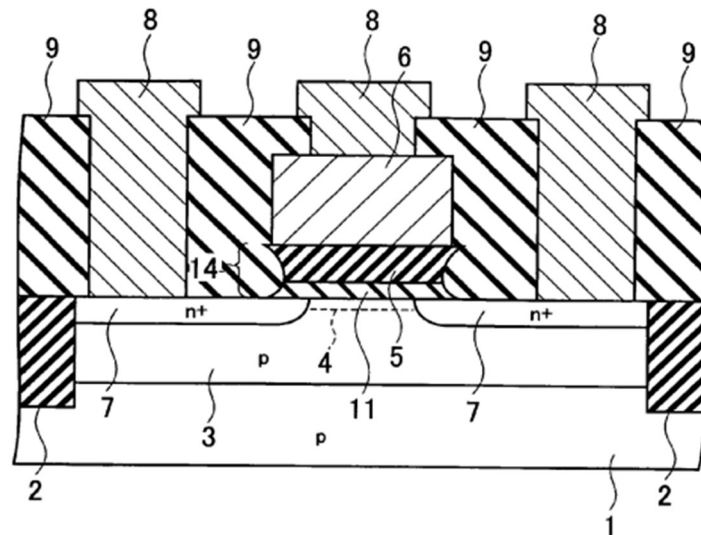
277. Also as shown in the figure above, the end of the gate insulating film shaped according to Ono's Figure 107 has a thickness that is smallest at its end, since the film tapers to points at the ends. Thus, "*the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof*" [12].

E. Dependent Claim 5

[5] *The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall includes a notch at the end thereof.*

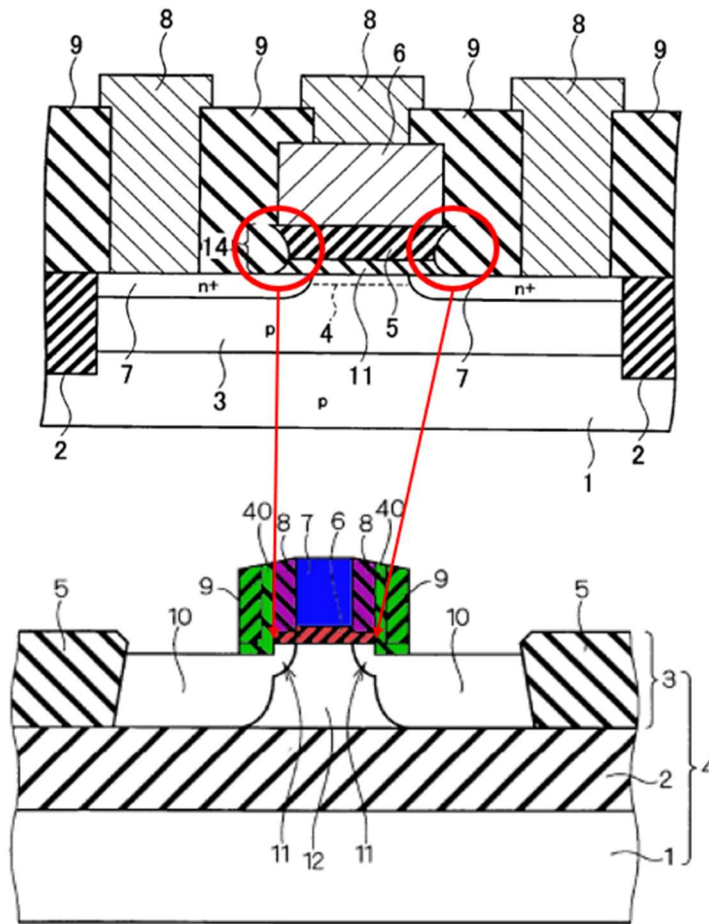
278. The combined Matsumoto and Ono device provides “*part of the gate insulating film located under the insulating sidewall includes a notch at the end thereof*” [5].

279. As discussed above with regard to limitation [1D] in Ground 8, Matsumoto's gate insulating film 6 extends from under gate electrode 7 to under sidewall film 8 (alone, or in combination with films 40 and 9, the "*insulating sidewall*"). As discussed above, in the device of the combination of Matsumoto and Ono, the end portion of the Matsumoto's gate insulating film 6 has a curved shape as taught by Ono. In Ono's Figure 108, shown below, Ono teaches that the side end of the gate insulating film has a semicircular shape.



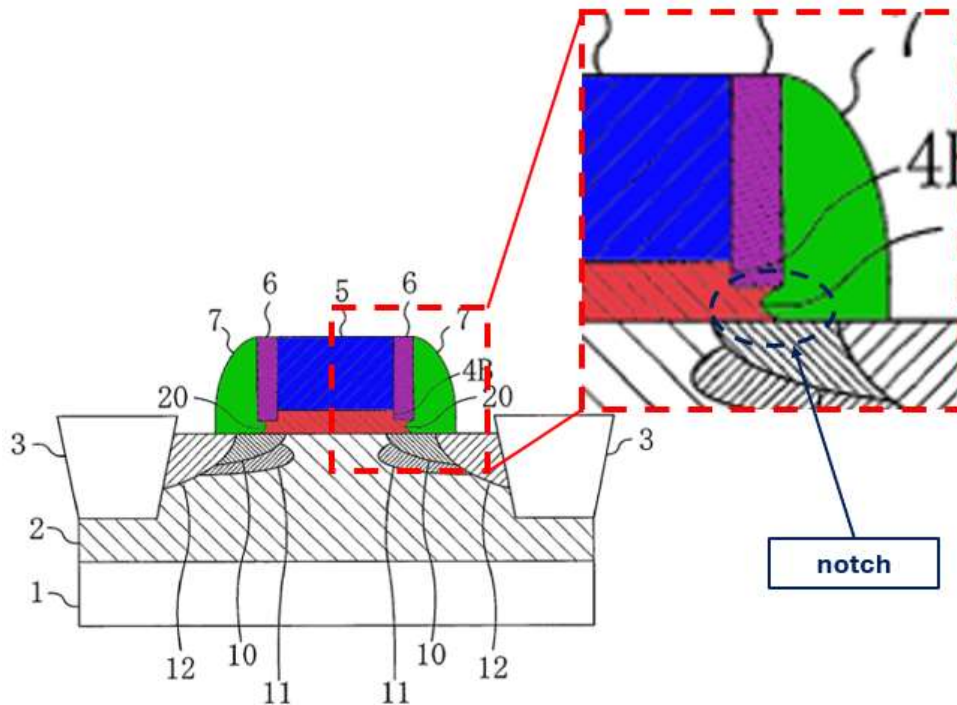
Ono, Figure 108

280. As shown below, a POSITA would have been motivated to apply the semicircular shape taught in Ono's Figure 108 to the ends of Matsumoto's gate insulating film located under film 8 (part of the collective "*insulating sidewall*"). The motivation to apply Ono's teachings to Matsumoto's device are the same as I discussed above.



Ono, Fig. 108 (top); Matsumoto, Fig. 22 (bottom) (annotated)

281. Ono's semicircular shape in Figure 108 is consistent with the "notch" disclosed in the '076 patent. (See, e.g., TSMC-1001, 8:41-46 (referring to notch 20 of Figure 7), Figure 7 (depicting notch 20 having a semicircular shape)).



'076 Patent, Fig. 7 (annotated and enlarged)

XVI. Conclusion

282. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 15th day of April, 2025, in Austin, Texas.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Jack Lee", followed by a period.

Jack Lee, Ph.D.