EXHIBIT 076-02: Invalidity of U.S. Patent No. 8,587,076 (the ’076 Patent) Based on *Guha*

The following list illustrates certain grounds for invalidity based on:

- U.S. Publication 2006/0091432 to Guha, et al. (“*Guha*”), filed November 2, 2004, is prior art to U.S. Patent No. 8,587,076 (the “’076 patent”) under at least pre-AIA 35 U.S.C. §102(e).

Guha, including any material incorporated by reference into *Guha*, anticipates at least claims 1-3, 6-8, and 10-13 of the ’076 patent under pre-AIA 35 U.S.C. §102(e).

To the extent any limitation is found not to be expressly or inherently disclosed in *Guha*, such a limitation would have been obvious either based on *Guha* alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 076-01 and 076-03 through 076-15, because the ’076 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

In particular, any disclosures identified for each limitation of the ’076 patent in the aforementioned Exhibits may be combined with the disclosures of *Guha* identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.[1]

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to

[1] Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

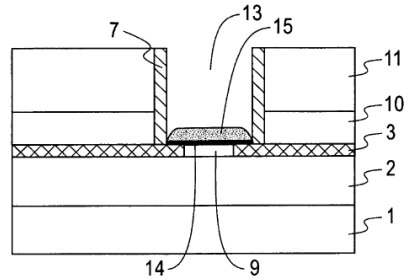
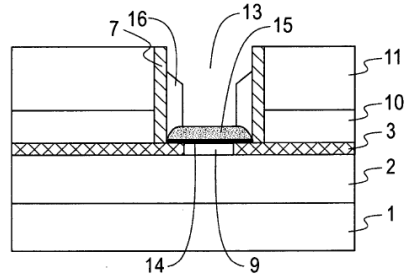
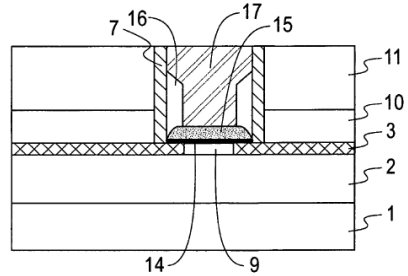
show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

U.S. Patent No. 8,587,076	**Exemplary Disclosures Relevant to *Guha***
Claim 1	
[1pre] A semiconductor device comprising:	*Guha*, alone or in combination with one or more references, discloses or suggests a semiconductor device. For example, *Guha* discloses the following at Title: DAMASCENE GATE FIELD EFFECT TRANSISTOR WITH AN INTERNAL SPACER STRUCTURE *Guha* discloses the following at Abstract: A MOSFET is disclosed that comprises a channel between a source extension and a drain extension, a dielectric layer over the channel, a gate spacer structure formed on a peripheral portion of the dielectric layer, and a gate formed on a non-peripheral portion of the dielectric layer, with at least a lower portion of the gate surrounded by and in contact with an internal surface of the gate spacer structure, and the gate is substantially aligned at its bottom with the channel. One method of forming the MOSFET comprises forming the dielectric layer, the gate spacer structure and the gate contact inside a cavity that has been formed by removing a sacrificial gate and spacer structure. *Guha* discloses the following at [0001]: The invention relates to a MOSFET device having a damascene gate with an internal spacer structure and a process of forming the device. *Guha* discloses the following at [0022]:

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	The structure shown in FIG. 1 can be manufactured from conventional materials with conventional processing steps that are well known in the art. For example, the substrate **1** may comprise any semiconducting material including, but not limited to: Si, Ge, SiGe, GaAs, InAs, InP and all other III/V semiconductor compounds, and may also be a layered substrate comprising different semiconductor materials, e.g., Si/SiGe. *Guha* discloses the following at [0023]: The channel layer 3 can comprise any semiconducting material such as Si, SiGe, SiGeC, InAs, GaAs, InP and other III/V compound semiconductors. Combinations of these semiconducting materials, strained or unstrained, are also contemplated herein. *Guha* discloses the following at [0043]: FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. In this embodiment, the structure of FIG. 7 is subjected to a deposition step in which the dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13. This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafiium, zirconium, aluminium, among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing a further reduction in sidewall capacitance. As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13. *Guha* discloses the following at claim 1: A MOSFET comprising: *Guha* discloses the following at claim 13: A method for forming a MOSFET, comprising the steps of:

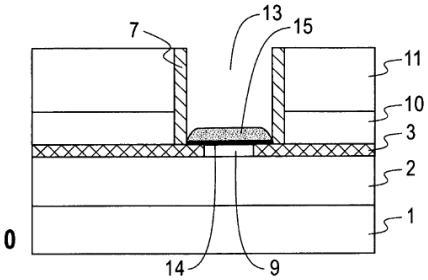
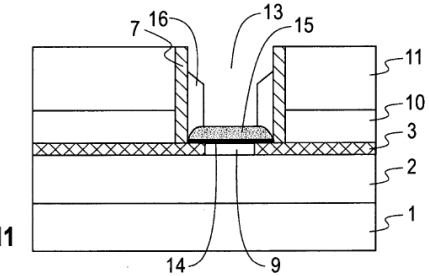
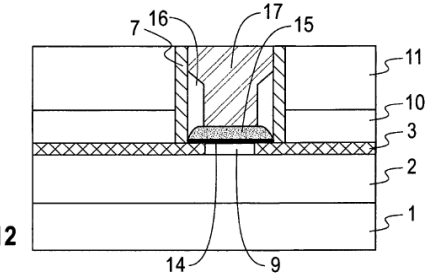
U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
[1A] a gate insulating film formed on an active region in a substrate and including Hf;	*Guha*, alone or in combination with one or more references, discloses or suggests a gate insulating film formed on an active region in a substrate and including Hf. For example, *Guha* discloses the following at [0021]: > FIG. 1 shows an initial stacked structure that comprises a substrate 1 having a bottom insulator 2, also referred to as buried oxide layer, located thereon. The initial stacked structure also includes a channel layer 3 on top of the bottom insulator 2, and an oxide layer 4, also referred to as pad protection layer, located atop the channel layer 3. *Guha* discloses the following at [0022]: > The substrate may be of the n or p-type depending on the desired device to be fabricated. The substrate may further contain active device regions, wiring regions, isolation regions or other like regions (not shown). *Guha* discloses the following at [0026]: > In the following step, source/drain extensions, also referred to as source/drain (S/D) junctions, are formed by implanting dopants through the pad protection layer 4 into the channel layer 3, with the dummy gate 5 acting as an implantation mask. Following ion implantation, the S/D extensions are annealed to activate dopants. A channel 9 (see FIG. 3), having a predetermined channel length substantially equal to the length of the dummy gate 5, is thus defined between the S/D extensions. *Guha* discloses the following at [0037]: > An optional gate-isolating layer 14 can then be formed at the bottom of the cavity 13, as shown in FIG. 7. The gate-isolating layer 14 acts as a buffering layer between channel 9 and the dielectric material to be deposited thereon. A preferred material for the gate-isolating layer 14 is silicon oxide, which can be thermally grown, and thinned if necessary. Other materials, however, may also be suitable. This gate-isolating layer,

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	for example, is used to prevent mobility degradation in the silicon channel that may be caused by scattering mechanisms in the dielectric layer. *Guha* discloses the following at [0038]: Thereafter a dielectric layer 15, preferably comprising a high-K dielectric material, is deposited. As shown in FIG. 8, the dielectric layer 15 covers the nitride overlayer 11, the walls of the isolating spacers 7 and the gate-isolating layer 14. A high-K material is a material that exhibits a dielectric constant of approximately above 10 or more. Examples of such materials, include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide. *Guha* discloses the following at [0043]: FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. In this embodiment, the structure of FIG. 7 is subjected to a deposition step in which the dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13. This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafiium, zirconium, aluminium, among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing a further reduction in sidewall capacitance. As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13. *Guha* discloses the following at Figures 10-12:

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	 Fig. 10  Fig. 11  Fig. 12 *Guha* discloses the following at claim 1: 1. A MOSFET comprising: a channel between said source extension and said drain extension;

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	a dielectric layer above said channel; *Guha* discloses the following at claim 13: b) forming a source extension and a drain extension in said channel layer thereby defining a channel between said source and drain extensions; c) forming a dielectric layer over said channel;
[1B] a gate electrode formed on the gate insulating film;	*Guha*, alone or in combination with one or more references, discloses or suggests a gate electrode formed on the gate insulating film. For example, *Guha* discloses the following at [0041]: Thereafter the cavity 13 is filled with a conductive material to form a gate 17. This can be done by depositing the material into the cavity 13 and onto the dielectric layer 15. For example, the conductive material may be formed from vapor phase deposition, such as tungsten or titanium nitride, or by depositing amorphous silicon and reacting it with a metal such as nickel to form a silicide, and subsequently thinning it down to the dielectric layer 15, and possibly removing the conductive material and the dielectric layer 15 lying outside of cavity 13, e.g., by CMP. Polysilicon may also be used, for example, either in-situ doped or doped by a conventional ion-implantation and annealing technique, as long as the annealing temperatures and conditions are compatible with the dielectric layer 15 and the second overlayer 11. *Guha* discloses the following at [0043]: FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. In this embodiment, the structure of FIG. 7 is subjected to a deposition step in which the dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13. This can be achieved, for example, by a

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	directional deposition process such as thermal evaporation of a metal such as hafiium, zirconium, aluminium, among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing a further reduction in sidewall capacitance. As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13. *Guha* discloses the following at [0044]: Thus, as shown in FIG. 11, internal gate spacer structure 16 is formed within cavity 13, as previously described in connection with FIG. 8. Here the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7. *Guha* discloses the following at [0045]: Thereafter the cavity 13 is filled with a conductive material to form the gate 17, as previously described. The resulting device is depicted in FIG. 12. Guha discloses the following at Figures 10-12:

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	 Fig. 10  Fig. 11  Fig. 12 *Guha* discloses the following at claim 1: a dielectric layer above said channel; a gate disposed on a non-peripheral portion of said top surface of said dielectric layer

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	Guha discloses the following at claim 13: c) forming a dielectric layer over said channel; d) forming a gate spacer structure over a peripheral portion of a top surface of said dielectric layer; e) forming a gate contact by disposing an electrically conductive material into said first cavity to contact said top surface of said dielectric layer.
[1C] a insulating sidewall formed on each side surface of the gate electrode; and	*Guha*, alone or in combination with one or more references, discloses or suggests a insulating sidewall formed on each side surface of the gate electrode. For example, *Guha* discloses the following at [0028]: An isolating spacer structure 7 is formed flanking the dummy-gate spacers 8. The resulting structure is depicted in FIG. 3. In this embodiment, the isolating spacer structure 7 is of unitary construction, e.g., present in form of a ring that surrounds the dummy gate spacer 8. As used herein, the isolating spacer structure 7 is used to denote the isolating spacer(s), whether it is of unitary construction or not. In practice, the unitary construction is preferred because of its relative ease of fabrication. Isolating spacer structure 7 can be composed of any insulating material including, for example, an oxide, nitride, oxynitride or any combination thereof; as long as the material can be selectively etched with respect to the material of the dummy gate spacers 8. Isolating spacer structure 7 can be formed by deposition of an insulating material and subsequent etching. A preferred material would be silicon nitride. *Guha* discloses the following at [0034]: Next, the dummy gate spacer 8 is removed, e.g. using dilute HF, which also removes the pad protection layer 4), leaving behind the structure depicted in FIG. 6. The first

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	overlayer 11 and the isolating spacer structure 7 can comprise silicon nitride which is resistant to HF. *Guha* discloses the following at [0035]: As shown in FIG. 6, the channel layer 3 and the isolating spacers 7 together define a cavity 13. In the absence of the optional isolating spacer structure 7, the cavity 13 will be defined at its bottom by channel layer 3 and at its sidewalls by side surfaces of S/D contacts 10 and the overlayer 11. *Guha* discloses the following at [0040]: Thus, according to the present invention, “internal” gate spacers 16, or more generally, a gate spacer structure, is formed inside the cavity 13, as shown in FIG. 8. This can be achieved, for example, by depositing a spacer material, e.g. an oxide or other suitable material, in the cavity 13 and etching the deposited material anisotropically, e.g. by RIE, such that the portion of the dielectric layer 15 above channel 9 is exposed, leaving the gate spacer structure 16 on the sidewalls of the cavity 13. This arrangement of the gate spacer structure 16 provides a narrowing of the cavity 13 above the channel 9. The gate spacer structure 16 has an internal surface 16S (i.e., surface facing the interior of the cavity 13, away from the cavity sidewalls) with a lower portion that is substantially perpendicular to the dielectric layer 15. *Guha* discloses the following at [0043]: FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. … As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13. *Guha* discloses the following at [0044]:

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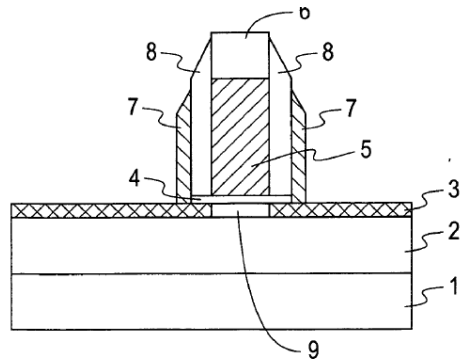
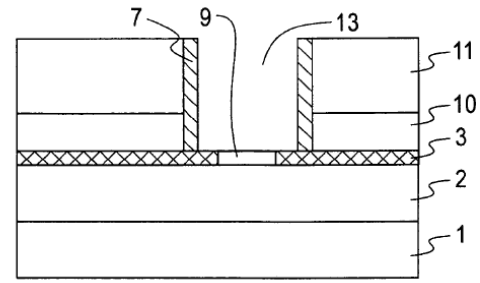
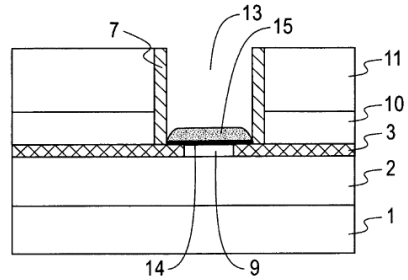
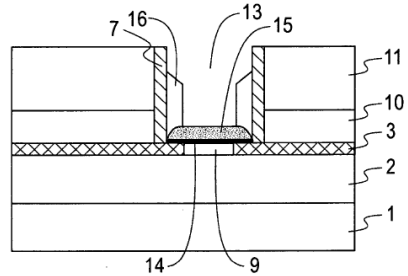
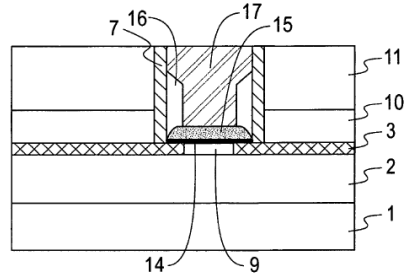
	Thus, as shown in FIG. 11, internal gate spacer structure 16 is formed within cavity 13, as previously described in connection with FIG. 8. Here the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7. *Guha* discloses the following at [0045]: Thereafter the cavity 13 is filled with a conductive material to form the gate 17, as previously described. The resulting device is depicted in FIG. 12. *Guha* discloses the following at Figures 3-6 and 10-12:  Fig. 3  Fig. 6

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	 Fig. 10  Fig. 11  Fig. 12 *Guha* discloses the following at claim 1: a gate spacer structure disposed on a peripheral portion of a top surface of said dielectric layer and having an internal surface that meets said top surface at about a right angle;

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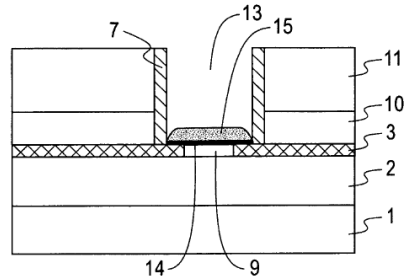
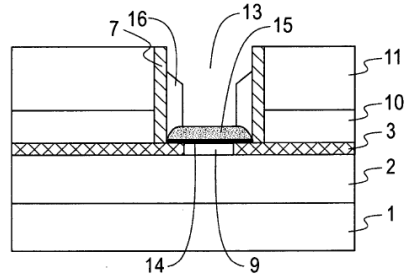
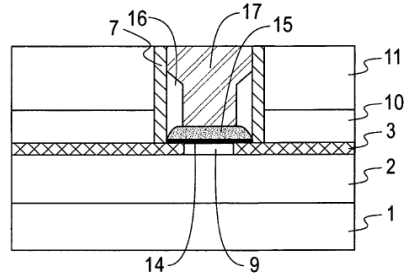
	a gate disposed on a non-peripheral portion of said top surface of said dielectric layer and having at least a lower portion surrounded by and in contact with said internal surface of said gate spacer structure; and said gate is substantially aligned at its bottom with said channel.
[1D] wherein a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length, and	*Guha*, alone or in combination with one or more references, discloses or suggests a width of the gate insulating film along a gate length is larger than a width of the gate electrode along the gate length. For example, *Guha* discloses the following at [0040]: Thus, according to the present invention, “internal” gate spacers 16, or more generally, a gate spacer structure, is formed inside the cavity 13, as shown in FIG. 8. … This arrangement of the gate spacer structure 16 provides a narrowing of the cavity 13 above the channel 9. *Guha* discloses the following at [0041]: Thereafter the cavity 13 is filled with a conductive material to form a gate 17. This can be done by depositing the material into the cavity 13 and onto the dielectric layer 15. *Guha* discloses the following at [0043]: FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. … As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13. *Guha* discloses the following at [0044]:

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	Thus, as shown in FIG. 11, internal gate spacer structure 16 is formed within cavity 13, as previously described in connection with FIG. 8. Here the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7. *Guha* discloses the following at [0045]: Thereafter the cavity 13 is filled with a conductive material to form the gate 17, as previously described. The resulting device is depicted in FIG. 12. *Guha* discloses the following at [0047]: In this embodiment, the internal surface 16S is a curved surface, e.g., with a curved region towards the top. Other variations are also possible, depending on the specific process steps used. For example, the internal spacer 16 a and 16 b may also have a rectangular cross-section, e.g., by polishing or removing the upper curved region to form a horizontal portion of the internal surface. *Guha* discloses the following at Figures 10-12:

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	 Fig. 10  Fig. 11  Fig. 12
[1E] an end of the gate insulating film under the insulating sidewall is retracted from an outer end	*Guha*, alone or in combination with one or more references, discloses or suggests an end of the gate insulating film under the insulating sidewall is retracted from an outer end of the insulating sidewall toward the gate electrode.

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
of the insulating sidewall toward the gate electrode.	For example, *Guha* discloses the following at [0043]: > FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. In this embodiment, the structure of FIG. 7 is subjected to a deposition step in which the dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13. This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafiium, zirconium, aluminium, among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing a further reduction in sidewall capacitance. As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13. However, the problem still exists that the edge where the dielectric layer 15 meets the isolating spacer structure 7 may not be well defined, and is rounded either upwards or downwards (e.g., similar to a cusp), which would lead to, in the first case, reduced control between the gate to be formed and the channel 9, and in the second case a danger of a short between the gate to be formed and the channel 9. *Guha* discloses the following at [0044]: > Thus, as shown in FIG. 11, internal gate spacer structure 16 is formed within cavity 13, as previously described in connection with FIG. 8. Here the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7. *Guha* discloses the following at [0045]: > Thereafter the cavity 13 is filled with a conductive material to form the gate 17, as previously described. The resulting device is depicted in FIG. 12. Again, by means of the gate spacer structure 16, the interface between the bottom of the gate 17 and the dielectric layer 15 is better defined and offers a better control over the channel 9. As

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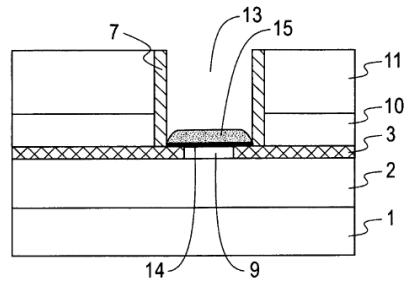
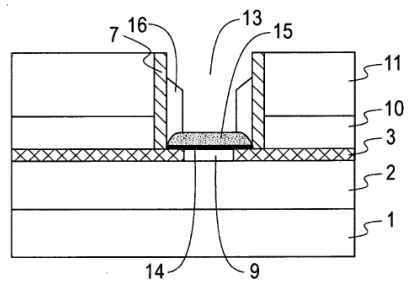
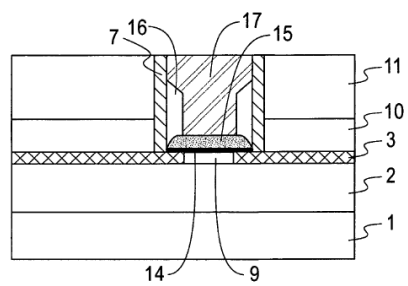
	previously discussed, the isolating spacer structure 7 and gate isolating layer 14 are optional, and either one or both may be omitted in alternative embodiments. *Guha* discloses the following at Figures 10-12:  Fig. 10  Fig. 11  Fig. 12

U.S. Patent No. 8,587,076	**Exemplary Disclosures Relevant to *Guha***
Claim 2	
2. The semiconductor device of claim 1, further comprising a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film.	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha*, alone or in combination with one or more references, discloses or suggests a buffer insulating film formed of a silicon oxide film and provided between the substrate and the gate insulating film. For example, *Guha* discloses the following at [0037]: > An optional gate-isolating layer 14 can then be formed at the bottom of the cavity 13, as shown in FIG. 7. The gate-isolating layer 14 acts as a buffering layer between channel 9 and the dielectric material to be deposited thereon. A preferred material for the gate-isolating layer 14 is silicon oxide, which can be thermally grown, and thinned if necessary. Other materials, however, may also be suitable. This gate-isolating layer, for example, is used to prevent mobility degradation in the silicon channel that may be caused by scattering mechanisms in the dielectric layer. *Guha* discloses the following at [0043]: > FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. In this embodiment, the structure of FIG. 7 is subjected to a deposition step in which the dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13. *Guha* discloses the following at Figures 10-12:

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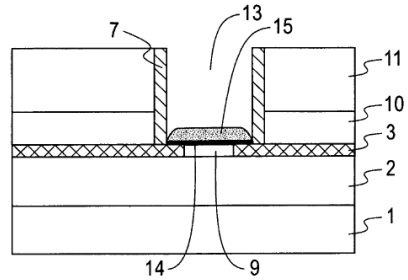
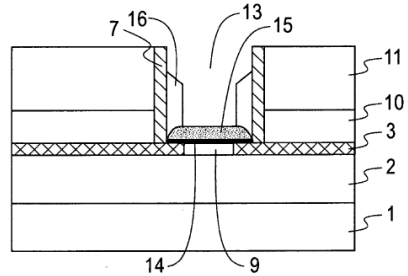
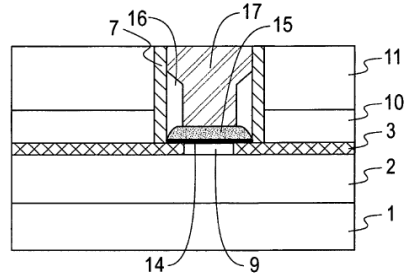
	 Fig. 10  Fig. 11  Fig. 12 *Guha* discloses the following at claim 1 in connection with claim 11: 1. A MOSFET comprising: a dielectric layer above said channel;

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	11. The MOSFET of claim 1, further comprising a gate-isolating layer between said channel and said dielectric layer.
Claim 3	
3. The semiconductor device of claim 1, wherein the gate insulating film is formed of a Hf based oxide.	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha*, alone or in combination with one or more references, discloses or suggests the gate insulating film is formed of a Hf based oxide. For example, *Guha* discloses the following at [0038]: Thereafter a dielectric layer 15, preferably comprising a high-K dielectric material, is deposited. As shown in FIG. 8, the dielectric layer 15 covers the nitride overlayer 11, the walls of the isolating spacers 7 and the gate-isolating layer 14. A high-K material is a material that exhibits a dielectric constant of approximately above 10 or more. Examples of such materials, include, but are not limited to hafnium oxide, hafnium silicate, aluminum oxide or zirconium oxide. *Guha* discloses the following at [0043]: FIGS. 10-12 show an alternative process sequence that can be used to form the gate with internal gate spacers. In this embodiment, the structure of FIG. 7 is subjected to a deposition step in which the dielectric layer 15 is formed only on the gate-isolating layer 14 at the bottom of the cavity 13. This can be achieved, for example, by a directional deposition process such as thermal evaporation of a metal such as hafiium, zirconium, aluminium, among others, and subsequent chemical conversion to a high-K dielectric such as metal oxides, silicates or other appropriate high-K materials, allowing

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	a further reduction in sidewall capacitance. As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13.
Claim 6	
6. The semiconductor device of claim 1, wherein a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha*, alone or in combination with one or more references, discloses or suggests a part of the gate insulating film located under the insulating sidewall has a thickness of 2 nm or less.
Claim 7	
7. The semiconductor device of claim 1, wherein an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall.	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha*, alone or in combination with one or more references, discloses or suggests an end of the gate insulating film protrudes from a side end of the gate electrode toward the insulating sidewall. *See* limitation [1D], *supra*.
Claim 8	
8. The semiconductor device of claim 1, wherein the insulating sidewall has a double layer structure including an oxide film and a nitride film.	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha*, alone or in combination with one or more references, discloses or suggests the insulating sidewall has a double layer structure including an oxide film and a nitride film. For example, *see* limitation [1C].

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	Guha discloses the following at [0028]: > Isolating spacer structure 7 can be composed of any insulating material including, for example, an oxide, nitride, oxynitride or any combination thereof; as long as the material can be selectively etched with respect to the material of the dummy gate spacers 8. Isolating spacer structure 7 can be formed by deposition of an insulating material and subsequent etching. A preferred material would be silicon nitride. *Guha* discloses the following at [0040]: > Thus, according to the present invention, “internal” gate spacers 16, or more generally, a gate spacer structure, is formed inside the cavity 13, as shown in FIG. 8. This can be achieved, for example, by depositing a spacer material, e.g. an oxide or other suitable material, in the cavity 13 and etching the deposited material anisotropically, e.g. by RIE, such that the portion of the dielectric layer 15 above channel 9 is exposed, leaving the gate spacer structure 16 on the sidewalls of the cavity 13. *Guha* discloses the following at [0044]: > Thus, as shown in FIG. 11, internal gate spacer structure 16 is formed within cavity 13, as previously described in connection with FIG. 8. Here the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7.
Claim 10	
10. The semiconductor device of claim 1, wherein a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha* alone or in combination with one or more references, discloses or suggests a width of a bottom surface of the gate insulating film along a gate length is larger than a width of a bottom surface of the gate electrode along the gate length.

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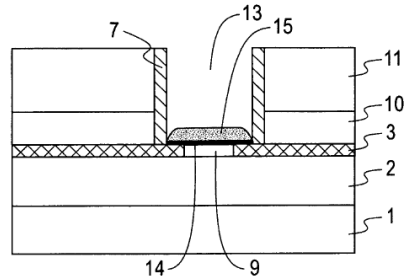
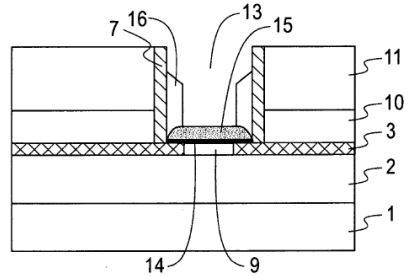
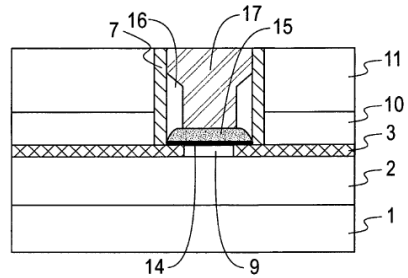
surface of the gate electrode along the gate length.	*See* limitation [1D], *supra*.
Claim 11	
11. The semiconductor device of claim 1, wherein the end of the gate insulating film located under the insulating sidewall has a tapered surface.	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha*, alone or in combination with one or more references, discloses or suggests the end of the gate insulating film located under the insulating sidewall has a tapered surface. For example, *Guha* discloses the following at [0043]: > As shown in FIG. 10, the dielectric layer 15 covers only the bottom of the cavity 13. However, the problem still exists that the edge where the dielectric layer 15 meets the isolating spacer structure 7 may not be well defined, and is rounded either upwards or downwards (e.g., similar to a cusp), which would lead to, in the first case, reduced control between the gate to be formed and the channel 9, and in the second case a danger of a short between the gate to be formed and the channel 9. *Guha* discloses the following at [0044]: > Here the gate spacer structure 16 contacts both the dielectric layer 15 and the isolating spacer structure 7. *Guha* discloses the following at Figures 10-12:

U.S. Patent No. 8,587,076	Exemplary Disclosures Relevant to *Guha*
	 Fig. 10  Fig. 11  Fig. 12
Claim 12	
12. The semiconductor device of claim 1, wherein the gate insulating film located under the insulating	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*.

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sidewall has a thickness which becomes smaller toward the end thereof.	*Guha*, alone or in combination with one or more references, discloses or suggests the gate insulating film located under the insulating sidewall has a thickness which becomes smaller toward the end thereof. For example, *see* claim 11, *supra*.
Claim 13	
13. The semiconductor device of claim 1, wherein the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length.	*Guha*, alone or in combination with one or more references, discloses or suggests the semiconductor device of claim 1. *See* claim 1, *supra*. *Guha*, alone or in combination with one or more references, discloses or suggests the width of the gate insulating film along a gate length is larger than a width of part of the gate electrode in a middle position in height along the gate length. For example, *see* claim 10, *supra*.