CERTIFICATE OF TRANSLATION ACCURACY

August 12, 2025

I, Xin Min Liu hereby declares the following under penalty of perjury:

1. I am a professional translator with Chinese as a native language and English as an acquired language. I am over 18 years of age, of sound mind, and competent to make this affidavit. The facts set out in the foregoing affidavit are based on my personal knowledge.

2. I am fluent in both Chinese and English. My qualifications include: I graduated from the United Nations Translators and Interpreters Training Program in 1993; served as a translator with the United Nations Chinese Translation Service from 1984 to 1989; was conferred a Juris Doctor's degree by the University of Cincinnati College of Law in 1993; and worked as a freelance translator with major law firms, the United States Department of Justice, the US Department of State and other clients around the United States since 1993.

3. I am familiar and competent with both the Chinese and English languages. I have received the following Chinese-language documents and provided English-language translations:

- Excerpts of CN 2006100938722 - PH 複製.pdf

4. The Chinese-language and English-language versions of these documents are submitted as TSMC-1156.

5. I hereby certify that the above-referenced English translations are complete and accurate renditions of the Chinese originals to the best of my knowledge and belief.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on August 12, 2025 in Fishers, Indiana.

Xin Min Liu

1. A semiconductor device, characterized in that:
it comprises: a high dielectric constant gate insulating film formed on the active region of the substrate,
a gate electrode formed on the high dielectric constant gate insulating film, and
an insulating sidewall formed on a side surface of the gate electrode;
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the insulating side wall;
at least a portion of the thickness of a region below the insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a region below the gate electrode in the high dielectric constant gate insulating film.

2. The semiconductor device according to claim 1, wherein:
the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on the side surface of the gate electrode, and the second insulating sidewall is formed on the side surface of the gate electrode with the first insulating sidewall sandwiched therebetween;
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the first insulating side wall; and
the thickness of a region below the first insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a region below the gate electrode in the high dielectric constant gate insulating film.

3. The semiconductor device according to claim 2, wherein:
the high dielectric constant gate insulating film is not formed below the second insulating sidewall.

4. The semiconductor device according to claim 2, wherein:
the high dielectric constant gate insulating film is continuously formed to the lower side of the second insulating side wall; and
the thickness of a region below the second insulating side wall in the high dielectric constant gate insulating film is equal to the thickness of a region below the first insulating side wall in the high dielectric constant gate insulating film.

5. The semiconductor device according to claim 2, wherein:
the high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the second insulating side wall; and
the thickness of a region below the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a region below the first insulating sidewall in the high dielectric constant gate insulating film.

6. The semiconductor device according to claim 1, wherein:
the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on a side surface of the gate electrode, and the second insulating sidewall is formed on a side surface of the gate electrode with the first insulating sidewall sandwiched therebetween;
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the second insulating side wall;
the thickness of a region below the first insulating sidewall in the high constant gate insulating film is equal to the thickness of a region below the gate electrode in the high constant gate insulating film; and
the thickness of a region below the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the region below the gate electrode in the high dielectric constant gate insulating film.

7. The semiconductor device according to claim 1, wherein:
a notch is provided at a side end portion of the high dielectric constant gate insulating film.

8. The semiconductor device according to claim 1, wherein:
a buffer insulating film is provided between the substrate and the high dielectric constant gate insulating film.

9. The semiconductor device according to claim 8, wherein:
a buffer insulating film is a silicon oxide film or a silicon oxynitride film.

10. The semiconductor device according to claim 1, wherein:
a gate electrode is a fully silicided gate electrode in which the entire region is silicided.

11. A method for manufacturing a semiconductor device, characterized in that:

the method comprises: step a, forming a high dielectric constant gate insulating film on the active region of the substrate;

step b, forming a gate electrode on the high dielectric constant gate insulating film;

step c, after step b, etching a portion of the high dielectric constant gate insulating film located outside the gate electrode to reduce the thickness of the portion; and

step d: after step c, forming an insulating sidewall on the side surface of the gate electrode.

12. The method for manufacturing a semiconductor device according to claim 11, characterized in that:

after the step d, the method further comprises the process of partially removing the gate insulating film.

13. The method for manufacturing a semiconductor device according to claim 1, wherein:

the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall;

the above-mentioned step d includes step d1 and step d2. In the step d1, the above-mentioned first insulating side wall is formed on the side of the above-mentioned gate electrode; in the step d2, the above-mentioned second insulating side wall is formed on the side of the above-mentioned gate electrode by sandwiching the above-mentioned first insulating side wall.

14. The method for manufacturing a semiconductor device according to claim 13, wherein:

between the step d1 and the step d2, a step of removing a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall is further included.

15. The method for manufacturing a semiconductor device according to claim 13, wherein:

the steps d1 and d2, a step of etching a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall to make the portion thinner is included;

after the step d2, the method further includes removing a portion of the high dielectric constant gate insulating film located outside the second insulating sidewall.

16. The method for manufacturing a semiconductor device according to any one of claims 12, 14 or 15, wherein:

the high dielectric constant gate insulating film is selectively removed by wet etching.

17. The method for manufacturing a semiconductor device according to claim 11, wherein:

the step b includes forming a protective film covering the upper surface of the gate electrode; and

after the step d, the method further includes removing the protective film after siliciding the surface of the active region located outside the insulating sidewall, and then siliciding the entire gate electrode.

18. The method for manufacturing a semiconductor device according to claim 11, further comprising:

forming a buffer insulating film on the active region before step a;

wherein in step a, the high dielectric constant gate insulating film is formed on the active region with the buffer insulating film interposed therebetween.

Postal Code J00083 Zhongke Patent and Trademark Agency Co., Ltd. 25th Floor, Building B, Tsinghua Tongfang Technology Building, No. 1 Wangzhuang Road, Haidian District, Beijing Wang Huimin	Date of issue August 25, 2006
Application number: 2006100938722	
Applicant: Panasonic Corporation	
Invention Title: Semiconductor device and manufacturing method thereof	

Notification of Passing Preliminary Examination of the Application for Invention

1. The above patent application has been preliminarily examined and found to be in compliance with the provisions of the Patent Law and its Implementing Regulations.

2. According to the provisions of Article 34 of the Patent Law, the above-mentioned patent application will be published eighteen months from the date of application.

The invention patent application that passed the preliminary examination is based on:

The specification filed on June 20, 2006: pages 1 to 24;

The claims filed on June 20, 2006: pages 1 to 3; and

The accompanying drawings attached to the specification filed on June 20, 2006: page 1 to 11.

Reminder:

The applicant for an invention patent may, within three years from the date of application, request substantive examination and pay the examination fee at the same time. If the applicant fails to request substantive examination or pay the examination fee within the prescribed time limit, the application shall be deemed withdrawn.

Examiner: Bi Chunsheng Examination department: Preliminary Review and Process Management Department

August 16, 2006

21223
2002.8

Please send reply to: 100088 No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing

Attention: China National Intellectual Property Administration

(Note: Any letter sent personally to the examiner shall have no legal effect)

Postal Code 100083 Zhongke Patent and Trademark Agency Co., Ltd. 25th Floor, Building B, Tsinghua Tongfang Technology Building, No. 1 Wangzhuang Road, Haidian District, Beijing Wang Huimin	Date of issue February 16, 2007
Application number: 2006100938722	
Applicant: Panasonic Corporation	
Invention Title: Semiconductor device and manufacturing method thereof	

Notice of Publication of Invention Patent Application

The above patent application has been found to be in compliance with the relevant provisions of the Patent Law and its Implementing Rules after preliminary examination. In accordance with Article 34 of the Patent Law, the application has been published in the Invention Patent Gazette, Volume 23, Issue 06.

Note: A copy of the published specification is attached.

Reminder:

The applicant for an invention patent may, within three years from the date of application, request substantive examination and pay the examination fee at the same time. If the applicant fails to request substantive examination or pay the examination fee within the prescribed time limit, the application shall be deemed withdrawn.

According to the provisions of Article 91 of the Implementing Regulations of the Patent Law, anyone who pays various fees to the Patent Administration must indicate the correct application number or patent number and the name of the fee. Failure to indicate such information will be deemed as failure to complete the payment procedures.

Examiner: Jin Li Examination department: Preliminary Review and Process Management Department
February 8, 2007

21227
2002.8

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Substantive examination request

Please fill in each column of this form correctly according to the "Notes on Filling in the Form" on the back of this form IA063392

① Patent application	Application No. 200610093872.2 Application date: June 20, 2006
	Name of invention Semiconductor device and method for manufacturing the same
	Applicant (representative) Panasonic Corporation
②Content of the request According to the provisions of Article 35 of the Patent Law, we request a substantive examination of the above patent application.	
③ List of attachments ☐ Reference documents related to the present invention before the filing date ☐ Information retrieved by foreign countries regarding the application ☐ Information on the foreign country's review results of the application ☐ [Bar code: 061938722]	
④ Remarks ☒ Reference documents are required to be listed in the copy the Patent Administration ☒ Currently, we have not received any foreign search data or examination results for this application ☐ Currently, no reference document materials related to the present invention have been received before the filing date ☐ The International Searching Authority for this international application is *JP/EP/SE*	
⑤ Replacement pages for the application document 2 copies of the claims, a total of 6 pages	
⑥ Seal of applicant or agency [seal: CHINA SCIENCE PATENT & TRADEMARK AGENT LTD] August 5, 2008	⑦Patent administration handling opinion

[Handwritten: 11103]

Claims

1. A semiconductor device, characterized in that:
the invention comprises: a high dielectric constant gate insulating film formed on the active region of the substrate,
a gate electrode formed on the high dielectric constant gate insulating film, and
insulating sidewalls formed on the side surfaces of the gate electrode;
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the insulating side wall;
the thickness of at least a portion of a lower region of the insulating sidewall in the high constant gate insulating film is smaller than the thickness of a lower region of the gate electrode in the high constant gate insulating film.
2. The semiconductor device according to claim 1, wherein:
the insulating sidewalls are composed of a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on a side surface of the gate electrode, and the second insulating sidewall is formed on a side surface of the gate electrode with the first insulating sidewall sandwiched therebetween.
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the first insulating side wall;
the thickness of a lower region of the first insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a lower region of the gate electrode in the high dielectric constant gate insulating film.
3. The semiconductor device according to claim 2, wherein:
the high dielectric constant gate insulating film is not formed on the lower side of the second insulating sidewall.
4. The semiconductor device according to claim 2, wherein:
the high dielectric constant gate insulating film is continuously formed to the lower side of the second insulating side wall;
the thickness of the second insulating sidewall in the high dielectric constant gate insulating film is equal to the thickness of the lower region of the first insulating sidewall in the high dielectric constant gate insulating film.
5. The semiconductor device according to claim 2, wherein:
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the second insulating side wall; and
the thickness of a lower region of the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a lower region of the first insulating sidewall in the high dielectric constant gate insulating film.
6. The semiconductor device according to claim 1, wherein:
the insulating sidewalls are composed of a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on a side surface of the gate electrode, and the second insulating sidewall is formed on a side surface of the gate electrode with the first insulating sidewall sandwiched therebetween;
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the second insulating side wall;
the thickness of the first insulating sidewall in the high constant gate insulating film is equal to the thickness of the lower region of the gate electrode in the high constant gate insulating film; and
the thickness of the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a lower region of the gate electrode in the high dielectric constant gate insulating film.
7. The semiconductor device according to claim 1, wherein:
a notch is provided at a side end portion of the high dielectric constant gate insulating film.
8. The semiconductor device according to claim 1, wherein:
a buffer insulating film is provided between the substrate and the high dielectric constant gate insulating film.
9. The semiconductor device according to claim 8, wherein:
the buffer insulating film is a silicon oxide film or a silicon oxynitride film.
10. The semiconductor device according to claim 1, wherein:
the gate electrode is a fully silicided gate electrode in which the entire region has undergone solicidation.

11. A method for manufacturing a semiconductor device, characterized in that:

the method comprises: step a, forming a high dielectric constant gate insulating film on the active region of the substrate;

step b, forming a gate electrode on the high dielectric constant gate insulating film;

step c, after step b, etching a portion of the high dielectric constant gate insulating film located outside the gate electrode to reduce the thickness of the portion; and

step d, after step c, forming insulating sidewalls on the side surfaces of the gate electrode.

12. The method for manufacturing a semiconductor device according to claim 11, wherein:

after the step d, the method further includes removing a portion of the high -dielectric constant gate insulating film located outside the insulating sidewall.

13. The method for manufacturing a semiconductor device according to claim 11, wherein:

the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall;

the above-mentioned step d includes step d1 and step d2. In the step d1, the above-mentioned first insulating side wall is formed on the side of the above-mentioned gate electrode. In the step d2, the above-mentioned second insulating side wall is formed on the side of the above-mentioned gate electrode by sandwiching the above-mentioned first insulating side wall.

14. The method for manufacturing a semiconductor device according to claim 13, wherein:

the step d1 and the step d2, a step of removing a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall is further included.

15. The method for manufacturing a semiconductor device according to claim 13, wherein:

the steps d1 and d2, a step of etching a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall to make the portion thinner is included;

after the step d2, the method further includes removing a portion of the high dielectric constant gate insulating film located outside the second insulating sidewall.

16. The method for manufacturing a semiconductor device according to any one of claims 12, 14 or 15, wherein:

the high dielectric constant gate insulating film is selectively removed by wet etching.

17. The method for manufacturing a semiconductor device according to claim 11, wherein:

step b includes forming a protective film covering the upper surface of said gate electrode; and after

said step d, the method further includes removing said protective film after silicideing the surface of said active region outside said insulating sidewall, and then silicideing the entire gate electrode.

18. The method for manufacturing a semiconductor device according to claim 11, further comprising:

before step a), forming a buffer insulating film on the active region;

wherein in step a, the high dielectric constant gate insulating film is formed on the active region with the buffer insulating film interposed therebetween.

Postal Code 100083 Zhongke Patent and Trademark Agency Co., Ltd. 25th Floor, Building B, Tsinghua Tongfang Technology Building, No. 1 Wangzhuang Road, Haidian District, Beijing Wang Huimin	Date of issue August 22, 2008
Application number: 2006100938722	
Applicant: Panasonic Corporation	
Invention Title: Semiconductor device and manufacturing method thereof	

Notice of Invention Patent Application Entering Substantive Examination Procedure

Regarding the above patent application, according to the substantive examination request filed by the applicant, after examination, it was found to be in compliance with the provisions of Article 35 of the Patent Law and Article 90 of the Implementing Regulations, and the patent application has entered the substantive examination procedure.

Reminder:

1. From the date of issuance of this notice, the application will enter the substantive application procedure. From then on, when the patent applicant submits various patent documents to the Patent Administration, the substantive examination procedure should be indicated on the documents.
2. In accordance with the provisions of Paragraph 1 of Article 51 of the Implementing Regulations of the Patent Law, an invention patent applicant may, within three months from the date of receipt of this notice issued by the Patent Administration, proactively propose amendments to the invention patent application.

3 Payments made by postal remittance should be made to: Recipient Name: State Intellectual Property Administration fee acceptance section, Merchant Customer Number: 110000860. Payments made by bank remittance should be made to: State Intellectual Property Administration of the People's Republic of China, Bank of deposit: Industrial and Commercial Bank of China, Beijing Beitaipingzhuang Branch, Account Number: 0200010009014400518. Please accurately indicate the application number, fee name, and itemized amount when making a remittance. Failure to specify the application number and/or fee name when making a payment will be deemed as incomplete payment.

Examiner: Liang Fang Examination department: Preliminary Review and Process Management Department

August 14, 2008

21231
2002.8

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Attention: China National Intellectual Property Administration
(Note: Any letter sent personally to the examiner shall have no legal effect)

Postal Code 100083 Zhongke Patent and Trademark Agency Co., Ltd. 25th Floor, Building B, Tsinghua Tongfang Technology Building, No. 1 Wangzhuang Road, Haidian District, Beijing Wang Huimin	Date of issue March 20, 2009
Application number: 2006100938722	
Applicant: Panasonic Corporation	
Invention Title: Semiconductor device and manufacturing method thereof	

Notice of First Examination Opinion

1. ☑ In response to the applicant's request for substantive examination, in accordance with the provisions of Paragraph 1 of Article 35 the Patent Law, the State Intellectual Property Administration conducted A substantive examination of the above-mentioned invention patent application.

☐ In accordance with the provisions of Paragraph 2 of Article 35 of the Patent Law, the State Intellectual Property Administration has decided to examine the above-mentioned invention patent application on its own.

2. ☑ The applicant requested that its:

JP Patent Office application date of August 5, 2005 be the priority date,
Patent Office application date of MM YY DD be the priority date,
Patent Office application date of MM YY DD be the priority date,

☑ The applicant in the country has submitted a copy of the first-filed prior application document certified by the receiving authority of the original application country.

☐ The applicant has not submitted a copy of the first application document certified by the receiving authority of the original application country, and it is deemed that no priority has been claimed in accordance with the provisions of Article 30 of the Patent Law.

3. ☑ The applicant submitted the amendment documents on August 5, 2008, and on MM DD YY.

After review, documents submitted by the applicant on MM DD YY do not comply with the requirements of the Paragraph 1 of Article 51 of the Implementing Regulations of the Patent Law.

☐

4. Application documents subject to review:

☐ Original application documents. ☑ The examination is for the following application documents:

Claim __ of the claims in the original application documents, page 1 to 2, 5 to 24 of the specification and page 1 to 11 of the accompanying drawings submitted on the application date;

Claim ___, page __ of the specification and page __ of the accompanying drawings submitted on the date of submission of the separate application;

Claims 1 to 18, page __ and accompanying drawings page __ submitted on August 5, 2008;

Claims ___, pages ___ of the specification and pages ___ of the accompanying drawings submitted on MM DD YY;

Claims ___, pages ___ of the specification and pages ___ of the accompanying drawings submitted on MM DD YY

Abstract of the specification submitted on the date of application and accompanying drawings of the abstract submitted on the date of application.

5. ☐ This notice was issued without conducting a search.
☑The national notice is issued after a search has been conducted.
☑ The following reference documents (their numbers will continue to be used in future examinations):

No.	Documents name or number	Publication date (or filing date of conflict application)
1	JP Patent No. 2005-64190A	March 10, 2005
2	CN1610129A	April 27, 2005
3	JP Patent No. 2004-356576A	December 16, 2004

6. Conclusive observations of the review:
☐ Regarding the specification:
☐ The content of the application falls within the scope of non-patentability stipulated in Article 5 of the Patent Law.
☐ The specification does not comply with the provisions of Paragraph 3 Article 26 of the Patent Law.
☐ The specification does not comply with the requirements of the provisions of Article 33 of the Patent Law.
☐ Preparation of the specification does not comply with the provisions of Article18 of the Implementing Regulations of the Patent Law.
☐
☑ Regarding the claims:
☑ Claims 1, 11 – 12 do not possess the novelty required by Paragraph 32of Article 22 of the Patent Law.
☑ Claims 2-4, 7-10, 13-14, and 16-18 do not possess the inventive step required by Paragraph 3 of Article 22 the Patent Law.
☐ Claims ____ do not have the utility required by Paragraph 4 of Article 22 the Patent Law.
☐ Claims ____ fall within the scope of non-patentability as stipulated in Article 25 of the Patent Law.
☐ Claims ____ do not comply with the provisions of Paragraph 4 of Article 26 of the Patent Law.
☐ Claims ____ do not comply with the provisions of Paragraph 1 of Article 31 of the Patent Law.
☐ Claims ____ do not comply with the provisions of Article 33 of the Patent Law.
☐ Claims ____ do not comply with the provisions of Paragraph 1 of Article 2 of the Implementing Regulations of the Patent Law.
☐ Claims ____ do not comply with the provisions of Paragraph 1 of Article 13of the Implementing Regulations of the Patent Law.
☑ Claim 16 does not comply with the provisions of Article 20 of the Implementing Regulations of the Patent Law.
☐ Claims ____ do not comply with the provisions of Article 21 of the Implementing Regulations of the Patent Law.
☐ Claims ____ do not comply with the provisions of Article 22 of the Implementing Regulations of the Patent Law.
☐ Claims ____ do not comply with the provisions of Article 23 of the Implementing Regulations of the Patent Law.
☐ _____
☐ The separate application does not comply with the provisions of Paragraph 1 of Article 43 of the Implementing Regulations of the Patent Law.
The detailed analysis of the above conclusive opinions can be found in the body text of this notice.
7. Based on the above conclusive opinions, the examiner believes that:
☐ The applicant should amend the application documents in accordance with the requirements set out in the body text of the notice.
☑ The applicant should explain in the statement of opinion the reasons why its patent application can be granted a patent right and amend the nonconforming part in the body text of the notice, otherwise the patent right will not be granted.
☐ The patent application does not contain substantial content that can be granted a patent right, and the applicant has failed to state the reasons or the reasons stated are insufficient. The application will be rejected.
☐ _____
8. Applicants should note the following:

(1) In accordance with the provisions of Article 37 of the Patent Law, the applicant shall state its opinion within six months from the date of receipt of this notice. If the applicant fails to respond within the time limit without justifiable reasons, its application shall be deemed to be withdrawn.
(2) The applicant's amendment to its application shall comply with the provisions of Article 33 of the Patent Law. The amendment text shall be made in duplicate copies and its format shall comply with the relevant provisions of the Examination Guidelines.
(3) The applicant's statement of opinion and/or amended text should be mailed or submitted to the Acceptance Office of the State Intellectual Property Administration. Any document not mailed or submitted to the Acceptance Office shall have no legal effect.
(4) Applicants and/or agents may not come to the Patent Administration of the State Intellectual Property Administration to meet with examiners without an appointment.

9. The body text of this notice consists of 5 pages, and is accompanied by the following attachments:

☑ A total of 3 photocopies and 59 pages the reference documents.

Examiner: Shao Ye (974K)
March 6, 2009 Examination department: Examination Cooperation Center

21301
2006.7

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Attention: China National Intellectual Property Administration
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on a dielectric film; and an insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on the side of the gate electrode, and the second insulating sidewall is formed on the side of the gate electrode with the first insulating sidewall sandwiched therebetween. The high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower sides of the first insulating sidewall and the second insulating sidewall. The thickness of the lower region of the first insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film. The thickness of the lower region of the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the first insulating sidewall in the high dielectric constant gate insulating film.

In the semiconductor device of the present invention, the insulating sidewalls are composed of a first insulating sidewall and a second insulating sidewall. The first insulating sidewall is formed on the side of the gate electrode, and the second insulating sidewall is formed on the side of the gate electrode, sandwiching the first insulating sidewall. The high constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the first insulating sidewall. The thickness of the high constant gate insulating film below the first insulating sidewall may be smaller than the thickness of the high constant gate insulating film below the gate electrode.

When the insulating sidewall is composed of the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may not be formed on the lower side of the second insulating sidewall.

When the insulating sidewalls are composed of the first insulating sidewalls and the second insulating sidewalls, the high constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the second insulating sidewall. The thickness of the lower region of the second insulating sidewall in the high constant gate insulating film may be equal to the thickness of the lower region of the first insulating sidewall in the high constant gate insulating film.

When the insulating sidewalls are composed of the first insulating sidewalls and the second insulating sidewalls, the high constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the second insulating sidewalls. The thickness of the lower region of the second insulating sidewall in the high constant gate insulating film may be smaller than the thickness of the lower region of the first insulating sidewall in the high constant gate insulating film.

In the semiconductor device of the present invention, the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall, the first insulating sidewall is formed on the side of the gate electrode, and the second insulating sidewall is formed on the side of the gate electrode sandwiching the first insulating sidewall. The high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the second insulating sidewall. The thickness of the lower region of the first insulating sidewall in the high dielectric constant gate insulating film is equal to the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film. The lower region of the second insulating sidewall in the high dielectric constant gate insulating film is equal to the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film. The thickness of the side region may be smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film.

In the semiconductor device of the present invention, a notch may be provided at a side end portion of the high dielectric constant gate insulating film.

In the semiconductor device of the present invention, a buffer insulating film may be provided between the substrate and the high dielectric constant gate insulating film. In this case, the buffer insulating film may be a silicon oxide film or a silicon oxynitride thin film.

In the semiconductor device of the present invention, the gate electrode may be a fully silicided gate electrode in which the entire region has undergone solicidation.

The method for manufacturing a semiconductor device according to the present invention comprises: step a, forming a high dielectric constant gate insulating film on an active region of a substrate; step b, forming a gate electrode on the high dielectric constant gate insulating film; step c, after step b, etching a portion of the high dielectric constant gate insulating film located outside the gate electrode to reduce the thickness of the portion; and step d, after step c, forming insulating sidewalls on the side surfaces of the gate electrode. The above-mentioned insulating side wall is composed of a first insulating side wall and a second insulating side wall; the above-mentioned step d includes a step d1 and a step d2, in which the above-mentioned first insulating side

wall is formed on the side of the above-mentioned gate electrode, and in the above-mentioned step d2, the above-mentioned second insulating side wall is formed on the side of the above-mentioned gate electrode with the above-mentioned first insulating side wall sandwiched therebetween. Between the above-mentioned step d1 and the above-mentioned step d2, the process includes etching the portion of the above-mentioned high dielectric constant gate insulating film located outside the above-mentioned first insulating side wall to make the portion thinner; after the above-mentioned step d2, the process also includes removing the portion of the above-mentioned high dielectric constant gate insulating film located outside the above-mentioned second insulating side wall.

The method for manufacturing a semiconductor device of the present invention may further include, after step d, a step of removing a portion of the high dielectric constant gate insulating film located outside the insulating sidewall.

In the semiconductor device manufacturing method of the present invention, the insulating sidewalls are composed of first and second insulating sidewalls. Step d includes step d1, in which the first insulating sidewalls are formed on the side surfaces of the gate electrode, and step d2, in which the second insulating sidewalls are formed on the side surfaces of the gate electrode with the first insulating sidewalls interposed therebetween.

When the step d includes the step d1 and the step d2, it may further include a step of removing a portion of the high dielectric constant gate insulating film located outside the first insulating side wall between the step d1 and the step d2.

When the step d includes the step d1 and the step d2, the step d1 and the step d2 include etching the portion of the high dielectric constant gate insulating film located outside the first insulating sidewall to make the portion thinner. After the step d2,

Claims

1. A semiconductor device, characterized in that:
the invention comprises: a high dielectric constant gate insulating film formed on the active region of the substrate,
a gate electrode formed on the high dielectric constant gate insulating film, and
an insulating sidewall comprising a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on a side surface of the gate electrode, and the second insulating sidewall is formed on a side surface of the gate electrode with the first insulating sidewall sandwiched therebetween;
the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower sides of the first insulating side wall and the second insulating side wall;
the thickness of first insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film; and
the thickness of a lower region of the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a lower region of the first insulating sidewall in the high dielectric constant gate insulating film.
2. The semiconductor device according to claim 1, wherein:
a notch is provided at a side end portion of the high dielectric constant gate insulating film.
3. The semiconductor device according to claim 1 or 2, wherein:
a buffer insulating film is provided between the substrate and the high dielectric constant gate insulating film.
4. The semiconductor device according to claim 3, wherein:
the buffer insulating film is a silicon oxide film or a silicon oxynitride film.
5. The semiconductor device according to claim 1, wherein:
the gate electrode is a fully silicided gate electrode in which the entire region has undergone solicidation.
6. A method for manufacturing a semiconductor device, characterized in that:
the method comprises: step a, forming a high dielectric constant gate insulating film on the active region of the substrate;
step b, forming a gate electrode on the high dielectric constant gate insulating film;
step c, after step b, etching a portion of the high dielectric constant gate insulating film located outside the gate electrode to reduce the thickness of the portion; and
step d, after step c, forming insulating sidewalls on the side of the gate electrode,
the insulating side wall is composed of a first insulating side wall and a second insulating side wall;
the step d includes a step d1 and a step d2. In the step d1, the first insulating sidewall is formed on the side of the gate electrode. In the step d2, the second insulating sidewall is formed on the side of the gate electrode with the first insulating sidewall interposed therebetween,
the steps d1 and d2, a step of etching a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall to make the portion thinner is included; and
the above step d2, the method further includes removing a portion of the high dielectric constant gate insulating film located outside the second insulating side wall.
7. The method for manufacturing a semiconductor device according to claim 6, wherein:
the high dielectric constant gate insulating film is selectively removed by wet etching.
8. The method for manufacturing a semiconductor device according to claim 6, wherein:
the step b includes forming a protective film covering the upper surface of the gate electrode; and
after the step d, the method further includes removing the protective film after silicideing the surface of the active region located outside the insulating sidewall, and then silicideing the entire gate electrode.
9. The method for manufacturing a semiconductor device according to claim 6, wherein:
the above step a, further comprising the step of forming a buffer insulating film on the active region; and
in the step a, the high dielectric constant gate insulating film is formed on the active region with the buffer insulating film interposed therebetween.

Postal Code 100083 Zhongke Patent and Trademark Agency Co., Ltd. 25th Floor, Building B, Tsinghua Tongfang Technology Building, No. 1 Wangzhuang Road, Haidian District, Beijing Wang Huimin	Date of issue The date of issuance of this authorization notice is the same as the date of the registration
Application number: 2006100938722	
Applicant: Panasonic Corporation	
Invention Title: Semiconductor device and manufacturing method thereof	

Notice of Grant of Invention Patent Right

1. In accordance with the provisions of Article 39 of the Patent Law and Article 54 of its Implementing Regulations, the above-mentioned invention patent application has been substantively examined and no grounds for rejection have been found. Notice of grant of patent right is hereby issued.

After receiving this notice, the applicant shall also go through the registration procedures in accordance with the contents of the notice on registration procedures.

After the applicant completes the registration procedures on time, the State Intellectual Property Administration will make a decision to grant the patent right, issue the invention patent certificate register and publish it.

Failure to complete the registration procedures before the expiration of the period will be deemed as a abandonment of the right to obtain the patent right.

2. ☐ The above invention patent application for which the patent right is granted is based on the documents submitted on the application date (MM DD YY).

The above invention patent application for which the patent right is granted is based on the following documents:

☑ Claim __ of the claims in the original application documents, pages 1 to 2, 5 to 24 of the specification and page 1 to 11 of the accompanying drawings submitted on the application date;

Claim ___, page __ of the specification and page __ of the accompanying drawings submitted on the date of submission of the separate application;

Claims 1 to 9, pages 3 to 4 and accompanying drawings page __ submitted on August 5, 2008;

Claims ___, pages ___ of the specification and pages ___ of the accompanying drawings submitted on MM DD YY;

Claims ___, pages ___ of the specification and pages ___ of the accompanying drawings submitted on MM DD YY

The abstract of the specification submitted on the application date, and the abstract drawings submitted on the application date.

3. Title of the patent application for the invention for which the patent right is granted:

☑ No change.

☐ Changed to the above name from _____.

4. The applicant submitted a "Statement of Abandonment of Patent Rights" with patent number on (MM DD YY) and upon examination:

☐ Has entered the procedure of abandoning patent rights.

☐ Has not entered the procedure for abandoning the patent right. The reason is: the patent that the applicant declares to have abandoned is not the same invention as the present invention patent application and complies with the provisions of Paragraph 1 Article 13 of the Implementing Regulations of the Patent Law.

5. The examiner ex officio has amended the application documents as follows:

6. Application documents amended by the applicant on its own initiative after the issuance of this notice will not be accepted.

Examiner: Shao Ye (974K)
October 10, 2009
Examination department: Review Collaboration Center

Please send reply to: 100088 No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing
Attention: China National Intellectual Property Administration
(Note: Any letter sent personally to the examiner shall have no legal effect)

Text of the first examination opinion notice

Application number: 200610093872.2

After review, the specific opinions are as follows:

1. Claim 1 seeks protection for a semiconductor device. Reference document 1 (JP-A-2005-64190A) has disclosed a semiconductor device and specifically has disclosed the following technical characteristics (see paragraphs 0076-0083 and Accompanying drawings 22-23 of reference document 1):

HfO2 gate insulating film 5 (equivalent to a high constant gate insulating film) is formed on the active region of substrate 1;

the gate electrode 6 is formed on the gate insulating film 5.

insulating sidewalls 10 are formed on the sides of the gate electrode 6;

the HfO2 gate insulating film 5 is continuously formed from the lower side of the gate electrode 6 to the lower side of the insulating side wall 10;

the thickness of at least a portion of the lower region of the insulating sidewall 10 in the HfO2 gate insulating film 5 is smaller than the thickness of the lower region of the gate electrode 6 in the HfO2 gate insulating film 5.

From here, it can be seen that all the technical characteristics of claim 1 have already been disclosed in D1. The technical solution claimed in claim 1 is identical to the technical solution disclosed in D1, is in the same field of semiconductor devices, solves the same technical problems, and is expected to achieve the same effect of preventing a decrease in the dielectric constant and insulation properties of the high constant gate insulating film in the gate electrode extreme portion. Therefore, the technical solution claimed in claim 1 does not possess novelty as provided for in Paragraph 32 of Article 22 of the Patent Law.

2. Claims 2 and 4 directly or indirectly refer to claim 1. It is a common practice in the art that the sidewall insulating film located on the sidewall of the gate, which is used to isolate the gate and the source and drain, is composed of two or three layers. On the basis of the technical solution disclosed in Figure 22 of the reference document 1, for certain practical needs of the process, those skilled in the art can, through conventional means (such as limited experiments), set the sidewall insulating film 10 in Figure 22 of the reference document 1 into two sidewall insulating films, that is, they can obtain the additional technical characteristics of claims 2 and 4: the sidewall insulating film 10 is set to be composed of a first insulating sidewall and a second insulating sidewall (<u>the third insulating sidewall is replaced by the second insulating sidewall by the HfO2 insulating film 10</u>), the first insulating sidewall is formed on the side of the above-mentioned gate electrode 6, and the second insulating sidewall is formed on the side of the above-mentioned gate electrode 6 by sandwiching the above-mentioned first insulating sidewall; at the same time, the HfO2 gate insulating film 5 (equivalent to the high constant gate insulating film) is continuously formed from the lower side of the gate electrode to the lower side of the first insulating side wall; the thickness of the lower region of the first insulating side wall of the HfO2 gate insulating film 5 (this thickness is equal to the thickness of the lower region of the insulating side wall 10 in the HfO2 gate insulating film 5) is smaller than the thickness of the lower region of the gate electrode 6 in the HfO2 gate insulating film 5 (equivalent to the additional technical characteristics of claim 2); the HfO2 gate insulating film 5 is continuously formed to the lower side of the second insulating side wall; the thickness of the lower region of the second insulating side wall in the HfO2 gate insulating film 5 is equal to the thickness of the lower region of the first insulating side wall in the HfO2 gate insulating film 5 (equivalent to the additional technical characteristics of claim 4).

When claim 1, directly or indirectly cited, lacks novelty, it is obvious to those skilled in the art that the technical solutions claimed in claims 2 and 4 can be obtained by combining conventional means with reference document 1 and conventional methods in the art. Therefore, the technical solutions claimed in claims 2 and 4 lack outstanding substantive characteristics and significant advancements, and do not possess the inventive step required by Paragraph 3 of Article 22 of the Patent Law.

3. Claims 2 and 3 directly or indirectly refer to claim 1. It is a common practice in the art that the sidewall insulating film located on the sidewall of the gate, which is used to isolate the gate and the source and drain, is composed of two or three layers. On the basis of the technical solution disclosed in Figure 22 of the reference document 1, for certain practical needs of the process, those skilled in the art can form another sidewall insulating film on the sidewall of the insulating sidewall 10 through conventional means (such as limited experiments), that is, they can obtain the additional technical characteristics of claims 2 and 3: that is, the insulating sidewall of the semiconductor device is composed of the insulating sidewall 10 (the first insulating sidewall) and another sidewall insulating film (the second insulating sidewall) located on the first insulating sidewall, the first insulating sidewall is formed on the side of the above-mentioned gate electrode 6, and the

second insulating sidewall is formed on the side of the above-mentioned gate electrode 6 by sandwiching the above-mentioned first insulating sidewall; at the same time, the HfO2 gate insulating film 5 (equivalent to a high constant gate insulating film) is continuously formed from the lower side of the above-mentioned gate electrode to the lower side of the above-mentioned first insulating side wall; the thickness of the lower side region of the above-mentioned first insulating side wall of the above-mentioned HfO2 gate insulating film 5 (the thickness is equal to the thickness of the lower side region of the above-mentioned insulating side wall 10 in the above-mentioned HfO2 gate insulating film 5) is smaller than the thickness of the lower side region of the above-mentioned gate electrode 6 in the above-mentioned HfO2 gate insulating film 5 (equivalent to the additional technical characteristics of claim 2); the above-mentioned HfO2 gate insulating film 5 is not formed on the lower side of the above-mentioned second insulating side wall (equivalent to the additional technical characteristics of claim 3).

When claim 1, directly or indirectly cited, lacks novelty, it is obvious to those skilled in the art that the technical solutions claimed in claims 2 and 3 can be obtained by combining conventional means with reference document 1 and conventional methods in the art. Therefore, the technical solutions claimed in claims 2 and 3 lack outstanding substantive characteristics and significant advancements, and do not possess the inventive step required by Paragraph 3 of Article 22 of the Patent Law.

4. Claim 7 is a dependent claim of claim 1. Reference document 2 (CN1610129A) has disclosed a semiconductor device in the technical solution of Figure 2, in which notches 8 and 9 are formed in the insulating layer 2 to reduce the overlap between the gate 3 and the source and drain 4, 5, so as to achieve the purpose of reducing parasitic capacitance (see pages 4-7 of the specification, Figure 2). It can be seen that reference document 2 provides the inspiration for further applying the technical means of setting notches in the side walls of the gate insulating layer to the technical solution of reference document 1. On the basis of this inspiration, those skilled in the art will certainly be able to obtain the characteristics of setting notches in the side ends of the HfO2 gate insulating film 5 (equivalent to the high constant gate insulating film) in reference document 1. When the cited claim 1 does not have novelty, on the basis of reference document 1, it is obvious to those skilled in the art to obtain the technical solution claimed in claim 7 by combining the above with reference document 2. Therefore, the technical solution claimed in claim 7 does not possess outstanding substantive characteristics or significant advancements, and does not possess the inventive step required by Paragraph 3 of Article 22 of the Patent Law.

5. Claim 8 is a dependent claim of claim 1. Reference document 3 (JP-A-2004-356576A) has disclosed a semiconductor device in the technical solution of Figure 1, wherein a buffer insulating film 6 is disposed between a substrate and a high constant gate insulating film 7. This indicates that the additional technical characteristics of this claim have already been disclosed in reference document 3, and that these characteristics serve the same function in reference document 3 as in this application, both preventing degradation of the interface between the substrate and the gate insulating film. In other words, reference document 3 suggests applying these characteristics to the technical solution of reference document 1 to further address its technical problem. When the cited claim 1 lacks novelty, it is obvious to those skilled in the art that the technical solution claimed in claim 8 can be derived by combining reference document 1 with reference document 3. Therefore, the technical solution claimed in claim 8 lacks outstanding substantive characteristics and significant advancements, and does not possess the inventive step required by Paragraph 3 of Article 22.

6. Claim 9 is a dependent claim of claim 8. Its additional technical characteristics have been disclosed in Reference document 3 (see paragraph 0030): namely, buffer insulating film 6 is a cinnabar oxide film. When the cited claims lack inventive steps, the technical solution claimed in claim 9 lacks inventive steps as provided for in Paragraph 3 of Article 22 of the Patent Law.

7. Claim 10 is a dependent claim of claim 1. Forming a metal cinnamate layer on the surface of the source, drain, and gate to reduce contact resistance is a common practice in the art; that is, this additional technical characteristic is a common practice in the art. If the cited claim 1 lacks novelty, the technical solution claimed in claim 10 lacks the inventive step required by Paragraph 3 of Article 22 of the Patent Law.

8. Claim 11 seeks protection for a method for manufacturing a semiconductor device. Reference document 1 (JP-A-2005-64190A) has disclosed a method for manufacturing a semiconductor device and specifically has disclosed the following technical characteristics (see paragraphs 0076-0083 and accompanying drawings 19-23 of reference document 1): including:

step a: forming a HfO2 gate insulating film 5 (equivalent to a high constant gate insulating film) on the active region of the substrate 1;

step b, forming a gate electrode 6 on the gate insulating film 5;

step c, after step b, etching a portion of the gate insulating film 5 located outside the gate electrode 6 to reduce the thickness of the portion;

step d: After step c, forming insulating sidewalls 10 on the side surfaces of the gate electrode 6.

It can be seen that all the technical characteristics of claim 11 have been disclosed in the reference document 1, and the technical solution claimed is the same as the technical solution disclosed in the reference document 1, and is in the same field of semiconductor device manufacturing method. The technical problems they solve are the same, and their expected effects of preventing a decrease in the dielectric constant and insulation properties of high constant gate insulating films in the gate electrode extremes are the same. Therefore, the technical solution claimed in claim 11 does not possess the novelty required by Paragraph 2 of Article 22 of the Patent Law.

9. Claim 12 is a dependent claim of claim 11. Its additional technical characteristics have been disclosed in Figure 22 of Reference document 1: namely, after step d, it includes a step of removing the portion of HfO2 gate insulating film 5 located outside the insulating sidewall 10. If the cited claim 11 lacks novelty, the technical solution claimed in claim 12 does not possess novelty as provided for in Paragraph 32 of Article 22 of the Patent Law.

10. Claims 13-14 directly or indirectly refer to claim 11. It is a common practice in the art that the sidewall insulating film located on the sidewall of the gate, which is used to isolate the gate and the source and drain, is composed of two or three layers. On the basis of the technical solution disclosed in Figure 22 of the reference document 1, for certain practical needs of the process, a person skilled in the art can form another sidewall insulating film on the sidewall of the insulating sidewall 10 by conventional means (such as a limited number of experiments), that is, the additional technical characteristics of claim 13 can be obtained: that is, the insulating sidewall of the semiconductor device is composed of the insulating sidewall 10 (the first insulating sidewall) and the other sidewall insulating film (the second insulating sidewall) located on the first insulating sidewall, and the above-mentioned step d of forming the insulating sidewall includes step d1 and step d2. In step d1, the first insulating sidewall is first formed on the side of the gate electrode 6, and then in step d2, the above-mentioned second insulating sidewall is formed on the side of the gate electrode 6 by sandwiching the above -mentioned first insulating sidewall; and the reference document has disclosed in paragraph 0079 that the insulating sidewall 10 is first etched to form the insulating sidewall. After the first insulating sidewall is formed, the portion of the HfO2 gate insulating film 5 located outside the insulating sidewall 10 is etched away. A person skilled in the art can obtain the step d2 (the additional technical characteristics of claim 14) of forming the second insulating sidewall after the portion of the HfO2 gate insulating film 5 located outside the insulating sidewall 10 is etched away by conventional means (such as a limited number of experiments).

When claim 11, directly or indirectly cited, lacks novelty, it is obvious to those skilled in the art that the technical solutions claimed in claims 13-14 can be obtained by combining conventional means with reference document 1 and conventional methods. Therefore, the technical solutions claimed in claims 13-14 lack outstanding substantive characteristics and significant advancements, and do not possess the inventive step required by Paragraph 3 of Article 22 of the Patent Law.

11. Claim 16 refers to claim 12, 14, or 15. Wet etching is a conventional etching method, meaning that this additional technical characteristic is a customary method in the art. If the reference document claim 12 lacks novelty or the reference document claim 14 lacks inventive steps, the technical solution claimed in claim 16 lacks inventive steps as defined in Paragraph 3 of Article 22 of the Patent Law.

12. Claim 17 is a dependent claim of claim 11. Part of the additional technical characteristics thereof is "the above-mentioned step b includes the step of forming a protective film covering the upper surface of the above-mentioned gate electrode, and after step d, the process of also including the step of halogenating the surface of the above-mentioned active region located outside the above-mentioned insulating side wall" has been disclosed in accompanying drawings 19-23 of the reference document 1: that is, the above-mentioned process b includes the process of forming a protective film 13 covering the upper surface of the above-mentioned gate electrode 6, and after step d, it also includes the process of halogenating the surface of the above-mentioned active region located outside the above-mentioned insulating side wall 10; as for the other characteristics of the additional technical characteristics "removing the protective film, including the process of halogenating the entire gate electrode", these can be obtained by those skilled in the art through logical reasoning and analysis, because in order to reduce contact resistance, forming a halogenated layer on the gate is a common means, and in order to form the halogenated layer, the protective film located on the gate must be removed first.

When the cited claim 11 does not possess novelty, the technical solution sought to be protected by claim 17 does not possess the inventive steps stipulated in Paragraph 3 of Article 22 of the Patent Law.

13. Claim 18 is a dependent claim of claim 11. Reference document 3 (JP-A-2004-356576A) has disclosed a method for manufacturing a semiconductor device in the technical solution shown in Figure 1, wherein, before forming a high constant insulating film 7 in the active region of a substrate (equivalent to step a), a buffer insulating film 6 is formed on the active region. In the step of forming the high constant insulating film 7, the high constant insulating film 7 is formed on the active region, sandwiching the buffer insulating film 6. Clearly, the additional technical characteristics of this claim have been disclosed in reference document 3, and the function of this characteristic in reference document 3 is the same as in the present application, both preventing degradation of the interface between the substrate and the gate insulating film. In other words, reference document 3 provides a suggestion for applying this characteristic to the technical solution of reference document 1 to further address its technical problem. If the cited claim 11 lacks novelty, it would be obvious to those skilled in the art to combine reference document 1 with reference document 3 to arrive at the technical solution claimed in claim 18. Therefore, the technical solution sought to be protected in claim 18 does not possess outstanding substantive characteristics and significant progress, and does not possess the creativity required by Paragraph 3 of Article 22 of the Patent Law.

14. "According to any one of claims 12, 14, or 15" appearing in **claim 16** is unclear and does not comply with Paragraph 1 of Article 20 of the Implementing Regulations of the Patent Law. If it is intended to be a selective reference document, consideration may be given to amend it to "according to any of claims 12, 14, or 15" or "according to any one of claims 12, 14, and 15."

Based on the above reasons, this application cannot be granted a patent as currently drafted. If the applicant amends the application in accordance with the examination opinions set forth in this notice within the four-month response period specified in this notice and overcomes the existing deficiencies, this application may be granted a patent. Applicants are advised that amendments to the application must comply with the provisions of Article 33 of the Patent Law and must not exceed the scope of the original specification and claims.

The amended documents submitted by the applicant should include: an amended reference document page with revision marks and a newly printed replacement page (in duplicate), ensuring the consistency of the contents of the two parts. The applicant should also explain the basis for the amendment.

Examiner: Shao Ye Code: 974K

Phone: (010) 62413923

Claims

1. A semiconductor device, characterized in that:

compriseing: a high dielectric constant gate insulating film formed on the active region of the substrate,

a gate electrode formed on the high dielectric constant gate insulating film, and

insulating sidewalls, comprising a first insulating sidewall and a second insulating sidewall, the first insulating sidewall being formed on the side of the gate electrode, the second insulating sidewall being formed on the side of the gate electrode sandwiching the first insulating sidewall;

the high dielectric constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower sides of the first insulating sidewall and the second insulating sidewall ~~insulating sidewall~~;

the thickness of ~~at least a portion of~~ the lower region of the first insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film,

the thickness of a lower region of the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of a lower region of the first insulating sidewall in the high dielectric constant gate insulating film.

~~2. The semiconductor device according to claim 1, characterized in that:~~

~~the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on the side of the gate electrode, and the second insulating sidewall sandwiches the first insulating sidewall;~~

~~the high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the first insulating layer; and~~

~~the thickness of the first insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film.~~

~~3. The semiconductor device according to claim 2, characterized in that:~~

~~the high dielectric constant gate insulating film is not formed on the lower surface of the insulating sidewall.~~

~~4. The semiconductor device according to claim 2, characterized in that:~~

~~the high dielectric constant gate insulating film is continuously formed to the lower side of the second insulating sidewall; and~~

~~the thickness of the lower side region of the second insulating sidewall in the high dielectric constant gate insulating film is equal to the thickness of the high dielectric constant gate insulating film in the lower region of the first insulating side.~~

~~5. The semiconductor device according to claim 2, characterized in that:~~

~~the high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the second insulating sidewall;~~

~~the thickness of the lower side region of the second insulating sidewall region of the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the insulating sidewall of the high dielectric constant gate insulating film.~~

~~6. The semiconductor device according to claim 1, characterized in that:~~

~~the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall, wherein the first insulating sidewall is formed on the side of the gate electrode, and the second insulating sidewall is formed on the side of the gate electrode with the first insulating sidewall sandwiched therebetween;~~

~~the high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the first insulating side wall;~~

~~the thickness of the first insulating sidewall in the high dielectric constant gate insulating film is equal to the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film; and~~

~~the thickness of the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film.~~

~~7~~2. The semiconductor device according to claim 1, characterized in that:

a notch is provided at a side end portion of the high dielectric constant gate insulating film.

~~8~~3. The semiconductor device according to claim 1 or 2, characterized in that:

a buffer insulating film is provided between the substrate and the high dielectric constant gate insulating film.

~~9~~4. The semiconductor device according to claim 1, wherein:

the buffer insulating film is a silicon oxide film or a silicon oxynitride film.

~~10~~5. The semiconductor device according to claim 1, wherein:

the gate electrode is a fully silicided gate electrode in which the entire region has undergone solicidation.

~~11~~6. A method for manufacturing a semiconductor device, characterized in that:

compriseing: step a, forming a high dielectric constant gate insulating film on the active region of the substrate;

step b, forming a gate electrode on the high dielectric constant gate insulating film;

step C, after step b, etching a portion of the high dielectric constant gate insulating film located outside the gate electrode to reduce the thickness of the portion; and

step d, after step C, forming insulating sidewalls on the side surfaces of the gate electrode,

wherein the insulating sidewalls are composed of a first insulating sidewall and a second insulating sidewall;

the step d includes a step d1 and a step d2. In the step d1, the first insulating sidewall is formed on the side of the gate electrode. In the step d2, the second insulating sidewall is formed on the side of the gate electrode with the first insulating sidewall interposed therebetween,

the steps d1 and d2, a step of etching a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall to make the portion thinner is included; and

the above step d2, the method further includes removing a portion of the high dielectric constant gate insulating film located outside the second insulating side wall.

~~12. The method for manufacturing a semiconductor device according to claim 11, which is characterized in that:~~

~~after the above d, including a step of removing a portion of the high dielectric constant gate insulating film located outside the insulating wall.~~

~~13. The method for manufacturing a semiconductor device according to claim 11, which is characterized in that:~~

~~the insulating side wall is composed of a first insulating side wall and a second insulating side wall;~~

~~the above-mentioned step 4 includes step d1 and step d2. In step d1, the first insulating sidewall is formed on the side surface of the gate electrode. In step d2, the second insulating sidewall is formed on the side surface of the gate electrode, sandwiching the first insulating sidewall.~~

~~14. The method for manufacturing a semiconductor device according to claim 13, which is characterized in that:~~

~~between the above-mentioned step d1 and the above-mentioned step d2, a step L a further step is included of removing a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall.~~

~~15. The method for manufacturing a semiconductor device according to claim 13, which is characterized in that:~~

~~between step d1 and step d2, a step of etching a portion of the high dielectric constant gate insulating film located outside the first insulating sidewall to make the portion thinner is included.~~

~~16~~7. The method for manufacturing a semiconductor device according to claim 6 ~~any one of claims 12, 14 or 15~~, which is characterized in that:

the high dielectric constant gate insulating film is selectively removed by wet etching.

~~17~~8. The method for manufacturing a semiconductor device according to claim 1, which is characterized in that:

the step b includes forming a protective film covering the upper surface of the gate electrode;

after the step d, the method further includes the step of silicideing the surface of the active region located outside the insulating sidewall, removing the protective film, and then silicideing the entire gate electrode.

~~18~~9. The method for manufacturing a semiconductor device according to claim 1, which is characterized in that:

before the step a, it also includes a step of forming a buffer insulating film on the active region; and

in step a, forming the high dielectric constant gate insulating film on the active region with the buffer insulating film interposed therebetween.

on insulating film; and insulating sidewalls are composed of a first insulating sidewall and a second insulating sidewall, the first insulating sidewall being formed on the side of the gate electrode, and the second insulating sidewall being formed on the side of the gate electrode with the first insulating sidewall sandwiched therebetween ~~formed on the side of the gate electrode~~. The high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower sides of the first insulating sidewall and the second insulating sidewall ~~insulating sidewall~~. The thickness of ~~at least a portion~~ of the lower region of the first insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film. The thickness of the lower region of the second insulating sidewall in the high dielectric constant gate insulating film is smaller than the thickness of the lower region of the first insulating sidewall in the high dielectric constant gate insulating film.

In the semiconductor device of the present invention, the insulating sidewalls are composed of a first insulating sidewall and a second insulating sidewall. The first insulating sidewall is formed on the side of the gate electrode, and the second insulating sidewall is formed on the side of the gate electrode, sandwiching the first insulating sidewall. The high constant gate insulating film is formed continuously from the bottom of the gate electrode to the bottom of the first insulating sidewall. The thickness of the high constant gate insulating film below the first insulating sidewall may also be smaller than the thickness of the high constant gate insulating film below the gate electrode.

When the insulating sidewall is composed of the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may not be formed on the lower side of the second insulating sidewall.

When the insulating sidewalls are composed of the first insulating sidewalls and the second insulating sidewalls, the high constant gate insulating film is continuously formed from the lower side of the gate electrode to the lower side of the second insulating sidewall. The thickness of the lower region of the second insulating sidewall in the high constant gate insulating film may be equal to the thickness of the lower region of the first insulating sidewall in the high constant gate insulating film.

When the insulating sidewalls are composed of the first insulating sidewalls and the second insulating sidewalls, the high constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the second insulating sidewalls. The thickness of the lower region of the second insulating sidewall in the high constant gate insulating film may be smaller than the thickness of the lower region of the first insulating sidewall in the high constant gate insulating film.

In the semiconductor device of the present invention, the insulating sidewall is composed of a first insulating sidewall and a second insulating sidewall, the first insulating sidewall is formed on the side of the gate electrode, and the second insulating sidewall is formed on the side of the gate electrode sandwiching the first insulating sidewall. The high dielectric constant gate insulating film is formed continuously from the lower side of the gate electrode to the lower side of the second insulating sidewall. The thickness of the lower region of the first insulating sidewall in the high dielectric constant gate insulating film is equal to the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film. The lower region of the second insulating sidewall in the high dielectric constant gate insulating film is equal to the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film. The thickness

of the side region may be smaller than the thickness of the lower region of the gate electrode in the high dielectric constant gate insulating film.

In the semiconductor device of the present invention, a notch may be provided at a side end portion of the high dielectric constant gate insulating film.

In the semiconductor device of the present invention, a buffer insulating film may be provided between the substrate and the high dielectric constant gate insulating film. In this case, the buffer insulating film may be a silicon oxide film or a silicon oxynitride thin film.

In the semiconductor device of the present invention, the gate electrode may be a fully silicided gate electrode in which the entire region has undergone solicidation.

The method for manufacturing a semiconductor device according to the present invention comprises: step a, forming a high dielectric constant gate insulating film on an active region of a substrate; step b, forming a gate electrode on the high dielectric constant gate insulating film; step c, after step b, etching a portion of the high dielectric constant gate insulating film located outside the gate electrode to reduce the thickness of the portion; and step d, after step c, forming insulating sidewalls on the side surfaces of the gate electrode, the insulating sidewalls being composed of a first insulating sidewall and a second insulating sidewall; step d comprises step d1 and step d2, in which the first insulating side wall is formed on the side of the gate electrode in step d1, and the second insulating side wall is formed on the side of the gate electrode with the first insulating side wall sandwiched therebetween, and between step d1 and step d2, a process is included for etching a portion of the high dielectric constant gate insulating film located outside the first insulating side wall to make the portion thinner; and after step d2, a process is also included for removing a portion of the high dielectric constant gate insulating film located outside the second insulating side wall.

The method for manufacturing a semiconductor device of the present invention may further include, after step d, a step of removing a portion of the high dielectric constant gate insulating film located outside the insulating sidewall.

In the semiconductor device manufacturing method of the present invention, the insulating sidewalls are composed of first and second insulating sidewalls. Step d includes step d1, in which the first insulating sidewalls are formed on the side surfaces of the gate electrode, and step d2, in which the second insulating sidewalls are formed on the side surfaces of the gate electrode with the first insulating sidewalls interposed therebetween.

When the step d includes the step d1 and the step d2, it may further include a step of removing a portion of the high dielectric constant gate insulating film located outside the first insulating side wall between the step d1 and the step d2.

When the step d includes the step d1 and the step d2, between the step d1 and the step d2, a step is included to etch the portion of the high dielectric constant gate insulating film located outside the first insulating sidewall to make the portion thinner. After the step d2,

Statement of Opinion

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<table>
<tr><td rowspan="3">① Patent application or patent</td><td colspan="2">Application number or patent number 200610093872.2 Date of application June 20, 2006</td></tr>
<tr><td colspan="2">Name of the invention: Semi conductor device and manufacturing method thereof [Bar code: 061938722]</td></tr>
<tr><td>Parties</td><td>☒ Name of applicant or patentee (representative) Panasonic Corporation
☐ Revocation of patent rights requester name (representative)
☐</td></tr>
<tr><td colspan="2">② In response to the notice of the first examination opinion made by the Patent Administration on March 20, 2009, the following statement of our opinion is hereby presented:</td><td>☒ Patent application
☐ Patent</td></tr>
<tr><td colspan="3">See attached page for details
If you have any questions, please contact our agent:
Contact: Li Guiliang
Tel: 82378686-6291
Thank you for your cooperation!</td></tr>
<tr><td colspan="3">③ List of attachments:
2 pages of replacement pages for the claims, 2 pages of replacement pages for pages 3-4 of the specification, 8 pages of the replacement pages in total in duplicate, and 6 pages of reference document attachments.</td></tr>
<tr><td colspan="2">④ Seal of the applicant or agency
[seal: CHINA SCIENCE PATENT & TRADEMARK AGENT LTD]
August 3, 2009</td><td>⑤ Handling the opinion of the Patent Administration
[seal: seal for pro forma examination (00–33)
MM DD YY</td></tr>
</table>

Statement of opinion

The applicant received the examiner's first office action dated March 20, 2009 regarding this application (Application No. 2006100938722). In response to the examiner's opinion, the applicant conducted an in-depth study of its application documents and references, amended the corresponding portions of its claims and specification (see the amendment reference page for details), and presents its opinions as follows.

Regarding the opinion of the examiner that claims 1 and 11-12 of this application lack novelty, and that claims 2-4, 7-10, 13-14, and 16-18 lack inventiveness, the applicant has amended its claims by adding the additional technical characteristics from the original claim 2 and claim 5, which the examiner did not identify as having an inventiveness problem, to the original claim 1, forming a new claim 1. Similarly, the applicant added the additional technical characteristics from the original claim 13 and claim 15, which the examiner did not identify as having an inventiveness problem, to the original claim 11, forming a new independent method claim 6. At the same time, the applicant has deleted original claims 2-6 and 12-15, and reordered the remaining claims (see the amendment reference page for details). The applicant believes that these amendments do not exceed the original claims and description and comply with the provisions of Article 33 of the Patent Law.

Through amendments to the claims, the applicant argues that at least the additional technical characteristics of original claim 5 in the technical solution of amended claim 1, as well as the technical solution as a whole, are not disclosed or implied in any of the references 1-3 identified by the examiner. Furthermore, the combination of references 1-3 is unlikely to achieve the technical effects achievable by the aforementioned technical solution. Therefore, the amended claim 1 of the present invention possesses outstanding substantive characteristics and significant advancements relative to these references and their combinations. It possesses novelty as provided for in Paragraph 2 of Article 22 of the Chinese Patent Law relative to reference 1, and inventive step as provided for in Paragraph 3 of Article 22 of the Patent Law relative to references 1-3 and their combinations.

By the same token, the amended claim 6 possesses novelty as provided for in Paragraph 2 of Article 22, of the Patent Law relative to reference 1, and possesses inventiveness as provided for in Paragraph 3 of Article 22 of the Patent Law relative to references 1-3 and their combination. Furthermore, since the remaining claims of this invention are all dependent claims that reference claim 1 or claim 6, if claims 1 and 6 possess inventiveness, the remaining claims naturally also possess inventiveness.

Furthermore, in response to the examiner's comments regarding the original claim 16 (amended claim 7), the applicant modified its reference relationship, overcoming the issues identified by the examiner.

I hope the examiner will continue to examine this application based on the above amendments and hope that it will be granted a patent as soon as possible.

Amendment Notes

Pursuant to Article 51 of the Implementing Regulations of the Chinese Patent Law, the applicant has proactively amended the claims. The specific amendments are as follows: The phrase "partial thickness" in line 8 of claim 1 has been amended to read "thickness of a part." The above amendments do not exceed the scope of the original disclosure and are acceptance by the examiner is requested.

The above amendments shall be submitted in the form of replacement pages.

6

权 利 要 求 书

1、一种半导体装置，其特征在于：

包括：高介电常数栅极绝缘膜，形成在衬底的活性区域上，

栅极电极，形成在上述高介电常数栅极绝缘膜上，以及

绝缘性侧壁，形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述绝缘性侧壁的下侧区域的至少一部分厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

2、根据权利要求 1 所述的半导体装置，其特征在于：

上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成，该第 1 绝缘性侧壁形成在上述栅极电极的侧面，该第 2 绝缘性侧壁夹着上述第 1 绝缘性侧壁形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 1 绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

3、根据权利要求 2 所述的半导体装置，其特征在于：

上述高介电常数栅极绝缘膜没有形成在上述第 2 绝缘性侧壁的下侧。

4、根据权利要求 2 所述的半导体装置，其特征在于：

上述高介电常数栅极绝缘膜连续形成到上述第 2 绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下侧区域的厚度，与上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度相等。

5、根据权利要求 2 所述的半导体装置，其特征在于：

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 2 绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度。

6、根据权利要求1所述的半导体装置，其特征在于：

上述绝缘性侧壁由第1绝缘性侧壁和第2绝缘性侧壁构成，该第1绝缘性侧壁形成在上述栅极电极的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第2绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度，与上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度相等；

上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度,小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

7、根据权利要求1所述的半导体装置，其特征在于：

在上述高介电常数栅极绝缘膜的侧端部设置有缺口。

8、根据权利要求1所述的半导体装置，其特征在于：

在上述衬底和上述高介电常数栅极绝缘膜之间设置有缓冲绝缘膜。

9、根据权利要求8所述的半导体装置，其特征在于：

上述缓冲绝缘膜是氧化硅膜或氧氮化硅膜。

10、根据权利要求1所述的半导体装置，其特征在于：

上述栅极电极是整个区域被硅化物化的全硅化物栅极电极。

11、一种半导体装置的制造方法，其特征在于：

包括：工序a，在衬底的活性区域上形成高介电常数栅极绝缘膜；

工序b，在上述高介电常数栅极绝缘膜上形成栅极电极；

工序c，在上述工序b之后，将位于上述栅极电极外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分的厚度变薄；以及

工序d，在上述工序c之后，在上述栅极电极的侧面形成绝缘性侧壁。

12、根据权利要求11所述的半导体装置的制造方法，其特征在于：

在上述工序d之后，包括将位于上述绝缘性侧壁外侧的上述高介电常

数栅极绝缘膜的部分除去的工序。

13、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：

上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成；

上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁。

14、根据权利要求 13 所述的半导体装置的制造方法，其特征在于：

在上述工序 d1 和上述工序 d2 之间，还包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

15、根据权利要求 13 所述的半导体装置的制造方法，其特征在于：

在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序；

在上述工序 d2 之后，还包括将位于上述第 2 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

16、根据权利要求 12、14 或 15 中的任意一项所述的半导体装置的制造方法，其特征在于：

上述高介电常数栅极绝缘膜的除去是利用湿蚀刻法选择性地进行的。

17、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：

上述工序 b 含有形成覆盖上述栅极电极的上表面的保护膜的工序；

在上述工序 d 之后，还包括在将位于上述绝缘性侧壁外侧的上述活性区域的表面硅化物化后，将上述保护膜除去，然后，使上述栅极电极全部硅化物化的工序。

18、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：

在上述工序 a 之前，还包括在上述活性区域上形成缓冲绝缘膜的工序；

在上述工序 a 中，夹着上述缓冲绝缘膜在上述活性区域上形成上述高介电常数栅极绝缘膜。

中华人民共和国国家知识产权局

邮政编码：100083 北京市海淀区王庄路1号清华同方科技大厦B座25层 中科专利商标代理有限责任公司 汪惠民	发文日期 2006年8月25日
申请号：2006100938722	

申请人：松下电器产业株式会社

发明创造名称：半导体装置及其制造方法

发明专利申请初步审查合格通知书

1.上述专利申请经初步审查,符合专利法及其实施细则的规定。

2.根据专利法第三十四条规定,上述专利申请自申请日起满十八个月即行公布。

初审合格的上述发明专利申请是以：

2006-6-20提交的说明书：1至24页；

2006-6-20提交的权利要求书：1至3页；

2006-6-20提交的说明书附图：1至11页 为基础的。

提示：

发明专利申请人可以自申请日起三年内，提出实审请求，并同时缴纳审查费，申请人逾期不请求实质审查的或逾期不缴纳审查费的，该申请即被视为撤回。

审查员：毕春生　　审查部门：初审及流程管理部

2006年8月16日

中华人民共和国国家知识产权局

100083 北京市海淀区王庄路1号清华同方科技大厦B座25层 中科专利商标代理有限责任公司 汪惠民	发文日期 2007年02月16日
申请号：2006100938722	

申请人：松下电器产业株式会社

发明创造名称：半导体装置及其制造方法

发明专利申请公布通知书

上述专利申请，经初步审查符合专利法及其实施细则的有关规定，根据专利法第三十四条规定，该申请已在第23卷，第06期发明专利公报上予以公布。

注：附公布说明书一份。

提示：

发明专利申请人可以自申请日起三年内提出实审请求，并同时缴纳审查费，申请人逾期不请求实质审查的或逾期不缴纳审查费的，该申请被视为撤回。

根据专利法实施细则第九十一条规定，凡向专利局缴纳各种费用的应写明正确的申请号或专利号以及费用名称，未写明的视为未办理缴费手续。

审查员：金莉　　审查部门：初审及流程管理部

2007年2月8日

电子扫描7

实质审查请求书

20080805

请按照本表背面“填表注意事项”正确填写本表各栏　　IA063392

① 专利申请	申请号 200610093872.2	申请日 2006.06.20
	发明创造名称	半导体装置及其制造方法
	申请人（代表）	松下电器产业株式会社

② 请求内容

根据专利法第三十五条规定，请求对上述专利申请进行实质性审查

③ 附件清单

☐申请日前与本发明有关的参考资料
☐外国对该申请检索到的资料
☐外国对该申请审查结果的资料
☐

061938722

④ 备注

☒需要专利局复印审查通知书中列举的对比文献
☒目前尚未收到外国对该申请的检索资料和审查结果的资料
☐目前尚未收到申请日前与本发明有关的参考资料
☐本国际申请的国际检索局为 *JP/EP/SE*

⑤ 申请文件替换页

权利要求书 2 份共 6 页

⑥ 申请人或代理机构签章	⑦ 专利局处理意见
CHINA SCIENCE PATENT & TRADEMARK AGENT LTD 中国专利商标代理有限责任公司 申请专用 2008 年 8 月 5 日	年　月　日

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电子扫描7

权 利 要 求 书

1、一种半导体装置，其特征在于：

包括：高介电常数栅极绝缘膜，形成在衬底的活性区域上，

栅极电极，形成在上述高介电常数栅极绝缘膜上，以及

绝缘性侧壁，形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述绝缘性侧壁的下侧区域的至少一部分的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

2、根据权利要求1所述的半导体装置，其特征在于：

上述绝缘性侧壁由第1绝缘性侧壁和第2绝缘性侧壁构成，该第1绝缘性侧壁形成在上述栅极电极的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第1绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

3、根据权利要求2所述的半导体装置，其特征在于：

上述高介电常数栅极绝缘膜没有形成在上述第2绝缘性侧壁的下侧。

4、根据权利要求2所述的半导体装置，其特征在于：

上述高介电常数栅极绝缘膜连续形成到上述第2绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，与上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度相等。

5、根据权利要求2所述的半导体装置，其特征在于：

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第2绝缘性侧壁的下侧；

电子扫描7

上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度。

6、根据权利要求1所述的半导体装置，其特征在于：

上述绝缘性侧壁由第1绝缘性侧壁和第2绝缘性侧壁构成，该第1绝缘性侧壁形成在上述栅极电极的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第2绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度，与上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度相等；

上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

7、根据权利要求1所述的半导体装置，其特征在于：

在上述高介电常数栅极绝缘膜的侧端部设置有缺口。

8、根据权利要求1所述的半导体装置，其特征在于：

在上述衬底和上述高介电常数栅极绝缘膜之间设置有缓冲绝缘膜。

9、根据权利要求8所述的半导体装置，其特征在于：

上述缓冲绝缘膜是氧化硅膜或氧氮化硅膜。

10、根据权利要求1所述的半导体装置，其特征在于：

上述栅极电极是整个区域被硅化物化的全硅化物栅极电极。

11、一种半导体装置的制造方法，其特征在于：

包括：工序a，在衬底的活性区域上形成高介电常数栅极绝缘膜；

工序b，在上述高介电常数栅极绝缘膜上形成栅极电极；

工序c，在上述工序b之后，将位于上述栅极电极外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分的厚度变薄；以及

工序d，在上述工序c之后，在上述栅极电极的侧面形成绝缘性侧壁。

12、根据权利要求11所述的半导体装置的制造方法，其特征在于：

电子扫描7

在上述工序 d 之后，包括将位于上述绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

13、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：

上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成；

上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁。

14、根据权利要求 13 所述的半导体装置的制造方法，其特征在于：

在上述工序 d1 和上述工序 d2 之间，还包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

15、根据权利要求 13 所述的半导体装置的制造方法，其特征在于：

在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序；

在上述工序 d2 之后，还包括将位于上述第 2 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

16、根据权利要求 12、14 或 15 中的任意一项所述的半导体装置的制造方法，其特征在于：

上述高介电常数栅极绝缘膜的除去是利用湿蚀刻法选择性地进行的。

17、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：

上述工序 b 含有形成覆盖上述栅极电极的上表面的保护膜的工序；

在上述工序 d 之后，还包括在将位于上述绝缘性侧壁外侧的上述活性区域的表面硅化物化后，将上述保护膜除去，然后，使上述栅极电极全部硅化物化的工序。

18、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：

在上述工序 a 之前，还包括在上述活性区域上形成缓冲绝缘膜的工序；

在上述工序 a 中，夹着上述缓冲绝缘膜在上述活性区域上形成上述高介电常数栅极绝缘膜。

中华人民共和国国家知识产权局

100083

北京市海淀区王庄路1号清华同方科技大厦B座25层
中科专利商标代理有限责任公司
汪惠民

申请号：2006100938722

发文日期

2008年8月22日

申请人：松下电器产业株式会社

发明创造名称：半导体装置及其制造方法

发明专利申请进入实质审查程序通知书

对于上述专利申请，根据申请人提出的实质审查请求，经审查符合专利法第三十五条，实施细则第九十条规定，该专利申请已进入实质审查程序。

提示：

1.自本通知书发文日起，该申请即进入实质申请程序，自此专利申请人向专利局递交各种专利文件时，应在文件上注明实质审查程序。

2.根据专利法实施细则第五十一条第一款的规定，发明专利申请人自收到专利局发出的本通知书之日起三个月内，可以对发明专利申请主动提出修改。

3 缴纳费用通过邮局汇付的，邮寄汇付：收款人姓名：国家知识产权局专利局收费处 商户客户号：110000860；缴纳费用通过银行汇付的，请寄交户名：中华人民共和国国家知识产权局专利局，开户银行：中国工商银行北京北太平庄支行，账号：0200010009014400518；汇款时应准确写明申请号、费用名称及分项金额。办理缴纳费用手续时未写明申请号和/或费用名称的视为未办理缴费手续。

审查员：梁芳　　审查部门：初审及流程管理部

2008年8月14日

中华人民共和国国家知识产权局

100083 北京市海淀区王庄路1号清华同方科技大厦B座25层 中科专利商标代理有限责任公司 汪惠民	发文日 2009年3月20日
申请号:2006100938722	

申请人:松下电器产业株式会社

发明名称:半导体装置及其制造方法

第一次审查意见通知书

1. ☑应申请人提出的实审请求,根据专利法第35条第1款的规定,国家知识产权局对上述发明专利申请进行实质审查。
   ☐根据专利法第35条第2款的规定,国家知识产权局决定自行对上述发明专利申请进行审查。
2. ☑申请人要求以其在:
   JP 专利局的申请日 2005年 08月 05日为优先权日,
   专利局的申请日 年 月 日为优先权日,
   专利局的申请日 年 月 日为优先权日。
   ☑申请人已经提交了经原申请国受理机关证明的第一次提出的在先申请文件的副本。
   ☐申请人尚未提交经原申请国受理机关证明的第一次提出的在先申请文件的副本,根据专利法第30条的规定视为未要求优先权。
3. ☑申请人于2008年8月5日和 年 月 日以及 年 月 日提交了修改文件。
   经审查,申请人于 年 月 日提交的 不符合专利法实施细则第51条第1款的规定。
   ☐
4. 审查针对的申请文件:
   ☐原始申请文件。☑审查是针对下述申请文件的
   申请日提交的原始申请文件的权利要求第 项、说明书第1-24页、附图第1-11页;
   分案申请递交日提交的权利要求第 项、说明书第 页、附图第 页;
   2008 年 8 月 5 日提交的权利要求第1-18 项、说明书第 页、附图第 页;
   年 月 日提交的权利要求第 项、说明书第 页、附图第 页;
   年 月 日提交的权利要求第 项、说明书第 页、附图第 页;
   申请日提交的说明书摘要,申请日提交的摘要附图。
5. ☐本通知书是在未进行检索的情况下作出的。
   ☑本通知书是在进行了检索的情况下作出的。
   ☑本通知书引用下述对比文件(其编号在今后的审查过程中继续沿用):

编号	文件号或名称	公开日期(或抵触申请的申请日)
1	JP特开2005-64190A	2005-3-10
2	CN1610129A	2005-4-27
3	JP特开2004-356576A	2004-12-16

6. 审查的结论性意见:
   ☐关于说明书:
   ☐申请的内容属于专利法第5条规定的不授予专利权的范围。
   ☐说明书不符合专利法第26条第3款的规定。

☐说明书不符合专利法第 33 条的规定。
☐说明书的撰写不符合专利法实施细则第 18 条的规定。
☐

☑关于权利要求书：
☑权利要求1, 11-12 不具备专利法第 22 条第 2 款规定的新颖性。
☑权利要求2-4, 7-10, 13-14, 16-18不具备专利法第 22 条第 3 款规定的创造性。
☐权利要求_____不具备专利法第 22 条第 4 款规定的实用性。
☐权利要求_____属于专利法第 25 条规定的不授予专利权的范围。
☐权利要求_____不符合专利法第 26 条第 4 款的规定。
☐权利要求_____不符合专利法第 31 条第 1 款的规定。
☐权利要求_____不符合专利法第 33 条的规定。
☐权利要求_____不符合专利法实施细则第 2 条第 1 款的规定。
☐权利要求_____不符合专利法实施细则第 13 条第 1 款的规定。
☑权利要求 16 不符合专利法实施细则第 20 条的规定。
☐权利要求_____不符合专利法实施细则第 21 条的规定。
☐权利要求_____不符合专利法实施细则第 22 条的规定。
☐权利要求_____不符合专利法实施细则第 23 条的规定。
☐_____

☐分案的申请不符合专利法实施细则第 43 条第 1 款的规定。

上述结论性意见的具体分析见本通知书的正文部分。

7. 基于上述结论性意见，审查员认为：

☐申请人应按照通知书正文部分提出的要求，对申请文件进行修改。

☑申请人应在意见陈述书中论述其专利申请可以被授予专利权的理由，并对通知书正文部分中指出的不符合规定之处进行修改，否则将不能授予专利权。

☐专利申请中没有可以被授予专利权的实质性内容，如果申请人没有陈述理由或者陈述理由不充分，其申请将被驳回。

☐_____

8. **申请人应注意下述事项：**

(1) 根据专利法第 37 条的规定，申请人应在收到本通知之日起的肆个月内陈述意见，如果申请人无正当理由逾期不答复，其申请将被视为撤回。

(2) 申请人对其申请的修改应符合专利法第 33 条的规定，修改文本应一式两份，其格式应符合审查指南的有关规定。

(3) 申请人的意见陈述书和/或修改文本应邮寄或递交国家知识产权局专利局受理处，凡未邮寄或递交给受理处的文件不具备法律效力。

(4) 未经预约，申请人和/或代理人不得前来国家知识产权局专利局与审查员举行会晤。

9. **本通知书正文部分共有 5 页，并附有下述附件：**

☑引用的对比文件的复印件共 3 份 59 页。☐_____

审查员：邵烨(974K)
2009 年 3 月 6 日

审查部门 审查协作中心

缘膜上；以及绝缘性侧壁，由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成，该第 1 绝缘性侧壁形成在上述栅极电极的侧面，该第 2 绝缘性侧壁夹着上述第 1 绝缘性侧壁形成在上述栅极电极的侧面。上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度。

在本发明的半导体装置中，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成，该第 1 绝缘性侧壁形成在上述栅极电极的侧面，该第 2 绝缘性侧壁夹着上述第 1 绝缘性侧壁形成在上述栅极电极的侧面。上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 1 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度，也可以小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

当上述绝缘性侧壁由上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁构成时，上述高介电常数栅极绝缘膜也可以不形成在上述第 2 绝缘性侧壁的下侧。

当上述绝缘性侧壁由上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁构成时，上述高介电常数栅极绝缘膜从上述栅极电极的下侧连续形成到上述第 2 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下侧区域的厚度，也可以与上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度相等。

当上述绝缘性侧壁由上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁构成时，上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 2 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下侧区域的厚度，也可以小于上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度。

在本发明的半导体装置中，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成，该第 1 绝缘性侧壁形成在上述栅极电极的侧面，该第 2 绝缘性侧壁夹着上述第 1 绝缘性侧壁形成在上述栅极电极的侧面。上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 2 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度，与上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度相等。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下

09.08.03
电子扫描8

侧区域的厚度，也可以小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

在本发明的半导体装置中，也可以在上述高介电常数栅极绝缘膜的侧端部设置缺口。

在本发明的半导体装置中，也可以在上述衬底和上述高介电常数栅极绝缘膜之间设置缓冲绝缘膜。此时，上述缓冲绝缘膜可以是氧化硅膜或氧氮化硅薄膜。

在本发明的半导体装置中，上述栅极电极可以是整个区域被硅化物化的全硅化物栅极电极。

本发明所涉及的半导体装置的制造方法，包括：工序 a，在衬底的活性区域上形成高介电常数栅极绝缘膜；工序 b，在上述高介电常数栅极绝缘膜上形成栅极电极；工序 c，在上述工序 b 之后，将位于上述栅极电极外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分的厚度变薄；以及工序 d，在上述工序 c 之后，在上述栅极电极的侧面形成绝缘性侧壁，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成；上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁，在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序；在上述工序 d2 之后，还包括将位于上述第 2 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

在本发明的半导体装置的制造方法中，也可以在上述工序 d 之后，包括将位于上述绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

在本发明的半导体装置的制造方法中，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成。上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁。

当上述工序 d 包含上述工序 d1 和上述工序 d2 时，也可以在上述工序 d1 和上述工序 d2 之间，还包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

当上述工序 d 包含上述工序 d1 和上述工序 d2 时，在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序。在上述工序 d2 之后，

电子扫描

权利要求书

1、一种半导体装置，其特征在于：

包括：高介电常数栅极绝缘膜，形成在衬底的活性区域上，

栅极电极，形成在上述高介电常数栅极绝缘膜上，以及

绝缘性侧壁，由第1绝缘性侧壁和第2绝缘性侧壁构成，该第1绝缘性侧壁形成在上述栅极电极的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第1绝缘性侧壁和上述第2绝缘性侧壁的下侧；

上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度，

上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度。

2、根据权利要求1所述的半导体装置，其特征在于：

在上述高介电常数栅极绝缘膜的侧端部设置有缺口。

3、根据权利要求1或2所述的半导体装置，其特征在于：

在上述衬底和上述高介电常数栅极绝缘膜之间设置有缓冲绝缘膜。

4、根据权利要求3所述的半导体装置，其特征在于：

上述缓冲绝缘膜是氧化硅膜或氧氮化硅膜。

5、根据权利要求1所述的半导体装置，其特征在于：

上述栅极电极是整个区域被硅化物化的全硅化物栅极电极。

6、一种半导体装置的制造方法，其特征在于：

包括：工序a，在衬底的活性区域上形成高介电常数栅极绝缘膜；

工序b，在上述高介电常数栅极绝缘膜上形成栅极电极；

工序c，在上述工序b之后，将位于上述栅极电极外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分的厚度变薄；以及

工序d，在上述工序c之后，在上述栅极电极的侧面形成绝缘性侧壁，

09.08.03 子扫描8

上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成；

上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁，

在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序；

在上述工序 d2 之后，还包括将位于上述第 2 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

7、根据权利要求 6 所述的半导体装置的制造方法，其特征在于：

上述高介电常数栅极绝缘膜的除去是利用湿蚀刻法选择性地进行的。

8、根据权利要求 6 所述的半导体装置的制造方法，其特征在于：

上述工序 b 含有形成覆盖上述栅极电极的上表面的保护膜的工序；

在上述工序 d 之后，还包括在将位于上述绝缘性侧壁外侧的上述活性区域的表面硅化物化后，将上述保护膜除去，然后，使上述栅极电极全部硅化物化的工序。

9、根据权利要求 6 所述的半导体装置的制造方法，其特征在于：

在上述工序 a 之前，还包括在上述活性区域上形成缓冲绝缘膜的工序；

在上述工序 a 中，夹着上述缓冲绝缘膜在上述活性区域上形成上述高介电常数栅极绝缘膜。

中华人民共和国国家知识产权局

100083 北京市海淀区王庄路1号清华同方科技大厦B座25层 中科专利商标代理有限责任公司 汪惠民	发文日 本授权通知书的发文日 同办理登记手续通知书
申请号:2006100938722	

申请人:松下电器产业株式会社

发明名称:半导体装置及其制造方法

授予发明专利权通知书

1.根据专利法第39条及其实施细则第54条的规定,上述发明专利申请经实质审查,没有发现驳回理由,现作出授予专利权的通知。

申请人收到本通知后,还应当依照办理登记手续通知书的内容办理登记手续。

申请人按期办理登记手续后,国家知识产权局将作出授予专利权的决定,颁发发明专利证书,并予以登记和公告。

期满未办理登记手续的,视为放弃取得专利权的权利。

2. ☐授予专利权的上述发明专利申请是以申请日　　年　月　日提交的文本为基础。

☑授予专利权的上述发明专利申请是以下述文件为基础:

申请日提交的原始申请文件的权利要求第　　项、说明书第1-2,5-24页、附图第1-11页;

分案申请递交日提交的权利要求第　　项、说明书第　　页、附图第　　页;

2009　　年8　月　3　日提交的权利要求第1-9　项、说明书第3-4　页、附图第　　页;

年　　月　　日提交的权利要求第　　项、说明书第　　页、附图第　　页;

年　　月　　日提交的权利要求第　　项、说明书第　　页、附图第　　页;

申请日提交的说明书摘要,申请日提交的摘要附图。

3.授予专利权的上述发明专利申请的名称:

☑未变更。

☐由_____变更为上述名称。

4.申请人于　　年　月　日提交了专利号为_____的"放弃专利权声明"。经审查:

☐进入放弃专利权的程序。

☐未进入放弃专利权的程序。理由是:申请人声明放弃的专利与本发明专利申请不属于相同的发明创造,符合专利法实施细则第13条第1款的规定。

5.审查员依职权对申请文件修改如下:

6.在本通知发出后收到的申请人主动修改的申请文件,不予受理。

审查员:邵烨(974K)　　审查部门:审查协作中心

2009年10月10日

第一次审查意见通知书正文

申请号：200610093872.2

经审查，具体意见如下：

1.权利要求1请求保护一种半导体装置。对比文件1（JP特开2005-64190A）公开了一种半导体装置，并具体披露了如下技术特征（参见对比文件1第0076-0083段、图22-23）：

HfO2栅极绝缘膜5（相当于高介电常数栅极绝缘膜），形成在衬底1的有源区域上；

栅极电极6，形成在上述栅极绝缘膜5上，

绝缘性侧壁10，形成在上述栅极电极6的侧面；

上述HfO2栅极绝缘膜5从上述栅极电极6的下侧一直连续形成到上述绝缘性侧壁10的下侧；

上述HfO2栅极绝缘膜5中的上述绝缘性侧壁10的下侧区域的至少一部分的厚度，小于上述HfO2栅极绝缘膜5中的上述栅极电极6的下侧区域的厚度。

由此可见，权利要求1的全部技术特征已经被对比文件1公开，其请求保护的技术方案与对比文件1披露的技术方案相同，属于相同的半导体装置领域，能解决的技术问题相同，预期到达的能避免栅极电极端部中高介电常数栅极绝缘膜的介电常数下降和绝缘性下降的效果相同。因此，权利要求1请求保护的技术方案不具备专利法第二十二条第二款规定的新颖性。

2.权利要求2、4直接或间接引用权利要求1。位于栅极侧壁的用于电隔绝栅极和源漏的侧壁绝缘膜由两层或者三层构成是本领域的一种惯用手段。在对比文件1图22公开的技术方案的基础上，出于工艺的某些实际需要，本领域技术人员通过常规手段（如有限次实验）就能将对比文件1中图22中的侧壁绝缘膜10设置成两个侧壁绝缘膜，即能得到权利要求2和4的附加技术特征：将侧壁绝缘膜10设置成由第1绝缘性侧壁和第2绝缘性侧壁构成（<u>即由第1绝缘性侧壁和第2绝缘性侧壁代替侧壁绝缘膜10</u>），该第1绝缘性侧壁形成在上述栅极电极6的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极6的侧面；同时HfO2栅极绝缘膜5（相当于高介电常数栅极绝缘膜）从上述栅极电极的下侧一直连续形成到上述第1绝缘性侧壁的下侧；上述HfO2栅极绝缘膜5的上述第1绝缘性侧壁的下侧区域的厚度（该厚度等于上述HfO2栅极绝缘膜5中的上述绝缘性侧壁10的下侧区域的厚度），小于上述HfO2栅极绝缘膜5中的上述栅极电极6的下侧区域的厚度（相当于权利要求2的附加技术特征）；上述HfO2栅极绝缘膜5连续形成到上述第2绝缘性侧壁的下侧；

上述HfO2栅极绝缘膜5中的上述第2绝缘性侧壁的下侧区域的厚度与上述HfO2栅极绝缘膜5中的上述第1绝缘侧壁的下侧区域的厚度相等（相当于权利要求4的附加技术特征）。

当直接或间接引用的权利要求1不具备新颖性时，在对比文件1的基础上结合本领域的惯用手段并通过常规手段以获得权利要求2、4请求保护的技术方案，对于本领域技术人员来说是显而易见的。因此，权利要求2、4请求保护的技术方案不具备突出的实质性特点和显著的进步，不具备专利法第二十二条第三款规定的创造性。

3.权利要求2、3直接或间接引用权利要求1。位于栅极侧壁的用于电隔绝栅极和源漏的侧壁绝缘膜由两层或者三层构成是本领域的一种惯用手段。在对比文件1图22公开的技术方案的基础上，出于工艺的某些实际需要，本领域技术人员通过常规手段（如有限次实验）就能在绝缘性侧壁10的侧壁再形成另一侧壁绝缘膜，即能得到权利要求2和3的附加技术特征：即该半导体装置的绝缘性侧壁由绝缘性侧壁10（第1绝缘性侧壁）和位于该第1绝缘性侧壁上的另一侧壁绝缘膜（第2绝缘性侧壁）构成，该第1绝缘性侧壁形成在上述栅极电极6的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极6的侧面；同时HfO2栅极绝缘膜5（相当于高介电常数栅极绝缘膜）从上述栅极电极的下侧一直连续形成到上述第1绝缘性侧壁的下侧；上述HfO2栅极绝缘膜5的上述第1绝缘性侧壁的下侧区域的厚度（该厚度等于上述HfO2栅极绝缘膜5中的上述绝缘性侧壁10的下侧区域的厚度），小于上述HfO2栅极绝缘膜5中的上述栅极电极6的下侧区域的厚度（相当于权利要求2的附加技术特征）；上述HfO2栅极绝缘膜5没有形成在上述第2绝缘性侧壁的下侧（相当于权利要求3的附加技术特征）。

当直接或间接引用的权利要求1不具备新颖性时，在对比文件1的基础上结合本领域的惯用手段并通过常规手段以获得权利要求2、3请求保护的技术方案，对于本领域技术人员来说是显而易见的。因此，权利要求2、3请求保护的技术方案不具备突出的实质性特点和显著的进步，不具备专利法第二十二条第三款规定的创造性。

4.权利要求7是权利要求1的从属权利要求。对比文件2（CN1610129A）在图2的技术方案中公开了一种半导体器件，其中利用在绝缘层2形成缺口8和9，以减小栅电极3和源漏4、5之间的重叠，以达到减小寄生电容的目的（参见说明书第4-7页、图2）。可见，对比文件2给出了在栅极绝缘层的侧壁设置缺口的技术手段进一步应用于对比文件1的技术方案的启示，在此启示的基础上，本领域技术人员必然能得到将对比文件1中的HfO2栅极绝缘膜5（相当于高介电常数栅极绝缘膜）的侧端部设置缺口的特征。当引用的权利要求1不具备新颖性时，在对比文件1的基础

上结合对比文件2以获得权利要求7请求保护的技术方案，对于本领域技术人员来说是显而易见的。因此，权利要求7请求保护的技术方案不具备突出的实质性特点和显著的进步，不具备专利法第二十二条第三款规定的创造性。

5.权利要求8是权利要求1的从属权利要求。对比文件3（JP特开2004-356576A）在图1的技术方案中公开了一种半导体器件，其中在衬底和高介电常数栅极绝缘膜7之间设置有缓冲绝缘膜6。可见，该权利要求的附加技术特征已被对比文件3公开，且该特征在对比文件3中的作用与在本申请中的作用相同，都能防止衬底和栅极绝缘膜界面的劣化，也就是对比文件3给出了将上述特征应用于对比文件1的技术方案以进一步解决其技术问题的启示。当引用的权利要求1不具备新颖性时，在对比文件1的基础上结合对比文件3以获得权利要求8请求保护的技术方案，对于本领域技术人员来说是显而易见的。因此，权利要求8请求保护的技术方案不具备突出的实质性特点和显著的进步，不具备专利法第二十二条第三款规定的创造性。

6.权利要求9是权利要求8的从属权利要求。其附加技术特征已被对比文件3公开（参见第0030段）：即该缓冲绝缘膜6是氧化硅膜。当引用的权利要求不具备创造性时，权利要求9请求保护的技术方案不具备专利法第二十二条第三款规定的创造性。

7.权利要求10是权利要求1的从属权利要求。为了减小接触电阻，在源漏和栅极的表面形成金属硅化物层是本领域的惯用手段，即该附加技术特征是本领域的惯用手段。当引用的权利要求1不具备新颖性时，权利要求10请求保护的技术方案不具备专利法第二十二条第三款规定的创造性。

8. 权利要求11请求保护一种半导体装置的制造方法。对比文件1（JP特开2005-64190A）公开了一种半导体装置的制造方法，并具体披露了如下技术特征（参见对比文件1第0076-0083段、图19-23）： 包括：

工序a，在衬底1的有源区域上形成HfO2栅极绝缘膜5（相当于高介电常数栅极绝缘膜）；

工序b，在上述栅极绝缘膜5上形成栅极电极6；

工序c，在工序b之后，将位于上述栅极电极6外侧的上述栅极绝缘膜5的部分刻蚀，使该部分的厚度变薄；

工序d，在上述工序c之后，在上述栅极电极6的侧面形成绝缘性侧壁10。

由此可见，权利要求11的全部技术特征已经被对比文件1公开，其请求保护的技术方案与对比文件1披露的技术方案相同，属于相同的半导体装置的制造方法领

域，能解决的技术问题相同，预期到达的能避免栅极电极端部中高介电常数栅极绝缘膜的介电常数下降和绝缘性下降的效果相同。因此，权利要求11请求保护的技术方案不具备专利法第二十二条第二款规定的新颖性。

9.权利要求12是权利要求11的从属权利要求。其附加技术特征已被对比文件1在图22中披露：即在上述工序d后，包括将位于上述绝缘性侧壁10外侧的HfO2栅极绝缘膜5的部分除去的工序。当引用的权利要求11不具备新颖性时，权利要求12请求保护的技术方案不具备专利法第二十二条第二款规定的新颖性。

10.权利要求13-14直接或间接引用权利要求11。位于栅极侧壁的用于电隔绝栅极和源漏的侧壁绝缘膜由两层或者三层构成是本领域的一种惯用手段。在对比文件1图22公开的技术方案的基础上，出于工艺的某些实际需要，本领域技术人员通过常规手段（如有限次实验）就能在绝缘性侧壁10的侧壁再形成另一侧壁绝缘膜，即能得到权利要求13的附加技术特征：即该半导体装置的绝缘性侧壁由绝缘性侧壁10（第1绝缘性侧壁）和位于该第1绝缘性侧壁上的另一侧壁绝缘膜（第2绝缘性侧壁）构成，且上述形成绝缘性侧壁的工序d包括工序d1和工序d2，在该工序d1中，先在栅极电极6的侧面形成第1绝缘性侧壁，然后在工序d2中，夹着上述第1绝缘性侧壁在上述栅极电极6的侧面形成上述第2绝缘性侧壁；且对比文件在第0079段公开了先刻蚀形成绝缘性侧壁10（第1绝缘性侧壁，即工序d1）后，刻蚀去除位于上述绝缘性侧壁10外侧的HfO2栅极绝缘膜5的部分，本领域技术人员通过常规手段（如有限次实验）就能得到在刻蚀去除位于上述绝缘性侧壁10外侧的HfO2栅极绝缘膜5的部分之后再实施形成第2绝缘性侧壁的工序d2（即权利要求14的附加技术特征）。

当直接或间接引用的权利要求11不具备新颖性时，在对比文件1的基础上结合本领域的惯用手段并通过常规手段以获得权利要求13-14请求保护的技术方案，对于本领域技术人员来说是显而易见的。因此，权利要求13-14请求保护的技术方案不具备突出的实质性特点和显著的进步，不具备专利法第二十二条第三款规定的创造性。

11.权利要求16引用权利要求12、14或15。湿法刻蚀是常规的一种刻蚀手段，即该附加技术特征为本领域的惯用手段。当引用的权利要求12不具备新颖性或引用的权利要求14不具备创造性时，权利要求16请求保护的技术方案不具备专利法第二十二条第三款规定的创造性。

12.权利要求17是权利要求11的从属权利要求。其附加技术特征中的部分特征“上述工序b含有形成覆盖上述栅极电极的上表面的保护膜的工序，在工序d之后，

还包括将位于上述绝缘性侧壁外侧的上述活性区域的表面硅化物化的工序”已被对比文件1在图19-23中公开：即上述工序b含有形成覆盖上述栅极电极6的上表面的保护膜13的工序，在工序d之后，还包括将位于上述绝缘性侧壁10外侧的上述活性区域的表面硅化物化的工序；至于该附加技术特征中的其它特征“除去保护膜，包括使栅极电极全部硅化物化的工序”是本领域技术人员通过合乎逻辑的推理分析就能得到的，因为为了减小接触电阻，在栅极上形成硅化物层是一种惯用手段，为了形成硅化物层，必然先去除位于栅极上的保护膜。

当引用的权利要求11不具备新颖性时，权利要求17请求保护的技术方案不具备专利法第二十二条第三款规定的创造性。

13.权利要求18是权利要求11的从属权利要求。对比文件3（JP特开2004-356576A）在图1的技术方案中公开了一种半导体器件的制造方法，其中在衬底的有源区域形成高介电常数绝缘膜7（相当于步骤a）之前还在上述有源区域上形成缓冲绝缘膜6的工序；在上述形成高介电常数绝缘膜7的步骤中，夹着上述缓冲绝缘膜6在上述有源区域上形成上述高介电常数绝缘膜7。可见，该权利要求的附加技术特征已被对比文件3公开，且该特征在对比文件3中的作用与在本申请中的作用相同，都能防止衬底和栅极绝缘膜界面的劣化，也就是对比文件3给出了将上述特征应用于对比文件1的技术方案以进一步解决其技术问题的启示。当引用的权利要求11不具备新颖性时，在对比文件1的基础上结合对比文件3以获得权利要求18请求保护的技术方案，对于本领域技术人员来说是显而易见的。因此，权利要求18请求保护的技术方案不具备突出的实质性特点和显著的进步，不具备专利法第二十二条第三款规定的创造性。

14.权利要求16出现的“根据权利要求12、14或15中的任意一项”表达不清楚，不符合专利法实施细则第二十条第一款的规定。若想表达成择一引用，可以考虑修改为“根据权利要求12或14或15”或“根据权利要求12、14和15中的任意一项”。

基于上述理由，本申请按照目前的文本还不能被授予专利权。如果申请人在本通知书指定的四个月答复期限内按照本通知书提出的审查意见对申请文件进行修改，克服所存在的缺陷，则本申请可望被授予专利权。请申请人注意，对申请文件的修改应当符合专利法第三十三条的规定，不得超出原说明书和权利要求书记载的范围。

申请人提交的修改文件应当包括：有修改标记的修改参照页，与新打印的替换页（一式两份），并确保上述两部分在内容上的一致性。并说明修改的依据。

审查员：邵烨　代码：974K

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09.08.03 子扫描8

修改参考页（共6页）

权 利 要 求 书

1、一种半导体装置，其特征在于：

包括：高介电常数栅极绝缘膜，形成在衬底的活性区域上，

栅极电极，形成在上述高介电常数栅极绝缘膜上，以及

绝缘性侧壁，由第1绝缘性侧壁和第2绝缘性侧壁构成，该第1绝缘性侧壁形成在上述栅极电极的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极的侧面；

上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第1绝缘性侧壁和上述第2绝缘性侧壁~~绝缘性侧壁~~的下侧；

上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的~~至少一部分的~~厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度，

上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度。

~~2、根据权利要求1所述的半导体装置，其特征在于：~~

~~上述绝缘性侧壁由第1绝缘性侧壁和第2绝缘性侧壁构成，该第1绝缘性侧壁形成在上述栅极电极的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极的侧面；~~

~~上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第1绝缘性侧壁的下侧；~~

~~上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。~~

~~3、根据权利要求2所述的半导体装置，其特征在于：~~

~~上述高介电常数栅极绝缘膜没有形成在上述第2绝缘性侧壁的下侧。~~

~~4、根据权利要求2所述的半导体装置，其特征在于：~~

~~上述高介电常数栅极绝缘膜连续形成到上述第2绝缘性侧壁的下侧；~~

~~上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚~~

~~度，与上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度相等。~~

~~5、根据权利要求2所述的半导体装置，其特征在于：~~

~~上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第2绝缘性侧壁的下侧；~~

~~上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度。~~

~~6、根据权利要求1所述的半导体装置，其特征在于：~~

~~上述绝缘性侧壁由第1绝缘性侧壁和第2绝缘性侧壁构成，该第1绝缘性侧壁形成在上述栅极电极的侧面，该第2绝缘性侧壁夹着上述第1绝缘性侧壁形成在上述栅极电极的侧面；~~

~~上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第2绝缘性侧壁的下侧；~~

~~上述高介电常数栅极绝缘膜中的上述第1绝缘性侧壁的下侧区域的厚度，与上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度相等；~~

~~上述高介电常数栅极绝缘膜中的上述第2绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。~~

~~7~~2、根据权利要求1所述的半导体装置，其特征在于：

在上述高介电常数栅极绝缘膜的侧端部设置有缺口。

~~8~~3、根据权利要求1或2所述的半导体装置，其特征在于：

在上述衬底和上述高介电常数栅极绝缘膜之间设置有缓冲绝缘膜。

~~9~~4、根据权利要求~~8~~3所述的半导体装置，其特征在于：

上述缓冲绝缘膜是氧化硅膜或氧氮化硅膜。

~~10~~5、根据权利要求1所述的半导体装置，其特征在于：

上述栅极电极是整个区域被硅化物化的全硅化物栅极电极。

~~11~~6、一种半导体装置的制造方法，其特征在于：

包括：工序a，在衬底的活性区域上形成高介电常数栅极绝缘膜；

工序b，在上述高介电常数栅极绝缘膜上形成栅极电极；

工序 c，在上述工序 b 之后，将位于上述栅极电极外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分的厚度变薄；以及

工序 d，在上述工序 c 之后，在上述栅极电极的侧面形成绝缘性侧壁，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成；

上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁，

在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序；

在上述工序 d2 之后，还包括将位于上述第 2 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

~~12、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：~~

~~在上述工序 d 之后，包括将位于上述绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。~~

~~13、根据权利要求 11 所述的半导体装置的制造方法，其特征在于：~~

~~上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成；~~

~~上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁。~~

~~14、根据权利要求 13 所述的半导体装置的制造方法，其特征在于：~~

~~在上述工序 d1 和上述工序 d2 之间，还包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。~~

~~15、根据权利要求 13 所述的半导体装置的制造方法，其特征在于：~~

~~在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序；~~

~~16~~7、根据权利要求 ~~12、14 或 15 中的任意一项~~ 6 所述的半导体装置的制造方法，其特征在于：

上述高介电常数栅极绝缘膜的除去是利用湿蚀刻法选择性地进行的。

~~17~~8、根据权利要求 ~~11~~6 所述的半导体装置的制造方法，其特征在于：

上述工序 b 含有形成覆盖上述栅极电极的上表面的保护膜的工序；

在上述工序 d 之后，还包括在将位于上述绝缘性侧壁外侧的上述活性区域的表面硅化物化后，将上述保护膜除去，然后，使上述栅极电极全部硅化物化的工序。

~~189~~、根据权利要求 ~~116~~ 所述的半导体装置的制造方法，其特征在于：

在上述工序 a 之前，还包括在上述活性区域上形成缓冲绝缘膜的工序；

在上述工序 a 中，夹着上述缓冲绝缘膜在上述活性区域上形成上述高介电常数栅极绝缘膜。

缘膜上；以及绝缘性侧壁，由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成，该第 1 绝缘性侧壁形成在上述栅极电极的侧面，该第 2 绝缘性侧壁夹着上述第 1 绝缘性侧壁形成在上述栅极电极的侧面~~形成在上述栅极电极的侧面~~。上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁~~绝缘性侧壁~~的下侧。上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的~~至少一部分~~厚度，小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下侧区域的厚度，小于上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度。

在本发明的半导体装置中，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成，该第 1 绝缘性侧壁形成在上述栅极电极的侧面，该第 2 绝缘性侧壁夹着上述第 1 绝缘性侧壁形成在上述栅极电极的侧面。上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 1 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度，也可以小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

当上述绝缘性侧壁由上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁构成时，上述高介电常数栅极绝缘膜也可以不形成在上述第 2 绝缘性侧壁的下侧。

当上述绝缘性侧壁由上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁构成时，上述高介电常数栅极绝缘膜从上述栅极电极的下侧连续形成到上述第 2 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下侧区域的厚度，也可以与上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度相等。

当上述绝缘性侧壁由上述第 1 绝缘性侧壁和上述第 2 绝缘性侧壁构成时，上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 2 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下侧区域的厚度，也可以小于上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度。

在本发明的半导体装置中，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成，该第 1 绝缘性侧壁形成在上述栅极电极的侧面，该第 2 绝缘性侧壁夹着上述第 1 绝缘性侧壁形成在上述栅极电极的侧面。上述高介电常数栅极绝缘膜从上述栅极电极的下侧一直连续形成到上述第 2 绝缘性侧壁的下侧。上述高介电常数栅极绝缘膜中的上述第 1 绝缘性侧壁的下侧区域的厚度，与上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度相等。上述高介电常数栅极绝缘膜中的上述第 2 绝缘性侧壁的下

侧区域的厚度，也可以小于上述高介电常数栅极绝缘膜中的上述栅极电极的下侧区域的厚度。

在本发明的半导体装置中，也可以在上述高介电常数栅极绝缘膜的侧端部设置缺口。

在本发明的半导体装置中，也可以在上述衬底和上述高介电常数栅极绝缘膜之间设置缓冲绝缘膜。此时，上述缓冲绝缘膜可以是氧化硅膜或氧氮化硅薄膜。

在本发明的半导体装置中，上述栅极电极可以是整个区域被硅化物化的全硅化物栅极电极。

本发明所涉及的半导体装置的制造方法，包括：工序 a，在衬底的活性区域上形成高介电常数栅极绝缘膜；工序 b，在上述高介电常数栅极绝缘膜上形成栅极电极；工序 c，在上述工序 b 之后，将位于上述栅极电极外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分的厚度变薄；以及工序 d，在上述工序 c 之后，在上述栅极电极的侧面形成绝缘性侧壁，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成；上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁，在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序；在上述工序 d2 之后，还包括将位于上述第 2 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

在本发明的半导体装置的制造方法中，也可以在上述工序 d 之后，包括将位于上述绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

在本发明的半导体装置的制造方法中，上述绝缘性侧壁由第 1 绝缘性侧壁和第 2 绝缘性侧壁构成。上述工序 d 包含工序 d1 和工序 d2，在该工序 d1 中，在上述栅极电极的侧面形成上述第 1 绝缘性侧壁，在该工序 d2 中，夹着上述第 1 绝缘性侧壁在上述栅极电极的侧面形成上述第 2 绝缘性侧壁。

当上述工序 d 包含上述工序 d1 和上述工序 d2 时，也可以在上述工序 d1 和上述工序 d2 之间，还包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分除去的工序。

当上述工序 d 包含上述工序 d1 和上述工序 d2 时，在上述工序 d1 和上述工序 d2 之间，包括将位于上述第 1 绝缘性侧壁外侧的上述高介电常数栅极绝缘膜的部分蚀刻，使该部分更薄的工序。在上述工序 d2 之后，

09.08.03

电子扫描8

意 见 陈 述 书

20090803

IA063392

① 专利或专利申请	中请号或专利号 200610093872.2	中 请 日 2006 年 6 月 20 日
	发明创造名称	半导体装置及其制造方法 061938722
	当事人	☒中请人或专利权人姓名或名称（代表） 松下电器产业株式会社 ☐撤消专利权请求人姓名或名称（代表） ☐

② 对专利局 2009 年 3 月 20 日 作出的上述 ☒专利中请 ☐专 利 的 第 1 次审查意见 通知书，陈述意见如下：

详见附页

如有疑问，请与我公司代理人联系：

联系人：李贵亮

电 话：82378686－6291

谢谢合作！

③ 附件清单：

权利要求书替换页 2 页，说明书第 3－4 页的替换页 2 页，替换页一式两份共 8 页，参考附件 6 页。

④申请人或代理机构签章	⑤ 专利局处理意见
CHINA SCIENCE PATENT & TRADEMARK AGENT LTD 中国专利商标代理有限责任公司 中请专用 2009 年 8 月 3 日	验章形章 (00-33) 年 月 日

13/02/03/24

09.08.03 子扫描8

意见陈述书

申请人收到了审查员于 2009 年 3 月 20 日针对本申请（申请号：2006100938722）发出的第一次审查意见通知书。针对审查员的意见，申请人对其申请文件和对比文件进行了深入的研究，对其权利要求书和说明书的相应部分进行了修改（详见修改参考页），并陈述意见如下。

针对审查员认为本申请权利要求 1 和 11－12 不具有新颖性，权利要求 2－4、7－10 以及 13－14 和 16－18 不具有创造性的意见，申请人对其权利要求进行了修改，将原权利要求 2 和没有被审查员指出创造性问题的权利要求 5 的附加技术特征追加到原权利要求 1 中，形成了新的权利要求 1。同理，将原权利要求 13 和没有被审查员指出创造性问题的权利要求 15 的附加技术特征追加到原权利要求 11 中，形成了新的方法独立权利要求 6。与此同时，删除了原权利要求 2－6 和 12－15，并对其余权利要求进行了重新排序（详见修改参考页）。申请人认为上述修改没有超出原权利要求和说明书的记载，符合专利法第三十三条的规定。

通过故事书修改，申请人认为，至少修改后的权利要求 1 的技术方案中原权利要求 5 的附加技术特征以及该技术方案整体在审查员指出的对比文件 1－3 中均没有任何的公开或暗示，当然，对比文件 1－3 的结合也不可能实现上述技术方案所可实现的技术效果。因此，本发明修改后的权利要求 1 相对于这些对比文件以及它们的结合具有突出的实质性特点和显著的进步，相对于对比文件 1 具有专利法第二十二条第二款规定的新颖性，相对于对比文件 1－3 以及它们的结合具有专利法第二十二条第三款规定的创造性。

同理，修改后的权利要求 6 相对于对比文件 1 具有专利法第二十二条第二款规定的新颖性，相对于对比文件 1－3 以及它们的结合具有专利法第二十二条第三款规定的创造性。另外，由于本发明其他的权利要求均是引用权利要求 1 或引用权利要求 6 的从属权利要求，因此，在权利要求 1 和 6 具有创造性的情况下，其它权利要求自然也都具备创造性。

此外，针对审查员指出原权利要求 16（修改后的权利要求 7），申请人对其引用关系进行了修改，克服了审查员指出的问题。

望审查员在上述修改的基础上，继续对本申请进行审查，并盼早日授予其专利权。

电子回执7

修改说明

根据中国专利法实施细则第 51 条规定，申请人对权利要求书进行主动修改，具体修改内容如下：

将权利要求 1 的第 8 行所记载的“部分厚度”修改为“部分的厚度”。

上述修改均未超出原始公开的范围，请审查员予以接受。

上述修改以替换页的形式提交。