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Case Docket Number: 071971-0620 **Customer Number: 53080**

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072406

UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Junji HIRASE, Akio SEBE, Naoki KOTANI, Gen OKAZAKI, Kazuhiko AIDA, Shinji TAKEOKA
FOR: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Enclosed are:

- ☒ 45 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application Number 2005-227457, filing date August 5, 2005
- ☒ 11 sheets of formal drawing.
- ☐ An assignment of the invention to _____ and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☐ Applicant is entitled to claim Small Entity status.
- ☐

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	20	-20	0	$50.00	$0.00
Independent Claims	2	-3	0	$200.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Sheets of specification and drawing ($250.00 for each 50 sheets in excess of 100)	$0.00
				Basic Filing Fee	$300.00

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Patent Search Fee	$500.00
Patent Examination Fee	$200.00
Total of Above Calculations	$1,000.00
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Assignment & Recording Fee	$0.00
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SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device and a method for fabricating the semiconductor device. Specifically, the present invention relates to a structure of a MISFET (metal insulator semiconductor field-effect transistor) and a method for fabricating the MISFET and, more particularly, relates to techniques for improving the driving power and reliability of a MISFET.

Description of Prior Art

In recent years, as the degree of integration, function and operation speed of semiconductor integrated circuit devices have been highly improved, there have been attempts to reduce a junction depth of an extension according to a scaling rule and, at the same time, to use, as a gate insulating film of a MISFET, a high dielectric constant film formed of a Hf based oxide, Al based oxide or the like, which has a relative dielectric constant of 10 or more, instead of an SiO_2 based insulating film having a relative dielectric constant of about 4.

FIGS. **16A** and **16B** are cross-sectional views illustrating respective structures of known MISFETs using a high dielectric constant gate insulating film, respectively (see Ken Watanabe, *HfSiON-CMOS technology for achieving high performance and high reliability*, Semi. Forum Japan, 2005).

As shown in FIG. **16A**, a gate electrode **105** is formed on a region of a well **102** surrounded by a STI (shallow trench isolation) **103**. The region of the well **102** surrounded by the STI serves as an active region of a substrate **101**. The gate electrode **105** is

provided on the region with a high dielectric constant gate insulating film **104** interposed therebetween. An insulating sidewall **107** is formed on each side of the gate electrode **105**. An extension region **110** is formed in part of the well **102** located under the insulating sidewall **107**. A pocket region **111** is formed in part of the well **102** located under the extension region **110**. Source/drain regions **112** are formed so that each of the source/drain regions **112** is provided in parts of the well **102** located at the external side to the extension region **110** and the pocket region **111** when viewed from the gate electrode **105**.

A structure shown in FIG. **16B** is different from a structure shown in FIG. **16A** in that a sidewall **107** is formed on each side of a gate electrode **105** with an insulating offset sidewall **106** interposed therebetween. Thus, an overlapping amount of the gate electrode **105** and an extension region **110** can be optimized in a simple manner.

SUMMARY OF THE INVENTION

However, in a structure of a known MISFET using a high dielectric constant gate insulating film, side end portions of the high dielectric constant gate insulating film are in direct contact with sidewalls. Thus, in forming sidewalls of, for example, a silicon oxide film or the like, a composition of the side end portions of the high dielectric constant gate insulating film becomes closer to SiO_2 or like other inconvenience occurs. As a result, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film is caused at gate electrode end part, so that device characteristics of the MISFET are deteriorated and the reliability of the gate insulating film is degraded.

In view of the above-described problems, it is therefore an object of the present invention to improve characteristics of a MISFET without degrading of a high dielectric constant gate insulating film.

To achieve the above-described object, the inventors of the present application have

devised a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls to prevent end portions of the high dielectric constant gate insulating film from being in contact with the sidewalls, and a method for forming the MISFET structure. In the mean time, when the high dielectric constant gate insulating film is kept remaining under the sidewalls, a capacitance between gate/drain regions is increased, thus resulting in adverse effects on circuit speed. Also, in such cases, when extension implantation or LDD (lightly doped drain) implantation is performed, it is necessary to implant ions through a high dielectric constant film. Thus, when ion implantation is performed, expansion of an implanted impurity in the depth direction is increased, in other words, a junction point of an extension or an LDD is located at a large depth, so that desired device characteristics can not be obtained. This is because implantation acceleration energy is increased for the following reasons.

Reason 1) With use of a high dielectric constant film as a gate insulating film, a desired dielectric constant can be achieved even without having the thickness of the high dielectric constant film reduced. Therefore, the thickness of the high dielectric constant film has to be set at a large value.

Reason 2) A high dielectric constant film contains heavy metal and Rp (projection range) of implanted ions is small.

To cope with this problem, the inventors have devised a MISFET structure in which a high dielectric constant gate insulating film is kept remaining under sidewalls and part of the high dielectric constant gate insulating film located under the sidewalls is made to have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under a gate electrode, and a method for forming the MISFET structure.

Specifically, a semiconductor device according to the present invention includes: a

gate electrode formed on the high dielectric constant gate insulating film; and an insulating sidewall formed on each side surface of the gate electrode. In the semiconductor device, the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

In the semiconductor device of the present invention, the insulating sidewall may include a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

When the insulating sidewall includes the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may be formed so as not to be located under the second insulating sidewall.

When the insulating sidewall includes the first insulating sidewall and the second insulating sidewall, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

When the insulating sidewall includes the first insulating sidewall and the second

insulating sidewall, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

In the semiconductor device of the present invention, the insulating sidewall may include a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film may be continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, part of the high dielectric constant gate insulating film located under the first insulating sidewall may have the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, and part of the high dielectric constant gate insulating film located under the second insulating sidewall may have a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

In the semiconductor device of the present invention, the high dielectric constant gate insulating film may include a notch at a side end portion.

The semiconductor device of the present invention may further include a buffer insulating film between the substrate and the high dielectric constant gate insulating film. In such a case, the buffer insulating film may be a silicon oxide film or a silicon oxynitride film.

In the semiconductor device of the present invention, the gate electrode may be a fully silicided gate electrode of which an entire region has been silicided.

A method for fabricating a semiconductor device according to the present invention

includes the steps of: a) forming a high dielectric constant gate insulating film on an active region of a substrate; b) forming a gate electrode on the high dielectric constant gate insulating film; c) etching, after the step b), part of the high dielectric constant gate insulating film located in an external side to the gate electrode to reduce a thickness of the part; and d) forming, after the step c), an insulating sidewall on a side surface of the gate electrode.

The method for fabricating a semiconductor device according to the present invention may further include, after the step d), the step of removing part of the high dielectric constant gate insulating film located in an external side to the insulating sidewall.

In the method for fabricating a semiconductor device according to the present invention, the insulating sidewall may include a first insulating sidewall and a second insulating sidewall, and the step d) may include the step d1) of forming the first insulating sidewall on a side surface of the gate electrode and the step of d2) of forming the second insulating sidewall on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.

When the step d) includes the step d1) and the step d2), the method for fabricating a semiconductor device according to the present invention may further include, between the step d) and the step d2), the step of removing part of the high dielectric constant gate insulating film located in the external side to the first insulating sidewall.

When the step d) includes the step d1) and the step d2), the method for fabricating a semiconductor device according to the present invention may further include, between d1) and the step d2), the step of etching part of the high dielectric gate insulating film located in an external side to the first insulating sidewall to reduce a thickness of the part; and after the step d2), the step of removing part of the high dielectric constant gate insulating film located in an external side to the second insulating sidewall.

In the method for fabricating a semiconductor device according to the present invention, the dielectric constant gate insulating film may be selectively removed by wet etching.

In the method for fabricating a semiconductor device according to the present invention, the step b) may include the step of forming a protective film for covering an upper surface of the gate electrode, and the method may further include, after the step d), the step of siliciding a surface of part of the active region located in the external side to the insulating sidewall, removing the protective film and then fully siliciding the gate electrode.

The method for fabricating a semiconductor device according to the present invention further includes, before the step a), the step of forming a buffer insulating film on the active region, and in the step a), the high dielectric constant gate insulating film may be formed on the active region with the buffer insulating film interposed therebetween.

According to the present invention, a high dielectric constant gate insulating film is continuously formed so as to extend from under a gate electrode to under a sidewall. In other words, continuity of the high dielectric constant gate insulating film at a gate end portion is maintained. Thus, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film at the gate end portion, caused by a side end portion of the high dielectric constant gate insulating film being in direct contact with a sidewall film, can be suppressed. Moreover, the high dielectric constant gate insulating film is formed so as to have a smaller thickness in the part located under the sidewall than a thickness of the part located under gate electrode. Thus, increase in a capacitance between a gate and a drain can be suppressed, so that adverse effects on circuit speed can be reduced. Furthermore, since extension implantation or LDD implantation is performed through the part of the high dielectric constant film which has a small thickness, increase in

implantation acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in an extension or a LDD in a simple manner. Therefore, device characteristics can be improved in a simple manner.

As has been described, the present invention relates to a semiconductor device and a method for fabricating the semiconductor device. Specifically, when the present invention is applied to a MISFET including a high dielectric constant gate insulating film, the effect of improving the driving power and reliability of the MISFET can be achieved and is therefore very useful.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view illustrating a structure of a semiconductor device according to a first embodiment of the present invention.

FIG. **2** is a cross-sectional view illustrating a structure of a semiconductor device according to a second embodiment of the present invention.

FIG. **3** is a cross-sectional view illustrating a structure of a semiconductor device according to a second modified example of the second embodiment of the present invention.

FIG. **4** is a cross-sectional view illustrating a structure of a semiconductor device according to a third modified example of the second embodiment of the present invention.

FIG. **5** is a cross-sectional view illustrating a structure of a semiconductor device according to a third embodiment of the present invention.

FIG. **6** is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the first embodiment of the present invention.

FIG. **7** is a cross-sectional view illustrating a structure of a semiconductor device according to a first modified example of the second embodiment of the present invention.

FIG. **8** is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the third embodiment of the present invention.

FIG. **9** is a cross-sectional view illustrating a structure of a semiconductor device according to a fourth embodiment of the present invention.

FIG. **10** is a cross-sectional view illustrating a structure of a semiconductor device according to a modified example of the fourth embodiment of the present invention.

FIGS. **11A** through **11F** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a fifth embodiment of the present invention.

FIGS. **12A** through **12G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a sixth embodiment of the present invention.

FIGS. **13A** through **13G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to a seventh embodiment of the present invention.

FIGS. **14A** through **14G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to an eighth embodiment of the present invention.

FIGS. **15A** through **15D** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the eighth embodiment of the present invention.

FIGS. **16A** and **16B** are cross-sectional views illustrating a structure of a known MISFET, respectively.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

Hereafter, a semiconductor device according to a first embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **1** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the first embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

As shown in FIG. **1**, a gate electrode **5** is formed on an active region of a p-type well **2** surrounded by a STI **3**. The p-type well **2** is formed in a substrate **1** made of, for example, silicon. The gate electrode **5** is formed on the active region with a high dielectric constant gate insulating film **4A** interposed therebetween. An insulating sidewall **7** is formed on each side surface of the gate electrode **5**. An n-type extension region **10** is formed in part of the p-type well **2** located under the sidewall **7**. Furthermore, a p-type pocket region **11** is formed in part of the p-type well **2** located under the n-type extension region **10**. N-type source/drain regions **12** are formed so that each of the source/drain regions **12** is provided in part of the p-type well **2** located in the external side to the n-type extension region **10** and the p-type pocket region **11** when viewed from the gate electrode **5**.

It is a first feature of this embodiment that the high dielectric constant gate insulating film **4A** is kept remaining not only under the gate electrode **5** but also under the sidewall **7**. That is, the high dielectric gate insulating film **4A** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film **4A** located under the sidewall **7** is smaller than a

thickness of the part of the high dielectric constant film **4A** located under the gate electrode **5**. That is, the gate insulating film **4A** is formed so as to have a convex shape.

According to this embodiment, each side end portion of the high dielectric constant gate insulating film **4A** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4A** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4A** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film **4A** under the sidewall **7** makes capacitive coupling between the gate electrode **5** and the n-type extension region **10** stronger in the vicinity of the end portion of the gate electrode **5**. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

Meanwhile, in this embodiment, because of the existence of the high dielectric constant gate insulating film **4A** under the sidewall **7**, there might be cases where a capacitance particularly between the gate electrode **5** and each of the n-type source/drain regions **12** is increased and, accordingly, a circuit speed is reduced. However, as described above, in this embodiment, the high dielectric constant gate insulating film **4A** is formed so as to have a smaller thickness in the part located under the sidewall **7** than a thickness of the part located under the gate electrode **5**. Therefore, increase in a capacitance between the gate and the drain and adverse effect on the circuit speed can be suppressed.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the

trade-off relationship, can be largely improved at the same time.

(Modified Example of First Embodiment)

Hereafter, a semiconductor device according to a modified example of the first embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **6** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall n-type MISFET) according to the modified example of the first embodiment.

As shown in FIG. **6**, this modified example is different from the first embodiment in that part of a high dielectric constant gate insulating film **4A** located under each side end portion of a sidewall **7**, i.e., a side portion of the high dielectric constant gate insulating film **4A** is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

(Second Embodiment)

Hereafter, a semiconductor device according to a second embodiment of the present invention will be described with reference to the accompanying drawings. In contrast with the first embodiment in which a single sidewall type MISFET is described, a double sidewall type MISFET (see H. Sayama et al., IEDM Tech. Dig., 2000, p. 239) in which an overlapping amount between a gate electrode and an extension region can be optimized in a simple manner will be described in the second embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this

embodiment can be achieved.

FIG. **2** is a cross-sectional view illustrating a structure of a semiconductor device according to the second embodiment. As shown in FIG. **2**, a gate electrode **5** is formed on an active region of a p-type well **2** surrounded by a STI **3**. The p-type well **2** is formed in a substrate **1** made of, for example, silicon. The gate electrode **5** is formed on the active region with a high dielectric constant gate insulating film **4B** interposed therebetween. An insulating sidewall **7** is formed on each side surface of the gate electrode **5** with an offset sidewall **6** interposed therebetween. An n-type extension region **10** is formed in each of parts of the p-type well **2** located under the offset sidewall **6** and the sidewall **7**. Furthermore, a p-type pocket region **11** is formed in part of the p-type well **2** located under the n-type extension region **10**. N-type source/drain regions **12** are formed so that each of the source/drain regions is provided in part of the p-type well **2** located in the external side to the n-type extension region **10** and the p-type pocket region **11** when viewed from the gate electrode **5**.

It is a first feature of this embodiment that the high dielectric constant gate insulating film **4B** is kept remaining not only under the gate electrode **5** but also under the offset sidewall **6**. That is, the high dielectric constant gate insulating film **4B** is continuously formed so as to extend from under the gate electrode **5** to under the offset sidewall **6**.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film **4B** located under the offset sidewall **6** is smaller than a thickness of the part of the high dielectric constant film **4B** located under the gate electrode **5**. That is, the gate insulating film **4B** is formed so as to have a convex shape.

According to this embodiment, each side end portion of the high dielectric constant gate insulating film **4B** is not in contact with the offset sidewall **6** and continuity of the

high dielectric constant gate insulating film **4B** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4B** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film **4B** under the offset sidewall **6** makes capacitive coupling between the gate electrode **5** and the n-type extension region **10** stronger in the vicinity of the end portion of the gate electrode **5**. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

Moreover, according to this embodiment, the high dielectric constant gate insulating film **4B** does not exist under the sidewall **7**. Thus, increase in a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** can be further suppressed so that a small capacitance can be maintained. Accordingly, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed at a minimum level.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the trade-off relationship, can be largely improved at the same time.

(First Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a modified example of the second embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **7** is a cross-sectional view illustrating a structure of the semiconductor

device (more specifically, a double sidewall type MISFET) according to the first modified example of the second embodiment.

As shown in FIG. **7**, this modified example is different from the second embodiment is that part of a high dielectric constant gate insulating film **4B** located under each side end portion of the offset sidewall **6**, i.e., a side portion of the high dielectric constant gate insulating film **4B** is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

(Second Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a second modified example of the second embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **3** is a cross-sectional view illustrating a structure of the semiconductor device (more specifically, a double sidewall type MISFET) according to the second modified example of the second embodiment.

This embodiment is different from the second embodiment in that a high dielectric constant gate insulating film **4C** is kept remaining not only under the gate electrode **5** and the offset sidewall **6** but also under the sidewall **7**. That is, the high dielectric constant gate insulating film **4C** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

In this modified example, the thickness of part of the high dielectric constant gate insulating film **4C** located under the sidewall **7** is the same as the thickness of part of the high dielectric constant gate insulating film **4C** located under the offset sidewall **6**. That is,

the high dielectric constant gate insulating film **4C** is formed so as to have a convex shape.

According to this modified embodiment, the high dielectric constant gate insulating film **4C** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4C** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4C** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4C** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

In this modified example, as in the first embodiment, because of the existence of the high dielectric constant gate insulating film **4C** under sidewall **7**, there might be cases where a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** is increased. However, as has been described, in this modified example, the high dielectric constant gate insulating film **4C** is formed so as to have a smaller thickness in the part located under the sidewall **7** than a thickness of the part located under the gate electrode **5**. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed.

(Third Modified Example of Second Embodiment)

Hereafter, a semiconductor device according to a third modified example of the second embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **4** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a double sidewall type MISFET) according to the

third modified example of the second embodiment.

A first difference between this modified example and the second embodiment is that in this modified example, a high dielectric constant gate insulating film **4D** is kept remaining not only under the gate electrode **5** and the offset sidewall **6** but also under the sidewall **7**. That is, the high dielectric constant gate insulating film **4D** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

A second difference between this modified example and the second embodiment is that in this modified example, the thickness of part of the high dielectric constant gate insulating film **4D** located under the offset sidewall **6** is the same as the thickness of part of the high dielectric constant gate insulating film **4D** located under the gate electrode **5**. The thickness of part of the high dielectric constant gate insulating film **4D** located under the sidewall **7** is smaller than the thickness of the part of the high dielectric constant gate insulating film **4D** located under the gate electrode **5**. That is, the high dielectric constant gate insulating film **4D** is formed so as to have a convex shape.

According to this modified example, the high dielectric constant gate insulating film **4D** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4D** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4D** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating film **4D** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

In this modified example, as in the first embodiment, because of the existence of

the high dielectric constant gate insulating film **4D** under sidewall **7**, there might be cases where a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** is increased. However, as has been described, in this modified example, the high dielectric constant gate insulating film **4D** is formed so as to have a smaller thickness in the part located under the sidewall **7** than a thickness of the part located under the gate electrode **5**. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed.

(Third Embodiment)

Hereafter, a semiconductor device according to a third embodiment of the present invention will be described with reference to the accompanying drawings. In contrast with the first embodiment in which a single sidewall type MISFET is described, a double sidewall type MISFET (see H. Sayama et al., IEDM Tech. Dig., 2000, p. 239) in which an overlapping amount between a gate electrode and an extension region can be optimized in a simple manner will be described in the third embodiment. In this embodiment, description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

FIG. **5** is a cross-sectional view illustrating a structure of a semiconductor device according to the third embodiment. As shown in FIG. **5**, a gate electrode **5** is formed on an active region of a p-type well **2** surrounded by a STI **3**. The p-type well **2** is formed in a substrate **1** made of, for example, silicon. The gate electrode **5** is formed on the active region with a high dielectric constant gate insulating film **4E** interposed therebetween. An insulating sidewall **7** is formed on each side surface of the gate electrode **5** with an offset sidewall **6** interposed therebetween. An n-type extension region **10** is formed in each of

parts of the p-type well **2** located under the offset sidewall **6** and the sidewall **7**. Furthermore, a p-type pocket region **11** is formed in part of the p-type well **2** located under the n-type extension region **10**. N-type source/drain regions **12** are formed so that each of the source/drain is provided in part of the p-type well **2** located in the external side to the n-type extension region **10** and the p-type pocket region **11** when viewed from the gate electrode **5**.

It is a first feature that the high dielectric constant gate insulating film **4E** is kept remaining not only under the gate electrode **5** and but also under each of the offset sidewall **6** and the sidewall **7**. That is, the high dielectric constant gate insulating film **4E** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**.

It is a second feature of this embodiment that the thickness of the part of the high dielectric constant gate insulating film **4E** located under the offset sidewall **6** is smaller than a thickness of the part of the high dielectric constant film **4E** located under the gate electrode **5** and the thickness of the high dielectric constant gate insulating film **4E** located under the sidewall **7** is smaller than the thickness of the part of the high dielectric constant film **4E** located under the offset sidewall **6**. That is, the gate insulating film **4E** is formed so as to have a double convex shape.

According to this embodiment, the high dielectric constant gate insulating film **4E** is continuously formed so as to extend from under the gate electrode **5** to under the sidewall **7**. Thus, even when the offset sidewall **6** has a very small width (thickness), each side end portion of the high dielectric constant gate insulating film **4E** is not in contact with the sidewall **7** and continuity of the high dielectric constant gate insulating film **4E** at an end portion of the gate electrode **5** is maintained. Accordingly, reduction in the dielectric constant and insulation property of the high dielectric constant gate insulating

film **4E** at the end portion of the gate electrode **5** can be suppressed, so that deterioration of device characteristics of the MISFET and reduction in the reliability of the gate insulating film can be prevented.

According to this embodiment, the existence of the high dielectric constant gate insulating film **4E** under the offset sidewall **6** makes capacitive coupling between the gate electrode **5** and the n-type extension region **10** stronger at the vicinity of the end portion of the gate electrode **5**. As a result, a high overlapping effect between a gate and a drain can be achieved (see T. Hori, IEDM Tech. Dig., 1989, p. 777). Therefore, device characteristics and hot carrier reliability can be improved at the same time.

As in the first embodiment, in this embodiment, because of the existence of the high dielectric constant gate insulating film **4E** under sidewall **7**, there might be cases where a capacitance between the gate electrode **5** and each of the n-type source/drain regions **12** is increased and, accordingly, a circuit speed is reduced. However, as has been described, in this embodiment, the high dielectric constant gate insulating film **4E** is formed so that the thickness of the high dielectric constant gate insulating film **4E** is reduced in the part located under the offset sidewall **6** and then is further reduced in the part located under the sidewall **7**. Therefore, increase in a parasitic capacitance and adverse effects on circuit speed due to the increase can be suppressed so that the parasitic capacitance is a very low level.

As has been described, according to this embodiment, device/circuit characteristics of an MISFET and the reliability of a gate insulating film, which are conventionally in the trade-off relationship, can be largely improved at the same time.

(Modified Example of Third Embodiment)

Hereafter, a semiconductor device according to a modified example of a third

embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **8** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a double sidewall type MISFET) according to the modified example of the third embodiment.

As shown in FIG. **8**, this modified example is different from the first embodiment in that part of a high dielectric constant gate insulating film **4E** located under each side end portion of a sidewall **7**, i.e., a side portion of the high dielectric constant gate insulating film **4E** is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

(Fourth Embodiment)

Hereafter, a semiconductor device according to a fourth embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **9** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the fourth embodiment of the present invention. In this embodiment description will be made using an n-type MISFET as an example. However, even when the present invention is applied to a p-type MISFET, the same effects as those of this embodiment can be achieved.

As shown in FIG. **9**, this embodiment is different from the first embodiment in that, for example, a silicon oxide film, a silicon oxynitride film or the like is provided as a buffer insulating film **25** between a substrate **1** and a high dielectric constant gate insulating film **4A**.

According to this embodiment, in addition to the effects of the first embodiment, an

interface between a substrate and a gate insulating film can be advantageously kept in a normal state. Specifically, by forming the high dielectric constant gate insulating film **4A** on the substrate **1** with the buffer insulating film **25** interposed therebetween, deterioration of an interface between a substrate and a gate insulating film can be suppressed, compared to the case where the high dielectric constant gate insulating film **4A** is formed directly on the substrate **1**.

In this embodiment, the buffer insulating film **25** is provided between the high dielectric constant gate insulating film **4A** of the first embodiment and the substrate **1**. However, instead of this structure, even if the buffer insulating film **25** is provided between the substrate **1** and the high dielectric constant gate insulating film **4B** of the second embodiment, the high dielectric constant gate insulating film **4C** of the second modified example of the second embodiment, the high dielectric constant gate insulating film **4D** of the third modified example of the second embodiment or the high dielectric constant gate insulating film **4E** of the third embodiment, the same effects as those of this embodiment can be achieved. Moreover, instead of providing the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**, a buffer insulating film may be provided between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**. With such a structure, compared to the case where the gate electrode **5** is directly formed on the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**, deterioration of an interface between a gate electrode and a gate insulating film can be prevented. As another alternative, a buffer insulating film may be formed between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E** as well as forming the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4E**. With such a structure, deterioration of each of the substrate-gate insulating film

interface and the gate insulating film-gate electrode interface can be prevented at the same time.

(Modified Example of Fourth Embodiment)

Hereafter, a semiconductor device according to a modified example of the fourth embodiment of the present invention will be described with reference to the accompanying drawings. FIG. **10** is a cross-sectional view illustrating a structure of a semiconductor device (more specifically, a single sidewall type MISFET) according to the modified example of the fourth embodiment.

As shown in FIG. **10**, this modified example is different from the fourth embodiment in that part of a laminated insulating film of a high dielectric constant gate insulating film **4A** and a buffer insulating film **25** located under a side end portion of each sidewall **7**, i.e., a side end portion of the laminated insulating film is removed in a notch shape, so that a notch **20** is provided.

According to this modified example, adverse effects on circuit speed due to increase in a capacitance between a gate electrode **5** and each of n-type source/drain regions **12** can be further suppressed.

In this modified example, the notch **20** is provided in the side end portion of the laminated insulating film of the high dielectric constant gate insulating film **4A** and the buffer insulating film **25** of the first embodiment. However, instead of this structure, even if a notch is provided in a side end portion of a laminated insulating film of the buffer insulating film **25** and the high dielectric constant gate insulating film **4B** of the second embodiment, the high dielectric constant gate insulating film **4C** of the second modified example of the second embodiment, the high dielectric constant gate insulating film **4D** of the third modified example of the second embodiment or the high dielectric constant gate insulating film **4E** of the third embodiment, the same effects of the modified example can

be achieved. In such cases, a buffer insulating film may be provided between the gate electrode **5** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4D** as well as forming the buffer insulating film **25** between the substrate **1** and the high dielectric constant gate insulating film **4A**, **4B**, **4C**, **4D** or **4D**.

(Fifth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a fifth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. **11A** through **11F** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the fifth embodiment.

First, as shown in FIG. **11A**, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B (boron) is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **11B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **11C**, for example, a gate electrode material film **5A** is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film **5A** so as to cover a gate electrode formation region, and then the gate electrode material film **5A** is etched using the resist pattern as a mask, thereby forming, as shown in FIG. **11D**, a gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4** becomes about 2 nm. Subsequently, using the gate electrode **5** as a mask, for example, As (arsenic) is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm $^{-2}$, thereby forming an n-type extension region **10**. Thereafter, using the gate electrode **5** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm $^{-2}$, thereby forming a p-type pocket region **11**. In this case, the n-type extension region **10** may be formed after forming the p-type pocket region **11**.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. **11E**, an insulating sidewall **7** on each side surface of the gate electrode **5**.

Next, using the gate electrode **5** and the sidewall **7** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as

shown in FIG. **11F**, n-type source/drain regions **12** are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **1**) of the first embodiment can be realized in a relatively simple manner.

Meanwhile, the high dielectric constant gate insulating film **4** contains heavy metal and thus Rp (projection range) of implanted ions passing through the high dielectric constant gate insulating film **4** tends to be small. Therefore, in the process step of FIG. **11D**, if without reducing the thickness of the high dielectric constant gate insulating film **4**, ion implantation is performed to the substrate **1** covered with the high dielectric constant gate insulating film **4** in the external side to the gate electrode **5** to form the n-type extension region **10** or the p-type pocket region **11**, an acceleration energy has to be increased. However, in this embodiment, the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** has a reduced thickness, so that increase in acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner.

In this embodiment, after the sidewall **7** has been formed, for example, part of the high dielectric constant gate insulating film **4** located in the external side to the sidewall **7** may be removed by wet etching using hydrofluoric acid or the like or selective dry etching. In such a case, when wet etching is used, part of the high dielectric constant gate insulating film **4** located under each side end portion of the sidewall **7**, i.e., a side end portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape, so that a notch is formed. Thus, the MISFET structure (see FIG. **6**) of the modified example of the first embodiment can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of

the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less (so that a surface of the substrate **1** is not exposed).

(Sixth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a sixth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. **12A** through **12G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the sixth embodiment.

First, as shown in FIG. **12A**, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **12B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e.,

about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **12C**, for example, a gate electrode material film **5A** is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film **5A** so as to cover a gate electrode formation region, and then the gate electrode material film **5A** is etched using the resist pattern as a mask, thereby forming, as shown in FIG. **12D**, a gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4** becomes about 2 nm.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 10 nm, and then the insulating film is etched back to form, as shown in FIG. **12E**, an insulating offset sidewall **6** on each side surface of the gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed by wet etching using, for example, hydrofluoric acid or selective dry etching. Subsequently, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm^{-2}, thereby forming an n-type extension region **10**. Thereafter, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm^{-2}, thereby forming a p-type pocket region **11**.

Next, an insulating film is deposited over the substrate **1** to a thickness of about

50 nm, and then the insulating film is etched back to form, as shown in FIG. **12F**, an insulating sidewall **7** on each side surface of the gate electrode **5** with the offset sidewall **6** interposed therebetween.

Next, using the gate electrode **5**, the offset sidewall **6** and the sidewall **7** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. **12G**, n-type source/drain regions **12** are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **2**) of the second embodiment can be realized in a relatively simple manner.

In this embodiment, after the offset sidewall **6** has been formed, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed , for example, by wet etching using hydrofluoric acid or the like. When this wet etching is performed, part of the high dielectric constant gate insulating film **4** located under each side end portion of the offset sidewall **6**, i.e., a side end portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape, so that a notch is formed. Thus, the MISFET structure (see FIG. **7**) of the first modified example of the second embodiment can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably

reduced to about 2 nm or less (so that a surface of the substrate **1** is not exposed).

In this embodiment, after the offset sidewall **6** has been formed, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, and then ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** is performed. However, instead of performing these process steps, ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** may be performed after the offset sidewall **6** is formed and with part of the high dielectric constant gate insulating film **4** having a reduced thickness remaining in the external side to the offset sidewall **6**. Even in this manner, according to this embodiment, the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** has a reduced thickness, so that increase in acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner. In this case, ion implantation for forming an extension region and a pocket region of an MISFET having a different channel type or another power supply system and being provided on the same substrate may be performed after ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** and then removal of the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6**.

(Seventh Embodiment)

Hereafter, a method for fabricating a semiconductor device according to a seventh embodiment of the present invention will be described with reference to the accompanying drawings. FIGS. **13A** through **13G** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the seventh embodiment.

First, as shown in FIG. **13A**, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **13B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **13C**, for example, a gate electrode material film **5A** is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm.

Next, a resist pattern (not shown) is formed on the gate electrode material film **5A** so as to cover a gate electrode formation region, and then the gate electrode material film **5A** is etched using the resist pattern as a mask, thereby forming, as shown in FIG. **13D**, a gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4** becomes about 2 nm.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 5 nm, and then the insulating film is etched back to form, as shown in FIG. **13E**, an insulating offset sidewall **6** on each side surface of the gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** which is not covered by the gate electrode **5** and the offset sidewall **6** is further removed by about 1 nm. Thus, the thickness of part of the high dielectric gate insulating film **4** located in the external side to the offset sidewall **6** can be reduced to a thickness of about 1 nm. Then, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm^{-2}, thereby forming an extension region **10**. Thereafter, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm^{-2}, thereby forming a p-type pocket region **11**.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. **13F**, an insulating sidewall **7** on each side surface of the gate electrode **5** with the offset sidewall **6** interposed therebetween.

Next, using the gate electrode **5**, the offset sidewall **6** and the sidewall **7** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. **13G**, n-type source/drain regions **12** are formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **5**) of the third embodiment can be realized in a relatively simple manner.

In this embodiment, the high dielectric constant gate insulating film **4E** is formed

so that the thickness of the high dielectric constant gate insulating film **4E** is reduced in the part located under the offset sidewall **6** and then is further reduced in the part located in the external side to the offset sidewall **6**. Therefore, even when ion implantation for forming the n-type extension region **10** is performed using the gate electrode **5** and the offset sidewall **6** as a mask, increase in acceleration energy can be suppressed at a minimum level. Accordingly, a shallow junction can be formed at an even shallower depth in the n-type extension region **10** in a simple manner and thus device characteristics can be improved in a simple manner.

In this embodiment, after the sidewall **7** has been formed, the part of the high dielectric constant gate insulating film **4** located in the external side to the sidewall **7** may be removed, for example, by wet etching using hydrofluoric acid or the like or selective dry etching. Moreover, in such a case, part of the high dielectric constant gate insulating film **4** located under each side end portion of the sidewall **7**, i.e., each side end portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape. Thus, the MISFET structure (see FIG. **8B**) of the modified embodiment of the third embodiment can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited either under the offset sidewall **6** or under the sidewall **7**. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less.

(Eighth Embodiment)

Hereafter, a method for fabricating a semiconductor device according to an eighth embodiment of the present invention will be described with reference to the accompanying drawings. In this embodiment, description will be made using a method for fabricating an n-type MISFET as an example. FIGS. **14A** through **14G** and FIGS. **15A** through **15D** are cross-sectional views illustrating respective steps for fabricating a semiconductor device according to the eighth embodiment.

First, as shown in FIG. **14A**, for example, a STI **3** which is to be an isolation region is selectively formed on a substrate **1** of, for example, silicon and then, for example, B is ion implanted into the substrate **1** at an implantation energy of 300 keV and a dose of 1×10^{13} cm^{-2}. Thus, a p-type well **2** which is to be an active region is formed. Subsequently, ion implantation (of B at an implantation energy of 150 keV and a dose of 1×10^{13} cm^{-2}) for punch-through stopper formation and ion implantation (of B at an implantation energy of 20 keV and a dose of 5×10^{12} cm^{-2}) for channel formation are performed.

Next, as shown in FIG. **14B**, as a buffer insulating film, for example, a silicon oxide film (not shown) is formed on the active region of the p-type well **2** surrounded by the STI **3** so as to have a thickness of about 0.5 nm and then, as a high dielectric constant film **4**, for example, a HfSiON film is deposited thereon to a thickness of about 4 nm (i.e., about 1 nm in terms of an equivalent oxide thickness).

Next, as shown in FIG. **14C**, as a gate electrode material film **5A**, for example, a polysilicon film is formed on the high dielectric constant gate insulating film **4** so as to have a thickness of about 100 nm, and then as a cover film (protective film) **15**, for example, a silicon oxide film is deposited over the gate electrode material film **5A** to a thickness of about 10 nm.

Next, a resist pattern (not shown) is formed on the cover film **15** so as to cover a

gate electrode formation region, and then the cover film **15** and the gate electrode material film **5A** are etched in this order using the resist pattern as a mask, thereby forming, as shown in FIG. **14D**, a gate electrode **5** with its upper surface covered by the cover film **15**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is removed by a thickness of about 2 nm by selective etching. Thus, a thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** can be reduced so that a remaining thickness of the part of the high dielectric constant gate insulating film **4** becomes about 2 nm.

Next, an insulating film is deposited over the substrate **1** to a thickness of about 10 nm, and then the insulating film is etched back to form, as shown in FIG. **14E**, an insulating offset sidewall **6** on each side surface of the gate electrode **5**. Thereafter, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, for example, by wet etching using hydrofluoric acid or the like or selective dry etching. Subsequently, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 2 keV and a dose of 1×10^{15} cm^{-2}, thereby forming an n-type extension region **10**. Thereafter, using the gate electrode **5** and the offset sidewall **6** as a mask, for example, B is ion implanted into the substrate **1** at an implantation energy of 10 keV and a dose of 3×10^{13} cm^{-2}, thereby forming a p-type pocket region **11**.

Next, an insulating film (for example, a SiN film) is deposited over the substrate **1** to a thickness of about 50 nm, and then the insulating film is etched back to form, as shown in FIG. **14F**, an insulating sidewall **7** on each side surface of the gate electrode **5** with the offset sidewall **6** interposed therebetween.

Next, using the gate electrode **5**, the offset sidewall **6** and the sidewall **7** as a mask, for example, As is ion implanted into the substrate **1** at an implantation energy of 10 keV

and a dose of 5×10^{15} cm^{-2}, and then, for example, spike RTA (rapid thermal annealing) is performed at a temperature of about 1050 °C, thereby activating the implanted impurity. Thus, as shown in FIG. **14G**, n-type source/drain regions **12** are formed.

Next, a metal film (for example, a Ni film) is deposited over the substrate **1** to a thickness of about 10 nm, and RTA is performed to bring a silicon portion of the substrate **1** and the metal film into reaction. Thus, as shown in FIG. **15A**, a silicide layer **13** is formed on the n-type source/drain regions **12**. Thereafter, unreacted part of the metal film which remains on the substrate **1** is exfoliated or removed.

Next, as shown in FIG. **15B**, an interlayer insulating film **14** is deposited over the substrate **1** as well as the gate electrode **5** to a thickness of about 400 nm.

Next, as shown in FIG. **15C**, the interlayer insulating film **14** is polished, for example, by CMP (chemical mechanical polishing) so that a surface of the interlayer insulating film **14** becomes at the same level as the upper surface of the cover film **15**, and then the exposed cover film **15** is removed by etching. In this case, respective upper portions of the interlevel insulating film **14** which has undergone through CMP and the offset sidewall **6** are also removed.

Next, a metal film (for example, a Ni film) is deposited over the substrate **1** to a thickness of about 100 nm, and then RTA is performed to bring a silicon portion of the gate electrode **5** and the metal film into reaction. Thus, as shown in FIG. **15D**, a fully silicided gate electrode **16** (obtained by siliciding the entire region over the high dielectric constant gate insulating film **4**) is formed.

According to the above-described fabrication method of this embodiment, the MISFET structure (see FIG. **2**) of the second embodiment using a FUSI (full silicide) structure can be realized in a relatively simple manner.

In this embodiment, when the offset sidewall **6** has been formed and then part of

the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, for example, by wet etching using hydrofluoric acid or the like, part of the high dielectric constant gate insulating film **4** located under each side end portion of the offset sidewall **6**, i.e., each side portion of the high dielectric constant gate insulating film **4** may be removed in a notch shape so that a notch is provided. Thus, the MISFET structure (see FIG. **7**) of the first modified example of the second embodiment using a FUSI structure can be realized in a simple manner.

In this embodiment, a target thickness for reduction in the thickness of the part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is not particularly limited. However, for example, when an HfSiON film is used as the high dielectric constant gate insulating film **4**, to suppress increase in a capacitance between a gate and a grain, the thickness of part of the high dielectric constant gate insulating film **4** located in the external side to the gate electrode **5** is preferably reduced to about 2 nm or less (so that a surface of the substrate **1** is not exposed).

In this embodiment, after the offset sidewall **6** has been formed, part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** is removed, and then ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** is performed. However, instead of performing these process steps, ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** may be performed after the offset sidewall **6** is formed and with part of the high dielectric constant gate insulating film **4** having a reduced thickness remaining in the outer side offset sidewall **6**. Even in this manner, according to this embodiment, the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6** has a reduced thickness, so that increase in acceleration energy can be suppressed. Accordingly, a shallow junction can be formed in the n-type extension region

10 in a simple manner and thus device characteristics can be improved in a simple manner. In this case, ion implantation for forming an extension region and a pocket region of an MISFET having a different channel type or another power supply system and formed on the same substrate may be performed after ion implantation for forming the n-type extension region **10** and the p-type pocket region **11** and then removal of the part of the high dielectric constant gate insulating film **4** located in the external side to the offset sidewall **6**.

In this embodiment, the MISFET structure of the second embodiment using a FUSI structure has been formed. However, instead of forming the MISFET structure of the second embodiment, the MISFET structure of the first embodiment, the modified example of the first embodiment, each of the modified examples of the second embodiment, the third embodiment, the modified example of the third embodiment, the fourth embodiment or the modified example of the fourth embodiment may be formed using a FUSI structure.

In each of the first through eighth embodiments, a single layer structure of a SiN film has been used as an example of the sidewall **7**. However, instead of the single layer structure of a SiN film, for example, a double layer structure of a combination of an oxide film (SiO_2 film) and a nitride film (SiN film) (for example, including a SiO_2 layer as an lower layer and a SiN film as an upper layer), a triple layer structure (for example including an SiO_2 film as a lower layer, a SiN film as a middle layer and a SiO_2 film as an upper layer) or the like may be used.

In each of the first through eighth embodiments, instead of the n-type extension region **10**, a LDD may be formed.

In each of the fifth through eighth embodiments, instead of the n-type MISFET, a p-type MISFET may be formed.

In each of the fifth through eighth embodiments, to prevent deterioration of the

interface of a gate insulating film and a gate electrode, a buffer insulating film may be formed between the gate electrode **5** and the high dielectric constant gate insulating film **4** so as to have a thickness of about 0.2 nm.

In each of the first through eighth embodiments, a shape of each side surface of the high dielectric constant gate insulating film **4** in which the notch **20** is provided in the part located under each side end portion of the sidewall **7** or the offset sidewall **6** is not limited to a semicircular shape shown in FIG. **6**, **7**, **8** or **10**. For example, each side surface of the high dielectric constant gate insulating film **4** may be a perpendicular plane to the substrate surface. That is, a side surface of the high dielectric constant gate insulating film **4** may be located at a predetermined distance from a side end surface of the sidewall **7** or the offset sidewall **6** toward the gate electrode **5**.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a high dielectric constant gate insulating film formed on an active region in a substrate;

a gate electrode formed on the high dielectric constant gate insulating film; and

an insulating sidewall formed on each side surface of the gate electrode,

wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, and

at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

2. The semiconductor device of claim 1, wherein the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

3. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.

4. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is continuously formed so as to extend to under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

5. The semiconductor device of claim 2, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

6. The semiconductor device of claim 1, wherein the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the second insulating sidewall,

part of the high dielectric constant gate insulating film located under the first insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has a smaller thickness than a thickness of part of the high dielectric

constant gate insulating film located under the gate electrode.

7. The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.

8. The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

9. The semiconductor device of claim 8, wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film.

10. The semiconductor device of claim 1, wherein the gate electrode is a fully silicided gate electrode of which an entire region has been silicided.

11. A method for fabricating a semiconductor device, the method comprising the steps of:

a) forming a high dielectric constant gate insulating film on an active region of a substrate;

b) forming a gate electrode on the high dielectric constant gate insulating film;

c) etching, after the step b), part of the high dielectric constant gate insulating film located in an external side to the gate electrode to reduce a thickness of the part; and

d) forming, after the step c), an insulating sidewall on a side surface of the gate electrode.

12. The method of claim 11, further comprising, after the step d), the step of removing part of the high dielectric constant gate insulating film located in an external side

to the insulating sidewall.

13. The method of claim 11, wherein the insulating sidewall includes a first insulating sidewall and a second insulating sidewall, and

the step d) includes the step d1) of forming the first insulating sidewall on a side surface of the gate electrode and the step of d2) of forming the second insulating sidewall on the side surface of the gate electrode with the first insulating sidewall interposed therebetween.

14. The method of claim 13, further comprising, between the step d1) and the step d2), the step of removing part of the high dielectric constant gate insulating film located in the external side to the first insulating sidewall.

15. The method of claim 13, further comprising:

between d1) and the step d2), the step of etching part of the high dielectric gate insulating film located in an external side to the first insulating sidewall to reduce a thickness of the part; and

after the step d2), the step of removing part of the high dielectric constant gate insulating film located in an external side to the second insulating sidewall.

16. The method of claim 12, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

17. The method of claim 14, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

18. The method of claim 15, wherein the high dielectric constant gate insulating film is selectively removed by wet etching.

19. The method of claim 11, wherein the step b) includes the step of forming a protective film for covering an upper surface of the gate electrode, and

the method further includes, after the step d), the step of siliciding a surface of part of the active region located in the external side to the insulating sidewall, removing the protective film and then fully siliciding the gate electrode.

20. The method of claim 11, further comprising before the step a), the step of forming a buffer insulating film on the active region,

wherein in the step a), the high dielectric constant gate insulating film is formed on the active region with the buffer insulating film interposed therebetween.

ABSTRACT OF THE DISCLOSURE

A semiconductor device includes: a high dielectric constant gate insulating film formed on an active region in a substrate; a gate electrode formed on the high dielectric constant gate insulating film; and an insulating sidewall formed on each side surface of the gate electrode. The high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall. At least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

FIG. 1

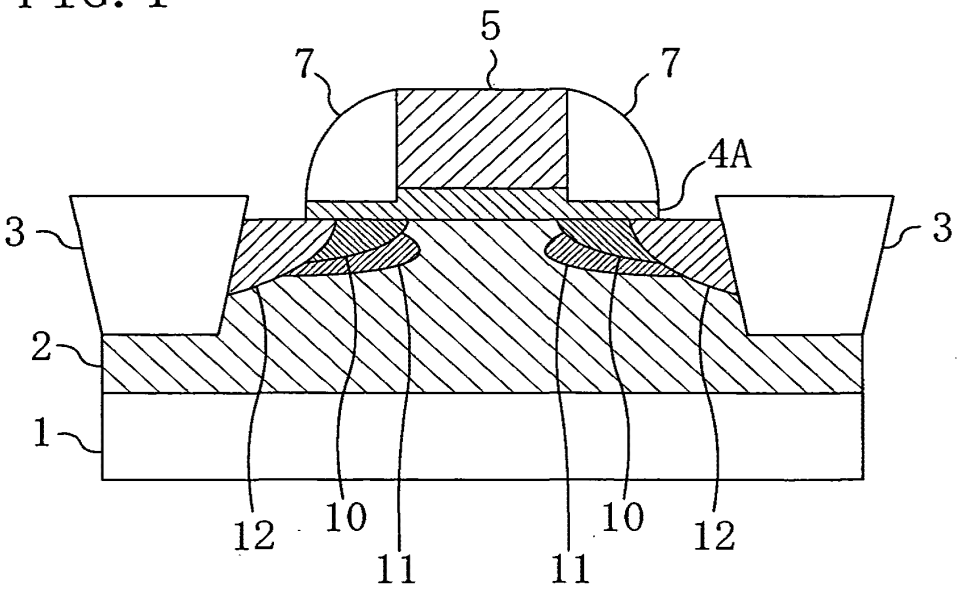

FIG. 2

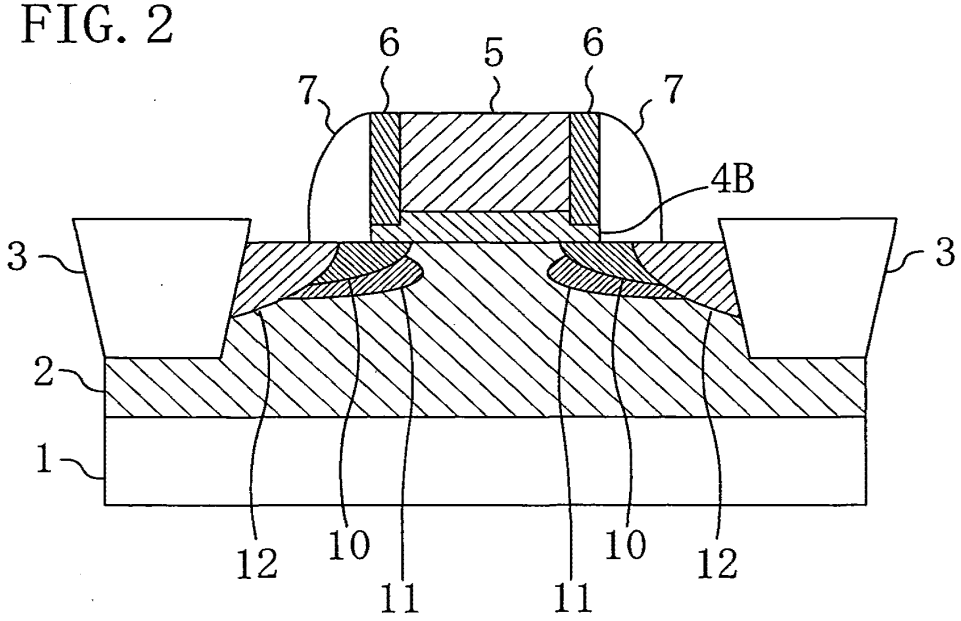

FIG. 3

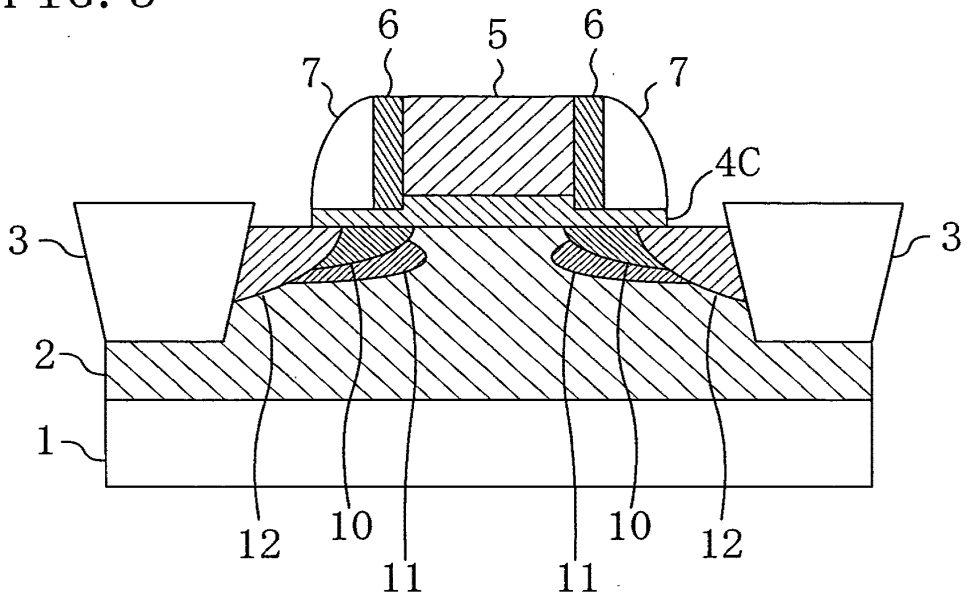

FIG. 4

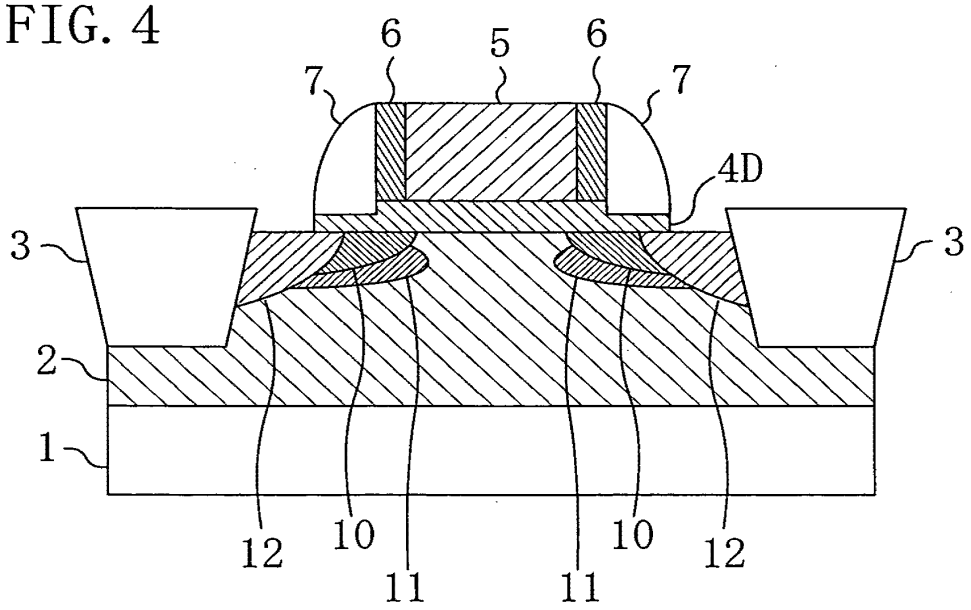

FIG. 5

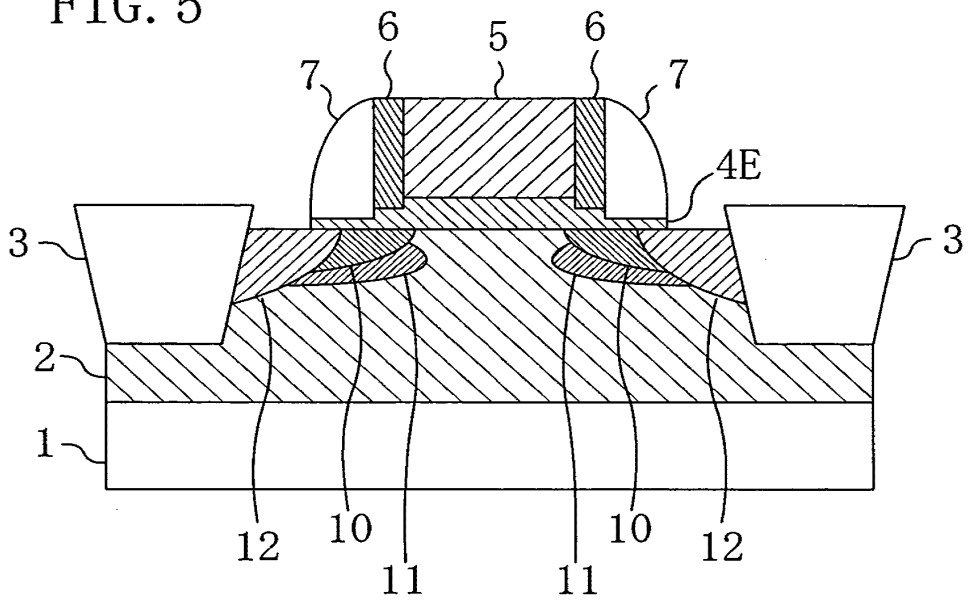

FIG. 6

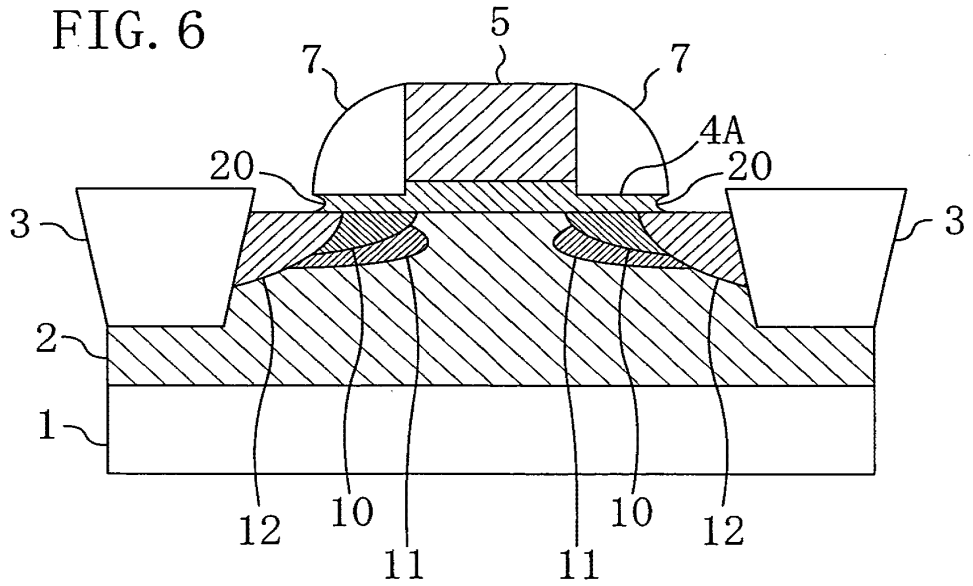

FIG. 7

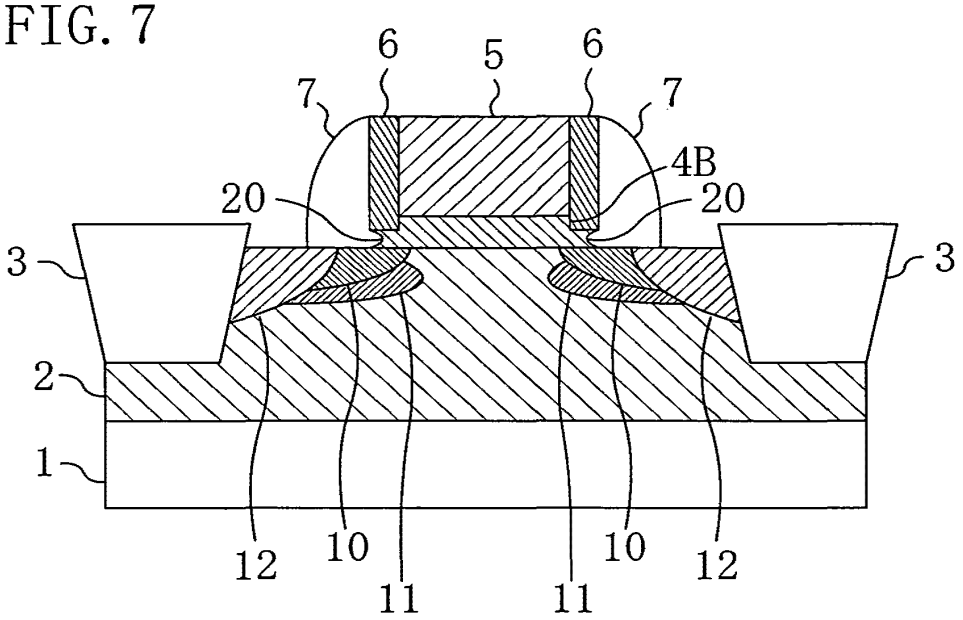
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FIG. 8

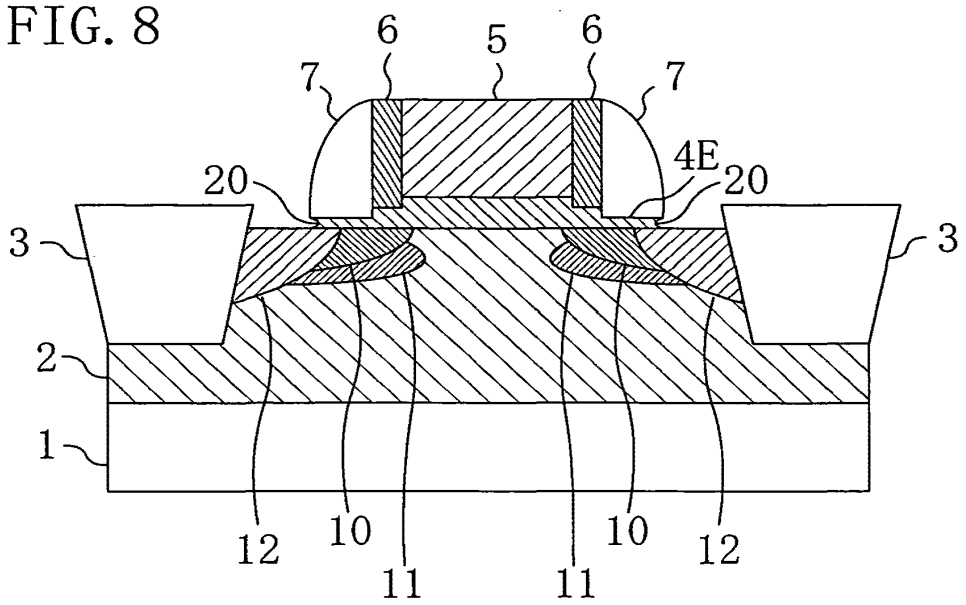
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FIG. 9

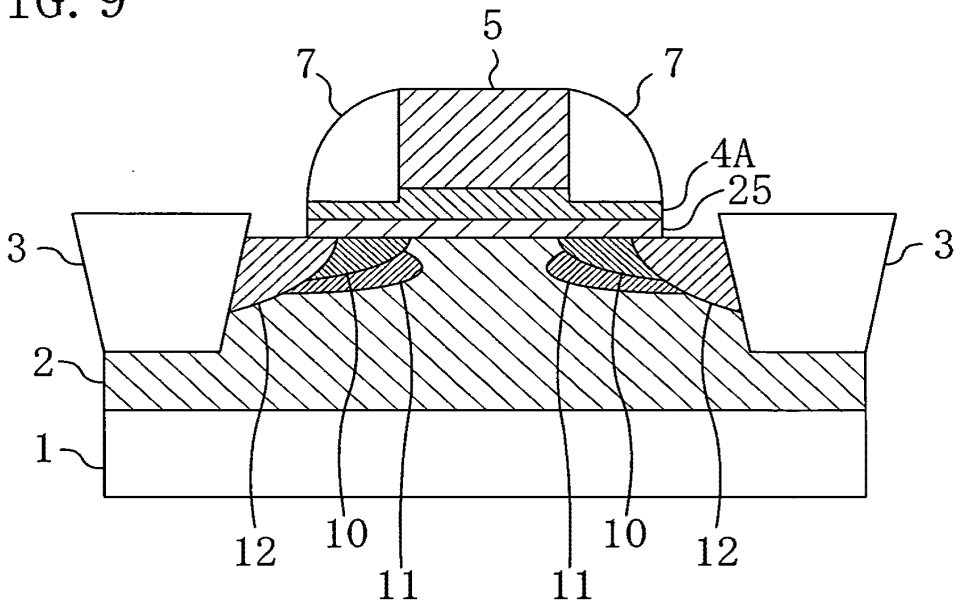
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FIG. 10

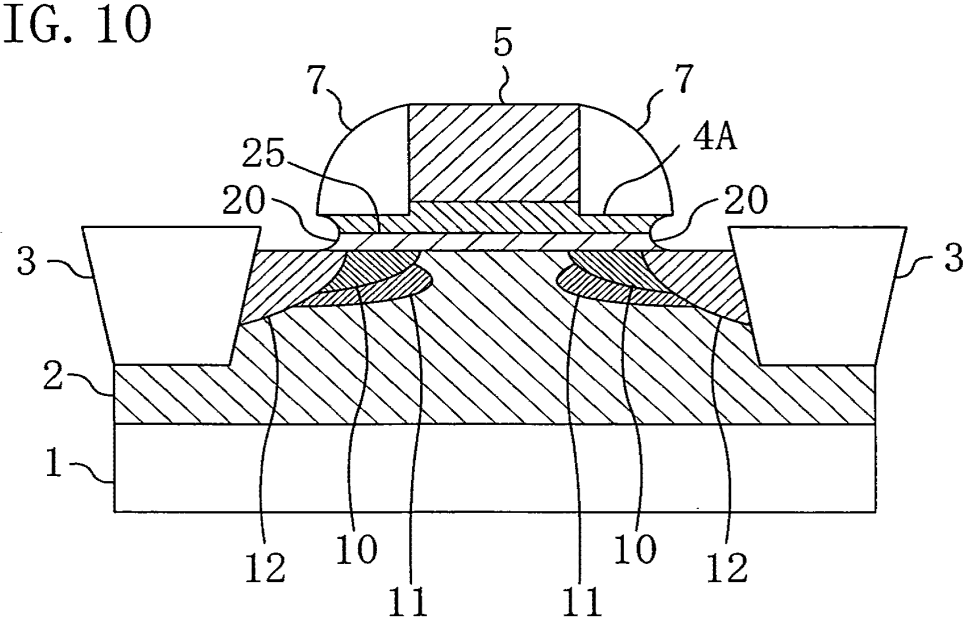
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FIG. 11A

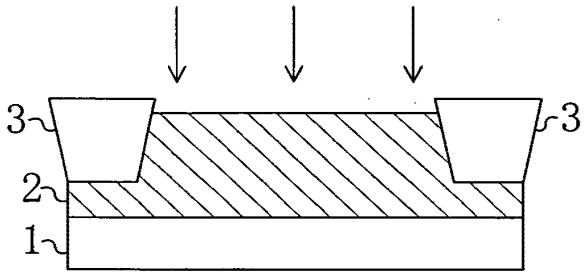


FIG. 11D

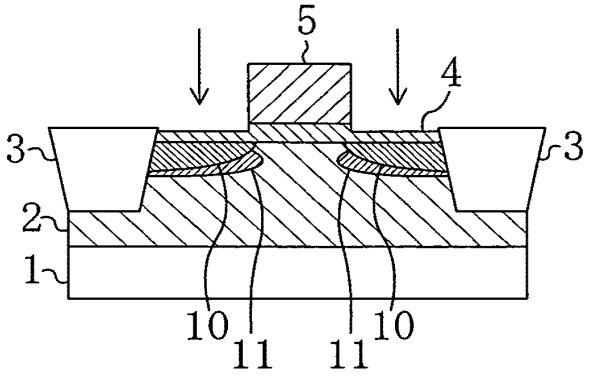


FIG. 11B

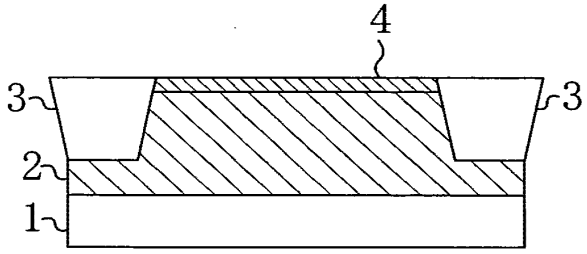


FIG. 11E

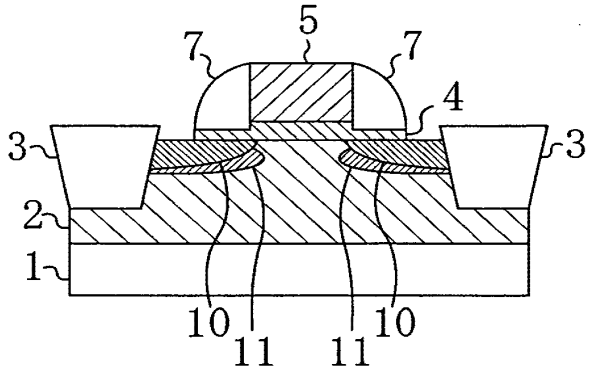


FIG. 11C

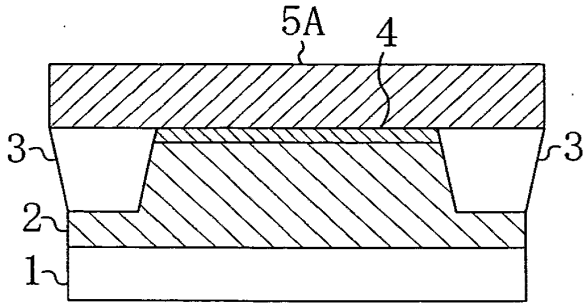


FIG. 11F

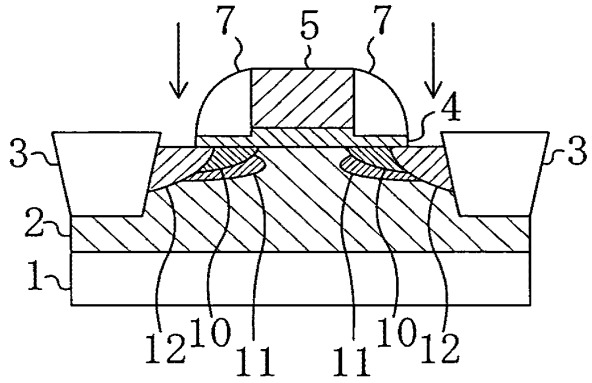


FIG. 12A

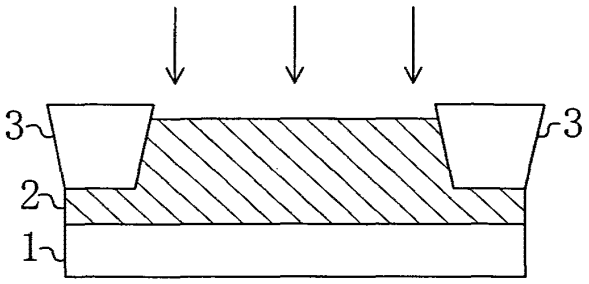


FIG. 12E

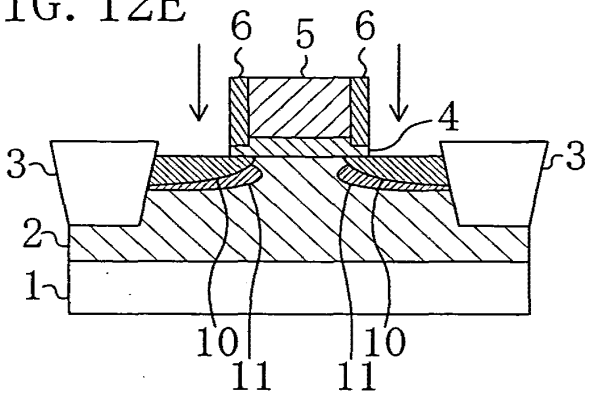


FIG. 12B

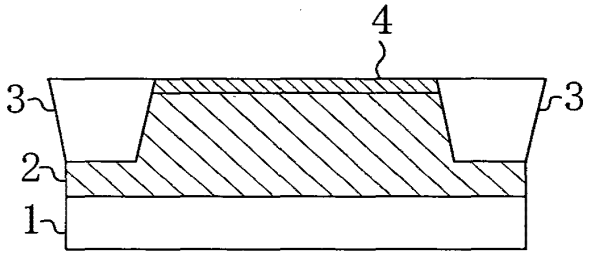


FIG. 12F

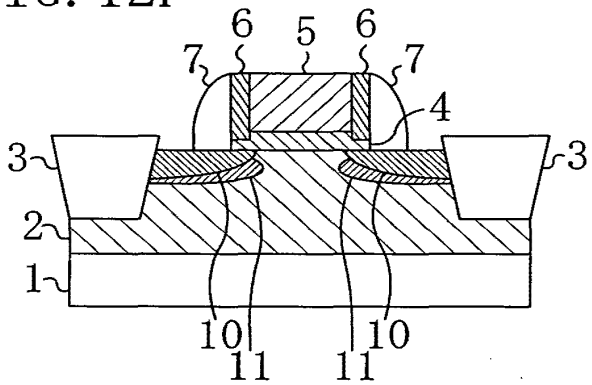


FIG. 12C

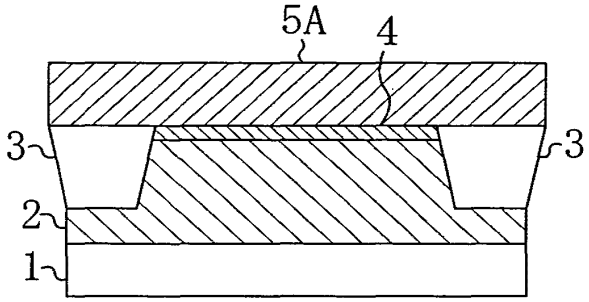


FIG. 12G

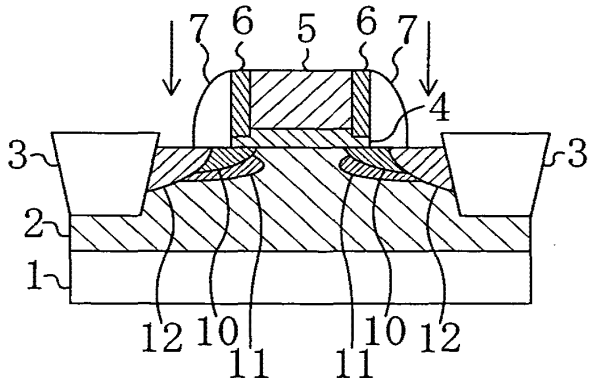


FIG. 12D

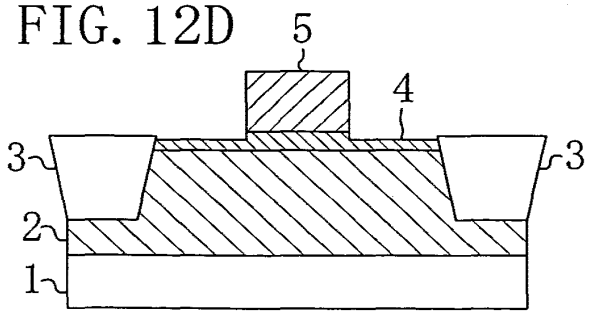


FIG. 13A

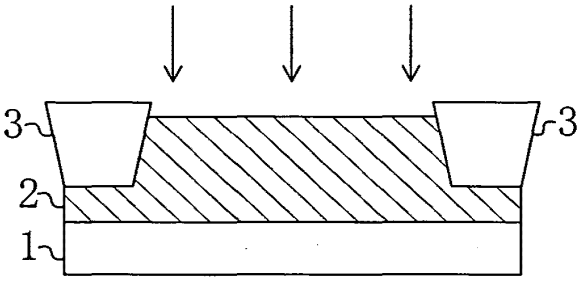


FIG. 13E

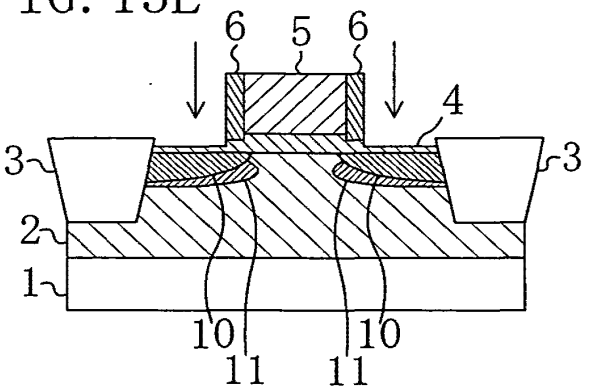


FIG. 13B

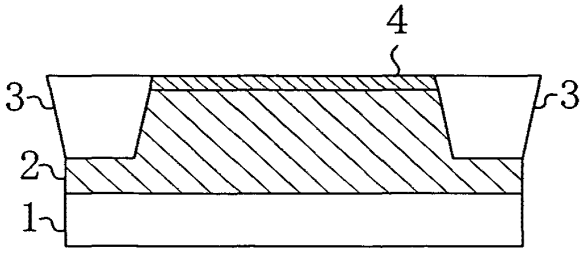


FIG. 13F

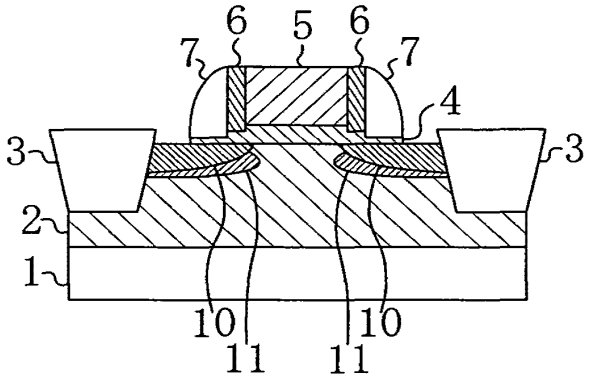


FIG. 13C

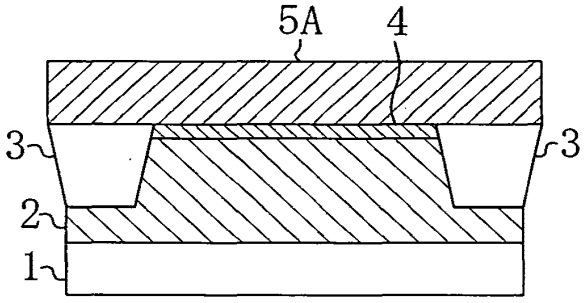


FIG. 13G

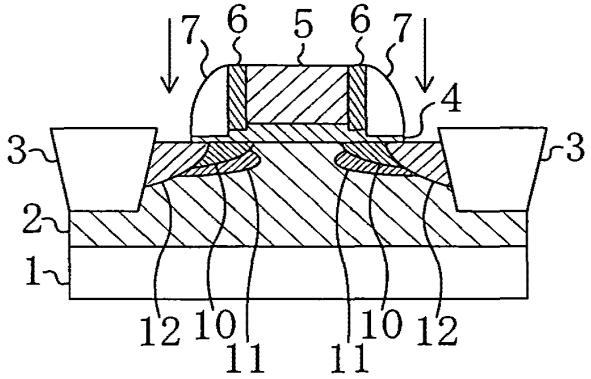


FIG. 13D

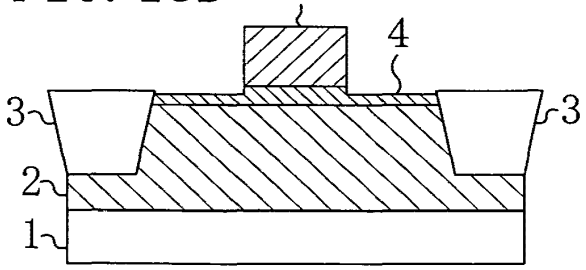


FIG. 14A

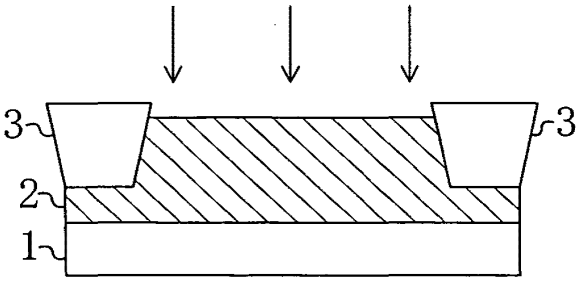


FIG. 14B

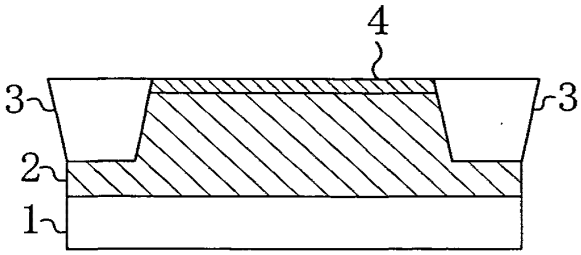


FIG. 14C

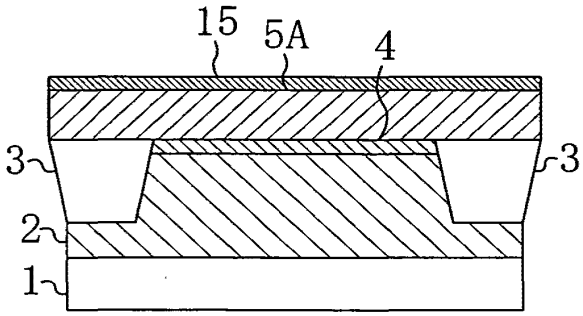


FIG. 14D

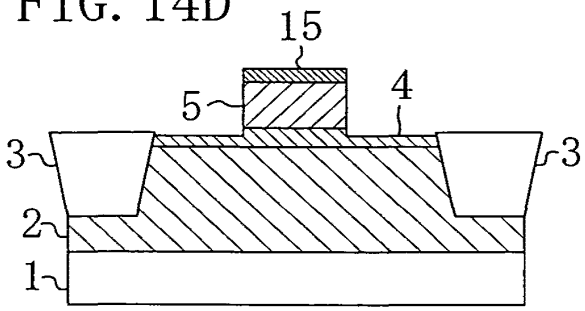


FIG. 14E

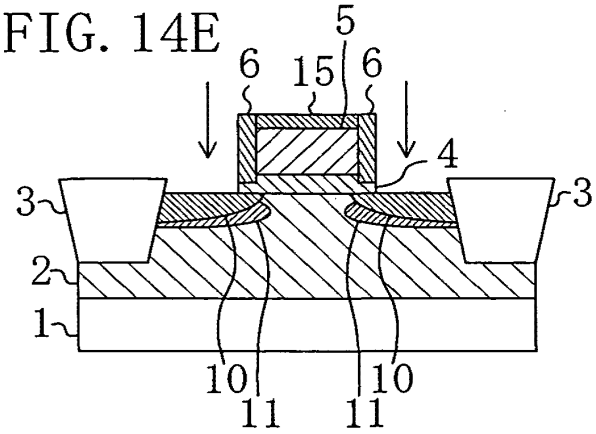


FIG. 14F

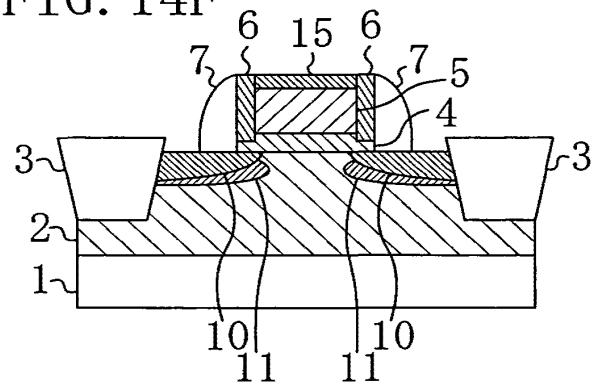


FIG. 14G

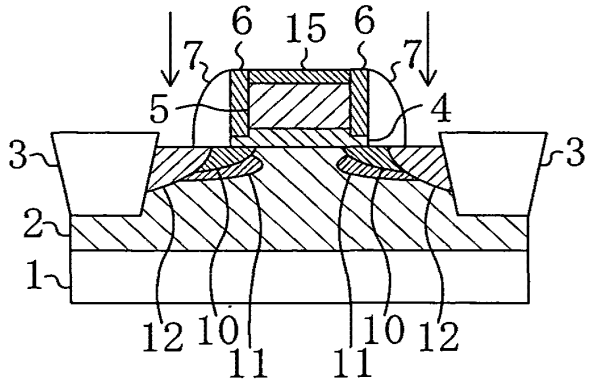


FIG. 15A

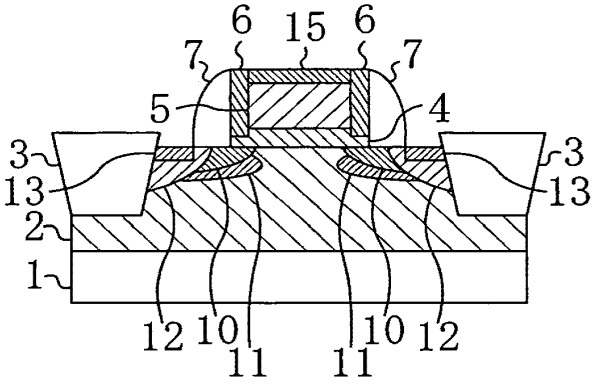


FIG. 15C

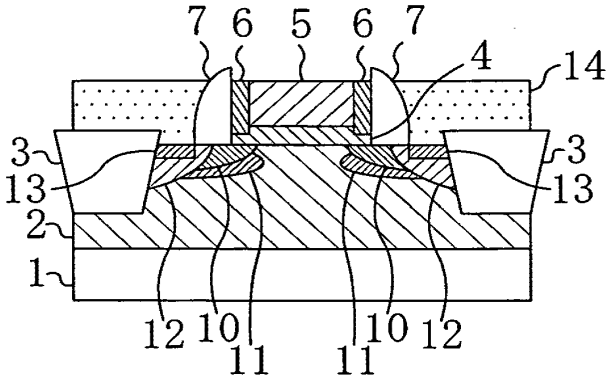


FIG. 15B

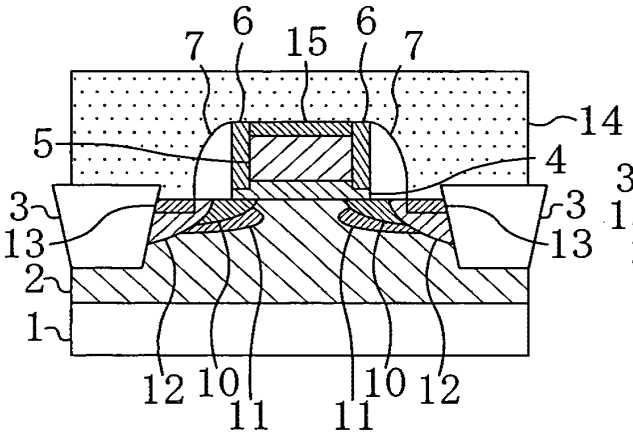


FIG. 15D

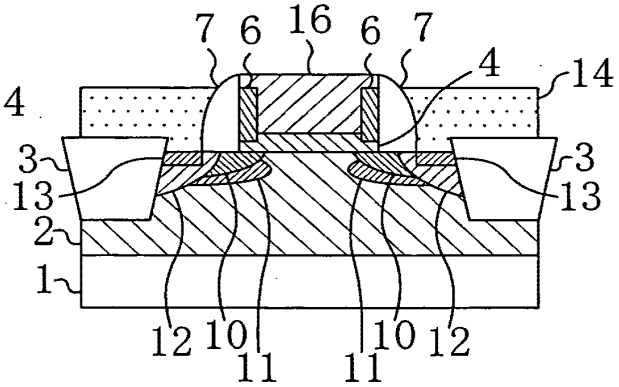


FIG. 16A
PRIOR ART

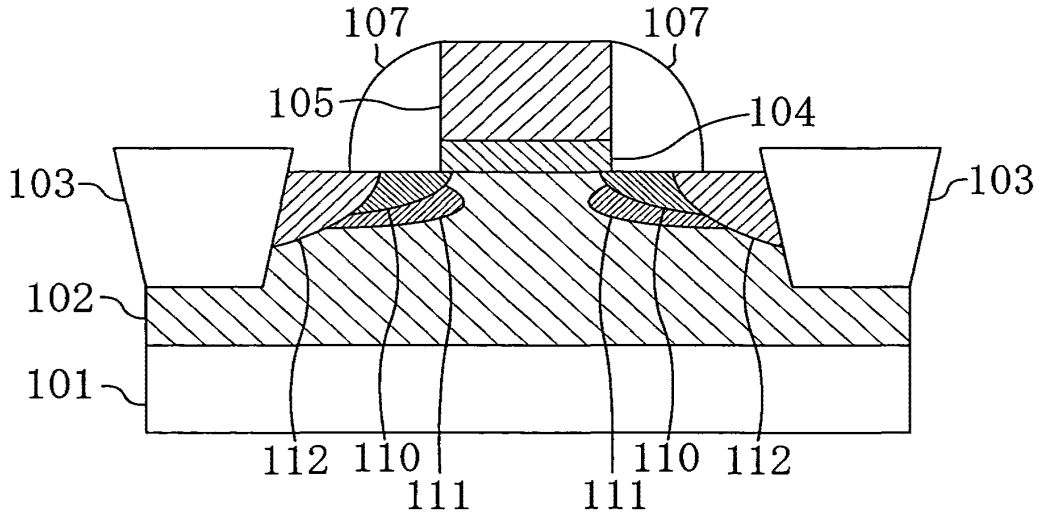
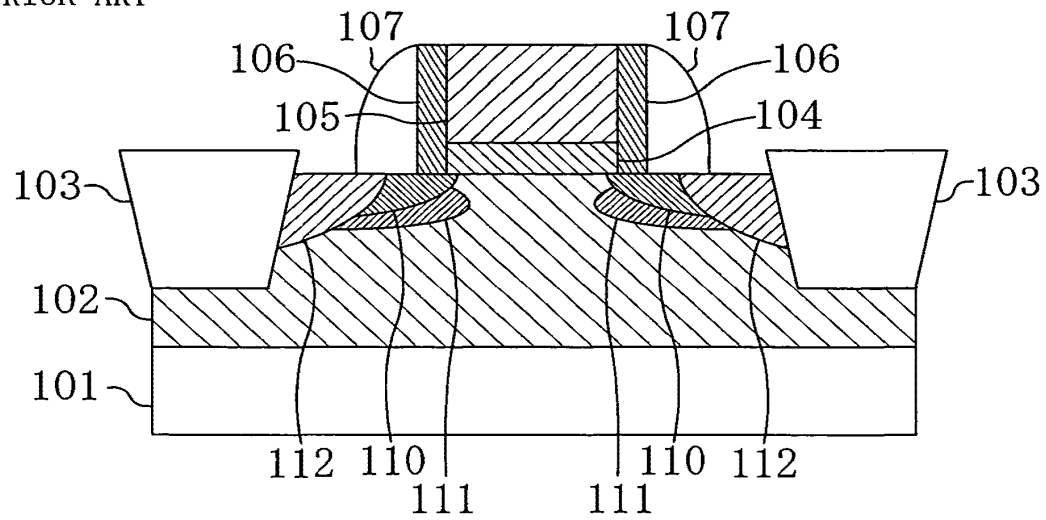


FIG. 16B
PRIOR ART



MEI Form -1.2, (July 1, 2005)

Docket No.

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

☒ Original ☐ Supplemental ☐ Substitute ☐ PCT ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

☒ the attached specification, or

☐ the specification in the Application No._____ filed on_____;
and with amendments filed on_____ (if applicable), or

☐ the specification in International Application No. PCT/_____,
filed _____and as amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
JAPAN	2005-227457	August 5, 2005	Yes

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

Number	(Day/Month/Year Filed)

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

MEI Form -1.2, (July 1, 2005)

Docket No.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

□ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with U.S. Patent and Trademark Office Customer Number identified bellow to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Matsushita Electric Industrial Co., Ltd., and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full Name of Sole or First Inventor	**FIRST NAME** Junji	**LAST NAME** HIRASE	**SIGNATURE** Junji Hirase	**DATE OF SIGNATURE** May. 11, 2006
Residence & Citizenship	**CITY** Osaka	**STATE OR COUNTRY** Japan		**COUNTRY OF CITIZENSHIP** Japan
Post Office Address	**ADDRESS** C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	**CITY**	**STATE OR COUNTRY** Japan	**ZIP CODE** 571-8501

Full Name of Second Inventor	**FIRST NAME** Akio	**LAST NAME** SEBE	**SIGNATURE** Akio Sebe	**DATE OF SIGNATURE** May. 11, 2006
Residence & Citizenship	**CITY** Osaka	**STATE OR COUNTRY** Japan		**COUNTRY OF CITIZENSHIP** Japan
Post Office Address	**ADDRESS** C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	**CITY**	**STATE OR COUNTRY** Japan	**ZIP CODE** 571-8501

MEI Form -1.2, (July 1, 2005)

Docket No.

Full Name of Third Inventor	FIRST NAME Naoki	LAST NAME KOTANI	SIGNATURE Naoki Kotani	DATE OF SIGNATURE May. 11, 2006
Residence & Citizenship	CITY Hyogo	STATE OR COUNTRY Japan		COUNTRY OF CITIZENSHIP Japan
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Fourth Inventor	FIRST NAME Gen	LAST NAME OKAZAKI	SIGNATURE Gen Okazaki	DATE OF SIGNATURE May 11. 2006
Residence & Citizenship	CITY Hyogo	STATE OR COUNTRY Japan		COUNTRY OF CITIZENSHIP Japan
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Fifth Inventor	FIRST NAME Kazuhiko	LAST NAME AIDA	SIGNATURE Kazuhiko Aida	DATE OF SIGNATURE May. 18, 2006
Residence & Citizenship	CITY Chiba	STATE OR COUNTRY Japan		COUNTRY OF CITIZENSHIP Japan
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Sixth Inventor	FIRST NAME Shinji	LAST NAME TAKEOKA	SIGNATURE Shinji TAKEOKA	DATE OF SIGNATURE May 11. 2006
Residence & Citizenship	CITY Osaka	STATE OR COUNTRY Japan		COUNTRY OF CITIZENSHIP Japan
Post Office Address	ADDRESS C/O Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka	CITY	STATE OR COUNTRY Japan	ZIP CODE 571-8501

Full Name of Seventh Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY	STATE OR COUNTRY		COUNTRY OF CITIZENSHIP
Post Office Address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

(If there are more than seven inventors, please add a copy of this page for identification and signature for the additional inventors)

The above application may be more particularly identified as follows:

U.S. Application No. _____ Filing Date _____

Applicant Reference Number P42042-01 Attorney Docket No. _____

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

7/26/2006 FFANAIA2 00000014 500417 11491260

1	FC:1011	300.00 DA
02	FC:1111	500.00 DA
03	FC:1311	200.00 DA

PTO-1556
(5/87)

U.S. Government Printing Office: 2002 — 469-267/60033

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number: 11491-260

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	150.00		N/A	300.00
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	$250		N/A	$500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	$100		N/A	$200
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	* —	X$ 25 =		OR	X$50 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* —	X100 =			X200 =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			+180=			+360=	
			TOTAL			TOTAL	1000

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI-TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI-TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)	OR	RATE ($)	ADDI-TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X$ 25 =		OR	X$50 =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X100 =		OR	X200 =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					+180=		OR	+360=	
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docket No.: 071971-0620 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Junji HIRASE, et al.	:	Confirmation Number: Not Yet Assigned
Application No.: Not Yet Assigned	:	Group Art Unit: Not Yet Assigned
Filed: July 24, 2006	:	Examiner: Not Yet Assigned

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of each non-English language reference, if any, is discussed in the present specification.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:MaM
Facsimile: 202.756.8087
Date: July 24, 2006

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 071971-0620	SERIAL NO. Not Yet Assigned
	APPLICANT Junji HIRASE, et al.	
	FILING DATE July 24, 2006	GROUP Not Yet Assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		WATANABE, Ken, Partial English Translation of "HfSiON-CMOS technology for achieving high performance and high reliability," SEMI FORUM Japan, 2005, IT System & ULSI Technology,	
		HORI, Takashi, "1/4-μm LATID (LArge-Tilt-angle Implanted Drain) TECHNOLOGY FOR 3.3-V OPERATION", CH2637-7/89/0000-0777 1989 IEEE, IEDM 89-777-780-IEDM 89	
		SAYAMA, et al., H.,, "80nm CMOSFET Technology Using Double Offset-Implanted Source/Drain Extension and Low Temperature SiN Process", IEDM 2000, IEDM 00-239-242-IEDM 00	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Docket No.: 071971-0620 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Junji HIRASE, et al.	:	Confirmation Number: Not Yet Assigned
Application No.: Not Yet Assigned	:	Group Art Unit: Not Yet Assigned
Filed: July 24, 2006	:	Examiner: Not Yet Assigned

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

CLAIM OF PRIORITY AND
TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. 119, Applicant hereby claims the priority of: Japanese Patent Application Number 2005-227457, filing date August 5, 2005 cited in the Declaration of the present application. Certified copy is submitted herewith.

Respectfully submitted,

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【書類名】特許請求の範囲
【請求項１】
基板の活性領域上に形成された高誘電率ゲート絶縁膜と、
前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、
前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記絶縁性サイドウォールの下側領域の少なくとも一部分の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。
【請求項２】
請求項１に記載の半導体装置において、
前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第１の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。
【請求項３】
請求項２に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側には形成されていないことを特徴とする半導体装置。
【請求項４】
請求項２に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さと同等であることを特徴とする半導体装置。
【請求項５】
請求項２に記載の半導体装置において、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さよりも小さいことを特徴とする半導体装置。
【請求項６】
請求項１に記載の半導体装置において、
前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、
前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、
前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さと同等であり、
前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さいことを特徴とする半導体装置。

【請求項７】
請求項１～６のいずれか１項に記載の半導体装置において、
前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていることを特徴とする半導体装置。
【請求項８】
請求項１～７のいずれか１項に記載の半導体装置において、
前記基板と前記高誘電率ゲート絶縁膜との間にバッファー絶縁膜が設けられていることを特徴とする半導体装置。
【請求項９】
請求項８に記載の半導体装置において、
前記バッファー絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であることを特徴とする半導体装置。
【請求項１０】
請求項１～９のいずれか１項に記載の半導体装置において、
前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であることを特徴とする半導体装置。
【請求項１１】
基板の活性領域上に高誘電率ゲート絶縁膜を形成する工程（ａ）と、
前記高誘電率ゲート絶縁膜上にゲート電極を形成する工程（ｂ）と、
前記工程（ｂ）の後に、前記ゲート電極の外側に位置する前記高誘電率ゲート絶縁膜をエッチングして薄膜化する工程（ｃ）と、
前記工程（ｃ）の後に、前記ゲート電極の側面に絶縁性サイドウォールを形成する工程（ｄ）とを備えていることを特徴とする半導体装置の製造方法。
【請求項１２】
請求項１１に記載の半導体装置の製造方法において、
前記工程（ｄ）の後に、前記絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程を備えていることを特徴とする半導体装置の製造方法。
【請求項１３】
請求項１１に記載の半導体装置の製造方法において、
前記絶縁性サイドウォールは第１の絶縁性サイドウォールと第２の絶縁性サイドウォールとからなり、
前記工程（ｄ）は、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを形成する工程（ｄ１）と、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して前記第２の絶縁性サイドウォールを形成する工程（ｄ２）とを含むことを特徴とする半導体装置の製造方法。
【請求項１４】
請求項１３に記載の半導体装置の製造方法において、
前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１５】
請求項１３に記載の半導体装置の製造方法において、
前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜をエッチングしてさらに薄膜化する工程を備え、
前記工程（ｄ２）よりも後に、前記第２の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１６】
請求項１２、１４又は１５のいずれか１項に記載の半導体装置の製造方法において、
前記高誘電率ゲート絶縁膜の除去は、ウェットエッチングを用いて選択的に行われるこ

とを特徴とする半導体装置の製造方法。
【請求項１７】
請求項１１～１６のいずれか１項に記載の半導体装置の製造方法において、
前記工程（ｂ）は、前記ゲート電極の上面を覆う保護膜を形成する工程を含み、
前記工程（ｄ）よりも後に、前記絶縁性サイドウォールの外側に位置する前記活性領域の表面をシリサイド化した後、前記保護膜を除去し、その後、前記ゲート電極をフルシリサイド化する工程をさらに備えていることを特徴とする半導体装置の製造方法。
【請求項１８】
請求項１１～１７のいずれか１項に記載の半導体装置の製造方法において、
前記工程（ａ）よりも前に、前記活性領域上にバッファー絶縁膜を形成する工程をさらに備え、
前記工程（ａ）では前記活性領域上に前記バッファー絶縁膜を介して前記高誘電率ゲート絶縁膜を形成することを特徴とする半導体装置の製造方法。

【書類名】明細書
【発明の名称】半導体装置及びその製造方法
【技術分野】
【０００１】
本発明は、半導体装置及びその製造方法、具体的にはＭＩＳＦＥＴ（metal insulator semiconductor field effect transistor ）の構造及び製造方法に関し、主にＭＩＳＦＥＴの駆動力及び信頼性を向上させる技術に関する。
【背景技術】
【０００２】
近年、半導体集積回路装置の高集積化、高機能化及び高速化に伴ない、スケーリング則に従ってエクステンション（Extension ）の接合深さを浅くすると同時に、ＭＩＳＦＥＴのゲート絶縁膜として比誘電率が４程度のＳｉO_2 系の絶縁膜に代えてＨｆ系酸化物又はＡｌ系酸化物等の比誘電率が１０以上の高誘電率膜を用いようとしている。
【０００３】
図１６（ａ）及び（ｂ）はそれぞれ従来の高誘電率ゲート絶縁膜を使ったＭＩＳＦＥＴの構造を示す断面図である（非特許文献１）。
【０００４】
図１６（ａ）に示すように、基板１０１の活性領域であるウェル１０２におけるＳＴＩ（shallow trench isolation）１０３によって囲まれた領域の上に高誘電率ゲート絶縁膜１０４を介してゲート電極１０５が形成されている。ゲート電極１０５の側面には絶縁性のサイドウォール１０７が形成されている。ウェル１０２におけるサイドウォール１０７の下側にはエクステンション領域１１０が形成されていると共にウェル１０２におけるエクステンション領域１１０の下側にはポケット領域１１１が形成されている。ウェル１０２におけるゲート電極１０５から見てエクステンション領域１１０及びポケット領域１１１の外側にはソース・ドレイン領域１１２が形成されている。
【０００５】
図１６（ｂ）に示す構造が図１６（ａ）に示す構造と異なっている点は、ゲート電極１０５の側面にサイドウォール１０７が絶縁性のオフセットサイドウォール１０６を介して形成されていることである。これにより、ゲート電極１０５とエクステンション領域１１０とのオーバーラップ量の最適化を容易に図ることができる。
【非特許文献１】渡辺健、「高性能・高信頼性を実現する HfSiON-CMOS技術」、Semi. Forum Japan 2005
【非特許文献２】T.Hori、IEDM Tech. Dig. 、1989年、p.777
【非特許文献３】H.Sayama他、IEDM Tech. Dig. 、2000年、p.239
【発明の開示】
【発明が解決しようとする課題】
【０００６】
しかしながら、従来の高誘電率ゲート絶縁膜を使ったＭＩＳＦＥＴの構造においては、高誘電率ゲート絶縁膜の側端部がサイドウォールに直接接しているため、例えばシリコン酸化膜等からなるサイドウォールの形成時に高誘電率ゲート絶縁膜の側端部の組成がＳｉO_2 に近づく等の問題が生じる。その結果、ゲート電極端部において高誘電率ゲート絶縁膜の誘電率低下や絶縁性低下が引き起こされ、それによってデバイス特性やゲート絶縁膜の信頼性が悪化してしまう。
【０００７】
前記に鑑み、本発明は、高誘電率ゲート絶縁膜を劣化させることなくＭＩＳＦＥＴの特性を向上させることを目的とする。
【課題を解決するための手段】
【０００８】
前記の目的を達成するために、本願発明者らは、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させ、それにより高誘電率ゲート絶縁膜の側端部とサイドウォールとの接

触を防止したＭＩＳＦＥＴ構造及びその製造方法を想到するに至った。ところで、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させた場合には、ゲート・ドレイン間の容量が上昇して回路速度に悪影響が生じる。また、この場合、エクステンション注入やＬＤＤ（lightly doped drain ）注入を実施する際に、高誘電率膜を介在させた状態でイオン注入を行う必要がある。その際、以下の理由によって注入加速エネルギーが高くなるため、注入不純物の深さ方向への拡がりが大きくなってしまい、言い換えると、エクステンションやＬＤＤの接合位置が深くなってしまい、その結果、所望のデバイス特性が得られなくなるという問題が生じる。

【０００９】

理由１）ゲート絶縁膜として高誘電膜を用いる場合、膜厚を薄くしなくても所望の誘電率が得られるため、膜厚が厚く設定される。

【００１０】

理由２）高誘電率膜は重金属を含んでいるため、注入イオン種のＲｐ（Projection Range）が小さくなる。

【００１１】

そこで、本願発明者らは、サイドウォールの下側に高誘電率ゲート絶縁膜を残存させ且つサイドウォール下側の高誘電率ゲート絶縁膜をゲート電極下側の高誘電率ゲート絶縁膜よりも薄く形成したＭＩＳＦＥＴ構造及びその製造方法を想到するに至った。

【００１２】

具体的には、本発明に係る半導体装置は、基板の活性領域上に形成された高誘電率ゲート絶縁膜と、前記高誘電率ゲート絶縁膜上に形成されたゲート電極と、前記ゲート電極の側面に形成された絶縁性サイドウォールとを備え、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記絶縁性サイドウォールの下側領域の少なくとも一部分の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さい。

【００１３】

本発明の半導体装置において、前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第１の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さくてもよい。

【００１４】

前記絶縁性サイドウォールが前記第１の絶縁性サイドウォールと前記第２の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記第２の絶縁性サイドウォールの下側には形成されていなくてもよい。

【００１５】

前記絶縁性サイドウォールが前記第１の絶縁性サイドウォールと前記第２の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さと同等であってもよい。

【００１６】

前記絶縁性サイドウォールが前記第１の絶縁性サイドウォールと前記第２の絶縁性サイドウォールとからなる場合、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート

絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さよりも小さくてもよい。

【００１７】
本発明の半導体装置において、前記絶縁性サイドウォールは、前記ゲート電極の側面に形成された第１の絶縁性サイドウォールと、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して形成された第２の絶縁性サイドウォールとからなり、前記高誘電率ゲート絶縁膜は前記ゲート電極の下側から前記第２の絶縁性サイドウォールの下側まで連続的に形成されており、前記高誘電率ゲート絶縁膜における前記第１の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さと同等であり、前記高誘電率ゲート絶縁膜における前記第２の絶縁性サイドウォールの下側領域の厚さは、前記高誘電率ゲート絶縁膜における前記ゲート電極の下側領域の厚さよりも小さくてもよい。

【００１８】
本発明の半導体装置において、前記高誘電率ゲート絶縁膜の側端部にノッチが設けられていてもよい。

【００１９】
本発明の半導体装置において、前記基板と前記高誘電率ゲート絶縁膜との間にバッファー絶縁膜が設けられていてもよい。この場合、前記バッファー絶縁膜はシリコン酸化膜又はシリコン酸窒化膜であってもよい。

【００２０】
本発明の半導体装置において、前記ゲート電極は、全領域がシリサイド化されたフルシリサイドゲート電極であってもよい。

【００２１】
本発明に係る半導体装置の製造方法は、基板の活性領域上に高誘電率ゲート絶縁膜を形成する工程（ａ）と、前記高誘電率ゲート絶縁膜上にゲート電極を形成する工程（ｂ）と、前記工程（ｂ）の後に、前記ゲート電極の外側に位置する前記高誘電率ゲート絶縁膜をエッチングして薄膜化する工程（ｃ）と、前記工程（ｃ）の後に、前記ゲート電極の側面に絶縁性サイドウォールを形成する工程（ｄ）とを備えている。

【００２２】
本発明の半導体装置の製造方法において、前記工程（ｄ）の後に、前記絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程を備えていてもよい。

【００２３】
本発明の半導体装置の製造方法において、前記絶縁性サイドウォールは第１の絶縁性サイドウォールと第２の絶縁性サイドウォールとからなり、前記工程（ｄ）は、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを形成する工程（ｄ１）と、前記ゲート電極の側面に前記第１の絶縁性サイドウォールを介して前記第２の絶縁性サイドウォールを形成する工程（ｄ２）とを含んでいてもよい。

【００２４】
前記工程（ｄ）が前記工程（ｄ１）と前記工程（ｄ２）とを含む場合、前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていてもよい。

【００２５】
前記工程（ｄ）が前記工程（ｄ１）と前記工程（ｄ２）とを含む場合、前記工程（ｄ１）と前記工程（ｄ２）との間に、前記第１の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜をエッチングしてさらに薄膜化する工程を備え、前記工程（ｄ２）よりも後に、前記第２の絶縁性サイドウォールの外側に位置する前記高誘電率ゲート絶縁膜を除去する工程をさらに備えていてもよい。

【００２６】
本発明の半導体装置の製造方法において、前記高誘電率ゲート絶縁膜の除去は、ウェットエッチングを用いて選択的に行われてもよい。

【００２７】
本発明の半導体装置の製造方法において、前記工程（ｂ）は、前記ゲート電極の上面を覆う保護膜を形成する工程を含み、前記工程（ｄ）よりも後に、前記絶縁性サイドウォールの外側に位置する前記活性領域の表面をシリサイド化した後、前記保護膜を除去し、その後、前記ゲート電極をフルシリサイド化する工程をさらに備えていてもよい。
【００２８】
本発明の半導体装置の製造方法において、前記工程（ａ）よりも前に、前記活性領域上にバッファー絶縁膜を形成する工程をさらに備え、前記工程（ａ）では前記活性領域上に前記バッファー絶縁膜を介して前記高誘電率ゲート絶縁膜を形成してもよい。
【発明の効果】
【００２９】
本発明によると、ゲート電極の下側からサイドウォールの下側まで高誘電率ゲート絶縁膜が連続的に形成されているため、言い換えると、ゲート端部での高誘電率ゲート絶縁膜の連続性が維持されているため、高誘電率ゲート絶縁膜の側端部がサイドウォール膜と直接接することに起因する、ゲート端部での高誘電率ゲート絶縁膜の誘電率低下及び絶縁性低下を抑制することができる。また、サイドウォール下側の高誘電率ゲート絶縁膜をゲート電極下側の高誘電率ゲート絶縁膜よりも薄く形成しているため、ゲート・ドレイン間の容量の上昇を抑制して回路速度への悪影響を低減することができる。さらに、エクステンション注入やＬＤＤ注入を実施する際に介在する高誘電率膜の膜厚が薄いため、注入加速エネルギーの増大を抑制できる。従って、エクステンションやＬＤＤにおいて浅い接合を容易に形成できるので、デバイス特性の向上を図りやすい。
【発明を実施するための最良の形態】
【００３０】
（第１の実施形態）
以下、本発明の第１の実施形態に係る半導体装置について、図面を参照しながら説明する。図１は、第１の実施形態に係る半導体装置（具体的にはシングルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。
【００３１】
図１に示すように、例えばシリコンからなる基板１に形成されたｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に高誘電率ゲート絶縁膜４Ａを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のサイドウォール７が形成されている。ｐ型ウェル２におけるサイドウォール７の下側にはｎ型エクステンション領域１０が形成されていると共にｐ型ウェル２におけるｎ型エクステンション領域１０の下側にはｐ型ポケット領域１１が形成されている。ｐ型ウェル２におけるゲート電極５から見てｎ型エクステンション領域１０及びｐ型ポケット領域１１の外側にはｎ型ソース・ドレイン領域１２が形成されている。
【００３２】
本実施形態の第１の特徴は、ゲート電極５の下側のみならずサイドウォール７の下側にも高誘電率ゲート絶縁膜４Ａが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ａはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。
【００３３】
また、本実施形態の第２の特徴は、高誘電率ゲート絶縁膜４Ａにおけるサイドウォール７の下側領域の厚さは、高誘電率ゲート絶縁膜４Ａにおけるゲート電極５の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜４Ａは凸型状に形成されている。
【００３４】
本実施形態によると、高誘電率ゲート絶縁膜４Ａの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ａの連続性が維持されている。

このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ａの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００３５】

また、本実施形態によると、サイドウォール７の下側に高誘電率ゲート絶縁膜４Ａが存在することによって、ゲート電極５端部近傍ではゲート電極５とｎ型エクステンション領域１０との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバラップ効果を得ることができる（非特許文献２）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【００３６】

一方、本実施形態においては、サイドウォール７の下側に高誘電率ゲート絶縁膜４Ａが存在することにより、特に、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇が発生し、それによって回路速度の低下がもたらされる可能性がある。しかし、前述のように、本実施形態においては、サイドウォール７下側の高誘電率ゲート絶縁膜４Ａをゲート電極５下側の高誘電率ゲート絶縁膜４Ａよりも薄く形成しているため、ゲート・ドレイン間の容量の上昇ひいては回路速度への悪影響を抑制することができる。

【００３７】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【００３８】

（第１の実施形態の変形例）

以下、本発明の第１の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図６は、第１の実施形態の変形例に係る半導体装置（具体的にはシングルサイドウォール型のｎ型ＭＩＳＦＥＴ）の構造を示す断面図である。

【００３９】

本変形例が第１の実施形態と異なっている点は、図６に示すように、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４Ａの一部つまり高誘電率ゲート絶縁膜４Ａの側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。

【００４０】

本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【００４１】

（第２の実施形態）

以下、本発明の第２の実施形態に係る半導体装置について、図面を参照しながら説明する。尚、第１の実施形態がシングルサイドウォール型のＭＩＳＦＥＴを対象としていたのに対して、第２の実施形態は、ゲート電極とエクステンション領域との間のオーバラップ量の最適化を図りやすいダブルサイドウォール型のＭＩＳＦＥＴ（非特許文献３）を対象とする。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。

【００４２】

図２は、第２の実施形態に係る半導体装置の構造を示す断面図である。図２に示すように、例えばシリコンからなる基板１に形成されたｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に高誘電率ゲート絶縁膜４Ｂを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のオフセットサイドウォール６を介して絶縁性のサイドウォール７が形成されている。ｐ型ウェル２におけるオフセットサイドウォール６及びサイドウォール７のそれぞれの下側にはｎ型エクステンション領域１０が形成されていると共にｐ型ウェル２におけるｎ型エクステンション領域１０の下側にはｐ型ポケット領域１１が形成されている。ｐ型ウェル２におけるゲート電極５から見てｎ型エクステンション領域１０及びｐ型ポケット領域１１の外側にはｎ型ソース・ドレイン領域１２が形成さ

れている。

【００４３】

本実施形態の第１の特徴は、ゲート電極５の下側のみならずオフセットサイドウォール６の下側にも高誘電率ゲート絶縁膜４Ｂが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｂはゲート電極５の下側からオフセットサイドウォール６の下側まで連続的に形成されている。

【００４４】

また、本実施形態の第２の特徴は、高誘電率ゲート絶縁膜４Ｂにおけるオフセットサイドウォール６の下側領域の厚さは、高誘電率ゲート絶縁膜４Ｂにおけるゲート電極５の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜４Ｂは凸型状に形成されている。

【００４５】

本実施形態によると、高誘電率ゲート絶縁膜４Ｂの側端部がオフセットサイドウォール６と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｂの連続性が維持されている。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｂの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００４６】

また、本実施形態によると、オフセットサイドウォール６の下側に高誘電率ゲート絶縁膜４Ｂが存在することによって、ゲート電極５端部近傍ではゲート電極５とｎ型エクステンション領域１０との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバラップ効果を得ることができる（非特許文献２）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【００４７】

さらに、本実施形態によると、サイドウォール７の下側には高誘電率ゲート絶縁膜４Ｂが存在しないため、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇をさらに小さく抑えることができるので、寄生容量上昇とそれに伴う回路速度への悪影響を最小限に抑制することができる。

【００４８】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【００４９】

（第２の実施形態の第１変形例）

以下、本発明の第２の実施形態の第１変形例に係る半導体装置について、図面を参照しながら説明する。図７は、第２の実施形態の第１変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００５０】

本変形例が第２の実施形態と異なっている点は、図７に示すように、オフセットサイドウォール６の側端部の下側に位置する高誘電率ゲート絶縁膜４Ｂの一部つまり高誘電率ゲート絶縁膜４Ｂの側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。

【００５１】

本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【００５２】

（第２の実施形態の第２変形例）

以下、本発明の第２の実施形態の第２変形例に係る半導体装置について、図面を参照しながら説明する。図３は、第２の実施形態の第２変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００５３】

本変形例が第２の実施形態と異なっている点は、ゲート電極５の下側及びオフセットサイドウォール６の下側のみならずサイドウォール７の下側にも高誘電率ゲート絶縁膜４Ｃが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｃはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。

【００５４】

尚、本変形例において、サイドウォール７の下側の高誘電率ゲート絶縁膜４Ｃの膜厚は、オフセットサイドウォール６の下側の高誘電率ゲート絶縁膜４Ｃの膜厚と同じである。すなわち、高誘電率ゲート絶縁膜４Ｃは凸型状に形成されている。

【００５５】

本変形例によると、高誘電率ゲート絶縁膜４Ｃがゲート電極５の下側からサイドウォール７の下側まで連続的に形成されているため、オフセットサイドウォール６の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜４Ｃの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｃの連続性を維持することができる。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｃの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００５６】

但し、本変形例においては、第１の実施形態と同様にサイドウォール７の下側に高誘電率ゲート絶縁膜４Ｃが存在することにより、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇が発生する可能性がある。しかし、前述のように、本変形例においては、サイドウォール７下側の高誘電率ゲート絶縁膜４Ｃをゲート電極５下側の高誘電率ゲート絶縁膜４Ｃよりも薄く形成しているため、寄生容量上昇及びそれに伴う回路速度への悪影響を抑制することができる。

【００５７】

（第２の実施形態の第３変形例）

以下、本発明の第２の実施形態の第３変形例に係る半導体装置について、図面を参照しながら説明する。図４は、第２の実施形態の第３変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００５８】

本変形例が第２の実施形態と異なっている第１の点は、ゲート電極５の下側及びオフセットサイドウォール６の下側のみならずサイドウォール７の下側にも高誘電率ゲート絶縁膜４Ｄが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｄはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。

【００５９】

本変形例が第２の実施形態と異なっている第２の点は、オフセットサイドウォール６の下側の高誘電率ゲート絶縁膜４Ｄの膜厚が、ゲート電極５の下側の高誘電率ゲート絶縁膜４Ｄの膜厚と同等であることである。尚、サイドウォール７の下側の高誘電率ゲート絶縁膜４Ｄの膜厚は、ゲート電極５の下側の高誘電率ゲート絶縁膜４Ｄの膜厚よりも小さい。すなわち、高誘電率ゲート絶縁膜４Ｄは凸型状に形成されている。

【００６０】

本変形例によると、高誘電率ゲート絶縁膜４Ｄがゲート電極５の下側からサイドウォール７の下側まで連続的に形成されているため、オフセットサイドウォール６の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜４Ｄの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｄの連続性を維持することができる。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｄの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００６１】

但し、本変形例においては、第１の実施形態と同様にサイドウォール７の下側に高誘電率ゲート絶縁膜４Ｄが存在することにより、ゲート電極５とｎ型ソース・ドレイン領域１

２との間の容量の上昇が発生する可能性がある。しかし、前述のように、本変形例においては、サイドウォール７下側の高誘電率ゲート絶縁膜４Ｄをゲート電極５下側の高誘電率ゲート絶縁膜４Ｄよりも薄く形成しているため、寄生容量上昇及びそれに伴う回路速度への悪影響を抑制することができる。

【００６２】

（第３の実施形態）

以下、本発明の第３の実施形態に係る半導体装置について、図面を参照しながら説明する。尚、第１の実施形態がシングルサイドウォール型のＭＩＳＦＥＴを対象としていたのに対して、第３の実施形態は、ゲート電極とエクステンション領域との間のオーバラップ量の最適化を図りやすいダブルサイドウォール型のＭＩＳＦＥＴ（非特許文献３）を対象とする。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。

【００６３】

図５は、第３の実施形態に係る半導体装置の構造を示す断面図である。図５に示すように、例えばシリコンからなる基板１に形成されたｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に高誘電率ゲート絶縁膜４Ｅを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のオフセットサイドウォール６を介して絶縁性のサイドウォール７が形成されている。ｐ型ウェル２におけるオフセットサイドウォール６及びサイドウォール７のそれぞれの下側にはｎ型エクステンション領域１０が形成されていると共にｐ型ウェル２におけるｎ型エクステンション領域１０の下側にはｐ型ポケット領域１１が形成されている。ｐ型ウェル２におけるゲート電極５から見てｎ型エクステンション領域１０及びｐ型ポケット領域１１の外側にはｎ型ソース・ドレイン領域１２が形成されている。

【００６４】

本実施形態の第１の特徴は、ゲート電極５の下側のみならずオフセットサイドウォール６及びサイドウォール７のそれぞれの下側にも高誘電率ゲート絶縁膜４Ｅが残存していることである。すなわち、高誘電率ゲート絶縁膜４Ｅはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。

【００６５】

また、本実施形態の第２の特徴は、高誘電率ゲート絶縁膜４Ｅにおけるオフセットサイドウォール６の下側領域の厚さが、高誘電率ゲート絶縁膜４Ｅにおけるゲート電極５の下側領域の厚さよりも小さく、且つ高誘電率ゲート絶縁膜４Ｅにおけるサイドウォール７の下側領域の厚さが、高誘電率ゲート絶縁膜４Ｅにおけるオフセットサイドウォール６の下側領域の厚さよりも小さいことである。すなわち、高誘電率ゲート絶縁膜４Ｅは２重凸型状に形成されている。

【００６６】

本実施形態によると、高誘電率ゲート絶縁膜４Ｅがゲート電極５の下側からサイドウォール７の下側まで連続的に形成されているため、オフセットサイドウォール６の幅が非常に薄い場合にも、高誘電率ゲート絶縁膜４Ｅの側端部がサイドウォール７と接することなく、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｅの連続性を維持することができる。このため、ゲート電極５端部での高誘電率ゲート絶縁膜４Ｅの誘電率低下及び絶縁性低下を抑制することができるので、デバイス特性の低下やゲート絶縁膜信頼性の劣化を防止することができる。

【００６７】

また、本実施形態によると、オフセットサイドウォール６の下側に高誘電率ゲート絶縁膜４Ｅが存在することによって、ゲート電極５端部近傍ではゲート電極５とｎ型エクステンション領域１０との間の容量結合が強まり、その結果、高いゲート・ドレイン間オーバラップ効果を得ることができる（非特許文献２）。従って、デバイス特性の向上及びホットキャリア信頼性の向上が同時に図れる。

【００６８】

一方、本実施形態においては、第１の実施形態と同様にサイドウォール７の下側に高誘電率ゲート絶縁膜４Ｅが存在することにより、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇が発生し、その結果、回路速度の低下がもたらされる可能性がある。しかし、前述のように、本実施形態においては、オフセットサイドウォール６下側で高誘電率ゲート絶縁膜４Ｅの膜厚を一旦薄くし且つサイドウォール７下側で高誘電率ゲート絶縁膜４Ｅの膜厚をさらに薄くしているため、寄生容量上昇及びそれに伴う回路速度への悪影響を非常に低く抑制することができる。

【００６９】

以上に説明したように、本実施形態によると、互いにトレードオフの関係にあるデバイス特性・回路特性とゲート絶縁膜信頼性とを共に大きく向上させることができる。

【００７０】

（第３の実施形態の変形例）

以下、本発明の第３の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図８は、第３の実施形態の変形例に係る半導体装置（具体的にはダブルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００７１】

本変形例が第３の実施形態と異なっている点は、図８に示すように、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４Ｅの一部、つまり高誘電率ゲート絶縁膜４Ｅの側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。

【００７２】

本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【００７３】

（第４の実施形態）

以下、本発明の第４の実施形態に係る半導体装置について、図面を参照しながら説明する。図９は、第４の実施形態に係る半導体装置（具体的にはシングルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。尚、本実施形態ではｎ型ＭＩＳＦＥＴを用いて説明するが、本発明をｐ型ＭＩＳＦＥＴに適用した場合にも同様の効果を得ることができる。

【００７４】

本実施形態が第１の実施形態と異なっている点は、図９に示すように、基板１と高誘電率ゲート絶縁膜４Ａとの間に、例えばシリコン酸化膜又はシリコン酸窒化膜等がバッファー絶縁膜２５として設けられていることである。

【００７５】

本実施形態によると、第１の実施形態の効果に加えて、基板・ゲート絶縁膜界面を正常に保つことができるという効果が得られる。すなわち、基板１上にバッファー絶縁膜２５を介して高誘電率ゲート絶縁膜４Ａを形成することによって、基板１上に高誘電率ゲート絶縁膜４Ａを直接形成した場合と比べて、基板・ゲート絶縁膜界面の劣化を防止することができる。

【００７６】

尚、本実施形態において、第１の実施形態の高誘電率ゲート絶縁膜４Ａと基板１との間にバッファー絶縁膜２５を設けた。しかし、これに代えて、第２の実施形態の高誘電率ゲート絶縁膜４Ｂ、第２の実施形態の第２変形例の高誘電率ゲート絶縁膜４Ｃ、第２の実施形態の第３変形例の高誘電率ゲート絶縁膜４Ｄ又は第３の実施形態の高誘電率ゲート絶縁膜４Ｅと基板１との間にバッファー絶縁膜２５を設けても、本実施形態と同様の効果が得られる。また、高誘電率ゲート絶縁膜４Ａ～４Ｅと基板１との間にバッファー絶縁膜２５を設ける代わりに、ゲート電極５と高誘電率ゲート絶縁膜４Ａ～４Ｅとの間にバッファー絶縁膜を設けてもよい。この構成によれば、高誘電率ゲート絶縁膜４Ａ～４Ｅ上にゲート電極５を直接形成した場合と比べて、ゲート電極・ゲート絶縁膜界面の劣化を防止するこ

とができる。或いは、高誘電率ゲート絶縁膜４Ａ～４Ｅと基板１との間にバッファー絶縁膜２５を設けると共にゲート電極５と高誘電率ゲート絶縁膜４Ａ～４Ｅとの間にバッファー絶縁膜を設けてもよい。この構成によれば、基板・ゲート絶縁膜界面及びゲート絶縁膜・ゲート電極界面の両方の劣化を防止することができる。

【００７７】

（第４の実施形態の変形例）

以下、本発明の第４の実施形態の変形例に係る半導体装置について、図面を参照しながら説明する。図１０は、第４の実施形態の変形例に係る半導体装置（具体的にはシングルサイドウォール型のＭＩＳＦＥＴ）の構造を示す断面図である。

【００７８】

本変形例が第４の実施形態と異なっている点は、図１０に示すように、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４Ａ及びバッファー絶縁膜２５の積層絶縁膜の一部、つまり当該積層絶縁膜の側端部をノッチ状に取り除くことにより、ノッチ２０が設けられていることである。

【００７９】

本変形例によると、ゲート電極５とｎ型ソース・ドレイン領域１２との間の容量の上昇に起因する回路速度への悪影響をより一層抑制することができる。

【００８０】

尚、本変形例において、第１の実施形態の高誘電率ゲート絶縁膜４Ａとバッファー絶縁膜２５との積層絶縁膜の側端部にノッチ２０を設けた。しかし、これに代えて、第２の実施形態の高誘電率ゲート絶縁膜４Ｂ、第２の実施形態の第２変形例の高誘電率ゲート絶縁膜４Ｃ、第２の実施形態の第３変形例の高誘電率ゲート絶縁膜４Ｄ又は第３の実施形態の高誘電率ゲート絶縁膜４Ｅのいずれかとバッファー絶縁膜２５との積層絶縁膜の側端部にノッチを設けても、本変形例と同様の効果が得られる。このとき、高誘電率ゲート絶縁膜４Ａ～４Ｅと基板１との間にバッファー絶縁膜２５を設けると共に、ゲート電極５と高誘電率ゲート絶縁膜４Ａ～４Ｅとの間にもバッファー絶縁膜を設けてもよい。

【００８１】

（第５の実施形態）

以下、本発明の第５の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１１（ａ）～（ｆ）は、第５の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【００８２】

まず、図１１（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢ（ボロン）を注入エネルギー３００ｋｅＶ、ドーズ量$1\times10^{13}\,cm^{-2}$の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量$1\times10^{13}\,cm^{-2}$）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量$5\times10^{12}\,cm^{-2}$）を行う。

【００８３】

次に、図１１（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【００８４】

次に、図１１（ｃ）に示すように、高誘電率ゲート絶縁膜４上に例えば膜厚１００ｎｍ程度のゲート電極材料膜５Ａを形成する。

【００８５】

次に、ゲート電極材料膜５Ａ上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜５Ａに対して

エッチングを行って、図１１（ｄ）に示すように、ゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。続いて、ゲート電極５をマスクとして基板１に対して、例えばＡｓ（ヒ素）を注入エネルギー２ｋｅＶ、ドーズ量1×10^{15} cm^{-2}の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量3×10^{13} cm^{-2}の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。ここで、ｐ型ポケット領域１１を形成した後、ｎ型エクステンション領域１０を形成してもよい。

【００８６】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１１（ｅ）に示すように、ゲート電極５の側面に絶縁性のサイドウォール７を形成する。

【００８７】

次に、ゲート電極５及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量5×10^{15} cm^{-2}の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡ（rapid thermal annealing ）を行い、注入不純物を活性化する。これにより、図１１（ｆ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【００８８】

以上に説明した本実施形態の製造方法によると、第１の実施形態のＭＩＳＦＥＴ構造（図１参照）を比較的簡単に実現することができる。

【００８９】

ところで、高誘電率ゲート絶縁膜４は重金属を含んでいるため、高誘電率ゲート絶縁膜４を通過する注入イオンのＲｐ（Projection Range ）は小さくなりやすい。従って、図１１（ｄ）に示す工程において、ｎ型エクステンション領域１０又はｐ型ポケット領域１１を形成するために、ゲート電極５の外側において高誘電率ゲート絶縁膜４に覆われた基板１に対してイオン注入する際には、加速エネルギーを大きくする必要がある。しかし、本実施形態ではゲート電極５の外側の高誘電率ゲート絶縁膜４が薄膜化されているため、加速エネルギーの増大を抑制できるので、ｎ型エクステンション領域１０において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。

【００９０】

尚、本実施形態において、サイドウォール７の形成後に、サイドウォール７の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去してもよい。このとき、ウェットエッチングを用いる場合には、サイドウォール７の側端部の下側に位置する高誘電率ゲート絶縁膜４の一部、つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、第１の実施形態の変形例のＭＩＳＦＥＴ構造（図６参照）を簡単に実現することができる。

【００９１】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化する（但し基板１の表面が露出しないように）ことが好ましい。

【００９２】

（第６の実施形態）

以下、本発明の第６の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１２（ａ）～（ｇ）は、第６

の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【００９３】

まず、図１２（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢを注入エネルギー３００ｋｅＶ、ドーズ量1×10^{13} cm^{-2}の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量1×10^{13} cm^{-2}）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量5×10^{12} cm^{-2}）を行う。

【００９４】

次に、図１２（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【００９５】

次に、図１２（ｃ）に示すように、高誘電率ゲート絶縁膜４上に例えば膜厚１００ｎｍ程度のゲート電極材料膜５Ａを形成する。

【００９６】

次に、ゲート電極材料膜５Ａ上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜５Ａに対してエッチングを行って、図１２（ｄ）に示すように、ゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側の高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。

【００９７】

次に、基板１の上に全面に亘って膜厚１０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１２（ｅ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を形成する。その後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去する。続いて、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＡｓを注入エネルギー２ｋｅＶ、ドーズ量1×10^{15} cm^{-2}の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量3×10^{13} cm^{-2}の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。

【００９８】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１２（ｆ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を介して絶縁性のサイドウォール７を形成する。

【００９９】

次に、ゲート電極５、オフセットサイドウォール６及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量5×10^{15} cm^{-2}の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡを行い、注入不純物を活性化する。これにより、図１２（ｇ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【０１００】

以上に説明した本実施形態の製造方法によると、第２の実施形態のＭＩＳＦＥＴ構造（図２参照）を比較的簡単に実現することができる。

【０１０１】

尚、本実施形態において、オフセットサイドウォール６の形成後に、オフセットサイド

ウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチングによって除去する際に、オフセットサイドウォール６の側端部の下側に位置する高誘電率ゲート絶縁膜４の一部、つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、第２の実施形態の第１変形例のＭＩＳＦＥＴ構造（図７参照）を簡単に実現することができる。

【０１０２】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化する（但し基板１の表面が露出しないように）ことが好ましい。

【０１０３】

また、本実施形態において、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を除去し、その後、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った。しかし、これに代えて、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側に薄膜化した高誘電率ゲート絶縁膜４を残存させた状態でｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行ってもよい。このようにしても、本実施形態ではオフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４が薄膜化されているため、加速エネルギーの増大を抑制できるので、ｎ型エクステンション領域１０において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。また、この場合、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を除去し、その後、同一基板上における他のチャネル型又は別の電源系のＭＩＳＦＥＴのエクステンション領域及びポケット領域を形成するためのイオン注入を行ってもよい。

【０１０４】

（第７の実施形態）

以下、本発明の第７の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１３（ａ）～（ｇ）は、第７の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【０１０５】

まず、図１３（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢを注入エネルギー３００ｋｅＶ、ドーズ量1×10^{13} cm^{-2}の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量1×10^{13} cm^{-2}）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量5×10^{12} cm^{-2}）を行う。

【０１０６】

次に、図１３（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【０１０７】

次に、図１３（ｃ）に示すように、高誘電率ゲート絶縁膜４上に例えば膜厚１００ｎｍ程度のゲート電極材料膜５Ａを形成する。

【０１０８】

次に、ゲート電極材料膜５Ａ上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてゲート電極材料膜５Ａに対して

エッチングを行って、図１３（ｄ）に示すように、ゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側の高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。

【０１０９】

次に、基板１の上に全面に亘って膜厚５ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１３（ｅ）に示すように、ゲート電極５の側面に絶縁性のオフセットサイドウォール６を形成する。その後、ゲート電極５及びオフセットサイドウォール６により被覆されていない高誘電率ゲート絶縁膜４をさらに膜厚１ｎｍ程度除去する。これにより、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を残存膜厚１ｎｍ程度まで薄くすることができる。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＡｓを注入エネルギー２ｋｅＶ、ドーズ量1×10^{15}ｃｍ$^{-2}$の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量3×10^{13}ｃｍ$^{-2}$の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。

【０１１０】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１３（ｆ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を介して絶縁性のサイドウォール７を形成する。

【０１１１】

次に、ゲート電極５、オフセットサイドウォール６及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量5×10^{15}ｃｍ$^{-2}$の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡを行い、注入不純物を活性化する。これにより、図１３（ｇ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【０１１２】

以上に説明した本実施形態の製造方法によると、第３の実施形態のＭＩＳＦＥＴ構造（図５参照）を比較的簡単に実現することができる。

【０１１３】

また、本実施形態においては、オフセットサイドウォール６下側で高誘電率ゲート絶縁膜４Ｅの膜厚を一旦薄くし且つオフセットサイドウォール６の外側の高誘電率ゲート絶縁膜４Ｅの膜厚をさらに薄くしている。このため、ゲート電極５及びオフセットサイドウォール６をマスクとして、ｎ型エクステンション領域１０を形成するためのイオン注入を行う際にも、加速エネルギーの増大を最小限に抑制できるので、ｎ型エクステンション領域１０においてさらに浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。

【０１１４】

尚、本実施形態において、サイドウォール７の形成後に、サイドウォール７の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去してもよい。また、この際に、サイドウォール７端部の高誘電率ゲート絶縁膜４つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてもよい。このようにすると、第３の実施形態の変形例のＭＩＳＦＥＴ構造（図８参照）を簡単に実現することができる。

【０１１５】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は、オフセットサイドウォール６の下側においてもサイドウォール７の下側においても特に限定されるものではない。しかし、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化することが好ま

しい。

【０１１６】

（第８の実施形態）

以下、本発明の第８の実施形態に係る半導体装置の製造方法について、ｎ型ＭＩＳＦＥＴの製造方法を例として、図面を参照しながら説明する。図１４（ａ）～（ｇ）及び図１５（ａ）～（ｄ）は、第８の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。

【０１１７】

まず、図１４（ａ）に示すように、例えばシリコンからなる基板上１に、素子分離領域となるＳＴＩ３を選択的に形成した後、基板１に対して、例えばＢを注入エネルギー３００ｋｅＶ、ドーズ量1×10^{13}ｃｍ$^{-2}$の条件でイオン注入する。これにより、活性領域となるｐ型ウェル２が形成される。続いて、パンチスルーストッパ形成用のイオン注入（注入イオン：Ｂ、注入エネルギー１５０ｋｅＶ、ドーズ量1×10^{13}ｃｍ$^{-2}$）及びチャネル形成用のイオン注入（注入イオン：Ｂ、注入エネルギー２０ｋｅＶ、ドーズ量5×10^{12}ｃｍ$^{-2}$）を行う。

【０１１８】

次に、図１４（ｂ）に示すように、ｐ型ウェル２におけるＳＴＩ３によって囲まれた活性領域の上に、バッファー絶縁膜として例えば膜厚０．５ｎｍ程度のシリコン酸化膜（図示省略）を形成した後、高誘電率ゲート絶縁膜４として例えば膜厚４ｎｍ程度のＨｆＳｉＯＮ膜（酸化膜換算膜厚は１ｎｍ程度）を堆積する。

【０１１９】

次に、図１４（ｃ）に示すように、高誘電率ゲート絶縁膜４上にゲート電極材料膜５Ａとして例えば膜厚１００ｎｍ程度のポリシリコン膜を形成した後、ゲート電極材料膜５Ａの上にカバー膜（保護膜）１５として例えば膜厚１０ｎｍ程度のシリコン酸化膜を堆積する。

【０１２０】

次に、カバー膜１５上にゲート電極形成領域を覆うレジストパターン（図示省略）を形成した後、当該レジストパターンをマスクとしてカバー膜１５及びゲート電極材料膜５Ａに対して順次エッチングを行って、図１４（ｄ）に示すように、カバー膜１５により上面が覆われたゲート電極５を形成する。その後、ゲート電極５の外側に位置する高誘電率ゲート絶縁膜４を選択的エッチングによって膜厚２ｎｍ程度除去する。これにより、ゲート電極５の外側の高誘電率ゲート絶縁膜４を残存膜厚２ｎｍ程度まで薄くすることができる。

【０１２１】

次に、基板１の上に全面に亘って膜厚１０ｎｍ程度の絶縁膜を堆積した後、当該絶縁膜に対してエッチバックを行って、図１４（ｅ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を形成する。その後、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチング又は選択ドライエッチングによって除去する。続いて、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＡｓを注入エネルギー２ｋｅＶ、ドーズ量1×10^{15}ｃｍ$^{-2}$の条件でイオン注入することにより、ｎ型エクステンション領域１０を形成する。その後、ゲート電極５及びオフセットサイドウォール６をマスクとして基板１に対して、例えばＢを注入エネルギー１０ｋｅＶ、ドーズ量3×10^{13}ｃｍ$^{-2}$の条件でイオン注入することにより、ｐ型ポケット領域１１を形成する。

【０１２２】

次に、基板１の上に全面に亘って膜厚５０ｎｍ程度の絶縁膜（例えばＳｉＮ膜）を堆積した後、当該絶縁膜に対してエッチバックを行って、図１４（ｆ）に示すように、ゲート電極５の側面にオフセットサイドウォール６を介して絶縁性のサイドウォール７を形成する。

【０１２３】

次に、ゲート電極５、オフセットサイドウォール６及びサイドウォール７をマスクとして基板１に対して、例えばＡｓを注入エネルギー１０ｋｅＶ、ドーズ量５×１０^{15}ｃｍ$^{-2}$の条件でイオン注入した後、例えば１０５０℃程度の温度でＳＰＩＫＥ　ＲＴＡを行い、注入不純物を活性化する。これにより、図１４（ｇ）に示すように、ｎ型ソース・ドレイン領域１２が形成される。

【０１２４】

次に、基板１の上に全面に亘って膜厚１０ｎｍ程度の金属膜（例えばＮｉ膜）を堆積した後、ＲＴＡを実施することにより基板１の露出部分と金属膜とを反応させ、それによって、図１５（ａ）に示すように、ｎ型ソース・ドレイン領域１２上にシリサイド層１３を形成する。その後、基板１上に残留する未反応の金属膜を剥離・除去する。

【０１２５】

次に、図１５（ｂ）に示すように、ゲート電極５の上を含む基板１の上に全面に亘って例えば膜厚４００ｎｍ程度の層間絶縁膜１４を堆積する。

【０１２６】

次に、図１５（ｃ）に示すように、例えばＣＭＰ（chemical mechanical polishing ）によって層間絶縁膜１４を、その表面がカバー膜１５の上面と面一になるまで削った後、当該露出したカバー膜１５をエッチングにより除去する。このとき、ＣＭＰ後の層間絶縁膜１４の上部及びオフセットサイドウォール６の上部も除去される。

【０１２７】

次に、基板１の上に全面に亘って膜厚１００ｎｍ程度の金属膜（例えばＮｉ膜）を堆積した後、ＲＴＡを実施することによりゲート電極５の露出部分と金属膜とを反応させ、それによって、図１５（ｄ）に示すように、フルシリサイド化されたゲート電極１６（高誘電率ゲート絶縁膜４上の全領域がシリサイド化されたゲート電極１６）を形成する。

【０１２８】

以上に説明した本実施形態の製造方法によると、ＦＵＳＩ（full silicide ）構造を用いた第２の実施形態のＭＩＳＦＥＴ構造（図２参照）を比較的簡単に実現することができる。

【０１２９】

尚、本実施形態において、オフセットサイドウォール６の形成後に、オフセットサイドウォール６の外側に位置する高誘電率ゲート絶縁膜４を、例えばフッ酸を用いたウェットエッチングによって除去する際に、オフセットサイドウォール６の側端部の下側に位置する高誘電率ゲート絶縁膜４の一部、つまり高誘電率ゲート絶縁膜４の側端部をノッチ状に取り除いてノッチを設けてもよい。このようにすると、ＦＵＳＩ構造を用いた第２の実施形態の第１変形例のＭＩＳＦＥＴ構造（図７参照）を簡単に実現することができる。

【０１３０】

また、本実施形態において、ゲート電極５の外側における高誘電率ゲート絶縁膜４の薄膜化の程度は特に限定されるものではないが、高誘電率ゲート絶縁膜４として例えばＨｆＳｉＯＮ膜を用いる場合、ゲート・ドレイン間の容量の上昇を抑制するためには、ゲート電極５の外側の高誘電率ゲート絶縁膜４を膜厚２ｎｍ程度以下に薄膜化する（但し基板１の表面が露出しないように）ことが好ましい。

【０１３１】

また、本実施形態において、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側の高誘電率ゲート絶縁膜４を除去し、その後、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った。しかし、これに代えて、オフセットサイドウォール６を形成した後、オフセットサイドウォール６の外側に薄膜化した高誘電率ゲート絶縁膜４を残存させた状態でｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行ってもよい。このようにしても、本実施形態ではゲート電極５の外側に位置する高誘電率ゲート絶縁膜４が薄膜化されているため、加速エネルギーの増大を抑制できるので、ｎ型エクステンション領域１０において浅い接合を容易に形成でき、それによりデバイス特性の向上を図りやすい。ま

た、この場合、ｎ型エクステンション領域１０及びｐ型ポケット領域１１を形成するためのイオン注入を行った後、オフセットサイドウォール６外側に位置する高誘電率ゲート絶縁膜４を除去し、その後、同一基板上における他のチャネル型又は別の電源系のＭＩＳＦＥＴのエクステンション領域及びポケット領域を形成するためのイオン注入を行ってもよい。

【０１３２】

また、本実施形態において、ＦＵＳＩ構造を用いた第２の実施形態のＭＩＳＦＥＴ構造を形成したが、これに代えて、第１の実施形態若しくはその変形例、第２の実施形態の各変形例、第３の実施形態若しくはその変形例、又は第４の実施形態若しくはその変形例のＭＩＳＦＥＴ構造をＦＵＳＩ構造を用いて形成してもよい。

【０１３３】

また、第１～第８の実施形態において、サイドウォール７として例えばＳｉＮ膜の１層構造を用いたが、これに代えて、例えば酸化膜（SiO_2 膜）と窒化膜（ＳｉＮ膜）とを組み合わせた２層構造（例えば下層SiO_2 膜と上層ＳｉＮ膜）又は３層構造（例えば下層SiO_2 膜と中層ＳｉＮ膜と上層SiO_2 膜）等を用いてもよい。

【０１３４】

また、第１～第８の実施形態において、ｎ型エクステンション領域１０に代えてＬＤＤを形成してもよい。

【０１３５】

また、第５～第８の実施形態において、ｎ型ＭＩＳＦＥＴに代えてｐ型ＭＩＳＦＥＴを形成してもよい。

【０１３６】

また、第５～第８の実施形態において、ゲート絶縁膜・ゲート電極界面の劣化を防止するために、ゲート電極５と高誘電率ゲート絶縁膜４との間に例えば膜厚０．２ｎｍ程度のバッファー絶縁膜を形成してもよい。

【０１３７】

また、第１～第８の実施形態において、サイドウォール７又はオフセットサイドウォール６の端部下側にノッチ２０が設けられた高誘電率ゲート絶縁膜４の側面形状は、図６、図７、図８又は図１０に示すような半円形状に限定されるものではない。例えば高誘電率ゲート絶縁膜４の側面形状は基板面に対して垂直な形状でもよい。すなわち、高誘電率ゲート絶縁膜４の側面は、サイドウォール７又はオフセットサイドウォール６の側端面からゲート電極５側に所定の距離だけ入り込んだ位置にあってもよい。

【産業上の利用可能性】

【０１３８】

以上に説明したように、本発明は、半導体装置及びその製造方法に関し、特に高誘電率ゲート絶縁膜を有するＭＩＳＦＥＴに適用した場合には、ＭＩＳＦＥＴの駆動力及び信頼性を向上させることができるという効果が得られ、非常に有用である。

【図面の簡単な説明】

【０１３９】

【図１】図１は本発明の第１の実施形態に係る半導体装置の構造を示す断面図である。

【図２】図２は本発明の第２の実施形態に係る半導体装置の構造を示す断面図である。

【図３】図３は本発明の第２の実施形態の第２変形例に係る半導体装置の構造を示す断面図である。

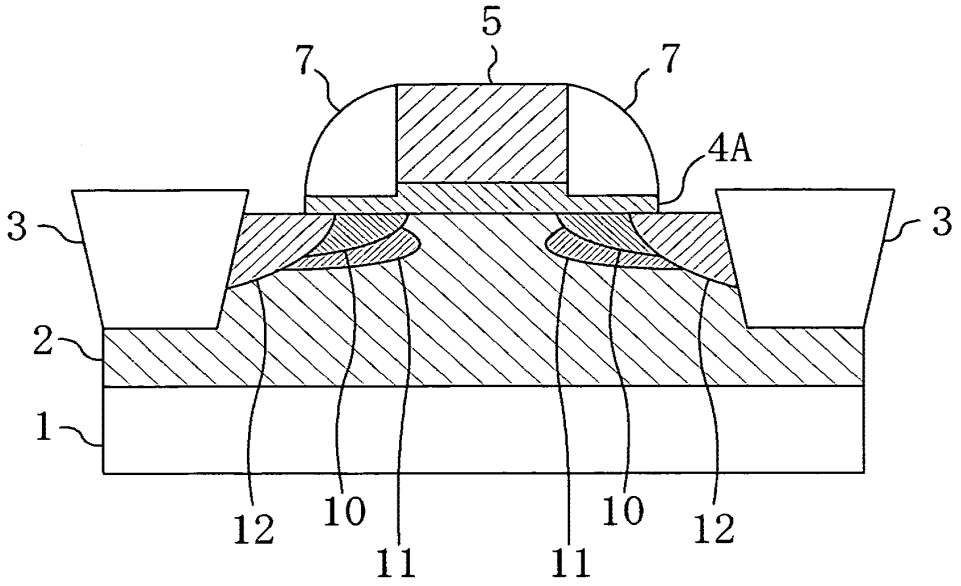
【図４】図４は本発明の第２の実施形態の第３変形例に係る半導体装置の構造を示す断面図である。

【図５】図５は本発明の第３の実施形態に係る半導体装置の構造を示す断面図である。

【図６】図６は本発明の第１の実施形態の変形例に係る半導体装置の構造を示す断面

図である。
【図７】図７は本発明の第２の実施形態の第１変形例に係る半導体装置の構造を示す断面図である。
【図８】図８は本発明の第３の実施形態の変形例に係る半導体装置の構造を示す断面図である。
【図９】図９は本発明の第４の実施形態に係る半導体装置の構造を示す断面図である。
【図１０】図１０は本発明の第４の実施形態の変形例に係る半導体装置の構造を示す断面図である。
【図１１】図１１（ａ）～（ｆ）は本発明の第５の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１２】図１２（ａ）～（ｇ）は本発明の第６の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１３】図１３（ａ）～（ｇ）は本発明の第７の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１４】図１４（ａ）～（ｇ）は本発明の第８の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１５】図１５（ａ）～（ｄ）は本発明の第８の実施形態に係る半導体装置の製造方法の各工程を示す断面図である。
【図１６】図１６（ａ）及び（ｂ）はそれぞれ従来のＭＩＳＦＥＴの構造を示す断面図である。
【符号の説明】
【０１４０】
１　基板
２　ｐ型ウェル
３　ＳＴＩ
４（４Ａ～４Ｅ）　高誘電率ゲート絶縁膜
５Ａ　ゲート電極材料膜
５　ゲート電極
６　オフセットサイドウォール
７　サイドウォール
１０　ｎ型エクステンション領域
１１　ｐ型ポケット領域
１２　ｎ型ソース・ドレイン領域
１３　シリサイド層
１４　層間絶縁膜
１５　カバー膜
１６　フルシリサイド化されたゲート電極
２０　ノッチ
２５　バッファー絶縁膜

【書類名】図面
【図１】



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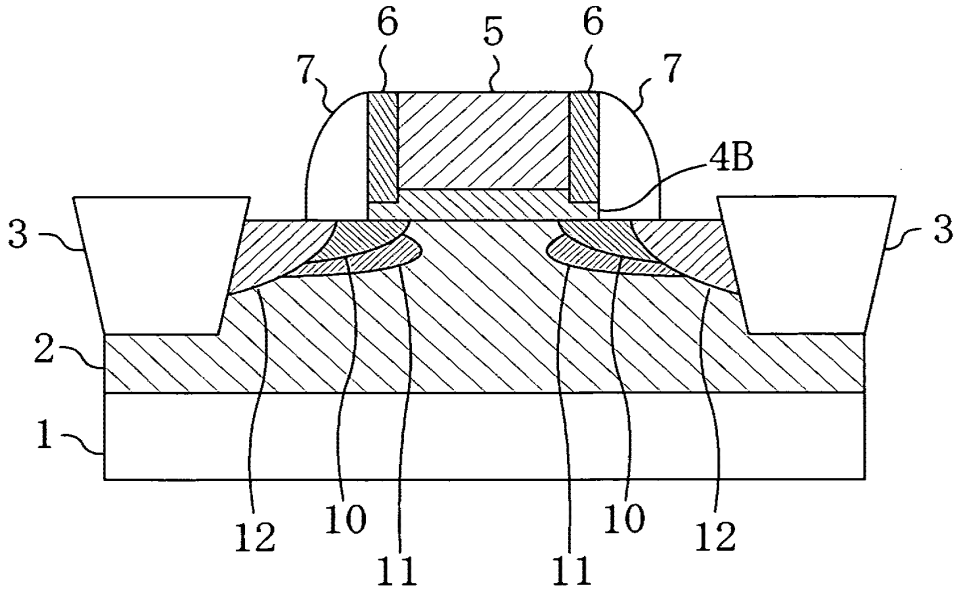

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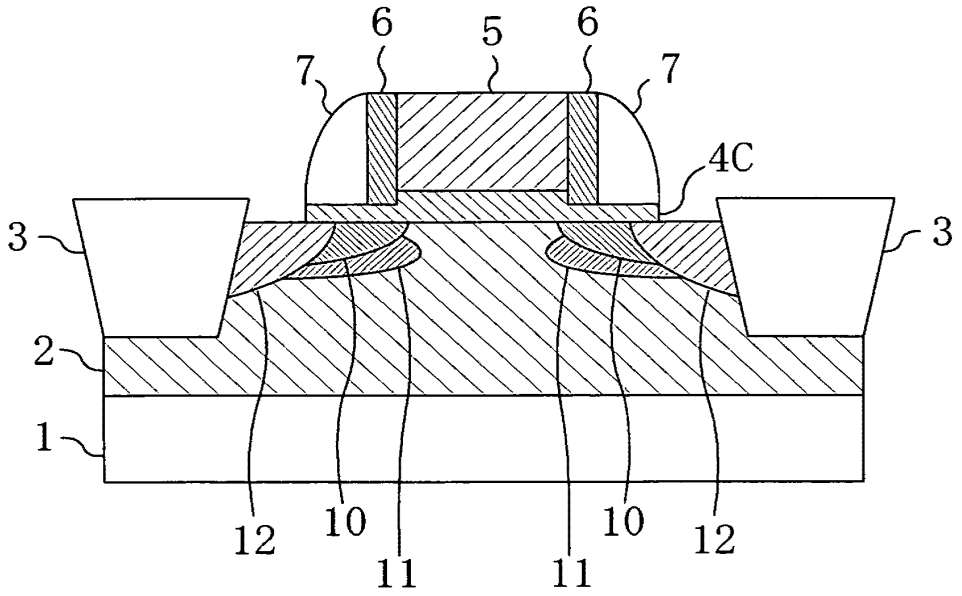

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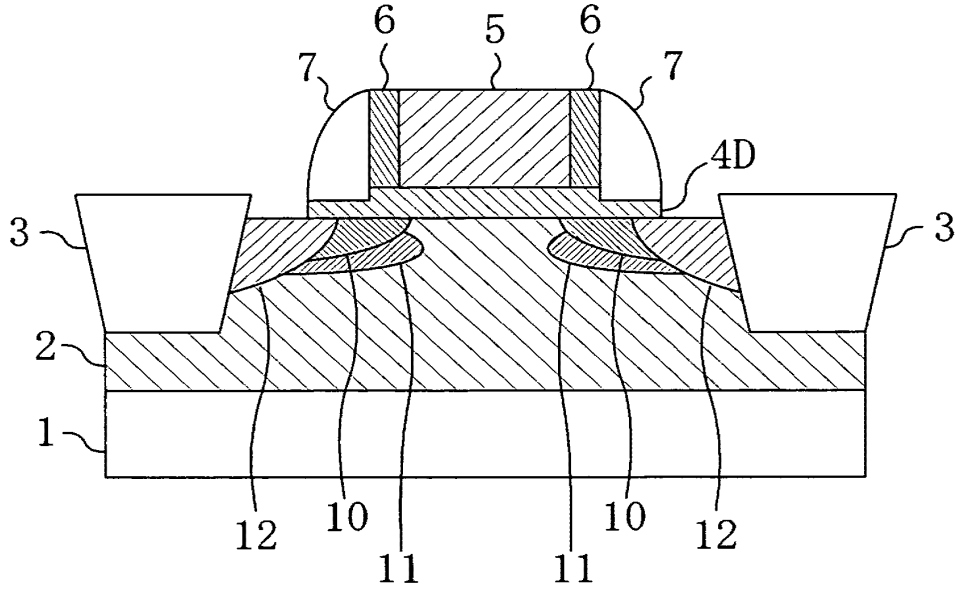

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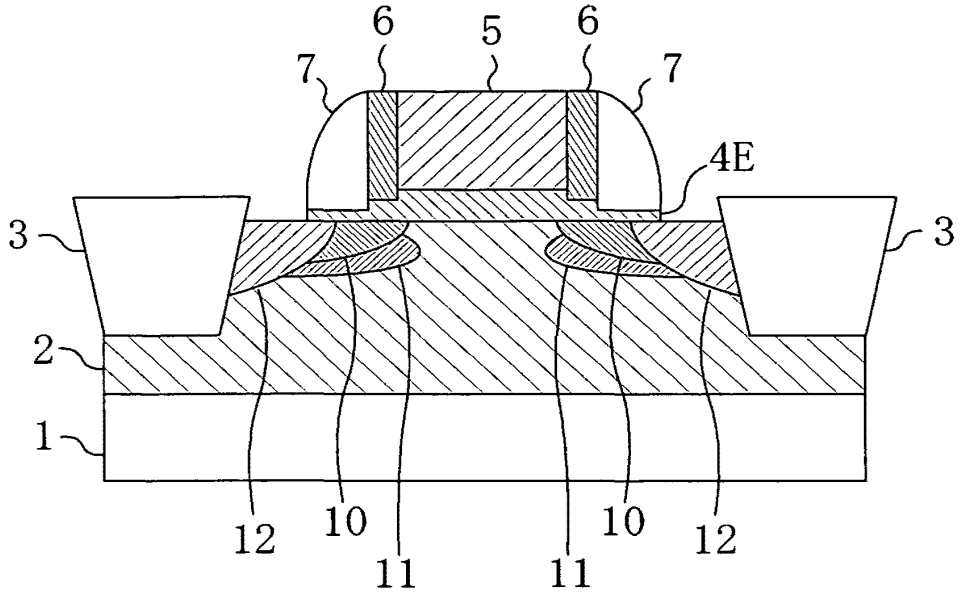

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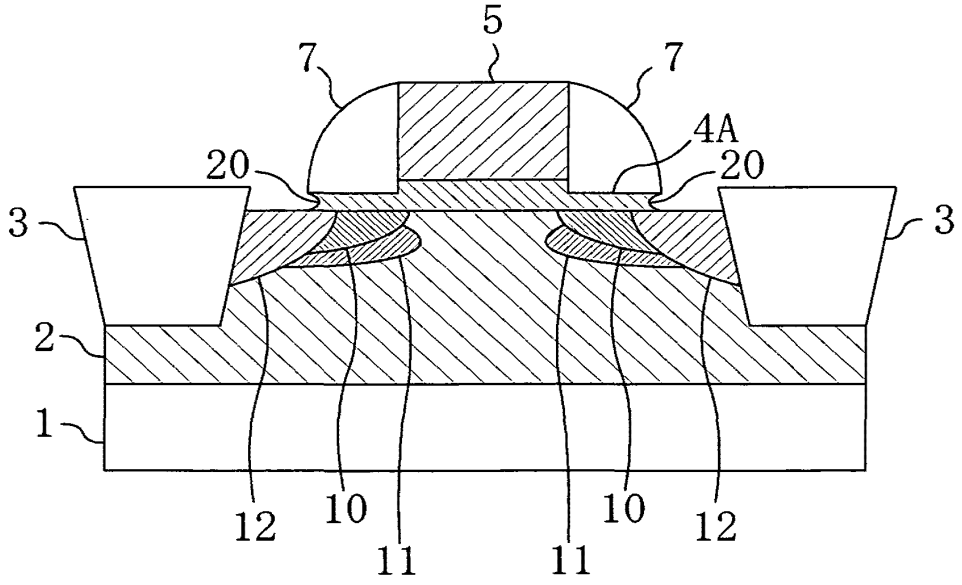

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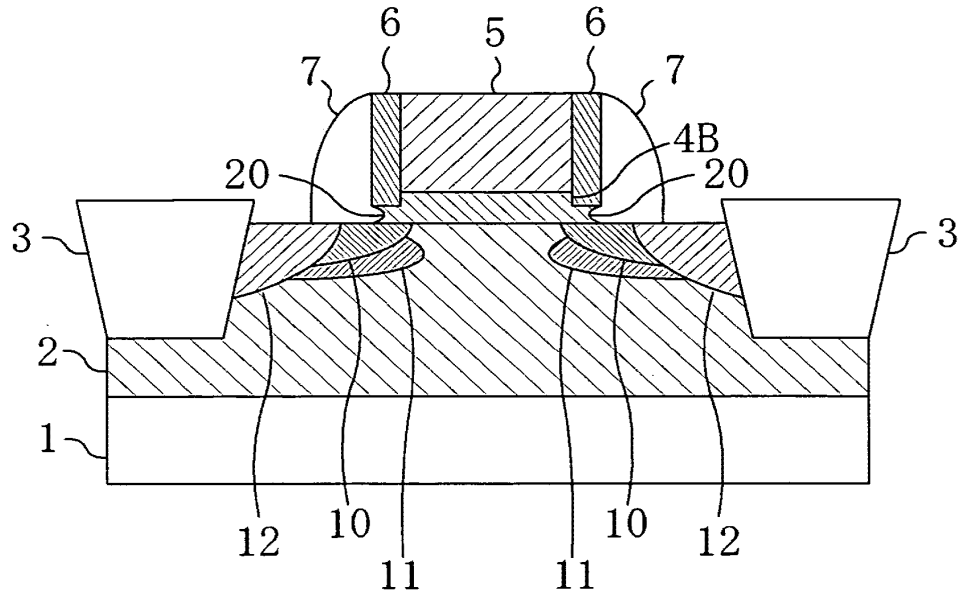
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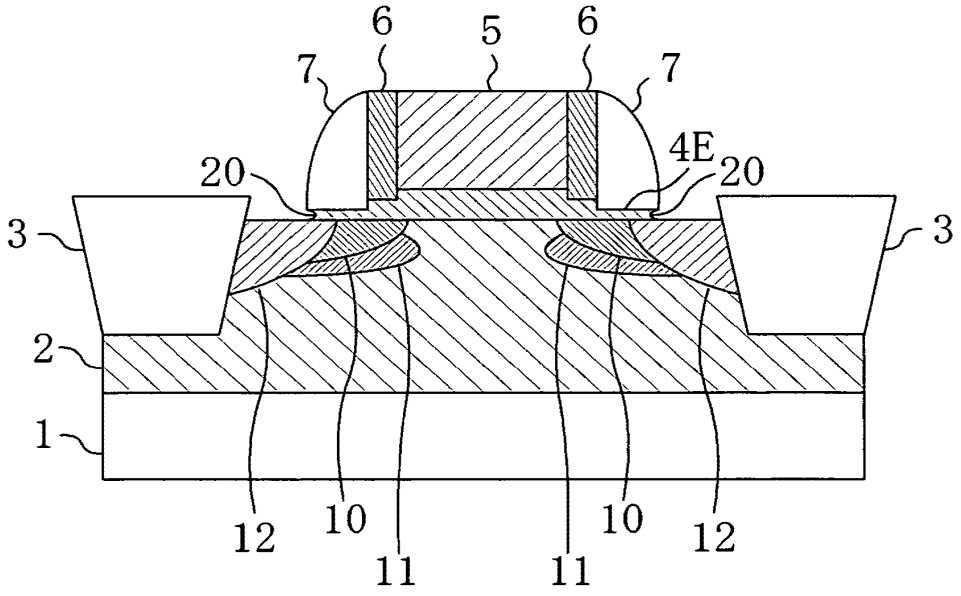
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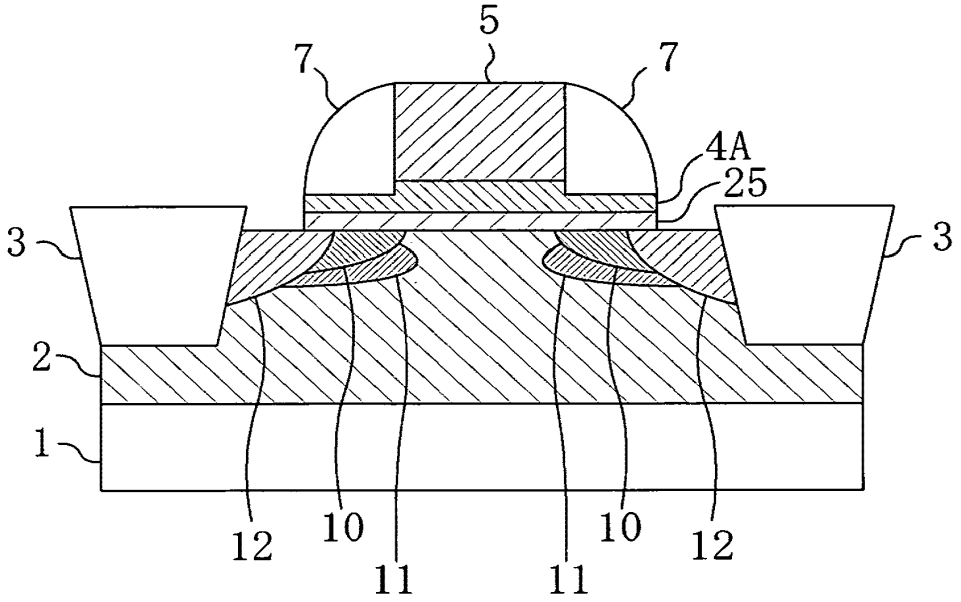
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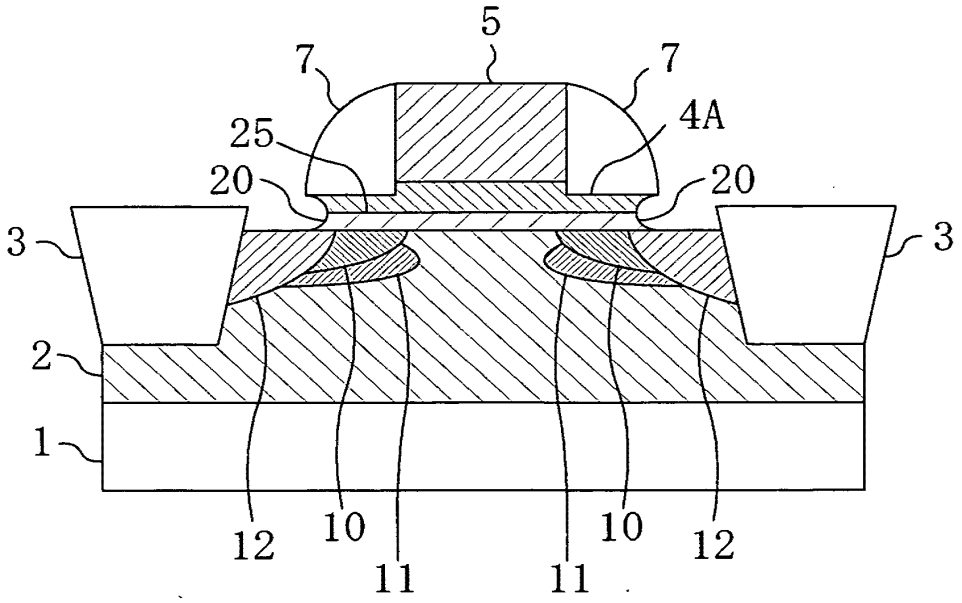
【図１０】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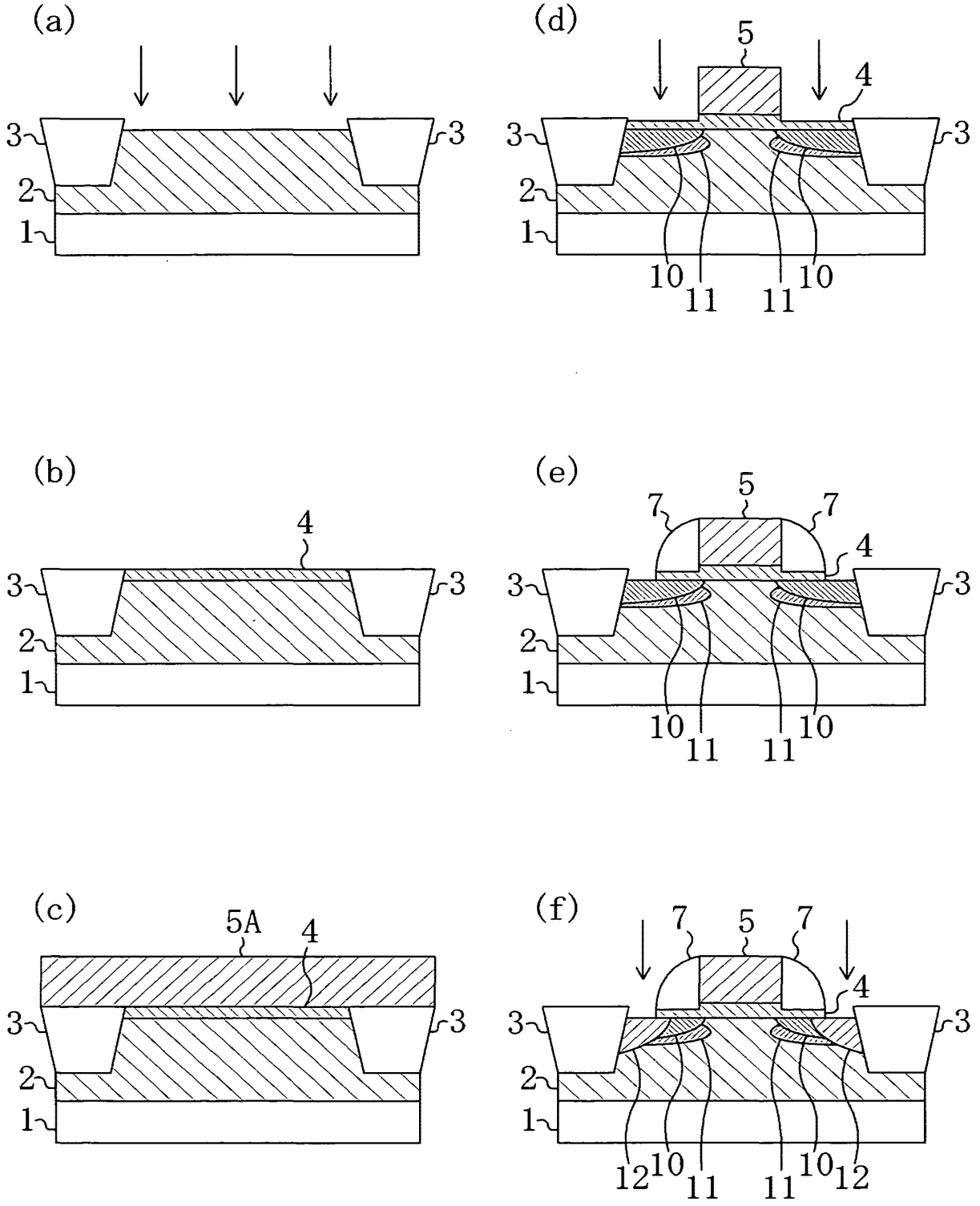
【図１１】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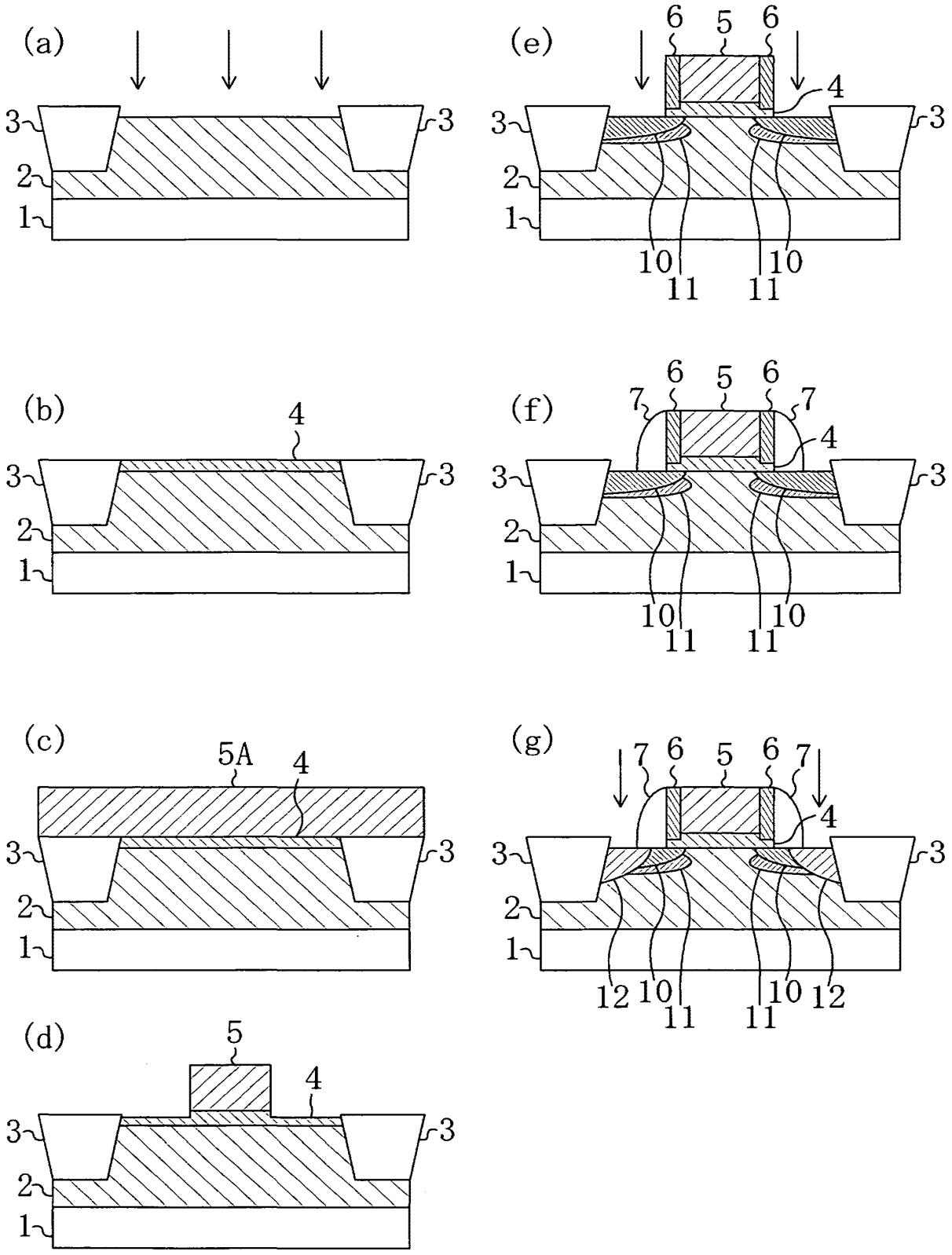
【図１２】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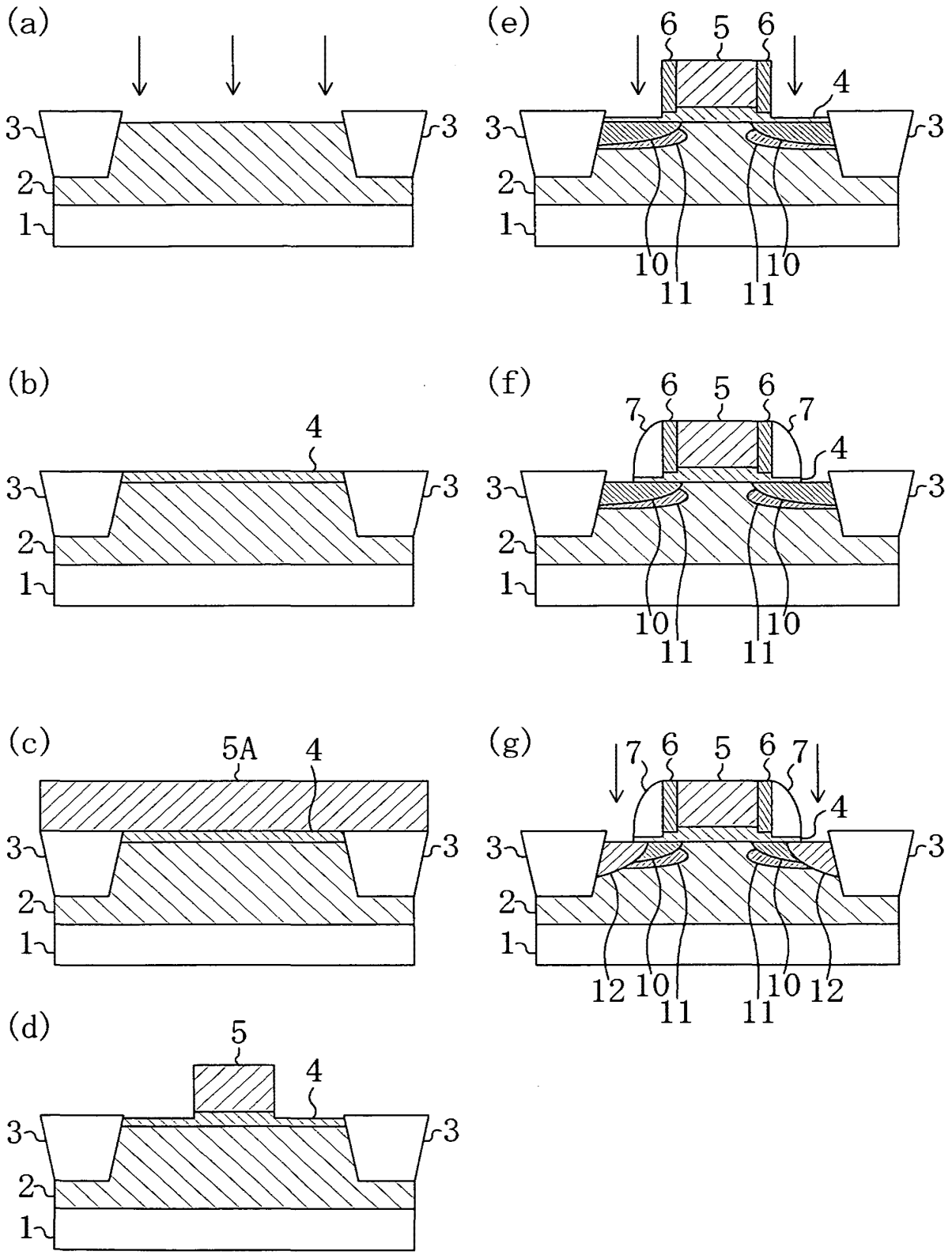
【図１３】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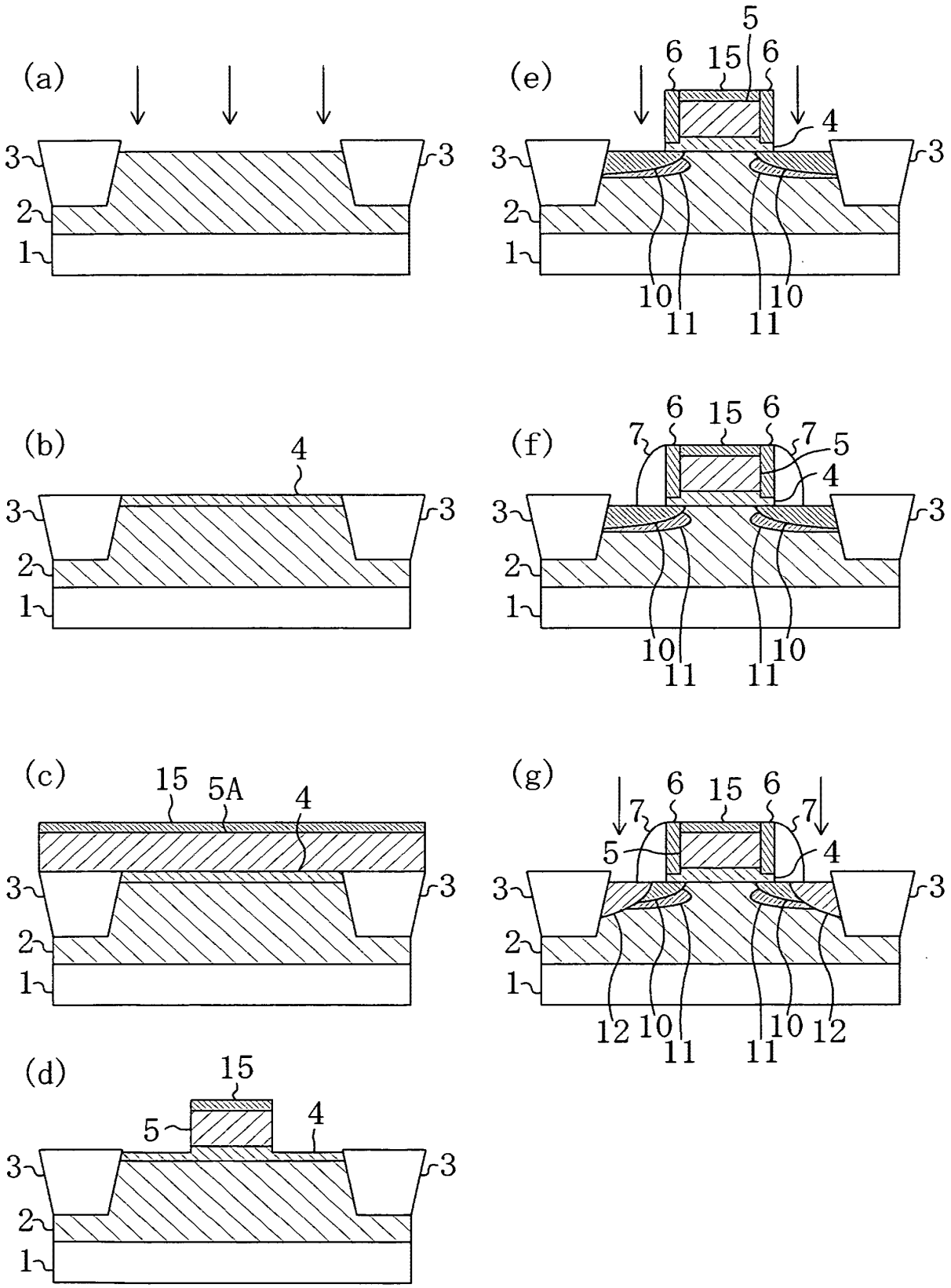
【図１４】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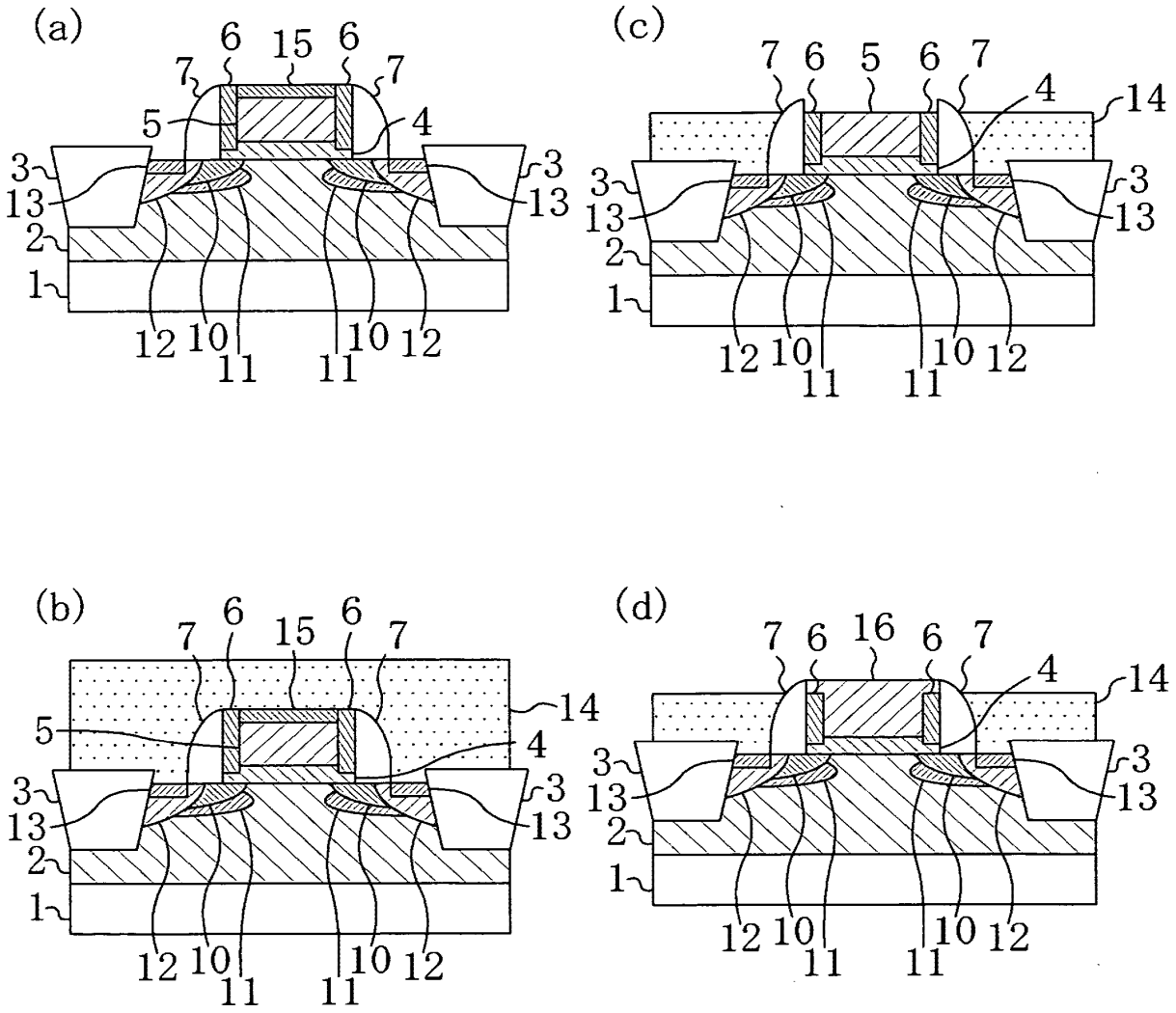
【図１５】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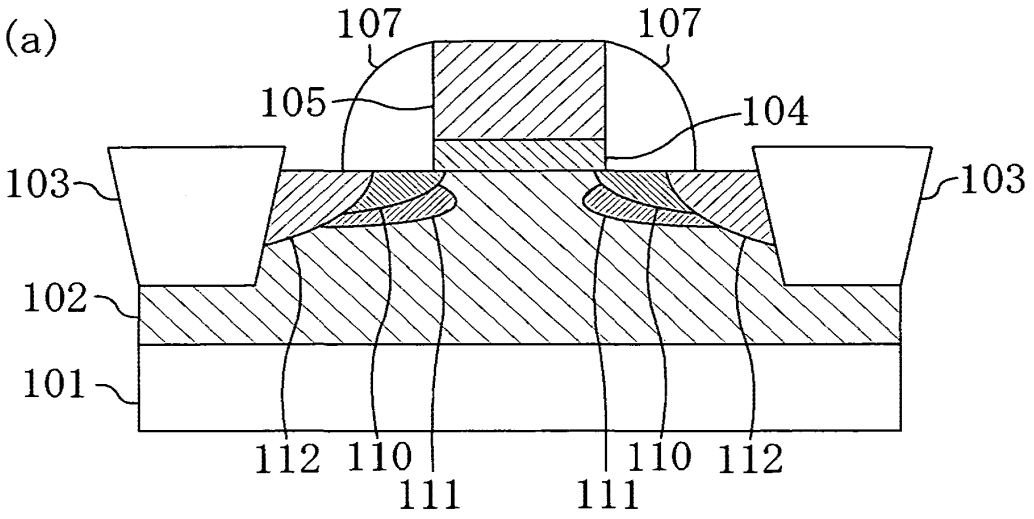
【図１６】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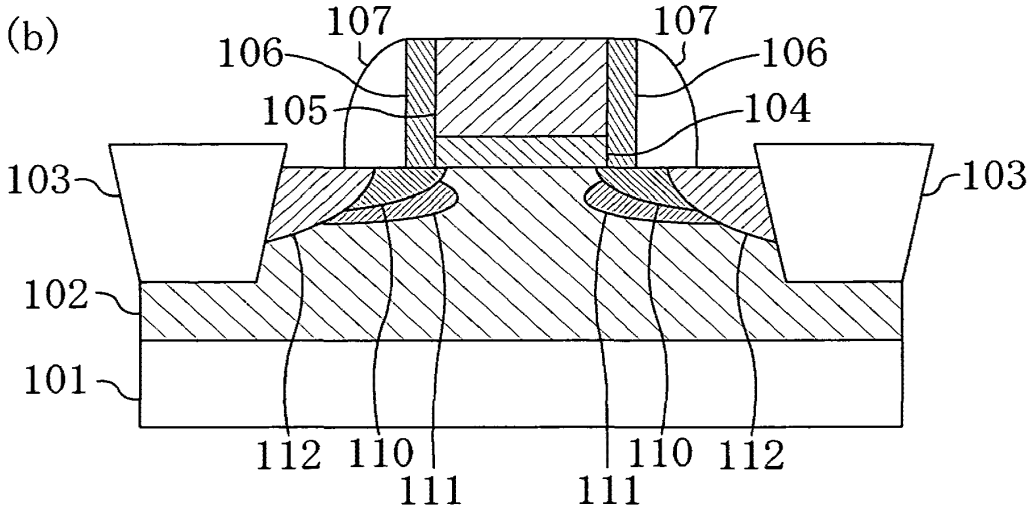
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【書類名】要約書
【要約】
【課題】　高誘電率ゲート絶縁膜を使用したＭＩＳＦＥＴにおいて高誘電率ゲート絶縁膜を劣化させることなくＭＩＳＦＥＴの特性を向上させる。
【解決手段】　基板１の活性領域上に高誘電率ゲート絶縁膜４Ａを介してゲート電極５が形成されている。ゲート電極５の側面には絶縁性のサイドウォール７が形成されている。高誘電率ゲート絶縁膜４Ａはゲート電極５の下側からサイドウォール７の下側まで連続的に形成されている。高誘電率ゲート絶縁膜４Ａにおけるサイドウォール７の下側領域の厚さは、高誘電率ゲート絶縁膜４Ａにおけるゲート電極５の下側領域の厚さよりも小さい。
【選択図】　図１

特願２００５－２２７４５７

出　願　人　履　歴　情　報

識別番号　［０００００５８２１］

１．変更年月日　１９９０年　８月２８日
［変更理由］　新規登録
住　所　大阪府門真市大字門真１００６番地
氏　名　松下電器産業株式会社

出証番号　出証特２００６－３００９２８５

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
11/491,260	07/24/2006	☐ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/TERRY MALLOY ROSS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/491,260	07/24/2006	Junji Hirase	071971-0620

CONFIRMATION NO. 4092

20277
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC20005-3096

Title: Semiconductor device and method for fabricating the same

Publication No. US-2007-0032007-A1
Publication Date: 02/08/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 703-305-3028.

Pre-Grant Publication Division, 703-605-4283

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	07/24/2006	Junji Hirase	071971-0620	4092

20277 7590 06/27/2008
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
06/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)	
	11/491,260	HIRASE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *01* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-10, drawn to a semiconductor device, classified in class 257, subclass 295.

   II. Claims 11-20, drawn to a method for fabricating a semiconductor device, classified in class 438, subclass 197.

2. Inventions Group II and Group I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the step c) etching part of the high dielectric constant gate insulating film can be substituted by lift-off technique.

3. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above <u>and</u> there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

   (a) the inventions have acquired a separate status in the art in view of their different classification;

   (b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

4. The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during

prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder**. Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
June 12, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	11/491,260	HIRASE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

Index of Claims	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/491,260	HIRASE ET AL.
	Examiner	**Art Unit**
	Chuong A. Luu	2892

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
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Docket No.: 071971-0620 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: 4092
Application No.: 11/491,260	:	Group Art Unit: 2892
Filed: July 24, 2006	:	Examiner: Chuong A. LUU

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Restriction
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Noting the Office Action of June 27, 2008 wherein restriction has been required, Applicant hereby elects Group I (claims 1-10) for prosecution in the above-identified application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:mjb
Facsimile: 202.756.8087

Please recognize our Customer No. 53080 as our correspondence address.

Date: July 18, 2008

WDC99 1593378-1.071971.0620

Electronic Acknowledgement Receipt

EFS ID:	3641945
Application Number:	11491260
International Application Number:	
Confirmation Number:	4092
Title of Invention:	Semiconductor device and method for fabricating the same
First Named Inventor/Applicant Name:	Junji Hirase
Customer Number:	20277
Filer:	Michael E. Fogarty/Michelle Bryant
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	071971-0620
Receipt Date:	18-JUL-2008
Filing Date:	24-JUL-2006
Time Stamp:	15:32:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	ResponsetoRestrictionRequirement-071971-0620.pdf	32301 861851acfea9ede8aa24c2c666cfff4caed06972	no	1

Warnings:

Information:

Total Files Size (in bytes):	32301

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	07/24/2006	Junji Hirase	071971-0620	4092

20277 7590 11/12/2008
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
11/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No.	Applicant(s)	
	11/491,260	HIRASE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1and 7-10* is/are rejected.

7)☒ Claim(s) *2-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/24/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Group I, claims 1-10 inn the reply filed on July 18, 2008 is acknowledged. -Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

PRIOR ARTS REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claim 1 is rejected under 35 U.S.C. 102(e as being anticipated by Hieda et al. (U.S. 6,992,358).

Hieda discloses a semiconductor device with

(1) a high dielectric constant gate insulating film (102-oxide) formed on an active region in a substrate (101);

a gate electrode (103) formed on the high dielectric constant gate insulating film (102-oxide);

an insulating sidewall (106) formed on each side surface of the gate electrode (103),

wherein the high dielectric constant gate insulating film (102-oxide) is continuously formed so as to extend from under the gate electrode (103) to under the insulating sidewall (106), and

at least part of the high dielectric constant gate insulating film (102-oxide) located under the insulating sidewall (106) has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film (102-oxide) located under the gate electrode (103) (see Figure 5B);

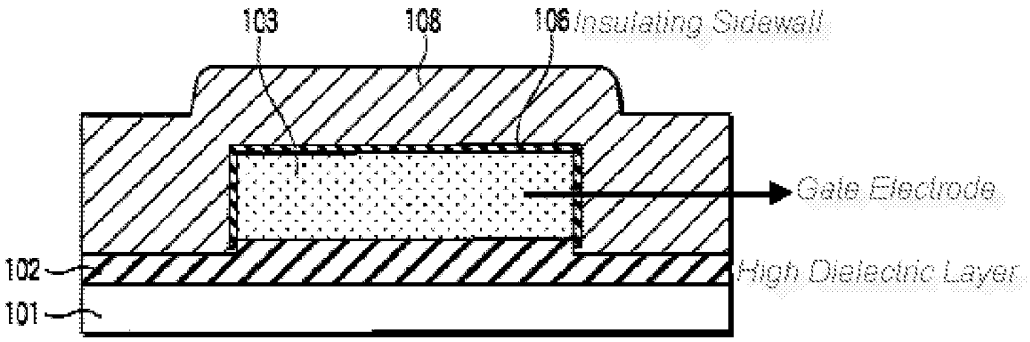

FIG. 5B

PRIOR ARTS REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda et al. (U.S. 6,992,358) in view of Cheng (U.S. 6,642,071).

Hieda teaches the above outlined features except for disclosing the high dielectric constant gate insulating film includes a notch at a side end portion; further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film and the buffer insulating film is a silicon oxide film. However, Cheng discloses a TFT array with**(7)** wherein the high dielectric constant gate insulating film includes a notch at a side end portion (see Figure 6); **(8)** further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film (see Figure 4); **(9)** wherein the buffer insulating film is a silicon oxide film (see column 4, lines 15-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hieda to include a notch at a side end portion; further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film and the buffer insulating film is a silicon oxide film as disclosed in Cheng because it prevent any junction between electrodes (For Example: See Column 5, Lines 29-33).

Additionally, since Hieda and Cheng are both from the same field of endeavor (semiconductors), the purpose disclosed by Cheng would have been recognized in the pertinent art of Hieda.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda et al. (U.S. 6,992,358) in view of Djomehri et al. (U.S. 6,929,992).

Hieda teaches everything above with the exception of disclosing the gate electrode is fully silicided. However, Djomehri discloses a NMOS device with **(10)** wherein the gate electrode is a fully silicided gate electrode of which an entire region has been silicided. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Hieda to include the gate electrode is a fully silicided gate electrode as disclosed in Cheng because in order to increase the gate work function (For Example: See Column 7, Lines 37-38).

Additionally, since Hieda and Djomehri are both from the same field of endeavor (semiconductors), the purpose disclosed by Djomehri would have been recognized in the pertinent art of Hieda.

Allowable Subject Matter

Claims 2-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Chuong A Luu/
Primary Examiner, Art Unit 2892
September 24, 2008

Notice of References Cited	Application/Control No. 11/491,260	Applicant(s)/Patent Under Reexamination HIRASE ET AL.	
	Examiner Chuong A. Luu	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,992,358	01-2006	Hieda et al.	257/407
*	B	US-6,929,992	08-2005	Djomehri et al.	438/199
*	C	US-6,642,071	11-2003	Cheng, Jia-Shyong	438/22
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	11/491,260	HIRASE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

UNITED STATES PATENT AND TRADEMARK OFFICE

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BIB DATA SHEET

CONFIRMATION NO. 4092

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/491,260	07/24/2006 RULE	438	2892	071971-0620

APPLICANTS

Junji Hirase, Osaka, JAPAN;
Akio Sebe, Osaka, JAPAN;
Naoki Kotani, Hyogo, JAPAN;
Gen Okazaki, Hyogo, JAPAN;
Kazuhiko Aida, Chiba, JAPAN;
Shinji Takeoka, Osaka, JAPAN;

**** CONTINUING DATA ****************************** None, CAL

**** FOREIGN APPLICATIONS ****************************** Yes, CAL

JAPAN 2005-227457 08/05/2005

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/08/2006

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /CHUONG A LUU/ Examiner's Signature	☑ Met after Allowance CAL Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 11	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2

ADDRESS

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096
UNITED STATES

TITLE

Semiconductor device and method for fabricating the same

FILING FEE RECEIVED 1000	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4123	(257/296,295,310.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:19
L2	491	(257/296,295,310.ccls.) and (gate or electrode) near ((gate or electrode) adj (insulat$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:20
L3	491	(257/296,295,310.ccls.) and ((gate or electrode) near ((gate or electrode) adj (insulat$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:20
L4	371	(257/296,295,310.ccls.) and ((gate or electrode) adj ((gate or electrode) adj (insulat$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:20
L5	48	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:21
L6	26	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:21
L7	12	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:22

L8	17	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:22
L9	36	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) with (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:22
L10	49	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:22
L11	5	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:24
S2	1	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/27 07:33
S3	2578	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/08/27 07:35
S4	1390	(257/310).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/08/27 07:35
S5	3	09/916509	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/01 13:58

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7/24/2006

SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 071971-0620	SERIAL NO. Not Yet Assigned 11/491,260
	APPLICANT Junji HIRASE, et al.	
	FILING DATE July 24, 2006	GROUP 2892 ~~Not Yet Assigned~~

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
/C.L./		WATANABE, Ken, Partial English Translation of "HfSiON-CMOS technology for achieving high performance and high reliability," SEMI FORUM Japan, 2005, IT System & ULSI Technology,	
/C.L./		HORI, Takashi, "1/4-μm LATID (LArge-Tilt-angle Implanted Drain) TECHNOLOGY FOR 3.3-V OPERATION", CH2637-7/89/0000-0777 1989 IEEE, IEDM 89-777-780-IEDM 89	
/C.L./		SAYAMA, et al., H.,, "80nm CMOSFET Technology Using Double Offset-Implanted Source/Drain Extension and Low Temperature SiN Process", IEDM 2000, IEDM 00-239-242-IEDM 00	

EXAMINER	DATE CONSIDERED
/Chuong Luu/	9/24/2008

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Index of Claims	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/491,260	HIRASE ET AL.
	Examiner	**Art Unit**
	Chuong A. Luu	2892

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date								
Final	Original	9/24/08								
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/491,260	HIRASE ET AL.
	Examiner	Art Unit
	Chuong A. Luu	2892

SEARCHED			
Class	Subclass	Date	Examiner
257	295-296 310	9/24/2008	CAL

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Please see the attachment.	9/24/2008	CAL

OIPE
JAN 1 2 2009
PATENT & TRADEMARK OFFICE

IFW

Docket No.: 071971-0620 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Customer Number: 53080
Junji HIRASE, et al.	Confirmation Number: 4092
Application No.: 11/491,260	Group Art Unit: 2892
Filed: July 24, 2006	Examiner: Not Yet Assigned

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

CERTIFICATION PARAGRAPH

The undersigned certifies that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR 1.97(e)(2).

The reference was cited in a corresponding U.S. Office Action and its relevance discussed therein. A copy of the U.S. Office Action is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:mkl
Facsimile: 202.756.8087
Date: January 12, 2009

OIPE
JAN 12 2009
PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
071971-0620	11/491,260
APPLICANT: Junji HIRASE, et al.	
FILING DATE: July 24, 2006	GROUP: 2892

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	2006/0121740 A2	6/8/2006	SAKAI et al	
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		U.S. Office Action issued in U.S. Patent Application No. 11/543,865 dated on November 12, 2008	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Docket No.: 071971-0620 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: 4092
Application No.: 11/491,260	:	Group Art Unit: 2892
Filed: July 24, 2006	:	Examiner: CHUONG A. LUU

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

In accordance with 37 CFR 1.17(p), please charge the fee of **$180.00** to Deposit Account No. 500417.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:mjb
Facsimile: 202.756.8087
Date: February 11, 2009

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
071971-0620	11/491,260
APPLICANT: Junji HIRASE, et al.	
FILING DATE: July 24, 2006	GROUP: 2892

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	2003/0022422 A1	01-30-2003	TORII et al.	
		US	2004/0004234 A1	01-08-2004	YAGISHITA et al.	
		US	2004/0129997 A1	07-08-2004	MORIFUJI	
		US	2005/0121733 A1	06-09-2005	CHEN et al.	
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal

Application Number:	11491260
Filing Date:	24-Jul-2006
Title of Invention:	Semiconductor device and method for fabricating the same
First Named Inventor/Applicant Name:	Junji Hirase
Filer:	Michael E. Fogarty/Margaret Barham
Attorney Docket Number:	071971-0620

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
			Total in USD ($)	**180**

Electronic Acknowledgement Receipt

EFS ID:	4775302
Application Number:	11491260
International Application Number:	
Confirmation Number:	4092
Title of Invention:	Semiconductor device and method for fabricating the same
First Named Inventor/Applicant Name:	Junji Hirase
Customer Number:	20277
Filer:	Michael E. Fogarty/Margaret Barham
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	071971-0620
Receipt Date:	11-FEB-2009
Filing Date:	24-JUL-2006
Time Stamp:	15:26:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	713
Deposit Account	500417
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement Letter	P04204201_IDS_071971-0620.pdf	81257 3006cff6eda7f912ccd2d7316c8a6a8e0ad6a942	no	3
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	29717 98a4c8729e9a0ec384b6ed9980aae127492c04a4	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	110974		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 071971-0620

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PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: 4092
Application No.: 11/491,260	:	Group Art Unit: 2892
Filed: July 24, 2006	:	Examiner: CHUONG A. LUU

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.

☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	15	20	0	$52.00 =	$0.00
Independent Claims	2	3	0	$220.00 =	$0.00
		Multiple dependent claims newly presented			$0.00
		Fee for extension of time			$0.00
				Total of Above Calculations	$0.00

☐ Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:rp
Facsimile: 202.756.8087
Date: February 12, 2009

Docket No.: 071971-0620 **PATENT**

FEB 12 2009 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: 4092
Application No.: 11/491,260	:	Group Art Unit: 2892
Filed: July 24, 2006	:	Examiner: Chuong A. LUU

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

In response to the Office Action dated November 12, 2008, having a three-month shortened statutory period for response set to expire February 12, 2009, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A semiconductor device comprising:

a high dielectric constant gate insulating film formed on an active region in a substrate;

a gate electrode formed on the high dielectric constant gate insulating film; and

an insulating sidewall formed on each side surface of the gate electrode,

wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall, [[and]]

at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode,

the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and

part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

2. (Canceled)

3. (Currently amended) The semiconductor device of claim [[2]] 1, wherein the high dielectric constant gate insulating film is formed so as not to be located under the second insulating sidewall.

4. (Currently amended) The semiconductor device of claim [[2]] 1, wherein the high dielectric constant gate insulating film is continuously formed so as to extend to under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

5. (Currently amended) The semiconductor device of claim [[2]] 1, wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the second insulating sidewall, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the first insulating sidewall.

6. (Currently amended) [[The]] A semiconductor device ~~of claim 1, wherein~~ comprising:

a high dielectric constant gate insulating film formed on an active region in a substrate;

a gate electrode formed on the high dielectric constant gate insulating film; and

an insulating sidewall formed on each side surface of the gate electrode,

wherein the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the insulating sidewall,

at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode,

the insulating sidewall includes a first insulating sidewall formed on a side surface of the

gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween,

the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the second insulating sidewall,

part of the high dielectric constant gate insulating film located under the first insulating sidewall has the same thickness as a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, and

part of the high dielectric constant gate insulating film located under the second insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode.

7. (Original) The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.

8. (Original) The semiconductor device of claim 1, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

9. (Original) The semiconductor device of claim 8, wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film.

10. (Original) The semiconductor device of claim 1, wherein the gate electrode is a fully silicided gate electrode of which an entire region has been silicided.

11-20. (Cancelled)

21. (New) The semiconductor device of claim 6, wherein the high dielectric constant gate insulating film includes a notch at a side end portion.

22. (New) The semiconductor device of claim 6, further comprising a buffer insulating film between the substrate and the high dielectric constant gate insulating film.

23. (New) The semiconductor device of claim 22, wherein the buffer insulating film is a silicon oxide film or a silicon oxynitride film.

24. (New) The semiconductor device of claim 6, wherein the gate electrode is a fully silicided gate electrode of which an entire region has been silicided.

25. (New) The semiconductor device of claim 1, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.

26. (New) The semiconductor device of claim 6, wherein the high dielectric constant gate insulating film is formed of a Hf based oxide.

REMARKS

In response to the pending Office Action, Applicants have cancelled claims 2 and 11-20, without prejudice. Claims 11-20 being subject to a restriction requirement and not elected for prosecution in the above-identified application. Claim 1 has been amended to include the elements of claim 2, and claim 6 has been amended into independent format. Finally, new claims 21-26 have been added. New claims 21-24 track original claims 7-10, respectively. No new matter has been added. It is further noted that an Information Disclosure Statement is being filed concurrently with this response.

As claims 2 and 6 were indicated to recite patentable subject matter, it is respectfully submitted that claims 1 and 6, as amended, are now in condition for allowance. Further, as all other pending claims depend on either claim 2 or claim 6, it is respectfully submitted that these claims are also in condition for allowance.

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:rp
Facsimile: 202.756.8087
Date: February 12, 2009

WDC99 1684197-1.071971.0620

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 11/491,260	Filing Date 07/24/2006	☒ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 02/12/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 15	Minus	** 20	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/NICHELE PETERSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PLUS Search Results for S/N 11491260, Searched Mon Apr 13 12:55:57 EDT 2009

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

6784035 99
6975001 99
7294898 99
20010050396 99
20030022422 99
20030139001 99
20030197224 99
20050003595 99
20060131670 99
20070032007 99
20070152277 99
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20080036008 99
20080067590 99
20080179752 99
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OIPE
APR 16 2009
PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
071971-0620	11/491,260
APPLICANT: Junji HIRASE, et al.	
FILING DATE: July 24, 2006	GROUP: 2892

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	2005/0127436 A1	06-16-2005	HENSON et al.	Corresponds w/ CN 1610129 A
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
		CN 1610129 A	04-27-2005		Corresponds w/ US 2005/0127436		X
		JP 2005-064190	03-10-2005	TOSHIBA CORP.		JAPAN (w/ English Abstract)	
		JP 2004-356576	12-16-2004	SEMICONDUCTOR LEADING EDGE TECHNOLOGIES INC.		JAPAN (w/ English Abstract)	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		Chinese Office Action, with English Translation, issued in Chinese Patent Application No. CN 200610093872.2, dated March 20, 2009.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

OIPE
APR 16 2009
PATENT & TRADEMARK OFFICE

IFW

Docket No.: 071971-0620 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Junji HIRASE, et al.	:	Confirmation Number: 4092
Application No.: 11/491,260	:	Group Art Unit: 2892
Filed: July 24, 2006	:	Examiner: Chuong A. LUU

For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection or Notice of Allowance.

CERTIFICATION PARAGRAPH

The undersigned certifies that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement as described in 37 CFR 1.97(e)(1).

References **CN 1610129, JP 2004-356576** and **JP 2005-064190** were cited in a Chinese Office Action and the relevance is discussed therein. A copy of the Chinese Office Action, together with an English language version thereof, is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ksa
Facsimile: 202.756.8087
Date: April 16, 2009

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

20277 7590 06/02/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2892	

DATE MAILED: 06/02/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	07/24/2006	Junji Hirase	071971-0620	4092

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/02/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20277 7590 06/02/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	07/24/2006	Junji Hirase	071971-0620	4092

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LUU, CHUONG A	2892	438-197000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____

2_____

3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	07/24/2006	Junji Hirase	071971-0620	4092

20277 7590 06/02/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2892	

DATE MAILED: 06/02/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 214 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 214 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	11/491,260	HIRASE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/12/2009*.

2. ☒ The allowed claim(s) is/are *1,3-10 and 21-26*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/12/09; 2/11/09; 4/16/09
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

Claims 1, 3-10 and 21-26 are allowed.

The following is an examiner's statement of reasons for allowance: The examiner has reviewed the prior art in light of applicant's claimed invention and finds that the combined claims define over the prior art. The cited prior art does not disclose or suggest a semiconductor device inter alia the limitations "….at least part of the high dielectric constant gate insulating film located under the insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode, the insulating sidewall includes a first insulating sidewall formed on a side surface of the gate electrode and a second insulating sidewall formed on the side surface of the gate electrode with the first insulating sidewall interposed therebetween, the high dielectric constant gate insulating film is continuously formed so as to extend from under the gate electrode to under the first insulating sidewall, and part of the high dielectric constant gate insulating film located under the first insulating sidewall has a smaller thickness than a thickness of part of the high dielectric constant gate insulating film located under the gate electrode. . …."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
April 26, 2009

Issue Classification	Application/Control No.	Applicant(s)/Patent under Reexamination	
	11/491,260	HIRASE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

ISSUE CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
438	197	257	295	310	410				
INTERNATIONAL CLASSIFICATION									
H 0 1 L	21/336								
H 0 1 L	21/8234								
H 0 1 L	29/76								
H 0 1 L	29/94								
H 0 1 L	27/108								

(Assistant Examiner) (Date)	/Chuong A. Luu/ 4/26/2009	Total Claims Allowed: 15
(Legal Instruments Examiner) (Date)	(Primary Examiner) (Date)	O.G. Print Claim(s): 1 / O.G. Print Fig.: 5

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181
	2		32		62		92		122		152		182
2	3		33		63		93		123		153		183
3	4		34		64		94		124		154		184
4	5		35		65		95		125		155		185
5	6		36		66		96		126		156		186
6	7		37		67		97		127		157		187
7	8		38		68		98		128		158		188
8	9		39		69		99		129		159		189
9	10		40		70		100		130		160		190
	11		41		71		101		131		161		191
	12		42		72		102		132		162		192
	13		43		73		103		133		163		193
	14		44		74		104		134		164		194
	15		45		75		105		135		165		195
	16		46		76		106		136		166		196
	17		47		77		107		137		167		197
	18		48		78		108		138		168		198
	19		49		79		109		139		169		199
	20		50		80		110		140		170		200
10	21		51		81		111		141		171		201
11	22		52		82		112		142		172		202
12	23		53		83		113		143		173		203
13	24		54		84		114		144		174		204
14	25		55		85		115		145		175		205
15	26		56		86		116		146		176		206
	27		57		87		117		147		177		207
	28		58		88		118		148		178		208
	29		59		89		119		149		179		209
	30		60		90		120		150		180		210

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
071971-0620	11/491,260
APPLICANT: Junji HIRASE, et al.	
FILING DATE: July 24, 2006	GROUP: 2892

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/C.L./		US	2005/0127436 A1	06-16-2005	HENSON et al.	Corresponds w/ CN 1610129 A
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
/C.L./		CN 1610129 A	04-27-2005		Corresponds w/ US 2005/0127436		X
/C.L./		JP 2005-064190	03-10-2005	TOSHIBA CORP.		JAPAN (w/ English Abstract)	
/C.L./		JP 2004-356576	12-16-2004	SEMICONDUCTOR LEADING EDGE TECHNOLOGIES INC.		JAPAN (w/ English Abstract)	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
/C.L./		Chinese Office Action, with English Translation, issued in Chinese Patent Application No. CN 200610093872.2, dated March 20, 2009.	

EXAMINER	DATE CONSIDERED
/Chuong Luu/	4/26/2009

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	5	(("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445")).PN.	US-PGPUB; USPAT	OR	OFF	2009/04/26 19:26
L3	3	09/824672	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 19:28
L4	2	09/848431	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 19:29
L6	8	(("20050127436") or ("6284630") or ("20020163039") or ("20010028086") or ("5223445") or ("6509612") or ("6794258") or ("6614081")).PN.	US-PGPUB; USPAT	OR	OFF	2009/04/26 19:32
L7	102	("20020028555" | "20020089022" | "3764865" | "3886584" | "3906620" | "4343078" | "5219773" | "5223445" | "5369297" | "5668028" | "5864160" | "5898207" | "5908307" | "5994747" | "6057217" | "6057582" | "6069041" | "6097069" | "6114735" | "6153455" | "6207485" | "6211045" | "6221708" | "6225669" | "6232187" | "6238978" | "6255165" | "6271094" | "6277681" | "6287917" | "6291865" | "6335549" | "6348385" | "6352885" | "6406945" | "6429496" | "6436774" | "6492695" | "6495890" | "6498374" | "6509612" | "6514808").PN. OR ("5223445" | "6284630" | "6509612" | "6614081" | "6794258"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/04/26 19:33
L8	3	10/904875	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 19:43
L9	6	("6015736" | "6025240").PN. OR ("6238978").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2009/04/26 21:34
L10	1424	(257/324).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/26 21:42

L13	6	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:44
L14	1140	(257/410).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/26 21:45
L15	159	257/e29.132.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:46
L16	1641	257/e29.133.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:46
L17	1558	257/e29.137.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:46
L18	180	257/e29.138.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:46
L19	645	257/e29.162.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:46
L20	543	257/e29.165.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:46
L21	1	(257/e29.132,e29.133,e29.134,e29.135, e29.136,e29.137,e29.138,e29.138,e29.162, e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat$4 or dielectric or oxide)) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:48

L22	1177	(257/411).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2009/04/26 21:52
L23	50	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat $4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:56
L24	48	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat $4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:56
L25	108	("257"/$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:56
L26	24	(257/e29.132,e29.133,e29.134,e29.135, e29.136,e29.137,e29.138,e29.138,e29.162, e29.163,e29.164,e29.164,e29.165.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat $4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:57
L27	100	(257/e$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:57
L28	29	("438"/$.ccls.) and (gate or electrode) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 21:57
L29	5360	(257/296,295,310,324,410,411.ccls.) and (gate or electrode) and ((gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 22:05
L30	48	(257/296,295,310,324,410,411.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj (gate or electrode) adj (dielectric or oxide or insulat$4)) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 22:21

L31	756	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat$4)) with ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 22:23
L32	182	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat$4)) near ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 22:23
L33	995	(257/296,295,310,324,410,411.ccls.) and (((gate or electrode) adj (dielectric or oxide or insulat$4)) same ((high adj dielectric adj constant) or (ferroelectric))) and @ad<="20050805"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/26 22:23
S2	1	11/491260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/27 07:33
S3	2578	(257/295).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/08/27 07:35
S4	1390	(257/310).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/08/27 07:35
S5	3	09/916509	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/01 13:58
S6	4123	(257/296,295,310.ccls.) and (gate or electrode) and ((gate or electrode) adj (insulat$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:19
S7	491	(257/296,295,310.ccls.) and (gate or electrode) near ((gate or electrode) adj (insulat$4 or dielectric or oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:20
S8	491	(257/296,295,310.ccls.) and ((gate or electrode) near ((gate or electrode) adj (insulat$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:20

S9	371	(257/296,295,310.ccls.) and ((gate or electrode) adj ((gate or electrode) adj (insulat$4 or dielectric or oxide)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:20
S10	48	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:21
S11	26	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:21
S12	12	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:22
S13	17	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:22
S16	5	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 23:24
S17	18	("20030209761" | "20040150520" | "20040178451" | "20050040464" | "20050051843" | "20050110085" | "4979014" | "6437404" | "6538916" | "6580132" | "6639246" | "6646307" | "6687152" | "6724046" | "6740938" | "6744390" | "6800513" | "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/03 19:45
S18	49	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) same (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/03 20:28
S19	78	gate near (fully adj silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/07 23:04
S20	15	gate near (fully adj silicide)	USPAT	OR	ON	2008/11/07 23:04

S21	5	"6992358"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/07 23:07
S22	18	("20030209761" | "20040150520" | "20040178451" | "20050040464" | "20050051843" | "20050110085" | "4979014" | "6437404" | "6538916" | "6580132" | "6639246" | "6646307" | "6687152" | "6724046" | "6740938" | "6744390" | "6800513" | "6822071").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/07 23:09
S24	25	("4403396" | "4689869" | "5034791" | "5053849" | "5286665" | "5405787" | "5545578" | "5547883" | "5751048" | "5866473" | "5895273" | "5960270" | "5963789" | "6011290" | "6017826" | "6037630" | "6060733" | "6110785" | "6204133" | "6303479" | "6326250" | "6352885" | "6383937" | "6399469" | "6417084").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/07 23:18
S25	20	("5751048").URPN.	USPAT	OR	ON	2008/11/07 23:40
S27	839	gate and ((gate adj (oxide or insulat$4 or dielectric)) with (notch$4 or undercut$4))	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/07 23:43
S28	112	gate and ((gate adj (oxide or insulat$4 or dielectric)) near (notch$4 or undercut$4))	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/07 23:43
S29	18	gate and ((gate adj (oxide or insulat$4 or dielectric)) adj (notch$4 or undercut$4))	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/07 23:43
S30	47	("20020036328" | "20020171113" | "20030209761" | "20040031979" | "20040099885" | "20040145000" | "20040150520" | "20040178451" | "20050017305" | "20050035417" | "20050040464" | "20050051843" | "20050110085" | "20050167766" | "20050205944" | "20050212055" | "20050224800" | "20050285189" | "20060071285" | "20060273409" | "4907041" | "4979014" | "5399896" | "5985724" | "6413802" | "6437404" | "6534787" | "6538916" | "6580132" | "6613624" | "6639246" | "6646307" | "6687152" | "6706571" | "6724046" | "6740914" | "6740938" | "6744103" | "6744390" | "6800513" | "6800885" | "6822071" | "6967379" | "6992358" | "7112478").PN. OR ("6992358" | "7176537" | "7348642").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/09 18:32
S31	36	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) with (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/09 19:15

S32	165	(257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) and (high adj dielectric adj constant)) and overlap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/09 19:33
S33	3	("5384729" | "5708284" | "6107656").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/09 21:13
S34	2	("6614066").URPN.	USPAT	OR	ON	2008/11/09 21:14
S35	4908	gate with ((spacers or sidewalls) with (notch or under$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/09 21:20
S37	7	gate adj ((spacers or sidewalls) with (notch or under$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/09 21:20
S38	127	gate near ((spacers or sidewalls) near (notch or under$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/09 21:23
S39	11	(gate near ((spacers or sidewalls) near (notch or under$4))) and (high adj dielectric adj constant)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/11/09 21:24
S44	0	"257"/$.ccls. and (gate with (porous adj silicon)) and (spacer with conductive)	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/09 22:26
S45	5	"257"/$.ccls. and (gate with (porous adj silicon)) and (spacers same conductive)	US-PGPUB; USPAT; USOCR	OR	ON	2008/11/09 22:26
S46	2	(("6642071") or ("6929992")).PN.	USPAT	OR	OFF	2008/11/09 23:05
S47	6	(257/296,295,310.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:04
S48	21	("257"/$.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:05
S49	15	("438"/$.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:05

S51	51	(semiconductor) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:05
S52	15	("438"/$.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:06
S53	21	("257"/$.ccls.) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:06
S54	378	gate near ((spacers or sidewalls) with (notch or under$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:33
S55	299	(gate near ((spacers or sidewalls) with (notch or under$4))) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:36
S56	45	((257/296,295,310.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant)))and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:41
S57	578	(("257"/$.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant)))and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:41
S58	365	(("438"/$.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant)))and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:41
S59	365	(("438"/$.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) near (high adj dielectric adj constant))) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:41
S60	1642	(("438"/$.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) with (high adj dielectric adj constant))) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:42

S61	2491	(("257"/$.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) with (high adj dielectric adj constant))) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:42
S62	255	(("257"/$.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:42
S63	192	(("438"/$.ccls.) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:42
S64	306	((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))) and @ad<="20060724"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/21 20:43
S65	55	(semiconductor) and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 07:38
S66	3	(("20070228442") or ("20040171280") or ("20030207097")).PN.	US-PGPUB; USPAT	OR	OFF	2009/04/22 14:44
S67	1470	hirase.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:46
S68	70	S67 and junji	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:47
S69	0	S68 and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:47
S70	0	S68 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:48

S71	213	sebe.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:48
S72	13	S71 and akio	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:48
S73	0	S72 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:48
S74	17541	kotani.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:48
S75	207	S74 and naoki	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:49
S76	0	S75 and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:49
S77	0	okazaki and gen and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:49
S78	0	aida and kazuhiko and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:50
S79	0	takeoka and shinji and (((high adj dielectric adj constant) or (ferroelectric)) adj gate adj (layer or film)) and (gate or electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:50
S80	32	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/22 14:51

S81	19	(((semiconductor) and (gate or electrode) and (((gate or electrode) adj (insulat$4 or dielectric or oxide)) adj (high adj dielectric adj constant)))).clm.	US-PGPUB	OR	ON	2009/04/22 14:51

4/26/09 10:55:17 PM
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Substitute for form 1449/PTO)

ATTY. DOCKET NO.	SERIAL NO.
071971-0620	11/491,260
APPLICANT: Junji HIRASE, et al.	
FILING DATE: July 24, 2006	GROUP: 2892

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/C.L./		US	2003/0022422 A1	01-30-2003	TORII et al.	
/C.L./		US	2004/0004234 A1	01-08-2004	YAGISHITA et al.	
/C.L./		US	2004/0129997 A1	07-08-2004	MORIFUJI	
/C.L./		US	2005/0121733 A1	06-09-2005	CHEN et al.	
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	

EXAMINER	DATE CONSIDERED
/Chuong Luu/	4/28/2009

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ATTY. DOCKET NO.	SERIAL NO.
071971-0620	11/491,260

APPLICANT
Junji HIRASE, et al.

FILING DATE	GROUP
July 24, 2006	2892

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/C.L./		US	2006/0121740 A2	6/8/2006	SAKAI et al	
		US				
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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
/C.L./		**U.S. Office Action issued in U.S. Patent Application No. 11/543,865 dated on November 12, 2008**	

EXAMINER	DATE CONSIDERED
/Chuong Luu/	4/27/2009

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BIB DATA SHEET

CONFIRMATION NO. 4092

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/491,260	07/24/2006 RULE	438	2892	071971-0620

APPLICANTS

Junji Hirase, Osaka, JAPAN;
Akio Sebe, Osaka, JAPAN;
Naoki Kotani, Hyogo, JAPAN;
Gen Okazaki, Hyogo, JAPAN;
Kazuhiko Aida, Chiba, JAPAN;
Shinji Takeoka, Osaka, JAPAN;

**** CONTINUING DATA ****************************** None, CAL

**** FOREIGN APPLICATIONS ****************************** Yes, CAL

JAPAN 2005-227457 08/05/2005

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/08/2006

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /CHUONG A LUU/ Examiner's Signature	☑ Met after Allowance CAL Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 11	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2

ADDRESS

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096
UNITED STATES

TITLE

Semiconductor device and method for fabricating the same

FILING FEE RECEIVED 1000	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Index of Claims	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/491,260	HIRASE ET AL.
	Examiner	**Art Unit**
	Chuong A. Luu	2892

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
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Claim		Date								
Final	Original	4/26/09								
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Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	11/491,260	HIRASE ET AL.
	Examiner	Art Unit
	Chuong A. Luu	2892

SEARCHED			
Class	Subclass	Date	Examiner
257	295-296 310	9/24/2008	CAL
Update	Searched	4/22/2009	CAL
257	324 410	4/26/2009	CAL
257	411	4/26/2009	CAL

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
PG PUB TEXT SEARCH, See interference search printout.		4/26/2009	CAL

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Please see the attachment.	9/24/2008	CAL
Please see the attachment including East Search(US-PGPUB; USPAT; USOCR;EPO;JPO;DERWENT; IBM_TDB)	4/26/2009	CAL
(257/E29.132; E29.133; E29.137; E29.138; E29.162; E29.165).CCLS.	4/26/2009	CAL

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	07/24/2006	Junji Hirase	071971-0620	4092

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LUU, CHUONG A	2892	438-197000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
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(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

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2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(B) RESIDENCE: (CITY and STATE OR COUNTRY): Osaka JAPAN

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5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Date July 15, 2009
Typed or printed name Michael E. Fogarty
Registration No. 30,139

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01 FC:1501 1510.00 DA
02 FC:1504 300.00 DA
03 FC:8001 12.00 DA

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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20277 7590 06/02/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

Customer No.: 53080

OIPE IAP28 JUL 15 2009 PATENT & TRADEMARK OFFICE

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	07/24/2006	Junji Hirase	071971-0620	4092

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LUU, CHUONG A	2892	438-197000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

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2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: PANASONIC CORPORATION

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Osaka JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies Four (4)

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 500417 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date July 15, 2009

Typed or printed name Michael E. Fogarty Registration No. 36,139

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Bib Data Sheet

CONFIRMATION NO. 4092

SERIAL NUMBER	FILING OR 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/491,260	07/24/2006 RULE	438	2892	071971-0620

APPLICANTS

Junji Hirase, Osaka, JAPAN;
Akio Sebe, Osaka, JAPAN;
Naoki Kotani, Hyogo, JAPAN;
Gen Okazaki, Hyogo, JAPAN;
Kazuhiko Aida, Chiba, JAPAN;
Shinji Takeoka, Osaka, JAPAN;

**** CONTINUING DATA ****************************

**** FOREIGN APPLICATIONS ************************

JAPAN 2005-227457 08/05/2005

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
** 08/08/2006

		STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged	☐ yes ☐ no ☐ yes ☐ no ☐ Met after Allowance Examiner's Signature Initials	JAPAN	11	20	2

ADDRESS
53080

TITLE

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

FILING FEE RECEIVED		
1300	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/491,260	08/25/2009	7579227	071971-0620	4092

53080 7590 08/05/2009
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 214 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Junji Hirase, Osaka, JAPAN;
Akio Sebe, Osaka, JAPAN;
Naoki Kotani, Hyogo, JAPAN;
Gen Okazaki, Hyogo, JAPAN;
Kazuhiko Aida, Chiba, JAPAN;
Shinji Takeoka, Osaka, JAPAN;

IR103 (Rev. 11/05)

PTO/SB/131 (01-10)
Approved for use through 02/28/2011. OMB 0651-0020
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
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REQUEST FOR RECALCULATION OF PATENT TERM ADJUSTMENT IN VIEW OF *WYETH**

Attorney Docket Number: 071971-0620 / P42042-01	Patent Number: 7,579,227
Filing Date (or 371(b) or (f) Date): 7/24/2006	Issue Date: 8/25/2009
First Named Inventor: Junji Hirase	
Title: Semiconductor device and method for fabricating the same	

PATENTEE HEREBY REQUESTS RECALCULATION OF THE PATENT TERM ADJUSTMENT (PTA) UNDER 35 USC 154(b) INDICATED ON THE ABOVE-IDENTIFIED PATENT. THE PATENTEE'S SOLE BASIS FOR REQUESTING THE RECALCULATION IS THE USPTO'S PRE-*WYETH* INTERPRETATION OF 35 U.S.C. 154(b)(2)(A).

Note: This form is only for requesting a recalculation of PTA for patents issued before March 2, 2010, if the sole basis for requesting the recalculation is the USPTO's pre-*Wyeth* interpretation of 35 U.S.C. 154(b)(2)(A). See Instruction Sheet on page 2 for more information.

Patentees are reminded that to preserve the right to review in the United States District Court for the District of Columbia of the USPTO's patent term adjustment determination, a patentee must ensure that he or she also takes the steps required under 35 U.S.C. 154(b)(3) and (b)(4) and 37 CFR 1.705 in a timely manner.

**Wyeth v. Kappos*, No. 2009-1120 (Fed. Cir., Jan. 7, 2010).

Signature	Date 2/22/10
Name (Print/Typed) MICHAEL E. FOGARTY	Registration Number 36,139

Note: *Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below**.*

☐ *Total of _____ forms are submitted.

The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	7060230
Application Number:	11491260
International Application Number:	
Confirmation Number:	4092
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Junji Hirase
Customer Number:	53080
Filer:	Michael E. Fogarty/3328/Matilda Mason
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	071971-0620
Receipt Date:	22-FEB-2010
Filing Date:	24-JUL-2006
Time Stamp:	16:46:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for PTA recalculation in view of Wyeth	071971-0620Request.pdf	59423 2cbd309577f21ceca89c2301723f12dca3d57e35	no	1

Warnings:

Information:

Total Files Size (in bytes):	59423

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Mail Date: 04/21/2010

Applicant	: Junji Hirase	: DECISION ON REQUEST FOR
Patent Number	: 7579227	: RECALCULATION of PATENT
Issue Date	: 08/25/2009	: TERM ADJUSTMENT IN VIEW
Appliction No	: 11/491,260	: OF WYETH AND NOTICE OF INTENT TO
Filed	: 07/24/2006	: ISSUE CERTIFICATE OF CORRECTION
		:

The Request for Recalculation is **GRANTED** to the extent indicated.

The patent term adjustment has been determined to be **246** days. The USPTO will *sua sponte* issue a certificate of correction reflecting the amount of PTA days determined by the recalculation.

Prior to the issuance of the certificate of correction, the USPTO will afford patentee an opportunity to be heard and request reconsideration. Accordingly, patentee has **one month or thirty (30) days**, whichever is longer, to file a request for reconsideration of this patent term adjustment calculation. See 35 U.S.C. 154(b)(3)(B)(ii) and 37 CFR 1.322(a)(4). No extensions of time will be granted under 37 CFR 1.136.

Patentee should use document code PET.OP if electronically filing a request for reconsideration of this patent term adjustment calculation. The patentee must also include the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e). If patentee does not file a timely request for reconsideration of this patent term adjustment calculation including the information required by 37 CFR 1.705(b)(2) and the fee required by 37 CFR 1.18(e), the USPTO will issue a certificate of correction reflecting the PTA determination noted above.

Patentee should be aware that in order to preserve the right to review in the United States District Court for the District of Columbia of the USPTO patent term adjustment determination, patentee must ensure that he or she also take the steps required under 35 U.S.C. 154(b)(4)(A) in a timely manner. Nothing in the request for recalculation should be construed as providing an alternative time frame for commencing a civil action under 35 U.S.C. 154(b)(4)(A).

Any questions concerning this decision should be directed to the Office of Patent Legal Administration at 571-272-7702.

PTOL-549G (04/10)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,579,227 B2
APPLICATION NO. : 11/491260
DATED : August 25, 2009
INVENTOR(S) : Hirase et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page:

The first or sole Notice should read --

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 246 days.

Signed and Sealed this

Fourteenth Day of September, 2010

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office