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Ito et al.

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(45) **Date of Patent: Aug. 5, 2014**

(54) **SEMICONDUCTOR DEVICE**

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(73) Assignee: **Panasonic Corporation**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 68 days.

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Sep. 14, 2010 (JP) 2010-205599

(51) **Int. Cl.**
H01L 27/088 (2006.01)

(52) **U.S. Cl.**
USPC **257/368**

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USPC 257/632, 635, E21.409, E21.645, 257/E29.001, 18–20, 55, 63–70, 178, 192, 257/213, 272–274, 368–369, 257/E21.43–E21.434, E21.619, E21.634, 257/E27.059–E27.067, E29.193, E31.049; 438/153–154, 203, 938, 933
See application file for complete search history.

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Assistant Examiner — Lawrence-Linh T Nguyen
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(57) **ABSTRACT**

A first MIS transistor and a second MIS transistor of the same conductivity type are formed on an identical semiconductor substrate. An interface layer included in a gate insulating film of the first MIS transistor has a thickness larger than that of an interface layer included in a gate insulating film of the second MIS transistor.

15 Claims, 13 Drawing Sheets

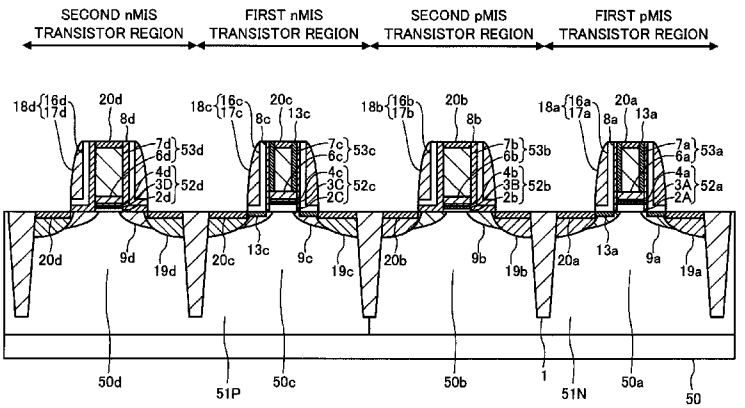

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FIG.1

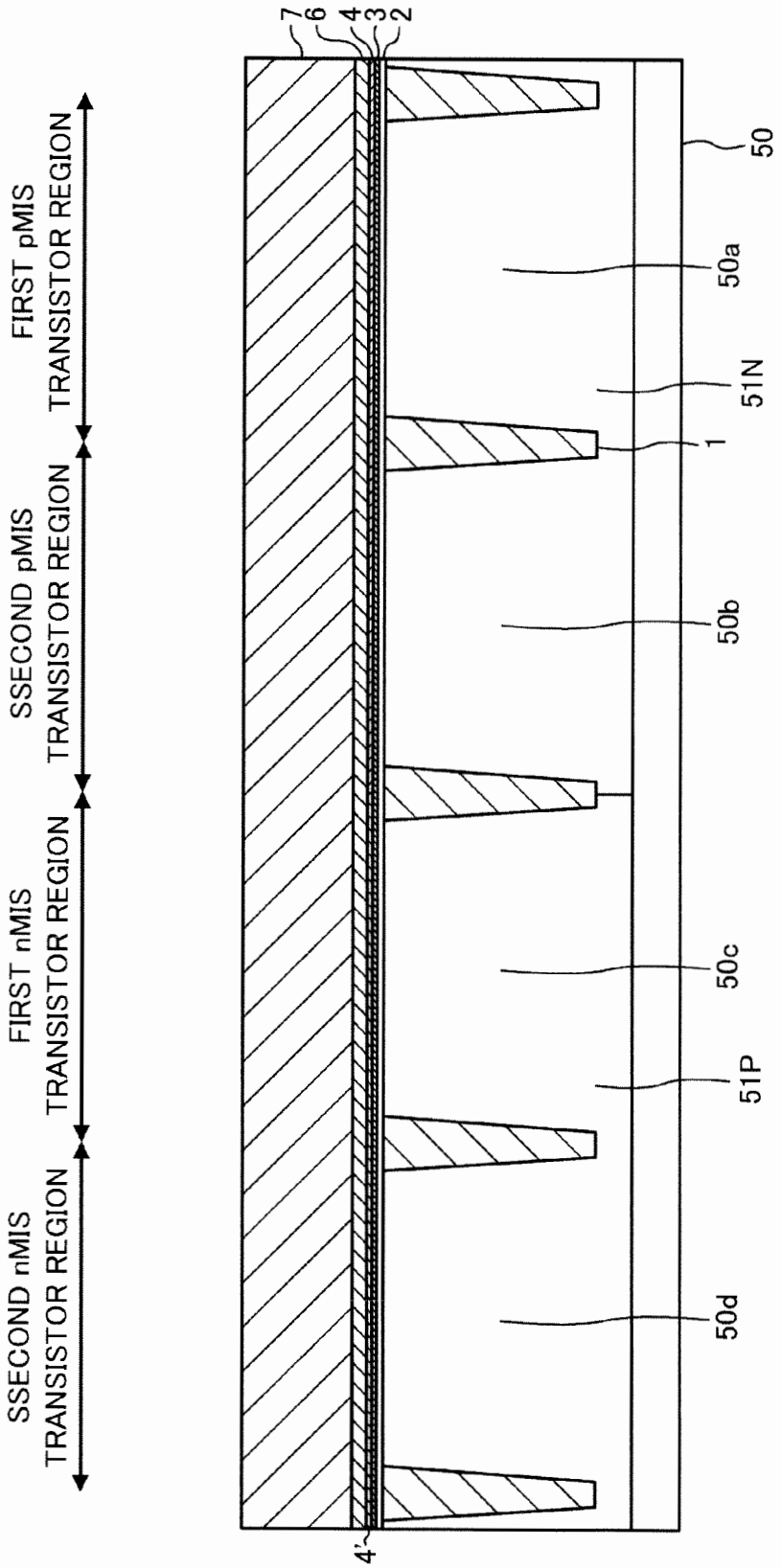

SSECOND nMIS TRANSISTOR REGION
FIRST nMIS TRANSISTOR REGION
SSECOND pMIS TRANSISTOR REGION
FIRST pMIS TRANSISTOR REGION
7
6
4
3
2
4'
50d
51P
50c
50b
1
51N
50a
50

FIG.2

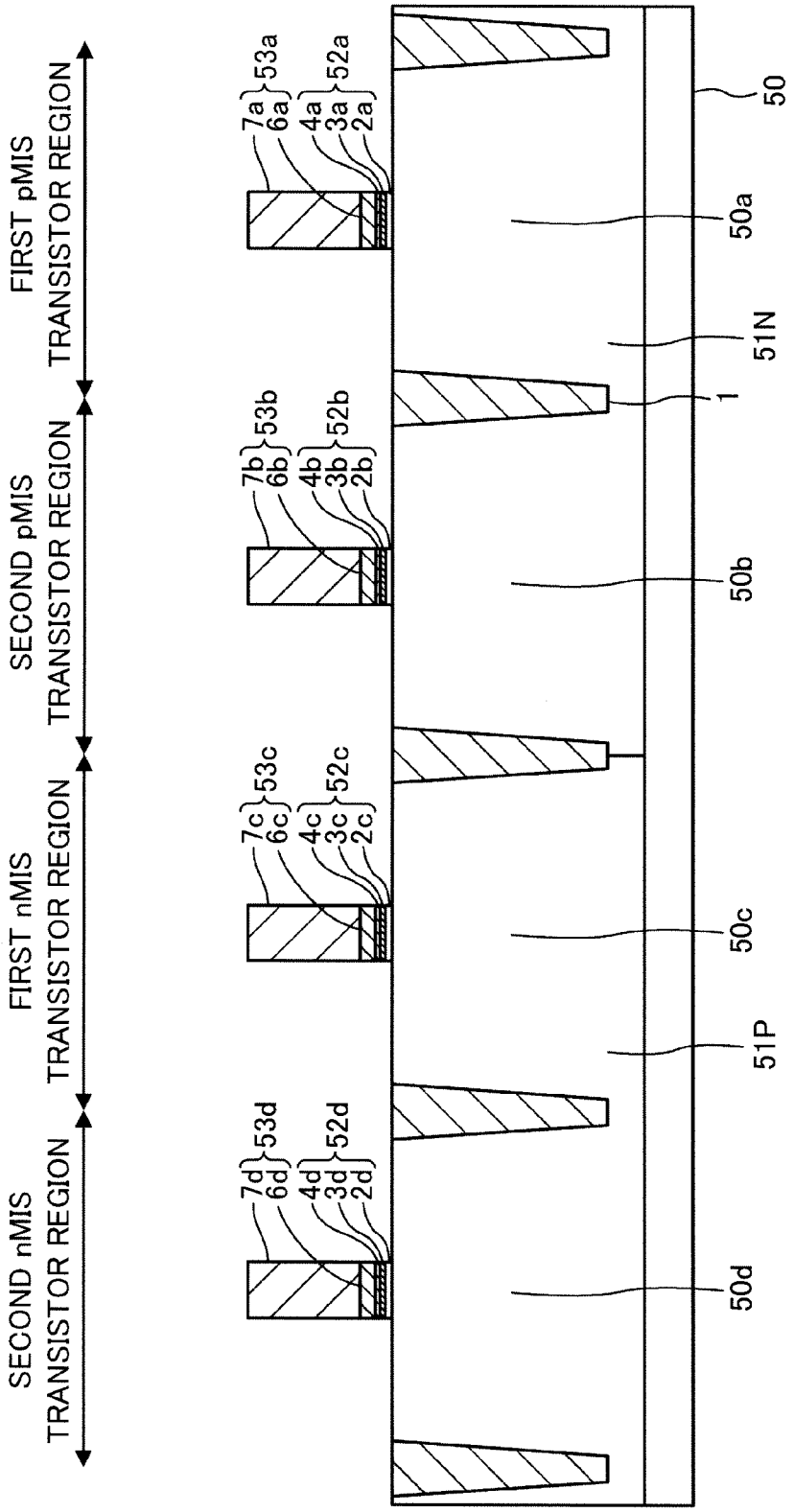
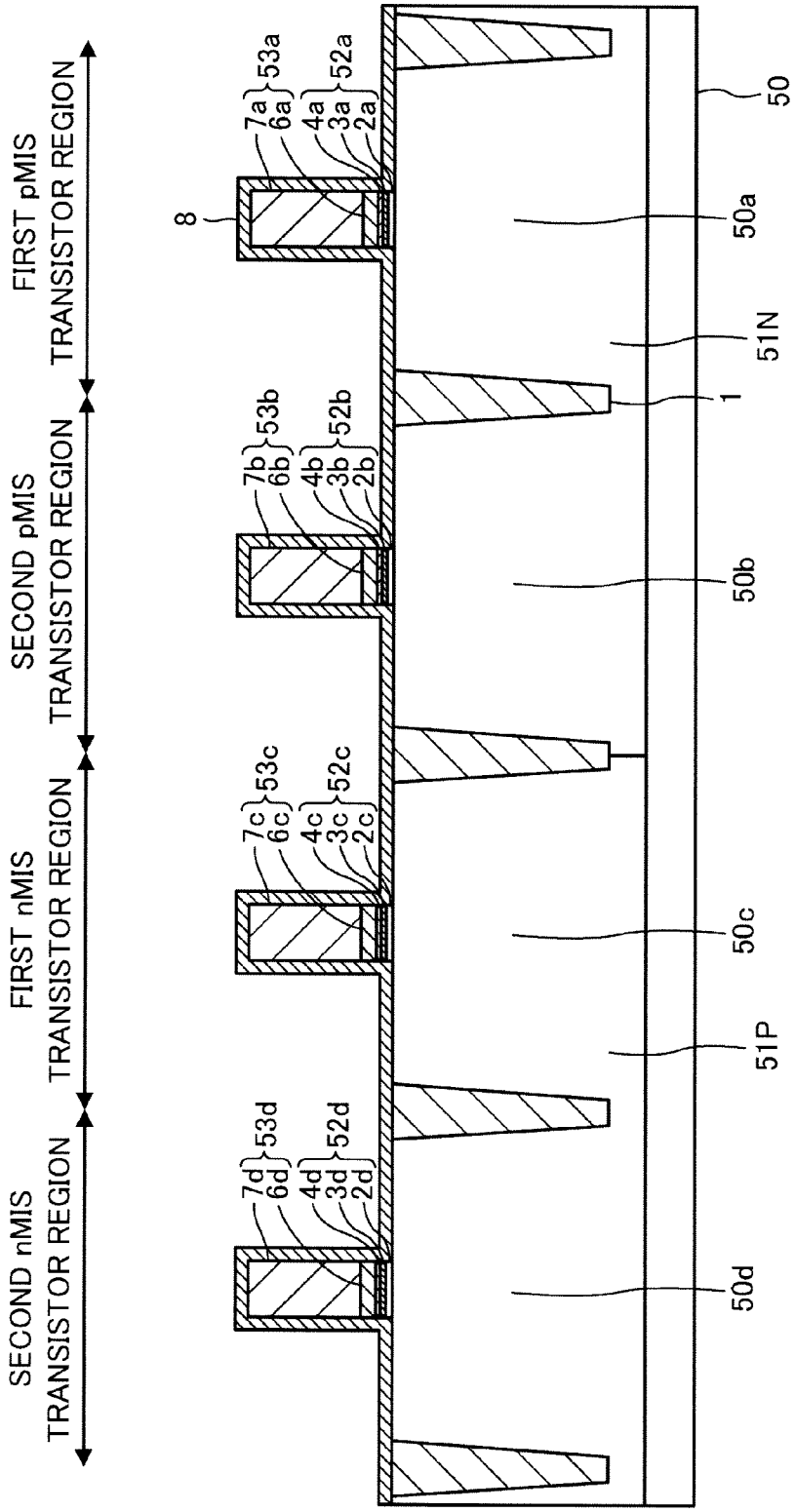

FIRST pMIS TRANSISTOR REGION
SECOND pMIS TRANSISTOR REGION
FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
7a
6a
53a
4a
3a
2a
52a
7b
6b
53b
4b
3b
2b
52b
7c
6c
53c
4c
3c
2c
52c
7d
6d
53d
4d
3d
2d
52d
50
50a
51N
1
50b
50c
51P
50d

FIG.3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FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
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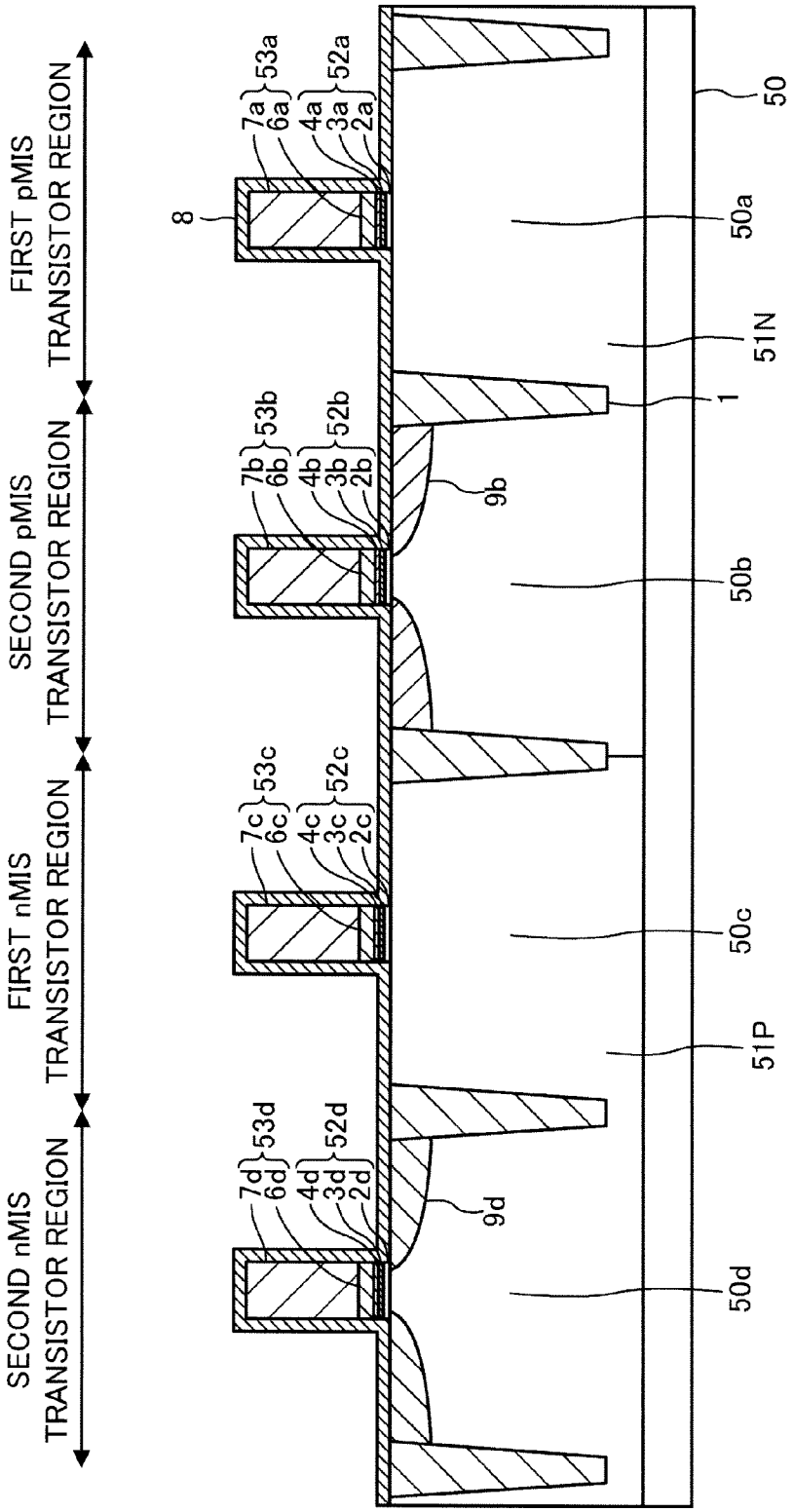
7a
6a
4a
3a
2a
53a
52a
7b
6b
4b
3b
2b
53b
52b
7c
6c
4c
3c
2c
53c
52c
7d
6d
4d
3d
2d
53d
52d
50
50a
51N
1
50b
50c
51P
50d

FIG.4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FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
8
7a
6a
4a
3a
2a
53a
52a
7b
6b
4b
3b
2b
53b
52b
7c
6c
4c
3c
2c
53c
52c
7d
6d
4d
3d
2d
53d
52d
9b
9d
1
50
50a
50b
50c
50d
51N
51P

FIG.5

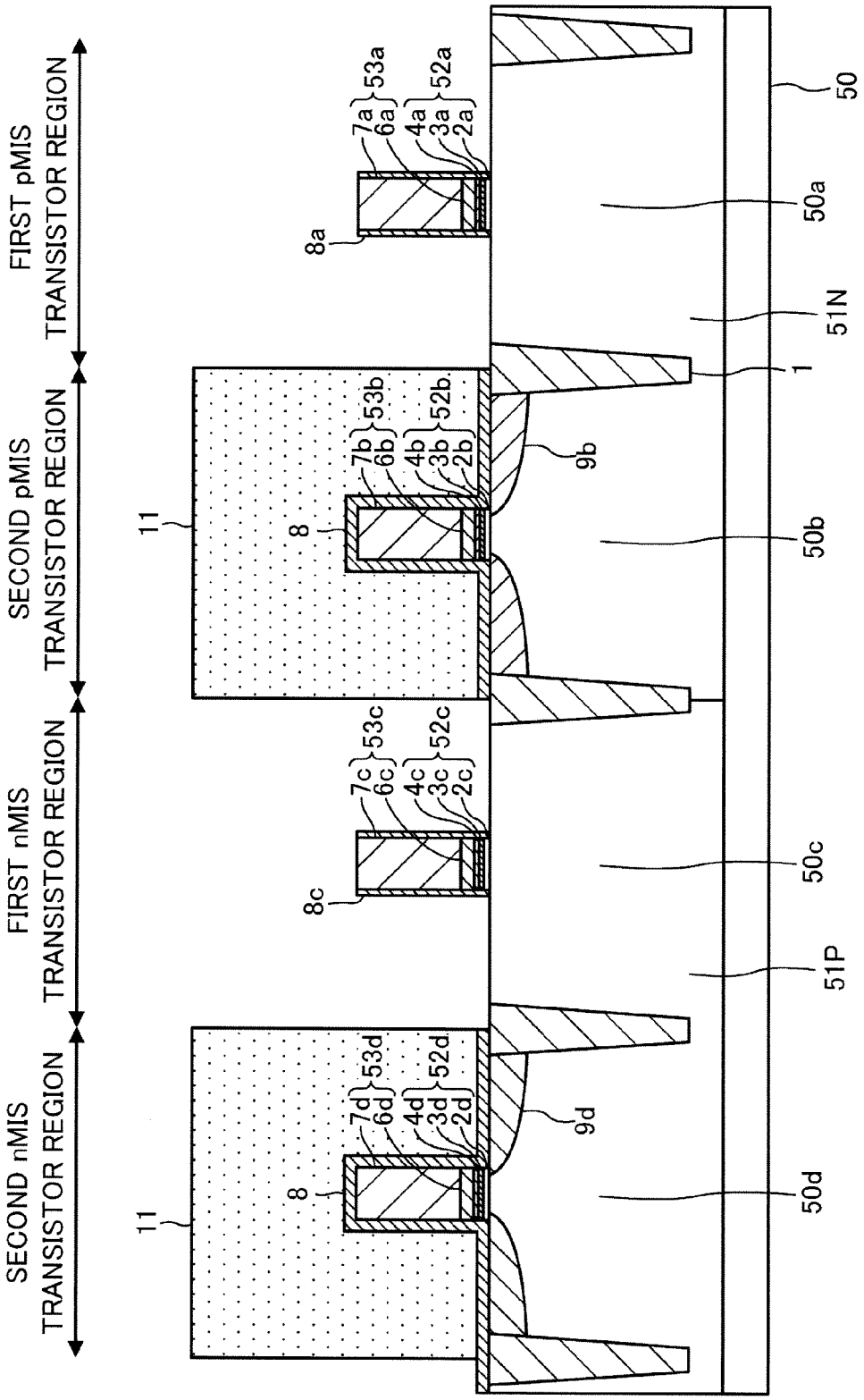

FIRST pMIS TRANSISTOR REGION
SECOND pMIS TRANSISTOR REGION
FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
7a
6a
53a
4a
3a
52a
2a
8a
50
50a
51N
1
7b
6b
53b
4b
3b
52b
2b
9b
11
8
50b
7c
6c
53c
4c
3c
52c
2c
8c
50c
51P
7d
6d
53d
4d
3d
52d
2d
9d
50d

FIG.6

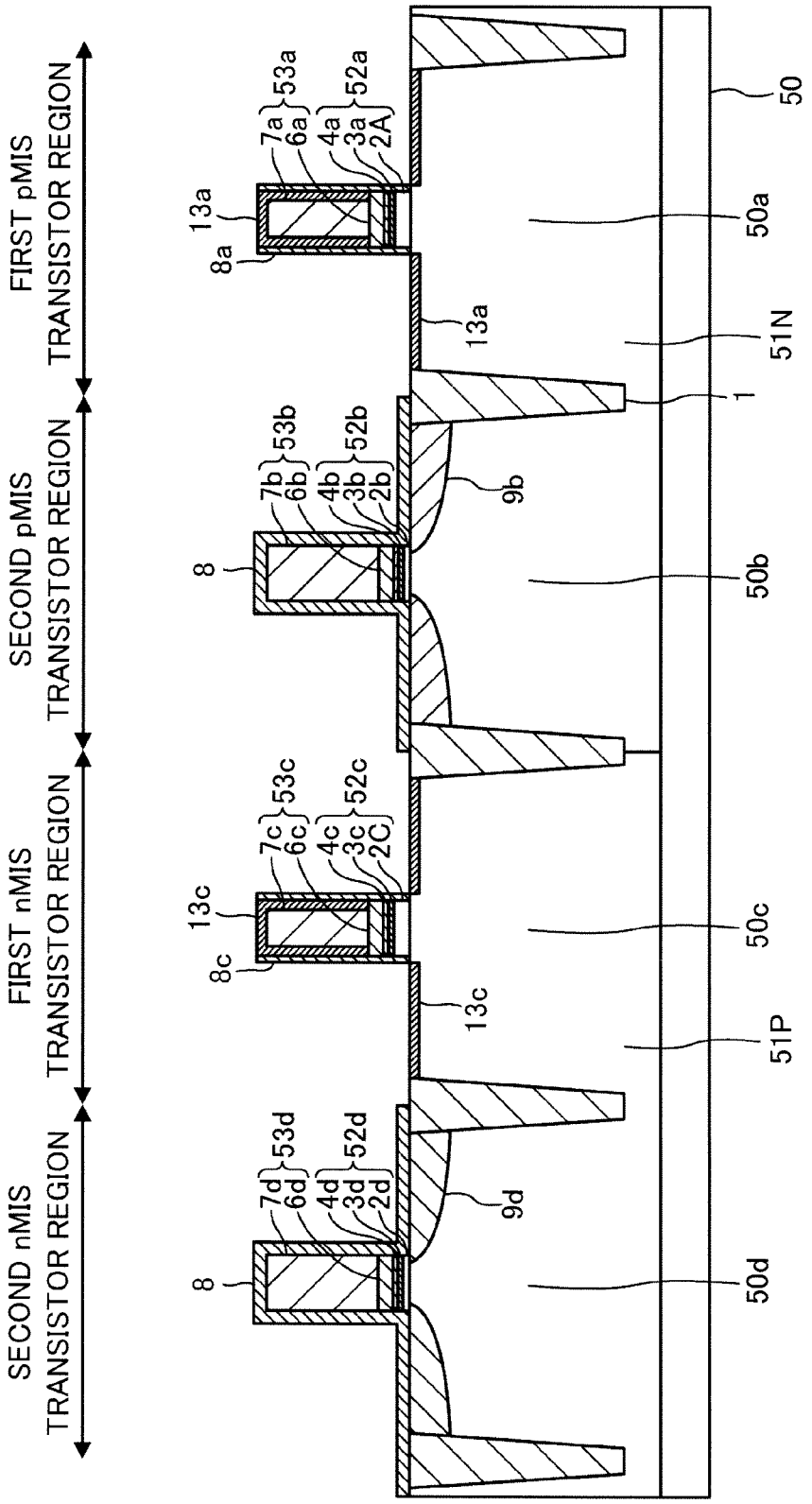

FIRST pMIS TRANSISTOR REGION
SECOND pMIS TRANSISTOR REGION
FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
53a
52a
7a
6a
4a
3a
2A
13a
8a
53b
52b
7b
6b
4b
3b
2b
8
53c
52c
7c
6c
4c
3c
2C
13c
8c
53d
52d
7d
6d
4d
3d
2d
9b
9d
50
50a
51N
1
50b
50c
51P
50d

FIG.7

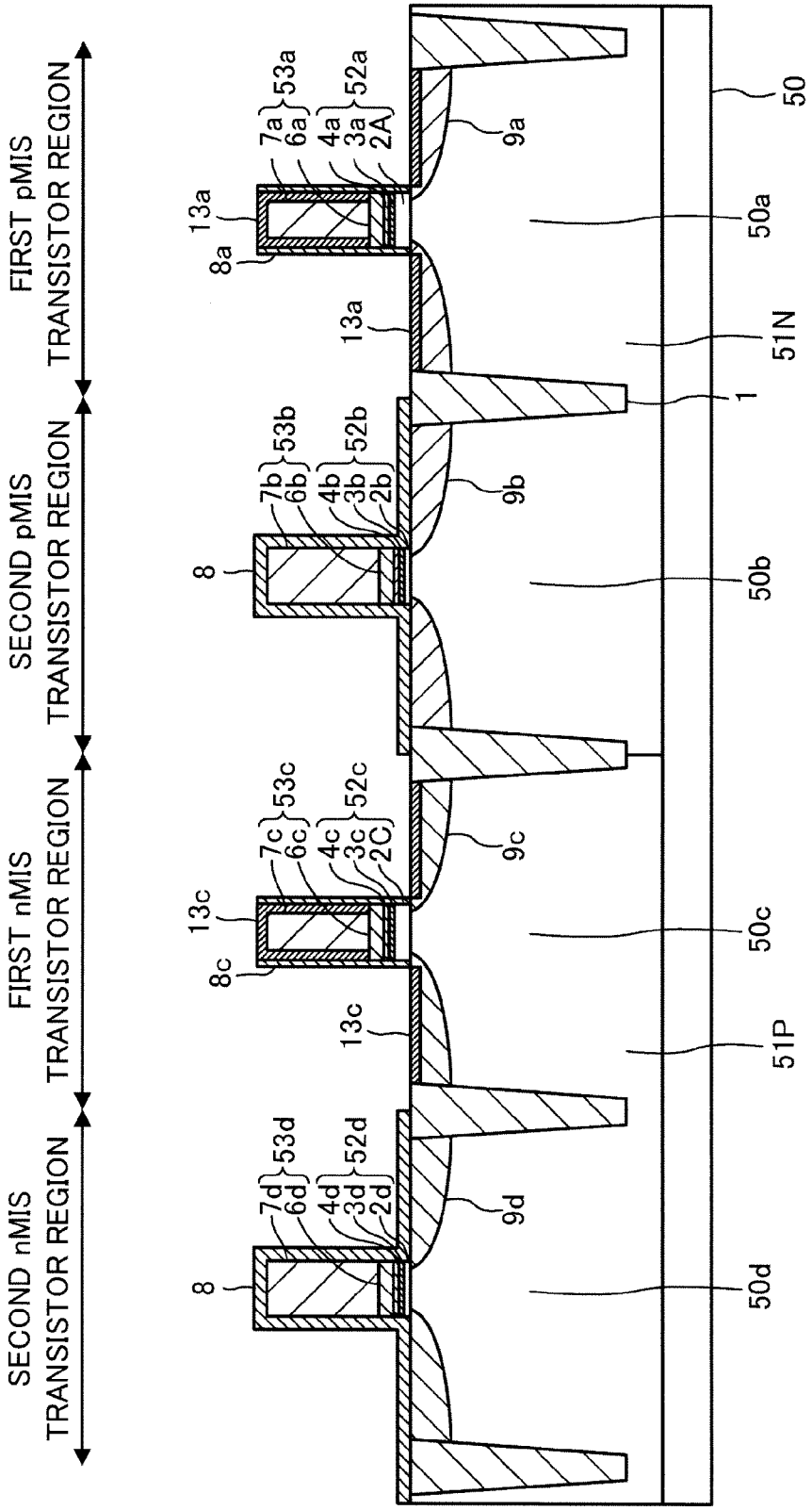

FIRST pMIS TRANSISTOR REGION
SECOND pMIS TRANSISTOR REGION
FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
53a
52a
7a
6a
4a
3a
2A
13a
8a
9a
50a
50
51N
1
53b
52b
7b
6b
4b
3b
2b
8
9b
50b
53c
52c
7c
6c
4c
3c
2C
13c
8c
9c
50c
51P
53d
52d
7d
6d
4d
3d
2d
9d
50d

FIG.8

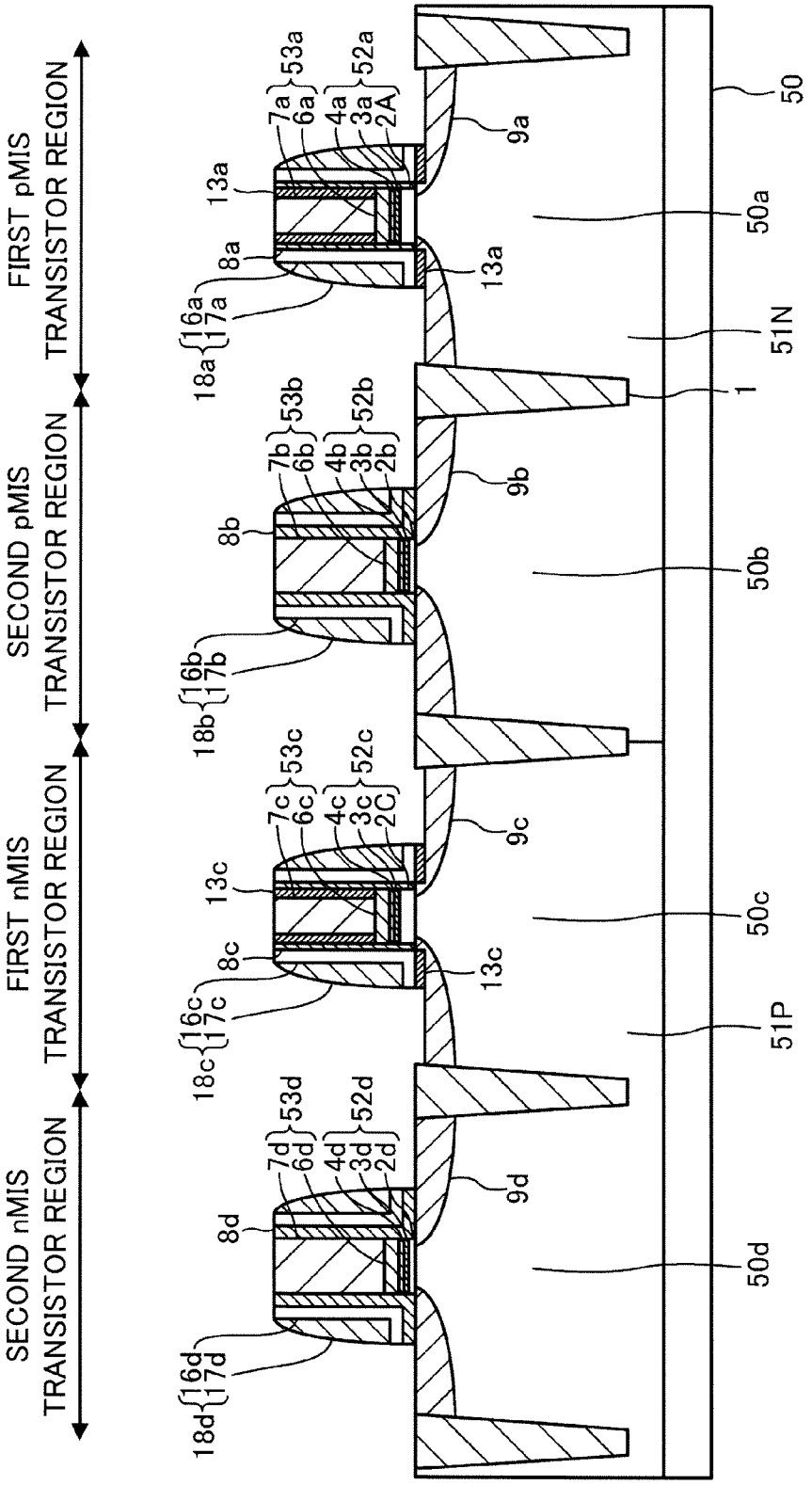

FIRST pMIS TRANSISTOR REGION
SECOND pMIS TRANSISTOR REGION
FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
53a
52a
7a
6a
4a
3a
2A
13a
8a
16a
17a
18a
9a
50a
51N
1
53b
52b
7b
6b
4b
3b
2b
8b
16b
17b
18b
9b
50b
53c
52c
7c
6c
4c
3c
2C
13c
8c
16c
17c
18c
9c
50c
51P
53d
52d
7d
6d
4d
3d
2d
8d
16d
17d
18d
9d
50d
50

FIG.9

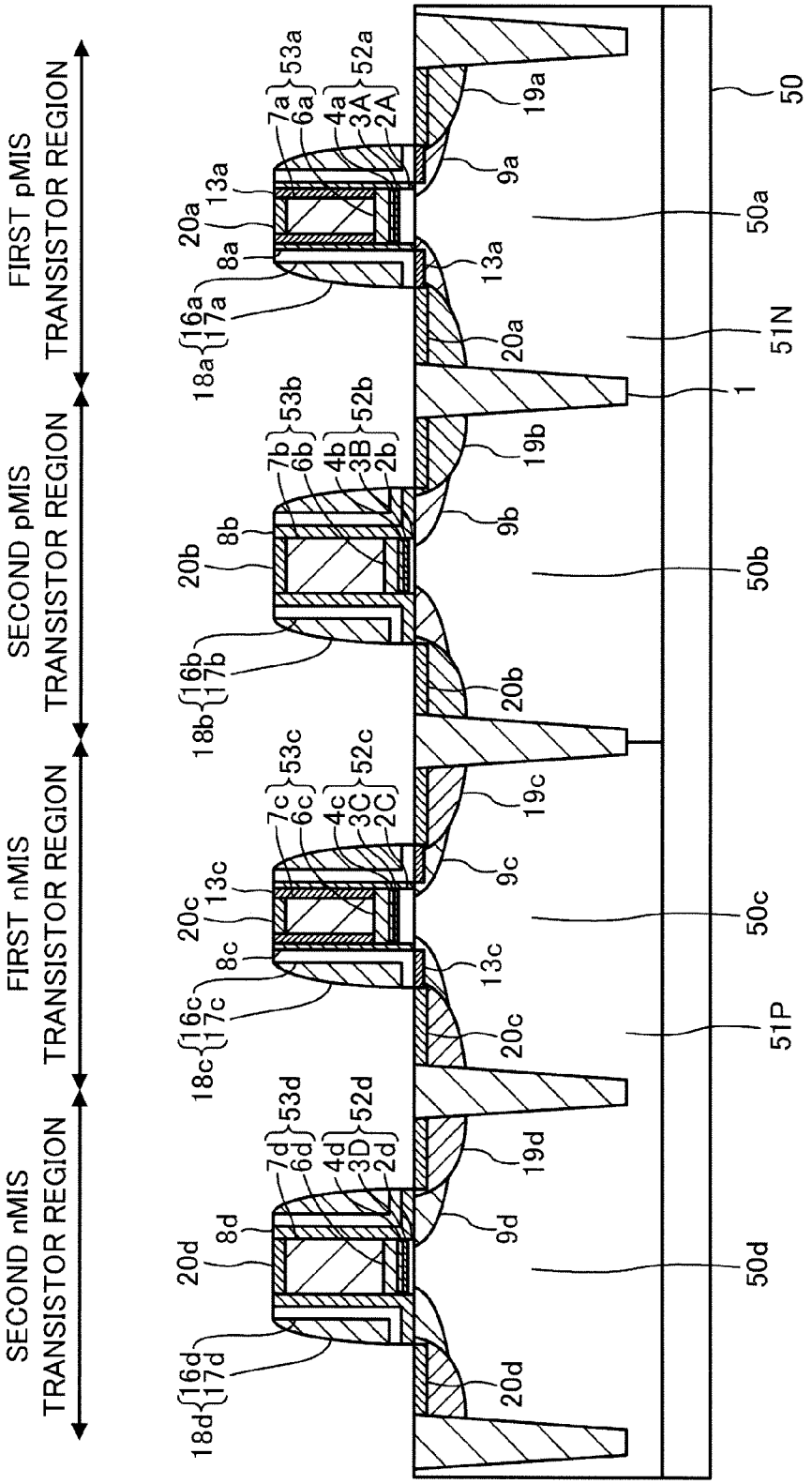

FIRST pMIS TRANSISTOR REGION
SECOND pMIS TRANSISTOR REGION
FIRST nMIS TRANSISTOR REGION
SECOND nMIS TRANSISTOR REGION
50
50a
50b
50c
50d
51N
51P
1
19a
19b
19c
19d
9a
9b
9c
9d
20a
20b
20c
20d
13a
13c
8a
8b
8c
8d
18a
18b
18c
18d
16a
17a
16b
17b
16c
17c
16d
17d
7a
6a
4a
3A
2A
53a
52a
7b
6b
4b
3B
2b
53b
52b
7c
6c
4c
3C
2C
53c
52c
7d
6d
4d
3D
2d
53d
52d

FIG.10

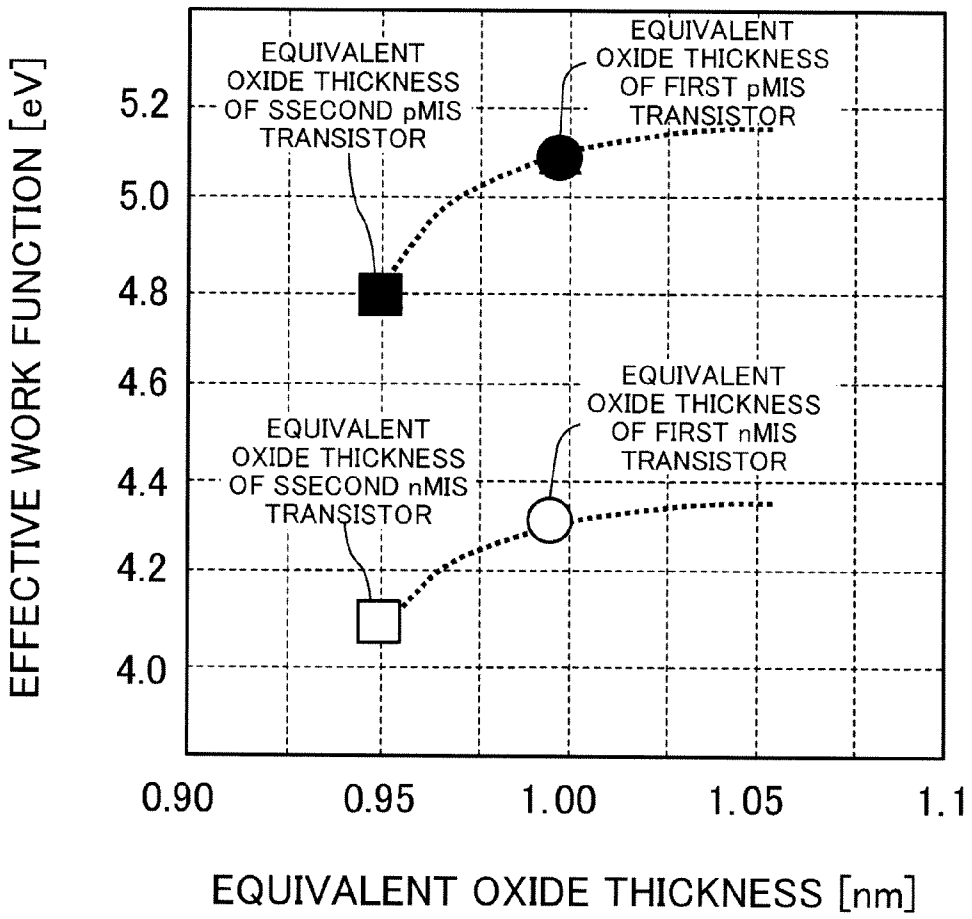

EFFECTIVE WORK FUNCTION [eV]
5.2
5.0
4.8
4.6
4.4
4.2
4.0
EQUIVALENT OXIDE THICKNESS OF SSECOND pMIS TRANSISTOR
EQUIVALENT OXIDE THICKNESS OF FIRST pMIS TRANSISTOR
EQUIVALENT OXIDE THICKNESS OF SSECOND nMIS TRANSISTOR
EQUIVALENT OXIDE THICKNESS OF FIRST nMIS TRANSISTOR
0.90
0.95
1.00
1.05
1.1
EQUIVALENT OXIDE THICKNESS [nm]

FIG.11
PRIOR ART

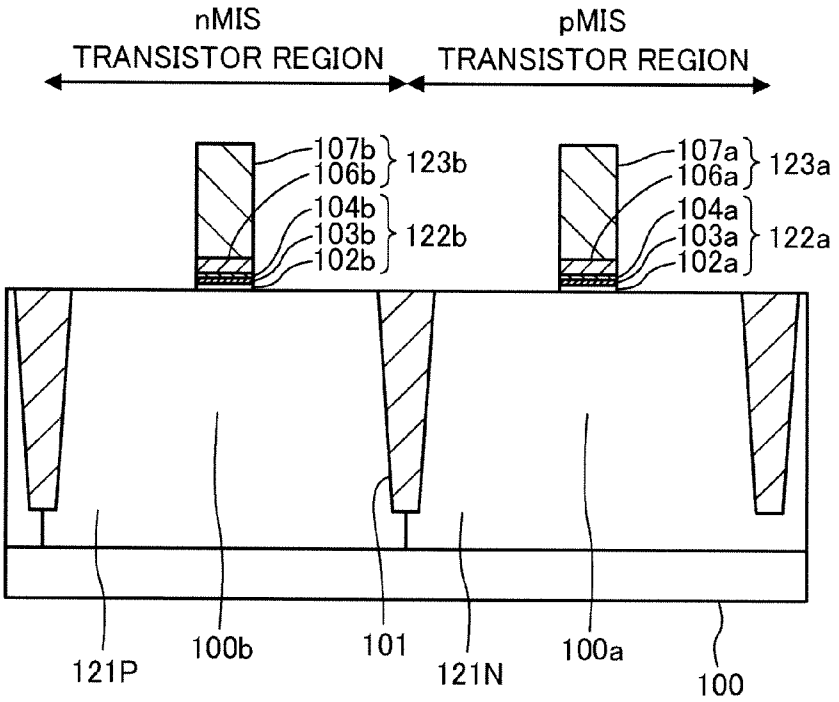


FIG.12
PRIOR ART

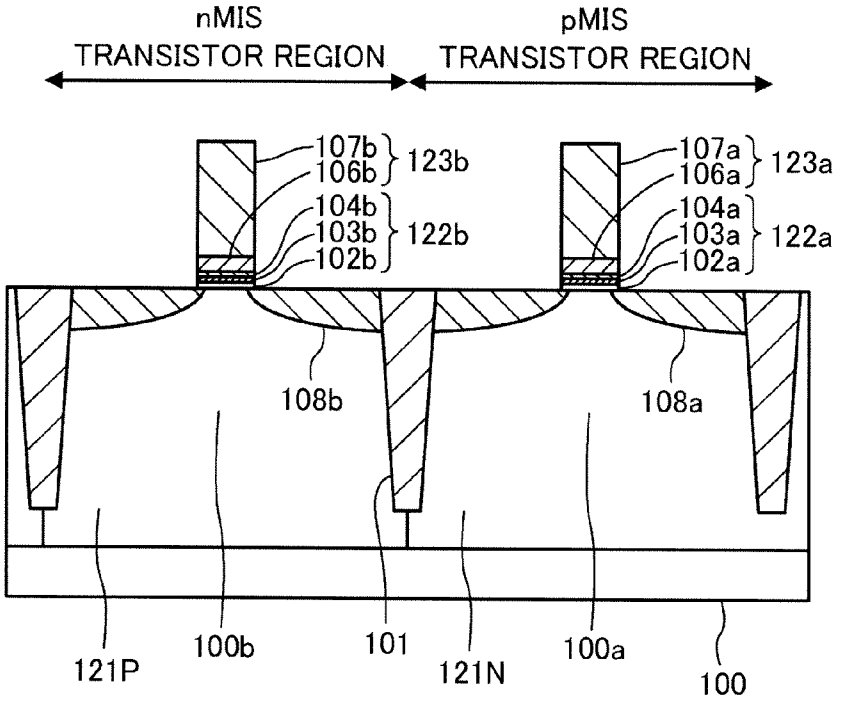


FIG.13
PRIOR ART

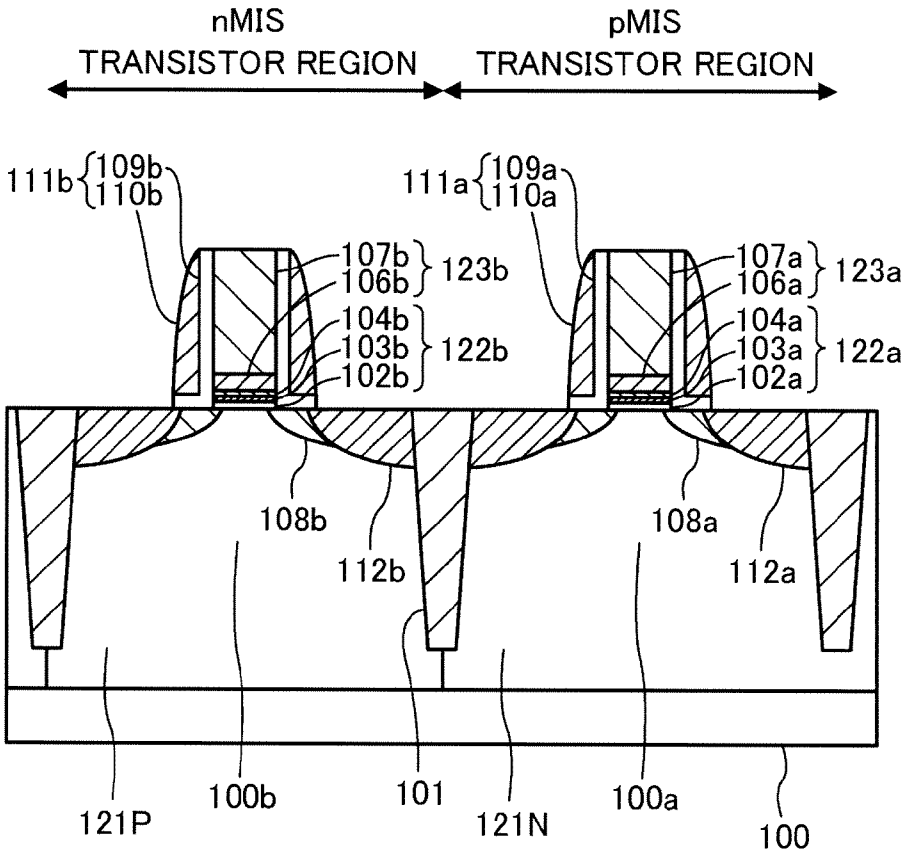
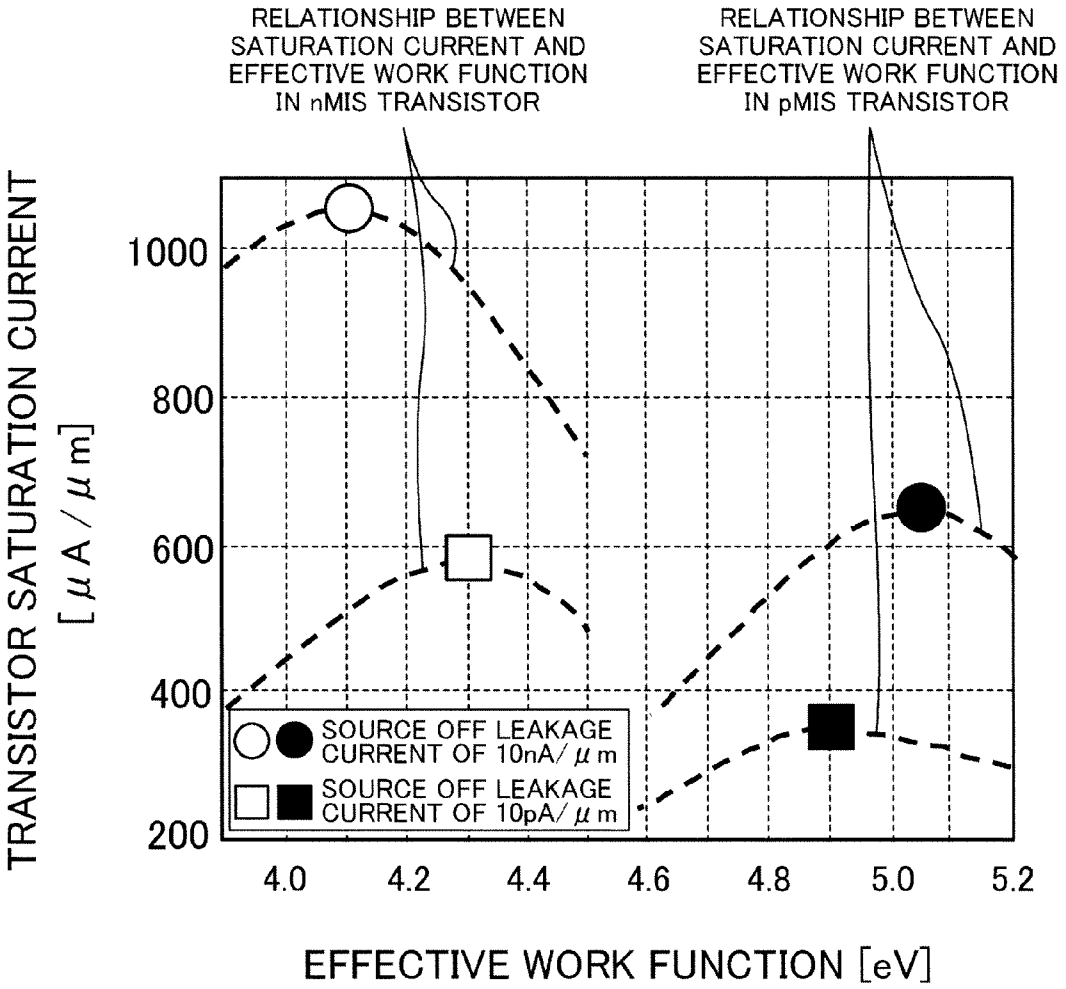


FIG.14


RELATIONSHIP BETWEEN SATURATION CURRENT AND EFFECTIVE WORK FUNCTION IN nMIS TRANSISTOR
RELATIONSHIP BETWEEN SATURATION CURRENT AND EFFECTIVE WORK FUNCTION IN pMIS TRANSISTOR
TRANSISTOR SATURATION CURRENT [μA/μm]
1000
800
600
400
200
SOURCE OFF LEAKAGE CURRENT OF 10nA/μm
SOURCE OFF LEAKAGE CURRENT OF 10pA/μm
4.0
4.2
4.4
4.6
4.8
5.0
5.2
EFFECTIVE WORK FUNCTION [eV]

SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation of PCT International Application PCT/JP2011/002868 filed on May 24, 2011, which claims priority to Japanese Patent Application No. 2010-205599 filed on Sep. 14, 2010. The disclosures of these applications including the specifications, the drawings, and the claims are hereby incorporated by reference in their entirety.

BACKGROUND

The present disclosure relates to semiconductor devices and methods for fabricating the same, and more particularly, to a metal insulator semiconductor (MIS) device including a gate insulating film formed on a semiconductor substrate and a gate electrode formed on the gate insulating film, and a method for fabricating the MIS device.

In order to meet the demands for increased speed and reduced power consumption of semiconductor integrated circuit devices, in respect of metal insulator semiconductor field-effect transistors (MISFET, hereinafter referred to as MIS transistors), progress has been made in reducing the thicknesses of gate insulating films. When silicon dioxide which has been conventionally used is formed into a thin film for the purpose of reducing the thickness of a gate insulating film, a gate leakage current caused by a tunnel current increases. Consequently, an attempt to prevent depletion of a gate electrode has been made. Specifically, the attempt has been carried out by reducing an equivalent oxide thickness (EOT) by means of use of, instead of the silicon dioxide film, a so-called high dielectric constant insulating film such as an HfO_2 film as the gate insulating film, and by employing a so-called metal inserted poly silicon (MIPS) structure in which a polysilicon film serving as a gate electrode and a gate insulating film sandwich a metal-containing film as part of the gate electrode (see, for example, T. Schram, et al., Novel Process To Pattern Selectively Dual Dielectric Capping Layers Using Soft-Mask Only, Symp. On VLSI technology, 44 (2008)). Note that the high dielectric constant insulating film refers to an insulating film having a relative dielectric constant of, for example, 8 or more, which is higher than that of a silicon nitride film.

A method for fabricating a conventional semiconductor device will be described below with reference to FIGS. **11-13**. This conventional semiconductor device includes a complementary metal insulator semiconductor (CMIS) device composed of an n-type MIS transistor and a p-type MIS transistor which are provided on an identical substrate. In this device, a gate insulating film is made of an HfO_2 film, and a gate electrode has a MIPS structure. FIGS. **11-13** are cross-sectional views (taken along a gate length direction) illustrating sequential steps of the method for fabricating the conventional semiconductor device. In FIGS. **11-13**, "nMIS transistor region" shown at the left refers to a region where the n-type MIS transistor is formed, and "pMIS transistor region" shown at the right refers to a region where the p-type MIS transistor is formed.

First, as shown in FIG. **11**, a pMIS transistor region and an nMIS transistor region are defined by selectively forming a shallow trench isolation **101** in an upper portion of a semiconductor substrate **100** of p-type silicon. Here, a portion of the semiconductor substrate **100** surrounded by the shallow trench isolation **101** and located in the pMIS transistor region serves as an active region **100***a*, and a portion of the semiconductor substrate **100** surrounded by the shallow trench isolation **101** and located in the nMIS transistor region serves as an active region **100***b*.

Next, an n-type well region **121**N is formed in the pMIS transistor region of the semiconductor substrate **100**, and a p-type well region **121**P is formed in the nMIS transistor region of the semiconductor substrate **100**. Thereafter, photolithography and dry etching are performed to form a gate electrode **123***a* on the active region **100***a* in the pMIS transistor region with a gate insulating film **122***a* interposed between the gate electrode **123***a* and the active region **100***a*. The photolithography and the dry etching also form a gate electrode **123***b* on the active region **100***b* in the nMIS transistor region with a gate insulating film **122***b* interposed between the gate electrode **123***b* and the active region **100***b*.

The gate insulating film **122***a* includes an interface layer **102***a* made of a silicon dioxide film, a high dielectric constant insulating film (hereinafter, referred to as a high-k film) **103***a* formed on the interface layer **102***a* and made of an HfO_2 film, and a pMIS cap film **104***a* formed on the high-k film **103***a*. The gate insulating film **122***b* includes an interface layer **102***b* made of a silicon dioxide film, a high-k film **103***b* formed on the interface layer **102***b* and made of an HfO_2 film, and an nMIS cap film **104***b* formed on the high-k film **103***b*. The pMIS cap film **104***a* and the nMIS cap film **104***b* enable control of a work function of each of the gate electrodes **123***a* and **123***b*.

The gate electrode **123***a* includes a metal film **106***a* and a polysilicon film **107***a* formed on the metal film **106***a*. The gate electrode **123***b* includes a metal film **106***b* and a polysilicon film **107***b* formed on the metal film **106***b*.

Next, as shown in FIG. **12**, extension regions **108***a* are formed at both sides of the gate electrode **123***a* by introducing a p-type impurity into the pMIS transistor region of the semiconductor substrate **100**, and extension regions **108***b* are formed at both sides of the gate electrode **123***b* by introducing an n-type impurity into the nMIS transistor region of the semiconductor substrate **100**.

After a silicon dioxide film and a silicon nitride film are sequentially deposited on the entire surface of the semiconductor substrate **100**, the deposited silicon nitride film and the deposited silicon dioxide film are subjected to anisotropic etching. Consequently, as shown in FIG. **13**, sidewall spacers **111***a* including a silicon dioxide film **109***a* and a silicon nitride film **110***a* are formed on both side surfaces of the gate electrode **123***a*, and sidewall spacers **111***b* including a silicon dioxide film **109***b* and a silicon nitride film **110***b* are formed on both side surfaces of the gate electrode **123***b*. Thereafter, source/drain regions **112***a* are formed at both sides of the gate electrode **123***a* sandwiched between the sidewall pacers **111***a* by introducing a p-type impurity into the pMIS transistor region of the semiconductor substrate **100**, and source/drain regions **112***b* are formed at both sides of the gate electrode **123***b* sandwiched between the sidewall pacers **111***b* by introducing an n-type impurity into the nMIS transistor region of the semiconductor substrate **100**. In this manner, the CMIS device is formed through the foregoing steps.

SUMMARY

Using the above CMIS device, transistors different in threshold voltage (Vth) can be formed in a semiconductor integrated circuit, and a semiconductor integrated circuit device with improved performance can be produced by employing a low-Vth transistor in a circuit requiring high-speed performance and a high-Vth transistor in a circuit requiring a reduced standby leakage current.

FIG. **14** shows a relationship between an effective work function and a saturation current in transistors. Specifically, in each transistor, an impurity in a transistor channel is adjusted to allow the saturation current to be maximized at each value of the effective work function which is varied. In FIG. **14**, the dashed lines indicate the saturation currents of the transistors corresponding to each of two different source off leakage currents.

As shown in FIG. **14**, the effective work function value at which a maximum saturation current is obtained in the nMIS transistor is different from the effective work function value at which a maximum saturation current is obtained in the pMIS transistor. FIG. **14** also shows that, even between transistors of the same conductivity type, a difference in the source off leakage current causes the saturation currents to be maximized at different effective work function values.

Note that the "effective work function" is a work function obtained from electrical characteristics of a MIS transistor. Specifically, the effective work function is obtained by incorporating influence such as a level in an insulating film into a work function related to physical properties and representing a difference between a vacuum level and an energy level of a metal. The "saturation current" shown in FIG. **14** corresponds to a driving current per gate width unit, and represents a driving force of each transistor.

Meanwhile, when an effective work function of an nMIS transistor is too low and an effective work function of a pMIS transistor is too high relative to desired source off leakage current and threshold voltage (Vth), a concentration of an impurity in a channel needs to be increased, and accordingly, a saturation current decreases. When an effective work function of an nMIS transistor is too high and an effective work function of a pMIS transistor is too low relative to desired source off leakage current and Vth, an insufficient amount of an impurity for regulating the Vth can be introduced into a channel. In such a case, subthreshold characteristic deteriorates, and accordingly, a saturation current decreases under conditions with a constant source off leakage current.

Accordingly, in a semiconductor integrated circuit device requiring two or more threshold voltages, gate structures having different work functions need to be formed in a single chip in order to maximize a transistor driving force at each threshold voltage.

However, the above-discussed method for fabricating the conventional semiconductor device allows nMIS transistors to have only one work function and pMIS transistors to have only one work function.

It is therefore an object of the present disclosure to enable formation of a plurality of transistors of the same conductivity type having different work functions in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film.

To achieve the object, the inventors of the present application studied methods for forming gate structures (a gate structure includes a stack of a gate insulating film and a gate electrode) having different work functions. Specifically, the inventors studied a method in which the thicknesses of an nMIS cap film and pMIS cap film are changed, and a method in which transistors were designed to have metal electrodes of different types. However, these methods were found not to be practical because they consisted of significantly increased number of steps.

As a result of further studies, the inventors have found the following. Thus, gate structures are allowed to have different work functions by increasing the thickness of an interface layer constituting the lowest layer of a gate insulating film by means of selective oxidation which is performed after formation of the gate structures.

Specifically, a semiconductor device of the present disclosure includes a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate, wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film, the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film, the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer, the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer, and the first interface layer has a thickness larger than that of the second interface layer.

In the semiconductor device of the present disclosure, the interface layer included in the gate insulating film of the first MIS transistor has a thickness larger than that of the interface layer included in the gate insulating film of the second MIS transistor which is of the same conductivity type as the first MIS transistor. Accordingly, since an EOT of the gate insulating film of the first MIS transistor increases, an effective work function of the first MIS transistor increases. Therefore, according to the present disclosure, a plurality of transistors of an identical conductivity type having different effective work functions can be formed in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film.

In the semiconductor device of the present disclosure, the first gate electrode may include first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers, the second gate electrode may include second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and the first insulating spacers may be thinner than the second insulating spacers. In this structure, after formation of the gate structures and before formation of the side spacers, the thickness of the interface layer included in the gate insulating film of the first MIS transistor can be increased by performing selective oxidation. In such a case, the first insulating spacers may be offset spacers each having an I-shaped cross section, and the second insulating spacers may be underlying spacers each having an L-shaped cross section. In addition, the first gate electrode may include a first metal-containing film formed on the first high dielectric constant insulating film and a first silicon film formed on the first metal-containing film, the second gate electrode may include a second metal-containing film formed on the second high dielectric constant insulating film and a second silicon film formed on the second metal-containing film, a silicon dioxide film may be interposed between the first silicon film and the first insulating spacers, and the second silicon film may be in contact with the second insulating spacers. Here, a first metal silicide layer may be formed on the first silicon film, and a second metal silicide layer may be formed on the second silicon film. Further, a silicon dioxide film may also be interposed between the first active region and the first side-

wall spacers. Furthermore, each of the first insulating spacers and the second insulating spacers may be made of a silicon nitride film.

In the semiconductor device of the present disclosure, the first and second MIS transistors may be pMIS transistors, and the first and second high dielectric constant insulating films may contain aluminum. In such a case, the first gate insulating film may further include a first cap film formed on the first high dielectric constant insulating film and containing aluminum, and the second gate insulating film may further include a second cap film formed on the second high dielectric constant insulating film and containing aluminum.

In the semiconductor device of the present disclosure, the first and second MIS transistors may be nMIS transistors, and the first and second high dielectric constant insulating films may contain lanthanum. In such a case, the first gate insulating film may further include a first cap film formed on the first high dielectric constant insulating film and containing lanthanum, and the second gate insulating film may further include a second cap film formed on the second high dielectric constant insulating film and containing lanthanum. The first and second high dielectric constant insulating films and the first and second cap films may contain, instead of lanthanum, dysprosium (Dy), scandium (Sc), or gadolinium (Gd).

In the semiconductor device of the present disclosure, each of the first and second high dielectric constant insulating films may contain hafnium or zirconium.

In the semiconductor device of the present disclosure, each of the first and second interface layers may be made of a silicon dioxide film.

In the semiconductor device of the present disclosure, the first and second high dielectric constant insulating films may be substantially equal in thickness. The first and second gate electrodes may be made of a substantially identical material. Thus, in the semiconductor device of the present disclosure, the first and second MIS transistors may have a substantially identical gate structure except for the thicknesses of the interface layers.

In the semiconductor device of the present disclosure, an effective work function of the first MIS transistor may be higher than an effective work function of the second MIS transistor.

A method for fabricating the semiconductor device of the present disclosure includes: a step (a) of forming an interface layer, a high dielectric constant insulating film, and a gate electrode material film in a sequential manner on a semiconductor substrate including a first active region and a second active region; a step (b) of patterning the gate electrode material film, the high dielectric constant insulating film, and the interface layer to form a first gate electrode of the gate electrode material film on the first active region with a first gate insulating film including the interface layer and the high dielectric constant insulating film and interposed between the first gate electrode and the first active region, and to form a second gate electrode of the gate electrode material film on the second active region with a second gate insulating film including the interface layer and the high dielectric constant insulating film and interposed between the second gate electrode and the second active region; and the step (c) of increasing the thickness of the interface layer of the first gate insulating film in a selective manner, after the step (b).

According to the method for fabricating the semiconductor device of the present disclosure, the thickness of the interface layer of the first MIS transistor is selectively increased. Consequently, the EOT of the gate insulating film of the first MIS transistor increases, and the effective work function of the first MIS transistor increases. Therefore, a plurality of transistors of an identical conductivity type and different from each other in effective work function can be formed in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film.

In the method for fabricating the semiconductor device of the present disclosure, the step (c) may include a step where, after covering the first and second gate electrodes with an insulating film, a portion of the insulating film covering the first gate electrode is selectively etched, and then, the interface layer of the first gate insulating film is selectively oxidized to increase in thickness. This step ensures that the thickness of the interface layer included in the gate insulating film of the first MIS transistor is selectively increased. In such a case, the insulating film covering the first and second gate electrodes may be a silicon nitride film, for example. A heat treatment or a plasma treatment may be performed in an oxygen-containing atmosphere to increase the thickness of the interface layer included in the gate insulating film of the first MIS transistor in a selective manner. In addition, the gate electrode material film may include a metal-containing film formed on the high dielectric constant insulating film and a silicon film formed on the metal-containing film. In the step (c), a silicon dioxide film may be formed to be interposed between the insulating film remaining on the side surfaces of the first gate electrode and the silicon film of the first gate electrode.

The method for fabricating the semiconductor device of the present disclosure may include a step of forming a cap film containing a metal for adjusting a threshold voltage (Vth) on the high dielectric constant insulating film between formation of the high dielectric constant insulating film and formation of the gate electrode material film.

As described above, the present disclosure enables formation of a plurality of transistors of the same conductivity type and different from each other in work function in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film. Therefore, the present disclosure is useful as a semiconductor device having a CMIS structure including a plurality of MIS transistors different in threshold voltage (Vth), and for fabricating the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view (taken along a gate length direction) illustrating a step of a method for fabricating a semiconductor device according to an embodiment of the present disclosure.

FIG. **2** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **3** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **4** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **5** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **6** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **7** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **8** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **9** is a cross-sectional view (taken along a gate length direction) illustrating a step of the method for fabricating the semiconductor device according to the embodiment of the present disclosure.

FIG. **10** is a graph showing a relationship between an equivalent oxide thickness (EOT) and a transistor effective work function of a semiconductor device of an embodiment.

FIG. **11** shows a cross-sectional view (taken along a gate length direction) illustrating a steps of a method for fabricating a conventional semiconductor device.

FIG. **12** shows a cross-sectional view (taken along a gate length direction) illustrating a steps of the method for fabricating the conventional semiconductor device.

FIG. **13** shows a cross-sectional view (taken along a gate length direction) illustrating a steps of the method for fabricating the conventional semiconductor device.

FIG. **14** is a graph showing a relationship between an effective work function and a saturation current of a transistor in which a channel dose is changed whereas a source off leakage current is kept constant.

DETAILED DESCRIPTION

A semiconductor device according to an embodiment of the present disclosure and a method for fabricating the same are described with reference to the drawings.

FIGS. **1-9** are cross-sectional views (taken along a gate length direction) illustrating steps of the method for fabricating a semiconductor device of this embodiment. Note that each of FIGS. **1-9** shows, in the order from right to left, the following regions: "First pMIS transistor region" referring to a region where a first pMIS transistor is to be formed, "Second pMIS transistor region," referring to a region where a second pMIS transistor is to be formed, "First nMIS transistor region" referring to a region where a first nMIS transistor is to be formed, and "Second nMIS transistor region" referring to a region where a second nMIS transistor is to be formed.

In this embodiment, for example, the first pMIS transistor and the second nMIS transistor are used as low-Vth (e.g., 0.1-0.25 V) transistors which are required for high-speed performance, and the second pMIS transistor and the first nMIS transistor are used as high-Vth (e.g., 0.35-0.5 V) transistors which are required for reducing a standby leakage current.

First, as shown in FIG. **1**, pMIS transistor regions and nMIS transistor regions are defined by selectively forming an isolation region **1** made of, for example, a shallow trench filled with a silicon dioxide film in an upper portion of a semiconductor substrate **50** of, for example, p-type silicon. Here, a portion of the semiconductor substrate **50** surrounded by the isolation region **1** and located in the first pMIS transistor region serves as an active region **50***a*, and a portion of the semiconductor substrate **50** surrounded by the isolation region **1** and located in the second pMIS transistor region serves as an active region **50***b*. A portion of the semiconductor substrate **50** surrounded by the isolation region **1** and located in the first nMIS transistor region serves as an active region **50***c*, and a portion of the semiconductor substrate **50** surrounded by the isolation region **1** and located in the second nMIS transistor region serves as an active region **50***d*.

Next, an n-type well region **51**N is formed by introducing an n-type impurity such as arsenic into the first and second pMIS transistor regions of the semiconductor substrate **50** by means of ion implantation. A p-type well region **51**P is formed by introducing a p-type impurity such as boron into the first and second nMIS transistor regions of the semiconductor substrate **50** by means of ion implantation. The concentrations of the n-type impurity may be different between the pMIS transistor region and the second pMIS transistor region. The concentration of the p-type impurity may be different between the first nMIS transistor region and the second nMIS transistor region.

Thereafter, an interface layer **2** with a thickness of about 0.8 nm of, for example, a silicon dioxide film and a high dielectric constant insulating film (a high-k film) **3** with a thickness of about 1.2 nm including, for example, Hf or Zr and O are sequentially formed on the semiconductor substrate **50** including the MIS transistor regions.

A pMIS cap film **4** including, for example, aluminum (Al) and oxygen (O) is formed on the high-k film **3**, and then, a portion of the pMIS cap film **4** covering the first and second nMIS transistor regions is removed. Subsequently, an nMIS cap film **4'** including, for example, lanthanum (La) and O is formed on the high-k film **3** and the pMIS cap film **4**, and then, a portion of the nMIS cap film **4'** covering the first and second pMIS transistor region is removed. The pMIS cap film **4** includes, for example, Al as a regulator metal capable of increasing effective work functions of the pMIS transistors. The nMIS cap film **4'** includes, for example, La as a regulator metal capable of increasing effective work functions of the nMIS transistors.

A metal-containing film **6** with a thickness of about 5 nm including, for example, N and a metal such as Ti, Ta or Ru, and a silicon film **7** with a thickness of about 60 nm of, for example, polysilicon are sequentially formed on the pMIS cap film **4** and the nMIS cap film **4'**.

Next, the silicon film **7**, the metal-containing film **6**, the pMIS cap film **4**, the nMIS cap film **4'**, the high-k film **3**, and the interface layer **2** are subjected to photolithography and dry etching to be patterned. The photolithography and dry etching form the structure shown in FIG. **2**. Specifically, a gate electrode **53***a* is formed on the active region **50***a* in the first pMIS transistor region with a gate insulating film **52***a* interposed between the gate electrode **53***a* and the active region **50***a*. A gate electrode **53***b* is formed on the active region **50***b* in the second pMIS transistor region with a gate insulating film **52***b* interposed between the gate electrode **53***b* and the active region **50***b*. A gate electrode **53***c* is formed on the active region **50***c* in the first nMIS transistor region with a gate insulating film **52***c* interposed between the gate electrode **53***c* and the active region **50***c*. A gate electrode **53***d* is formed on the active region **50***d* in the second nMIS transistor region with a gate insulating film **52***d* interposed between the gate electrode **53***d* and the active region **50***d*.

The gate insulating film **52***a* includes an interface layer **2***a*, a high-k film **3***a*, and a pMIS cap film **4***a*. The gate insulating film **52***b* includes an interface layer **2***b*, a high-k film **3***b*, and a pMIS cap film **4***b*. The gate insulating film **52***c* includes an interface layer **2***c*, a high-k film **3***c*, and an nMIS cap film **4***c*. The gate insulating film **52***d* includes an interface layer **2***d*, a high-k film **3***d*, and an nMIS cap film **4***d*.

The gate electrode **53***a* includes a metal-containing film **6***a* and a silicon film **7***a*. The gate electrode **53***b* includes a metal-containing film **6***b* and a silicon film **7***b*. The gate electrode **53***c* includes a metal-containing film **6***c* and a silicon film **7***c*. The gate electrode **53***d* includes a metal-containing film **6***d* and a silicon film **7***d*.

Next, as shown in FIG. **3**, an insulating film **8** with a thickness of about 6 nm of, for example, a silicon nitride film is formed on the entire surface of the semiconductor substrate **50** inclusive of the upper surfaces of the gate electrodes **53***a*, **53***b*, **53***c* and **53***d*.

Using a resist pattern (not shown) which exposes the second pMIS transistor region, a p-type impurity such as boron is introduced into the semiconductor substrate **50** by means of ion implantation. Consequently, as shown in FIG. **4**, p-type extension regions **9***b* are formed under both sides of the gate electrode **53***b* in the active region **50***b*. The resist pattern is removed after formation of the p-type extension regions **9***b*. Here, concerning conditions of the ion implantation, an implantation energy is 0.8 keV and a dose is 1×10^{15} cm^{-2}, for example. Germanium (Ge) and carbon (C) may be implanted in the second pMIS transistor region of the semiconductor substrate **50** before the ion implantation of the p-type impurity such as boron. In such a case, Ge may be implanted, for example, at an implantation energy of 5 keV and a dose of 5×10^{14} cm^{-2}, and C may be implanted, for example, at an implantation energy of 2 keV and a dose of 5×10^{14} cm^{-2}.

Next, using a resist pattern (not shown) which exposes the second nMIS transistor region, an n-type impurity such as arsenic is introduced into the semiconductor substrate **50** by means of ion implantation. Consequently, n-type extension regions **9***d* are formed under both sides of the gate electrode **53***d* in the active region **50***d*. The resist pattern is removed after formation of the n-type extension regions **9***d*. Here, concerning conditions of the ion implantation, an implantation energy is 1.2 keV and a dose is 1×10^{15} cm^{-2}, for example. Ge and C may be implanted in the second nMIS transistor region of the semiconductor substrate **50** before the ion implantation of the n-type impurity such as arsenic. In such a case, Ge may be implanted, for example, at an implantation energy of 5 keV and a dose of 5×10^{14} cm^{-2}, and C may be implanted, for example, at an implantation energy of 2 keV and a dose of 5×10^{14} cm^{-2}.

As shown in FIG. **5**, after forming a resist pattern **11** covering the second pMIS transistor region and the second nMIS transistor region by photolithography, the insulting film **8** is subjected to dry etching with the resist pattern **11** used as a mask. This dry etching forms offset spacers **8***a* each having an I-shaped cross-section on the side surfaces of the gate electrode **53***a* located in the first pMIS transistor region, and offset spacers **8***c* each having an I-shaped cross-section on the side surfaces of the gate electrode **53***c* located in the first nMIS transistor region. In this step, each of the offset spacers **8***a* and **8***c* has a thickness of about 2.5 nm, which is smaller than the original thickness (e.g., about 6 nm) of the insulating film **8**.

After removing the resist pattern **11**, the semiconductor substrate **50** is subjected to an oxidation treatment in, for example, plasma composed of a gas containing oxygen and at, for example, about 400° C. Consequently, as shown in FIG. **6**, the thickness of the interface layer **2***a* of the gate insulating film **52***a* in the first pMIS transistor region increases, from both sides thereof, by about 0.3 nm, and the thickness of the interface layer **2***c* of the gate insulating film **52***c* in the first nMIS transistor region increases, from both sides thereof, by about 0.3 nm. These interface layers with the increased thickness are denoted by reference characters **2**A and **2**C, respectively. Even after the thick interface layers **2**A and **2**C are formed, the thicknesses of the high-k films **3***a* and **3***c* remain substantially unchanged. Thus, each of the high-k films **3***a*, **3***b*, **3***c*, and **3***d* continues to have substantially the same thickness after the thick interface layers **2**A and **2**C are formed.

Further, in the step shown in FIG. **6**, a silicon dioxide film **13***a* with a thickness of about 0.3 nm is formed on the upper surface and the side surfaces of the silicon film **7***a* of the gate electrode **53***a* located in the first pMIS transistor region. A silicon dioxide film **13***c* with a thickness of about 0.3 nm is also formed on the upper surface and the side surfaces of the silicon film **7***c* of the gate electrode **53***c* located in the first nMIS transistor region. Specifically, the resultant silicon dioxide film **13***a* is interposed between the silicon film **7***a* of the gate electrode **53***a* located in the first pMIS transistor region and the offset spacers **8***a*, and the resultant silicon dioxide film **13***c* is interposed between the silicon film **7***c* of the gate electrode **53***c* located in the first nMIS transistor region and the offset spacers **8***c*. In addition, a silicon dioxide film **13***a* with a thickness of about 0.3 nm is also formed on the surfaces of portions of the active region **50***a* located at both sides of the gate electrode **53***a*, and a silicon dioxide film **13***c* with a thickness of about 0.3 nm is also formed on the surfaces of portions of the active region **50***c* located at both sides of the gate electrode **53***c*.

The interface layer **2***a* of the gate insulating film **52***a* and side portions of the silicon film **7***a* of the gate electrode **53***a* are oxidized by oxygen having passed through the offset spacers **8***a*, and the interface layer **2***c* of the gate insulating film **52***c* and side portions of the silicon film **7***c* of the gate electrode **53***c* are oxidized by oxygen having passed through the offset spacers **8***c*.

On the other hand, in the step shown in FIG. **6**, since the gate structures of the second pMIS transistor region and the second nMIS transistor region are covered by the insulating film **8** having a thickness of about 6 nm, the interface layer **2***b* of the gate insulating film **52***b* located in the second pMIS transistor region and the interface layer **2***d* of the gate insulating film **52***d* located in the second nMIS transistor region do not increase in thickness.

The interface layers **2***a* and **2***c* are oxidized through the treatment carried out using plasma in an oxygen-containing atmosphere in this embodiment. Alternatively, a heat treatment at about 600° C. in an oxygen-containing atmosphere may be performed.

Using a resist pattern (not shown) which exposes the first pMIS transistor region, a p-type impurity such as boron is introduced into the semiconductor substrate **50** by means of ion implantation. Consequently, as shown in FIG. **7**, p-type extension regions **9***a* are formed under both sides of the gate electrode **53***a* in the active region **50***a*. The resist pattern is removed after formation of the p-type extension regions **9***a*. Here, concerning conditions of the ion implantation, an implantation energy is 0.8 keV and a dose is 1×10^{15} cm^{-2}, for example. Ge and C may be implanted in the first pMIS transistor region of the semiconductor substrate **50** before the ion implantation of the p-type impurity such as boron. In such a case, Ge may be implanted, for example, at an implantation energy of 5 keV and a dose of 5×10^{14} cm^{-2}, and C may be implanted, for example, at an implantation energy of 2 keV and a dose of 5×10^{14} cm^{-2}.

Next, using a resist pattern (not shown) which exposes the first nMIS transistor region, an n-type impurity such as arsenic is introduced into the semiconductor substrate **50** by means of ion implantation. Consequently, n-type extension regions **9***c* are formed under both sides of the gate electrode **53***c* in the active region **50***c*. The resist pattern is removed

after formation of the n-type extension regions **9***c*. Here, concerning conditions of the ion implantation, an implantation energy is 1.2 keV and a dose is 1×10^{15} cm^{-2}, for example. Ge and C may be implanted in the first nMIS transistor region of the semiconductor substrate **50** before the ion implantation of the n-type impurity such as arsenic. In such a case, Ge may be implanted, for example, at an implantation energy of 5 keV and a dose of 5×10^{14} cm^{-2}, and C may be implanted, for example, at an implantation energy of 2 keV and a dose of 5×10^{14} cm^{-2}.

A silicon dioxide film and a silicon nitride film are sequentially deposited on the entire surface of the semiconductor substrate **50**, and then, the deposited silicon nitride film and the deposited silicon dioxide film are etched back. Consequently, as shown in FIG. **8**, sidewall spacers **18***a*, **18***b*, **18***c*, and **18***d* are formed on both sides of the gate electrodes **53***a*, **53***b*, **53***c*, and **53***d*, respectively. Each of the sidewall spacers **18***a* includes an inner sidewall spacer **16***a* of a silicon dioxide film with an L-shaped cross section and an outer sidewall spacer **17***a* of a silicon nitride film formed on the inner sidewall spacer **16***a*. Each of the sidewall spacers **18***b* includes an inner sidewall spacer **16***b* of a silicon dioxide film with an L-shaped cross section and an outer sidewall spacer **17***b* of a silicon nitride film formed on the inner sidewall spacer **16***b*. Each of the sidewall spacers **18***c* includes an inner sidewall spacer **16***c* of a silicon dioxide film with an L-shaped cross section and an outer sidewall spacer **17***c* of a silicon nitride film formed on the inner sidewall spacer **16***c*. Each of the sidewall spacers **18***d* includes an inner sidewall spacer **16***d* of a silicon dioxide film with an L-shaped cross section and an outer sidewall spacer **17***d* of a silicon nitride film formed on the inner sidewall spacer **16***a*

In the step shown in FIG. **8**, the insulating film **8** remaining in the second pMIS transistor region and the second nMIS transistor region is also etched back. Consequently, an underlying spacer **8***b* with an L-shaped cross section is formed between the gate electrode **53***b* and an associated one of the sidewall spacers **18***b* (the inner sidewall spacers **16***b*). At the same time, an underlying spacer **8***d* with an L-shaped cross section is formed between the gate electrode **53***d* and an associated one of the sidewall spacers **18***d* (the inner sidewall spacers **16***d*). The underlying spacers **8***b* are in contact with the silicon film **7***b* of the gate electrode **53***b*. The underlying spacers **8***d* are in contact with the silicon film **7***d* of the gate electrode **53***d*. The thicknesses of the underlying spacers **8***b* and **8***d* are approximately the same as the original thickness (e.g., about 6 nm) of the insulating film **8**, and larger than the thicknesses (e.g., about 2.5 nm) of the offset spacers **8***a* and **8**.

In the step shown in FIG. **8**, the silicon dioxide film **13***a* present on the upper face of the gate electrode **53***a* and on the active region **50***a* and the silicon dioxide film **13***c* present on the upper face of the gate electrode **53***c* and on the active region **50***c* are also etched back. Consequently, the offset spacers **8***a* and the remaining silicon dioxide film **13***a* are interposed between the side surfaces of the gate electrode **53***a* and the sidewall spacers **18***a*, and the remaining silicon dioxide film **13***a* is also interposed between the active region **50***a* (the p-type extension regions **9***a*) and the sidewall spacers **18***a*. The offset spacers **8***c* and the remaining silicon dioxide film **13***c* are interposed between the side surfaces of the gate electrode **53***c* and the sidewall spacers **18***c*, and the remaining silicon dioxide film **13***c* is also interposed between the active region **50***c* (p-type extension regions **9***c*) and the sidewall spacers **18***c*.

Using a resist pattern (not shown) which exposes the first and second pMIS transistor regions, a p-type impurity such as boron is introduced into the semiconductor substrate **50** by means of ion implantation. Consequently, as shown in FIG. **9**, p-type source/drain regions **19***a* are formed under the outer sides of the sidewall spacers **18***a* in the active region **50***a*, and p-type source/drain regions **19***b* are formed under the outer sides of the sidewall spacers **18***b* in the active region **50***b*. The resist pattern is removed after formation of the p-type source/drain regions **19***a* and **19***b*. Here, concerning conditions of the ion implantation, an implantation energy is 1.6 keV and a dose is 1×10^{15} cm^{-2}, for example. Ge may be implanted in the first and second pMIS transistor regions of the semiconductor substrate **50** before the ion implantation of the p-type impurity such as boron. In such a case, Ge may be implanted, for example, at an implantation energy of 10 keV and a dose of 5×10^{15} cm^{-2}.

Next, using a resist pattern (not shown) which exposes the first and second nMIS transistor regions, an n-type impurity such as arsenic is introduced into the semiconductor substrate **50** by means of ion implantation. Consequently, n-type source/drain regions **19***c* are formed under the outer sides of the sidewall spacers **18***c* in the active region **50***c*, and n-type source/drain regions **19***d* are formed under the outer sides of the sidewall spacers **18***d* in the active region **50***d*. The resist pattern is removed after formation of the n-type source/drain regions **19***c* and **19***d*. Here, concerning conditions of the ion implantation, an implantation energy is 10 keV and a dose is 1×10^{15} cm^{-2}, for example.

Thereafter, annealing is performed at about 1000° C., thereby activating the impurities which have been introduced by means of ion implantation. In this step, Al contained in the pMIS cap films **4***a* and **4***b* diffuses into the high-k films **3***a* and **3***b*. These Al-containing high-k films are denoted by reference characters **3**A and **3**C, respectively. At the same time, La contained in the nMIS cap films **4***c* and **4***d* diffuses into the high-k films **3***c* and **3***d*. These La-containing high-k films are denoted by reference characters **3**C and **3**D, respectively.

After a metal film of, for example, Ni is deposited on the entire surface of the semiconductor substrate **50**, annealing is performed at about, for example, 260° C. The surface portions of the silicon films **7***a*, **7***b*, **7***c*, and **7***c* of the gate electrodes **53***a*, **53***b*, **53***c*, and **53***d*, the surface portions of the p-type source/drain regions **19***a* and **19***b*, and the surface portions of the n-type source/drain regions **19***c* and **19***d* are caused to react with the deposited metal film to form metal silicide layers **20***a*, **20***b*, **20***c*, and **20***d*. Thereafter, unreacted portions of the metal film are removed. A CMIS structure is formed through the above steps.

FIG. **10** shows the relationship between an equivalent oxide thickness (EOT) and an effective work function of each of the transistors of this embodiment. As shown in FIG. **10**, the first pMIS transistor and the first nMIS transistor, because of the thick interface layers **2**A and **2**C, show an increase in equivalent oxide thickness and an increase in effective work function, compared to the second pMIS transistor and the second nMIS transistor. Reason for the increases in equivalent oxide thickness and effective work function will be discussed below.

For example, a heat treatment performed in a step causes oxygen contained in a high-k film including, for example, HfO_2 to diffuse and escape from the high-k film. Accordingly, an interface dipole is formed between the high-k film and an interface layer. Formation of the dipole is considered to cause effective work functions to decrease in the both of a pMIS transistor and an nMIS transistor.

On the other hand, as described in the step shown in FIG. **6**, in respect of the first pMIS transistor and the first nMIS transistor, the gate electrodes **53***a* and **53***c* are exposed to an oxidation atmosphere with both sides surfaces covered with

the thin offset spacers **8***a* and **8***c*. Accordingly, the interface layers **2***a* and **2***c* increase in thickness to be denoted by reference characters **2**A and **2**C. The interface layers **2**A and **2**C containing sufficient oxygen supply a sufficient amount of oxygen to the high-k films **3***a* and **3***c* (in which the metal have not yet diffused from the cap films), thereby reducing detachment of oxygen from the high-k films **3***a* and **3***c*. As a result, the dipole is unlikely to be formed, and the effective work function of each of the first pMIS transistor and the first nMIS transistor can be set high.

In the first nMIS transistor with a high effective work function, a source off leakage current is reduced since a threshold voltage (Vth) increases. Thus, the first nMIS transistor can be used for reducing a leakage current. In the first pMIS transistor with a high effective work function, a driving force increases since a threshold voltage (Vth) decreases. Thus, the first pMIS transistor can be used for increasing the driving force.

As described above, in this embodiment, the interface layer **2***a* included in the gate insulating film **52***a* of the first pMIS transistor and the interface layer **2***c* included in the gate insulating film **52***c* of the first nMIS transistor are selectively increased in thickness. Accordingly, the EOT of the gate insulating film **52***a* of the first pMIS transistor and that of the gate insulating film **52***c* of the first nMIS transistor increase, thereby causing the effective work functions of the first pMIS transistor and the first nMIS transistor to increase. As a result, a plurality of MIS transistors of the same conductivity type and different from each other in work function can be provided in a semiconductor device with a MIS structure in which a high-k film is used as a gate insulating film. In an integrated circuit which is thus allowed to include a plurality of MIS transistors having different work functions, a driving force can be maximized in each of the low-Vth MIS transistors and the high-Vth transistors, thereby enabling the integrated circuit to operate at a high speed with a low leakage current.

In this embodiment, a silicon dioxide film is formed as the interface layer **2***a* (**2**A), **2***b*, **2***c* (**2**C), and **2***d*. Alternatively, a silicon oxynitride film may be formed.

In this embodiment, the pMIS cap films **4***a* and **4***b* and the nMIS cap films **4***c* and **4***d* are allowed to remain in the final structure of the semiconductor device. However, the Al-containing high-k films **3**A and **3**B and the La-containing high-k films **3**C and **3**D are essential for the final structure, and it is not always necessary to allow the pMIS cap films **4***a* and **4***b* and the nMIS cap films **4***c* and **4***d* to remain in the final structure. For example, if an Al-containing film and a La-containing film are formed before formation of the metal-containing film **6** in the step shown in FIG. **1**, the pMIS cap film **4** and the nMIS cap film **4'** do not need to remain when the metal-containing film **6** is formed.

In this embodiment, a cap film containing La is used as the nMIS cap film **4'**. Alternatively, a cap film containing, for example, dysprosium (Dy), scandium (Sc), or gadolinium (Gd) may be used.

The MIS transistors of this embodiment have substantially the same gate structure (except for the thicknesses of the interface layers). Alternatively, the MIS transistors may have cap films with different thicknesses or gate electrodes made of different materials, for example.

What is claimed is:

1. A semiconductor device comprising:

a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,

wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,

the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,

the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,

the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,

the first interface layer has a thickness larger than that of the second interface layer, and

each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.

2. The semiconductor device of claim **1**, wherein

the first gate electrode includes first sidewall spacers formed on side surfaces thereof and first insulating spacers interposed between the first gate electrode and the first sidewall spacers,

the second gate electrode includes second sidewall spacers formed on side surfaces thereof and second insulating spacers interposed between the second gate electrode and the second sidewall spacers, and

the first insulating spacers are thinner than the second insulating spacers.

3. The semiconductor device of claim **2**,

the first insulting spacers are offset spacers each having an I-shaped cross section, and

the second insulating spacers are underlying spacers each having an L-shaped cross section.

4. The semiconductor device of claim **2**, wherein

the first gate electrode includes a first metal-containing film formed on the first high dielectric constant insulating film and a first silicon film formed on the first metal-containing film,

the second gate electrode includes a second metal-containing film formed on the second high dielectric constant insulating film and a second silicon film formed on the second metal-containing film,

a silicon dioxide film is interposed between the first silicon film and the first insulating spacers, and

the second silicon film is in contact with the second insulating spacers.

5. The semiconductor device of claim **4**, wherein

a first metal silicide layer is formed on the first silicon film, and

a second metal silicide layer is formed on the second silicon film.

6. The semiconductor device of claim **4**, wherein a silicon dioxide film is also interposed between the first active region and the first sidewall spacers.

7. The semiconductor device of claim **2**, wherein each of the first insulating spacers and the second insulating spacers is made of a silicon nitride film.

8. The semiconductor device of claim **1**, wherein

the first and second MIS transistors are pMIS transistors, and

the first and second high dielectric constant insulating films contain aluminum.

9. The semiconductor device of claim **8**, wherein

the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum, and

the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum.

10. The semiconductor device of claim **1**, wherein

the first and second MIS transistors are nMIS transistors, and

the first and second high dielectric constant insulating films contain lanthanum.

11. The semiconductor device of claim **10**, wherein

the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum, and

the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum.

12. The semiconductor device of claim **1**, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.

13. The semiconductor device of claim **1**, wherein the first and second high dielectric constant insulating films are equal in thickness.

14. The semiconductor device of claim **1**, wherein the first and second gate electrodes are made of an identical material.

15. The semiconductor device of claim **1**, wherein an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.

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