

Jakub T. Kedzierski

E-mail: jakub@ll.mit.edu

Education

- 1995-2001 **University of California, Berkeley** *(Berkeley, CA)*
Received M.S., and Ph.D. degrees from the Department of Electrical Engineering and Computer Sciences with a specialization in Solid State Devices and Silicon Processing.
- 1992-1995 **The Ohio State University** *(Columbus, OH)*
Received B.S. degree from the Department of Electrical Engineering.
Graduated Summa Cum Laude with 3.78 GPA

Work Experience

- 2005-current **MIT Lincoln Laboratory** *(Lexington, MA)*
Senior Staff – Advanced Materials and Microsystems Group
Research Milestones: Highest performance top-gated graphene transistors (2007).
Design of subthreshold operation FDSOI technology (2006-2012).
Lowest voltage electrowetting behavior (2006) Electrowetting on inorganic dielectrics (2010). Microfluidic pyrosequencing (2010). Microhydraulic Electrowetting Actuators (2014). Microhydraulic Stepping Actuators (2016).
- 2012 On leave from MIT to serve as a **visiting professor** at the Indian Institute of Technology Bombay (**IITB**) for spring and fall semesters – Taught Nanoelectronics EE724 and a course on experimental methods in nanotechnology. Delivered over a dozen invited seminars on nanoelectronics in India, Malaysia and Singapore.
- 2001-2005 **IBM T. J. Watson Research Center** *(Yorktown Heights, NY)*
Research Staff Member – Advanced Silicon Technology Group
Research Milestones: Utilizing angled extensions and selective epitaxy raised source drains to fabricate the highest performance double-gate devices (2001). Developing of two methods for silicide gate workfunction engineering (2002). The first demonstration of scaled, undoped-body, dual workfunction metal-gate FinFET devices with high mobility and performance (2002). Physical analysis of silicide induced impurity segregation for workfunction control of silicide gates (2003). Demonstration of a scaled high performance metal-gate FDSOI device architecture (2003).
- 1995-2001 **University of California, Berkeley** *(Berkeley, CA)*
Fall 96 - Spring 01 - Graduate Student Researcher
Research Milestones: Co-inventor of the FinFET electronic device (1998). Fabrication of 5nm Si nanowires (1997). Demonstration of semiconductor nanowire transistors (1999). Developing a complementary silicide technology and utilizing it to fabricate sub-20nm NMOS and PMOS transistors without the use of doping in source, drain or body (2000).
Fall 95 - Spring 96 - Graduate Student Instructor for Electromagnetics Course (117A)

Personal Information

Date of Birth: March 1, 1973; Place of Birth: Warsaw, Poland; Immigrated to the US: November 1983; Obtained US citizenship: March 7, 1992;

Consulting/Teaching Experience

2019 Short course on Nanoelectronics (Singapore)
2019 Short course on Nanoelectronics (Kuala Lumpur, Malaysia)
2018 Short course on Nanoelectronics (Singapore)
2018 Short course on Nanoelectronics (Penang, Malaysia)
2017 Short course on Nanoelectronics (Singapore)
2017 Short course on Nanoelectronics (Penang, Malaysia)
2017 Consulting work on FinFET related patent dispute
2016 Consulting work on FinFET related patent dispute (GBH Intellect)
2013 Short course on Nanoelectronics (Kulim, Malaysia)
2012 Semester course on Experimental Methods in Electronics Research (IITB Mumbai, India)
2012 Semester course on Nanoelectronics (IITB Mumbai, India)
2012 Short course on Nanoelectronics (UKM Malaysia)

Honors

- 1) Antarctica Service Medal (National Science Foundation, 1992)
- 2) OSU University Honors Scholarship (1992)
- 3) Frank Louise Orton Caldwell Scholarship (1992)
- 4) W. Carl Townsend Memorial Engineering Scholarship (1993)
- 5) University Honors Scholarship (1994)
- 6) Intel Graduate Student Fellowship (1998-1999)
- 7) Demetri Angelakos Award – for research assistance given to fellow graduate students (2000)
- 8) DARPA Most Significant Research Project Award – for work on the FinFET (Awarded to Project Principal Investigators: Chenming Hu, Tsu-Jae King, Jeffrey Bokor) (2000)
- 9) 2002 EDS Paul Rappaport Award – For best 2002 *Trans. Electr. Dev.* paper (2003)
- 10) ECS SOI 2003 session co-chair (2003)
- 11) IEDM 2003 process technology committee member (2003-2004)
- 12) VLSI 2005 rump session on metal gates
- 13) NSF Review panel for graphene electronics (2009)
- 14) 2009 EDS George E. Smith Award – For best 2009 *Elec. Dev. Letters* paper (2009)
- 15) 2012 Visiting Professor at the Indian Institute of Technology Bombay
- 16) MIT LL 2016 Best Paper Award – For best paper published by MIT Lincoln Laboratory in 2016
- 17) 2021 Recipient of the RD 100 award for Microhydraulic Motor invention

Publications

- 1) *Multilayer microhydraulic actuators with speed and force configurations*, Jakub Kedzierski, Hero Chea, *Nature Microsystems and Nanoengineering (cover article)*, **7**, 22 (2021)
- 2) *Linear and Rotational Microhydraulic Actuators Driven by Electrowetting*, Jakub Kedzierski, Eric Holihan, *Science Robotics (cover article)*, **3**, 22, (2018)
- 3) *Re-engineering Artificial Muscle with Microhydraulics*, Jakub Kedzierski, Eric Holihan, Rafmag Cabrera, Isaac Weaver, *Nature Microsystems and Nanoengineering*, **3**, 17016 (2017)
- 4) *Microhydraulic Electrowetting Actuators*, Jakub Kedzierski, Kevin Meng, Shaun Berry, Todd Thorsen, Rafmag Cabrera, *Journal of Microelectromechanical Systems*, **25**, 394 (2016)
- 5) *Validation of the trapped charge model of electrowetting contact angle saturation on lipid bilayers*, Jakub Kedzierski, Richa Barta, Shaun Berry, Ingrid Guha, and Behrouz Abedian, *Journal of Applied Physics*, **114**, 024901 (2013)
- 6) *Cyclic Compression and Decompression of a Lipid Bilayer*, Ingrid Guha, Jakub Kedzierski, and Behrouz Abedian, *Journal of Physical Chemistry B*, **117** (28), pp. 8469 (2013)
- 7) *Electrical conductance across self-assembled lipid bilayers*, Ingrid Guha, Jakub Kedzierski, and Behrouz Abedian, *Journal of Applied Physics*, **113**, 054301 (2012)

- 8) *A Glucose Fuel Cell for Implantable Brain–Machine Interfaces*, Rappaport BI, Kedzierski JT, Sarpeshkar R (2012) PLoS ONE 7(6): e38436.doi:10.1371/journal.pone.0038436
- 9) *Low-voltage electrowetting on a lipid bilayer formed on hafnium oxide*, Ingrid Guha, Jakub Kedzierski, Behrouz Abedian, *Applied Physics Letters*, v. 99, n. 2, July 11 2011
- 10) *Work-function-tuned TiN metal gate FDSOI transistors for subthreshold operation*, Steven Vitale, Jakub Kedzierski, Paul Healey, Peter Wyatt, and Craig Keast, *IEEE Transactions on Electron Devices*, v. 58, n. 2, p. 419-426, February 2011
- 11) *Improvement of SOI MOSFET RF performance by implant optimization*, Chen, C.L.; Knecht, J.M.; Kedzierski, J.; Chen, C.K.; Gouker, P.M.; Yost, D.-R.; Healey, P.; Wyatt, P.W.; Keast, C.L. *IEEE Microwave and Wireless Components Letters*, v 20, n 5, p 271-273, May 2010
- 12) *FDSOI metal gate transistors for ultra low power subthreshold operation*, Steven Vitale, Jakub Kedzierski, Peter Wyatt, Matt Renzi, Craig Keast, *Proceedings IEEE SOI Conference, 2010*
- 13) *FDSOI process technology for subthreshold-operation ultralow-power electronics*, Vitale, Steven A.; Wyatt, Peter W.; Checka, Nisha; Kedzierski, Jakub; Keast, Craig L. *Proceedings of the IEEE*, v 98, n 2, p 333-342, February 2010
- 14) *Engineering polycrystalline Ni films to improve thickness uniformity of the chemical-vapor-deposition-grown graphene films*, Thiele, S.; Reina, A.; Healey, P.; Kedzierski, J.; Wyatt, P.; Pei-Lan Hsu; Keast, C.; Schaefer, J.; Jing Kong *Nanotechnology*, v 21, n 1, p 015601 (8 pp.), 8 Jan. 2010
- 15) *High density plasma etching of titanium nitride metal gate electrodes for fully depleted silicon-on-insulator subthreshold transistor integration*, Vitale, Steven A.; Kedzierski, Jakub; Keast, Craig L. *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures*, v 27, n 6, p 2472-2479, 2009
- 16) *Development of Polydimethylsiloxane self-assembled monolayers for electrowetting*, Ingrid Guha, Jakub Kedzierski, Shaun Berry (to be published)
- 17) *Channel engineering of SOI MOSFETs for RF applications*, Chen, C.L.; Knecht, J.M.; Kedzierski, J.; Chen, C.K.; Gouker, P.M.; Yost, D.-R.; Healey, P.; Wyatt, P.W.; Keast, C.L., 2009 IEEE International SOI Conference, p 2 pp., 2009
- 18) *Graphene on Insulator Transistors made using C on Ni Chemical Vapor Deposition*, **Jakub Kedzierski**, P.-L. Hsu, A. Reina, J. Kong, P. Healey, P. Wyatt, and C. Keast, *IEEE Electron Device Letters*, V. 30 n. 7, July 2009, p. 745 (**2009 EDS George E. Smith Award Winner**)
- 19) *Morphology of graphene on SiC (000 1-) surfaces*, Fisher, P.J. (Department of Physics, Carnegie Mellon University, Pittsburgh, PA 15213, United States); Srivastava, N.; Feenstra, R.M.; Sun, Yugang; Kedzierski, J.; Healey, P.; Gu, Gong; Luxmi Source: *Applied Physics Letters*, v 95, n 7, 2009
- 20) *New Generation of Digital Microfluidic Devices*, **Jakub Kedzierski**, S. Berry, and B. Abedian, *IEEE Journal of Microelectromechanical Systems*, V. 18 n. 4, Aug. 2009, p. 845
- 21) *Epitaxial Graphene Transistors on SiC Substrates*, **Jakub Kedzierski**, Pei-Lan Hsu, Peter Wyatt, Paul Healey, Craig Keast, Walt de Heer, Claire Berger, *IEEE Transactions on Electron Devices*, V. 55, n. 8, p. 2078, Aug 2008
- 22) *Irreversible Electrowetting on Thin Fluoropolymer Films*, Shaun Berry, Jakub Kedzierski, Behrouz Abedian, *Langmuir*, Vol 23, p. 12429
- 23) *Low Voltage Electrowetting on Fluoropolymer Films*, Shaun Berry, Kedzierski, Jakub; Abedian, Behrouz, *Journal of Colloid and Interface Science*, v 303, n 2, Nov 15, 2006, p 517-524
- 24) *Engineering the electrocapillary behavior of electrolyte droplets on thin fluoropolymer films*, **Jakub Kedzierski**, Shaun Berry, *Langmuir*, V. 22, n. 13, Jun 2006, p. 5690
- 25) *Mobility and CMOS devices/circuits on sub-10nm (110) ultra thin body SOI*, *Mobility and CMOS devices/circuits on sub-10nm (110) ultra thin body SOI*, Shang, Huiling; Rubino, J.; Doris, B.; Topol, A.; Sleight, J.; Cai, J.; Chang, L.; Ott, J.A.; Kedzierski, J.; Chan, K.; Shi, L.; Babich, K.; Newbury, J.; Sikorski, E.; To, B.N.; Zhang, Y.; Guarini, K.W.; Ieong, Meikei, *Symposium on VLSI Technology*, 2005, p.78
- 26) *Threshold Voltage Control in NiSi-Gated MOSFETs through SIIS*, **Jakub Kedzierski**, Diane Boyd, Cyril Cabral Jr., Paul Ronsheim, Sufi Zafar, Paul M. Kozlowski, John Ott, Meikei Ieong, *IEEE Transactions on Electron Devices*, Vol. 52, No. 1, Jan. 2005, p. 39-46

- 27) *Scaling beyond conventional CMOS device*, Meikei Jeong; Dons, B.; Kedzierski, J.; Zhibin Ren; Ken Rim; Min Yang; Huiling Shang Source: 2004 7th International Conference on Solid-State and Integrated Circuits Technology Proceedings, 2005, pt. 1, p 31-4 vol.1
- 28) *Quantum-based simulation analysis of scaling in ultrathin body device structures*, Kumar, Arvind; Kedzierski, Jakub; Laux, Steven E., IEEE Transactions on Electron Devices, v 52, n 4, April, 2005, p 614-617
- 29) *Advanced gate stacks with fully silicided (FUSI) gates and high- κ dielectrics: enhanced performance at reduced gate leakage*, Gusev, E.P.; Cabral, C., Jr.; Under, B.P.; Kim, Y.H.; Maitra, K.; Carrier, E.; Nayfeh, H.; Amos, R.; Biery, G.; Bojarczuk, N.; Callegari, A.; Carruthers, R.; Cohen, S.A.; Copel, M.; Fang, S.; Frank, M.; Guha, S.; Gribelyuk, M.; Jamison, P.; Jammy, R.; Jeong, M.; Kedzierski, J.; Kozlowski, P.; Ku, K.; Lacey, D.; LaTulipe, D.; Narayanan, V.; Ng, H.; Nguyen, P.; Newbury, J.; Paruchuri, V.; Rengarajan, R.; Shahidi, G.; Steegen, A.; Steen, M.; Zafar, S.; Zhang, Y. Source: 2004 International Electron Devices Meeting , 2005, p 79-82
- 30) *Silicon device scaling to the sub-10-nm regime*, Meikei Jeong; Doris, B.; Kedzierski, J.; Ken Rim; Min Yang Source: Science, v 306, n 5704, 17 Dec. 2004, p 2057-60
- 31) *(Invited) Design considerations for advanced metal-gate FDSOI technology*, **Jakub Kedzierski**, The 4th international Symposium on Advanced Science and Technology of Silicon Materials (JSPS Si), Nov. 22-26, (2004)
- 32) *Fabrication of Metal Gated FinFETs Through Complete Gate Silicidation with Ni*, **Jakub Kedzierski**, Meikei Jeong, Thomas Kanarsky, Ying Zhang, and Philip Wong, IEEE Transactions on Electron Devices, Vol. 51, No. 12, Dec. 2004, p. 2115-2120
- 33) *Device and substrate design for sub-10 nm MOSFETs*, Jeong, Meikei; Doris, Bruce; Kedzierski, Jakub; Ren, Zhibin; Rim, Ken; Yang, Min; Shang, Huiling; Chang, Leland Source: Meeting Abstracts, Meeting Abstracts - 205th Meeting of The Electrochemical Society, MA 2004 01, 2004, p 253
- 34) *Dual Workfunction Fully Silicided Metal Gate*, C. Cabral Jr., Jakub Kedzierski, B. Linder, S. Zafar, V. Narayanan, S. Fang, A. Steen, P. Kozlowski, R. Carruthers, and R. Jammy, 2004 Symposium on VLSI technology, p.184-185, (2004)
- 35) *Threshold voltage control in NiSi-gated MOSFETs through silicidation induced impurity segregation (SIIS)*, **Jakub Kedzierski**, Diane Boyd, Paul Ronsheim, Sufi Zafar, Joseph Newbury, Cyril Cabral Jr., Meikei Jeong, Wilfried Haensch, IEDM 2003, p. 315, (2003)
- 36) *Issues in NiSi-gated FDSOI device integration*, **Jakub Kedzierski**, Diane Boyd, Ying Zhang, Michelle Steen, Fen F. Jamin, John Benedict, Meikei Jeong, Wilfried Haensch, IEDM 2003, p. 441 (2003)
- 37) *(Invited) Challenges and Opportunities of Ultrathin Channel Single- and Multiple-gate MOSFETs*, Meikei Jeong, Jakub Kedzierski, Ken Rim, Bruce Doris, Min Yang, 4th European workshop on Ultimate Integration of Silicon, ULIS March 20 (2003)
- 38) *Scaling Beyond the 65nm Node with FinFET-DGCMOS*, E. J. Nowak, I. Aller, J. Kedzierski, M. Jeong, B. Rainey, M. Breitwisch, V. Gernhoefer, J. Keinert, D. M. Fried, Custom Integrated Circuits Conference, CICC September 22 (2003)
- 39) *A fin-type independent double gate NFET*, David Fried, Edward Nowak, Jakub Kedzierski, J. Duster, and K. Kornegay, Proceedings of the Device Research Conference, Salt Lake City, UT, June 23-25 2003
- 40) *(Invited) Dual workfunction metal-gate FinFET devices fabricated using total gate silicidation*, **Jakub Kedzierski**, Edward Nowak, Thomas Kanarsky, Ying Zhang, and Meikei Jeong, SSDM 2003, p. 6-7, September 2003
- 41) *(Invited) Issues in high performance FinFET and FDSOI transistor design*, **Jakub Kedzierski**, Meikei Jeong, Edward Nowak, (ECS) Proceedings of Silicon on Insulator Technology and Devices (XI) p. 185-196, (2003)
- 42) *(Invited) Recent Progress in Devices and Materials for CMOS Technology*, H.-S. Philip Wong, B. Doris, E. Gusev, M. Jeong, E. C. Jones, J. Kedzierski, Z. Ren, K. Rim, H. Shang, VLSI-TSA conference in Taiwan (Oct. 2003)
- 43) *Moore's Law lives on (CMOS transistors)*, Leland Chang, Yang-Kyu Choi, Jakub Kedzierski, Nick Lindert, Peiqi Xuan, Jeffrey Bokor, Chenming Hu, and Tsu-Jae King, IEEE Circuits Devices Mag. (USA) Vol.19, No.1 Jan. 2003 P35-42

- 44) *Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation*, **Jakub Kedzierski**, Edward Nowak, Thomas Kanarsky, Ying Zhang, Diane Boyd, Roy Carruthers, Cyril Cabral, Rick Amos, Christian Lavoie, Ronnen Roy, Joseph Newbury, Elizabeth Sullivan, John Benedict, Philip Saunders, Keith Wong, Donald Canaperi, M. Krishnan, Kam-Leung Lee, Beth-Ann Rainey, David Fried, Peter Cottrell, H-S Philip Wong, Meikei Ieong, Wilfried Haensch, IEDM 2003, p. 247-250, Dec 2002
- 45) *Extension and source/drain design for high performance FinFET devices*, **Jakub Kedzierski**, Meikei Ieong, Edward Nowak, Thomas Kanarsky, Ying Zhang, Ronnen Roy, Diane Boyd, David Fried, H-S Philip Wong, IEEE Transactions on Electron Devices, Vol. 50, No. 4, p. 952-958, April 2003
- 46) *(Invited) Scaling beyond 65-nm Node with FinFET double-gate CMOS*, Edward Nowak, T. Ludwig, I. Aller, Jakub Kedzierski, M. Ieong, B.A. Rainey, M. Breitwisch, V. Gernhoefer, J. Keinert, D.M. Fried, CICC 2002
- 47) *A functional FinFET-DGCMOS SRAM Cell*, Edward Nowak, Beth-Ann Rainey, David Fried, Jakub Kedzierski, Meikei Ieong, W. Leipold, J. Wright, M. Breitwisch, IEDM 2002, p. 411-414, Dec. 2002
- 48) *Demonstration of FinFET CMOS Circuits*, B.A. Rainey, D.M. Fried, M. Ieong, J. Kedzierski, E. J. Nowak, Proceedings of the Device Research Conference, pp. 47-48, June 2002
- 49) *(Invited) Ultra-thin Silicon Channel Single- and Double-gate MOSFETs*, Meikei Ieong, Jakub Kedzierski, Zhibin Ren, Bruce Doris, and H-S Philip Wong, 2002 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICE AND MATERIALS, P. 136, Nagoya, 2002
- 50) *Design and Fabrication of 50-nm Thin-Body p-MOSFETs with a Silicon-Germanium Heterostructure Channel*, Yee-Chia Yeo, Vivek Subramanian, Jakub Kedzierski, Peiqi Xuan, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu, IEEE Transactions on Electron Devices, vol. 49, no. 2, pp. 279-286, Feb. 2002. **(2002 EDS Paul Rappaport Award Winner)**
- 51) *FinFET design considerations based on 3-D simulation and analytical modeling*, Gen Pei, Jakub Kedzierski, Phil Oldiges, Meikei Ieong, Edwin Kan, IEEE Transactions on Electron Devices, Vol. 49(8), p. 1411, Aug. 2002
- 52) *High-performance symmetric-gate and CMOS compatible V_t asymmetric-gate FinFET devices*, **Jakub Kedzierski**, David M. Fried, Edward J. Nowak, Thomas Kanarsky, Jed H. Rankin, Hussein Hanafi, W. Natzle, Diane Boyd, Ying Zhang, Ronnen A. Roy, J. Newbury, Chienfan Yu, Qingyun Yang, P. Saunders, Christa P. Willets, A. Johnson, S. P. Cole, H. E. Young, N. Carpenter, D. Rakowski, Beth Ann Rainey, Peter E. Cottrell, Meikei Ieong, and H.-S. Philip Wong, IEDM 2001, p. 437, Dec 2001
- 53) *Design analysis of thin-body silicide source drain devices*, **Jakub Kedzierski**, MeiKei Ieong, Peiqi Xuan, Jeffrey Bokor, Tsu-Jae King, and Chenming Hu, IEEE International SOI 2001 Conference Proceedings, p 21-22, Oct. 2001
- 54) *Sub 50nm P channel FinFET*, .X Huang, W-C. Lee, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, Y-K. Choi, V. Subramanian, J. Bokor, T-J. King, C. Hu, IEEE Transactions on Electron Devices, Vol. 48(5), p. 880, May 2001
- 55) *Calixarine G-line double resist process with 15nm resolution and large area exposure capability*, **Jakub Kedzierski**, Erik Anderson, Jeffrey Bokor, Journal of Vacuum Science and Technology B, Vol. 18(6), p. 3428, Nov 2000
- 56) *FinFET a self aligned double gate MOSFET scalable to 20 nm*, D. Hisamoto, W-C. Lee, J. Kedzierski, E. Anderson, T-J. King, J. Bokor, C. Hu, IEEE Transactions on Electron Devices, Vol. 46(12), p. 2320, Dec. 2000
- 57) *Complementary silicide source/drain thin-body MOSFETs for the 20nm gate-length regime*, **Jakub Kedzierski**, Peiqi Xuan, Erik H. Anderson, Jeffrey Bokor, Tsu-Jae King, Chenming Hu, Proceedings of the IEDM 2000, p. 57, Dec. 2000
- 58) *A 20nm gate-length ultra-thin body P-MOSFET with silicide source drain*, **Jakub Kedzierski**, Patrick Xuan, Vivek Subramanian, Jeffrey Bokor, Tsu-Jae King, Chenming Hu, Erik Anderson, Superlattices and Microstructures, Vol. 28 (5-6), p. 445, June 2000
- 59) *60nm planarized ultra-thin body solid phase epitaxy MOSFETs*, Peiqi Xuan, Jakub Kedzierski, Vivek Subramanian, Jeffrey Bokor, Tsu-Jae King, Chenming Hu, Proceedings of the 58th Device Research Conference 2000, p. 67, June 2000

- 60) *Nanoscale ultra-thin body silicon on insulator PMOSFET with SiGe/Si heterostructure channel*, Y.-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, C. Hu, IEEE Electron Device Letters, Vol 21(4), p. 161, April 2000
- 61) *Sub-50nm FinFET: PMOS*, X. Huang, W-C. Lee, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, Y-K. Choi, V. Subramanian, J. Bokor, T-J. King, C. Hu, Proceedings of the IEDM 1999, p. 67, Dec. 1999
- 62) *A folded-channel MOSFET for deep sub-tenth micron era*, D. Hisamoto, W-C. Lee, J. Kedzierski, E. Anderson, T-J. King, J. Bokor, C. Hu, Proceedings of the IEDM 1998, p. 1033, Dec. 1998
- 63) *Nanoscale Si Ge channel ultra thin body silicon on insulator PMOSFETs*, Y.-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T-J. King, J. Bokor, C. Hu, International Semiconductor Device Research Conference 1999 Proceedings, 1999
- 64) *A bulk Si compatible ultra thin body SOI technology for sub-100nm MOSFETs*, V. Subramanian, J. Kedzierski, N. Lindert, Y. Su, J. McHale, K. Cao, T-J. King, J. Bokor, C. Hu, Device Research Conference 1999 Proceedings, p. 28, 1999
- 65) *Novel method for silicon quantum wire transistor fabrication*, **Jakub Kedzierski**, Jeffrey Bokor, Erik Anderson, Journal of Vacuum Science and Technology B, Vol. 17(6), p. 3244, Dec. 1999
- 66) *Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation*, **Jakub Kedzierski**, Jeffrey Bokor, Christian Kisielowski, Journal of Vac. Sci. and Tech. B, Vol 15 (6), p. 2825, Dec 1997