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(54) CMOS SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

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(57) ABSTRACT

A CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising: a gate electrode of the n-type MOSFET having a first insulation layer composed of a high-k material, and a first metal layer provided on the first insulation layer and composed of a metal material; and a gate electrode of the p-type MOSFET having a second insulation layer composed of a high-k material, and a second metal layer provided on the second insulation layer and composed of a metal material, wherein the first insulation layer and the second insulation layer are composed of the different high-k materials, and the first metal layer and the second metal layer are composed of the same metal material.

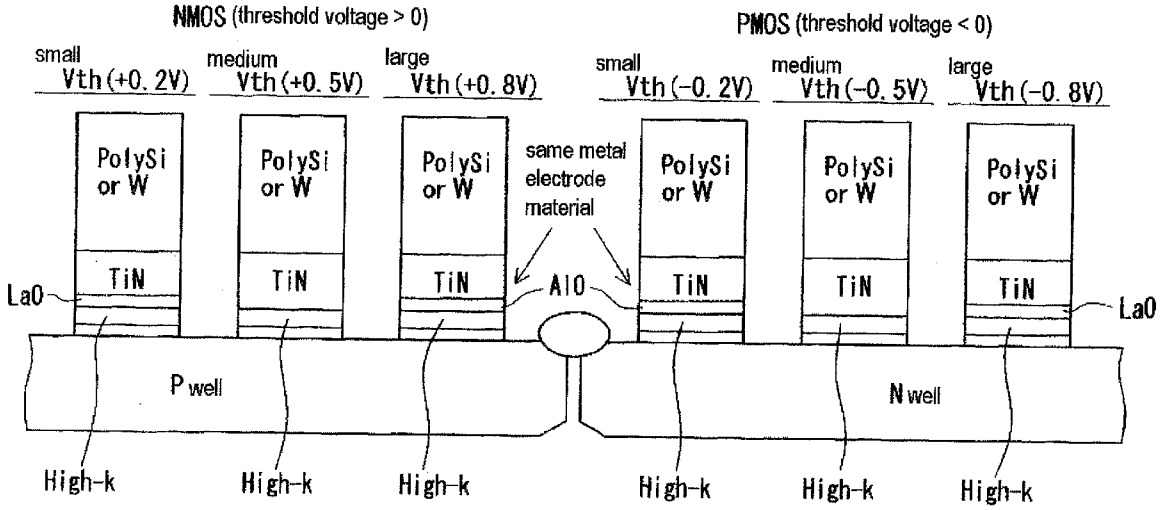

Fig. 1

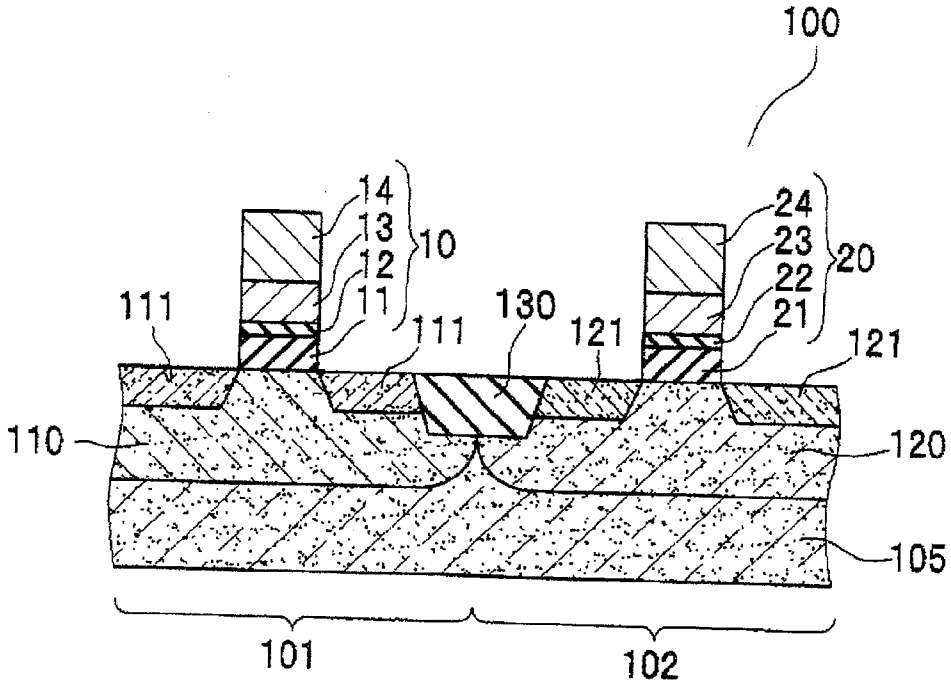
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Fig. 1A

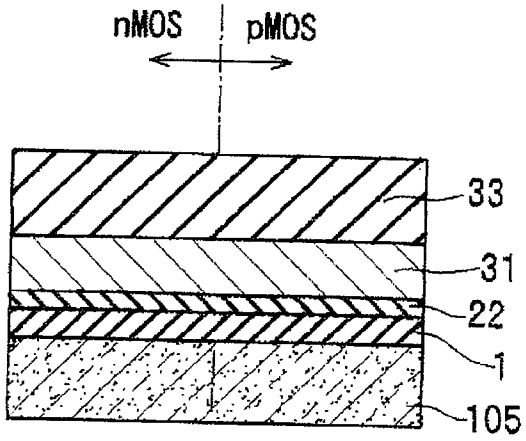
nMOS
pMOS
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Fig. 1B

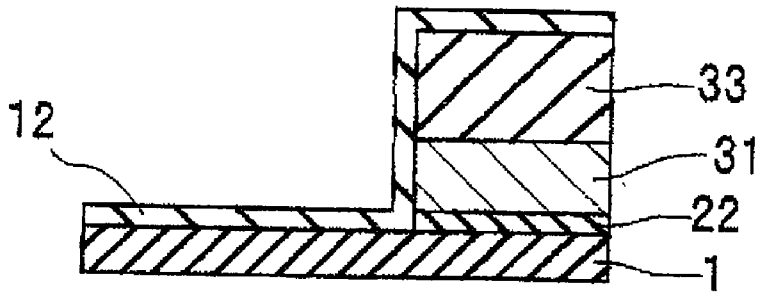
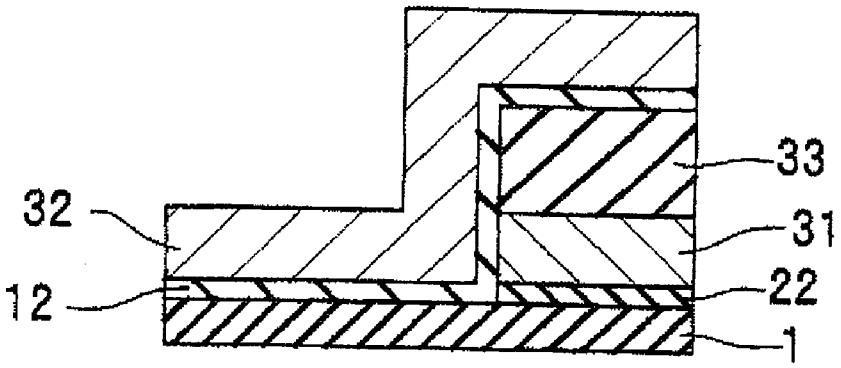


Fig. 1C



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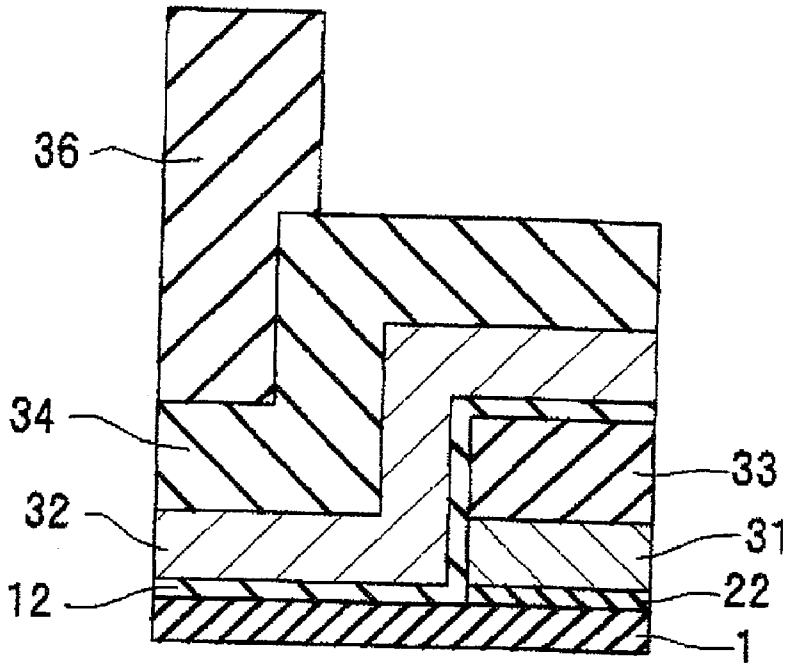

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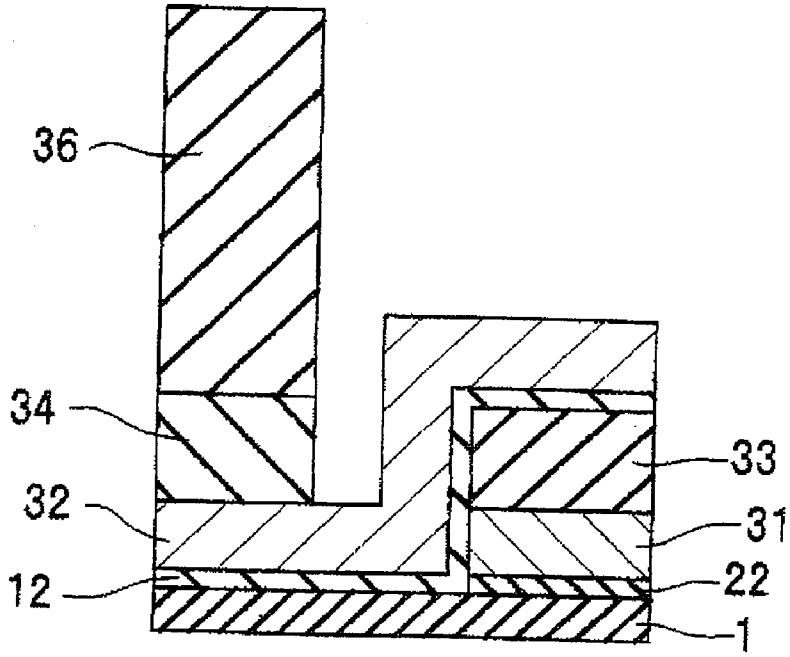

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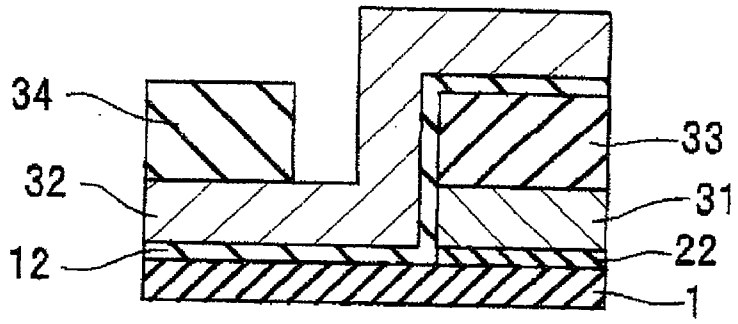

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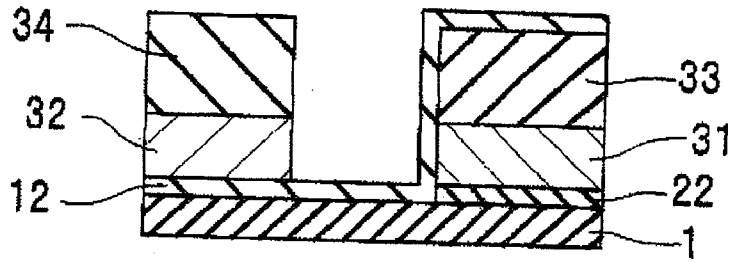

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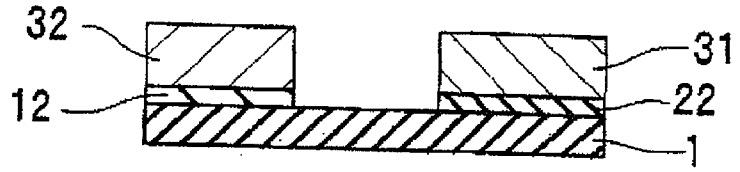
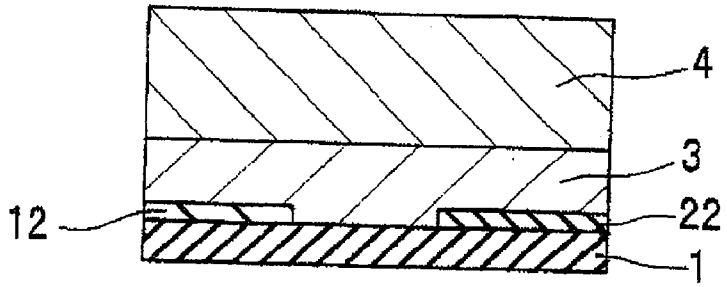


Fig.1I

Fig.1J



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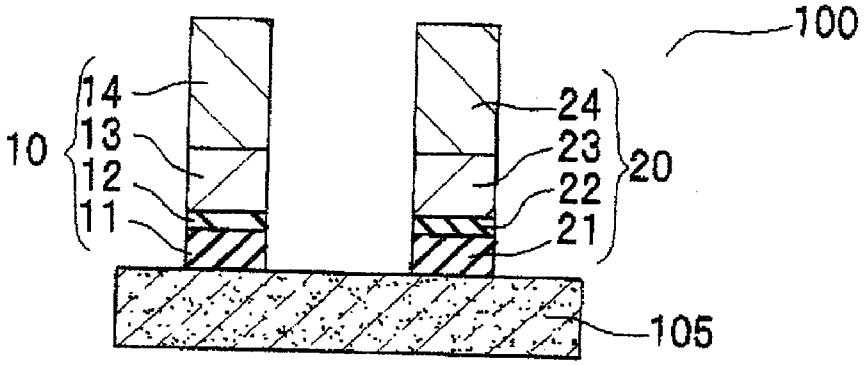

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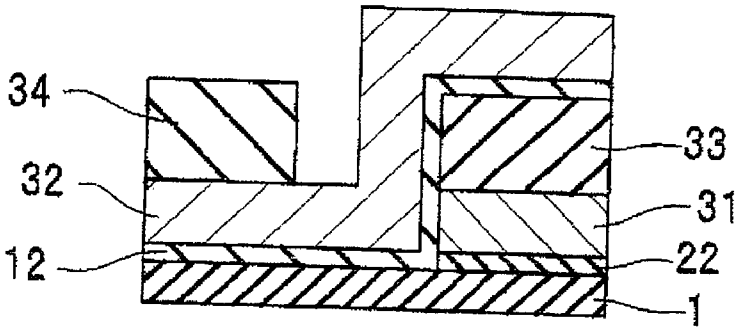

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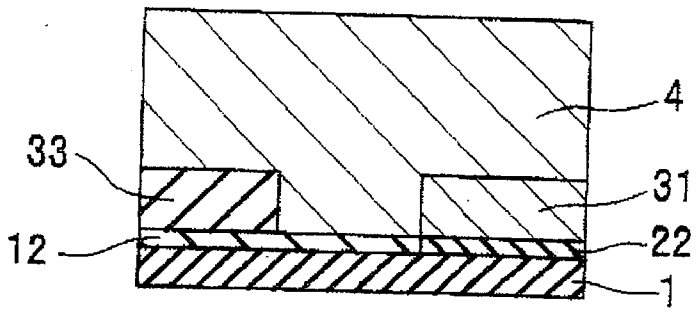

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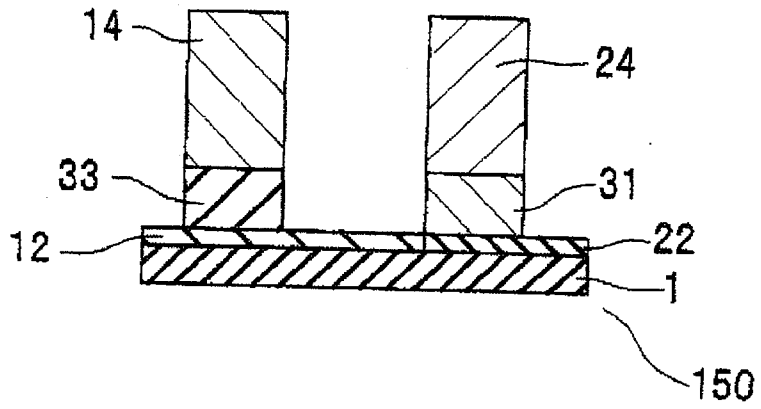
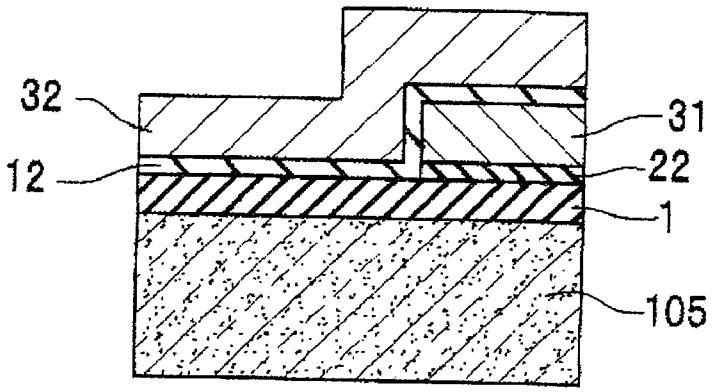


Fig.3A



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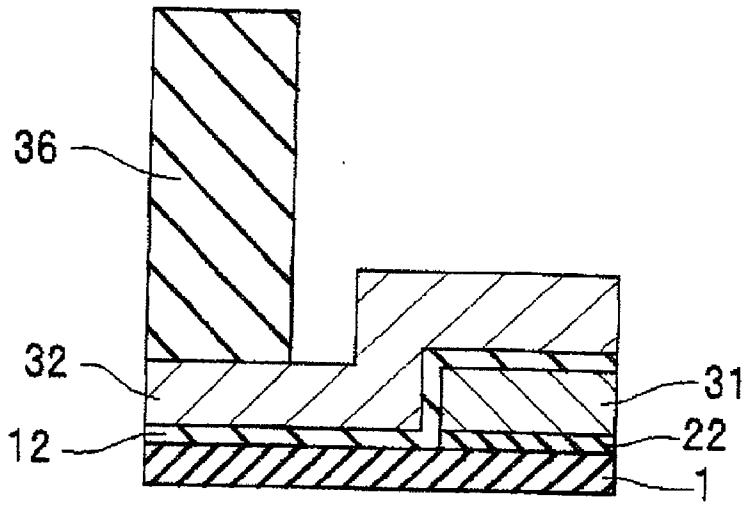

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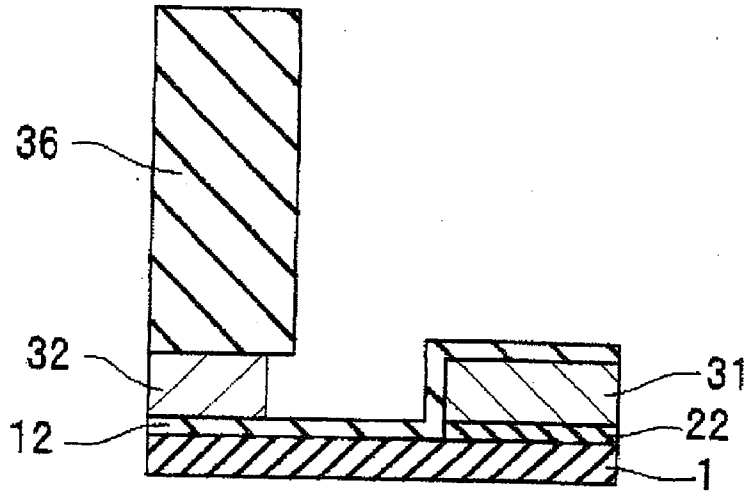

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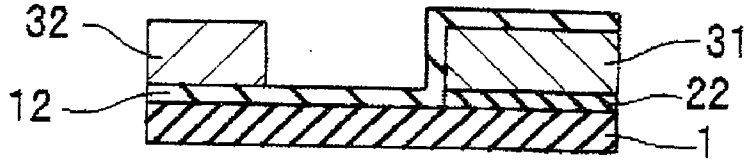

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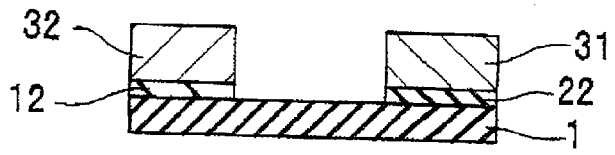

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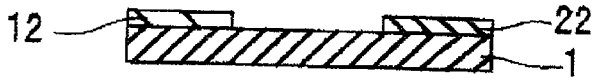

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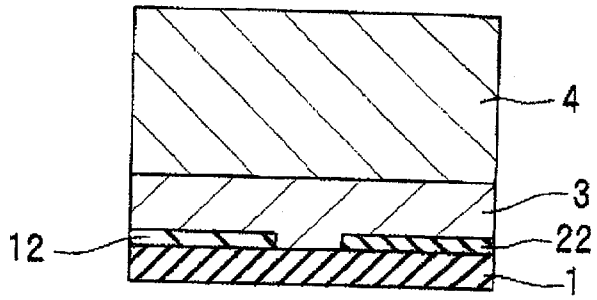

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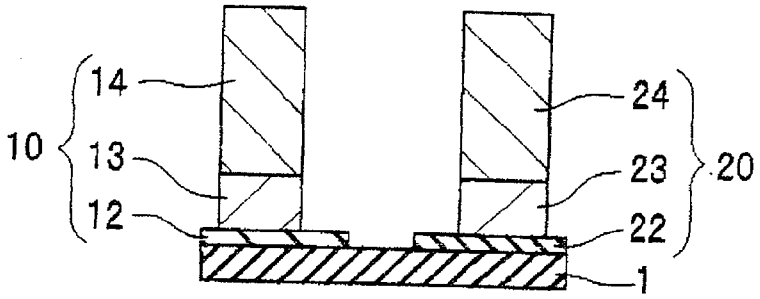

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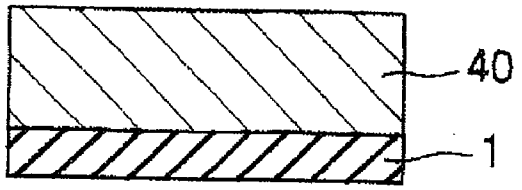

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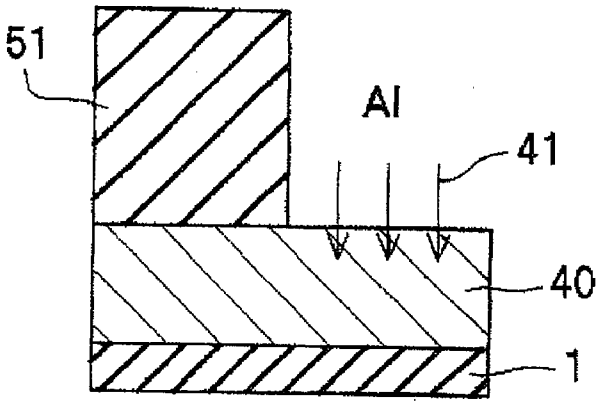

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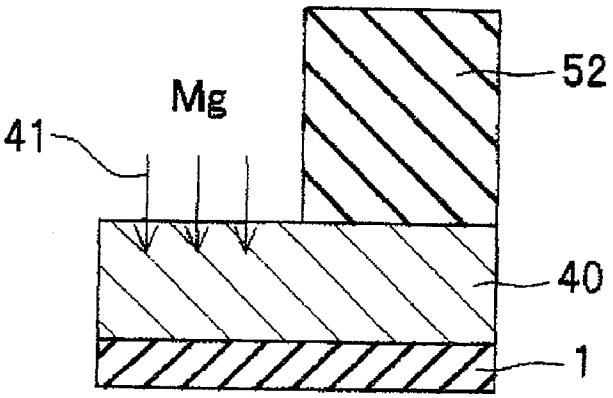

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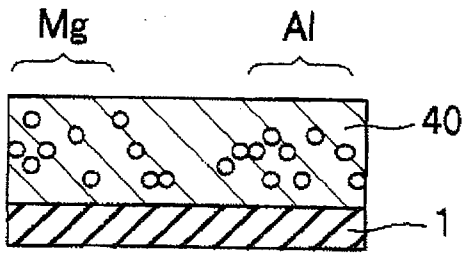

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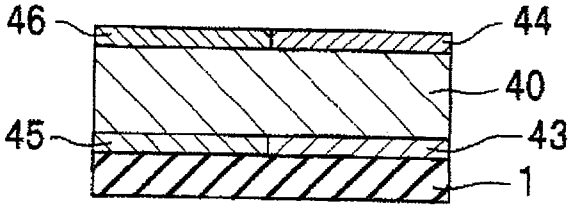

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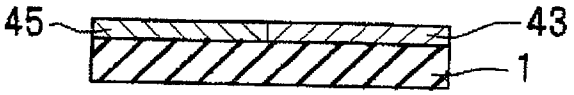

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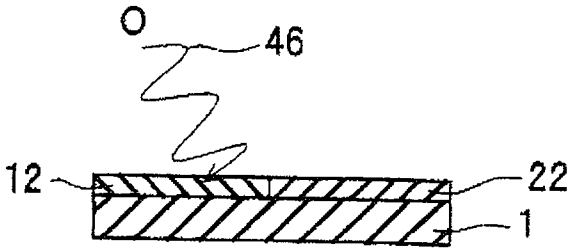

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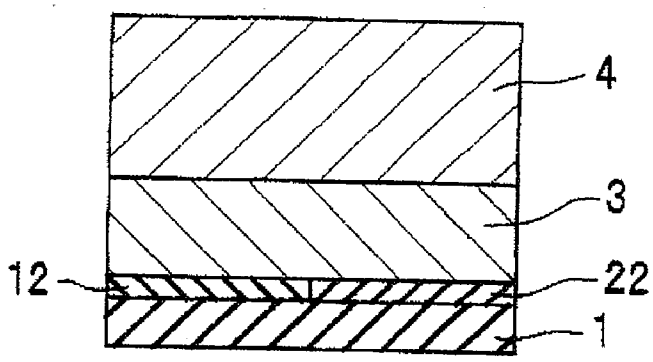

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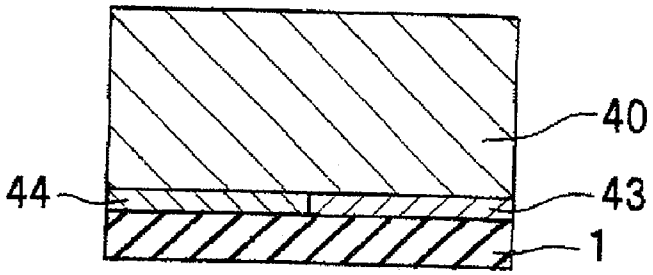

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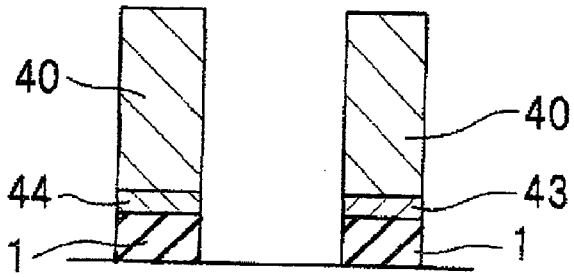

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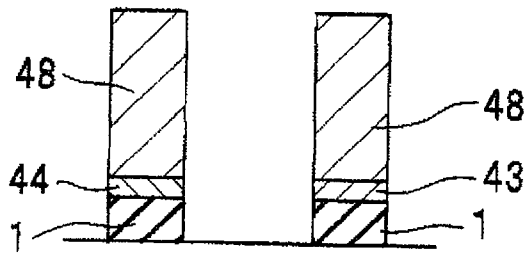
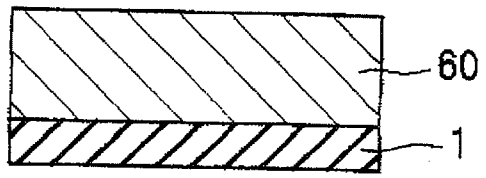


Fig.6A



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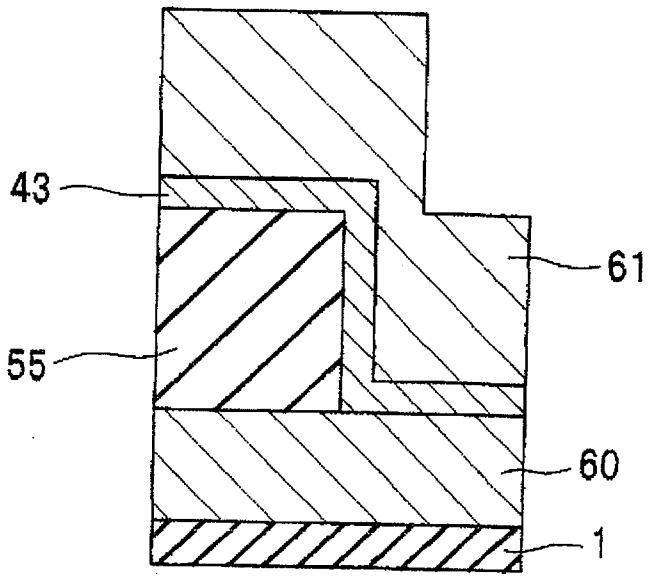

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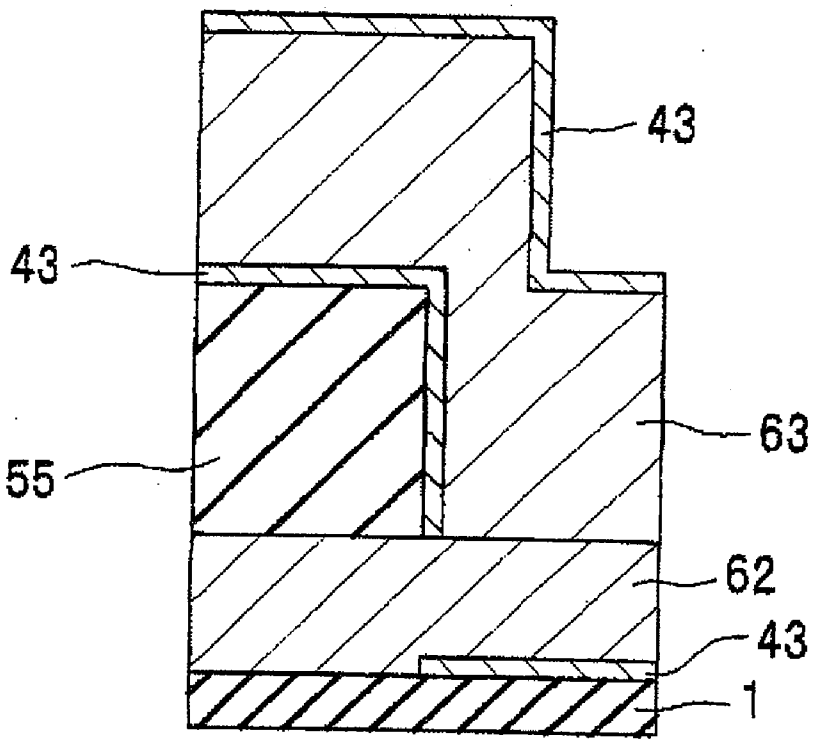

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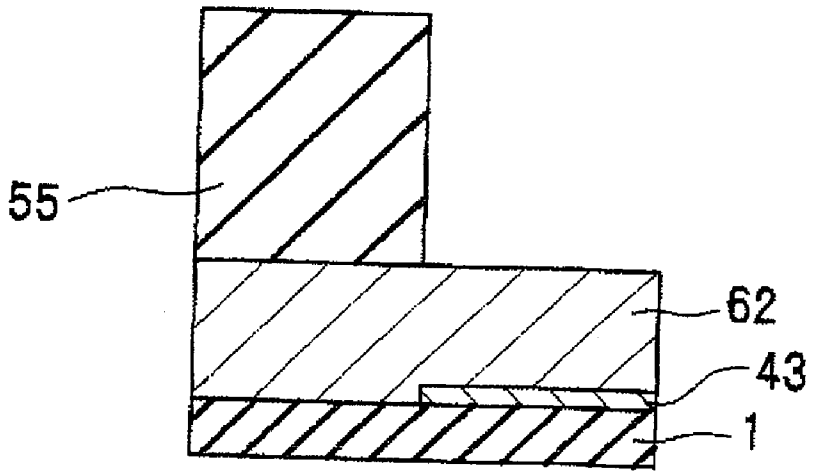

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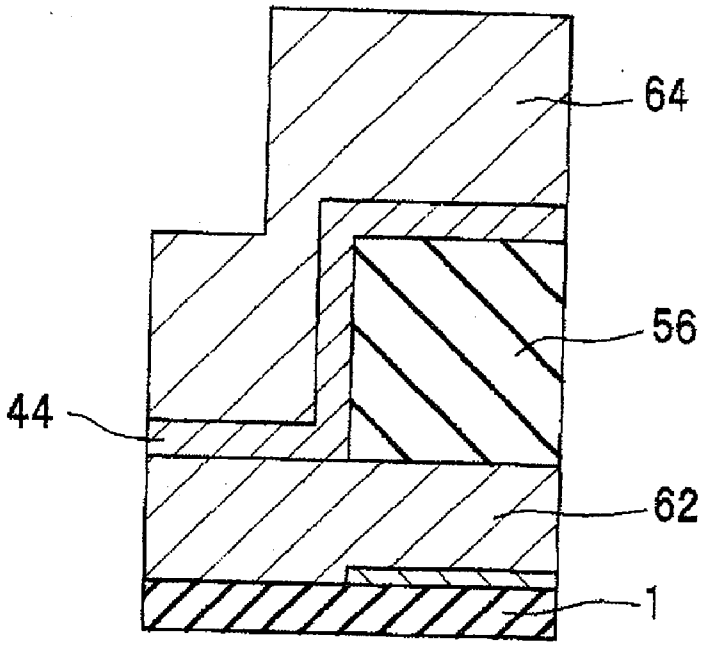

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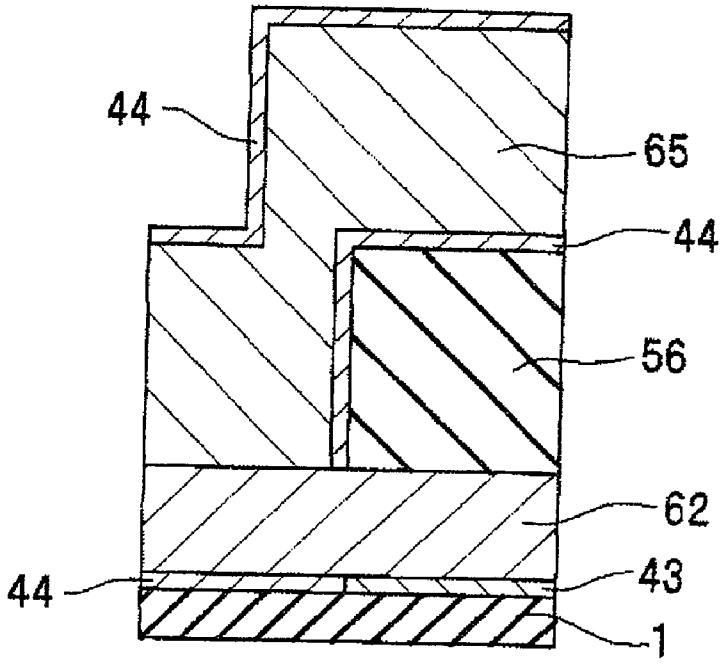


Fig.6G

Fig.6H

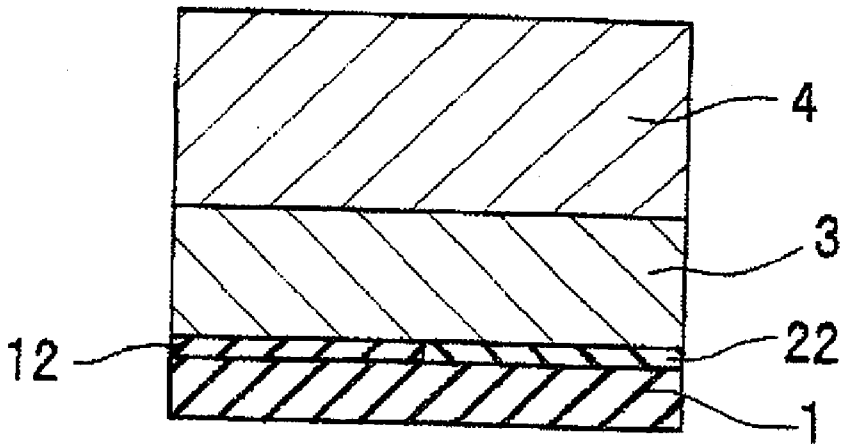
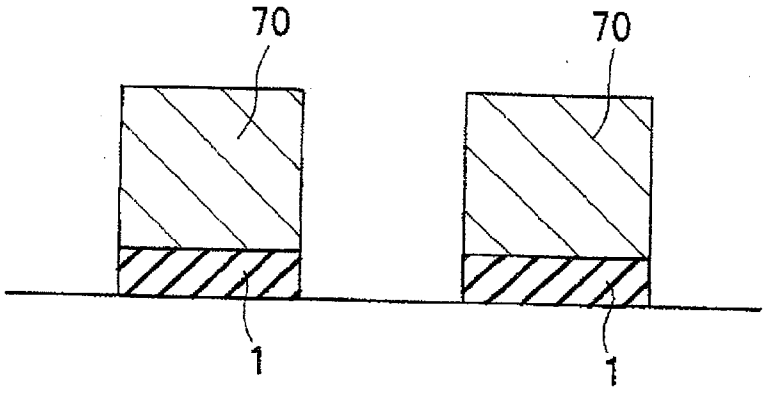


Fig.7A



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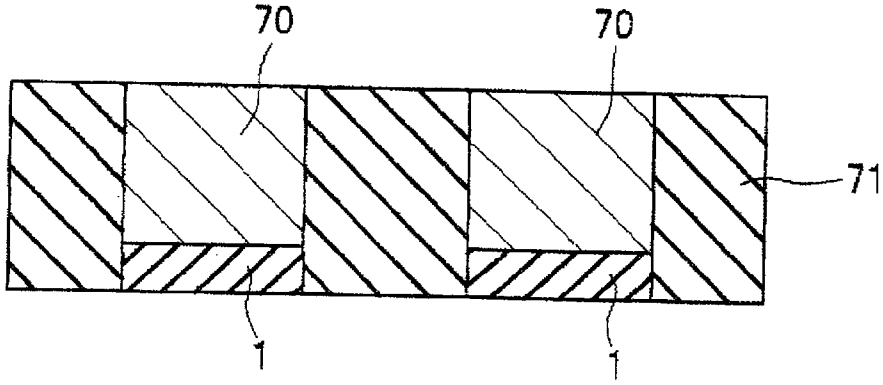

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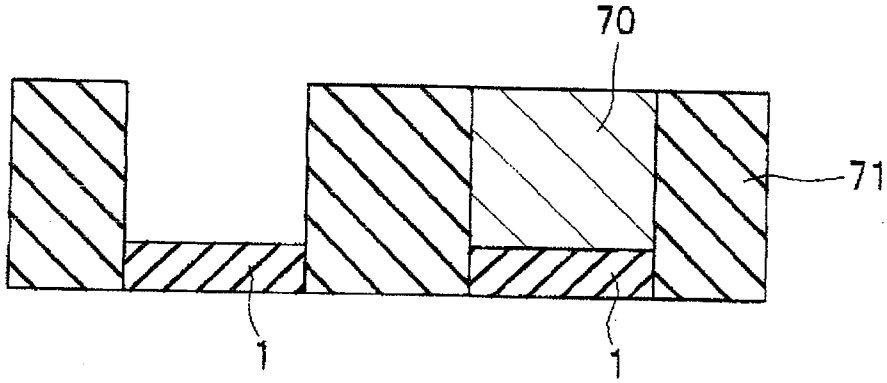

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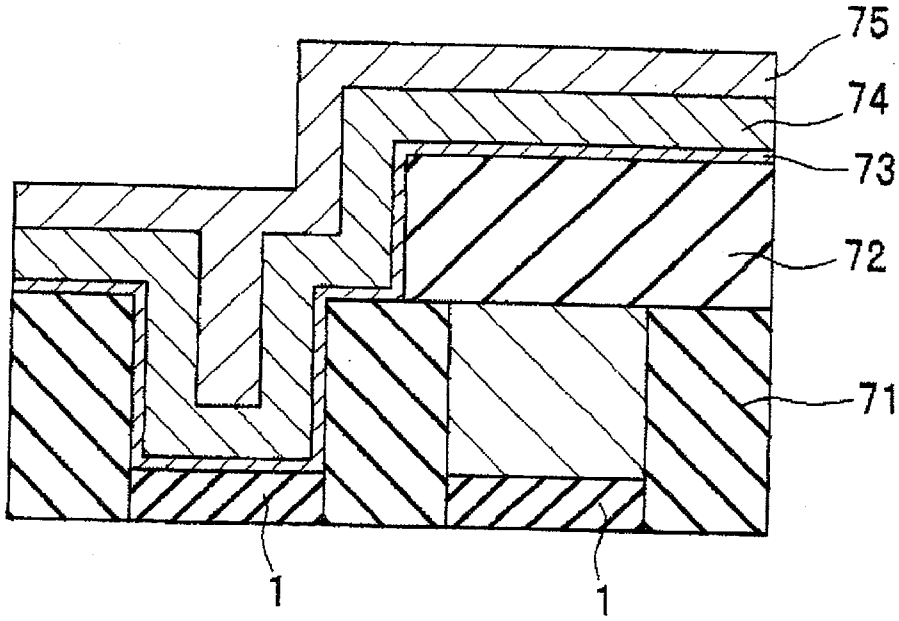

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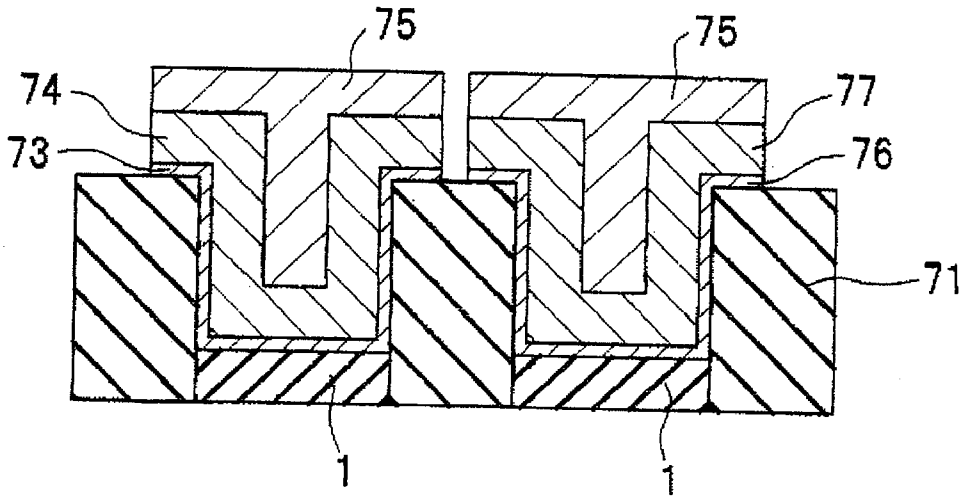

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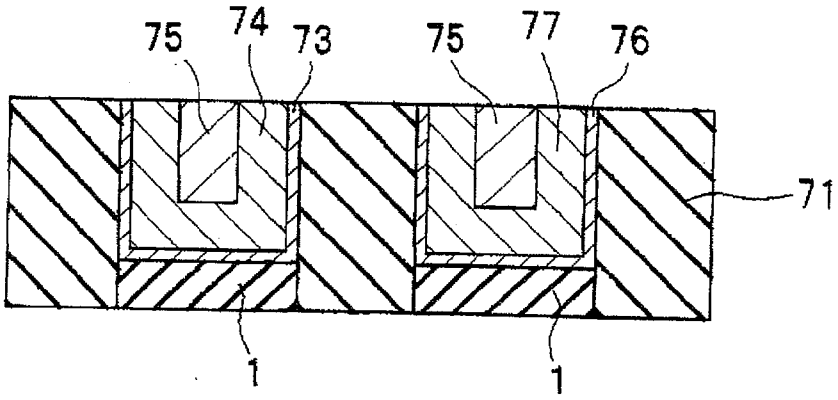

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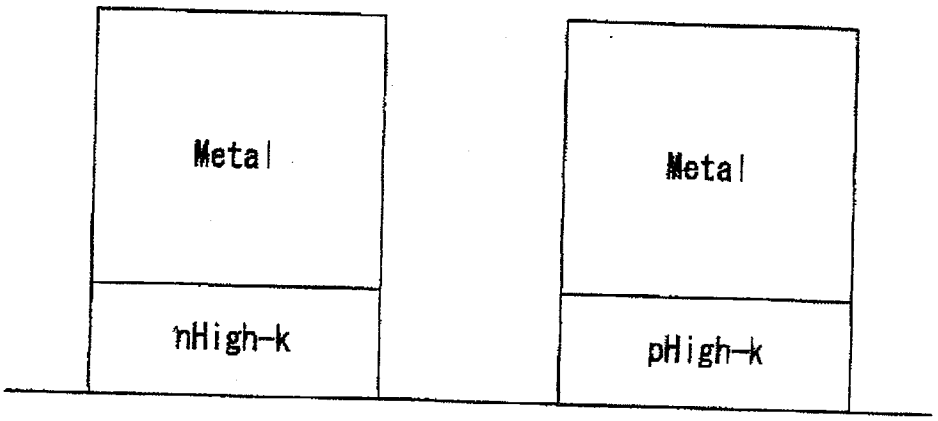


Fig.9

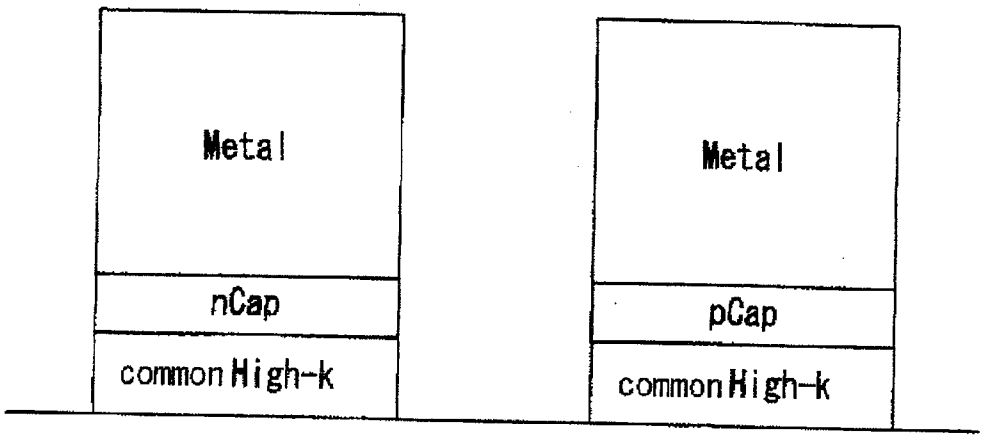

Metal
nCap
common High-k
Metal
pCap
common High-k

Fig.10A

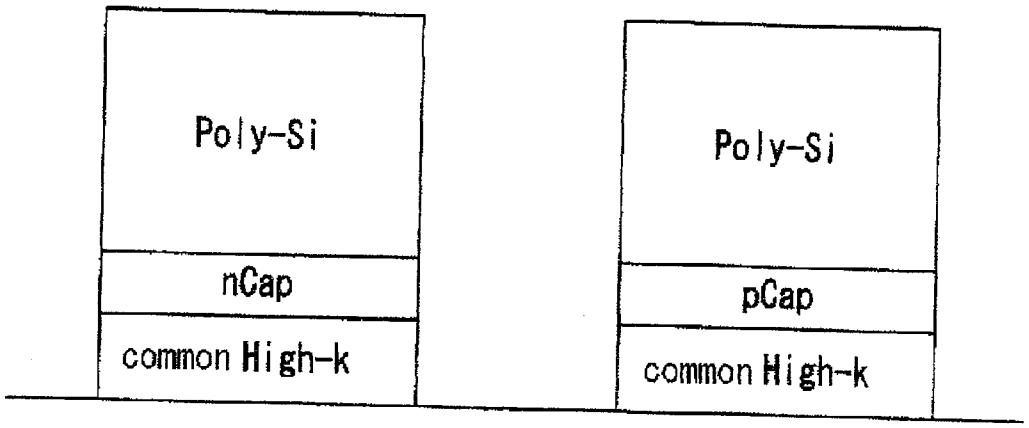

Poly-Si
nCap
common High-k
Poly-Si
pCap
common High-k

Fig.10B

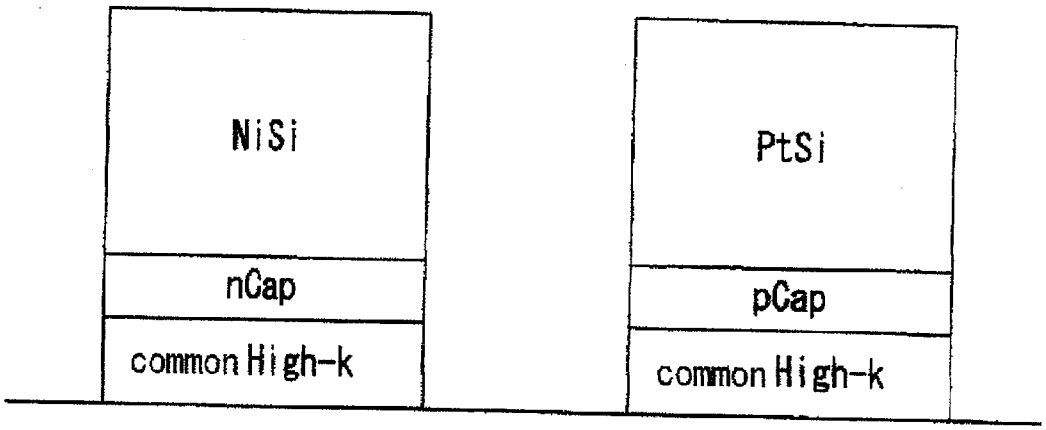
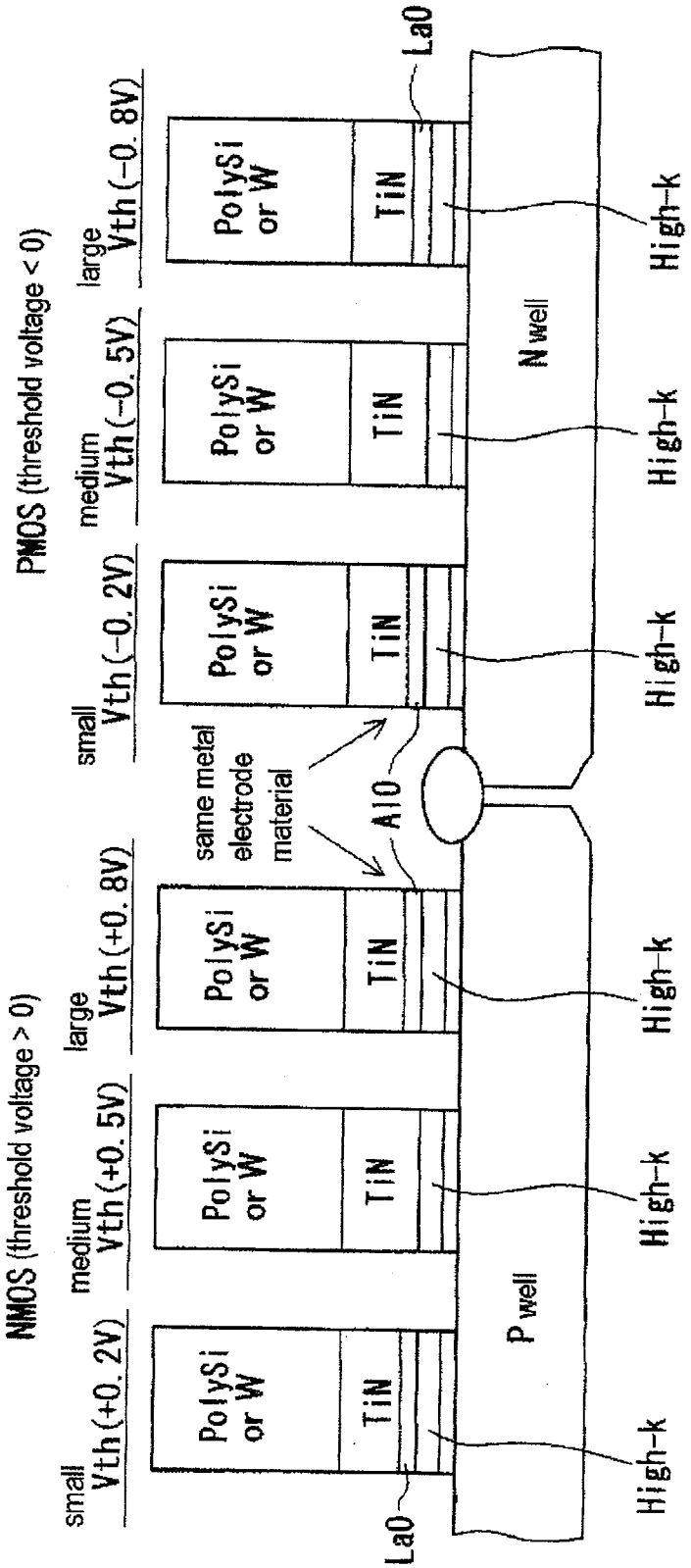


Fig. 11


NMOS (threshold voltage > 0)
PMOS (threshold voltage < 0)
small Vth (+0. 2V)
medium Vth (+0. 5V)
large Vth (+0. 8V)
small Vth (−0. 2V)
medium Vth (−0. 5V)
large Vth (−0. 8V)
PolySi or W
TiN
LaO
AlO
same metal electrode material
High-k
P well
N well

CMOS SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

TECHNICAL FIELD

[0001] The present invention relates to a CMOS semiconductor device and a method for producing the same, and more particularly to a CMOS semiconductor device using a high-k material for a gate electrode and a method for producing the same.

BACKGROUND ART

[0002] Recently, as a CMOS semiconductor device is miniaturized, what is troubling is that a gate insulation layer composed of SiON or SiO_2 becomes thin and a leak current goes through the gate insulation layer due to a tunneling phenomenon.

[0003] To solve this problem, a high-k material (high-dielectric material) such as hafnium is used for the gate insulation layer and a thickness of the gate insulation layer is set to a constant value to prevent the leak current from being generated. In addition, when the high-k material is used for a gate electrode, Fermi level pinning is generated at a boundary with a silicon gate electrode, so that as a gate electrode material, a metal such as nickel silicide is used instead of polycrystalline silicon.

[0004] For example, when the high-k material is used for the gate insulation layer, NiSi is used for a metal gate electrode of a p-channel MOSFET, and Ni_2Si is used for a metal gate electrode of an n-channel MOSFET.

Patent document 1: Japanese Unexamined Patent Publication No. 2002-359295

DISCLOSURE OF THE INVENTION

Problems to be Solved by the Invention

[0005] In the CMOS semiconductor device, it is necessary to control a gate length Lg with a high degree of accuracy to control threshold voltages of the p-channel MOSFET and the n-channel MOSFET. When the gate length Lg is 20 nm, for example, allowable LWR (Line Width Roughness) of the gate length is about 5%, which means about 1 nm.

[0006] However, the gate electrodes composed of different materials such as NiSi and Ni_2Si cannot be processed with a high degree of accuracy in the same etching step, that is, in one etching step using one kind of etching gas, so that a side wall of the electrode is tapered in general.

[0007] On the other hand, when the two gate electrodes composed of different materials are processed in different etching steps, etching masks cannot be aligned due to a fine structure in which the gate length Lg is as small as 20 nm.

[0008] Thus, it is an object of the present invention to provide a CMOS semiconductor device capable of controlling a gate length with a high degree of accuracy in the CMOS semiconductor device using a high-k material, and a production method for producing the same.

Means for Solving the Problem

[0009] Therefore, the present invention is a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising: a gate electrode of the n-type MOSFET having a first insulation layer composed of a high-k material, and a first metal layer provided on the first insulation layer and composed of a metal material; and a gate electrode of the p-type MOSFET having a second insulation layer composed of a high-k material, and a second metal layer provided on the second insulation layer and composed of a metal material, wherein the first insulation layer and the second insulation layer are composed of the different high-k materials, and the first metal layer and the second metal layer are composed of the same metal material.

[0010] Furthermore, the present invention is a method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising the steps of: preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region; forming a high-k material layer, a first cap layer, and a first metal layer, sequentially on the semiconductor substrate; removing the first cap layer and the first metal layer except for those in the p-type MOSFET formation region; forming a second cap layer and a second metal layer, sequentially on the semiconductor substrate; removing the second metal layer except for that in the n-type MOSFET formation region; removing the second cap layer provided between the n-type MOSFET formation region and the p-type MOSFET formation region, using the first metal layer and the second metal layer as masks; removing the first metal layer and the second metal layer; forming a gate metal material layer on the semiconductor substrate; and forming a gate metal layer of a gate electrode of each of the n-type MOSFET and the p-type MOSFET by etching the gate metal material layer in the same etching step.

EFFECT OF THE INVENTION

[0011] The CMOS semiconductor device according to the present invention can control a threshold voltage with a high degree of accuracy.

[0012] In addition, according to the method for producing a CMOS semiconductor device in the present invention, since the gate metal layer of the gate electrode each of the n-type MOSFET and the p-type MOSFET can be formed in the same etching step, the gate electrode can be processed with a high degree of accuracy.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. **1** is a cross-sectional view of a CMOS semiconductor device according to a first embodiment.

[0014] FIG. **1**A is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0015] FIG. **1**B is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0016] FIG. **1**C is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0017] FIG. **1**D is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0018] FIG. **1**E is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0019] FIG. **1**F is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0020] FIG. **1**G is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0021] FIG. **1**H is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0022] FIG. **1**I is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0023] FIG. **1**J is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0024] FIG. **1**K is a cross-sectional view of a production step of the CMOS semiconductor device according to the first embodiment.

[0025] FIG. **2**A is a cross-sectional view of a production step of a CMOS semiconductor device according to a second embodiment.

[0026] FIG. **2**B is a cross-sectional view of a production step of the CMOS semiconductor device according to the second embodiment.

[0027] FIG. **2**C is a cross-sectional view of a production step of the CMOS semiconductor device according to the second embodiment.

[0028] FIG. **3**A is a cross-sectional view of a production step of a CMOS semiconductor device according to a third embodiment.

[0029] FIG. **3**B is a cross-sectional view of a production step of the CMOS semiconductor device according to the third embodiment.

[0030] FIG. **3**C is a cross-sectional view of a production step of the CMOS semiconductor device according to the third embodiment.

[0031] FIG. **3**D is a cross-sectional view of a production step of the CMOS semiconductor device according to the third embodiment.

[0032] FIG. **3**E is a cross-sectional view of a production step of the CMOS semiconductor device according to the third embodiment.

[0033] FIG. **3**F is a cross-sectional view of a production step of the CMOS semiconductor device according to the third embodiment.

[0034] FIG. **3**G is a cross-sectional view of a production step of the CMOS semiconductor device according to the third embodiment.

[0035] FIG. **3**H is a cross-sectional view of a production step of the CMOS semiconductor device according to the third embodiment.

[0036] FIG. **4**A is a cross-sectional view of a production step of a CMOS semiconductor device according to a fourth embodiment.

[0037] FIG. **4**B is a cross-sectional view of a production step of the CMOS semiconductor device according to the fourth embodiment.

[0038] FIG. **4**C is a cross-sectional view of a production step of the CMOS semiconductor device according to the fourth embodiment.

[0039] FIG. **4**D is a cross-sectional view of a production step of the CMOS semiconductor device according to the fourth embodiment.

[0040] FIG. **4**E is a cross-sectional view of a production step of the CMOS semiconductor device according to the fourth embodiment.

[0041] FIG. **4**F is a cross-sectional view of a production step of the CMOS semiconductor device according to the fourth embodiment.

[0042] FIG. **4**G is a cross-sectional view of a production step of the CMOS semiconductor device according to the fourth embodiment.

[0043] FIG. **4**H is a cross-sectional view of a production step of the CMOS semiconductor device according to the fourth embodiment.

[0044] FIG. **5**A, is a cross-sectional view of a production step of another CMOS semiconductor device according to the fourth embodiment.

[0045] FIG. **5**B is a cross-sectional view of a production step of another CMOS semiconductor device according to the fourth embodiment.

[0046] FIG. **5**C is a cross-sectional view of a production step another CMOS semiconductor device according to the fourth embodiment.

[0047] FIG. **6**A is a cross-sectional view of a production step of a CMOS semiconductor device according to a fifth embodiment.

[0048] FIG. **6**B is a cross-sectional view of a production step of the CMOS semiconductor device according to the fifth embodiment.

[0049] FIG. **6**C is a cross-sectional view of a production step of the CMOS semiconductor device according to the fifth embodiment.

[0050] FIG. **6**D is a cross-sectional view of a production step of the CMOS semiconductor device according to the fifth embodiment.

[0051] FIG. **6**E is a cross-sectional view of a production step of the CMOS semiconductor device according to the fifth embodiment.

[0052] FIG. **6**F is a cross-sectional view of a production step of the CMOS semiconductor device according to the fifth embodiment.

[0053] FIG. **6**G is a cross-sectional view of a production step of the CMOS semiconductor device according to the fifth embodiment.

[0054] FIG. **6**H is a cross-sectional view of a production step of the CMOS semiconductor device according to the fifth embodiment.

[0055] FIG. **7**A is a cross-sectional view of a production step of a CMOS semiconductor device according to a sixth embodiment.

[0056] FIG. **7**B is a cross-sectional view of a production step of the CMOS semiconductor device according to the sixth embodiment.

[0057] FIG. **7**C is a cross-sectional view of a production step of the CMOS semiconductor device according to the sixth embodiment.

[0058] FIG. **7**D is a cross-sectional view of a production step of the CMOS semiconductor device according to the sixth embodiment.

[0059] FIG. **7**E is a cross-sectional view of a production step of the CMOS semiconductor device according to the sixth embodiment.

[0060] FIG. **7**F is a cross-sectional view of a production step of the CMOS semiconductor device according to the sixth embodiment.

[0061] FIG. **8** is a structural drawing of gate electrodes of a CMOS semiconductor device according to a seventh embodiment.

[0062] FIG. **9** is a structural drawing of gate electrodes of the CMOS semiconductor device described in the first to sixth embodiments.

[0063] FIG. **10**A is a schematic view of a production step of a CMOS semiconductor device according to an eighth embodiment.

[0064] FIG. **10**B is a schematic view of a production step of the CMOS semiconductor device according to the eighth embodiment.

[0065] FIG. **11** is a structural drawing of gate electrodes of a CMOS semiconductor device according to a ninth embodiment.

EXPLANATION OF REFERENCES

[0066] **1**, **11**, **21** . . . insulation layer, **12**, **22** . . . cap layer, **13**, **14**, **23**, **24** . . . metal layer, **10**, **20** . . . gate electrode, **100** . . . CMOS semiconductor device, **101** . . . n-type MOSFET, **102** . . . p-type MOSFET, **105** . . . semiconductor substrate, **110** . . . n-well region, **120** . . . p-well region, **111**, **121** . . . gate/source regions, **130** . . . element isolation layer

BEST MODE FOR CARRYING OUT THE INVENTION

[0067] Hereinafter, preferred embodiments of the present invention will be described with reference to the drawings. In addition, while "upper", "lower", "left" and "right", and names including these terms are occasionally used in the following descriptions, these directions are used to easily understand the present invention with reference to the drawings, so that a configuration where the embodiment is vertically inverted or rotated in a certain direction may be included in the technical scope of the present invention as a matter of course.

First Embodiment

[0068] FIG. **1** is a cross-sectional view of a CMOS semiconductor device (complementary metal oxide semiconductor device) represented by **100** as a whole according to a first embodiment.

[0069] The CMOS semiconductor device **100** includes an n-type MOSFET **101** and a p-type MOSFET **102**.

[0070] The CMOS semiconductor device **100** includes a semiconductor substrate **105** composed of silicon, for example. An n-type well region **110** and a p-type well region **120** are provided in the semiconductor substrate **100**. The n-type well region **110** and the p-type well region **120** are insulated by an interlayer insulation layer **130** composed of silicon oxide, for example.

[0071] Source/drain regions **111** are provided in the n-type well region **110**. A gate electrode **10** is provided on a channel region sandwiched between the source/drain regions **111**. The gate electrode **10** includes a gate insulation layer **11**, a cap layer **12**, and gate metal layers **13** and **14** provided thereon. The gate insulation layer **11** is composed of a high-k material such as HfLaO or HfMgO, and the cap layer **12** is composed of MgO or LaO, for example. In addition, the gate metal layer **13** is composed of a mid-gap material having high heat resistance such as TiN, TaN, TaSiN, NiSi, PtSi, or $CoSi_2$, and the gate metal layer **14** is made of a low resistance material such as W.

[0072] Meanwhile, source/drain regions **121** are provided in the p-type well region **120**. A gate electrode **20** is provided on a channel region sandwiched between the source/drain regions **121**. The gate electrode **20** includes a gate insulation layer **21**, a cap layer **22**, and gate metal layers **23** and **24** provided thereon. The gate insulation layer **21** is composed of a high-k material such as HfAlO, and the cap layer **22** is composed of AlO, for example. In addition, the gate metal layers **23** and **24** are composed of the same materials as those of the gate metal layers **13** and **14** of the n-type MOSFET **101**, respectively.

[0073] The gate electrode can be processed with a high degree of accuracy, and a threshold voltage can be easily and correctly controlled in the CMOS semiconductor device **100**. The LWR of a gate length Lg can be 5% or less.

[0074] Specific structures of the gates of the CMOS semiconductor device **100** are as follows, for example.

[0075] n-type MOSFET: W/TiN/MgO (or LaO)/HfSiON/Si substrate

[0076] p-type MOSFET: W/TiN/AlO/HfSiON/Si substrate

[0077] A method for producing the CMOS semiconductor device **100** according to the first embodiment will be described with reference to FIGS. **1**A to **1**K. The same reference as that in FIG. **1** represents the same or corresponding part in the drawings. The production method includes the following step 1 to step 9.

[0078] Step 1: As shown in FIG. **1**A, the semiconductor substrate **105** composed of silicon is prepared. As described in FIG. **1**A, the n-type MOSFET **101** is formed on the left side, and the p-type MOSFET **102** is formed on the right side. In addition, the semiconductor substrate **105** is omitted after FIG. **1**B.

[0079] Then, a silicon oxide film (not shown) having a film thickness of 1 nm or less is formed on the semiconductor substrate **105**, and then an insulation layer **1** is formed thereon. The insulation layer **1** is composed of a high-k (high-dielectric) material such as HfSiON. The insulation layer **1** is formed by an ALD method, a MOCVD method, a sputtering method, or the like. According to need, a nitriding treatment or a heat treatment may be performed in the middle of or after this process.

[0080] The cap layer **22** composed of Al_2O_3 is formed on the insulation layer **1**. The cap layer **22** is about 1 nm in thickness, and made by the ALD method, the MOCVD method, the sputtering method, or the like. According to need, a heat treatment may be performed.

[0081] Then, a first TiN layer **31** is formed to be about 10 nm in thickness on the cap layer **22**, and then a SiN layer **33** is formed to be about 10 nm in thickness. These are formed by the sputtering method, a CVD method, or the like.

[0082] Step 2: As shown in FIG. **1**B, the SiN layer **33** in an n-MOSFET formation region is removed by dry etching using a photoresist (not shown) as an etching mask, for example. Then, the photoresist mask is removed, and the first TiN layer **31** and the cap layer **22** are removed by wet etching with H_2O_2, using the SiN layer **33** as an etching mask. The insulation layer **1** is hardly damaged through the above steps.

[0083] Then, the cap layer **12** composed of MgO or LaO is formed by the ALD method, the MOCVD method or the sputtering method, for example. The film thickness of the cap layer **12** is about 1 nm, but this is not necessarily the same as that of the cap layer **22** in a p-MOSFET formation region.

[0084] In addition, a Hf layer may be further formed on the cap layers **12** and **22**. In this case, the gate insulation layer has a structure of HfO/MgO/HfSiON in the n-type MOSFET, and the gate insulation layer has a structure of HfO/AlO/HfSiON in the p-type MOSFET.

[0085] Step 3: As shown in FIG. **1**C, a second TiN layer **32** is formed to be about 10 nm in thickness by the sputtering method or the CVD method, for example.

[0086] In addition, although the first and second TiN layers **31** and **32** are needed in the production steps, they do not remain in a final product. Therefore, they are preferably formed of the material which can be easily formed, high in selectivity, and easily removed. For example, polycrystalline Si may be used instead of TiN.

[0087] Step 4: As shown in FIG. **1**D, a SiN layer **34** is formed to be about 10 nm in thickness by the sputtering method or the CVD method, for example. Then, a resist mask **36** is formed in the n-MOSFET formation region.

[0088] Step 5: As shown in FIG. **1**E, the SiN layer **34** is selectively etched using the resist mask **36** as an etching mask. The etching stops on the second TiN layer **32**.

[0089] Step 6: As shown in FIG. **1**F, the resist mask **36** is selectively removed by plasma ashing or the like.

[0090] Step 7: As shown in FIG. **1**G, the second TiN layer **32** is selectively removed using the SiN layer **34** as an etching mask.

[0091] Step 8: As shown in FIG. **1**H, the SiN layers **33** and **34** and the exposed cap layer **12** are removed by wet etching.

[0092] Step 9: As shown in FIG. **1**I, the first and second TiN layers **31** and **32** are selectively removed by wet etching with H_2O_2, for example.

[0093] Step 10: As shown in FIG. **1**J, a TaN layer **3** composed of a mid-gap material having high heat resistance is formed to be 30 nm or less in thickness by a sputtering method, for example. As the mid-gap material, TiN may be used instead of TaN.

[0094] Then, a low-resistance tungsten layer **4** is formed on the TaN layer **3** by a sputtering method, for example. Its film thickness is 50 nm, for example.

[0095] Step 11: Finally, as shown in FIG. **1**K, the tungsten layer **4**, the TiN layer **3**, the cap layers **12** and **22**, and the insulation layer **1** are etched using a hard mask (not shown) composed of SiN as an etching mask, whereby the gate electrode **10** of the n-type MOSFET and the gate electrode **20** of the p-type MOSFET are formed.

[0096] In the above steps, the CMOS semiconductor device **100** is formed as shown in FIG. **1**K.

[0097] In addition, although not described in the above, the well region, the interlayer insulation layer, and the source/drain regions are formed by the same production steps as those of the conventional CMOS semiconductor device.

[0098] As described above, since the metal layers (the tungsten layer **4** and the TaN layer in this case) of the gate electrodes of the n-MOSFET and the p-MOSFET are made of the same material, in the steps of producing the CMOS semiconductor device **100** according to this embodiment, they can be etched in the same etching step (step 11 in this case). Therefore, a fine gate electrode having a gate length which is as small as 20 nm, for example, can be etched with a high degree of accuracy.

[0099] That is, according to the production method according to this first embodiment, since the gate metal layers for the n-type MOSFET and the p-type MOSFET are made of the same material, the controllability can be improved as compared with the case where different materials are etched at the same time.

[0100] For example, when the material of the gate metal layer is different from each other, its etched shape differs from each other, and the selectivity with the lower insulation layer (high-k material) becomes low. When the etched shape is different, a gate length and a channel length are different between the n-type MOSFET and the p-type MOSFET. In addition, when the selectivity becomes low, the semiconductor substrate **1** is also etched.

[0101] In addition, since the metal used to form the gate electrode finally is directly formed on the high-k material (insulation layer) such as HfSiON, a part of an element isolation region made of STI or the like is not etched by the etching step. Thus, preferable element isolation characteristic can be obtained.

Second Embodiment

[0102] A method for producing a CMOS semiconductor device according to a second embodiment is shown in FIGS. **2**A to **2**C.

[0103] According to this production method, a structure shown in FIG. **2**A is provided through the same steps as those shown in FIGS. **1**A to **1**F.

[0104] Then, as shown in FIG. **2**B, the second TiN layer **32** and the cap layer **12** are etched by selective etching using the SiN layer **34** as an etching mask.

[0105] Then, the tungsten layer **4** is formed on the whole surface by the CVD method or the sputtering method, for example.

[0106] Then, as shown in FIG. **2**C, the tungsten layer **4**, and the TiN layers **31** and **33** are etched using a hard mask (not shown) composed of SiN, for example, as an etching mask, whereby gate electrodes of the n-type MOSFET and the p-type MOSFET are formed.

[0107] In the above steps, a CMOS semiconductor device **150** is formed as shown in FIG. **2**C.

Third Embodiment

[0108] FIGS. **3**A to **3**H show a method for producing a CMOS semiconductor device according to a third embodiment. The production method includes the following steps 1 to 8. According to this production method, the SiN layers **33** and **34** formed in the production method shown in FIGS. **1**A to **1**K in the first embodiment are not formed. In the drawings, the same references as those in FIGS. **1**A to **1**K show the same or corresponding parts.

[0109] Step 1: As shown in FIG. **3**A, the insulation layer **1** composed of HfSiON, for example, and the cap layers **12** and **22**, and TiN layers **31** and **32** are formed on the semiconductor substrate **105** (omitted after FIG. **3**B). These layers are made by roughly the same steps as those in FIGS. **1**A to **1**C except for the step of forming the SiN layer **33**.

[0110] Step 2: As shown in FIG. **3**B, the photoresist mask **36** is formed in the n-MOSFET formation region.

[0111] Step 3: As shown in FIG. **3**C, the TiN layer **32** is selectively removed by wet etching with H_2O_2, for example, using the resist mask **36** as an etching mask.

[0112] Step 4: As shown in FIG. **3**D, the resist mask **36** is removed by an ashing method. In this step, a surface of the cap layer **12** is exposed to an ashing environment.

[0113] Step 5: As shown in FIG. **3**E, the cap layer **12** on the insulation layer **1** is removed by wet etching using the TiN layers **31** and **32** as etching masks.

[0114] Step 6: As shown in FIG. **3**F, the TiN layers **31** and **32** are selectively removed.

[0115] Step 7: As shown in FIG. **3**G, the TaN layer **3** is formed to be 30 nm or less in thickness by a sputtering

method, for example. Here, TiN may be used instead of TaN. Then, the low-resistance tungsten layer **4** is formed on the TaN layer **3** by a sputtering method, for example. Its film thickness is 50 nm, for example.

[0116] Step 8: Finally, as shown in FIG. **3**H, the tungsten layer **4**, the TaN layer **3**, and the cap layers **12** and **22** are etched using a hard mask (not shown) composed of SiN, for example, as an etching mask, whereby the gate electrode **10** of the n-type MOSFET and the gate electrode **20** of the p-type MOSFET are formed.

[0117] According to the production method, since the SiN layer is not formed, the production steps can be simplified. Meanwhile, the surface of the cap layer **12** is exposed to the ashing environment in step 4 (FIG. **3**D). Therefore, the production method is preferably used in a case where the ashing step does not affect the device characteristics.

Fourth Embodiment

[0118] FIGS. **4**A to **4**H show a method for producing a CMOS semiconductor device according to a fourth embodiment. The production method includes the following steps 1 to 8. In the drawings, the same references as those in FIGS. **1**A to **1**K show the same or corresponding parts.

[0119] Step 1: As shown in FIG. **4**A, the insulation layer **1** composed of HfSiON is formed on a semiconductor substrate (not shown) and then an amorphous silicon layer **40** is formed by the CVD method or the like thereon.

[0120] Step 2: As shown in FIG. **4**B, a photoresist layer **51** is formed in the n-type MOSFET formation region. Then, Al ions **41** are implanted into the amorphous silicon layer **40** in the p-type MOSFET formation region using the photoresist layer **51** as an implantation mask.

[0121] Step 3: As shown in FIG. **4**C, the photoresist layer **51** is removed and then a photoresist layer **52** is formed in the p-type MOSFET formation region. Then, Mg ions **42** are implanted into the amorphous silicon layer **40** in the n-type MOSFET formation region, using the photoresist layer **52** as an implantation mask.

[0122] Step 4: As shown in FIG. **4**D, the photoresist layer **52** is removed. Thus, the Mg ions are implanted in the n-type MOSFET formation region of the amorphous silicon layer **40** and the Al ions are implanted in the p-type MOSFET formation region thereof.

[0123] Step 5: As shown in FIG. **4**E, a heat treatment is performed to segregate Mg and Al at an upper part and a lower part of the amorphous silicon layer **40**. The heat treatment is performed at a processing temperature of 600° C. for a processing time of 30 seconds by a RTA method, for example. As a result, as shown in FIG. **4**E, Mg segregated layers **45** and **46** are formed on the lower and upper parts of the amorphous silicon layer **40** in the n-type MOSFET formation region, and Al segregated layers **43** and **44** are formed on the lower and upper parts of the amorphous silicon layer **40** in the p-type MOSFET formation region.

[0124] Step 6: As shown in FIG. **4**F, the Mg segregated layer **46**, the Al segregated layer **44**, and the amorphous silicon layer **40** are removed by wet etching with a KOH aqueous solution, for example.

[0125] Step 7: As shown in FIG. **4**G, the Mg segregated layer **45** and the Al segregated layer **43** are oxidized by plasma oxidization with oxygen plasma, whereby the cap layer **12** composed of MgO and the cap layer **22** composed of AlO are formed.

[0126] Step 8: As shown in FIG. **4**H, the TiN layer **3** and the tungsten layer **4** are sequentially formed.

[0127] Finally, in the same step as step 11 (FIG. **1**K) in the first embodiment, the TiN layer **3** and the tungsten layer **4** are etched at the same time, and the cap layers **12** and **22**, and the insulation layer **1** are etched, whereby the gate electrodes are formed.

[0128] FIGS. **5**A to **5**C show a method for producing another CMOS semiconductor device according to the fourth embodiment.

[0129] According to this production method, after step 5 (FIG. **4**E), only the Mg segregated layer **46** and the Al segregated layer **44** formed on the upper part of the amorphous silicon layer **40** are etched, and the amorphous silicon layer **40** remains.

[0130] Then, as shown in FIG. **5**B, the amorphous silicon layers **40** in the n-type MOSFET formation region and the p-type MOSFET formation region are etched at the same time using a resist mask (not shown), for example. In addition, the Mg segregated layer **44**, the Al segregated layer **43**, and the insulation layer **1** are etched, whereby gate electrodes are formed.

[0131] Finally, a gate metal **48** composed of NiSi is formed by a reaction between amorphous silicon and nickel, using a step of producing a FUSI gate.

[0132] As described above, according to the production method according to the fourth embodiment, since the amorphous silicon layer is etched to form the gate electrodes of the n-type MOSFET formation region and the p-type MOSFET formation region at the same time, the process can be performed with a high degree of accuracy.

Fifth Embodiment

[0133] FIGS. **6**A to **6**H show a method for producing a CMOS semiconductor device according to a fifth embodiment. The production method includes the following steps 1 to 8. In the drawings, the same references as those in FIGS. **1**A to **1**K show the same or corresponding parts.

[0134] Step 1: As shown in FIG. **6**A, the insulation layer **1** composed of HfSiON is formed on a semiconductor substrate (not shown) and then an amorphous silicon layer **60** is formed by the CVD method or the like.

[0135] Step 2: As shown in FIG. **6**B, a TEOS (or SiN) layer **55** is formed in the n-type MOSFET formation region. Then, an Al layer **43** and an amorphous silicon layer **61** are formed by the sputtering method or the CVD method.

[0136] Step 3: As shown in FIG. **6**C, a heat treatment is performed to diffuse Al, and the Al layer **43** is formed on a surface of a polycrystalline silicon layer **63** and on the insulation layer **1**. In addition, in the heat treatment step, the amorphous silicon layer **61** becomes the polycrystalline silicon layer **63**.

[0137] Step 4: As shown in FIG. **6**D, the polycrystalline silicon layer **63** and the Al layer **43** are removed, so that the Al layer **43** remains only on the insulation layer **1** in the p-type MOSFET formation region.

[0138] Step 5: As shown in FIG. **6**E, the TEOS layer **55** is removed. Then, a TEOS layer **56** is formed in the p-type MOSFET formation region. Then, an Mg layer **44** and an amorphous silicon layer **64** are formed by the sputtering method or the CVD method.

[0139] Step 6: As shown in FIG. **6**F, a heat treatment is performed to diffuse Mg, and the Mg layer **44** is formed on a surface of a polycrystalline silicon layer **65** and on the insu-

lation layer **1**. In addition, in the heat treatment step, the amorphous silicon layer **64** becomes the polycrystalline silicon layer **65**.

[0140] Step 7: As shown in FIG. **6**G, the layers formed above the polycrystalline silicon layer **62** are all removed. Thus, there remain the insulation layer **1**, the Mg layer **44** formed on the insulation layer **1** in the n-type MOSFET formation region, and the Al layer **43** formed on the insulation layer in the p-type MOSFET formation region. In addition, plasma oxidation is performed with oxygen plasma, so that the cap layer **12** composed of MgO and the cap layer **22** composed of AlO are formed.

[0141] Step 8: As shown in FIG. **6**H, the TiN layer **3** and the tungsten layer **4** are sequentially formed.

[0142] Finally, in the same step as step 11 (FIG. **1**K) in the first embodiment, the TiN layer **3** and the tungsten layer **4** are etched at the same time, and then the cap layers **12** and **22**, and the insulation layer **1** are etched, whereby gate electrodes are formed.

[0143] As described above, according to the production method according to the fifth embodiment, since the gate electrodes of the n-type MOSFET formation region and the p-type MOSFET formation region are formed at the same time, the processing can be implemented with a high degree of accuracy.

Sixth Embodiment

[0144] FIGS. **7**A to **7**F show a method for producing a CMOS semiconductor device according to a sixth embodiment. The production method includes the following steps 1 to 6. In the drawings, the same references as those in FIGS. **1**A to **1**K show the same or corresponding parts.

[0145] Step 1: As shown in FIG. **7**A, a dielectric body composed of HfSiON or the like, and a polycrystalline silicon layer are laminated on the semiconductor substrate (not shown) composed of silicon, for example. Then, these are etched at the same time to form a gate electrode composed of the insulation layer **1** and a polycrystalline silicon layer **70** in each of the n-type MOSFET formation region and the p-type MOSFET formation region.

[0146] Since a gate metal of each gate electrode is composed of the polycrystalline silicon layer **70**, the high-accuracy processing can be implemented by one etching step. For example, a gate length of the gate electrode is about 20 μm.

[0147] Step 2: As shown in FIG. **7**B, a silicon oxide layer is formed on the whole surface by the CVD method, for example. Then, an upper surface is flattened by a CMP method, and an interlayer insulation layer **71** is formed.

[0148] Step 3: As shown in FIG. **7**C, a mask **72** (not shown in FIG. **7**C) is formed in the p-type MOSFET formation region, and the polycrystalline silicon **70** in the n-type MOSFET formation region is selectively removed.

[0149] Step 4: As shown in FIG. **7**D, a cap layer **73** composed of MgO, for example, a TaSiN layer **74**, and a tungsten layer **75** are sequentially formed on the mask **72**. These layers are formed by the ALD method, or the MOCVD method, for example.

[0150] Step 5: As shown in FIG. **7**E, the cap layer **73**, the TaSiN layer **74**, and the tungsten layer **75** are etched from the above. Then, a mask (not shown) is formed on the n-type MOSFET, and the polycrystalline silicon **70** of the p-type MOSFET is selectively etched. Then, a cap layer **76** composed of AlO, a Pt layer **77**, and the tungsten layer **75** are formed.

[0151] Step 6: As shown in FIG. **7**F, after flattening the surface by the CMP method, the interlayer insulation layer **71** is removed, and a gate electrode (replacement gate) is formed in each of the n-type MOSFET formation region and the p-type MOSFET formation region.

[0152] When this production method is used, the metal material having low heat resistance can be selected as the gate metal material, so that a range of options to choose materials can be expanded.

[0153] In addition, when the control of the threshold voltage is not sufficient only by selecting the high-k material, the threshold voltage can be adjusted by appropriately selecting a material of the gate metal.

Seventh Embodiment

[0154] According to the above embodiments **1** to **6**, as shown in FIG. **9**, the gate electrode of the n-type MOSFET and the gate electrode of the p-type MOSFET each have the insulation layer made of the common high-k material such as HfSiON, and the cap layer made of the different material such as nCap composed of LaO or MgO, for example, or pCap composed of AlO, for example. Thus, the threshold voltage is correctly controlled.

[0155] In addition, the metal layer (metal) formed on the cap layer is made of the same material in each gate electrode.

[0156] Alternatively, the gate electrodes of the n-type MOSFET and the p-type MOSFET may only have the same metal layer (metal) and have different insulation layers (n-high-k and p-high-k).

[0157] For example, even when produced to have the structure as shown in FIG. **9**, they finally have the structure as shown in FIG. **8** in some cases because the insulation layers composed of the common high-k materials react with the cap layers thereon by the heat treatment in the manufacturing step.

[0158] Specifically, the gate electrodes have the following stacked structures.

[0159] n-type MOSFET: W/TiN/HfMgO/Si substrate

[0160] p-type MOSFET: W/TiN/HfAlO/Si substrate

[0161] These structures are different from that in FIG. **9** in that the gate insulation layers have a two-layer structure instead of the one-layer structure.

[0162] In addition, as another structure, the gate electrodes may have the following structures.

[0163] n-type MOSFET: W/TiN/MgO/AlO/HfSiON/Si substrate

[0164] p-type MOSFET: W/TiN/AlO/MgO/HfSiON/Si substrate

[0165] Thus, the cap layer may have a two-layer structure. In addition, AlO and MgO may be exchanged in a vertical direction.

[0166] In addition, an additional cap layer may be inserted to only one of the n-type MOSFET and the p-type MOSFET. In this case, the gate electrodes have the following stacked structures.

[0167] n-type MOSFET: W/TiN/MgO/HfSiON/Si substrate

[0168] p-type MOSFET: W/TiN//HfSiON/Si substrate

[0169] Alternatively, SiO_2 or SiON is provided on the Si substrate, the cap layer is provided thereon, and the insulation layer composed of the high-k material such as HfSiON is provided thereon as follows.

[0170] n-type MOSFET: W/TiN/HfSiON/MgO/SiO_2 (SiON)/Si substrate

[0171] p-type MOSFET: W/TiN/HfSiON/AlO/SiO_2 (SiON)/Si substrate

[0172] In this case, in the case where a vertical relationship of the insulation layer and the cap layer is reversed, the cap layer composed of MgO or AlO can be arranged at a position close to the Si substrate. As a result, the threshold voltage can be controlled more easily.

Eighth Embodiment

[0173] After etching the gate electrode under the condition that both gate metals are composed of polycrystalline silicon as shown in FIG. **10**A, a final structure may become as shown in FIG. **10**B due to a reaction between polycrystalline silicon and Ni or Pt.

[0174] That is, the present invention is characterized in that since the gate electrodes of the n-type MOSFET and the p-type MOSFET are composed of the same gate metal, these gate electrodes can be formed at the same time in one etching step, so that the etching process can be performed with a very high degree of accuracy.

[0175] Therefore, as shown in FIG. **10**A and FIG. **10**B, after etching the gate metal, the materials of the gate metals may be different between the n-type MOSFET and the p-type MOSFET.

[0176] Specifically, the stacks at the time of etching of the gate electrode is as follows.

[0177] n-type MOSFET: Poly-Si/MgO/HfSiO/Si substrate

[0178] p-type MOSFET: Poly-Si/AlO/HfSiON/Si substrate

[0179] Then, the stacks of the final structure is as follows.

[0180] n-type MOSFET: FUSI/NiSi/MgO/HfSiO/Si substrate

[0181] p-type MOSFET: FUSI-PtSi/AlO/HfSiO/Si substrate

[0182] In addition, while the gate electrode structure has been mainly described in this embodiment, the other structures such as the source/drain are the same as those of the CMOS semiconductor device **100** shown in FIG. **1**. Furthermore, a HALO layer or an extension layer may be formed according to need.

Ninth Embodiment

[0183] FIG. **11** is a schematic view of a CMOS semiconductor device according to a ninth embodiment.

[0184] The CMOSFET has three kinds of structures as gate electrodes of n-type CMOSFETs as follows.

[0185] n-type MOSFET1: Poly-SI/TiN/LaO/HfSiO/Si substrate

[0186] n-type MOSFET2: Poly-SI/TiN/HfSiO/Si substrate

[0187] n-type MOSFET3: Poly-SI/TiN/AlO/HfSiO/Si substrate

In addition, while a SiO_2 film is provided on the surface of the Si substrate in FIG. **11**, it may be omitted.

[0188] As for the n-type MOSFETs 1 to 3, threshold voltages (Vth) are shifted to +0.2V (MOSFET1), +0.5V (MOSFET2), and +0.8V (MOSFET3) as compared with the structure in which the gate insulation layer is only composed of SiO_2.

[0189] On the other hand, three kinds of structures are used for gate electrodes of p-type CMOSFETs as follows.

[0190] p-type MOSFET1: Poly-SI/TiN/LaO/HfSiO/Si substrate

[0191] p-type MOSFET2: Poly-SI/TiN/HfSiO/Si substrate

[0192] p-type MOSFET3: Poly-SI/TiN/AlO/HfSiO/Si substrate

[0193] As for the p-type MOSFETs 1 to 3, threshold voltages (Vth) are shifted to −0.2V (MOSFET1), −0.5V (MOSFET2), and −0.8V (MOSFET3) as compared with the structure in which the gate insulation layer is only composed of SiO_2.

[0194] Since these gate electrodes are each formed of the same gate metal material, they can be made through only one etching step, so that the gate electrode can be high in processing accuracy.

[0195] In addition, three kinds of gate electrodes having different shift amounts of the threshold voltages are provided in each of the n-type and p-type MOSFETs. Therefore, an integrated CMOS semiconductor device containing a plurality of MOSFETs having different threshold voltages can be produced by combining the six kinds of gate electrodes.

1. A CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising:

a gate electrode of the n-type MOSFET having a first insulation layer composed of a high-k material, and a first metal layer provided on the first insulation layer and composed of a metal material; and

a gate electrode of the p-type MOSFET having a second insulation layer composed of a high-k material, and a second metal layer provided on the second insulation layer and composed of a metal material, wherein

the first insulation layer and the second insulation layer are composed of the different high-k materials, and the first metal layer and the second metal layer are composed of the same metal material.

2. The CMOS semiconductor device according to claim **1**, wherein

the first insulation layer is composed of the high-k material containing an element which is not contained in the second insulation layer, and the second insulation layer is composed of the high-k material containing an element which is not contained in the first insulation layer.

3. The CMOS semiconductor device according to claim **1** or **2**, wherein

the first insulation layer and the second insulation layer are each composed of the high-k material containing three or more kinds of elements in which only one kind is different from all the others and the others are the same.

4. The CMOS semiconductor device according to any one of claims **1** to **3**, wherein

the first insulation layer is composed of HfLaO or HfMgO, and the second insulation layer is composed of HfAlO.

5. A CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising:

a gate electrode of the n-type MOSFET having a first insulation layer containing a high-k material and a cap material, and a first metal layer provided on the first insulation layer and composed of a metal material; and

a gate electrode of the p-type MOSFET having a second insulation layer containing a high-k material and a cap material, and a second metal layer provided on the second insulation layer and composed of a metal material, wherein

the first insulation layer and the second insulation layer are each composed of the same high-k material and the cap materials different from one another, and the first metal layer and the second metal layer are composed of the same metal material.

6. The CMOS semiconductor device according to claim **5**, wherein

the first insulation layer is composed of a common high-k material layer formed on a surface of a semiconductor substrate, and a first cap material layer formed thereon, the second insulation layer is composed of a common high-k material layer formed on the surface of the semiconductor substrate, and a second cap material layer formed thereon, and the first cap material layer or the second cap material layer covers the semiconductor substrate positioned between the gate electrode of the n-type MOSFET and the gate electrode of the p-type MOSFET.

7. The CMOS semiconductor device according to claim **5** or **6**, wherein

the first insulation layer comprises the high-k material layer composed of HfO_2, HfSiO or its nitride, and the cap material layer composed of LaO or MgO, and

the second insulation layer comprises the high-k material layer composed of HfO_2, HfSiO or its nitride, and the cap material layer composed of AlO.

8. The CMOS semiconductor device according to any one of claims **1** to **7**, wherein

the first metal layer and the second metal layer are each composed of one material selected from a group including TiN, TaN, TaSiN, NiSi, PtSi, and $CoSi_2$.

9. A method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising the steps of:

preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region;

forming a high-k material layer, a first cap layer, and a first metal layer sequentially on the semiconductor substrate;

removing the first cap layer and the first metal layer except for those in the p-type MOSFET formation region;

forming a second cap layer and a second metal layer sequentially on the semiconductor substrate;

removing the second metal layer except for that in the n-type MOSFET formation region;

removing the second cap layer provided between the n-type MOSFET formation region and the p-type MOSFET formation region, using the first metal layer and the second metal layer as masks;

removing the first metal layer and the second metal layer;

forming a gate metal material layer on the semiconductor substrate; and

forming a gate metal layer of a gate electrode of each of the n-type MOSFET and the p-type MOSFET by etching the gate metal material layer in the same etching step.

10. A method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising the steps of:

preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region;

forming a high-k material layer, a first cap layer, a first metal layer, and a first silicon insulation layer sequentially on the semiconductor substrate;

removing the first cap layer, the first metal layer, and the first silicon insulation layer except for those in the p-type MOSFET formation region;

forming a second cap layer, a second metal layer, and a second silicon insulation layer sequentially on the semiconductor substrate;

removing the second metal layer and the second silicon insulation layer except for those in the n-type MOSFET formation region;

removing the second cap layer provided between the n-type MOSFET formation region and the p-type MOSFET formation region, using the first silicon insulation layer and the second silicon insulation layer as masks;

removing the first silicon insulation layer and the second silicon insulation layer;

removing the first metal layer and the second metal layer;

forming a gate metal material layer on the semiconductor substrate; and

forming a gate metal layer of a gate electrode of each of the n-type MOSFET and the p-type MOSFET by etching the gate metal material layer in the same etching step.

11. The method for producing a CMOS semiconductor device according to claim **9** or **10**, wherein

the gate metal material layer has a laminated structure of a mid-gap material layer and a low-resistance material layer.

12. The method for producing a CMOS semiconductor device according to claim **11**, wherein

the mid-gap material is composed of TiN, and the low-resistance material is composed of W.

13. A method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising steps of:

preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region;

forming a high-k material layer, a first cap layer, a first metal layer, and a first silicon insulation layer sequentially on the semiconductor substrate;

removing the first cap layer, the first metal layer, and the first silicon insulation layer except for those in the p-type MOSFET formation region;

forming a second cap layer, a second metal layer, and a second silicon insulation layer sequentially on the semiconductor substrate;

removing the second metal layer and the second silicon insulation layer except for those in the n-type MOSFET formation region;

removing the second cap layer formed on a side wall or an upper surface of the first metal layer and the first silicon insulation layer;

removing the first silicon insulation layer and the second silicon insulation layer.

removing the first metal layer and the second metal layer;

forming a gate metal material layer on the semiconductor substrate; and

forming a gate metal layer of a gate electrode of each of the n-type MOSFET and the p-type MOSFET by etching the gate metal material layer in the same etching step.

14. The method for producing a CMOS semiconductor device according to any one of claims **9** to **13**, wherein

the first metal layer and the second metal layer are each composed of one material selected from a group including TiN, TaN, TaSiN, NiSi, PtSi, and $CoSi_2$.

15. The method for producing a CMOS semiconductor device according to any one of claims **10** to **13**, wherein

the first silicon insulation layer and the second silicon insulation layer are each composed of silicon nitride.

16. A method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising the steps of:

preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region;

forming a high-k material layer and an amorphous silicon layer, on the semiconductor substrate;

implanting first metal ions in the amorphous silicon in the p-type MOSFET formation region;

implanting second metal ions in the amorphous silicon in the n-type MOSFET formation region;

segregating a first segregated layer of a first metal and a second segregated layer of a second metal, in a boundary between the high-k material layer and the amorphous silicon layer by a heat treatment;

removing the amorphous silicon layer;

making a first cap layer and a second cap layer by oxidizing the first segregated layer and the second segregated layer;

forming a gate metal material layer on the semiconductor substrate; and

forming a gate metal layer of a gate electrode of each of the n-type MOSFET and the p-type MOSFET, by etching the gate metal material layer in the same etching step.

17. A method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising the steps of:

preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region;

forming a high-k material layer and a silicon layer, on the semiconductor substrate;

depositing a first metal on the silicon layer in the p-type MOSFET formation region;

segregating a first segregated layer of the first Metal, in a boundary between the high-k material layer and the silicon layer by a heat treatment;

forming a deposit layer of a second metal, on the silicon layer in the n-type MOSFET formation region;

segregating a second segregated layer of the second metal, in a boundary between the high-k material layer and the silicon layer by a heat treatment;

removing the silicon layer;

making a first cap layer and a second cap layer by oxidizing the first segregated layer and the second segregated layer;

forming a gate metal material layer on the semiconductor substrate; and

forming a gate metal layer of a gate electrode of each of the n-type MOSFET and the p-type MOSFET, by etching the gate metal material layer in the same etching step.

18. A method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising the steps of:

preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region;

forming a high-k material layer on the semiconductor substrate;

forming a first cap metal layer in the n-type MOSFET formation region and a second cap metal layer in the p-type MOSFET formation region;

forming a polycrystalline silicon layer on the semiconductor substrate;

forming a polycrystalline silicon gate layer in each of the n-type MOSFET formation region and the p-type MOSFET formation region, by etching the polycrystalline silicon layer in the same etching step; and

making the polycrystalline silicon gate layers of the n-type MOSFET formation region and the p-type MOSFET formation region into silicide metal gate layers composed of different materials.

19. A method for producing a CMOS semiconductor device having an n-type MOSFET and a p-type MOSFET, comprising the steps of:

preparing a semiconductor substrate defined by an n-type MOSFET formation region and a p-type MOSFET formation region;

forming a high-k material layer and a polycrystalline silicon layer, on the semiconductor substrate;

forming a polycrystalline silicon gate layer in each of the n-type MOSFET formation region and the p-type MOSFET formation region, by etching at least the polycrystalline silicon layer in the same etching step; and

forming an insulation layer to cover the polycrystalline silicon gate layer, on the semiconductor substrate, and forming an interlayer insulation layer provided by reducing a film thickness of the insulation layer to expose an upper part of the polycrystalline silicon gate layer;

removing the polycrystalline silicon gate in the n-type MOSFET formation region and forming a first cap layer and a gate metal layer instead; and

removing the polycrystalline silicon gate in the p-type MOSFET formation region and forming a second cap layer and a gate metal layer instead.

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