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(54) **FULLY DEPLETED SOI MULTIPLE THRESHOLD VOLTAGE APPLICATION**

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(22) Filed: **Mar. 29, 2005**

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(51) **Int. Cl.**
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H01L 27/12 (2006.01)
H01L 31/392 (2006.01)

(52) **U.S. Cl.** **257/348**; 257/E21.623; 257/E21.637

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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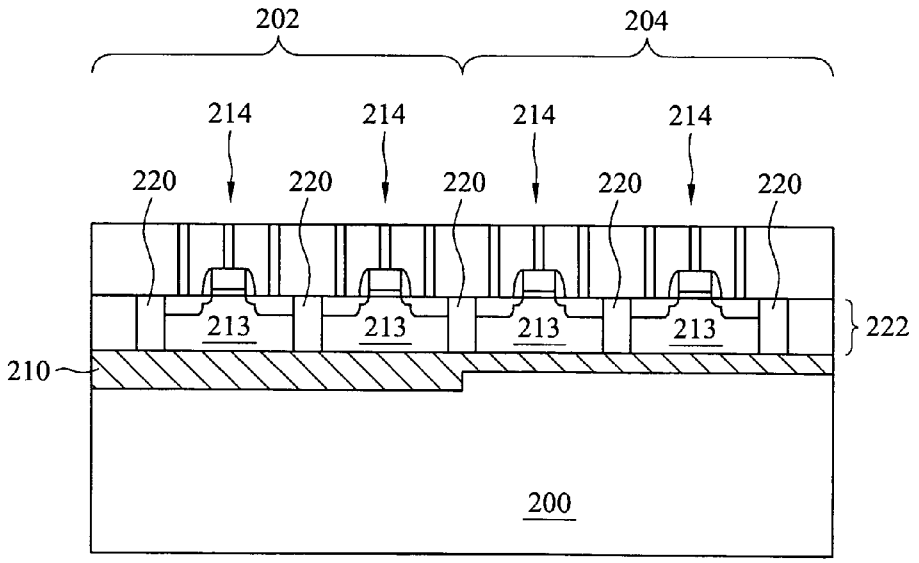
(57) **ABSTRACT**

An integrated circuit comprises a substrate and a buried dielectric formed in the substrate. The buried dielectric has a first thickness in a first region, a second buried dielectric thickness in a second region, and a step between the first and second regions. A semiconductor layer overlies the buried dielectric.

31 Claims, 9 Drawing Sheets



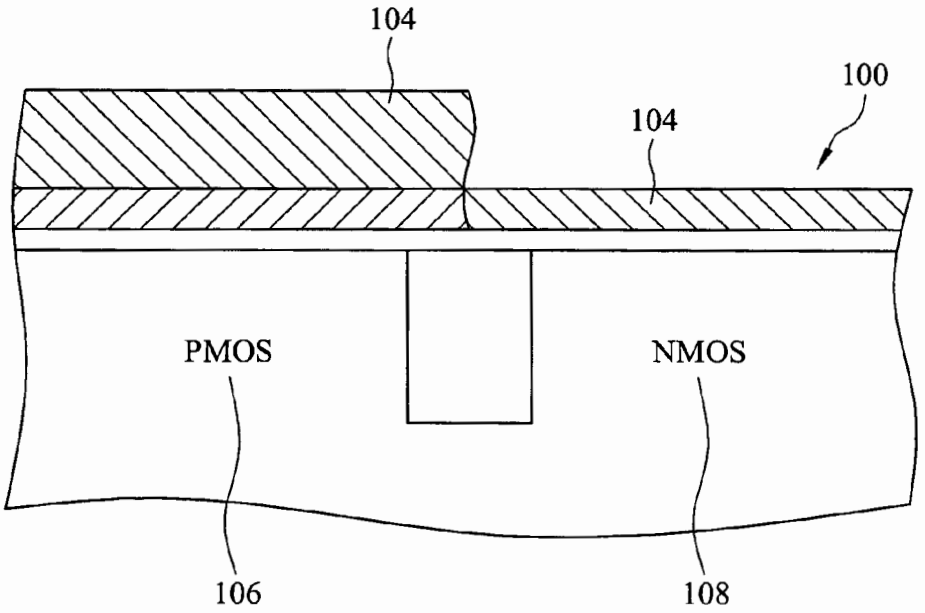


Fig. 1a
(PRIOR ART)

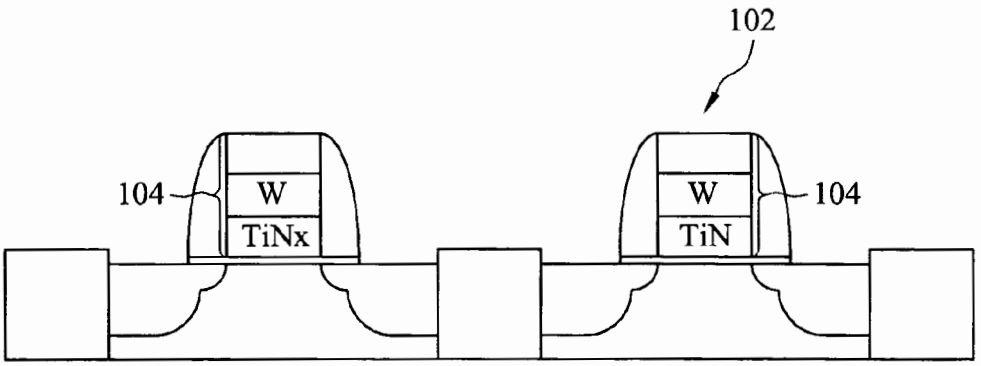


Fig. 1b
(PRIOR ART)

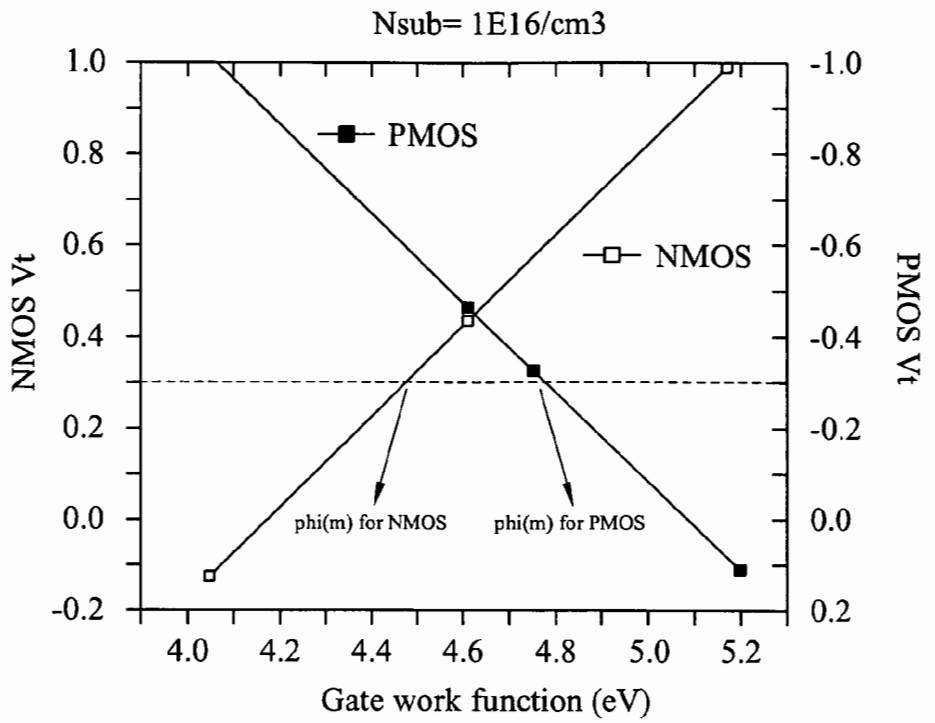

Nsub= 1E16/cm3
PMOS
NMOS
NMOS Vt
PMOS Vt
phi(m) for NMOS
phi(m) for PMOS
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-1.0
-0.8
-0.6
-0.4
-0.2
0.0
0.2
4.0
4.2
4.4
4.6
4.8
5.0
5.2
Gate work function (eV)

Fig. 1c

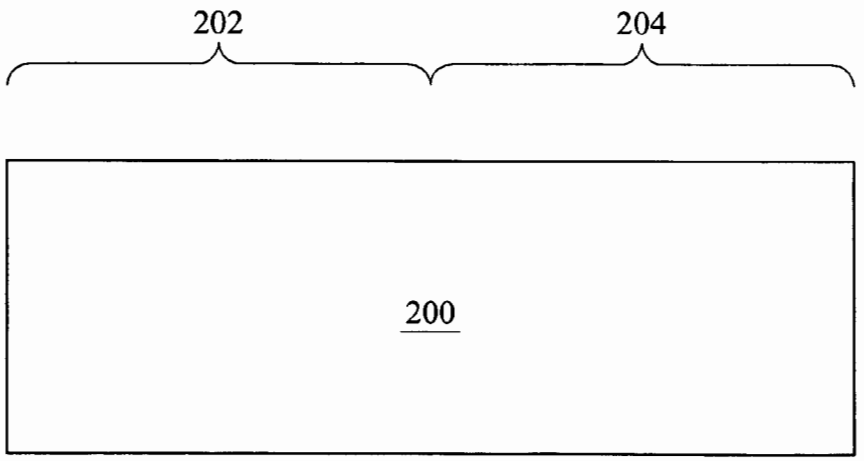

202
204
200

Fig. 2a

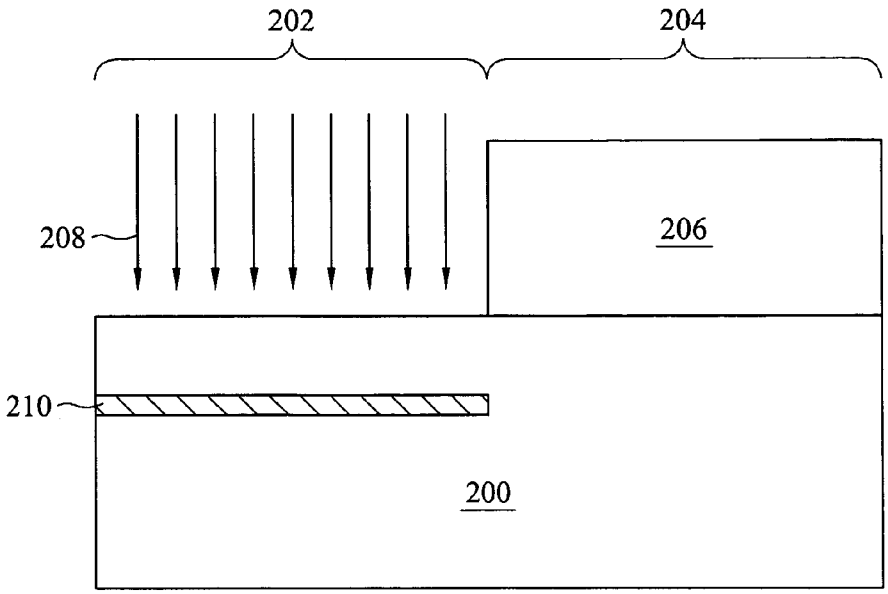

202
204
208
206
210
200

Fig. 2b

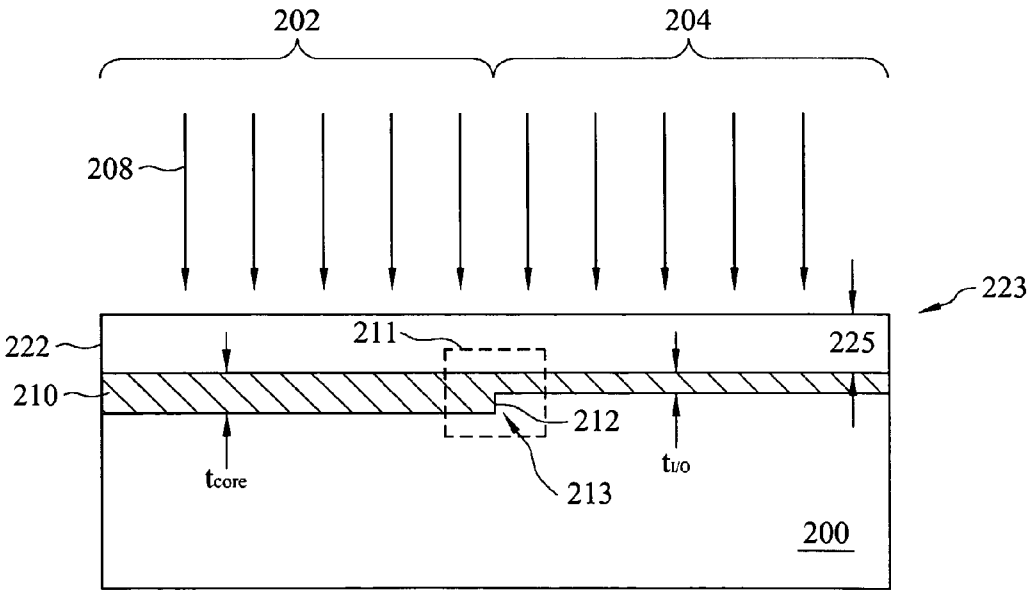

202
204
208
223
222
211
225
210
212
t_{core}
$t_{I/O}$
213
200

Fig. 2c

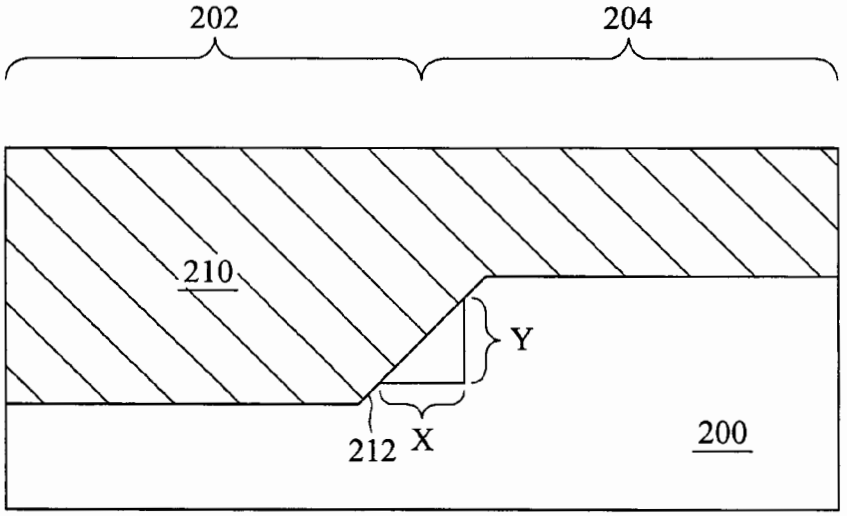

202
204
210
Y
212
X
200

Fig. 2d

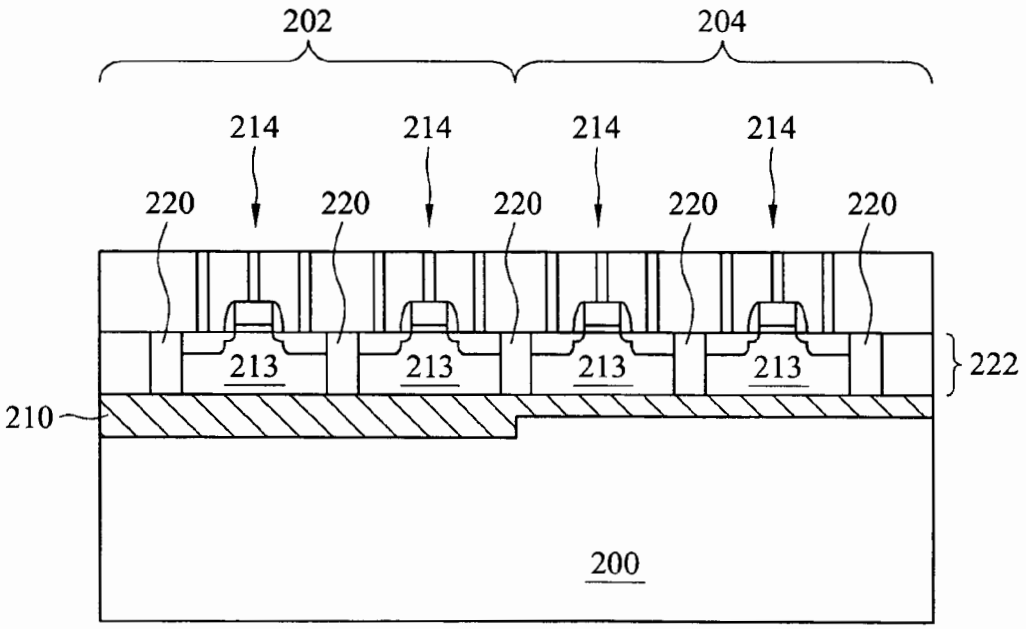

202
204
214
214
214
214
220
220
220
220
220
213
213
213
213
222
210
200

Fig. 2e

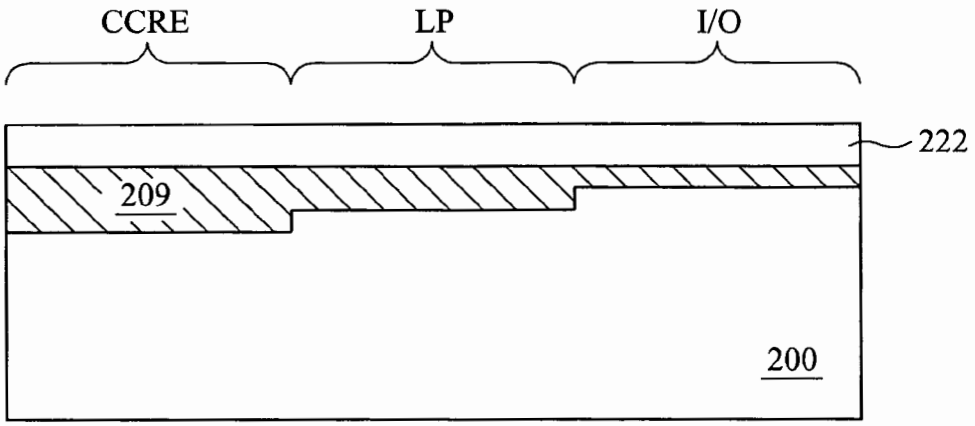


Fig. 2f

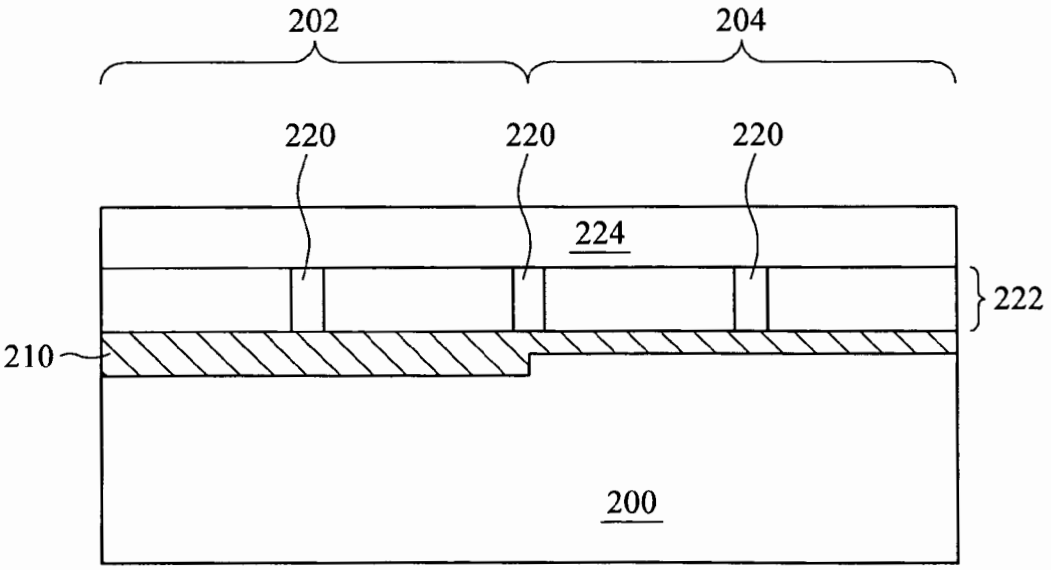


Fig. 3a

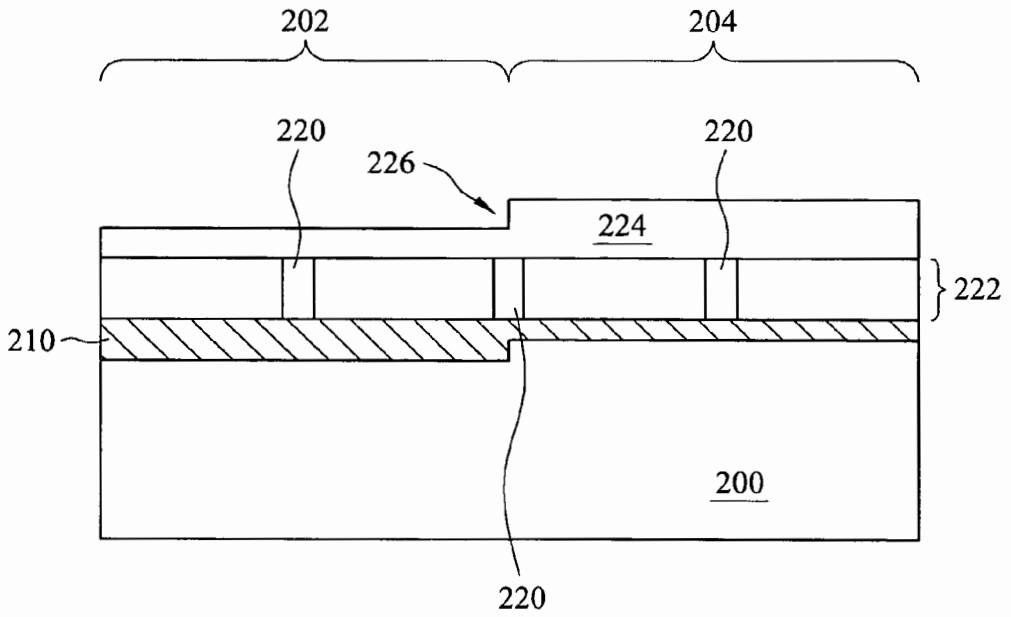

202
204
220
226
220
224
222
210
200
220

Fig. 3b

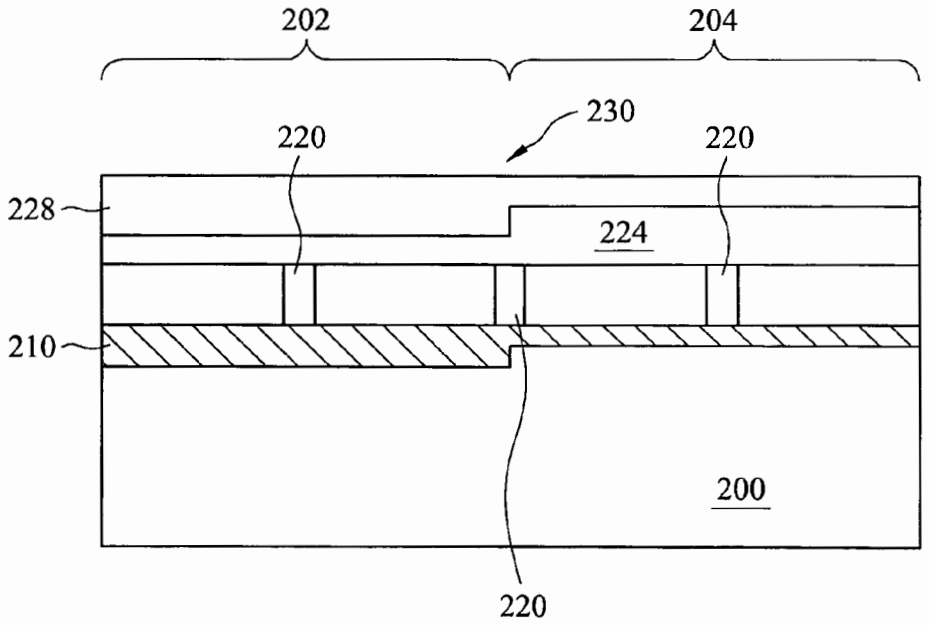

202
204
230
220
220
228
224
210
200
220

Fig. 3c

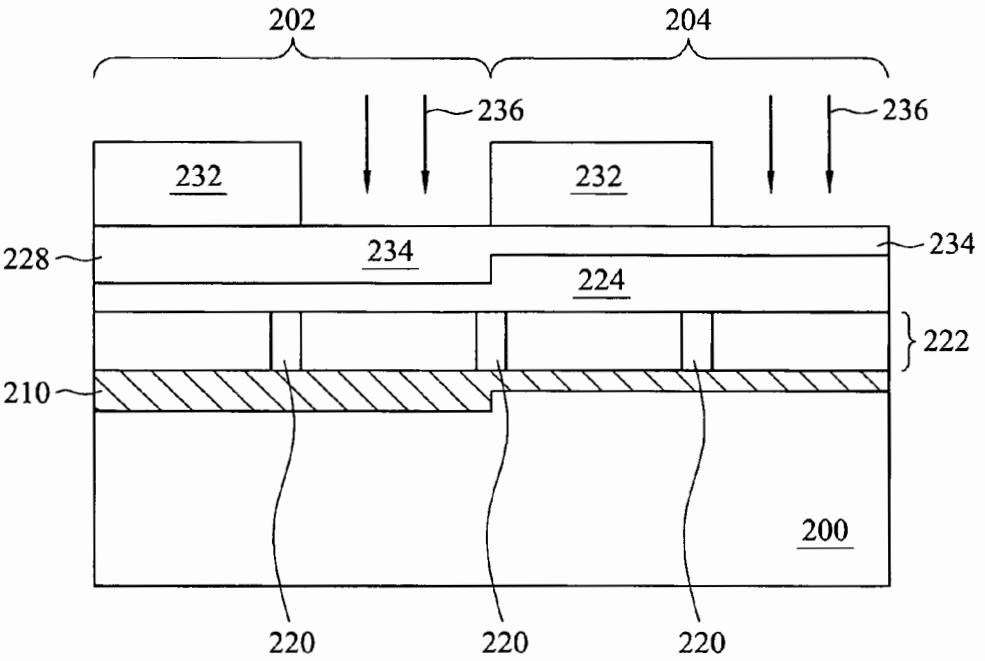

202
204
236
236
232
232
228
234
234
224
222
210
200
220
220
220

Fig. 3d

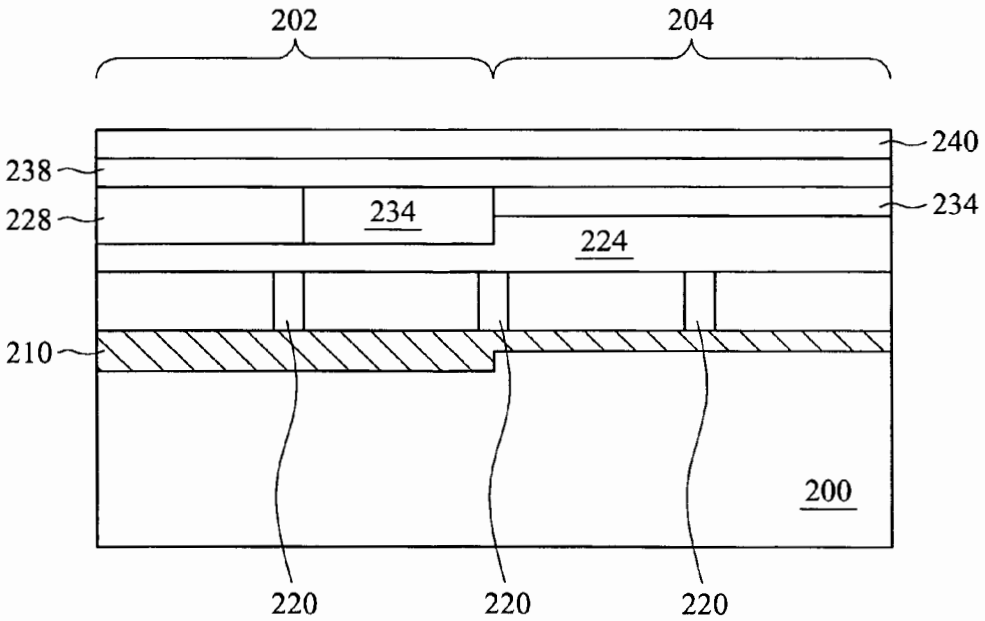

202
204
240
238
228
234
234
224
210
200
220
220
220

Fig. 3e

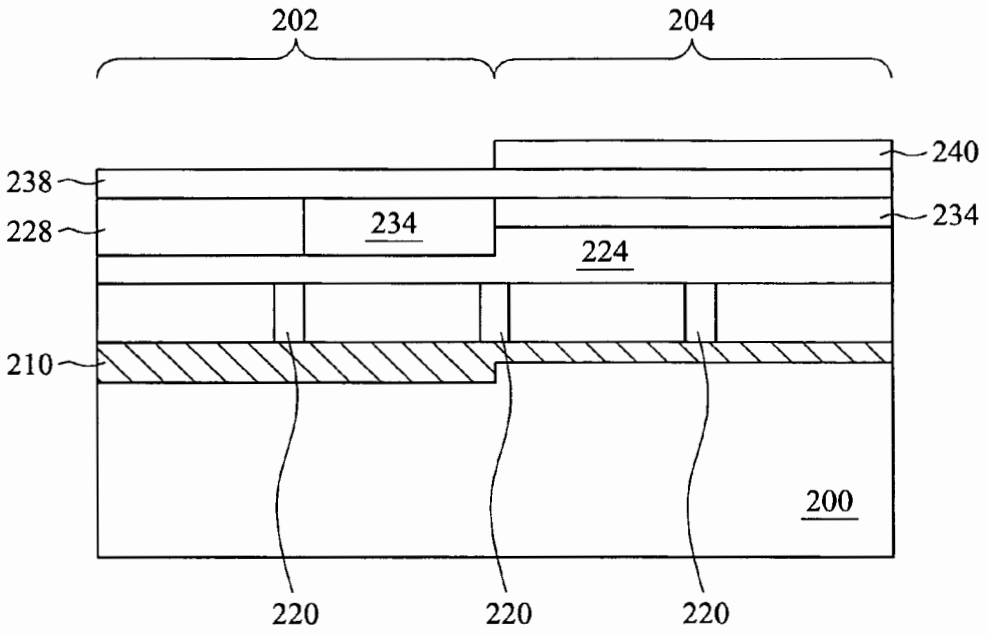

202
204
240
238
234
228
234
224
210
200
220
220
220

Fig. 3f

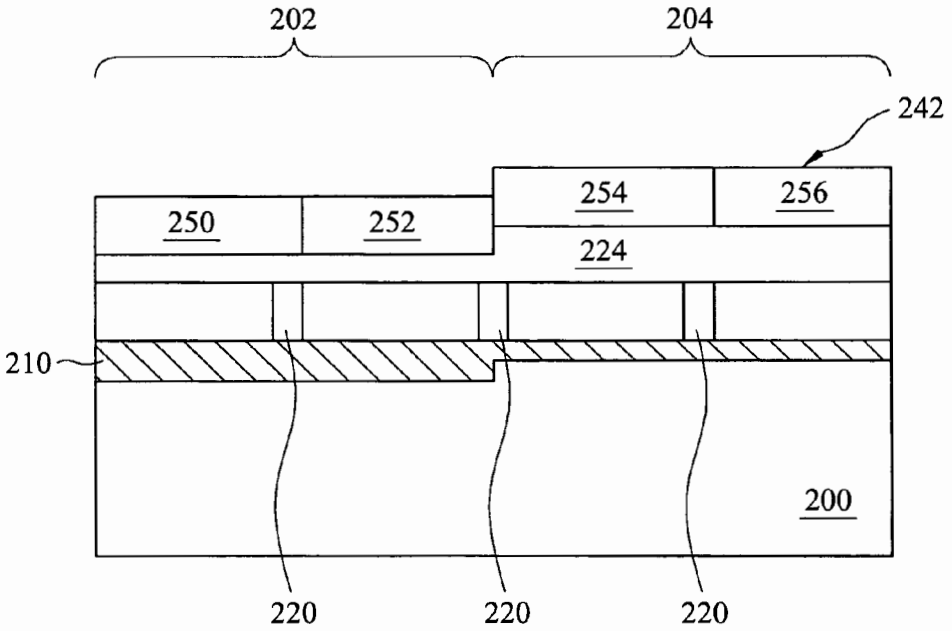

202
204
242
254
256
250
252
224
210
200
220
220
220

Fig. 3g

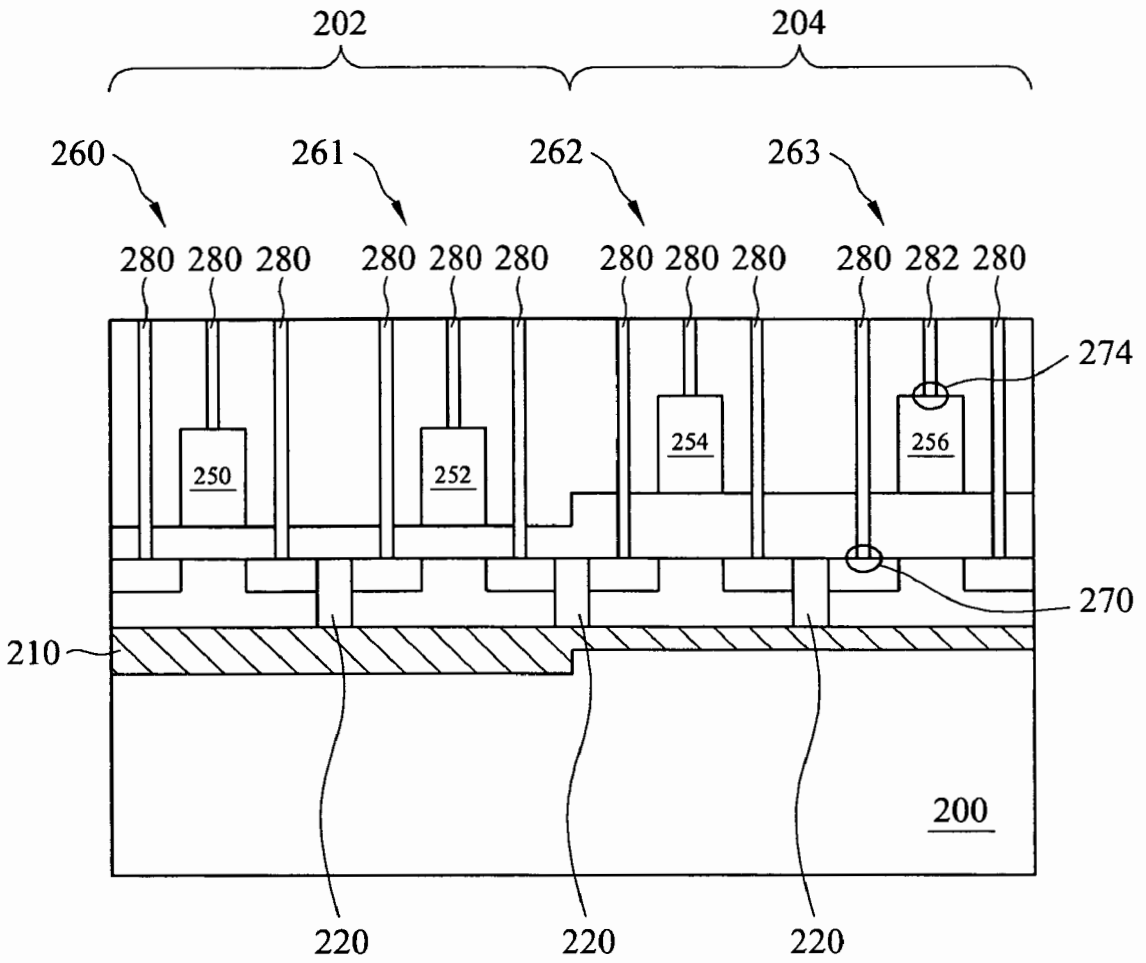

202
204
260
261
262
263
280 280 280 280 280 280 280 280 280 280 282 280
274
250
252
254
256
270
210
200
220
220
220

Fig. 3h

FULLY DEPLETED SOI MULTIPLE THRESHOLD VOLTAGE APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/566,040, filed on Apr. 28, 2004, entitled Fully Depleted SOI Multiple Threshold Voltage Application, which application is hereby incorporated herein by reference.

TECHNICAL FIELD

The present invention relates generally to semiconductor devices, and more particularly to a system and method for a fully depleted SOI multiple threshold voltage application.

BACKGROUND

In order to produce competitive electronic devices, it is often desired to produce semiconductor chips with several different regions (e.g., core region, low power region, I/O region) having semiconductor devices that vary according to speed and power, for example. Semiconductor devices that provide some or all of these features include silicon-on-insulator (SOI) devices. An existing challenge in SOI technology, however, is forming thin Si channel SOI I/O devices with significant voltage threshold (V_{th}) control. For example, in an SOI I/O application, a higher V_{th} is necessary because SOI devices suffer from a larger drain induced barrier lowering (DIBL) effect (which is caused by the floating body characteristics) than do bulk silicon wafer devices. Further, the higher voltages typically applied in the I/O regions increase the concern regarding leakage current. Overcoming these shortcomings will become increasingly significant as SOI device thickness is scaled down to improve performance and to reduce the floating body effects.

Several known methods attempt to control V_{th} by controlling the body potential of the SOI transistor. A first method is to tie the transistor body to a fixed voltage level through a substrate contact. However, despite reducing the floating body effect (FBE) in SOI devices, the body-tied method may suffer from area and speed penalties. In addition, the benefits obtained by the body-tied method may diminish as SOI silicon thicknesses scale downward because the increasing body resistance will make the body contact useless.

Another known body method for controlling V_{th} is channel region doping. Despite raising the V_{th}, however, channel implants reduce the depletion ability of an SOI device, thereby incurring performance degradation from the FBE.

Another commonly used method for FBE reduction is to fully deplete (FD) the channel region of the SOI device by thinning the silicon thickness. The FD SOI device enables an additional impact ionization (I-I) induced carrier sweep out of the channel, thereby suppressing the FBE. Substantial suppression of the FBE in the transistor channel region significantly enhances voltage threshold control.

Biasing the body region of an SOI transistor is conventionally an important part of device V_{th} control, and thinning the silicon body thickness has become a preferred method that contributes to V_{th} control. However, there is still a need for SOI technology with the capacity to provide sufficient back gate bias to achieve desired V_{th} values.

Another known and accepted method of achieving a desired V_{th} is to modify the gate electrode work function by modifying the material composition of the gate electrode. FIGS. **1***a* and **1***b* show known devices **100** and **102**, in which the gate electrode **104** material composition, and correspondingly the gate electrode **104** work function, is varied to control the voltage threshold of the devices. The CMOS structure **100** shown in FIG. **1***a* is disclosed by Polishchuk, et al. in a paper entitled "Dual Work Function Metal Gate CMOS Transistors by Ni—Ti Interdiffusion," IEEE Electron Device Letters, Vol. 23, No. 4, April 2002, incorporated herein by reference. FIG. **1***a* shows a gate electrode **104** comprising nickel and titanium over the PMOS region **106** and comprising titanium over the NMOS region **108**.

The FD SOI transistors **102** shown in FIG. **1***b* and disclosed by H. Wakabayashi in a paper entitled "A Novel W/TiNx Metal Gate CMOS Technology Using Nitrogen-Concentration-Controlled TiNx Film," IEEE IEDM, December 1999, which paper is incorporated by reference herein, have gate electrode **104** material compositions of tungsten W, titanium Ti, a first concentration of nitrogen N and a second concentration of nitrogen Nx. The variation of material composition varies the gate work function of each gate electrode **104**, thereby varying the voltage threshold of the FD SOI transistors **102**.

FIGS. **1***a* and **1***b* show gate electrode material composition variation within a small region of the chip. It is difficult, however, to apply different gate work function materials for SOI core applications and I/O device applications on the same chip, for example. In the conventional circuit application, the threshold voltage for a 3.3 eV I/O device is about 0.65 eV and the threshold voltage for a 1.0 eV core device is about 0.2 eV. The target threshold voltages are achieved by using a well or a pocket implantation in the bulk substrate. However, for a fully-depleted SOI device, the threshold voltage cannot be adjusted by the channel or pocket implantation because heavy substrate concentration will turn the FD device into a partially depleted device and degrade the performance. One method to achieve a different threshold voltage for a fully depleted SOI device is to change the gate work function. This can be demonstrated with reference to the following formula:

$$Vth = \underbrace{\boxed{\Phi_{ms} - \frac{Q_f}{C_{ox}}}}_{V_{FB}} + \Phi_s + \frac{\sqrt{2\varepsilon q N_{A(D)} \Phi_s}}{Cox}$$

For example, if we keep the Na (substrate concentration) constant, we may need another variable to control the threshold voltage to a desired value in a different application. The gate workfunction (ϕm) is a good candidate for V_{th} tuning because recently metal gate development has become mainstream technology. This is because metal gates not only improve gate resistance, but they also show better characteristics, compared to polysilicon, in integrating with high-k dielectric materials, as illustrated in FIG. **1***c*.

SUMMARY OF THE INVENTION

These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by preferred embodiments of the present invention, which provide for a fully depleted SOI multiple threshold voltage application. In other embodiments, the present invention provides for an integrated circuit having fully depleted SOI multiple threshold voltage devices and non-SOI multiple threshold voltage devices.

In accordance with an illustrative embodiment of the present invention, an integrated circuit comprises a substrate

and a buried dielectric formed in said substrate. The buried dielectric has a first thickness in a first region, a second buried dielectric thickness in a second region, and a step between said first and second regions. A semiconductor layer overlies said buried dielectric.

In accordance with another illustrative embodiment of the present invention, a semiconductor chip (also known as a die) has a first region and a second region. The semiconductor chip also has a substrate and a semiconductor layer overlying the substrate. The semiconductor chip further comprises a buried dielectric under the semiconductor layer formed at least partially in said substrate. The buried dielectric has a first thickness in said first region and a second thickness in said second region separated by a step. A first transistor has a first gate electrode and a second transistor has a second gate electrode formed in said first region. A third transistor has a third gate electrode and a fourth transistor has a fourth gate electrode formed in said second region.

In accordance with another illustrative embodiment of the present invention, a semiconductor chip comprises a substrate. The substrate comprises at least one buried dielectric, the buried dielectric having a first buried dielectric thickness in a first V_{th} region greater than a second buried dielectric thickness in a second V_{th} region, wherein the difference between the first V_{th} and the second V_{th} is about 0.15~0.45 eV. Specific examples would include a core region having a V_{th} of about 0.2 eV (less than 1.8 eV) and an I/O region having a V_{th} of about 0.65 eV, wherein the barrier dielectric thickness of the core region is greater than the barrier dielectric thickness of the I/O region. For other applications, the threshold voltage of the I/O region may be greater than 1.8 eV.

In accordance with another illustrative embodiment of the present invention, a semiconductor chip comprises a substrate. The substrate comprises at least one buried dielectric, the buried dielectric having a first buried dielectric thickness in a core region greater than a second buried dielectric thickness in an I/O region. The chip also comprises a first fully depleted silicon on insulator p-channel metal oxide semiconductor (FD SOI PMOS) transistor in the core region, the first FD SOI PMOS transistor with a first gate electrode overlying a first gate dielectric, the first gate electrode having a first work function. The semiconductor chip further comprises a first FD SOI n-channel metal oxide semiconductor (NMOS) transistor in the core region, the first FD SOI NMOS transistor with a second gate electrode overlying a second gate dielectric, the second gate electrode having a second work function. The semiconductor chip further comprises a second FD SOI PMOS transistor in the input/output (I/O) region, the second FD SOI PMOS transistor with a third gate electrode overlying a third gate dielectric, the third gate electrode having a third work function. The semiconductor chip still further comprises a second FD SOI NMOS transistor in the input/output region, the second FD SOI NMOS transistor with a fourth gate electrode overlying a fourth gate dielectric, the fourth gate electrode having a fourth work function. The first, second, third and fourth work functions are substantially different from one another.

DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1***a* and **1***b* show known dual work function metal gate transistors; and FIG. **1***c* graphically illustrates the relationship between threshold voltage and gate work function;

FIGS. **2***a*-**2***c* show cross-sectional views demonstrating steps in a first method of manufacturing in accordance with a first illustrative embodiment of the present invention;

FIG. **2***d* shows a cross-sectional view of a buried dielectric step;

FIG. **2***e* shows a first illustrative embodiment of the present invention;

FIG. **2***f* shows a second illustrative embodiment of the present invention; and

FIGS. **3***a*-**3***h* show cross-sectional views demonstrating steps of a second method of manufacturing in accordance with a third illustrative embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

The present invention will be described with respect to preferred embodiments in a specific context, namely a fully depleted SOI multiple threshold voltage application. The invention may also be applied, however, to other semiconductor devices and semiconductor applications having a need for multiple threshold voltages on the same substrate.

A substrate **200**, shown in FIG. **2***a*, comprises a semiconductor substrate material. The substrate material is preferably a p-type doped substantially crystalline silicon material with a crystal orientation of <100>. Alternatively, the substrate **200** may be doped n-type and have a crystal orientation the same as the p-type doped substrate, or other crystal orientations such as <111> and <110>, for example. The substrate **200** may comprise any material suitable as a semiconductor substrate, such as gallium arsenide, indium phosphide, silicon, germanium, carbon, and combinations thereof, including buffer layers comprising graded proportions of semiconductor materials such as a graded silicon germanium buffer layer, for example. The substrate **200** may also be a strained semiconductor such as strained silicon or ceramic wafer, for example.

The substrate **200** has a core region **202** and an input/output (I/O) region **204**. Illustrative embodiments of the present invention include substrates with any number of regions having any number of voltage threshold requirements. For example, illustrative embodiments include substrates with regions designated for low noise applications. Transistors formed in I/O regions of semiconductor chips typically have a higher threshold voltage than transistors in the core regions of the same chip, for example.

Examples of I/O devices may include tri-state buffers, input buffers, and output buffers, for example. I/O devices may include electrostatic discharge (ESD) circuitry and may provide a tolerance to multiple voltages. I/O regions, such as the I/O region **204**, are typically formed on the outskirts of a chip, in parts remote from the center. Core regions, such as the core region **202**, are typically located in regions of a chip that are proximate the center. Other arrangements of the I/O and core regions are contemplated, however. Core regions **202** typically include transistors having high speed

and low power requirements for large scale integrated (LSI) circuits (e.g., ULSI, VLSI), such as processors, controllers, and application specific integrated circuits (ASICs), for example.

Referring to FIG. **2***b*, a mask **206** is deposited over the I/O region **204** of the substrate **200**, exposing the core region **202** of the substrate **200**. The substrate **200** is subjected to implantation of a dielectric material **208** into exposed portions of the silicon substrate **200**, forming a buried dielectric **210**. The implantation process is preferably an oxygen implant process, such as separation by implanted oxygen (SIMOX). The implantation process may alternatively be separation by implanted nitrogen (SIMNI), separation by implanted oxygen and nitrogen, or internal thermal oxidation (ITOX), for example. The SIMOX implantation step preferably includes ion implantation of oxygen (e.g., 1.8×10^{18} per cm^2) with substrate temperatures greater than about 600 degrees Celsius.

The implantation of other materials such as nitrogen and hydrogen may be performed concurrently or subsequently. For example, the buried dielectric **210** may be a nitrided oxide or a hydrogenated oxide composite of silicon oxide. Implanting nitrided oxide contributes to the prevention of impurity dopant diffusion into the buried oxide, thereby preventing device performance degradation. Impurity dopant diffusion may occur from impurity dopants implanted during a well formation manufacturing step, such as for n-type wells (n wells), for example. As another example, carbon may be implanted to form a silicon carbide layer.

Referring to FIG. **2***c*, the mask **206** is stripped and dielectric material **208**, preferably oxygen, is again implanted into the core region **202** and the I/O region **204** of the silicon substrate **200**. The second oxygen implantation step extends the buried dielectric **210** into the I/O region **204** of the silicon substrate **200** and thickens the buried dielectric **210** in the core region **202**. The thickness t_{core} of the buried dielectric **210** in the core region **202** is preferably about 1000 angstroms. The thickness of the buried dielectric **210** in the I/O region **204** $t_{I/O}$ is preferably about 300 angstroms. The thickness of the buried dielectric may alternatively range between about 50 angstroms and about 2000 angstroms.

After implantation, the SIMOX process includes a high temperature (e.g., about 1300 degrees Celsius) anneal of the substrate. In other illustrative embodiments, the steps of masking and buried dielectric implantation are repeated any number of times, forming a buried dielectric of any number of thicknesses in any number of regions on the wafer.

The buried dielectric **210** isolates a semiconductor layer **222** from the wafer substrate **200**. The wafer **223**, comprising silicon **222** over an insulator **210**, is conventionally referred to as a silicon-on-insulator (SOI) wafer. The semiconductor layer **222** commonly has a thickness **225** of about 200 angstroms. However, the thickness **225** may range between about 50 angstroms and about 500 angstroms.

Although a buried dielectric step **215** in the dashed box **211** is shown with right angles, the step **211** preferably has a sloped sidewall **212**, as shown in FIG. **2***d*. FIG. **2***d* is an enlarged view of the dashed box **211**. The slope of the sidewall **212** is a thickness gradient, which is dependent on circuit design. For example, the gradient region may be a forbidden region for active devices but dummy devices or passive devices may be formed therein. This is because the gradient region may contain dislocations and a non-uniform capacitance, which may result in unstable electric performance of active devices. In illustrative embodiments, steps in the buried oxide may have different thickness gradients, however, each thickness gradient (in the vertical direction) preferably ranges between about 50 angstroms and about 200 angstroms. In some instances, a small spacing (less than about 0.3 um) may be desired between two active regions, one with a thin barrier dielectric and another with a thick barrier dielectric. In those instances, the step may be preferably no greater than about 1/10 of the spacing to avoid the threshold voltage fluctuation due to a closed active region.

Subsequent manufacturing steps form the first illustrative embodiment shown in FIG. **2***e*. Shallow trench isolation structures **220** isolate FD SOI transistors **214**. The transistors **214** over the thicker portion of the buried dielectric **210** in the core region **202** will have a lower threshold voltage than the transistors **214** over the thinner portion of the buried dielectric **210** in the I/O region **204**.

Varying the thickness of the buried dielectric **210** in different regions **202** and **204** of the same substrate **200** provides substantial control of the voltage threshold of the FD SOI devices **214**. For each transistor **214**, the underlying buried dielectric **210** acts as a capacitor dielectric between the anode, represented by the well or body region **213**, and the cathode, represented by the substrate **200** underlying the buried dielectric **210**, respectively. Varying the buried dielectric **210** thickness varies the capacitance tied to the transistor channel region in the well region **213**, thereby providing a different voltage threshold to the FD SOI devices **214** according to region **202** or **204**.

An FD SOI device **214** in the I/O region **204** has a higher possible V_{th} than a substantially similar device **214** in the core region **202** because of the difference in buried dielectric **210** thickness. In general, a thinner buried dielectric will provide a larger V_{th} tuning range, and a thicker buried dielectric will provide a smaller V_{th} tuning range.

In other illustrative embodiments, variation of the buried dielectric thickness is not limited to variation by region. The buried dielectric thickness may be varied on a chip or a wafer as desired for any number of areas having any number of sizes. Although the buried dielectric thickness is preferably varied in accordance with voltage threshold requirements for FD SOI devices, the buried dielectric thickness may alternatively be varied in accordance with other application requirements relating to semiconductor device operation, such as temperature (e.g., SOI self heating effect), current, and noise, for example.

Ion implantation steps that form the n-type or p-type well regions **213** in the semiconductor material **222** overlying the buried dielectric **210** may produce phosphorus or boron doped silicon oxide in top regions of the buried dielectric **210**. The diffusion of III-V type impurities into the buried dielectric **210** from overlying well regions **213** may also contribute to doped silicon oxide in regions of the buried dielectric **210**.

A second illustrative embodiment shown in FIG. **2***f* shows more than two buried dielectric **209** thicknesses for regions CORE, LP, and I/O on the same wafer substrate **200**. The FD SOI transistors subsequently formed in the silicon substrate **222** over the buried dielectric **209** will have different V_{th} in accordance with the underlying thickness of the buried dielectric **209**. Preferably, FD SOI transistors formed overlying the thickest portion of the buried dielectric **209** will have a lower V_{th} than FD SOI transistors formed in the LP region or the I/O region. FD SOI transistors formed in the LP region will have a higher V_{th} than the transistors formed in the CORE region. The FD SOI transistors formed in the I/O region will have a higher V_{th} than the transistors in the LP region and the CORE region.

A second method in accordance with a third illustrative embodiment, shown in FIGS. **3***a*-**3***h*, comprises the buried dielectric **210** of the first illustrative embodiment. In FIG. **3***a*, shallow trench isolation structures **220** are formed in the silicon region **222** overlying the buried dielectric **210**. Alternatively, other isolation structures (e.g., mesa isolation and LOCOS isolation) may be used. The silicon region **222** over the buried dielectric **210** is about 200 angstroms thick.

A gate dielectric **224** comprising silicon oxide is deposited. The thickness of the gate dielectric **224** is about 100 angstroms and may alternatively range between about 20 angstroms and about 100 angstroms. The gate dielectric may alternatively be formed of a high k dielectric material having a high dielectric constant, greater than about 4.0. The high k dielectric material may be a metal dielectric, including metal oxide such as Al_2O_3, Ta_2O_5, ZrO_2, and HfO_2, or HfSi for example. Various kinds of treatment can be used on high k dielectrics such as NH_3 anneal, O^+ anneal, NO anneal, and N_2O anneal, all well known.

A mask material such as a photoresist (not shown), covers the gate dielectric **224** in the I/O region **204**, and a portion of the exposed gate dielectric **224** in the core region **202** is removed, as shown in FIG. **3***b*. The resulting thickness of the gate dielectric **224** in the core region **202** is about 8 angstroms and may alternatively range between about 8 angstroms and about 20 angstroms. For emphasis, the step **226** formed between the core region **202** and the I/O region **204** is shown on a larger scale.

The thicker portion of the gate dielectric **224** will enable a higher voltage threshold in the FD SOI devices that will subsequently be formed in the I/O region **204**. In contrast, the FD SOI devices to be formed in the core region **202** will have a thinner gate dielectric **224** and a corresponding lower voltage threshold.

A layer of polysilicon **228** is deposited on the gate dielectric **224** as shown in FIG. **3***c*. Although, a polysilicon step (not shown) may form over the gate dielectric step **226** in the polysilicon surface **230**, the polysilicon step is a relatively insignificant surface feature and the polysilicon surface **230** is represented in FIG. **3***c* as being substantially planar for illustrative purposes.

FIG. **3***d* shows subsequent steps of forming a photoresist material **232** on the polysilicon **228**. Unmasked portions **234** of the polysilicon **228** are doped **236** with an n-type dopant, forming n-doped polysilicon region **234**. The dopant is preferably implanted by known ion implantation methods such as plasma immersion ion implantation (PIII) or metal plasma immersion ion implantation (MePIII), for example. The dopant is preferably phosphorus and may alternatively be arsenic, boron, mescaline (BF_2), hydrogen, nitrogen, oxygen, argon, or combinations thereof.

As shown in FIG. **3***e*, a first metal layer **238** and a second metal layer **240** are consecutively deposited over the gate dielectric **224**. The thickness of the first metal layer **238** is about 50 angstroms and the thickness of the second metal layer **240** is about 200 angstroms. The metal layers **238** and **240** are deposited using known deposition methods such as evaporation, sputtering, or various types of chemical vapor deposition such as plasma enhanced chemical vapor deposition, for example. The first metal layer **238** preferably comprises titanium and the second metal layer **240** preferably comprises platinum. However, the first **238** and second **240** metal layers may alternatively comprise nickel, palladium, platinum, iridium, ruthenium, rhodium, molybdenum, hafnium, aluminum, cobalt, tungsten, or combinations thereof, for example. Combinations may include metal alloys such as binary metal alloys, metal silicides, metal silicon nitrides, doped metal alloys, and doped silicide alloys, for example.

Subsequent photolithography steps mask a portion of the second metal layer **240** in the I/O region **204**, and the exposed portion of the second metal layer **240** in the core region **202** is removed, as shown in FIG. **3***f*. A wet etch or reactive ion etching may be used to remove portions of the second metal layer **240**.

A thermal anneal at about 500° C. for about 10 minutes causes the metals **238** and **240** to diffuse into the undoped **228** and doped **234** regions of the polysilicon, as shown in FIG. **3***g*. The anneal process produces a silicon titanium alloy gate electrode **250** and an n-doped silicon titanium alloy gate electrode **252** in the core region **202**. The anneal process also produces a titanium, platinum and silicon alloy **254** and an n-doped titanium, platinum and silicon alloy **256** in the I/O region **204**. In the illustrated embodiments, only a single gate electrode doping step is illustrated. One skilled in the art will recognize, however, that the gate electrodes can have differing doping concentrations and differing doping impurities. This can be accomplished, e.g., by multiple doping steps and by in-situ doping during deposition of gate polysilicon layer **228**. Preferably, the ratio of doping concentration between the gate electrodes is in the order of 10^5 or less.

FIG. **3***h* shows the structure of FIG. **3***g* after further processing produces FD SOI PMOS transistors **260**, **261** and FD SOI NMOS transistors **262**, **263**. Varying the material composition, and thereby the work function of the gate electrodes **250**, **252**, **254**, and **256**, provides a corresponding difference in voltage threshold between the FD SOI devices **260**, **261**, **262**, and **263**. The voltage thresholds of the FD SOI transistors **260**, **261**, **262**, and **263** in FIG. **3***h* are partially controlled by the work function of the gate electrodes **250**, **252**, **254**, and **256**. The gate electrode **250** has a work function ranging between about 4.7 eV and about 5.0 eV. The gate electrode **254** has a work function ranging between about 4.4 eV and about 4.7 eV. The gate electrode **252** has a work function ranging between about 4.2 eV and about 4.5 eV. The gate electrode **256** has a work function ranging between about 4.5 eV and about 4.8 eV.

The combination of buried dielectric **210** thickness variation, gate dielectric **224** thickness variation, and the variation of gate electrode **250**, **252**, **254**, and **256** work functions, provides a high degree of control of the voltage threshold variation of the FD SOI transistors **260**, **261**, **262**, and **263** and other devices on the same chip die **200** or in the same wafer.

The FD SOI transistors **260**, **261**, **262**, **263** used in the illustrative embodiments described herein are meant to be illustrative of depleted substrate devices in general. The present invention may also be applied to partially depleted devices such as partially depleted silicon-on-insulator (PD SOI) transistors, for example. Other devices in illustrative embodiments of the present invention include field effect transistors (FET) such as metal oxide semiconductor FETs (MOSFETs), metal semiconductor FETs (MESFETs), thin film transistors (TFTs), strained channel transistors, and double gate MOSFETs, for example. Although the present invention is suitable for any technology node, the present invention is preferably suitable for the 65 nm node and smaller technology nodes.

Contacts **280**, such as those coupled at the source **270**, drain **272** and gate **274** regions of the transistor **263**, for example, alter or otherwise form new work functions in the transistors. For example, silicide formed in the source region

270 of the FD SOI NMOS 263, provides a fifth work function in the source region as a result of the diffusion of the tungsten material in the contact 280 with the doped polysilicon in the top portion of source region 270. Another gate work function is provided by diffusion of the tungsten material in the contact 282 with the n-doped polysilicon and titanium of the gate electrode 256 in the top portion of the gate electrode 274.

The preferred embodiments of the present invention provide a significant advantage relating to the control of the voltage threshold of semiconductor devices, and specifically to fully depleted silicon-on-insulator devices in different circuit applications on a chip. The present invention may be used to include devices requiring thin and ultra-thin buried oxides on a single die, for example. Applications include core applications, low power applications, and I/O applications, for example. Improved control of the voltage threshold of devices in different applications provides more control of the drain induced barrier lowering in FD SOI devices, and enhanced device and circuit performance.

An advantage of the preferred embodiments of the present invention is that the buried dielectric thickness may be varied according to applications having transistors with different desired voltage thresholds, e.g., core applications, low power applications, and I/O applications. Another advantage is that different buried oxide thicknesses in the same wafer may be used to provide V_{th} adjustment substantially reserved for FD SOI back-gate biased devices requiring V_{th} adjustment, e.g., core applications, low power applications, and I/O applications.

Although preferred embodiments of the present invention and their advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, it will be readily understood by those skilled in the art that a fully depleted SOI multiple threshold voltage application may be varied while remaining within the scope of the present invention.

Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. An integrated circuit comprising:

a substrate;

a buried dielectric formed in said substrate, the buried dielectric having a first thickness in a first region and a second thickness in a second region, the first region designated for a first application requiring a first voltage threshold and the second region designated for a second application requiring a second voltage threshold, wherein the first application is a core application having a first threshold voltage and the second application is an input/output application having a second threshold voltage, wherein the second threshold voltage is greater than about 1.8 eV, and wherein the difference between the first threshold voltage and the second threshold voltage is about 0.45 eV or less; and

a semiconductor layer overlying said buried dielectric.

2. The integrated circuit of claim 1, wherein the buried dielectric has a substantially planar top surface.

3. The integrated circuit of claim 1, wherein a substantial portion of the substrate comprises crystalline silicon.

4. The integrated circuit of claim 1, wherein said semiconductor layer overlying the buried dielectric comprises strained silicon.

5. The integrated circuit of claim 1, wherein said semiconductor layer overlying the buried dielectric comprises a germanium containing semiconductor material.

6. The integrated circuit of claim 1, further comprising a step between said first and second regions, wherein said step is about 200 angstroms or less.

7. The integrated circuit of claim 6, wherein said step is a gradient region and further comprising a forbidden region overlying said gradient region wherein no active devices are formed.

8. The integrated circuit of claim 1, further comprising a fully depleted silicon-on-insulator transistor formed in said semiconductor layer.

9. The integrated circuit of claim 1, wherein the buried dielectric comprises silicon oxide.

10. The integrated circuit of claim 1, wherein the buried dielectric comprises nitrided oxide.

11. The integrated circuit of claim 1, wherein the buried dielectric comprises hydrogenated oxide.

12. The integrated circuit of claim 1, wherein the buried dielectric comprises Al_xO_y, wherein x is about 2 and y is about 3.

13. The integrated circuit of claim 1, wherein the buried dielectric comprises silicon carbide.

14. The integrated circuit of claim 1, further comprising:

a first transistor having a first gate electrode and a second transistor having a second gate electrode formed in said first region; and

a third transistor having a third gate electrode and a fourth transistor having a fourth gate electrode formed in said second region.

15. The integrated circuit of claim 14, wherein:

said first gate electrode is formed of a first material and has a first concentration of a first impurity therein and said second gate electrode is formed of a second material and has a second concentration of a second impurity therein; and

said third gate electrode is formed of a third material and has a third concentration of a third impurity therein and said fourth gate electrode is formed of a fourth material and has a fourth concentration of a fourth impurity therein.

16. The integrated circuit of claim 15, wherein said first material and said third material are substantially the same.

17. The integrated circuit of claim 15, wherein said second material and said fourth material are substantially the same.

18. The integrated circuit of claim 15, wherein said first and second concentrations have a ratio equal to about 105 or less.

19. The integrated circuit of claim 15, wherein said third and fourth concentrations have a ratio equal to about 105 or less.

20. The integrated circuit of claim 15, wherein said first and third impurities are the same impurity.

21. The integrated circuit of claim 15, wherein said second and fourth impurities are the same impurity.

22. The integrated circuit of claim **15**, wherein said first and third gate electrodes comprise a silicide of silicon and a first metal and wherein said second and fourth gate electrodes comprise a silicide of silicon and a second metal.

23. The integrated circuit of claim **22**, wherein said second and fourth gate electrodes further comprise said first metal.

24. The integrated circuit of claim **14**, further comprising:

a first gate dielectric having a first gate dielectric thickness underlying said first and second gate electrodes; and

a second gate dielectric having a second gate dielectric thickness underlying said third and fourth gate electrodes, wherein said second gate dielectric thickness varies from said first gate dielectric thickness by a predetermined amount.

25. The integrated circuit of claim **14**, wherein the first gate dielectric thickness is thinner than the second gate dielectric thickness.

26. The integrated circuit of claim **14**, wherein the first and third gate electrodes comprise titanium.

27. The integrated circuit of claim **15**, wherein the third and fourth gate electrodes comprise platinum.

28. The integrated circuit of claim **25**, wherein the first gate dielectric thickness ranges between about 8 angstroms and about 20 angstroms.

29. The integrated circuit of claim **25**, wherein the second transistor's gate dielectric thickness ranges between about 20 angstroms and about 100 angstroms.

30. The integrated circuit of claim **14**, further comprising a step in said buried dielectric and wherein said step is a gradient region and further comprising a forbidden region overlying said gradient region wherein no active devices are formed.

31. The integrated circuit of claim **14**, wherein the first transistor is a fully depleted silicon-on-insulator p-channel metal oxide semiconductor transistor (FD SOI PMOS) with a first work function ranging between about 4.7 electron-volts and about 5.0 electron-volts, the second transistor is an FD SOI n-channel metal oxide semiconductor (NMOS) device with a second work function ranging between about 4.2 electron-volts and about 4.5 electron-volts, the third transistor is an FD SOI PMOS device with a third work function ranging between about 4.4 electron-volts and about 4.7 electron-volts, and the fourth transistor is an FD SOI NMOS device with a fourth work function ranging between about 4.5 electron-volts and about 4.8 electron-volts.

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