

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING
COMPANY, LTD.,

Petitioner

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC

Patent Owner.

IPR2025-00832

U.S. Patent 8,796,779

**DECLARATION OF JAKUB KEDZIERSKI, PHD
IN SUPPORT OF INTER PARTES REVIEW OF U.S. PATENT 8,796,779**

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**TSMC-1003
U.S. Patent 8,796,779**

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I, Dr. Jakub Kedzierski, declare as follow:

1. I have been retained on behalf of Taiwan Semiconductor Manufacturing Company, Ltd. (“Petitioner” or “TSMC”), to provide this Declaration concerning technical subject matter relevant to the petition for Inter Partes Review (“Petition”) of U.S. Patent 8,796,779 (“the ’779 patent”). It is my understanding that the ’779 patent is currently assigned to Advanced Integrated Circuit Process LLC (“Patent Owner”).

2. I am over 18 years of age. I have personal knowledge of the facts stated in this Declaration and could testify competently to them if asked to do so. I have reviewed and am familiar with the specification and the claims of the ’779 patent and its prosecution history. In general, I will cite to the specification of a United States patent using the following formats: (Patent No., Col:Line Number(s)) or (Patent No., Paragraph Number(s)). For example, the citation (’779 patent, 1:1-10) points to the ’779 patent specification at column 1, lines 1-10. Also, for convenience, I use italics to denote limitations from the challenged claims.

3. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, I reviewed the documents listed in the

attached Appendix. I have also reviewed and am familiar with any other document referred to in this Declaration.

4. I have been asked to provide my technical opinions regarding how a person of ordinary skill in the art (“POSITA”) would have understood the claims of the ’779 patent at the time of the alleged invention. For purposes of whether the teachings of the prior art render the claims of the ’779 patent anticipated or obvious in the analysis applied in this document, I have been asked to assume the date of September 14, 2010, which I understand is the foreign application priority date. However, except as noted herein, my opinion would not change if the priority date of the ’779 patent was, e.g., May 24, 2011 which I understand is the PCT filing date or October 31, 2012, which I understand is the filing date of the ’779 patent. I have also been asked to provide my technical opinions on how concepts in the ’779 patent specification relate to claim limitations of the ’779 patent. In reaching the opinions provided herein, I have considered the ’779 patent, its U.S. prosecution history, the prosecution history of the foreign priority application (JP2010-20599) and the references cited in the Appendix, and have drawn as appropriate on my own education, training, research, knowledge, and personal and professional experience. To the extent that certain materials are discussed below but not cited in the Appendix, they are among the materials I have considered.

I. Qualifications

5. In formulating my opinions, I have relied on my knowledge, training, and experience in the relevant field, which I will summarize briefly. A more detailed summary of my background, education, experience, and publications is set forth in my curriculum vitae (“CV”), which is provided as TSMC-1004.

6. I have personal knowledge of the facts and opinions set forth in this declaration and believe them to be true. If called upon to do so, I would testify competently thereto. I have been warned that willful false statements and the like are punishable by fine or imprisonment, or both.

7. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the ’779 patent.

8. I received my Ph.D. in electrical engineering from the University of California at Berkeley in 2001, where I worked on novel transistor technologies. Among my projects at Berkeley, I was a co-inventor of the FinFET transistor. The FinFET device was later introduced by Intel as a manufacturable technology in

2012 and then became the dominant technology for electronic nodes after 20 nm, from 2014 to the current date. Currently, almost all of the high-performance chips in cellphones, laptops, personal computers, and servers use FinFET transistors. My other work at Berkeley included the fabrication of one of the first silicon nanowire transistors, and trigate metal source/drain transistors. At Berkeley I received the Paul Rappaport award from IEEE for best paper in 2001, and the Dimitry Angelakos award for assistance and mentorship given to junior graduate students.

9. Following my graduation, I joined IBM's flagship research center, T. J. Watson Research Center, from 2001 to 2005, as an RSM (Research Staff Member) and continued working on advanced silicon devices. At IBM, I built the first industrial FinFET, enabling IBM to obtain a several year lead time in advanced technology. Later, I advanced FinFET technology by incorporating critical components such as a metal gate, and a raised source/drain into the FinFET devices. At IBM, I also worked on metal gate integration, pioneering the full gate silicidation process with NiSi, and developing a segregation-based work function engineering technique for metal gates. This method allowed for the fabrication of metal gate transistors with appropriate threshold voltages and CMOS operation.

10. In 2005, I joined MIT Lincoln Laboratory, where I am still employed, and became the head of the Advanced Silicon Technology Group. I led a group of

over 40 researchers and support-staff with multiple programs on advanced electronics technology. These programs included multi-tier 3D transistor integration, low-power electronics, and graphene devices. My team built the first 3-layer 3D transistor technology, as well as the first top gated graphene transistor. The graphene transistor work won the IEEE George Smith award in 2009, for best paper in Electron Device Letters. My team developed custom electronics technology for the Department of Defense, including radiation hard electronics that can operate in radioactive environments, and better survive irradiation. My team also integrated fluidic and power elements into electronics technology, developing a glucose fuel cell, and a novel microfluidic technology based on electrowetting.

11. In 2012, I took a sabbatical to become a visiting faculty at IITB the Indian Institute of Technology in Mumbai, the highest ranked technology university in India. There I taught graduate level courses on nanoelectronics, and experimental methods in electronics research. On my return to MIT in 2013, I became a Senior Staff, a position I currently hold, in the Advanced Materials and Microsystems group at MIT Lincoln Laboratory, working on microsystem actuation and power. Currently, I am working on microrobotics and microactuation technology based on microhydraulics, with multiple publications in Science and Nature on the subject. Over the years I have served on the IEDM paper selection

committee and have taught multiple international courses on advanced electronics in Singapore and Malaysia.

II. Understanding of Relevant Legal Principles

12. I am not a lawyer, and I will not provide any legal opinions. Although I am not a lawyer, I have been advised certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and invalidity of patent claims.

13. I understand that a patent claim is invalid if it is anticipated or obvious in view of the prior art, and that a claim can be unpatentable even if all of the requirements of the claim cannot be found in a single prior-art reference. I further understand that invalidity of a claim requires that the claim be anticipated or obvious from the perspective of a person of ordinary skill in the art at the time the invention was made.

14. I have been informed the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I have been informed that, in inter partes review (“IPR”) proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication. I have been informed that for a

claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

15. I have been informed that a patent claim is invalid if it would have been obvious to a person of ordinary skill in the art. In analyzing the obviousness of a claim, I understand the following factors may be taken into account: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims; (3) the level of ordinary skill in the art; and (4) any so called “secondary considerations” of non-obviousness, if they are present. I am not aware of any evidence of secondary considerations of non-obviousness relevant to the ’779 patent. I reserve the right to supplement this Declaration if Patent Owner (“PO”) introduces evidence of secondary considerations of non-obviousness.

16. I understand that to prove that prior art or a combination of prior art renders a patent obvious, it is necessary to:

- (1) identify the particular references that, singly or in combination, make the patent obvious;
- (2) specifically identify which elements of the patent claim appear in each of the asserted references; and
- (3) explain why a person of ordinary skill in the art would have combined the references, and how they would have done so, to create the

inventions claimed in the patent. I further understand that exemplary rationales that may support a conclusion of obviousness include:

- combining prior art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of known technique(s) to improve similar devices (methods or products) in the same way;
- applying a known technique to a known device (method or product) ready for improvement to yield predictable results;
- “obvious to try” – choosing from a finite number of identified, predictable solutions with a reasonable expectation of success;
- known work in one field of endeavor may prompt variations of the work for use in either the same field or a different field based on design incentives or other market forces if the variations are predictable to a person of ordinary skill in the art; and
- some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

17. I have been informed that, in considering obviousness, hindsight reasoning derived from the patent-at-issue may not be used.

III. '779 Patent – Technical Background and Overview

18. The '779 patent titled “Semiconductor Device” to Ito, et al. (“the '779 patent”) was filed on October 31, 2012 as a continuation of application No. PCT/JP2011/002868, filed May 24, 2011. The '779 patent claims priority to JP Application 2010-205599, filed September 14, 2010. Solely for purposes of this IPR, I assume September 14, 2010 as the earliest possible priority date claimed on the face of the '779 patent. However, my opinion set forth herein would not change if the priority date was determined to be May 24, 2011 which I understand to be the PCT filing date or October 31, 2012 which I understand to be the filing date of the '779 patent.

A. Technical Background

19. Over the sixty years prior to the earliest possible priority date of the '779 patent, the “semiconductor industry has seen the continuous development of new and improved processes.” (TSMC-1011, 5.) The process improvements “in turn led to the more highly integrated and reliable circuits” which “fueled the continuing electronics revolution.” (*Id.*) The book, “Microchip Fabrication” by Van Zant (“Van Zant”), explains that “process improvements fall into broad categories: process and structure.” (*Id.*) “*Process improvements* are those that allow the fabrication of the devices and circuits in smaller dimensions, in ever

higher density, quantity and reliability." (*Id.* (italics in original).) Structure improvements allow "greater circuit performance, power control, and reliability." (*Id.*)

20. "Device component size and number of components in an IC are the two common trackers of IC development." (TSMC-1011, 5.) The dimensions of a component "are characterized by the smallest dimension in the design" which is called the feature size and is usually expressed in microns or nanometers. (TSMC-1011, 5-6.) The term "node" historically refers to the size of the smallest feature of a transistor.

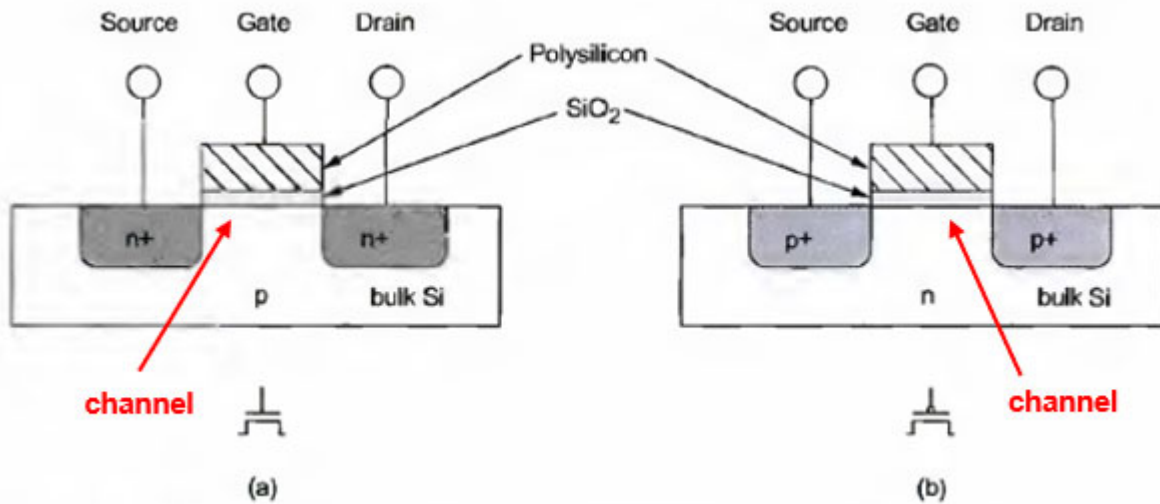
21. ICs "are composed of individual conductors, fuses, resistors, capacitors, diodes, and transistors." (TSMC-1011, 513.) At the time of the earliest possible priority date of the '779 patent (September 2010), the most popular transistor was the metal-oxide-semiconductor field effect transistor ("MOSFET"). (*See* TSMC-1011, 7.) Because the '779 patent is directed to MOSFETs, I describe these transistors in further detail in the next section. I note that the '779 patent uses the term "metal insulator semiconductor field-effect transistor" ("MISFET") instead of MOSFET. A POSITA would have understood that these terms were used interchangeably prior to the '779 patent because, for example, an oxide is an insulator. I also note that the term MOSFET and MISFET also encompasses

devices with gates formed from polycrystalline silicon (polysilicon), a conductive non-metal material. (TSMC-1012, 8.)

1. MOSFET/MISFET

a. Structure

22. A MOSFET generally includes a stack of the conducting gate, an insulating layer, and “the silicon wafer, also called the *substrate*, *body* or *bulk*.” (TSMC-1012, 8 (italics in original).) The substrate can be doped with impurities (e.g., arsenic for n-type or boron for p-type) to influence the electrical behavior of the transistors built on it. A planar nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain” as illustrated in Figure 1.8(a) from “CMOS VLSI Design: A Circuits and Systems Perspective” by Weste (“Weste”). (*Id.*) The source and drain are physically equivalent and often they are regarded as interchangeable. (*See, e.g., Id.*) A planar pMOS transistor, illustrated below in Weste’s Figure 1.8(b), “is just the opposite, consisting of p-type source and drain regions with an n-type body.” (*Id.*)



Weste, Figure 1.8

23. “In CMOS technology with both flavors of transistors, the substrate is either n-type or p-type” and the “other flavor of transistor must be built in a special well in which dopant atoms have been locally added to form the body of the opposite type.” (TSMC-1012, 8.) One of the first steps in most CMOS processes is to define the well regions for the transistors. (TSMC-1012, 117.) As shown in the exemplary triple well below, a deep n-well is driven into the p-substrate and shallower n-well and p-well regions are implanted. (*Id.*) After the wells are formed, the doping levels can be adjusted to set the desired threshold voltages for the nMOS and pMOS transistors. (*Id.*) I discuss threshold voltage in further detail in §III.A.3.

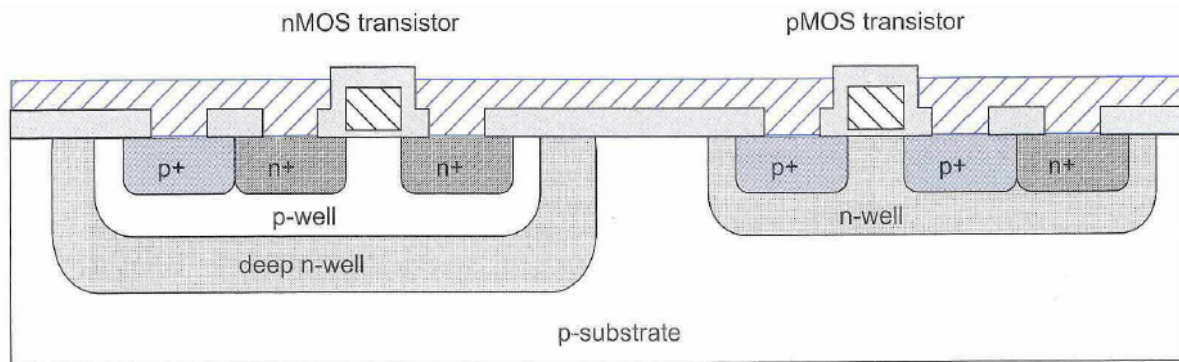
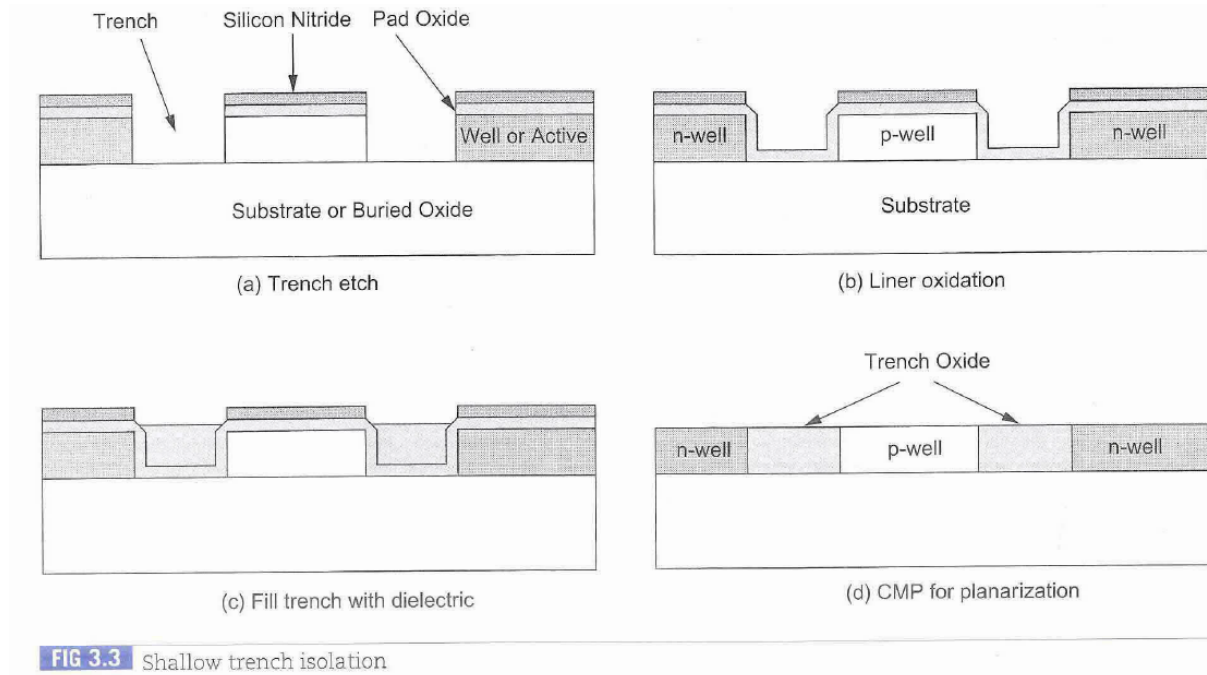


FIG 3.2 Well structure in triple-well process

Weste, Figure 3.2

24. Individual devices “need to be isolated from one another so that they do not have unexpected interactions.” (TSMC-1012, 119.) Therefore, one of the early steps in the fabrication process is the creation of structures to isolate the devices. One common technique to achieve isolation is referred to as **shallow trench isolation** (STI). (See, e.g., TSMC-1012, 117.) In STI, trenches are etched into the silicon and filled with an insulating material which isolates the active areas of the silicon wafer and prevents electrical interference between adjacent transistors. (TSMC-1012, 119.) Figure 3.3 from Weste illustrates STI regions.



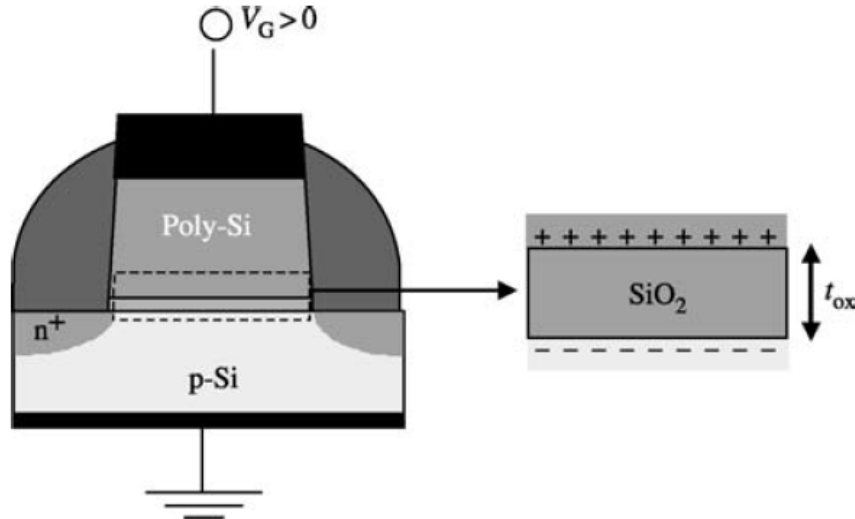
Weste, Figure 3.3

(i) Gate Dielectric and Equivalent Oxide Thickness (EOT)

25. A key feature of the device is the gate insulating film also commonly referred to as a “gate dielectric”, which separates the gate electrode from the semiconductor channel between the source and drain. For over 40 years (1961-2007), silicon-based oxides were the primary materials used for gate dielectrics in MOSFETs due to their excellent insulating properties, thermal stability, and compatibility with silicon. Silicon-based oxides provided a reliable interface with silicon, minimizing charge trapping and enabling precise control over gate dielectric thickness, essential for device performance. However, as transistors

scaled down, the silicon-based oxide layer had to become thinner, leading to increased gate leakage due to quantum tunneling. (TSMC-1013, 5-8.)

26. From an electrical viewpoint, the metal-oxide/insulator-semiconductor structure “behaves like a parallel plate capacitor: when a gate voltage V_G is applied to the gate, charges on the metal are compensated by opposite charges in the semiconductor, these latter charges forming the channel connecting the source and drain of the transistor,” as illustrated in Figure 1.1.4 from “High-k Dielectrics” to Houssa. (TSMC-1013, 8.) I describe the general operation of MOSFET/MISFET devices in further detail in §III.A.1.b.



Houssa, Figure 1.1.4

27. Houssa explains that the capacitance C of this parallel plate capacitor is given by the following equation (labeled 1.1.1¹ in Houssa):

$$C = \frac{A\epsilon_r\epsilon_0}{t_{ox}} \quad (1.1.1)$$

“where A is the capacitor area, ϵ_r the relative dielectric constant of the material (3.9 for SiO_2), ϵ_0 the permittivity of free space ($8.85 \times 10^{-12} \text{ F m}^{-1}$) and t_{ox} the gate oxide thickness.” (TSMC-1013, 8.) From the above equation, it appears that decreasing the gate oxide thickness (t_{ox}) allows the capacitance of the structure to increase and hence an “increase in the number of charges in the channel for a fixed value of V_G .” (*Id.*) However, as I noted above, there is a limit to how much the thickness of the SiO_2 layer can be decreased. “An alternative way of increasing the capacitance is to use an insulator with a higher relative dielectric constant than SiO_2 .” (*Id.*)

28. Transistor designs therefore migrated to the use of high dielectric constant materials to replace silicon-based oxides. (TSMC-1013, 8-9.) Exemplary high-k materials include, e.g., tantalum oxide (Ta_2O_5), hafnium oxide (HfO_2),

¹ Houssa notes that this equation is for the capacitor “in accumulation and inversion” and “neglecting poly-Si depletion effects”. (TSMC-1013, 8.) I discuss accumulation/inversion in §III.A.1.b.

barium strontium titanate (BST), and zirconium oxide (ZrO₂). (TSMC-1014, 146.)

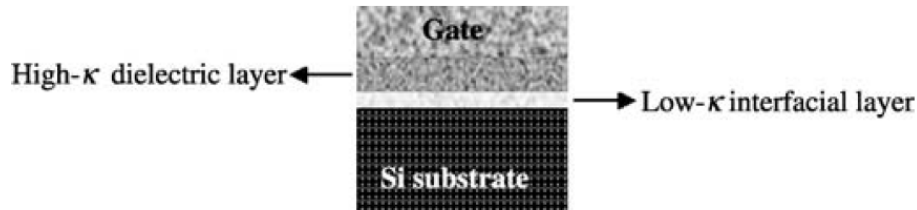
I note that the relative dielectric constant is also represented by the letter “k” and so documents often refer simply to “high-k” materials rather than “high dielectric constant materials.” (*See* TSMC-1013, 8-9.) I use the terms interchangeably in this declaration. With a high-k material, a thicker gate dielectric can be used with a reduction of leakage current and improvement in the reliability of the gate dielectric. (TSMC-1013, 9.)

29. Equivalent Oxide Thickness (EOT) is a key concept used in assessing high-k dielectrics. The EOT (t_{eq}) of a material “is defined as the thickness of the SiO₂ layer that would be required to achieve the same capacitance density as the high-k material in consideration.” (TSMC-1013, 9.) The EOT is therefore given by the following equation (labeled 1.1.2 in Houssa):

$$\frac{t_{eq}}{\epsilon_{r,SiO_2}} = \frac{t_{high-\kappa}}{\epsilon_{r,high-\kappa}} \quad (1.1.2)$$

“where t_{high-k} and $\epsilon_{r,high-k}$ are the thickness and relative dielectric constant of the high-k material, respectively.” (*Id.*) In the example provided by Houssa, “using ZrO₂ as gate dielectric ($\epsilon_r \approx 20$)” allows “use a 5.1 nm thick layer in order to achieve a capacitance equivalent to a 1 nm thick SiO₂ layer; the equivalent oxide thickness of this ZrO₂ layer is thus 1 nm.” (*Id.*)

30. Houssa further notes that a low-k interfacial layer exists between the high-k metal oxide and silicon substrate interface. (*See* TSMC-1013, 9.) Houssa explains that such an interfacial layer “either grows during the deposition of the high-k dielectric or during post-deposition anneal process.” (*Id.*) Although not mentioned by Houssa, an interfacial layer may also be formed separately.



Houssa, Figure 1.1.5

31. The total capacitance, C_{tot} , combines, in series, the low-k and high-k dielectric layer capacitance and is represented by the following equation from Houssa (labeled 1.1.3 in Houssa):

$$\frac{1}{C_{\text{tot}}} = \frac{1}{C_{\text{low-}\kappa}} + \frac{1}{C_{\text{high-}\kappa}} \quad (1.1.3)$$

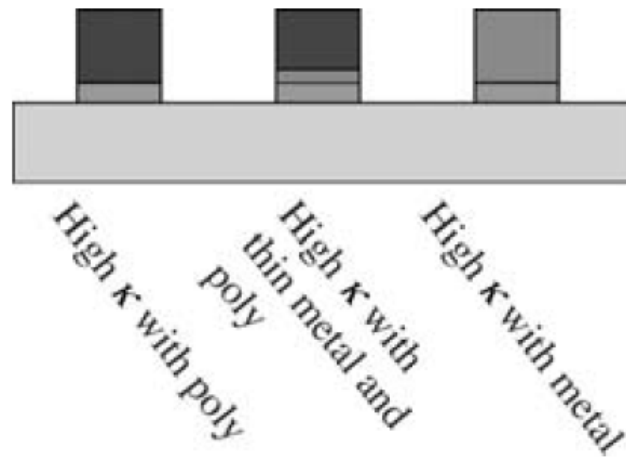
From this equation, the total EOT is as follows (labeled 1.14 in Houssa):

$$t_{\text{eq}} = \left(\frac{\epsilon_{\text{r,SiO}_2}}{\epsilon_{\text{r,low-}\kappa}} \right) t_{\text{low-}\kappa} + \left(\frac{\epsilon_{\text{r,SiO}_2}}{\epsilon_{\text{r,high-}\kappa}} \right) t_{\text{high-}\kappa} \quad (1.1.4)$$

(TSMC-1013, 9.)

(ii) Gate Electrode

32. Gates of early transistors were built from metal so the gate stack “was called metal-oxide-semiconductor” (“MOS”). (TSMC-1012, 8.) Gates later migrated to polycrystalline silicon (polysilicon or poly), a conductive non-metal material, due to its stability and compatibility with silicon. However, “the name [MOS] stuck.” (*Id.*) With the introduction of high-k dielectrics and the continual shrinking of transistor dimensions, polysilicon gates began to exhibit performance issues like poly-depletion, which reduced gate capacitance. To overcome these challenges, metal gates replaced polysilicon in advanced nodes (45 nm and below), starting around 2007. Metal gates, when combined with high-k dielectrics like HfO₂, addressed issues like Fermi-level pinning, eliminated polysilicon gate depletion, provided lower resistance, enhancing switching speeds, and improved overall transistor performance. The following figure from Houssa illustrates different exemplary gate stack configurations: (1) high-k gate dielectric with a polysilicon gate electrode, (2) high-k gate dielectric with gate electrode having a thin metal and polysilicon layer, and (3) high-k dielectric with a metal gate electrode.

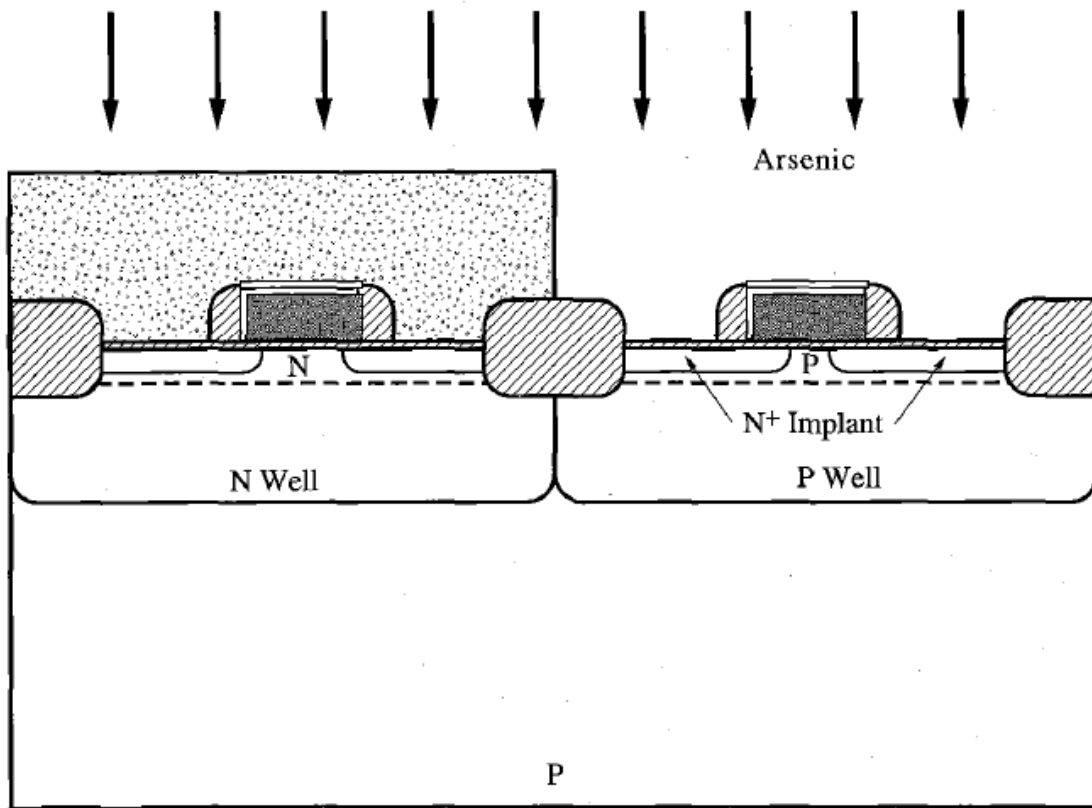


Houssa, Figure 5.1.18

(iii) Source and Drain

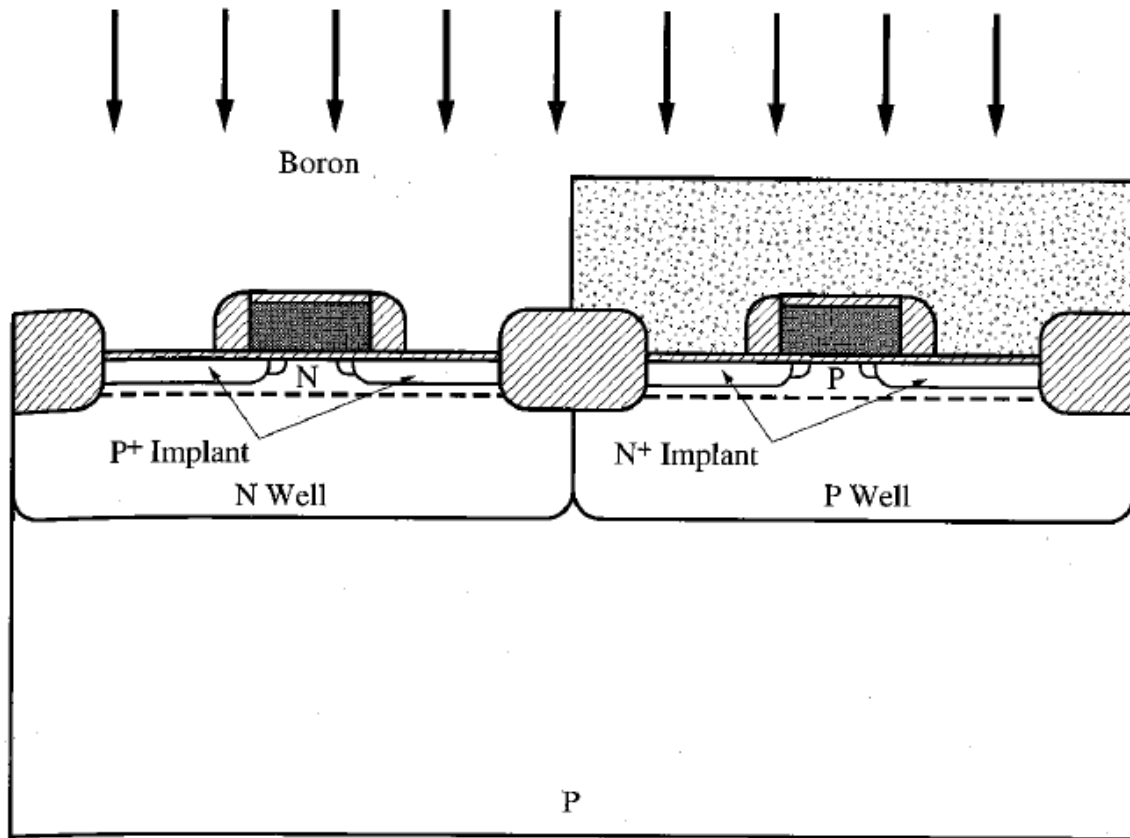
33. The source and drain regions in a transistor are formed by implanting dopants (either n-type or p-type) into the silicon substrate on both sides of the gate electrode. Dopants either contribute extra electrons and become n-type dopants, or they contribute extra holes (i.e., electron vacancies or positively charged carriers) and become p-type dopants. (TSMC-1015, 17, 20.) As a result, to the extent the doping concentration is accurately controlled, the free electron and hole concentrations, and therefore the conductivity of the silicon substrate, can be precisely controlled. (*Id.*) Thus, these regions are heavily doped to improve conductivity and facilitate current flow when the transistor is on. The formation of these regions is critical for defining the transistor's electrical characteristics.

34. The formation of the source/drain regions involves one or more annealing steps necessary to electrically activate the dopants and repair the crystal structure of the body from the ion bombardment. (TSMC-1015, 80-82.) “Silicon VLSI Technology: Fundamentals, Practice and Modeling” by Plummer, et al. (“Plummer”) describes an example of source/drain formation for a CMOS device. As shown in Plummer’s Figure 2-31 below, in a first source/drain implant, photoresist and mask are used to define regions where NMOS source/drain implants are done. (TSMC-1015, 80.) An Arsenic implant then forms the NMOS source and drain regions.



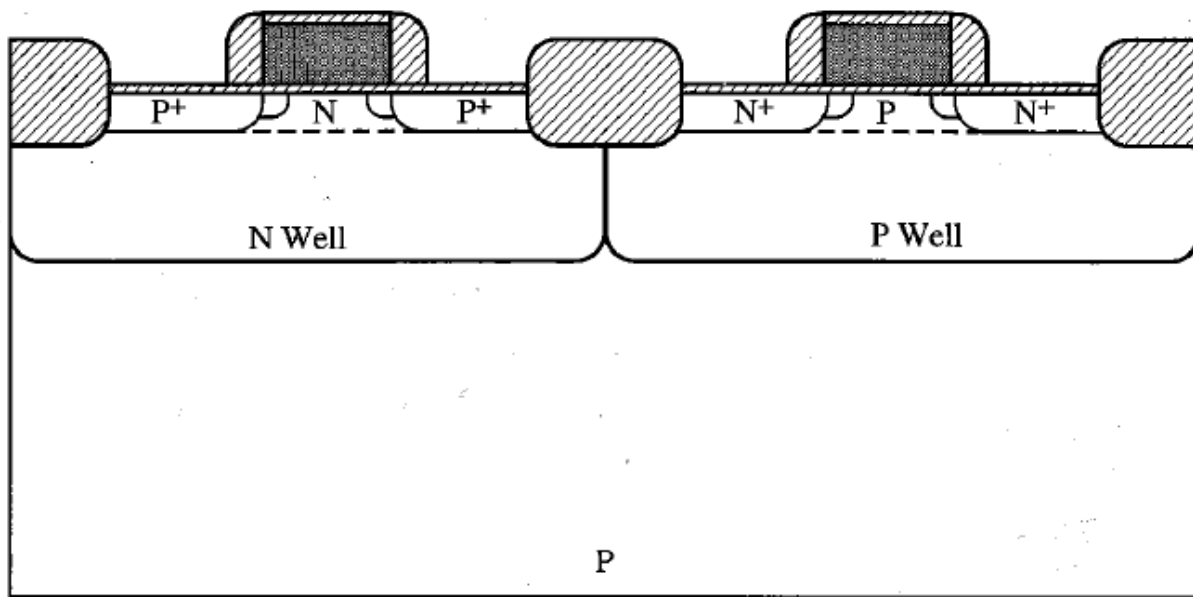
Plummer, Figure 2-31

35. Next, as shown in Plummer's Figure 2-32 below, a photoresist and mask allow a boron implant to form the PMOS source/drain regions.



Plummer, Figure 2-32

36. “Because the ion implantation process creates damage, most dopants are not electrically active at the end of the implantation.” (TSMC-1015, 470.) To activate the dopants, the wafers are subjected to a rapid thermal anneal, often called a RTA, typically done at a temperature over 1000°C. (See, e.g., TSMC-1015, 81.) The RTA time can range from one second to a few minutes, with more advanced technologies using the shorter times. (See, e.g., TSMC-1015, 393-394.)



Plummer, Figure 2-33

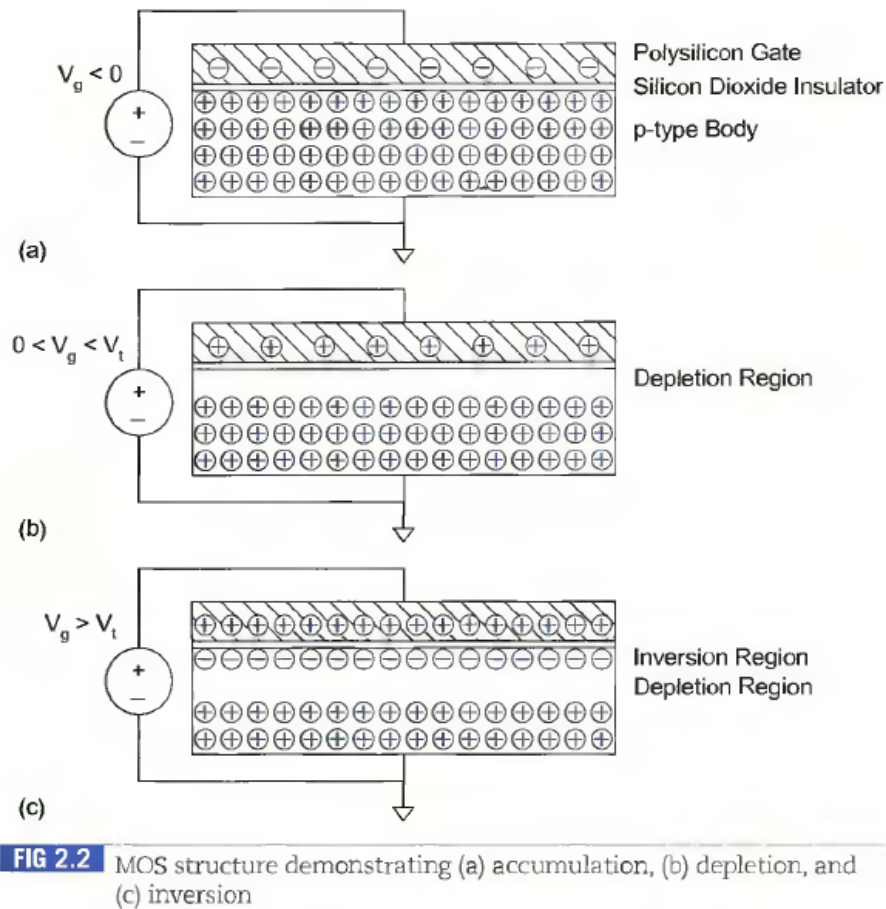
37. The dopant activation is not the only annealing step performed during the chip manufacturing process and additional annealing steps or thermal process steps at different stages of the integrated circuit fabrication are necessary. For example, formation of a silicide on the gate and source/drain terminals also requires an annealing step to promote the silicidation process and the deposition of dielectric and/or metal layers may occur at elevated temperatures (e.g., at 600 °C or above). (TSMC-1014, 608, 611.) And because thermal processing steps and/or annealing steps can cause thermal diffusion of species between previously formed layers, the transistors are engineered to account for the diffusion of species occurring during these thermal processing and/or annealing steps. (TSMC-1011, 345.)

b. Operation

38. A MOS transistor is a majority carrier device “in which the current in a conducting channel between the source and drain is controlled by a voltage applied to the gate.” (TSMC-1012, 67.) Generally, in a MOSFET, when a voltage is applied to the gate through the gate metal (the gate voltage), a “*field effect* takes place in the surface of the semiconductor” which is “either a buildup of charge or a depletion of charges in the wafer surface under the top plate.” (TSMC-1011, 525 (*italics in original*).) “Which event occurs depends on the doping conductivity type in the wafer under the gate and the polarity of the gate voltage. (*Id.*) This “buildup or depletion of charge creates an inversion channel under the gate that connects the source and drain.” (*Id.*) When the gate voltage is raised above a certain threshold, known as the threshold voltage, an inversion channel forms between the source and the drain, electrically connecting them. Then, with a difference in the drain to source voltage, “current starts to flow as the inverted surface creates an electrically connecting channel.” (*Id.*) “Applying more voltage to the gate increases the size of the channel, allowing more current to flow through the channel.” (*Id.*) I explain this more specifically for nMOS and pMOS devices below.

39. In an nMOS transistor, “the majority carriers are electrons” and in a pMOS transistor, “the majority carriers are holes.” (TSMC-1012, 67.) As discussed

above, the holes represent an electron vacancy. (TSMC-1015, 20.) Figure 2.2 from Weste (below) illustrates an MOS structure without source and drain to describe the behavior of a MOS transistor. In this figure, a p-type body is used. In Figure 2.2(a), “a negative voltage is applied to the gate” and a negative charge therefore exists on the gate. (TSMC-1012, 67-68.) “In Figure 2.2(b), a low positive voltage is applied to the gate, resulting in some positive charge on the gate.” (*Id.*) As shown, the holes in the body are repelled from the region directly beneath the gate, resulting in a depletion region forming below the gate. (*Id.*) In Figure 2.2(c), a higher positive potential exceeding a critical threshold voltage is applied, attracting more positive charge to the gate which repels the holes further. (TSMC-1012, 68.) A “small number of free electrons in the body are attracted to the region beneath the gate.” (*Id.*) This conductive layer of electrons in the p-type body is called the inversion layer. (*Id.*)



Weste, Figure 2.2

40. Weste's Figure 2.3 (below) illustrates operation of an nMOS transistor with a grounded source and p-type body. In Figure 2.3(a), the gate-to-source voltage is less than the threshold voltage and the source and drain have free electrons. (TSMC-1012, 68-69.) As shown, the "body has free holes but no free electrons." (*Id.*) "The junctions between the body and the source or drain are reverse biased, so almost no current flow." (TSMC-1012, 68.) This mode of operation is referred to as "cutoff" or "off-state." (*Id.*) Then, as shown in Figure

2.3(b), the gate voltage is greater than the threshold voltage causing “an inversion region of electrons (majority carriers)”, called the channel, which “creat[es] a conductive path” between the source and drain. (TSMC-1012, 68-69.) When a small positive potential V_{ds} is applied to the drain, as shown in Figure 2.3(c), current flows through the channel from drain to source. (TSMC-1012, 69-70.) This mode of operation is referred to as linear, resistive, nonstaturated or unsaturated. (TSMC-1012, 70.) If V_{ds} becomes sufficiently large that the gate-to-drain voltage, V_{dg} , exceeds the threshold voltage, as shown in Figure 2.3(d), the channel is no longer inverted near the drain and becomes pinched off. (TSMC-1012, 70.) This mode is referred to as saturation. (TSMC-1012, 80.) Both the unsaturated and saturated modes, when V_{gs} is greater than V_t , are commonly referred to as the ‘on-state’ because the transistor conducts from source to drain.

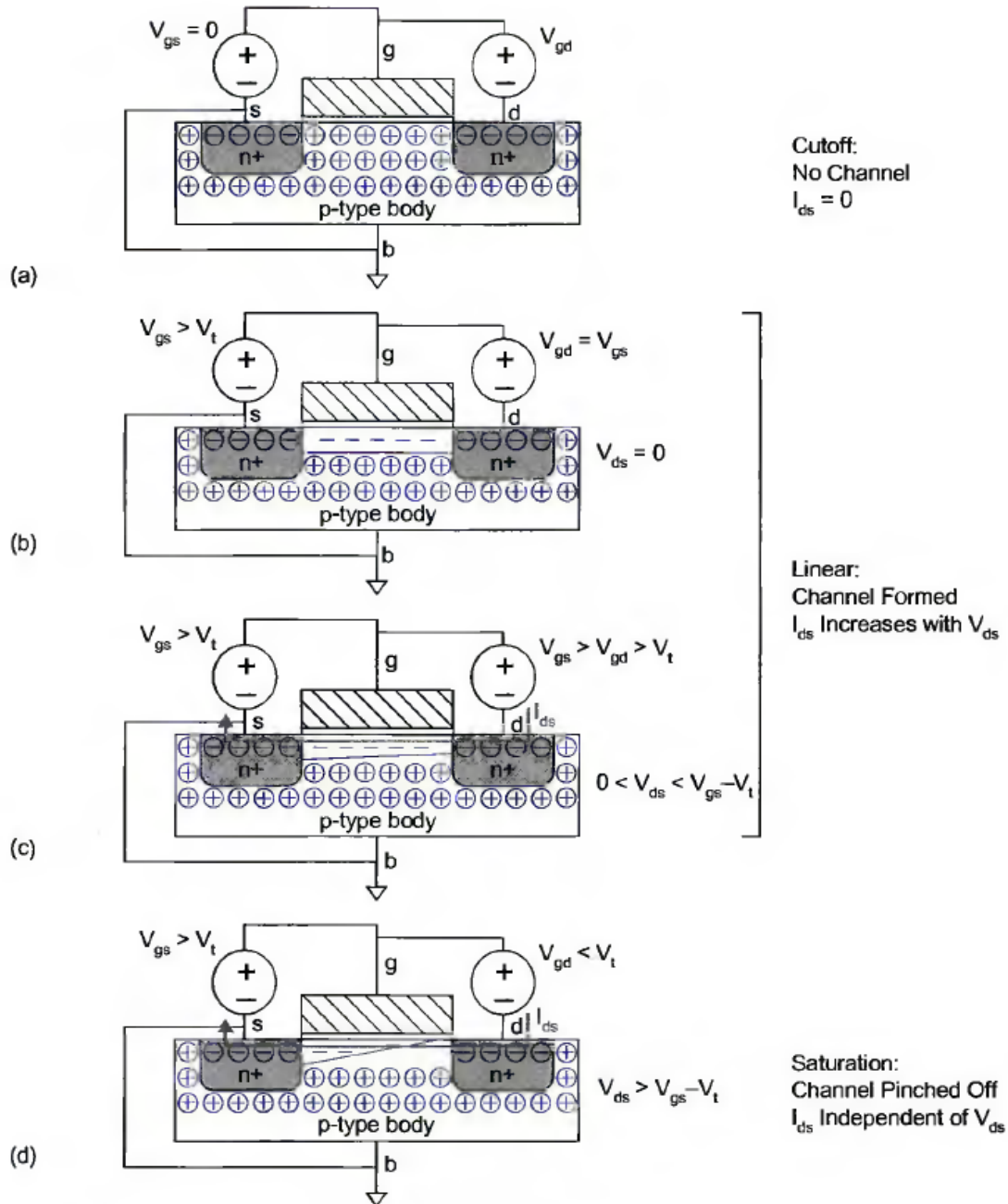
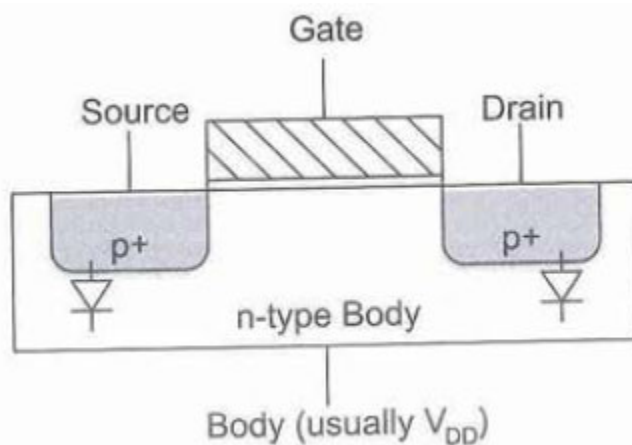


FIG 2.3 nMOS transistor demonstrating cutoff, linear, and saturation regions of operation

Weste, Figure 2.3

41. A pMOS transistor, illustrated in Weste's Figure 2.4 below, "operates in just the opposite fashion." (TSMC-1012, 70.) The n-type body is tied to a high potential causing the junctions with the p-type source and drain to be normally reverse biased. (TSMC-1012, 80.) When the gate is also at a high potential, no current flows between the source and drain. (*Id.*) When the gate voltage is lowered, holes are attracted to form a p-type channel immediately below the gate, allowing current to flow between the drain and source. (*Id.*)

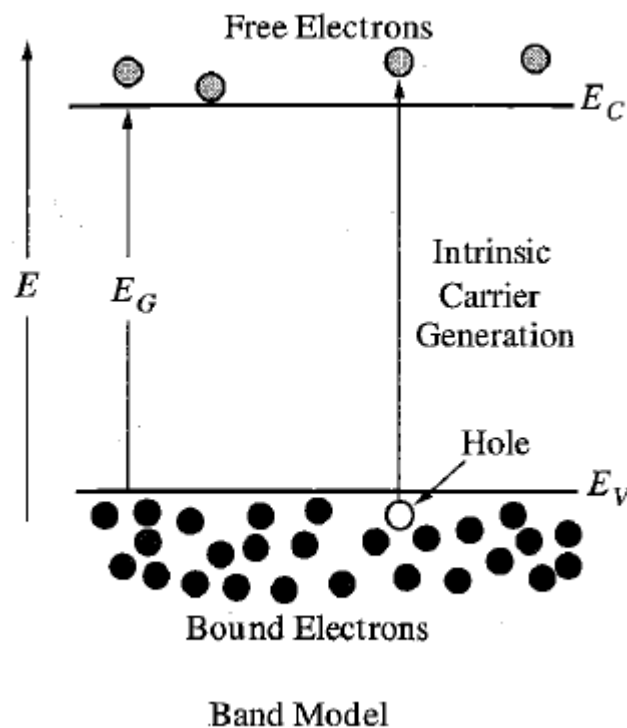


Weste, Figure 2.4

2. Band Model

42. Electrical properties of semiconductors are often described through the use of the band model, illustrated below in an excerpt from Figure 1-19 of Plummer. In the band model, "the vertical direction is the potential energy of electrons in the [silicon] crystal." (TSMC-1015, 19.) As shown, "in a perfect crystal, electrons are either bound to host silicon atoms or they are free." (*Id.*) The

conduction band is a band of energy levels that is partially filled with electrons. The conduction band contains the electrons responsible for conduction. The valence band describes the energy levels of electrons in an atomic structure's valence shell. The bandgap is the energy difference between the valence band's highest energy level energy state and the conduction band's lowest occupied energy state. The bandgap is a measurement of a material's electrical conductivity.

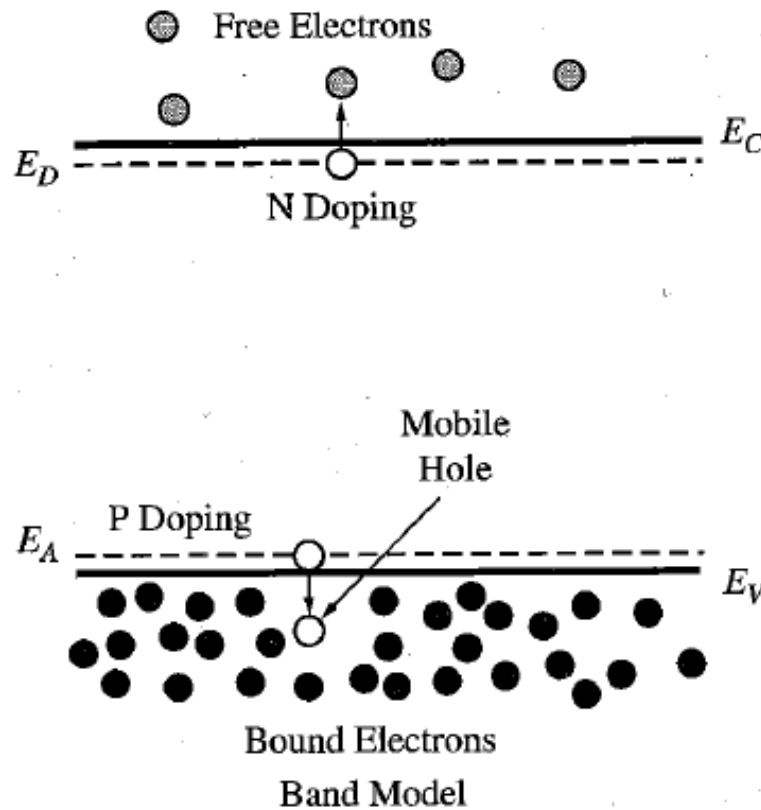


Plummer, Figure 1-19

43. “A finite amount of energy is required to free the electron.” (TSMC-1015, 19.) This is represented with bound electron energy levels below the valence band (E_V) and the free electron energy levels above the conduction band (E_C). (*Id.*)

“The energy gap between E_v and E_c represents the energy needed to free the electron.” (*Id.*) That is, when given enough energy, valence electrons become free electrons and travel to the conduction band, resulting in conductivity.

44. In Figure 1-20 from Plummer, the introduction of dopants is represented in the band diagram by the E_D and E_A energy levels. The E_D level represents a donor atom, e.g., Arsenic (As). “When an As atom is introduced into the crystal, it brings with it an extra electron in its outermost shell, beyond the four needed for covalent bonding in the silicon lattice.” (TSMC-1015, 20.) The binding energy of this fifth valence electron is usually “rather small” and as a result, “the fifth electron can be quite easily freed.” (*Id.*) This is represented in the band diagram with an energy level E_D which is close to E_C . (*Id.*)

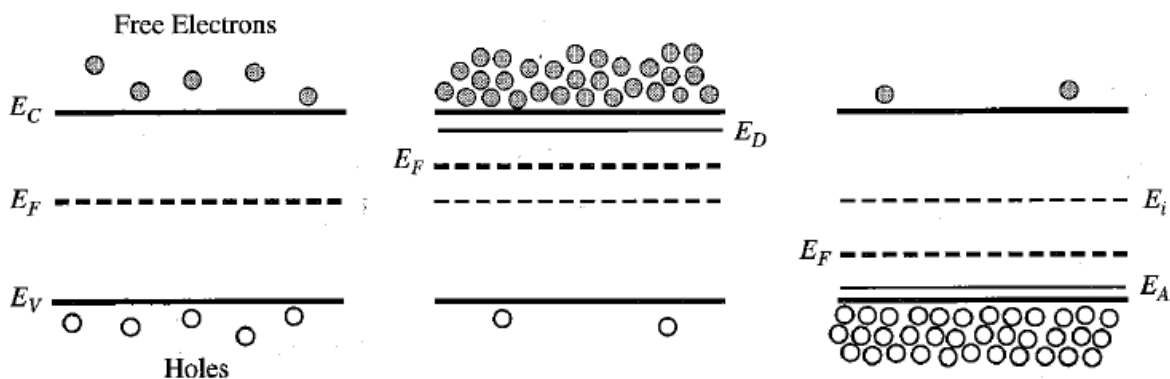


Plummer, Figure 1-20

45. For p-type dopants such as Boron (B), E_A represents the energy level introduced into the crystal by the p-type dopant. (TSMC-1015, 20.) These dopants “have one fewer valence electrons per atom than the host crystal.” (*Id.*) “The hole or missing electron is weakly bound to the B atom.” (*Id.*) As a result, an “electron from a neighboring Si atom can exchange positions with the hole, effectively allowing the hole to move through the crystal as a positively charged carrier.” (*Id.*)

46. The Fermi level, E_F , represents the energy level at which the probability of finding an electron is exactly 0.5. (TSMC-1015, 23.) This concept is

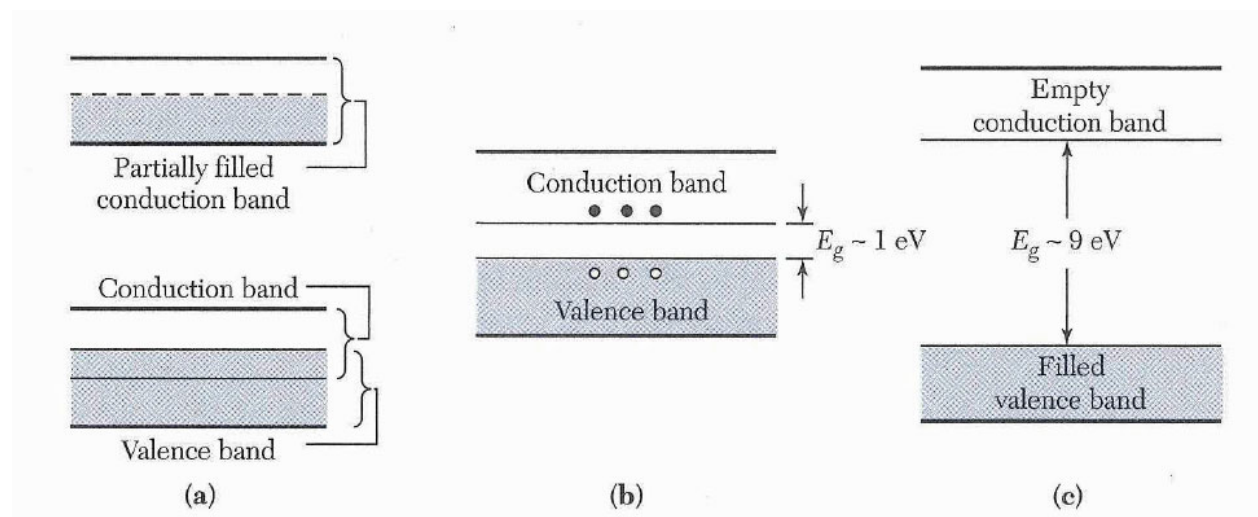
illustrated in Plummer's Figure 1-22 (below). The illustration on the left represents an undoped semiconductor. In this case, the probability of a valence band energy level being occupied by an electron is essentially 1 and the probability of finding an electron in the conduction band is essentially 0. (*Id.*) "Therefore, E_F must be located somewhere in the forbidden band between E_v and E_C ." (*Id.*) In middle case, when N-type doping is added, the number of electrons in the conduction band increases and "the probability of finding an electron above E_C also increases." (*Id.*) The Fermi level moves up in this case. (*Id.*) On the right case, when P-type doping is added, the hole population in the valence band increases and the free electron population in the conduction band decreases. (TSMC-1015, 24.) In this case, the Fermi level "moves down the bandgap to reflect the lower free electron population." (*Id.*)



Plummer, Figure 1-22

47. The variation in electrical conductivity of metals, semiconductors, and insulators “may be explained qualitatively in terms of their energy bands.”

(TSMC-1023, 32.) Figure 19 from “Semiconductor Devices: Physics and Technology” by Sze (“Sze”; TSMC-1023) illustrates the energy band diagrams of three classes of solids—metals, semiconductors, and insulators.



Sze, Figure 19

48. **Metals:** The characteristics of a metal (also called a conductor) include a very low value of resistivity and the conduction band either is partially filled or overlaps with the valence band so that there is no bandgap, as shown in Figure 19a above. (TSMC-1023, 32-33.) “As a consequence, the uppermost electrons in the partially filled band or electrons at the top of the valence band can move to the next-higher available energy level when they gain kinetic energy (e.g., from an applied electric field).” (*Id.*)

49. **Insulator:** In an insulator, the valence electrons form strong bonds between neighboring atoms which are difficult to break. (TSMC-1023, 33.) Consequently, “there are no free electrons to participate in current conduction at or near room temperature.” (*Id.*) As shown in Figure 19(c) above, “insulators are characterized by a large bandgap.” (*Id.*) “Thermal energy or the energy of an applied electric field is insufficient to raise the uppermost electron in the valence band to the conduction band.” (*Id.*) That is, insulators have high resistivity and cannot conduct current. (*Id.*)

50. **Semiconductor:** Semiconductors have a smaller energy gap, on the order of 1 eV. (TSMC-1023, 33.) At T=0K, “all electrons are in the valence band, and there are no electrons in the conduction band.” (*Id.*) Semiconductors are poor conductors at low temperatures. (*Id.*) However, at room temperature, an “appreciable numbers of electrons are thermally excited from the valence band to the conduction band.” (*Id.*) “Since there are many empty states in the conduction band, a small applied potential can easily move these electrons, resulting in a moderate current.” (*Id.*)

51. The book, “Silicon Processing for the VLSI Era, Volume 3—The Submicron MOSFET” by Wolf (Wolf-3) further describes the energy band for an ideal MOS-C (MOS capacitor), illustrated in Figure 3-3 in which the work

functions and doping levels happen to line up so that the semiconductor is uncharged with zero bias applied to the gate. The vacuum level is the energy level of a charge particle when it is in a vacuum with zero kinetic energy. The work function is the amount of energy needed to remove a free electron from a molecule and is equal to the distance between the Fermi and vacuum levels, as shown below. (TSMC-1029, 91.) When a p-type semiconductor with a work function (ϕ_s) is joined with a metal with a different work function (ϕ_m), the characteristics of the metal-semiconductor junction depend on the difference between their work functions, as I discuss further below.

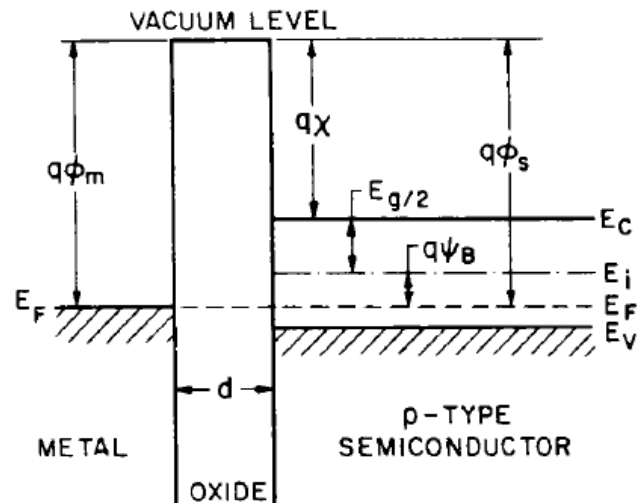


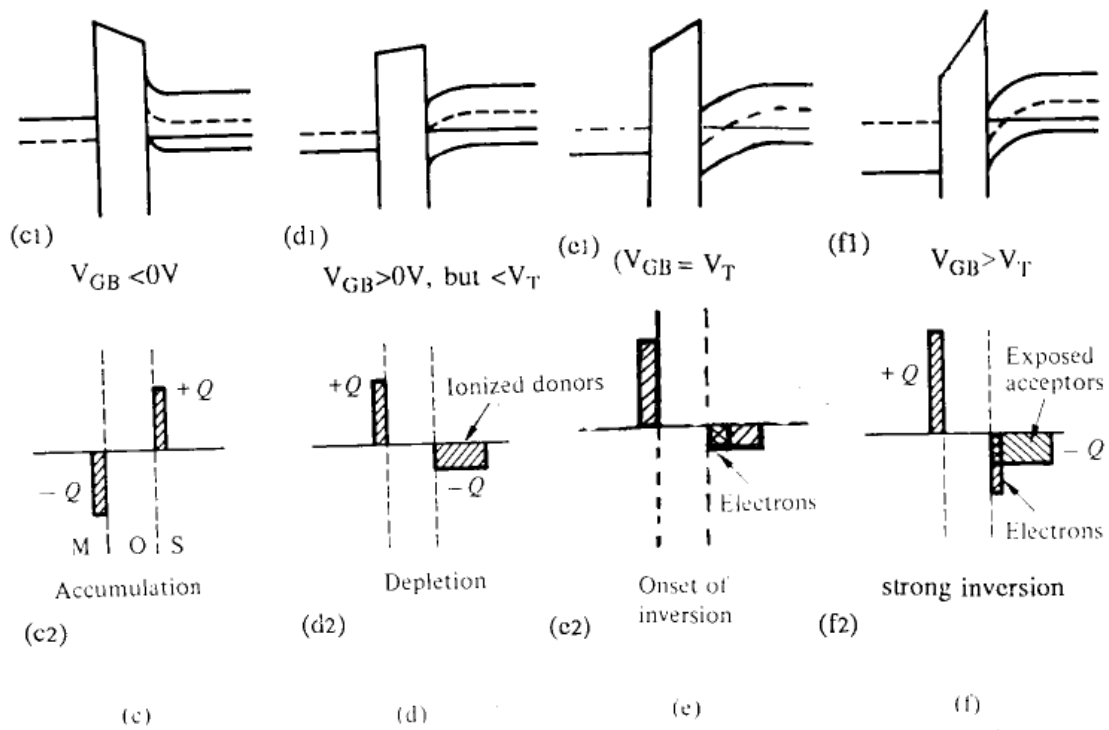
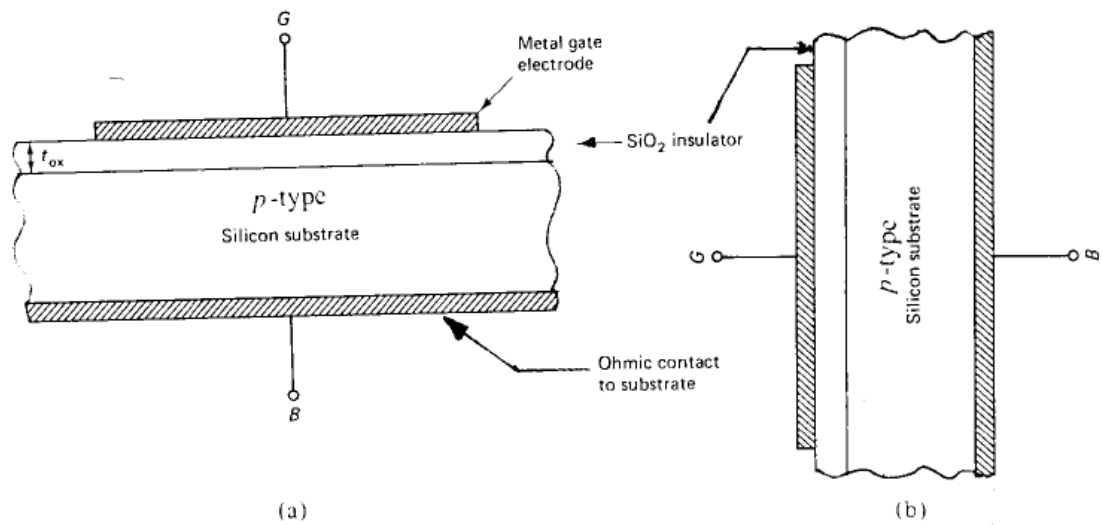
Fig. 3-3 Energy band diagram of an ideal MOS-C when $V_{GB} = 0V$ (flat-band condition).

Wolf-3, Figure 3-3

52. The figure above illustrates an isolated metal and an isolated semiconductor with an oxide sandwiched between them. In this situation, all bands are flat and this is referred to as a flat-band condition. (TSMC-1029, 91.)

53. As shown in Figure 3-4 below, a dc bias is applied between the gate and the substrate. (TSMC-1029, 92-93.) The silicon region remains in equilibrium, implying that E_f remains flat. (*Id.*) However, the other bands are altered. (*Id.*)

Figure 3-4 illustrates four different gate-bias conditions.



Wolf-3, Figure 3-4

3. Threshold Voltage

54. The threshold voltage is the voltage applied at the gate which brings the onset of inversion (formation of the current-carrying channel)—i.e., the “turn-on” voltage of the transistor. (TSMC-1011, 526.) “Every MOS transistor is designed to operate at a specific threshold voltage.” (TSMC-1011, 474.) Because pMOS and nMOS transistors are built on different dopant type bodies and feature different types of dopants for their respective source/drain terminals, one would understand that pMOS and nMOS transistors require different polarity gate voltages. For example, as discussed above for Weste’s Figure 2.3, nMOS transistors, which use electrons in a p-type body to form the channel between the source and drain terminals, require a **positive** voltage applied to the gate, and therefore will have a **positive** threshold voltage. Conversely, pMOS transistors, which use holes in an n-type body to form the channel between the source and drain terminals, require a **negative** voltage applied to the gate, and therefore will have a **negative** threshold voltage. (*See, e.g.*, TSMC-1012, 74, 293-296, 302.)

55. Additionally, consumer devices often have transistors of the same conductivity types but with different threshold voltages to cope with various demands on standby power and operation speed. For example, the International Technology Roadmap for Semiconductors (ITRS) acknowledges that

“[i]nnovations in circuit design and architecture for performance management, as well as utilization of multiple transistors on chip, are needed to design chips with both the desired performance and power dissipation. The multiple transistors have different threshold voltages (V_t), with the low V_t , high leakage devices used mainly in the critical paths, and higher V_t , lower leakage devices used in the rest of the chip.” (TSMC-1016, 3-4.) To this end, the ITRS identifies three types of logic that can be used in chips: high performance (HP) logic, low standby power (LSTP) logic, and low operating power (LOP) logic. (TSMC-1016, 5.) Specifically, “[h]igh-performance [HP] logic refers to chips of high complexity, high performance, and high power dissipation, such as microprocessor unit (MPU) chips for desktop PCs, servers, etc. Low-power logic refers to chips for mobile systems, where the allowable power dissipation and hence the allowable leakage currents are limited by battery life.” (*Id.*) Within the low-power spectrum, there are two major categories, the LOP and the LSTP logic. (*Id.*) The transistors in the HP logic (i.e., the HP transistors) have the highest operating speed, the shortest gate length, the thinnest gate oxide, and the lowest V_{th} among the three (e.g., from the LOP and LSTP transistors). (TSMC-1016, 11, 17, 21.) However, HP transistors suffer from high OFF-leakage current (i.e., current flow through the transistor during the OFF state). “The transistors for LOP chips have somewhat lower

performance and considerably lower leakage current, while the transistors for LSTP chips have both the lowest performance and the lowest leakage current of all.” (*Id.*) Thus, LSTP transistors are designed for low performance and low leakage current, and therefore have thicker gate oxides (i.e., larger EOT) and higher V_{th} ; while LOP transistors are between the HP and LSTP transistors in terms of performance, leakage current, and V_{th} . (TSMC-1016, 11, 17, and 21.) As explained by ITRS:

For high-performance chips, the high subthreshold leakage current must be dealt with to keep chip static power dissipation within tolerable limits. One common approach is to fabricate more than one type of transistor on the chip, including the high-performance, low V_t device described above, as well as other MOSFET(s) with higher V_t and sometimes larger EOT to reduce the leakage current. These alternate, lower leakage devices will have lower saturation drive current and hence poorer device performance (i.e., lower MOSFET intrinsic switching frequency, $1/\tau$) than the high-performance devices. The high-performance device is used just in critical paths, and the low leakage devices are used everywhere else. Extensive use of the low leakage devices can significantly reduce the chip static power dissipation without seriously degrading chip performance. ... Hence, a realistic picture of scaled high-performance ICs is that the static power dissipation is controlled by utilizing more than one type of transistor and by utilizing device/design/architectural techniques.

(TSMC-1016, 7.) In other words, as opposed to having different chips for different purposes, modern, scalable, high-performance ICs can be obtained when HP, LOP, and LSTP transistors, as described above, are formed on a **single** chip to take advantage of their respective features and to strike a balance between performance and power dissipation.

56. Additionally, because pMOS and nMOS transistors have different electrical characteristics, comparing, for instance, the threshold voltage characteristics between pMOS and nMOS transistors is less important than comparing the threshold voltage characteristics of transistors with the same polarity requirements—i.e., pMOS transistors to pMOS transistors and nMOS transistors to nMOS transistors (*See, e.g.*, TSMC-1012, 233, 235-237, 296). For example, comparing the threshold voltage values between similar type pMOS (i.e., transistors that were intentionally built with the same electrical characteristics for an application purpose), one can obtain the threshold voltage variability across a large number of nominally identical pMOS transistors. (TSMC-1012, 235 (“There are many cases in which the designer cares how well two nominally identical transistors match”).) Similarly, comparing the threshold voltage (or other electrical characteristics) between different types of pMOS transistors (i.e., transistors that were intentionally built with different electrical characteristics for different

application purposes), one can identify defective transistors and/or verify that different types of pMOS transistors operate as intended. The same is true for comparing nMOS transistors.

57. Threshold voltage has three main components: the flatband voltage (V_{FB}), the voltage drop across the gate oxide (V_o), and the semiconductor potential at the semiconductor surface during strong inversion ($\psi_s(inv)$). (TSMC-1023, 175, 178, 194.) Notably, and without getting into details that are beyond the scope of this section, under a threshold voltage condition, $\psi_s(inv)$ becomes equal to $2\psi_B$, where ψ_B is the potential between the Fermi level (E_F) and the intrinsic Fermi level (E_i) of the semiconductor, and V_o takes the form $\frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_o}$, where the numerator is the charge per unit area in the semiconductor (in this exemplary case acceptors N_A), while the denominator is the oxide capacitance per unit area which is equal to ε_o/t_{ox} , with ε_o being the dielectric constant of the oxide and t_{ox} being the oxide thickness. (TSMC-1023, 175-176, 178, and 194.) In other words, the threshold voltage can be written as:

$$V_T \approx V_{FB} + 2\psi_B + t_{ox} \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{\varepsilon_o}.$$

58. In an ideal MOS structure, and at zero applied bias, the energy band diagram across the MOS structure is flat because it is assumed that the work

function difference between the metal Φ_m and the semiconductor Φ_s is zero (i.e., $\Phi_{ms} = 0$). (TSMC-1023, 171.) However, in reality, Φ_{ms} is a non-zero term, and this causes the energy bands of the MOS structure to bend. (TSMC-1023, 179-180.) I discuss energy bands and band bending in §III.A.2. To achieve the ideal flat-band condition, a voltage needs to be applied to offset the work function difference Φ_{ms} . (TSMC-1023, 180.) This voltage is known as the flatband voltage, V_{FB} , and in this simplified example is equal to Φ_{ms} ($V_{FB} = \Phi_{ms}$). In real world applications, it is more than the work function difference that affects the V_{FB} . More specifically, the MOS structure is also affected by charges present in the oxide and charge traps at the oxide-silicon interface. (TSMC-1023, 180.) If the work function difference between metal and the semiconductor is not zero and the value of the interface-trapped charges is negligible, the flatband voltage that needs to be applied to the MOS structure to achieve the flat-band condition is provide by the equation below (TSMC-1023, 183):

$$V_{FB} = \Phi_{ms} + \frac{(Q_f + Q_m + Q_{ot})}{C_o}.$$

The term on the right represents the voltage drop across the oxide due to the presence of different types of oxide charges, such as fixed charges (Q_f), mobile charges (Q_m), and oxide trapped charges (Q_{ot}). (*Id.*) From the above equation, it is becoming apparent that the V_{FB} may be modulated by eliminating or minimizing

the contribution of the gate oxide charges and/or by engineering Φ_{ms} —either via substrate doping (which tunes Φ_s) and/or via the selection of the metal gate electrode (which defines Φ_m).

59. Based on the above, the threshold voltage may be re-written as follows:

$$V_T \approx \Phi_{ms} + \frac{(Q_f + Q_m + Q_{ot})}{C_o} + 2\psi_B + t_{ox} \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{\varepsilon_o}.$$

Accordingly, and for a given semiconductor and dielectric material, the primary “knobs” that can be used to predictably tune the threshold voltage of a transistor are the substrate doping (N_A), the oxide thickness t_{ox} , and the metal work function Φ_m . (TSMC-1013, 535, 537.) When the substrate doping and the gate oxide thickness are carefully engineered to control channel mobility and the gate capacitance, respectively, the gate electrode work function is the “knob” of choice to optimize (fine-tune) the threshold voltage further. I discuss work function and work function engineering in the next section.

4. Work Function

60. As I discussed above, in addition to body doping and oxide thickness, a “primary parameter that determines the threshold voltage is the *work function* between the gate material and the doping level in the semiconductor.” (TSMC-1011, 526 (italics in original).) A material’s “work function” is “the minimum

energy required to bring an electron from the Fermi level to the vacuum level.”

(TSMC-1029, 117.)

a. “Effective Work Function” of Metal Gate

61. However, in MOS/MIS structures, the metal is in direct contact with a dielectric, not with the vacuum. Moreover, work functions of metal gates are highly dependent on the material properties and interfaces. Thus, a metal work function measured on, for example, tungsten (W), by the photo-electric effect in vacuum, will differ from the work function seen from a tungsten gate threshold voltage calculation. To differentiate this, an “effective work function” of **the metal gate** is commonly used to refer to the metal work function as measured, e.g., through the threshold voltage of the device. I discuss the ’779 patent’s use the term “effective work function” of **the transistor** in §§III.B-C.

b. Gate Electrode Work Function Engineering

62. As I mentioned above, the gate electrode work function (incorporated into V_{FB} term) is the “knob” of choice to optimize the threshold voltage of a transistor. Work function engineering was well-known long before the earliest possible priority date of the ’779 patent.

63. I note that while many papers discuss work function engineering in the context of engineering the gate work functions of nMOS and pMOS transistors,

a POSITA would have recognized that these techniques are equally applicable to tuning the work function among transistors of the same conductivity type—i.e., among nMOS transistors or among pMOS transistors.

64. As I discussed in §III.A.1.a.ii, metal gates are commonly used with high-k gate dielectrics because metal gates eliminate the polysilicon depletion effect, have very low resistance, and have better compatibility with high-k dielectrics (e.g., are immune to Fermi level pinning). However, because the work function of a metal is an intrinsic material property that cannot be easily tuned via doping as in the case of polysilicon gates, introducing metal gates into transistors means that the threshold voltage of the MOSFET becomes tied to the metal selection. (TSMC-1016, 3.) Specifically, for transistors with metal gates, “the metal gate work function needs to be near the silicon conduction band edge for nMOS and near the silicon valence band edge for pMOS to properly set the MOSFET threshold voltage, as with polysilicon gates.” (TSMC-1016, 15, 27.) For example, nMOS transistors require a metal with a work function preferably between about 4.0 eV and about 4.4 eV while pMOS transistors require a metal with a work function preferably between about 4.9 eV and about 5.2 eV. (TSMC-1013, 520.)

65. Many techniques were in use to tune the work function of the metal gate electrode. As one example, the paper, “An Adjustable Work Function Technology Using Mo Gate for CMOS Devices” to Lin, et al. discloses that ion implantation of nitrogen into films decreases (i.e., tunes) the work function in Mo and TiN metal gates. (See TSMC-1032.) Lin specifically found that the work function of Mo could be reduced from 4.95 eV to 4.53 eV, which means that undoped Mo metal gates could potentially be used for pMOS transistors and nitrogen doped Mo metal gates could potentially be used for nMOS transistors. (TSMC-1032, Abstract, 50.)

66. Another class of structures used to tune work function are layered gate structures. In this approach, two metals with different work functions are deposited in sequence and annealed to produce an alloy with a new work function value. (See TSMC-1033, 200.) For example, in the paper, “Dual Work Function Metal Gate CMOS Transistors by Ni-Ti Interdiffusion” to Polishchuk, et al, a layer of low work function Ti is deposited for both nMOS and pMOS transistors. (TSMC-1033, 200, Figure 1(a).) Then, Ni is selectively deposited over the Ti layer in the pMOS transistors, and the stack Ti/Ni is annealed to promote the reaction between the two layers. (TSMC-1003, 200-201, Figure 1(b).) This process achieves two separate work functions for the nMOS and pMOS transistors. The work function of the

pMOS transistors can be controlled by the relative thicknesses of the two metal layers.

5. Other Techniques for Tuning the Threshold Voltage

67. In addition to the techniques discussed above for tuning the work function of a metal gate, the '779 patent acknowledges that the use of a cap layer in the pMIS and nMIS gate insulating film “enable control of a work function of each of the gate electrodes 123a and 123b.” (TSMC-1001, 2:24-27.) U.S. Patent Publication to Mise (TSMC-1006) also discloses the use of W/TiN/MgO (or LaO)/HfSiON gate stacks for nMOS transistors and W/TiN/AlO/HfSiON gate stacks for pMOS transistors. (TSMC-1006, ¶75; *see also*, TSMC-1031, 6:15-24, 8:37-45.) The advantage of the this approach is that only a single layer (i.e., the capping layer) needs to be different between the nMOS and the pMOS gate stacks, which simplifies the transistor fabrication process.

6. Dual-Gate Oxide Thickness

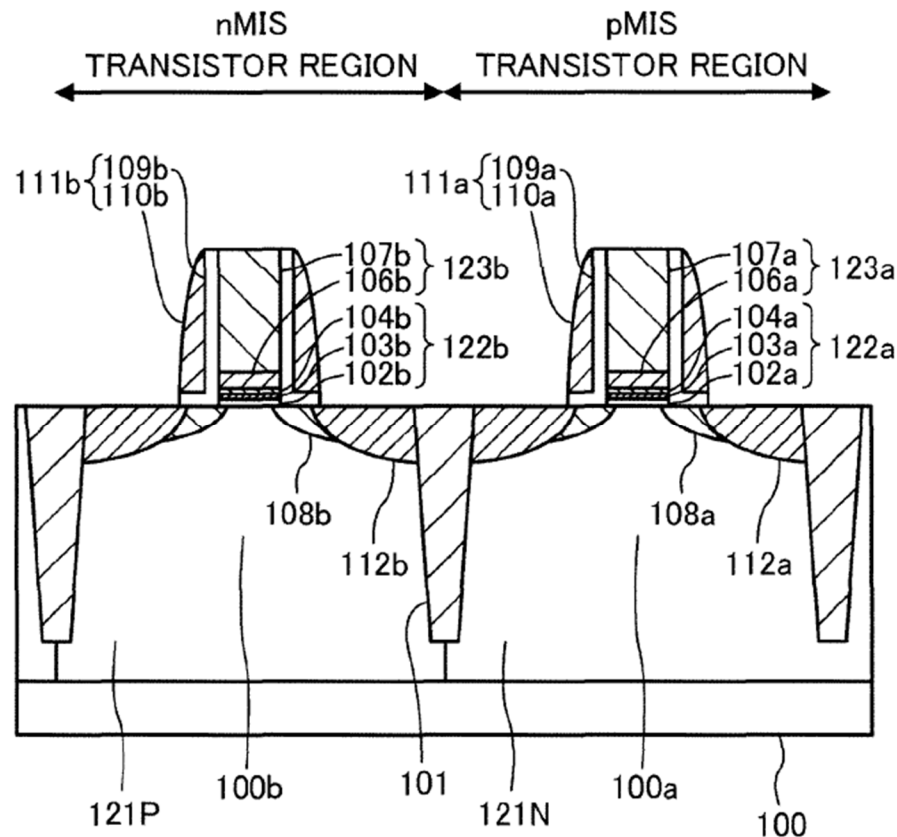
68. Because “[a]n increasing number of mixed-signal and system-on-a-chip applications require dual on-chip power-supply-voltages[,]” different types of transistors of the same conductivity type (e.g., pMOS or nMOS) are needed to handle different power-supply-voltages. (TSMC-1014, 121.) For example, “[t]he higher-voltage may be used for the analog and input/output (I/O) circuitry, and the

lower-voltage for the core-digital-logic devices.” (*Id.*) And since analog and I/O regions of the chip must be able to handle higher operating voltages, “the analog and I/O devices require thicker gate oxides than the core logic devices.” (*Id.*) Accordingly, a dual-gate-oxide (DGO) thickness process was developed to form different gate oxide thicknesses for higher-voltage transistors and lower-voltage transistors. The term DGO devices “relates to devices that are formed on the same substrate, but have different gate oxide thicknesses.” (TSMC-1026, 1:11-13.)

69. Different approaches have been developed to achieve DGO thickness across different transistors. (*See, e.g.*, TSMC-1026, 3:45-4:36 (describing formation of nMOS-DGO with thicker gate oxide than core nMOS), Figures 5-6, 8; TSMC-1027, 5:61-7:58 (describing formation of nMOS-DGO and nMOS core devices).) One approach is to include two oxidation steps “with a masked etch-step in between to remove the first oxide from regions intended to have thinner oxide.” (TSMC-1014, 121.) Another approach is to use nitrogen implants to retard the growth of oxide in selective areas. This is because “the rate of thermal-oxidation on silicon is reduced by nitrogen implants.” (*Id.*) “Hence, nitrogen implantation into the silicon substrate prior to the oxidation process can be used to facilitate the implementation of such “dual-gate-oxide” ICs.” (*Id.*)

B. '779 Patent's Background Section

70. The '779 patent describes a conventional “complementary metal insulator semiconductor (CMIS) device composed of an n-type MIS transistor and a p-type MIS transistor which are provided on an identical substrate.” (TSMC-1001, 1:48-51.) The pMIS transistor, illustrated in Figure 13 below, has “a gate electrode 123a on the active region 100a” with “a gate insulating film 122a interposed between the gate electrode 123a and the active region 100a.” (TSMC-1001, 2:4-11.) Gate insulating film 122a “includes an interface layer 102a made of a silicon dioxide film, a high dielectric constant insulating film (hereinafter, referred to as a high-k film) 103a formed on the interface layer 102a and made of an HfO₂ film, and a pMIS cap film 104a formed on the high-k film 103a.” (TSMC-1001, 2:16-20.)



'779 Patent, Figure 13 [Admitted Prior Art]

71. The nMIS transistor, illustrated in Figure 13 above, similarly has “a gate electrode 123b on the active region 100b” with “a gate insulating film 122b interposed between the gate electrode 123b and the active region 100b.” (TSMC-1001, 2:12-15.) Gate insulating film 122b “includes an interface layer 102b made of a silicon dioxide film, a high dielectric constant insulating film (hereinafter, referred to as a high-k film) 103b formed on the interface layer 102b and made of

an HfO₂ film, and a pMIS cap film formed on the high-k film 103b.” (TSMC-1001, 2:21-27.)

1. Gate Electrode Work Function

72. The background section admits that adjusting the gate electrode work function of a transistor through the use of a cap layer in the gate insulating film was known: “[t]he pMIS cap film 104a and the nMIS cap film 104b enable control of a work function of each of the gate electrodes 123a and 123b.” (TSMC-1001, 2:24-27; *see also*, §III.A.4.)

73. The ’779 patent contends the prior art “method for fabricating the conventional semiconductor device allows nMIS transistors to have only one [gate] work function and pMIS transistors to have only one [gate] work function,” which can be limiting when devices with two or more threshold voltages are required in a single chip—i.e., when “gate structures having different work functions need to be formed in a single chip in order to maximize a transistor driving force at each threshold voltage.” (TSMC-1001, 3:41-49.)

74. As I discussed in §III.A.3-4, techniques for tuning the gate electrode work function and threshold voltage of transistors of the same conductivity type were known long before the ’779 patent.

2. Effective Work Function of a Transistor

75. The '779 patent also refers to an effective work function of a transistor which it describes as “a work function obtained from electrical characteristics of a MIS transistor.” (TSMC-1001, 3:18-19.) The '779 patent contends “the effective work function is obtained by incorporating influence such as a level in an insulating film into a work function related to physical properties and representing a difference between a vacuum level and an energy level of a metal.” (TSMC-1001, 3:20-24.) The '779 patent provides no equations for calculating effective work function or any details of how to determine the effective work function value for a transistor. The '779 patent only broadly relates the thickness of the EOT of the transistor's gate insulating film to its effective work function, as I discuss further below.

C. '779 Patent Overview

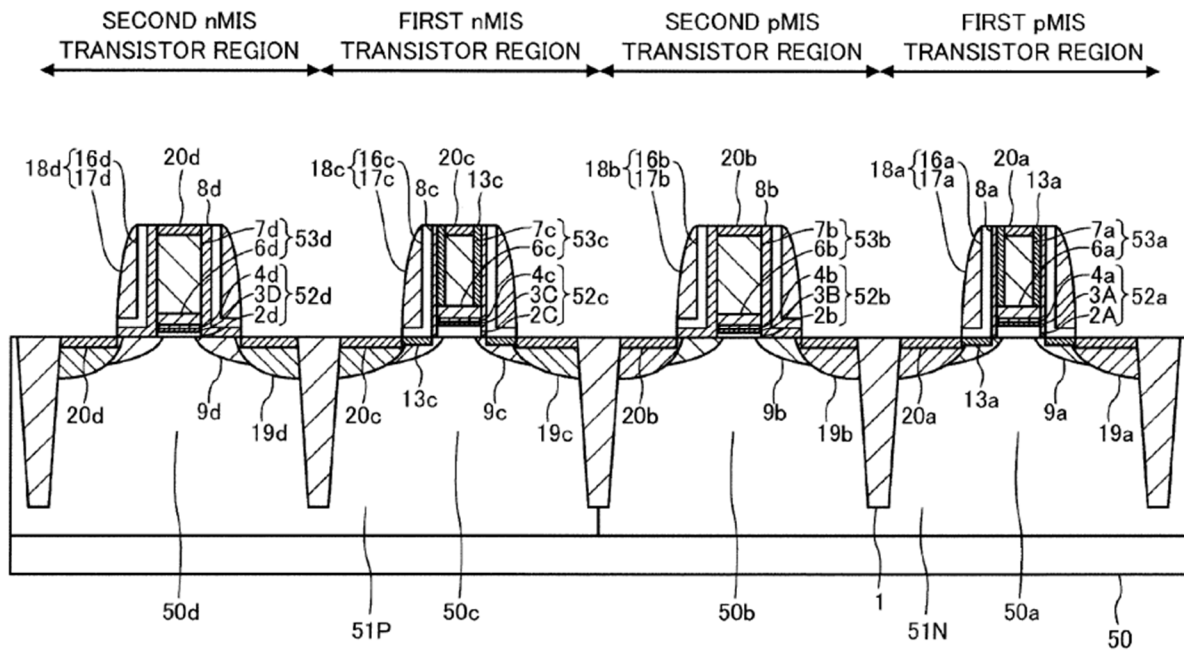
76. In view of the above background, the purported objective of the '779 patent is to “enable formation of a plurality of transistors of the same conductivity type having different work functions in a semiconductor device having a MIS structure in which a high-k film is used as a gate insulating film.” (TSMC-1001, 3:50-54.) Here, my understanding is that the '779 patent is referring to the “effective work function of a transistor.” To “achieve the object” of the '779

patent, the patent purports that the individuals listed as inventors “studied methods for forming gate structures (a gate structure includes a stack of a gate insulating film and a gate electrode) having different [effective] work functions.” (TSMC-1001, 3:55-58.)

77. The ’779 patent therefore presents a semiconductor device in which “the interface layer included in the gate insulating film of the first MIS transistor has a thickness larger than that of the interface layer included in the gate insulating film of the second MIS transistor which is of the same conductivity type as the first MIS transistor.” (TSMC-1001, 4:24-29.) The patent concludes that “since an EOT of the gate insulating film of the first MIS transistor increases, an effective work function of the first MIS transistor increases.” (TSMC-1001, 4:29-31.) Assuming this, for two transistors having the same structure and differing in the EOT of their respective gate insulating films, the transistor with the thicker EOT has a higher effective work function.

78. Figure 9 of the ’779 patent illustrates the semiconductor device summarized above. (TSMC-1001, 7:13-14.) The device includes “First pMIS transistor region” where a first pMIS transistor is formed, “Second pMIS transistor region,” where a second pMIS transistor is formed, “First nMIS transistor region” where a first nMIS transistor is formed, and “Second nMIS transistor region”

where a second nMIS transistor is formed. (TSMC-1001, 7:43-49.) The “first pMIS transistor and the second nMIS transistor are used as low- V_{th} (e.g., 0.1-0.25 V) transistors which are required for high-speed performance.” (TSMC-1001, 7:50-53.) The “second pMIS transistor and the first nMIS transistor are used as high- V_{th} (e.g., 0.35-0.5 V) transistors which are required for reducing a standby leakage current.” (TSMC-1001, 7:53-56.)



'779 Patent, Figure 9

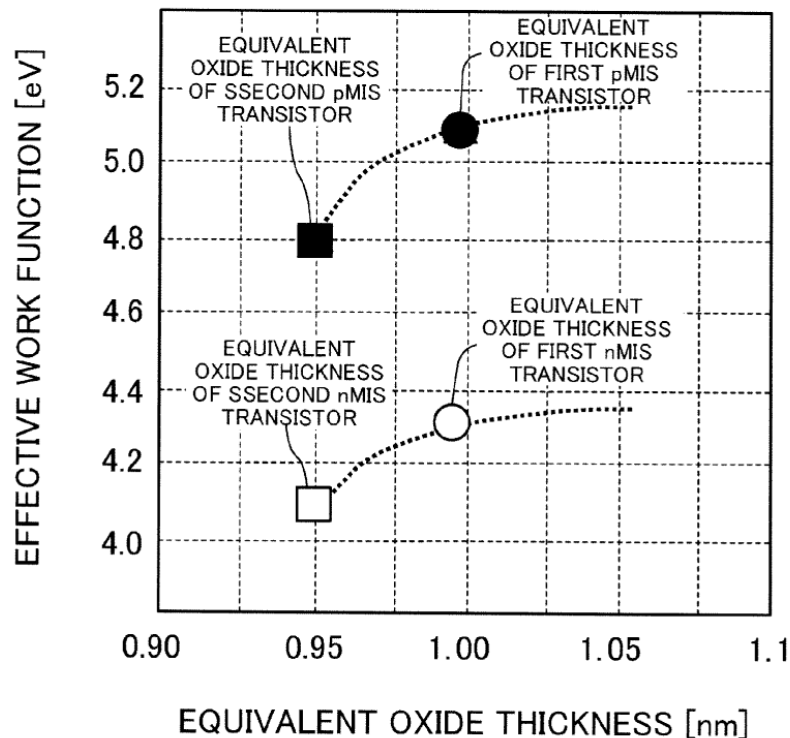
79. Each transistor includes a gate electrode (53a-d) formed on an active region (50a-d) with a gate insulating film (52a-52d) interposed between the gate electrode and active region. (TSMC-1001, 8:47-60.) Each gate insulating film includes an interface layer 2a-2d, a high-k film 3a-3d, and a cap film 4a-4d.

(TSMC-1001, 8:61-67.) The interface layers 2A and 2C in the first nMIS and pMIS regions are thicker than the interface layers 2b and 2d in the second nMIS and pMIS regions. (See TSMC-1001, 9:55-10:5.) The '779 patent discloses that the pMIS cap film and nMIS cap film have different materials. The pMIS film includes “for example, aluminum (Al) and oxygen (O)” and the nMIS film includes “for example, lanthanum (La) and O.” (TSMC-1001, 8:25-30.) The '779 patent notes that Al is “a regulator metal capable of increasing effective work functions of the pMIS transistors” and La is “a regulator metal capable of increasing² effective work functions of the nMIS transistors.” (TSMC-1001, 8:32-37.) These properties of Al and La were known well before the '779 patent's earliest possible priority date. (See TSMC-1019, TSMC-1020, TSMC-1022.)

80. Figure 10, reproduced below, shows the “effective work function” allegedly resulting from the variation in EOT between the first and second transistors. As shown in this figure, “the first pMIS transistor and the first nMIS transistor, because of the thick interface layers 2A and 2C, show an increase in

² The use of “increasing” in this context appears to be an error. A POSITA would have understood that the addition of a La cap has the effect of changing the work function from midgap (4.6 eV) to n-band (4.1 eV) so it is a “decrease.”

equivalent oxide thickness and an increase in effective work function.” (TSMC-1001, 12:47-54; *see also*, TSMC-1001, 4:29-31 (“Accordingly, since an EOT of the gate insulating film of the first MIS transistor increases, an effective work function of the first MIS transistors increases”).)



'779 Patent, Figure 10

81. Specifically, the '779 patent explains that “interface layer 2a included in the gate insulating film 52a of the first pMIS transistor and the interface layer 2c included in the gate insulating film 52c of the first nMIS transistor are selectively increased in thickness.” (TSMC-1001, 13:19-23.) “Accordingly, the EOT of the

gate insulating film 52a of the first pMIS transistor and that of the gate insulating film 52c of the first nMIS transistor increase, **thereby causing** the effective work functions of the first pMIS transistor and the first nMIS transistor to increase.”
(TSMC-1001, 13:23-27.)

D. Prosecution History

1. U.S. Prosecution

82. The '779 patent was filed with 16 claims directed to a “semiconductor device” (1 independent claim and 15 dependent claims). Independent claim 1, as filed, is reproduced below.

1. A semiconductor device comprising:

a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate, wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,

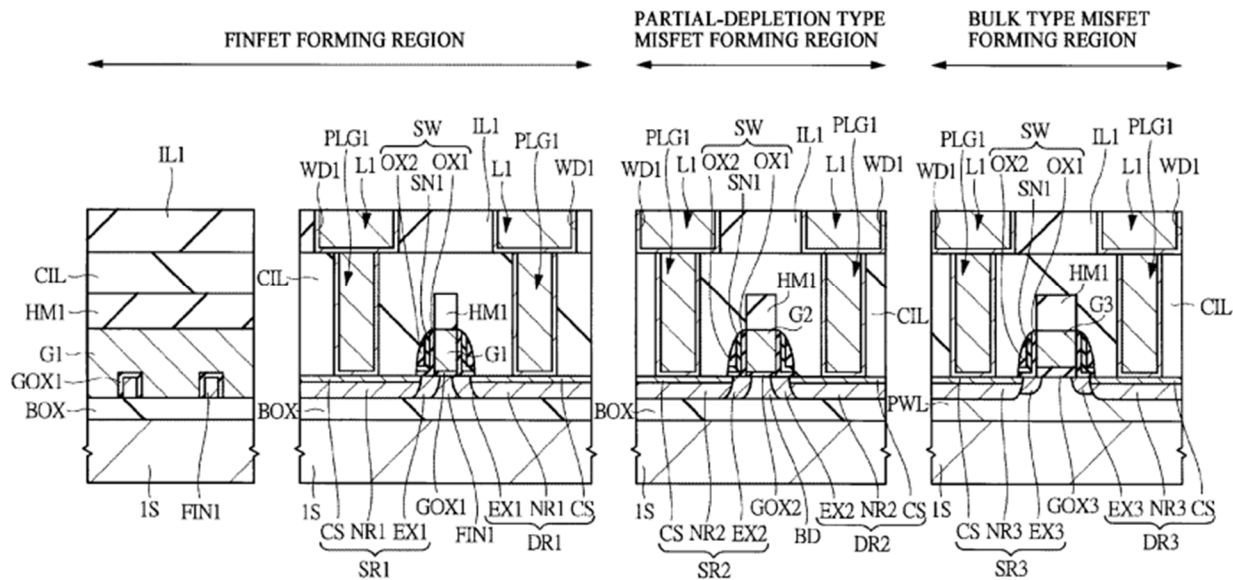
the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,

the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,

the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer, and

the first interface layer has a thickness larger than that of the second interface layer

83. The Examiner rejected the claims as anticipated by U.S. Patent 8,492,230 to Ishikawa, et al. (“Ishikawa”). (TSMC-1002, 204-205.) In response, Applicant distinguished independent claim 1 over Ishikawa based on the limitation that the first and second transistors are “provided on an identical semiconductor substrate.” (TSMC-1002, 298-299.) Specifically, with reference to Ishikawa’s Figure 3 which I have reproduced below, Applicant argued that that the insulating film (GOX3) of the bulk type MISFET is formed on a bulk substrate 1s whereas the insulating film (GOX2) of the partial-depletion MISFET is formed on a silicon-on-insulator (SOI) portion of the substrate 1s. (TSMC-1002, 300.) According to Applicant, in Ishikawa the gate insulating films of the two transistors “are formed above different base substrate[s]” and therefore Ishikawa does not anticipate claim 1. (TSMC-1002, 300-301.)



Ishikawa, Figure 3

84. In addition to this argument, Applicant also amended claim 1 to recite that “each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.” (TSMC-1002, 294.) The Examiner allowed the claims based on this argument and amendment. (TSMC-1002, 312-313.)

2. Foreign Prosecution

85. The JP application was filed on September 14, 2010 with 19 claims directed to a semiconductor device. Originally filed independent claim 1 substantially corresponds to issued claim 1 in the '779 patent and is reproduced below:

A semiconductor device having

a first MIS transistor and a second MIS transistor of the same conductive type on the same semiconductor substrate,

wherein the first MIS transistor comprises a first gate insulating film formed on a first active region in the aforementioned semiconductor substrate and a first gate electrode formed on the first gate insulating film,

and the second MIS transistor comprises a second gate insulating film formed on a second active region in the aforementioned semiconductor substrate and a second gate electrode formed on the second gate insulating film,

the first gate insulating film includes a first interface layer in contact with the aforementioned semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,

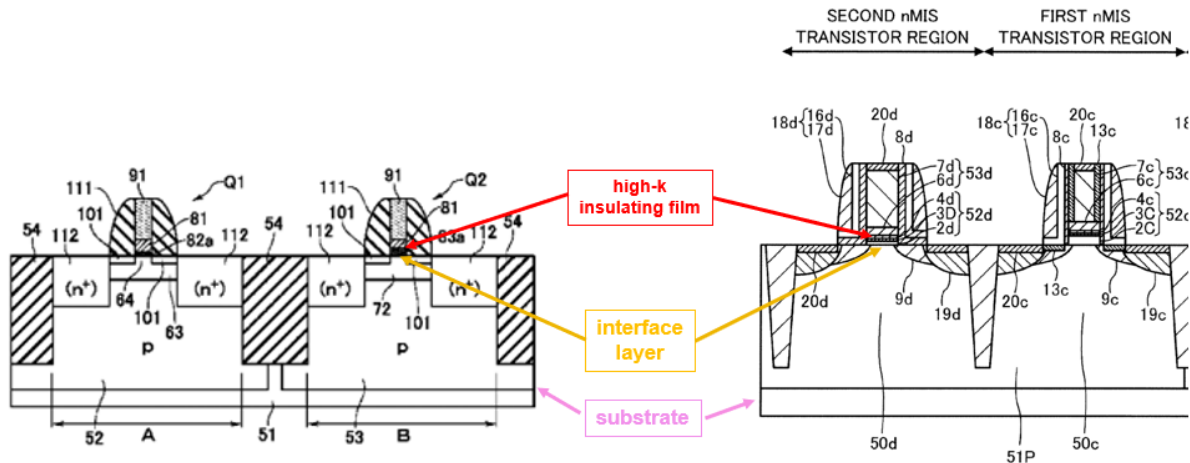
and the second gate insulating film includes a second interface layer in contact with the aforementioned semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,

and the thickness of the first interface layer is greater than the thickness of the second interface layer in the semiconductor device.

(TSMC-1030, 1.)

86. The Japanese Examiner found the claim scope unpatentable, citing JP2003-100896 to Fujiwara (“Fujiwara”), JP2004-079606 to Irino (“Irino”), and JP 2004-140197 to Suzuki (“Suzuki”), all of which disclose transistors of same conductivity type formed on the same substrate with varying the thickness of the interface layer between a high dielectric constant film and the substrate. (TSMC-1030, 4-5.) I have reproduced Figure 11 of Fujiwara below (left) to illustrate the

similarity to the '779 patent's Figure 9 (right). I note that the JP notice of refusal issued on August 20, 2013, prior to the issuance of the '779 patent.



Fujiwara's, Figure 11³; '779 Patent, Figure 9

87. In response, on September 13, 2013, Applicant narrowed the independent claim to recite limitations directed to sidewall spacers: “a first sidewall spacer is formed on a side surface of the first gate electrode with a first insulating spacer interposed therebetween, and a second sidewall spacer is formed on a side surface of the second gate electrode with a second insulating spacer interposed therebetween, ... a thickness of the second insulating spacer is smaller

³ Unless otherwise noted, all shading and annotation to Figures has been added.

than a thickness of the first insulating spacer.” (TSMC-1030, 7.) The Japanese Examiner allowed the claim based on this amendment.

E. Level Of Ordinary Skill In The Art

88. I understand that certain issues relating to the validity of the ’779 patent must be judged from the perspective of a person of ordinary skill in the relevant art, as I discuss below. I have been asked to define the level of a “person of ordinary skill in the art” or “POSITA” at the time the alleged invention as claimed was made. In deciding the level of ordinary skill, I have considered the following factors, which I have been informed are relevant to the determination of ordinary skill in the art.

- levels of education and experience of persons working in the field;
- types of problems encountered in the art;
- prior art solutions to these problems;
- rapidity with which innovations are made; and
- sophistication of the technology.

89. In my opinion, a POSITA at the time of the alleged invention of the ’779 patent would have had at least a Master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing, including planar transistors.

Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. My level of experience, described above, is higher than that of a POSITA.

F. Claim Construction

90. I understand that “claim construction” is the process of determining a patent claim’s meaning. I understand the claim construction standard used in IPRs seeks to give claim terms their plain and ordinary meaning to a POSITA at the time of the claimed invention in view of the claims, specification, and prosecution history. I also understand that if the patent applicant gave a term a special meaning in the specification or during prosecution, then the special meaning should be used.

91. In my declaration, I apply the above understanding. In my view, no claim terms require explicit construction in this proceeding to resolve the patentability of the claims.

IV. Overview of Grounds

92. I discuss three grounds (Grounds 1, 4, 5) demonstrating that independent claim 1 and dependent claims 12-14 are unpatentable and two grounds (Grounds 2, 6) demonstrating dependent claims 8-11 are unpatentable. Regarding claim 15, as I discussed in §§III.B-C, the ’779 patent only discloses adjusting the “effective work function of transistors” of the same conductivity type by altering

the thickness of the interfacial layer of the gate insulating layer and hence the EOT of the gate insulating layer. Claim 15 is specifically directed to this concept, reciting “*an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.*” Grounds 1 and 4 establish the combination renders claim 15 obvious in the same manner as disclosed in the ’779 patent.

93. I understand that PO alleged in the co-pending district court litigation a transistor with an additional metal layer in its gate electrode would demonstrate a slightly higher effective work function than another MIS transistor missing this layer because the additional layer allegedly possesses a higher effective work function. I note that the ’779 patent does not provide any description of adjusting the metal work function of the gate electrode in this manner. I present Grounds 3 and 5 which demonstrates adjusting the metal work function by changing the composition of the gate electrode under PO’s litigation allegations.

V. GROUND 1: Torii Anticipates Claims 1, 12-15

A. Torii

94. U.S. Patent 6,881,657 to Torii, et al. (“Torii”; TSMC-1005) was filed on July 13, 2004 and issued on April 19, 2005. Torii claims priority to JP2003-197954, filed July 16, 2003, over seven years before the ’779 patent.

1. Background Art

95. Torii recognized that “[c]oncurrent with the advance of the down-sizing technology of semiconductor integrated circuits” prior to its priority date, “the dimension of an element has been reduced, and a larger number of elements have been able to be mounted in a chip.” (TSMC-1005, 1:16-19.) As a result, “an integrated-circuit device referred to as SoC (system on chip) that can individually realize functions conventionally realized using a plurality of element[s] has been widely used.” (TSMC-1005, 1:20-23.)

96. Torii notes that “[i]n the **logic circuit** portion of an SoC, it is required to lower the driving voltage for reducing power consumption” and “[a]t the same time, in order to prevent the lowering of the driving current due to the reduction of the driving voltage, the thickness of the gate insulating film of an MOSFET (metal oxide semiconductor field effect transistor) has been reduced.” (TSMC-1005, 1:25-31.)

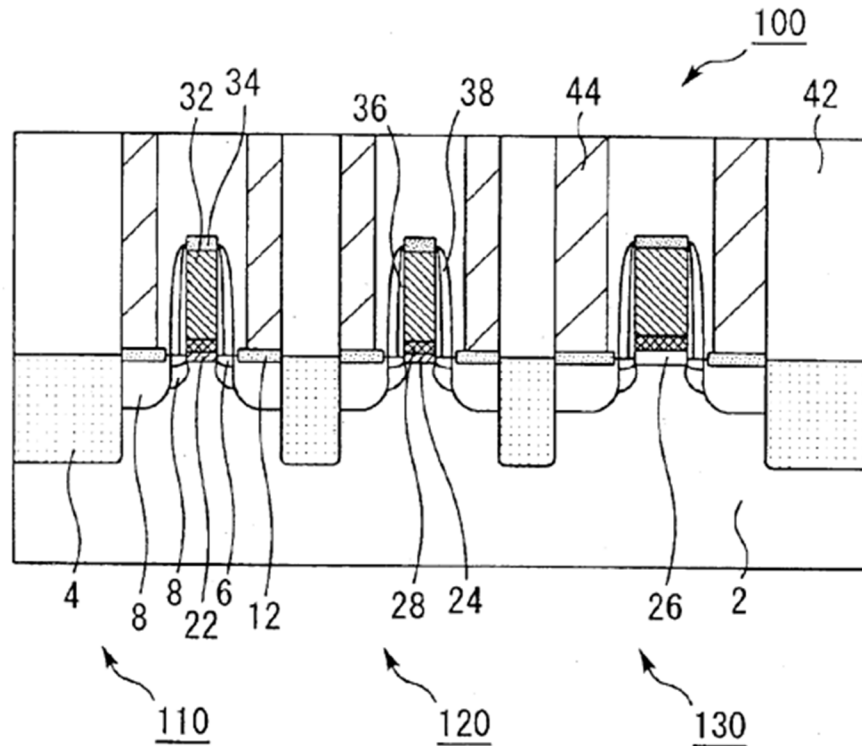
97. “On the other hand, the MOSFET used in the **peripheral circuit** portions accompanying inputs and outputs must be directly driven by an external voltage.” (TSMC-1005, 1:32-34.) A “high withstand voltage is required in the MOSFET used in the peripheral circuit portions, and a gate insulating film having a large film thickness to some extent is required.” (TSMC-1005, 1:34-37.) “For

example, a thick gate insulating film having a thickness of about 6.0 nm to 10 nm has been used in a high-withstand-voltage 3.3V MOSFET.” (TSMC-1005, 1:37-40.)

98. Torii explains that in the art prior to the filing date of its JP provisional, “[w]hen a logic circuit portion and a peripheral circuit portion are formed in a semiconductor device, **the gate insulating films of the different thickness require to be formed in these circuit portions on a substrate.**” (TSMC-1005, 1:41-44.) Torii presents several prior art methods for forming gate insulating films of different thicknesses but notes problems associated with each. Torii “proposes the solution of” these problems. (TSMC-1005, 3:54-55.)

2. Overview of Torii

99. Torii “relates to a semiconductor device having a plurality of transistors comprising gate insulating films of different film thickness.” (TSMC-1005, 1:11-14.) Torii’s semiconductor device of a first embodiment, illustrated in Figure 1 below, “is composed of a MISFET (metal insulator semiconductor field effect transistor) 110 for LOP (low operating power) ...; an MISFET 120 for LSTP (low stand-by power) ...; and an MISFET 130 for high withstand voltage” (TSMC-1005, 4:61-5:4.)



Torii, Figure 1

100. Torii acknowledges that LOP MISFETs, which require “relatively high-speed operation,” and LSTP MISFETs, “which require both the operation speed for a long time operated by batteries and high performance,” are essential components in logic circuit portions of “an integrated-circuit device referred to as SoC (system on chip).” (TSMC-1005, 2:51-65, 1:20-21.) As I mentioned above, “the logic circuit portion of an SoC, [] is required to lower the driving voltage for reducing power consumption.” (TSMC-1005, 1:24-25.) Meanwhile, MISFETs withstanding high operating voltages (e.g., external voltages), such as MISFET

130, are formed in the peripheral circuit portions of the SoC. (TSMC-1005, 1:32-34, 2:51-61.)

101. Because these types of transistors have different purposes in the SoC circuit, “the thickness of the gate insulating films in these MISFETs is different from each other.” (TSMC-1005, 3:1-2.) For instance, “[t]he ITRS (The International Technology Roadmap for Semiconductors)⁴ recommends that the EOT of a gate insulating film of the MISFET for LOP in a 65-nm technology node is 1.0 nm to 1.4 nm, and the EOT of the MISFET for LSTP is 1.2 to 1.6 nm as the target values.” (TSMC-1005, 3:2-8) That is, “the difference between the thickness of MISFETs for LOP and LSTP is 0.2 nm to 0.4 nm.” (TSMC-1005, 3:9-10.) In other words, building transistors with gate insulating films having different thicknesses was contemplated in the semiconductor industry well before the ’779 patent.

⁴ The ITRS roadmap is a set of documents that was coordinated and organized by Semiconductor Research Corporation and produced by a group of experts in the semiconductor industry. (*See, e.g.*, TSMC-1016.)

B. Independent Claim 1

102. Torii teaches every limitation of independent claim 1. I note the striking similarity between Torii's issued claim 1 (below left) and claims 1 and 13 of the '779 patent in the table below.

Torii – Claim 1	'779 Patent – Claims 1 and 13
1. A semiconductor device comprising; a substrate, a first field-effect transistor, including a first gate insulating film and a first gate electrode, on the major surface of said substrate, and	1. A semiconductor device comprising: a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate, wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,
a second field-effect transistor, including a second gate insulating film and a second gate electrode, on the major surface of said substrate, wherein	the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,
each of said first gate insulating film and said second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film,	the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,

Torii – Claim 1	'779 Patent – Claims 1 and 13
	the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,
equivalent-oxide thickness of said first gate insulating film is thicker than equivalent-oxide thickness of said second gate insulating film, and	the first interface layer has a thickness larger than that of the second interface layer, and
	each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film .
the high-dielectric-constant film in said first gate insulating film-has the same thickness as the high-dielectric-constant film in said second gate insulating film.	13. The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.

1. Preamble

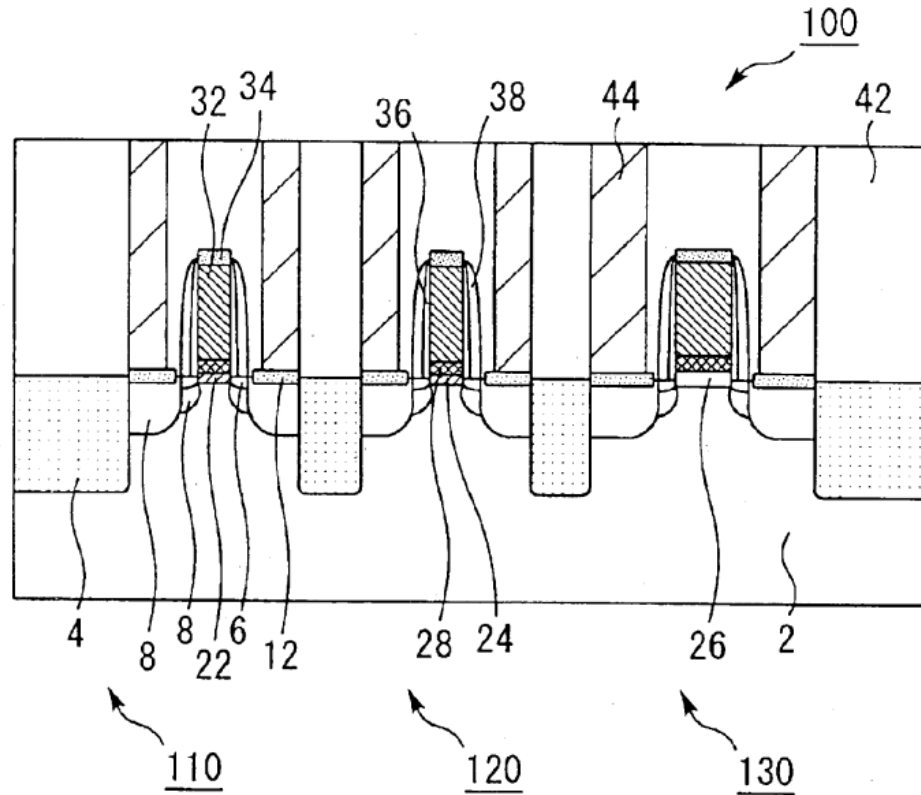
[1P] *A semiconductor device*

103. Torii discloses a “*semiconductor device*”⁵. Torii discloses that its “present invention relates to a **semiconductor device**⁶ having a plurality of transistors comprising gate insulating films of different film thickness.” (TSMC-1005, 1:11-14.) Torii stresses that “it is the object of the present invention to provide a **semiconductor device** wherein gate insulating films highly controlled their thickness are formed when a plurality of transistors are formed on a chip, even if the difference between the thickness of the gate insulating films is small.” (TSMC-1005, 3:54-60.)

104. Specifically, in “one aspect” corresponding to the first embodiment, the “**semiconductor device**” includes a first FET and a second FET formed on a common substrate. (TSMC-1005, 3:62-65.) Figure 1, reproduced below, depicts this aspect, referring to the device a “system on chip” or SoC. (TSMC-1005, 4:30-32.)

⁵ Claim language is indicated by italics throughout.

⁶ Unless otherwise noted, all emphasis added.



Torii, Figure 1

105. Torii's issued claims also confirm that Torii discloses a “*semiconductor device*.” Independent claim 1 recites a “**semiconductor device** comprising” and independent claim 9 recites a “method for manufacturing a **semiconductor device**.”

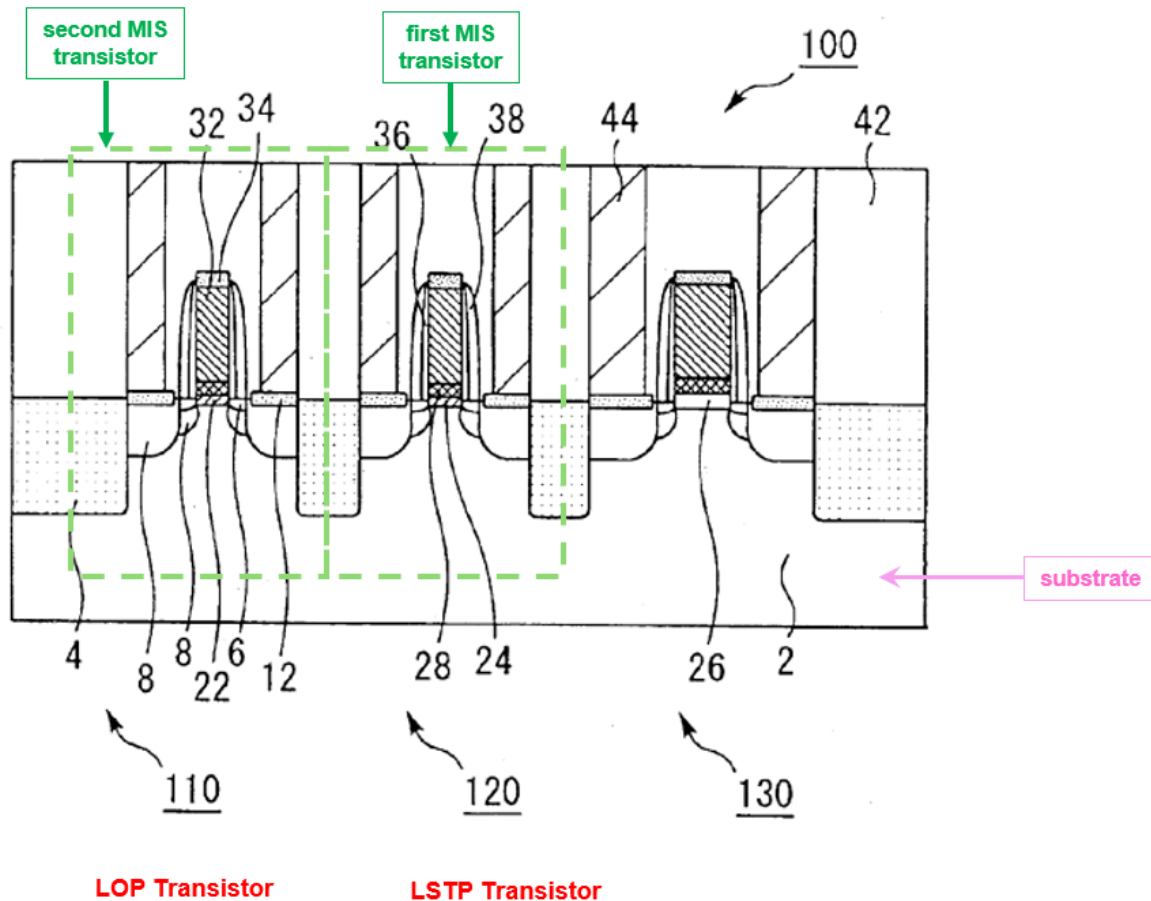
2. Limitations [1A]-[2A]

[1A] *a first MIS transistor and [2A] a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate*

106. Torii's "*semiconductor device*" includes "[1A] *a first MIS transistor* and [2A] *a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate.*"

107. Torii's device includes a Si substrate 2 ("*semiconductor substrate*") having regions "isolated by STI (shallow trench isolation) 4." (TSMC-1005, 5:1-4.) The "Si substrate 2 is divided into a region for forming **an MISFET** for LOP [low operating power] 110, a region for forming **an MISFET** for LSTP [low stand-by power] 120, and a region for forming **an MISFET** for high withstand voltage 130." (TSMC-1005, 6:14-18; *see also*, 4:61-67.) I note that Torii's gate electrode is formed of a "polycrystalline silicon film" 54, not of a metal. (TSMC-1005, 7:6-10.) Torii's usage of "MIS" to refer to its transistors with a conductive gate electrode (whether metal or another conductive material) is consistent with the common convention in the field prior to the '779 patent (and today). Weste explains "[g]ates of early transistors were built from metal, so the stack was called metal-oxide-semiconductor, or MOS" and "[n]ow the gate is typically formed from polycrystalline silicon (*polysilicon*), but **the name stuck.**" (TSMC-1012, 8 (emphasis by italics in original); *see also*, TSMC-1007, 2:22-29.) Indeed, the gate electrode of the '779 patent also includes "a silicon film 7". (*See, e.g.*, TSMC-1001, 9:1-2.) Torii's LSTP transistor is therefore the recited "*first MIS transistor*"

and the LOP transistor is the recited “*second MIS transistor*.” Figure 1 of Torii below highlights these features.



Torii, Figure 1

108. In Torii’s method of manufacturing the device of Figure 1, Torii explains that “[f]irst, an STI 4 is formed on an Si substrate 2, and the Si substrate 2 is divided into a region for forming an MISFET for LOP 110, a region for forming an MISFET for LSTP 120, and a region for forming an MISFET for high withstand voltage 130.” (TSMC-1005, 6:14-18.) Because the LOP, LSTP, and MISFET

transistors are formed in a common substrate, the transistors are “*provided on an identical substrate.*” This is confirmed by Torii’s “summary of the invention” in which Torii indicates that “[a]ccording to one aspect of the present invention, a semiconductor device comprises a substrate, and a first field-effect transistor and a second field effect transistor **formed on the substrate.**” (TSMC-1005, 3:62-65.) Torii’s independent claims 1 and 9 also reflect that the transistors are provided on a common (i.e., the “*identical*”) substrate. (See TSMC-1005, claims 1 and 9.)

109. Torii teaches that “in the first embodiment, the case wherein an n-type transistor is formed is described.” (TSMC-1005, 10:39-40.) An n-type transistor is also referred to as an nMIS transistor. (See, e.g., TSMC-1012, 8, Figure 1.8(a); §III.A.1.) Thus, Torii further teaches that the “*first MIS transistor and a second MIS transistor [are] of an identical conductivity type*” (i.e., n-type).

110. Torii further teaches that its “present invention may be applied to the case wherein a p-type transistor is formed.” (TSMC-1005, 10:40-42.) A p-type transistor is also referred to as a pMIS transistor. (See TSMC-1012, 8, Figure 1.8(b); §III.A.1.) In this implementation, the “*first MIS transistor and a second MIS transistor [are] of an identical conductivity type*” (i.e., p-type).

3. Limitations [1A.1]-[1A.2]/[2A.1]-[2A.2]

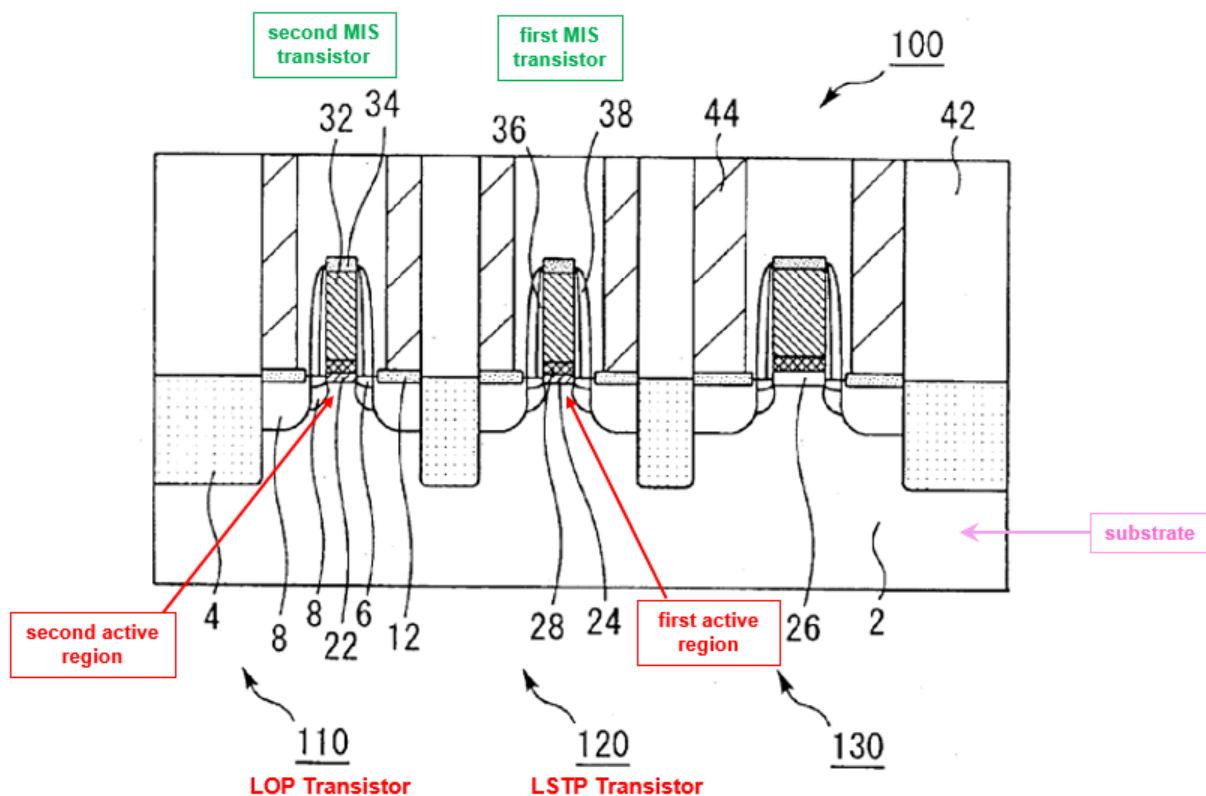
111. Independent claim 1 recites features associated with “*the first MIS transistor*” in limitations [1A.1] and [1A.2]: “*a first gate insulating film*” including a “*first interface layer*” and “*a first high dielectric constant insulating film*” and “*a first gate electrode*.” Claim 1 also recites identical features associated with “*the second MIS transistor*” in limitations [2A.1] and [2A.2]: “*a second gate insulating film*” including a “*second interface layer*” and “*a second high dielectric constant insulating film*” and “*a second gate electrode*.” I reproduce the complete claim language below. For ease of discussion, I address these limitations together in this section.

- [1A.1] *wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film*
- [2A.1] *the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,*
- [1A.2] *the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,*
- [2A.2] *the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,*

a. “Active Region[s] in the Semiconductor Substrate”

112. As I discussed in §V.B.2, Torii teaches that “the Si substrate 2 is divided into a region for forming an MISFET for LOP 110, a region for forming an MISFET for LSTP 120, and a region for forming an MISFET for high withstand voltage 130.” (TSMC-1005, 6:14-18.) Torii refers to these as “the region for LOP”, “the region for LSTP”, and the “region for high withstand voltage.” (TSMC-1005, 6:18-23.) As shown in Figure 1 below, these regions are “isolated by STI (shallow trench isolation) 4.” (TSMC-1005, 5:1-3.) The LOP region and LSTP region are therefore each an “active region.” (See, e.g., TSMC-1015, 52-53 (regions between

isolation structures “where transistors will be built, are called the ‘active’ regions of the substrate”).) Torii’s teachings are consistent with the disclosure in the ’779 patent. In the background section, the ’779 patent explains that “a portion of the semiconductor substrate 100 surrounded by the shallow trench isolation 101 and located in the nMIS transistor region **serves as an active region 100b.**” (TSMC-1001, 1:67-2:3.)



Torii, Figure 1

113. Torii’s fabrication method confirms the presence of an “*active region*” in each transistor. In its discussion of the method for manufacturing the device of

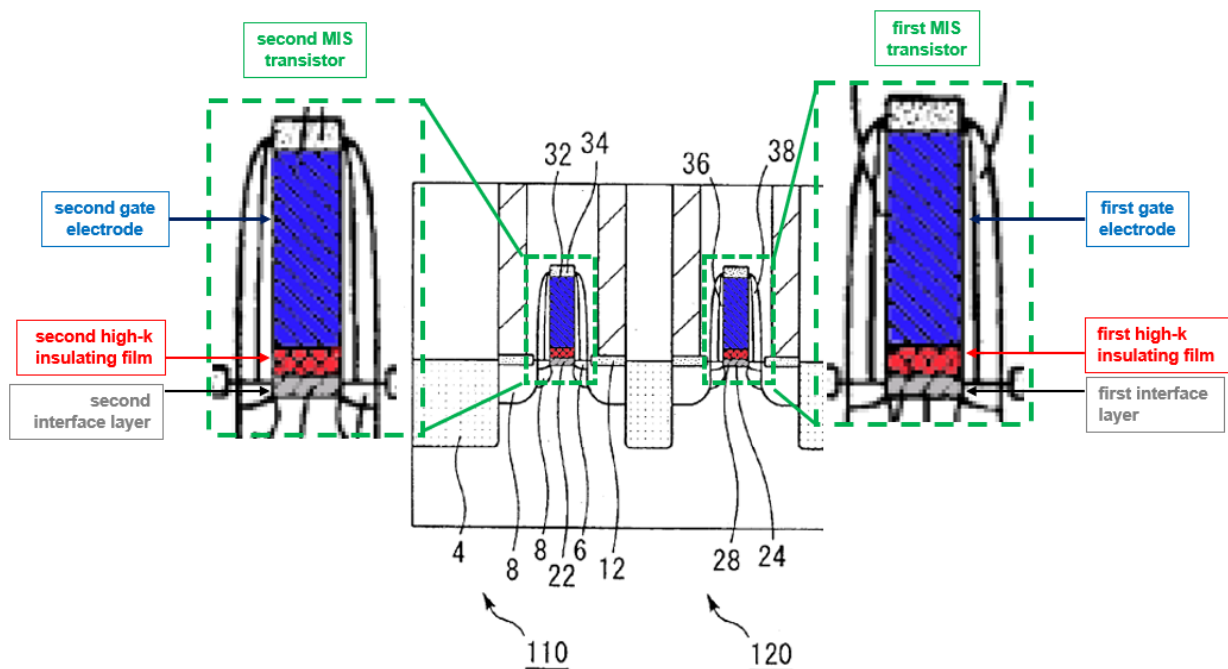
Figure 1, Torii notes that, prior to its Step S2, “implantation of p-type ions for controlling the impurity content in the substrate, heat treatment the impurity diffusion, ion implantation for controlling the threshold voltage, and heat treatment for activation are performed.” (TSMC-1005, 6:24-27.) These steps indicate that the areas bounded by STI 4 are “*active regions*.” Indeed, Torii teaches “[o]n each region of the Si substrate isolated by STI 4, a **source-drain extension 6**, which is a diffusion layer having a relatively shallow junction and a low impurity content is formed, and a **punch-through stopper 8** is formed underneath the source-drain extension 6” and “[o]utside each source-drain extension 6, a **source-drain region 10**, which is a diffusion layer having a relatively deep junction and a high impurity content is formed.” (TSMC-1005, 5:5-12.)

114. As highlighted in Figure 1 above, the LSTP transistor (“*first MIS transistor*”) includes a “*first active region in the semiconductor substrate*” and the LOP transistor (“*second MIS transistor*”) includes a “*second active region in the semiconductor substrate*.”

b. “Gate Insulating Film” Limitations

115. Torii teaches that in its SoC 100 (“*semiconductor device*”), the LSTP transistor (“*first MIS transistor*”) includes “*a first gate insulating film*” and the LOP transistor (“*second MIS transistor*”) includes “*a second gate insulating film*.”

As shown in the enlargements of the LSTP and LOP transistors in Figure 1 below, in Torii's LOP transistor, "silicon oxynitride film 22 [shaded grey] is formed as an **interfacial** gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2." (TSMC-1005, 5:14-17; *see also*, TSMC-1005, 6:55-63.) In the LSTP transistor, "a silicon oxynitride film 24 [shaded grey] is formed in an equivalent area." (TSMC-1005, 5:17-18.) On each of silicon oxynitride films 22 and 24, a "**high-k film** [shaded red] such as a hafnia (HfO_2) film 28" is formed. (TSMC-1005, 5:33-36; *see also*, TSMC-1005, 6:66-7:5, 8:14-23.)



Torii, Excerpt from Figure 1 with enlargements

116. Torii refers to oxynitride film and high-k film collectively as an "insulating film of a laminate structure." (See TSMC-1005, 8:14-18 ("According to

the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively”).) I note that in the summary of the invention, Torii also refers to these films collectively as “*gate insulating films*”: “Each of the first gate insulating film and the second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film.” (TSMC-1005, 4:1-4.) This convention is also repeated in Torii’s claim 1 which recites:

1. A semiconductor device comprising;
a substrate,
a first field-effect transistor, including a **first gate insulating film** and a first gate electrode, on the major surface of said substrate, and
a second field-effect transistor, including a **second gate insulating film** and a second gate electrode, on the major surface of said substrate, wherein
each of said **first gate insulating film and said second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film,**

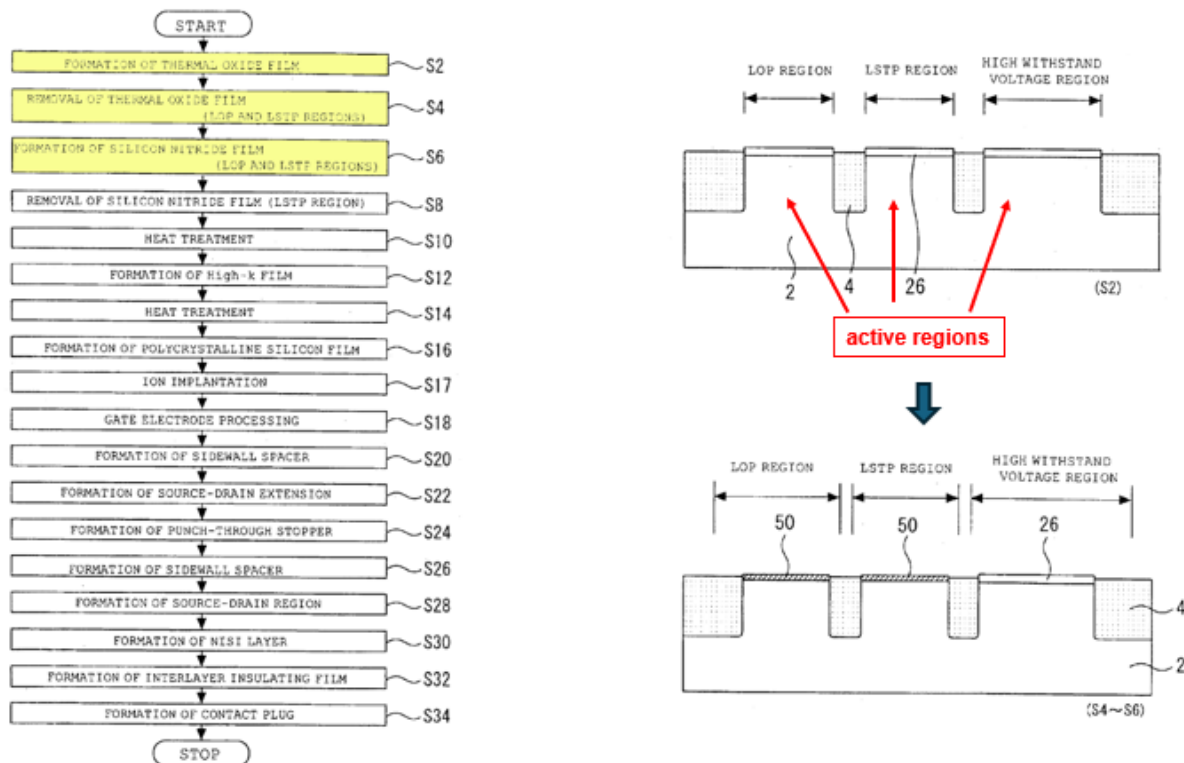
117. Thus, oxynitride film 24 and high-k film 28 are collectively “*a first gate insulating film*” of the “*first MIS transistor*” (LSTP transistor) and oxynitride film 22 and high-k film 28 are collectively “*a second gate insulating film*” of the “*second MIS transistor*” (LOP transistor).

118. Silicon oxynitride film 24 is the “*first interface layer*” and silicon oxynitride film 22 is the “*second interface layer*.” Torii explicitly refers to silicon oxynitride film 22, 24 as “an interfacial gate insulating film.” (See TSMC-1005, 5:14-17 (“a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2”), 9:32-38 (“the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film”).)

119. As shown in the enlargements of Figure 1 above, oxynitride films 24 and 22 are “*in contact with the semiconductor substrate*” and therefore the “*gate insulating film* [oxynitride film 24/22 and high-k film 28]” of both the LSTP and LOP transistors is “*formed on a [first/second] active region in the semiconductor substrate*.” This is confirmed by the method of manufacturing the device of Figure 1. In my discussion below, I have included the flow diagram of the method in the figures below at the left with intermediate device structures at the right.

120. In Step S2, “a thermal oxide film 26 of a thickness of about 5 nm is formed” on the Si substrate 2. (TSMC-1005, 6:28-29.) Figure 3 (right-top) illustrates the device after this intermediate step. Next, “heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds”

and “[t]hereby a silicon nitride film of a thickness of about 0.6 nm is formed in each of the regions for LOP and LSTP.” (TSMC-1005, 6:37-41.) This process is reflected by Step S6 which states “a silicon nitride 50 is formed in each of the regions for LOP and LSTP.” (TSMC-1005, 6:36-37.) Figure 4 (right-bottom) illustrates the device after this intermediate step.

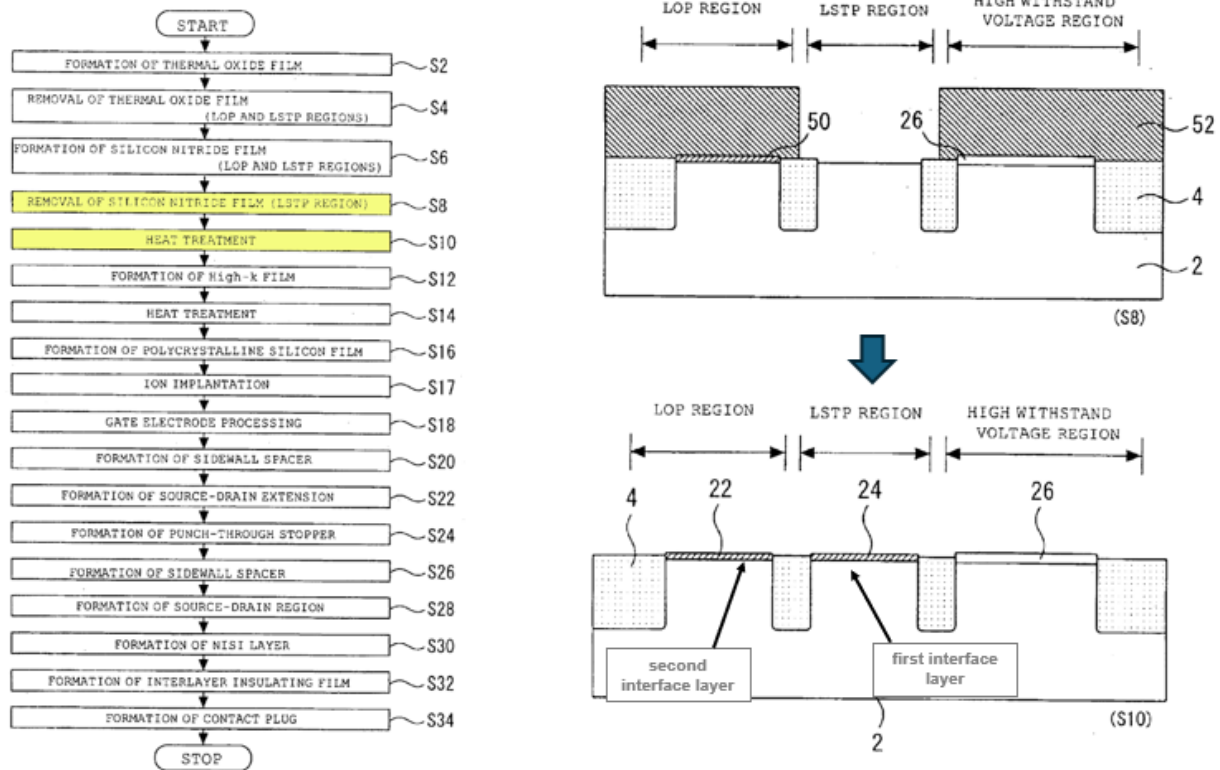


**Torii, Figure 2 (left), Figure 3 (right-top),
Figure 4 (right-bottom)**

121. The regions for LOP and high withstand voltage “are coated with a resist mask 52 [and] wet etching is performed to remove silicon nitride film 50.” (TSMC-1005, 6:47-50.) This is reflected in Step S8 which states “silicon nitride

film 50 in the region for LSTP is removed (Step S8).” (TSMC-1005, 6:46-47.)

Figure 5 (right-top) illustrates the intermediate device.



**Torii, Figure 2 (left), Figure 5 (right-top),
Figure 6 (right-bottom)**

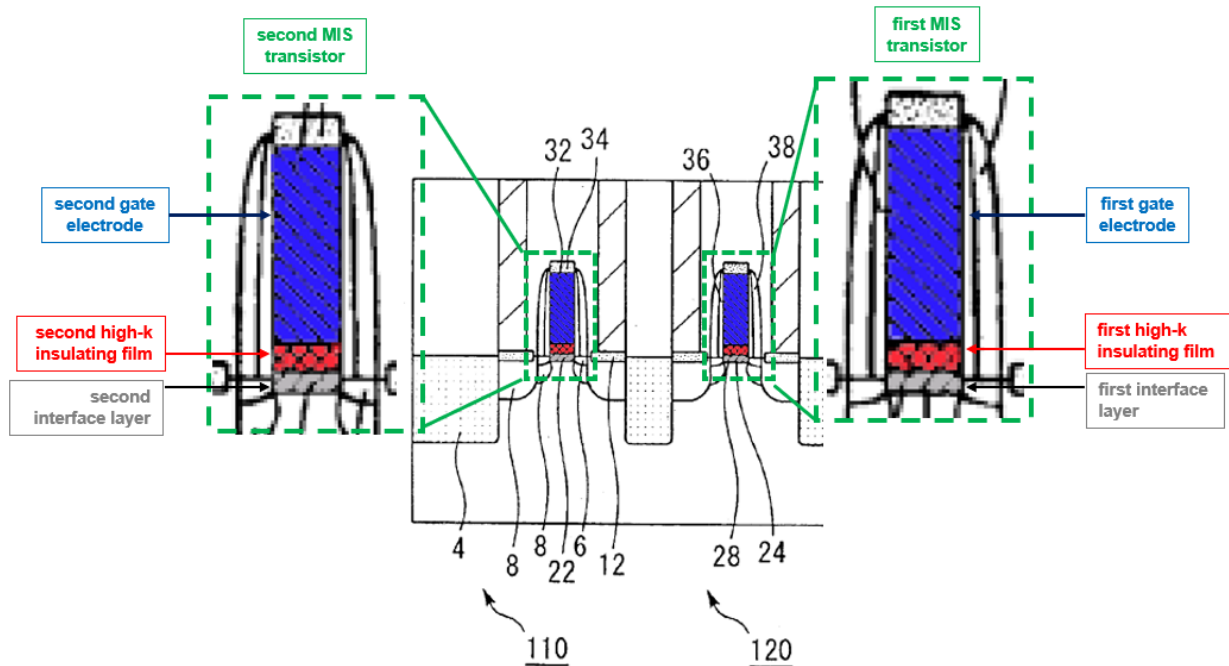
122. The resist mask is removed and “heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10).” (TSMC-1005, 6:52-53.) In this step, the “temperature of the heat treatment is about 800 to 900° C., and the treating time is about 5 to 60 seconds” and “thereby ... a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP.” (TSMC-1005, 6:53-57.) That is, silicon oxynitride film 24 (“*first*

interface layer”) is “*in contact with the semiconductor substrate*” and therefore the “*first gate insulating layer*” is “*formed on a first active region in the semiconductor substrate.*” The silicon nitride film 50, formed in the region for LOP, is also “oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm.” (TSMC-1005, 6:57-60.) Figure 6 (right-bottom) illustrates the intermediate device. As a result of this step, silicon oxynitride film 22 (“*second interface layer*”) is “*in contact with the semiconductor substrate*” and therefore the “*second gate insulating layer*” is “*formed on a second active region in the semiconductor substrate.*”

123. As confirmed by the process steps, Torii’s LSTP transistor (“*the first MIS transistor*”) includes “*a first gate insulating film **formed on a first active region in the semiconductor substrate***” [1A.1] with “*a first interface layer [oxynitride film 24] **being in contact with the semiconductor substrate***” [1A.2]. Torii’s LOP transistor (“*the second MIS transistor*”) similarly includes “*a second gate insulating film **formed on a second active region in the semiconductor substrate***” [2A.1] with “*a second interface layer [oxynitride film 22] **being in contact with the semiconductor substrate***” [2A.2].

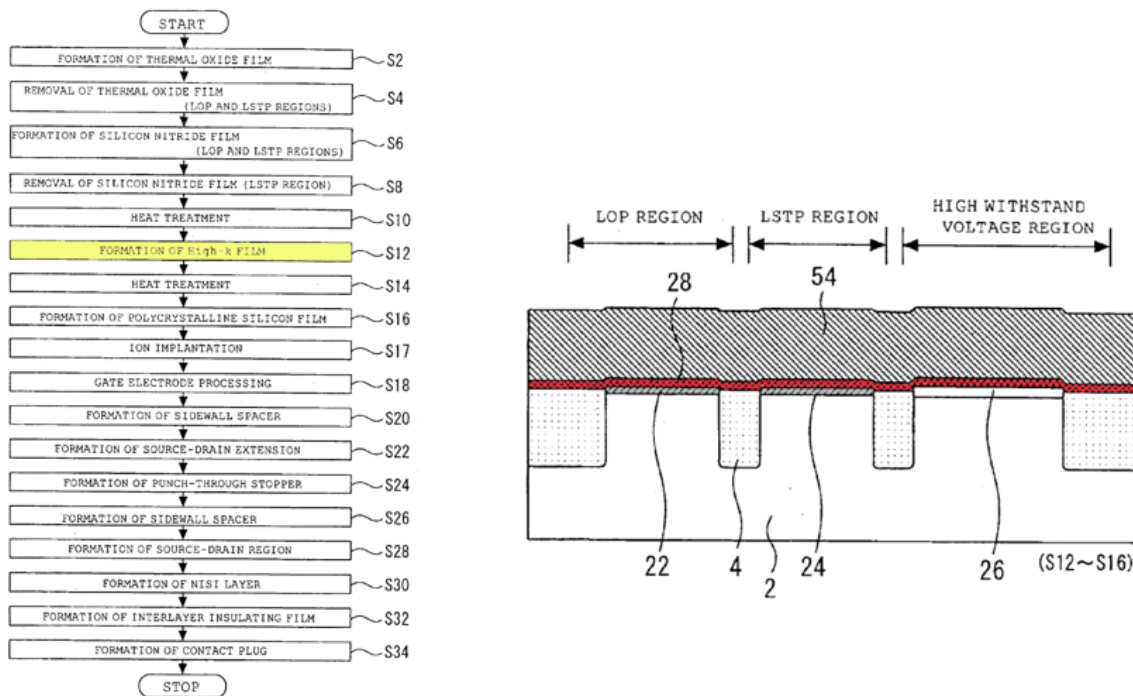
124. On each of silicon oxynitride films 22 and 24, a “high-k film [shaded red] such as a hafnia (HfO₂) film 28” is formed. (TSMC-1005, 5:33-36.) The high-

k film in each of the LSTP and LOP transistors, illustrated in the device of Figure 1, is the “[*first*]/[*second*] high dielectric constant insulating film.”



Torii, Excerpt from Figure 1 with enlargements

125. As shown above, the high-k film 28 (shaded red) in both the LSTP and LOP transistors is “formed on the [*first/second*] interface layer.” This is confirmed by the method of manufacturing the device of Figure 1. Specifically, “a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method.” (TSMC-1005, 6:67-7:3.) This process is reflected in Step S12 which states “high-k film 28 [shaded red] is formed on the entire surface of the substrate.” (TSMC-1005, 6:66-67.) Figure 7 (below right) illustrates the intermediate device.

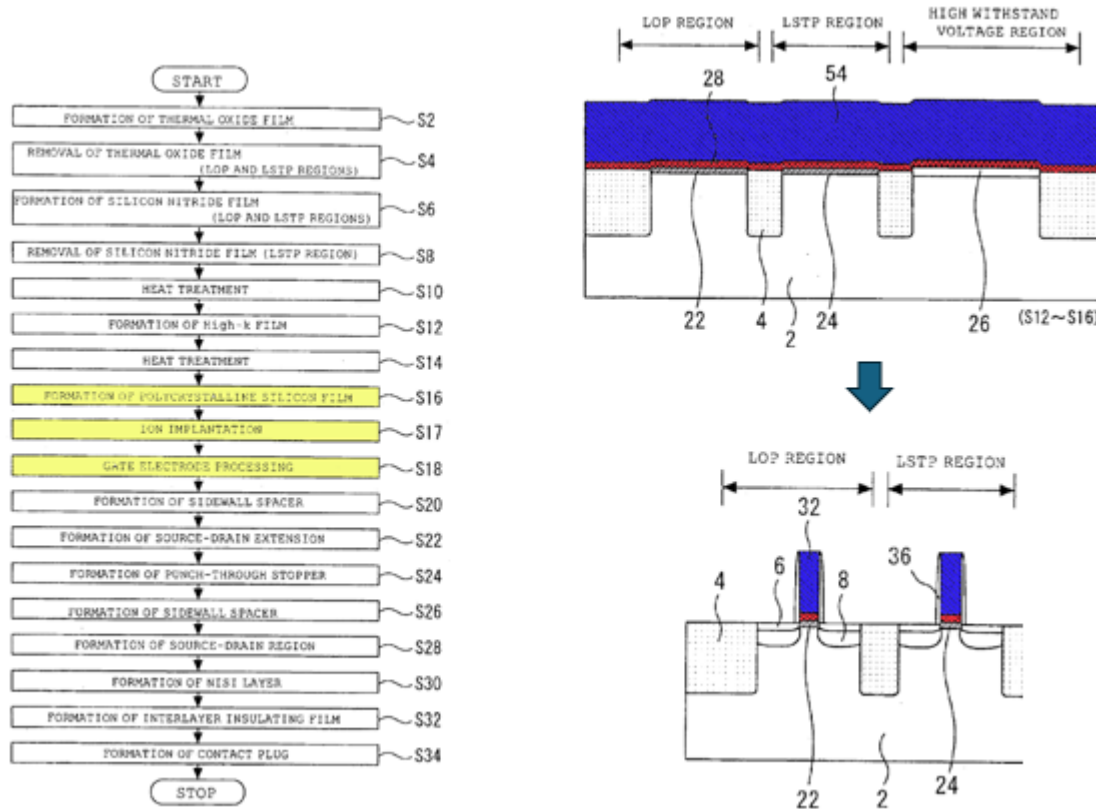


Torii, Figure 2 (left), Figure 7

c. “Gate Electrode” Limitations

126. Torii further teaches that each of its LSTP and LOP transistors includes a “gate electrode formed on the [first/second] gate insulating film.” Torii teaches that “[o]n each high-k film 28, a gate electrode 32 [shaded blue] is formed” as highlighted in the enlargements of portions of Figure 1 above. (TSMC-1005, 5:42.) This is confirmed by the method of manufacturing the device of Figure 1. Specifically, a non-doped polycrystalline silicon film 54, “a material film for gate electrodes”, “is formed on the high-k film 28” in Step S16, as shown in Figure 7 (right-top). (TSMC-1005, 7:6-9.) “Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54” in Step S17.

(TSMC-1005, 7:9-12.) The “polycrystalline silicon film 54 is processed for a gate electrode 32 of each region” in Step S18, illustrated in the excerpt from Figure 8 (right-bottom). (TSMC-1005, 7:13-15.)



**Torii, Figure 2 (left), Figure 7 (right-top),
Excerpt from Figure 8 (right-bottom)**

* * *

127. In summary, the “*first MIS transistor* [LSTP transistor]” of Torii’s device includes “*a first gate insulating film* [silicon oxynitride film 24 and high-k film 28] *formed on a first active region in the semiconductor substrate and a first*

gate electrode formed on the first gate insulating film” [1A.1] where “the first gate insulating film includes a first interface layer [silicon oxynitride film 24] being in contact with the semiconductor substrate and a first high dielectric constant insulating film [high-k film 28] formed on the first interface layer” [1A.2].

128. And the “second MIS transistor [LOP transistor]” of Torii’s device further includes “a second gate insulating film [silicon oxynitride film 22 and high-k film 28] formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film” [2A.1] where “the second gate insulating film includes a second interface layer [silicon oxynitride film 22] being in contact with the semiconductor substrate and a second high dielectric constant insulating film [high-k film 28] formed on the second interface layer” [2A.2].

4. Thickness Limitation [1B]

[1B] <i>the first interface layer has a thickness larger than that of the second interface layer</i>

129. In Torii’s semiconductor device (SoC 100), “the first interface layer [oxynitride film 24]” of the LSTP transistor “has a thickness larger than that of the second interface layer [oxynitride 22]” of the LOP transistor.

130. Torii “relates to a semiconductor device having a plurality of transistors comprising **gate insulating films of different film thicknesses.**”

(TSMC-1005, 1:11-13.) Torii also notes that the EOT of the gate insulating film of the first transistor is greater than the EOT of the second transistor: “[t]he equivalent-oxide thickness of the first gate insulating film is thicker than the equivalent-oxide thickness of the second gate insulating film.” (TSMC-1005, 4:4-6; *see also*, claim 1 (“equivalent-oxide thickness of said first gate insulating film is thicker than equivalent-oxide thickness of said second gate insulating film”).) Because both transistors use the same material for the interface layer and both have high-k layers with identical thicknesses and EOTs, a higher gate insulating film EOT indicates a thicker interface layer. (*See* §§III.A.1.a.i, V.E.)

131. More specifically, in the LSTP transistor (the “*first MIS transistor*”), the “thickness of the silicon oxynitride film 24 [*“first interface layer”*] ... is about 1.3 nm; and the EOT [equivalent oxide thickness] thereof is about 1.0 nm.” (TSMC-1005, 5:23-25.) In the LOP transistor (the “*second MIS transistor*”), “the thickness of the silicon oxynitride film 22 [*“second interface layer”*] ... is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm.” (TSMC-1005, 5:20-23.) That is, the silicon oxynitride film 24 in the LSTP MISFET 120 is thicker than the silicon oxynitride film 22 in the LOP MISFET 110.

132. Thus, Torii teaches “*the first interface layer has a thickness [1.3 nm, EOT of 1.0 nm] larger than that of the second interface layer [0.9-0.95 nm, EOT of 0.7 nm].*”

5. Limitation [1C]

[1C] <i>each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film</i>

133. As I discussed in §V.B.3.b, the “*first interface layer*” is silicon oxynitride film 24 and the “*second interface layer*” is silicon oxynitride film 22. (See TSMC-1005, 5:14-18.) Torii’s claim 1 further states “each of said first gate insulating film and said second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film.” Thus, Torii discloses that “*each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.*”

C. Claims 12-13

12. <i>The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.</i>

13. <i>The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.</i>
--

134. Torii teaches “*each of the first and second high dielectric constant insulating films contains **hafnium** or zirconium*” as recited in claim 12. As I

discussed in §V.B.3.b, “[o]n each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, **the high-k film such as a hafnia (HfO_2) film 28** of a thickness of about 3.0 nm, which is a high-k film, is formed.” (TSMC-1005, 5:33-36; *see also*, TSMC-1005, 6:66-7:3, 8:14-18.) Torii also lists alternatives for the high-k film: “In the first embodiment, as the high-k film, the metal oxide film, such as **hafnia (HfO_2)**, **hafnium aluminate ($\text{Hf}_x\text{Al}_{1-x}\text{O}_y$)**, alumina (Al_2O_3), lanthanum oxide (La_2O_3), praseodymium oxide (Pr_2O_3), yttrium oxide (Y_2O_3), tantalumoxide (Ta_2O_5), niobiumoxide (Nb_2O_5), titanium oxide (TiO_2), and cerium oxide (CeO_2), or the nitride thereof, or the solid solution thereof, or the solid solution of these metal oxides and SiO_2 ; or the film of a titanate such as strontium barium titanate ($(\text{BaSr})\text{TiO}_3$) may also be used.” (TSMC-1005, 10:9-16.)

135. Torii further teaches “*the first and second high dielectric constant insulating films are equal in thickness*” [13]. Torii discloses that “[o]n each of the silicon oxynitride films 22 and 24”, the high-k film 28 “of a thickness of about 3.0 nm” is formed. (TSMC-1005, 5:33-36.) Torii discloses that the “EOT of the high-k film 28 is about 0.5 nm.” (TSMC-1005, 5:36-37.) Thus, the high-k film in both the LSTP transistor and the LOP transistor are of equal thickness.

136. The processing sequence that I discussed in §V.B.3 confirms the high-k film on both the LOP and LSTP transistors are equal. Torii describes that the

“high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method.” (TSMC-1005, 6:67-7:3.) Specifically, “high-k film 28 is formed on the entire surface of the substrate.” (TSMC-1005, 6:66-67; *See also*, TSMC-1005, Figure 7.) Because the high-k film is formed over both silicon oxynitride films 22 and 24 using ALD, the thickness of the film in both the LSTP and LOP transistors is the same.

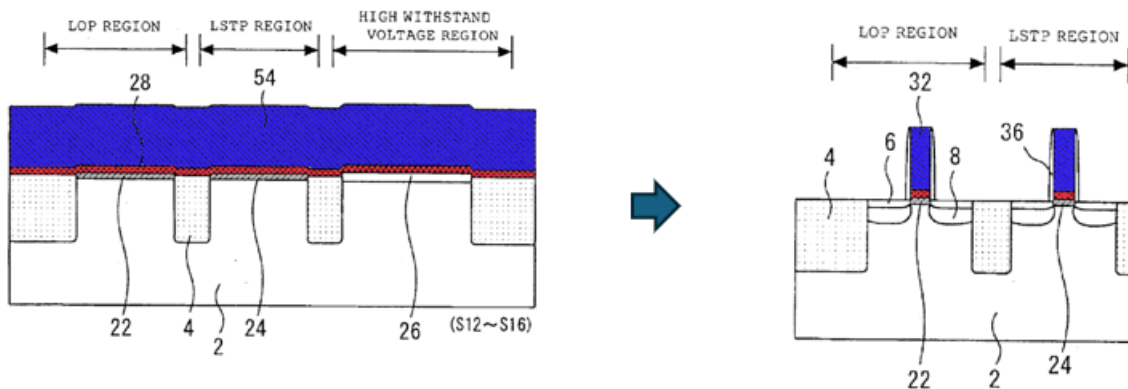
137. Torii explicitly confirms this, stating in the summary of the invention that “high-dielectric-constant film in the first gate insulating film has the same thickness as the high-dielectric-constant film in the second gate insulating film.” (TSMC-1005, 4:6-9.) Issued claim 1 also recites that “the high-dielectric constant film in said first gate insulating film has the same thickness as the high dielectric-constant film in said second gate insulating film.” Thus, Torii teaches that “*the first and second high dielectric constant insulating films are equal in thickness*” [13].

D. Claim 14

14. <i>The semiconductor device of claim 1, wherein the first and second gate electrodes are made of an identical material.</i>

138. Torii teaches that the “*the first and second gate electrodes are made of an identical material*” [14]. During formation of Torii’s device, a “polycrystalline silicon film 54 is formed on the high-k film” as shown in Figure 7 (below-left). (TSMC-1005, 6:66-7:7.) A “resist mask of a width of the gate

electrode is formed on the polycrystalline silicon film 54 using a conventional method, and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width of the gate electrode 32.” (TSMC-1005, 7:13-19.) “Thereby, a **gate electrode 32** and a gate insulating film are **formed in each of the regions for LOP, LSTP**, and high withstand voltage” as shown in Figure 8 (below-right). (TSMC-1005, 7:20-22.) Because the gate electrodes of both the LSTP and LOP transistors are formed from the same polycrystalline silicon film layer, “*the first and second gate electrodes are made of an identical material*”, as recited in claim 14. (See also, §V.B.3.c (discussing gate electrode).)



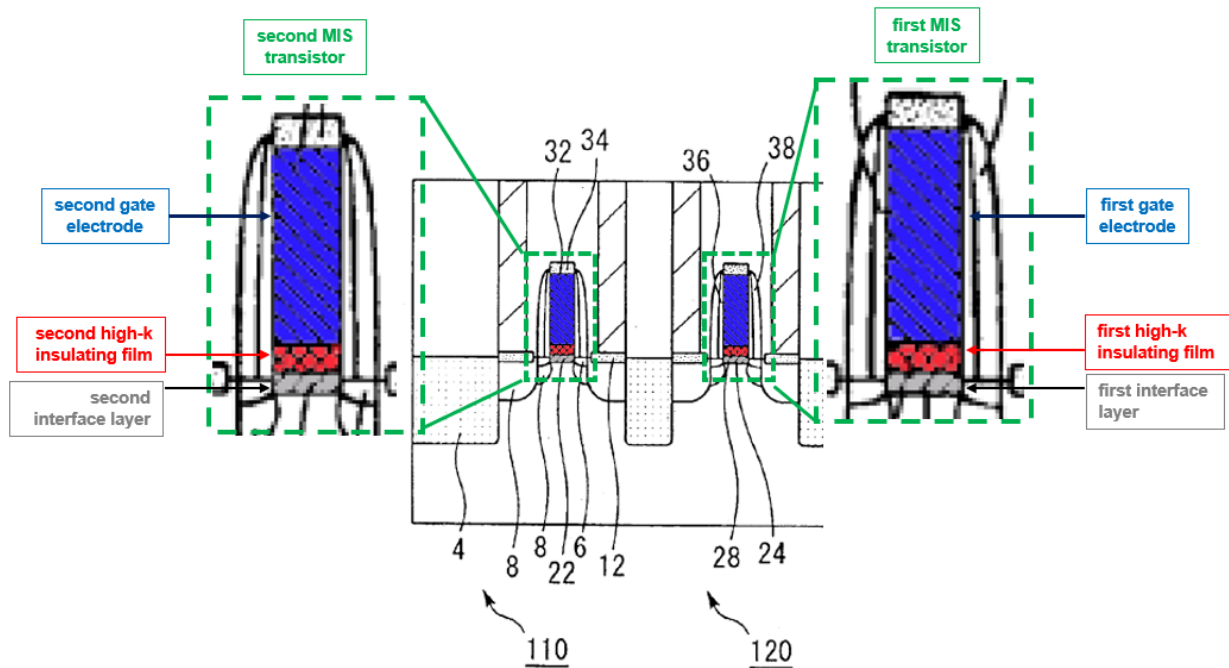
Torii, Figure 7 (left), Excerpt of Figure 8 (right)

E. Claim 15

15. The semiconductor device of claim 1, wherein an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.

139. Torii discloses claim 15. As I discussed in §§III.B-C, the '779 patent teaches that the result of having a greater EOT in a first transistor than in a second transistor which is otherwise identical is a higher effective work function. (TSMC-1001, 4:29-31 (“since an EOT of the gate insulating film of the first MIS transistor increases, an effective work function of the first MIS transistor increases”), 12:47-54 (the first pMIS transistor and the first nMIS transistor, because of the thick interface layers 2A and 2C, show an increase in equivalent oxide thickness and an increase in effective work function”), 13:23-27.) The gate insulating film of Torii’s LSTP transistor has a greater EOT than the gate insulating film of the LOP transistor and therefore the LSTP transistor has a higher effective work function than the LOP transistor, according to the '779 patent’s disclosure.

140. As I discussed in §V.B.2 and illustrate again in Figure 1 below, Torii’s device includes two transistors of the same conductivity type: LSTP transistor (“*first MIS transistor*”) and LOP transistor (“*second MIS transistor*”). And as discussed in §V.D, the gate electrodes of the LSTP and LOP transistors are the same. Further, the LSTP transistor includes silicon oxynitride film 24 and high-k film 28 and the LOP transistor includes silicon oxynitride film 22 and high-k film 28. (TSMC-1005, 5:14-17, 5:33-36, 6:55-7:5.)



Torii, Excerpt from Figure 1 with enlargements

141. Torii teaches that the high-k film of both the LSTP and LOP transistors is formed in the same process step and therefore the high-k film in both has the same thickness and is formed of the same material (i.e., both have the same dielectric constant). (TSMC-1005, 6:66-7:3; §V.C.) Torii explicitly teaches that the EOT of the high-k film in both is “about 0.5 nm.” (TSMC-1005, 5:36-37.) Accordingly, when comparing the EOTs of the gate insulating films of the two transistors as shown in the equation below, the high-k contributions effectively cancel one another, as I indicate in the equation below by greying out these contributions.

EOT (LSTP)

EOT (LOP)

$$\left(\frac{t_{28}}{\epsilon_{28}}\right) \epsilon_{\text{SiO}_2} + \left(\frac{t_{24}}{\epsilon_{24}}\right) \epsilon_{\text{SiO}_2} [1.0 \text{ nm}] > \left(\frac{t_{28}}{\epsilon_{28}}\right) \epsilon_{\text{SiO}_2} + \left(\frac{t_{22}}{\epsilon_{22}}\right) \epsilon_{\text{SiO}_2} [0.7 \text{ nm}]$$

142. The interface layer of both the LSTP and LOP transistors uses the same material (silicon oxynitride) and therefore both have the same dielectric constant (i.e., $\epsilon_{24} = \epsilon_{22}$). Therefore, because the LSTP interface layer (t_{24}) is thicker than the LOP interface layer (t_{22}), the EOT of the LSTP transistor's gate insulating film is greater than the EOT of the LOP transistor's gate insulating film, which is what Torii discloses.

143. Specifically, Torii teaches that the contribution of the silicon oxynitride film 24 to the LSTP transistor's EOT is greater than contribution of the silicon oxynitride film 22 to the LOP transistor's EOT: the “thickness of the silicon oxynitride film 24 [*“first interface layer”*] ... is about 1.3 nm; and the EOT [equivalent oxide thickness] thereof is about 1.0 nm” (TSMC-1005, 5:23-25.) and “the thickness of the silicon oxynitride film 22 [*“second interface layer”*] ... is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm.” (TSMC-1005, 5:20-23.)

144. Because the LSTP transistor (*“first MIS transistor”*) has a greater EOT than the LOP transistor (*“second MIS transistor”*), the *“effective work*

function of the” LSTP transistor (“*first MIS transistor*”) “*is higher than an effective work function of the*” LOP transistor (“*second MIS transistor*”), according to the disclosure of the ’779 patent.

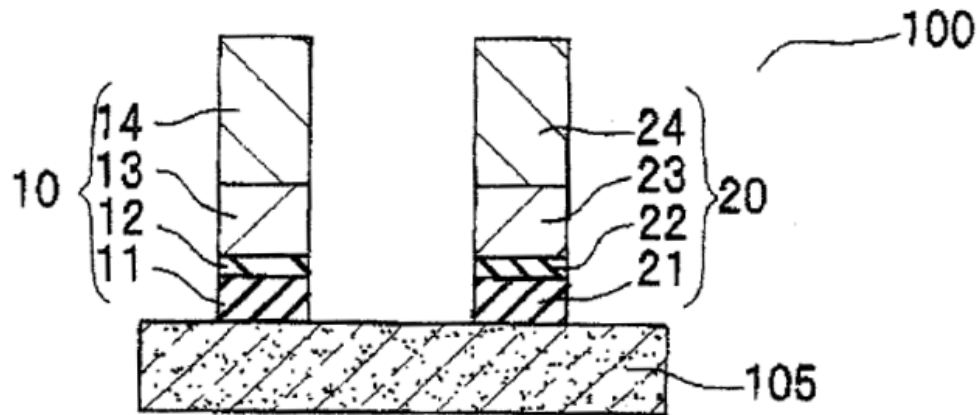
VI. GROUND 2: Combination of Torii and Mise Renders Claims 8-11 Obvious.

145. As I discussed in §V.B.2, Torii discloses that the “*first and second MIS transistors*” of its semiconductor device “*are pMIS transistors*” [8A] or alternatively “*are nMIS transistors*” [10A]. (TSMC-1005, 10:39-42.) Torii however does not explicitly disclose that when “*the first and second MIS transistors are pMIS transistors*” [8A], “*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum, and the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum*” [9]. Torii further does not explicitly discuss that when “*the first and second MIS transistors are nMIS transistors*” [10A], “*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum, and the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum*” [11]. Mise provides these teachings.

A. Mise

146. U.S. Patent Publication 2010/0258878 to Mise, et al. (“Mise”; TSMC-1006) was filed on November 26, 2008 and claims priority to JP Application 2007-312010, filed on December 3, 2007. Both Torii and Mise are in the same field as the ’779 patent “semiconductor devices and methods for fabricating the same.” (TSMC-1001, 1:15-16; TSMC-1005, 1:9-10 (“[t]he present invention relates to a semiconductor device and a method for manufacturing a semiconductor device”); TSMC-1006, ¶1.)

147. Mise relates “to a CMOS semiconductor device using a high-k material for a gate electrode and a method for producing the same.” (TSMC-1006, ¶1.) Figure 1(k) of Mise, illustrated below, “is a cross-sectional view of a CMOS semiconductor device (complementary metal oxide semiconductor device) represented by 100 as a whole according to a first embodiment.” (TSMC-1006, ¶68.) Device 100 includes an n-type MOSFET 101 and a p-type MOSFET 102. (See TSMC-1006, ¶¶68-71, Figure 1 (gate stack 10 corresponds to n-type MOSFET and gate stack 20 corresponds to p-type MOSFET).)



Mise, Figure 1(k)

148. I note that Mise’s specification contains a typographical error. Specifically, Mise states that p-type MOSFET 102 has a p-type well region 120 and n-type MOSFET 101 has a n-type well region 110. (TSMC-1006, ¶70.) A POSITA would have understood that the p-type MOSFET has an n-type well and the n-type MOSFET has a p-type well. (TSMC-1017, 8-9; *see also*, §III.A.1.a.) The correct wells are presented in Figure 11 in Mise.

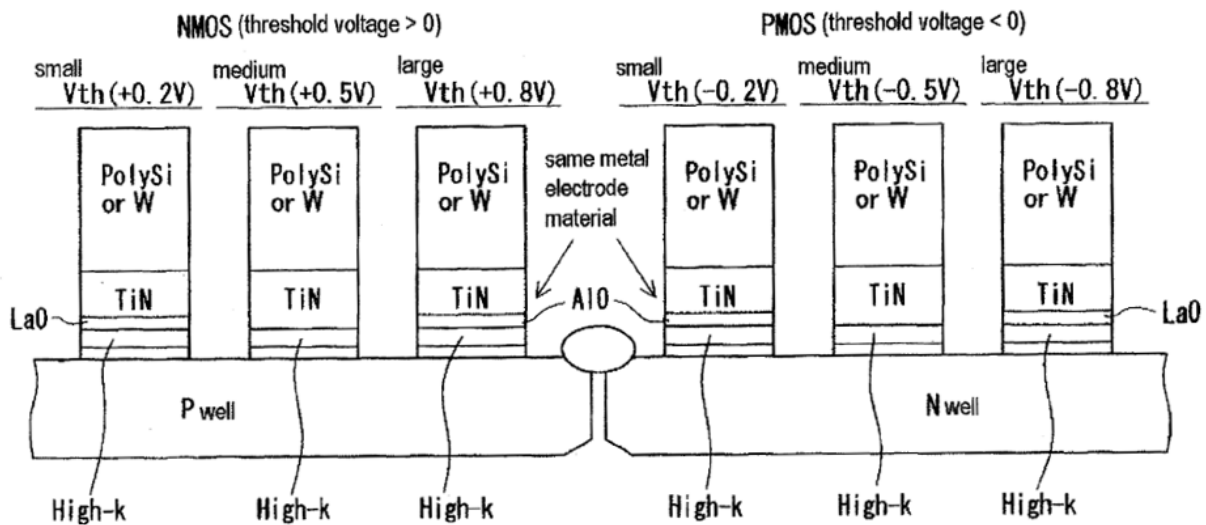
149. Device 100 “includes a semiconductor substrate 105 composed of silicon, for example” with an “n-type well region 110 and a p-type well region 120” provided in the semiconductor substrate 100. (TSMC-1006, ¶70.) Source/drain regions 111 are provided in the n-type well region 110 and “gate electrode 10 is provided on a channel region sandwiched between the source/drain

regions 111.” (TSMC-1006, ¶71.) Gate electrode⁷ 10 includes gate insulation layer 11, cap layer 12, and gate metal layers 13 and 14 provided thereof. (*Id.*) The gate insulation layer includes “high-k material such as HfLaO or HfMgO, and the cap layer 12 is composed of MgO or LaO, for example.” (*Id.*) Gate metal layer 13 “is composed of a mid-gap material having high heat resistance such as TiN, TaN, TaSiN, NiSi, PtSi, or CoSi₂,” and “gate metal layer 14 is made of a low resistance material such as W.” (TSMC-1006, ¶71.) The p-type MOSFET includes gate stack 20 having gate insulation layer 21 “composed of a high-k material such as HfAlO”, cap layer 22 “is composed of AlO”, and gate metal layers 23 and 24 provided thereon.” (TSMC-1006, ¶72.) The gate metal layers “are composed of the same materials as those of the gate metal layers 13 and 14.” (*Id.*)

150. Figure 11, reproduced below, is “a schematic view of a CMOS semiconductor device according to a ninth embodiment.” (TSMC-1006, ¶183.) The “CMOS device includes three kinds of structures” as the gate stacks of the nMOS

⁷ Mise uses the term gate electrode to refer to collection of layers that form the gate stack. In the declaration, I use the term “gate stack” to refer to the collection of layers and the term “gate electrode” to refer to the conductive (e.g., metal) layers of the gate stack, which is consistent with usage in the field.

devices. (TSMC-1006, ¶¶184-187.) Specifically with the nMOS devices, “threshold voltages (V_{th}) are shifted to +0.2V (MOSFET1), +0.5V (MOSFET2), and +0.8V (MOSFET3) as compared with the structure in which the gate insulation layer is only composed of SiO_2 .” (TSMC-1006, ¶188.)



Mise, Figure 11

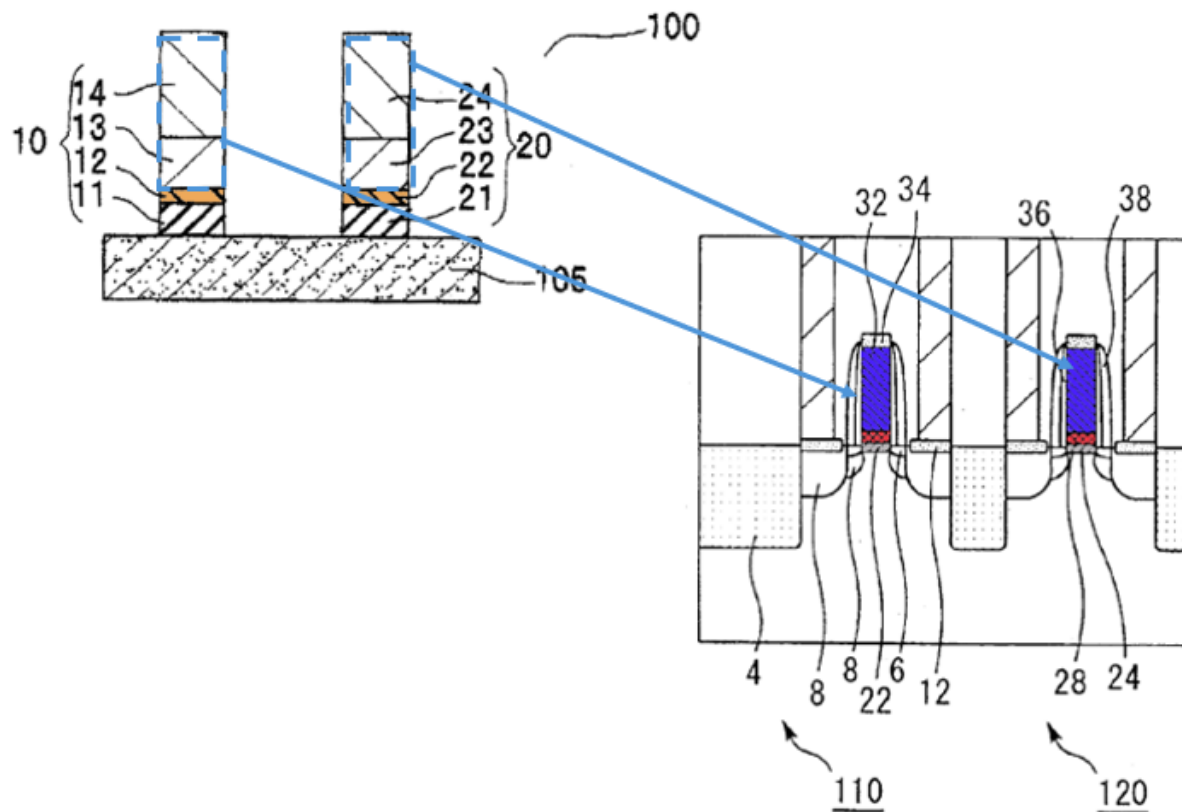
151. The CMOS device also includes “three kinds of structures” as the gate stacks of the pMOS devices. (TSMC-1006, ¶¶189-192.) Specifically with the pMOS devices, “threshold voltages (V_{th}) are shifted to $-0.2V$ (MOSFET1), $-0.5V$ (MOSFET2), and $-0.8V$ (MOSFET3) as compared with the structure in which the gate insulation layer is only composed of SiO_2 .” (TSMC-1006, ¶193.)

B. Motivation to Combine

152. A POSITA would have motivated to make at least the following two combinations with Torii's device based on the teachings of Mise. I address each and their specific motivations below.

1. Combining Mise's teaching of a two-layer metal gate electrode with Torii.

153. A POSITA would have been motivated to integrate Mise's teaching of using a two-layer metal gate electrode in the transistors of Torii, as illustrated in the below figure.



Mise, Figure 1 (top-left); Torii, Figure 1 (top-right)

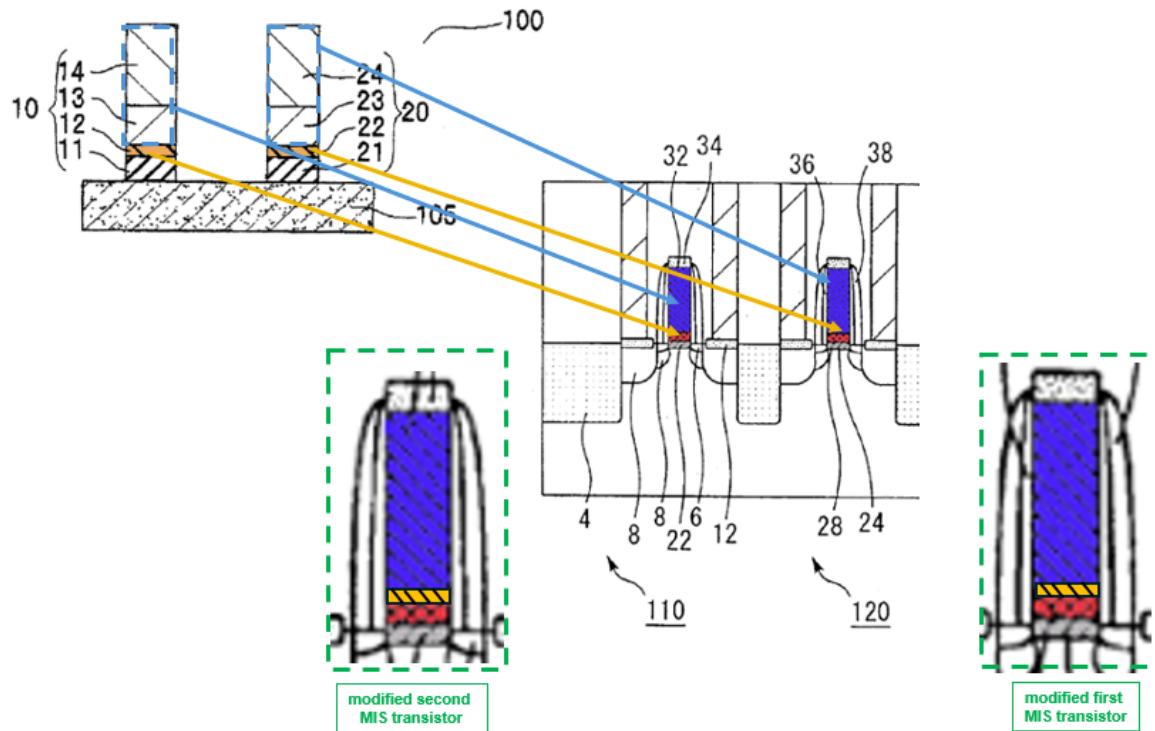
154. The LSTP and LOP transistors of Torii include a “*gate insulating film*” having a “*high dielectric constant insulating film*” and also include a polysilicon “*gate electrode*” on the high-k film. (See TSMC-1005, 5:33-36, 5:42, 6:66-7:15; §V.B.3.) A POSITA would have been motivated to make the above combination because the challenges with using high-k dielectrics with polySi gates were known prior to the ’779 patent. For example, high-k dielectrics and polySi have an issue with compatibility due to Fermi level pinning at their interface which causes threshold voltage shifts. (TSMC-1006, ¶23 (“In addition, when the high-k material is used for a gate electrode, Fermi level pinning is generated at a boundary with a silicon gate electrode, so that as a gate electrode material, a metal such as nickel silicide is used instead of polycrystalline silicon”); TSMC-1018, 1.) Polysilicon/high-k transistors also exhibit degraded channel mobility. (See TSMC-1018, 1.) A POSITA would have understood that metal gates are more effective with high-k gate dielectrics but require additional adjustment to achieve an optimal threshold voltage, which is a motivation to use Mise’s cap layer, as I discuss in the next section. (See TSMC-1018, 1.) A POSITA would have therefore been motivated to improve Torii’s device using the metal gate electrodes discussed by Mise to avoid Fermi level pinning and improve channel mobility.

155. Using metal gate layers in Torii's transistors would be nothing more than using a known technique (e.g., using metal gate layers according to Mise's teachings) to improve similar devices in the same way. I describe the motivation for doing so above. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. Mise describes that its metal layers are formed "by the sputtering method." (TSMC-1006, ¶¶80, 85, 94.) A POSITA would know that sputtering was a conventional and well known deposition method in semiconductor fabrication prior to the '779 patent. (See, e.g., TSMC-1017, 335) Further, the metal gate layers of Mise serve the same purpose in Torii's transistors as they do in Mise's similar transistors. Thus, results of the combination would have been predictable to a POSITA and would improve similar semiconductor devices in the same way (improve reliability and reduce leakage current) because the principles of operation of the semiconductor device would remain unchanged.

2. Combining Mise's teaching of a cap layer with Torii.

156. A POSITA would also have motivated to apply Mise's teaching regarding use of a cap layer on a high-k film, as taught by Mise to the LSTP and LOP transistors of Torii using Mise's gate stack, as illustrated in the figure below. Specifically, a POSITA would have been motivated to integrate a cap layer over

the high-k dielectric in Torii's gate insulating stack, as taught by Mise and to include an Al containing cap layer in Torii's p-type MISFETs, and a La containing cap layer in Torii's n-type MISFETs. I provide the motivation for each below.



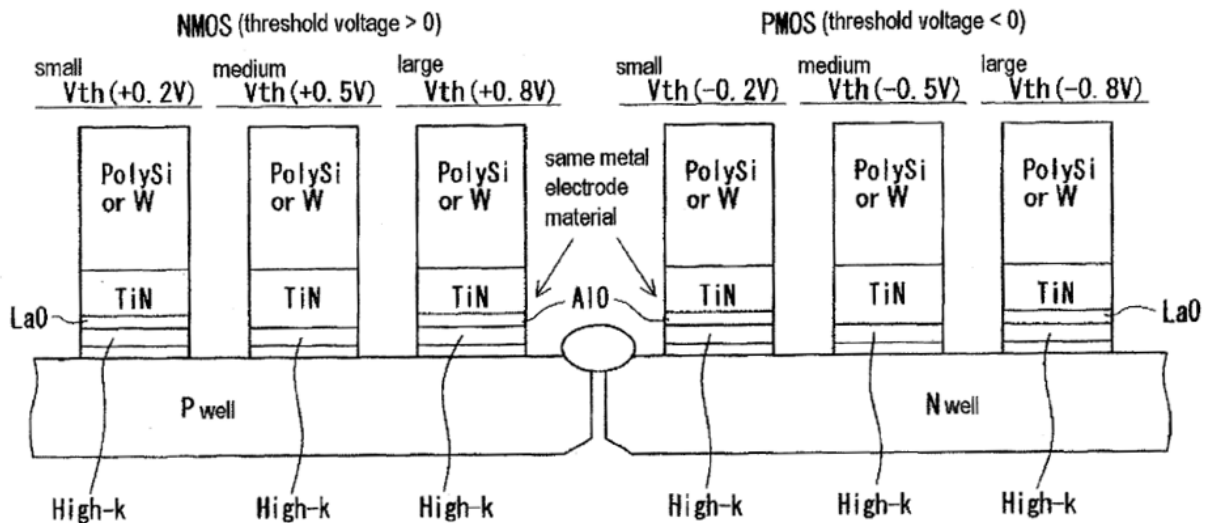
**Mise, Figure 1 (top-left); Torii, Figure 1 (top-right)
enlargements showing transistors of combination of Torii and Mise**

157. A POSITA would have been motivated to apply a cap layer to the high-k dielectric of Torii's LSTP and LOP transistors as discussed above to improve operation of the transistors. A POSITA would have understood that the cap layer helps reduce defects that negatively impact electrical performance when metal gate electrodes are used. For example, use of a cap layer helps reduce

leakage current by misaligning “the grain boundaries within the layers.” (*See* TSMC-1009, 5:21-24.) A POSITA would have also understood the cap layer improves the interface between a metal gate electrode and the gate insulating film. For example, the high-k film may not be compatible with the metal gate electrode. (*See* TSMC-1009, 5:25-31.) The cap layer alleviates these compatibility concerns and helps adjust the threshold voltage to an appropriate range, as I explain further below. (TSMC-1009, 5:31-35.)

158. Mise’s gate metal layer 13 “is composed of a mid-gap material having high heat resistance such as TiN, TaN, TaSiN, NiSi, PtSi, or CoSi₂,” and “gate metal layer 14 is made of a low resistance material such as W.” (TSMC-1006, ¶71; ¶72 (“gate metal layers 23 and 24 are composed of the same materials as those of the gate metal layers 13 and 14”).) A POSITA would have been motivated to include aluminum in the cap layer of the pMIS transistors in the combined device using Mise’s gate electrode to adjust the threshold voltage of the transistor. Mise suggests the combination, showing in Figure 11 that the appropriate absolute threshold voltage value (of ~0.2V) is for a pMOS device using aluminum in the cap layer. (*See*, TSMC-1006, Figure 11.) A POSITA would have understood that the absolute (threshold voltage) value of 0.5V and 0.8V of the other two pMOS transistors is too high for modern CMOS technology. The paper, “Dual High-k

Gate Dielectric With Poly Gate Electrode: HfSiON on nMOS and Al₂O₃ Capping Layer on pMOS” by Li and Gardner (“Li/Gardner”) also proposes the use of an Al₂O₃ cap layer on top of HfSiON to adjust the threshold voltage of a pMOS device. (See TSMC-1020, 441-444.) Similarly, U.S. Patent 7,807,990 to Koyama, et al. (“Koyama”) “made an intensive study on the mechanism of lowering the threshold voltage V_{th} of a p-channel MIS transistor by adding an Al-based insulating film to the interface between a gate electrode and an insulating film made of a high-k material (the interface being hereinafter referred to as the upper interface), which was reported in a document of a conventional technique.” (See TSMC-1021, 6:25-46.)

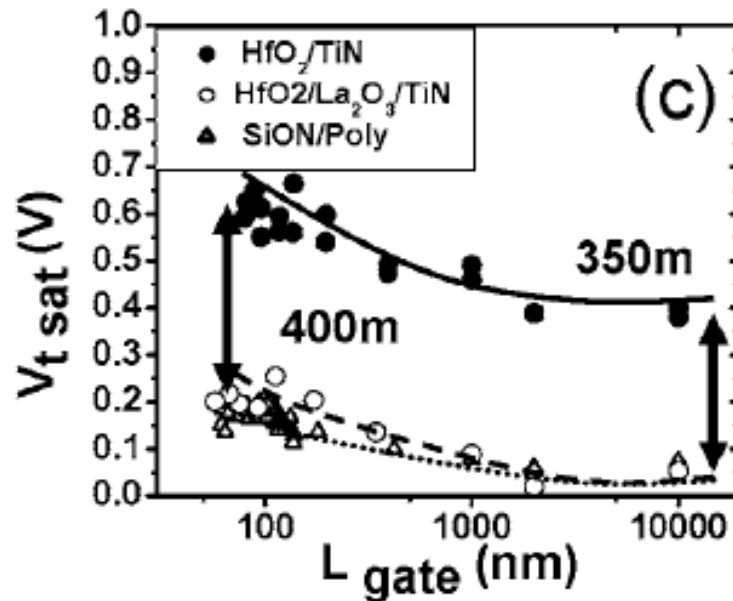


Mise, Figure 11

159. A POSITA would have also been motivated to include lanthanum in the cap layer of the nMIS transistors of the combined device. Mise’s gate metal

layer 13 “is composed of a mid-gap material having high heat resistance such as TiN, TaN, TaSiN, NiSi, PtSi, or CoSi₂,” and “gate metal layer 14 is made of a low resistance material such as W.” (TSMC-1006, ¶71.) These mid-gap materials result in a threshold voltage which is too high for nMIS devices. (*See* TSMC-1019, 1 (noting that the “resulting threshold voltages” for a HfO₂ dielectric and TiN electrode “are unacceptably high and an additional threshold adjustment technique is needed to produce devices suitable for high performance logic applications”).) A POSITA would have therefore been motivated to use a cap layer material that appropriately adjusts the threshold voltage of the nMIS transistor. Specifically, a cap layer having lanthanum oxide adjusts the threshold voltage to a value suitable for nMIS devices. (*See*, TSMC-1019, 1 (“We have recently solved this problem and shown that by introducing ultrathin La₂O₃ cap layers between the HfO₂ dielectric and TiN electrode, the threshold voltage can be controllably shifted to a position ideal for nMOSFETs”).) For example, from Mise’s Figure 11 above, a POSITA would have understood the appropriate threshold voltage value (of ~0.2V) is for an nMOS device using lanthanum in the cap layer. (*See*, TSMC-1006, Figure 11.) A POSITA would have understood that the (threshold voltage) value of 0.5V and 0.8V for the other nMOS transistors is too high for modern CMOS technology.

160. Figure 1(c) from the paper “Examination of flatband and threshold voltage tuning of HfO₂/TiN field effect transistors by dielectric cap layers” to Guha, et al (“Guha”; TSMC-1019) highlights and confirms the motivation for using lanthanum in the capping layer of the nMIS transistor of the combination of Torii and Mise. For example, Guha explains that a TiN gate electrode layer by itself on a high-k dielectric (i.e., without an intervening cap layer) will result in a threshold voltage of 0.6V at 100 nm gate length. (*See, e.g.*, TSMC-1019, 2 and Figure 1(c).) A POSITA would have understood that this threshold voltage is too high for an nMIS device, as explained by Guha. The traditional nMOS device with SiON and poly-silicon gate is shown in the bottom curve. (*Id.*) The traditional device has a threshold voltage of 0.2V at 100 nm length. (*Id.*) The HfO₂-La₂O₃-TiN device has a threshold voltage close to the traditional device at 0.25V at 100 nm gate length which is close to that of the traditional device. (*Id.*) Therefore, a POSITA would have understood that the device with lanthanum in the capping layer shifted the threshold voltage to near the ideal for an nMOS transistor. This disclosure would have confirmed to a POSITA the motivation to select La₂O₃ as the capping layer and the likelihood of success in the combination.



Guha, Figure 1(c)

161. A POSITA would have further been motivated to make the combination (selections) above to adjust the threshold voltages and improve the operation of the pMIS and nMIS devices. It was known, prior to the '779 patent, that MOSFETs “fabricated with a hafnium-based dielectric as the gate dielectric suffer from a non-ideal voltage.” (TSMC-1022, ¶4.) It was further well-known that one of the primary purposes of a cap layer, such as disclosed in Mise, is to ensure optimal threshold voltage. Indeed, the admitted prior art in the '779 patent acknowledges this primary purpose of a cap layer. (See, TSMC-1001, 2:24-27.) Mise also recognizes this purpose, disclosing use of an AlO, LaO cap layer for the pMOS, nMOS respectively as threshold voltage adjustment. (See, e.g., TSMC-1006, ¶¶154, 183-193, 195.)

162. Adding cap in Torii's transistors would be nothing more than using a known technique (e.g., incorporating cap layers between the high-k dielectric and the gate electrode material) to improve similar devices in the same way. I describe the motivations for doing so above. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. Mise describes that its cap layers are "made by the ALD method, the MOCVD method, the sputtering method, or the like." (TSMC-1006, ¶¶80, 85, 94.) A POSITA would know that ALD (atomic layer deposition), MOCVD (metal-organic chemical vapor deposition), and sputtering were conventional and well known deposition methods in semiconductor fabrication prior to the '779 patent. (*See, e.g.*, TSMC-1017, 335, 380, 409.) Further, each element in the prior art, in a combination of Torii and Mise, merely performs the same function that it does separately. In particular, the cap layers of Mise serve the same purpose in Torii's transistors as they do in Mise's similar transistors.

C. PMIS Claims 8-9

8. *The semiconductor device of claim 1, wherein*
 [8A] *the first and second MIS transistors are pMIS transistors, and*
 [8B] *the first and second high dielectric constant insulating films*
contain aluminum.

9. *The semiconductor device of claim 8, wherein*
 [9A] *the first gate insulating film further includes a first cap film*
formed on the first high dielectric constant insulating film and
containing aluminum, and
 [9B] *the second gate insulating film further includes a second cap*
film formed on the second high dielectric constant insulating film and
containing aluminum.

163. Torii teaches that “*first and second MIS transistors are pMIS transistors*” [8A]: “the present invention may be applied to the case wherein a p-type transistor is formed.” (TSMC-1005, 10:40-42; §V.B.2.)

164. The combination of Torii and Mise uses a cap layer containing aluminum on the high-k insulating film in Torii’s LSTP and LOP pMIS transistors, as taught by Mise. (§VI.B.) Mise teaches the cap layer 22 of the gate insulation film of the pMOS transistor “is composed of AlO.” (TSMC-1006, ¶72.) A POSITA would have been motivated to use a cap layer containing aluminum in both the LSTP and LOP transistors (“*first and second MIS transistors*”) for the reasons I discussed above. Thus, the combination provides that “*the first gate insulating film*

further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum” [9A] and “the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum” [9B].

165. Torii further teaches that the material for the high-k gate insulating film in its transistor includes hafnium aluminate ($\text{Hf}_x\text{Al}_{1-x}\text{O}_y$) and alumina (Al_2O_3). (TSMC-1005, 10:8-16.) Mise similarly teaches that gate insulation film of the pMOS transistor “is composed of a high-k material such as **HfAlO**.” (TSMC-1006, ¶72.)

166. A POSITA would have also understood the high-k material in the combination contains aluminum, as taught by Torii and Mise, at least because of aluminum diffusion from the overlaying aluminum containing cap layer due to subsequent thermal processing. Specifically, after the gate electrode is formed, source-drain region 10 “is formed in each region for LOP, LSTP, and high withstand voltage” by implanting ions “using the gate electrode 32, sidewall spacers 38 and the like of each region as masks.” (TSMC-1005, 7:54-57.) A heat treatment is then performed “at about 1050° C.” (TSMC-1005, 7:57-58.) Torii further describe formation of nickel silicide layers 12 and 14 using “heat treatment.” (TSMC-1005, 7:63-66.) Koyama describes Al diffusion in its gate

stack due to heat treatments at different temperatures (e.g., 800° C and 1000° C). (TSMC-1021, 11:1-26; *see also*, TSMC-1021, 6:25-37.) For example, U.S. Patent Publication 2006/0244035 to Bojarczuk (“Bojarczuk”) describes diffusion of rare earth metals through the gate insulating layers of the gate stack. (*See, e.g.*, TSMC-1022, ¶19.) A POSITA would have understood similar diffusion occurs with Al.

167. Thus, in the combination of Torii and Mise, the “*the first and second MIS transistors are pMIS transistors*” [8A] and the “*high dielectric constant insulating films*” of both the LSTP transistor and the LOP transistor “*contain aluminum*” [8B].

168. For the reasons discussed above, the combination further discloses that “*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum*” [9A] and “*the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum*” [9B].

D. NMIS Claims 10-11

169. Torii teaches that “*first and second MIS transistors are nMIS transistors*” [10A]: the LOP transistor and LSTP transistor are “n-type transistor[s].” (TSMC-1005, 10:39-40; §V.B.2.)

170. The combination of Torii and Mise uses a cap layer containing lanthanum on the high-k insulating film in the LSTP and LOP nMIS transistors of Torii, as taught by Mise. (§VI.B.) Mise teaches the cap layer 22 of the gate insulation film of the nMOS transistor “is composed of MgO or LaO.” (TSMC-1006, ¶71.) A POSITA would have been motivated to use a cap layer containing lanthanum in both the LSTP and LOP transistors (“*first and second MIS transistors*”) for the reasons I discussed above. Thus, in the combination of Torii and Mise, “*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum*” [11A] and “*the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum*” [11B].

171. Regarding the high-k film, Torii teaches the high-k film in its transistors includes lanthanum oxide. (TSMC-1005, 10:8-16.) Mise teaches the gate insulation film of its nMOS transistor “is composed of a high-k material such as **HfLaO** or HfMgO.” (TSMC-1006, ¶71.) A POSITA would have also understood that the high-k material in the combination contains lanthanum, as taught by Torii and Mise, at least because of lanthanum diffusion from the overlaying lanthanum containing cap layer due to subsequent thermal processing

performed during the fabrication process discussed above. (*See, e.g.*, TSMC-1005, 7:54-58, 7:63-66; *see also*, TSMC-1022, ¶19 (mentioning diffusion of metal atoms across the gate stack); §VI.C.)

172. Thus, in the combination of Torii and Mise, the “*first and second MIS transistors are nMIS transistors*” [10A] and the “*high dielectric constant insulating films*” of both the LSTP transistor and the LOP transistor “*contain lanthanum*” [10B].

VII. GROUND 3: Combination of Torii and Yu Renders Claim 15 Obvious.

173. While Torii discloses claim 15 in the same manner disclosed in the ’779 patent, Torii does not disclose modifying the work function of a metal gate electrode to adjust the gate effective work function (and threshold voltage) of the transistor. (*See IV.*) U.S. Patent 6,693,333 to Yu, et al. (“Yu”; TSMC-1008) discloses such metal work function engineering. Yu issued on February 17, 2004 from an application filed on May 1, 2001, over a decade before the ’779 patent.

174. Yu generally relates “to an integrated circuit (IC) and the fabrication of an integrated circuit” which is a semiconductor device. (TSMC-1008, 1:27-28, 1:35-40 (describing that an IC includes “transistors”), 1:62-63 (referring to CMOS technology).) Yu is therefore in the same field as Torii and the ’779 patent. (TSMC-1001, 1:15-16; TSMC-1005, 1:9-10 (“[t]he present invention relates to a

semiconductor device and a method for manufacturing a semiconductor device”),
TSMC-1008, 1:27-28.)

A. Combination of Torii and Yu

1. Yu

175. Yu “relates to an integrated circuit with transistors having multiple threshold voltage values.” (TSMC-1008, 1:28-31.)

a. Yu’s Background

176. Yu explains that ultra-large-scale integrated (ULSI) “circuits generally include a multitude of transistors, such as, more than one million transistors and even several million or more transistors, that cooperate to perform various functions of an electronic component.” (TSMC-1008, 1:35-39.) “Some transistors perform functions for circuits in the critical signal path of the IC, where speed is crucial to the proper operation of the IC.” (TSMC-1008, 1:42-44.) Other transistors “perform functions for circuits in the noncritical signal path of the IC, where speed is not as important.” (TSMC-1008, 1:44-46.) These noncritical signal path transistors “are preferably designed to consume less power than transistors in the critical signal path.” (TSMC-1008, 1:46-48.) Still other transistors “perform functions for a signal path having a criticality somewhere between the critical signal path and non-critical signal path and, accordingly, have different speed and power consumption requirements.” (TSMC-1008, 1:-52.)

177. In general, “transistors which have higher threshold voltages (V_{th}) consume less power than transistors which have low threshold voltages due to smaller off-state current leakage.” (TSMC-1008, 1:53-56.) “Transistors which have lower threshold voltages are faster (e.g., have quicker switching speeds) than transistors which have higher threshold voltages.” (TSMC-1008, 1:58-61.) In ULSI circuits, transistors “with low threshold voltages can be used in logic paths which have high speed requirements.” (TSMC-1008, 3:1-3.) In contrast, transistors “with higher threshold voltages can be used in the non-critical signal path (e.g., storage devices), thereby reducing the off-state leakage current and, hence, reducing the standby power consumption of the entire IC.” (TSMC-1008, 3:3-7.) The above description from Yu is consistent with a POSITA’s common knowledge of the art, as I discussed above in §III.A.3 with regards to HP, LSTP, and LOP transistors in integrated circuits (ICs). For example, the ITRS explains “more than one type of transistor” is fabricated on the chip including “the high-performance, low V_t device” as well as other transistors “with higher V_t and sometimes larger EOT to reduce the leakage current.” (TSMC-1016, 7.) ITRS further explains “lower leakage devices will have lower saturation drive current and hence poorer device performance” than “the high-performance devices.” (TSMC-1016, 7.) The “high-

performance device is used just in critical paths, and the low leakage devices are used everywhere else.” (TSMC-1016, 7.)

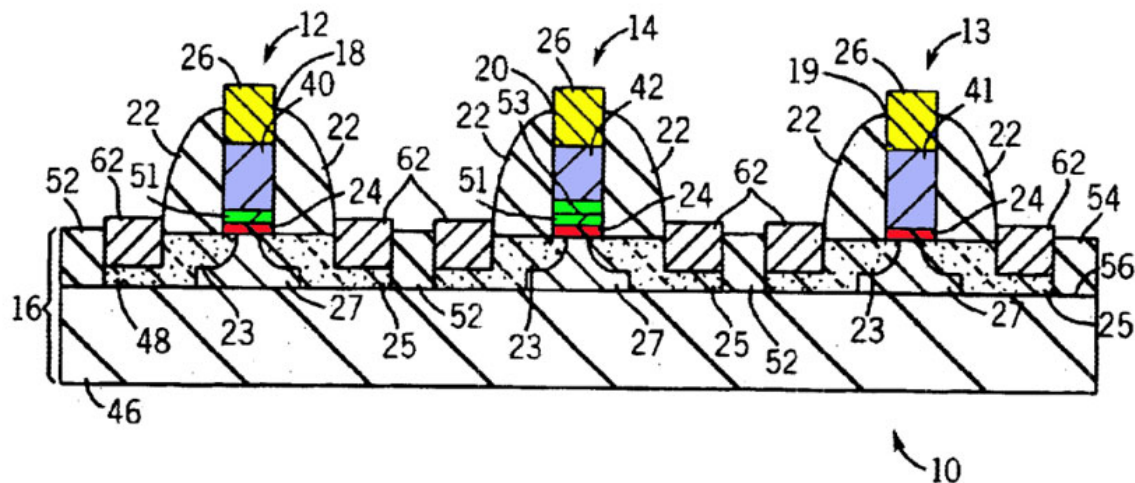
178. Yu notes that in conventional designs “multiple threshold voltages for transistors on a single IC are obtained by selectively providing channel implants for the transistors.” (TSMC-1008, 3:16-18.) And additional “channel implants (e.g., doping the channel region to change the work function difference between the gate and the channel) are used for those transistors with higher threshold voltage requirements (e.g., $V_{th} > 0.3V$).” (TSMC-1008, 3:20-23.) The transistors with the “lower voltage threshold requirements (e.g., $V_{th} \leq 0.2V-0.3V$) do not receive the additional channel implants.” (TSMC-1008, 3:22-25.) However, Yu explains that “[u]tilizing channel implants to adjust the threshold voltages of transistors can be problematic because transistor short-channel performance is very susceptible to process variations.” (TSMC-1008, 3:27-30.) “This characteristic is particularly problematic as transistors become smaller and packing densities increase.” (TSMC-1008, 3:35-37.)

179. Yu therefore provides “an ULSI circuit that does not utilize channel implants to adjust threshold voltages among transistors” and “a process for fabricating transistors having multiple threshold voltages that is higher in density and can be more efficiently manufacture.” (TSMC-1008, 3:64-4:2.) Yu’s

disclosure and teachings are therefore consistent with the general direction of the semiconductor industry, as documented by the ITRS in 2007 (TSMC-1016).

b. Yu's Multiple Threshold Voltages

180. Yu's integrated circuit, illustrated in part in Figure 1 below, includes transistor 12, transistor 13, and transistor 14. (TSMC-1008, 5:4-6.) Each transistor includes a drain 23, source 25, and channel 27. "Transistors 12, 13, and 14 have a threshold voltage between 0.15V and 0.4V or less." (TSMC-1008, 5:16-17.)



Yu, Figure 1

181. The gate stack 18 of transistor 12 includes gate dielectric 24 (shaded red), metal layer 51 (shaded green), gate conductor 40 (shaded blue), and silicide layer 26 (shaded yellow).

182. The gate stack 20 of transistor 14 includes gate dielectric 24 (shaded red), metal layer 51 (shaded green), metal layer 53 (shaded green), gate conductor 42 (shaded blue), and silicide layer 26 (shaded yellow).

183. The gate stack of transistor 13 includes gate dielectric 24 (shaded red), gate conductor 41 (shaded blue), and silicide layer 26 (shaded yellow)

184. Each transistor is “disposed on a substrate 16” separated by isolation structures 52. (TSMC-1008, 5:10-11, 6:56-63.) Although Yu teaches that substrate 16 “provides an SOI substrate,” Yu teaches that transistors 12, 13, and 14 could “utilize the principles of the present invention on a bulk-type substrate.” (TSMC-1008, 6:65-67.) The gate dielectric 24 of each transistor is a layer of silicon dioxide or alternatively “can be a silicon nitride (Si_3N_4) material or other insulative material.” (TSMC-1008, 5:26-29.)

185. The work function of each gate stack 18, 19 and 20 “is locally controlled by the presence of layers 51 and 53.” (TSMC-1008, 5:50-51.) Metal layer 51 of gate stacks 18 and 20 and metal layer 53 of gate stack 20 “are preferably very thin (ultra-thin layers such as 10-30 Å thick metal layers).” (TSMC-1008, 5:55-56.) By inserting layer 51 in gate stack 18 and layers 51 and 53 in gate stack 20, “the threshold voltages can be adjusted.” (TSMC-1008, 5:51-53.) Specifically, the “band structure of gate structures 18 and 19 is interfered by layers

51 and 53, thereby providing a different work function than gate structure 13” which does not include the metal layers. (TSMC-1008, 5:61-63.) Accordingly, the “presence of layers 51 and 53 adjusts the work function associated with the material of conductors 40, 41, and 42 (e.g., polysilicon).” (TSMC-1008, 5:63-65, *see also*, TSMC-1008, 5:65-67.)

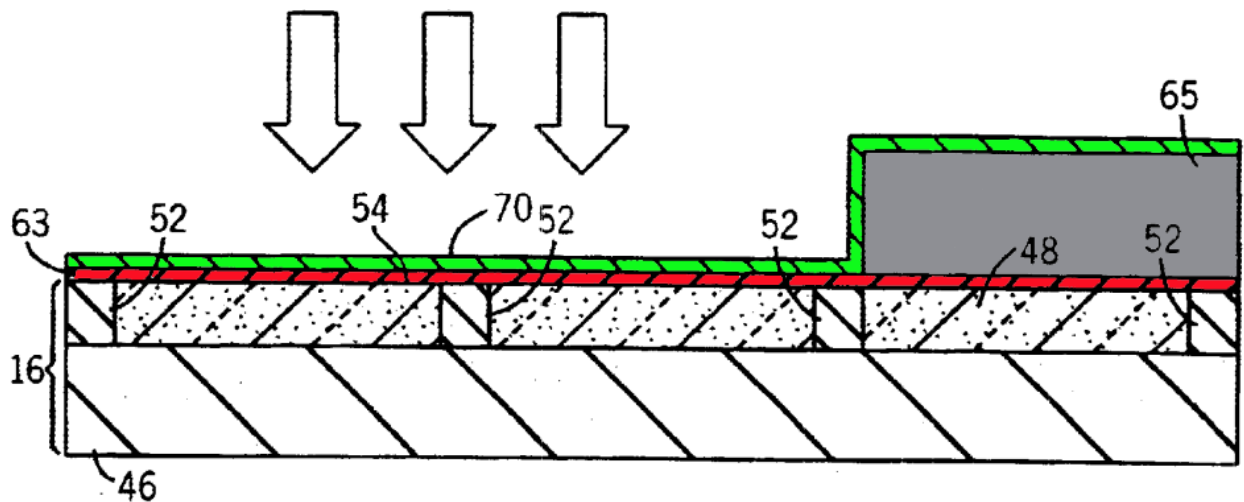
186. The thickness and types of materials for layers 51 and 53 used in the gate stacks “can be controlled to control the adjustment to the work function, thereby selecting threshold voltage.” (TSMC-1008, 6:1-3.) “Therefore, by using two metal layers, at least three different transistors (transistors 12, 13, and 14) having three different threshold voltages can be formed.” (TSMC-1008, 6:3-6.)

187. In the portion of the IC shown in Figure 1, “[i]f transistors 12 and 14 are N-channel transistors, transistor 12 has a lower threshold voltage than transistor 14.” (TSMC-1008, 6:25-26.) For example, transistor 12 “has a threshold voltage of approximately 0.2V” and transistor 14 “has a threshold voltage of approximately 0.32V.” (TSMC-1008, 6:36-38.)

188. Yu describes the fabrication of its multiple threshold voltage IC. As shown in Figure 2 below, dielectric layer 63, corresponding to gate dielectric 24, “is provided on top surface of layer 48.” (TSMC-1008, 7:11-14.) Mask 65 (shaded grey) “cover[s] the entire active region associated with transistor 13.” (TSMC-

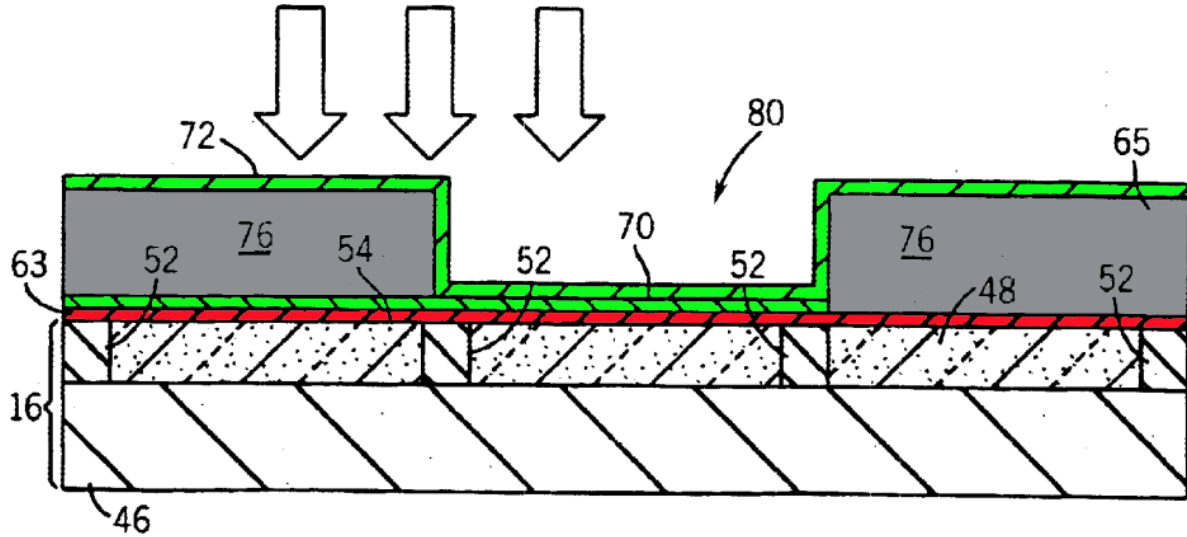
1008, 7:19-22.) Metal layer 70, corresponding to layer 51 of gate stacks 18 and 20, “is deposited above gate dielectric layer 63 and above photoresist layer 65.”

(TSMC-1008, 7:23-25.)



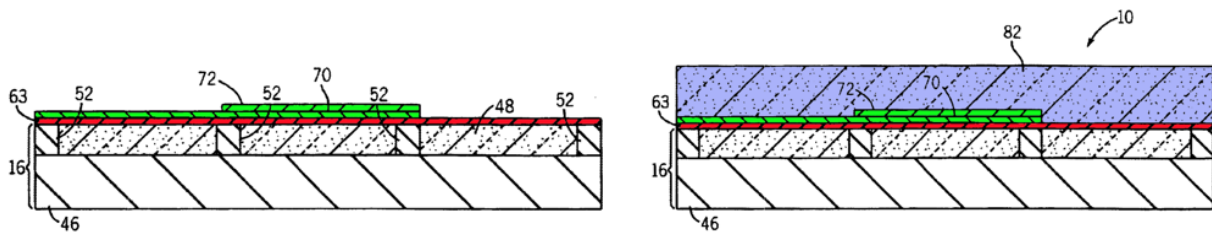
Yu, Figure 2

189. Mask layer 65 is then removed, “thereby removing layer 70 above layer 65.” (TSMC-1008, 7:41-42.) As shown in Figure 3 below, a mask layer 76 (shaded grey) “is provided above layer 70” and above the active region for transistor 13. (TSMC-1008, 7:47-48.) Metal layer 72, corresponding to layer 53, is then “deposited over layer 76 and over layer 70.” (TSMC-1008, 7:58-59.) “Layer 72 preferably has a different work function associated with it than layer 70.” (TSMC-1008, 7:63-64.)



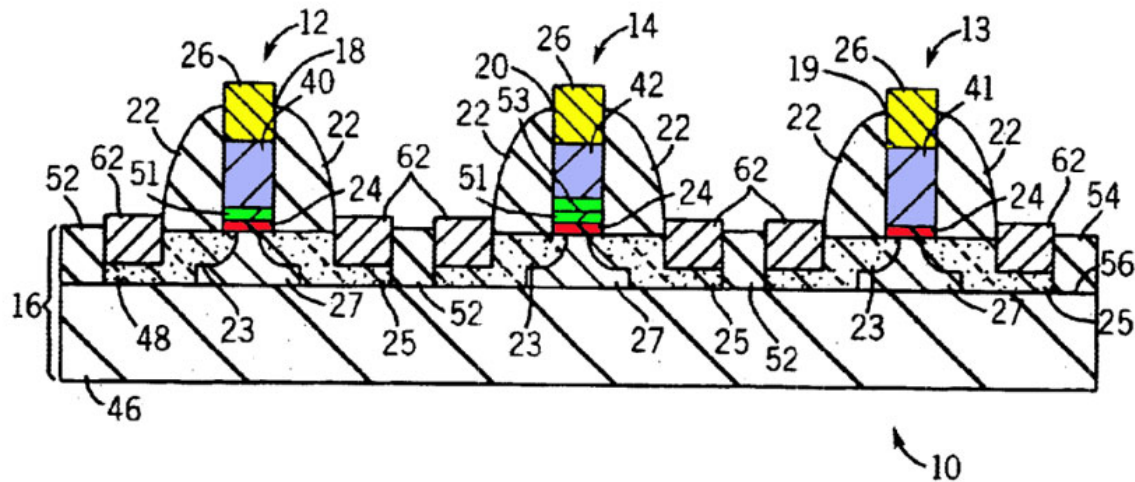
Yu, Figure 3

190. After “patterning layer 76, layer 76 is removed” which “removes layer 72 above the gate area for transistor 12 and transistor 13.” (TSMC-1008, 8:1-4, Figure 4 (below-left).) Layer 72 then “remains above the gate area associated with transistor 14.” (TSMC-1008, 8:4-6.) A semiconductor material layer 82, corresponding to gate conductor 40, 41, and 42 of transistors 12, 13, and 14 respectively, “is deposited above layer 63 (transistor 13), layer 72 (transistor 14), and layer 70 (transistor 12).” (TSMC-1008, 8:6-10, Figure 5 (below-right).)



Yu, Figure 4 (right), Figure 5 (left)

191. Layers 82, 70 and 63 “are selectively etched in accordance with a conventional process to form gate structures 18, 19, and 20” shown in Figure 1 which I reproduce again below. (TSMC-1008, 8:23-25.)



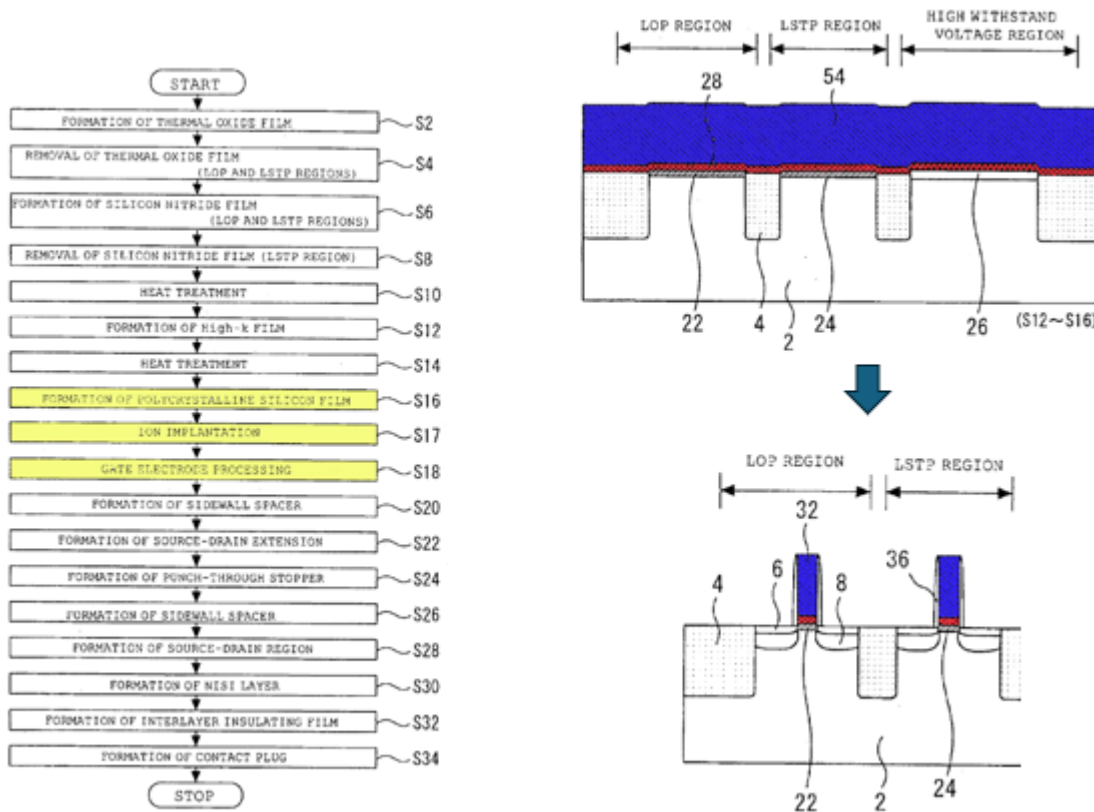
Yu, Figure 1

B. Claim 15

192. The combination of Torii and Yu discloses or at least suggests “*an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.*”

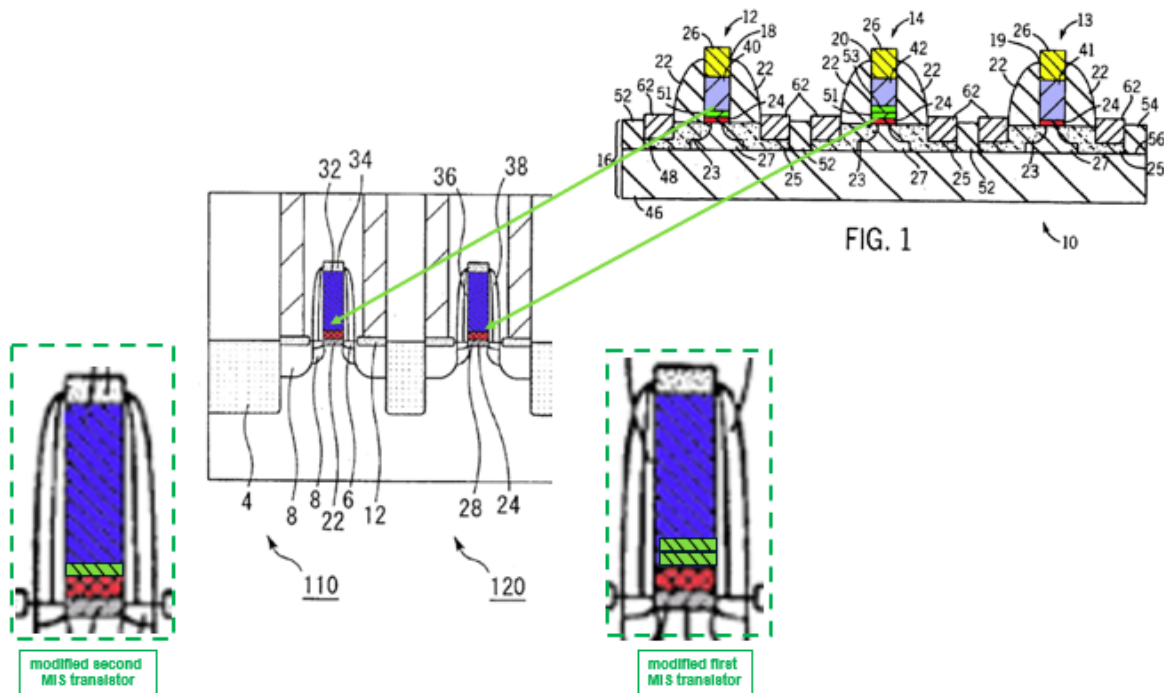
193. As I discussed in §§V.B.2, VI.D, Torii teaches that the LSTP and LOP transistors are nMIS transistors. (*See*, Torii, 10:39-40.) And as I discussed in §V.B.3.c, to form the gate electrode in Torii, a non-doped polycrystalline silicon film 54, “a material film for gate electrodes”, “is formed on the high-k film 28” in Step S16, as shown in Figure 7 (right-top). (TSMC-1005, 7:6-9.) “Thereafter,

impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54” in Step S17. (TSMC-1005, 7:9-12.) The “polycrystalline silicon film 54 is processed for a gate electrode 32 of each region” in Step S18, illustrated in the excerpt from Figure 8 (right-bottom). That is, Torii’s transistors use doped polysilicon for the gate electrode.



**Torii, Figure 2 (left), Figure 7 (right-top),
Excerpt from Figure 8 (right-bottom)**

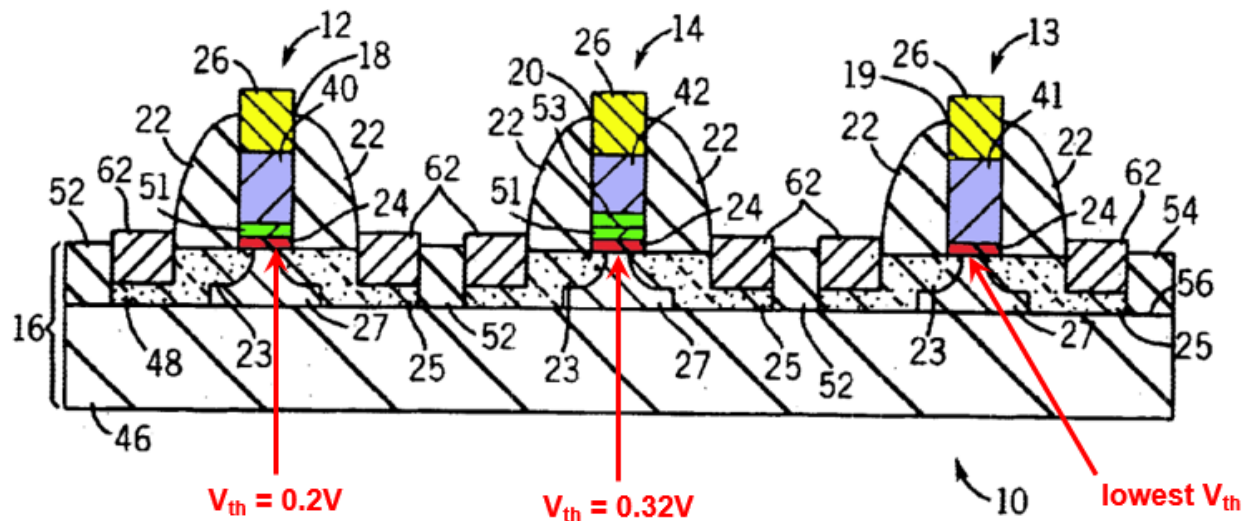
194. A POSITA would have been motivated to use Yu's teachings regarding varying the work function of individual gate electrodes by adding one or more metal layers to the gate stack of the LOP and LSTP nMIS transistors and adjusting the thickness and type of metal layers to further fine tune the threshold voltages of Torii's transistors. A POSITA would have been motivated to use a similar process as described in Yu to form gate electrodes with the necessary work function variations to obtain the required threshold voltage for the LOP and LSTP nMIS transistors of Torii without the need to rely on doping for additional threshold voltage adjustment. Torii's transistors use polysilicon in the gate electrode, like Yu's transistor. (TSMC-1005, 7:13-19; TSMC-1008, 5:30-34.) To add additional metal layers to Torii's transistors, a POSITA would have understood that Yu's fabrication process steps for forming the metal layers through use of masks and metal layer deposition (which I describe above) can be used with Torii's fabrication process. Specifically, as illustrated below, a POSITA would have been motivated to insert a metal layer into the LOP nMIS transistor ("*second MIS transistor*") and first and second metal layers into the LSTP nMIS transistor ("*first MIS transistor*"), as taught by Yu to ensure that the LOP nMIS transistor has the lower threshold voltage and that both the LOP and LSTP nMIS transistors obtain their intended threshold voltages.



Torii, Modified Figure 1 (left); Yu, Figure 1 (right)

195. In Yu, the thickness and types of materials for layers 51 and 53 used in the gate stacks “can be controlled to control the adjustment to the work function, thereby selecting threshold voltage.” (TSMC-1008, 6:1-3.) “If transistors 12 and 14 are N-channel transistors, transistor 12 has a lower threshold voltage than transistor 14.” (INTEL-1008, 6:26-31.) For example, if transistors are nMOS transistors, transistor 12 “has a threshold voltage of approximately 0.2V” and transistor 14 “has a threshold voltage of approximately 0.32V.” (TSMC-1008, 6:36-38.) Transistor 13 “has the lowest threshold voltage.” (TSMC-1008, 6:34-35.) That is, for nMOS transistors, the transistor with two metal layers has higher threshold

voltage than the transistor with one metal layer which has a higher threshold voltage than the transistor without a metal layer.



Yu, Figure 1

196. Thus, in the combination of Torii and Yu, the LSTP nMIS transistor (with two added metal layers) has a higher threshold voltage than the LOP nMIS transistor (with one added metal layer), as taught by Yu, consistent with Torii's disclosure that the LSTP nMIS transistor has a higher threshold voltage than the LOP nMIS transistor.

197. Based on this disclosure, the combination of Torii and Yu also discloses or at least suggests claim 15 under PO's litigation allegations. I understand that in the co-pending district court litigation the PO alleges a transistor with an additional metal layer in its gate electrode would demonstrate a slightly

higher effective work function than another MIS transistor missing this layer because the additional layer allegedly possesses a higher effective work function. The combination of Torii and Yu teaches addition of a metal layer with a higher work function into the gate stack of the LSTP transistor.

198. In the combination of Torii and Yu, the LSTP nMIS transistor has two metal layers 51 and 53 and the LOP nMIS transistor has a single metal layer 51. In Yu, layers 51 and 53 “can be nickel or titanium layers formed on top of each other or on top of gate dielectric 24.” (TSMC-1008, 5:56-58; *see also*, TSMC-1008, 7:22-30.) Yu stresses that the second metal layer (layer 53) “preferably has a different work function associated with it than” the first layer. (TSMC-1008, 7:63-67.) Accordingly, Yu teaches two options for the LSTP gate stack: Ti (layer 51)-Ni (layer 53) or Ni (layer 51)-Ti (layer 53). That is, only two alternatives exist for depositing Ti and Ni as layers in Yu’s transistors—either Ti is deposited as layer 51 followed by depositing Ni as layer 53 or the reverse, Ni is deposited as layer 51 followed by depositing Ti as layer 53. Each deposition ordering would have been obvious to try and a POSITA would have had a reasonable expectation of success because depositing Ni followed by Ti or Ti followed by Ni is the product of ordinary skill and common sense, not the product of innovation in the

semiconductor field by September 2010, the earliest priority date of the '779 patent.

199. It is well established that Ti is a low work function metal ($\Phi_m \sim 4\text{eV}$) and Ni is a high work function metal ($\Phi_m \sim 5\text{eV}$). (See, e.g., TSMC-1033, 200⁸.) Thus, when layer 51 is Ti ($\Phi_m \sim 4\text{eV}$) and layer 53 is Ni ($\Phi_m \sim 5\text{eV}$), the additional layer 53 in the LSTP transistor has a higher effective work function than layer 51, the only layer present in the LOP transistor. According to PO's litigation allegations, the LSTP transistor (having both Ti (layer 51) and Ni (layer 53)) will

⁸ I note that although the Polishchuk reference expresses the work functions of Ti and Ni metals in Volts (V) rather than the customary energy units of electron volts (eV), a POSITA would understand that these units are practically interchangeable in this context. This is because the work function represents the minimum energy required to move a single electron (an elementary charge) from the metal's Fermi energy level to the vacuum level. (See § III.A.4.) Because an eV is defined as the product of voltage (V) and the elementary charge (e), a POSITA would recognize that 1 eV is equivalent to $1\text{ V} \times e$, or that 1 V produces 1 eV of energy for a single electron (e). Therefore, and in reference to Polishchuk, I have replaced V with eV for consistency.

exhibit a higher effective work function than the LOP transistor (having only the Ti layer (layer 51). Thus, the combination of Torii and Yu discloses or at least suggests “*an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor*” under PO’s litigation allegations.

200. A POSITA would have been motivated to combine Yu’s teaching regarding inserting metal layers into the LOP and LSTP nMIS transistors of Torii to vary the gate work functions and hence further tune the threshold voltages of the LOP and LSTP nMIS transistors. Torii suggests, and a POSITA would have known, that LOP and LSTP nMIS transistors require different threshold voltages. (TSMC-1005, 2:51-54, 3:2-10; TSMC-1016, 11, 17, 21; § III.A.3.) A POSITA would have been motivated to combine Torii and Yu to fine tune the gate effective work functions of the LOP and LSTP transistors by adding metal layers so that their threshold voltages can be set to the desired values without having to rely on gate dielectric thickness engineering, and channel and gate electrode doping engineering, which can be burdensome and fabrication intensive.

201. Yu confirms this motivation, explaining that “[u]tilizing channel implants to adjust the threshold voltages of transistors can be problematic because transistor short-channel performance is very susceptible to process variations”

which “is particularly problematic as transistors become smaller and packing densities increase.” (TSMC-1008, 3:27-37.) This sentiment is also consistent with a POSITA’s knowledge of the art. ITRS (2007) warns about the limitations of doping in scaled transistors: “Finally, the total number of dopants in the channel for such small MOSFETs becomes relatively small, which results in large random fluctuations in the dopant placement and number, and hence unacceptably large statistical variation of the threshold voltage.” (TSMC-1016, 27.) Yu’s disclosure is therefore consistent with the general direction of the semiconductor industry, as documented by ITRS (2007). For this reason, a POSITA would have been motivated to modify the metal work function to fine tune the threshold voltages of Torii’s transistors.

202. A POSITA would have been further motivated to apply the teachings of Yu in Torri to address the challenges with using high-k dielectrics with polysilicon gates, as I discussed in §VI.B.1 in the combination of Torii and Mise. (*See also*, §§III.A.1, III.A.3-4.) ITRS (2007) which presents current trends in the semiconductor industry notes that “[f]or all three logic types [HP, LSTP, and LOP transistors], it is projected that high-k gate dielectric will be required by 2008” and for all three logic types “metal gate electrodes are projected for 2008, in order to effectively prevent gate electrode depletion and hence allow acceptable scaling of

the equivalent electrical oxide thickness in inversion.” (TSMC-1016, 27.) That is, a POSITA would have been aware that prior to the ’779 patent, the semiconductor industry was shifting toward high-k dielectrics and metal gates. A POSITA would therefore have understood that the addition of metal layers between Torii’s polysilicon gate electrode and the high-k dielectric, as taught by Yu, is consistent with ITRS’s proposed goal and alleviates integration challenges. For example, the metal layers in Yu shield Torii’s polysilicon gate electrode from Fermi level pinning by spatially moving the polysilicon gate away from the high-k dielectric.

203. Adding metal gate layers in Torii’s transistors would be nothing more than using a known technique (inserting one or more metal layers into the gate stack and adjusting the thicknesses and types of materials of those meta layers) to a known device (Torri’s semiconductor device) ready for improvement. I discussed the motivation for this combination above. Yu’s gate electrode uses polysilicon, like the gate electrode of Torii, and includes additional metal layers, as I discussed above. (TSMC-1005, 7:13-19; TSMC-1008, 5:30-34.) Therefore, applying Yu’s teaching to Torii would simply involve applying the fabrication process disclosed in Yu for forming the additional metal layers of the gate electrode to Torii’s fabrication process. A POSITA would have had a reasonable expectation of success and the results of the combination would have been predictable. Both Yu

and Torii describe devices having transistors of the same conductivity device with different threshold voltages and Yu teaches that its technique is applicable to both SOI and “bulk-type substrates.” (TSMC-1008, 6:65-67.) Moreover, Yu, filed a decade before the ’779 patent, uses conventional photolithography and processes to add the metal layers to a gate stack. Such conventional techniques would have been well-known and understood by a POSITA. (*See* TSMC-1008, 7:29-30, 7:61-62.)

VIII. GROUND 4: Gilmer Renders Claims 1, 12-15 Obvious.

204. U.S. Patent 6,787,421 to Gilmer, et al. (“Gilmer”; TSMC-1009) issued on September 7, 2004 from an application filed in August 15, 2002, over 8 years before the ’779 patent.

A. Gilmer

205. Gilmer recognized in the prior art, “there is often a need to form transistors with different gate dielectric thicknesses on the same semiconductor substrate or wafer.” (TSMC-1009, 1:13-15.) As an example, Gilmer explains that “transistors for input/output (I/O) devices may require thicker gate dielectrics than, e.g., transistors used for the core logic.” (TSMC-1009, 1:15-17.) Gilmer describes a “conventional process for forming differing thickness” called Dual Gate Oxide (DGO). (TSMC-1009, 1:18-19.) I described the DGO process in §III.A.6.

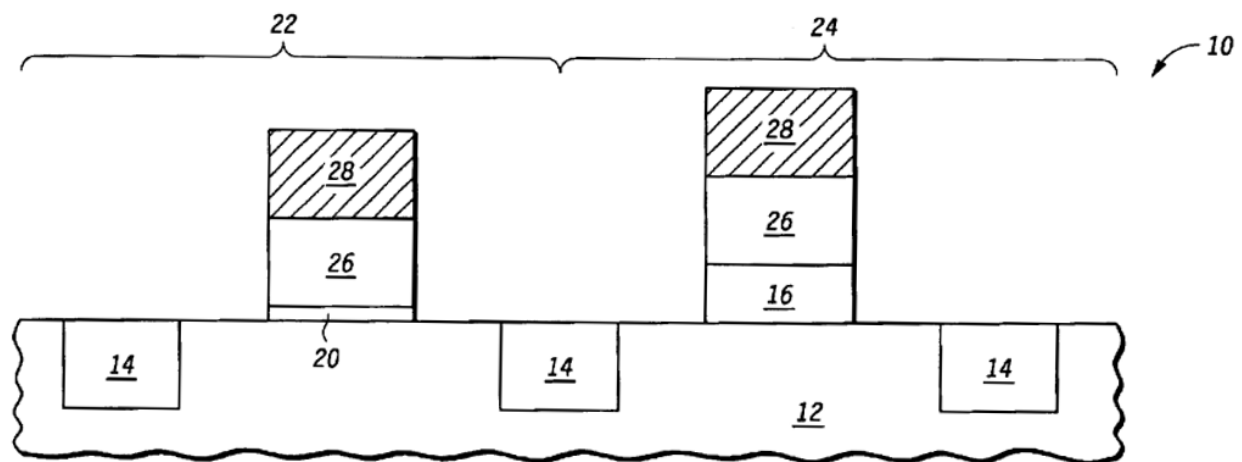
According to Gilmer, in the DGO process, “a ‘thick’ silicon dioxide layer (e.g. for the I/O devices) is formed and a resist mask is used to mask the thick silicon dioxide layer in the I/O regions.” (TSMC-1009, 1:20-22.) “The thick silicon dioxide layer is then etched away or otherwise removed from the unmasked region, where the core logic devices are to be formed.” (TSMC-1009, 1:23-25.) The mask is then “removed and a thin silicon dioxide layer is then grown over the core logic device region.” (TSMC-1009, 1:25-27.)

206. Gilmer notes that this approach has problems “as transistor sizes shrink” because “there is a move ... to replace traditional silicon dioxide gate dielectrics with higher-k dielectric materials” such as metal oxides. (TSMC-1009, 1:36-40.) For example, “because metal oxides cannot be thermally grown on a silicon substrate as silicon dioxide can, there are problems associated with multiple metal oxide depositions to form differing oxide thicknesses.” (TSMC-1009, 1:40-46.)

207. Gilmer purportedly addresses these problems and is directed “to semiconductor devices formed having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials such as metal oxides.” (TSMC-1009, 1:7-10.) Gilmer’s “invention integrates a high-k dielectric material, preferably a metal oxide, in a dual gate process sequence using a single metal oxide deposition to

form multiple gate dielectric stacks of differing thicknesses.” (TSMC-1009, 2:14-17.) The “metal oxide is formed over prepared surfaces of the substrate that already provide a difference in equivalent oxide thickness (EOT) between two different regions of the substrate (e.g. the core logic region and the I/O region).” (TSMC-1009, 2:17-22.)

208. Gilmer’s Figure 4 (reproduced below) illustrates its semiconductor device 10. Device 10 includes a semiconductor substrate having trench isolation regions 14 which “electrically isolat[e] different individual devices.” (TSMC-1009, 2:36-46.) The device includes core device region 22 and I/O device region 24. (TSMC-1009, 2:58-60.)



Gilmer, Figure 4

209. Core device 22 includes a gate dielectric 20, high-k dielectric (metal oxide) 26, and gate electrode 28 “patterned and etched to form the gate stack[.]” (TSMC-1009, 4:35-38.) Similarly, I/O device includes gate dielectric 16, high-k

dielectric (metal oxide) 26, and gate electrode 28 “patterned and etched to form the gate stack[.]” (TSMC-1009, 4:35-38.) After the device of Figure 4 is formed, “conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).” (TSMC-1009, 4:43-47.)

B. Independent Claim 1

210. Gilmer teaches each limitation of claim. I reproduce claim 1 of the '779 patent again below.

[1P] A semiconductor device comprising:

[1A] a first MIS transistor and [2A] a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,

[1A.1] wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,

[2A.1] the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,

[1A.2] the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and

a first high dielectric constant insulating film formed on the first interface layer,

[2A.2] the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,

[1B] the first interface layer has a thickness larger than that of the second interface layer, and

[1C] each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.

1. Preamble [1P]

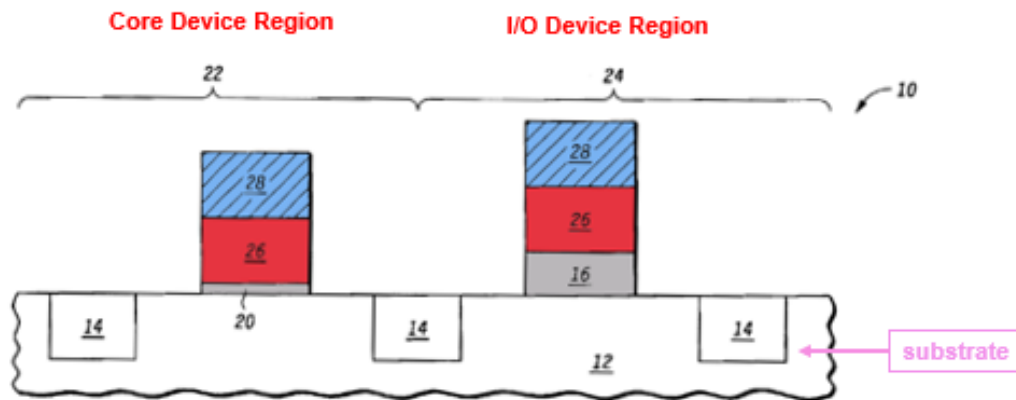
[1P] <i>A semiconductor device</i>

211. Gilmer discloses a “*semiconductor device*” [1P]. Gilmer is directed to “[a] **semiconductor device** (10) having two different gate dielectric thicknesses [] formed using a single high-k dielectric layer, preferably a metal oxide.” (TSMC-1009, Abstract; *see also* TSMC-1009, 1:7-10 (“The present invention relates generally to **semiconductor devices**”).) Gilmer’s Figures 1-4 “illustrate partial cross-sectional views of a **semiconductor device** formed to have two gate dielectric thickness (e.g. one for core devices and one for I/O devices) as it undergoes processing in accordance with one embodiment of the present invention[.]” (TSMC-1009, 1:57-60.)

2. Limitations [1A]-[2A]

[1A] *a first MIS transistor and [2A] a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate*

212. Gilmer's "semiconductor device 10 includes a **semiconductor substrate 12** which in a preferred embodiment is a single crystal silicon substrate." (TSMC-1009, 2:38-40, Figure 4 (below).) Gilmer's device, shown in Figure 4, "includes two different device regions, namely a core device region 22 and an I/O device region 24." (TSMC-1009, 2:59-60.) Gilmer teaches that "conventional processing occurs to complete the **transistor**" and thus each region includes "*a transistor*." (TSMC-1009, 4:43-44.)



Gilmer, Figure 4

213. The device structure of Figure 4 (above) shows a patterned gate stack in core device region 22 having a gate dielectric 20 (shaded gray), high-k metal oxide layer 26 (shaded red), and gate electrode material 28 (shaded blue). The

structure also shows a patterned gate stack in I/O device region 24 having gate dielectric 16 (shaded grey), high-k metal oxide layer 26, and gate electrode material 28. Gate dielectrics 16/20 and high-k metal oxide layer 26 are insulators. Gate electrode material 28 is “conductive (doped) polysilicon or a metal (e.g., titanium nitride).” (TSMC-1009, 2:48-50.) Therefore, the transistors in each region are metal-insulator-semiconductor or MIS transistors.

214. The transistor formed in the I/O device region 24 is a “*first MIS transistor*” [1A] and the transistor formed in the core device region 22 is a “*second MIS transistor*” [2A]. As shown above and described in Gilmer’s fabrication process (2:36-4:47), both transistors are provided on the same silicon substrate 12 and are therefore “*provided on an identical semiconductor substrate.*”

215. Gilmer does not explicitly specify that the I/O transistor and the core transistor are “*of an identical conductivity type.*” However, it would have been obvious to a POSITA that both transistors in Gilmer’s device share the same conductivity type (e.g., n-type or p-type) based on the teachings of Gilmer. For example, Gilmer extensively discusses the concept of Dual Gate Oxide (DGO), which relates to the formation of transistors having different gate dielectric thickness on the same semiconductor substrate or wafer. (TSMC-1009, 1:14-16.) As Gilmer acknowledges, the “DGO process ... has found acceptance in the

industry as a manufacturable and cost effective way of producing transistors having two different gate dielectric thicknesses.” (TSMC-1009, 1:34-37.) A POSITA would have understood that the core and I/O transistors of Gilmer formed by DGO process have the same conductivity type. As two examples, U.S. Patent 7,709,331 and U.S. Patent 8,014,469 each describe formation of a pair of transistors of the same conductivity type using DGO processes. (TSMC-1026, 3:45-4:36; TSMC-1027, 5:61-7:58; TSMC-1014, 121; §III.A.6.)

216. Gilmer also suggests that its transistors share the same conductivity type. As I mentioned previously, Gilmer’s semiconductor device 10 “includes a semiconductor substrate 12 which in a preferred embodiment is a single crystal substrate.” (TSMC-1009, 2:36-41.) The substrate typically has a conductivity type (e.g., n-type or p-type). For example, the substrate body may be p-type or n-type. Gilmer does not teach or suggest different conductivity types in the I/O and core regions, e.g., formation of well regions of a different conductivity type. This means that nMOS and pMOS pairs of transistors, such as those discussed in Gilmer, would be formed based on the POSITA’s understanding of the art.

217. “CMOS VLSI Design: A Circuits and System Perspective” by Weste and Harris (“Weste”) published in 2004 provides a background of nMOS and pMOS devices and of CMOS processing which demonstrates these concepts. An

nMOS transistor “is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain.” (TSMC-1012, 8.) A pMOS transistor “is just the opposing, consisting of p-type source and drain regions with an n-type body.” (*Id.*) Figure 1.8 of Weste provides a simplified depiction of nMOS and pMOS transistors using a polysilicon gate and SiO₂ gate insulating film. A POSITA would understand that other materials can be used.

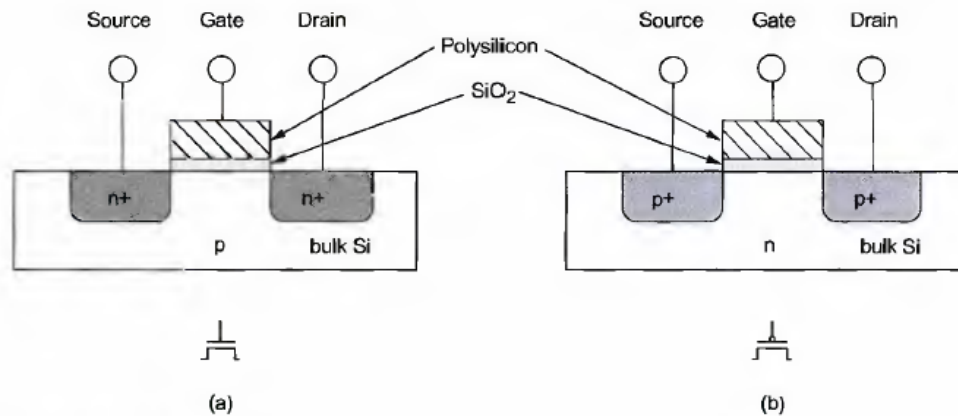
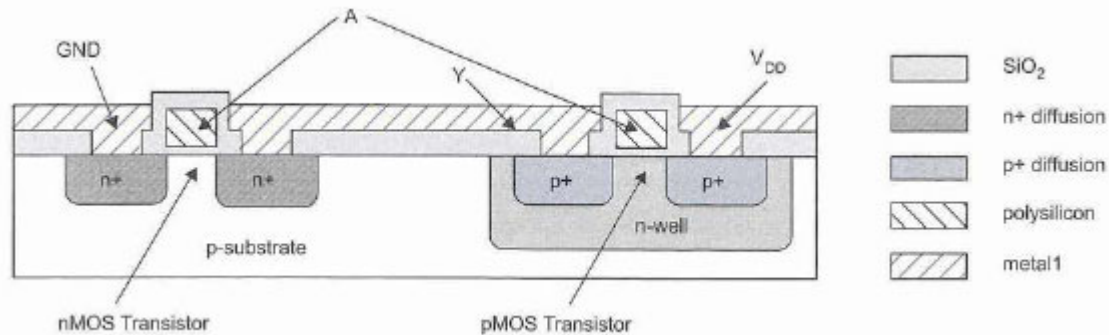


FIG 1.8 nMOS transistor (a) and pMOS transistor (b)

218. To form a transistor of a different conductivity type in one of Gilmer’s regions, an area of different conductivity type must be formed. This concept is illustrated in CMOS technology. Complementary MOS (CMOS) technology has been an important processing technology since the 1980s and is used today in all ICs. CMOS incorporates both nMOS and pMOS in a single IC as complementary pMOS-nMOS pairs. This means that for every pair of DGO pMOS transistors there is a corresponding counterpart pair of DGO nMOS transistors on the same

substrate. In CMOS technology, the substrate “is either n-type or p-type” and the “other flavor of transistor must be build in a special well in which dopant atoms have been locally added to form the body of the opposite type.” (TSMC-1012, 8.)

Figure 1.33 of Weste illustrates a CMOS device. As shown in this example, the nMOS transistor is formed on a p-type substrate and the pMOS transistor is formed in an n-well in the p-type substrate.



Weste, Figure 1.33

219. In view of the above background, a POSITA would ascertain from Gilmer’s description that both transistors share at least the same conductivity type because Gilmer does not disclose (i) the formation of any particular doped regions (i.e., wells) within the substrate in either the core or I/O regions which would provide for a conductivity type separate from that of the substrate, or (ii) any indication that each of the transistors in the core or I/O regions are formed on different conductivity type regions (i.e., wells) on the substrate.

220. Additionally, Gilmer compares the performance and electrical characteristics of the I/O and logic transistors. (*See, e.g.*, Gilmer, 2:60-65 (discussing voltages for core and I/O devices).) A POSITA would have understood such comparison applies only when the devices share a conductivity type as I discussed in §III.A.3.

221. Furthermore, a POSITA would have understood prior to the earliest possible priority date of the '779 patent that CMOS was the dominant processing technology in the semiconductor industry. (TSMC-1015, 42.) CMOS processing technology integrates both n- and p-type MOS devices side-by-side. (TSMC-1015, 42.) Therefore, although only one is depicted, a POSITA would have understood that the I/O device had both an n-type and a p-type transistor and the core device had both an n-type and p-type device, as I discussed above.

222. Moreover, a POSITA would have understood that only two alternatives exist in Gilmer for the conductivity type of its transistors: (1) the core and I/O transistors are of an identical conductivity type or (2) the core and I/O transistors are of different conductivity types. Pursuing both alternatives would have been obvious to try to a POSITA and a POSITA would have had a reasonable expectation of success in pursuing both alternatives, as I discuss below.

223. By the 2010 priority date of the '779 patent, having two transistors of the same conductivity type on a semiconductor substrate was not a product of innovation but a product of ordinary skill in semiconductor device manufacturing and common sense. Forming transistors of the same conductivity type (e.g., nMIS or pMIS transistors) in a substrate was well-known long before the '779 patent. (*See, e.g.*, TSMC-1012, 8.) Additionally, CMOS processing which forms both nMIS and pMIS transistors was also well-known before the '779 patent as I have discussed above and in §III.A.1.a. (*See, e.g.*, TSMC-1012, 113-125.) Because the processes were well-known, trying these two alternatives would have led a POSITA to anticipated success with either alternative. It would also mean that both p-type and n-type flavors of Gilmer's transistor pairs would co-exist on the same substrate, as this would have been a common practice in the art well before the filing of the '779 patent.

224. Gilmer therefore teaches or at least suggests “[1A] *a first MIS transistor and [2A] a second MIS transistor*” are “*of an identical conductivity type provided on an identical semiconductor substrate.*”

225. Should an argument be presented that Gilmer does not suggest both transistors share the same conductivity type, I disagree for the reasons discussed

above. However, an alternative ground which explicitly teaches two transistors of the same conductivity type on the same substrate is provided in Ground 5.

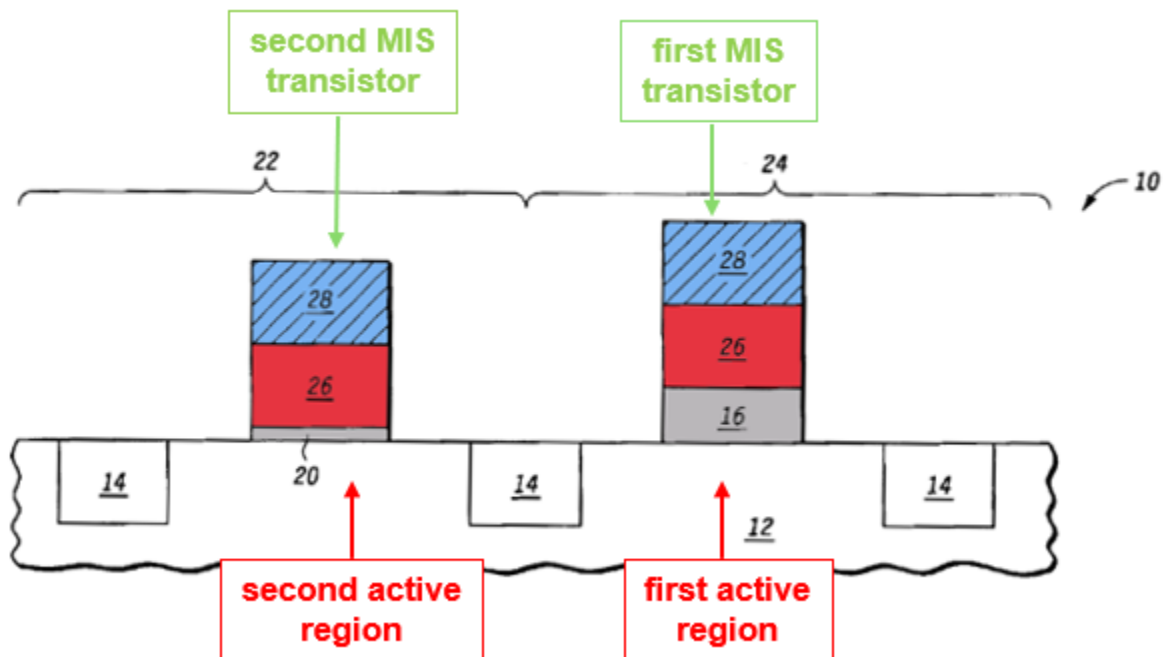
3. First and Second MIS Transistor Structure Limitations
[1A.1]-[1A.2]/[2A.1]-[2A.2]

[1A.1]	<i>wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film</i>
[2A.1]	<i>the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,</i>
[1A.2]	<i>the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer</i>
[2A.2]	<i>the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,</i>

a. “Active Region[s] in the Semiconductor Substrate”

226. The I/O and core transistors in Gilmer’s device each has an “*active region in the semiconductor substrate.*” As shown in Figure 4 below, “[w]ithin substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed.” (TSMC-1009, 2:43-46; *see*

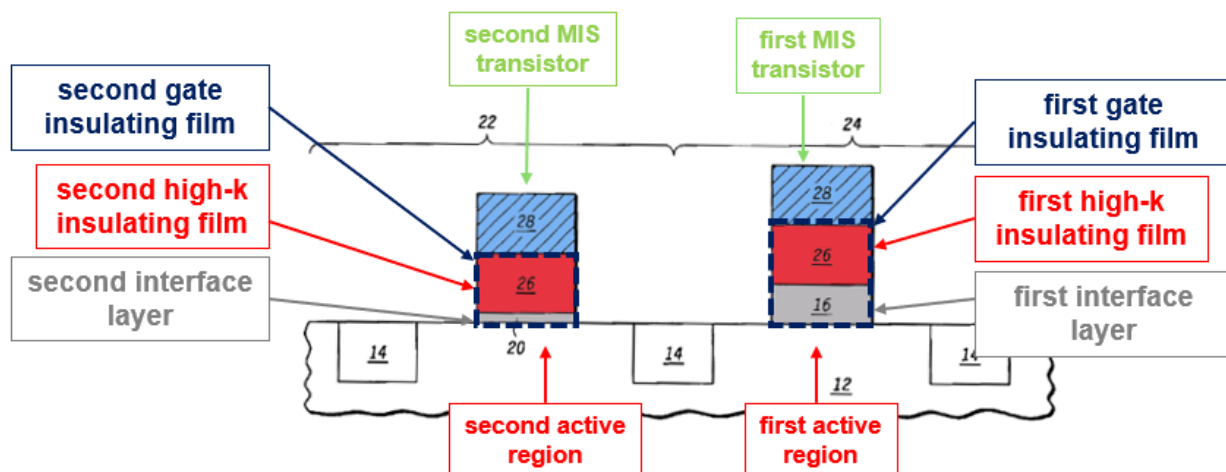
also, e.g., TSMC-1012, 119-120 (describing isolation processes.) I/O region 24 is a “first active region in the semiconductor substrate” and core region 22 is a “second active region in the semiconductor substrate.” Gilmer’s teachings are consistent with the disclosure in the background of the ’779 patent which explains that “a portion of the semiconductor substrate 100 surrounded by the shallow trench isolation 101 and located in the nMIS transistor region **serves as an active region 100b.**” (TSMC-1001, 1:67-2:3.)



Gilmer, Figure 4

b. “First MIS Transistor” and “Second MIS Transistor” Structure Limitations [1A.1]-[1A.2]/[2A.1]-[2A.2]

227. Gilmer teaches the structure recited in limitations [1A.1]-[1A.2] and [2A.1]-[2A.2]. As shown in Figure 4 (below), the gate stack of Gilmer’s I/O transistor (“*first MIS transistor*”) includes gate dielectric 16 (shaded grey) “formed over substrate 12” and metal oxide 26 (shaded red) formed on dielectric 16. (See TSMC-1009, 2:46-48, 3:44-47.) Metal oxide layer 26 is a “high-k dielectric.” (TSMC-1009, 3:44-54.) Gate dielectric 16 is the “*first interface layer being in contact with the semiconductor substrate*” and metal oxide 26 is a “*first high dielectric constant insulating film formed on the first interface layer* [gate dielectric 16]” [1A.2]. These layers, which are dielectrics, are collectively the “*first gate insulating film formed on a first active region in the semiconductor substrate*” [1A.1].



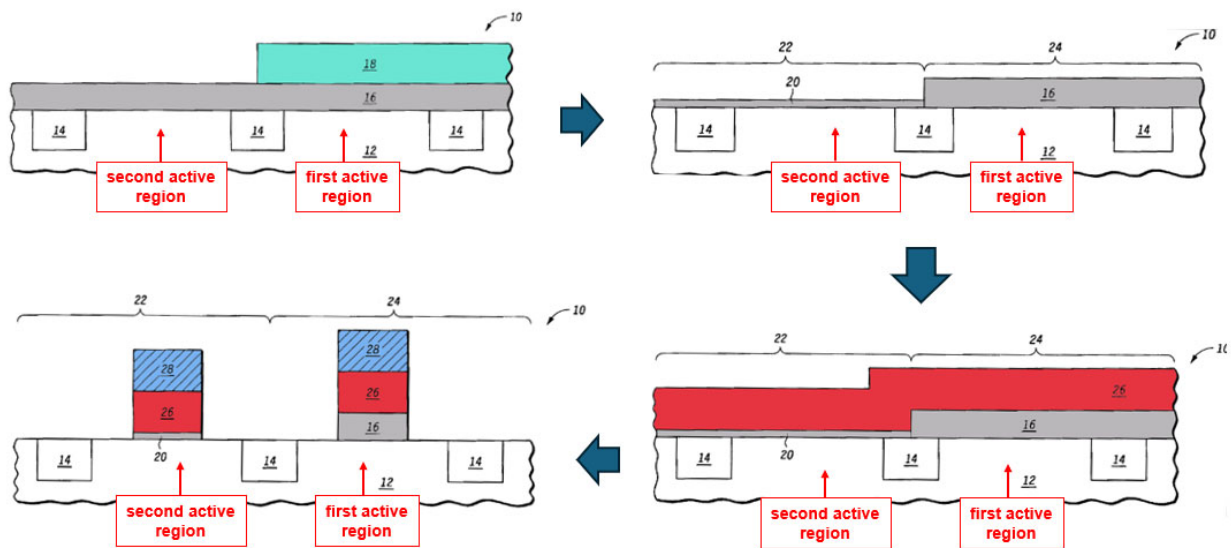
Gilmer, Figure 4

228. Similarly, as shown above, the gate stack of Gilmer's core transistor (*"second MIS transistor"*) includes gate dielectric 20 (shaded grey) and metal oxide 26 (shaded red) formed on dielectric 20. (See TSMC-1009, 2:46-48, 3:44-47.) Gate dielectric 20 is the *"second interface layer being in contact with the semiconductor substrate"* and metal oxide 26 is a *"second high dielectric constant insulating film formed on the second interface layer [gate dielectric 20]"* [2A.2]. These layers, which are dielectrics, are collectively the *"second gate insulating film formed on a second active region in the semiconductor substrate"* [2A.1].

229. The gate stack of I/O transistor 24 and core transistor 22 each also includes gate electrode 28 *"deposited over the metal oxide"* (the high-k dielectric) which is the top layer of the *"gate insulating film."* (TSMC-1009, 4:35-38.) Thus, the I/O transistor includes a *"first gate electrode formed on the first gate insulating film"* and the core logic transistor includes a *"second gate electrode formed on the second gate insulating film."*

230. Gilmer's fabrication process confirms the Figure 4 device structure. During fabrication of the Gilmer's device, *"after forming trench isolation regions 14, a first gate dielectric 16 [shaded grey] is formed over substrate 12."* (TSMC-1009, 2:46-48, Figure 1 (top-left).) Subsequently, *"a (photo)resist mask 18 [shaded light blue] is formed over the substrate to mask off a portion of the first gate*

dielectric layer” which will “serve, in part, as a gate dielectric for the higher voltage I/O devices.” (TSMC-1009, 2:56-58, 2:65-67.) The device 10 is then etched “to remove unprotected portions of first gate dielectric 16 in core device region 22” and after removal of mask 18, “second gate dielectric 20 [shaded grey] is formed on exposed portions of substrate 12 within the core device region 22.” (TSMC-1009, 3:7-12, Figure 2 (top-right).)



**Gilmer, Figures 1 (top-left), 2 (top-right)
3 (bottom-right), 4 (bottom-left)**

231. After the first and second gate dielectrics with “two different thicknesses have been formed, a high-k dielectric ... is deposited over semiconductor device 10.” (TSMC-1009, 3:44-47, Figure 3 (bottom-right). A “gate electrode material 28 [shaded blue] is deposited over the metal oxide, and

semiconductor device 10 is patterned and etched to form the gate stacks”, as shown in Figure 4. (TSMC-1009, 4:35-38.)

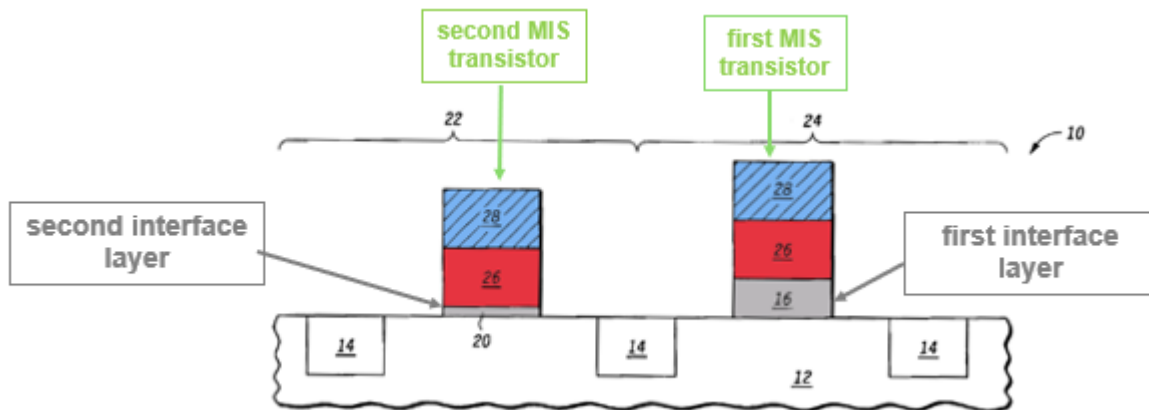
4. Limitation [1B]

[1B] <i>the first interface layer has a thickness larger than that of the second interface layer</i>
--

232. Gilmer repeatedly teaches that the first gate dielectric 16 (“*first interface layer*”) of the transistor in the I/O device region 24 “*has a thickness larger than that of*” the second gate dielectric 20 (“*second interface layer*”) of the transistor in the core device region 22:

- “[i]n operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher voltages required for I/O functions.” (Gilmer, 2:60-65.)
- “A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22).” (Gilmer, Abstract)
- “forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness” (Gilmer, claim 1)

233. Specifically, Gilmer teaches that the “thickness of gate dielectric 16 ... generally will be within a range of 30-50 Angstroms (3-5 nanometers)” (2:51-55) whereas the “thickness of gate dielectric 20 ... will be within a range of 4-12 Angstroms (0.4-1.2 nanometers)” (3:17-21). As shown clearly in Figure 4 below, “the first interface layer [gate dielectric 16] has a thickness larger than that of the second interface layer [gate dielectric 20]” [1B].



Gilmer, Figure 4

5. Limitation [1C]

[1C] each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film

234. Gilmer teaches that the “[f]irst gate dielectric 16 [“the first interface layer”] is preferably silicon dioxide or **silicon oxynitride**, and is preferably formed by thermal oxidation [sic] in accordance with conventional practices.” (TSMC-1009, 2:48-51.) Gilmer similarly teaches that “second gate dielectric 20 [“the

second interface layer”] is also silicon dioxide or **silicon oxynitride**.” (TSMC-1009, 3:12-14.) Thus, in the I/O and core transistors, “*each of the first interface layer and the second interface layer is made of ... a silicon oxynitride film*” [1C].

C. Claims 12-13

235. Dependent claim 12 and 13 further recite limitations directed to the high dielectric constant (high-k) insulating film of claim 1. I reproduce these claims again below. As I detail in this section, Gilmer teaches the subject matter of both claims.

12. *The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.*

13. *The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.*

236. As discussed in §VIII.B.3, Gilmer teaches that after the “gate dielectrics of two different thicknesses have been formed, a **high-k dielectric** ... is deposited over semiconductor device 10.” (TSMC-1009, 3:44-47.) Preferable, the high-k dielectric is a metal oxide 26 such as “**hafnium oxide (HfO₂)**, **hafnium silicate (Hf_xSi_yO_z)**, or lanthanum aluminate (LaAlO₃), but lanthanum oxide, hafnium aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable high-k dielectrics.” (TSMC-1009, 3:49-54.)

Because Gilmer teaches use of high-k film containing hafnium, Gilmer discloses an embodiment in which “*each of the first and second high dielectric constant insulating films contains hafnium or zirconium*” [12]. A POSITA would have been motivated to select, e.g., HfO₂ given its known benefits, e.g., “its superior thermal stability with poly-Si and reasonable band alignment.” (TSMC-1024, 2.4.1; *see also* TSMC-1013, 207; TSMC-1025, 134.)

237. Gilmer teaches that “[b]ecause metal oxide 26 is deposited as a **single blanket deposition**, its **thickness will not vary much** across the substrate surface and thus one should use the thicknesses of the first and second dielectrics as the ‘variables’ to achieve the final EOTs for the core and I/O devices.” (TSMC-1009, 4:2-7.) A POSITA would understand from this language that the metal oxide film, which is deposited as a single blanket deposition, is “*equal in thickness*” in both the I/O and core region subject to very minor variations. Gilmer’s teaching is consistent with the ’779 patent which only discloses that the “first and second high dielectric insulating films may be **substantially equal** in thickness.” (TSMC-1001, 5:31-33.) Thus, Gilmer teaches “*the first and second high dielectric constant insulating films are equal in thickness*” [13].

D. Claim 14

14. *The semiconductor device of claim 1, wherein the first and second gate electrodes are made of an identical material.*

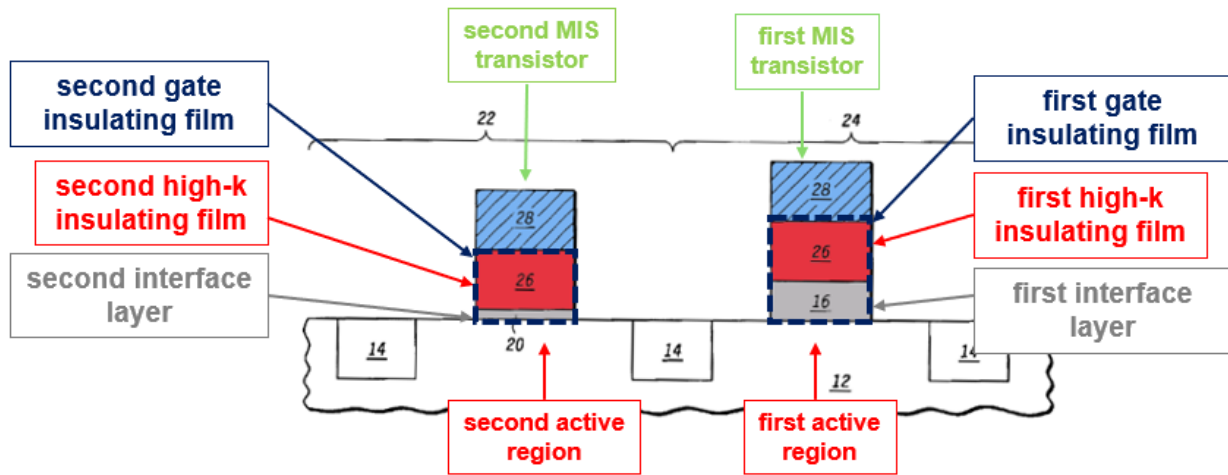
238. As discussed in §VIII.B.3, “[a]fter metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4.” (TSMC-1009, 4:35-38.) Gilmer teaches that “gate electrode material 28 will generally be conductive (doped) polysilicon or a metal (e.g. titanium nitride).” (TSMC-1009, 4:38-40.) Both gate stacks in Figure 4 use the same element label 28 for the gate electrode further indicating that both gate electrodes are made of the same material. Because the gate electrode layer is blanket deposited over the entire substrate and subsequently etched when gate stacks are formed, gate electrode layer 28 in both the I/O and core transistors “*are made of an identical material.*” Thus, Gilmer teaches that in its device, “*the first and second gate electrodes are made of an identical material*” [14].

E. Claim 15

15. *The semiconductor device of claim 1, wherein an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.*

239. Gilmer discloses claim 15, according to the disclosures of the '779 patent regarding “effective work function.” (See §§III.B-C; TSMC-1001, 4:29-31, 12:47-54, 13:23-27.) Gilmer’s I/O transistor has a greater EOT than its core transistor and therefore the I/O transistor has a higher effective work function than the core transistor according to the '779 patent.

240. As I discussed in §VIII.B.2 and illustrated again in Figure 4 below, Gilmer’s device includes two transistors of the same conductivity type: I/O transistor (“*first MIS transistor*”) and core transistor (“*second MIS transistor*”). The I/O transistor has a gate insulating film comprising gate dielectric 16 (shaded grey) and high-k metal oxide 26 (shaded red). Core transistor has a gate insulating film comprising gate dielectric 20 (shaded grey) and high-k metal oxide 26 (shaded red). Gilmer teaches that the high-k film of both the I/O and core transistors is formed in the same process step and therefore the high-k film in both gate stacks has the same thickness and same material (i.e., the same dielectric constant). (TSMC-1009, 3:44-47.)



Gilmer, Figure 4

241. The gate dielectric 16 and gate dielectric 20 are each preferably silicon oxynitride. (TSMC-1009, 2:48-49, 3:12-13.) Because the high-k layer of both transistors has the same thickness and use the same material (i.e., have same dielectric constant), the contributions of the high-k layer to the EOT of I/O transistor and the core transistor are the same and therefore cancel each other out in the comparison. Further, because the interface layer of both the I/O and core transistors use the same material (silicon oxynitride, $\epsilon_{16} = \epsilon_{20}$) but have different thickness (i.e., the $t_{16} > t_{20}$), the EOT of the I/O transistor is greater than the EOT of the core transistor.

EOT (I/O)

EOT (Core)

$$\left(\frac{t_{26}}{\epsilon_{26}}\right) \epsilon_{\text{SiO}_2} + \left(\frac{t_{16}}{\epsilon_{16}}\right) \epsilon_{\text{SiO}_2} > \left(\frac{t_{26}}{\epsilon_{26}}\right) \epsilon_{\text{SiO}_2} + \left(\frac{t_{20}}{\epsilon_{20}}\right) \epsilon_{\text{SiO}_2}$$

242. Accordingly, because the I/O transistor (“*first MIS transistor*”) has a greater EOT than the core transistor (“*second MIS transistor*”), the “*effective work function of the*” I/O transistor (“*first MIS transistor*”) “*is higher than an effective work function of the*” core transistor (“*second MIS transistor*”), according to the disclosure of the ’779 patent.

IX. GROUND 5: The Combination of Gilmer and Chen Renders Claim 1 and 12-15 Obvious.

243. Gilmer teaches a “*semiconductor device*” having “*first*” and “*second MIS*” transistors. As I discussed in §§VIII.B-D, Gilmer alone renders claims 1 and 12-14 obvious and in §VIII.E, Gilmer alone renders claim 15 obvious according to the disclosure of the ’779 patent. But should an argument be made that Gilmer alone does not render obvious that the “*first MIS*” and “*second MIS*” transistors are “*of the same conductivity type*”, U.S. Patent 7,382,023 to Chen, et al (“Chen”; TSMC-1010), issued June 3, 2008, provides this teaching as I discuss in §§IX.A-B below. Both Gilmer and Chen are in the same field as the ’779 patent “semiconductor devices and methods for fabricating the same.” (TSMC-1001, 1:15-16; TSMC-1009, 1:7-10, 2:36-38; TSMC-1010, 1:12-14, 4:14-16.) Thus, the combination of Gilmer and Chen renders claims 1 and 12-14 obvious and claim 15 obvious according to the disclosure of the ’779 patent.

244. While Gilmer discloses claim 15 in the same manner discloses in the '779 patent, Gilmer does not disclose modifying the effective metal work function of the gate electrode, according to PO's litigation allegations. Chen discloses such metal work function engineering, as I discuss in §IX.C below.

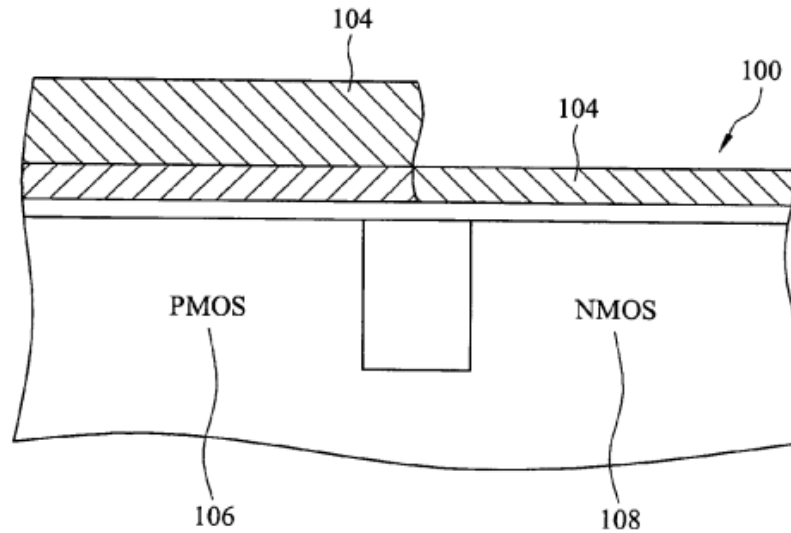
A. Chen

1. Background

245. Chen explains that “to produce competitive electronic devices, it is often desired to produce semiconductor chips with several different regions (e.g., core region, low power region, I/O region) having semiconductor devices that vary according to speed and power, for example.” (TSMC-1010, 1:18-22.)

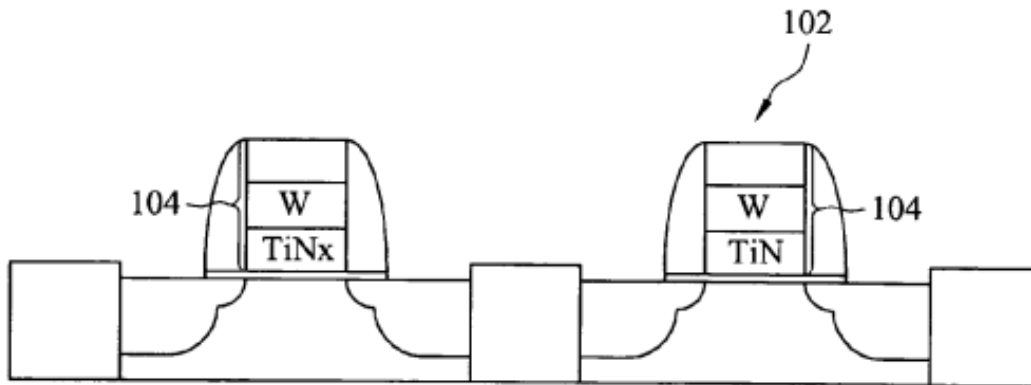
246. Chen describes prior art methods for controlling V_{th} of these transistors including “controlling the body potential of the SOI transistor” (TSMC-1010, 1:37-45) and “channel region doping” (TSMC-1010, 1:46-49). Chen also notes that “[a]nother known and accepted method of achieving a desired V_{th} is to modify the gate electrode work function by modifying the material composition of the gate electrode.” (TSMC-1010, 1:63-65.) For example, in prior art device 100 shown in Figure 1A (below), “the gate electrode 104 material composition, and correspondingly the gate electrode 104 work function, is varied to control the voltage threshold of the devices.” (TSMC-1010, 1:66-2:2.) Specifically, gate

electrode 104 “compris[es] nickel and titanium over the PMOS region 106 and comprising titanium over the NMOS region 108.” (TSMC-1010, 2:7-9.)



Chen, Figure 1A (Prior Art)

247. Chen’s prior art Figure 1B illustrates transistors 102 that “have gate electrode 104 material compositions of tungsten W, titanium Ti, a first concentration of nitrogen N and a second concentration of nitrogen Nx.” (TSMC-1010, 2:10-17.) “The variation of material composition varies the gate work function of each gate electrode 104, thereby varying the voltage threshold of the FD SOI transistors 102.” (TSMC-1010, 2:17-20.)



Chen, Figure 1B (Prior Art)

248. Chen describes that one “method to achieve a different threshold voltage for a fully depleted SOI device is to change the gate work function”, as demonstrated by the following equation from Chen. I also discussed this equation for threshold voltage in detail in §III.A.3.

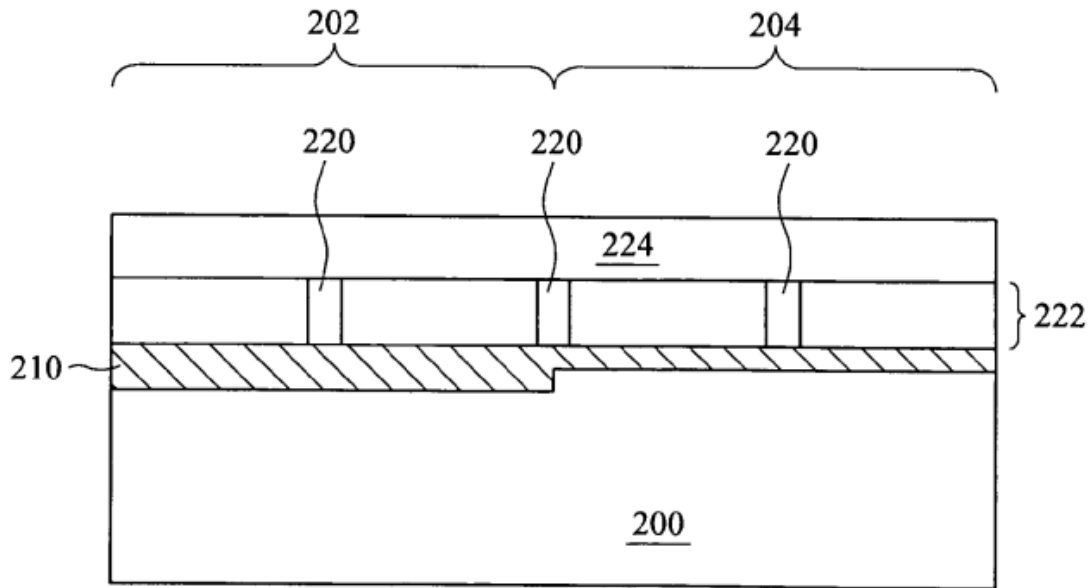
$$V_{th} = \underbrace{\Phi_{ms} - \frac{Q_f}{C_{ox}}}_{V_{FB}} + \Phi_s + \frac{\sqrt{2\epsilon q N_{A(D)} \Phi_s}}{C_{ox}}$$

249. If the substrate concentration ($N_{A(D)}$) is kept constant, another variable is needed “to control the threshold voltage to a desired value in a different application.” (TSMC-1010, 2:45-49.) The gate work function (the Φ_m component of Φ_{ms}) “is a good candidate for V_{th} tuning because recently metal gate development has become mainstream technology.” (TSMC-1010, 2:49-51.)

2. Chen's Gate Electrode Work Function Adjustment Technique

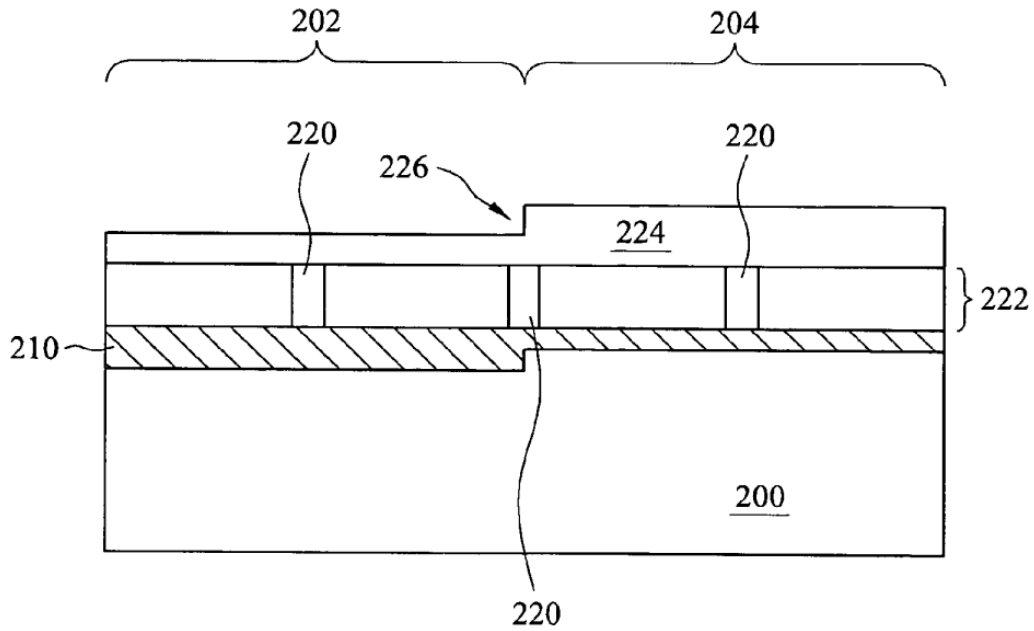
250. Chen discloses the combination of (1) buried dielectric thickness variation, (2) gate dielectric thickness variation, and (3) gate electrode work function variation provides a high degree of control of the voltage threshold of the transistors and other devices on the same chip die or in the same wafer. (TSMC-1010, 8:43-49.) Chen's third embodiment illustrates each of these control mechanisms.

251. As shown in Figures 3a-3h (third embodiment), the substrate "has a core region 202 and an input/output (I/O) region 204." (TSMC-1010, 4:49-50.) In Figure 3a, STI structures 220 "are formed in the silicon region 222 overlying the buried dielectric 210." (TSMC-1010, 7:3-5.) Gate dielectric 224 is then deposited. (TSMC-1010, 7:9-10.) The gate dielectric is "formed of a high k dielectric material having a high dielectric constant, greater than about 4" such as a "metal dielectric, including metal oxide such as Al_2O_3 , Ta_2O_5 , ZrO_2 , and HfO_2 , or HfSi for example." (TSMC-1010, 7:12-17.)



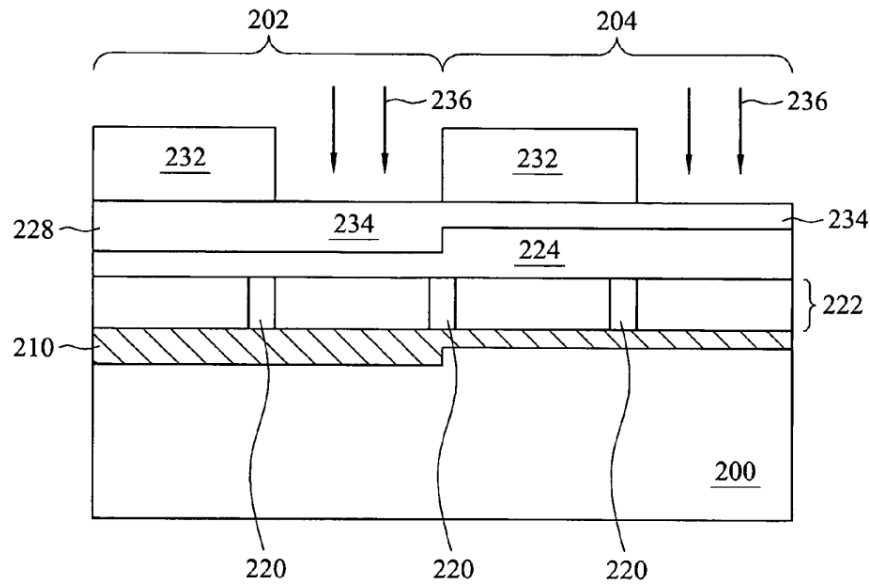
Chen, Figure 3a

252. The gate dielectric 224 in the I/O region 204 is masked “and a portion of the exposed gate dielectric 224 in the core region 202 is removed.” (TSMC-1010, 7:20-23, Figure 3b (below).) The “thicker portion of the gate dielectric 224 will enable a higher voltage threshold in the FD SOI devices that will subsequently be formed in the I/O region 204.” (TSMC-1010, 7:30-32.) In contrast, the “devices to be formed in the core region 202 will have a thinner gate dielectric 224 and a corresponding lower voltage threshold.” (TSMC-1010, 7:32-35.)



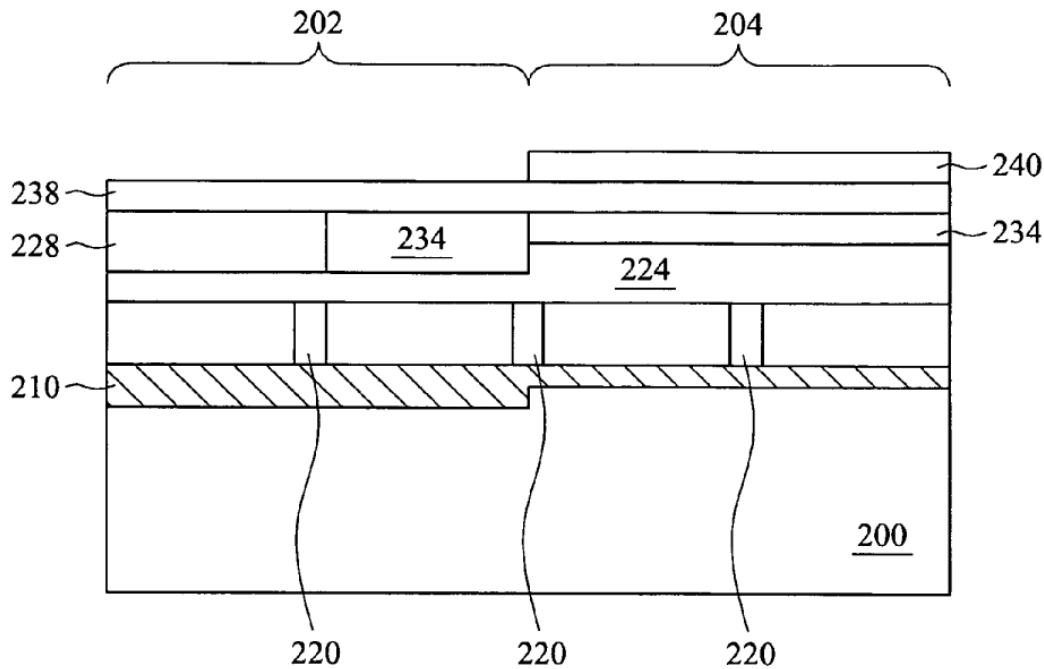
Chen, Figure 3b

253. Polysilicon 228 “is deposited on the gate dielectric 224.” (TSMC-1010, 7:35-36.) A photoresist is formed on the polysilicon, as shown in Figure 3d. “Unmasked portions 234 of the polysilicon 228 are doped 236 with an n-type dopant, forming n-doped polysilicon region 234.” (TSMC-1010, 7:44-46.)



Chen, Figure 3d

254. Once the mask (photoresist material 232) is removed, first metal layer 238, preferably comprising titanium, and second metal layer 240, preferably comprising platinum, “are consecutively deposited over the gate dielectric 224.” (TSMC-1010, 7:53-63.) The first 238 and second 240 metal layers may, for example, “alternatively comprise nickel, palladium, platinum, iridium, ruthenium, rhodium, molybdenum, hafnium, aluminum, cobalt, tungsten, or combinations thereof” including “metal alloys such as binary metal alloys, metal silicides, metal silicon nitrides, doped metal alloys, and doped silicide alloys, for example.” (TSMC-1010, 7:63-8:3.) Subsequently, a portion of the second metal layer 240 in the I/O region is masked and the second metal layer 240 in the core region is removed. (TSMC-1010, 8:4-7, Figure 3f (below).)

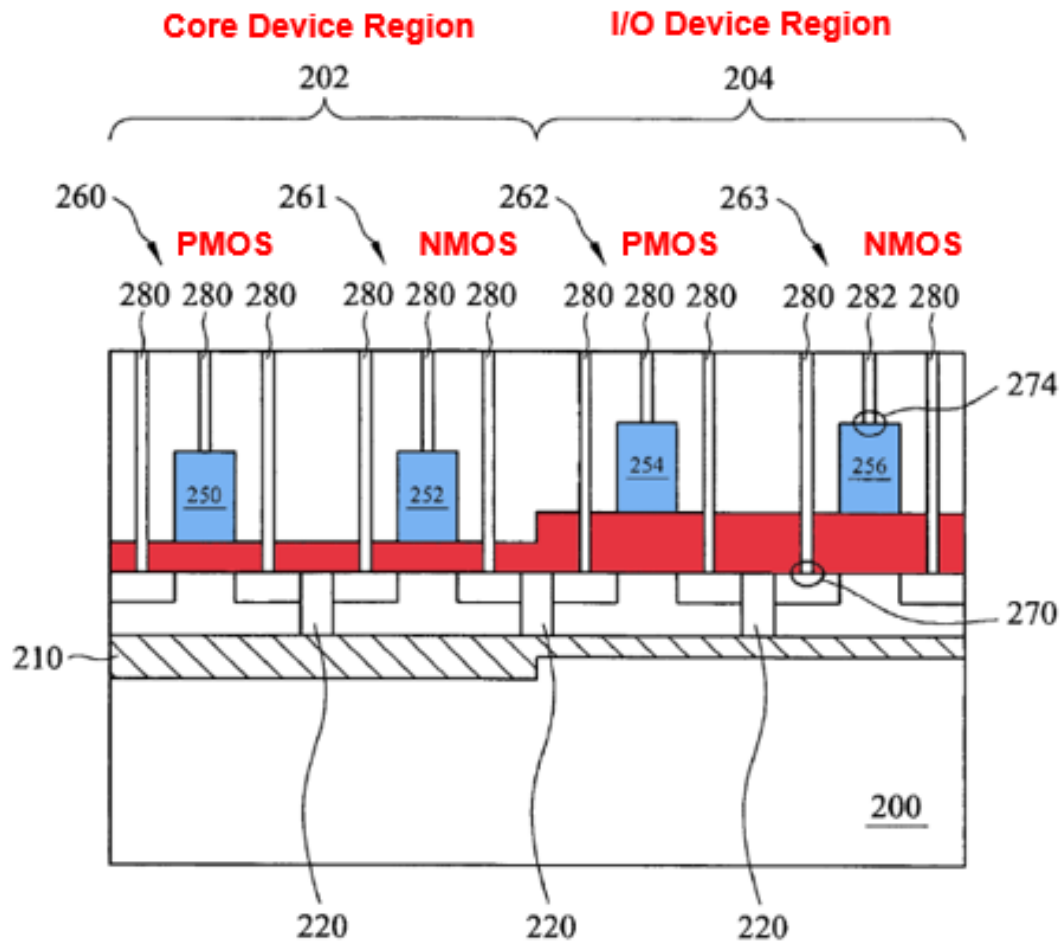


Chen, Figure 3f

255. A thermal anneal then “causes the metals 238 and 240 to diffuse into the undoped 228 and doped 234 regions of the polysilicon.” (TSMC-1010, 8:10-13.) This anneal process “produces a silicon titanium alloy gate electrode 250 and an n-doped silicon titanium alloy gate electrode 252 in the core region and a titanium, platinum and silicon alloy 254 and an n-doped titanium, platinum and silicon alloy 256 in the I/O region 204.” (TSMC-1010, 8:13-18.)

256. After further processing, transistors are produced as shown in Figure 3h below. Chen discloses that the resulting chip includes a first pMOS transistor with a “first gate electrode having a first work function” and a first nMOS transistor with a “second gate electrode having a second work function” in the

“core region.” (TSMC-1010, 3:39-46.) The chip also includes a second pMOS transistor with a “third gate electrode having a third work function” and a second nMOS transistor with a “fourth gate electrode having a fourth work function” in the I/O region. (TSMC-1010, 3:49-58.) I note that Chen has a typographic error referring to devices 260 and 261 as pMOS devices and devices 262 and 263 as nMOS devices (*See* TSMC-1010, 8:27-29.) A POSITA would have understood devices 260 and 262 to be pMOS devices and devices 261 and 263 to be nMOS devices because Chen makes clear each of the core and I/O regions include, respectively, a pMOS and an nMOS transistor pair. (*See, e.g.*, TSMC-1010, 3:34-60.) This is also evident from Chen’s claim 31. Further evidence for devices 261 and 263 being nMOS devices is the description of the n-type implants for source/drain regions (TSMC-1010, 7:45 and Figure 3d), as well as the description of device 263 being an nMOS device (TSMC-1010, 9:1). Conversely the other two devices, 260, and 262, are pMOS devices.



Chen, Figure 3h

257. Chen teaches that “[v]arying the material composition, and thereby the work function of the gate electrodes 250, 252, 254, and 256, provides a corresponding difference in voltage threshold” between the devices 260, 261, 262, and 263. (TSMC-1010, 8:29-33.) That is, the threshold voltages of the transistors 260, 261, 262, and 263 “are partially controlled by the work function of the gate electrodes 250, 252, 254, and 256.” (TSMC-1010, 8:33-35.) The gate electrode 252

of the first region nMOS transistor has a work function ranging between about 4.2 eV and about 4.5 eV and the gate electrode 256 of the second region nMOS transistor has a higher work function, ranging between about 4.5 eV and about 4.8 eV. (TSMC-1010, 8:39-42.) And the gate electrode 250 of the first region pMOS transistor has a work function ranging between about 4.7 eV and about 5.0 eV and the gate electrode 254 of the second region pMOS transistor has a work function ranging between about 4.4 eV and about 4.7 eV. (TSMC-1010, 8:36-38.)

B. Combination of Chen's Core and I/O transistors of the same conductivity type with Gilmer

258. Gilmer discloses core and I/O transistors formed in a shared substrate as illustrated in Figure 4 (below-top). Chen teaches core and I/O transistors having similar structures formed in the same substrate and having “*the same conductivity type*”, as shown in Figure 3h (below-bottom). (*See also*, TSMC-1010, 3:39-60, 8:27-42 (describing two pMOS and two NMOS transistors).)



Gilmer, Figure 4



Chen, Figure 3h

259. A POSITA would have been motivated to combine Chen's teachings regarding forming transistors having the same conductivity type (e.g., two nMIS transistors or two pMIS transistors) with Gilmer's semiconductor device. As I discussed in §VIII.B.2, Gilmer suggests forming transistors of the same conductivity type. For these same reasons, Gilmer suggests the combination with Chen. Additionally, a POSITA would have been motivated to make the combination based on his/her background knowledge in the relevant art and common sense. Because Gilmer does not specify the conductivity type of its transistors, a POSITA would have been motivated to apply background knowledge to implement the transistors. Fundamental to this implementation detail is conductivity type – whether the device is nMIS or pMIS. The '779 patent acknowledges in its background section the well-known concept that devices have conductivity types and describes use of an n-well for a pMIS transistor and a p-well for an nMIS transistor. (TSMC-1001, 1:61-2:15.) I discussed this well-known concept in the technical background as well. Based on this background knowledge, a POSITA would have been motivated to combine Gilmer and Chen and would have had a reasonable expectation of success in forming devices of the same conductivity type in Gilmer, as taught by Chen.

1. Independent Claim 1

260. Gilmer teaches every limitation of claim 1 but does not expressly state that the “*first*” and “*second*” MIS transistors are “*of the same conductivity type*.” Chen discloses its device of Figure 3h includes a pMOS transistor 260 and nMOS transistor 261 in the core device region 202 and a pMOS transistor 262 and nMOS transistor 263 in the I/O device region 204. (See TSMC-1010, 3:39-60, 8:27-29.) That is, the device includes two nMOS transistors (i.e., two transistors “*of the same conductivity type*”) and two pMOS transistors (i.e., two transistors “*of the same conductivity type*”). Thus, the combination of Gilmer and Chen explicitly discloses “[1A] *a first MIS transistor and [2A] a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate.*” (See also, §VIII.B.2.)

261. For this reason and the reasons I discussed in §VIII.B for the preamble [1P] and limitations [1A.1]-[1A.2], [2A.1]-[2A.2], [1B] and [1C], the combination of Gilmer and Chen renders claim 1 obvious.

2. Dependent Claims 12-15

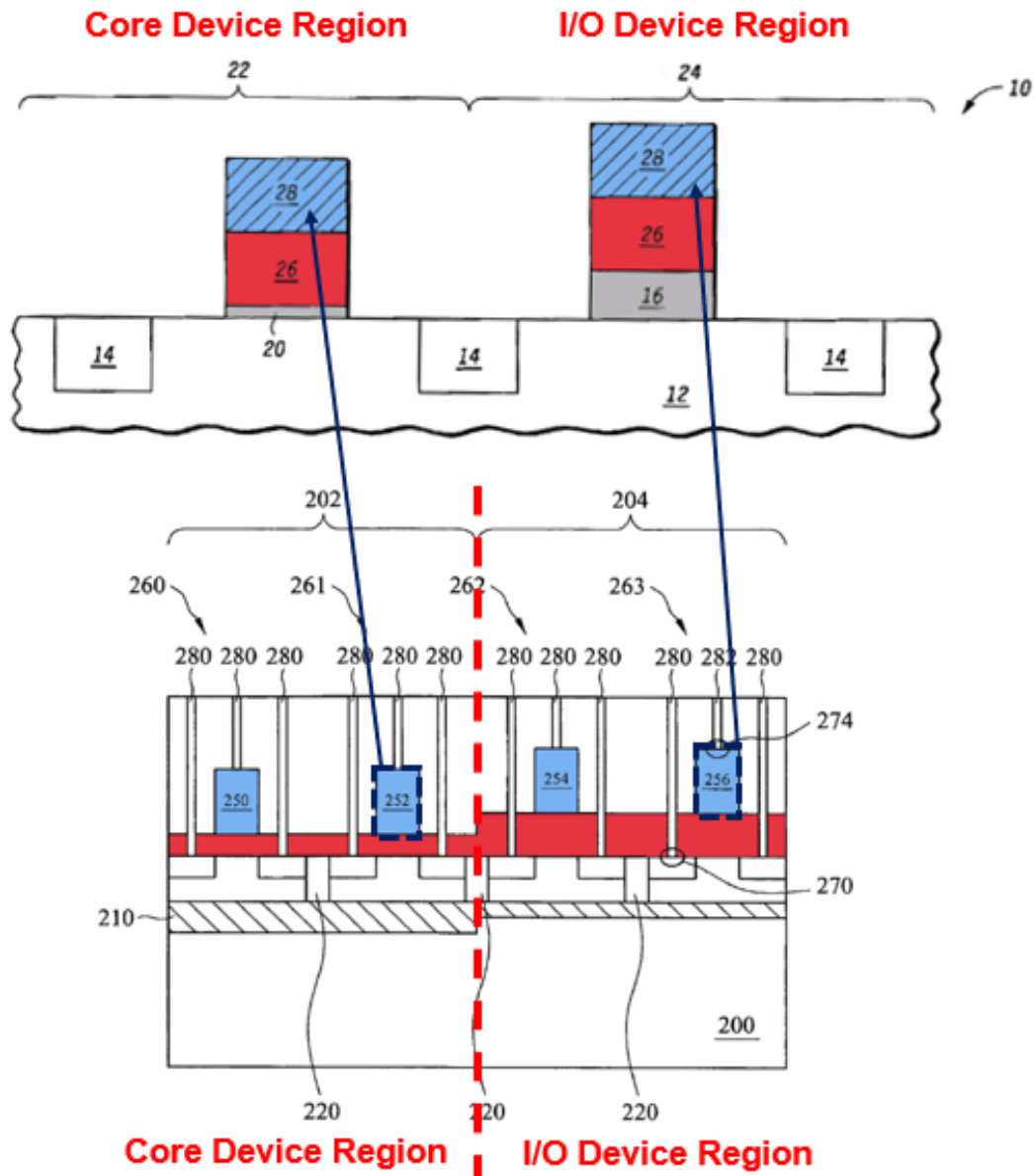
262. The combination of Gilmer and Chen renders claims 12-14 obvious for the same reasons discussed in §§VIII.C-D and claim 15 obvious according to the disclosure of the ’779 patent for the same reasons discussed in §VIII.E.

C. Combination of Chen's gate electrode work function variation teachings with Gilmer's transistors renders claim 15 obvious.

263. Gilmer generally mentions that after deposition of the high-k layer 26, “a gate electrode material 28 is deposited.” (TSMC-1009, 4:35-38.) In Gilmer, the gate electrode material “will generally be conductive (doped) polysilicon or a metal (e.g., titanium nitride).” (TSMC-1009, 4:38-40.) A POSITA would have been motivated to combine Chen's teachings regarding varying the composition of the gate electrode to vary the gate electrode work functions and better control the threshold voltage of the core and I/O transistors of Gilmer.

264. Specifically, the combination would use a process similar to that disclosed in Chen to produce metal alloys with different work functions. For example, Chen discloses first depositing polysilicon 228 on the gate dielectric 224 and doping portions of the polysilicon layer with “n-type dopant.” (TSMC-1010, 7:35-46.) Then a first metal layer 238 (e.g., titanium) and a second metal layer 240 (e.g., platinum) “are consecutively deposited over the gate dielectric 224” of the transistors in both the core and I/O regions. (TSMC-1010, 7:53-63.) The second metal layer 240 in the I/O region is then masked and the second metal layer 240 in the core region is removed. (TSMC-1010, 8:4-7.) A thermal anneal then “causes the metals 238 and 240 to diffuse into the undoped 228 and doped 234 regions of the polysilicon.” (TSMC-1010, 8:10-13.) This anneal process “produces a silicon

titanium alloy gate electrode 250 and an n-doped silicon titanium alloy gate electrode 252 in the core region 202” and “a titanium, platinum and silicon alloy 254 and an n-doped titanium, platinum and silicon alloy 256 in the I/O region 204.” (TSMC-1010, 8:13-18.) A POSITA would have been motivated to use these teachings to form the gate electrodes of Gilmer, as illustrated in the figures below.



Gilmer, Figure 4 (top); Chen, Figure 3h (bottom)

265. A POSITA would have been motivated to make the above combination because Chen expressly motivates the combination. Chen teaches that the threshold voltage of a core transistor differs from the threshold voltage of an I/O transistor, which is consistent with the POSITA's knowledge of the art. (See

§III.A.3.) Further, Chen, like Gilmer, discloses that the transistors in the core device region are built with a thinner gate dielectric stack compared to the transistors in the I/O device region. In other words, the transistors disclosed by Chen are similar to those of Gilmer and therefore suggest the combination.

266. Chen teaches that the “gate workfunction (ϕ_m) is a good candidate for V_{th} tuning” and discloses adjusting gate work function to achieve multiple threshold voltage devices on the same substrate. (TSMC-1010, 2:49-51.) A POSITA would be motivated to use Chen’s teachings to further tune or better control the V_{th} of the I/O transistor (e.g., by adjusting up its gate work function) if the thicker oxide in Gilmer’s I/O transistor did not offer sufficient V_{th} adjustment, as, for example, in the case of the nMOS I/O transistor. Similarly, a POSITA would be motivated to apply Chen’s teachings to further tune or better control the V_{th} of the core transistor (e.g., by adjusting down its gate work function) if the thinner oxide of the core transistor did not offer sufficient V_{th} adjustment, as, for example, in the case of the nMOS core transistor. Additionally, Gilmer would have benefitted from Chen’s low resistance silicided gate electrodes, whose resistance is lower than that of doped polysilicon, as would be understood by a POSITA. Accordingly, the combination would have been straightforward and therefore a

POSITA would have had a reasonable expectation of success in the combination and the combination would have yielded predictable results.

267. Chen discloses that “[v]arying the material composition” of the gate electrode, “and thereby the work function of the gate electrodes,” “provides a corresponding difference in voltage threshold between” the devices. (TSMC-1010, 8:27-33.) The gate electrode 252 of the nMOS core device “has a work function ranging between about 4.2 eV and about 4.5 eV” and the gate electrode 256 of the respective nMOS I/O device “has a work function ranging between 4.5 eV and about 4.8 eV.” (TSMC-1010, 8:39-42.) Thus, the “*effective work function*” of the nMOS I/O transistor (“*first MIS transistor*”) in the combination of Gilmer and Chen “*is higher than an effective work function*” of the NMOS core transistor (“*second MIS transistor*”) under PO’s litigation allegations.

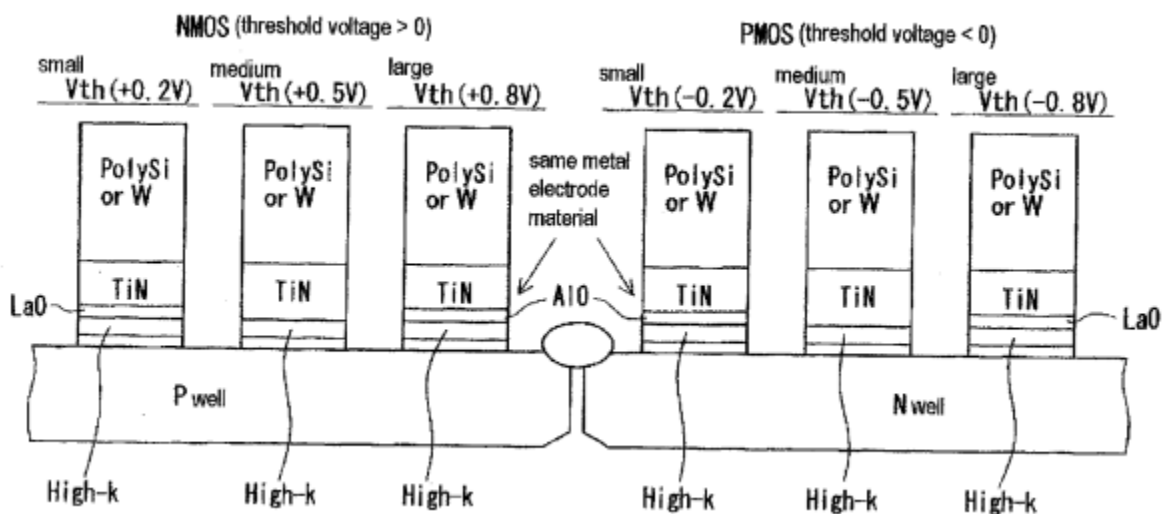
X. GROUND 6: The Combination of Gilmer, Chen, and Mise Renders Claims 8-11 Obvious.

268. In the combination of Gilmer and Chen, the “*first and second MIS transistors*” of its semiconductor device are “*pMIS transistors*” [8A] or “*nMIS transistors*” [10A], as taught by Chen. Neither Gilmer nor Chen however explicitly discloses the remaining limitations of claims 8-11. Mise provides these teachings, as discussed in §VI.A. Gilmer, Chen, and Mise are in the same field as the ’779 patent “semiconductor devices and methods for fabricating the same.” (TSMC-

1001, 1:15-16; TSMC-1009, 1:7-10, 2:36-38; TSMC-1010, 1:12-14, 4:14-16;
TSMC-1006, ¶1.)

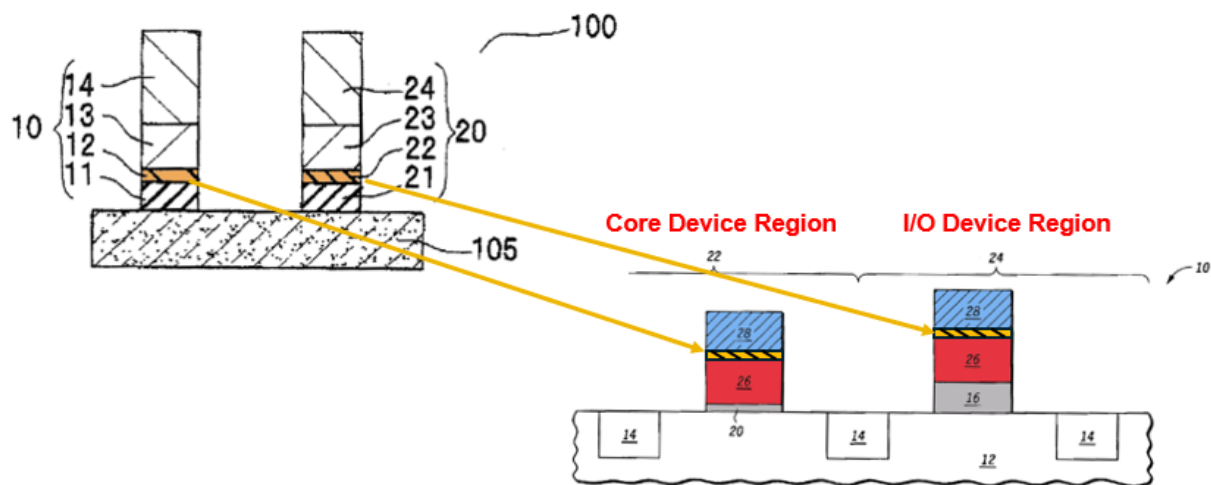
A. Combination of Gilmer, Chen, and Mise

269. Gilmer discloses core and I/O transistors formed in a common substrate. (TSMC-1009, Figure 4.) Chen teaches core and I/O transistors having similar structures formed in the same substrate and having “*the same conductivity type*.” (See, TSMC-1010, 3:39-60.) Mise teaches three NMIS transistors with the same conductivity type and different threshold voltages by incorporating capping layers in the gate stacks. (TSMC-1006, Figure 11-ninth embodiment (below).) Mise teaches three PMIS transistors with the same conductivity type and different threshold voltages by also incorporating capping layers in the gate stacks. (TSMC-1006, Figure 11-ninth embodiment (below).)



Mise, Figure 11

270. The combination of Chen and Gilmer uses Gilmer's suggestion of a semiconductor device having two transistors of the same conductivity type, as confirmed by the teachings of Chen. A POSITA would have motivated to apply Mise's teaching regarding use of a cap layer on a high-k film to the Gilmer-Chen device, illustrated in the figure below.



Mise, Figure 1 (left); Gilmer, Modified Figure 4

271. A POSITA would have been motivated to make this combination to further adjust/fine-tune the threshold voltage of the transistors. Gilmer teaches that the gate electrode material 28 “will generally be conductive (doped) polysilicon or a metal (e.g., titanium nitride).” (TSMC-1009, 4:38-40.) A POSITA would have been motivated to use the metal gate (TiN) for the reasons I discussed in §VI.B.1.

(TSMC-1018, 1.) Gilmer also teaches “[m]etal gate electrodes may also benefit from use of a capping layer” (TSMC-1009, 5:38-39.) Indeed, a primary purpose of a cap layer is to adjust the threshold voltage of a transistor, as acknowledged by the admitted prior art in the ’779 patent. (TSMC-1001, 2:24-27; *see also*, TSMC-1020, 441-444, TSMC-1021, 6:25-46; TSMC-1022, ¶4.) A POSITA would have been further motivated to apply a cap layer to improve operation of the devices by, e.g., reducing leakage current and improving compatibility between layers, as discussed in §VI.B.2.

B. PMIS Claims 8-9

272. Chen’s device includes first and second pMIS transistors. (§§IX.A-B.) Therefore, the combination of Gilmer and Chen discussed in §IX.B provides the “*first and second MIS transistors are pMIS transistors*” [8A].

273. Mise further teaches the cap layer 22 of the gate insulation film of the pMOS transistor “is composed of AlO.” (TSMC-1006, ¶72.) A POSITA would have been motivated to select a cap film containing aluminum, as taught by Mise in the pMIS devices of the combination of Gilmer and Chen. In the combination, the metal gate material (TiN) is “mid-gap” material. (*See, e.g.*, TSMC-1019, 1.) A POSITA would have therefore been motivated to include aluminum in the cap layer to shift the threshold voltage, making it appropriate for pMIS devices, as I

discussed in §VI.B. (See TSMC-1006, ¶¶154, 183-193, 195; TSMC-1020, 441-444; *see also*, TSMC-1021, 6:25-46, 12:8-23; §§VI.A, C.) The combination therefore provides “*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing aluminum*” [9A] and “*the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing aluminum*” [9B].

274. Regarding the high-k film, Gilmer teaches that suitable materials include “lanthanum aluminate (**LaAlO₃**), but lanthanum oxide, **hafnium aluminate**, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable.” (TSMC-1009, 3:49-54.) Mise similarly teaches that gate insulation film of the pMOS transistor “is composed of a high-k material such as **HfAlO**.” (TSMC-1006, ¶72.) A POSITA would have also understood that the high-k material in the combination contains aluminum, as taught by Gilmer and Mise, at least because of aluminum diffusion from the overlaying aluminum containing cap layer due to subsequent thermal processing. (TSMC-1021, 6:25-37, 11:1-26 (describing Al diffusion through the gate insulating stack); TSMC-1022, ¶19 (mentioning diffusion of metal atoms across the gate stack). Thus, in the

combination of Gilmer, Chen, and Mise, the “*high dielectric constant insulating films*” of both pMIS transistors “*contain aluminum*” [8B].

C. NMIS Claims 10-11

275. Chen’s device also includes first and second nMIS transistors. (§IX.A-B.) The combination of Gilmer and Chen discussed in §IX.B therefore provides “*first and second MIS transistors are nMIS transistors*” [10A].

276. Mise further teaches the cap layer 22 of the gate insulation film of the nMOS transistor “is composed of MgO or LaO.” (TSMC-1006, ¶71.) In the combination, the metal gate material (TiN) is “mid-gap” material. (*See, e.g.,* TSMC-1019, 1.) A POSITA would have therefore been motivated to select a cap layer containing lanthanum to shift the threshold voltage, making it appropriate for nMIS devices, for the reasons I discussed above in the combination of Torii and Mise. (*See* §VI.B.) Thus, the combination provides “*the first gate insulating film further includes a first cap film formed on the first high dielectric constant insulating film and containing lanthanum*” [11A] and “*the second gate insulating film further includes a second cap film formed on the second high dielectric constant insulating film and containing lanthanum*” [11B].

277. Regarding the high-k film, Gilmer teaches that suitable materials include “lanthanum aluminate (**LaAlO₃**), but **lanthanum oxide**, hafnium

aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable.” (TSMC-1009, 3:49-54.) Mise also teaches the gate insulation film of its nMOS transistor “is composed of a high-k material such as **HfLaO** or HfMgO.” (TSMC-1006, ¶71.) A POSITA would have also understood that the high-k material in the combination contains lanthanum, as taught by both Gilmer and Mise, at least because of lanthanum diffusion from the overlaying lanthanum containing cap layer due to thermal processing. (See §§VI.B, D.) Thus, in the combination of Gilmer and Mise, the “*high dielectric constant insulating films*” of both nMIS transistors “*contain lanthanum*” [10B].

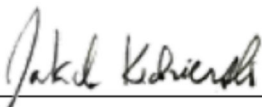
XI. Conclusion

278. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 11th day of April, 2025 in Lexington, MA.

Respectfully submitted,



Jakub Kedzierski, Ph.D.

EXHIBIT LIST

Exhibit	Description
1001	U.S. Patent 8,796,779 to Ito et al. (“the ’779 patent”)
1002	File History of U.S. Patent 8,796,779 (“’779 File History”)
1003	Declaration of Jakub Kedzierski
1004	CV of Jakub Kedzierski
1005	U.S. Patent 6,881,657 to Torii, et al. (“Torii”)
1006	U.S. Patent Publication 2010/0258878 to Mise, et al. (“Mise”)
1007	U.S. Patent 8,114,739 to Chowdhury, et al. (“Chowdhury”)
1008	U.S. Patent 6,693,333 to Yu (“Yu”)
1009	U.S. Patent 6,787,421 to Gilmer, et al. (“Gilmer”)
1010	U.S. Patent 7,382,023 to Chen (“Chen”)
1011	Van Zant, “Microchip Fabrication” (Fifth Edition, 2004) (“Van Zant”)
1012	Weste, “CMOS VLSI Design: A Circuits and Systems Perspective” (Third Edition, 2005) (“Weste”)
1013	Houssa, M., “High-k Dielectrics” to Houssa (IOP Publishing Ltd. 2004) (“Houssa”)
1014	Wolf, “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (2002) (“Wolf-4”)
1015	Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”)
1016	“International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures” (2007 Edition) (“ITRS”)

Exhibit	Description
1017	Campbell, “The Science and Engineering of Microelectronic Fabrication” (Second Edition, 2001) (“Campbell”)
1018	Chau, “Advanced Metal Gate/High-K Dielectric Stacks” (“Chau”)
1019	Guha, et al. “Examination of flatband and threshold voltage tuning of HfO ₂ /TiN field effect transistors by dielectric cap layers”, Applied Physics Letters (March 1, 2007) (“Guha”)
1020	H.-J. Li and M. Gardner, “Dual high-k gate dielectric with poly gate electrode: HfSiON on nMOS and Al ₂ O ₃ capping layer on pMOS,” IEEE Electron Device Lett., vol. 26, no. 7, pp. 441-443, 2005. (“Li/Gardner”)
1021	U.S. Patent 7,807,990 to Koyama (“Koyama”)
1022	U.S. Publication 2006/0244035 to Bojarczuk, JR, et al. (“Bojarczuk”)
1023	“Semiconductor Devices: Physics and Technology” by Sze (Second Edition, 2002) (“Sze”)
1024	Lee, S. J., et al. “High Quality Ultra Thin CVD HfO ₂ Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)
1025	Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)
1026	U.S. Patent 7,709,331 to Karve, et al. (“Karve”)
1027	U.S. Patent 8,017,469 to Luo, et al. (“Luo”)
1029	Wolf, “Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET” (1995) (“Wolf-3”)

Exhibit	Description
1030	Translated Excerpts from File History of JP2010-205599
1031	U.S. Patent 8,384,160 to Onishi, et al. (“Onishi”)
1032	“An Adjustable Work Function Technology Using Mo Gate for CMOS Devices”, Lin, et al., IEEE Electron Device Letters, Vol. 23, No. 1, January 2002
1033	“Dual Work Function Metal Gate CMOS Transistors by Ni-Ti Interdiffusion”, Polishchuk, et al., IEEE Electron Device Letters, Vol. 23, No. 4, April 2002