

## EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer

The following list illustrates certain grounds for invalidity:

- U.S. Patent 6,787,421 to Gilmer et al. (“*Gilmer*”) issued on September 4, 2004. Accordingly, *Gilmer* is prior art to U.S. Patent No. 8,796,779 (the “’779 patent”) under at least pre-AIA 35 U.S.C. §102(b).

*Gilmer*, including any material incorporated by reference into *Gilmer* anticipates claims 1 and 12-15 (the “asserted claims”) of the ’779 patent under pre-AIA 35 U.S.C. §102(b).

To the extent any limitation is found not to be expressly or inherently disclosed in *Gilmer*, such a limitation would have been obvious either based on *Gilmer* alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 779-02 through 779-17, because the ’779 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

In particular, any disclosures identified for each limitation of the ’779 patent in the aforementioned Exhibits may be combined with the disclosures of *Gilmer* identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.<sup>1</sup>

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to

---

<sup>1</sup> Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends

| <u>U.S. Patent No. 7,923,779</u>          | <u>Exemplary Disclosures Relevant to <i>Gilmer</i></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Claim 1                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| [1pre] A semiconductor device comprising: | <p>Gilmer, alone or in combination with one or more references, discloses or suggests a semiconductor device.</p> <p>For example, <i>Gilmer</i> discloses the following at 1:7-10:</p> <p style="padding-left: 40px;">The present invention relates generally to semiconductor devices, and more particularly to semiconductor devices formed having dual gate dielectric thicknesses and utilizing high-k gate dielectric materials such as metal oxides.</p> <p>For example, <i>Gilmer</i> discloses the following at 1:57-61:</p> <p style="padding-left: 40px;">FIGS. 1-4 illustrate partial cross-sectional views of a semiconductor device formed to have two gate dielectric thickness (e.g. one for core devices and one for I/O devices) as it undergoes processing in accordance with one embodiment of the present invention;</p> <p>For example, <i>Gilmer</i> discloses the following at 2:36-42:</p> <p style="padding-left: 40px;">Referring now to FIGS. 1-4, a semiconductor device 10 is fabricated in accordance with one embodiment of the invention. As shown in FIG. 1, semiconductor device 10 includes a semiconductor substrate 12 which in a preferred embodiment is a single crystal silicon substrate (also sometimes referred to as a wafer), but which can instead be formed from other semiconductor substrate materials.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:43-47:</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| U.S. Patent No. 7,923,779 | Exemplary Disclosures Relevant to <i>Gilmer</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | <p>At this point, conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).</p> <p>For example, <i>Gilmer</i> discloses the following at Figure 4:</p> <div data-bbox="871 492 1656 787" data-label="Image"> </div> <p align="center"><b>FIG. 4</b></p> <p>For example, <i>Gilmer</i> discloses the following at Abstract:</p> <p>A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22). First and second dielectrics are preferably silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric stack for each transistor, together with high quality silicon dioxide or oxynitride dielectric layers, problems associated with selective etching of the metal oxide may be avoided,</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 1 recites:</p> <p>1. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;</p> <p>removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;</p> <p>forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and</p> <p>forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 14 recites:</p> <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u>                                                                                                            | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                    | <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose the preamble, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <p>[1A] a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,</p> | <p>Gilmer, in combination with one or more references, discloses or suggests a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate.</p> <p>For example, <i>Gilmer</i> discloses the following at 1:14-50:</p> <p>In integrated circuit manufacturing, there is often a need to form transistors with different gate dielectric thicknesses on the same semiconductor substrate or wafer. For example, transistors for input/output (I/O) devices may require thicker gate dielectrics than, e.g., transistors used for the core logic. A conventional process for forming differing thickness is called a DGO process, which stands for Dual Gate Oxide. In a conventional DGO process, a "thick" silicon dioxide layer (e.g. for the I/O devices) is formed and a resist mask is used to mask the thick silicon dioxide layer in the I/O regions. The thick silicon dioxide layer is then etched away or otherwise removed from the unmasked region, where the core logic devices are to be formed. The mask is removed and a thin silicon dioxide layer is then grown over the core logic device region. The gate electrode material, typically polysilicon, is then deposited over the substrate, which at this point includes gate dielectrics of two different thicknesses. The gate electrode material and gate</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| U.S. Patent No. 7,923,779 | Exemplary Disclosures Relevant to <i>Gilmer</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | <p>dielectrics are then patterned and etched to form the gate electrode and oxide stack of each transistor.</p> <p>The DGO process described above has found acceptance in the industry as a manufacturable and cost effective way of producing transistors having two different gate dielectric thicknesses. However, as transistor sizes shrink there is a move in the semiconductor industry to replace traditional silicon dioxide gate dielectrics with higher-k dielectric materials (i.e. dielectrics having higher dielectric constants), such as metal oxides. But because metal oxides cannot be thermally grown on a silicon substrate as silicon dioxide can, there are problems associated with multiple metal oxide depositions to form differing oxide thicknesses and with etching of the metal oxide if one were to attempt to merely substitute a metal oxide for silicon dioxide in a conventional DGO process. Accordingly, there is a need for a semiconductor manufacturing process in which dual gate dielectric thicknesses can be achieved with metal oxides or other high-k dielectric materials.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:36-46:</p> <p>As shown in FIG. 1, semiconductor device 10 includes a semiconductor substrate 12 which in a preferred embodiment is a single crystal silicon substrate (also sometimes referred to as a wafer), but which can instead be formed from other semiconductor substrate materials. Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:58-65</p> <p>As shown in FIG. 1, semiconductor device 10 includes two different device regions, namely a core device region 22 and an I/O device region 24. In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower voltages than, e.g., I/O</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <b><u>U.S. Patent No. 7,923,779</u></b> | <b><u>Exemplary Disclosures Relevant to <i>Gilmer</i></u></b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                         | <p>devices to be formed in I/O device region 24 that can withstand higher voltages required for I/O functions.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:46-48</p> <p>After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:9-12:</p> <p>The resist mask 18 is then removed and a second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:44-47:</p> <p>Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with <math>k &gt; 4</math>, preferably with <math>k &gt; 6</math>, and most preferably with <math>k &gt; 7</math>) is deposited over semiconductor device 10.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:35-40:</p> <p>After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4. Gate electrode material 28 will generally be conductive (doped) polysilicon or a metal (e.g. titanium nitride).</p> <p>For example, <i>Gilmer</i> discloses the following at 4:43-47:</p> <p>At this point, conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

For example, *Gilmer* discloses the following at Figure 4:

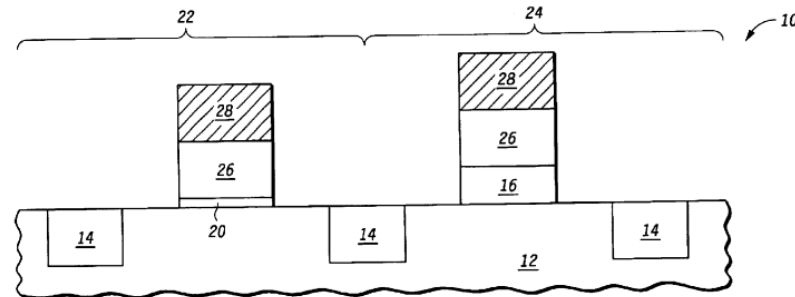


**FIG. 4**

For example, *Gilmer* discloses the following at Abstract:

A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22). First and second dielectrics are preferably silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric stack for each transistor, together with high quality silicon dioxide or oxynitride dielectric layers, problems associated with selective etching of the metal oxide may be avoided, as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.

For example, *Gilmer* discloses the following at claim 1:

1. A method for forming a semiconductor device comprising:  
providing a semiconductor substrate;

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;</p> <p>removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;</p> <p>forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and</p> <p>forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</p> <p>For example, Gilmer discloses the following at claim 14:</p> <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the</p> |
|--|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u>                                                                                                                                                                                | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                        | <p>references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <p>[1B] wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:43-46:</p> <p style="padding-left: 40px;">Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:46-55:</p> <p style="padding-left: 40px;">After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30-50 Angstroms (3-5 nanometers).</p> <p>For example, <i>Gilmer</i> discloses the following at 3:44-4:7:</p> <p style="padding-left: 40px;">Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with <math>k &gt; 4</math>, preferably with <math>k &gt; 6</math>, and most preferably with <math>k &gt; 7</math>) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (<math>\text{HfO}_2</math>), hafnium silicate (<math>\text{Hf}_x\text{Si}_y\text{O}_z</math>), or lanthanum aluminate (<math>\text{LaAlO}_3</math>), but lanthanum oxide, hafnium aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable high-k dielectrics. The thickness of the high-k dielectric layer</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

will be dependent on the particular device requirements in each region of the substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen so that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the substrate surface and thus one should use the thicknesses of the first and second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.

For example, *Gilmer* discloses the following at 4:35-43:

After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4. Gate electrode material 28 will generally be conductive (doped) polysilicon or a metal (e.g. titanium nitride). Preferably the same etch mask is used to pattern gate stacks in both the I/O and core device regions, but etch requirements may make it more desirable to use two masks, one for each of the two regions.

For example, *Gilmer* discloses the following at Abstract:

A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22). First and second dielectrics are preferably silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric stack for each transistor, together with high quality silicon dioxide or oxynitride dielectric layers, problems associated with selective etching of the metal oxide may be avoided,

EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer

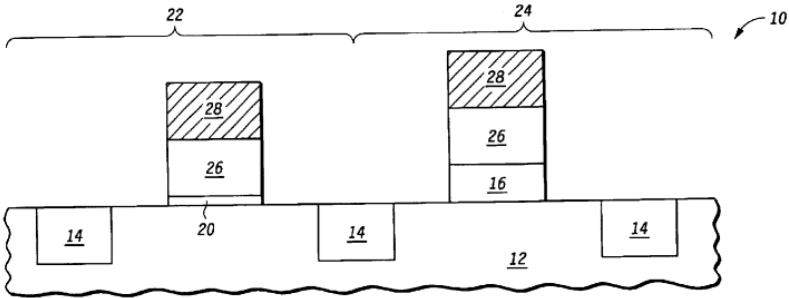
| U.S. Patent No. 7,923,779 | Exemplary Disclosures Relevant to <i>Gilmer</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | <p>as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:43-47:</p> <p>At this point, conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).</p> <p>For example, <i>Gilmer</i> discloses the following at Figure 4:</p> <div data-bbox="877 670 1661 966"></div> <p>For example, <i>Gilmer</i> discloses the following at claim 1:</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>1. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;</p> <p>removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;</p> <p>forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and</p> <p>forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</p> <p>For example, <i>Gilmer</i> discloses the following at claims 7-8:</p> <p>7. The method of claim 1, further comprising:</p> <p>forming a gate layer overlying the metal oxide layer and</p> <p>patterning the gate layer, metal oxide layer, first gate dielectric layer, and second gate dielectric layer to form a first gate electrode stack and a second gate electrode stack.</p> <p>8. The method of claim 7 wherein the first gate electrode stack is used in a core logic device and the second gate electrode stack is used in an I/O device.</p> <p>For example, <i>Gilmer</i> claim 14 recites:</p> <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u>                                                                                                                                                                             | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                     | <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p> |
| <p>[1C] the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:43-46:</p> <p style="padding-left: 40px;">Within substrate 12, trench isolation regions 14, preferably shallow trench isolation regions, are formed in a conventional manner for the purpose of electrically isolating different individual devices to be formed.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:9-33:</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| U.S. Patent No. 7,923,779 | Exemplary Disclosures Relevant to <i>Gilmer</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | <p>The resist mask 18 is then removed and a second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used. This second gate dielectric can be formed by thermal oxidation and/or chemical oxidation in accordance with conventional practices. The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers). Because second gate dielectric 20 is so thin, it may be difficult to adequately control the thickness or obtain an oxide of sufficient quality using thermal oxidation processes and therefore chemical oxidation may be useful. For instance, the thin dielectric may be formed by growing a thin oxide by rinsing the substrate in ozonated water. A combination of thermal and chemical treatment may also be used to form second dielectric 20. It may also be sufficient for second gate dielectric 20 to be a native oxide which is grown on substrate 12 as a result of exposing the substrate to ambient or other oxygen containing environment. In other embodiments, second gate dielectric 20 can be deposited, e.g., by atomic layer deposition.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:44-4:7:</p> <p>Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with <math>k &gt; 4</math>, preferably with <math>k &gt; 6</math>, and most preferably with <math>k &gt; 7</math>) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (<math>\text{HfO}_2</math>), hafnium silicate (<math>\text{Hf}_x\text{Si}_y\text{O}_z</math>), or lanthanum aluminate (<math>\text{LaAlO}_3</math>), but lanthanum oxide, hafnium aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen so that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric)</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>thickness or second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the substrate surface and thus one should use the thicknesses of the first and second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:35-43:</p> <p>After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4. Gate electrode material 28 will generally be conductive (doped) polysilicon or a metal (e.g. titanium nitride). Preferably the same etch mask is used to pattern gate stacks in both the I/O and core device regions, but etch requirements may make it more desirable to use two masks, one for each of the two regions.</p> <p>For example, <i>Gilmer</i> discloses the following at Abstract:</p> <p>A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22). First and second dielectrics are preferably silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric stack for each transistor, together with high quality silicon dioxide or oxynitride dielectric layers, problems associated with selective etching of the metal oxide may be avoided, as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:43-47:</p> |
|--|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer

| U.S. Patent No. 7,923,779 | Exemplary Disclosures Relevant to <i>Gilmer</i>                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | <p>At this point, conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).</p> <p>For example, <i>Gilmer</i> discloses the following at Figure 4:</p> <div data-bbox="877 500 1661 792"><p>FIG. 4</p></div> <p>For example, <i>Gilmer</i> discloses the following at claim 1:</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>1. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;</p> <p>removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;</p> <p>forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and</p> <p>forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</p> <p>For example, <i>Gilmer</i> discloses the following at claims 7-8:</p> <p>7. The method of claim 1, further comprising:</p> <p>forming a gate layer overlying the metal oxide layer and</p> <p>patterning the gate layer, metal oxide layer, first gate dielectric layer, and second gate dielectric layer to form a first gate electrode stack and a second gate electrode stack.</p> <p>8. The method of claim 7 wherein the first gate electrode stack is used in a core logic device and the second gate electrode stack is used in an I/O device.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 14:</p> <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> |
|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u>                                                                                                                                                                                 | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                         | <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p> |
| <p>[1D] the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:46-55:</p> <p>After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>device region 24 as further explained below, but generally will be within a range of 30-50 Angstroms (3-5 nanometers).</p> <p>For example, <i>Gilmer</i> discloses the following at 3:44-4:7:</p> <p>Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with <math>k &gt; 4</math>, preferably with <math>k &gt; 6</math>, and most preferably with <math>k &gt; 7</math>) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (<math>\text{HfO}_2</math>), hafnium silicate (<math>\text{Hf}_x\text{Si}_y\text{O}_z</math>), or lanthanum aluminate (<math>\text{LaAlO}_3</math>), but lanthanum oxide, hafnium aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen so that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the substrate surface and thus one should use the thicknesses of the first and second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p>For example, <i>Gilmer</i> discloses the following at Abstract:</p> <p>A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22). First and second dielectrics are preferably silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by</p> |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><b>U.S. Patent No. 7,923,779</b></p> | <p><b><u>Exemplary Disclosures Relevant to <i>Gilmer</i></u></b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|                                         | <p>deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric stack for each transistor, together with high quality silicon dioxide or oxynitride dielectric layers, problems associated with selective etching of the metal oxide may be avoided, as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:43-47:</p> <p>At this point, conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).</p> <p>For example, <i>Gilmer</i> discloses the following at Figure 4:</p> <div data-bbox="871 774 1663 1118"> <p style="text-align: center;"><b>FIG. 4</b></p> </div> <p>For example, <i>Gilmer</i> discloses the following at claim 1:</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>1. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;</p> <p>removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;</p> <p>forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and</p> <p>forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 14:</p> <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| U.S. Patent No. 7,923,779                                                                                                                                                                                                   | Exemplary Disclosures Relevant to <i>Gilmer</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                             | <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| <p>[1E] the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer</p> <p>For example, <i>Gilmer</i> discloses the following at 3:9-33:</p> <p>The resist mask 18 is then removed and a second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used. This second gate dielectric can be formed by thermal oxidation and/or chemical oxidation in accordance with conventional practices. The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers). Because second gate dielectric 20 is so thin, it may be difficult to adequately control the thickness or obtain an oxide of sufficient quality using thermal oxidation processes and therefore chemical oxidation may be useful. For instance, the thin dielectric may be formed by growing a thin oxide by rinsing the substrate in ozonated water. A combination of thermal and chemical treatment may also be used to form second dielectric 20. It may also be sufficient for second gate dielectric 20 to be a native oxide which is grown on substrate 12 as a</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| U.S. Patent No. 7,923,779 | Exemplary Disclosures Relevant to <i>Gilmer</i>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | <p>result of exposing the substrate to ambient or other oxygen containing environment. In other embodiments, second gate dielectric 20 can be deposited, e.g., by atomic layer deposition.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:44-4:7:</p> <p>Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with <math>k &gt; 4</math>, preferably with <math>k &gt; 6</math>, and most preferably with <math>k &gt; 7</math>) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (<math>\text{HfO}_2</math>), hafnium silicate (<math>\text{Hf}_x\text{Si}_y\text{O}_z</math>), or lanthanum aluminate (<math>\text{LaAlO}_3</math>), but lanthanum oxide, hafnium aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen so that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the substrate surface and thus one should use the thicknesses of the first and second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p>For example, <i>Gilmer</i> discloses the following at Abstract:</p> <p>A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

requirements, e.g. a core device region (22). First and second dielectrics are preferably silicon dioxide or oxynitride. A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric stack for each transistor, together with high quality silicon dioxide or oxynitride dielectric layers, problems associated with selective etching of the metal oxide may be avoided, as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.

For example, *Gilmer* discloses the following at 4:43-47:

At this point, conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).

For example, *Gilmer* discloses the following at Figure 4:

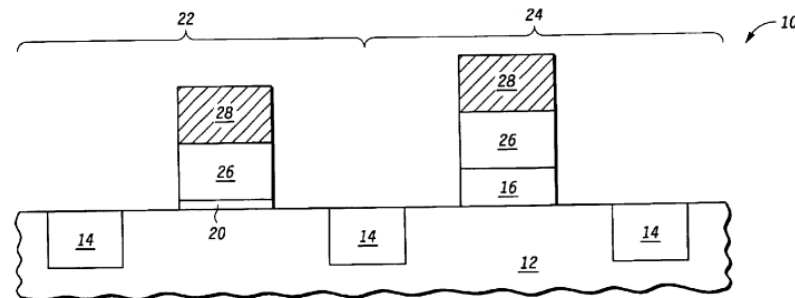


**FIG. 4**

For example, *Gilmer* discloses the following at claim 1:

1. A method for forming a semiconductor device comprising:  
providing a semiconductor substrate;

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;</p> <p>removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;</p> <p>forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and</p> <p>forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 14:</p> <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the</p> |
|--|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u>                                                                   | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                           | <p>references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <p>[1F] the first interface layer has a thickness larger than that of the second interface layer, and</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests the first interface layer has a thickness larger than that of the second interface layer</p> <p>For example, <i>Gilmer</i> discloses the following at 2:46-55:</p> <p style="padding-left: 40px;">After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30-50 Angstroms (3-5 nanometers).</p> <p>For example, <i>Gilmer</i> discloses the following at 2:60-65:</p> <p style="padding-left: 40px;">In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher voltages required for I/O functions.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:17-21:</p> <p style="padding-left: 40px;">The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers).</p> <p>For example, <i>Gilmer</i> discloses the following at 3:44-45:</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>Now that gate dielectrics of two different thicknesses have been formed ...</p> <p>For example, <i>Gilmer</i> discloses the following at Abstract:</p> <p>A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22).</p> <p>For example, <i>Gilmer</i> discloses the following at 1:14-32 in the “Background of the Invention”:</p> <p>In integrated circuit manufacturing, there is often a need to form transistors with different gate dielectric thicknesses on the same semiconductor substrate or wafer. For example, transistors for input/output (I/O) devices may require thicker gate dielectrics than, e.g., transistors used for the core logic. A conventional process for forming differing thickness is called a DGO process, which stands for Dual Gate Oxide. In a conventional DGO process, a “thick” silicon dioxide layer (e.g. for the I/O devices) is formed and a resist mask is used to mask the thick silicon dioxide layer in the I/O regions. The thick silicon dioxide layer is then etched away or otherwise removed from the unmasked region, where the core logic devices are to be formed. The mask is removed and a thin silicon dioxide layer is then grown over the core logic device region. The gate electrode material, typically polysilicon, is then deposited over the substrate, which at this point includes gate dielectrics of two different thicknesses. The gate electrode material and gate dielectrics are then patterned and etched to form the gate electrode and oxide stack of each transistor.</p> <p>For example, <i>Gilmer</i> discloses the following at Figure 4:</p> |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p><b>U.S. Patent No. 7,923,779</b></p> | <p><b><u>Exemplary Disclosures Relevant to <i>Gilmer</i></u></b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                                         | <div data-bbox="877 284 1659 581" data-label="Diagram"> </div> <p style="text-align: center;"><b>FIG. 4</b></p> <p>For example, <i>Gilmer</i> discloses the following at claim 1:</p> <ol style="list-style-type: none"> <li>1. A method for forming a semiconductor device comprising:<br/> providing a semiconductor substrate;<br/> forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;<br/> removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;<br/> forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and<br/> forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</li> </ol> <p>For example, <i>Gilmer</i> discloses the following at claim 14:</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u>                                                                                                      | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                              | <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p> |
| <p>[1G] each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.</p> | <p><i>Gilmer</i> alone or in combination with one or more references, discloses or suggests each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:46-55:</p> <p>After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

device region 24 as further explained below, but generally will be within a range of 30-50 Angstroms (3-5 nanometers).

For example, *Gilmer* discloses the following at 2:67-3:6:

Other dielectric materials may instead be used for first gate dielectric 16. Silicon dioxide and silicon oxynitride are attractive choices because of the industry's understanding of these materials, the ability to form high gate quality films, and because they can be formed by selective growth techniques rather than requiring blanket depositions and etch steps.

For example, *Gilmer* discloses the following at 3:10-14:

... a second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used.

For example, *Gilmer* discloses the following at Figure 4:

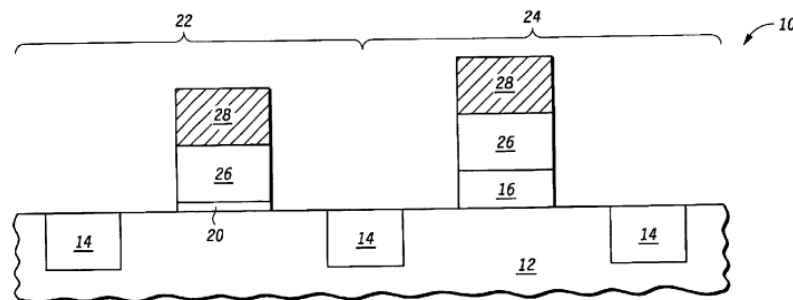


**FIG. 4**

For example, *Gilmer* discloses the following at Abstract:

First and second dielectrics are preferably silicon dioxide or oxynitride.

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <b><u>U.S. Patent No. 7,923,779</u></b>                                                                                                                       | <b><u>Exemplary Disclosures Relevant to <i>Gilmer</i></u></b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                               | <p>For example, <i>Gilmer</i> discloses the following at claims 2-3:</p> <p>2. The method of claim 1, wherein the first gate dielectric layer comprises a material selected from a group consisting of silicon oxide and silicon oxynitride.</p> <p>3. The method of claim 1, wherein the second gate dielectric layer comprises a material selected from a group consisting of silicon oxide and silicon oxynitride.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 15:</p> <p>15. The method of claim 14, wherein the first dielectric material comprises a material selected from a group consisting of silicon dioxide and silicon oxynitride.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p> |
| <b>Claim 12</b>                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <p>12. The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:47-54:</p> <p>In a preferred embodiment, this high-k dielectric is a metal oxide, such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (HfO<sub>2</sub>), hafnium silicate (Hf<sub>x</sub>Si<sub>y</sub>O<sub>z</sub>), or lanthanum aluminate (LaAlO<sub>3</sub>), but lanthanum oxide, hafnium</p>                                                                                                                                                                                                                                                                                                                                                                                                     |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <b><u>U.S. Patent No. 7,923,779</u></b>                                                                                                        | <b><u>Exemplary Disclosures Relevant to <i>Gilmer</i></u></b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                | <p>aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable high-k dielectrics.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 4:</p> <p>4. The method of claim 1, wherein the metal oxide layer comprises a material selected from a group consisting of hafnium dioxide, hafnium silicate, and lanthanum aluminate.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 17:</p> <p>17. The method of claim 16, wherein the metal oxide comprises a material selected from a group consisting of hafnium dioxide, hafnium silicate, and lanthanum, aluminate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p> |
| <b>Claim 13</b>                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| <p>13. The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests the first and second high dielectric constant insulating films are equal in thickness.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:54-4:7:</p> <p>The thickness of the high-k dielectric should be chosen so that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the</p>                                                                                                                                     |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

substrate surface and thus one should use the thicknesses of the first and second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.

For example, *Gilmer* discloses the following at Figure 4:

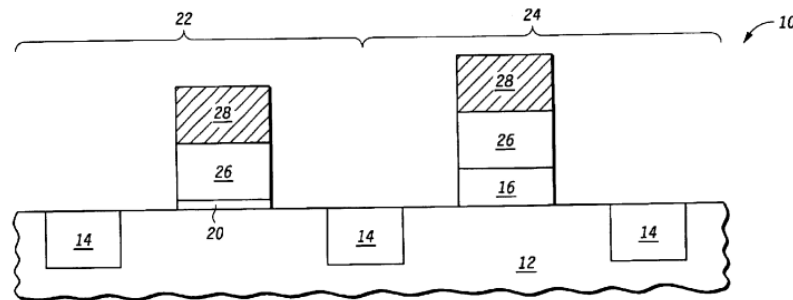


**FIG. 4**

For example, *Gilmer* discloses the following at Abstract:

A metal oxide (26) is deposited over both dielectrics, followed by deposition of a gate electrode material (28). By using a single metal oxide layer in forming the gate dielectric stack for each transistor, together with high quality silicon dioxide or oxynitride dielectric layers, problems associated with selective etching of the metal oxide may be avoided, as may problems associated with various interfaces between the metal oxide and damaged or treated surfaces.

For example, *Gilmer* discloses the following at claim 1:

1. A method for forming a semiconductor device comprising:

providing a semiconductor substrate;

forming a first gate dielectric layer overlying the semiconductor substrate, the first gate dielectric layer having a first thickness in a range of 30-50 Angstroms;

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>removing a portion of the first gate dielectric layer overlying a first region of the semiconductor substrate;</p> <p>forming a second gate dielectric layer overlying the first region of the semiconductor substrate, the second gate dielectric layer having a second thickness less than the first thickness; and</p> <p>forming a metal oxide layer overlying the first gate dielectric layer and the second gate dielectric layer.</p> <p>For example, <i>Gilmer</i> discloses the following at claim 14:</p> <p>14. A method for forming a semiconductor device comprising:</p> <p>providing a semiconductor substrate;</p> <p>forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p> |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u>                                                                                         | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|---------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Claim 14</b>                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <p>14. The semiconductor device of claim 1, wherein the first and second gate electrodes are made of an identical material.</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests the first and second gate electrodes are made of an identical material.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:35-43:</p> <p style="padding-left: 40px;">After metal oxide layer 26 has been deposited, a gate electrode material 28 is deposited over the metal oxide, and semiconductor device 10 is patterned and etched to form the gate stacks as shown in FIG. 4. Gate electrode material 28 will generally be conductive (doped) polysilicon or a metal (e.g. titanium nitride). Preferably the same etch mask is used to pattern gate stacks in both the I/O and core device regions, but etch requirements may make it more desirable to use two masks, one for each of the two regions.</p> <p>For example, <i>Gilmer</i> discloses the following at 4:43-47:</p> <p style="padding-left: 40px;">At this point, conventional processing occurs to complete the transistor and integrated circuit formation (e.g. implants, spacers, interlayer dielectrics, interconnects, and passivation formation).</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

For example, *Gilmer* discloses the following at Figure 4:

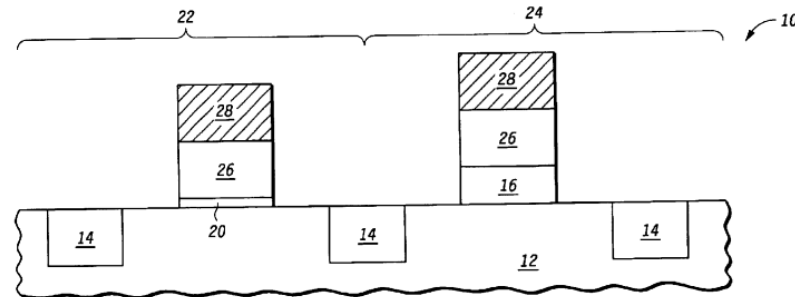


**FIG. 4**

For example, *Gilmer* discloses the following at claims 7-8:

7. The method of claim 1, further comprising:

forming a gate layer overlying the metal oxide layer and

patterning the gate layer, metal oxide layer, first gate dielectric layer, and second gate dielectric layer to form a first gate electrode stack and a second gate electrode stack.

8. The method of claim 7 wherein the first gate electrode stack is used in a core logic device and the second gate electrode stack is used in an I/O device.

For example, *Gilmer* discloses the following at claim 14:

14. A method for forming a semiconductor device comprising:

providing a semiconductor substrate;

forming a first dielectric material overlying the semiconductor substrate wherein a first portion of the first dielectric material overlying a first region of the semiconductor substrate has a first thickness and a second portion of the first dielectric material overlying a second region of the

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <b><u>U.S. Patent No. 7,923,779</u></b>                                                                                                                                                | <b><u>Exemplary Disclosures Relevant to <i>Gilmer</i></u></b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                                                                                                                                                                        | <p>semiconductor substrate has a second thickness different from the first thickness, and wherein the first thickness is in a range of 30 to 50 Angstroms;</p> <p>forming a high-k dielectric layer overlying the first dielectric material;</p> <p>forming a gate layer overlying the high-k dielectric layer, and</p> <p>patterning the gate layer and the high-k dielectric layer to form a gate of a first device within the first region of the semiconductor substrate and a gate of a second device within the second region of the semiconductor substrate.</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.</p>                             |
| <b>Claim 15</b>                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| <p>15. The semiconductor device of claim 1, wherein an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.</p> | <p><i>Gilmer</i>, alone or in combination with one or more references, discloses or suggests an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor, according to the '779 Patent.</p> <p>For example, <i>Gilmer</i> discloses the following at 2:46-55:</p> <p style="padding-left: 40px;">After forming trench isolation regions 14, a first gate dielectric 16 is formed over substrate 12. First gate dielectric 16 is preferably silicon dioxide or silicon oxynitride, and is preferably formed by thermal oxidation in accordance with conventional practices. The thickness of gate dielectric 16 is determined by the particular device requirements for devices to be formed in I/O device region 24 as further explained below, but generally will be within a range of 30-50 Angstroms (3-5 nanometers).</p> <p>For example, <i>Gilmer</i> discloses the following at 2:60-65:</p> |

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>In operation, devices to be formed in core device region 22 require thinner gate dielectrics that operate at lower voltages than, e.g., I/O devices to be formed in I/O device region 24 that can withstand higher voltages required for I/O functions.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:9-33:</p> <p>The resist mask 18 is then removed and a second gate dielectric 20 is formed on exposed portions of substrate 12 within the core device region 22. In a preferred embodiment, second gate dielectric 20 is also silicon dioxide or silicon oxynitride, but like first gate dielectric 16 other materials could be used. This second gate dielectric can be formed by thermal oxidation and/or chemical oxidation in accordance with conventional practices. The thickness of gate dielectric 20 is also determined by the particular device requirements for devices to be formed in core device region 22 as further explained below, but generally will be within a range of 4-12 Angstroms (0.4-1.2 nanometers). Because second gate dielectric 20 is so thin, it may be difficult to adequately control the thickness or obtain an oxide of sufficient quality using thermal oxidation processes and therefore chemical oxidation may be useful. For instance, the thin dielectric may be formed by growing a thin oxide by rinsing the substrate in ozonated water. A combination of thermal and chemical treatment may also be used to form second dielectric 20. It may also be sufficient for second gate dielectric 20 to be a native oxide which is grown on substrate 12 as a result of exposing the substrate to ambient or other oxygen containing environment. In other embodiments, second gate dielectric 20 can be deposited, e.g., by atomic layer deposition.</p> <p>For example, <i>Gilmer</i> discloses the following at 3:44-4:7:</p> <p>Now that gate dielectrics of two different thicknesses have been formed, a high-k dielectric (generally with <math>k &gt; 4</math>, preferably with <math>k &gt; 6</math>, and most preferably with <math>k &gt; 7</math>) is deposited over semiconductor device 10. In a preferred embodiment, this high-k dielectric is a metal oxide, such as metal oxide 26 shown in FIG. 3. Suitable materials for metal oxide 26 preferably include hafnium oxide (<math>\text{HfO}_2</math>), hafnium silicate (<math>\text{Hf}_x\text{Si}_y\text{O}_z</math>), or lanthanum aluminate (<math>\text{LaAlO}_3</math>), but lanthanum oxide, hafnium aluminate, zirconium oxide, and zirconium silicate, and other like materials, may also be suitable high-k dielectrics. The thickness of the high-k dielectric layer will be dependent on the particular device requirements in each region of the substrate (the core region and the I/O region), but generally it is believed the thickness of a metal oxide will be</p> |
|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**EXHIBIT 779-01: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Gilmer**

| <u><b>U.S. Patent No. 7,923,779</b></u> | <u><b>Exemplary Disclosures Relevant to <i>Gilmer</i></b></u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                         | <p>between about 15-50 angstroms (1.5-5.0 nanometers). The underlying thicknesses of first gate dielectric 16 and second gate dielectric 20 will also affect the choice of thickness of the high-k dielectric. The thickness of the high-k dielectric should be chosen so that its equivalent oxide thickness (EOT), when added to the EOT of the first gate dielectric 16 (I/O device dielectric) thickness or second gate dielectric 20 (core device dielectric) thickness, provides a total EOT appropriate for the I/O and core device, respectively. Similarly, this calculation should be used to determine the initial deposited or grown thicknesses of the first and second gate dielectrics. Because metal oxide 26 is deposited as a single blanket deposition, its thickness will not vary much across the substrate surface and thus one should use the thicknesses of the first and second dielectrics as the “variables” to achieve the final EOTs for the core and I/O devices.</p> <p>For example, <i>Gilmer</i> discloses the following at Abstract:</p> <p>A semiconductor device (10) having two different gate dielectric thicknesses is formed using a single high-k dielectric layer, preferably a metal oxide. A thicker first gate dielectric (16) is formed in a region of the device for higher voltage requirements, e.g. an I/O region (24). A thinner second gate dielectric (20) is formed in a region of the device for lower voltage requirements, e.g. a core device region (22).</p> <p>To the extent that <i>Gilmer</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Gilmer</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-02 through 779-17 for the reasons discussed herein and in Defendant’s cover pleading.</p> |