

EXHIBIT 779-03: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Torii

The following illustrates certain grounds for invalidity based on:

- U.S. Patent 6,881,657 to Torii et al. (“*Torii*”) was filed on July 13, 2004 and issued on April 19, 2005. *Torii* claims priority to JP2003-197954 filed on July 16, 2003. Accordingly, *Torii* constitutes prior art to U.S. Patent No. 8,796,779 (the “’779 patent”) under at least pre-AIA 35 U.S.C. §102(b).

Torii, including any material incorporated by reference into *Torii*, anticipates claims 1 and 12-15 (the “asserted claims”) of the ’779 patent under pre-AIA 35 U.S.C. §102(b).

To the extent any limitation is found not to be expressly or inherently disclosed in *Torii*, such a limitation would have been obvious either based on *Torii* alone, given the state of the art, or in combination with one or more of the references cited in Exhibits 779-01, 779-02 and 779-04 through 779-17, because the ’779 patent is merely a collection of prior art elements that fails to meet the statutory requirement of non-obviousness under 35 U.S.C. § 103, and the factors delineated in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), weigh against a finding of non-obviousness.

In particular, any disclosures identified for each limitation of the ’779 patent in the aforementioned Exhibits may be combined with the disclosures of *Torii* identified below for the same limitation to render that limitation obvious. A POSITA would have found such a combination / modification obvious for the reasons discussed herein and in Defendant’s cover pleading.¹

The citations to portions of any reference in this chart are exemplary only. Citations to the written description should be interpreted to include the figures associated with or relevant to the cited passages. Similarly, citations to a figure should be understood to encompass any description, text, or discussion of that figure. Defendant reserves the right to use the entirety of any reference cited in this chart to

¹ Plaintiff appears in many instances to be pursuing overly broad constructions of limitations of the asserted claims in an effort to piece together an infringement claim where none exists. This claim chart accounts for overly broad construction of the claim limitations. Any assertion that a particular limitation is disclosed by a prior art reference or references may be based on Plaintiff’s apparent constructions and is not intended to be, and is not, an admission that such constructions are supportable or proper. Defendant is investigating this prior art and has not yet completed discovery from third parties, who may have relevant information concerning the prior art. Therefore, Defendant reserves the right to supplement this chart after additional discovery is received. To the extent that any of the prior art discloses the same or similar functionality or feature(s) of any of the accused products, Defendant reserves the right to argue that said feature or functionality does not practice any limitation of any of the asserted claims, and to argue, in the alternative, that if said feature or functionality is found to practice any limitation of any of the asserted claims, then the prior art reference teaches the limitation and that the claim is not patentable.

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show that the asserted claims are anticipated and/or are obvious. Citations presented for one claim limitation are expressly incorporated by reference into all other limitations for that claim as well as all limitations of all claims on which that claim depends.

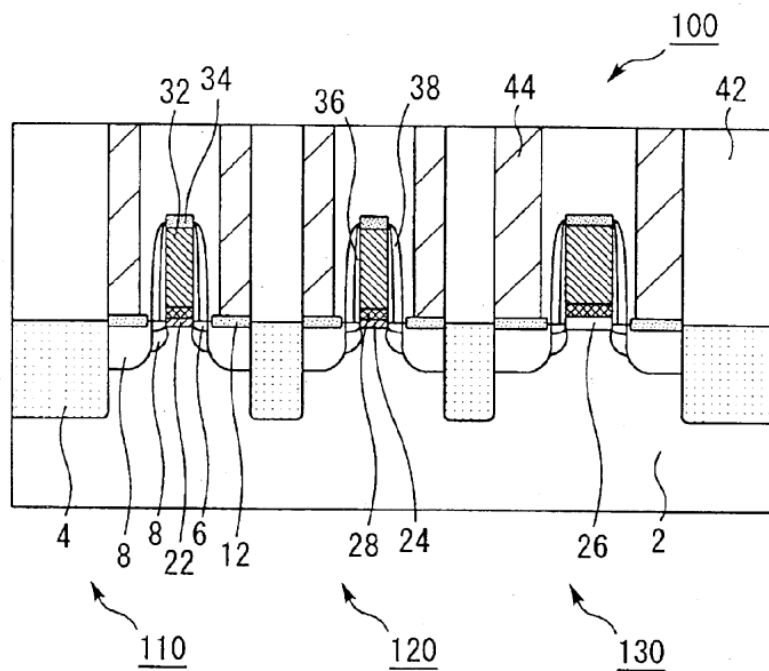
<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
Claim 1	
[1pre] A semiconductor device comprising:	Torii, alone or in combination with one or more references, discloses or suggests a semiconductor device. For example, <i>Torii</i> discloses the following at Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE For example, <i>Torii</i> discloses the following at Abstract: In a method for forming a semiconductor device, the major surface of a substrate is separated into a first element region for forming a first field-effect transistor and a second element region for forming a second field-effect transistor. A silicon nitride film is formed in each of the first and second element regions. Thereafter, the silicon nitride film formed in the second element region is removed, and the substrate is subjected to heat treatment in an ambient that contains nitrogen oxide. Thereby, the silicon nitride film in the first element region is oxidized to form an oxynitride film, and a silicon oxynitride film is formed in the second element region. Thereafter, a high-dielectric-constant film is formed on the silicon oxynitride films in each of the first and second element regions. For example, <i>Torii</i> discloses the following at 1:9-14: The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device. More specifically, the present invention relates to a semiconductor device

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	having a plurality of transistors comprising gate insulating films of different film thickness, and a method for manufacturing such a semiconductor device. For example, <i>Torii</i> discloses the following at 3:54-61: Therefore, the present invention proposes the solution of the above-described problems, and it is the object of the present invention to provide a semiconductor device wherein gate insulating films highly controlled their thickness are formed when a plurality of transistors are formed on a chip, even if the difference between the thickness of the gate insulating films is small, and to provide a method for manufacturing such a semiconductor device. For example, <i>Torii</i> discloses the following at 3:62-65: According to one aspect of the present invention, a semiconductor device comprises a substrate, and a first field-effect transistor and a second field-effect transistor formed on the substrate. For example, <i>Torii</i> discloses the following at 4:10-14: According to another aspect of the present invention, in a method for manufacturing a semiconductor device, the major surface of a substrate is separated into a first element region for forming a first field-effect transistor and a second element region for forming a second field-effect transistor. For example, <i>Torii</i> discloses the following at 4:30-32, 4:58-60: FIG. 1 is a schematic sectional view for illustrating an SoC (system on chip) 100 according to the first embodiments of the present invention. For example, <i>Torii</i> discloses the following at Figure 1:

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FIG. 1



For example, *Torii* discloses the following in claim 1:

1. A semiconductor device comprising;

For example, *Torii* discloses the following in claim 9:

9. A method for manufacturing a semiconductor device comprising:

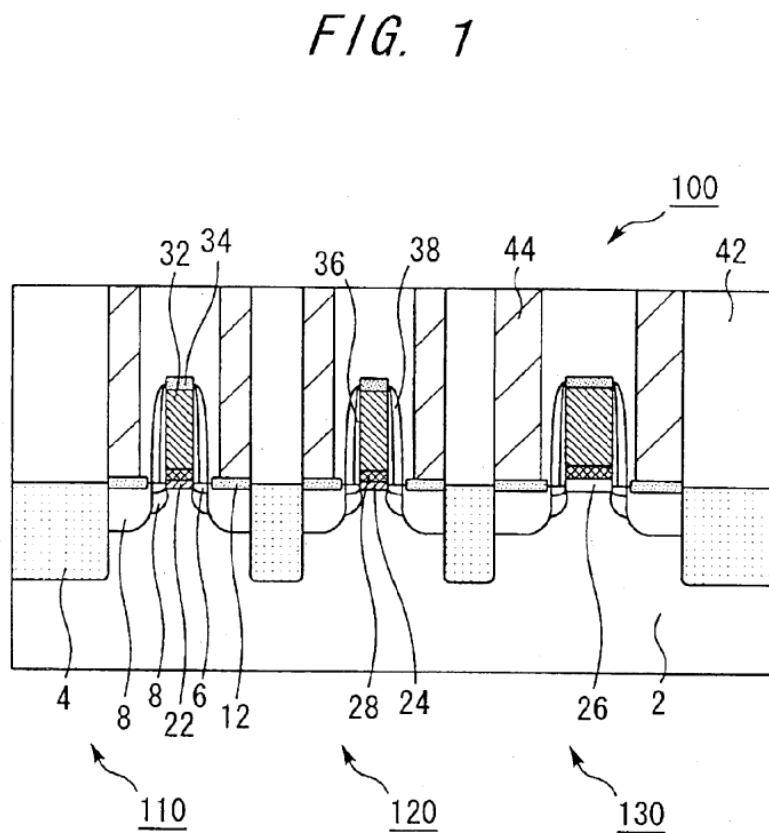
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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	To the extent that <i>Torii</i> is found not to disclose the preamble, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
[1A] a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate,	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests a first MIS transistor and a second MIS transistor of an identical conductivity type provided on an identical semiconductor substrate. For example, <i>Torii</i> discloses the following at 3:62-65: According to one aspect of the present invention, a semiconductor device comprises a substrate, and a first field-effect transistor and a second field-effect transistor formed on the substrate. For example, <i>Torii</i> discloses the following at 4:61-67: As FIG. 1 shows, the SoC 100 is composed of a MISFET (metal insulator semiconductor field effect transistor) 110 for LOP (low operating power) (hereafter referred to as MISFET for LOP 110); an MISFET 120 for LSTP (low stand-by power) (hereafter referred to as MISFET for LSTP 120); and an MISFET 130 for high withstand voltage (hereafter referred to as MISFET for high withstand voltage 130). For example, <i>Torii</i> discloses the following at 5:1-4: The MISFETs for LOP 110, for LSTP 120, and for high withstand voltage 130 are formed in regions of an Si substrate 2 isolated by STI (shallow trench isolation) 4, respectively. For example, <i>Torii</i> discloses the following at 6:14-18:

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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	First, an STI 4 is formed on an Si substrate 2, and the Si substrate 2 is divided into a region for forming an MISFET for LOP 110, a region for forming an MISFET for LSTP120, and a region for forming an MISFET for high withstand voltage 130. For example, <i>Torii</i> discloses the following at 7:6-12: Next, a non-doped polycrystalline silicon film 54 is formed on the high-k film 28 (Step S16). The non-doped polycrystalline silicon film 54 is a material film for gate electrodes 32, and here, it is deposited to have a thickness of about 120 nm. Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54 (Step S17). For example, <i>Torii</i> discloses the following at 10:39-42: Furthermore, in the first embodiment, the case wherein an n-type transistor is formed is described. However, the present invention may be applied to the case wherein a p-type transistor is formed. For example, <i>Torii</i> discloses the following at Figure 1:

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For example, *Torii* discloses the following in claim 1:

a substrate,

a first field-effect transistor, including a first gate insulating film and a first gate electrode, on the major surface of said substrate, and

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	a second field-effect transistor, including a second gate insulating film and a second gate electrode, on the major surface of said substrate, wherein For example, <i>Torii</i> discloses the following in claim 9: 9. A method for manufacturing a semiconductor device comprising: separating a major surface of a substrate into a first element region for forming a first field-effect transistor and a second element region for forming a second field-effect transistor, For example, <i>Torii</i> discloses the following at 1:16-39 in its discussion of “Background Art”: Concurrent with the advance of the down-sizing technology of semiconductor integrated circuits in recent years, the dimension of an element has been reduced, and a larger number of elements have been able to be mounted in a chip. Therefore, an integrated-circuit device referred to as SoC (system on chip) that can individually realize functions conventionally realized using a plurality of element has been widely used. In the logic circuit portion of an SoC, it is required to lower the driving voltage for reducing power consumption. At the same time, in order to prevent the lowering of the driving current due to the reduction of the driving voltage, the thickness of the gate insulating film of an MOSFET (metal oxide semiconductor field effect transistor) has been reduced. On the other hand, the MOSFET used in the peripheral circuit portions accompanying inputs and outputs must be directly driven by an external voltage. Therefore, a high withstand voltage is required in the MOSFET used in the peripheral circuit portions, and a gate insulating film having a large film thickness to some extent is required. For example, a thick gate insulating film having a thickness of about 6.0 nm to 10 nm has been used in a high-withstand-voltage 3.3V MOSFET. For example, <i>Torii</i> discloses the following at 2:51-65 in its discussion of “Background Art”: MISFETs used in the logic circuit portion of SoC are classified into a low operating power (LOP) version that requires relatively high-speed operation, a low stand-by power (LSTP) version, and the like. Some SoC use either an MISFET for LOP or an MISFET for LSTP in the
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	logic circuit portion, and an MISFET for a high withstand voltage in the peripheral circuit portion. In recent years, however, the number of semiconductor devices using both MISFETs for LOP and LSTP in the logic circuit portion, and an MISFET for a high withstand voltage in the peripheral circuit portion is increasing. Such semiconductor devices are useful when used in mobile phones or the like, which require both the operation speed for a long time operated by batteries and high performance, and the demand for such semiconductor devices will further be increased in future. To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
[1B] wherein the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film,	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests the first MIS transistor includes a first gate insulating film formed on a first active region in the semiconductor substrate and a first gate electrode formed on the first gate insulating film. For example, <i>Torii</i> discloses the following at 4:1-4: Each of the first gate insulating film and the second gate insulating film includes a silicon oxynitride film and a high-dielectric constant film. For example, <i>Torii</i> discloses the following at 5:1-4: The MISFETs for LOP 110, for LSTP 120, and for high withstand voltage 130 are formed in regions of an Si substrate 2 isolated by STI (shallow trench isolation) 4, respectively For example, <i>Torii</i> discloses the following at 5:5-13: On each region of the Si substrate 2 isolated by STI 4, a source-drain extension 6, which is a diffusion layer having a relatively shallow junction and a low impurity content is formed, and a

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	punch-through stopper 8 is formed underneath the source-drain extension 6. Outside each source-drain extension 6, a source-drain region 10, which is a diffusion layer having a relatively deep junction and a high impurity content is formed. On each source-drain region 10, a nickel silicide (NiSi) layer 12 is formed. For example, <i>Torii</i> discloses the following at 5:14-18: In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. For example, <i>Torii</i> discloses the following at 5:33-41: On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO₂) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed. For example, <i>Torii</i> discloses the following at 5:42-49: On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 μm. For example, <i>Torii</i> discloses the following at 5:62-6:6: Specifically, the MISFET for LOP 110 is a low-power-consumption transistor included the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film

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	having a reduced EOT. The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film, controlling the EOT to be low to some extent, and sufficiently securing the effective film thickness. The MISFET for high withstand voltage 130 is a high-withstand-voltage transistor securing the thickness of the thermal oxide film so as to withstand the external high voltage. For example, <i>Torii</i> discloses the following at 6:14-23: First, an STI 4 is formed on an Si substrate 2, and the Si substrate 2 is divided into a region for forming an MISFET for LOP 110, a region for forming an MISFET for LSTP 120, and a region for forming an MISFET for high withstand voltage 130. For the simplicity of the following description, the region for forming an MISFET for LOP 110 is referred to as the region for LOP, the region for forming an MISFET for LSTP 120 is referred to as the region for LSTP, and the region for forming an MISFET for high withstand voltage 130 is referred to as the region for high withstand voltage. For example, <i>Torii</i> discloses the following at 6:24-27: The implantation of p-type ions for controlling the impurity content in the substrate, heat treatment the impurity diffusion, ion implantation for controlling the threshold voltage, and heat treatment for activation are performed.
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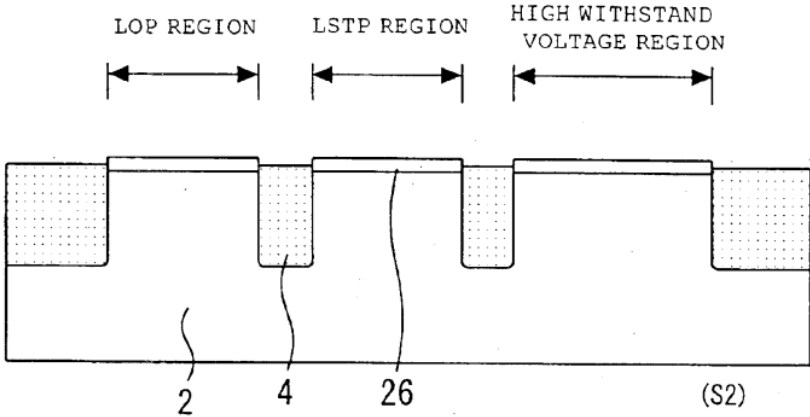
U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	<i>FIG. 3</i>  For example, <i>Torii</i> discloses the following at 6:55-63: Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 mm. At this time, the nitrogen content in the Silicon oxynitride film 22 in the region for LOP is about 15

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	to 20%, and the nitrogen content in the Silicon oxynitride film 24 in the region for LSTP is about 9%. For example, <i>Torii</i> discloses the following at 6:66-7:5: Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700° C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14). For example, <i>Torii</i> discloses the following at 7:6-22: Next, a non-doped polycrystalline silicon film 54 is formed on the high-k film 28 (Step S16). The non-doped polycrystalline silicon film 54 is a material film for gate electrodes 32, and here, it is deposited to have a thickness of about 120 nm. Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54 (Step S17). Next, as FIG. 8 shows, the polycrystalline silicon film 54 is processed for a gate electrode 32 of each region (Step S18). Here, a resist mask of a width of the gate electrode is formed on the polycrystalline silicon film 54 using a conventional method, and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width of the gate electrode 32. Thereby, a gate electrode 32 and a gate insulating film are formed in each of the regions for LOP, LSTP, and high withstand voltage.
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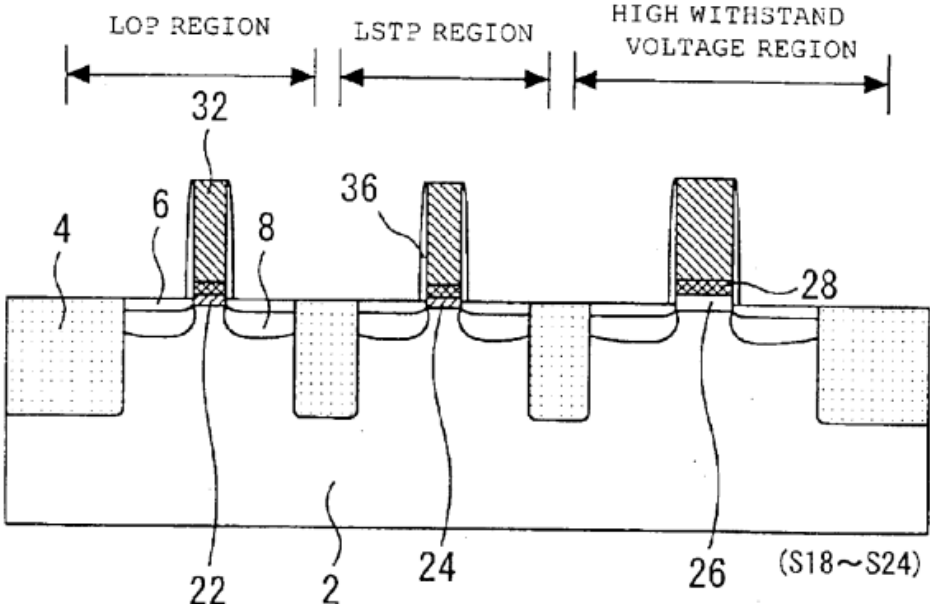
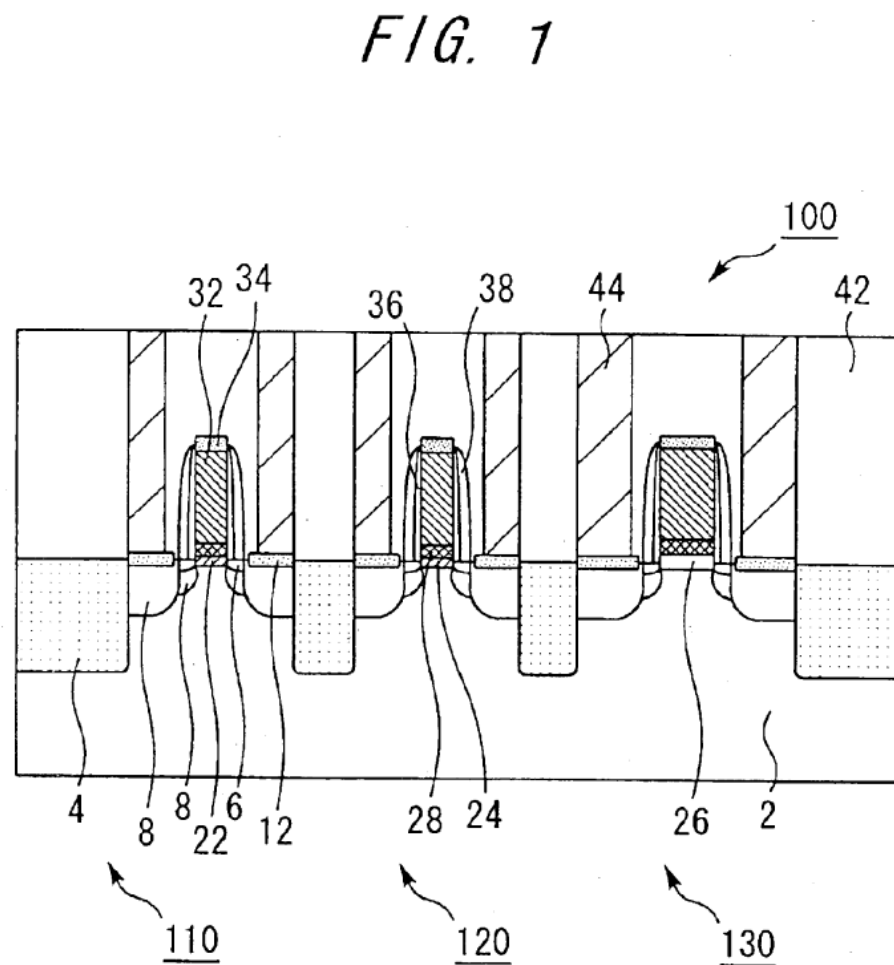
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	<i>FIG. 8</i>  For example, <i>Torii</i> discloses the following at 8:14-23: According to the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of such a structure enables a highly

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	reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip. For example, <i>Torii</i> discloses the following at 9:32-38: Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the semiconductor devices can be improved For example, <i>Torii</i> discloses the following at 12:13-21: In one aspect of the present invention, a laminate film of a silicon oxynitride film and a high-k film is used as each gate insulating film of a plurality of transistors formed on a substrate. The thickness of the high-k film in each gate insulating film is equalized, and the thickness of silicon oxynitride films is differentiated. Thereby, even if the thickness of the gate insulating films is slightly different, a semiconductor device of highly controlled film thickness can be realized. For example, <i>Torii</i> discloses the following at 10:34-38: In the first embodiment, the case wherein a non-doped polycrystalline silicon film is used as the material for the gate electrode 32 is described. However, in the present invention, the material for the gate electrode 32 may be other material. For example, <i>Torii</i> discloses the following at Figure 1:
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For example, *Torii* discloses the following in claim 1:

a substrate,

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	a first field-effect transistor, including a first gate insulating film and a first gate electrode, on the major surface of said substrate, and a second field-effect transistor, including a second gate insulating film and a second gate electrode, on the major surface of said substrate, wherein To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
[1C] the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film,	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests the second MIS transistor includes a second gate insulating film formed on a second active region in the semiconductor substrate and a second gate electrode formed on the second gate insulating film For example, <i>Torii</i> discloses the following at 4:1-4: Each of the first gate insulating film and the second gate insulating film includes a silicon oxynitride film and a high-dielectric constant film. For example, <i>Torii</i> discloses the following at 5:1-4: The MISFETs for LOP 110, for LSTP 120, and for high withstand voltage 130 are formed in regions of an Si substrate 2 isolated by STI (shallow trench isolation) 4, respectively For example, <i>Torii</i> discloses the following at 5:5-13: On each region of the Si substrate 2 isolated by STI 4, a source-drain extension 6, which is a diffusion layer having a relatively shallow junction and a low impurity content is formed, and a punch-through stopper 8 is formed underneath the source-drain extension 6. Outside each source-drain extension 6, a source-drain region 10, which is a diffusion layer having a relatively

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	deep junction and a high impurity content is formed. On each source-drain region 10, a nickel silicide (NiSi) layer 12 is formed. For example, <i>Torii</i> discloses the following at 5:14-18: In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. For example, <i>Torii</i> discloses the following at 5:33-41: On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO₂) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed. For example, <i>Torii</i> discloses the following at 5:42-49: On each high-k film 28, a gate electrode 32 is formed. The surface of the gate electrode 32 is silicided, thereby a nickel silicide layer 34 is formed. The gate length of the gate electrode 32 in the MISFET for LOP 100 is about 35 nm, and the gate length of the gate electrode 32 in the MISFET for LSTP 120 is about 50 nm. The gate length of the gate electrode 32 in the MISFET for high withstand voltage 130 is about 0.4 μm. For example, <i>Torii</i> discloses the following at 5:62-6:6: Specifically, the MISFET for LOP 110 is a low-power-consumption transistor included the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film having a reduced EOT. The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film, controlling the EOT to be low to some extent, and sufficiently securing the effective film
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	thickness. The MISFET for high withstand voltage 130 is a high-withstand-voltage transistor securing the thickness of the thermal oxide film so as to withstand the external high voltage. For example, <i>Torii</i> discloses the following at 6:14-23: First, an STI 4 is formed on an Si substrate 2, and the Si substrate 2 is divided into a region for forming an MISFET for LOP 110, a region for forming an MISFET for LSTP 120, and a region for forming an MISFET for high withstand voltage 130. For the simplicity of the following description, the region for forming an MISFET for LOP 110 is referred to as the region for LOP, the region for forming an MISFET for LSTP 120 is referred to as the region for LSTP, and the region for forming an MISFET for high withstand voltage 130 is referred to as the region for high withstand voltage. For example, <i>Torii</i> discloses the following at 6:24-27: The implantation of p-type ions for controlling the impurity content in the substrate, heat treatment the impurity diffusion, ion implantation for controlling the threshold voltage, and heat treatment for activation are performed.
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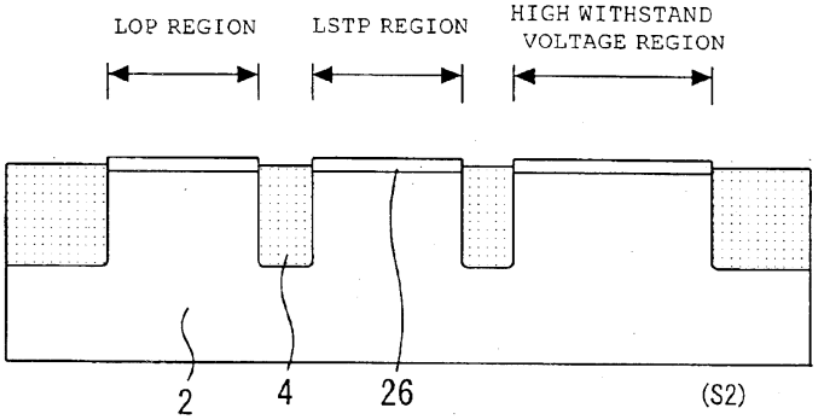
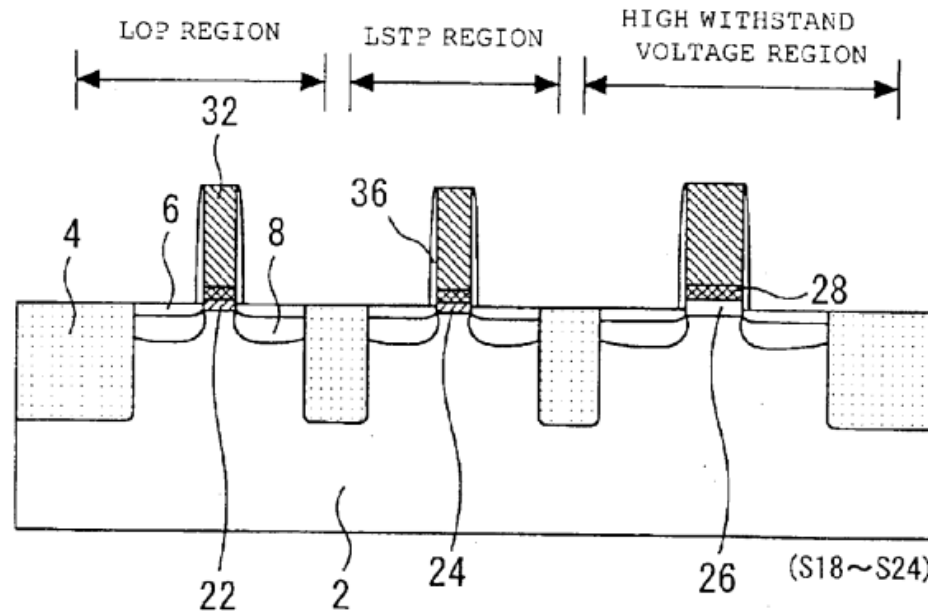
U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	<i>FIG. 3</i>  For example, <i>Torii</i> discloses the following at 6:55-63: Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 mm. At this time, the nitrogen content in the Silicon oxynitride film 22 in the region for LOP is about 15

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	to 20%, and the nitrogen content in the Silicon oxynitride film 24 in the region for LSTP is about 9%. For example, <i>Torii</i> discloses the following at 6:66-7:5: Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700° C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14). For example, <i>Torii</i> discloses the following at 7:6-22: Next, a non-doped polycrystalline silicon film 54 is formed on the high-k film 28 (Step S16). The non-doped polycrystalline silicon film 54 is a material film for gate electrodes 32, and here, it is deposited to have a thickness of about 120 nm. Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54 (Step S17). Next, as FIG. 8 shows, the polycrystalline silicon film 54 is processed for a gate electrode 32 of each region (Step S18). Here, a resist mask of a width of the gate electrode is formed on the polycrystalline silicon film 54 using a conventional method, and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width of the gate electrode 32. Thereby, a gate electrode 32 and a gate insulating film are formed in each of the regions for LOP, LSTP, and high withstand voltage.
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FIG. 8



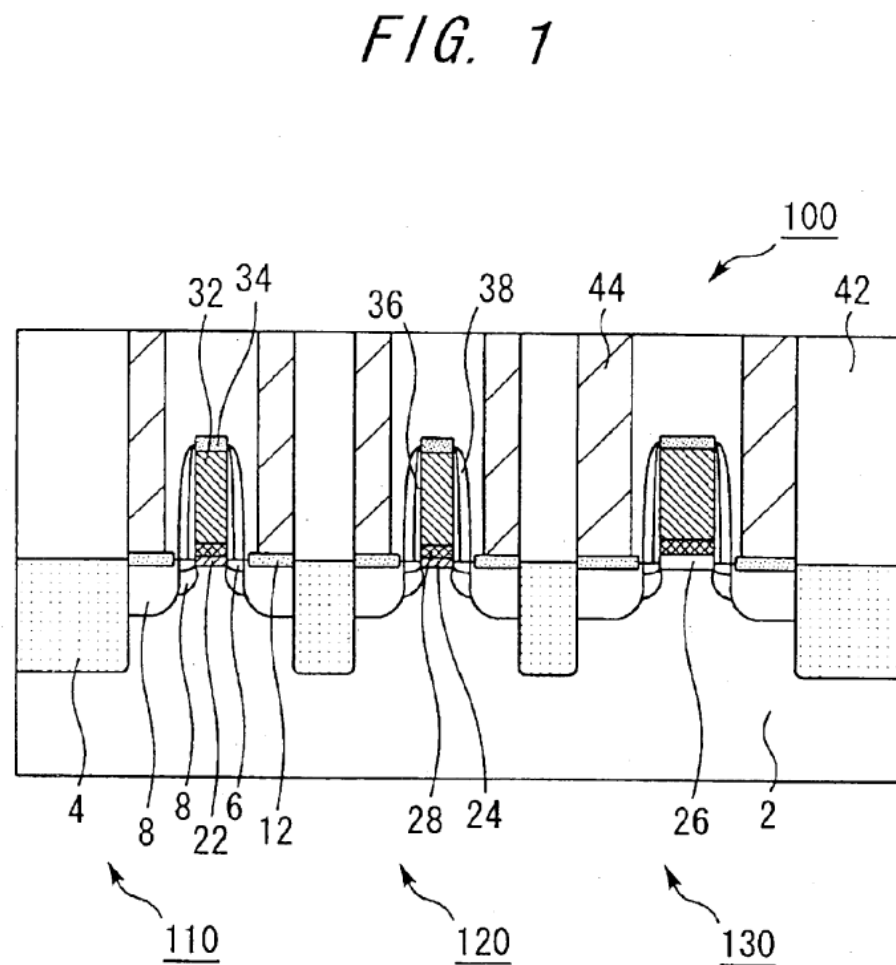
For example, *Torii* discloses the following at 8:14-23:

According to the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film **28** is deposited on silicon oxynitride films **22** and **24** as the gate insulating film of MISFETs **110** and **120** for LOP and LSTP, respectively. Here, by the use of the silicon oxynitride films **22** and **24**, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.

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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	For example, <i>Torii</i> discloses the following at 9:32-38: Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the semiconductor devices can be improved For example, <i>Torii</i> discloses the following at 12:13-21: In one aspect of the present invention, a laminate film of a silicon oxynitride film and a high-k film is used as each gate insulating film of a plurality of transistors formed on a substrate. The thickness of the high-k film in each gate insulating film is equalized, and the thickness of silicon oxynitride films is differentiated. Thereby, even if the thickness of the gate insulating films is slightly different, a semiconductor device of highly controlled film thickness can be realized. For example, <i>Torii</i> discloses the following at 10:34-38: In the first embodiment, the case wherein a non-doped polycrystalline silicon film is used as the material for the gate electrode 32 is described. However, in the present invention, the material for the gate electrode 32 may be other material. For example, <i>Torii</i> discloses the following at Figure 1:

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For example, *Torii* recites the following in claim 1:

substrate,

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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	a first field-effect transistor, including a first gate insulating film and a first gate electrode, on the major surface of said substrate, and a second field-effect transistor, including a second gate insulating film and a second gate electrode, on the major surface of said substrate, wherein To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
[1D] the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer,	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests the first gate insulating film includes a first interface layer being in contact with the semiconductor substrate and a first high dielectric constant insulating film formed on the first interface layer. For example, <i>Torii</i> discloses the following at 4:1-4: Each of the first gate insulating film and the second gate insulating film includes a silicon oxynitride film and a high-dielectric constant film. For example, <i>Torii</i> discloses the following at 5:14-29: In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally-oxidized (SiO₂) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm; and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is

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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest. For example, <i>Torii</i> discloses the following at 5:33-41: On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO₂) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed. For example, <i>Torii</i> discloses the following at 6:28-65: On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (Step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (Step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed. Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (Step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6 nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide films 26 is also simultaneously nitrified. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (Step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed.

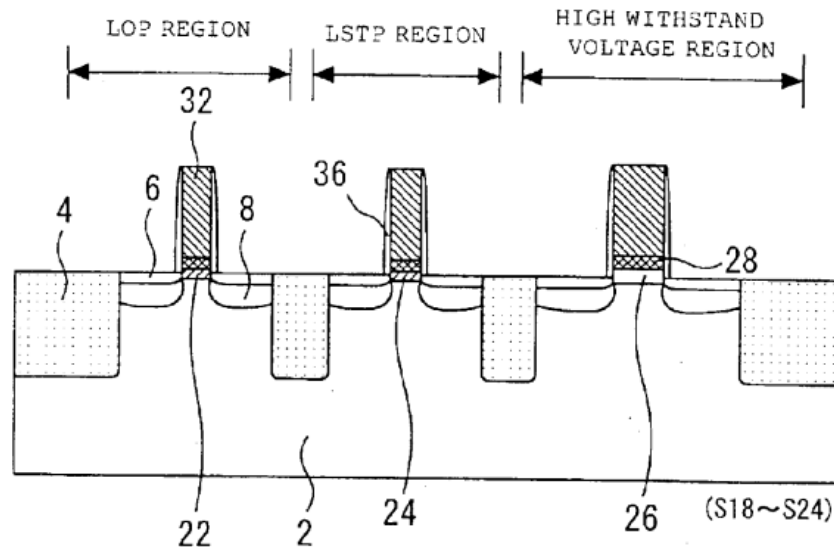
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U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900° C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrided to form a silicon oxynitride film. For example, <i>Torii</i> discloses the following at 6:66-7:5: Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700° C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14). For example, <i>Torii</i> discloses the following at 8:14-23: According to the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of such a structure enables a highly

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reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.

FIG. 8



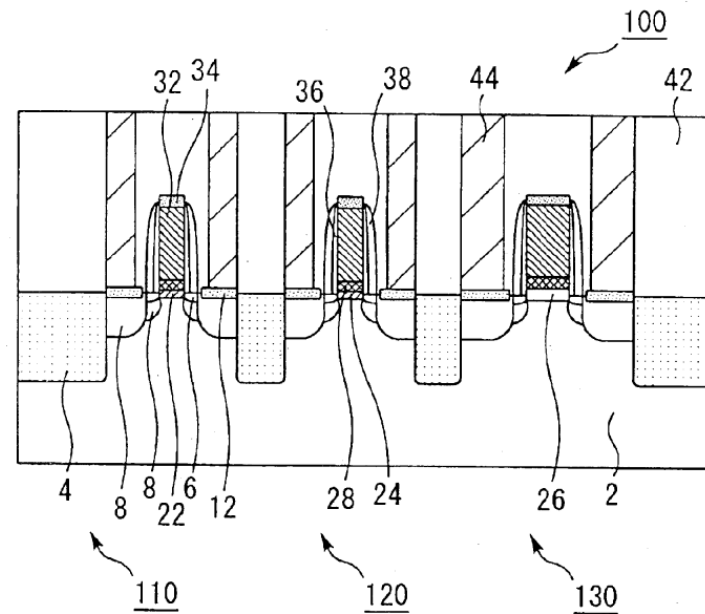
For example, *Torii* discloses the following at 9:32-38:

Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the semiconductor devices can be improved.

For example, *Torii* discloses the following at Figure 1:

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FIG. 1



For example, *Torii* discloses the following at Figure 6:

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	<i>FIG. 6</i> For example, <i>Torii</i> discloses the following in claim 1: each of said first gate insulating film and said second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film For example, <i>Torii</i> discloses the following at 2:28-49 in its discussion of “Background Art”: Therefore, in order to produce finer elements and reduce power consumption, the use of a high-dielectric-constant film (hereafter referred to as high-k film) as a gate insulating film has been studied. The high-k film can be formed thicker than the silicon oxide film, while maintaining the

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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	effective film thickness that determines the transistor current sufficiently thin, and can inhibit the increase of power consumption. As such an SoC, there has been proposed a semiconductor device that uses a high-k film as the gate insulating film of an MISFET (metal insulator semiconductor field effect transistor) for the logic circuit, and a thick silicon oxide film and a high-k film as the gate insulating film for the peripheral circuit. When this semiconductor device is formed, a silicon oxide film is first formed on the entire surface of a substrate using an ordinary method. Thereafter, the silicon oxide film in the region for forming the MISFET for the logic circuit is removed, and then, a high-k film is formed on the entire surface using a CVD method or the like. Thereby, the gate insulating films having different thickness between the peripheral circuit side and the logic circuit side can be formed ... To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
[1E] the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer,	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests the second gate insulating film includes a second interface layer being in contact with the semiconductor substrate and a second high dielectric constant insulating film formed on the second interface layer. For example, <i>Torii</i> discloses the following at 5:14-29: In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally-oxidized (SiO₂) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The

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U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm; and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest. For example, <i>Torii</i> discloses the following at 5:33-41: On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO₂) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed. For example, <i>Torii</i> discloses the following at 6:28-65: On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (Step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (Step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed. Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (Step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6 nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide films 26 is also simultaneously nitrided. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (Step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet

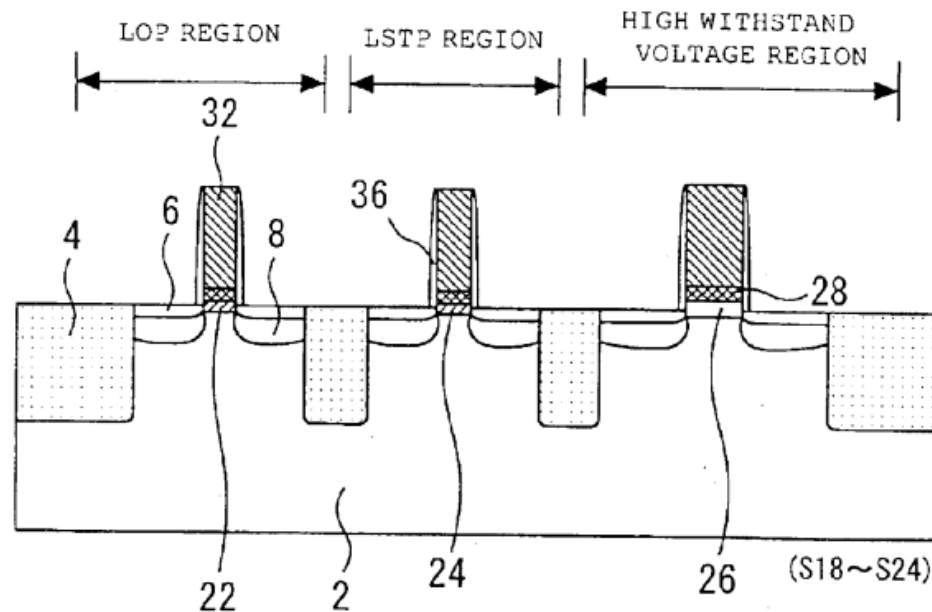
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U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed. Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900° C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrided to form a silicon oxynitride film. For example, <i>Torii</i> discloses the following at 6:66-7:5: Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700° C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14). For example, <i>Torii</i> discloses the following at 8:14-23: According to the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of such a structure enables a highly

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reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip.

FIG. 8



For example, *Torii* discloses the following at 9:32-38:

Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the semiconductor devices can be improved.

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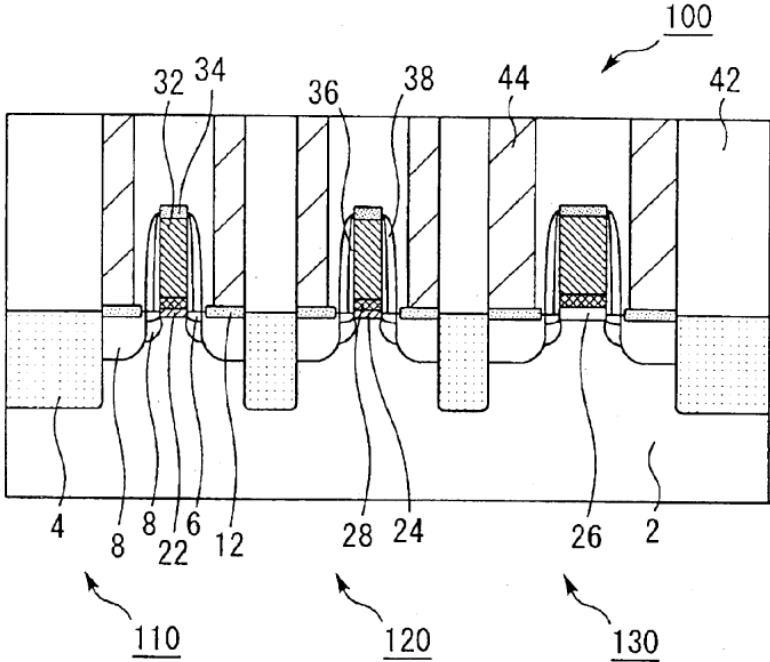
U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	For example, <i>Torii</i> discloses the following at Figure 1: <i>FIG. 1</i>  For example, <i>Torii</i> discloses the following at Figure 6:

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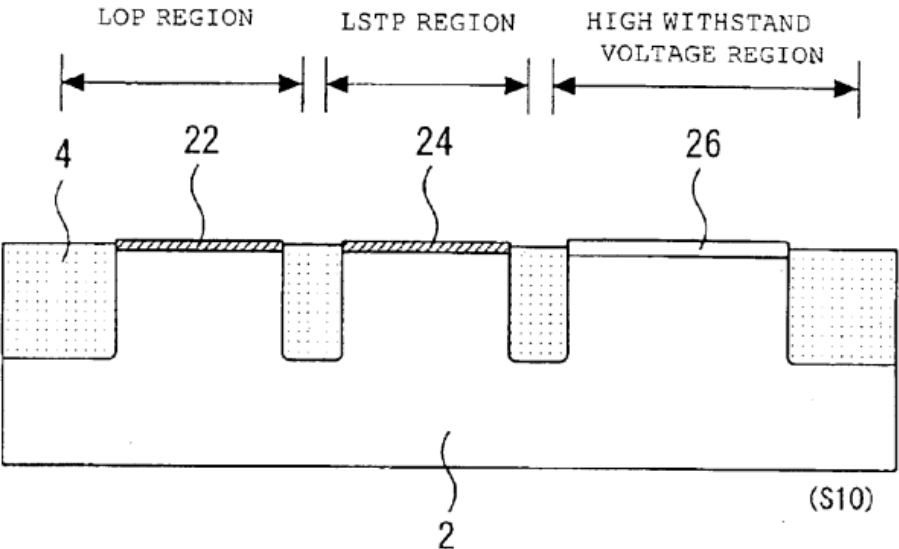
U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	<i>FIG. 6</i>  For example, <i>Torii</i> recites the following in claim 1: each of said first gate insulating film and said second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film For example, <i>Torii</i> discloses the following at 2:28-49 in its discussion of “Background Art”: Therefore, in order to produce finer elements and reduce power consumption, the use of a high-dielectric-constant film (hereafter referred to as high-k film) as a gate insulating film has been studied. The high-k film can be formed thicker than the silicon oxide film, while maintaining the

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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	effective film thickness that determines the transistor current sufficiently thin, and can inhibit the increase of power consumption. As such an SoC, there has been proposed a semiconductor device that uses a high-k film as the gate insulating film of an MISFET (metal insulator semiconductor field effect transistor) for the logic circuit, and a thick silicon oxide film and a high-k film as the gate insulating film for the peripheral circuit. When this semiconductor device is formed, a silicon oxide film is first formed on the entire surface of a substrate using an ordinary method. Thereafter, the silicon oxide film in the region for forming the MISFET for the logic circuit is removed, and then, a high-k film is formed on the entire surface using a CVD method or the like. Thereby, the gate insulating films having different thickness between the peripheral circuit side and the logic circuit side can be formed ... To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
[1F] the first interface layer has a thickness larger than that of the second interface layer, and	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests the first interface layer has a thickness larger than that of the second interface layer. For example, <i>Torii</i> discloses the following at 1:9-14: The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device. More specifically, the present invention relates to a semiconductor device having a plurality of transistors comprising gate insulating films of different film thickness, and a method for manufacturing such a semiconductor device. For example, <i>Torii</i> discloses the following at 4:4-6:

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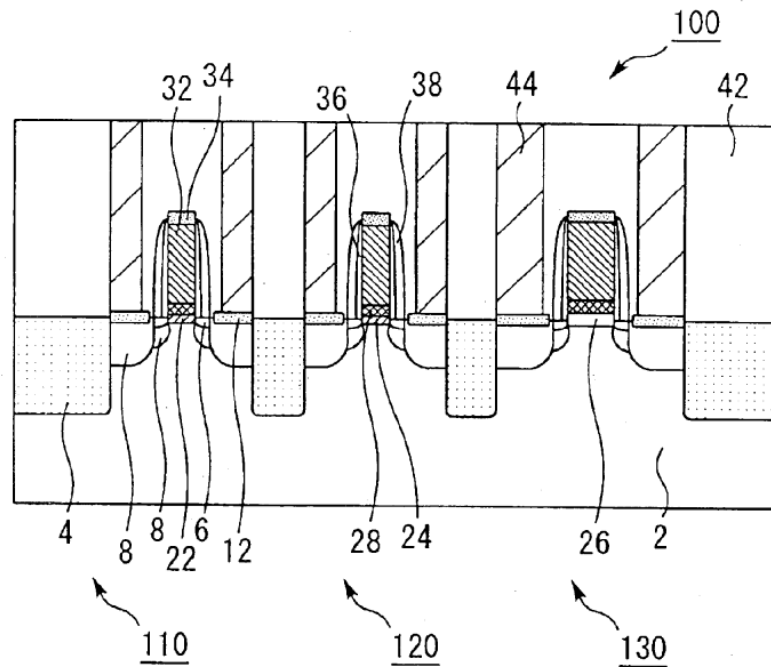
<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	The equivalent-oxide thickness of the first gate insulating film is thicker than the equivalent-oxide thickness of the second gate insulating film. For example, <i>Torii</i> discloses the following at 5:14-29: In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally-oxidized (SiO₂) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm; and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest. For example, <i>Torii</i> discloses the following at 5:62-6:3: Specifically, the MISFET for LOP 110 is a low-power-consumption transistor included the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film having a reduced EOT. The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film, controlling the EOT to be low to some extent, and sufficiently securing the effective film thickness. For example, <i>Torii</i> discloses the following at 12:13-21: In one aspect of the present invention, a laminate film of a silicon oxynitride film and a high-k film is used as each gate insulating film of a plurality of transistors formed on a substrate. The thickness of the high-k film in each gate insulating film is equalized, and the thickness of silicon

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oxynitride films in differentiated. Thereby, even if the thickness of the gate insulating films is slightly different, a semiconductor device of highly controlled film thickness can be realized.

For example, *Torii* discloses the following at Figure 1:

FIG. 1



For example, *Torii* discloses the following in claim 1:

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	equivalent-oxide thickness of said first gate insulating film is thicker than equivalent-oxide thickness of said second gate insulating film, For example, Torii discloses the following at 1:41-2:14 in its discussion of “Background Art”: When a logic circuit portion and a peripheral circuit portion are formed in a semiconductor device, the gate insulating films of the different thickness require to be formed in these circuit portions on a substrate. One of the methods for forming gate insulating films of different thickness is as follows: First, a silicon oxide film of a thickness equivalent to the difference between the thickness of the thick gate insulating film of the high-withstand-voltage MOSFET for the peripheral circuit and the thickness of the thin gate insulating film of the MOSFET for the logic circuit. Thereafter, the silicon oxide film on the portion for forming the MOSFET for the logic circuit is selectively removed. Then, heat-treatment is performed to grow the silicon oxide film by the thickness of the gate insulating film of the MOSFET for the logic circuit. At this time, the gate oxide film of the high-withstand-voltage MOSFET for the peripheral circuit is also grown ... As another method, the method as described below has also been proposed. First, in the same manner as the process for forming an ordinary MOSFET, a gate insulating film of a thickness equal to the thickness of the insulating film of the high-withstand-voltage MOSFET for the peripheral circuit, and a gate electrode are formed in each of the logic circuit portion and the peripheral circuit portion. Thereafter, ion implantation and heat treatment for the formation of a diffusion layer are performed. Then, an interlayer insulating film is formed on the entire surfaces of the gate insulating film and the gate electrode. Next, the peripheral circuit portion is coated with a resist film, and the gate electrode and the gate insulating film in the logic circuit side are removed from the interlayer insulating film. Thereby, a trench of the width of the gate electrode is formed in the interlayer insulating film. Then, a thin gate insulating film of the MOSFET for the logic circuit is formed in the trench, and a gate electrode is buried to form an MOSFET for the logic circuit. Here, since the gate insulating film and the gate electrode initially formed in the region for the logic circuit are removed later, these are called dummy gates ...
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EXHIBIT 779-03: Invalidity of U.S. Patent No. 8,796,779 (the '779 Patent) Based on Torii

<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
	For example, Torii discloses the following at 2:35-49 in its discussion of “Background Art”: As such an SoC, there has been proposed a semiconductor device that uses a high-k film as the gate insulating film of an MISFET (metal insulator semiconductor field effect transistor) for the logic circuit, and a thick silicon oxide film and a high-k film as the gate insulating film for the peripheral circuit. When this semiconductor device is formed, a silicon oxide film is first formed on the entire surface of a substrate using an ordinary method. Thereafter, the silicon oxide film in the region for forming the MISFET for the logic circuit is removed, and then, a high-k film is formed on the entire surface using a CVD method or the like. Thereby, the gate insulating films having different thickness between the peripheral circuit side and the logic circuit side can be formed ... For example, Torii discloses the following at 2:66-3:8 in its discussion of “Background Art”: In such SoC carrying an MISFET for LOP, an MISFET for LSTP, and an MISFET for a high withstand voltage in one chip, the thickness of the gate insulating films in these MISFETs is different from each other. The ITRS (The International Technology Roadmap for Semiconductors) recommends that the EOT (film thickness converted to the thickness of a silicon oxide film) of a gate insulating film of the MISFET for LOP in a 65-nm technology node is 1.0 nm to 1.4 nm, and the EOT of the MISFET for LSTP is 1.2 to 1.6 nm as the target values. To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant’s cover pleading.
[1G] each of the first interface layer and the second interface layer is made of a silicon dioxide	<i>Torii</i> alone or in combination with one or more references, discloses or suggests each of the first interface layer and the second interface layer is made of a silicon dioxide film or a silicon oxynitride film.

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film or a silicon oxynitride film.	For example, <i>Torii</i> discloses the following at 5:14-29: In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally-oxidized (SiO₂) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm; and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest. For example, <i>Torii</i> discloses the following at 6:28-65: On the Si substrate 2 in each region, a thermal oxide film 26 of a thickness of about 5 nm is formed (Step S2). Next, as FIG. 3 shows, the thermal oxide films 26 on the regions for LOP and LSTP are removed (Step S4). Concretely, after the region for high withstand voltage is coated with a resist mask, wet etching is performed using an aqueous solution of hydrofluoric acid to selectively remove the thermal oxide films 26. Thereafter, the resist mask is removed. Next, as FIG. 4 shows, a silicon nitride film 50 is formed in each of the regions for LOP and LSTP (Step S6). Here, heat treatment is performed in an ammonia atmosphere at 600° C. to 700° C. for about 30 seconds. Thereby a silicon nitride film of a thickness of about 0.6 nm is formed in each of the regions for LOP and LSTP. At this time, the surface of the thermal oxide films 26 is also simultaneously nitrided. Here, since the thickness of the silicon nitride film 50 can be easily controlled, a thin film of a uniform thickness to some extent can be formed. Next, as FIG. 5 shows, the silicon nitride film 50 in the region for LSTP is removed (Step S8). Here, after the regions for LOP and high withstand voltage are coated with a resist mask 52, wet

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	etching is performed to remove the silicon nitride film 50. Thereafter, the resist mask 52 is removed. Next, heat treatment is performed in a nitrogen monoxide (NO) environment (Step S10). The temperature of the heat treatment is about 800 to 900° C., and the treating time is about 5 to 60 seconds. Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the silicon oxynitride film 24 in the region for LSTP is about 9%. The surface of the thermal oxide films 26 is further nitrided to form a silicon oxynitride film. For example, <i>Torii</i> discloses the following at 8:14-23: According to the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip. For example, <i>Torii</i> discloses the following at 8:24-40: In the first embodiment, the silicon nitride film in the region for LSTP is removed, leaving the silicon nitride film 50 only in the region for LOP. Thereafter, by performing heat treatment in a nitrogen monoxide atmosphere, the silicon nitride film 50 is oxidized to form a silicon oxynitride film 22 in the region for LOP; on the other hand, a silicon oxynitride film 24 is formed in the region for LSTP. Thus, the use of oxynitride films realizes the formation of highly controlled uniform thin films. Particularly in the first embodiment, by using the silicon nitride film 50, and

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	by using a means for forming an oxynitride film at the same time as the oxidation thereof, highly controlled uniform thin films can be formed even when both the silicon oxynitride films in the region for LOP and the region for LSTP are thin, and have little thickness difference. Thereby, the target value recommended by ITRS for the 65-nm technology can also be achieved. For example, <i>Torii</i> discloses the following at 9:32-38: Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the semiconductor devices can be improved. For example, <i>Torii</i> discloses the following in claim 1: each of said first gate insulating film and said second gate insulating film includes a silicon oxynitride film and a high-dielectric-constant film, To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
Claim 12	
12. The semiconductor device of claim 1, wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium.	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests wherein each of the first and second high dielectric constant insulating films contains hafnium or zirconium. For example, <i>Torii</i> discloses the following at 5:33-36:

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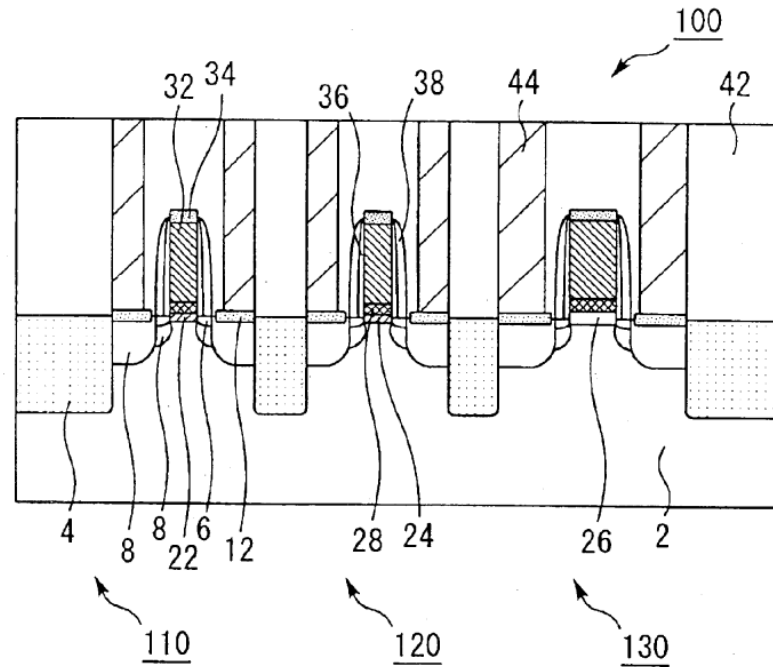
U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO₂) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. For example, <i>Torii</i> discloses the following at 10:9-33: In the first embodiment, as the high-k film, the metal oxide film, such as hafnia (HfO₂), hafnium aluminate (Hf_xAl_{1-x}O_y), alumina (Al₂O₃), lanthanum oxide (La₂O₃), praseodymium oxide (Pr₂O₃), yttrium oxide (Y₂O₃), tantalumoxide (Ta₂O₅), niobiumoxide (Nb₂O₅), titanium oxide (TiO₂), and cerium oxide (CeO₂), or the nitride thereof, or the solid solution thereof, or the solid solution of these metal oxides and SiO₂; or the film of a titanate such as strontium barium titanate ((BaSr)TiO₃) may also be used. For example, when a hafnium aluminate film is used, it is considered to form the film by an ALD method using trimethyl aluminum, hafnium chloride and water, and by heat treatment at about 1000° C. for about 1 second, in the formation of the high-k film 28 in Step S12 described in the first embodiment. When a hafnium silicon oxynitride film is used, it is considered to form the film by forming the hafnium silicate film and nitridation thereof (annealing in atmosphere of ammonia (NH₃)) using ALD method or MOCVD (metal organic chemical vapor deposition) method, in place of Step S12 described in the first embodiment. The method for forming the high-k film is not limited to the ALD method, but other methods, such as a CVD (chemical vapor deposition) method, a sputtering method, a vacuum evaporation method, and the combination of these methods and a reoxidation method, can be used for forming the film. To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
Claim 13	

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<u>U.S. Patent No. 7,923,779</u>	<u>Exemplary Disclosures Relevant to <i>Torii</i></u>
13. The semiconductor device of claim 1, wherein the first and second high dielectric constant insulating films are equal in thickness.	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests the first and second high dielectric constant insulating films are equal in thickness. For example, <i>Torii</i> discloses the following at 4:6-9: The high dielectric-constant film in the first gate insulating film has the same thickness as the high-dielectric-constant film in the second gate insulating film. For example, <i>Torii</i> discloses the following at 5:33-37: On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO₂) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. For example, <i>Torii</i> discloses the following at 6:66-7:5: Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700° C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14). For example, <i>Torii</i> discloses the following at 12:13-21: In one aspect of the present invention, a laminate film of a silicon oxynitride film and a high-k film is used as each gate insulating film of a plurality of transistors formed on a substrate. The thickness of the high-k film in each gate insulating film is equalized, and the thickness of silicon oxynitride films is differentiated. Thereby, even if the thickness of the gate insulating films is slightly different, a semiconductor device of highly controlled film thickness can be realized. For example, <i>Torii</i> discloses the following at Figure 1:

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FIG. 1



For example, *Torii* discloses the following in claim 1:

the high-dielectric-constant film in said first gate insulating film-has the same thickness as the high-dielectric-constant film in said second gate insulating film,

To the extent that *Torii* is found not to disclose this feature, it would have been obvious based on the disclosures of *Torii* alone or in combination with the disclosures of one or more of the references

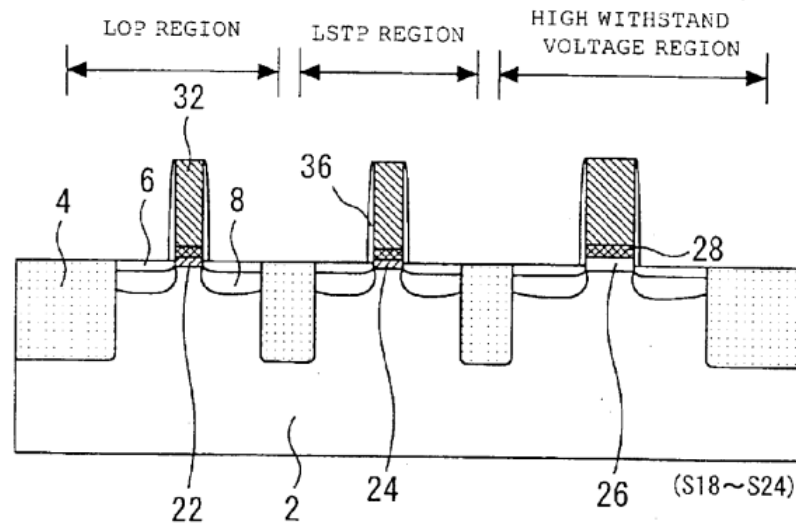
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	cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
Claim 14	
14. The semiconductor device of claim 1, wherein the first and second gate electrodes are made of an identical material.	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests the first and second gate electrodes are made of an identical material. For example, <i>Torii</i> discloses the following at 7:6-22: Next, a non-doped polycrystalline silicon film 54 is formed on the high-k film 28 (Step S16). The non-doped polycrystalline silicon film 54 is a material film for gate electrodes 32, and here, it is deposited to have a thickness of about 120 nm. Thereafter, impurity ions for the gate electrodes are implanted into the non-doped polycrystalline silicon film 54 (Step S17). Next, as FIG. 8 shows, the polycrystalline silicon film 54 is processed for a gate electrode 32 of each region (Step S18). Here, a resist mask of a width of the gate electrode is formed on the polycrystalline silicon film 54 using a conventional method, and etching is performed using the resist mask to process the polycrystalline silicon film 54 and the high-k film 28 to have the width

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of the gate electrode 32. Thereby, a gate electrode 32 and a gate insulating film are formed in each of the regions for LOP, LSTP, and high withstand voltage.

FIG. 8



For example, *Torii* discloses the following at 10:34-38:

In the first embodiment, the case wherein a non-doped polycrystalline silicon film is used as the material for the gate electrode 32 is described. However, in the present invention, the material for the gate electrode 32 may be other material.

For example, *Torii* discloses the following at Figure 1:

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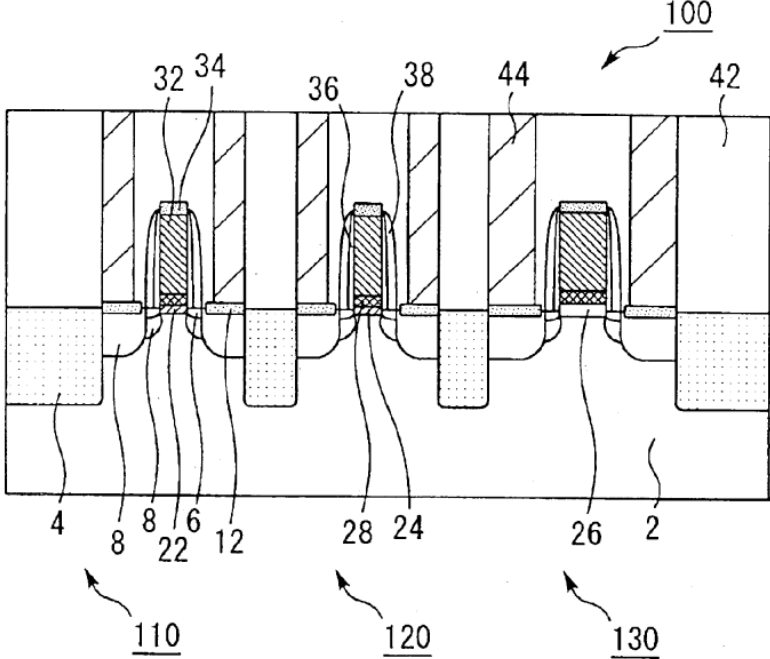
U.S. Patent No. 7,923,779	Exemplary Disclosures Relevant to <i>Torii</i>
	<i>FIG. 1</i>  To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.
Claim 15	

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15. The semiconductor device of claim 1, wherein an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor.	<i>Torii</i>, alone or in combination with one or more references, discloses or suggests an effective work function of the first MIS transistor is higher than an effective work function of the second MIS transistor, according to the '779 Patent. For example, <i>Torii</i> discloses the following at 1:9-14: The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device. More specifically, the present invention relates to a semiconductor device having a plurality of transistors comprising gate insulating films of different film thickness, and a method for manufacturing such a semiconductor device. For example, <i>Torii</i> discloses the following at 4:1-6: Each of the first gate insulating film and the second gate insulating film includes a silicon oxynitride film and a high-dielectric constant film. The equivalent-oxide thickness of the first gate insulating film is thicker than the equivalent-oxide thickness of the second gate insulating film. For example, <i>Torii</i> discloses the following at 5:14-29: In the MISFET for LOP 110, a silicon oxynitride film 22 is formed as an interfacial gate insulating film in the area sandwiched by source-drain extensions 6 on the Si substrate 2. In the MISFET for LSTP 120, a silicon oxynitride film 24 is formed in the equivalent area. In the MISFET for high withstand voltage 130, a surface-nitrided thermally-oxidized (SiO₂) film 26 is formed in the equivalent area. Here, the thickness of the silicon oxynitride film 22 in the MISFET for LOP 110 is about 0.9 to 0.95 nm, and the EOT thereof is about 0.7 nm. The thickness of the silicon oxynitride film 24 in the MISFET for LSTP 120 is about 1.3 nm; and the EOT thereof is about 1.0 nm. Furthermore, the thickness of the thermally-oxidized film 26 is

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	about 5 nm. In short, the silicon oxynitride film 22 for the MISFET for LOP 110 is thinnest, and the thermally-oxidized film 26 for the MISFET for high withstand voltage 130 is thickest. For example, <i>Torii</i> discloses the following at 5:33-41: On each of the silicon oxynitride films 22 and 24 and the thermally-oxidized film 26, the high-k film such as a hafnia (HfO₂) film 28 of a thickness of about 3.0 nm, which is a high-k film, is formed. The EOT of the high-k film 28 is about 0.5 nm. In each of MISFET 110, 120, and 130 for LOP, LSTP, and for high withstand voltage, respectively, a high-k film 28 is laminated on the silicon oxynitride films 22 and 24 or the thermally-oxidized film 26, thereby each gate insulating film is formed. For example, <i>Torii</i> discloses the following at 5:62-6:6: Specifically, the MISFET for LOP 110 is a low-power-consumption transistor included the laminated film of the silicon oxynitride film 22 and the high-k film 28 as gate insulating film having a reduced EOT. The MISFET for LSTP 120 is a low-standby-power transistor using the laminated film of the silicon oxynitride film 24 and the high-k film 28 as gate insulating film, controlling the EOT to be low to some extent, and sufficiently securing the effective film thickness. The MISFET for high withstand voltage 130 is a high-withstand-voltage transistor securing the thickness of the thermal oxide film so as to withstand the external high voltage. For example, <i>Torii</i> discloses the following at 6:55-63: Thereby, as FIG. 6 shows, a silicon oxynitride film 24 of a thickness of about 1.3 nm and an EOT of about 1.0 nm is formed in the region for LSTP. The silicon nitride film 50 formed in the region for LOP is oxidized to form a silicon oxynitride film 22 of an EOT of about 0.7 nm. At this time, the nitrogen content in the Silicon oxynitride film 22 in the region for LOP is about 15 to 20%, and the nitrogen content in the Silicon oxynitride film 24 in the region for LSTP is about 9%. For example, <i>Torii</i> discloses the following at 6:66-7:5:
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	Next, as FIG. 7 shows, a high-k film 28 is formed on the entire surface of the substrate (Step S12). Here, a high-k film of a thickness of 3.0 nm is deposited using hafnium chloride and water as the materials using an ALD (atomic layer deposition) method. Thereafter, heat treatment at about 700° C. is performed in a reduced pressure oxygen atmosphere for about 5 seconds (Step S14). For example, <i>Torii</i> discloses the following at 8:14-23: According to the first embodiment, as described above, the insulating film of a laminate structure wherein a high-k film 28 is deposited on silicon oxynitride films 22 and 24 as the gate insulating film of MISFETs 110 and 120 for LOP and LSTP, respectively. Here, by the use of the silicon oxynitride films 22 and 24, the thin gate insulating films having little thickness difference can be uniformly formed. Therefore, the use of such a structure enables a highly reliable semiconductor device to be formed even when both MISFETs for LOP and LSTP must be mounted in a chip. For example, <i>Torii</i> discloses the following at 9:32-38: Here, the formation of the high-k film 28, after forming the silicon oxynitride films 22 and 24, and the thermal oxide film 26 as the interfacial gate insulating film of each gate insulating film, can be performed in one step. Therefore, the gate insulating films having different thickness can be easily formed, and the productivity of the semiconductor devices can be improved For example, <i>Torii</i> discloses the following at 12:13-21: In one aspect of the present invention, a laminate film of a silicon oxynitride film and a high-k film is used as each gate insulating film of a plurality of transistors formed on a substrate. The thickness of the high-k film in each gate insulating film is equalized, and the thickness of silicon oxynitride films is differentiated. Thereby, even if the thickness of the gate insulating films is slightly different, a semiconductor device of highly controlled film thickness can be realized. To the extent that <i>Torii</i> is found not to disclose this feature, it would have been obvious based on the disclosures of <i>Torii</i> alone or in combination with the disclosures of one or more of the references
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	cited for this limitation in Exhibits 779-01, 779-02 and 779-04 through 779-17 for the reasons discussed herein and in Defendant's cover pleading.