

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,

Petitioner,

v.

ADVANCED INTEGRATED CIRCUIT PROCESS LLC

Patent Owner

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IPR2025-00832

U.S. Patent 8,796,779

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**PETITIONER'S UPDATED EXHIBIT LIST**

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Patent Trial and Appeal Board  
U.S. Patent & Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

Pursuant to 37 C.F.R. § 42.63(e), Petitioner Taiwan Semiconductor Manufacturing Company Ltd. hereby submits a current listing of exhibits. Exhibit TSMC-1034 is being filed today.

| <b>Exhibit</b> | <b>Description</b>                                                                                                   |
|----------------|----------------------------------------------------------------------------------------------------------------------|
| 1001           | U.S. Patent 8,796,779 to Ito et al. (“the ’779 patent”)                                                              |
| 1002           | File History of U.S. Patent 8,796,779 (“’779 File History”)                                                          |
| 1003           | Declaration of Jakub Kedzierski                                                                                      |
| 1004           | CV of Jakub Kedzierski                                                                                               |
| 1005           | U.S. Patent 6,881,657 to Torii, et al. (“Torii”)                                                                     |
| 1006           | U.S. Patent Publication 2010/0258878 to Mise, et al. (“Mise”)                                                        |
| 1007           | U.S. Patent 8,114,739 to Chowdhury, et al. (“Chowdhury”)                                                             |
| 1008           | U.S. Patent 6,693,333 to Yu (“Yu”)                                                                                   |
| 1009           | U.S. Patent 6,787,421 to Gilmer, et al. (“Gilmer”)                                                                   |
| 1010           | U.S. Patent 7,382,023 to Chen (“Chen”)                                                                               |
| 1011           | Van Zant, “Microchip Fabrication” (Fifth Edition, 2004) (“Van Zant”)                                                 |
| 1012           | Weste, “CMOS VLSI Design: A Circuits and Systems Perspective” (Third Edition, 2005) (“Weste”)                        |
| 1013           | Houssa, M., “High-k Dielectrics” to Houssa (IOP Publishing Ltd. 2004) (“Houssa”)                                     |
| 1014           | Wolf, “Silicon Processing for the VLSI Era, Volume 4 – Deep-Submicron Process Technology” (2002) (“Wolf-4”)          |
| 1015           | Plummer, J., et al., “Silicon VLSI Technology: Fundamentals, Practice and Modeling” (Prentice Hall 2000) (“Plummer”) |

| Exhibit | Description                                                                                                                                                                                                                             |
|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1016    | “International Technology Roadmap for Semiconductors: Process Integration, Devices, and Structures” (2007 Edition) (“ITRS”)                                                                                                             |
| 1017    | Campbell, “The Science and Engineering of Microelectronic Fabrication” (Second Edition, 2001) (“Campbell”)                                                                                                                              |
| 1018    | Chau, “Advanced Metal Gate/High-K Dielectric Stacks” (“Chau”)                                                                                                                                                                           |
| 1019    | Guha, et al. “Examination of flatband and threshold voltage tuning of HfO <sub>2</sub> /TiN field effect transistors by dielectric cap layers”, Applied Physics Letters (March 1, 2007) (“Guha”)                                        |
| 1020    | H.-J. Li and M. Gardner, “Dual high-k gate dielectric with poly gate electrode: HfSiON on nMOS and Al <sub>2</sub> O <sub>3</sub> capping layer on pMOS,” IEEE Electron Device Lett., vol. 26, no. 7, pp. 441-443, 2005. (“Li/Gardner”) |
| 1021    | U.S. Patent 7,807,990 to Koyama (“Koyama”)                                                                                                                                                                                              |
| 1022    | U.S. Publication 2006/0244035 to Bojarczuk, JR, et al. (“Bojarczuk”)                                                                                                                                                                    |
| 1023    | “Semiconductor Devices: Physics and Technology” by Sze (Second Edition, 2002) (“Sze”)                                                                                                                                                   |
| 1024    | Lee, S. J., et al. “High Quality Ultra Thin CVD HfO <sub>2</sub> Gate Stack with Poly-Si Gate Electrode,” Digest of International Electron Devices Meeting, pp. 31-34, Dec. 10-13, 2000 (“Lee”)                                         |
| 1025    | Lee, B.H., et al., “Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application,” Digest of International Electron Devices Meeting, pp. 133-36, Dec. 5-8, 1999 (“Lee-1999”)          |
| 1026    | U.S. Patent 7,709,331 to Karve, et al. (“Karve”)                                                                                                                                                                                        |
| 1027    | U.S. Patent 8,017,469 to Luo, et al. (“Luo”)                                                                                                                                                                                            |
| 1028    | Reserved                                                                                                                                                                                                                                |

| Exhibit | Description                                                                                                                                            |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1029    | Wolf, “Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET” (1995) (“Wolf-3”)                                                         |
| 1030    | Translated Excerpts from File History of JP2010-205599                                                                                                 |
| 1031    | U.S. Patent 8,384,160 to Onishi, et al. (“Onishi”)                                                                                                     |
| 1032    | “An Adjustable Work Function Technology Using Mo Gate for CMOS Devices”, Lin, et al., IEEE Electron Device Letters, Vol. 23, No. 1, January 2002       |
| 1033    | “Dual Work Function Metal Gate CMOS Transistors by Ni-Ti Interdiffusion”, Polishchuk, et al., IEEE Electron Device Letters, Vol. 23, No. 4, April 2002 |
| 1034    | TSMC’s stipulation regarding U.S. Patent Nos. 8,198,686; 8,907,425; 7,579,227; 7,923,764; 8,253,180; 8,587,076; and 8,796,779                          |

Respectfully submitted,

/Lori A. Gordon/

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Date: July 25, 2025

**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that the foregoing **Petitioner's Updated Exhibit List** and **Exhibit TSMC-1034** were served on July 25, 2025, via e-mail directed to counsel of record for Patent Owner at the following:

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Respectfully submitted,

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