UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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AMPHENOL CORP.,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD.,
Patent Owner.

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Case No. IPR2025-00834
Patent No. 11,012,252

_____

DECLARATION OF PAUL S. MIN, Ph.D.
IN SUPPORT OF PETITION FOR
***INTER PARTES* REVIEW OF U.S. PATENT NO. 11,012,252**

Amphenol Exhibit 1003
Amphenol v. Credo

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I, Paul S. Min, declare:

I. INTRODUCTION

A. Engagement

1. I have been engaged by Amphenol Corp. ("Petitioner" or "Amphenol") as an independent expert on the subject matters in connection with Amphenol's Petition for *Inter Partes* Review ("IPR") of U.S. Patent No. 11,012,252 (the "'252 patent").

2. I understand that the '252 patent is assigned to Credo Technology Group Ltd. ("Patent Owner" or "Credo").

3. This Declaration is based on the information currently available to me. To the extent that additional information becomes available, I reserve the right to continue my investigation and analysis, which may include a review of documents and information that have not yet been produced, as well as testimony from depositions that have not yet been taken.

4. All of the opinions set forth in this Declaration are based on my own personal knowledge, professional experience, education and judgment, in consideration of the documents, materials and information that I reference.

5. In connection with my work as an expert in this matter, I am being compensated at my standard hourly rate for consulting services, including time spent testifying at any hearing that may be held. I am also being reimbursed for

reasonable and customary expenses associated with my work in this case. I receive no other forms of compensation related to this case. No portion of my compensation is dependent or otherwise contingent upon the results of this proceeding or the specifics of my testimony.

B. Background and Qualifications

6. I am an expert in the field of high speed communication and computing, and the development of electronic devices and software systems and for the related applications. I am currently a Senior Professor in the Department of Electrical and Systems Engineering at Washington University in Saint Louis.

7. I received a B.S. degree in Electrical Engineering in 1982, an M.S. degree in Electrical Engineering in 1984, and a Ph.D. degree in Electrical Engineering in 1987 from the University of Michigan in Ann Arbor. I received several academic honors, including my B.S. degree with honors, a best graduate student award and a best teaching assistant award during my M.S. study, and a best paper award from a major international conference for reporting results from my Ph.D. thesis.

8. After receiving my Ph.D., I worked at Bellcore in New Jersey from August 1987 until August 1990. At Bellcore, I was responsible for evolving the public switched telephone network (PSTN) into a multi-services voice and data network that incorporated packet switches, optical technologies, and wireless

technologies. I received an Outstanding Achievement Award for my contributions to Bellcore in 1989.

9. In September 1990, I joined the faculty at Washington University in St. Louis. Upon arriving at Washington University, I developed a communication and computer curricula in the School of Engineering and Applied Science. I regularly teach undergraduate and graduate courses. In July 1996, I was promoted to an Associate Professor of Electrical Engineering with tenure. I am currently a Senior Professor of Electrical and Systems Engineering at Washington University. I have served as the Chair of the Graduate Curriculum (2000–2002) and the Chair of the Undergraduate Curriculum (2011–2014) for the Department of Electrical and Systems Engineering.

10. At Washington University, I have conducted research in communication, computing, and related electronic hardware and software. My research group has pioneered a new paradigm for computing and communication systems that can alleviate the speed and performance mismatch against optical technology. I have received several grants from U.S. Federal Agencies, including the National Science Foundation (NSF), the Defense Advanced Research Project Agency (DARPA), and the Air Force Office of Scientific Research (AFOSR), and numerous contracts from companies and organizations around the world.

11. I have developed and incorporated various types of SerializerDeserializer (in short "SerDes") devices in the electronic circuits. These electronic circuits perform various functions in high speed communication, for which the integrated circuit chips are notoriously input/output (I/O) limited. To overcome the fundamental I/O limitations in the integrated circuit chips I developed, different types of SerDes blocks such as the RapidIO, the LVDS, and the PCIe were utilized.

12. In addition, my research group at Washington University has significantly contributed to development of future generations of wireless technology. We developed methods that enable coordinated transmission and reception of wireless signals among multiple base stations. Previously, radio signals from multiple base stations were considered as interference. Leveraging our research, a cluster of base stations can work together as a single resource enhancing the quality of radio signals across extremely noisy wireless channels.

13. I developed and implemented a number of semiconductor integrated circuit chips. These integrated circuit chips include switch fabrics, processors, high speed interfaces, protocol transposers, controllers, content search engines, look up table processors, and memory cells and arrays.

14. I have researched a variety of technologies for the packet switches and routers including packet scheduler, traffic shaper, traffic policing, buffer

management, and interposer. In addition, I have researched and implemented various look-up table configurations for fast packet processing, which is particularly applicable to the Multi Protocol Label Switching or MPLS. Moreover, since mid-1990s, I have been researching and developing various security technologies such as the deep packet inspection, content searching and matching, regular expression processing, etc.

15. As a faculty member at Washington University, I have taught a number of courses in electronics, communication, and computing at both the undergraduate and graduate levels. For example, I have taught Electronics (Washington University ESE 232), Communication Theory (Washington University ESE 471), Transmission and Multiplexing (Washington University ESE 571), and Signaling and Control of Communication Networks (Washington University ESE 572).

16. I have directly supervised numerous graduate students, a number of whom received a doctoral degree under my guidance. A number of doctoral theses that I have supervised relate specifically to the aforementioned-communication and computing technologies related to this litigation. My students and I have published a number of peer-reviewed articles in these topics.

17. In addition to my responsibilities as a university faculty member, I have founded two companies. In May 1997, I founded MinMax Technologies, Inc.,

a fabless semiconductor company that developed switch fabric integrated circuit chips for the Internet. In March 1999, I founded Erlang Technology, Inc., a fabless semiconductor company that focused on the design and development of integrated circuit chips and software for the Internet. One of Erlang's products received a best product of the year award in 2004 from a major trade journal for the electronics industry.

18. Outside my own start-up companies, I have also served in various technology and business advisor roles for other companies and organizations around the world. I was the main technical author for one of two winning proposals to the Korean government for CDMA wireless service licenses (1996). I was responsible for designing a commercial scale IS-95 CDMA cellular network, which I understand to be one of the earliest such networks deployed in the world. I worked with numerous engineers and scientists around the world to implement this commercial-scale cellular network before IS-95 CDMA was widely accepted. This provided me with extensive insight into various components of commercial-scale communication technology used today. I have also been involved in a semiconductor company that specializes in semiconductor memories, such as flash EEPROMs, as a board member and as a technical advisor (2007–2011).

19. I am a named inventor on eleven U.S. patents. I have authored and co-authored numerous technical papers and memoranda, many of which have

appeared in various peer-reviewed international journals and conferences. I have given more than 100 seminars and invited talks around the world. I have organized several international conferences and served as an international journal editor.

20. I am a member of, and have been actively involved in, a number of professional organizations. I have served as the Chair of the St. Louis Section of the IEEE, which has more than 3,000 members (2014), and a member of the Eta Kappa Nu Honor Society for electrical engineers. I have also been an Ambassador of the McDonnell International Scholars Academy (2007–2013).

21. I was a member of the Presidential Business Advisors Committee (to President George W. Bush) and was named 2002 Businessman of the Year by the Wall Street Journal for the State of Missouri, for my entrepreneurial efforts.

22. I have received multiple awards for my publications and contributions to technical communication systems. In 1988, I received the Best Paper Award at 18th ISATA Award of Technical Excellence in Florence, Italy. I was also a Rockwell Fellow at the University of Michigan in Ann Arbor in 1988 and 1989. I received a Research Initiation Award in 1993 from the Defense Advance Research Project Agency (DARPA). I received the Best Paper Award at MOBILITY 2011 in Barcelona, Spain. In my nearly 40 years of professional experience, I have acquired significant knowledge about telecommunications, computer, and

electronics industry standards and standard setting organizations such as ANSI, IEEE, ITU, IETF, Bellcore, and 3GPP.

23. Additional details of my education and work experience, awards and honors, and publications that may be relevant to the opinions I have formed are set forth in my curriculum vitae. *See* EX1004.

24. In forming my opinions, I have relied upon the materials listed below, my education, training, and knowledge of connector technologies, electrical and electronic materials, and related experience.

C. Bases of My Opinions and Materials Considered

25. I have reviewed the ’252 patent, its prosecution history, and the prior art and other documents and materials cited herein. For ease of reference, the full list of documents that I have considered is in the exhibit list below. I have also considered the documents cited and referenced herein, even if not included in the exhibit list below. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions and would have had access to either through the applicable patent office and/or well-known libraries, conferences, publications, organizations, and websites in the field as further discussed herein.

26. My opinions, as explained below, are based on my years of education, research, experience, and background in the field of microelectronics and

computing systems, as well as my investigation and study of relevant materials for this declaration. When developing the opinions set forth in this declaration, I assumed the perspective of a person having ordinary skill in the art, as set forth in Section III below. In forming my opinions, I have studied and considered the materials identified in the list below.

Exhibit	Description
1001	U.S. Patent No. 11,012,252
1002	Prosecution History of U.S. Patent No. 11,012,252
1003	*Intentionally left blank*
1004	Curriculum Vitae of Paul S. Min, Ph.D.
1005	U.S. Patent No. 9,337,993 ("Lugthart-993")
1006	U.S. Patent No. 7,762,727 ("Aronson")
1007	U.S. Patent Application Publication No. 2013/0115803 ("Tang")
1008	DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer Datasheet, SNLS482B, Texas Instruments Incorporated, (January 2017) ("TI-Retimer")
1009	Affidavit of Tanya Zeif
1010	U.S. Patent Application Publication No. 2020/0194911 ("Ayzenberg")
1011	U.S. Patent Application Publication No. 2011/0228821 ("van der Horst")
1012	U.S. Patent Application Publication No. 2010/0210142 ("McGrath")
1013	U.S. Patent Application Publication No. 2013/0280955 ("Alden")
1014	U.S. Patent Application Publication No. 2006/0045176 ("Moughabghab")
1015	U.S. Patent Application Publication No. 2010/0232492 ("Mezer-492")
1016	U.S. Patent No. 7,239,665 ("Mezer-665")
1017	U.S. Patent No. 6,621,862 ("Dabell")

Exhibit	Description
1018	U.S. Patent No. 6,055,269 (“Drost”)
1019	U.S. Patent No. 5,856,980 (“Doyle”)
1020	U.S. Patent No. 5,452,333 (“Guo”)
1021	U.S. Patent Application Publication No. 2014/0281067 (“Das Sharma”)
1022	U.S. Patent No. 8,787,430 (“Raghavan”)
1023	U.S. Patent No. 6,147,826 (“Hashimura”)
1024	U.S. Patent Application Publication No. 2017/0187463 (“Nedovic”)
1025	SFF-8436 Specification for QSFP+ 4X 10 Gb/s Pluggable Transceiver Rev 4.9, SFF Committee, August 31, 2018
1026	SFF-8642 Specification for MINI MULTILANE SERIES: SHIELDED INTEGRATED CONNECTOR, Rev 2.7, SFF Committee, February 26, 2010
1027	SFF-8432 Specification for SFP+ Module and Cage, Rev 5.2a, SFF Committee, November 30, 2018
1028	IEEE Standard for Ethernet, IEEE 802.3 (2015) Section One
1029	IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Six
1030	Texas Instruments Application Report SNLA225, “Selecting TI SigCon Devices for SFF-8431 SFP+ Applications.” Texas Instruments Inc. (June 2014) (available at https://web.archive.org/web/20151031185909/https://www.ti.com/lit/an/snla225/snla225.pdf)
1031	Proakis, John G., “Digital Communication,” 4th Edition, 2000, McGraw-Hill, pp. 583-635 (“Proakis”)
1032	Hanumolu, P. K. et al., “Equalizers for High-Speed Serial Links.” International Journal of High Speed Electronics and Systems 15 (2005), pp. 429-458 (“Hanomolu”)
1033	*Intentionally left blank*
1034	*Intentionally left blank*
1035	*Intentionally left blank*
1036	*Intentionally left blank*

Exhibit	Description
1037	*Intentionally left blank*
1038	*Intentionally left blank*
1039	Dkt. 1-5, Exh. 5 To Complaint, *Credo Semiconductor Inc. et al. v. Amphenol Corp.*, No. 2:25-cv-00296 (E.D. Tex. Mar. 13, 2025)
1040	*Intentionally left blank*
1041	*Intentionally left blank*
1042	*Intentionally left blank*
1043	*Intentionally left blank*
1044	Liu, Jin and Xiaofeng Lin, "Equalization in high-speed communication systems." IEEE Circuits and Systems Magazine 4 (2004) pp. 4-17 ("Liu")
1045	Hsieh, Ming-ta and Gerald E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery." IEEE Circuits and Systems Magazine 8 (2008), pp. 45-57 ("Hsieh")

D. My Understanding of Patent Law

27. In developing my opinions, I discussed various relevant legal principles with Petitioner's attorneys. Though I do not purport to have prior knowledge of such principles, I understood them when they were explained to me and have relied upon such legal principles, as explained to me, in the course of forming the opinions set forth in this declaration. My understanding in this respect is as follows:

28. I understand that "*inter partes* review" (IPR) is a proceeding before the United States Patent & Trademark Office for evaluating the patentability of an issued patent's claims based on prior-art patents and printed publications.

29. I understand that, in this proceeding, Petitioner has the burden of proving that the challenged claims of the ’252 patent are unpatentable by a preponderance of the evidence. I understand that “preponderance of the evidence” means that a fact or conclusion is more likely true than not true.

30. I understand that, in IPR proceedings, claim terms in a patent are given their ordinary and customary meaning as understood by a person of ordinary skill in the art (“POSA”) in the context of the entire patent and the prosecution history pertaining to the patent. If the specification provides a special definition for a claim term that differs from the meaning the term would otherwise possess, the specification’s special definition controls. If a claim element is expressed as a “means” for performing a specified function, I understand that it covers the corresponding structure described in the specification and equivalents of the described structure. I have applied these standards in preparing the opinions in this declaration.

31. I understand that determining whether a particular patent or printed publication constitutes prior art to a challenged patent claim can require determining the effective filing date (also known as the priority date) to which the challenged claim is entitled. I understand that for a patent claim to be entitled to the benefit of the filing date of an earlier application to which the patent claims priority, the earlier application must have described the claimed invention in

sufficient detail to convey with reasonable clarity to the POSA that the inventor had possession of the claimed invention as of the earlier application's filing date. I understand that a disclosure that merely renders the claimed invention obvious is not sufficient written description for the claim to be entitled to the benefit of the filing date of the application containing that disclosure.

32. I understand that for an invention claimed in a patent to be patentable, it must be, among other things, new (novel—*i.e.*, not anticipated) and not obvious from the prior art. My understanding of these two legal standards is set forth below.

1. Anticipation

33. I understand that, for a patent claim to be "anticipated" by the prior art (and therefore not novel), each and every limitation of the claim must be found, expressly or inherently, in a single prior-art reference. I understand that a claim limitation is disclosed for the purpose of anticipation if a POSA would have understood the reference to disclose the limitation based on inferences that a POSA would reasonably be expected to draw from the explicit teachings in the reference when read in light of the POSA's knowledge and experience.

34. I understand that a claim limitation is inherent in a prior art reference if that limitation is necessarily present when practicing the teachings of the

reference, regardless of whether a person of ordinary skill recognized the presence of that limitation in the prior art.

2. Obviousness

35. I understand that a patent claim may be unpatentable if it would have been obvious in view of a single prior-art reference or a combination of prior-art references.

36. I understand that a patent claim is obvious if the differences between the subject matter of the claim and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the relevant field at the time the invention was made. Specifically, I understand that the obviousness question involves a consideration of:

- the scope and content of the prior art;
- the differences between the prior art and the claims at issue;
- the knowledge of a person of ordinary skill in the pertinent art; and
- if present, objective factors indicative of non-obviousness, sometimes referred to as "secondary considerations." To my knowledge, the Patent Owner has not asserted any such secondary considerations with respect to the '252 patent.

37. I understand that in order for a claimed invention to be considered obvious, a POSA must have had a reason for combining teachings from multiple prior-art references (or for altering a single prior-art reference, in the case of obviousness in view of a single reference) in the fashion proposed.

38. I further understand that in determining whether a prior-art reference would have been combined with other prior art or with other information within the knowledge of a POSA, the following are examples of approaches and rationales that may be considered:

- combining prior-art elements according to known methods to yield predictable results;
- simple substitution of one known element for another to obtain predictable results;
- use of a known technique to improve similar devices in the same way;
- applying a known technique to a known device ready for improvement to yield predictable results;
- applying a technique or approach that would have been "obvious to try," *i.e.*, choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success.

- known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art;
- some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior-art reference or to combine prior-art reference teachings to arrive at the claimed invention. I understand that this teaching, suggestion or motivation may come from a prior-art reference or from the knowledge or common sense of one of ordinary skill in the art.

39. I understand that for a single reference or a combination of references to render the claimed invention obvious, a POSA must have been able to arrive at the claimed invention by altering or combining the applied references.

3. Claim Interpretation

40. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the claim. In this section, I discuss the interpretations I have applied to certain claim terms in my analysis.

41. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art at the time of the alleged invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of ordinary skill in the art in the relevant time period (*i.e.*, at the time of the purported invention, or the so called "effective filing date" of the patent application), after reviewing the patent claim language, the specification and the prosecution history (*i.e.*, the intrinsic record).

42. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office, and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or to clearly and unambiguously disavow claim coverage.

43. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of skill in the art at the time of the alleged invention. This can be useful for technical terms whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

44. I understand that determining whether a claimed invention is novel and non-obvious requires comparing the prior art to the challenged claim. In this Declaration, I apply the above standards to the terms in the challenged claims. The meanings of specific terms are discussed below in connection with evaluating the disclosure in the priority documents.

II. DESCRIPTION OF THE RELEVANT FIELD AND THE RELEVANT TIME FRAME

45. I have reviewed the '252 patent (EX1001) and its prosecution history (EX1002).

46. I understand that the ’252 patent issued from U.S. Patent Application No. 16/539,910 (“the ’910 application”), filed on August 13, 2019. EX1001, codes (21), (22).

47. I understand that the ’910 application relates to Chinese Patent Application No. 201910155535.9, which was filed on March 1, 2019. EX1001, code (30).

48. I have been instructed by counsel to assume the relevant timeframe for my analysis of the prior art in this Declaration is on or before March 1, 2019.

49. Based on my review of this material, I believe that the relevant general field for the purposes of the ’252 patent is digital communication system design.

III. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)

50. I have been informed and understand that for purposes of assessing whether prior-art references disclose every element of a patent claim (thus “anticipating” the claim) and/or would have rendered the claim obvious, the patent and the prior-art references must be assessed from the perspective of a person having ordinary skill in the art (“POSA”) to which the patent is related, based on the understanding of that person at the time of the patent claim’s priority date.

51. I have been informed and understand that various factors may be considered in assessing the level of a POSA, including (1) educational level of the

inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. I have also been informed and understand that not all of these factors may be present in every case, and one or more of these or other factors may predominate in a particular case. I have further been informed and understand that these factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art. I have applied this standard throughout my declaration.

52. The ’252 patent involves technology in the field of network communication designs. I have been asked to provide my opinions as to the state of the art in this field by March 2019. Whenever I offer an opinion in this declaration about the knowledge of a POSA, the manner in which a POSA would have understood the claims of the ’252 patent or its description, the manner in which a POSA would have understood the prior art, or what a POSA would have been led to do based on the prior art, I am referencing the March 2019 timeframe, even if I do not say so specifically in each case.

53. In the context of the ’252 patent and the prior art, it is my opinion that the POSA to whom the patent is addressed, on March 1, 2019, would have had a Bachelor of Science in Electrical or Computer Engineering with at least three years of experience in digital communication system design. For example, a POSA

would have had a working knowledge of assuring the signal integrity over noisy channels and how the signal integrity is affected by PCB and cable designs, and methods for addressing those concerns. More education could substitute for experience, and vice versa. This person would have been capable of understanding and applying the teachings of the ’252 patent and the prior-art references discussed in this declaration.

54. The basis for my familiarity with the level of ordinary skill is my own technical experience and my interaction with students and professionals in the field of Electrical and Computer Engineering who were at this level of skill as of March 1, 2019. I am also very familiar with the professional background of those who worked in the field around the priority date of the ’252 patent as I personally have worked in the industry extensively at the time. I am well aware of the knowledge that a POSA would have had at the time this patent was written as I have been actively consulting, teaching, and carrying out research with such students and/or professionals all through that period.

55. In reaching this opinion as to the hypothetical POSA, I have considered the standard recited above such as types of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level and professional capabilities of workers in the field.

56. As summarized above with regard to my qualifications and experience, I possessed at least the level of skill of a person of ordinary skill in the art at the time of the alleged invention of the ’252 patent.

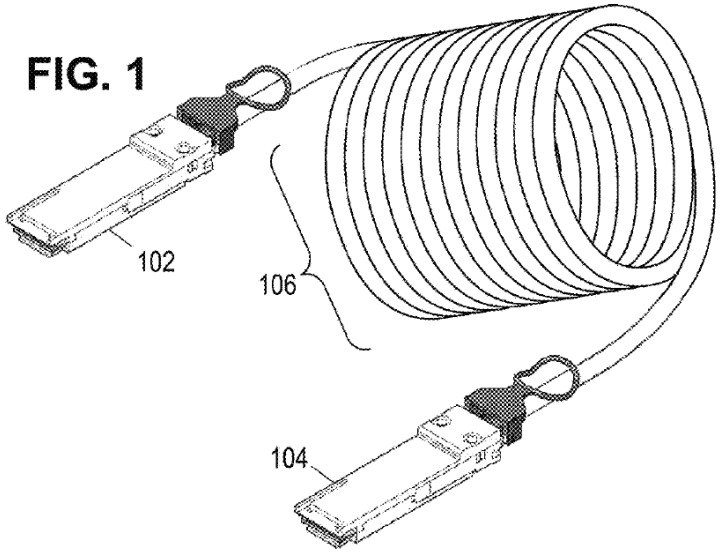
57. I have worked with many people who fit the characteristics of the POSA, and I am familiar with their level of skill in and around March 2019. When developing the opinions set forth in this declaration, I assumed the perspective of a POSA as set forth above.

IV. THE ’252 PATENT

58. The ’252 patent is titled “Active Ethernet Cable.” The ’252 patent states that “[t]his Ethernet standard provides a common media access control specification for local area network (LAN) operations at selected speeds from 1 Mb/s to 100 Gb/s over coaxial cable, twinaxial cable, twisted wire pair cable, fiber optic cable, and electrical backplanes, with various channel signal constellations.” EX1001, 1:9-14. The ’252 patent goes on to state that “[a]s demand continues for ever-higher data rates, the standard is being extended. Such extensions to the standard must account for increased channel attenuation and dispersion even as the equalizers are forced to operate at faster symbol rates. It is becoming increasingly difficult to provide affordable, mass-manufactured network hardware that assures consistently robust performance as the proposed per-lane bit rates rise beyond 50 Gbps with PAM4 or larger signal constellations.” EX1001, 1:14-22.

A. Described Embodiments

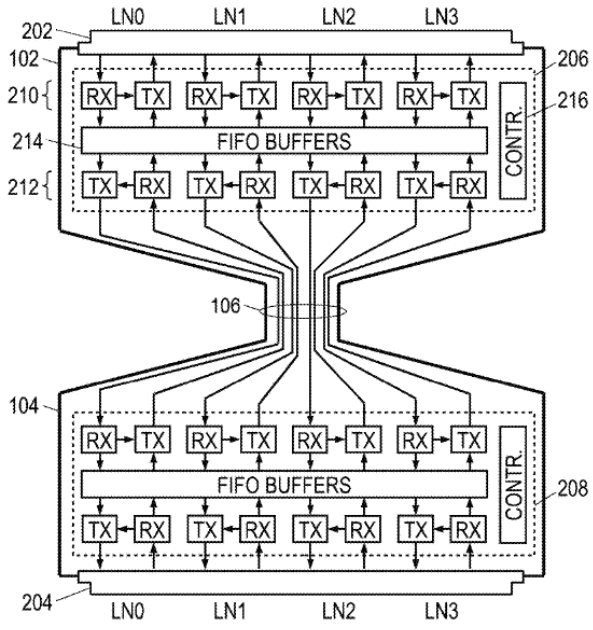
59. The ’252 patent shows in FIG. 1 “a perspective view of an illustrative active Ethernet cable.” EX1001, 3:19-20.



60. With regard to FIG. 1 above, the ’252 patent states that “[p]ursuant to the Ethernet standard, each conductor pair may provide unidirectional transport of a differential signal. To enable robust performance over even extended cable lengths (greater than, say, 3 m, 6 m, or 9 m), each connector 102, 104 may include a powered transceiver that performs clock and data recovery (CDR) and re-modulation of data streams in each direction. Notably, the transceivers perform CDR and re-modulation not only of the outbound data streams as they exit the cable, but also of the inbound data streams as they enter the cable.” EX1001, 3:61-4.3.

61. With regard to FIG.2 shown below, the ’252 patent further explains that “[c]onnector 102 includes a plug 202 adapted to fit a standard-compliant Ethernet port in a first host device 302 (FIG. 3) to receive an inbound data stream as an electrical input signal from the host device and to provide an outbound data stream as an electrical output signal to the host device. Similarly, connector 104 includes a plug 204 that fits an Ethernet port of a second host device 304. Connector 102 includes a first transceiver 206 to perform CDR and remodulation of the data streams entering and exiting the cable at connector 102, and connector 104 includes a second transceiver 208 to perform CDR and re-modulation of the data streams entering and exiting the cable at connector 104.” EX1001, 4:28-39.

FIG. 2



62. Notably, the ’252 patent describes that “[i]n at least some contemplated embodiments, the host-facing transmitter and receiver set 210 employ fixed equalization parameters that are cable-independent, *i.e.*, they are not customized on a cable-by-cable basis. The center-facing transmitter and receiver set 212 preferably employ cable-dependent equalization parameters that are customized on a cable-by-cable basis.” EX1001, 4:60-66. The ’252 patent further explains that “[t]he cable-dependent equalization parameters may be adaptive or fixed, and initial values for these parameters may be determined during manufacturer tests of the cable. The equalization parameters may include filter coefficient values for pre-equalizer filters in the transmitters, and gain and filter coefficient values for the receivers.” EX1001, 4:66-5:5.

B. Prosecution History of the ’252 Patent

63. The ’252 patent issued from U.S. patent application no. 16/539,910, filed 2019-08-13. EX1002, 22-55.

64. The Examiner issued a non-final rejection, rejecting pending claims 1-2, 8-9, and 15-16 as being anticipated by Lugthart-993, but at the same time allowed pending dependent claims 3-7, 10-14, and 17-20. EX1002, 192-199.

65. The Applicant then amended the claims to include subject matter that was deemed allowable. EX1002, 210-217. For example, the dependent claim 3 was amended into an independent claim with subject matter from former parent claims

1 and 2. The independent claim 3 recited "respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal," which was apparently deemed allowable over Lugthart-993. EX1002, 211.

66. The application was then allowed with no further discussion. EX1002, 227-233.

C. The Challenged Claims

67. The '252 patent has 14 claims. Claims 1, 6, and 11 are independent.

68. Claim 1 recites [1.PRE] An active Ethernet cable that comprises: [1.A] electrical conductors connected between a first connector and a second connector, [1.B] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable, [1.C] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream, [1.D] the respective transceiver for each of the first and second

connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and [1.E] the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

69. Claim 6 recites a "communication method" that generally recites the same functions described for the active cable of claim 1. Claim 11 recites a "cable manufacturing method" that recites "connecting" and "packaging" steps for manufacturing a cable with generally the same functions described for the active cable of claim 1.

70. Dependent claims 2-4 add limitations on equalization parameters used for particular cable functions. Dependent claim 5 adds limitations on a symbol rate of data streams. Dependent claims 7-9 and 12-14 largely repeat limitations from claims 2-4, and dependent claim 10 largely repeats limitations from claim 5.

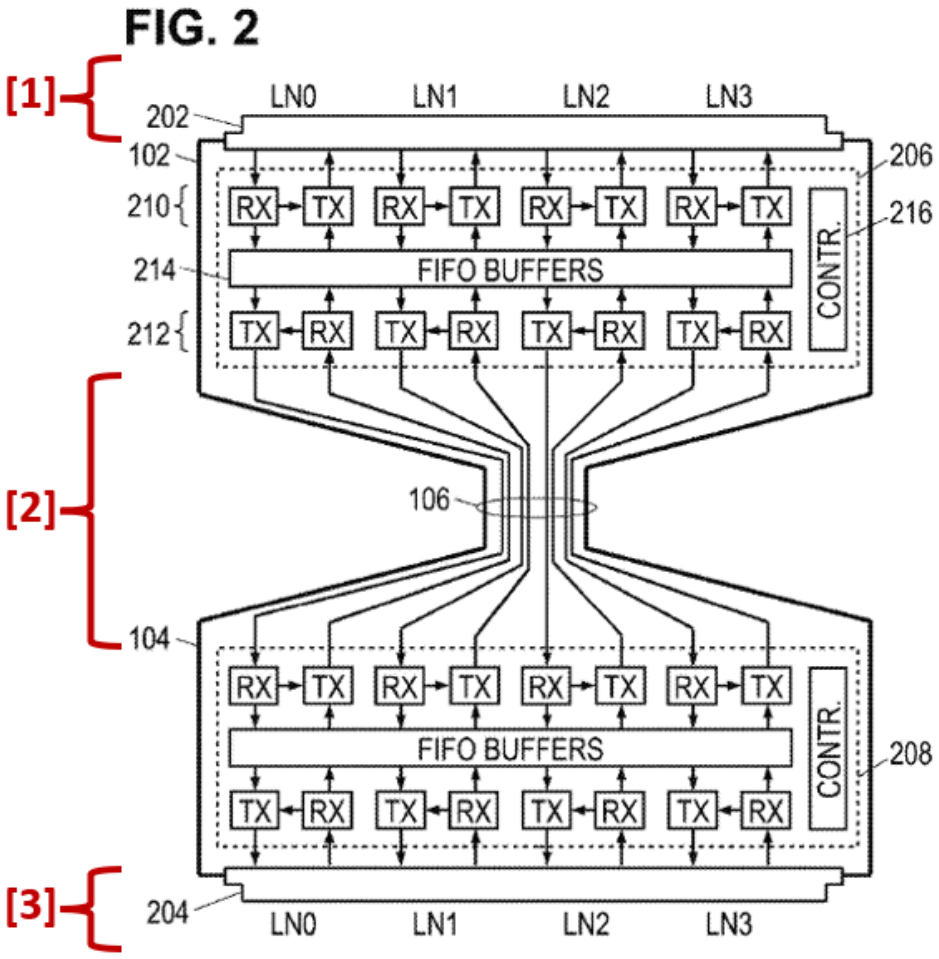
D. Additional Technical Background

71. Below, I will briefly describe technical concepts that are described in the '252 patent and/or the prior art.

1. Active Ethernet Cables

72. The ’252 patent relates to active Ethernet cables that connect two “host devices” (*e.g.*, computers). EX1001, 3:44-48, 1:5-23 (“Ethernet” is an IEEE standard). “Active” cables have powered components that process signals transmitted into and/or out of the cable. EX1005 (Lugthart-993), 14:3-5. Active Ethernet cables have “connectors” at their ends to connect to mating ports on host devices and each connector has a transceiver (*i.e.*, a transmitter and receiver) that processes signals transmitted into and out of the cable. EX1001, 1:29-42.

73. The transceivers in each of the connectors split the link between two hosts into three segments–[1] from the first host to the first transceiver (a first host interface), [2] between the first transceiver and the second transceiver (over the cable), and [3] between the second transceiver and the second host (a second host interface).



Each transceiver receives a signal from its host, demodulates, processes, and remodulates it for transmission over the cable. The transceiver at the other end of the cable receives the signal, demodulates, processes, and remodulates it to pass through its host interface. EX1001, 4:4-26. Modulation sets the properties of an analog signal (*e.g.*, its amplitude) to represent digital data, which facilitates transmission over a communication channel. Lugthart-993, 30:40-63. Demodulation reconstructs the digital data from the analog signal. EX1001, 7:3-11; Lugthart-993, 8:37-41.

74. As the analog signal passes over a communication channel, it may be degraded/distorted. EX1001, 4:20-21; Lugthart-993, 6:22-43. The transceivers of the '252 patent include "clock and data recovery" (CDR) circuits. EX1001, 4:27-43. CDR circuits in a signal's path will retime and attempt to recreate the signal (as best as it is able to; *see* my discussion of CDR in Section IV.D.4 below), and so degradation/distortion of signals over each segment of the link between hosts to be addressed separately (*i.e.*, degradation/distortion before CDR is separated from degradation/distortion after CDR), rather than addressing a larger aggregate amount of degradation/distortion over the entire link. One form of degradation/distortion is jitter, an unwanted variation in the timing of changes in the analog signal that represents digital data. EX1020, 1:24-26, 1:58-2:2; EX1006 (Aronson), 11:6-10. A transceiver with CDR can "recover the clock and retime the signal" to compensate for jitter. Aronson, 11:1-6, 11:20-24.

75. Intersymbol interference (ISI) is another form of degradation/distortion, *e.g.*, caused by lossy channels, in which one symbol in a data stream interferes with subsequent symbols. Lugthart-993, 6:27-43. Equalization is signal processing that may be used to compensate for channel losses—and therefore compensate for ISI—so that a received signal approximates the transmitted signal. Lughtart-993, 8:58-9:5; EX1016, 1:9-12; Aronson, 15:2-4. Equalization can be performed at the transmitter (called pre-equalization) and/or

the receiver. Aronson, 14:19-23, 15:1-8. Equalization was commonly achieved via filters using parameters (*e.g.*, coefficients) controlling the filter's modification of the signal. Lugthart-993, 9:19-31, 21:33-46.

76. Equalization parameters could be fixed, adjustable, or "adaptive" via a process, *e.g.*, during which equalization parameters are modified in response to sending known test signals through the channel using different equalization parameters until the error in the equalized signal at the receiver is low. Aronson, 15:5-8; Mezer-665, 6:36-41, 2:47-50; Das Sharma, [0080]-[0081].

77. I further discuss these concepts, such as ISI, equalization, and CDRs, below.

2. SerDes for Transmission of High-Speed Serial Data

78. In today's environment, many of the specialized integrated chips (or ICs) are in the form of the Application Specific Integrated Chip (or ASIC). In particular, the ASICs used in the communications and computer environments are notoriously input-output (IO) limited.

79. By way of background, some integrated circuit chips are die-limited when the ICs contain large number of complex functional blocks comprising a large number of transistors. For example, certain complex processors may be die-limited as they contain multiple functional blocks such as a large number of processor cores, memory interfaces, off-load engines, security features, IO

interfaces, etc. To implement these functional block takes up large areas of silicon die, and thus the sizes of such ICs are determined by the size of the silicon die, that the IC packages contain.

80. In other cases, some integrated circuit chips are IO limited. The inputs and outputs from an IC must be accessible to the outside of the package containing the IC in the form of IO pins or pads. When there are a large number of inputs and outputs from the IC, the size of the package containing the silicon die of the IC must be increased since the IO pins or pads must be spaced apart to provide proper electrical connectivity of the IC to the printed circuit board. In this case, the size of the IC is determined by the number of input and output pins or pads. Many of the ASICs used in the communication environment are IO limited IC.

81. When the number of IO pins or pads becomes so large, *e.g.*, more than a thousand, in order to provide the IO pins or pads outside the IC package becomes untenable since in this case, the size of the IC package becomes too large for the IC to be mounted on a printed circuit board, which is often crowded with many components necessary to perform the required functions.

82. To cope with the IO limitation in the communication ICs, the electronic industry developed the Serializer/Deserializer (or SerDes). In designing an IO-limited IC, one or more of the SerDes blocks are incorporated as the external

interfaces from the IC. For transmission, the serializer portion of the SerDes combines multiple output data streams into a single data stream via multiplexing these output data streams, which otherwise would be transmitted separately. Then, the serialized data stream is transmitted from the IC to the receiving end, for example, another IC with similar SerDes blocks. The receiving IC then deserializes the received serial data stream by way of the Des portion of the SerDes block, which is embedded in the receiving IC.

83. While the use of the SerDes mitigates or minimizes the IO limitation in the IC design, it creates different challenges, specifically the increase in the transmission rate as the data rate increases according to the number of the data streams combined during the serialization process.

3. Equalization

84. In explaining the basic concept of the equalization, I refer to a widely referenced textbook entitled, "Digital Communication" by John G. Proakis (EX1031; "Proakis"). In addition, I also refer to a tutorial paper entitled, "Equalizers for High-Speed Serial Link" by Pavan K. Hanumolu, G. Y. Wei, and U. K. Moon (EX1032; "Hanumolu"), and a featured article entitled "Equalization in High-Speed Communication Systems" by J. Liu and X. Lin (EX1044; "Liu").

85. Liu describes that "[c]ommunication systems may be described by the block diagram shown in Figure 1. They always involve three basic parts: the

transmitter (TX), the channel, and the receiver (RX). The signal, *s(t)*, is the transmitted signal and the signal, *r(t)*, is the received signal. Non-ideal channel characteristics, for example, limited channel bandwidth and crosstalk noise, often deteriorate the signal quality of the received signal and causes error in data recovery." Liu, page 5. The following is Figure 1 of Liu.

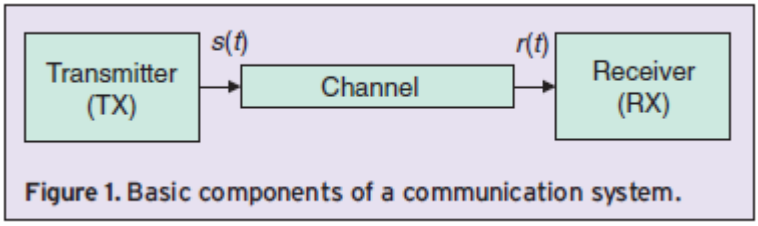


Figure 1. Basic components of a communication system.

86. In high-speed communication systems, for example utilizing the SerDes in the transmitter and the receiver, the channel bandwidth may be limited in comparison to potentially up to hundreds of gigabits per second data rate. In this case, the "deterior[ation of] the signal quality of the received signal" that Liu refers to above requires the use of signal processing techniques known as the equalization.

87. In particular, Liu states that "[t]he term of inter-symbol interference describes the dispersion effect in discrete time domain, where the transmitted data are treated as digital symbols with pulse modulation. Figure 5 shows the communication channel with transmitter pulse modulation and receiver filter. For binary data, which is also known as two level pulse amplitude modulation (2-PAM) shown in Figure 2, the discrete information-bearing symbol $\{I_n\}$ is either

"1" or "0" and the modulation pulse is a square pulse as shown." The following is Figure 5 of Liu.

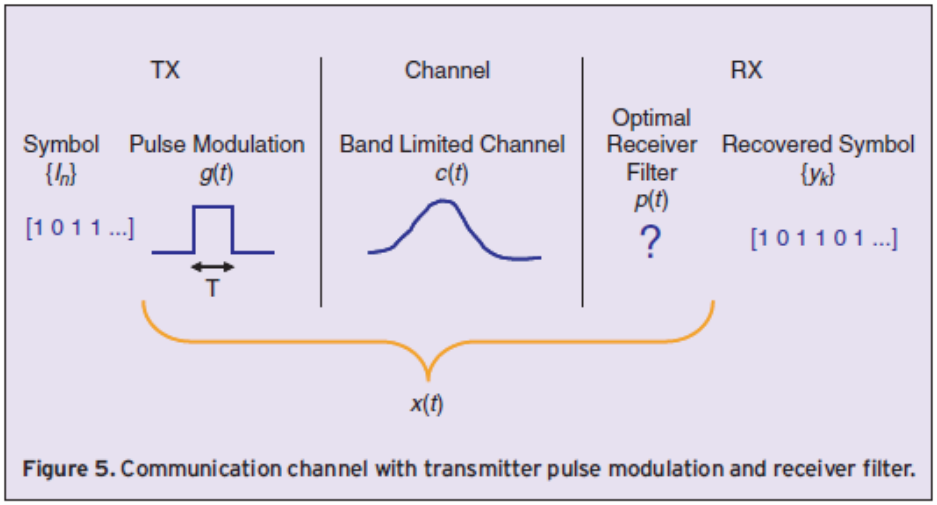


Figure 5. Communication channel with transmitter pulse modulation and receiver filter.

88. As shown in Figure 5 of Liu above, square pulse *g(t)* is transmitted during a time period T from the transmitter TX. Because the channel is bandwidth limited, the transmitted signal *g(t)* cannot maintain its sharp transitions in both leading and trailing edges, making more rounded shape of signal shown in *c(t),* which is received at the receiver RX. Importantly, the received signals *c(t)* has trailing edge lasting longer than the transmission interval T. If the transmitter has more signal to transmit after one transmission interval of T, then by the time the leading edge of the successively transmitted signal arrive at the receiver, the trailing edge of the received signal *c(t)* from the previously transmitted signal is present at the receiver. In other words, the trailing edge of the signal received may overlap with the leading edges of one or more of the signals transmitted successively. This phenomenon is called the intersymbol interference (or ISI).

89. Proakis describes that "[t]he channel distortion results in intersymbol interference, which, if left uncompensated, causes high error rates. The solution to the ISI problem is to design a receiver that employs a means for compensating or reducing the ISI in the received signal. The compensator for the ISI is called an *equalizer*" (Proakis, page 583), and that "[t]he discrete-time white noise linear filter model for the intersymbol interference effects that arise in high-speed digital transmission over nonideal band-limited channels will be used throughout the remainder of this chapter in our discussion of compensation techniques for the interference. In general, the compensation methods are called *equalization techniques* or *equalization algorithms"* (Proakis, page 589).

90. Liu explains that "[t]here are two types of equalization: transmitter pre-emphasis and receiver equalization. Both seek to either emphasize the high-frequency components or to deemphasize the low frequency components of the transmitted or received signal, in order to compensate the effect that the high-frequency components are attenuated more than the low-frequency components through the channel. Using both the transmitter and receiver equalization allows the best system performance in terms of BER." Lui, page 9.

4. Clock and Data Recovery (CDR)

91. In "Architectures for multi-gigabit wire-linked clock and data recovery" by Ming-ta Hsieh and Gerald E. Sobelman (EX1045; "Hsieh"), Hsieh

states that "[a] clock and data recovery (CDR) circuit is an essential block in many high-speed wire-linked data transmission applications such as optical communications systems, backplane data-link routing and chip-to-chip interconnection. The important role of a CDR is to extract the transmitted data sequence from the distorted received signal and to recover the associated clock timing information." Hsieh, page 46.

92. Hsieh further states that "Figure 2 illustrates a simplified functional diagram of clock recovery and data retiming using a CDR circuit. The clock recovery circuit detects the transitions in the received data and generates a periodic clock. The decision circuit often uses D-type Flip-Flops (DFFs) driven by the recovered clock to retime the received data, which samples noisy data and then regenerates it with less jitter and skew." Hsieh, page 46. The following is Figure 2 of Hsieh.

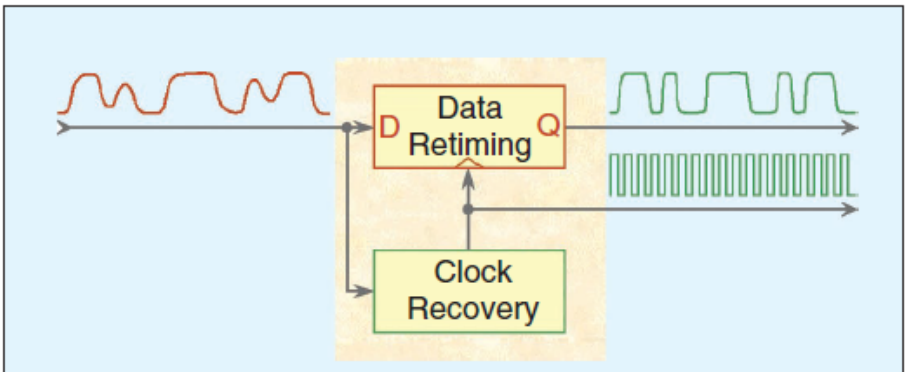


Figure 2. Clock recovery and data retiming for a CDR circuit.

93. The figure above shows that the CDR circuit receives data signals from the channel, which is distorted by, among others, the limited bandwidth of the channel. From the received signal, the clock is recovered, and using the clock, the received signal is sampled and the data is stored in its original form.

94. Hsieh states that "[a] generic block diagram of a high-speed wire-linked data transmission system is shown in Figure 3, where the received data is equalized in the receiver input buffer and retimed in the CDR module before proceeding into the deserializer module." Hsieh, page 46. The following is Figure 3 of Hsieh.

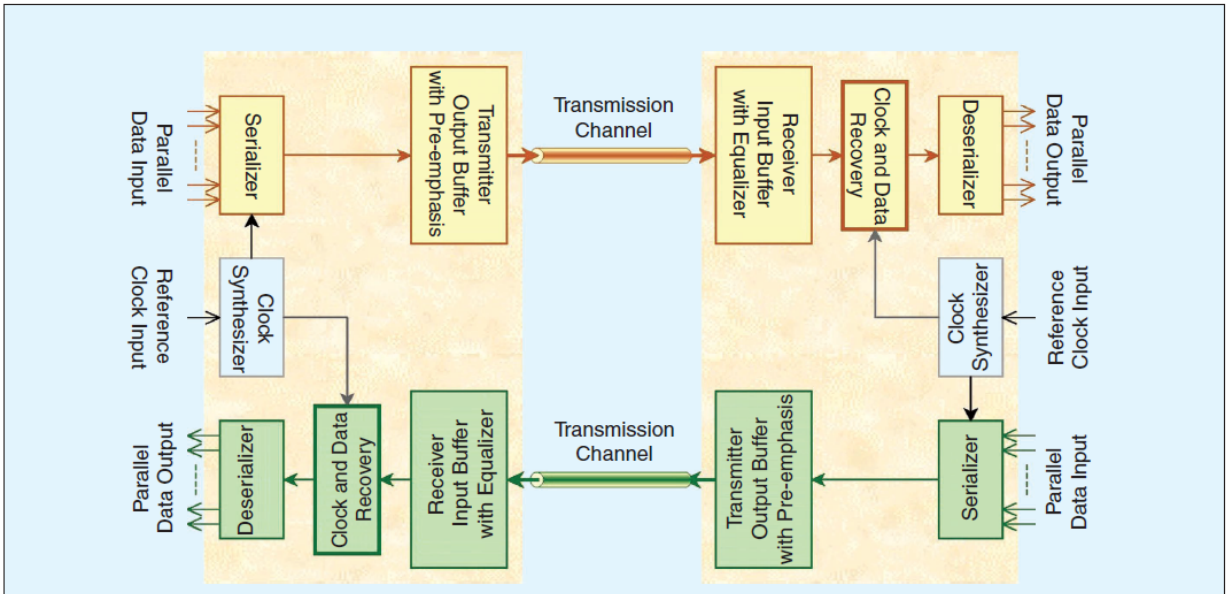


Figure 3. Block diagram of a generic high-speed wire-linked transmission system.

95. With reference to the figure above, the "Parallel Data Input" shown at the top left of the figure enters the "Serializer" block." The signal conveying the "Parallel Data Input" may be in a variety of forms, for example, Non Return to

Zero (NRZ), Pulse Amplitude Modulation 4 (PAM4), BPSK, QPSK, etc. At this point, the signal conveying the "Parallel Data Input" is an analog signal, into which the underlying digital information (*e.g.*, "1" and "0") is modulated. Then, multiple streams of "Parallel Data Input" is multiplexed by the "Serializer" block (at the top left of the figure in yellow), creating a single stream of modulated data.

96. The serialized data stream, which is output from the "Serializer" block, is entered into the "Transmitter Output Buffer with Pre-emphasis" block. The "Transmitter Output Buffer with Pre-emphasis" block then pre-emphasizes the serialized data stream and transmits the pre-emphasized serialized data stream over the "Transmission Channel."

97. At the receiver, the "Receiver Input Buffer with Equalizer" block received the transmitted signal, which is likely to have been distorted by the channel. The "Receiver Input Buffer with Equalizer" block at the receiver equalizes the distortion in the received signal. Then, the Clock and Data Recovery" block attempts to recover the originally transmitted serialized data stream as shown in Figure 2 of Hsieh. The final step in the receive sequence is the "Deserializer" block, which demultiplexes the recovered serialized data stream into multiple parallel data streams for subsequent output as streams of modulated digital data.

98. The block diagram of a generic high-speed wire-linked transmission system shown in Figure 3 of Hsieh describes various processes performed between a pair of transmitter and receiver. This generic block diagram of Hsieh has cross relationship with the embodiment disclosed in the '252 patent. For example, the following is FIG. 5 of the '252 patent, which "is a block diagram of a transmitter in an illustrative multi-lane transceiver." EX1001, 3:27-28.

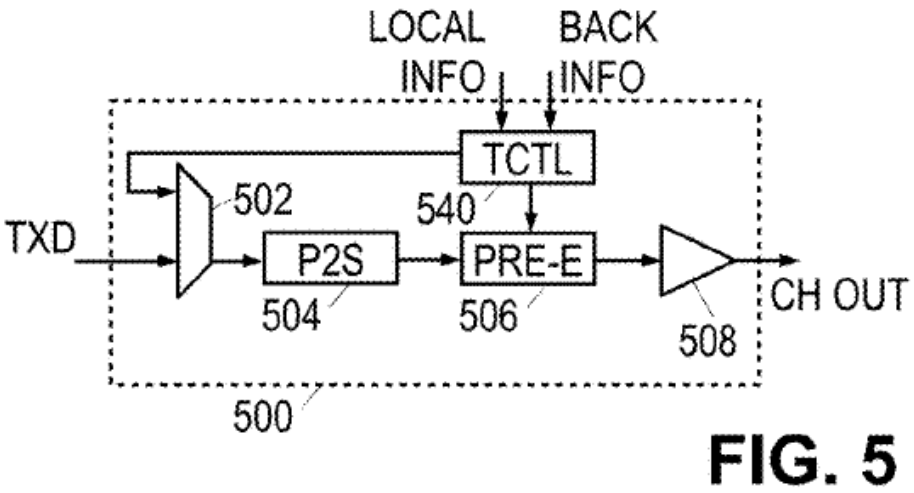
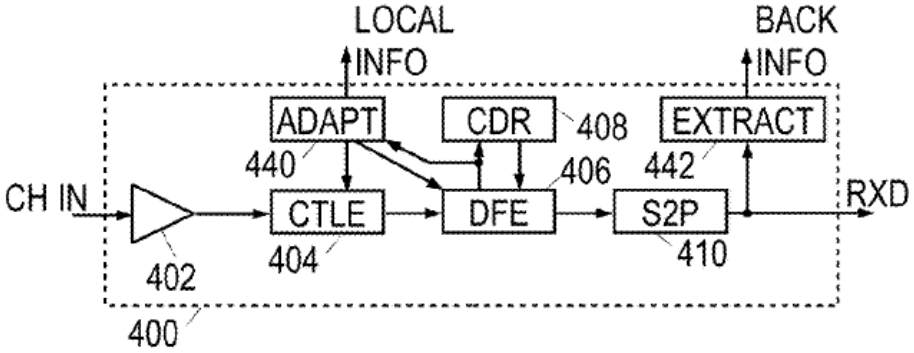


FIG. 5

99. Setting aside the "LOCAL INFO" and "BACK INFO" portions of the block diagram, which are used for configuration of the pre-emphasis function performed by "PRE-E" 506, the "P2S" block 504 performs parallel to serial conversion, which is performed by the "Serializer" block in Figure 3 of Hsieh and the "PRE-E" block 506 perform pre-emphasis function, which is performed by the "Transmitter Output Buffer with Pre-emphasis" block in Figure 3 of Hsieh.

100. Similarly, the following is FIG. 4 of the '252 patent, which "is a block diagram of a receiver in an illustrative multi-lane transceiver." (EX1001, 3:25-26.)

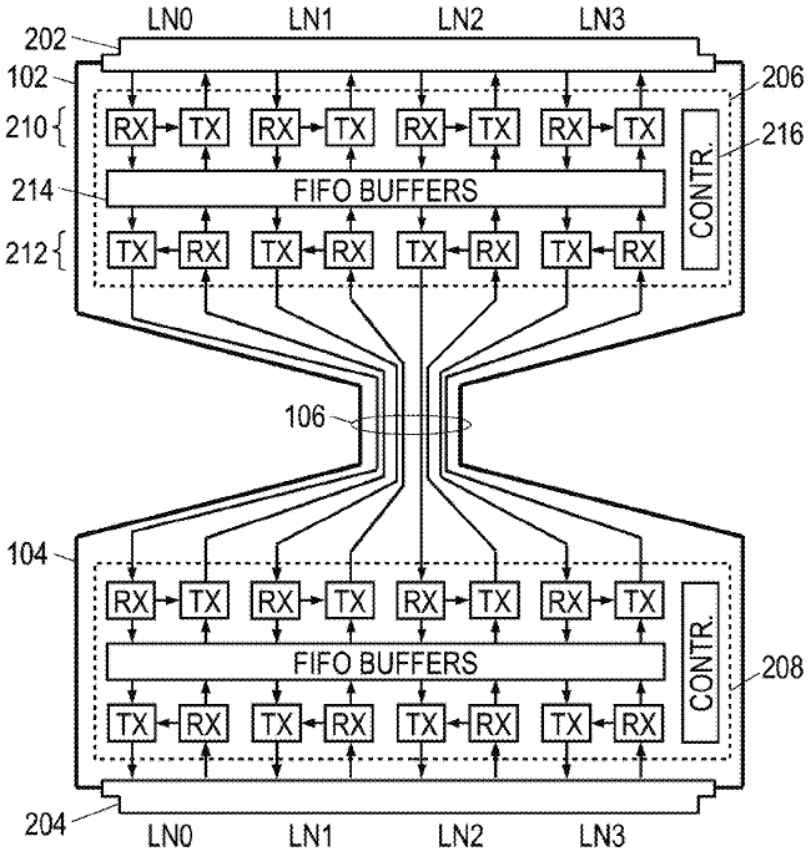
FIG. 4



101. Again, setting aside the "LOCAL INFO" and "BACK INFO" portions of the block diagram, which are used for configuration of the equalization functions performed by "CTLE" 404 and DFE 406, the "CDR" block 408 performs clock and data recovery function, which is performed by the "Clock and Data Recovery" block in Figure 3 of Hsieh, and the "CTLE" and "DFE" blocks together perform the equalization function, which is performed by the "Receiver Input Buffer with Equalizer" block in Figure 3 of Hsieh. Finally, the "S2P" block 410 performs the serial to parallel conversion, which is performed by the "Deserializer" block in Figure 3 of Hsieh.

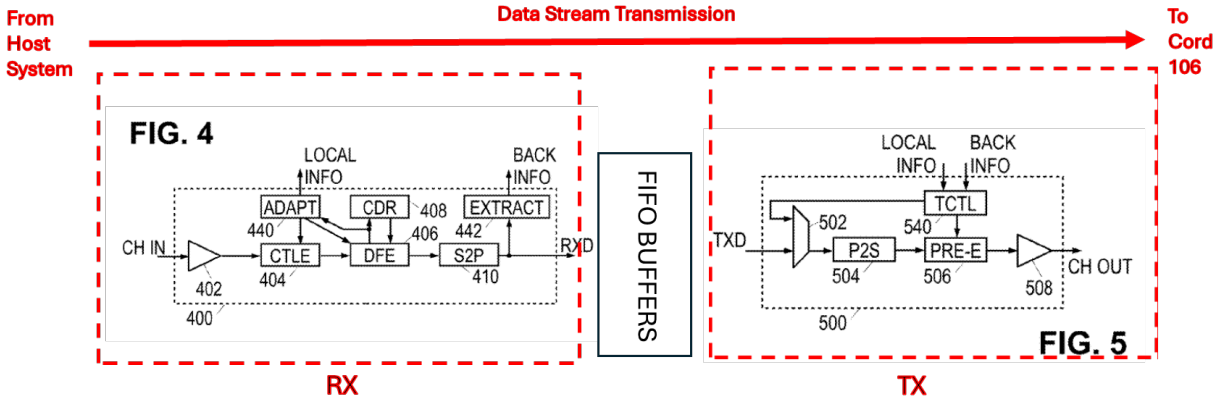
102. The '252 patent discloses an "active Ethernet cable" (EX1001, 3:19-20), as part of the "function-block" diagram of the illustrative cable" (EX1001, 3:21-22), plug 202 "adapted to fit a standard-compliant Ethernet port (EX1001, 4:28-29), as shown in FIG. 2 below.

FIG. 2



103. As shown in the figure above, plug 202 has multiple receivers and transmitters in sets 210 and 212. In particular, when plug 202 receives a data stream on one of the lanes, the data stream goes through one of the receivers and one of the transmitters before the data stream is transmitted onto the cable cord 106. For example, the data stream received on the left most lane, *i.e.*, LN0, it goes through the leftmost RX among the receivers 210 and the leftmost TX among the transmitters 212.

104. In the context of FIG. 4 and FIG. 5, which respectively illustrates the RX and the TX shown in FIG. 2 above, the following figure shows the processes, to which the data stream to be transmitted is subject.



105. In the figure above, the "S2P" block in RX (FIG. 4) and the "P2S" block in TX (FIG.5) negate each other – the serial to parallel conversion by the "S2P" block negates the parallel to serial conversion by the "P2S" block. The center of the overall transmission path shown in the figure above is the "CDR" 408 (FIG. 4), which restores the data stream transmitted from the host system, which is distorted by the channel formed over the path comprising the package of the IC where the data stream is originated, through the electrical trace over the printed circuit board on which the IC is mounted, to the connector on the plug, and to the "CH IN" shown in FIG. 4. Once the data stream is recovered by the "CDR" block 408, the data stream is pre-emphasized by the "PRE-E" block 506 in FIG. 5 in preparation for the transmission over the cord 106.

V. PRIOR-ART REFERENCES

106. I briefly introduce in this section various prior-art references discussed in this declaration.

A. Lugthart-993 (EX1005)

107. Lugthart-993 is titled "Timing Recovery in a High Speed Link." Lugthart-993 is directed to "[s]ystems and methods for high speed communications" that "include innovative transceiver architectures and techniques for re-timing, multiplexing, de-multiplexing and transmitting data." Lugthart-993, Abstract.

108. According to the face of the document, Lugthart-993- is a United States Patent issued on May 10, 2016 as Patent No. 9,337,993 from its Application No. 14/582,930, which was filed on December 23, 2014. I have been informed by counsel that Lugthart-993 qualifies as prior art to the '252 patent based on Lugthart-993's issuance date. *See also* Section VI.A.1 (additional discussion of Lugthart-993).

B. Aronson (EX1006)

109. Aronson is titled "Active Optical Cable with Integrated Control Features." Aronson is directed to "[a]n active cable" with circuitry to provide "pre-emphasis" and/or "equalization" of electrical signals. Aronson, Abstract.

110. According to the face of the document, Aronson (EX1005) is a United States patent issued on July 27, 2010 as Patent No. 7,762,727 from an application

filed on October 31, 2008 noted as Application No. 12/262,872. I have been informed by counsel that Aronson qualifies as prior art to the '252 patent based on Aronson's issuance date. *See also* Section VI.A.2 (additional discussion of Aronson).

C. Tang (EX1007)

111. Tang is titled "System and Method for Providing a Visual Indicator for Cables." Tang is directed to a "data cable… that includes an indicator." Tang, Abstract.

112. According to the face of the document, Tang (EX1006) is a United States Patent Application Publication published on May 9, 2013 as Publication No. 2013/0115803, which was filed on November 9, 2011 as Application No. 13/292,846. I have been informed by counsel that Tang qualifies as prior art to the '252 patent based on Tang's publication date. *See also* Section VI.B.1 below (additional discussion of Tang).

D. TI-Retimer (EX1008)

113. TI-Retimer is titled "DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer." TI-Retimer is directed to Texas Instruments Corporation's DS125DF1610 retimer, which is a "sixteen-channel multi-rate retimer with integrated signal conditioning features." TI-Retimer, §3.

114. According to the face of the document, TI-Retimer (EX1007) is identified as datasheet SNLS482B last revised January 2017. I have been informed by counsel that TI-Retimer was publicly available on Texas Instruments' website as early as March 6, 2017 and qualifies as prior art to the '252 patent based on that date. Section VI.B.2 below (additional discussion of TI-Retimer).

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE IN LIGHT OF THE PRIOR ART

115. I have been asked to provide my opinion concerning whether claims 1-14 of the '252 patent would have been obvious to a POSA in light of the prior-art references discussed below. For the reasons explained below, it is my opinion that each of claims 1-14 would have been obvious to a POSA. The following table summarizes the Grounds I discuss in the sections below (independent claims have been indicated in **bold** in the table below):

Ground	Reference(s)	Claims	Basis
1	Lugthart-993 (EX1005) + Aronson (EX1006)	**1**-5, **6**-10, **11**-14	obviousness
2	Tang (EX1007) + TI-Retimer (EX1008) + Aronson (EX1006)	**1**-4, **6**-9, **11**-14	obviousness

A. Ground 1: Lugthart-993 in view of Aronson Renders Obvious Claims 1-14

116. As explained in this section below, in my opinion claims 1-14 of the '252 patent would have been rendered obvious over Lugthart-993 in view of Aronson.

1. Discussion of Lugthart-993 (EX1005)

117. Lugthart-993 "relates to methods and systems for high-speed point-to-point communications" used, for example, in data centers. Lugthart-993, 1:32-50. One aspect of Lugthart-993's system is a clock and data recovery (CDR) circuit that "digitize[s]… incoming signals as well as… implement[ing] timing recovery to recover a clock and a data signal." Lugthart-993, 9:6-17, 21:6-15. Lugthart-993's exemplary CDRs include separate data and clock recovery paths that operate at different resolutions to enhance performance with fast lock times and high data recovery accuracy. Lugthart-993, 31:6-45.

118. Lugthart-993 describes implementing such CDR circuits in the ingress and egress paths of transceivers, for example as part of an "active cable" that includes "first and second transceiver assemblies 105a, 105b" connected via conductive lines 111, each transceiver assembly including a respective transceiver 107a, 107b. Lugthart-993, 14:3-26, 15:14-23, Fig. 2A (below). Cable 110 connects electronic devices 101a, 101b ("host devices"), such that transceiver assemblies 105a, 105b each have electrical connections on "host sides" and "line sides."

Lugthart-993, 13:49-14:16.

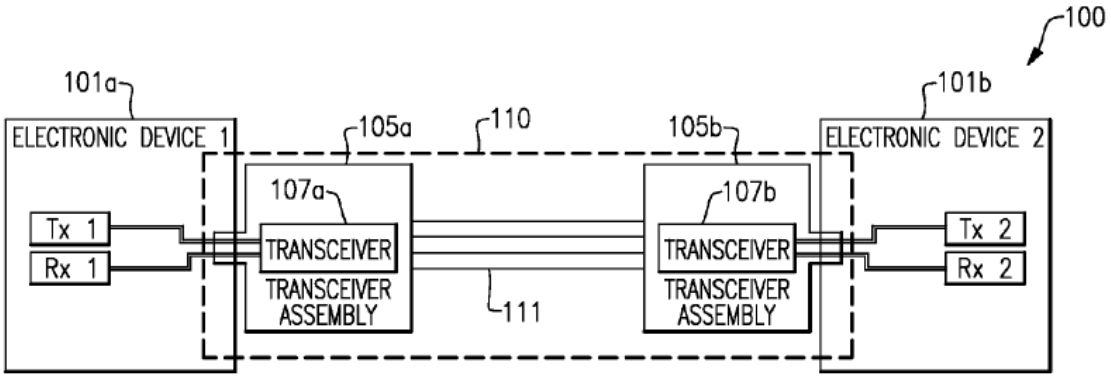


FIG.2A

119. Lugthart-993 Fig. 1A (below) illustrates exemplary processing by a transceiver 10 for data over an "EGRESS/TRANSMIT" path (from host to line/cable) and over a "INGRESS/RECEIVE" path (from line/cable to host). Lugthart-993, 7:49-8:14. While one transceiver 10 is shown, it is understood that a cable, for example as shown in Figs. 2A, 4A and elsewhere in Lugthart-993, will include transceivers in each transceiver assembly. Lugthart-993, 14:21-26, 14:64-15:1.

120. In the EGRESS/TRANSMIT path in Fig. 1A, equalizers 11a, 11b receive host side transmit data (TX DATA) and provide "equalization to compensate for transmission line losses on the host side." Lugthart-993, 7:63-67, 8:60-62. The equalizer outputs are next received by CDR circuits 12a, 12b, which "recover data in data streams generated by the first and second transmit path equalizers." Lugthart-993, 7:63-67, 9:15-18. A digital signal processor (DSP) 13

follows CDR circuits 12a, 12b and includes feed-forward equalizer and/or decision feedback equalizers (FFE/DFE) 15a, 15b, a physical coding sublayer (PCS) block 16, and finite impulse response (FIR) filter 17. Lugthart-993, 7:67-8:2, 9:19-31.

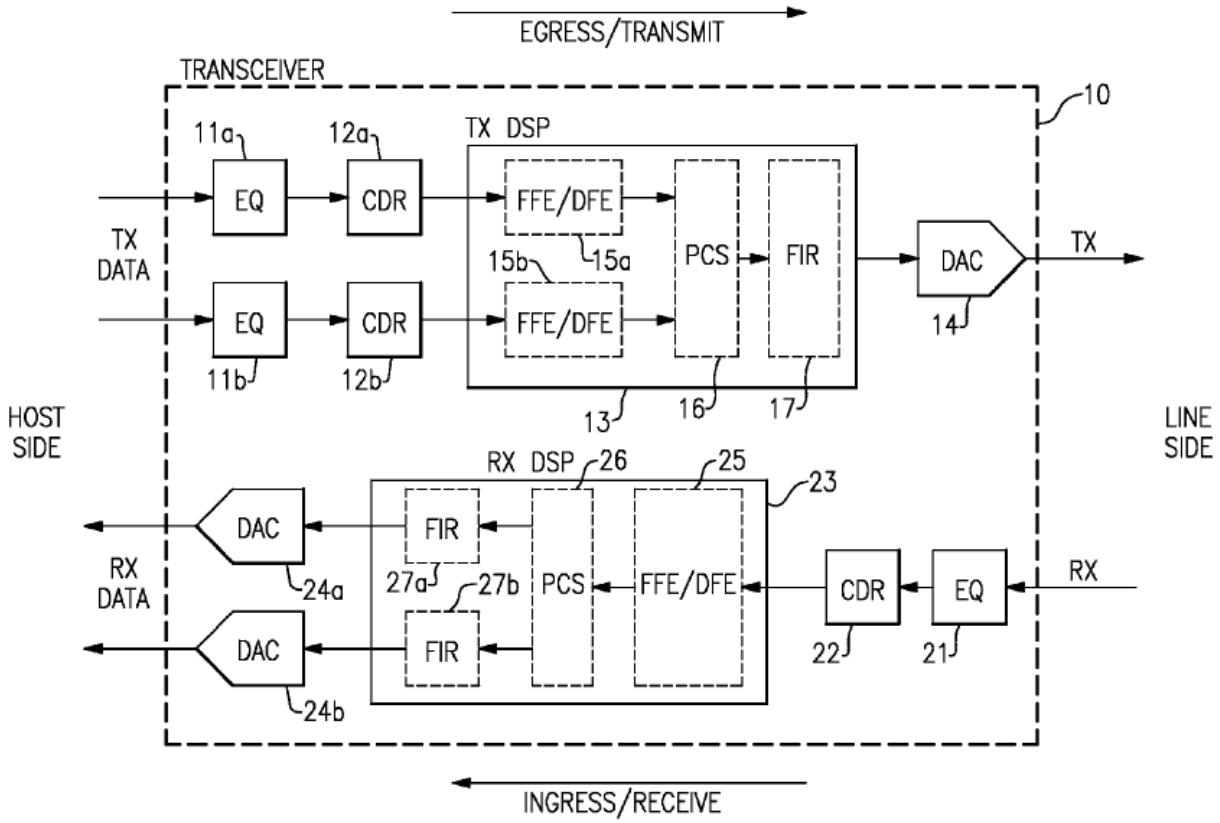


FIG.1A

121. Equalizer 11a, CDR 12a, and FFE/DFE 15a may, together, be functionally considered part of an overall CDR system 500, wherein CDR circuit 502 corresponds to CDR 12a shown in Fig. 1A above. Similarly, equalizer 11b, CDR 12b, and FFE/DFE 15b may be functionally considered another CDR system 500. Lugthart-993, Fig. 10 (below), 34:29-43.

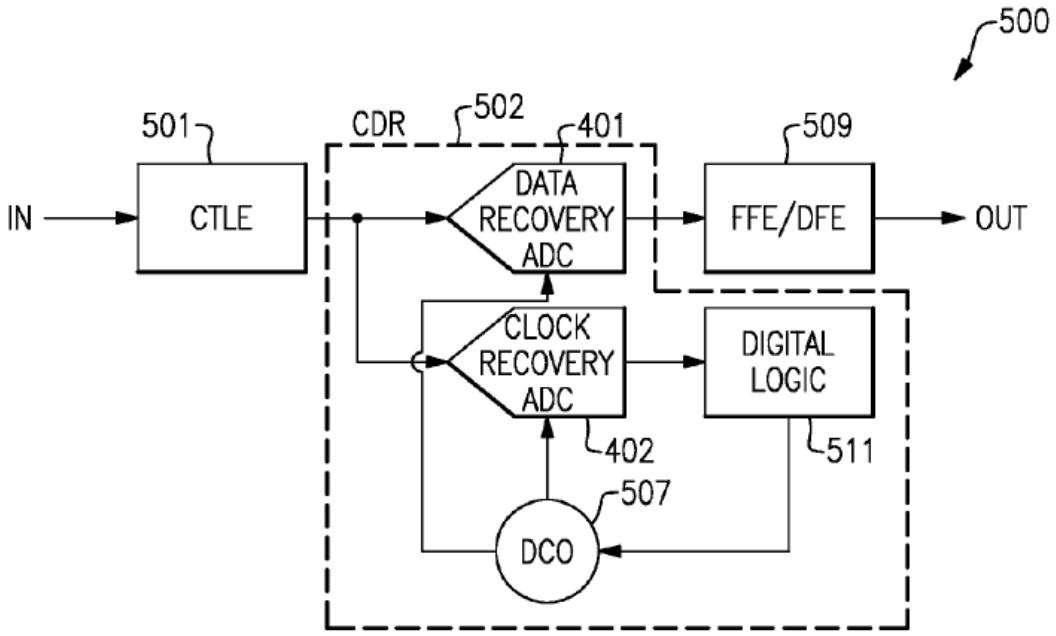


FIG.10

122. As shown in Fig. 10, the CDR system receives an analog input signal IN and first equalizes the signal for distortions (by CTLE 501), after which digital signals and clocks are recovered (by ADCs 401, 402) by aligning sampling clock signals (from digital controlled oscillator (DCO) 507) to the input signal and generating a digital representation of the analog input signal. Lugthart-993, 34:54-35:26. The recovered data is input to FFE/DFE509 for conditioning as output signal OUT. Lugthart-993, 35:27-32.

123. In Fig. 1A, PCS block 16 performs various processing functions, including framing, error correction, and mapping (*e.g.*, from multiple NRZ-encoded channels into a single PAM-4-encoded channel). Lugthart-993, 23:4-19. FIR filter 17 conditions the signal for output and provides compensation for

channel losses. Lugthart-993, 23:20-30. DAC 14 converts digital signals in the form of, for example, PAM-4, NRZ, duobinary, DPSK, PSK, etc., to analog signal for output. Lugthart-993, 21:49-56, 23:20-30.

124. As shown in Fig. 1A, the transceiver includes analogous components in both the EGRESS/TRANSMIT and INGRESS/RECEIVE path directions: EQs 11a/11b and 21, CDRs 12a/12b and 22, DSPs 13 and 23, FFE/DFEs 15a/15b and 25, PCSs 16 and 26, FIR filters 17 and 27, and DACs 14 and 24a/24b. Although I reference the EGRESS/TRANSMIT path components above (EQ 11a/11b, CDR 12, DSP 16), the INGRESS/RECEIVE path components (EQ 21, CDR 22, DSP 26) are configured to perform analogous functions. Lugthart-993, 7:49-8:14, 8:58-10:8, 23:31-43. For example, transmit equalizers 11a, 11b "compensate for transmission line losses on the host side," while receive equalizer 21 "compensate[s] for transmission line losses on the line side." Lugthart-993, 8:58-67.

125. Fig. 4A (below) illustrates exemplary communications between two hosts via respective cable transceivers 10a, 10b and cable 205 therebetween. Lugthart-993, 19:1-11.

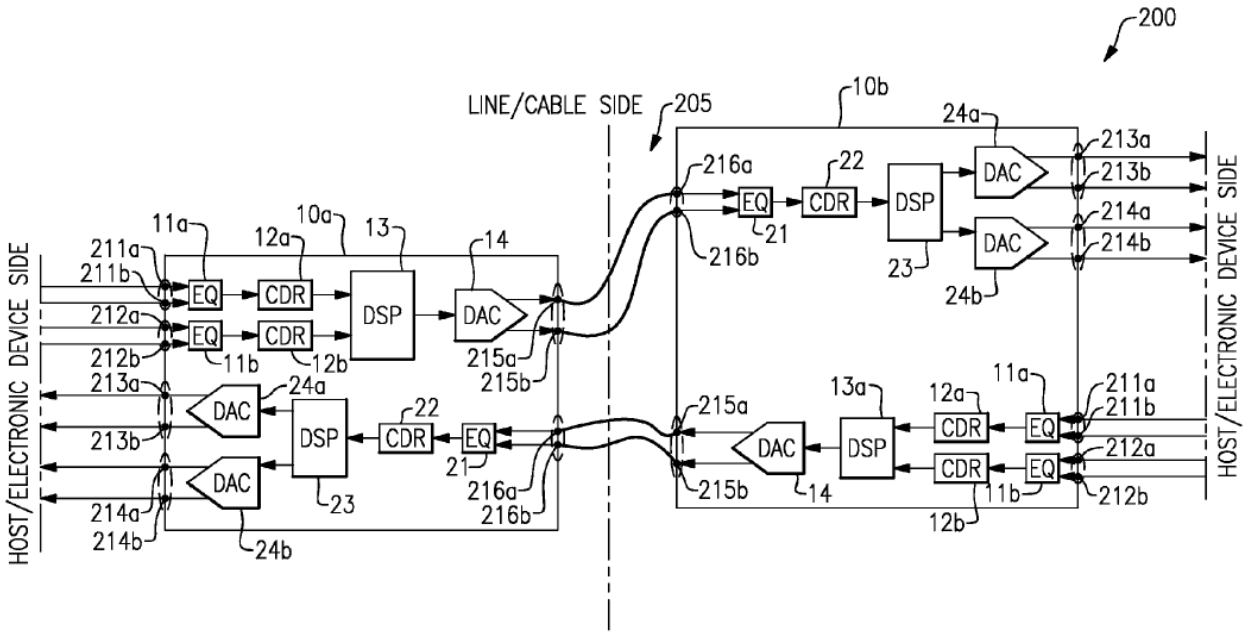


FIG.4A

2. Discussion of Aronson (EX1006)

126. Aronson, like Lugthart-993, is directed to an active cable for bi-directional high speed transmissions between network nodes, including integrated circuits providing pre-emphasis and equalization signal processing functions. Aronson, Abstract, 1:12-21. Aronson describes various high bandwidth links using copper-based and/or optical fiber-based solutions. Aronson, 1:29-2:24, 2:29-33, 7:17-20.

127. Figs. 12A-12B (below) illustrate a copper-based cable including "useful features which might be incorporated into the ICs in a copper active cable design." Aronson, 14:16-15:24.

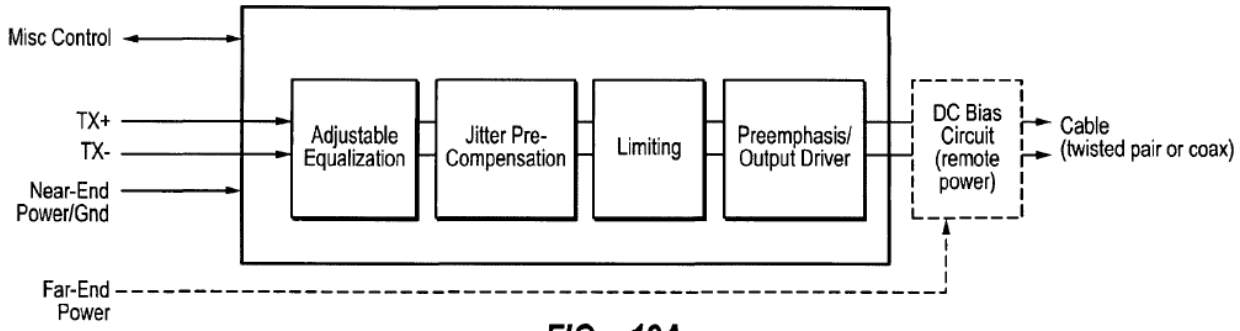


FIG. 12A

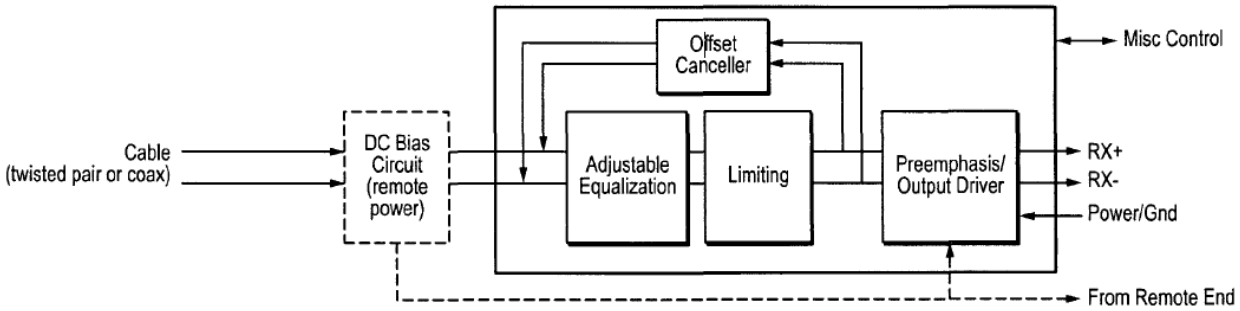


FIG. 12B

128. The transmitter of Fig. 12A and the receiver of Fig. 12B each include a number of signal processing blocks, and both include "Adjustable Equalization" and "Pre-emphasis/Output Driver" at each end.

129. For the transmitter of Fig. 12A that transmits signals over the cable (right side of figure), equalization is performed "to compensat[e] for high frequency loss in the host board traces," while pre-emphasis is performed to "overcome the larger loss on the cable of… high frequencies" and can be adjusted to "match the particular length [and] characteristics of the copper cabling." Aronson, 14:19-21, 14:33-43. For the receiver of Fig. 12B that receives signals over the cable (left side of figure), equalization is performed "to compensate for

the cable high frequency rolloff, rather than the host PCB traces," while pre-emphasis is performed to "overcome high frequency losses on long PCB traces." Aronson, 15:1-4, 15:17-21.

130. Aronson describes that the "pre-emphasis and/or equalization can be fixed, adjustable, or adaptable," and other variations such as being host selectable or factory set. Aronson, Abstract, 14:21-23, 14:36-39, 15:4-8, 15:21-24. Thus, the different combinations of equalization, pre-emphasis, fixed parameters, adaptive parameters, etc., were known, including adaptive pre-emphasis. Aronson, Abstract (active cable "pre-emphasis… can be fixed, adjustable, or adaptable" for pre-emphasis of electrical signals). These design choice options were well-known to POSAs. *See*, *e.g.*, EX1019, 13:47-51 ("Pre-equalizers… adjust the amplitude and phase response of the outgoing symbols either based on an approximation of the twisted pair cable length, or based on an adaptive technique").

3. Discussion of the Lugthart-993+Aronson Combination

131. As noted above in Sections VI.A.1-2, both Lugthart-993 and Aronson teach active Ethernet cables with signal conditioning functions. I further reference this combination as "Lugthart-993+Aronson."

a. Reasons to Combine

i. Fixed Cable-Independent Parameters for Host-Side Equalization

132. On the EGRESS/TRANSMIT path, Lugthart-993's transceivers equalize the signals conveying inbound data stream TX, using equalizers 11a/11b, to "compensate for transmission line losses on the ***host*** side." Lugthart-993, 8:58-9:5, Fig. 1A (annotated below). *See* my discussion of [1.C] below.

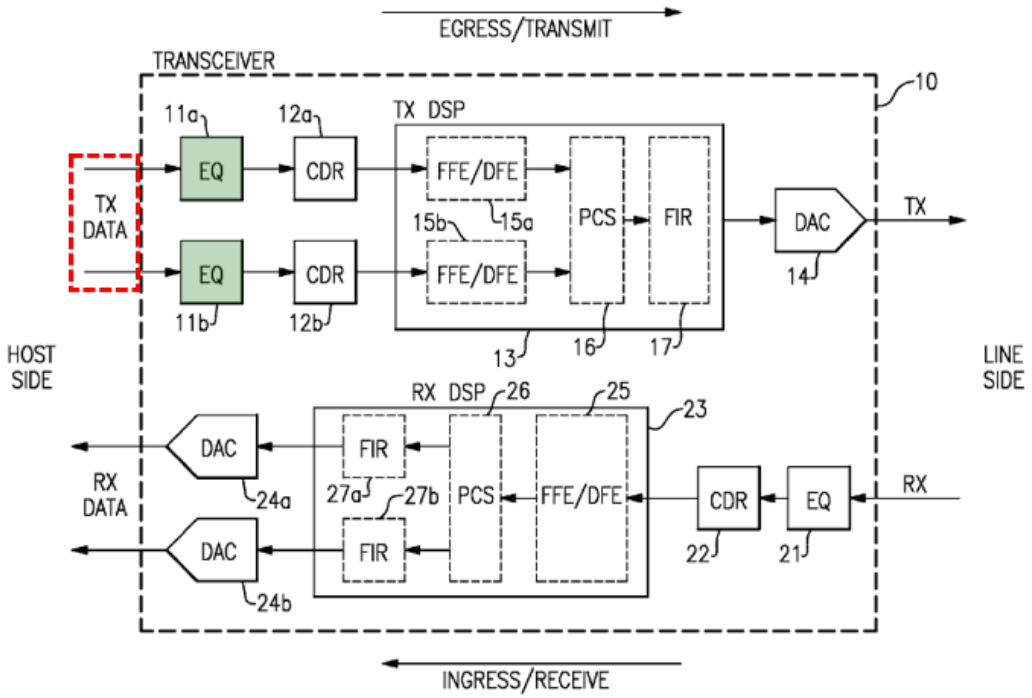


FIG.1A

133. On the INGRESS/RECEIVE path, DSP 23's FIR filters 27a/27b ("FIRs 27a/27b") pre-equalize the signals conveying outbound data stream RX, thereby pre-compensating for ***host-side*** distortion/losses on a line-side data stream

that was already equalized for line-side losses by equalizer 21. Lugthart-993, 8:58-60. *See* my discussion of [1.C]-[1.D] below.

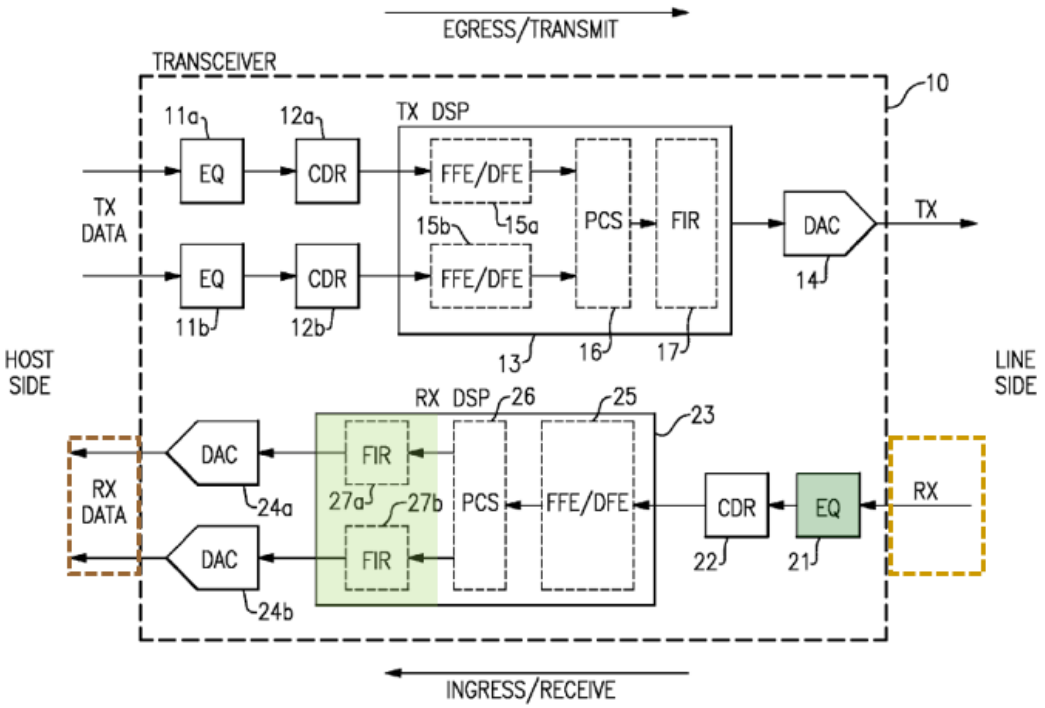


FIG.1A

134. Because of CDR functionality recovering signals prior to cable-side output in the egress path (via CDRs 12a/12b and FFE/DFEs 15a/15b; for example as I discuss for [1.C] below) and after cable-side reception in the ingress path (via CDR 22 and FFE/DFE 25; for example as I discuss for [1.D] below), POSAs understood that for equalizers 11a/11b and FIRs 27a/27b to compensate for ***host-side*** distortion/losses, each would employ equalization parameters based on the characteristics of the host interface, and not a cable on the line side (from which

they are separated by CDR processes), such that they would be "*cable-independent*" per the '252 patent.

135. However, Lugthart-993 does not expressly state that the cable-independent parameters are fixed—which is why the Examiner appeared to allow the claims. *See* my discussion in Section IV.B above.

136. To the extent Lugthart-993 is considered to not expressly teach or suggest using ***cable-independent*** parameters for pre-equalizing and equalizing signals to and from the host, Aronson does. Aronson also teaches that these cable-independent parameters are ***fixed***. The cable's transmitter Integrated Circuit (IC) in Aronson Figure 12A (below) performs *cable-independent* equalization on inbound data stream TX+/TX- to "compensat[e] for high frequency loss in the ***host board traces***." Aronson, 14:16-23. Host board traces are independent of the cable, so parameters compensating for them are cable-independent. While Figure 12A labels the block as "adjustable" equalization, "[s]uch equalization could be ***fixed***." Aronson, 14:20-23.

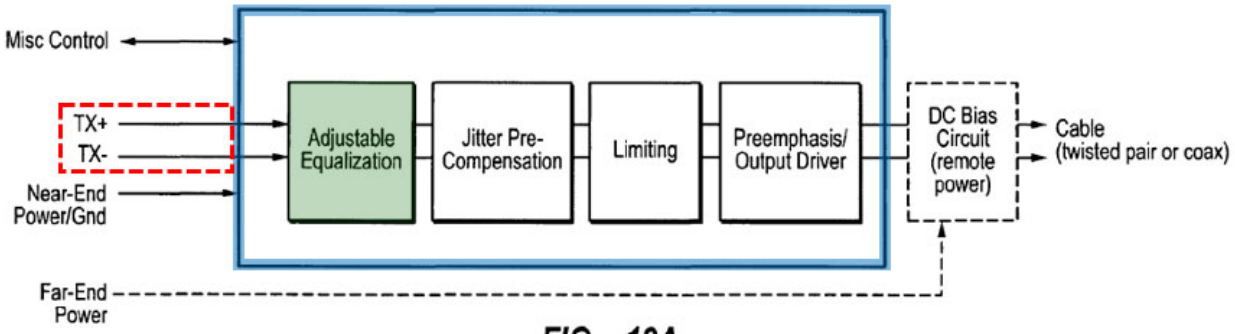


FIG. 12A

137. The cable's receiver IC in Aronson Figure 12B (below) generates outbound data stream RX+/RX- to the host in several steps or functional blocks, including by performing equalization in a pre-emphasis/output driver that drives "***host PCB traces***." Aronson, 15:1-8. Pre-emphasis is the term typically used to describe altering a signal for output, and equalization is typically used to describe altering a signal that has been received, but pre-emphasis was another term for pre-equalization. EX1022, 2:39-41. Pre-equalizing outbound stream RX+/RX- addresses "losses on ***long PCB traces***" and "could be ***fixed***." Aronson, 15:17-24. The PCB traces are on the host (Aronson, 15:1-8 ("host PCB traces")) so pre-equalization parameters addressing them are cable-independent.

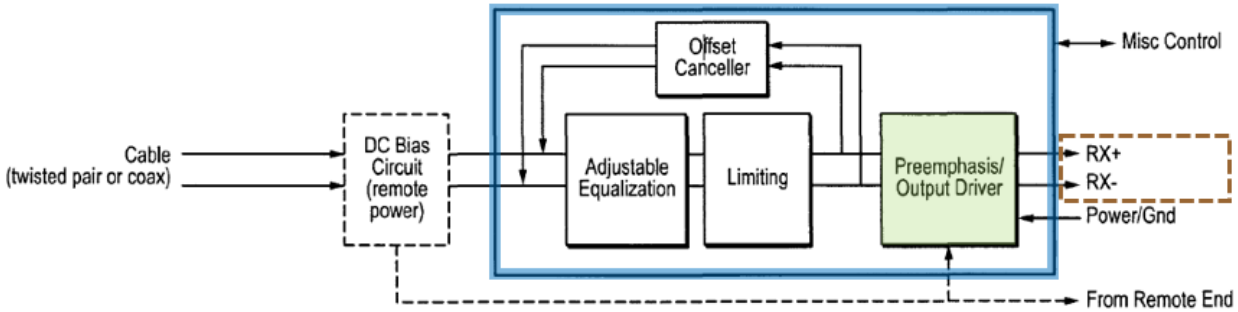


FIG. 12B

138. Aronson's teachings to use ***cable-independent*** parameters to perform equalization compensating for ***host-side losses*** gave POSAs reason to implement Lugthart-993 in the same manner.

139. POSAs understood that there were tradeoffs between fixed and adaptive equalization for a communication channel, such as the host interface of an

active copper cable. Aronson, 15:17-24. These tradeoffs were made, for example, with respect to accuracy, speed, manufacturing cost, and complexity, and POSAs were well aware of these tradeoffs and would have chosen between fixed and adaptive equalization depending on the specific system at hand. EX1016, 1:7-18 (discussing slow convergence with adaptive equalization); EX1011, [0009]-[0011] ("[f]ixed equalization is common," discussing tradeoffs between fixed and adaptive equalization); EX1017, 1:52-55 ("Conventional adaptive equalization has generally required substantial overhead, i.e. large gate count, which has translated into high chip costs."); EX1014, [0034] ("The adaptive equalizer can be trapped in a failure state (*i.e.*, incorrect state) and not able to recover from the failure state."); EX1024, [0058] ("[E]qualization techniques… come with different engineering tradeoffs, including trade-offs in power consumption, performance, and/or cost.").

140. A POSA's background knowledge of these well-known tradeoffs between fixed and adaptive parameters would have given POSAs additional reasons—beyond Aronson's specific teaching to use fixed parameters—to make the design choice to fix the cable-independent equalization parameters in Lugthart-993's equalizers 11a/11b and DSP 23's FIRs 27a/27b. In light of a POSA's understanding about the particular environment in which a cable assembly is used, the POSA can elect to use a cable assembly with fixed equalization parameters on the host-side of the transceiver. For example, in a data center with stacks of

servers, cable assemblies with fixed equalization parameters on the host-side of the transceiver may be preferred. This is because the data centers are typically environmentally controlled (*e.g.*, temperature and humidity controlled), and as such the channel characteristics between from the host system (*e.g.*, server) to the transceiver in the cable assembly may be relatively constant over time compared to the longer distances between cable assembly transceivers, which may also be bundled together with a large number of other cable assemblies. *See also* my discussion of adapting line-side parameters in Section VI.A.3.a.ii below. In this case, reducing the power consumption by not performing real-time adaptive equalization on the host-side of the transceiver may be preferred. Moreover, the cable assemblies with fewer adaptive equalization components would be simpler to implement and would be less costly.

141. The '252 patent says the cable-independent parameters are fixed "[i]n ***at least some*** contemplated embodiments." EX1001, 4:60-64. Thus, the cable-independent parameter need not be fixed in all embodiments. The '252 patent does not explain how or why one would use either fixed or adaptive parameters in any of its cable embodiments. There is nothing critical or inventive about fixing the cable-independent parameters—the inventors claimed one of the known, obvious, design choices.

142. The use of fixed cable-independent parameters to compensate for host-side losses is a combination of known prior art elements in Lugthart-993 and Aronson that the yield predictable result of compensating for host-side losses. These techniques—fixed equalization parameters; equalization parameters that compensate for hosts—were known in the art and known for the same usage described in the '252 patent.

ii. Cable-Dependent Parameters For Line-Side Equalization

143. Lugthart-993's DSP 13 uses FIR 17 to "perform [pre-]emphasis on the signal to compensate for channel losses" over the cable (*e.g.*, on the transceiver's line-side). Lugthart-993, 23:4-30, Fig. 1A (annotated below). Lugthart-993's equalizer 21 "provide[s] signal equalization to compensate for transmission line losses on the line side." Lugthart-993, 8:58-9:5; *see also* 22:4-9 (compensates for losses "over the cable"). POSAs understood that FIR 17 and equalizer 21 use "cable dependent" parameters because they compensate for losses over the cable (*e.g.*, "line side").

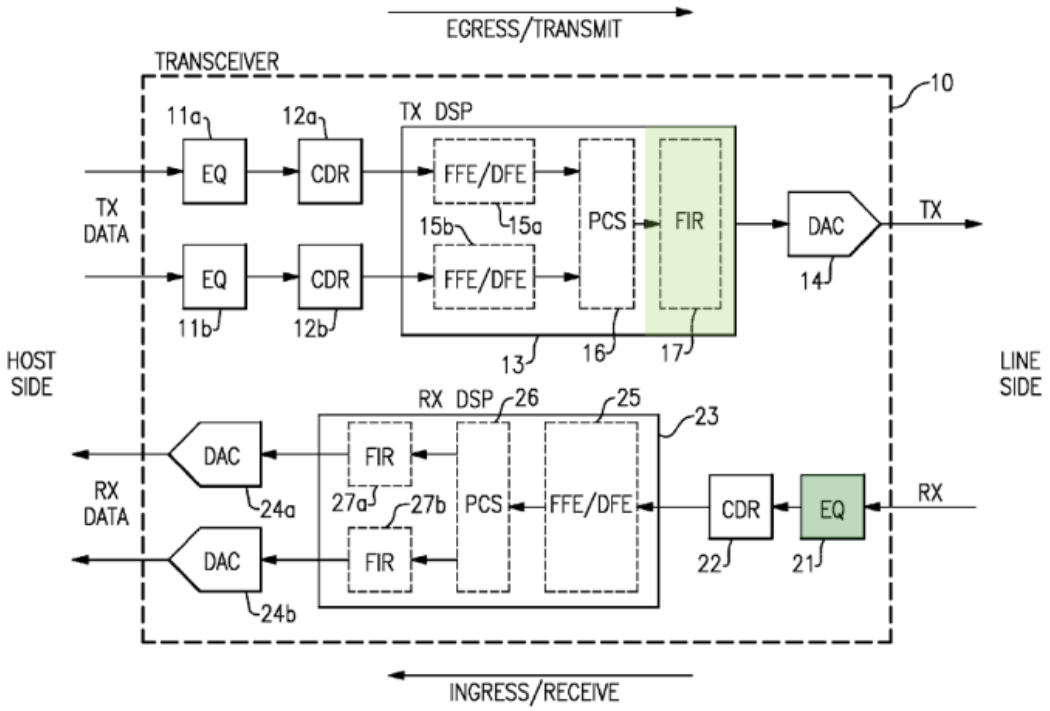


FIG.1A

144. To the extent Lugthart-993 is considered to not explicitly describe the equalization parameters used by FIR 17 and equalizer 21 as ***cable-dependent***, Aronson confirms that would have been the conventional and obvious way to implement Lugthart-993's equalization addressing cable-side losses. Specifically, Aronson's transmitter IC's line-side pre-emphasis/output driver overcomes "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling." Aronson, 14:33-43, Fig. 12A (annotated below). Similarly, Aronson's receiver IC equalizes received line-side signals to "compensat[e] for the cable" losses using cable-dependent parameters based on "cable length and characteristics." Aronson, 15:1-8, Fig. 12B (annotated below). Thus, POSAs recognized that transmitter equalization (or "pre-emphasis")

typically addressed losses in the channel prior to transmission (*i.e.*, in Fig. 12A, compensating for the cable before transmission over the cable), while receiver equalization typically addressed losses in the channel over which a signal was received (*i.e.*, in Fig. 12B, compensating for the cable losses after transmission over the cable).

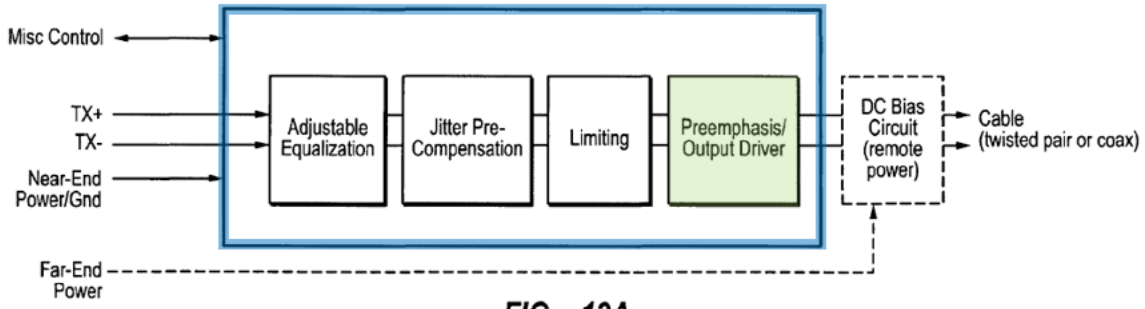


FIG. 12A

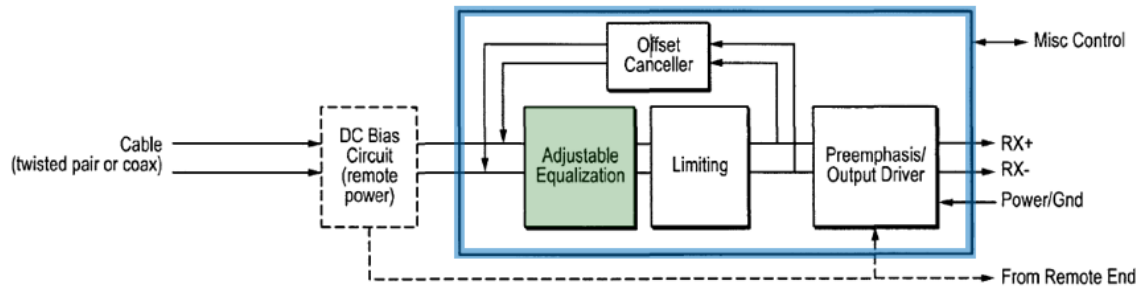


FIG. 12B

145. Aronson's express teachings to use cable-dependent parameters to perform equalization on signals the cable transceiver transmits to, and receives over, the cable, gave POSAs reason to implement Lugthart-993 using cable-dependent equalization parameters in the same manner. Additionally, doing so was nothing more than combining known prior art elements from Luthgart-993 and

Aronson to yield the predictable result of equalizing line-side signals using cable-dependent parameters.

146. Aronson describes that it was a known design choice to set equalization parameters by fixing them or using an adaptive scheme. Aronson, 15:1-6. As explained below, POSAs had reasons to use either alternative.

(1) Adapting The Line-Side Cable-Dependent Parameters

147. It was well-known that equalization parameters could be adapted by adjusting them based on distortions to known training signals transmitted over the cable. *See*, for example, my discussion in Section IV.D.1. Lugthart-993 describes training phases during which the cable-dependent equalization parameters for DSP 13's FIR 17 and equalizer 21 are adapted as discussed for claim 3 below. To the extent Lugthart-993 is considered to not teach expressly that the equalization coefficients for DSP 13 and equalizer 21 are among the parameters adapted during Lugthart-993's training phases, POSAs had reasons to implement Lugthart-993 in this manner based on Aronson and a POSA's background knowledge of the benefits of adapting equalization parameters.

148. Aronson explains that "pre-emphasis and/or equalization can be fixed, adjustable or ***adaptable***." Aronson, Abstract. While Aronson's Abstract refers to pre-emphasis for electrical signals in an optical cable embodiment, POSAs understood that adaptation applies equally to Aronson's copper cable

embodiments, as in Figs. 12A-12B, and was well-known to POSAs. Aronson, Abstract, 3:62-65; 14:16-15:24; *see* EX1015, Abstract (adaptively adjusting transmitter equalizer settings), [0023] (exemplary cables including twin axial and coaxial copper cables), [0027] (describing "[a]daptive transmit equalization"). Indeed, Aronson is explicit that adjustable equalization in Figure 12B (annotated below) that "compensate[s] for the cable" losses can be "adaptive." Aronson, 15:1-7 (noting that adjustable factory set equalization is of "particular interest" because cable characteristics are established at manufacture but disclosing the alternative of "adaptive" equalization).

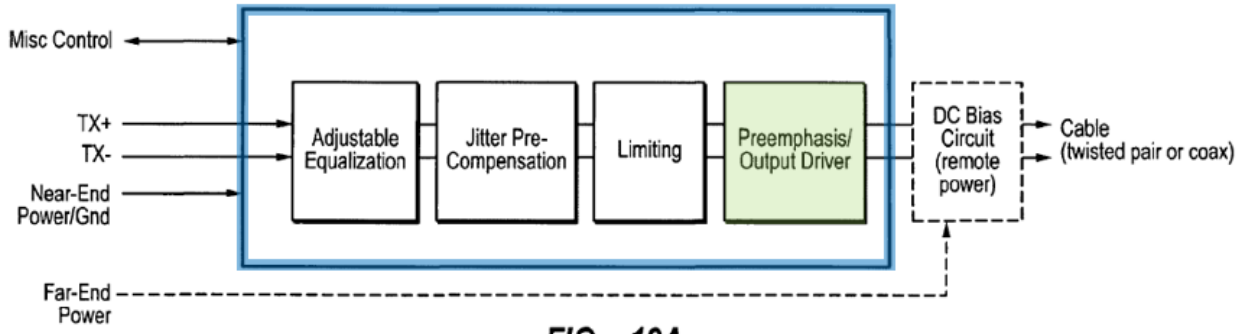


FIG. 12A

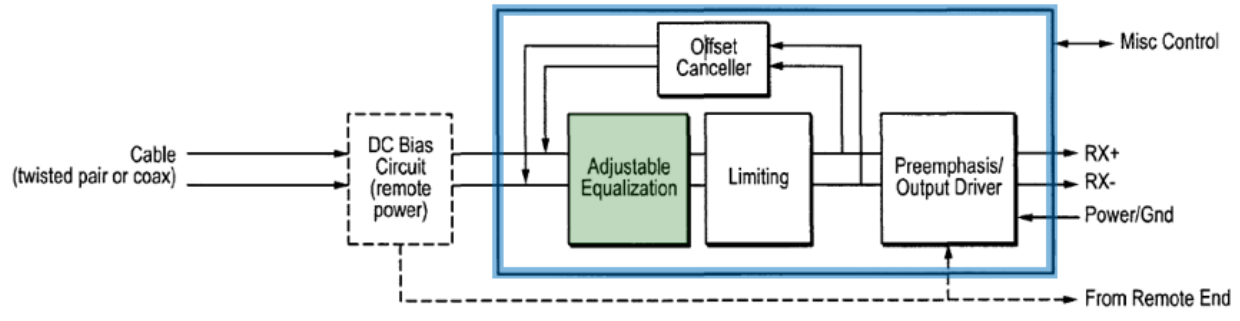


FIG. 12B

149. Thus POSAs understood that the pre-equalization by pre-emphasis/output driver (Figure 12A) is "adaptive" given Aronson's teachings that "pre-emphasis… can be… ***adaptable***" (Aronson, Abstract), and adaptive equalization can similarly be used for line-side losses (Aronson, 15:1-7).

150. Aronson's teaching of adapting cable-dependent equalization parameters gave POSAs reason to make the design choice to adapt the cable-dependent equalization parameters for Lugthart-993's DSP 13's FIR 17 and equalizer 21 during Lugthart-993's training phases, as it is during Lugthart-993's training phases that parameters for equalizers are adjusted. Lugthart-993, 47:67-48:27.

151. A POSA's knowledge of the benefits of using adaptive cable-dependent parameters in active copper cables like Lugthart-993's and Aronson's—including better compensation for conditions in use to yield better signal quality and lower error rates—gave POSAs additional reasons to make the design choice to make the cable-dependent parameters in Lugthart-993's FIR 17 and equalizer 21 adaptive during Lugthart-993's training phases. Lugthart-993, 47:56-48:27; EX1017, 1:39-51 (adaptive equalization yields "[b]etter signal quality and lower bit error rates" than "static equalization"); EX1015, [0027] ("Adaptive transmit equalization enables enhanced performance compared to fixed equalization," can support "a broader range of cable lengths" and "tolerances," can "simplif[y]

receiver design," and "may save [transmitter] power… by using power back-off," compared to fixed transmit equalization or receiver equalization).

152. It was known that environmental conditions like temperature, bending and vibration can impact signal transmission through a cable and that adaptive equalization was used to compensate for such environmental conditions that may differ from a factory-testing environment. EX1024, [0057] (inter-symbol interference changes over time based on environmental conditions like temperature, physical bending, vibrations); EX1018, 2:5-11, 3:16-17 (adaptive equalization can compensate variations in channel distortion from changes in humidity, temperature, and power); EX1017, 1:39-51 ("Conventional adaptive equalization… is… better able to compensate for unpredictable and time-dependent distortion [than static equalization]."). POSAs also understood that these various environmental conditions may have a greater impact on the cable than on host traces (*e.g.*, because host components may be better secured) and thus lead a POSA to choose adaptive cable-dependent parameters while choosing fixed cable-independent parameters for host-side losses as described above. I note that the line-side channel is subject to more variations than the host-side. As explained above, the host-side channel is likely to be stable over time in environmentally controlled data centers, as the host-side channel is formed from one cable connector mating with one port on the host system. On the other hand, the line-

side channel is formed across the entire length of the cable assembly, which is subject to interference and signal corruption as the cable assembly is likely to be bundled together with potentially a large number of other cable assemblies as the cable assembly is routed between the host systems. Each of the cable assemblies in the bundle of cable assemblies may have active components for processing, transmitting, and receiving signals, which can interfere and/or corrupt the signals on other cable assemblies through the inductive and/or capacitive coupling.

153. Using fixed (rather than adaptive) cable-dependent parameters was also a known obvious alternative as discussed above in Section VI.A.3.a.i and below in Section VI.A.3.a.ii.(2). The ’252 patent does not explain how or why one would use either fixed or adaptive parameters in any of its cable embodiments. The inventors claiming of both known alternatives does not render either non-obvious. *See* claims 3 (“adapt”) and 4 (“fixed”).

154. Using ***adaptive*** cable-dependent parameters in Lugthart-993’s FIR 17 and equalizer 21—trained during Lugthart-993’s training phases (Lugthart-993, 47:67-48:27) – would have been nothing more than combining prior art elements using known methods to yield the predictable results of cable-dependent equalization parameters that better compensate for the cable’s installed environment. These techniques—adaptive equalization parameters; equalization

parameters that compensate for cables—were known in the art and known for the same usage described in the ’252 patent.

(2) Line-Side Cable-Dependent Parameters Determined During Manufacture-Testing and Fixed During Normal Usage

155. While Aronson teaches the design choice of adapting the cable-dependent line-side equalization parameters, Aronson is explicit that line-side pre-equalization by the pre-emphasis/output driver and equalization on the received line-side signal in Figs. 12A-12B (below) can be determined during manufacturing-testing and then fixed. Aronson, 14:33-39 (Fig. 12A’s pre-equalization can be “adjusted at factory setup”), 15:1-7 (Fig. 12B’s equalization may be “fixed” and “[a]djustable but factory set” is of “***particular interest***”). That is, the relevant transceiver components parameters are not completely unchangeable—they are adjustable and, in this case, set by the manufacturer. After manufacture, when in use by the consumer, they are fixed. *See* EX1023, 8:10-17 (in data processing context, equalizer coefficients that are factory set are “fixed”).

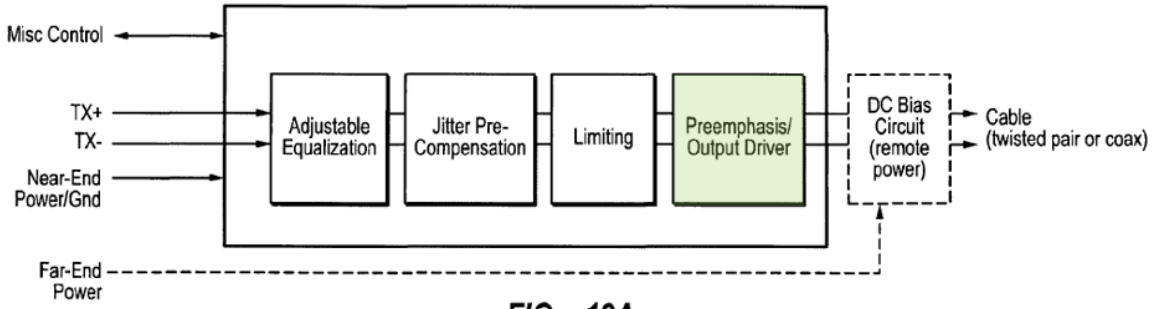


FIG. 12A

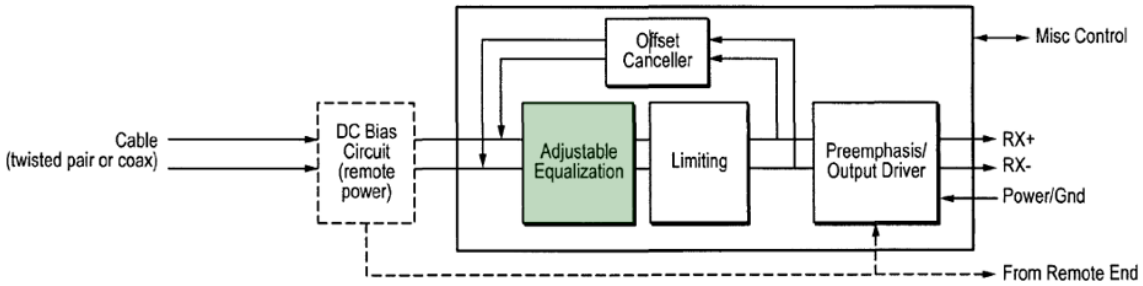


FIG. 12B

156. A POSA's knowledge of benefits of using fixed parameters—to reduce complexity and manufacturing cost—for equalizing received and transmitted (pre-equalization) signals for distortion from transmission over a copper cable, as in Lugthart-993 and Aronson, would have given POSAs further reason to make the design choice to fix the cable-dependent parameters in Lugthart's DSP 13's FIR 17 and equalizer 21. I have discussed some of these known tradeoffs above in Sections VI.A.3.a.i and VI.A.3.a.ii.(2) (Reasons to Combine).

157. Signal noise and degradation is typically more pronounced as a cable's length increases—*i.e.*, the longer a cable is, the more difficult it is to reliably transmit and receive an electrical signal over it—and so if the cable's length and other characteristics are known (particularly by the manufacturer manufacturing it), they may be at least partly compensated for via fixed parameters. Indeed, POSAs understood that factory-set fixed parameters for line-side equalizers are of "***particular interest*** because the cable length and

characteristics are established at the time of the cable manufacture." Aronson, 15:6-8; EX1014, [0031]-[0032] (fixed parameters optimized for known cable length are simple and reliable).

158. Finally, fixing the parameters for Lugthart-993's FIR 17 and equalizer 21 to values determined during manufacture-testing would have been nothing more than combining prior art elements using known methods to yield the predictable results of fixed equalization parameters that require less complexity and cost to implement.

iii. Reasonable Expectation of Success

159. POSAs would have had a reasonable expectation of success in implementing Lugthart-993's transceivers in any and all of the ways discussed above, including with fixed or adaptive parameters. As discussed above, Lugthart-993 already discloses cable-dependent and cable-independent parameters that POSAs understood can be fixed or adaptive, and every one of above-discussed design choices was well-known as demonstrated by Aronson and numerous other references corroborating a POSA's background knowledge. Implementing these techniques well-known for use in active copper cables like Lugthart-993's was well within a POSA's capabilities. For example, implementation of fixed parameters was well-known through, for example, stored values in memory, programming default settings, potentiometers, etc. EX1021, [0078] (default

coefficients provided by manufacturer and stored in registers). Similarly, adaptive parameters were part of well-known processes that involved, for example, transmitting known training sequences and, upon reception, continually updating equalization parameters to minimize differences between the signal that was received and the known expected signal. EX1021, [0078]-[0081] (training to generate new coefficients that achieve a desired error rate and are applied to transmission and receiver logic settings); Lugthart-993, 48:11-27 (training phase to update parameters for equalizers).

4. Mapping of Lugthart-993 and Aronson to claims 1-14

a. Claim 1

i. Preamble [1.PRE]: An active Ethernet cable that comprises:

160. Lugthart-993+Aronson meets [1.PRE] because it teaches an active cable 110 including "actively powered componentry." Lugthart-993, 14:3-5, Fig. 2A (annotated below highlighting cable 110). Cable 110 is an active Ethernet cable because it can support data communications according to the Ethernet standard. Lugthart-993, 15:64-16:5 (supports the "gigabit Ethernet" protocol).

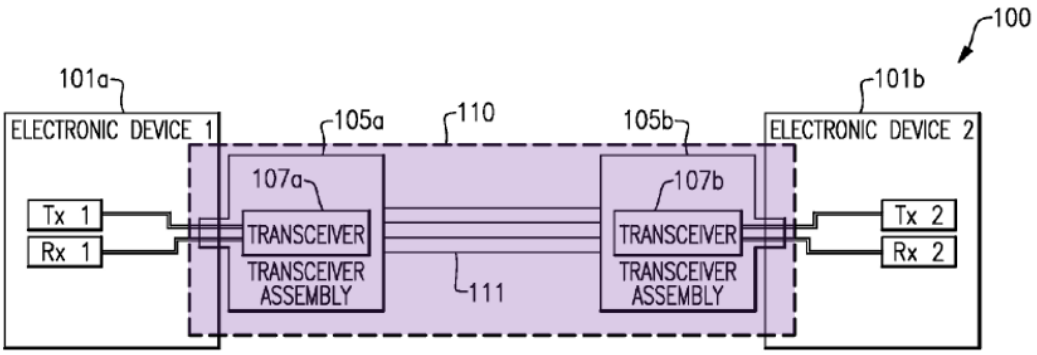


FIG.2A

161. As I will discuss below, it is my opinion that Lugthart-993+Aronson meets all the limitations of claim 1.

ii. Limitation [1.A]: electrical conductors connected between a first connector and a second connector,

162. Lugthart-993+Aronson meets [1.A] because it teaches that cable 110 includes "electrical conducting lines 111." Lugthart-993, 15:48-60. Conducting lines 111 are electrical conductors connected between first and second transceiver assemblies 105a/105b configured to be "electrically connected" to first and second electronic devices 101a/101b, respectively. Lugthart-993, Fig. 2A (annotated below), 14:3-16.

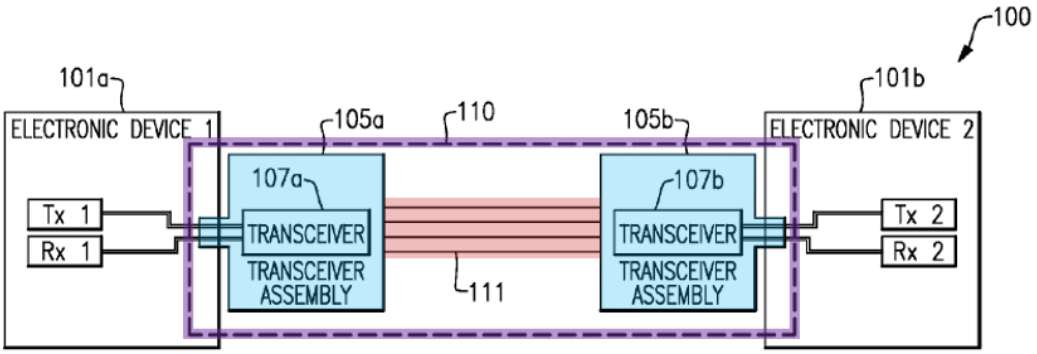


FIG.2A

163. Lugthart-993 describes transceiver assemblies 105a and 105b each comprising "an input port that is configured to mechanically and electrically connect, *e.g.*, in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b and an output port that is connected to the cable. The input port can include a connector similar to… small form-factor pluggable (SFP)… and/or quad [SFP] (QSFP)," meeting the first (*i.e.*, 105a) and second connector (*i.e.*, 105b), respectively. Lugthart-993, 15:8-23;

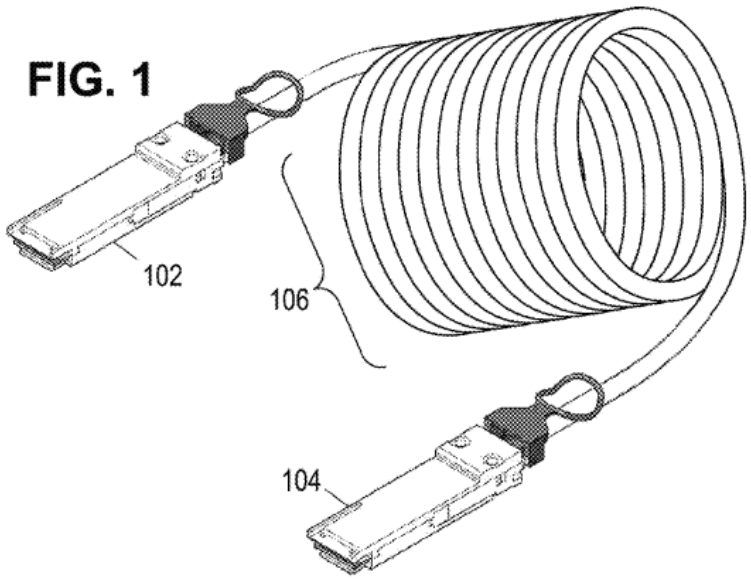
164. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [1.A].

iii. Limitation [1.B]: each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,

(1) Limitation [1.B.i]: "*each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device*"

165. In the'252 patent, a cable connector with a plug is "adapted to fit a standard-compliant Ethernet port" in a host device. EX1001, 4:27-34. The '252 patent admits that "information regarding the operation of the sublayers, as well as the electrical and physical specifications of the connections between the nodes and the communications media…, and the electrical and physical specifications for the communications medium itself…, can be found in the current Ethernet standard, and any such details should be considered to be well within the knowledge of those having ordinary skill in the art." EX1001, 6:44-54.

166. '252 patent Figure 1 (below) illustrates connectors 102 and 104. The illustrated connectors are representative of industry-standard SFP or QSFP-type Ethernet port connectors well known to POSAs.

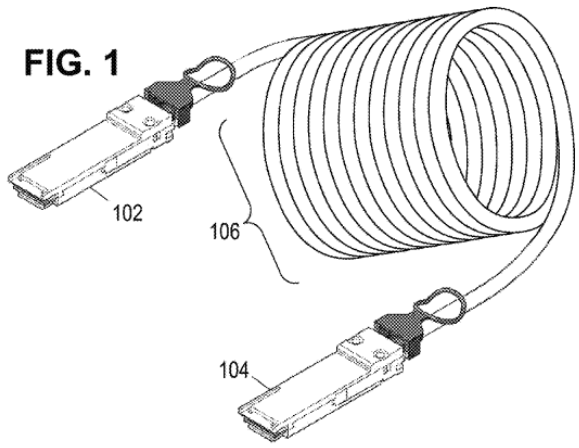


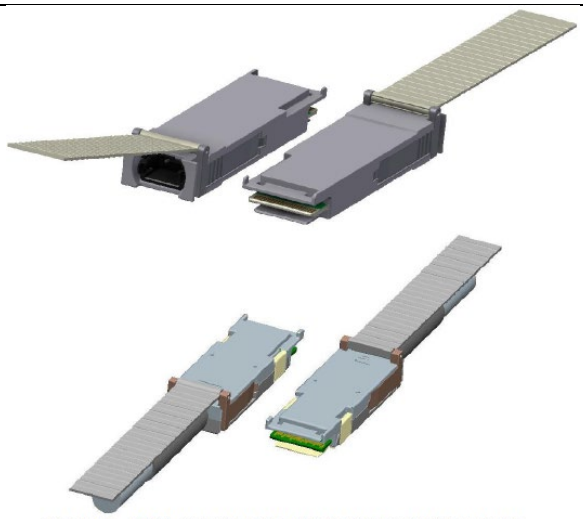
167. For example, the following table lists several connector specifications that are referenced in the IEEE 802.3 standard.

Document / Exhibit	Relevant Section(s)	Relevance
802.3-2015 (Section 1) (EX1028)	Section 1.3	Identifying standards to be applied, including the SFF-8436, Rev. 4.1, and SFF-8642, Rev. 2.7, specifications for pluggable transceivers and connectors
802.3-2015 (Section 6) (EX1029)	Section 85.11.1.1	Identifying the quad small form factor pluggable (QSFP+) interface, defined by SFF-8436
802.3-2015 (Section 6) (EX1029)	Section 85.11.2	Identifying interfaces from the SFF-8642 specification
802.3-2015 (Section 6) (EX1029)	Section 85.13.4.5-6	Tables listing cable assembly and MDI connector specifications, including the SFF-8436 and SFF-8642 specifications
802.3-2015 (Section 6) (EX1029)	Section 92.12.1.1	Identifying QSFP+ plugs, defined by SFF-8665
802.3-2015 (Section 6) (EX1029)	Section 92.14.4.5-6	Tables listing cable assembly and MDI connector

		specifications, including the SFF-8665 specification
SFF-8436, Rev. 4.9 (EX1025)	Page 24	Illustrating QSFP+ modules and plugs
SFF-8642, Rev. 3.3 (EX1026)	Pages 8-9	Illustrating CXP connectors

168. The connector shown in Figure 1 of the '252 patent is similar to Figure 6 from the QSFP+ specification, for example. EX1025, §5.1. A POSA would have recognized that similar standards-based connectors are "*connectors being adapted to fit into an Ethernet port of a corresponding host device*," as claimed.




Figure 6 – QSFP+ pluggable and direct attach module rendering

169. Lugthart-993+Aronson meets [1.B.i] because it teaches that each of cable 110's connectors (transceiver assemblies 105a/105b) are adapted to "mechanically and electrically connect… to a corresponding port" on an electronic device 101a/101b, which is a host device. Lugthart-993, Fig. 2A (annotated

below), 15:14-19. Each host device port is an Ethernet port of a corresponding host device because cable 110 is configured for Ethernet communications (Lugthart-993, 15:64-16:5), and transceiver assemblies 105a/105b have connectors compliant with the same standards – SFP, QSFP, etc. (Lugthart-993, 15:8-23) shown above in '252 patent Figure 1.

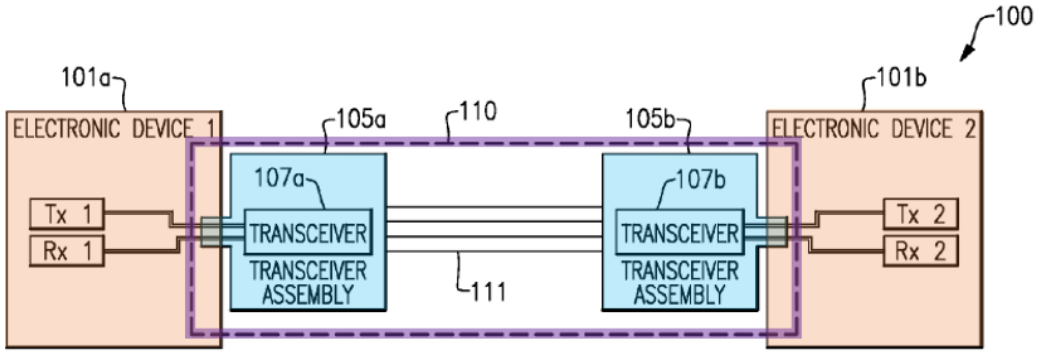


FIG.2A

170. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [1.B.i].

(2) Limitation [1.B.ii]: "*to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,*"

171. In this claim (and in the '252 patent), "inbound" and "outbound" are from the overall cable's perspectives: "inbound data stream to the cable" and "outbound data stream from the cable." EX1001, 1:31-37, 3:67-4:3 ("outbound data streams… exit the cable" and "inbound data streams… enter the cable"), 4:27-

32. In Lugthart-993+Aronson, cable 110's "EGRESS/TRANSMIT" path is "inbound," and its "INGRESS/RECEIVE" path is "outbound," from the cable's perspective. *See* Section VI.A.1 above; Lugthart-993, Fig. 1A (annotated below).

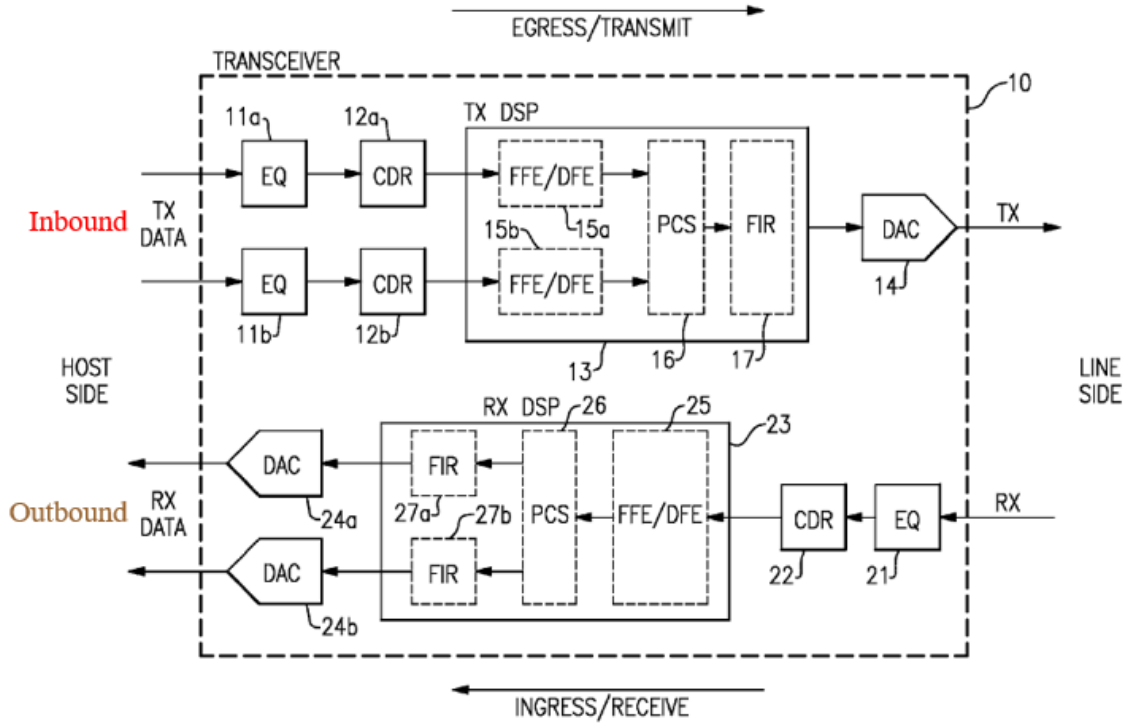


FIG.1A

172. Lugthart-993+Aronson meets [1.B.ii] because the connectors (transceiver assemblies 105a/105b) each receive, from respective host devices, an electrical input signal conveying an inbound data stream to the cable ("egress/transmit" data stream) and provides, to its respective host device, an electrical output signal conveying an output data stream from the cable ("ingress/receive" data stream). Lugthart-993, 15:35-47, Fig. 1A, 7:6-17 (describing host-side and line side "data streams"), 9:6-17 and 23:4-7 (transceiver

components generate and/or process "data streams"). Lugthart-993's streams are conveyed as electrical signals. Lugthart-993, 13:33-35, 15:48-52.

173. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [1.B.ii].

iv. Limitation [1.C]: each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,

174. Lugthart-993+Aronson meets [1.C] because Lugthart-993+Aronson's connectors (Lugthart-993's transceiver assemblies 105a/105b) each includes a respective transceiver (transceivers 107a/107b, respectively). Lugthart-993, Fig. 2A (annotated below), 14:21-26, 14:64-15:1. Transceivers 107a/107b each perform clock and data recovery on the input signal to extract and re-modulate the inbound data stream for transit via conductive lines 111, as discussed below.

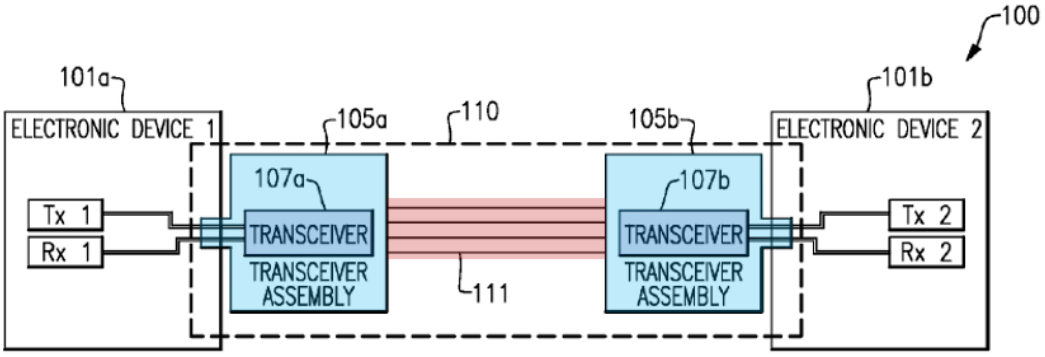


FIG.2A

175. As shown in annotated Figure 1A below, each transceiver processes an *electrical input signal* conveying inbound data stream TX by equalizing the signals using equalizers 11a/11b, then *performs clock and data recovery* ("CDR"), via CDR circuits 12a/12b and DSP13's FFE/DFE 15a/15b, on the equalized *electrical input signal to extract the inbound data stream*. Lugthart-993, 9:6-18, 1:57-2:23, 7:49-8:5, *also* 34:29-35:32 (equalizer, CDR, and FFE/DFE conceptually a "CDR system;" FFE/DFE provides the CDR system output).

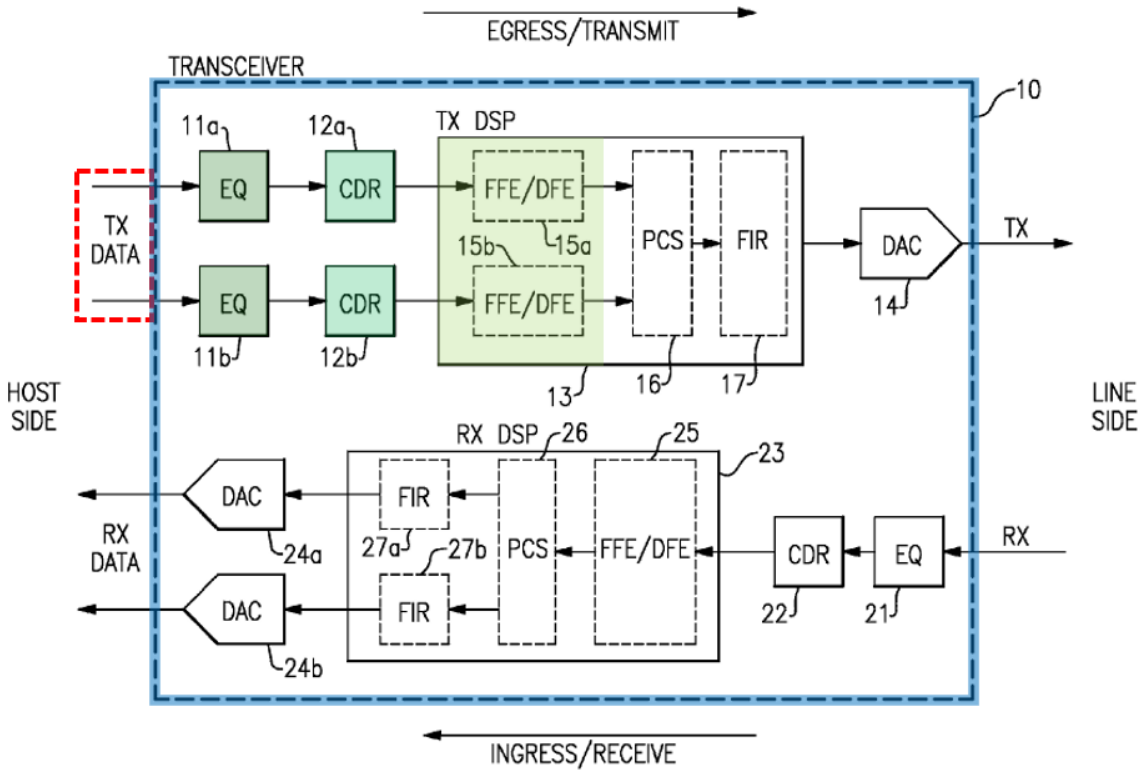


FIG.1A

176. Shown in annotated Figure 1A below, the extracted and recovered data is then processed by DSP 13's PCS 16 and FIR 17 to "generate a serialized or multiplexed output signal having a desired ***modulation*** format" and to perform

output pre-emphasis for the output signal, respectively, which DAC 14 then converts into an analog signal for transmission as line-side signal TX. Lugthart-993, 4:11-19, 7:67-8:2, 9:19-51; *see also* 8:32-41 (transceivers 107a/107b communicate with host-side NRZ signals and line-side PAM-4 signals), 9:41-46, 12:56-13:28, 23:13-19, and 52:52-53:67 (listing modulation formats and conversions), 9:52-10:3 (DACs convert digital-to-analog); 23:20-30, 28:42-47, 30:24-39 (FIR filters used for output pre-emphasis). NRZ and PAM-4 in the example above are different modulation schemes that represent data in different ways—using two and four voltage levels, respectively. Lugthart-993, 30:40-63. Therefore, each transceiver further *re-modulate[s] the* extracted *inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream.*

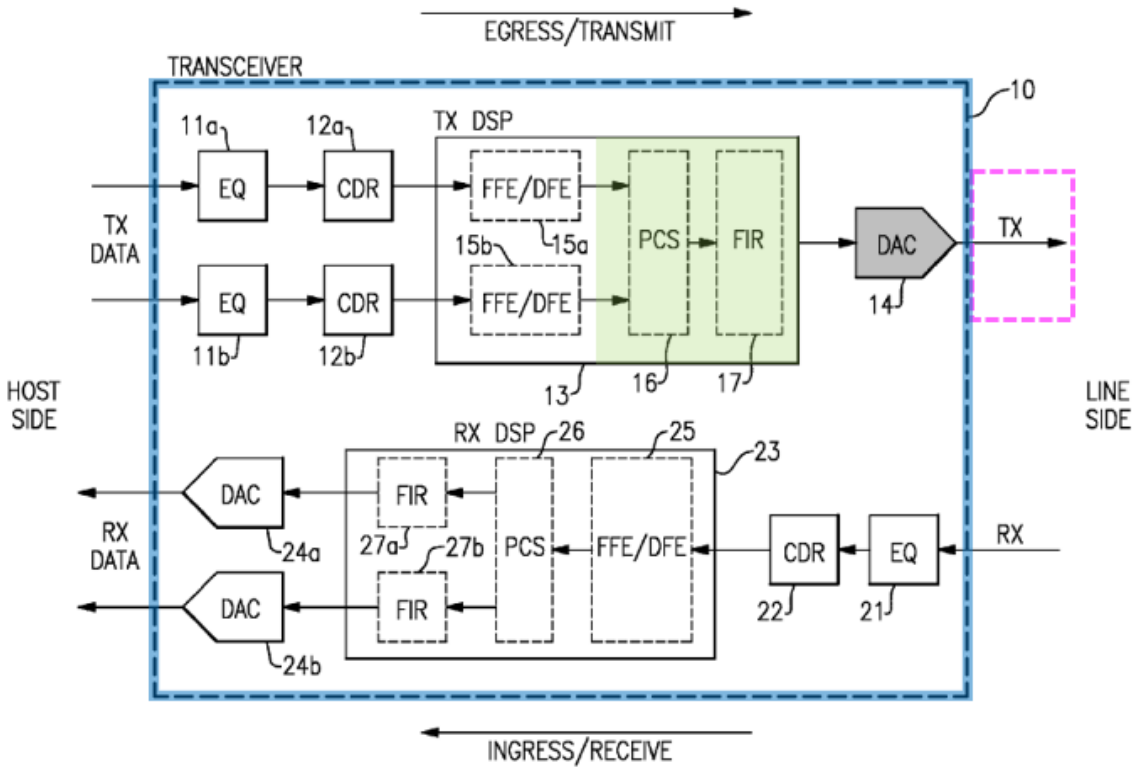
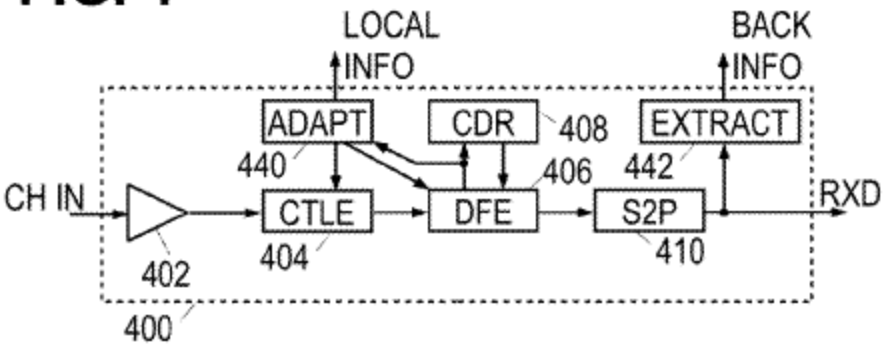


FIG.1A

177. Nothing in the '252 patent specification precludes pre-processing of the input signal conveying the inbound data stream received from the host before performing CDR, as the CDR performed in the '252 patent specification by CDR 408 in Figure 4 (below) is performed on a signal that is pre-processed in the transceiver including by being equalized in CTLE 404. EX1001, 6:62-7:16, Fig. 4.

FIG. 4



178. I have also been informed that the Patent Owner in district court has pointed to alleged infringement by products that perform "input equalization," which does not appear to be an internal process of the separately identified clock and data recovery itself. EX1039, 11-17 (limitations [1.C]-[1.D], identifying clock and data recovery via "retiming"), 17-25 (limitation [1.E], identifying parameters for "input equalization" and "output equalization").

179. From this disclosure and the '252 patent disclosures above, I understand that equalization for clock and data recovery may be performed in two different steps or functional blocks.

180. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [1.C].

v. Limitation [1.D]: the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and

181. Lugthart-993+Aronson meets [1.D] because, first, in generating outbound data stream RX DATA, *the respective transceiver* (transceiver 107a/107b) *for each of the first and second connectors* (transceiver assemblies 105a/105b) *perform[s] clock and data recovery on the respective electrical transit signal* (line-side received signal RX) by equalizing the signal using equalizer 21, and *performing CDR*, via CDR circuit 22 and DSP 23's FFE/DFE 25, on the equalized *electrical transit signal to extract the transit data stream.* Lugthart-993, 1:57-2:23, 9:6-18; *see also* my discussion of [1.C] in Section VI.A.4.iv above and Lugthart-993, 8:58-9:17, 22:48-50, 23:31-37 (similar components in egress and ingress paths have similar functions). As I discussed in Section VI.A.1 above, Lugthart-993 loosely considers equalizer, CDR, and FFE/DFE together as part of a "CDR system" in which the FFE/DFE provides the "system" output. Lughtart-993, 34:29-35:32

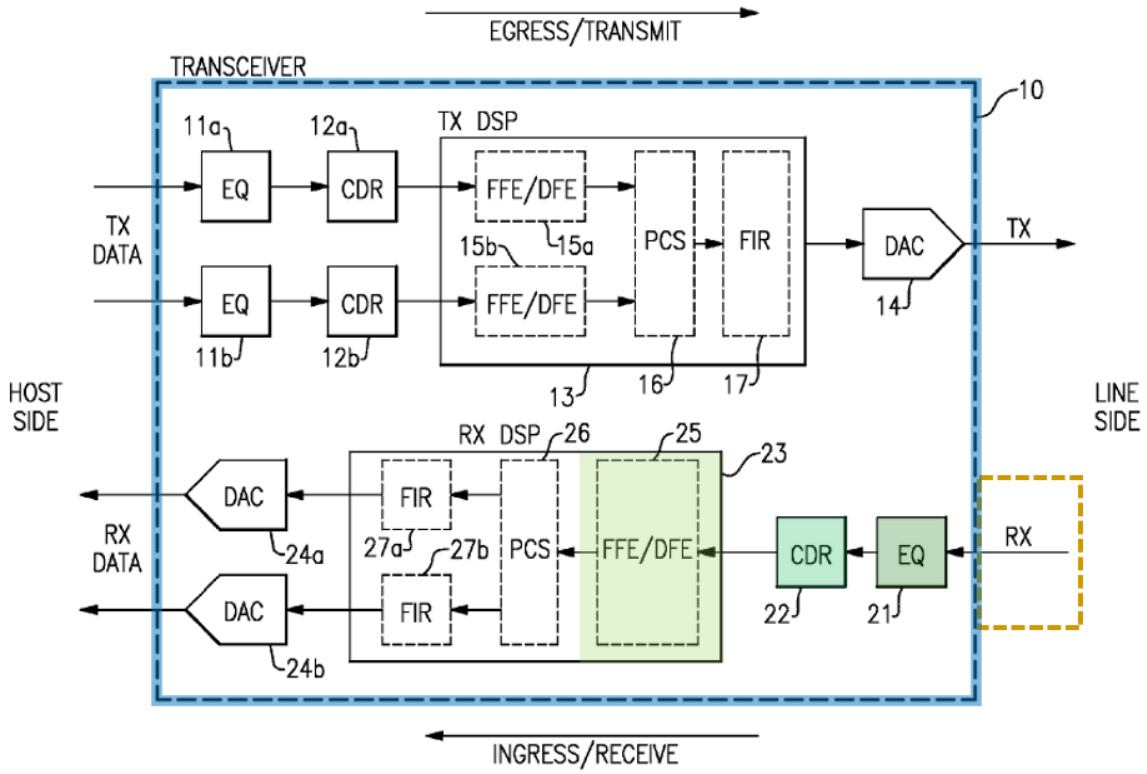


FIG.1A

182. Second, transceiver assemblies 105a/105b then each *re-modulate the transit data stream*, via DSP 23's PCS 26 and FIRs 27a/27b to "deserialize the data to generate output signals having a desired ***modulation*** format for host side transmission" and to perform output pre-emphasis for the output signal, respectively, which DACs 24a/24b then convert into analog signals for transmission *as the outbound data stream from the cable* RX DATA. Lugthart-993, 7:49-57, 7:63-8:14, 8:5-10, 9:19-22, 9:46-10:3, 22:31-40 (outputting the stream in NRZ or "any other suitable ***modulation*** format"); *see also* my discussion of [1.C] in Section VI.A.4.iv above and Lugthart-993, 8:58-9:17, 22:48-50, 23:31-37 (similar components in egress and ingress paths have similar functions).

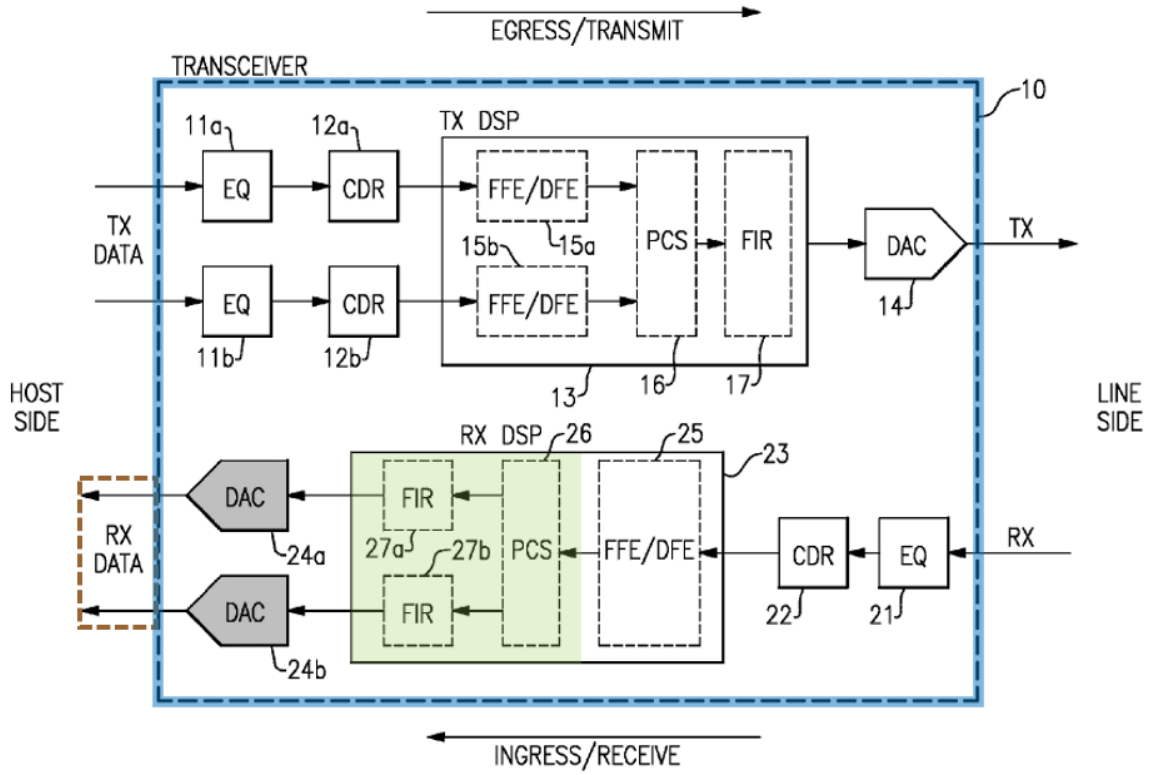


FIG.1A

183. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [1.D].

vi. Limitation [1.E]: the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

184. Lugthart-993+Aronson meets [1.E] because *transceivers* (107a/107b) each performs equalization *for the remodulation of the transit data stream as the outbound data stream* (by DSP 23's FIRs 27a/27b coupled to DACs 24a/24b) and

for the [CDR] performed on the electrical input signal (by equalizers 11a/11b), both using *fixed cable-independent parameters* as I explain below.

(1) Equalization for CDR on the electrical input signal

185. Lugthart-993's equalizers 11a/11b equalize the *electrical input signal* conveying inbound data stream TX DATA so CDR circuits 12a/12b and DSP13's FFE/DFE 15a/15b perform *clock and data recovery* on the equalized input signal. *See* my discussion of [1.C] above; Lugthart-993, Fig. 1A (annotated below).

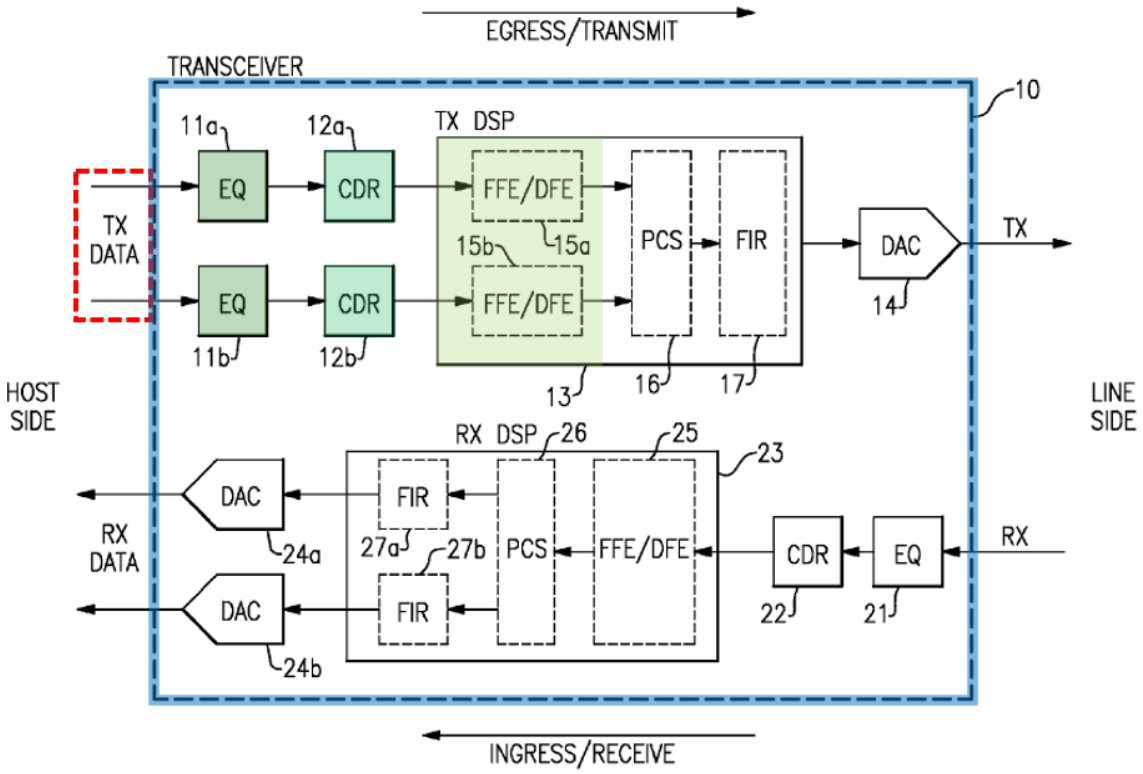


FIG.1A

186. Equalizers 11a/11b "compensate for transmission line losses on the ***host*** side." Lugthart-993, 8:58-9:5. From this disclosure, POSAs would have

recognized that the equalizers use at least some *parameters* that are related to the host (not the cable) and therefore *cable-independent equalization parameters*. *See also* my discussion of Lugthart-993+Aronson in Section VI.A.3.a above.

187. As I had discussed in relation to [1.C] above, the '252 patent also describes performing equalization on a signal before performing CDR. Lugthart-993's equalizers 11a/11b and CDRs 12a/12b disclose the same.

(2) Equalization for re-modulation as the outbound data stream

188. First, I note that while the term used in this claim limitation is "equalization" of an output signal, other terms that POSAs would have used for the function of conditioning a signal for output include "pre-emphasis" and "pre-equalization." *See also* EX1001, 5:2-5 ("*equalization parameters*" include parameters for transmitter-side pre-equalizers) and my discussion of Equalization in Section IV.D.3 above.

189. Lugthart-993's FIRs 27a/27b provide output pre-emphasis in the *remodulation of the transit data stream as the outbound data stream* performed by DSP 23's PCS 26 and FIRs 27a/27b and DACs 24a/24b. *See* my discussion of [1.D] in Section VI.A.4.v; Lugthart-993, Fig. 1A (below).

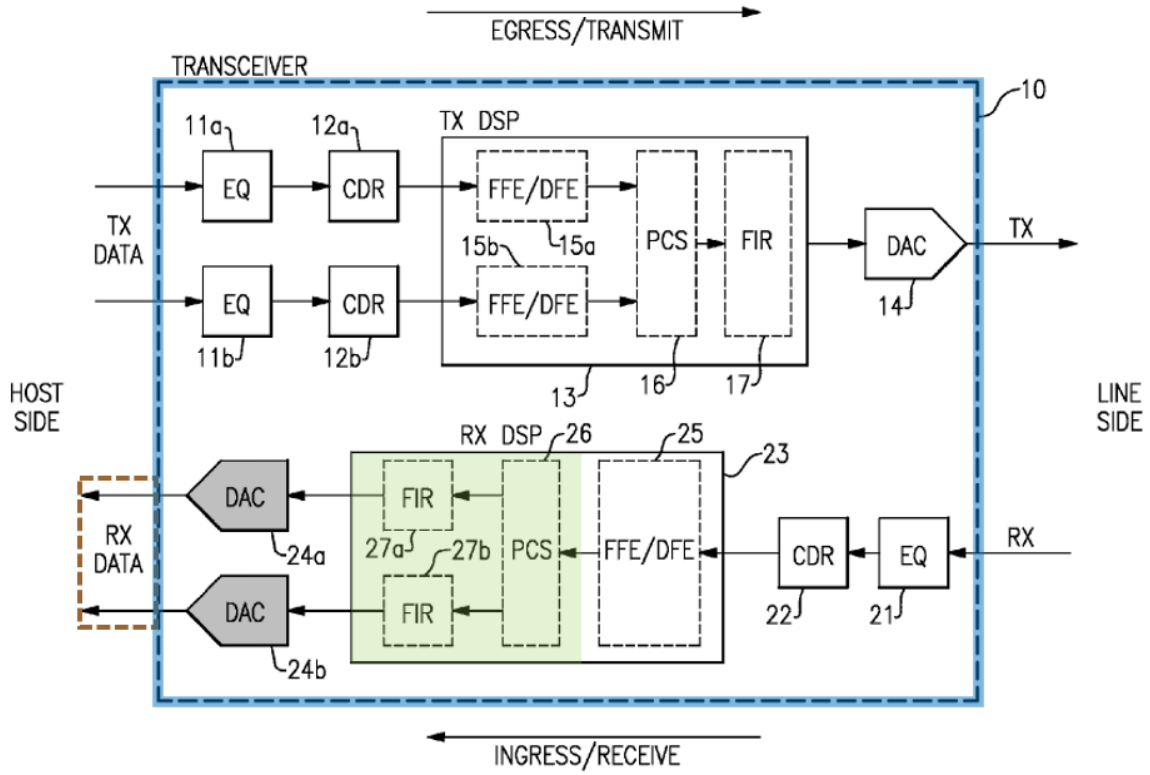


FIG.1A

190. FIRs 27a/27b's output pre-emphasis uses *cable-independent equalization parameters* for the *remodulation*. Specifically, FIRs 27a/27b condition the data signal by outputting time-varying levels that, when converted to analog by DACs 24a/24b, yield a remodulated signal equalized to suffer less distortion/degradation when transmitted. Lugthart-993, 30:24-39 (the FIR filters condition signals for output), 23:23-25 ("FIR filters… perform emphasis on the signal to compensate for channel losses"), 21:33-46 (FIR filter tap coefficients are *equalization* parameters), 22:41-50 (components of DSP 13 and DSP 23 are functionally similar), 28:42-47 (transceivers perform "output pre-emphasis"). FIRs 27a/27b prepare the outbound data stream for transmission to the host and operates

on a data stream already equalized (by equalizer 21) for ***line-side*** losses (which I discuss, for example, for claim 2 below). Lugthart-993, 8:58-60. Thus, POSAs understood that FIRs 27a/27b employ "*cable-independent*" equalization parameters to pre-equalize the signal for ***host-side*** losses. *See also* my discussion of cable-independent parameters in Section VI.A.3.a above.

191. FIRs 27a/27b with associated DACs 24a/24b of Lugthart-993 meet the language of the claim. They collectively perform the same functions as transmit filter 506 of the '252 patent. EX1001, 7:53-56. The description of the transmit filter 506 does not recite "re-modulation," but even if the functions of the transmit filter 506 were interpreted as the claimed "*re-modulation*," nothing in the '252 patent specification supports interpreting [1.E] to require that equalization and remodulation be performed by a single functional block in Lugthart-993's transceiver. The transmit filter 506 of the '252 patent is simply part of a high-level block diagram, and no details are provided about its operation. And, to the contrary, limitation [1.E] uses the same "*employing ... equalization parameters for*" language in connection with "*each of*" remodulation as the outbound stream to the host and CDR on the input signal from the host, and the specification is explicit that equalization can be performed by a different functional block than the one that does the CDR, as I discussed above for [1.C].

(3) Fixed, cable-independent parameters

192. To the extent Lugthart-993 does not explicitly describe its equalizers 11a/11b and FIRs 27a/27b as utilizing "*cable-independent*" parameters, that would have been the conventional and obvious way to implement what Lugthart-993 describes, as confirmed by Aronson and other references corroborating a POSA's background knowledge. Additionally, it would have been obvious to use "***fixed*** *cable-independent*" parameters for Lugthart-993's equalizers 11a/11b and FIRs 27a/27b as taught by Aronson and other references corroborating a POSA's background knowledge. I discuss these reasons in Section VI.A.3.a.i above.

193. Thus, Lugthart-993+Aronson's pre-equalization of the output data stream to the host, and its equalization of the input stream's electrical signal from the host, both use *fixed cable-independent equalization parameters*.

194. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [1.E].

b. Claim 2: The active Ethernet cable of claim 1, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal.

195. Dependent claim 2 recites the transceivers as each employing "*cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit* [to the line- side]*, and the [CDR] performed on the*

electrical transit signal" from the line-side. Meeting claim 2 only requires meeting "at least one" of those uses. Lugthart-993+Aronson meets claim 2 two alternative ways because it meets both uses.

(1) Equalization for re-modulation for transit

196. Lugthart-993+Aronson's *transceivers* (107a/107b), via DSP 13's PCS 16 and FIR 17 and DAC 14, each remodulates the inbound data stream for transit over the cable as a line-side signal TX. *See* my discussion of [1.C] above. FIR 17 performs part of the re-modulation by shaping signals for better transmission through the cable's conductors, with DAC 14 converting the shaped signal to an analog signal. Lugthart-993, 23:4-30, 30:24-39, Fig. 1A.

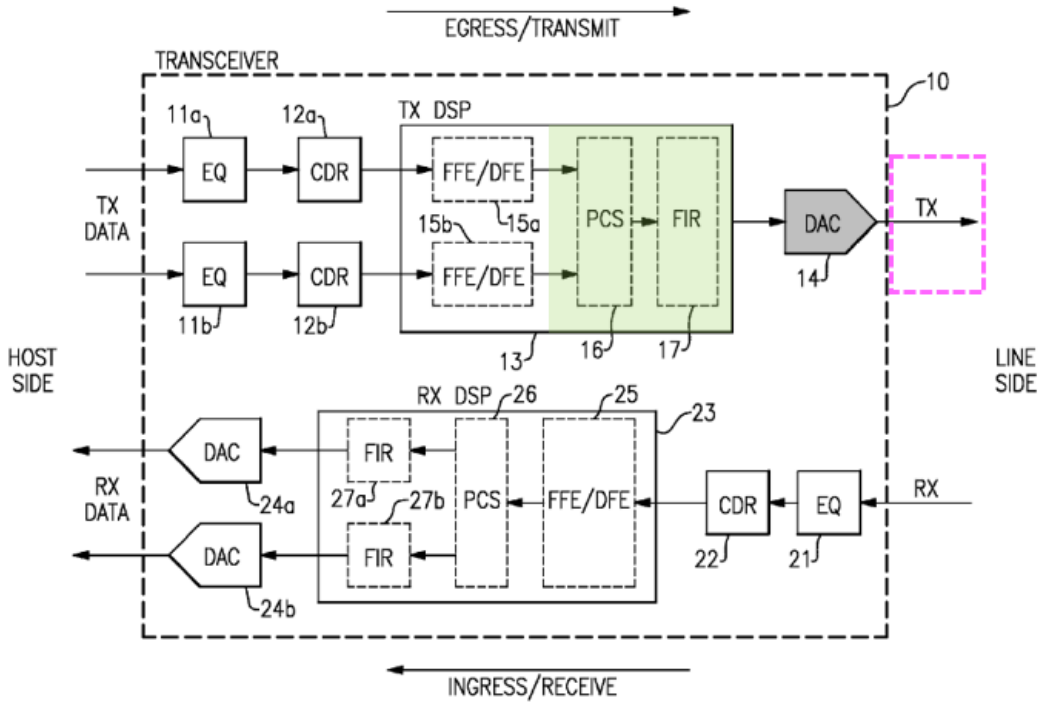


FIG.1A

197. FIR 17 employs equalization parameters for "perform[ing] emphasis on the signal to compensate for channel losses." Lugthart-993, 23:20-25. POSAs understood this describes pre-equalization for "channel" losses through the cable's conductors (line-side) because equalizers 11a/11b already compensated for host-side losses for CDR and because Lugthart-993's transceivers perform pre-equalization. Lugthart-993, 9:19-32 (DSPs process data already recovered by CDR circuits), 28:42-47 (output pre-emphasis), 29:59-30:5, 30:24-39 (the FIR filters condition signals for output). Because its equalization compensates for transmission losses over the cable, POSA's understood that FIR 17 employs equalization parameters that are "cable-dependent." *See* my discussion in Section VI.A.3.a.ii.

198. To the extent Lugthart-993 is considered to not explicitly describe FIR 17's equalization as using "cable-dependent" parameters, that would have been the conventional and obvious way to implement Lugthart-993's described equalization to address losses over the cable, as confirmed by Aronson and numerous other references corroborating a POSA's background knowledge. *See* my discussion in Section VI.A.3.a.ii above. *See also* Aronson, Fig. 12A (annotated below), 14:33-43 (pre-emphasis/output driver performs pre-equalization to overcome "loss on the cable" using *cable-dependent* parameters that "match the particular length [and/or] the characteristics of the copper cabling").

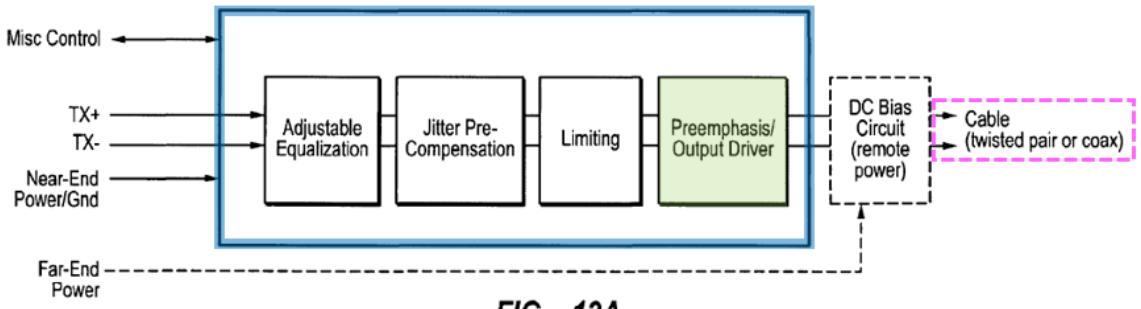


FIG. 12A

199. Performing equalization and conversion to analog in separate functional blocks meets the proper construction of employing "equalization parameters for the remodulation" of a data stream for the same reasons I discussed above for limitation [1.E].

200. Thus, Lugthart-993+Aronson meets claim 2's alternative ("at least one") of *employing cable-dependent equalization parameters for the remodulation of the inbound data stream for transmit*.

(2) Equalization for CDR on the electrical transit signal

201. CDR circuit 22 and FFE/DFE 25 in Lugthart-993+Aronson's *transceiver* (107a/107b) performs CDR on the equalized received line-side transit data stream. *See* my discussion above for [1.D]. Equalizer 21 "compensate[s] for transmission line losses on the line side" and thus uses *cable-dependent equalization parameters*. Lugthart-993, 8:58-9:5; *see also* 22:4-9 (compensates for losses "over the cable"), Fig. 1A.

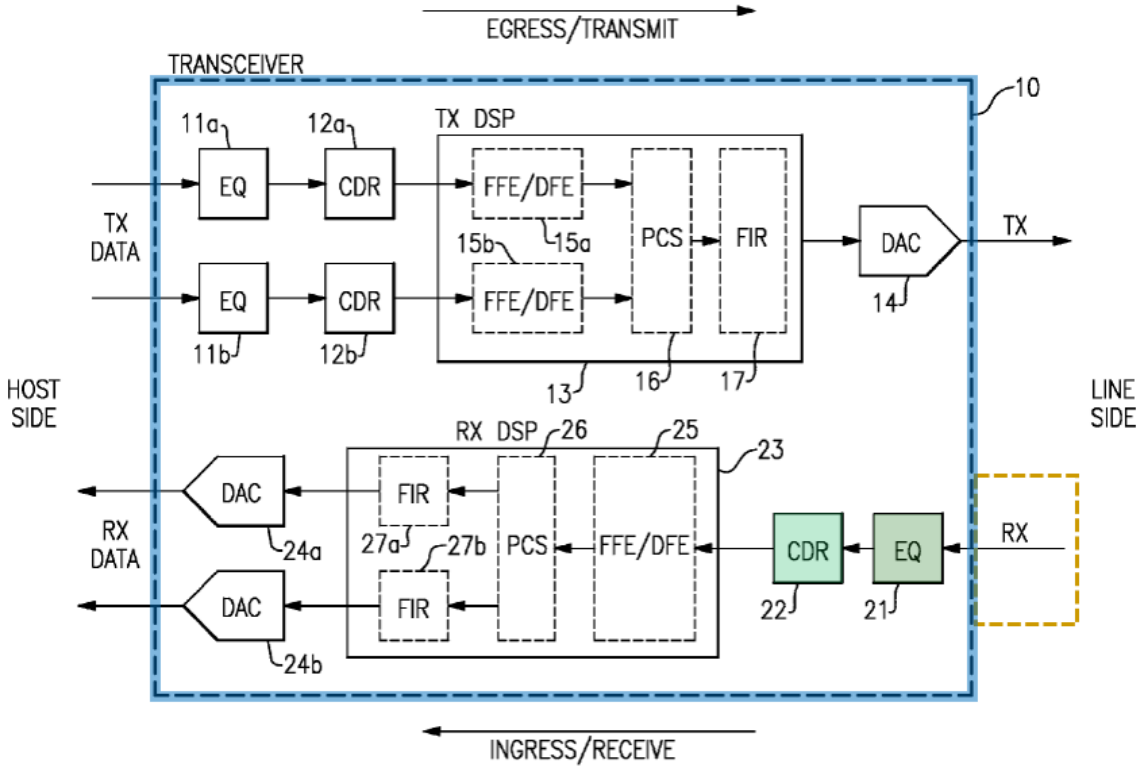


FIG.1A

202. To the extent Lugthart-993 is considered to not explicitly describe equalizer 21 as using "cable-dependent" parameters, that would have been a conventional and obvious way to implement what Lugthart-993 describes as confirmed by Aronson and other references corroborating a POSA's background knowledge. *See* my discussion in Section VI.A.3.a.ii above. *See also* Aronson, Fig. 12B (annotated below), 15:1-8 (equalization "compensat[es] for the cable" losses using *cable-dependent parameters* based on "cable length and characteristics").

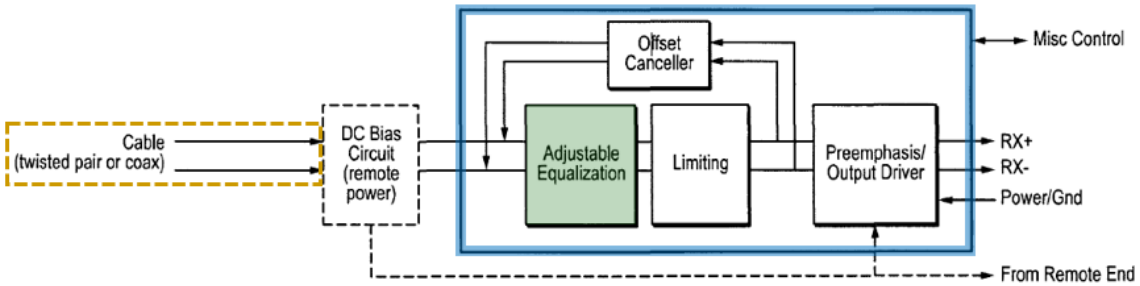


FIG. 12B

203. Performing equalization and CDR in separate functional blocks meets the proper construction of employing "equalization parameters for [CDR]" for the same reasons for limitation [1.E].

204. Thus, using cable-dependent parameters in Lugthart-993's equalizer 21 meets claim 2's alternative ("at least one") of *employing cable-dependent equalization parameters for the [CDR] performed on the electrical transit signal*.

c. Claim 3: The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.

205. The '252 patent describes three "usage" phases: (1) the cable is tested during a manufacturing-testing phase (EX1001, 8:16-38); (2) after cable installation in the field a training phase is performed during which equalization parameters can be adapted from factory-set values (EX1001, 7:27-47, 8:31-37); and (3) "normal operations" begin after the training phase (EX1001, 7:46-50). While claim 4 refers to "normal usage," claim 3 more broadly recites "during usage" which encompasses adaptation during use of the cable in a training phase.

206. Lugthart-993 describes training phases during which "parameters of the components in the transceivers connected to the first and second electronic devices are adjusted" including "parameters for the equalizers." Lugthart-993, 47:56-48:27. POSAs understood that the transceivers "connected to" the host electronic devices are the cable's transceivers. Lugthart-993, 28:40-47 (cable transceivers are "adaptive" for performing equalization including pre-emphasis). As I discussed in at least Sections VI.A.3.a.i and IV.D.3, pre-emphasis is a form of equalization and is "pre" transmission, and so pre-emphasis is a form of equalization, for which parameters may be adjusted in Lugthart-993.

207. Claim 3's "*said cable-dependent equalization parameters*" find their antecedent in claim 2 which requires their use in "at least one" of two alternative ways. The cable-dependent equalization performed by Lugthart-993+Aronson's FIR 17 and equalizer 21 meet both alternatives. *See* my discussion of claim 2 above in Section VI.A.4.b; Lugthart-993, 8:58-60, Fig. 1A (annotated below). To the extent Lugthart-993 is considered to not specifically teach ***adapting*** the equalization coefficients used by FIR 17 and equalizer 21 during Lugthart-993's training phases, that would have been a conventional and obvious way to implement what Lugthart-993 describes—confirmed by Aronson and other references corroborating a POSA's background knowledge, as discussed above in Sections VI.A.3.a.ii.(1) and VI.A.3.a.iii.

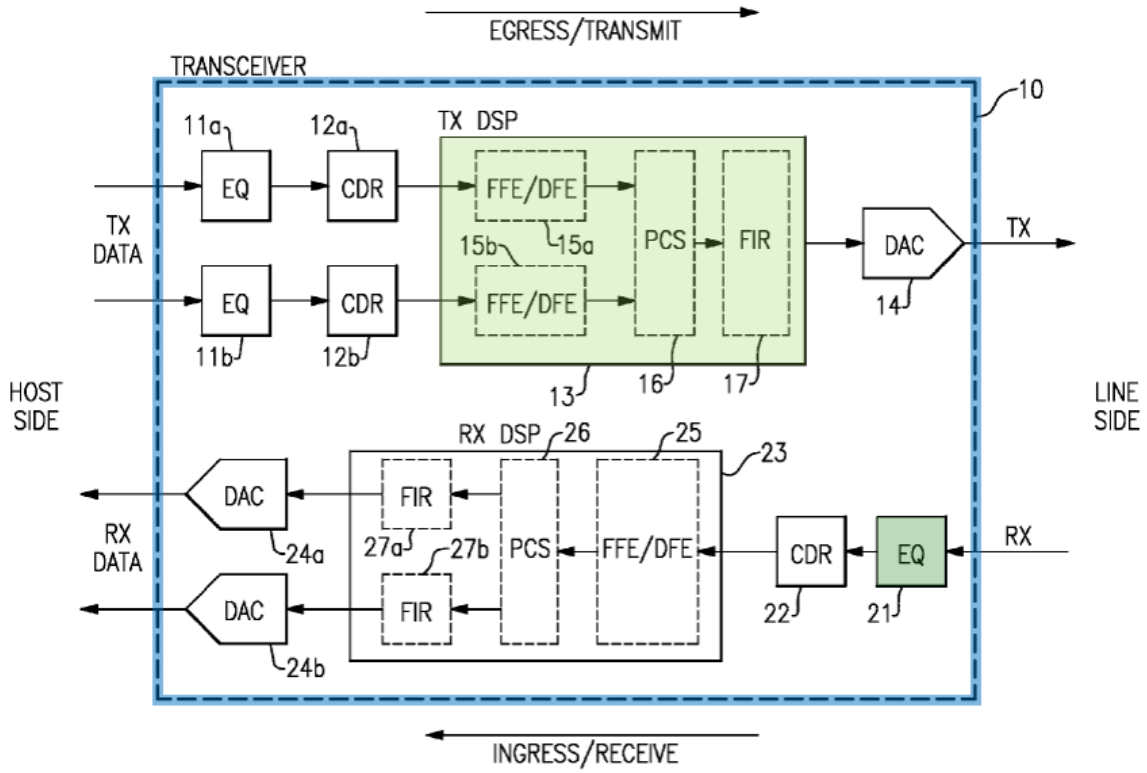


FIG.1A

208. Lugthart-993+Aronson's cable-dependent parameters (1) used by FIR 17 to perform equalization *for the remodulation of the inbound data stream for transmit* to the line side, and (2) used by equalizer 21 *for the [CDR] performed on the electrical transit signal* (*see* my discussion of claim 2 above in Section VI.A.4.b), are adapted during training (*see* my discussion of Lughtart-993+Aronson in Sections VI.A.3.a.ii and VI.A.3.a.iii above) and thus "*adapt[ed] during use of the Ethernet cable*" because, as discussed above, claim 3's "*during usage of the Ethernet cable*" is broader than claim 4's "*normal usage*" and encompasses usage during training.

209. Thus, it is my opinion that Lugthart-993+Aronson meets claim 3.

d. Claim 4: The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing -testing of the Ethernet cable.

210. Claim 4's "*said cable-dependent equalization parameters*" find their antecedent in claim 2 which requires their use in "at least one" of two alternative ways. The cable-dependent equalization performed by Lugthart-993+Aronson's FIR 17 and equalizer 21 separately meet both claim 2 alternatives. *See* my discussion of claim 2 in Section VI.A.4.b above; Lugthart-993, 8:58-60, Fig. 1A.

211. And as discussed for claim 2, one obvious way to implement Lugthart-993, based on Aronson and numerous other references confirming a POSA's background knowledge, was to fix the equalization coefficients used by FIR 17 and equalizer 21 during manufacture-testing. Aronson, 14:35-39 (Fig. 12A's pre-equalization parameters for transit over the line-side are "adjusted at factory setup"), 15:1-8 (Fig. 12B's equalization may be "fixed" or "adjustable but factory set" "at the time of the cable manufacture"). Cable equalization parameters that are "set" at the factory during manufacturer are not expected to change after manufacture and are therefore "fixed" during normal usage of the cable. *See* EX1023, 8:10-17 (in data processing context, equalizer coefficients that are factory set are "fixed").

212. Thus, it is my opinion that Lugthart-993+Aronson meets claim 4.

e. Claim 5: The active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.

(1) Terms

213. A "lane" is single data communication path. EX1028 (802.3 Section 1), 86 (defining "lane").

214. A "symbol" is the smallest unit of data transmission over a medium and depends on the coding system used, and a "symbol rate" is a measure of symbols transferred per second, expressed in baud ("Bd"). EX1028 (802.3 Section 1), 95-96 (defining "symbol" and "symbol rate").

215. Data streams with a "*per-lane symbol rate in excess of 50 GBd*," as claimed, exceed 50 giga (billion) symbols per second, per lane.

(2) Analysis

216. Lugthart-993's transceivers support multiple lanes for the inbound (TX) and outbound (RX) data streams. Lugthart-993, Fig. 1A. For the input lanes shown in Figure 1A below, CDR processing by equalizers 11a/11b, CDR circuits 12a/12b, and FFE/DFEs 15a/15b has a "data rate between about 100 Mbits/s to about 300 Gbit/s." Lugthart-993, 34:39-53. POSAs understood that the other components in the same lane as these components support the same data rate because Lugthart-993's described data rate for CDR would be meaningless if other components in the same lane only supported a lower data rate. For example, if

subsequent components, such as PCS 16, FIR 17, and DAC 14 in the egress/transmit path, were incapable of processing data at the same or better rate than EQ 11a, CDR 12a, and FFE/DFE 15a, an immediate overflow of data would form, and unless the system is configured to handle that excess data (*e.g.*, with buffers, adjustments to transmission rates, etc., that lower the system's overall data rate), that data may be lost.

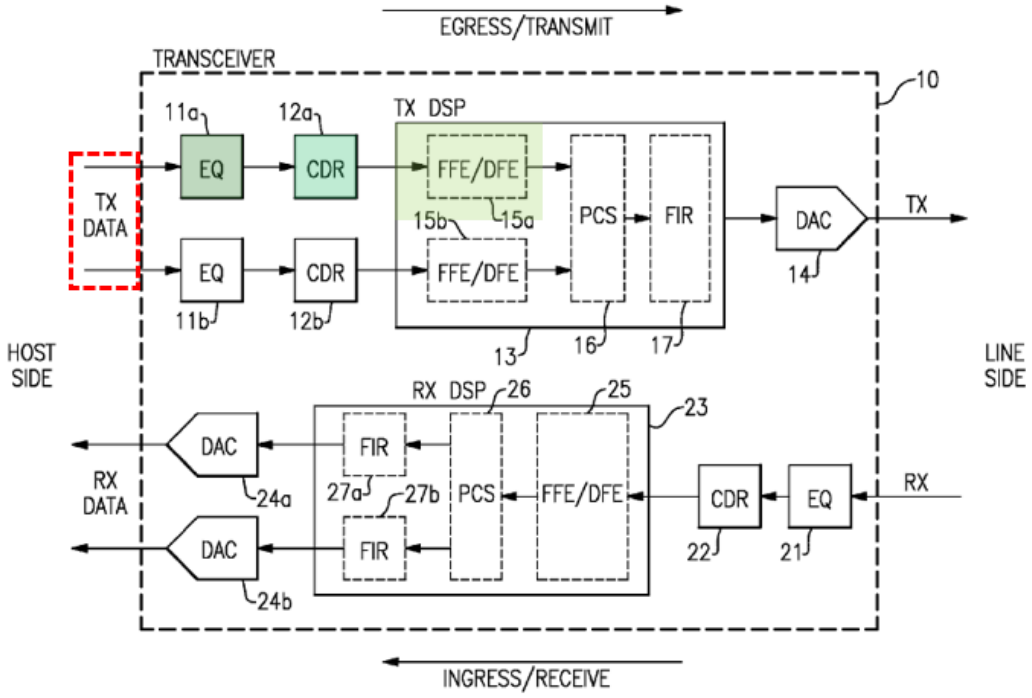


FIG.1A

217. Lugthart-993 teaches that the input signal may be in any format, for example PAM-4. Lugthart-993, 34:48-50. PAM-4 signaling operates at 4 different voltage levels, thus providing 2 bits of data per symbol. Lugthart-993, 30:54-63 (for example, the symbol "00" is represented by a -0.3V voltage level, "01" by -1V, "10" by +1V, and "11" by 0.3V). Thus, for PAM-4 signals, Lugthart-993's

CDR circuits 12a/12b and the rest of the components in each lane for processing the inbound data stream support per-lane symbol rates up to 150 GBd (300 gigabits/second at a rate of 2 bits/symbol is 150 giga symbols/second, which is 150 GBd) which is *in excess of 50 GBd*. Given that Lugthart-993's transceiver can support the same number of lanes (*e.g.*, two each in Figure 1A) for the inbound and outbound data streams, POSAs understood that Lugthart-993 also teaches an outbound data stream with a per-lane symbol rate *in excess of 50 GBd*.

218. Thus, it is my opinion that Lugthart-993+Aronson meets claim 5.

f. Claim 6

219. Lugthart-993+Aronson meets claim 6 for essentially the same reasons it meets claim 1. Claim 6 recites a "communication method" using a "network cable" having limitations mirroring those in claim 1.

i. Preamble [6.PRE]: A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:

220. Lugthart-993+Aronson meets [6.PRE] because Lugthart-993+Aronson's cable is a *network* (*e.g.*, Ethernet) *cable having conductor pairs* (conducting lines 111 include sets of paired egress/transmit and ingress/receive conductors) *electrically connecting a first connector* (transceiver assembly 105a) *to a second connector* (transceiver assembly 105b). *See* my discussions of [1.PRE]-[1.B] above. Lugthart-993, 13:54-14:2 (link between electronic devices

can connect computer and network router), 15:48-16:5, Fig. 2A (annotated below), 16:50-54 ("a first ***paired*** differential cable for communication in a first direction and a second ***paired*** differential cable for communication in a second direction. A paired differential cable… includes a ***pair*** of wires").

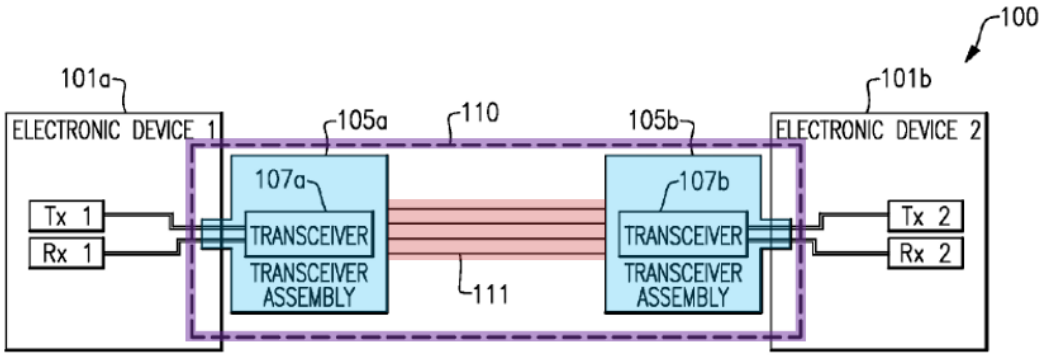


FIG.2A

221. For example, Lugthart-993 shows cross sections of micro coax cables in Figs. 3A-3B below.

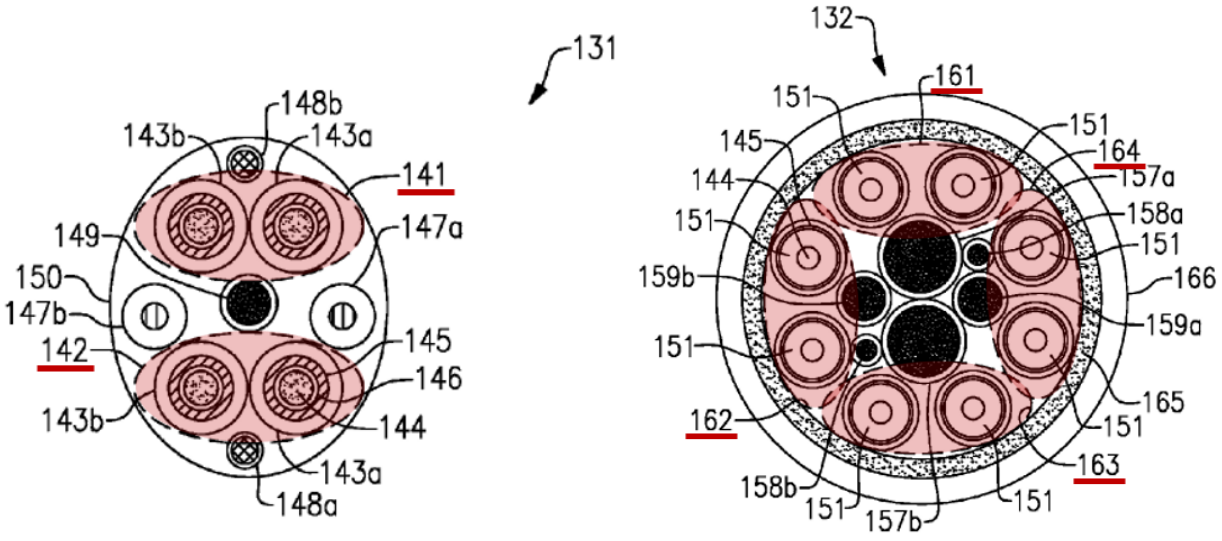


FIG.3A FIG.3B

222. Each dashed oval portion shaded in red (141 and 142 in Fig. 3A; 161, 162, 163, and 164 in Fig. 3B) includes a pair of conducting lines within micro coaxial cables, for example. Lugthart-993, 17:48-57, 17:63-18:9.

223. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [6.PRE].

ii. Limitations [6.A]-[6.K]

224. The limitations in [6.A]-[6.K] recites method steps for a communication method that mirrors limitations [1.B]-[1.E], but they are recited in a slightly different way as highlighted in the table below. For example, where claim 1 reference "corresponding" host devices and "respective" transceivers," claim 6 references "first" and "second" host devices and "first" and "second" transceivers. However, the limitations are met by Lugthart-993+Aronson in the same way in claims 1 and 6.

[1.B.i]-[1.B.ii] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,	**[6.A]** receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;

[1.C] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,	**[6.B]** performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;
	[6.C] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;
[1.B.i]-[1.B.ii] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,	**[6.D]** receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;
[1.C] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,	**[6.E]** performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;
	[6.F] re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;
[1.D] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to	**[6.G]** performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;

extract and re-modulate the transit data stream as the outbound data stream from the cable, and	**[6.H]** re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;
[1.D] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and	**[6.I]** performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and
	[6.J] re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,
[1.E] the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.	**[6.K]** wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [*sic*] parameters.

225. These steps of claim limitations [6.A]-[6.K] are met by Lugthart-993+Aronson in the same way as in claim 1.

226. Lugthart-993+Aronson's cable is used in a bi-directional communication method. *See* my discussion of claim 1 above. Lugthart-993 Figures 2A and 4A are annotated below to show the two data streams (one blue and one yellow) and their corresponding steps in claim 6. Lugthart-993, 19:1-11 (Figure 4A uses Figure 1A transceivers).

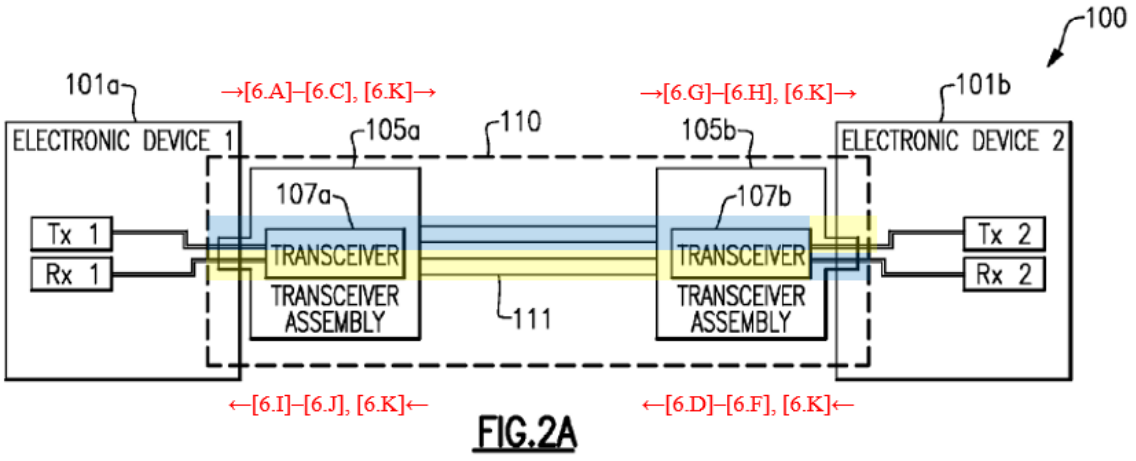


FIG.2A

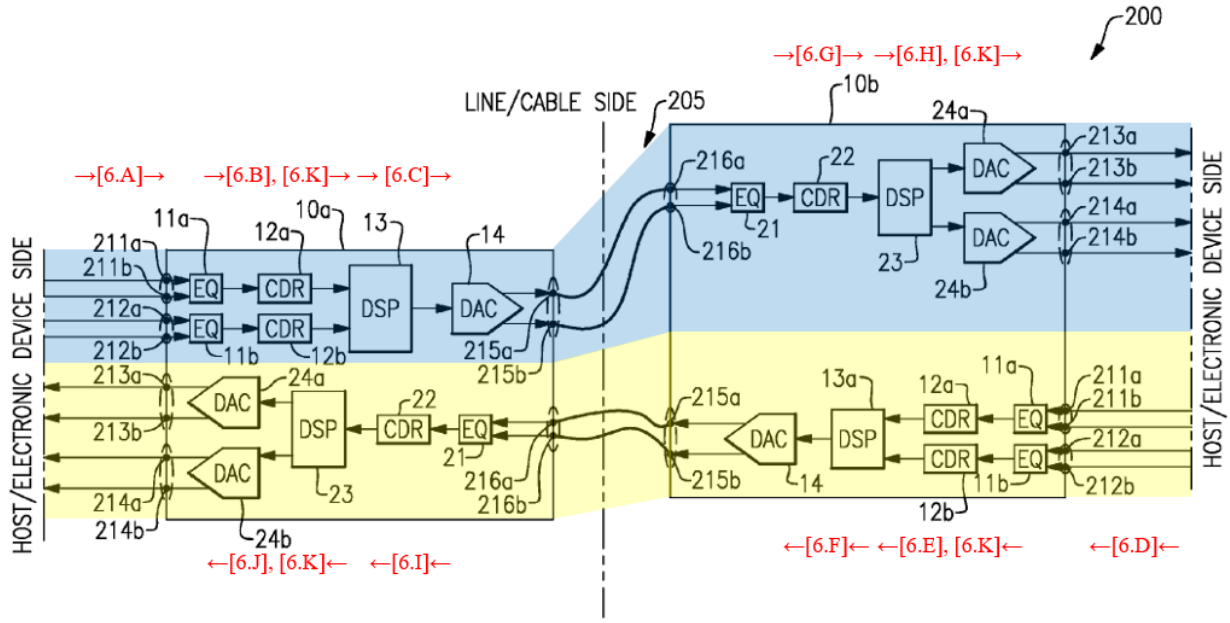


FIG.4A

227. The blue stream depicts a *first inbound data stream from a first host device* [left side of Figures 2A/4A] that is received by the *first connector* ([6.A]), passed through cable conductors, and conveyed as a *second outbound data stream to the second host device* ([6.B]-[6.C], [6.G]-[6.H], [6.K]).

228. The yellow stream is a *second inbound data stream from the second host device* [right side of Figures 2A/4A] that is received by the *second connector*

([6.D]), passed through cable conductors, and conveyed as a *first outbound data stream to the first host device* ([6.E]-[6.F], [6.I]-[6.J]).

229. Steps [6.A]-[6.C] recite the first connector's transceiver *performing CDR* and *re-modulating* the first inbound stream for transmission over the first conductor pair, and [6.D]-[6.F] recite the same steps performed by the second connector's transceiver on the second inbound stream for transmission over the second conductor pair. Lugthart-993+Aronson meets these steps for the reasons I discussed above for limitation [1.C].

230. Steps [6.G]-[6.H] recite the second connector's transceiver *performing CDR* and *re-modulating* the (blue) data stream received over the first conductor pair, and [6.I]-[6.J] recite the same steps performed by the first connector's transceiver on the (yellow) data stream received over the second conductor pair. Lugthart-993+Aronson meets these steps for the reasons I discussed above for limitation [1.D].

231. Step [6.K] requires that each of the remodulating and CDR in steps [6.B]-[6.C] and [6.E]-[6.J] employ *fixed, cable independent equalization parameters* and is met for the reasons I discussed above for limitation [1.E].

232. Thus, it is my opinion that Lugthart-993+Aronson meets Limitations [6.A]-[6.K].

g. Claim 7: The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said [performing] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.

233. I have been informed that because claim 7 contains a printing error—reciting language that was not in the claims examined at the U.S. Patent and Trademark Office—that I should read claim 7 without the erroneous language. In particular, the final phrase in claim 7, "*, each employ fixed, cable-independent, equalization parameters*," does not belong. Properly construed, it is my opinion that Lugthart-993+Aronson meets claim 7 for the same reasons I discussed for claim 2.

h. Claim 8: The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.

234. It is my opinion that Lugthart-993+Aronson meets claim 8 for the same reasons I discussed for claim 3.

i. Claim 9: The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.

235. It is my opinion that Lugthart-993+Aronson meets claim 9 for the same reasons I discussed for claim 4.

j. Claim 10: The communication method of claim 9, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.

236. It is my opinion that Lugthart-993+Aronson meets claim 10 for the same reasons I discussed for claim 5.

k. Claim 11

237. Lugthart-993+Aronson meets claim 11 for essentially the same reasons it meets claims 1 and 6. Claim 11 recites a "cable manufacturing method" for making a cable having limitations mirroring those in claims 1 and 6.

i. Preamble [11.PRE]: A cable manufacturing method that comprises:

238. Lugthart-993+Aronson meets [11.PRE] because they describe a cable, as I discussed for claims 1 and 6, which is manufactured, as I will discuss below.

ii. Limitation [11.A]: connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;

239. It is my opinion that Lugthart-993+Aronson meets claim [11.A]'s conductor pairs, transceivers, and electrical transit signals for the same reasons I discussed for at least claims [1.PRE]-[1.C], [6.PRE], [6.C], [6.F], [6.G], and [6.I].

240. Lugthart-993+Aronson also meet limitation [11.A]'s "connecting" of conductor pairs to the first and second transceivers. Manufacturing the cable according to Lugthart-993+Aronson would have included a step of "connecting" the first and second transceivers with the ends of the conductor pairs because it is the physical connections which allow the described electrical signals to be conveyed from one end of the cable (and its transceiver(s) and/or other circuitry) to the other end of the cable (with its own transceiver(s) and/or other circuitry) or to the hosts connected at either end. Ideally, connections are strong and reliable such that transmissions are not interrupted. Prior art methods for connecting conductors (wires) to transceivers in cable assemblies were well known and obvious to POSAs and included, for example, soldering transceivers and conductors to pads. EX1010, Figs. 4A-4B, 6A-7, [0065], [0073]-[0075] (cable assembly involves connecting transceivers and cable conductors via contact/solder pads); EX1012, [0050],

[0057], Figs. 1-3 and 7; EX1013, [0019]-[0021] and Fig. 3 (mounting pads for connecting electrical wires).

241. Thus, it is my opinion that Lugthart-993+Aronson meets Limitations [11.A].

iii. Limitation [11.B]: packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and

iv. Limitation [11.C]: packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,

242. It is my opinion that Lugthart-993+Aronson meets claim [11.B]'s and [11.C]'s first and second transceivers, connectors, input signals, network interface ports, host devices, and output signals—via Lugthart-993+Aronson's transceiver assemblies, transceivers, input signals, host devices, host ports, and output signals that I discussed for at least claims [1.B.i]-[1.C], [6.A], [6.D], [6.H], and [6.J].

243. Lugthart-993+Aronson also meet limitation [11.B]'s and [11.C]'s "packaging" of first and second transceivers (*i.e.*, transceivers (107a/107b)) into first and second connectors (*i.e.*, transceiver assemblies (105a/105b)).

Manufacturing the cable according to Lugthart-993+Aronson would have obviously included a step of "packaging" the transceivers because Lugthart-993 describes the transceivers included in the transceiver assemblies, which include an "enclosed" packaging. Lugthart-993, 14:64-15:23 (assemblies 105a/105b "include" transceivers 107a/107b and use "enclosed" packaging conforming to interface standards such as SFP+). The packaging conforms to known standards, such as SFP+, QSFP, and others, which are known to use housing that contain and secure internal components. EX1027, 7-10 (SFP+ housing "contains" transceiver); EX1010, [0065] and Figs. 4A-4B (paddle card with contact pads for attaching active components, including transceivers), [0075] and Figs. 6A-7 (cable assembly including outer portions, fixed with screws, that surround a paddle card); EX1012, [0050]-[0051] (connector housing with shell and cover secured with rivets, screws, or other fasteners), Figs. 1-3. The "packaging" of electric components inside packages, housings, cases, etc., even if not standardized as described above, would have been obvious to POSAs because the act of packaging protects devices' internal components, such as transceivers, from the environment and from accidental damage or inadvertent electrical contacts.

244. Thus, it is my opinion that Lugthart-993+Aronson meets Limitations [11.B]-[11.C].

v. Limitation [11.D]: the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

245. It is my opinion that Lugthart-993+Aronson meets claim [11.D]'s respective transceiver functions of clock and data recovery and re-modulation of inbound data streams (as I discussed for limitations [1.C], [6.B], [6.C], [6.E], [6.F]) and transit signals (as I discussed for limitations [1.D], [6.G]-[6.J]), where fixed, cable-independent, equalization parameters are employed for clock and data recovery on electrical input signals and for generating the respective electrical output signals (as I discussed for limitations [1.E], [6.K]).

246. Thus, it is my opinion that Lugthart-993+Aronson meets Limitation [11.D].

l. Claim 12: The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.

247. It is my opinion that Lugthart-993+Aronson meets claim 12 for the same reasons I discussed for claim 2.

m. Claim 13: The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.

248. While claim 3 recites adapting parameters "during usage" and claim 13 recites adapting "during operation" of the cable, I can discern no significant difference between usage and operation in the '252 patent, and it is my opinion that Lugthart-993+Aronson meets claim 13 for the same reasons I discussed for claim 3.

n. Claim 14: The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.

249. It is my opinion that Lugthart-993+Aronson meets claim 14 for the same reasons I discussed for claim 4.

B. Ground 2: The Combination of Tang, TI-Retimer, and Aronson Renders Obvious Claims 1-14

1. Discussion of Tang (EX1007)

250. Tang is directed to visual indicators for data cables used in networking environments, such as those supporting Ethernet communications between transceivers in servers, routers, and switches. Tang, [0001]-[0002], [0014]-[0017].

251. Cables may be configured in a number of ways. For example, cable 10 may include one end having a QSFP+ end for plugging into a first transceiver 12, and another end having four SFP+ ends for plugging into four transceivers 14a-14d. Tang, [0017]-[0019]. *See* Fig. 1A.

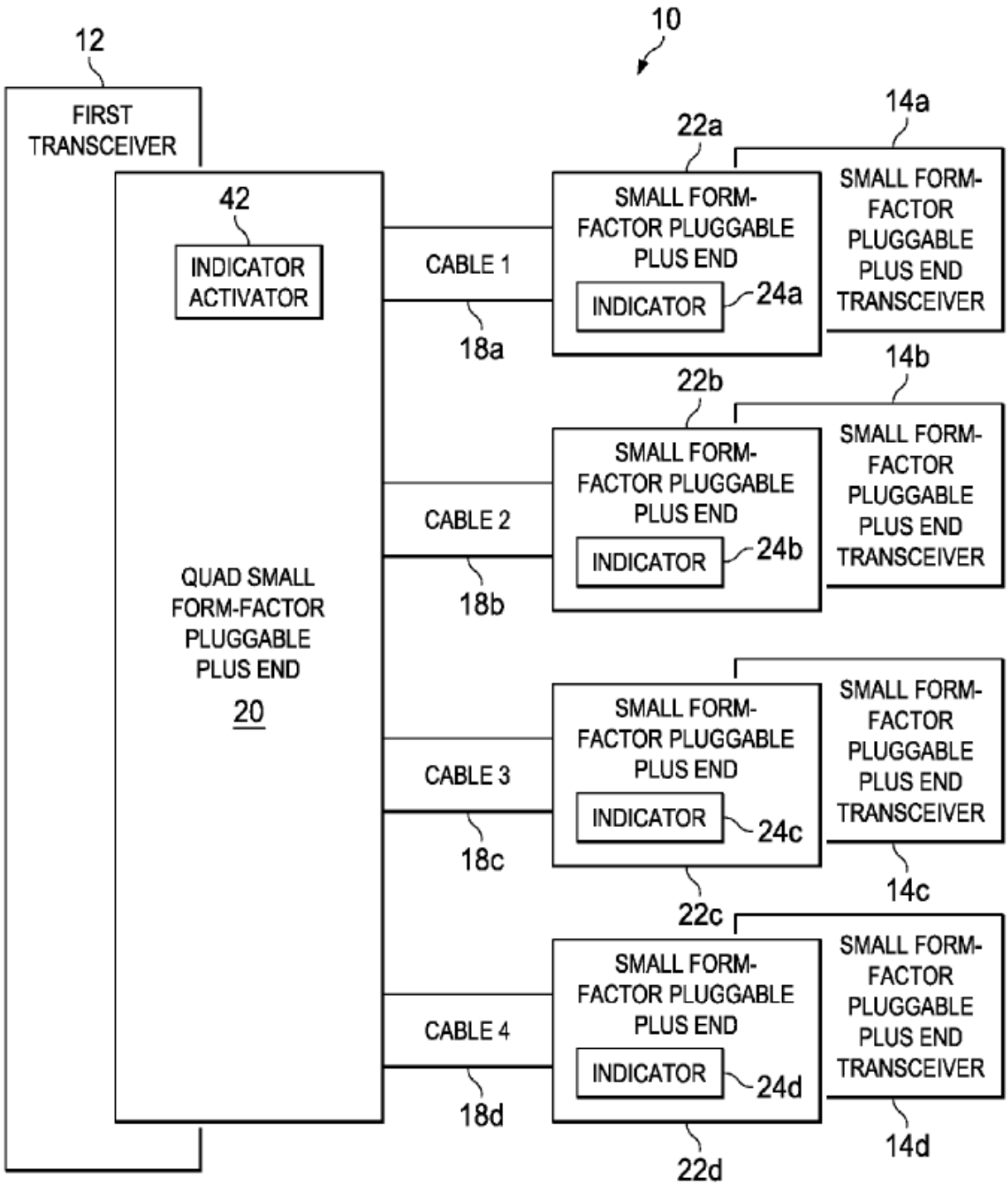


FIG. 1A

252. In another variation shown below, cable 10 includes SFP+ ends on each side, connected by twinaxial copper cable 18a. Tang, Fig. 6, [0045]-[0047].

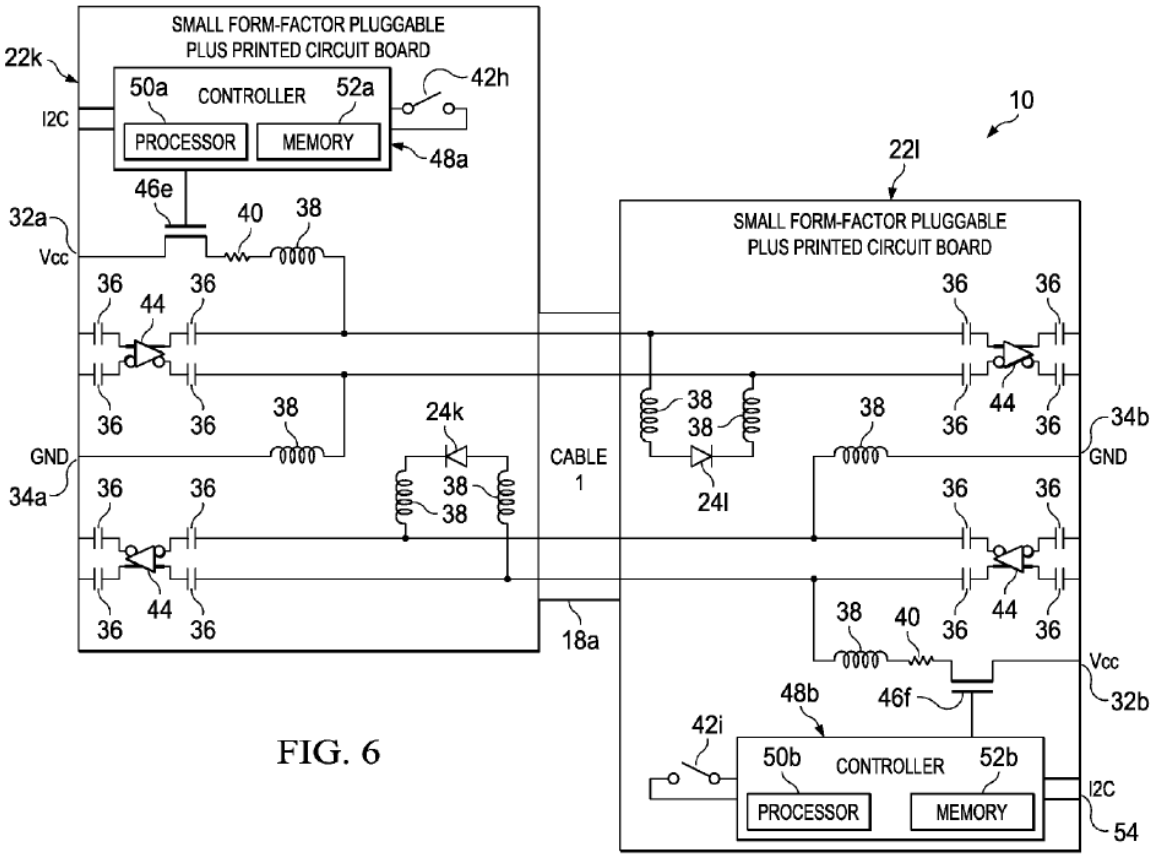


FIG. 6

253. Each SFP+ end 22k, 22l includes two "signal drivers 44 (*e.g.*, CDR)" facing opposite directions for processing signals that are received from or transmitted to the connected transceivers. Tang, [0045]; [0037] (defining "CDR").

2. Discussion of TI-Retimer (EX1008)

254. TI-Retimer is a datasheet for Texas Instruments Incorporated's "DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer." The DS125DF1610 Retimer is a retimer with integrated signal conditioning features including, *e.g.*, a continuous time linear equalizer (CTLE), clock and data recovery (CDR), and a transmit FIR filter for each of its sixteen channels. TI-Retimer, §§3, 7. Figure 2

(below) illustrates the data path for a received input signal IN, as it is processed by a CTLE (EQ), Retimer/CDR, and FIR Filter, before output as signal OUT.

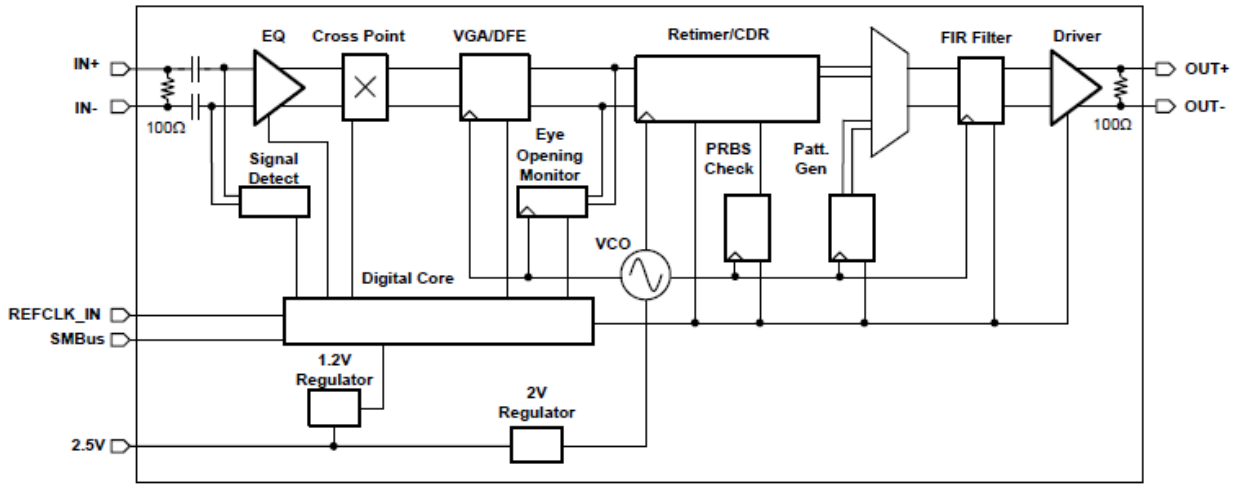


Figure 2. DS125DF1610 Simplified Data Path Diagram

255. The signal conditioning features "enhance… reach and robustness over long, lossy, crosstalk impaired high speed serial links," such as "lossy copper interconnects and backplanes." TI-Retimer, §§3, 7.3.3 (CTLE is an "equalizer"), 7.3.6 ("equalized data is fed into the CDR for clock and data recovery" and "recovered data is then output to the FIR filter"), 7.3.8 (FIR filter "assist[s] with transmit equalization").

256. The DS125DF1610 retimer may be implemented in various places, including in Ethernet network backplane and front port applications. TI-Retimer, §§8.1-8.2.

3. Discussion of Aronson (EX1006)

257. *See* summary of Aronson for Ground 1 above.

4. Discussion of the Tang+TI-Retimer+Aronson Combination

258. As noted in Sections VI.B.1-3, Tang, TI-Retimer, and Aronson each teach signal processing for network communications.

a. Reasons to Combine Tang and TI-Retimer

259. Tang's active Ethernet data cable has signal drivers 44 that include, *e.g.*, CDR. Tang, Abstract, [0014]-[0017], [0045]-[0047] (describing "signal drivers 44 (*e.g.*, CDR); *see also* [0037] ("CDR" means "clock and data recovery"). Tang leaves to the POSA details of how to implement signal drivers 44 and other aspects of the cable, so a POSA implementing Tang's cable would have been motivated to look to known components for implementing Tang's signal drivers 44. Tang, [0052].

260. POSAs had reasons to use TI-Retimer's chip to implement Tang's signal driving circuits 44. Texas Instruments, which produces the DS125DF1610 chip in TI-Retimer, specifically suggests use of the chip in a variety of applications, including in active copper cables. EX1030, 2-7 (use of TI-Retimer's DS125DF1610 chip in active copper cables). Moreover, Tang describes "data cable 10" for 10 Gb "Ethernet connectivity" (Tang, [0016]), which TI-Retimer supports (TI-Retimer, 1, 10 (§6.6, input data rate)). TI-Retimer describes a signal driving circuit of the type used in Tang and was well-suited to use in Tang's active cable because TI-Retimer's chip has the CDR signal processing Tang describes

(Tang, [0037]) and "enhance[s]… robustness over long, lossy, crosstalk impaired high speed serial links," such as "lossy copper interconnects and backplanes" (TI-Retimer, §3), which POSAs understood describe the line-side and host-side connections for the transceivers in the connectors of Tang's active cable.

261. Additionally, standard-based connectors of the type Tang describes were known by POSAs to be customizable with various circuitry, including filters, amplifiers, transceivers, and other "active" components. EX1010, [0065], [0099]. The use of the known TI-Retimer chip would have produced predictable results, consistent with its well documented functions, when used as a signal driver/CDR as in Tang. The benefits of using active components was well known to POSAs. Lugthart-993, 14:45-53 (active cables with transceivers "can achieve a wide variety of advantages" over passive cables by, for example, addressing jitter, noise, and ISI).

262. In Figure 6 below, the Tang/TI-Retimer combination uses a channel of TI-Retimer's chip for each transmit and receive channel in Tang's connectors ("Form Factor Pluggable), with one TI-Retimer chip channel handling the inbound data stream (highlighted yellow below) from the host and the other (shown upside down below) handling the outbound data stream (highlighted blue below) to the host.

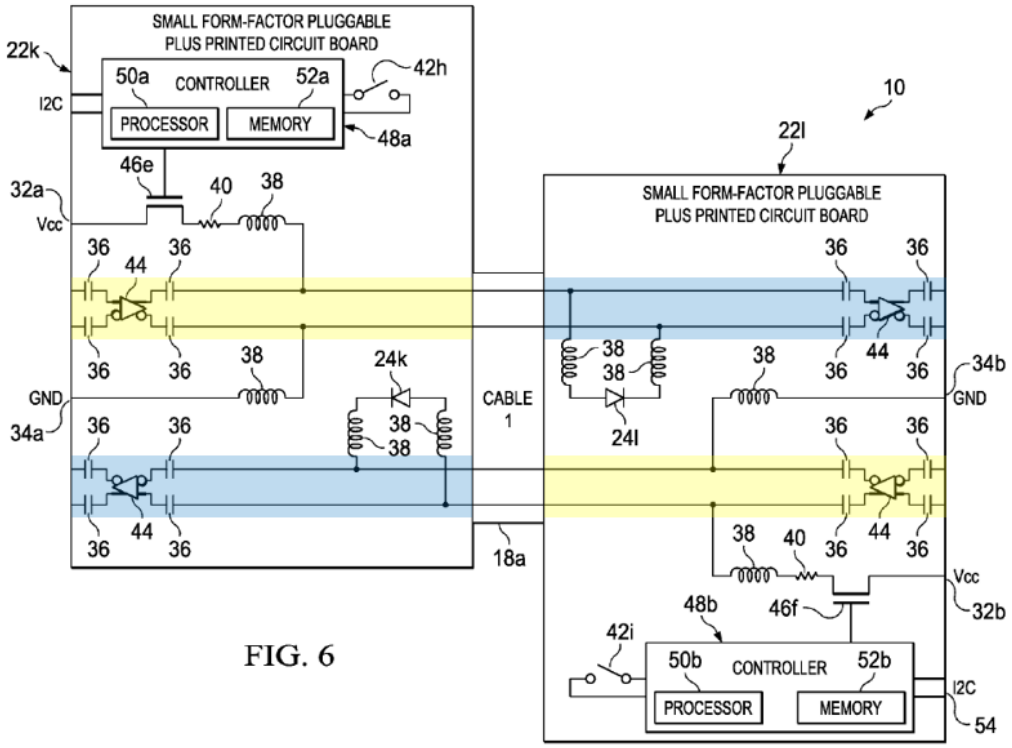


FIG. 6

For example, processing by each of the four signal drivers 44 would be according to the "Simplified Data Path Diagram" shown in Figure 2 of TI-Retimer.

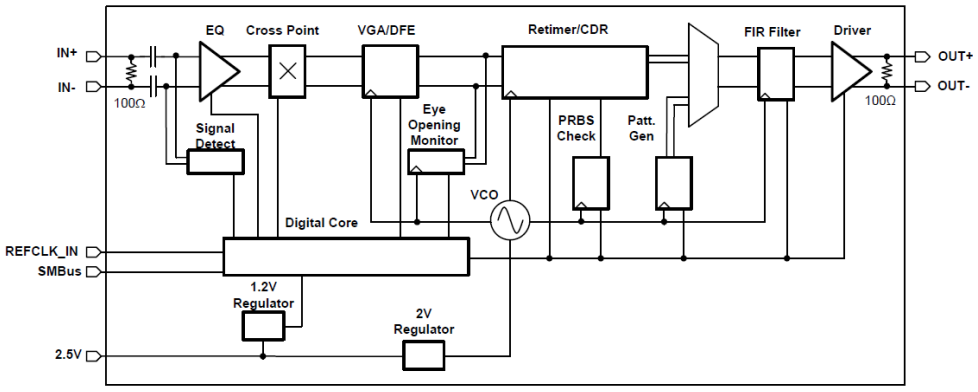


Figure 2. DS125DF1610 Simplified Data Path Diagram

By functionally replacing signal driver 44 in each of the transmit and receive paths in FIG. 6 of Tang with the circuitry corresponding to the "Simplified Data Path Diagram" in Figure 2 of TI-Retimer, signals in the transmit and receive paths of

Tang become more robust with respect to imperfect channel conditions at various points across the cable assembly. TI-Retimer, §3. POSAs would have known that TI-Retimer's processing, including equalization, retiming, and filtering, produces these benefits.

263. While my detailed analysis references Tang's Figure 6 for simplicity (showing two channels that are analogous to the '252 patent's claims), POSAs would have found the TI-Retimer chip advantageous for single-chip implementation in any of Tang's embodiments (or variations thereof) with additional channels (*e.g.*, Tang Figure 1A-1B, 3A-3B, 4A-4B's "quad" ends process eight channels each). Tang, [0017]-[0018]. Thus, the TI-Retimer chip's 16 channels per chip may be used in the variety of configurations described by Tang.

264. Thus, in my opinion, a POSA would have had reasons to combine Tang and TI-Retimer to provide an active cable with enhanced robustness, as discussed above. The combination would have used known components and techniques (cables and chips), according to their conventional uses, with predictable results. I further reference this combination as "Tang+TI-Retimer."

b. Reasons to Further Combine with Aronson

i. Fixed Cable-Independent Parameters for Host-Side Equalization

265. In the figures of the Tang/TI-Retimer combination shown above, the equalizer EQ in the channel handling the yellow-highlighted data stream performs

equalization on inbound signals from the host, and the FIR filter in the channel handling the blue-highlighted data stream performs pre-equalization on outbound signals transmitted to the host.

266. For all of the same reasons discussed in connection with the host-side equalization and pre-equalization in Lugthart-993+Aronson (Ground 1, Section VI.A.3.a.i), POSAs would have implemented the host-side equalization (via the yellow-highlighted EQ) and the host-side pre-equalization (via the blue-highlighted FIR Filter) in Tang/TI-Retimer by using fixed cable-independent parameters to address host-side losses as taught by Aronson and numerous references corroborating a POSA's background knowledge.

ii. Cable-Dependent Parameters For Line-Side Equalization

267. In the figures of the Tang/TI-Retimer combination shown above, the equalizer EQ in the blue-highlighted signal processing channel performs equalization on line-side signals received from across the cable from the other connector, and the FIR filter in the yellow-highlighted signal processing channel performs pre-equalization on signals transmitted across the cable to the other connector.

268. For all of the same reasons discussed in connection with the line-side equalization and pre-equalization in Lugthart-993+Aronson (Ground 1, Section

VI.A.3.a.ii), POSAs would have implemented the line-side equalization (via the blue-highlighted EQ) and the line-side pre-equalization (via the yellow FIR Filter) in Tang/TI-Retimer by using cable-dependent parameters to address cable-side losses as taught by Aronson and numerous references corroborating a POSA's background knowledge.

(1) Adapting The Line-Side Cable-Dependent Parameters

269. For all of the same reasons discussed in connection with the line-side equalization and pre-equalization in Lugthart-993+Aronson (Ground 1, Section VI.A.3.a.ii.(1)), POSAs had reason to use adaptive cable-dependent parameters for the line-side equalization (via the blue-highlighted EQ) and line-side pre-equalization (via the yellow FIR Filter) in Tang/TI-Retimer as taught by Aronson and numerous references corroborating a POSA's background knowledge of the desirable design choice option of using adaptive equalization parameters. This adaption would have been obvious to perform during TI-Retimer's CDR lock acquisition process—*i.e.*, during an adjustment period when the system is preparing to reliably process signals. TI-Retimer, §7.3.3 (CTLE adaption).

(2) Line-Side Cable-Dependent Parameters Determined During Manufacture-Testing and Fixed During Normal Usage

270. For all of the same reasons I discussed above in connection with the line-side equalization and pre-equalization in Lugthart-993+Aronson (Ground 1,

Section VI.A.3.a.ii.(2)), POSAs had reason to determine the cable-dependent parameters for the line-side equalization (via the blue-highlighted EQ) and line-side pre-equalization (via the yellow FIR Filter) in Tang/TI-Retimer during manufacture-testing and then fix those parameters during normal usage as taught by Aronson and numerous references corroborating a POSA's background knowledge of the desirable design choice option of using adaptive equalization parameters.

iii. Reasonable Expectation of Success

271. POSAs would have had a reasonable expectation of success in implementing Tang+TI-Retimer in any and all of the ways discussed above. As shown Sections §§VI.A.3.a and VI.B.4.b (Reasons to Combine in Grounds 1 and 2), Aronson and numerous other references corroborating a POSA's background knowledge demonstrate that every one of above-discussed design choices was well-known. Implementing these techniques that were well-known for use in active cables like Tang's, using signal processing circuits like TI-Retimer's, was well within a POSA's capabilities. I further reference this combination as "Tang+TI-Retimer+Aronson."

272. POSAs understood that TI-Retimer worked with or without adaptation because it provides configurable settings for enabling/disabling adaptation and other functions. TI-Retimer, §7.5, Address 31 (describing a setting for "no

adaption" of the CTLE). If every equalization component of TI-Retimer does not specifically implement selectable fixed and adaptive equalization, the known benefits of fixed and adaptive equalizers (and tradeoffs between choosing one over the other) provided a reason to implement that functionality, as discussed above. *See*, for example, my discussions in Section VI.A.3.a above. Tang+TI-Retimer+Aronson with compensation for the host, compensation for the cable, and fixed or adaptive equalization would have required no more than ordinary skill in the art.

273. Finally, POSAs would have had confidence in implementing the Tang+TI-Retimer+Aronson combination especially because TI-Retimer is a commercially available solution, which was designed to work in providing active Ethernet cables.

5. Mapping of Tang, TI-Retimer, and Aronson to claims 1-14

a. Claim 1

i. Preamble [1.PRE]: An active Ethernet cable that comprises:

274. Tang+TI-Retimer+Aronson meets [1.PRE] because it teaches cable 10 that is an "active twinaxial cable" with SFP+ ends for "ten (10) Gigabit Ethernet connectivity." Tang, Fig. 6 (below, showing cable 10), [0016], [0045].

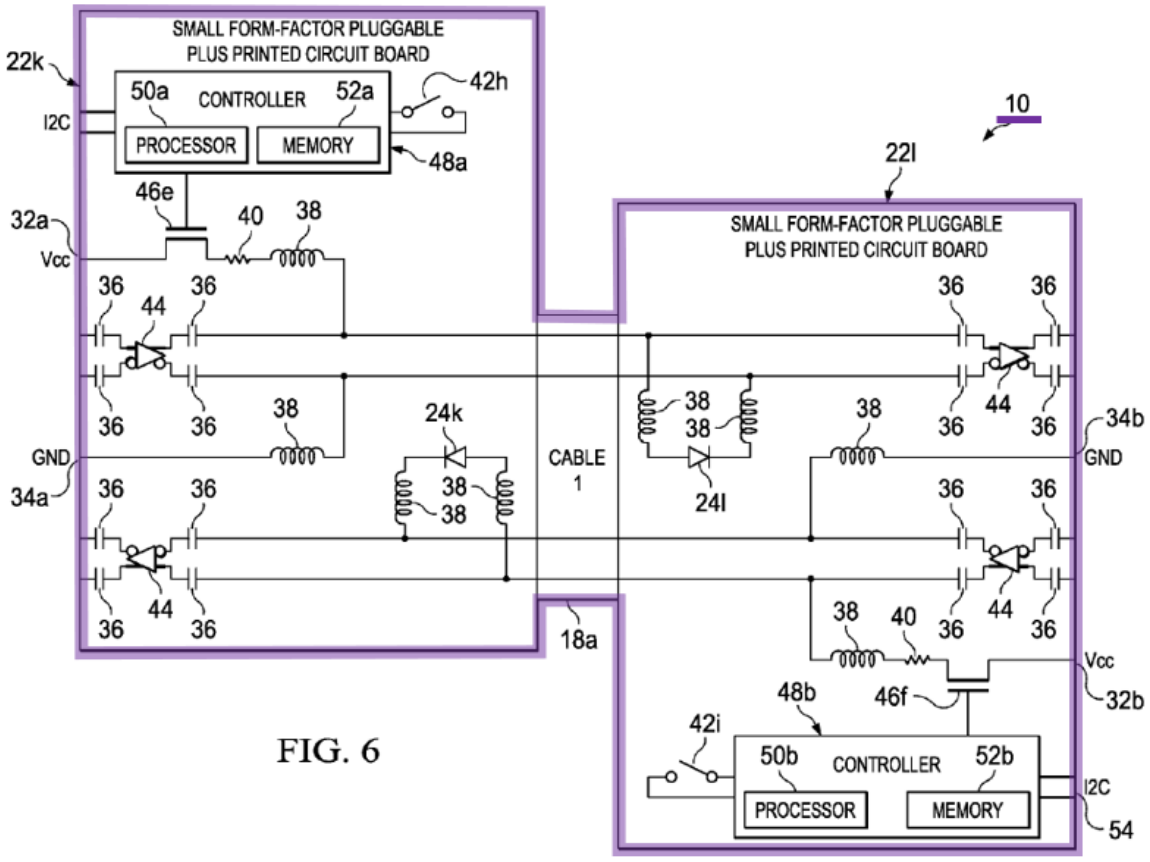


FIG. 6

As I will discuss below, it is my opinion that Tang+TI-Retimer+Aronson meets all the limitations of claim 1.

ii. Limitation [1.A]: electrical conductors connected between a first connector and a second connector,

275. Tang+TI-Retimer+Aronson meets [1.A] because cable 10 is a twinaxial copper cable 18a that includes *electrical conductors connected between a first connector* (SFP+ end 22k) *and a second connector* (SFP+ end 22l). Tang, Fig. 6 (annotated below), [0015] ("small form-factor pluggable plus (SFP+) end"), [0045]-[0047] (current flows through cable 18a).

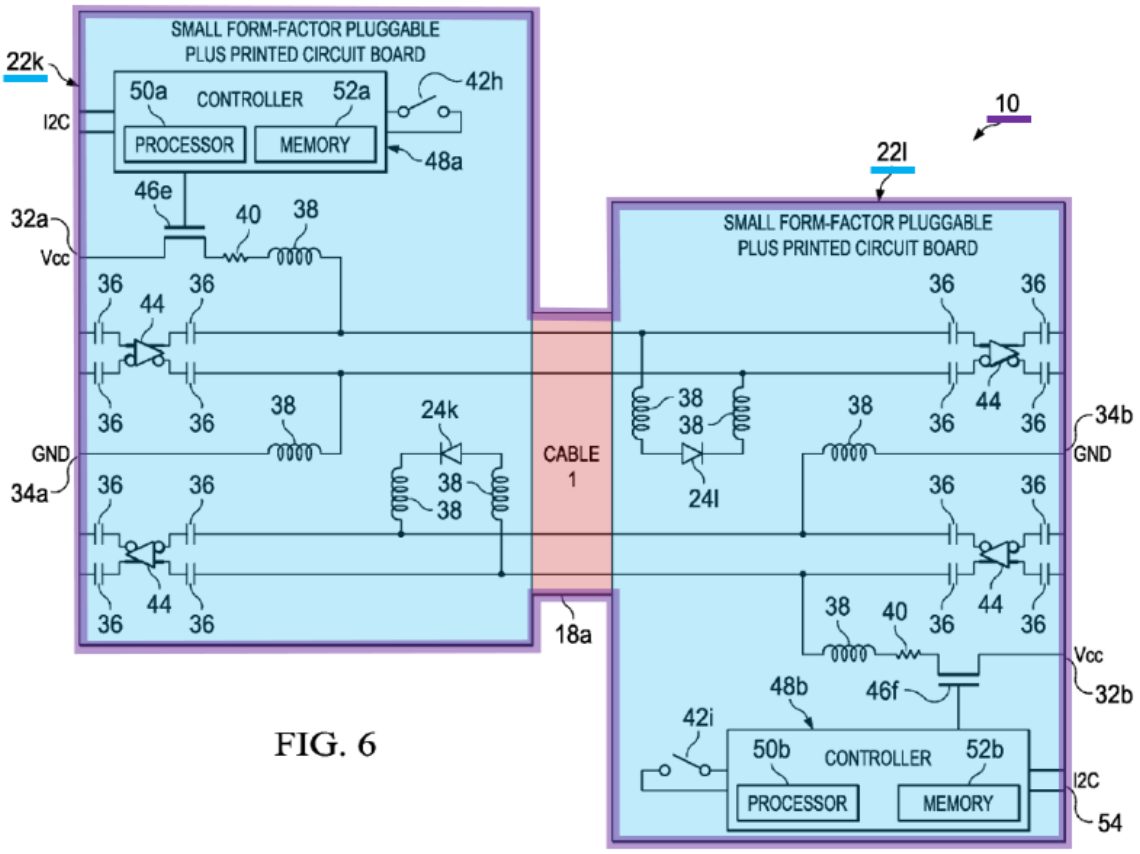


FIG. 6

276. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [1.A].

iii. Limitation [1.B]: each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,

(1) Limitation [1.B.i]: "*each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device*"

277. Tang+TI-Retimer+Aronson meets [1.B.i] because *each of the first and second connectors* (SFP+ ends 22k and 22l) is *adapted to fit into an Ethernet port of a corresponding host device*. Tang, [0002]. SFP+ ends 22k and 22l are adapted to connect to an SFP+ housing port of transceivers 12 and 14, respectively. Tang, [0046]-[0047], Fig. 1A (below), Fig. 6.

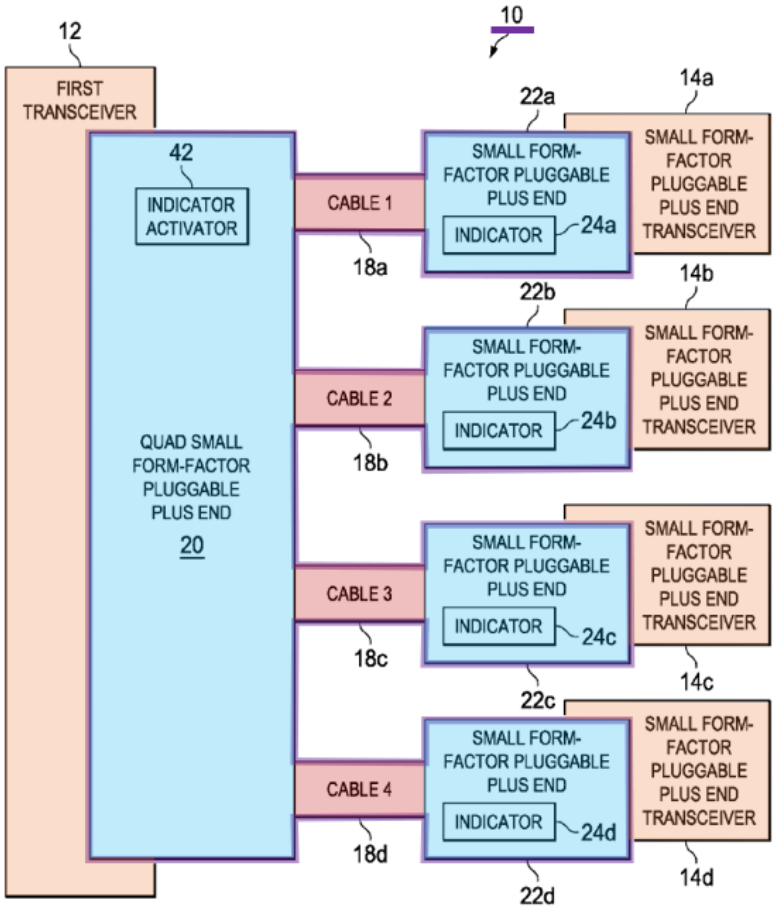


FIG. 1A

278. Transceivers 12 and 14 correspond to respective host devices, like a server, router or switch, and have "SFP+ end housing[s]" for connection. Tang, [0002], [0021], [0026]-[0028] (SFP+/QFP assemblies "plugged [in/into]" cages, racks, and housings. "*Ethernet port of a corresponding host device*" comprises a port that receives these industry-standard SFP connectors. As I discussed for [1.B.i] in Ground 1 (Section VI.A.4.a.iii above), the '252 patent relates to Ethernet communications and follows the Ethernet standards regarding physical connections, which include SFP and QSFP-type port connectors. Thus, POSAs

understood that Tang's SFP+ cable connectors (or modules) fit into ports of the corresponding host device transceivers. EX1027, 1 and 11 (modules are plugged into and retained inside port cages), 7 (illustrating an SFP+ module and cage), 18 (examples of one-port and two-port transceiver cages).

279. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [1.B.i].

(2) Limitation [1.B.ii]: "*to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,*"

280. Tang+TI-Retimer+Aronson's Ethernet cable 10 facilitates bidirectional communication between two connected host devices, which is accomplished according to the IEEE 802.3 standard. EX1028, 54 ("This standard defines Ethernet local area, access and metropolitan area networks."), 55 ("Full duplex operation allows simultaneous communication between a pair of stations.").

281. Tang+TI-Retimer+Aronson meets [1.B.ii] because Tang's SFP+ ends 22k, 22l each includes at least two signal drivers 44 handling data flows in opposite directions. Tang, [0045], Fig. 6. Tang Fig. 6 is annotated below to show one upper data stream flowing from the host on the left to the host on the right and another lower data stream flowing in the opposite direction, with both data streams conveyed by electrical signals. The orientation of the signal drivers 44 points in the

direction that electrical signals are output of the signal drivers 44. Annotated Fig. 6 illustrates that Tang+TI-Retimer+Aronson meets [1.B.ii] because *each of the first and second connectors* (SFP+ ends 22k and 22l) *receives an electrical signal conveying an inbound data stream to the cable* from its connected host and provides to that host *an electrical output signal conveying an outbound data stream from the cable*.

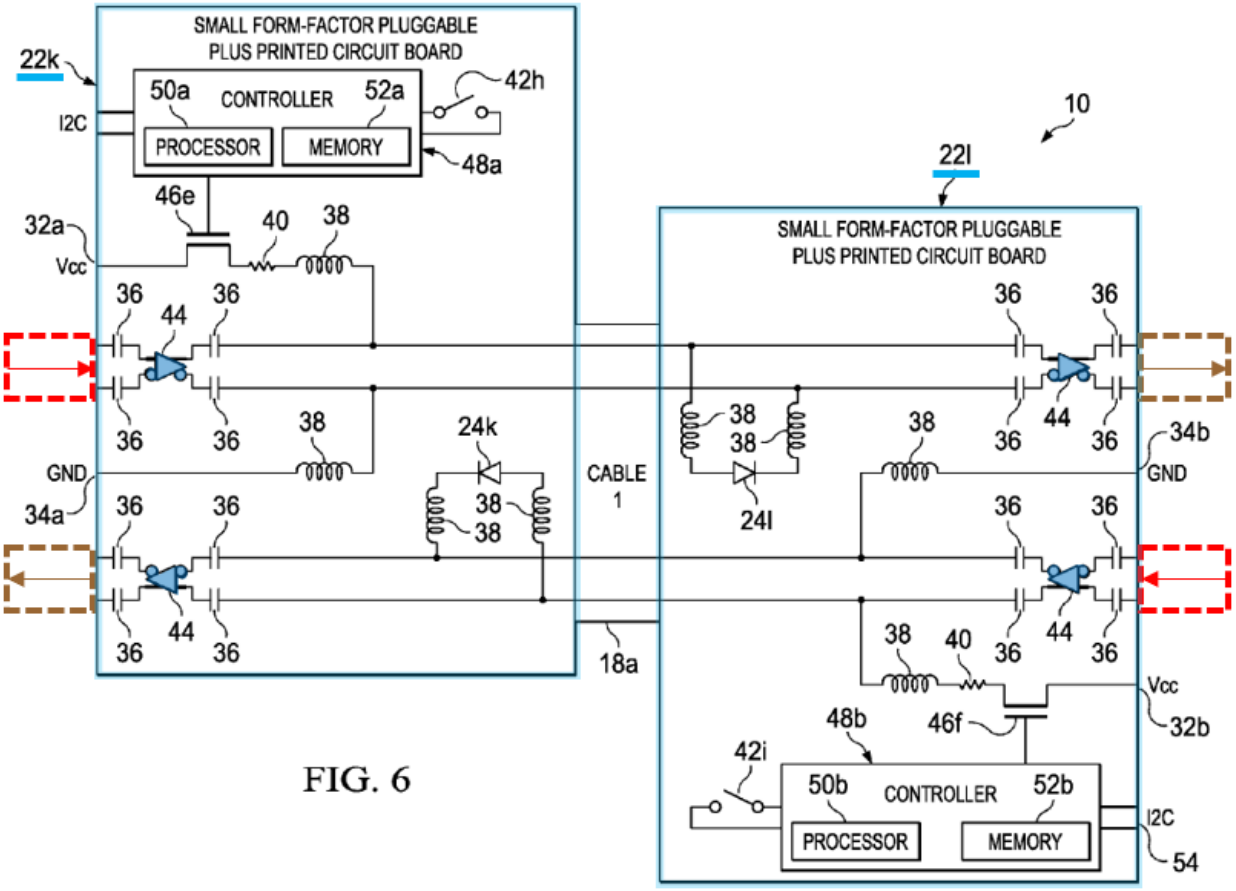


FIG. 6

282. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [1.B.ii].

iv. Limitation [1.C]: each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,

283. Tang+TI-Retimer+Aronson meets [1.C] because *each of the first and second connectors* (SFP+ ends 22k and 22l) *include[es] a respective transceiver* (TI-Retimer's retimer that implements Tang's signal driver 44) *that performs CDR on the electrical input signal to extract and remodulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream* as shown in annotated Fig. 6 below.

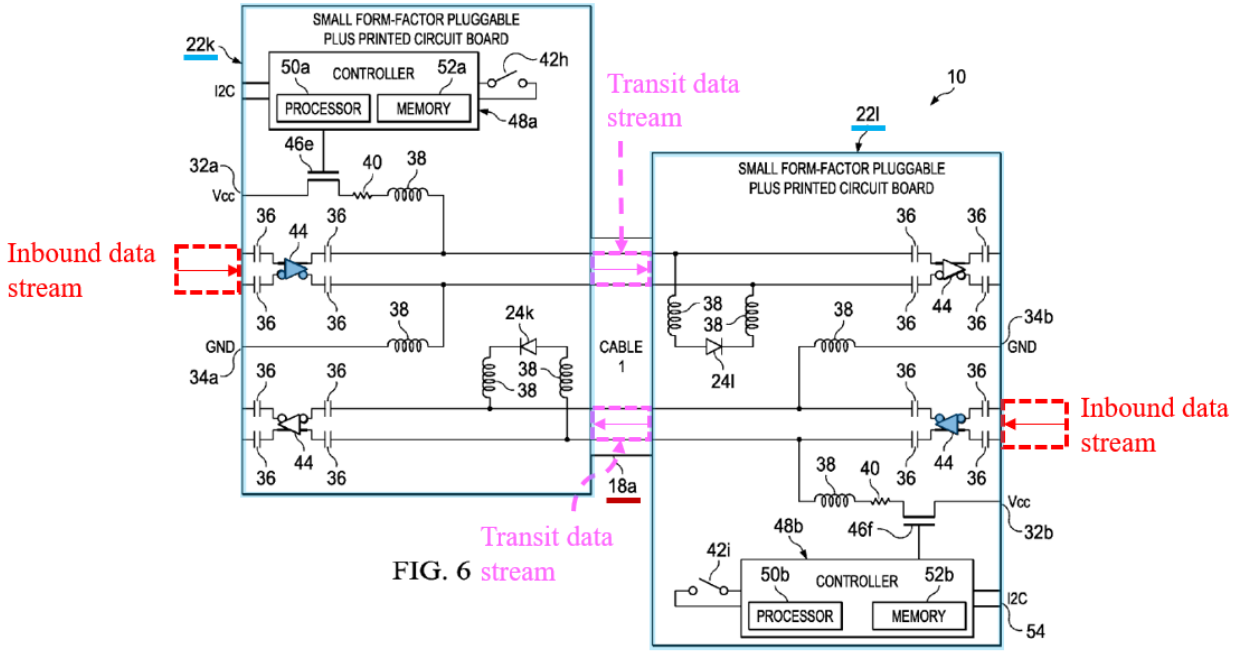
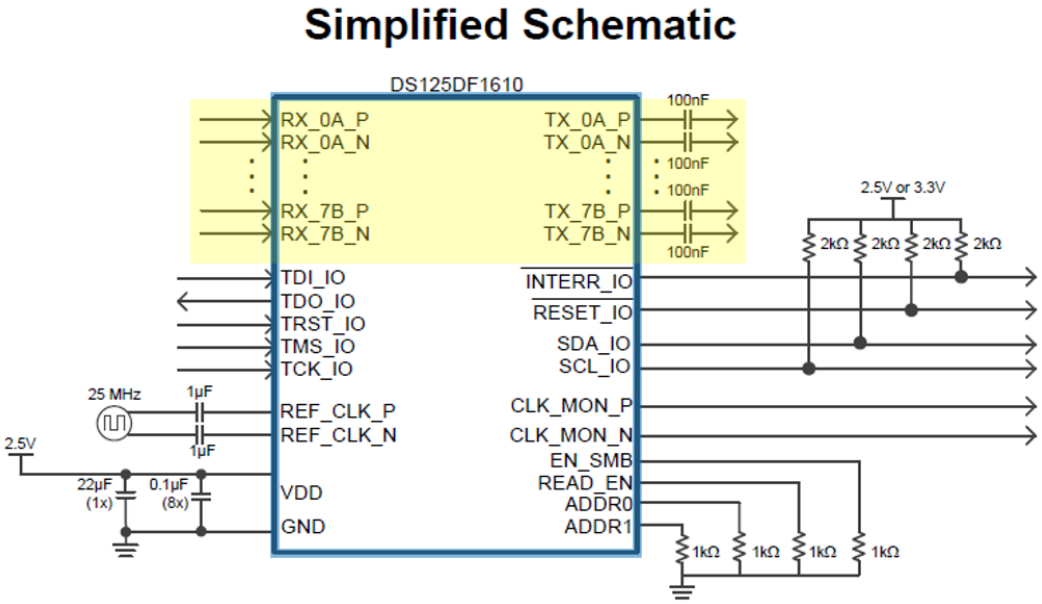


FIG. 6

284. TI-Retimer's retimer is illustrated in the Simplified Schematic and Figure 1 below. The highlighted pins illustrate sixteen channels of data, with each

channel having two differential (Positive and Negative) input pins (RX_0A_P/N through RX_7B_P/N) to receive the channel of data and corresponding output pins (TX_0A_P/N through TX_7B_P/N) to transmit the channel of data after processing. TI-Retimer, §§3, 7.2. The Simplified Schematic shows all 16 channels, while Figure 1 shows 4 channels in "1 of 4 Quads"—*i.e.*, 4 of the 16 total channels. Thus, TI-Retimer's retimer is a transceiver that, when used in Tang's cable, receives one or more inbound data streams (on RX_0A_P/N through RX_7B_P/N) and transmits one or more transit data streams (via pins TX_0A_P/N through TX_7B_P/N).



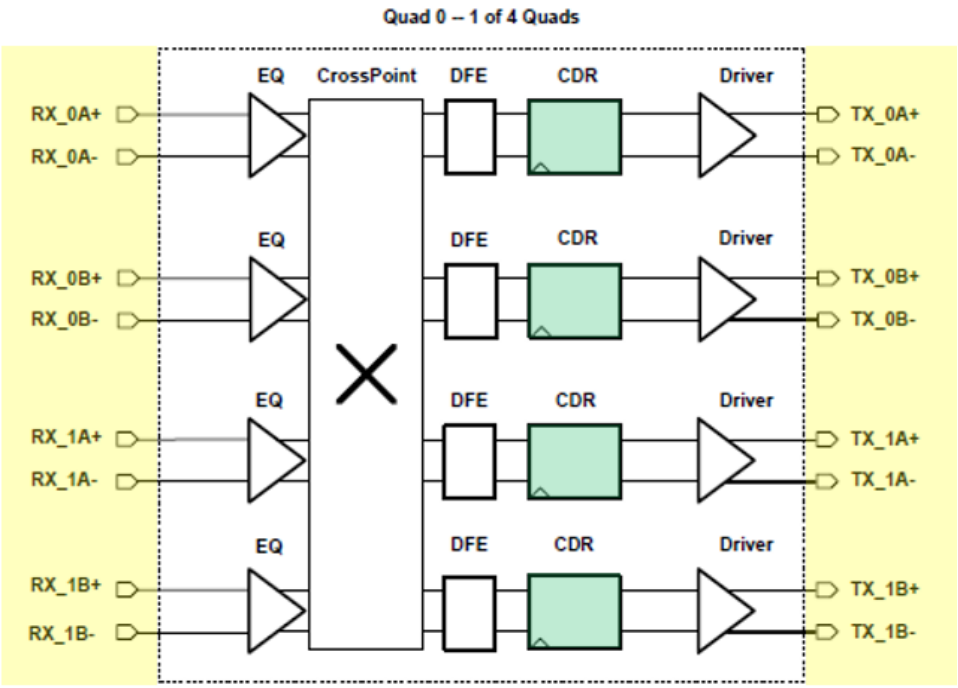


Figure 1. DS125DF1610 Simplified Cross Point Diagram

285. Figure 1 above shows four channels and illustrates that TI-Retimer's retimer processes each data channel by performing "clock and data recovery (CDR)." TI-Retimer, §§3, 7.1. A channel's data path is shown in more detail in TI-Retimer Figure 2 below, which is annotated to illustrate the input signal conveying an inbound data stream and the transit signal conveying a transit data stream in Tang's cable when TI-Retimer's retimer implements Tang's signal driver 44.

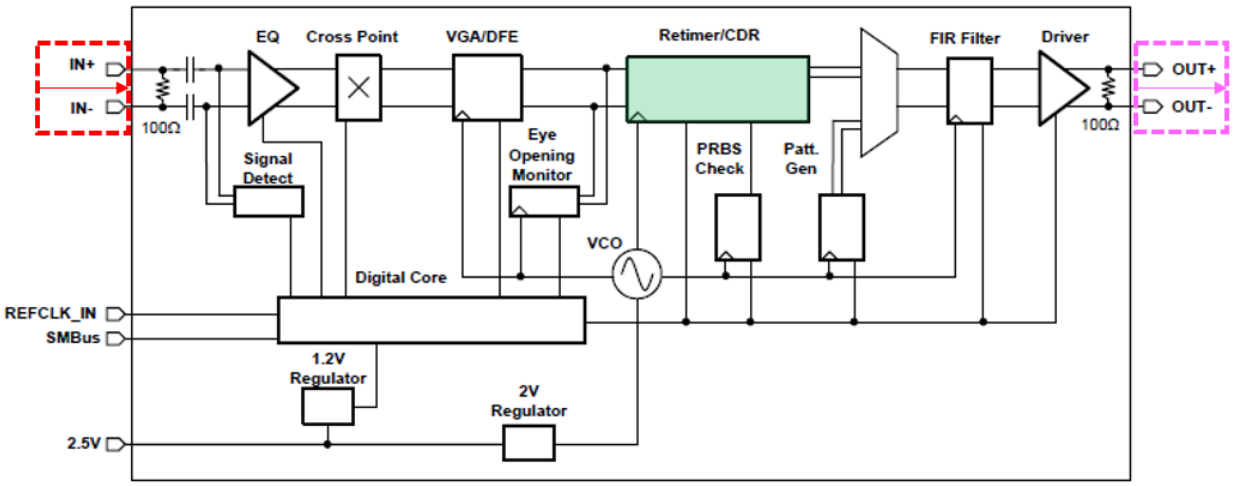


Figure 2. DS125DF1610 Simplified Data Path Diagram

286. The Retimer/CDR circuit *performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream*. TI-Retimer, §7.3.6. As discussed for [1.C] in Ground 1 above (Section VI.A.4.a.iv), the '252 patent specification makes clear that the input signal from the host can be pre-processed before CDR is performed on it.

287. POSAs understood that TI-Retimer's retimer remodulates the data for output as the transit data stream because after extracting the input signal's data and its timing using an analog-to-digital process, the retimer generates a newly-timed signal for equalization by the FIR Filter (a digital-to-analog process) to convey the transit data stream as an analog signal over the cable conductors, where the newly-timed signal is a "*re-modulation*" of the data. TI-Retimer, §7.3.6 ("…equalized

data is fed into the CDR for clock and data recovery. The recovered data is then output to the FIR filter and differential driver."). As I explained above in Section IV.D.4, CDRs function by taking an analog input signal, recovering a clock (timing information) from that signal, and using that recovered clock to sample the analog input signal and generate a new data stream with the sampled data. In Tang+TI-Retimer+Aronson, the retimer ultimately outputs a differential signal after conditioning by the FIR filter, as shown in Figure 2 above. TI-Retimer, §§7.3.6-7.3.9. The output differential signal is an analog representation of the recovered digital data and, therefore, a result of "*re-modulating*" the data. I have also been informed that the Patent Owner in district court has pointed to alleged infringement by products that re-modulate via retiming—*i.e.*, that CDR includes or facilitates a re-modulation of the data. EX1039, 11-17 ("'retiming'… to extract and re-modulate"). To the extent TI-Retimer is considered to not expressly disclose this, that would have been the conventional and obvious way to implement what TI-Retimer discloses, because unless the recovered data is merely meant for internal storage on the chip and is not forwarded to the next connected device (*i.e.*, across cable lines to the far-end transceiver, or to a connected host transceiver, as shown in Tang+TI-Retimer+Aronson), the recovered underlying data will be represented in an output signal having voltage levels representing that data—a "*re-modulation*" of the data.

288. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [1.C].

v. Limitation [1.D]: the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and

289. Tang+TI-Retimer+Aronson meets [1.D] because *the respective transceiver* (TI-Retimer's retimer implementing Tang's signal driver 44) *for each of the first and second connectors* (SFP+ ends 22k and 22l) *perform[s] CDR on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable* as shown in annotated Fig. 6 below.

290. TI-Retimer's retimer implementing Tang's signal driver 44 (highlighted blue below) performs CDR for respective transit signals conveying transit data streams received from cable 18a (electrical conductors) to generate output signals conveying outbound data streams that exit cable 10 to respective hosts, as shown in Tang Figure 6 and TI-Retimer Fig. 2 below. For similar reasons to those discussed for [1.C] above, POSA's understood that TI-Retimer's retimer remodulates the data as the outbound data after extracting the input signal's data and generating a newly-timed signal that is a "*re-modulation*" of the data, or that

would have been the conventional and obvious way to implement what TI-Retimer discloses.

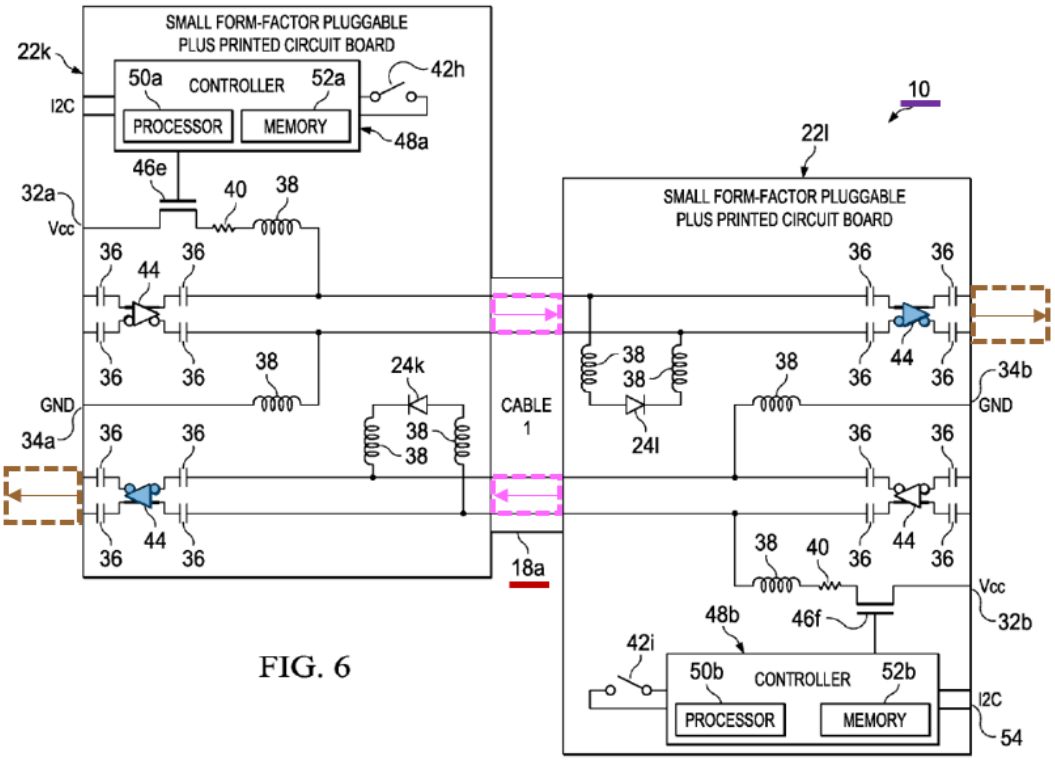


FIG. 6

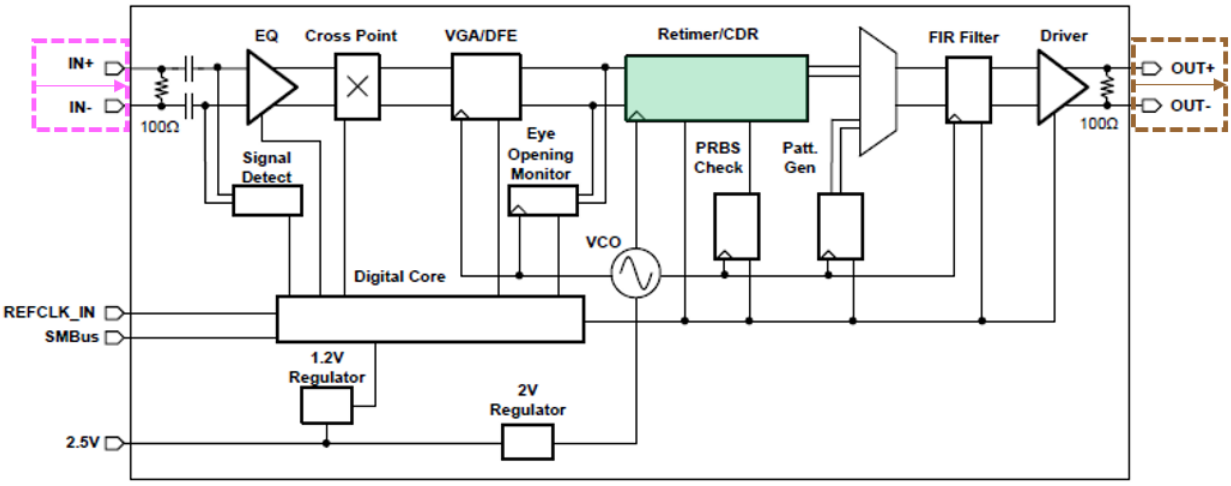


Figure 2. DS125DF1610 Simplified Data Path Diagram

291. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [1.D].

vi. Limitation [1.E]: the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

292. Tang+TI-Retimer+Aronson meets [1.E] because Tang+TI-Retimer+Aronson's *transceivers* (TI-Retimer's retimer) each performs equalization *for the remodulation of the transit data stream as the outbound data stream* (by the retimer's FIR filter) and *for the [CDR] performed on the electrical input signal* (by the retimer's EQ), both using *fixed cable-independent parameters*.

293. As I discussed in Section VI.B.4 (explaining the combination), and Sections VI.B.5.a.iv-v ([1.C]-[1.D]), in Tang+TI-Retimer+Aronson, TI-Retimer's retimer implements Tang's signal driver 44 and is used to handle both the inbound data stream and the outbound data stream as highlighted blue and yellow, respectively, in Tang Fig. 6 below.

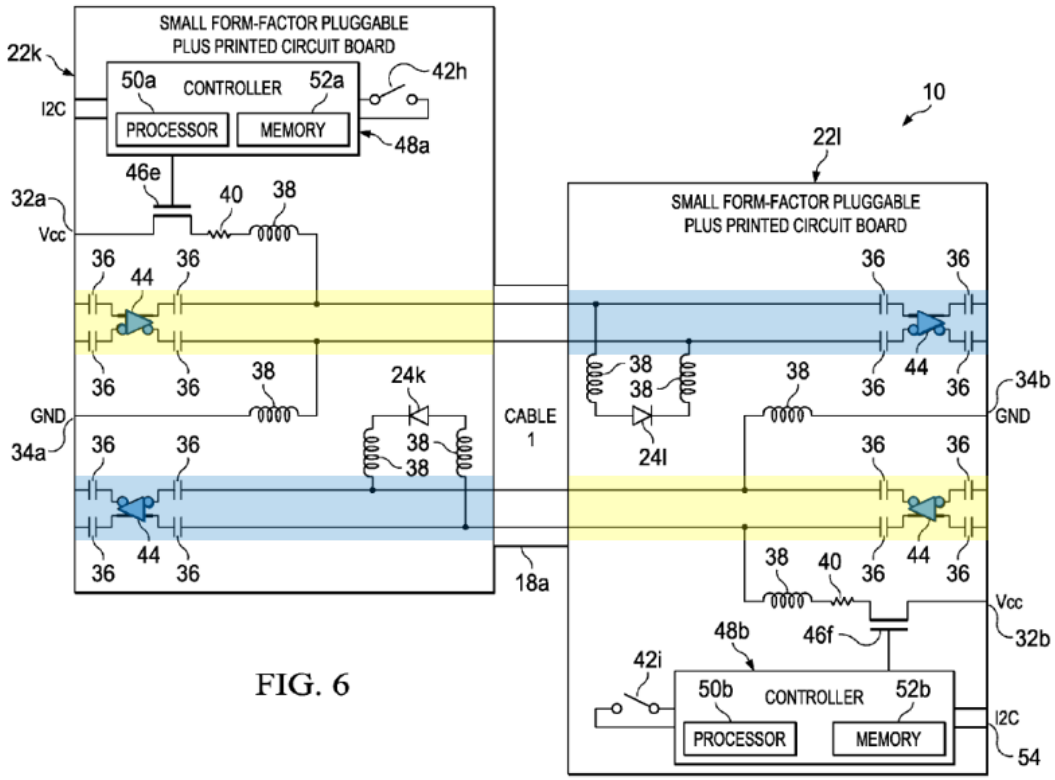


FIG. 6

294. TI-Retimer's Figure 2 is annotated twice below – once to show the retimer processing the inbound data stream (top) and the other showing the retimer processing the outbound data stream (bottom). In the top (inbound from a host on the left) use case below, EQ to equalizes an input signal from a host transceiver for Retimer/CDR circuit. TI-Retimer, §7.3.3. In the bottom (outbound to a host on the right) use case, FIR Filter equalizes the remodulated signal provided as the output signal transmitted to a host transceiver. TI-Retimer, §§3, 7.3.8. Equalizing the inbound signal before performing CDR and pre-equalizing the remodulated signal before transmitting it to the host meets "*employing … equalization parameters for each of the remodulation of the transit data stream as the outbound data stream,*

and the [CDR] performed on the electrical signal" for the same reasons discussed for [1.E] in Ground 1 above (Section VI.A.4.a.vi).

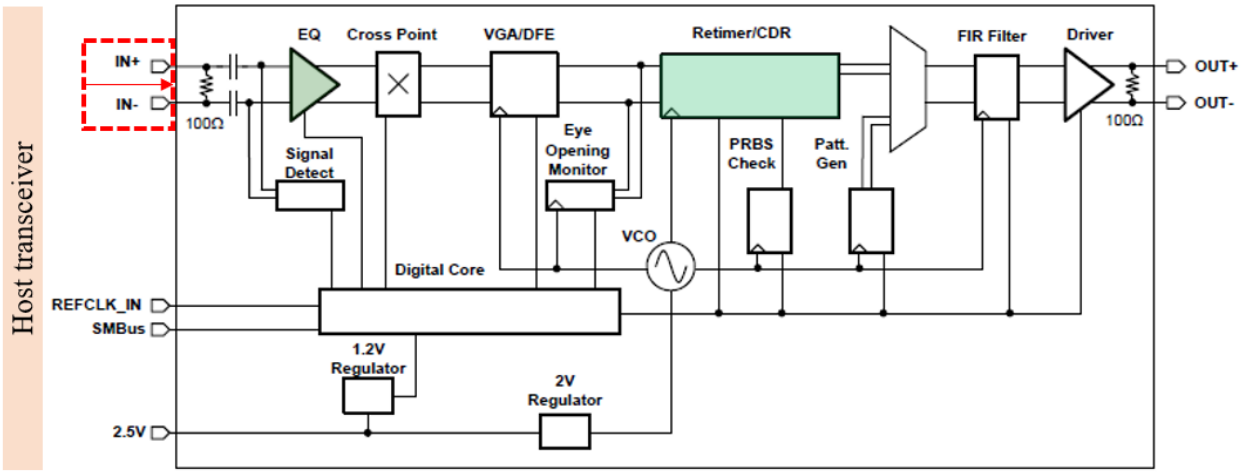


Figure 2. DS125DF1610 Simplified Data Path Diagram

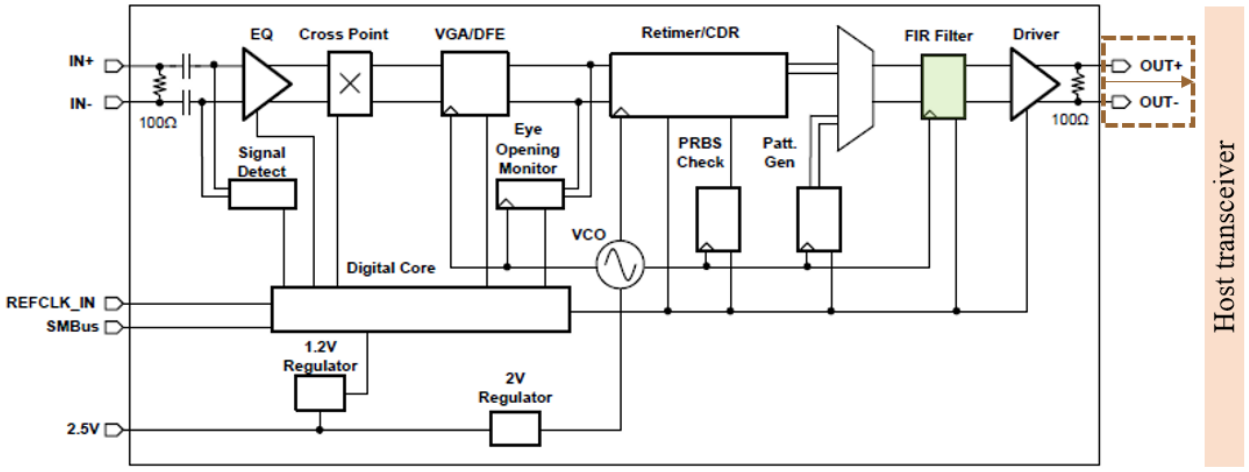


Figure 2. DS125DF1610 Simplified Data Path Diagram

295. As discussed above in Section VI.B.4.b.i, in the Tang+TI-Retimer+Aronson combination, the host-side equalization (performed by EQ) and pre-equalization (performed by FIR Filter) use fixed cable-independent parameters

to address host-side losses as taught by Aronson and numerous references corroborating a POSA's background knowledge.

296. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [1.E].

b. Claim 2: The active Ethernet cable of claim 1, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal.

297. Tang+TI-Retimer+Aronson meets claim 2.

298. As I discussed in Sections VI.B.4 and VI.B.5.a.iv-v, in Tang+TI-Retimer+Aronson, TI-Retimer's retimer implements Tang's signal driver 44 and is used to handle both generation of the transit signal across the cable (highlighted yellow) and the receipt of the transit signal over the cable (highlighted blue) in Tang Fig. 6 annotated below.

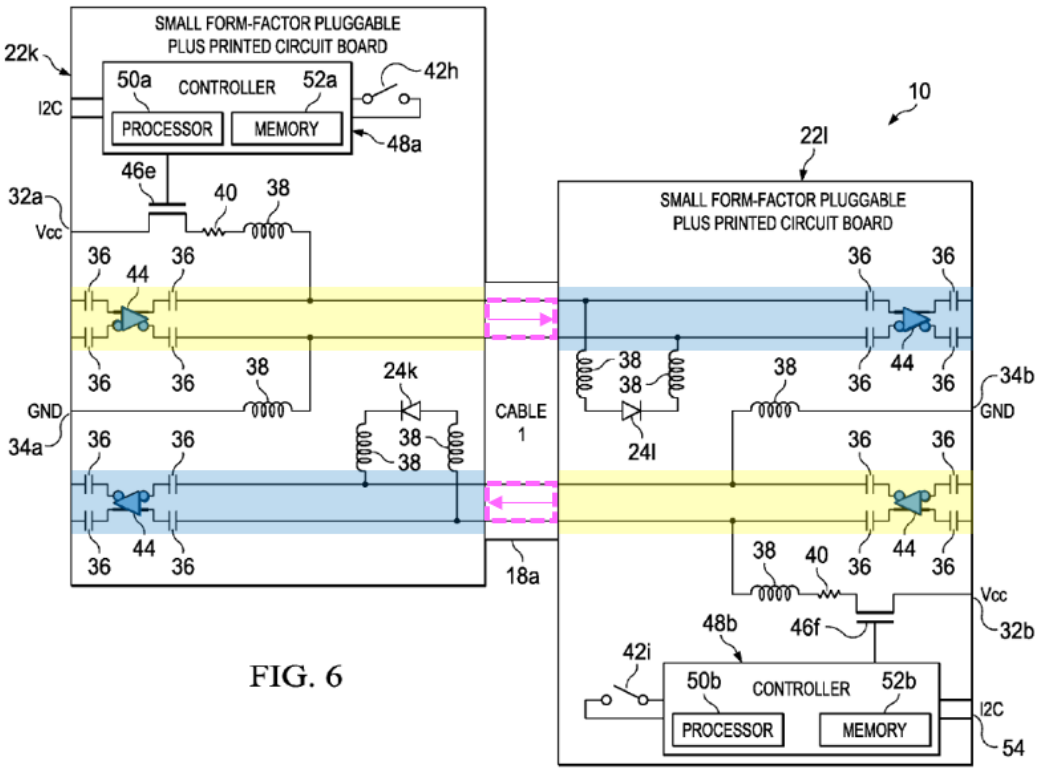


FIG. 6

299. TI-Retimer's Figure 2 is annotated twice below – once to show the retimer processing the transit signal for transmission over the cable (top, cable on the right side) and the other showing the retimer processing the transit signal received from the other side of the cable (bottom, cable on the left side). In the top use case, FIR Filter equalizes the remodulated signal provided as the transit signal transmitted over cable 18a. TI-Retimer, §§3, 7.3.8. In the bottom use case, EQ equalizes the transit signal received over cable 18a for Retimer/CDR circuit. TI-Retimer, §7.3.3. Equalizing the transit signal before performing CDR and pre-equalizing the transit signal before transmission over the cable meets "*employing … equalization parameters for… the remodulation of the inbound data stream for*

transit, and the [CDR] performed on the electrical transit signal" for the same reasons I discussed for claim 2 in Ground 1 (Section VI.A.4.b).

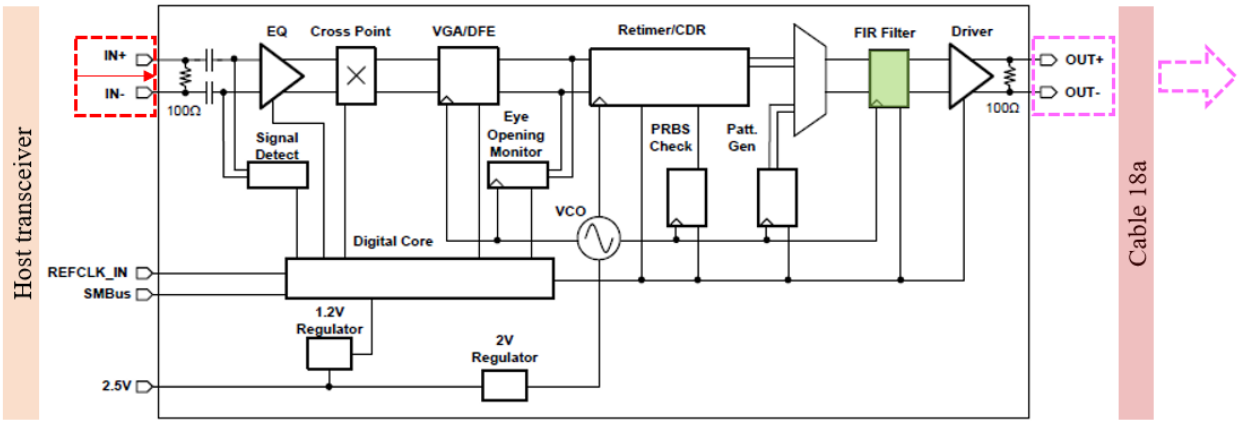


Figure 2. DS125DF1610 Simplified Data Path Diagram

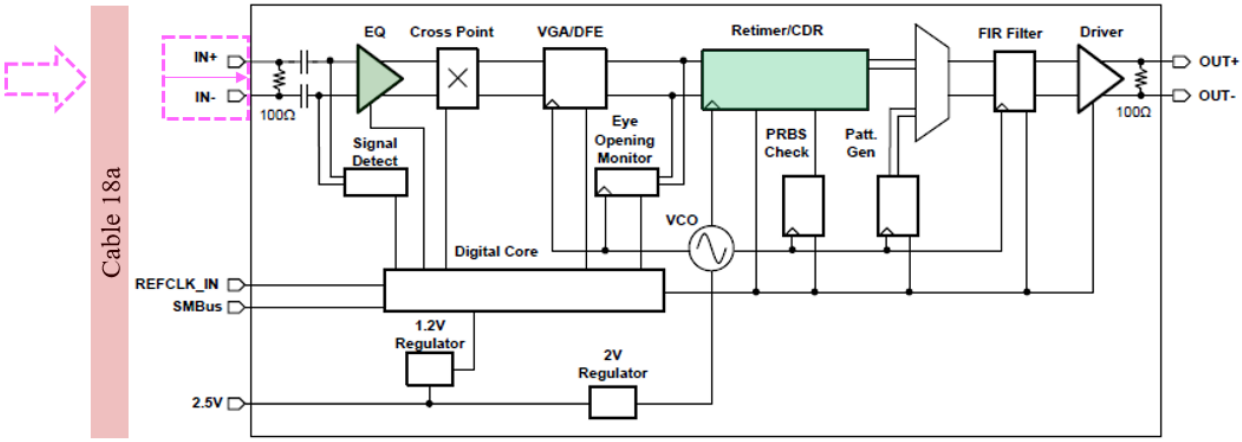


Figure 2. DS125DF1610 Simplified Data Path Diagram

300. As discussed above in Section VI.B.4.b.ii, in the Tang+TI-Retimer+Aronson combination the cable-side equalization (performed by EQ) and pre-equalization (performed by FIR Filter) use cable-dependent parameters to address cable-side losses as taught by Aronson and numerous references corroborating a POSA's background knowledge. Aronson, 14:33-43, 15:1-8.

301. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets claim 2.

c. Claim 3: The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.

302. Tang+TI-Retimer+Aronson meets claim 3 because, as I discussed in Section VI.B.4.b.ii.(1), in the Tang+TI-Retimer+Aronson combination *said cable-dependent equalization parameters* used by TI-Retimer's EQ and FIR Filter for cable-side equalization and pre-equalization, respectively (as discussed for claim 2 above), are *adapt[ed] during usage of the Ethernet cable* as taught by Aronson and numerous references corroborating a POSA's background knowledge. Aronson, Figs. 12A-12B, 15:1-8.

303. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets claim 3.

d. Claim 4: The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing -testing of the Ethernet cable.

304. Tang+TI-Retimer+Aronson meets claim 4 because, as I discussed in Section VI.B.4.b.ii.(2), in the Tang+TI-Retimer+Aronson combination *said cable-dependent equalization parameters* used by TI-Retimer's EQ and FIR Filter for cable-side equalization and pre-equalization, respectively (as discussed for claim 2 above), are *fixed during normal usage of the Ethernet cable* and *determined during manufacturing-testing of the Ethernet cable* as taught by Aronson and numerous references corroborating a POSA's background knowledge. *See also* my

discussion of claim 4 in Ground 1 (Sections VI.A.3.b.ii and VI.A.4.d). Aronson, 14:35-39, 15:4-8, 15:21-23 (describing factory-set cable-dependent equalization parameters). Cable equalization parameters that are "set" at the factory during manufacturer are not expected to change after manufacture and are therefore "fixed" during normal usage of the cable. *See* EX1023, 8:10-17 (in data processing context, equalizer coefficients that are factory set are "fixed").

305. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets claim 4.

e. Claim 6

306. Tang+TI-Retimer+Aronson meets claim 6 for essentially the same reasons it meets claim 1. Claim 6 recites a "communication method" using a "network cable" having limitations mirroring those in claim 1.

i. Preamble [6.PRE]: A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:

307. Tang+TI-Retimer+Aronson meets [6.PRE] because its cable 10 is used in a communications method meeting all the steps of claim 6 as detailed below, and is a *network* (*e.g.*, Ethernet) *cable having conductor pairs* (twinaxial copper conductors) *electrically connecting a first connector* (SFP+ end 22k) *to a second connector* (SFP+ end 22l). Tang, [0015] (describing a "twinaxial copper cable"), Fig. 6 (annotated below). *See* my discussions of limitations [1.PRE]-[1.B.ii] above (Sections VI.B.5.a.i-iii).

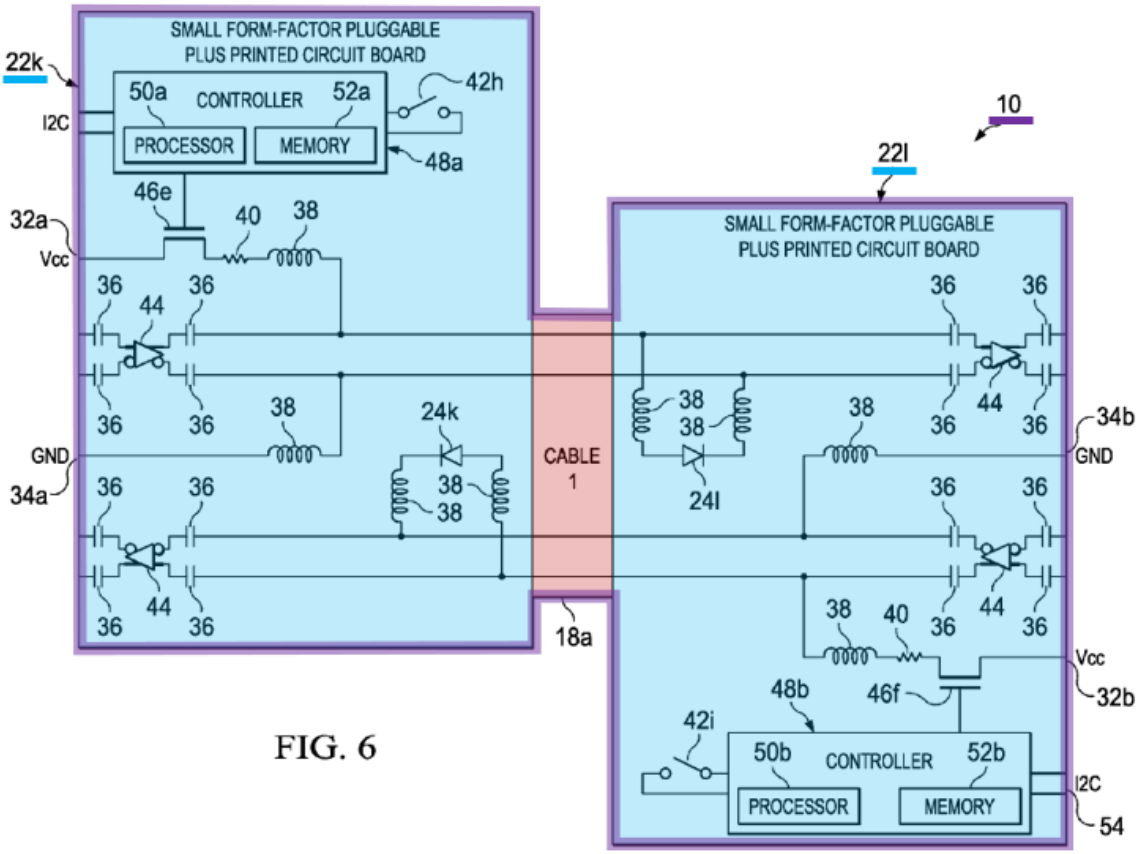


FIG. 6

ii. Limitations [6.A]-[6.K]

308. The limitations in [6.A]-[6.K] recites method steps for a communication method that mirrors limitations [1.B]-[1.E], but they are recited in a slightly different way as highlighted in the table below. For example, where claim 1 reference "corresponding" host devices and "respective" transceivers," claim 6 references "first" and "second" host devices and "first" and "second" transceivers. However, the limitations are met by Tang+TI-Retimer+Aronson in the same way in claims 1 and 6.

[1.B.i]-[1.B.ii] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,	**[6.A]** receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;
[1.C] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,	**[6.B]** performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;
	[6.C] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;
[1.B.i]-[1.B.ii] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,	**[6.D]** receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;
[1.C] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the	**[6.E]** performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;

inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,	**[6.F]** re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;
[1.D] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and	**[6.G]** performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;
	[6.H] re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;
[1.D] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and	**[6.I]** performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and
	[6.J] re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,
[1.E] the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.	**[6.K]** wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [*sic*] parameters.

309. These steps of claim limitations [6.A]-[6.K] are met by Tang+TI-Retimer+Aronson in the same way as in claim 1.

310. Tang+TI-Retimer+Aronson's cable is used in such a bi-directional communication method. *See* my discussion of claim 1 above. Simplified Tang Figure 6 is annotated below to show the two data streams (one blue and one yellow) and claim 6's steps corresponding thereto. The blue stream (left-to-right) is a *first inbound data stream from a first host device* that is received by the *first connector* ([6.A]), passed through cable conductors, and conveyed as a *second outbound data stream to the second host device* ([6.B]-[6.C], [6.G]-[6.H], [6.K]. The yellow stream (right-to-left) is a *second inbound data stream from the second host device* that is received by the *second connector* ([6.D]), passed through cable conductors, and conveyed as a *first outbound data stream to the first host device* ([6.E]-[6.F], [6.I]-[6.J]).

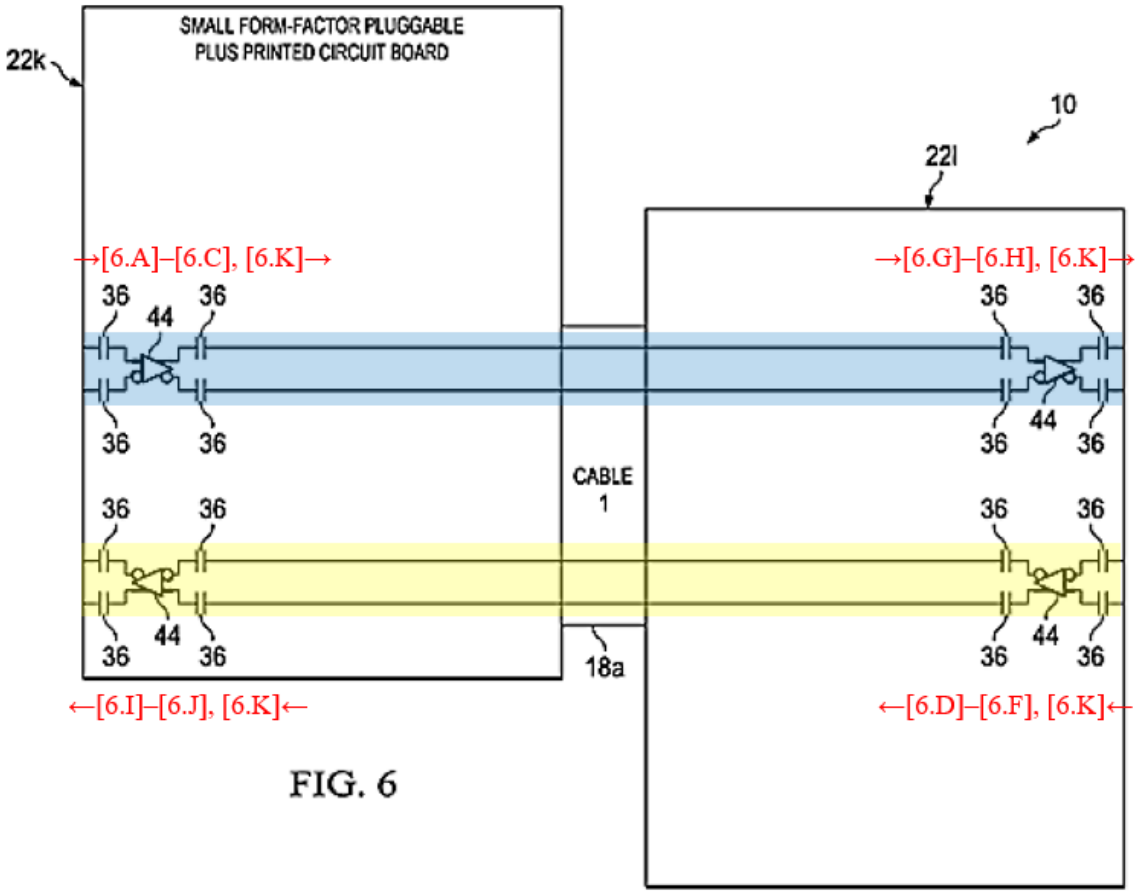


FIG. 6

311. Steps [6.A]-[6.C] recite the first connector's transceiver *performing CDR* and *re-modulating* the first inbound stream for transmission over the first conductor pair, and [6.D]-[6.F] recite the same steps performed by the second connector's transceiver on the second inbound stream for transmission over the second conductor pair. Tang+TI-Retimer+Aronson meets these steps for the reasons discussed for limitation [1.C] (Section VI.B.5.a.iv).

312. Steps [6.G]-[6.H] recite the second connector's transceiver *performing CDR* and *re-modulating* the (blue) data stream received over the first conductor pair, and [6.I]-[6.J] recite the same steps performed by the first

connector's transceiver on the (yellow) data stream received over the second conductor pair. Tang+TI-Retimer+Aronson meets these steps for the reasons discussed for limitation [1.D] (Section VI.B.5.a.v).

313. Step [6.K] requires that each of the remodulating and CDR in steps [6.B]-[6.C] and [6.E]-[6.J] employ *fixed, cable-independent equalization parameters* and is met for the reasons discussed for limitation [1.E] (Section VI.B.5.a.vi).

314. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitations [6.A]-[6.K].

f. Claim 7: The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said [performing] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.

315. I have been informed that because claim 7 contains a printing error—reciting language that was not in the claims examined at the U.S. Patent and Trademark Office—that I should read claim 7 without the erroneous language. In particular, the final phrase in claim 7, "*, each employ fixed, cable-independent, equalization parameters*," does not belong.

316. Properly construed, it is my opinion that Tang+TI-Retimer+Aronson meets claim 7 for the same reasons I discussed for claim 2.

g. Claim 8: The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.

317. It is my opinion that Tang+TI-Retimer+Aronson meets claim 8 for the same reasons I discussed for claim 3.

h. Claim 9: The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.

318. It is my opinion that Tang+TI-Retimer+Aronson meets claim 9 for the same reasons I discussed for claim 4.

i. Claim 11

i. Preamble [11.PRE]: A cable manufacturing method that comprises:

319. Tang+TI-Retimer+Aronson meets [11.PRE] because they describe a cable, as I discussed for claims 1 and 6, which is manufactured, as I will discuss below.

ii. Limitation [11.A]: connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;

320. It is my opinion that Tang+TI-Retimer+Aronson meets claim [11.A]'s conductor pairs (Tang, [0015] (twinaxial copper cables)), transceivers (Tangs SFP+ ends 22k/22l implementing TI-Retimer's retimer chip), and electrical transit signals for the same reasons I discussed for at least claims [1.PRE]-[1.C], [6.PRE], [6.C], [6.F], [6.G], and [6.I].

321. Tang+TI-Retimer+Aronson also meet limitation [11.A]'s "connecting" of conductor pairs to the first and second transceivers. Manufacturing the cable according to Tang+TI-Retimer+Aronson would have included a step of "connecting" the first and second transceivers with the ends of the conductor pairs because it is the physical connections which allow the described electrical signals to be conveyed from one end of the cable (and its transceiver(s) and/or other circuitry) to the other end of the cable (with its own transceiver(s) and/or other circuitry) or to the hosts connected at either end. Ideally, connections are strong and reliable such that transmissions are not interrupted. Prior art methods for connecting conductors (wires) to transceivers in cable assemblies were well known and obvious to POSAs included, for example, soldering transceivers and

conductors to pads. EX1010, Figs. 4A-4B, 6A-7, [0065], [0073]-[0075] (cable assembly involves connecting transceivers and cable conductors via contact/solder pads); EX1012, [0050], [0057], Figs. 1-3 and 7; EX1013, [0019]-[0021] and Fig. 3 (mounting pads for connecting electrical wires).

322. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [11.A].

iii. Limitation [11.B]: packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and

iv. Limitation [11.C]: packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,

323. It is my opinion that Tang+TI-Retimer+Aronson meets claim [11.B]'s and [11.C]'s first and second transceivers, connectors, input signals, network interface ports, host devices, and output signals—via Tang+TI-Retimer+Aronson's transceiver assemblies, transceivers, input signals, host devices, host ports, and output signals that I discussed for at least claims [1.B.i]-[1.C], [6.A], [6.D], [6.H], and [6.J].

324. Tang+TI-Retimer+Aronson also meet limitation [11.B]'s and [11.C]'s "packaging" of first and second transceivers (*i.e.*, TI-Retimer's retimer chips) into first and second connectors (*i.e.*, Tang's SFP+ ends 22k/22l). Manufacturing the cable according to Tang+TI-Retimer+Aronson would have obviously included a step of "packaging" the transceivers because Tang Fig. 6 (below) describes SFP+ ends 22k/22l as "Small Form-Factor Pluggable Plus Printed Circuit Board[s]." POSAs further understood that SFP+ "pluggable" form factors are modules that package the printed circuit board (PCB) inside. The packaging conforms to known standards, such as SFP+, QSFP, and others, which are known to use housing that contain and secure internal components. EX1027, 7-10 (SFP+ housing "contains" transceiver); EX1010, [0065] and Figs. 4A-4B (paddle card with contact pads for attaching active components, including transceivers), [0075] and Figs. 6A-7 (cable assembly including outer portions, fixed with screws, that surround a paddle card); EX1012, [0050]-[0051] (connector housing with shell and cover secured with rivets, screws, or other fasteners), Figs. 1-3. The "packaging" of electric components inside packages, housings, cases, etc., even if not standardized as described above, would have been obvious to POSAs because the act of packaging protects devices' internal components, such as transceivers, from the environment and from accidental damage or inadvertent electrical contacts.

325. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [11.C].

v. Limitation [11.D]: the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

326. It is my opinion that Tang+TI-Retimer+Aronson meets claim [11.D]'s respective transceiver functions of clock and data recovery and re-modulation of inbound data streams (as I discussed for limitations [1.C], [6.B], [6.C], [6.E], [6.F]) and transit signals (as I discussed for limitations [1.D], [6.G]-[6.J]), where fixed, cable-independent, equalization parameters are employed for clock and data recovery on electrical input signals and for generating the respective electrical output signals (as I discussed for limitations [1.E], [6.K]).

327. Thus, it is my opinion that Tang+TI-Retimer+Aronson meets Limitation [11.D].

j. Claim 12: The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.

328. It is my opinion that Tang+TI-Retimer+Aronson meets claim 12 for the same reasons I discussed for claim 2.

k. Claim 13: The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.

329. While claim 3 recites adapting parameters "during usage" and claim 13 recites adapting "during operation" of the cable, I can discern no significant difference between usage and operation in the '252 patent, and it is my opinion that Tang+TI-Retimer+Aronson meets claim 13 for the same reasons I discussed for claim 3.

l. Claim 14: The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.

330. It is my opinion that Tang+TI-Retimer+Aronson meets claim 14 for the same reasons I discussed for claim 4.

VII. DECLARATION

I declare that all statements made herein of my own knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.

Dated: April 8, 2025



Paul S. Min, Ph.D.

APPENDIX A: U.S. PATENT NO. 11,012,252 CLAIM LIST

Ref	Limitation
1.PRE	An active Ethernet cable that comprises:
1.A	electrical conductors connected between a first connector and a second connector,
1.B.i	each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device
1.B.ii	to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,
1.C	each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,
1.D	the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and
1.E	the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.
2	The active Ethernet cable of claim 1, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal.

Ref	Limitation
3	The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.
4	The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable.
5	The active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.
6.PRE	A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:
6.A	receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;
6.B	performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;
6.C	re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;
6.D	receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;
6.E	performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;
6.F	re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;

Ref	Limitation
6.G	performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;
6.H	re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;
6.I	performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and
6.J	re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,
6.K	wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [*sic*] parameters.
7	The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [*sic*] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.
8	The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.
9	The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.

Ref	Limitation
10	The communication method of claim 9, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.
11.PRE	A cable manufacturing method that comprises:
11.A	connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;
11.B	packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and
11.C	packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,
11.D.i	the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and
11.D.ii	each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

Ref	Limitation
12	The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.
13	The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.
14	The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.