

AMENDED EXHIBIT 35

Exhibit 35 – Claim Chart Showing Amphenol’s Infringement of U.S. Patent 11,012,252 (“’252 Patent”)

The following chart is based on information known to date. Credo reserves the right to amend and update this chart as additional information is obtained and analyzed. The exemplary claim mappings below rely on images and data from Amphenol and its suppliers’ public-facing materials. The following chart is representative of Amphenol’s infringement by its unlawful importation into the United States, sale for importation into the United States, and/or sale within the United States after importation of all the Amphenol Accused Products.

As outlined in the below claim chart, the Accused Amphenol Products infringe, either literally or under the doctrine of equivalents, at least Claims 1, 6, and 11 of the ’252 patent.

<u>’252 Patent</u>	<u>Accused Amphenol Products</u>
<u>Claim 1</u>	
[1pre] An active Ethernet cable that comprises:	The Accused Amphenol Products comprise an active Ethernet cable. See, e.g.:

OSFP (Octal Small Form Factor Pluggable) Copper Cable Assemblies

200G / 400G / 800G / 1.6T SOLUTIONS

Amphenol is leading the industry in OSFP cable development. Our Electronics Products 'Product of the Year' award-winning OSFP (Octal Small Form Factor Pluggable) cable assemblies are compatible with 25G/lane channel NRZ up to 224G/lane channel PAM4 signaling protocols that allow the cables to deliver aggregate bandwidths of 200G, 400G, 800G, and 1.6T per cable assembly. Available in both Passive and Active variants.

- Comprehensive system integrated interconnect design for copper or optical based cable solutions
- Addresses current and future market desired bandwidth port capability requirements
- Optimized heat dissipative and airflow features to maximize the heat dissipative properties of the system
- Data Rate: 25G NRZ / 56G PAM4 / 112G PAM4 / 224G PAM4
- Cable sizes: 25AWG – 32AWG
- 112G Passive cable lengths up to 2 meters
- 112G Active cable lengths up to 4 meters
- 224G Passive cable lengths up to 1 meter



Ex. 46, *Amphenol OSFP Copper Cable Assemblies Datasheet*.

**'252 Patent
Claim 1**

Accused Amphenol Products

☐ PART NUMBER	DESCRIPTION	PRODUCT DRAWING	3D MODEL (STP)	STATUS	DISTRIBUTOR STOCK CHECK
☐ NUJJN8-0004	 OSFP Cable Assembly, DSP Active, 32AWG, 4M, 112G / Lane, Flex Sleeve			Active	
☐ NUJJN8-0007	 OSFP Cable Assembly, DSP Active, 32AWG, 1.5M, 112G / Lane, Flex Sleeve			Active	
☐ NUJJN8-0008	 OSFP Cable Assembly, DSP Active, 32AWG, 2.5M, 112G / Lane, Flex Sleeve			Active	
☐ NUJJN8-0009	 OSFP Cable Assembly, DSP Active, 32AWG, 3.5M, 112G / Lane, Flex Sleeve			Active	
☐ NUJJN80001	 OSFP Cable Assembly, DSP Active, 32AWG, 1M, 112G / Lane, Flex Sleeve			Active	
☐ NUJJN80002	 OSFP Cable Assembly, DSP Active, 32AWG, 2M, 112G / Lane, Flex Sleeve			Active	
☐ NUJJN80003	 OSFP Cable Assembly, DSP Active, 32AWG, 3M, 112G / Lane, Flex Sleeve			Active	
☐ NUJJN80010	 OSFP Cable Assembly, DSP Active, 32AWG, 4.5M, 112G / Lane, Flex Sleeve			Active	

Ex. 47, *Amphenol OSFP Cable Assemblies Webpage* (annotated).

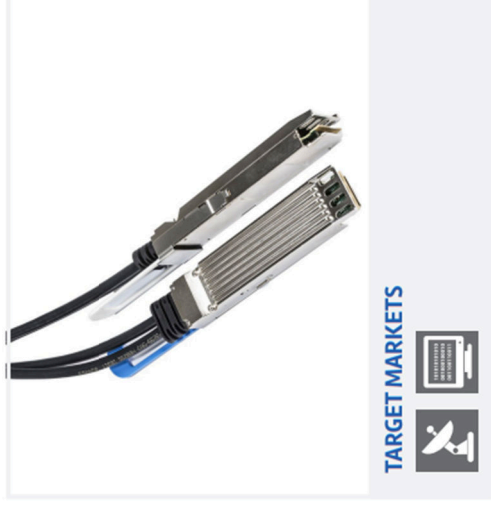
'252 Patent Claim 1	Accused Amphenol Products
	QSFP DD Cable Assemblies 200G / 400G / 800G SOLUTIONS Amphenol's QSFP DD (Double Density) copper cable assemblies double the number of channels from 4 to 8 lanes when compared to the existing QSFP cabling systems, enabling more bandwidth within the same mechanical envelope. Compatible with 25G/Lane NRZ up to 112G/Lane PAM4 signaling protocols that allow cables to deliver aggregate bandwidths of 200G, 400G, and 800G per cable assembly. Available in both Passive and Active variants. ■ Addresses current and future market desired bandwidth port capability requirements ■ Backwards mate compatible with QSFP receptacles ■ Data Rate: 25G NRZ / 56G PAM4 / 112G PAM4 ■ Cable sizes: 25AWG – 32AWG ■ 112G Passive cable lengths up to 2 meters ■ 112G Active cable lengths up to 4 meters ■ Ultra–low–power Active Electrical Cable featuring Smart CDR SoC up to 3 meters at only 4.5W per side  TARGET MARKETS  Ex. 79, <i>Amphenol QSFP DD Cable Assemblies Datasheet</i>.
[1a] electrical conductors connected between a first connector and a second connector,	The Accused Amphenol Products comprise electrical conductors connected between a first connector and a second connector. For example, the Accused Amphenol Products have first and second connectors at the end of the cables (e.g., the QSFP plugs shown below). See, e.g.:

OSFP (Octal Small Form Factor Pluggable) Copper Cable Assemblies

200G / 400G / 800G / 1.6T SOLUTIONS

Amphenol is leading the industry in OSFP cable development. Our Electronics Products 'Product of the Year' award-winning OSFP (Octal Small Form Factor Pluggable) cable assemblies are compatible with 25G/lane channel NRZ up to 224G/lane channel PAM4 signaling protocols that allow the cables to deliver aggregate bandwidths of 200G, 400G, 800G, and 1.6T per cable assembly. Available in both Passive and Active variants.

- Comprehensive system integrated interconnect design for copper or optical based cable solutions
- Addresses current and future market desired bandwidth port capability requirements
- Optimized heat dissipative and airflow features to maximize the heat dissipative properties of the system
- Data Rate: 25G NRZ / 56G PAM4 / 112G PAM4 / 224G PAM4
- Cable sizes: 25AWG – 32AWG
- 112G Passive cable lengths up to 2 meters
- 112G Active cable lengths up to 4 meters
- 224G Passive cable lengths up to 1 meter



Ex. 46, *Amphenol OSFP Copper Cable Assemblies Datasheet*.

QSFP DD Cable Assemblies

200G / 400G / 800G SOLUTIONS

Amphenol's QSFP DD (Double Density) copper cable assemblies double the number of channels from 4 to 8 lanes when compared to the existing QSFP cabling systems, enabling more bandwidth within the same mechanical envelope. Compatible with 25G/Lane NRZ up to 112G/Lane PAM4 signaling protocols that allow cables to deliver aggregate bandwidths of 200G, 400G, and 800G per cable assembly. Available in both Passive and Active variants.

- Addresses current and future market desired bandwidth port capability requirements
- Backwards mate compatible with QSFP receptacles
- Data Rate: 25G NRZ / 56G PAM4 / 112G PAM4
- Cable sizes: 25AWG – 32AWG
- 112G Passive cable lengths up to 2 meters
- 112G Active cable lengths up to 4 meters
- Ultra-low-power Active Electrical Cable featuring Smart CDR SoC up to 3 meters at only 4.5W per side

Ex. 79, *Amphenol QSFP DD Cable Assemblies Datasheet*.

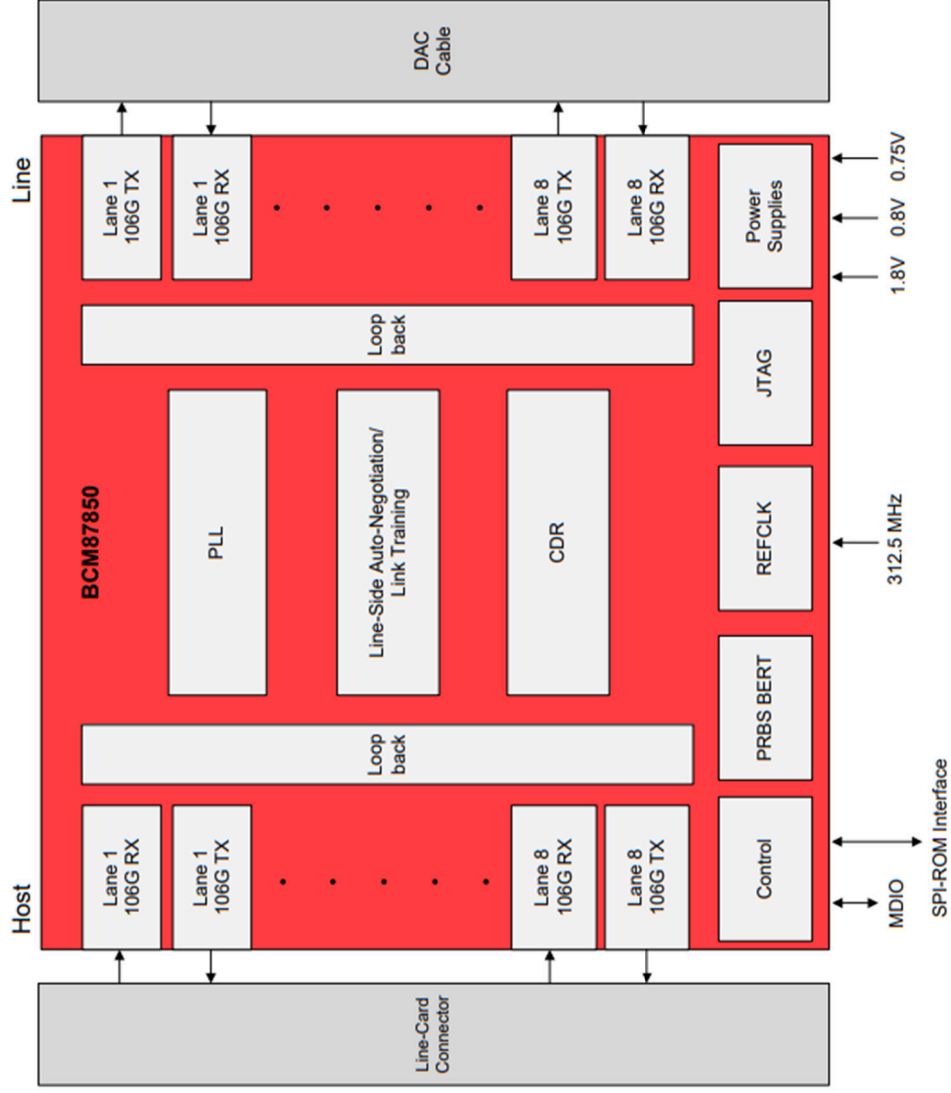


The electrical conductors are twin-axial, 8-pair or 16-pair wire.

- **Assembled with industry leading twin-axial SKEWCLEAR® 8-pair or 16-pair wire**

Ex. 46, *Amphenol OSFP Copper Cable Assemblies Datasheet*.

'252 Patent Claim 1	Accused Amphenol Products
	▪ Assembled with industry leading twin-axial SKEWCLEAR® 8-pair or 16-pair wire <i>Ex. 79, Amphenol QSFP DD Cable Assemblies Datasheet.</i>
[1b] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable. For example, the connectors in the Accused Amphenol Products include DSPs manufactured by Broadcom and others. These DSPs are retimers that receive inbound Ethernet data streams from a host and convey them to the cable and conversely receive outbound Ethernet data streams from the cable and provide them to the host. - Amphenol will highlight OAI expansion version 1.0, featuring Broadcom's 1.6T (2x800G), 5nm retimer PHY, ExaMAX2® 112G backplane connector, OSFP 112 I/O connector and Mini Cool Edge, Expo Hall, Booth A8. <i>Ex. 48, Broadcom 2022 OCP Global Summit Press Release</i> Key components used for validation include (1) Broadcom's BCM85361 1.6Tbps retimer/crossbar and Amphenol's ExaMAX2 112Gb/s high-speed backplane connector system. - Broadcom's BCM85361 is a 16 lane, 112G SerDes retimer with support for long-reach backplanes with ~45dB of insertion loss and passive DAC cables up to 3 meters. The retimer supports Ethernet rates up to 2 x 800 GbE for scale-out and can also be configured as a flexible crossbar for scale-up requirements. BCM85361 is designed in the advanced 5nm process node, delivering low power to meet the challenges of increasing energy consumption in data centers. - Amphenol's ExaMAX2 connector system delivers industry leading SI performance needed to support OAI applications. The Vertical Header (VH) P/N: 10167063c and Right-Angle Receptacle (RAR) P/N: 10167059c are configured as 4x16 and provide the connectivity to support both scale-out and switch implementations of the Expansion Card. The innovative beam-on-beam mating interface of the ExaMAX2 solution demonstrates a resonance-free Insertion Loss profile thru 60GHz and superb Return Loss performance. <i>Ex. 49, Broadcom B-Connected Blog Post.</i>	



Ex. 50, Broadcom BCM87850 Product Brief.

'252 Patent Claim 1	Accused Amphenol Products
	Overview The Broadcom® BCM87850 is a single-chip, eight-lane, ultra-low power, ultra-low latency PHY that integrates retimer and equalizer to support active cable applications. The BCM87850 is capable of equalizing 22 dB of loss on both the client-side and line-side interfaces. Each lane is capable of multiple data rates, including 106.25 Gb/s. The on-chip clock synthesis is performed by a low-cost 312.5-MHz reference clock through high-frequency, low jitter phase-locked loops (PLLs). The BCM87850 is fabricated in low-power 7-nm CMOS technology and is available in a 12 mm x 12 mm, 0.5-mm pitch, 485-ball BGA, RoHS-compliant package. Ex. 50, <i>Broadcom BCM87850 Product Brief</i> (annotated).
[1c] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,	Each of the first and second connectors in the Accused Amphenol Products includes a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. For example, the Accused Amphenol Products include a transceiver in the DSP chip on each end of the cable. The transceiver in each DSP performs clock and data recovery via “retiming” on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. See, e.g.:

'252 Patent Claim 1	Accused Amphenol Products
	Overview The Broadcom® BCM87850 is a single-chip, eight-lane, ultra-low power, ultra-low latency PHY that integrates retimer and equalizer to support active cable applications. The BCM87850 is capable of equalizing 22 dB of loss on both the client-side and line-side interfaces. Each lane is capable of multiple data rates, including 106.25 Gb/s. The on-chip clock synthesis is performed by a low-cost 312.5-MHz reference clock through high-frequency, low jitter phase-locked loops (PLLs). The BCM87850 is fabricated in low-power 7-nm CMOS technology and is available in a 12 mm x 12 mm, 0.5-mm pitch, 485-ball BGA, RoHS-compliant package. Ex. 50, <i>Broadcom BCM87850 Product Brief</i> (annotated).
[1d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and remodulate the transit data stream as the outbound data stream from the cable, and	The respective transceiver for each of the first and second connectors in the Accused Amphenol Products performs clock and data recovery on the respective electrical transit signal to extract and remodulate the transit data stream as the outbound data stream from the cable. For example, the transceiver in each DSP performs clock and data recovery via “retiming” on the electrical input signal to extract and re-modulate the transit data stream as the outbound data stream from the cable. See, e.g.:

'252 Patent Claim 1	Accused Amphenol Products
	Overview The Broadcom® BCM87850 is a single-chip, eight-lane, ultra-low power, ultra-low latency PHY that integrates retimer and equalizer to support active cable applications. The BCM87850 is capable of equalizing 22 dB of loss on both the client-side and line-side interfaces. Each lane is capable of multiple data rates, including 106.25 Gb/s. The on-chip clock synthesis is performed by a low-cost 312.5-MHz reference clock through high-frequency, low jitter phase-locked loops (PLLs). The BCM87850 is fabricated in low-power 7-nm CMOS technology and is available in a 12 mm x 12 mm, 0.5-mm pitch, 485-ball BGA, RoHS-compliant package. Ex. 50, <i>Broadcom BCM87850 Product Brief</i> (emphasis added).
[1e] the respective transceivers each employing fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.	The respective transceivers in the Accused Amphenol Products employ fixed, cable-independent equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal. For example, the DSPs at each end of the cable employ fixed, cable-independent equalization parameters for the remodulation of the transit data stream as the outbound stream and the clock and data recovery performed on the input signal. These parameters (i.e., transmit and receive filter coefficient values) are fixed and cable-independent per the IEEE 802.3ck standard (which are independent of communications through the cable). See, e.g.:

'252 Patent Claim 1	Accused Amphenol Products
	120G.3.4 Module input characteristics The module input shall meet the specifications given in Table 120G-9. Channel equalization is provided by an adaptive equalizer in the module Ex. 52, <i>IEEE 802.3ck Specification</i> at 7283 (annotated). The Accused Amphenol Products comply with the OSFP standard.¹ Amphenol is leading the industry in OSFP cable development. Our Electronics Products 'Product of the Year' award-winning OSFP (Octal Small Form Factor Pluggable) cable assemblies are compatible with 25G/lane channel NRZ up to 224G/lane channel PAM4 signaling protocols that allow the cables to deliver aggregate bandwidths of 200G, 400G, 800G, and 1.6T per cable assembly. Available in both Passive and Active variants. Ex. 46, <i>Amphenol OSFP Copper Cable Assemblies Datasheet</i>. As explained in the OSFP specification, the high-speed signals of the Accused Amphenol Products meet the requirements of the IEEE 802.3ck standard. The high-speed signals follow the electrical specifications of IEEE802.3bs, IEEE802.3cd, IEEE 802.3ck and CEI-56G-VSR-PAM4 as defined in OIF-CEI-05.2 for 400GAUI-8 mode and IEEE802.3bj, IEEE802.3bm for CAUI-4 mode.

¹ The Accused Amphenol Products that use a QSFP form factor likewise comply with the IEEE 802.3ck standard and the Common Management Interface Specification (CMIS) standard. See Ex. 79, Amphenol QSFP DD Cable Assemblies Datasheet at 2 (noting compliance with IEEE 802.3ck); Ex. 77, QSFP-DD Specification at 34; Ex. 78, *QSFP112 Specification* at 10.

'252 Patent Claim 1	Accused Amphenol Products
	Ex. 54, <i>OSFP Specification</i> at 147. The 802.3ck standard defines the chip-to-module connection, including requiring that the transmitters use a pre-equalized set of filters as part of selecting a short or long channel. 120G.3.2.1 Module output modes The module output shall support two modes: short and long. The means of controlling the module output mode is implementation dependent. For each output mode, the module shall meet the requirements for eye height (min) and VEC (max) in Table 120G-3 for both near-end and far-end measurements (see 120G.3.2.2.1). Ex. 52, <i>IEEE 802.3ck Specification</i> at 7275 (annotated). The OSFP standard also requires compliance of the control plane to the CMIS standard. The OSFP specification defines: • The OSFP module mechanical form factor, including the latching mechanism; • The host cage together with the mating connector; • The electrical interface, including pin-out, data, control, and power and ground signals; • The mechanical interface, including the package outline, front panel, and printed circuit board (PCB) layout requirements; • Thermal requirements and limitations, including heat sink design and airflow; • Electrostatic discharge (ESD) requirements; • The module management interface as contained in the Common Management Interface Specification (CMIS). Ex. 54, <i>OSFP Specification</i> at 15 (annotated). The CMIS standard controls the equalization of the port transceiver, including employing fixed, cable-independent equalization parameters for each of: the remodulation of the transit

'252 Patent	Accused Amphenol Products											
Claim 1	data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal. 6.2.5.1 Tx Input Equalization Control The controls for Tx input equalization can be grouped by equalization type, as shown in Table 6-5. Table 6-5 Tx Input Eq control relationship to AdaptiveInputEqEnableTx <table><tr><th>Equalization Type</th><th>Control</th><th>AdaptiveInputEqEnableTx</th></tr><tr><td rowspan="3">Adaptive</td><td>AdaptiveInputEqFreezeTx</td><td rowspan="3">1</td></tr><tr><td>AdaptiveInputEqStoreTx</td></tr><tr><td>AdaptiveInputEqRecallTx</td></tr><tr><td>Non-Adaptive</td><td>FixedInputEqTargetTx</td><td>0</td></tr></table> The controls relevant for adaptive Tx input equalization are described in section 6.2.5.4. The controls relevant for non-adaptive Tx input equalization, when Tx input equalization settings are pre-determined or host provisioned, are described below. The module ignores control field values that are not relevant for the current AdaptiveInputEqEnableTx setting.	Equalization Type	Control	AdaptiveInputEqEnableTx	Adaptive	AdaptiveInputEqFreezeTx	1	AdaptiveInputEqStoreTx	AdaptiveInputEqRecallTx	Non-Adaptive	FixedInputEqTargetTx	0
Equalization Type	Control	AdaptiveInputEqEnableTx										
Adaptive	AdaptiveInputEqFreezeTx	1										
	AdaptiveInputEqStoreTx											
	AdaptiveInputEqRecallTx											
Non-Adaptive	FixedInputEqTargetTx	0										

'252 Patent	Accused Amphenol Products																														
Claim 1	Host Controlled Equalization Tx input equalization values in dB are based on a reference CTLE and may not directly apply to the equalizer implemented in the module. SCS<k>::FixedInputEqTargetTx<i> is a four-bit control field for lane <i> and encoded as shown in Table 6-6. This field allows the host to specify a fixed (non-adaptive) Tx input equalization target and is ignored by the module if AdaptiveInputEqEnableTx<i> is set for that lane. The module advertises support of non-adaptive Tx input equalization control as described in Table 8-48. The module advertises the maximum supported Tx input equalization values as described in Table 8-44. Table 6-6 Fixed Tx Input Equalization Codes <table><tr><th>Code Value</th><th>Bit pattern</th><th>Input Equalization</th></tr><tr><td>0</td><td>0000b</td><td>No Equalization</td></tr><tr><td>1</td><td>0001b</td><td>1 dB</td></tr><tr><td>2</td><td>0010b</td><td>2 dB</td></tr><tr><td>3 - 8</td><td>0011b ... 1000b</td><td>3 dB ... 8 dB</td></tr><tr><td>9</td><td>1001b</td><td>9 dB</td></tr><tr><td>10</td><td>1010b</td><td>10 dB</td></tr><tr><td>11</td><td>1011b</td><td>11 dB</td></tr><tr><td>12</td><td>1100b</td><td>12 dB</td></tr><tr><td>13-15</td><td></td><td>Custom</td></tr></table>	Code Value	Bit pattern	Input Equalization	0	0000b	No Equalization	1	0001b	1 dB	2	0010b	2 dB	3 - 8	0011b ... 1000b	3 dB ... 8 dB	9	1001b	9 dB	10	1010b	10 dB	11	1011b	11 dB	12	1100b	12 dB	13-15		Custom
Code Value	Bit pattern	Input Equalization																													
0	0000b	No Equalization																													
1	0001b	1 dB																													
2	0010b	2 dB																													
3 - 8	0011b ... 1000b	3 dB ... 8 dB																													
9	1001b	9 dB																													
10	1010b	10 dB																													
11	1011b	11 dB																													
12	1100b	12 dB																													
13-15		Custom																													

6.2.5.2 Rx Output Equalization Control

Rx output equalization is defined at an appropriate test point defined by the relevant standard.

SCS<k>::**OutputEqPreCursorTargetRx**<i> and SCS<k>::**OutputEqPostCursorTargetRx**<i> are four-bit control fields for lane <i> and encoded as shown in Table 6-7.

The module advertises support of Rx output equalization control as described in Table 8-48.

The module advertises the maximum supported Rx output equalization values as described in Table 8-44.

Modules that require only output emphasis utilize the SCS<k>::**OutputEqPostCursorTargetRx**<i> fields and set the SCS<k>::**OutputEqPreCursorTargetRx**<i> fields to zero.

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	Reserved	Reserved
11-15	1011b-1111b	Custom	Custom

Note: The pre-cursor equalizer settings in dB approximates to
Pre EQ (dB) = $-20 \cdot \log_{10}(1 - C_{-1} / (C_{-1} + C_0 + C_1))$ (Eq. 6-1)
The post-cursor equalizer settings in dB approximates to
Post EQ (dB) = $-20 \cdot \log_{10}(1 - C_1 / (C_1 + C_0 + C_1))$ (Eq. 6-2)
Equalizer coefficients C_n are pre-cursor for $n < 0$ and post-cursor when $n > 0$.

Ex. 55, CMIS Specification at 60–61.

The datasheets for the exemplary Accused Amphenol Products notes that they support the 802.3ck standard:

See, e.g.:

'252 Patent	Accused Amphenol Products
Claim 1	SPECIFICATIONS ▪ Refer to the latest revision specification of the OSFP octal small form factor pluggable module ▪ Applicable IEEE specifications ▪ IEEE802.3by ▪ IEEE802.3bj ▪ IEEE802.3cd ▪ IEEE802.3ck ▪ The InfiniBand™ architecture specification and annexes Ex. 46, <i>Amphenol OSFP Copper Cable Assemblies Datasheet</i>.

'252 Patent	Accused Amphenol Products
Claim 1	
	SPECIFICATIONS ▪ Refer to the latest revision of the QSFP-DD hardware specification for QSFP double density 8X pluggable transceiver ▪ Applicable IEEE specifications ▪ IEEE802.3by ▪ IEEE802.3bj ▪ IEEE802.3cd ▪ IEEE802.3ck ▪ The InfiniBand™ architecture specification and annexes Ex. 79, <i>Amphenol QSFP DD Cable Assemblies Datasheet</i>.

'252 Patent	Accused Amphenol Products
Claim 6	
[6pre] A communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector	Amphenol performs a communication method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector. <i>See [1pre] above.</i>
[6a] receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;	The Accused Amphenol Products receive with the first connector a first electrical input signal conveying a first inbound data stream from a first host device <i>See [1b] above.</i>

'252 Patent	Accused Amphenol Products
Claim 6	
[6b] performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;	The Accused Amphenol Products perform clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream. <i>See</i> [1c], [1d] above.
[6c] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;	The Accused Amphenol Products re-modulate the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs <i>See</i> [1c], [1d] above.
[6d] receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;	The Accused Amphenol Products receive with the second connector a second electrical input signal conveying a second inbound data stream from a second host device <i>See</i> [1b] above.
[6e] performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;	The Accused Amphenol Products perform clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream. <i>See</i> [1c], [1d] above.
[6f] re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;	The Accused Amphenol Products re-modulate the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs <i>See</i> [1c], [1d] above.
[6g] performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;	The Accused Amphenol Products perform clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream. <i>See</i> [1c], [1d] above.

'252 Patent	Accused Amphenol Products
Claim 6	
[6h] re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;	The Accused Amphenol Products re-modulate the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device. <i>See [1c], [1d] above.</i>
[6i] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and	The Accused Amphenol Products perform clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream. <i>See [1c], [1d] above.</i>
[6j] re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,	The Accused Amphenol Products re-modulate the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device <i>See [1c], [1d] above.</i>
[6k] wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.	The Accused Amphenol Products perform wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters. <i>See [1e] above.</i>

'252 Patent	Accused Amphenol Products
Claim 11	
[11pre] A cable manufacturing method that comprises:	The Accused Amphenol Products are produced using a cable manufacturing method. <i>See [1pre] above.</i>
[11a] connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;	The Accused Amphenol Products are produced using a cable manufacturing method, including connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver. <i>See [1a], [1b] above.</i>
[11b] packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and	The Accused Amphenol Products are produced using a cable manufacturing method, including packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device. <i>See [1b] above.</i>
[11c] packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the	The Accused Amphenol Products are produced using a cable manufacturing method, including packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device. <i>See [1b] above.</i>

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Claim 11 network interface port of the second host device,	
[11d] the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.	The Accused Amphenol Products are produced using a cable manufacturing method, wherein the first and second transceivers of the Accused Amphenol Products are configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals <i>See</i> [1c], [1d], [1e] above.