IEEE Standard for Ethernet

SECTION TWO

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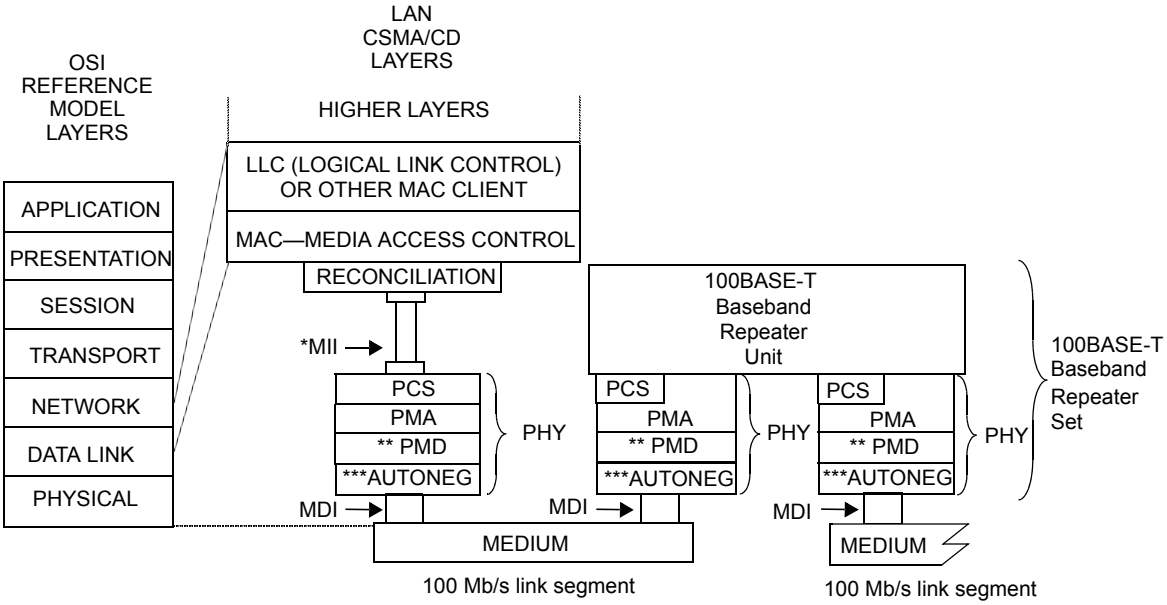
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21. Introduction to 100 Mb/s baseband networks, type 100BASE-T

21.1 Overview

100BASE-T couples the IEEE 802.3 CSMA/CD MAC with a family of 100 Mb/s Physical Layers. While the MAC can be readily scaled to higher performance levels, new Physical Layer standards are required for 100 Mb/s operation.

The relationships between 100BASE-T, the existing IEEE 802.3 (CSMA/CD MAC), and the ISO/IEC Open System Interconnection (OSI) reference model is shown in Figure 21–1.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
Use of MII between PCS and Baseband Repeater Unit is optional.
*** AUTONEG is optional.

Figure 21–1—Architectural positioning of 100BASE-T

100BASE-T uses the existing IEEE 802.3 MAC layer interface, connected through a Media-Independent Interface layer to a Physical Layer entity (PHY) sublayer such as 100BASE-T4, 100BASE-TX, or 100BASE-FX.

100BASE-T extends the IEEE 802.3 MAC to 100 Mb/s. The bit rate is faster, bit times are shorter, packet transmission times are reduced, and cable delay budgets are smaller—all in proportion to the change in bandwidth. This means that the ratio of packet duration to network propagation delay for 100BASE-T is the same as for 10BASE-T.

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21.1.1 Reconciliation Sublayer (RS) and Media Independent Interface (MII)

The Media Independent Interface (Clause 22) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer entities (PHY) and between PHY Layer and Station Management (STA) entities. This MII is capable of supporting both 10 Mb/s and 100 Mb/s data rates through four bit wide (nibble wide) transmit and receive paths. The Reconciliation sublayer provides a mapping between the signals provided at the MII and the MAC/PLS service definition.

21.1.2 Physical Layer signaling systems

The following portion of this standard specifies a family of Physical Layer implementations. Typically 100BASE-TX (Clauses 24 and 25) uses two pairs of Category 5 balanced cabling as defined by ISO/IEC 11801, 100BASE-FX (Clauses 24 and 26) uses two multimode fibers. There are a number of other PHY types and their associated media.

21.1.3 Repeater

Repeater sets (Clause 27) are an integral part of any 100BASE-T network with more than two DTEs in a collision domain. They extend the physical system topology by coupling two or more segments. Multiple repeaters are permitted within a single collision domain to provide the maximum path length.

21.1.4 Auto-Negotiation

Auto-Negotiation (Clause 28) provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10BASE-T link integrity test sequence.

21.1.5 Management

Managed objects, attributes, and actions are defined for all 100BASE-T components (Clause 30).

21.2 References

See 1.3.

21.3 Definitions

See 1.4.

21.4 Abbreviations

See 1.5.

21.5 State diagrams

State diagrams take precedence over text.

The conventions of 1.2 are adopted, with the following extensions.

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21.5.1 Actions inside state blocks

The actions inside a state block execute instantaneously. Actions inside state blocks are atomic (i.e., uninterruptible).

After performing all the actions listed in a state block one time, the state block then continuously evaluates its exit conditions until one is satisfied, at which point control passes through a transition arrow to the next block. While the state awaits fulfillment of one of its exit conditions, the actions inside do not implicitly repeat.

The characters • and [bracket] are *not* used to denote any special meaning.

Valid state actions may include .indication and .request messages.

No actions are taken outside of any state block.

21.5.2 State diagram variables

Once set, variables retain their values as long as succeeding blocks contain no references to them.

Setting the parameter of a formal interface message assures that, on the next transmission of that message, the last parameter value set will be transmitted.

Testing the parameter of a formal interface messages tests the value of that message parameter that was received on the last transmission of said message. Message parameters may be assigned default values that persist until the first reception of the relevant message.

21.5.3 State transitions

The following terms are valid transition qualifiers:

a) Boolean expressions
b) An event such as the expiration of a timer: timer_done
c) An event such as the reception of a message: PMA_UNITDATA.indication
d) An unconditional transition: UCT
e) A branch taken when other exit conditions are not satisfied: ELSE

Any open arrow (an arrow with no source block) represents a global transition. Global transitions are evaluated continuously whenever any state is evaluating its exit conditions. When a global transition becomes true, it supersedes all other transitions, including UCT, returning control to the block pointed to by the open arrow.

21.5.4 Operators

The state diagram operators are shown in Table 21–1.

Table 21–1—State diagram operators

Character	Meaning
*	Boolean AND
+	Boolean OR
^	Boolean XOR
!	Boolean NOT

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Table 21–1—State diagram operators *(continued)*

Character	Meaning
<	Less than
≤	Less than or equal to
=	Equals (a test of equality)
≠	Not equals
≥	Greater than or equal to
>	Greater than
( )	Indicates precedence
⇐	Assignment operator
∈	Indicates membership
∉	Indicates nonmembership
|	Catenate
ELSE	No other state condition is satisfied

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21.6 Protocol implementation conformance statement (PICS) proforma

21.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to any 100 Mb/s portion of this standard shall complete a protocol implementation conformance statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. The PICS can be used for a variety of purposes by various parties, including the following:

a) As a checklist by the protocol implementer, to reduce the risk of failure to conform to the standard through oversight;
b) As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;
c) As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICS);
d) As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

21.6.2 Abbreviations and special symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
!	negation
O	optional field/function
O.<n>	optional field/function, but at least one of the group of options labeled by the same numeral <n> is required
O/<n>	optional field/function, but one and only one of the group of options labeled by the same numeral <n> is required
X	prohibited field/function
<item>:	simple-predicate condition, dependent on the support marked for <item>
<item1>*<item2>:	AND-predicate condition, the requirement must be met if both optional items are implemented

21.6.3 Instructions for completing the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the sixth column contains values and/or comments pertaining to the question

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to be answered. The remaining columns record the status of the items—whether the support is mandatory, optional or conditional—and provide the space for the answers.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the protocol implementation conformance statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

21.6.4 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features that, although optional, are nonetheless commonly present in implementations.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

21.6.5 Exceptional information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

21.6.6 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M (Mandatory), O (Optional), or X (Not Applicable).

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If the item referred to by the conditional symbol is marked as supported, then 1) the conditional item is applicable, 2) its status is given by "<s>", and 3) the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

21.7 MAC delay constraints (exposed MII)

100BASE-T makes the following assumptions about MAC performance. These assumptions apply to any MAC operating in half duplex mode with an exposed MII.

Table 21–2—MAC delay assumptions (exposed MII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MII	MAC transmit start to TX_EN sampled		4		TX_CLK rising
	CRS assert to MAC detect	0	8		
	CRS deassert to MAC detect	0	8		
	CRS assert to TX_EN sampled (worst case nondeferred transmit)		16		TX_CLK rising
	COL assert to MAC detect	0	8		
	COL deassert to MAC detect	0	8		
	COL assert to TXD = Jam sampled (worst-case collision response)		16		TX_CLK rising; first nibble of jam

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22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

This clause defines the logical, electrical, and mechanical characteristics for the Reconciliation Sublayer (RS) and Media Independent Interface (MII) between CSMA/CD media access controllers and various PHYs. Figure 22–1 shows the relationship of the Reconciliation sublayer and MII to the ISO/IEC OSI reference model.

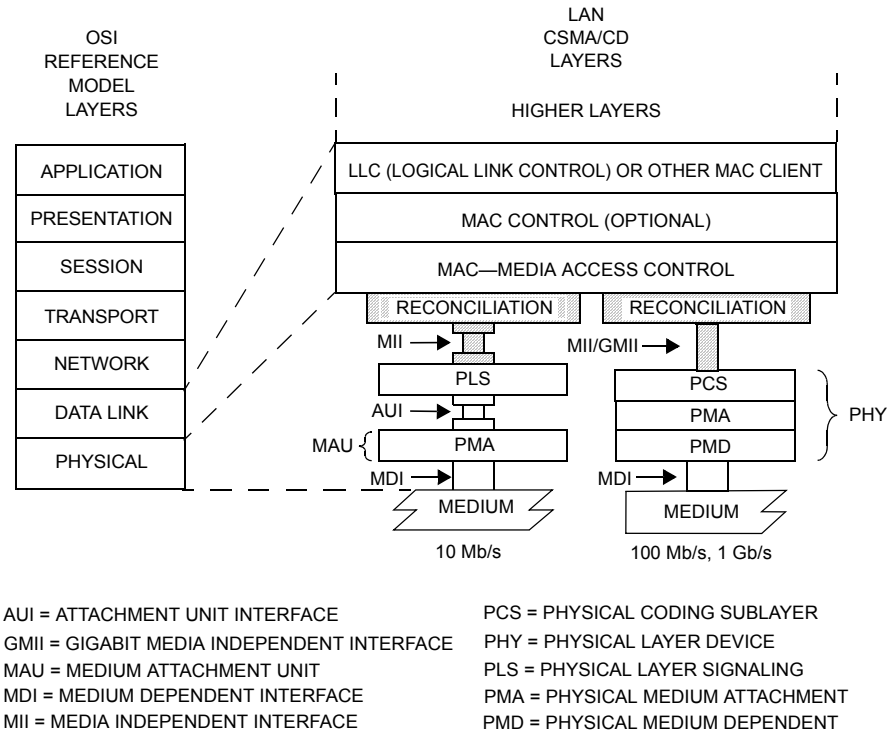


Figure 22–1—MII relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayers and PHYs for data transfer at 10 Mb/s and 100 Mb/s, and between Station Management (STA) and PHYs.

This interface has the following characteristics:

a) It is capable of supporting 10 Mb/s and 100 Mb/s rates for data transfer, and management functions.
b) Data and delimiters are synchronous to clock references.
c) It provides independent four bit wide transmit and receive data paths.
d) It uses TTL signal levels, compatible with common digital CMOS ASIC processes.
e) It provides a simple management interface.
f) It is capable of driving a limited length of shielded cable.
g) It provides full duplex operation.

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22.1.1 Summary of major concepts

a) Each direction of data transfer is serviced with seven (making a total of 14) signals: Data (a four-bit bundle), Delimiter, Error, and Clock.
b) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.
c) A management interface comprised of two signals provides access to management parameters and services.
d) The Reconciliation sublayer maps the signal set provided at the MII to the PLS service definition specified in Clause 6.

22.1.2 Application

This clause applies to the interface between MAC sublayer and PHYs, and between PHYs and Station Management entities. The implementation of the interface may assume any of the following three forms:

a) A chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board.
b) A motherboard to daughterboard interface between two or more printed circuit boards.
c) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector.

Figure 22–2 provides an example of the third application environment listed above. All MII conformance tests are performed at the mating surfaces of the MII connector, identified by the line A-A.

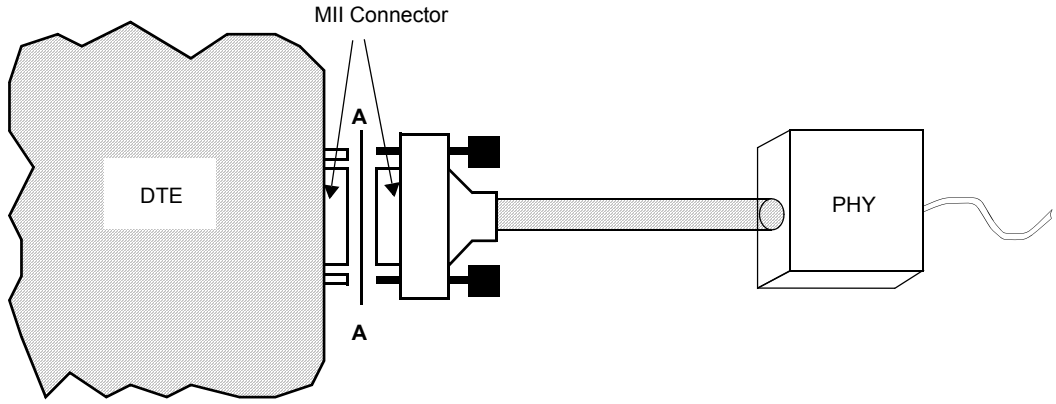


Figure 22–2—Example application showing location of conformance test

This interface is used to provide media independence for various forms of unshielded twisted-pair wiring, shielded twisted-pair wiring, fiber optic cabling, and potentially other media, so that identical media access controllers may be used with any of these media.

To allow for the possibility that multiple PHYs may be controlled by a single station management entity, the MII management interface has provisions to accommodate up to 32 PHYs, with the restriction that a maximum of one PHY may be attached to a management interface via the mechanical interface defined in 22.6.

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22.1.3 Rates of operation

The MII can support two specific data rates, 10 Mb/s and 100 Mb/s. The functionality is identical at both data rates, as are the signal timing relationships. The only difference between 10 Mb/s and 100 Mb/s operation is the nominal clock frequency.

PHYs that provide an MII are not required to support both data rates, and may support either one or both. PHYs must report the rates they are capable of operating at via the management interface, as described in 22.2.4.

22.1.4 Allocation of functions

The allocation of functions at the MII is such that it readily lends itself to implementation in both PHYs and MAC sublayer entities. The division of functions balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Media Attachment (PMA) sublayers for 10 Mb/s DTEs, the MII maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling of the PLS or PCS sublayer and the PMA sublayer.

22.1.5 Relationship of MII and GMII

The Gigabit Media Independent Interface (GMII) is similar to the MII. The GMII uses the MII Management Interface and register set specified in 22.2.4. These common elements of operation allow Station Management to determine PHY capabilities and configure the station based on those capabilities. In a station supporting both MII and GMII operation, configuration of the station would include enabling either the MII or GMII operation as appropriate for the data rate of the selected PHY.

Most of the MII and GMII signals use the same names, but the width of the RXD and TXD data bundles and the semantics of the associated control signals differ between MII and GMII operation. The GMII transmit path clocking also differs significantly from MII clocking. MII operation of these signals and clocks is specified within Clause 22 and GMII operation is specified within Clause 35.

22.2 Functional specifications

The MII is designed to make the differences among the various media absolutely transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end. Additionally, the MII is designed to be easily implemented at minimal cost using conventional design techniques and manufacturing processes.

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in Clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in Clause 6. The MII signals are defined in detail in 22.2.2.The mapping is changed if EEE capability is supported (see 78.3), as described in 22.7. EEE capability requires the use of the MAC defined in Annex 4A for simplified full duplex operation (with carrier sense deferral). This provides full duplex operation but uses the carrier sense signal to defer transmission when the PHY is in its low power state.

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Figure 22–3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the station management entity (STA).

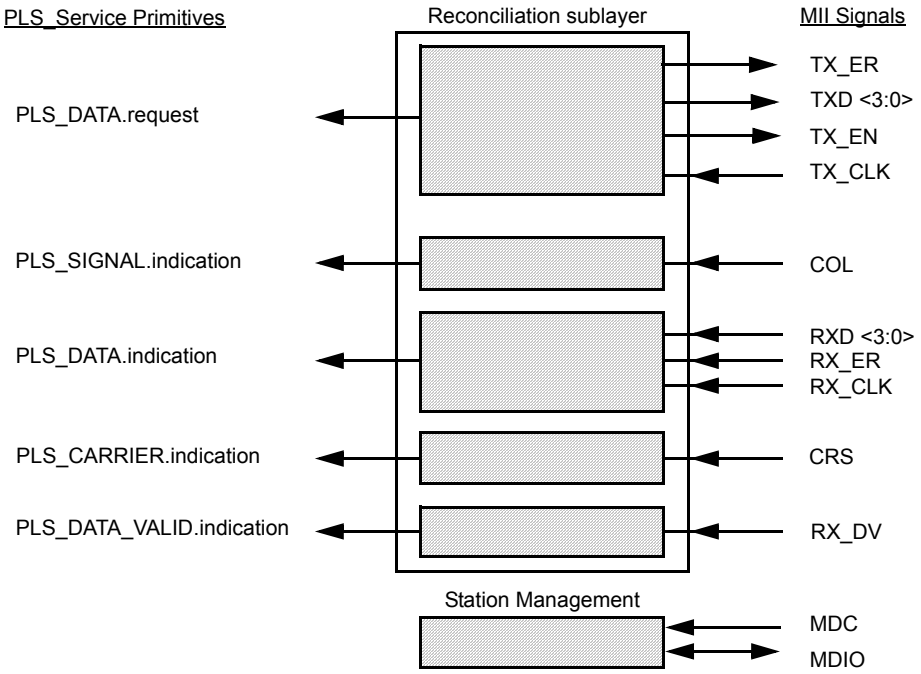


Figure 22–3—Reconciliation Sublayer (RS) inputs and outputs, and STA connections to MII

22.2.1.1 Mapping of PLS_DATA.request

22.2.1.1.1 Function

Map the primitive PLS_DATA.request to the MII signals TXD<3:0>, TX_EN, and TX_CLK.

22.2.1.1.2 Semantics of the service primitive

PLS_DATA.request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the signals TXD<3>, TXD<2>, TXD<1> and TXD<0>, each of which conveys one bit of data while TX_EN is asserted. The value DATA_COMPLETE is conveyed by the deassertion of TX_EN. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the TX_CLK signal.

22.2.1.1.3 When generated

The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the Reconciliation sublayer after every group of four PLS_DATA.request transactions from the MAC sublayer to request the transmission of four data bits on the physical medium or to stop transmission.

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22.2.1.2 Mapping of PLS_DATA.indication

22.2.1.2.1 Function

Map the primitive PLS_DATA.indication to the MII signals RXD<3:0>, RX_DV, RX_ER, and RX_CLK.

22.2.1.2.2 Semantics of the service primitive

PLS_DATA.indication (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit. The values ONE and ZERO are derived from the signals RXD<3>, RXD<2>, RXD<1>, and RXD<0>, each of which represents one bit of data while RX_DV is asserted.

The value of the data transferred to the MAC is controlled by the RX_ER signal, see 22.2.1.5, Response to RX_ER indication from MII.

Synchronization between the PHY and the Reconciliation sublayer is achieved by way of the RX_CLK signal.

22.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each nibble of data transferred on RXD<3:0> will result in the generation of four PLS_DATA.indication transactions.

22.2.1.3 Mapping of PLS_CARRIER.indication

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indication to the MII signal CRS, and the LPI assert function if the EEE capability supported (see 22.7.2).

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indication (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signal CRS.

22.2.1.3.3 When generated

The PLS_CARRIER.indication service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

Any transition of the CRS signal from deasserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to deasserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to

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the receiveDataValid variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC processBitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

For EEE capability, CARRIER_STATUS is overridden according to the behavior of the LPI transmit state diagram (see Figure 22–23). The signal CRS has no effect on CARRIER_STATUS while in states LPI_ASSERTED and LPI_WAIT. A transition to the LPI_ASSERTED state in the transmit LPI state diagram shall cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and a transition to the LPI_DEASSERTED state in the transmit LPI state diagram shall cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value.

22.2.1.4 Mapping of PLS_SIGNAL.indication

22.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indication to the MII signal COL.

22.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indication (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the MII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is deasserted.

22.2.1.4.3 When generated

The PLS_SIGNAL.indication service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

22.2.1.5 Response to RX_ER indication from MII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

This requirement may be met by incorporating a function in the Reconciliation sublayer that produces a result that is guaranteed to be not equal to the CRC result, as specified by the algorithm in 3.2.9, of the sequence of nibbles comprising the received frame as delivered to the MAC sublayer. The Reconciliation sublayer must then ensure that the result of this function is delivered to the MAC sublayer at the end of the received frame in place of the last nibble(s) received from the MII.

Other techniques may be employed to respond to RX_ER, provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

22.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then the signal TX_ER may be generated.

For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

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Since there is no mechanism in the definition of the MAC sublayer by which the transmit data stream can be deliberately corrupted, the Reconciliation sublayer is not required to generate TX_ER.

22.2.1.7 Mapping of PLS_DATA_VALID.indication

22.2.1.7.1 Function

Map the primitive PLS_DATA_VALID.indication to the MII signal RX_DV.

22.2.1.7.2 Semantics of the service primitive

PLS_DATA_VALID.indication (DATA_VALID_STATUS)

The DATA_VALID_STATUS parameter can take one of two values: DATA_VALID or DATA_NOT_VALID. DATA_VALID_STATUS assumes the value DATA_VALID when the MII signal RX_DV is asserted, and assumes the value DATA_NOT_VALID when RX_DV is deasserted.

22.2.1.7.3 When generated

The PLS_DATA_VALID.indication service primitive is generated by the Reconciliation sublayer whenever the DATA_VALID_STATUS parameter changes from DATA_VALID to DATA_NOT_VALID or vice versa.

22.2.2 MII signal functional specifications

22.2.2.1 TX_CLK (transmit clock)

TX_CLK (Transmit Clock) is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals from the Reconciliation sublayer to the PHY. TX_CLK is sourced by the PHY.

The TX_CLK frequency shall be 25% of the nominal transmit data rate ± 100 ppm. For example, a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz, and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. The duty cycle of the TX_CLK signal shall be between 35% and 65% inclusive.

NOTE—See additional information in 22.2.4.1.5.

22.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the PHY. The PHY may recover the RX_CLK reference from the received data or it may derive the RX_CLK reference from a nominal clock (e.g., the TX_CLK reference).

The minimum high and low times of RX_CLK shall be 35% of the nominal period under all conditions.

While RX_DV is asserted, RX_CLK shall be synchronous with recovered data, shall have a frequency equal to 25% of the data rate of the received signal, and shall have a duty cycle of between 35% and 65% inclusive.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the

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medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is deasserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame or while the PHY is asserting LPI, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the deassertion of RX_DV at the end of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period. For EEE capability, RX_CLK may be stopped by the PHY during LPI when the Clock stop enable bit is asserted (see 22.2.2.9 and 45.2.3.1.4).

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5 and 22.2.2.9.

22.2.2.3 TX_EN (transmit enable)

TX_EN indicates that the Reconciliation sublayer is presenting nibbles on the MII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TX_EN shall be negated prior to the first TX_CLK following the final nibble of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the TX_CLK.

Figure 22–4 depicts TX_EN behavior during a frame transmission with no collisions.

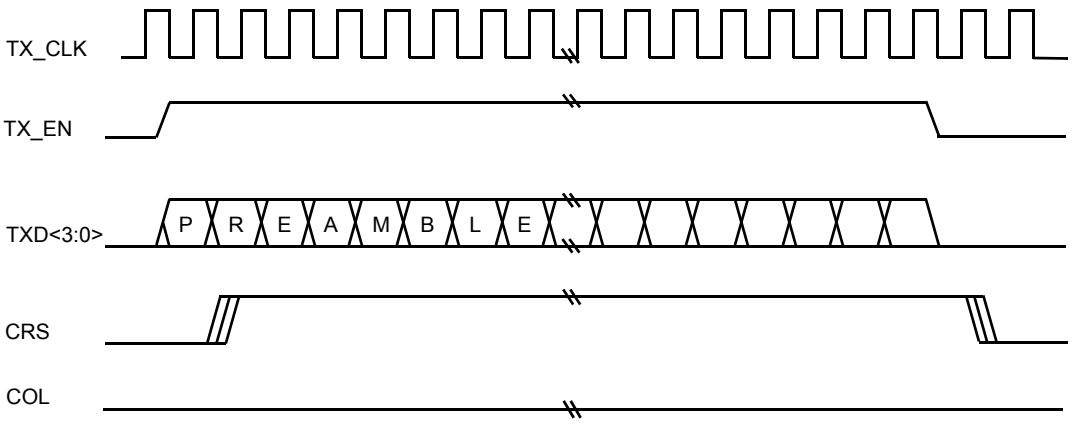


Figure 22–4—Transmission with no collision

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0 >is the least significant bit. While TX_EN and TX_ER are both deasserted, TXD<3:0> shall have no effect upon the PHY.

For EEE capability, the RS shall use the combination of TX_EN deasserted, TX_ER asserted, and TXD<3:0> equal to 0001 as shown in Table 22–1 as a request to enter, or remain in a low power state. Other values of TXD<3:0> with this combination of TX_EN and TX_ER shall have no effect upon the PHY.

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Figure 22–4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

22.2.2.5 TX_ER (transmit coding error)

TX_ER shall transition synchronously with respect to the TX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.

Assertion of the TX_ER signal shall not affect the transmission of data when a PHY is operating at 10 Mb/s, or when TX_EN is deasserted.

Figure 22–5 shows the behavior of TX_ER during the transmission of a frame propagating an error.

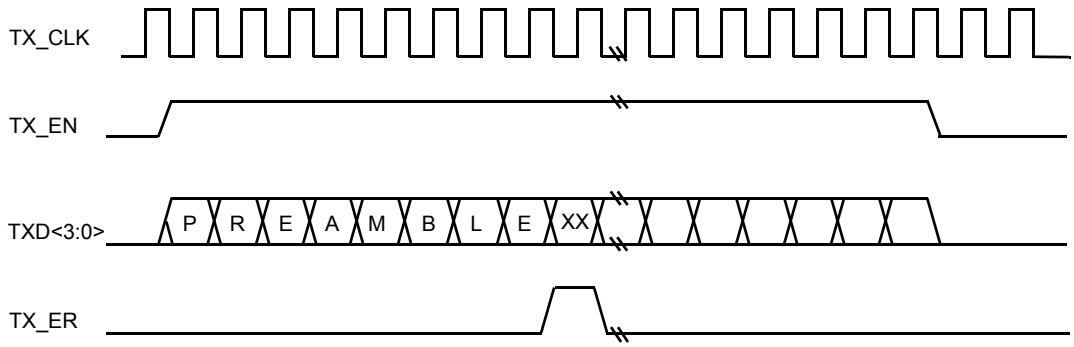


Figure 22–5—Propagating an error

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

The TX_ER signal shall be implemented at the MII of a PHY, may be implemented at the MII of a repeater that provides an MII port, and may be implemented in MAC sublayer devices. If a Reconciliation sublayer or a repeater with an MII port does not actively drive the TX_ER signal, it shall ensure that the TX_ER signal is pulled down to an inactive state at all times.

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22.2.2.6 Transmit direction LPI transition

When the transmit LPI state diagram is in state LPI_ASSERTED, the LPI client requests the PHY to transition to the LPI state by deasserting TX_EN, asserting TX_ER, and setting TXD<3:0> to 0001. The LPI client maintains the same state for these signals for the entire time that the PHY is to remain in the LPI state.

The LPI client requests the PHY to transition out of the LPI state by deasserting TX_ER and TXD. The LPI client should not assert TX_EN for valid transmit data until after the resolved wake up time specified for the PHY.

Figure 22–6 shows the behavior of TX_EN, TX_ER, and TXD<3:0> during the transition into and out of the LPI state.

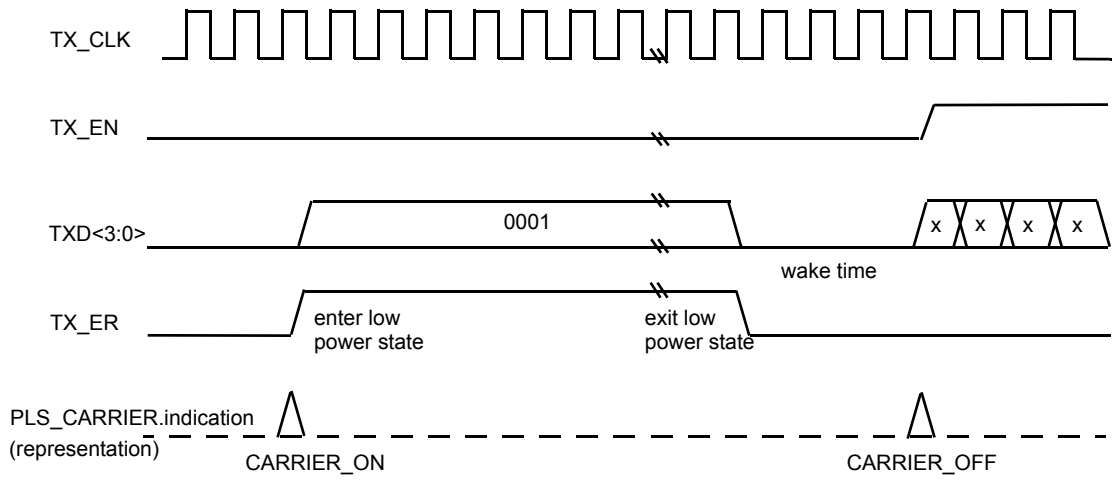


Figure 22–6—LPI transition

Table 22–1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

22.2.2.7 RX_DV (Receive Data Valid)

RX_DV (Receive Data Valid) is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the RXD<3:0> bundle and that the data on RXD<3:0> is synchronous to RX_CLK. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall remain asserted continuously from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first RX_CLK that follows the final nibble. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

Figure 22–7 shows the behavior of RX_DV during frame reception.

22.2.2.8 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. While RX_DV is deasserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

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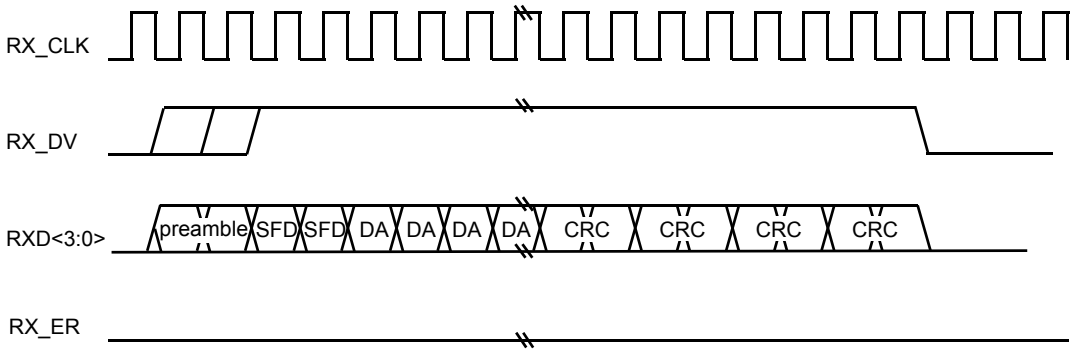


Figure 22–7—Reception with no errors

While RX_DV is deasserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 22.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

For EEE capability, the PHY indicates that it is receiving LPI by asserting the RX_ER signal and driving the value 0001 onto RXD<3:0> while RX_DV is deasserted.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the MII. In a DTE operating in half duplex mode, a PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2. In a DTE operating in full duplex mode, data transmitted on TXD <3:0> must not be looped back to RXD <3:0> unless the loopback mode of operation is selected.

Figure 22–7 shows the behavior of RXD<3:0> during frame reception.

Table 22–2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

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22.2.2.9 Receive direction LPI transition

When the PHY receives signals from the link partner to indicate transition into the low power state, it indicates this to the LPI client by asserting RX_ER and setting RXD<3:0> to 0001 while keeping RX_DV deasserted. The PHY maintains these signals in this state while it remains in the low power state. When the PHY receives signals from the link partner to indicate transition out of the low power state, it indicates this to the LPI client by deasserting RX_ER and returning to a normal interframe state.

While the PHY device is indicating LPI, it may halt the RX_CLK at any time more than 9 clock cycles after the start of the low power state as shown in (Figure 22–8) if and only if the Clock stop enable bit is asserted (see 45.2.3.1.4). The PHY may restart RX_CLK at any time while it is asserting LPI, but shall restart RX_CLK so that at least one positive transition occurs before it deasserts LPI.

Figure 22–8 shows the behavior of RX_ER, RX_DV and RXD<3:0> during LPI transitions.

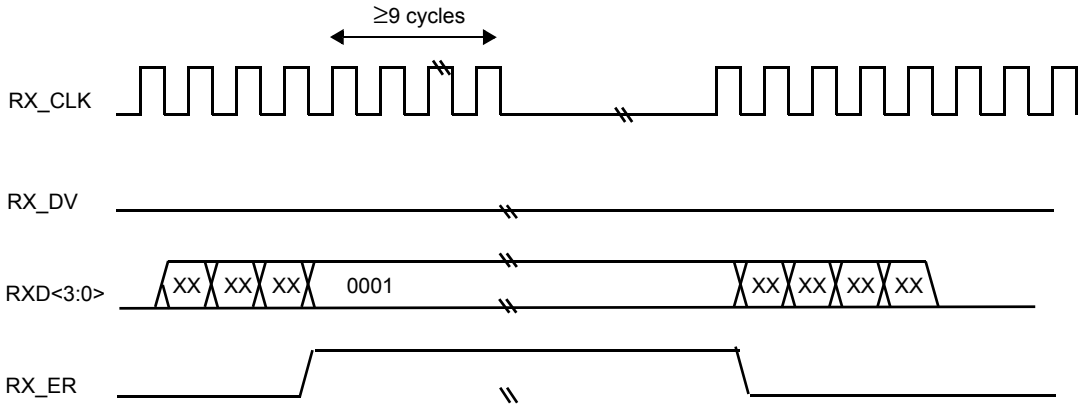


Figure 22–8—LPI transitions (receiver)

22.2.2.10 RX_ER (receive error)

RX_ER (Receive Error) is driven by the PHY. RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. RX_ER shall transition synchronously with respect to RX_CLK. While RX_DV is deasserted, RX_ER shall have no effect on the Reconciliation sublayer.

While RX_DV is deasserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<3:0>, as defined in 22.2.2.8. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

The effect of RX_ER on the Reconciliation sublayer is defined in 22.2.1.5, Response to RX_ER indication from MII.

Figure 22–9 shows the behavior of RX_ER during the reception of a frame with errors.

Figure 22–10 shows the behavior of RX_ER, RX_DV and RXD<3:0> during a False Carrier indication.

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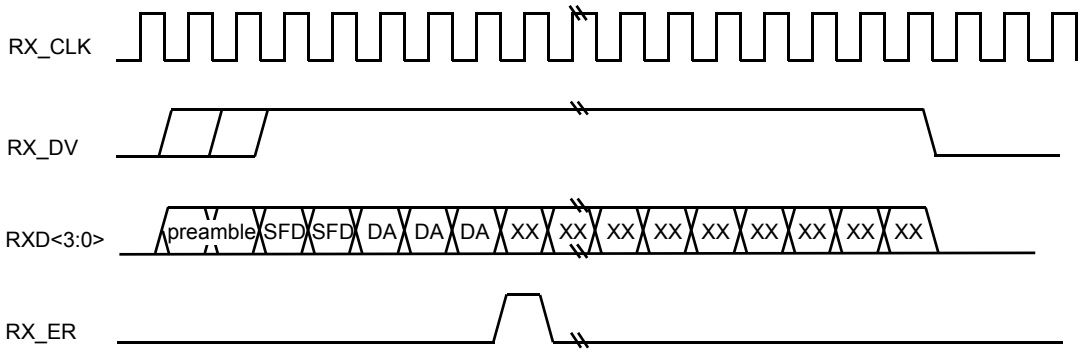


Figure 22–9—Reception with errors

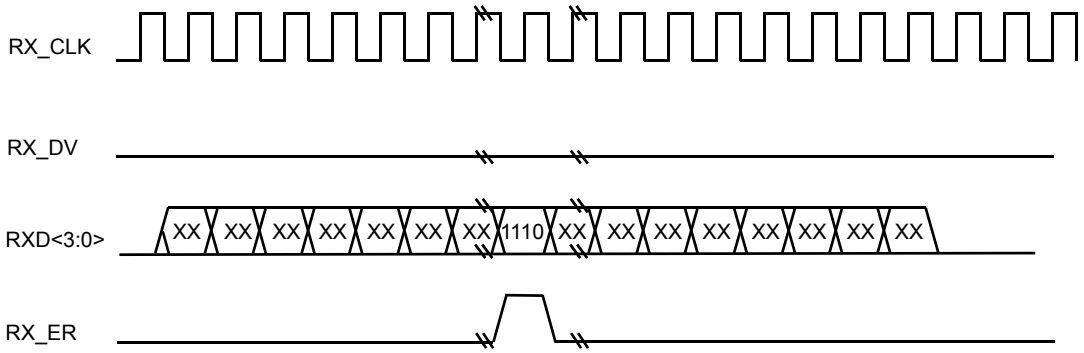


Figure 22–10—False Carrier indication

22.2.2.11 CRS (carrier sense)

CRS shall be asserted by the PHY when either the transmit or receive medium is nonidle. CRS shall be deasserted by the PHY when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

CRS is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the CRS signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–4 shows the behavior of CRS during a frame transmission without a collision, while Figure 22–11 shows the behavior of CRS during a frame transmission with a collision.

22.2.2.12 COL (collision detected)

COL shall be asserted by the PHY upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

COL shall be asserted by a PHY that is operating at 10 Mb/s in response to a *signal_quality_error* message from the PMA.

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COL is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22–11 shows the behavior of COL during a frame transmission with a collision.

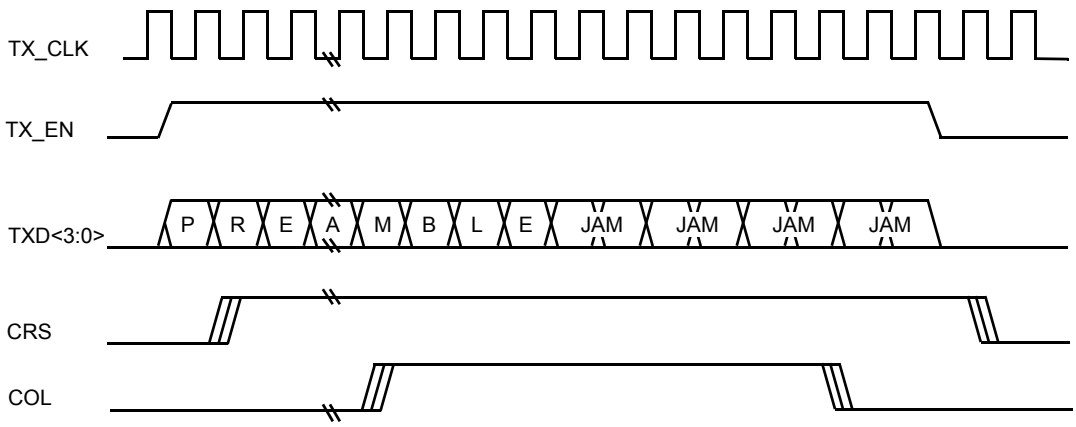


Figure 22–11—Transmission with collision

NOTE—The circuit assembly that contains the Reconciliation sublayer may incorporate a weak pull-up on the COL signal as a means of detecting an open circuit condition on the COL signal at the MII. The limit on the value of this pull-up is defined in 22.4.4.2.

22.2.2.13 MDC (management data clock)

MDC is sourced by the station management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC shall be 160 ns each, and the minimum period for MDC shall be 400 ns, regardless of the nominal period of TX_CLK and RX_CLK.

22.2.2.14 MDIO (management data input/output)

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control information and status between the PHY and the STA. Control information is driven by the STA synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the STA.

MDIO shall be driven through three-state circuits that enable either the STA or the PHY to drive the signal. A PHY that is attached to the MII via the mechanical interface specified in 22.6 shall provide a resistive pull-up to maintain the signal in a high state. The STA shall incorporate a resistive pull-down on the MDIO signal and thus may use the quiescent state of MDIO to determine if a PHY is connected to the MII via the mechanical interface defined in 22.6. The limits on the values of these pull-ups and pull-downs are defined in 22.4.4.2.

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22.2.3 MII data stream

Packets transmitted through the MII shall have the format shown in Figure 22–12.

<inter-frame><preamble><sfd><data><efd>

Figure 22–12—MII data stream

For the MII, transmission and reception of each octet of data shall be done a nibble at a time with the order of nibble transmission and reception as shown in Figure 22–13.

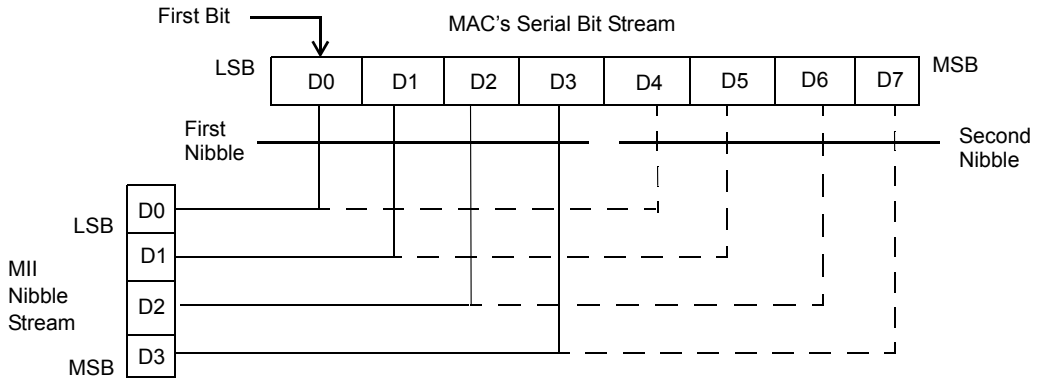


Figure 22–13—Octet/nibble transmit and receive order

The bits of each octet are transmitted and received as two nibbles, bits 0 through 3 of the octet corresponding to bits 0 through 3 of the first nibble transmitted or received, and bits 4 through 7 of the octet corresponding to bits 0 through 3 of the second nibble transmitted or received.

22.2.3.1 Inter-frame

The inter-frame period provides an observation window for an unspecified amount of time during which no data activity occurs on the MII. The absence of data activity is indicated by the deassertion of the RX_DV signal on the receive path, and the deassertion of the TX_EN signal on the transmit path. The MAC interFrameSpacing parameter defined in Clause 4 is measured from the deassertion of the CRS signal to the assertion of the CRS signal.

22.2.3.2 Preamble and start of frame delimiter

22.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the MII is unchanged from that specified in 7.2.3.2 and shall consist of 7 octets with the following bit values:

10101010 10101010 10101010 10101010 10101010 10101010 10101010

In the preceding example, the preamble is displayed using the bit order it would have if transmitted serially. This means that for each octet the leftmost l value represents the LSB of the octet, and the rightmost 0 value the octet MSB.

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The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value of the SFD at the MII is unchanged from that specified in 7.2.3.3 and is the bit sequence:

10101011

The preamble and SFD shall be transmitted through the MII as nibbles starting from the assertion of TX_EN as shown in Table 22–3.

Table 22–3—Transmitted preamble and SFD

Signal	Bit values of nibbles transmitted through MII																		
TXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
TXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble transmitted.
[b]1st SFD nibble transmitted.
[c]1st data nibble transmitted.
[d]D0 through D7 are the first eight bits of the data field from the Protocol Data Unit (PDU).

22.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 22.2.2.7.

The alignment of the received SFD and data at the MII shall be as shown in Table 22–4 and Table 22–5. Table 22–4 depicts the case where no preamble nibbles are conveyed across the MII, and Table 22–5 depicts the case where the entire preamble is conveyed across the MII.

Table 22–4—Start of receive with no preamble preceding SFD

Signal	Bit values of nibbles received through MII										
RXD0	X	X	X	X	X	X	X	1[a]	1	D0[b]	D4[c]
RXD1	X	X	X	X	X	X	X	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	1	1	1	1

[a]1st SFD nibble received.
[b]1st data nibble received.
[c]D0 through D7 are the first eight bits of the data field from the PDU.

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Table 22–5—Start of receive with entire preamble preceding SFD

Signal	Bit values of nibbles received through MII																		
RXD0	X	1[a]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[b]	1	D0[c]	D4[d]
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[a]1st preamble nibble received.
[b]1st SFD nibble received.
[c]1st data nibble received.
[d]D0 through D7 are the first eight bits of the data field from the PDU.

22.2.3.3 Data

The data in a well formed frame shall consist of N octets of data transmitted as 2N nibbles. For each octet of data the transmit order of each nibble is as specified in Figure 22–13. Data in a collision fragment may consist of an odd number of nibbles.

22.2.3.4 End-of-Frame delimiter (EFD)

Deassertion of the TX_EN signal constitutes an End-of-Frame delimiter for data conveyed on TXD<3:0>, and deassertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<3:0>.

22.2.3.5 Handling of excess nibbles

An excess nibble condition occurs when an odd number of nibbles is conveyed across the MII beginning with the SFD and including all nibbles conveyed until the End-of-Frame delimiter. Reception of a frame containing a non-integer number of octets shall be indicated by the PHY as an excess nibble condition.

Transmission of an excess nibble may be handled by the PHY in an implementation-specific manner. No assumption should be made with regard to truncation, octet padding, or exact nibble transmission by the PHY.

22.2.4 Management functions

The management interface specified here provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface.

The MII Management Interface consists of a pair of signals that physically transport the management information across the MII or GMII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register definition specifies a basic register set with an extension mechanism. The MII uses two basic registers. The GMII also uses the same two basic registers and adds a third basic register.

The MII basic register set consists of two registers referred to as the Control register (Register 0) and the Status register (Register 1). All PHYs that provide an MII Management Interface shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). The

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status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through 14 are part of the extended register set. The format of Registers 4 through 10 are defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of Registers 1 and 15.

The full set of management registers is listed in Table 22–6.

Table 22–6—MII management register set

Register address	Register name	Basic/Extended	
		MII	GMII
0	Control	B	B
1	Status	B	B
2,3	PHY Identifier	E	E
4	Auto-Negotiation Advertisement	E	E
5	Auto-Negotiation Link Partner Base Page Ability	E	E
6	Auto-Negotiation Expansion	E	E
7	Auto-Negotiation Next Page Transmit	E	E
8	Auto-Negotiation Link Partner Received Next Page	E	E
9	MASTER-SLAVE Control Register	E	E
10	MASTER-SLAVE Status Register	E	E
11	PSE Control register	E	E
12	PSE Status register	E	E
13	MMD Access Control Register	E	E
14	MMD Access Address Data Register	E	E
15	Extended Status	Reserved	B
16 through 31	Vendor Specific	E	E

22.2.4.1 Control register (Register 0)

The assignment of bits in the Control Register is shown in Table 22–7. The default value for each bit of the Control Register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

22.2.4.1.1 Reset

Resetting a PHY is accomplished by setting bit 0.15 to a logic one. This action shall set the status and control registers to their default states. As a consequence this action may change the internal state of the PHY and the state of the physical link associated with the PHY. This bit is self-clearing, and a PHY shall return a value of one in bit 0.15 until the reset process is completed. A PHY is not required to accept a write transaction to the control register until the reset process is completed, and writes to bits of the control register other than 0.15 may have no effect until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 0.15.

The default value of bit 0.15 is zero.

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Table 22–7—Control register bit definitions

Bit(s)	Name	Description	R/W[a]
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
0.13	Speed Selection (LSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.12	Auto-Negotiation Enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
0.11	Power Down	1 = power down 0 = normal operation[b]	R/W
0.10	Isolate	1 = electrically Isolate PHY from MII or GMII 0 = normal operation[b]	R/W
0.9	Restart Auto-Negotiation	1 = restart Auto-Negotiation process 0 = normal operation	R/W SC
0.8	Duplex Mode	1 = full duplex 0 = half duplex	R/W
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
0.6	Speed Selection (MSB)	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s	R/W
0.5	Unidirectional enable	When bit 0.12 is one or bit 0.8 is zero, this bit is ignored. When bit 0.12 is zero and bit 0.8 is one: 1 = Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established	R/W
0.4:0	Reserved	Write as 0, ignore on read	R/W

[a]R/W = Read/Write, SC = Self-clearing.
[b]For normal operation, both 0.10 and 0.11 must be cleared to zero; see 22.2.4.1.5.

NOTE—This operation may interrupt data communication.

22.2.4.1.2 Loopback

The PHY shall be placed in a loopback mode of operation when bit 0.14 is set to a logic one. When bit 0.14 is set, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII or GMII shall not result in the transmission of data on the network medium. When bit 0.14 is set, the PHY shall accept data from the MII or GMII transmit data path and return it to the MII or GMII receive data path in response to the assertion of TX_EN. When bit 0.14 is set, the delay from the assertion of TX_EN to

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the assertion of RX_DV shall be less than 512 BT. When bit 0.14 is set, the COL signal shall remain deasserted at all times, unless bit 0.7 is set, in which case the COL signal shall behave as described in 22.2.4.1.9. Clearing bit 0.14 to zero allows normal operation.

The default value of bit 0.14 is zero.

NOTE—The signal path through the PHY that is exercised in the loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY circuitry as is practical. The intention of providing this loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths through a PHY may be enabled via the extended register set, in an implementation-specific fashion.

22.2.4.1.3 Speed selection

Link speed can be selected via either the Auto-Negotiation process, or manual speed selection. Manual speed selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled and bit 0.6 is cleared to a logic zero, setting bit 0.13 to a logic one configures the PHY for 100 Mb/s operation, and clearing bit 0.13 to a logic zero configures the PHY for 10 Mb/s operation. When Auto-Negotiation is disabled and bit 0.6 is set to a logic one, clearing bit 0.13 to a logic zero selects 1000 Mb/s operation. The combination of both bits 0.6 and 0.13 set to a logic one is reserved for future standardization. When Auto-Negotiation is enabled, bits 0.6 and 0.13 can be read or written, but the state of bits 0.6 and 0.13 have no effect on the link configuration, and it is not necessary for bits 0.6 and 0.13 to reflect the operating speed of the link when it is read. If a PHY reports via bits 1.15:9 and bits 15.15:12 that it is not able to operate at all speeds, the value of bits 0.6 and 0.13 shall correspond to a speed at which the PHY can operate, and any attempt to change the bits to an invalid setting shall be ignored.

The default value of bits 0.6 and 0.13 are the encoding of the highest data rate at which the PHY can operate as indicated by bits 1.15:9 and 15.15:12.

22.2.4.1.4 Auto-Negotiation enable

The Auto-Negotiation process shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13, 0.8, and 0.6 shall have no effect on the link configuration, and station operation other than that specified by the Auto-Negotiation protocol. If bit 0.12 is cleared to a logic zero, then bits 0.13, 0.8, and 0.6 will determine the link configuration, regardless of the prior state of the link configuration and the Auto-Negotiation process.

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, the PHY shall return a value of zero in bit 0.12. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, bit 0.12 should always be written as zero, and any attempt to write a one to bit 0.12 shall be ignored.

The default value of bit 0.12 is one, unless the PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 0.12 is zero.

22.2.4.1.5 Power down

The PHY may be placed in a low-power consumption state by setting bit 0.11 to a logic one. Clearing bit 0.11 to zero allows normal operation. The specific behavior of a PHY in the power-down state is implementation specific. While in the power-down state, the PHY shall respond to management transactions. During the transition to the power-down state and while in the power-down state, the PHY shall not generate spurious signals on the MII or GMII.

A PHY is not required to meet the RX_CLK and TX_CLK signal functional requirements when either bit 0.11 or bit 0.10 is set to a logic one. A PHY shall meet the RX_CLK and TX_CLK signal functional requirements defined in 22.2.2 within 0.5 s after both bit 0.11 and 0.10 are cleared to zero.

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The default value of bit 0.11 is zero.

22.2.4.1.6 Isolate

The PHY may be forced to electrically isolate its data paths from the MII or GMII by setting bit 0.10 to a logic one. Clearing bit 0.10 allows normal operation. When the PHY is isolated from the MII or GMII it shall not respond to the TXD data bundle, TX_EN, TX_ER and GTX_CLK inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD data bundle, COL, and CRS outputs. When the PHY is isolated from the MII or GMII it shall respond to management transactions.

A PHY that is connected to the MII via the mechanical interface defined in 22.6 shall have a default value of one for bit 0.10 so as to avoid the possibility of having multiple MII output drivers actively driving the same signal path simultaneously.

NOTE—This clause neither requires nor assumes any specific behavior at the MDI resulting from setting bit 0.10 to a logic one.

22.2.4.1.7 Restart Auto-Negotiation

If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the PHY shall return a value of zero in bit 0.9. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, bit 0.9 should always be written as zero, and any attempt to write a one to bit 0.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 0.9 to a logic one. This bit is self-clearing, and a PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall not be affected by writing a zero to bit 0.9.

The default value of bit 0.9 is zero.

22.2.4.1.8 Duplex mode

The duplex mode can be selected via either the Auto-Negotiation process, or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by clearing bit 0.12 to zero. When Auto-Negotiation is disabled, setting bit 0.8 to a logic one configures the PHY for full duplex operation, and clearing bit 0.8 to a logic zero configures the PHY for half duplex operation. When Auto-Negotiation is enabled, bit 0.8 can be read or written, but the state of bit 0.8 has no effect on the link configuration. If a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate in only one duplex mode, the value of bit 0.8 shall correspond to the mode in which the PHY can operate, and any attempt to change the setting of bit 0.8 shall be ignored.

When a PHY is placed in the loopback mode of operation via bit 0.14, the behavior of the PHY shall not be affected by the state of bit 0.8.

The default value of bit 0.8 is zero, unless a PHY reports via bits 1.15:9 and 15.15:12 that it is able to operate only in full duplex mode, in which case the default value of bit 0.8 is one.

22.2.4.1.9 Collision test

The COL signal at the MII or GMII may be tested by setting bit 0.7 to a logic one. When bit 0.7 is set to one, the PHY shall assert the COL signal within 512 BT in response to the assertion of TX_EN. While bit 0.7 is set to one, the PHY shall deassert the COL signal within 4 BT when connected to an MII, or 16 BT when connected to a GMII, in response to the deassertion of TX_EN. Clearing bit 0.7 to zero allows normal operation.

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The default value of bit 0.7 is zero.

NOTE—It is recommended that the Collision Test function be used only in conjunction with the loopback mode of operation defined in 22.2.4.1.2.

22.2.4.1.10 Speed selection

Bit 0.6 is used in conjunction with bits 0.13 and 0.12 to select the speed of operation as described in 22.2.4.1.3.

22.2.4.1.11 Reserved bits

Bits 0.4:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.1.12 Unidirectional enable

If a PHY reports via bit 1.7 that it lacks the ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established, the PHY shall return a value of zero in bit 0.5, and any attempt to write a one to bit 0.5 shall be ignored.

The ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established is controlled by bit 0.5 as well as the status of Auto-Negotiation Enable bit 0.12 and the Duplex Mode bit 0.8 as this ability can only be supported if Auto-Negotiation is disabled and the PHY is operating in full-duplex mode. If bit 0.5 is set to a logic one, bit 0.12 to logic zero and bit 0.8 to logic one, encoding and transmitting data from the media independent interface shall be enabled regardless of whether the PHY has determined that a valid link has been established. If bit 0.5 is set to a logic zero, bit 0.12 to logic one or bit 0.8 to logic zero, encoding and transmitting data from the media independent interface shall be dependent on whether the PHY has determined that a valid link has been established. When bit 0.12 is one or bit 0.8 is zero, bit 0.5 shall be ignored.

A management entity shall set bit 0.5 to a logic one only after it has enabled an associated OAM sublayer (see Clause 57) or if this device is a 1000BASE-PX-D PHY. A management entity shall clear bit 0.5 to a logic zero prior to it disabling an associated OAM sublayer when this device is not a 1000BASE-PX-D PHY. To avoid collisions, a management entity should not set bit 0.5 of a 1000BASE-PX-U PHY to a logic one.

The default value of bit 0.5 is zero, except for 1000BASE-PX-D, where it is one.

22.2.4.2 Status register (Register 1)

The assignment of bits in the Status register is shown in Table 22–8. All of the bits in the Status register are read only, a write to the Status register shall have no effect.

22.2.4.2.1 100BASE-T4 ability

When read as a logic one, bit 1.15 indicates that the PHY has the ability to perform link transmission and reception using the 100BASE-T4 signaling specification. When read as a logic zero, bit 1.15 indicates that the PHY lacks the ability to perform link transmission and reception using the 100BASE-T4 signaling specification.

22.2.4.2.2 100BASE-X full duplex ability

When read as a logic one, bit 1.14 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit

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Table 22–8—Status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO
1.14	100BASE-X Full Duplex	1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X	RO
1.13	100BASE-X Half Duplex	1 = PHY able to perform half duplex 100BASE-X 0 = PHY not able to perform half duplex 100BASE-X	RO
1.12	10 Mb/s Full Duplex	1 = PHY able to operate at 10 Mb/s in full duplex mode 0 = PHY not able to operate at 10 Mb/s in full duplex mode	RO
1.11	10 Mb/s Half Duplex	1 = PHY able to operate at 10 Mb/s in half duplex mode 0 = PHY not able to operate at 10 Mb/s in half duplex mode	RO
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full duplex 100BASE-T2 0 = PHY not able to perform full duplex 100BASE-T2	RO
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half duplex 100BASE-T2	RO
1.8	Extended Status	1 = Extended status information in Register 15 0 = No extended status information in Register 15	RO
1.7	Unidirectional ability	1 = PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established 0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established	RO
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
1.4	Remote Fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO/ LH
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
1.2	Link Status	1 = link is up 0 = link is down	RO/ LL
1.1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	RO/ LH
1.0	Extended Capability	1 = extended register capabilities 0 = basic register set capabilities only	RO

[a]RO = Read only, LL = Latching low, LH = Latching high

1.14 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-X signaling specification.

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22.2.4.2.3 100BASE-X half duplex ability

When read as a logic one, bit 1.13 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification. When read as a logic zero, bit 1.13 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-X signaling specification.

22.2.4.2.4 10 Mb/s full duplex ability

When read as a logic one, bit 1.12 indicates that the PHY has the ability to perform full duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.12 indicates that the PHY lacks the ability to perform full duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.5 10 Mb/s half duplex ability

When read as a logic one, bit 1.11 indicates that the PHY has the ability to perform half duplex link transmission and reception while operating at 10 Mb/s. When read as a logic zero, bit 1.11 indicates that the PHY lacks the ability to perform half duplex link transmission and reception while operating at 10 Mb/s.

22.2.4.2.6 100BASE-T2 full duplex ability

When read as a logic one, bit 1.10 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.10 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.7 100BASE-T2 half duplex ability

When read as a logic one, bit 1.9 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification. When read as a logic zero, bit 1.9 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 100BASE-T2 signaling specification.

22.2.4.2.8 Unidirectional ability

When read as a logic one, bit 1.7 indicates that the PHY has the ability to encode and transmit data from the media independent interface regardless of whether the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.7 indicates the PHY is able to transmit data from the media independent interface only when the PHY has determined that a valid link has been established.

A PHY shall return a value of zero in bit 1.7 if it is not a 100BASE-X PHY using the PCS and PMA specified in 66.1 or a 1000BASE-X PHY using the PCS and PMA specified in 66.2.

22.2.4.2.9 MF preamble suppression ability

When read as a logic one, bit 1.6 indicates that the PHY is able to accept management frames regardless of whether they are or are not preceded by the preamble pattern described in 22.2.4.5.2. When read as a logic zero, bit 1.6 indicates that the PHY is not able to accept management frames unless they are preceded by the preamble pattern described in 22.2.4.5.2.

22.2.4.2.10 Auto-Negotiation complete

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the extended registers implemented by the Auto-Negotiation protocol (either Clause 28 or

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Clause 37) are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of the extended registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

22.2.4.2.11 Remote fault

When read as a logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

If a PHY has no provision for remote fault detection, it shall maintain bit 1.4 in a cleared state. Further information regarding the remote fault indication can be found in 37.2.1.5, 22.2.1.2, and 24.3.2.1.

22.2.4.2.12 Auto-Negotiation ability

When read as a logic one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

22.2.4.2.13 Link Status

When read as a logic one, bit 1.2 indicates that the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.2 indicates that the link is not valid. The criteria for determining link validity is PHY specific. The Link Status bit shall be implemented with a latching function, such that the occurrence of a link failure condition will cause the Link Status bit to become cleared and remain cleared until it is read via the management interface. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

22.2.4.2.14 Jabber detect

When read as a logic one, bit 1.1 indicates that a jabber condition has been detected. This status indication is intended to support the management attribute defined in 30.5.1.1.6, aJabber, and the MAU notification defined in 30.5.1.3.1, nJabber. The criteria for the detection of a jabber condition is PHY specific. The Jabber Detect bit shall be implemented with a latching function, such that the occurrence of a jabber condition will cause the Jabber Detect bit to become set and remain set until it is cleared. The Jabber Detect bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

PHYs specified for 100 Mb/s operation or above do not incorporate a Jabber Detect function, as this function is defined to be performed in the repeater unit at these speeds. Therefore, PHYs specified for 100 Mb/s operation and above shall always return a value of zero in bit 1.1.

22.2.4.2.15 Extended capability

When read as a logic one, bit 1.0 indicates that the PHY provides an extended set of capabilities which may be accessed through the extended register set. When read as a logic zero, bit 1.0 indicates that the PHY provides only the basic register set.

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22.2.4.2.16 Extended status

When read as a logic one, bit 1.8 indicates that the base register status information is extended into Register 15. All PHYs supporting 1000 Mb/s operation shall have this bit set to a logic one. When read as a logic zero, bit 1.8 indicates that the extended status is not implemented.

22.2.4.3 Extended capability registers

In addition to the basic register set defined in 22.2.4.1 and 22.2.4.2, PHYs may provide an extended set of capabilities that may be accessed and controlled via the MII management interface. Thirteen registers have been defined within the extended address space for the purpose of providing a PHY-specific identifier to layer management, to provide control and monitoring for the Auto-Negotiation process, and to provide control and monitoring of power sourcing equipment, and to provide MDIO Manageable Device (MMD) register access.

If an attempt is made to perform a read transaction to a register in the extended register set, and the PHY being read does not implement the addressed register, the PHY shall not drive the MDIO line in response to the read transaction. If an attempt is made to perform a write transaction to a register in the extended register set, and the PHY being written does not implement the addressed register, the write transaction shall be ignored by the PHY.

22.2.4.3.1 PHY Identifier (Registers 2 and 3)

Registers 2 and 3 provide a 32-bit value, which shall constitute a unique identifier for a particular type of PHY. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier.

Bit 2.15 shall be the MSB of the PHY Identifier, and bit 3.0 shall be the LSB of the PHY Identifier.

The PHY Identifier shall be composed of the third through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the PHY manufacturer by the IEEE,[1] plus a six-bit manufacturer's model number, plus a four-bit manufacturer's revision number. The PHY Identifier is intended to provide sufficient information to support the oResourceTypeID object as required in 30.1.2.

The third bit of the OUI is assigned to bit 2.15, the fourth bit of the OUI is assigned to bit 2.14, and so on. Bit 2.0 contains the eighteenth bit of the OUI. Bit 3.15 contains the nineteenth bit of the OUI, and bit 3.10 contains the twenty-fourth bit of the OUI. Bit 3.9 contains the MSB of the manufacturer's model number. Bit 3.4 contains the LSB of the manufacturer's model number. Bit 3.3 contains the MSB of the manufacturer's revision number, and bit 3.0 contains the LSB of the manufacturer's revision number.

NOTE—The use of only 22 bits of the OUI as described here has been deprecated by the IEEE Registration Authority. The definition of vendor-specific device identifiers for other applications is expected to use the full 24 bits to accommodate the use of either an OUI or Company ID.

[1]Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854, USA.

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Figure 22–14 depicts the mapping of this information to the bits of Registers 2 and 3. Additional detail describing the format of OUIs can be found in IEEE Std 802.

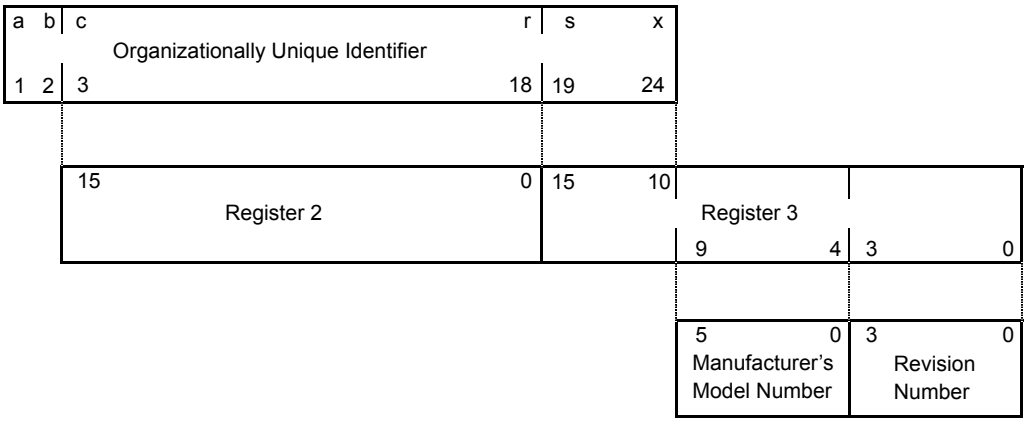


Figure 22–14—Format of PHY Identifier

22.2.4.3.2 Auto-Negotiation advertisement (Register 4)

Register 4 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.3 Auto-Negotiation link partner ability (Register 5)

Register 5 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.4 Auto-Negotiation expansion (Register 6)

Register 6 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.5 Auto-Negotiation Next Page (Register 7)

Register 7 provides 16 bits that are used by the Auto-Negotiation process. See 28.2.4.1 and 37.2.5.1.

22.2.4.3.6 Auto-Negotiation link partner Received Next Page (Register 8)

Register 8 provides 16 bits that are used by the Auto-Negotiation process. See 32.5.1 and 37.2.5.1.

22.2.4.3.7 MASTER-SLAVE control register (Register 9)

Register 9 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.8 MASTER-SLAVE status register (Register 10)

Register 10 provides bit values by 100BASE-T2 (as specified in 32.5) and 1000BASE-T (as specified in 40.5).

22.2.4.3.9 PSE Control register (Register 11)

Register 11 provides control bits that are used by a PSE. See 33.5.1.1.

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22.2.4.3.10 PSE Status register (Register 12)

Register 12 provides status bits that are supplied by a PSE. See 33.5.1.2.

22.2.4.3.11 MMD access control register (Register 13)

The assignment of bits in the MMD access control register is shown in Table 22–9. The MMD access control register is used in conjunction with the MMD access address data register (Register 14) to provide access to the MMD address space using the interface and mechanisms defined in 22.2.4.

Table 22–9—MMD access control register bit definitions

Bit(s)	Name	Description	R/W[a]
13.15:14	Function	13.1513.14 00= address 01= data, no post increment 10= data, post increment on reads and writes 11= data, post increment on writes only	R/W
13.13:5	Reserved	Write as 0, ignore on read	R/W
13.4:0	DEVAD	Device address	R/W

[a]R/W = Read/Write

Each MMD maintains its own individual address register as described in 45.2.8. The DEVAD field directs any accesses of Register 14 to the appropriate MMD as described in 45.2. If the access of Register 14 is an address access (bits 13.15:14 = 00) then it is directed to the address register within the MMD associated with the value in the DEVAD field (bits 13.4:0). Otherwise, both the DEVAD field and that MMD's address register direct the Register 14 data accesses to the appropriate registers within that MMD.

The Function field can be set to any of four values:

a) When set to 00, accesses to Register 14 access the MMD's individual address register. This address register should always be initialized before attempting any accesses to other MMD registers.
b) When set to 01, accesses to Register 14 access the register within the MMD selected by the value in the MMD's address register.
c) When set to 10, accesses to Register 14 access the register within the MMD selected by the value in the MMD's address register. After that access is complete, for both read and write accesses, the value in the MMD's address field is incremented.
d) When set to 11, accesses to Register 14 access the register within the MMD selected by the value in the MMD's address register. After that access is complete, for write accesses only, the value in the MMD's address field is incremented. For read accesses, the value in the MMD's address field is not modified.

For additional insight into the operation and usage of this register, see Annex 22D.

22.2.4.3.12 MMD access address data register (Register 14)

The assignment of bits in the MMD access address data register is shown in Table 22–10. The MMD access address data register is used in conjunction with the MMD access control register (Register 13) to provide access to the MMD address space using the interface and mechanisms defined in 22.2.4. Accesses to this

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register are controlled by the value of the fields in Register 13 and the contents of the MMD's individual address field as described in 22.2.4.3.11.

Table 22–10—MMD access address data register bit definitions

Bit(s)	Name	Description	R/W[a]
14.15:0	Address Data	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register	R/W

[a]R/W = Read/Write

For additional insight into the operation and usage of this register, see Annex 22D.

22.2.4.3.13 PHY specific registers

A particular PHY may provide additional registers beyond those defined above. Register addresses 16 through 31 (decimal) may be used to provide vendor-specific functions or abilities. The definition of Registers 4 through 14 are dependent on the version (Clause 28 or Clause 37) of Auto-Negotiation protocol used by the PHY.

22.2.4.4 Extended Status register (Register 15)

The Extended Status register is implemented for 1000BASE-T PHYs and all PHYs using the 1000BASE-X signaling specifications. The assignment of bits in the Extended Status register is shown in Table 22–11. All of the bits in the Extended Status register are read only; a write to the Extended Status register shall have no effect.

Table 22–11—Extended Status register bit definitions

Bit(s)	Name	Description	R/W[a]
15.15	1000BASE-X Full Duplex	1 = PHY able to perform full duplex 1000BASE-X 0 = PHY not able to perform full duplex 1000BASE-X	RO
15.14	1000BASE-X Half Duplex	1 = PHY able to perform half duplex 1000BASE-X 0 = PHY not able to perform half duplex 1000BASE-X	RO
15.13	1000BASE-T Full Duplex	1 = PHY able to perform full duplex 1000BASE-T 0 = PHY not able to perform full duplex 1000BASE-T	RO
15.12	1000BASE-T Half Duplex	1 = PHY able to perform half duplex 1000BASE-T 0 = PHY not able to perform half duplex 1000BASE-T	RO
15.11:0	Reserved	Ignore when read	RO

[a]RO = Read only

22.2.4.4.1 1000BASE-X full duplex ability

When read as a logic one, bit 15.15 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the

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bit 15.15 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification.

22.2.4.4.2 1000BASE-X half duplex ability

When read as a logic one, bit 15.14 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification. When read as a logic zero, the bit 15.14 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-X signaling specification.

22.2.4.4.3 1000BASE-T full duplex ability

When read as a logic one, bit 15.13 indicates that the PHY has the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.13 indicates that the PHY lacks the ability to perform full duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.4 1000BASE-T half duplex ability

When read as a logic one, bit 15.12 indicates that the PHY has the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification. When read as a logic zero, the bit 15.12 indicates that the PHY lacks the ability to perform half duplex link transmission and reception using the 1000BASE-T signaling specification.

22.2.4.4.5 Reserved bits

Bits 15:11:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

22.2.4.5 Management frame structure

Frames transmitted on the MII Management Interface shall have the frame structure shown in Table 22–12. The order of bit transmission shall be from left to right.

Table 22–12—Management frame format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

22.2.4.5.1 IDLE (IDLE condition)

The IDLE condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the PHY's pull-up resistor will pull the MDIO line to a logic one.

22.2.4.5.2 PRE (preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can

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use to establish synchronization. A PHY shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

If the STA determines that every PHY that is connected to the MDIO signal is able to accept management frames that are not preceded by the preamble pattern, then the STA may suppress the generation of the preamble pattern, and may initiate management frames with the ST (Start of Frame) pattern.

22.2.4.5.3 ST (start of frame)

The start of frame is indicated by a <01> pattern. This pattern assures transitions from the default logic one line state to zero and back to one.

22.2.4.5.4 OP (operation code)

The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.

22.2.4.5.5 PHYAD (PHY Address)

The PHY Address is five bits, allowing 32 unique PHY addresses. The first PHY address bit transmitted and received is the MSB of the address. A PHY that is connected to the station management entity via the mechanical interface defined in 22.6 shall always respond to transactions addressed to PHY Address zero <00000>. A station management entity that is attached to multiple PHYs must have prior knowledge of the appropriate PHY Address for each PHY.

22.2.4.5.6 REGAD (Register Address)

The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address. The register accessed at Register Address zero <00000> shall be the control register defined in 22.2.4.1, and the register accessed at Register Address one <00001> shall be the status register defined in 22.2.4.2.

22.2.4.5.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY shall remain in a high-impedance state for the first bit time of the turnaround. The PHY shall drive a zero bit during the second bit time of the turnaround of a read transaction. During a write transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–15 shows the behavior of the MDIO signal during the turnaround field of a read transaction.

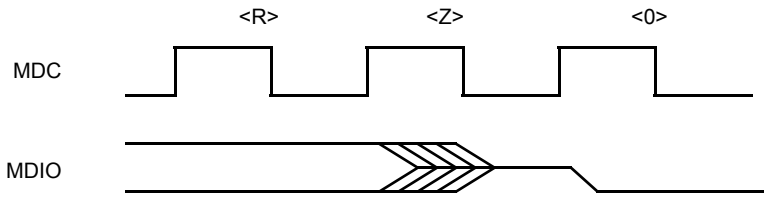


Figure 22–15—Behavior of MDIO during TA field of a read transaction

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22.2.4.5.8 DATA (data)

The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

22.3 Signal timing characteristics

All signal timing characteristics shall be measured using the techniques specified in Annex 22C. The signal threshold potentials $V_{ih(min)}$ and $V_{il(max)}$ are defined in 22.4.4.1.

The HIGH time of an MII signal is defined as the length of time that the potential of the signal is greater than or equal to $V_{ih(min)}$. The LOW time of an MII signal is defined as the length of time that the potential of the signal is less than or equal to $V_{il(max)}$.

The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

The propagation delay from an MII clock edge to a valid MII signal is defined as the length of time between when the clock exits the switching region and when the signal exits and remains out of the switching region.

22.3.1 Signals that are synchronous to TX_CLK

Figure 22–16 shows the timing relationship for the signals associated with the transmit data path at the MII connector. The clock to output delay shall be a minimum of 0 ns and a maximum of 25 ns.

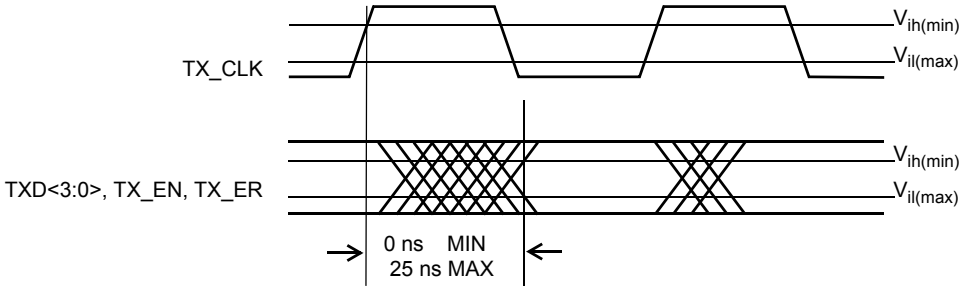


Figure 22–16—Transmit signal timing relationships at the MII

22.3.1.1 TX_EN

TX_EN is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as shown in Figure 22–16.

22.3.1.2 TXD<3:0>

TXD<3:0> is transitioned by the Reconciliation sublayer synchronously with respect to the TX_CLK rising edge with the timing as depicted in Figure 22–16.

22.3.1.3 TX_ER

TX_ER is transitioned synchronously with respect to the rising edge of TX_CLK as shown in Figure 22–16.

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22.3.2 Signals that are synchronous to RX_CLK

Figure 22–17 shows the timing relationship for the signals associated with the receive data path at the MII connector. The timing is referenced to the rising edge of the RX_CLK. The input setup time shall be a minimum of 10 ns and the input hold time shall be a minimum of 10 ns.

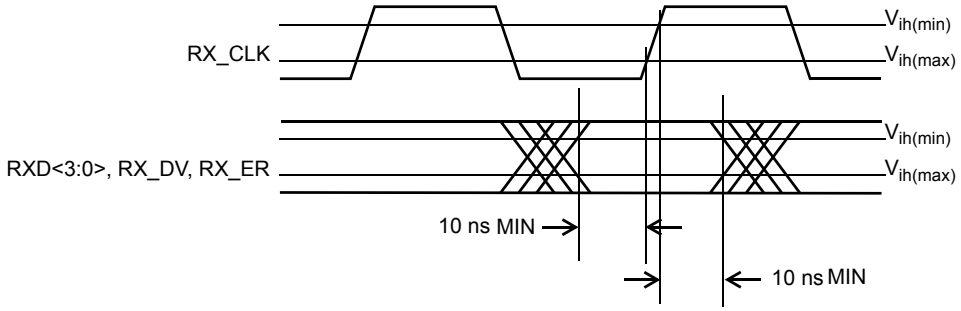


Figure 22–17—Receive signal timing relationships at the MII

22.3.2.1 RX_DV

RX_DV is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK with the timing shown in Figure 22–17.

22.3.2.2 RXD<3:0>

RXD<3:0> is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–17. The RXD<3:0> timing requirements must be met at all rising edges of RX_CLK.

22.3.2.3 RX_ER

RX_ER is sampled by the Reconciliation sublayer synchronously with respect to the rising edge of RX_CLK as shown in Figure 22–17. The RX_ER timing requirements must be met at all rising edges of RX_CLK.

22.3.3 Signals that have no required clock relationship

22.3.3.1 CRS

CRS is driven by the PHY. Transitions on CRS have no required relationship to either of the clock signals provided at the MII.

22.3.3.2 COL

COL is driven by the PHY. Transitions on COL have no required relationship to either of the clock signals provided at the MII.

22.3.4 MDIO timing relationship to MDC

MDIO (Management Data Input/Output) is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the PHY. When the STA sources the MDIO signal, the STA shall provide a

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minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 22–18, measured at the MII connector.

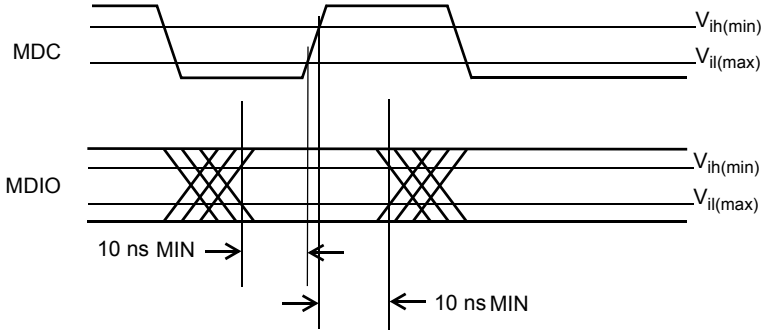


Figure 22–18—MDIO sourced by STA

When the MDIO signal is sourced by the PHY, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the PHY, as measured at the MII connector, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 22–19.

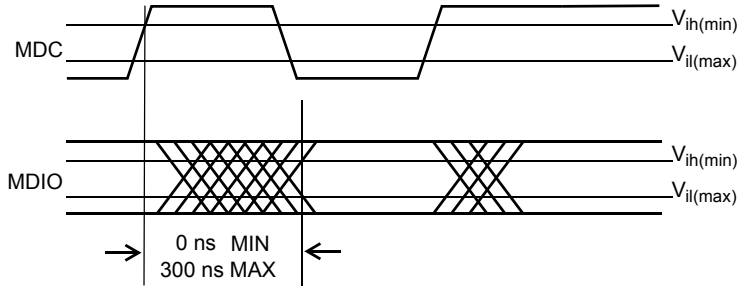


Figure 22–19—MDIO sourced by PHY

22.4 Electrical characteristics

The electrical characteristics of the MII are specified such that the three application environments described in 22.1 are accommodated. The electrical specifications are optimized for the integrated circuit to integrated circuit application environment, but integrated circuit drivers and receivers that are implemented in compliance with the specification will also support the mother board to daughter board and short cable application environments, provided those environments are constrained to the limits specified in this clause.

NOTE—The specifications for the driver and receiver characteristics can be met with TTL compatible input and output buffers implemented in a digital CMOS ASIC process.

22.4.1 Signal levels

The MII uses TTL signal levels, which are compatible with devices operating at a nominal supply voltage of either 5.0 V or 3.3 V.

NOTE—Care should be taken to ensure that all MII receivers can tolerate dc input potentials from 0.00 V to 5.50 V, referenced to the COMMON signal, and transient input potentials as high as 7.3 V, or as low as –1.8 V, referenced to the COMMON signal, which can occur when MII signals change state. The transient duration will not exceed 15 ns. The dc

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source impedance will be no less than $R_{oh(min)}$. The transient source impedance will be no less than ($68 \times 0.85 = 57.8\ \Omega$) .

22.4.2 Signal paths

MII signals can be divided into two groups: signals that go between the STA and the PHY, and signals that go between the Reconciliation sublayer and the PHY.

Signals between the STA and the PHY may connect to one or more PHYs. When a signal goes between the STA and a single PHY, the signal's path is a point-to-point transmission path. When a signal goes between the STA and multiple PHYs, the signal's transmission path has drivers and receivers attached in any order along the length of the path and is not considered a point-to-point transmission path.

Signals between the Reconciliation sublayer and the PHY may also connect to one or more PHYs. However, the transmission path of each of these signals shall be either a point-to-point transmission path or a sequence of point-to-point transmission paths connected in series.

All connections to a point-to-point transmission path are at the path ends. The simplest point-to-point transmission path has a driver at one end and a receiver at the other. Point-to-point transmission paths can also have more than one driver and more than one receiver if the drivers and receivers are lumped at the ends of the path, and if the maximum propagation delay between the drivers and receivers at a given end of the path is a very small fraction of the 10%–90% rise/fall time for signals driven onto the path.

The MII shall use unbalanced signal transmission paths. The characteristic impedance Z_o of transmission paths is not specified for electrically short paths where transmission line reflections can be safely ignored.

The characteristic impedance Z_o of electrically long transmission paths or path segments shall be $68\ \Omega \pm 15\%$.

The output impedance of the driver shall be used to control transmission line reflections on all electrically long point-to-point signal paths.

NOTE—In the context of this clause, a transmission path whose round-trip propagation delay is less than half of the 10%–90% rise/fall time of signals driven onto the path is considered an electrically short transmission path.

22.4.3 Driver characteristics

The driver characteristics defined in this clause apply to all MII signal drivers. The driver characteristics are specified in terms of both their ac and dc characteristics.

NOTE—Rail-to-rail drivers that comply with the driver output V-I diagrams in Annex 22B will meet the following ac and dc characteristics.

22.4.3.1 DC characteristics

The high (one) logic level output potential V_{oh} shall be no less than 2.40 V at an output current I_{oh} of –4.0 mA. The low (zero) logic level output potential V_{ol} shall not be greater than 0.40 V at an output current I_{ol} of 4.0 mA.

22.4.3.2 AC characteristics

Drivers must also meet certain ac specifications in order to ensure adequate signal quality for electrically long point-to-point transmission paths. The ac specifications shall guarantee the following performance requirements.

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The initial incident potential change arriving at the receiving end of a point-to-point MII signal path plus its reflection from the receiving end of the path must switch the receiver input potential monotonically from a valid high (one) level to $V_{il} \leq V_{il(max)} - 200$ mV, or from a valid low (zero) level to $V_{ih} \geq V_{ih(min)} + 200$ mV.

Subsequent incident potential changes arriving at the receiving end of a point-to-point MII signal path plus their reflections from the receiving end of the path must not cause the receiver input potential to reenter the range $V_{il(max)} - 200\ mV < V_i < V_{ih(min)} + 200$ mV except when switching from one valid logic level to the other. Such subsequent incident potential changes result from a mismatch between the characteristic impedance of the signal path and the driver output impedance.

22.4.4 Receiver characteristics

The receiver characteristics are specified in terms of the threshold levels for the logical high (one) and logical low (zero) states. In addition, receivers must meet the input current and capacitance limits.

22.4.4.1 Voltage thresholds

An input potential V_i of 2.00 V or greater shall be interpreted by the receiver as a logical high (one). Thus, $V_{ih(min)} = 2.00$ V. An input potential V_i of 0.80 V or less shall be interpreted by the receiver as a logical low (zero). Thus, $V_{il(max)} = 0.80$ V. The switching region is defined as signal potentials greater than $V_{il(max)}$ and less than $V_{ih(min)}$. When the input signal potential is in the switching region, the receiver output is undefined.

22.4.4.2 Input current

The input current requirements shall be measured at the MII connector and shall be referenced to the +5 V supply and COMMON pins of the connector. The input current requirements shall be met across the full range of supply voltage specified in 22.5.1.

The bidirectional signal MDIO has two sets of input current requirements. The MDIO drivers must be disabled when the input current measurement is made.

The input current characteristics for all MII signals shall fall within the limits specified in Table 22–13.

NOTE—These limits for dc input current allow the use of weak resistive pull-ups or pull-downs on the input of each MII signal. They allow the use of weak resistive pull-downs on the signals other than COL, MDC, and MDIO. They allow the use of a weak resistive pull-up on the signal COL. They allow the use of a resistive pull-down of 2 kΩ ± 5% on the MDIO signal in the STA. They require a resistive pull-up of 1.5 kΩ ± 5% on the MDIO signal in a PHY that is attached to the MII via the mechanical interface specified in 22.6. The limits on MDC and MDIO allow the signals to be "bused" to several PHYs that are contained on the same printed circuit assembly, with a single PHY attached via the MII connector.

22.4.4.3 Input capacitance

For all signals other than MDIO, the receiver input capacitance C_i shall not exceed 8 pF.

For the MDIO signal, the transceiver input capacitance shall not exceed 10 pF.

22.4.5 Cable characteristics

The MII cable consists of a bundle of individual twisted pairs of conductors with an overall shield covering this bundle. Each twisted pair shall be composed of a conductor for an individual signal and a return path dedicated to that signal.

NOTE—It is recommended that the signals RX_CLK and TX_CLK be connected to pairs that are located in the center of the cable bundle.

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Table 22–13—Input current limits

Symbol	Parameter	Condition	Signal(s)	Min (µA)	Max (µA)
I_{ih}	Input high current	V_i=5.25 V	All except COL, MDC, MDIO[a]	—	200
			COL[b]	—	20
			MDC[c]	—	20
			MDIO[d]	—	3000
			MDIO[e]	—	20
I_{il}	Input low current	V_i=0.00 V	All except COL, MDC, MDIO[a]	–20	—
			COL[b]	–200	—
			MDC[c]	–20	—
			MDIO[d]	–180	—
			MDIO[e]	–3800	—
I_{iq}	Input quiescent current	V_i=2.4 V	MDIO[d]	—	1450
			MDIO[e]	–1450	—

[a]Measured at input of Reconciliation sublayer for CRS, RXD<3:0>, RX_CLK, RX_DV, RX_ER, and TX_CLK. Measured at inputs of PHY for TXD<3:0>, TX_EN, and TX_ER.
[b]Measured at input of Reconciliation sublayer.
[c]Measured at input of PHY.
[d]Measured at input of STA.
[e]Measured at input of PHY, which can be attached via the mechanical interface specified in 22.6.

22.4.5.1 Conductor size

The specifications for dc resistance in 22.4.5.6 and characteristic impedance in 22.4.5.2 assume a conductor size of 0.32 mm (28 AWG).

22.4.5.2 Characteristic impedance

The single-ended characteristic impedance of each twisted pair shall be 68 Ω ± 10%. The characteristic impedance measurement shall be performed with the return conductor connected to the cable's overall shield at both ends of the cable.

22.4.5.3 Delay

The propagation delay for each twisted pair, measured from the MII connector to the PHY, shall not exceed 2.5 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable. The propagation delay shall be measured at a frequency of 25 MHz.

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22.4.5.4 Delay variation

The variation in the propagation delay of the twisted pairs in a given cable bundle, measured from the MII connector to the PHY, shall not exceed 0.1 ns. The measurement shall be made with the return conductor of the pair connected to the cable's overall shield at both ends of the cable.

22.4.5.5 Shielding

The overall shield must provide sufficient shielding to meet the requirements of protection against electromagnetic interference.

The overall shield shall be terminated to the connector shell as defined in 22.6.2. A double shield, consisting of both braid and foil shielding, is strongly recommended.

22.4.5.6 DC resistance

The dc resistance of each conductor in the cable, including the contact resistance of the connector, shall not exceed 150 mΩ measured from the MII connector to the remote PHY.

22.4.6 Hot insertion and removal

The insertion or removal of a PHY from the MII with power applied (hot insertion or removal) shall not damage the devices on either side of the MII. In order to prevent contention between multiple output buffers driving the PHY output signals, a PHY that is attached to the MII via the mechanical interface defined in 22.6 shall ensure that its output buffers present a high impedance to the MII during the insertion process, and shall ensure that this condition persists until the output buffers are enabled via the Isolate control bit in the management interface basic register.

NOTE—The act of inserting or removing a PHY from an operational system may cause the loss of one or more packets or management frames that may be in transit across the MII or MDI.

22.5 Power supply

When the mechanical interface defined in 22.6 is used to interconnect printed circuit subassemblies, the Reconciliation sublayer shall provide a regulated power supply for use by the PHY.

The power supply shall use the following MII lines:

+5 V: The plus voltage output to the PHY.
COMMON: The return to the power supply.

22.5.1 Supply voltage

The regulated supply voltage to the PHY shall be 5 Vdc ± 5% at the MII connector with respect to the COMMON circuit at the MII over the range of load current from 0 mA to 750 mA. The method of over/under voltage protection is not specified; however, under no conditions of operation shall the source apply a voltage to the +5 V circuit of less than 0 V or greater than +5.25 Vdc.

Implementations that provide a conversion from the MII to the Attachment Unit Interface (AUI) to support connection to 10 Mb/s Medium Attachment Units (MAUs) will require a supplemental power source in order to meet the AUI power supply requirements specified in 7.5.2.5.

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22.5.2 Load current

The sum of the currents carried on the +5 V lines shall not exceed 750 mA, measured at the MII connector. The surge current drawn by the PHY shall not exceed 5 A peak for a period of 10 ms. The PHY shall be capable of powering up from 750 mA current limited sources.

22.5.3 Short-circuit protection

Adequate provisions shall be made to ensure protection of the power supply from overload conditions, including a short circuit between the +5 V lines and the COMMON lines.

22.6 Mechanical characteristics

When the MII is used to interconnect two printed circuit assemblies via a short length of cable, the cable shall be connected to the circuit assembly that implements the Reconciliation sublayer by means of the mechanical interface defined in this clause.

22.6.1 Definition of mechanical interface

A 40-pole connector having the mechanical mateability dimensions as specified in IEC 61076-3-101:1997 shall be used for the MII connector. The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall have a female connector with screw locks, and the mating cable shall have a male connector with jack screws.

No requirements are imposed on the mechanical interface used to connect the MII cable to the PHY circuit assembly when the MII cable is permanently attached to the PHY circuit assembly, as shown in Figure 22–2. If the cable is not permanently attached to the PHY circuit assembly, then a male connector with jack screws shall be used for the MII connector at the PHY circuit assembly.

NOTE—All MII conformance tests are performed at the mating surfaces of the MII connector at the Reconciliation sublayer end of the cable. If a PHY circuit assembly does not have a permanently attached cable, the vendor must ensure that all of the requirements of this clause are also met when a cable that meets the requirements of 22.4.5 is used to attach the PHY circuit assembly to the circuit assembly that contains the Reconciliation sublayer.

22.6.2 Shielding effectiveness and transfer impedance

The shells of these connectors shall be plated with conductive material to ensure the integrity of the current path from the cable shield to the chassis. The transfer impedance of this path shall not exceed the values listed in Table 22–14, after a minimum of 500 cycles of mating and unmating. The shield transfer impedance values listed in the table are measured in accordance with the procedure defined in Annex L of IEEE Std 1394-1995 [B45].[2]

All additions to provide for female shell to male shell conductivity shall be on the shell of the connector with male contacts. There should be multiple contact points around the sides of this shell to provide for shield continuity.

[2]The numbers in brackets correspond to those of the bibliography in Annex A in Section One of this standard.

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Table 22–14—Transfer impedance performance requirements

Frequency	Value
30 MHz	–26 dBΩ
159 MHz	–13 dBΩ
500 MHz	–5 dBΩ

22.6.3 Connector pin numbering

Figure 22–20 depicts the MII connector pin numbering, as seen looking into the contacts of a female connector from the mating side.

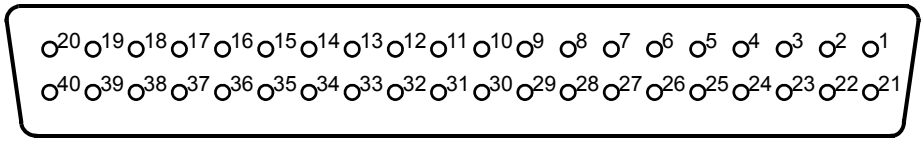


Figure 22–20—MII connector pin numbering

22.6.4 Clearance dimensions

The circuit assembly that contains the MAC sublayer and Reconciliation sublayer shall provide sufficient clearance around the MII connector to allow the attachment of cables that use die cast metal backshells and overmold assemblies. This requirement may be met by providing the clearance dimensions shown in Figure 22–21.

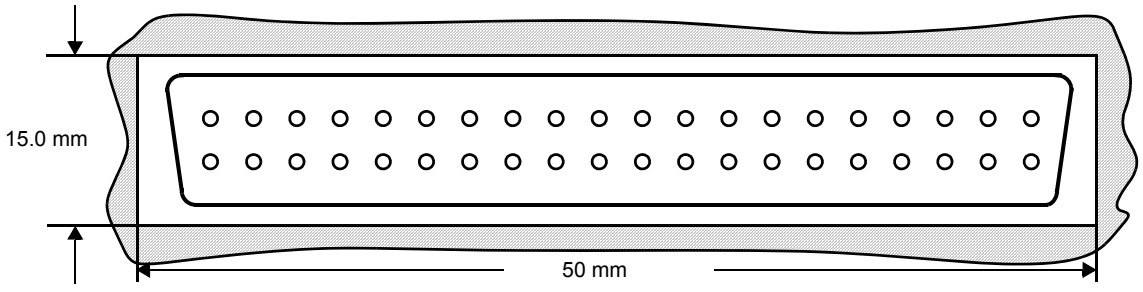


Figure 22–21—MII connector clearance dimensions

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22.6.5 Contact assignments

Table 22–15 shows the assignment of circuits to connector contacts.

Table 22–15—MII connector contact assignments

Contact	Signal name	Contact	Signal name
1	+5 V	21	+5 V
2	MDIO	22	COMMON
3	MDC	23	COMMON
4	RXD<3>	24	COMMON
5	RXD<2>	25	COMMON
6	RXD<1>	26	COMMON
7	RXD<0>	27	COMMON
8	RX_DV	28	COMMON
9	RX_CLK	29	COMMON
10	RX_ER	30	COMMON
11	TX_ER	31	COMMON
12	TX_CLK	32	COMMON
13	TX_EN	33	COMMON
14	TXD<0>	34	COMMON
15	TXD<1>	35	COMMON
16	TXD<2>	36	COMMON
17	TXD<3>	37	COMMON
18	COL	38	COMMON
19	CRS	39	COMMON
20	+5 V	40	+5 V

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22.7 LPI assertion and detection

Certain PHYs support Energy-Efficient Ethernet (EEF) (see Clause 78). PHYs with EEE capability support LPI assertion and detection. LPI operation and the LPI client are described in 78.1. LPI signaling allows the LPI client to signal to the PHY and to the link partner that an interruption in the data stream is expected and components may use this information to enter power-saving modes that require additional time to resume normal operation. Similarly, it allows the LPI client to understand that the link partner has sent such an indication. LPI signaling on the MII is specified only for 100 Mb/s operation.

The LPI assertion and detection mechanism fits conceptually between the PLS Service Primitives and the MII signals as shown in Figure 22–22.

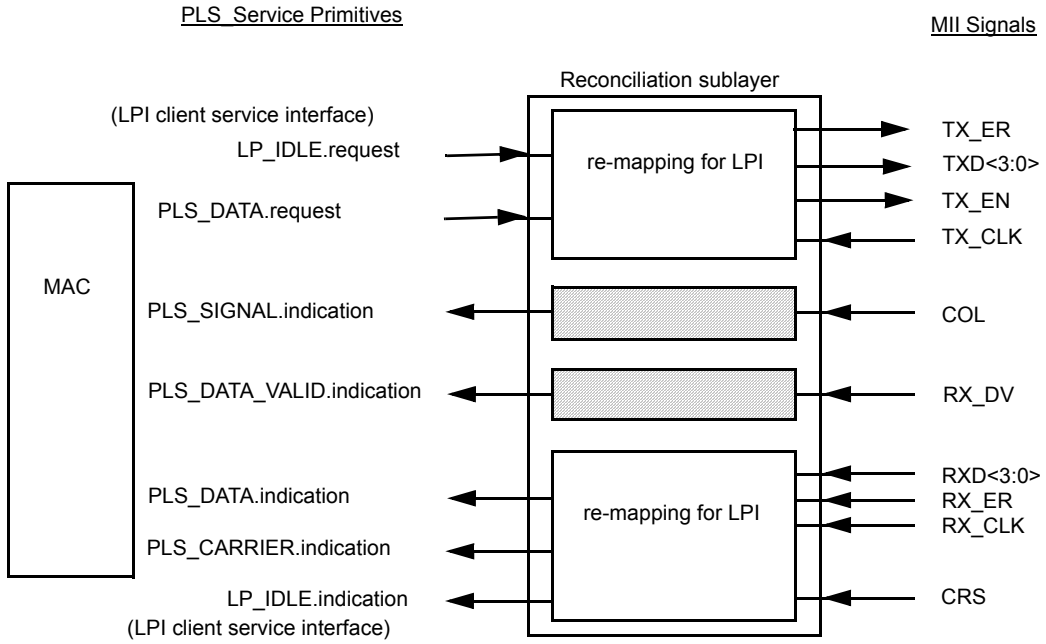


Figure 22–22—LPI assertion and detection mechanism

The definition of TX_EN, TX_ER and TXD<3:0> is derived from the state of PLS_DATA.request (22.2.1.1), except when it is overridden by an assertion of LP_IDLE.request. Similarly, RX_ER and RXD<3:0> are mapped to PLS_DATA.indication except when LP_IDLE is detected. CRS is mapped to PLS_CARRIER.indication except when LP_IDLE.request is asserted or the wake timer has yet to expire. The timing of PLS_CARRIER.indication when used for the LPI function is controlled by the LPI transmit state diagram.

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22.7.1 LPI messages

LP_IDLE.indication(LPI_INDICATION)

A primitive that indicates to the LPI client that the PHY has detected the assertion or deassertion of LPI from the link partner.

Values:DEASSERT: The link partner is operating with normal interframe behavior (default).

ASSERT: The link partner has asserted LPI.

LP_IDLE.request(LPI_REQUEST)

The LPI_REQUEST parameter can take one of two values: ASSERT or DEASSERT. ASSERT initiates the signaling of LPI to the link partner. DEASSERT stops the signaling of LPI to the link partner. The effect of receipt of this primitive is undefined if link_status is not OK (see 28.2.6.1.1) or if LPI_REQUEST=ASSERT within 1 second of the change of link_status to OK.

22.7.2 Transmit LPI state diagram

The operation of LPI in the PHY requires that the MAC does not send valid data for a time after LPI has been deasserted as governed by resolved Transmit T_{w_sys} defined in 78.4.2.3.

This wake up time is enforced by the transmit LPI state diagram and the rules mapping CARRIER_SENSE.indication defined in 22.2.1.3. The implementation shall conform to the behavior described by the transmit LPI state diagram shown in Figure 22–23.

22.7.2.1 Conventions

The notation used in the state diagram follows the conventions of 21.5.

22.7.2.2 Variables and counters

The transmit LPI state diagram uses the following variables and counters:

power_on

Condition that is true until such time as the power supply for the device that contains the RS has reached the operating region.

Values:FALSE: The device is completely powered (default).

TRUE: The device has not been completely powered.

rs_reset

Used by management to control the resetting of the RS.

Values:FALSE: Do not reset the RS (default).

TRUE: Reset the RS.

tw_timer

A timer that counts the time since the deassertion of LPI. The terminal count of the timer shall be the value of the resolved $T_{w\_sys\_tx}$ as defined in 78.2 and 78.4. The minimum value of $T_{w\_sys\_tx}$ shall be 30 μs for 100BASE-TX. Signal tw_timer_done is asserted on reaching its terminal count.

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22.7.2.3 State diagram

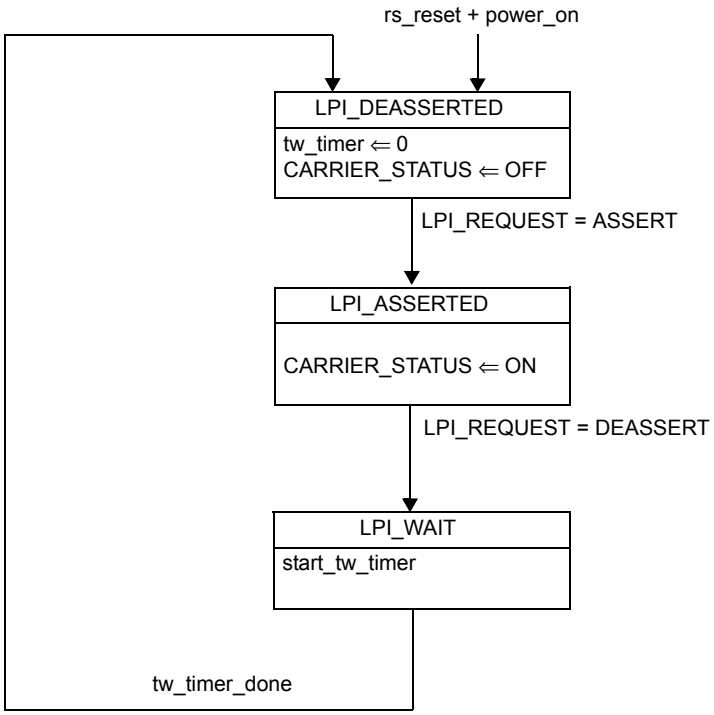


Figure 22–23—Transmit LPI state diagram

22.7.3 Considerations for transmit system behavior

The transmit system should expect that egress data flow will be halted for at least resolved $T_{w\_sys\_tx}$ (see 78.2) time, in microseconds, after it requests the deassertion of LPI. Buffering and queue management should be designed to accommodate this.

22.7.3.1 Considerations for receive system behavior

The mapping function of the Reconciliation Sublayer shall continue to signal IDLE on PLS_DATA.indicate while it is detecting LP_IDLE on the MII. The receive system should be aware that data frames may arrive at the MII following the deassertion of LPI_INDICATION with a delay corresponding to the link partner's resolved $T_{w\_sys\_rx}$ (as specified in 78.5) time, in microseconds.

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22.8 Protocol implementation conformance statement (PICS) proforma for Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)[3]

22.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

22.8.2 Identification

22.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

22.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 22, Reconciliation Sublayer (RS) and Media Independent Interface (MII)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	No [ ] Yes [ ]

Date of Statement	

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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22.8.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*GM	Implementation of GMII	22.2.4	O		
*MUNI	Implementation of unidirectional PCS	22.2.4	O		
*LPI	Implementation of LPI	22.7	O		

22.8.3 PICS proforma tables for reconciliation sublayer and media independent interface

22.8.3.1 Mapping of PLS service primitives

Item	Feature	Subclause	Status	Support	Value/Comment
PL1	Response to RX_ER	22.2.1.5	M		Must produce FrameCheckError at MAC

22.8.3.2 MII signal functional specifications

Item	Feature	Subclause	Status	Support	Value/Comment
SF1	TX_CLK frequency	22.2.2.1	M		25% of transmitted data rate (25 MHz or 2.5 MHz)
SF2	TX_CLK duty cycle	22.2.2.1	M		35% to 65%
SF3	RX_CLK min high/low time	22.2.2.2	M		35% of nominal period
SF4	RX_CLK synchronous to recovered data	22.2.2.2	M		
SF5	RX_CLK frequency	22.2.2.2	M		25% of received data rate (25 MHz or 2.5 MHz)
SF6	RX_CLK duty cycle	22.2.2.2	M		35% to 65%
SF7	RX_CLK source due to loss of signal	22.2.2.2	M		Nominal clock reference (e.g., TX_CLK reference)
SF8	RX_CLK transitions only while RX_DV deasserted	22.2.2.2	M		
SF9	RX_CLK max high/low time following deassertion of RX_DV	22.2.2.2	M		Max 2 times the nominal period
SF10	TX_EN assertion	22.2.2.3	M		On first nibble of preamble
SF11	TX_EN remains asserted	22.2.2.3	M		Stay asserted while all nibbles are transmitted over MII
SF12	TX_EN transitions	22.2.2.3	M		Synchronous with TX_CLK
SF13	TX_EN negation	22.2.2.3	M		Before first TX_CLK after final nibble of frame

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22.8.3.2 MII signal functional specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SF14	TXD<3:0> transitions	22.2.2.4	M		Synchronous with TX_CLK
SF15	TXD<3:0> effect on PHY while TX_EN is deasserted	22.2.2.4	M		No effect
SF16	TX_ER transitions	22.2.2.5	M		Synchronous with TX_CLK
SF17	TX_ER effect on PHY while TX_EN is asserted	22.2.2.5	M		Cause PHY to emit invalid symbol
SF18	TX_ER effect on PHY while operating at 10 Mb/s, or when TX_EN is deasserted	22.2.2.5	M		No effect on PHY
SF19	TX_ER implementation	22.2.2.5	M		At MII of a PHY
SF20	TX_ER pulled down if not actively driven	22.2.2.5	M		At MII of a repeater or MAC/ RS only
SF21	RX_DV transitions	22.2.2.7	M		Synchronous with RX_CLK
SF22	RX_DV assertion	22.2.2.7	M		From first recovered nibble to final nibble of a frame per Figure 22–7
SF23	RX_DV negation	22.2.2.7	M		Before the first RX_CLK follows the final nibble per Figure 22–7
SF24	RXD<3:0> effect on Reconciliation sublayer while RX_DV is deasserted	22.2.2.8	M		No effect
SF25	RX_ER assertion	22.2.2.10	M		By PHY to indicate error
SF26	RX_ER transitions	22.2.2.10	M		Synchronous with RX_CLK
SF27	RX_ER effect on Reconciliation sublayer while RX_DV is deasserted	22.2.2.10	M		No effect
SF28	CRS assertion	22.2.2.11	M		By PHY when either transmit or receive is NON-IDLE

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22.8.3.2 MII signal functional specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SF29	CRS deassertion	22.2.2.11	M		By PHY when both transmit and receive are IDLE
SF30	CRS assertion during collision	22.2.2.11	M		Remain asserted throughout
SF31	COL assertion	22.2.2.12	M		By PHY upon detection of collision on medium
SF32	COL remains asserted while collision persists	22.2.2.12	M		
SF33	COL response to SQE	22.2.2.12	M		Assertion by PHY
SF34	MDC min high/low time	22.2.2.13	M		160 ns
SF35	MDC min period	22.2.2.13	M		400 ns
SF36	MDIO uses three-state drivers	22.2.2.14	M		
SF37	PHY pull-up on MDIO	22.2.2.14	M		1.5 kΩ ± 5% (to +5 V)
SF38	STA pull-down on MDIO	22.2.2.14	M		2 kΩ ± 5% (to 0 V)

22.8.3.3 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
L1	Transitions to LPI_ASSERTED and LPI_DEASSERTED reflected in CARRIER_STATUS	22.2.1.3.3	LPI:M		
L2	RX_CLK max high/low time while the PHY is asserting LPI	22.2.2.2	LPI:M		Max 2 times the nominal period
L3	Assertion of LPI as defined in Table 22–1	22.2.2.4	LPI:M		
L4	RX_CLK stoppable during LPI	22.2.2.9	LPI:O		At least 9 cycles after LPI assertion
L5	RX_CLK restart before LPI deasserted	22.2.2.9	LPI:O		At least 1 positive edge before LPI deassertion
L6	Behavior matches the transmit LPI state diagram	22.7.2	LPI:M		
L7	Terminal count for tw_timer	22.7.2.2	LPI:M		Based on resolved $T_{w\_sys\_tx}$
L8	RS continues to indicate IDLE on PLS_DATA.indicate	22.7.3.1	LPI:M		

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22.8.3.4 Frame structure

Item	Feature	Subclause	Status	Support	Value/Comment
FS1	Format of transmitted frames	22.2.3	M		Per Figure 22–12
FS2	Nibble transmission order	22.2.3	M		Per Figure 22–13
FS3	Preamble 7 octets long	22.2.3.2.1	M		10101010 10101010 10101010 10101010 10101010 10101010 10101010
FS4	Preamble and SFD transmission	22.2.3.2.1	M		Per Table 22–3
FS5	Preamble and SFD reception	22.2.3.2.2	M		Per Table 22–4, Table 22–5
FS6	N octets transmitted as 2N nibbles	22.2.3.3	M		Per Figure 22–13
FS7	Indication of excess nibbles	22.2.3.5	M		Frame contains non-integer number of octets is received

22.8.3.5 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Incorporate of basic register set	22.2.4	M		Two 16-bit registers as Control register (Register 0) and Status register (Register 1)
MF2	Action on reset	22.2.4.1.1	M		Reset the entire PHY including Control and Status to default value and set bit 0.15 = 1
MF3	Return 1 until reset completed	22.2.4.1.1	M		Yes (when reset is done, 0.15 is self-clearing)
MF4	Reset completes within 0.5 s	22.2.4.1.1	M		
MF5	Loopback mode	22.2.4.1.2	M		Whenever 0.14 is 1
MF6	Receive circuitry isolated from network in loopback mode	22.2.4.1.2	M		
MF7	Effect of assertion of TX_EN in loopback mode	22.2.4.1.2	M		No transmission
MF8	Propagation of data in loopback mode	22.2.4.1.2	M		PHY accepts transmit data and return it as receive data
MF9	Delay from TX_EN to RX_DV in loopback mode	22.2.4.1.2	M		Less than 512 BT
MF10	Behavior of COL in loopback mode	22.2.4.1.2	M		Deasserted (for 0.7 = 0)
MF11	Behavior of COL in loopback mode	22.2.4.1.2	M		If 0.7 = 1, see MF33 and MF34
MF12	Value of speed selection bits	22.2.4.1.3	M		Set to match a valid PHY speed

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF13	Ignore writes to speed selection bits for unsupported speed	22.2.4.1.3	M		
MF14	Auto-Negotiation enable	22.2.4.1.4	M		By setting 0.12 = 1
MF15	Duplex mode, speed selection have no effect when Auto-Negotiation is enabled	22.2.4.1.4	M		If 0.12=1, bits 0.13, 0.8 and 0.6 have no effect on link configuration
MF16	PHY without Auto-Negotiation returns value of zero	22.2.4.1.4	M		Yes (if 1.3=0, then 0.12=0)
MF17	PHY without Auto-Negotiation ignores writes to enable bit	22.2.4.1.4	M		Yes (if 1.3=0, 0.12 always = 0 and cannot be changed)
MF18	Response to management transactions in power down	22.2.4.1.5	M		Remains active
MF19	Spurious signals in power down	22.2.4.1.5	M		None (not allowed)
MF20	TX_CLK and RX_CLK stabilize within 0.5 s	22.2.4.1.5	M		Yes (after both bits 0.11 and 0.10 are cleared to zero)
MF21	PHY Response to input signals while isolated	22.2.4.1.6	M		NONE
MF22	High impedance on PHY output signals while isolated	22.2.4.1.6	M		Yes (TX_CLK, RX_CLK, RX_DV, RX_ER, RXD bundle, COL, and CRS)
MF23	Response to management transactions while isolated	22.2.4.1.6	M		Remains active
MF24	Default value of isolate	22.2.4.1.6	M		0.10 =1
MF25	PHY without Auto-Negotiation returns value of zero	22.2.4.1.7	M		0.9 = 0 if 1.3 = 0 or 0.12 = 0
MF26	PHY without Auto-Negotiation ignores writes to restart bit	22.2.4.1.7	M		0.9 = 0, cannot be changed if 1.3 = 0 or 0.12 = 0
MF27	Restart Auto-Negotiation	22.2.4.1.7	M		When 0.9 = 1 if 0.12 = 1 and 1.3 = 1
MF28	Return 1 until Auto-Negotiation initiated	22.2.4.1.7	M		0.9 is self-clearing to 0
MF29	Auto-Negotiation not effected by clearing bit	22.2.4.1.7	M		
MF30	Value of duplex mode bit for PHYs with one duplex mode	22.2.4.1.8	M		Set 0.8 to match the correct PHY duplex mode
MF31	PHY with one duplex mode ignores writes to duplex bit	22.2.4.1.8	M		Yes (0.8 remains unchanged)

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF32	Loopback not affected by duplex mode	22.2.4.1.8	M		Yes (0.8 has no effect on PHY when 0.14 = 1)
MF33	Assertion of COL in collision test mode	22.2.4.1.9	M		Within 512 BT after TX_EN is asserted
MF34	deassertion of COL in collision test mode	22.2.4.1.9	M		After TX_EN is deasserted within: MII = 4 BT, GMII = 16 BT
MF35	Reserved bits written as zero	22.2.4.1.11	M		
MF36	Reserved bits ignored when read	22.2.4.1.11	M		
MF37	PHY returns 0 in reserved bits	22.2.4.1.11	M		
MF38	PHY without unidirectional ability	22.2.4.1.12	M		PHY returns a value of 0 in 0.5 if 1.7=0
MF39	PHY without unidirectional ability	22.2.4.1.12	M		PHY always maintains a value of 0 in 0.5 if 1.7=0
MF40	Unidirectional enable	22.2.4.1.12	MUNI:M		By setting 0.12 = 0, 0.8 = 1 and 0.5 = 1
MF41	Unidirectional disable	22.2.4.1.12	MUNI:M		By setting 0.12 = 1, 0.8 = 0 or 0.5 = 0
MF42	Ignore bit 0.5	22.2.4.1.12	MUNI:M		Ignore 0.5 when 0.12 = 1 or 0.8 = 0
MF43	Enable unidirectional mode	22.2.4.1.12	MUNI:M		Enable only when OAM sublayer is enabled or when part of 1000BASE-PX-D PHY
MF44	Disable unidirectional mode	22.2.4.1.12	MUNI:M		Unidirectional mode is disabled before disabling OAM sublayer when not part of 1000BASE-PX-D PHY
MF45	Unidirectional ability	22.2.4.2.8	M		Bit 1.7 = 0 for all PHYs except those using 66.1 and 66.2
MF46	Effect of write on status register	22.2.4.2	M		No effect
MF47	Reserved bits ignored when read	22.2.4.2.8	M		
MF48	PHY returns 0 in reserved bits	22.2.4.2.8	M		
MF49	PHY returns 0 if Auto-Negotiation disabled	22.2.4.2.10	M		Yes (1.5 = 0 when 0.12 = 0)
MF50	PHY returns 0 if it lacks ability to perform Auto-Negotiation	22.2.4.2.10	M		Yes (1.5 = 0 when 1.3 = 0)
MF51	Remote fault has latching function	22.2.4.2.11	M		Yes (once set will remain set until cleared)
MF52	Remote fault cleared on read	22.2.4.2.11	M		Yes

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF53	Remote fault cleared on reset	22.2.4.2.11	M		Yes (when 0.15 = 1)
MF54	PHY without remote fault returns value of zero	22.2.4.2.11	M		Yes (1.4 always 0)
MF55	Link status has latching function	22.2.4.2.13	M		Yes (once cleared by link failure will remain cleared until read by MII)
MF56	Jabber detect has latching function	22.2.4.2.14	M		Yes (once set will remain set until cleared)
MF57	Jabber detect cleared on read	22.2.4.2.14	M		
MF58	Jabber detect cleared on reset	22.2.4.2.14	M		
MF59	All PHYs operating at rates of 100 Mb/s or above return 0 for jabber detect	22.2.4.2.14	M		Yes (1.1 always = 0 for all PHYs operating at rates of 100 Mb/s or above)
MF60	MDIO not driven if register read is unimplemented	22.2.4.3	M		Yes (MDIO remain high impedance)
MF61	Write has no effect if register written is unimplemented	22.2.4.3	M		
MF62	Registers 2 and 3 constitute unique identifier for PHY type	22.2.4.3.1	M		
MF63	MSB of PHY identifier is 2.15	22.2.4.3.1	M		
MF64	LSB of PHY identifier is 3.0	22.2.4.3.1	M		
MF65	Composition of PHY identifier	22.2.4.3.1	O		22-bit OUI, 6-bit model, 4-bit version per Figure 22–14
MF66	Format of management frames	22.2.4.5	M		Per Table 22–11
MF67	Idle condition on MDIO	22.2.4.5.1	M		High impedance state
MF68	MDIO preamble sent by STA	22.2.4.5.2	M		32 contiguous logic one bits
MF69	MDIO preamble observed by PHY	22.2.4.5.2	M		32 contiguous logic one bits
MF70	Assignment of PHYAD 0	22.2.4.5.5	M		Address of PHY attached via Mechanical Interface
MF71	Assignment of REGAD 0	22.2.4.5.6	M		MII control register address
MF72	Assignment of REGAD 1	22.2.4.5.6	M		MII status register address
MF73	High impedance during first bit time of turnaround in read transaction	22.2.4.5.7	M		

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22.8.3.5 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF74	PHY drives zero during second bit time of turnaround in read transaction	22.2.4.5.7	M		
MF75	STA drives MDIO during turnaround in write transaction	22.2.4.5.7	M		
MF76	First data bit transmitted	22.2.4.5.8	M		Bit 15 of the register being addressed
MF77	Incorporate Extended Status register	22.2.4	GM:M		16-bit register Extended Status register (Register 15)
MF78	Reserved bits written as zero	22.2.4.2.8	GM:M		
MF79	Extended Status	22.2.4.2.16	GM:M		Yes (1.8 always = 1 for 1000 Mb/s operation)
MF80	Write to Extended Status register	22.2.4.4	GM:M		No effect
MF81	Reserved bits written as zero	22.2.4.4.5	GM:M		
MF82	Reserved bits ignored when read	22.2.4.4.5	GM:M		
MF83	PHY returns 0 in reserved bits	22.2.4.4.5	GM:M		

22.8.3.6 Signal timing characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
ST1	Timing characteristics measured in accordance with Annex 22C	22.3	M		
ST2	Transmit signal clock to output delay	22.3.1	M		Min = 0 ns; Max = 25 ns per Figure 22–16
ST3	Receive signal setup time	22.3.2	M		Min = 10 ns per Figure 22–17
ST4	Receive signal hold time	22.3.2	M		Min = 10 ns per Figure 22–17
ST5	MDIO setup and hold time	22.3.4	M		Setup min = 10 ns; Hold min = 10 ns per Figure 22–18
ST6	MDIO clock to output delay	22.3.4	M		Min = 0 ns; Max = 300 ns per Figure 22–19

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22.8.3.7 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
EC1	Signal paths are either point to point, or a sequence of point-to-point transmission paths	22.4.2	M		
EC2	MII uses unbalanced signal transmission paths	22.4.2	M		
EC3	Characteristic impedance of electrically long paths	22.4.2	M		68 Ω ± 15%
EC4	Output impedance of driver used to control reflections	22.4.2	M		On all electrically long point to point signal paths
EC5	V_{oh}	22.4.3.1	M		≥ 2.4 V (I_{oh} = –4 mA)
EC6	V_{ol}	22.4.3.1	M		≤ 0.4 V (I_{ol} = 4 mA)
EC7	Performance requirements to be guaranteed by ac specifications	22.4.3.2	M		Min switching potential change (including its reflection) ≥ 1.8 V
EC8	$V_{ih(min)}$	22.4.4.1	M		2 V
EC9	$V_{il(max)}$	22.4.4.1	M		0.8 V
EC10	Input current measurement point	22.4.4.2	M		At MII connector
EC11	Input current reference potentials	22.4.4.2	M		Reference to MII connector +5 V and COMMON pins
EC12	Input current reference potential range	22.4.4.2	M		0 V to 5.25 V
EC13	Input current limits	22.4.4.2	M		Per Table 22–12
EC14	Input capacitance for signals other than MDIO	22.4.4.3	M		≤ 8 pF
EC15	Input capacitance for MDIO	22.4.4.3	M		≤ 10 pF
EC16	Twisted-pair composition	22.4.5	M		Conductor for each signal with dedicated return path
EC17	Single-ended characteristic impedance	22.4.5.2	M		68 Ω ± 10%
EC18	Characteristic impedance measurement method	22.4.5.2	M		With return conductor connected to cable shield

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22.8.3.7 Electrical characteristics *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
EC19	Twisted-pair propagation delay	22.4.5.3	M		≤ 2.5 ns
EC20	Twisted-pair propagation delay measurement method	22.4.5.3	M		With return conductor connected to cable shield
EC21	Twisted-pair propagation delay measurement frequency	22.4.5.3	M		25 MHz
EC22	Twisted-pair propagation delay variation	22.4.5.4	M		≤ 0.1 ns
EC23	Twisted-pair propagation delay variation measurement method	22.4.5.4	M		With return conductor connected to cable shield
EC24	Cable shield termination	22.4.5.5	M		To the connector shell
EC25	Cable conductor DC resistance	22.4.5.6	M		≤ 150 mΩ
EC26	Effect of hot insertion/removal	22.4.6	M		Causes no damage
EC27	State of PHY output buffers during hot insertion	22.4.6	M		High impedance
EC28	State of PHY output buffers after hot insertion	22.4.6	M		High impedance until enabled via Isolate bit

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22.8.3.8 Power supply

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Regulated power supply provided	22.5	M		To PHY by Reconciliation sublayer
PS2	Power supply lines	22.5	M		+5 V and COMMON (return of +5 V)
PS3	Regulated supply voltage limits	22.5.1	M		5 Vdc ± 5%
PS4	Over/under voltage limits	22.5.1	M		Over limit = 5.25 Vdc Under limit = 0 V
PS5	Load current limit	22.5.2	M		750 mA
PS6	Surge current limit	22.5.2	M		≤ 5 A peak for 10 ms
PS7	PHY can power up from current limited source	22.5.2	M		From 750 mA current limited source
PS8	Short-circuit protection	22.5.2	M		When +5 V and COMMON are shorted

22.8.3.9 Mechanical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
*MC1	Use of Mechanical Interface	22.6	O		Optional
MC2	Connector reference standard	22.6.1	MC1:M		IEC 61076-3-101:1997
MC3	Use of female connector	22.6.1	MC1:M		At MAC/RS side
MC4	Use of male connector	22.6.1	MC1:M		At PHY mating cable side
MC5	Connector shell plating	22.6.2	MC1:M		Use conductive material
MC6	Shield transfer impedance	22.6.2	MC1:M		After 500 cycles of mating/ unmating, per Table 22–13
MC7	Additions to provide for female shell to male shell conductivity	22.6.2	MC1:M		On shell of conductor with male contacts
MC8	Clearance dimensions	22.6.4	MC1:M		15 mm × 50 mm, per Figure 22–21

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23. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

NOTE—This PHY is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

23.1 Overview

The 100BASE-T4 PCS, PMA, and baseband medium specifications are aimed at users who want 100 Mb/s performance, but would like to retain the benefits of using voice-grade twisted-pair cable. 100BASE-T4 signaling requires four pairs of Category 3 or better cable, installed according to ISO/IEC 11801: 1995, as specified in 23.6. This type of cable, and the connectors used with it, are simple to install and reconfigure. 100BASE-T4 does not transmit a continuous signal between packets, which makes it useful in battery powered applications. The 100BASE-T4 PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications.

23.1.1 Scope

This clause defines the type 100BASE-T4 Physical Coding Sublayer (PCS), type 100BASE-T4 Physical Medium Attachment (PMA) sublayer, and type 100BASE-T4 Medium Dependent Interface (MDI). Together, the PCS and PMA layers comprise a 100BASE-T4 Physical Layer (PHY). Provided in this document are full functional, electrical, and mechanical specifications for the type 100BASE-T4 PCS, PMA, and MDI. This clause also specifies the baseband medium used with 100BASE-T4.

23.1.2 Objectives

The following are the objectives of 100BASE-T4:

a) To support the CSMA/CD MAC in the half duplex mode of operation.
b) To support the 100BASE-T MII, Repeater, and optional Auto-Negotiation.
c) To provide 100 Mb/s data rate at the MII.
d) To provide for operating over twisted pairs of Category 3, 4, or 5 cable, installed as horizontal runs in accordance with ISO/IEC 11801: 1995, as specified in 23.6, at distances up to 100 m (328 ft).
e) To allow for a nominal network extent of 200 m, including:
    1) Unshielded twisted-pair links of 100 m.
    2) Two-repeater networks of approximately a 200 m span.
f) To provide a communication channel with a mean ternary symbol error ratio, at the PMA service interface, of less than one part in 10^8.

23.1.3 Relation of 100BASE-T4 to other standards

Relations between the 100BASE-T4 PHY and the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model are shown in Figure 23–1. The PHY Layers shown in Figure 23–1 connect one Clause 4 Media Access Control (MAC) layer to a Clause 27 repeater. This clause also discusses other variations of the basic configuration shown in Figure 23–1. This whole clause builds on Clause 1 through Clause 4 of this standard.

23.1.4 Summary

The following paragraphs summarize the PCS and PMA clauses of this standard.

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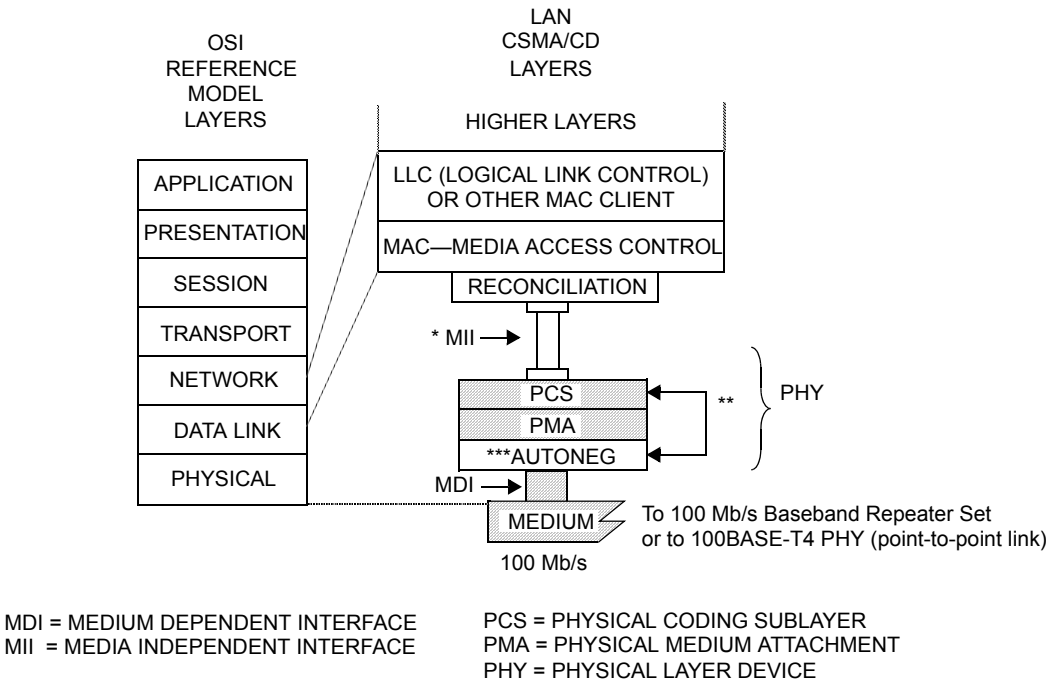


Figure 23–1—Type 100BASE-T4 PHY relationship to the ISO Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

23.1.4.1 Summary of Physical Coding Sublayer (PCS) specification

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in Clause 22, to a Physical Medium Attachment sublayer (PMA).

The PCS Transmit function accepts data nibbles from the MII. The PCS Transmit function encodes these nibbles using an 8B6T coding scheme (to be described) and passes the resulting ternary symbols to the PMA. In the reverse direction, the PMA conveys received ternary symbols to the PCS Receive function. The PCS Receive function decodes them into octets, and then passes the octets one nibble at a time up to the MII. The PCS also contains a PCS Carrier Sense function, a PCS Error Sense function, a PCS Collision Presence function, and a management interface.

Figure 23–2 shows the division of responsibilities between the PCS, PMA, and MDI layers.

Physical level communication between PHY entities takes place over four twisted pairs. This specification permits the use of Category 3, 4, or 5 twisted pairs, installed according to ISO/IEC 11801: 1995, as specified in 23.6. Figure 23–3 shows how the PHY manages the four twisted pairs at its disposal.

The 100BASE-T4 transmission algorithm always leaves one pair open for detecting carrier from the far end (see Figure 23–3). Leaving one pair open for carrier detection in each direction greatly simplifies media access control. All collision detection functions are accomplished using only the unidirectional pairs TX_D1 and RX_D2, in a manner similar to 10BASE-T. This collision detection strategy leaves three pairs in each direction free for data transmission, which uses an 8B6T block code, schematically represented in Figure 23–4.

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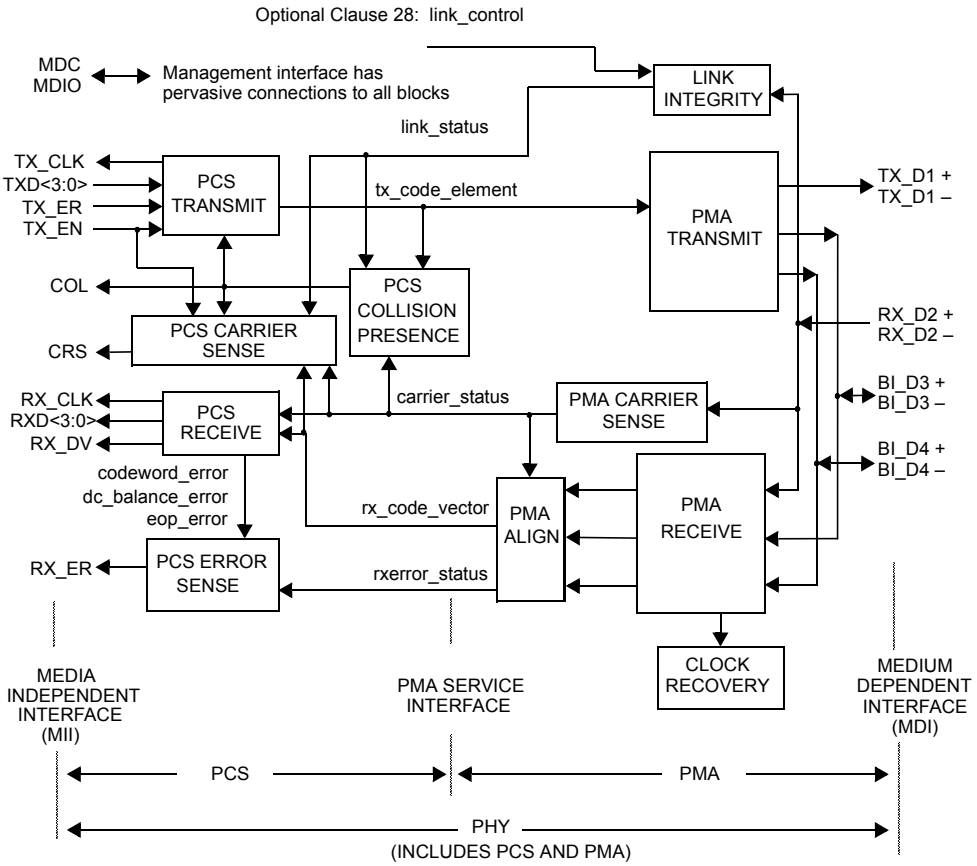


Figure 23–2—Division of responsibilities between 100BASE-T4 PCS and PMA

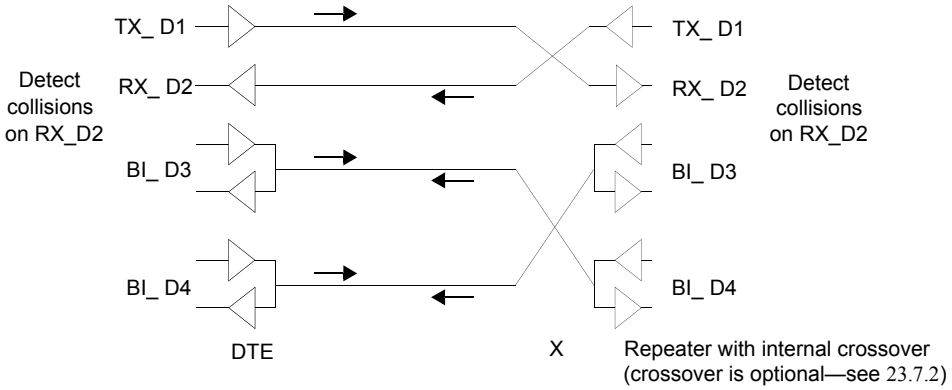


Figure 23–3—Use of wire pairs

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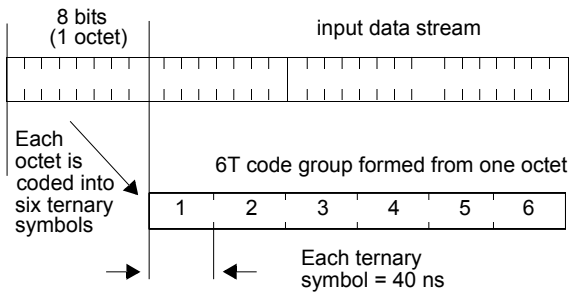


Figure 23–4—8B6T coding

8B6T coding, as used with 100BASE-T4 signaling, maps data octets into ternary symbols. Each octet is mapped to a pattern of 6 ternary symbols, called a 6T code group. The 6T code groups are fanned out to three independent serial channels. The effective data rate carried on each pair is one third of 100 Mb/s, which is 33.333... Mb/s. The ternary symbol transmission rate on each pair is 6/8 times 33.33 Mb/s, or precisely 25.000 MHz.

Refer to Annex 23A for a complete listing of 8B6T codewords.

The PCS functions and state diagrams are specified in 23.2. The PCS electrical interface to the MII conforms to the interface requirements of Clause 21. The PCS interface to the PMA is an abstract message-passing interface specified in 23.3.

23.1.4.2 Summary of physical medium attachment (PMA) specification

The PMA couples messages from the PMA service interface onto the twisted-pair physical medium. The PMA provides communications, at 100 Mb/s, over four pairs of twisted-pair wiring up to 100 m in length.

The PMA Transmit function, shown in Figure 23–2, comprises three independent ternary data transmitters. Upon receipt of a PMA_UNITDATA.request message, the PMA synthesizes one ternary symbol on each of the three output channels (TX_D1, BI_D3, and BI_D4). Each output driver has a *ternary* output, meaning that the output waveform can assume any of three values, corresponding to the transmission of ternary symbols CS0, CS1, or CS-1 (see 23.4.3.1) on each of the twisted pairs.

The PMA Receive function comprises three independent ternary data receivers. The receivers are responsible for acquiring clock, decoding the Start of Stream Delimiter (SSD) on each channel, and providing data to the PCS in the synchronous fashion defined by the PMA_UNITDATA.indication message. The PMA also contains functions for PMA Carrier Sense and Link Integrity.

PMA functions and state diagrams appear in 23.4. PMA electrical specifications appear in 23.5.

23.1.5 Application of 100BASE-T4

23.1.5.1 Compatibility considerations

All implementations of the twisted-pair link shall be compatible at the MDI. The PCS, PMA, and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA (in an application-dependent manner) provided the MDI (and MII, when implemented) specifications are met.

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23.1.5.2 Incorporating the 100BASE-T4 PHY into a DTE

The PCS is required when used with a DTE. The PCS provides functions necessary to the overall system operation (such as 8B6T coding) and cannot be omitted. Refer to Figure 23–1.

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII interface is optional, provided that the observable behavior of the resulting system is identical to a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

23.1.5.3 Use of 100BASE-T4 PHY for point-to-point communication

The 100BASE-T4 PHY, in conjunction with the MAC specified in Clause 1 through Clause 4 (including parameterized values in 4.2.2 to support 100 Mb/s operation), may be used at both ends of a link for point-to-point applications between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an MII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed MII.

23.1.5.4 Support for Auto-Negotiation

The PMA service interface contains primitives used by the Auto-Negotiation algorithm (Clause 28) to automatically select operating modes when connected to a like device.

23.2 PCS functional specifications

The 100BASE-T4 PCS couples a Media Independent Interface (MII), as described in Clause 22, to a 100BASE-T4 Physical Medium Attachment sublayer (PMA).

At its interface with the MII, the PCS communicates via the electrical signals defined in Clause 22.

The interface between PCS and the next lower level (PMA) is an abstract message-passing interface described in 23.3. The physical realization of this interface is left to the implementer, provided the requirements of this standard, where applicable, are met.

23.2.1 PCS functions

The PCS comprises one PCS Reset function and five simultaneous and asynchronous operating functions. The PCS operating functions are PCS Transmit, PCS Receive, PCS Error Sense, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 23–5, shows how the five operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 23–5. The management functions are specified in Clause 30. See also Figure 23–6, which defines the structure of frames passed from PCS to PMA. See also Figure 23–7, which presents a reference model helpful for understanding the definitions of PCS Transmit function state variables ohr1-4 and tsr.

23.2.1.1 PCS Reset function

The PCS Reset function shall be executed any time either of two conditions occur. These two conditions are “power on” and the receipt of a reset request from the management entity. The PCS Reset function initializes

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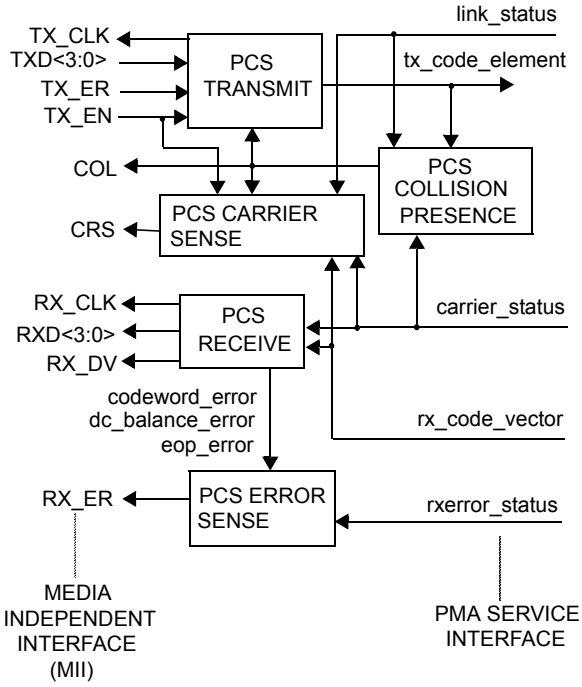


Figure 23–5—PCS reference diagram

all PCS functions. The PCS Reset function sets pcs_reset=ON for the duration of its reset function. All state diagrams take the open-ended pcs_reset branch upon execution of the PCS Reset function. The reference diagrams do not explicitly show the PCS Reset function.

23.2.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 23–8.

The PCS Transmit function receives nibbles from the TXD signals of the MII, assembles pairs of nibbles to form octets, converts the octets into 6T code groups according to the 8B6T code table, and passes the resulting ternary data to the PMA using the PMA_UNITDATA.request message. The state diagram of Figure 23–8 depicts the PCS Transmit function operation. Definitions of state variables tsr, ohr, sosa, sosb, eop1-5, and tx_extend used in that diagram, as well as in the following text, appear in 23.2.4.1. The physical structure represented in Figure 23–7 is not required; it merely serves to explain the meaning of the state diagram variables ohr and tsr in Figure 23–8. Implementers are free to construct any logical devices having functionality identical to that described by this functional description and the PCS Transmit state diagram, Figure 23–8.

PCS Transmit makes use of the tsr and ohr shift registers to manage nibble assembly and ternary symbol transmission. Nibbles from the MII go into tsr, which PCS Transmit reads as octets. PCS Transmit then encodes those octets and writes 6T code groups to the ohr registers. The PMA_UNITDATA.request message passes ternary symbols from the ohr registers to the PMA. In each state diagram block, the ohr loading operations are conducted first, then tx_code_vector is loaded and the state diagram waits 40 ns.

The first 5 octets assembled by the PCS Transmit function are encoded into the sosa codeword and the next 3 octets assembled are encoded into the sosb codeword. This guarantees that every packet begins with a valid preamble pattern. This is accomplished by the definition of tsr. In addition, the PCS Transmit state

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diagram also specifies that at the start of a packet all three output holding registers ohr1, ohr3 and ohr4 will be loaded with the same value (sosa). This produces the ternary symbols labeled P3 and P4 in Figure 23–6.

At the conclusion of the MAC frame, the PCS Transmit function appends eop1-5. This is accomplished by defining a variable tx_extend to stretch the TX_EN signal, and defining tsr during this time to be a sequence of constants that decodes to the proper eop code groups.

The encoding operation shall use the 8B6T code table listed in Annex 23A, and the dc balance encoding rules listed below. Encoding is performed separately for each transmit pair.

23.2.1.2.1 DC balance encoding rules

The encoding operation maintains dc balance on each transmit pair by keeping track of the cumulative weight of all 6T code groups (see *weight of 6T code group*, Annex 23A) transmitted on that pair. For each pair, it initiates the cumulative weight to 0 when the PCS Transmit function is in the AWAITING DATA TO TRANSMIT state. All 6T code groups in the code table have weight 0 or 1. The dc balance algorithm conditionally negates transmitted 6T code groups, so that the code weights transmitted on the line include 0, +1, and –1. This dc balance algorithm ensures that the cumulative weight on each pair at the conclusion of each 6T code group is always either 0 or 1, so only one bit per pair is needed to store the cumulative weight. As used below, the phrase “invert the cumulative weight bit” means “if the cumulative weight bit is zero then set it to one, otherwise set it to zero.”

After encoding any octet, except the constants sosa, sosb, eop1-5 or bad_code, update the cumulative weight bit for the affected pair according to rules a) through c):

a) If the 6T code group weight is 0, do not change the cumulative weight.
b) If the 6T code group weight is 1, and the cumulative weight bit is 0, set the cumulative weight bit to 1.
c) If the 6T code group weight is 1, and the cumulative weight bit is also 1, set the cumulative weight bit to 0, and then algebraically negate all the ternary symbol values in the 6T code group.

After encoding any of the constants sosa, sosb, or bad_code, update the cumulative weight bit for the affected pair according to rule d):

d) Do not change the cumulative weight. Never negate sosa, sosb or bad_code.

After encoding any of the constants eop1-5, update the cumulative weight bit for the affected pair according to rules e) and f):

e) If the cumulative weight is 0, do not change the cumulative weight; algebraically negate all the ternary symbol values in eop1-5.
f) If the cumulative weight is 1, do not change the cumulative weight.

NOTE—The inversion rules for eop1-5 are opposite rule b). That makes eop1-5 look very unlike normal data, increasing the number of errors required to synthesize a false end-of-packet marker.

23.2.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 23–9.

The PCS Receive function accepts ternary symbols from the PMA, communicated via the PMA_UNITDATA.indication message, converts them using 8B6T coding into a nibble-wide format and passes them up to the MII. This function also generates RX_DV. The state diagram of Figure 23–9 depicts the PCS Receive function. Definitions of state variables ih2, ih3, and ih4 used in that diagram, as well as in the following text, appear in 23.2.4.1.

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The last 6 values of the rx_code_vector are available to the decoder. PCS Receive makes use of these stored rx_code_vector values as well as the ih2-4 registers to manage the assembly of ternary symbols into 6T code groups, and the conversion of decoded data octets into nibbles. The last 6 ternary symbols for pair BI_D3 (as extracted from the last 6 values of rx_code_vector) are referred to in the state diagram as BI_D3[0:5]. Other pairs are referenced accordingly.

The PCS Receive state diagram starts the first time the PCS receives a PMA_UNITDATA.indication message with rx_code_vector=DATA (as opposed to IDLE or PREAMBLE). The contents of this first PMA_UNITDATA.indication (DATA) message are specified in 23.4.1.6.

After the sixth PMA_UNITDATA.indication (DATA) message (state DECODE CHANNEL 3), there is enough information to decode the first data octet. The decoded data is transmitted across the MII in two parts, a least significant nibble followed by a most significant nibble (see Clause 22).

During state COLLECT 4TH TERNARY SYMBOL the PCS Receive function raises RX_DV and begins shifting out the nibbles of the 802.3 MAC SFD, least significant nibble first (SFD:LO). The most significant nibble of the 802.3 MAC SFD, called SFD:HI, is sent across the MII during the next state, COLLECT 5TH TERNARY SYMBOL.

Once eop is signaled by the decode operation, the state diagram deasserts RX_DV, preventing the end-of-packet bits from reaching the MII. At any time that RX_DV is deasserted, RXD<3:0> shall be all zeros.

The decode operation shall use the 8B6T code table listed in Annex 23A, and the error-detecting rules listed in 23.2.1.3.1. Decoding and maintenance of the cumulative weight bit is performed separately for each receive pair.

23.2.1.3.1 Error-detecting rules

The decoding operation checks the dc balance on each receive pair by keeping track of the cumulative weight of all 6T code group received on that pair. For each pair, initialize the cumulative weight to 0 when the PCS Receive function is in the AWAITING INPUT state. As in the encoding operation, only one bit per pair is needed to store the cumulative weight.

Before decoding each octet, check the weight of the incoming code group and then apply rules a) through h) in sequence:

a) If the received code group is eop1 (or its negation), set eop=ON. Then check the other pairs for conformance to the end-of-packet rules as follows: Check the last four ternary symbols of the next pair, and the last two ternary symbols from the third pair for exact conformance with the end-of-packet pattern specified by PCS Transmit, including the cumulative weight negation rules. If the received data does not conform, set the internal variable eop_error=ON. Skip the other rules.
b) If the received code group weight is greater than 1 or less than –1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
c) If the received code group weight is zero, use the code table to decode. Do not change the cumulative weight.
d) If the received code group weight is +1, and the cumulative weight bit is 0, use the code table to decode. Invert the cumulative weight bit.
e) If the received code group weight is –1, and the cumulative weight bit is 1, algebraically negate each ternary symbol in the code group and then use the code table to decode. Invert the cumulative weight bit.
f) If the received code group weight is +1 and the cumulative weight bit is 1, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.
g) If the received code group weight is –1 and the cumulative weight bit is 0, set the internal variable dc_balance_error=ON. Decode to all zeros. Do not change the cumulative weight.

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h) If the (possibly negated) code group is not found in the code table, set codeword_error =ON. Decode to all zeros. Do not change the cumulative weight.

The variables dc_balance_error, eop_error and codeword_error shall remain OFF at all times other than those specified in the above error-detecting rules.

The codeword_error=ON indication for a (possibly negated) code group not found in the code table shall set RX_ER during the transfer of both affected data nibbles across the MII.

The dc_balance_error=ON indication for a code group shall set RX_ER during the transfer of both affected data nibbles across the MII.

The eop_error=ON indication shall set RX_ER during the transfer of the last decoded data nibble of the previous octet across the MII. That is at least one RX_CLK period earlier than the requirement for codeword_error and dc_balance_error.

These timing requirements imply consideration of implementation delays not specified in the PCS Receive state diagram.

RX_DV is asserted coincident with the transmission across the MII of valid packet data, including the Clause 4 MAC SFD, but not including the 100BASE-T4 end-of-packet delimiters eop1-5. When a packet is truncated due to early deassertion of carrier_status, an RX_ER indication shall be generated and RX_DV shall be deasserted, halting receive processing. The PCS Receive Function may use any of the existing signals codeword_error, dc_balance_error, or eop_error to accomplish this function.

23.2.1.4 PCS Error Sense function

The PCS Error Sense function performs the task of sending RX_ER to the MII whenever rxerror_status=ERROR is received from the PMA sublayer or when any of the PCS decoding error conditions occur. The PCS Error Sense function shall conform to the PCS Error Sense state diagram in Figure 23–10.

Upon detection of any error, the error sense process shall report RX_ER to the MII before the last nibble of the Clause 4 MAC frame has been passed across the MII. Errors attributable to a particular octet are reported to the MII coincident with the octet in which they occurred.

The timing of rxerror_status shall cause RX_ER to appear on the MII no later than the last nibble of the first data octet in the frame.

23.2.1.5 PCS Carrier Sense function

The PCS Carrier Sense function shall perform the function of controlling the MII signal CRS according to the rules presented in this clause.

While link_status = OK, CRS is asserted whenever rx_crs=ON or TX_EN=1, with timing as specified in 23.11.2, and Table 23-6.

23.2.1.6 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of tx_code_vector≠IDLE and the assertion of carrier_status=ON while link_status=OK. While a PCS collision is detected, the MII signal COL shall be asserted, with timing as specified in 23.11.2 and Table 23–7.

At other times COL shall remain deasserted.

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23.2.2 PCS interfaces

23.2.2.1 PCS–MII interface signals

The following signals are formally defined in 22.2.2. Jabber detection as specified in 22.2.4.2.14 is not required by this standard.

Table 23–1—MII interface signals

Signal name	Meaning
TX_CLK	Transmit Clock
TXD<3:0>	Transmit Data
TX_ER	Forces transmission of illegal code
TX_EN	Frames Transmit Data
COL	Collision Indication
CRS	Non-Idle Medium Indication
RX_CLK	Receive Clock
RXD<3:0>	Receive Data
RX_DV	Frames Receive SFD and DATA
RX_ER	Receive Error Indication
MDC	Management Data Clock
MDIO	Management Data

23.2.2.2 PCS–Management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in Clause 22 and Clause 30, respectively.

The loopback mode of operation shall be implemented in accordance with 22.2.4.1.2. The loopback mode of operation loops back transmit data to receive data, thus providing a way to check for the presence of a PHY.

No spurious signals shall be emitted onto the MDI when the PHY is held in power-down mode as defined in 22.2.4.1.5 (even if TX_EN is ON) or when released from power-down mode, or when external power is first applied to the PHY.

23.2.3 Frame structure

Frames passed from the PCS sublayer to the PMA sublayer shall have the structure shown in Figure 23–6. This figure shows how ternary symbols on the various pairs are synchronized as they are passed by the PMA_UNITDATA.indication and PMA_UNITDATA.request messages. Time proceeds from left to right in the figure.

In the frame structure example, the last 6T code group, DATA N, happens to appear on transmit pair BI_D3. It could have appeared on any of the three transmit pairs, with the five words eop1 through eop5 appended afterward as the next five octets in sequence. The end of packet as recognized by the PCS is defined as the end of the last ternary symbol of eop1. At this point a receiver has gathered enough information to locate the last word in the packet and check the dc balance on each pair.

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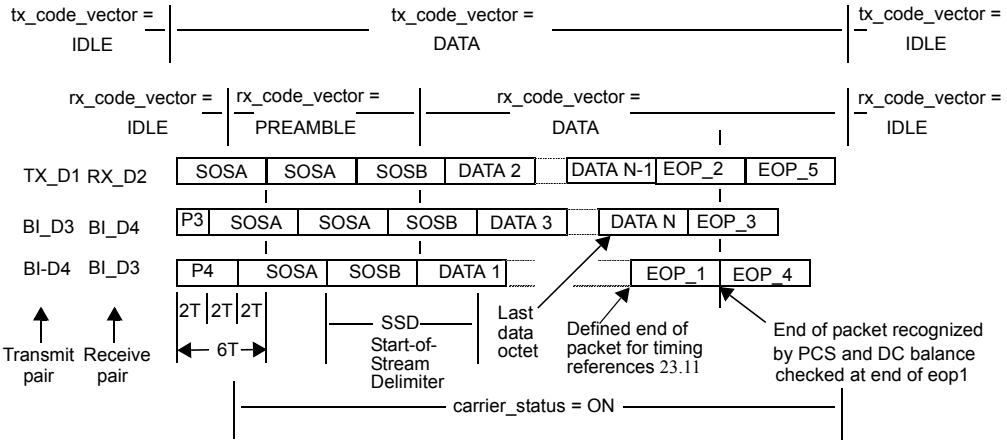


Figure 23–6—PCS sublayer to PMA sublayer frame structure

If the PMA service interface is exposed, data carried between PCS and PMA by the PMA_UNITDATA.indication and PMA_UNITDATA.request messages shall have a clock in each direction. Details of the clock implementation are left to the implementer. The choice of binary encoding for each ternary symbol is left to the implementer.

The following frame elements appear in Figure 23–6 (ternary symbols are transmitted leftmost first):

SOSA	The succession of six ternary symbols: `[ 1 -1 1 -1 1 -1]`, which is the result of encoding the constant sosa.
SOSB	The succession of six ternary symbols: `[ 1 -1 1 -1 -1 1]`, which is the result of encoding the constant sosb.
P3	The succession of two ternary symbols: `[ 1 -1]`.
P4	The succession of four ternary symbols: `[ 1 -1 1 -1]`.
DATA	A 6T code group that is the result of encoding a data octet in a packet that is not part of the Clause 4 MAC preamble or SFD.
EOP1-5	A 6T code group that is the result of encoding one of the end-of-packet patterns eop1-5.

23.2.4 PCS state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.2.4.1 PCS state diagram constants

Register tsr may take on any of the nine constant values listed below (sosa through eop5, bad_code, and zero_code). These values are used to describe the functional operation of the coding process.

NOTE—Implementers are under no obligation to implement these constants in any particular way. For example, some implementers may choose to implement these codes as special flag bits attached to MII TXD nibble registers. Other implementers may choose to implement insertion of these codes on the downstream side of the coder function, using precoded 6T sequences.

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All 6T codewords are sent leftmost ternary symbol first.

sosa	A constant that encodes to:	[1 -1 1 -1 1 -1].
sosb	A constant that encodes to:	[1 -1 1 -1 -1 1].
eop1	A constant that encodes to:	[1 1 1 1 1 1].
eop2	A constant that encodes to:	[1 1 1 1 -1 -1].
eop3	A constant that encodes to:	[1 1 -1 -1 0 0].
eop4	A constant that encodes to:	[-1 -1 -1 -1 -1 -1].
eop5	A constant that encodes to:	[-1 -1 0 0 0 0].
bad_code	A constant that encodes to:	[-1 -1 -1 1 1 1].
zero_code	A constant that encodes to:	[0 0 0 0 0 0].

23.2.4.2 PCS state diagram variables

codeword_error

Indicates reception of invalid 6T code group.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

dc_balance_error

Indicates reception of dc coding violation.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop

Indicates reception of eop1.

A state variable set by the decoding operation. Reset to OFF when in PCS Receive state AWAITING INPUT. When the decoder detects eop1 on any pair, it sets this flag ON. The timing of eop shall be adjusted such that the last nibble of the last decoded data octet in a packet is the last nibble sent across the MII by the PMA Receive state diagram with RX_DV set ON.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

eop_error

Indicates reception of data with improper end-of-packet coding.

Values: ON and OFF

Set by: PCS Receive; error-detecting rules

ih2, ih4, and ih3 (input holding registers)

A set of holding registers used for the purpose of holding decoded data octets in preparation for sending across the MII one nibble at a time. One register is provided for each of the three receive pairs RX_D2, BI_D4, and BI_D3, respectively.

Value: octet

Set by: PCS Receive

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Each time the PCS Receive function decodes a 6T code group, it loads the result (an octet) into one of the ih2-4 registers. These three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times.

The PCS Receive state diagram reads nibbles as needed from the ih2-4 registers and stuffs them into RXD.

ohr1, ohr3, and ohr4 (output holding registers)

(See Figure 23–7.) A set of shift registers used for the purpose of transferring coded 6T ternary symbol groups one ternary symbol at a time into the PMA. One register is provided for each of the three transmit pairs TX_D1, BI_D3, and BI_D4, respectively.

Value: 6T code group. Each of the six cells holds one ternary symbol (i.e., –1, 0, or 1).

Set by: PCS Transmit

Each time the PCS Transmit function encodes a data octet, it loads the result (a 6T code group) into one of the ohr registers. Three registers are loaded in round-robin fashion, one register being loaded every two ternary symbol times. The PCS shall transmit octets on the three transmit pairs in round-robin fashion, in the order TX_D1, BI_D3, and BI_D4, starting with TX_D1.

The PMA_UNITDATA.request (DATA) message picks the least significant (rightmost) ternary symbol from each ohr register and sends it to the PMA, as shown below. (Note that 6T codewords in Annex 23A are listed with lsb on the left, not the right.)

tx_code_vector[TX_D1] = the LSB of ohr1, also called ohr1[0]

tx_code_vector[BI_D3] = the LSB of ohr3, also called ohr3[0]

tx_code_vector[BI_D4] = the LSB of ohr4, also called ohr4[0]

After each PMA_UNITDATA.request message, all three ohr registers shift right by one ternary symbol, shifting in zero from the left. The PCS Transmit function loads a new 6T code group into each ohr immediately after the last ternary symbol of the previous group is shifted out.

At the beginning of a preamble, the PCS Transmit function loads the same value (sosa) into all three output holding registers, which causes alternating transitions to immediately appear on all three output pairs. The result on pairs BI_D3 and BI_D4 is depicted by codewords P3 and P4 in Figure 23–6.

pcs_reset

Causes reset of all PCS functions when ON.

Values: ON and OFF

Set by: PCS Reset

rx_crs

A latched asynchronous variable. Timing for the MII signal CRS is derived from rx_crs.

Values: ON and OFF

Set ON when: carrier_status changes to ON

Set OFF when either of two events occurs:

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carrier_status changes to OFF, or
detection of eop1, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3

Additionally, if, 20 ternary symbol times after rx_crs falls, carrier_status remains set to ON then set rx_crs=ON.

NOTE—A special circuit for the detection of eop1 and subsequent deassertion of rx_crs, faster than the full 8B6T decoding circuits, is generally required to meet the timing requirements for CRS listed in 23.11.

tsr (transmit shift register)

(See Figure 23–7.) A shift register defined for the purpose of assembling nibbles from the MII TXD into octets.

Values: The variable tsr always contains both the current nibble of TXD and the previous nibble of TXD. Valid values for tsr therefore include all octets. Register tsr may also take on any of the nine constant values listed in 23.2.4.1.

Nibble order: When encoding the tsr octet, the previous TXD nibble is considered the least significant nibble.

Set by: PCS Transmit

During the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall assume the following values in sequence regardless of TXD: sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb. This action substitutes the 100BASE-T4 preamble for the Clause 4 MAC preamble. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of sosa and sosb constants actually coded to 5 and 3, respectively.

During the first 10 TX_CLK cycles after TX_EN is deasserted, tsr shall assume the following values in sequence, regardless of TXD: eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5. This action appends the 100BASE-T4 end-of-packet delimiter to each pair. The PCS Transmit state diagram samples the tsr only every other clock, which reduces the number of eop1-5 constants actually coded to 1 each.

Except for the first 16 TX_CLK cycles after TX_EN is asserted, any time TX_ER and TX_EN are asserted, tsr shall assume the value bad_code with such timing as to cause both nibbles of the affected octet to be encoded as bad_code. If TX_ER is asserted at any time during the first 16 TX_CLK cycles after TX_EN is asserted, tsr shall during the 17th and 18th clock cycles assume the value bad_code.

If TX_EN is deasserted on an odd nibble boundary, the PCS shall extend TX_EN by one TX_CLK cycle, and behave as if TX_ER were asserted during that additional cycle.

Except for the first 10 TX_CLK cycles after TX_EN is deasserted, any time TX_EN is not asserted, tsr shall assume the value zero_code.

tx_extend

A latched, asynchronous state variable used to extend the TX_EN signal long enough to ensure complete transmission of all nonzero ternary symbols in eop1-5.

Values: ON and OFF

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Set ON upon: rising edge of TX_EN

Set OFF upon either of two conditions:
a) In the event of a collision (COL is asserted at any time during transmission) set tx_extend=OFF when TX_EN deasserts.
b) In the event of no collision (COL remains deasserted throughout transmission) set tx_extend=OFF upon completion of transmission of last ternary symbol in eop4.

NOTE 1—The 6T code group eop5 has four zeros at the end. The 6T code group eop4 contains the last non-zero ternary symbol to be transmitted.

NOTE 2—The effect of a collision, if present, is to truncate the frame at the original boundary determined by TX_EN. Noncolliding frames are extended, while colliding frames are not.

23.2.4.3 PCS state diagram timer

tw1_timer

A continuous free-running timer.

Values: The condition tw1_timer_done goes true when the timer expires.

Restart when: Immediately after expiration (restarting the timer resets condition tw1_timer_done).

Duration: 40 ns nominal.

TX_CLK shall be generated synchronous to tw1_timer (see tolerance required for TX_CLK in 23.5.1.2.10).

On every occurrence of tw1_timer_done, the state diagram advances by one block. The message PMA_UNITDATA.request is issued concurrent with tw1_timer_done.

23.2.4.4 PCS state diagram functions

encode()

The encode operation of 23.2.1.2.

Argument: octet

Returns: 6T code group

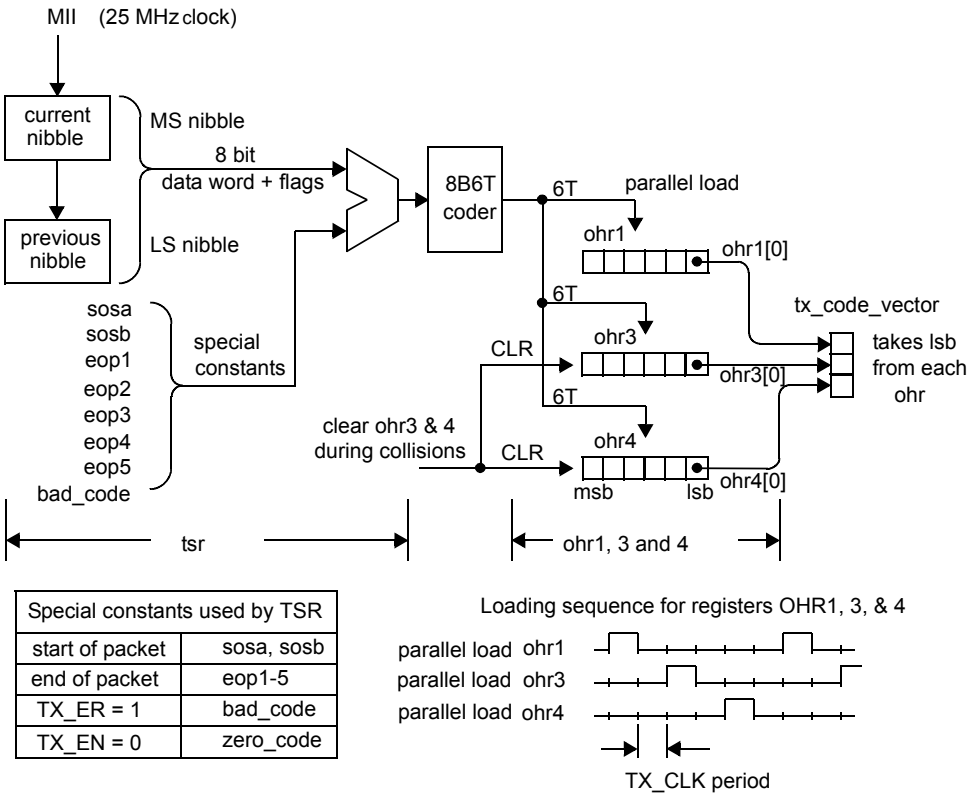
decode()

The decode operation of 23.2.1.3.

Argument: 6T code group

Returns: octet

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Special constants used by TSR	
start of packet	sosa, sosb
end of packet	eop1-5
TX_ER = 1	bad_code
TX_EN = 0	zero_code

Figure 23–7—PCS Transmit reference diagram

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23.2.4.5 PCS state diagrams

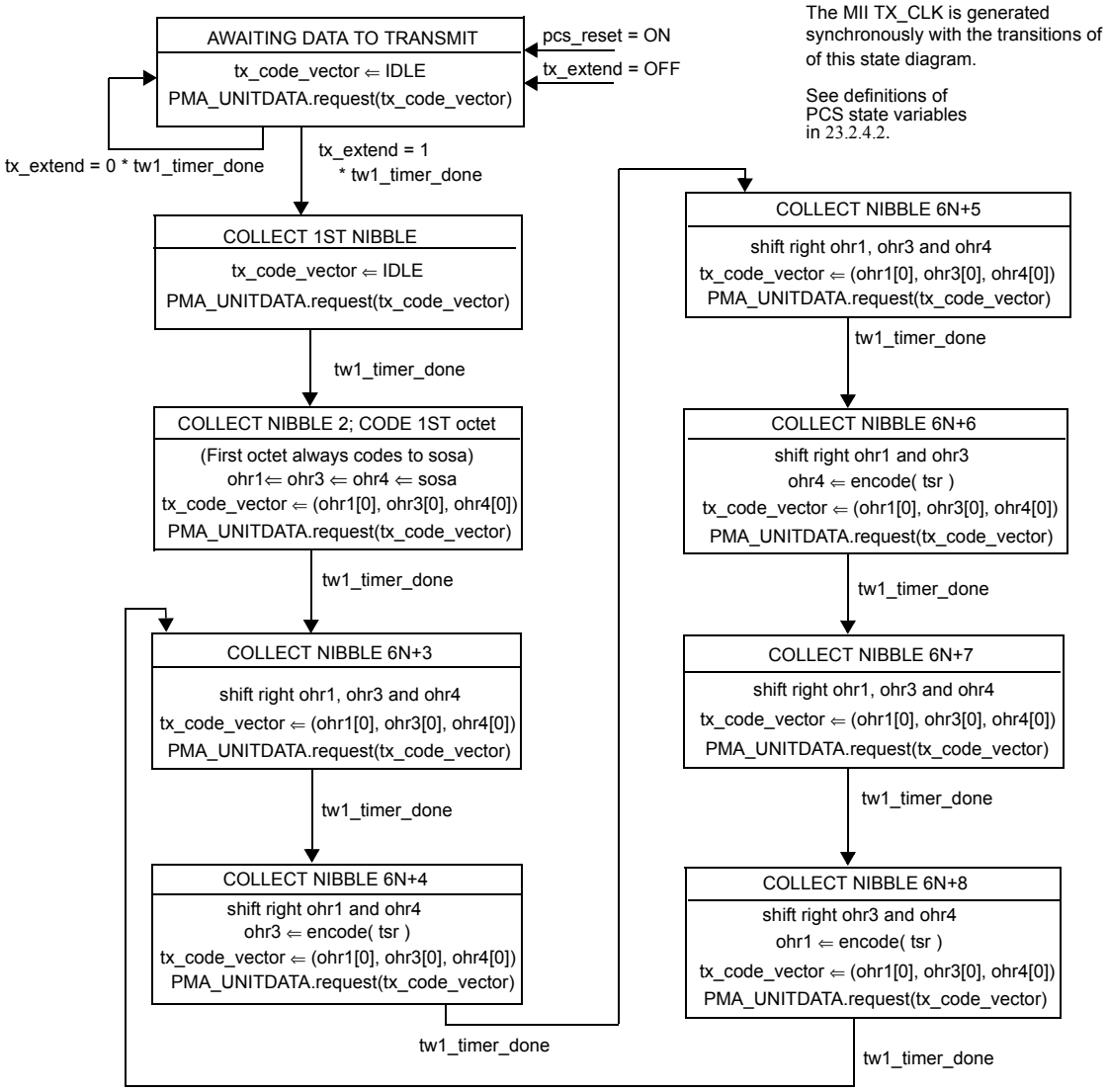


Figure 23–8—PCS Transmit state diagram

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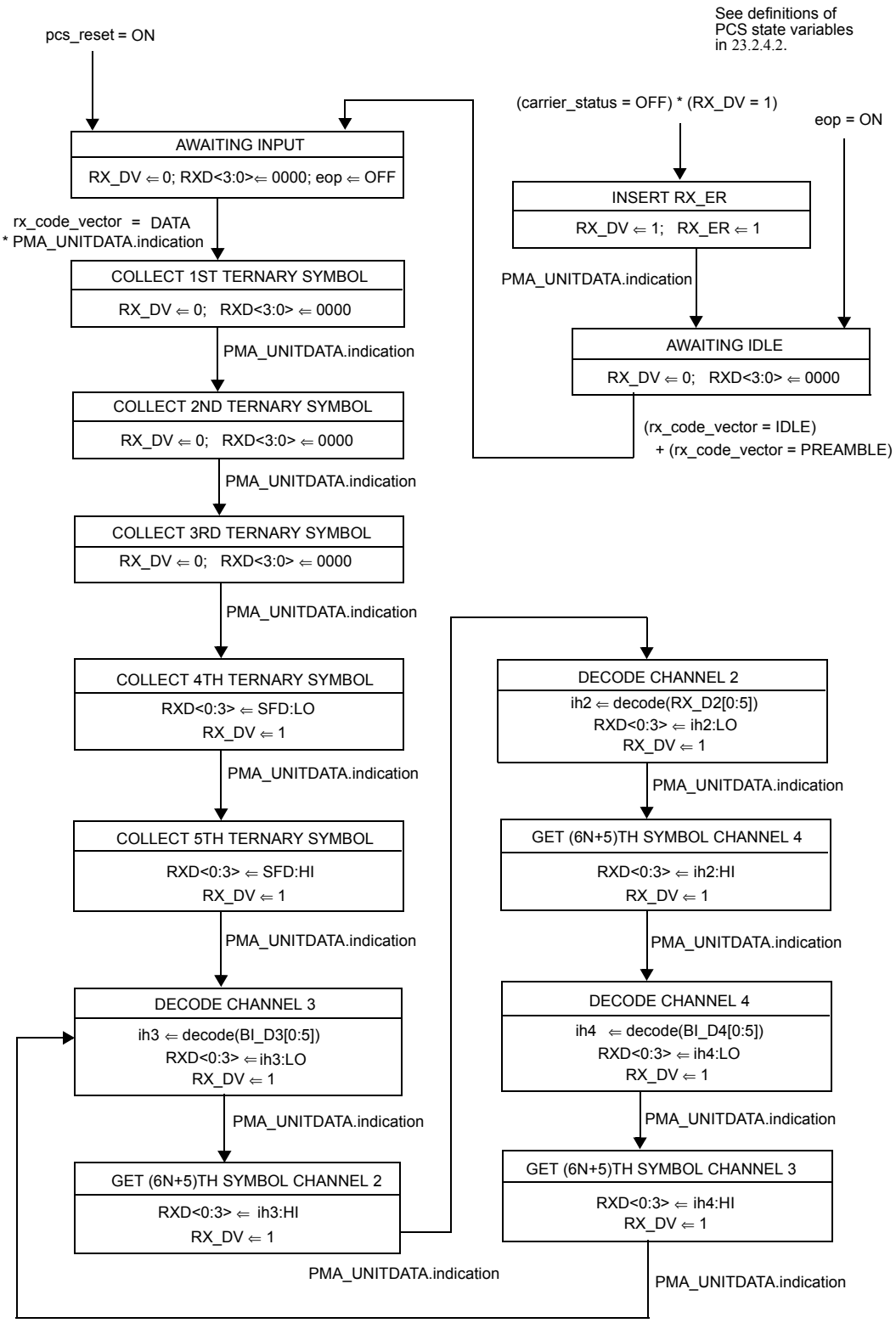


Figure 23–9—PCS Receive state diagram

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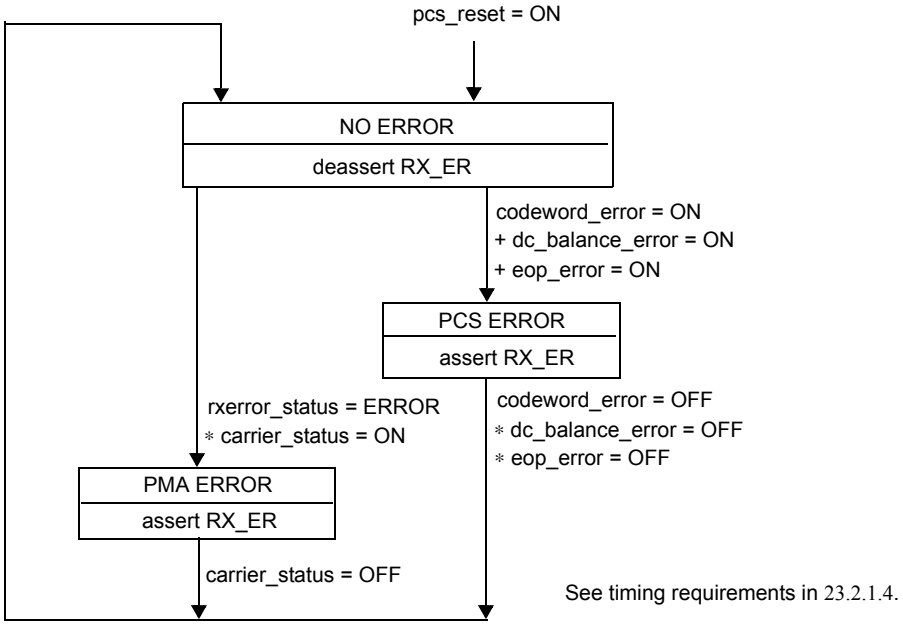


Figure 23–10—PCS Error Sense state diagram

23.2.5 PCS electrical specifications

The interface between PCS and PMA is an abstract message-passing interface, having no specified electrical properties.

Electrical characteristics of the signals passing between the PCS and MII may be found in Clause 22.

23.3 PMA service interface

This clause specifies the services provided by the PMA to either the PCS or a Repeater client. These services are described in an abstract manner and do not imply any particular implementation.

The PMA Service Interface supports the exchange of code vectors between the PMA and its client (either the PCS or a Repeater). The PMA also generates status indications for use by the client.

The following primitives are defined:

PMA_TYPE.indication

PMA_UNITDATA.request

PMA_UNITDATA.indication

PMA_CARRIER.indication

PMA_LINK.indication

PMA_LINK.request

PMA_RXERROR.indication

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23.3.1 PMA_TYPE.indication

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

23.3.1.1 Semantics of the service primitive

PMA_TYPE.indication (pma_type)

The pma_type parameter for use with the 100BASE-T4 PMA is T4.

23.3.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

23.3.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the PMA_UNITDATA.request and PMA_UNITDATA.indication primitives.

23.3.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of tx_code_vector parameters) from the PCS or repeater to the PMA.

23.3.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code_vector)

When transmitting data using 100BASE-T4 signaling, the PMA_UNITDATA.request conveys to the PMA simultaneously the logical output value for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The value of tx_code_vector during data transmission is therefore a three-element vector, with one element corresponding to each output pair. Each of the three elements of the tx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and - listed for each ternary symbol in the 8B6T code table (see Annex 23A).

Between packets, the 100BASE-T4 PMA layer sends the 100BASE-T4 idle signal, TP_IDL_100. The PCS informs the PMA layer that it is between packets, thus enabling the PMA idle signal, by setting the tx_code_vector parameter to IDLE.

For pma_type 100BASE-T4, the tx_code_vector parameter can take on either of two forms:

IDLE	A single value indicating to the PMA that there is no data to convey. The PMA generates link integrity pulses during the time that tx_code_vector = IDLE.
DATA	A vector of three ternary symbols, one for each of the three transmit pairs TX_D1, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising tx_code_vector, when they are conveyed using the DATA format, are called, according to the pair on which each will be transmitted, tx_code_vector[BI_D4], tx_code_vector[TX_D1], and tx_code_vector[BI_D3].

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23.3.2.2 When generated

The PCS or Repeater client generates PMA_UNITDATA.request synchronous with every MII TX_CLK.

For the purposes of state diagram descriptions, it may be assumed that at the time PMA_UNITDATA.request is generated, the MII signals TX_EN, and TX_ER, and TXD instantly become valid and that they retain their values until the next PMA_UNITDATA.request.

In the state diagrams, PMA_UNITDATA.request is assumed to occur at the conclusion of each tw1 wait function.

23.3.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits the indicated ternary symbols on the MDI.

23.3.3 PMA_UNITDATA.indication

This primitive defines the transfer of data (in the form of rx_code_vector parameters) from the PMA to the PCS or repeater during the time that link_status=OK.

23.3.3.1 Semantics of the service primitive

PMA_UNITDATA.indication (rx_code_vector)

When receiving data using 100BASE-T4 signaling, the PMA_UNITDATA.indication conveys to the PCS simultaneously the logical input value for each of the three receive pairs RX_D2, BI_D4, and BI_D3. The value of rx_code_vector during data reception is therefore a three-element vector, with one element corresponding to each input pair. Each of the three elements of the rx_code_vector may take on one of three logical values: 1, 0, or –1, corresponding to the three ternary possibilities +, 0, and – listed for each ternary symbol in the 8B6T code table (see Annex 23A).

Between packets, the rx_code_vector is set by the PMA to the value IDLE.

From the time the PMA asserts carrier_status=ON until the PMA recognizes the SSD pattern (not all of the pattern need be received in order for the PMA to recognize the pattern), the PMA sets rx_code_vector to the value PREAMBLE.

For pma_type 100BASE-T4, the rx_code_vector parameter can take on any of three forms:

IDLE	A single value indicating that the PMA has no data to convey.
PREAMBLE	A single value indicating that the PMA has detected carrier, but has not received a valid SSD.
DATA	A vector of three ternary symbols, one for each of the three receive pairs RX_D2, BI_D3, and BI_D4. The ternary symbol for each pair may take on one of three values, 1, 0, or –1.

The ternary symbols comprising rx_code_vector, when they are conveyed using the DATA format, are called, according to the pair upon which each symbol was received, rx_code_vector[BI_D3], rx_code_vector[RX_D2], and rx_code_vector[BI_D4].

23.3.3.2 When generated

The PMA shall generate PMA_UNITDATA.indication (DATA) messages synchronous with data received at the MDI.

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23.3.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.4 PMA_CARRIER.indication

This primitive is generated by the PMA to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client the earliest reliable indication of activity on the underlying medium.

23.3.4.1 Semantics of the service primitive

PMA_CARRIER.indication (carrier_status)

The carrier_status parameter can take on one of two values: OFF or ON, indicating whether the incoming signal should be interpreted as being between packets (OFF) or as a packet in progress (ON).

23.3.4.2 When generated

The PMA shall generate this primitive to indicate the value of carrier_status.

23.3.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.3.5 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS or repeater client or Auto-Negotiation algorithm a means of determining the validity of received code elements.

23.3.5.1 Semantics of the service primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK:

FAIL	The link integrity function does not detect a valid 100BASE-T4 link.
READY	The link integrity function detects a valid 100BASE-T4 link, but has not been enabled by Auto-Negotiation.
OK	The 100BASE-T4 link integrity function detects a valid 100BASE-T4 link, and has been enabled by Auto-Negotiation.

23.3.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status.

23.3.5.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

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23.3.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm. The purpose of this primitive is to allow the Auto-Negotiation algorithm to enable and disable operation of the PHY.

23.3.6.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PHY reports link_status=READY if it recognizes 100BASE-T4 carrier from the far end, but no other actions are enabled.
DISABLE	Used by the Auto-Negotiation algorithm to disable PHY processing in the event fast link pulses are detected. This gives the Auto-Negotiation algorithm a chance to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions. This is the default mode if Auto-Negotiation is not present.

23.3.6.2 Default value of parameter link_control

Upon power-on, reset, or release from power-down, the link_control parameter shall revert to ENABLE. If the optional Auto-Negotiation algorithm is not implemented, no PMA_LINK.request message will arrive and the PHY will operate indefinitely with link_control=ENABLE.

23.3.6.3 When generated

The Auto-Negotiation algorithm generates this primitive to indicate to the PHY how to behave.

Upon power-on, reset, or release from power down, the Auto-Negotiation algorithm, if present, issues the message PMA_LINK.request (SCAN_FOR_CARRIER).

23.3.6.4 Effect of receipt

Whenever link_control=SCAN_FOR_CARRIER, the PHY shall enable the Link Integrity state diagram, but block passage into the state LINK_PASS, while holding rcv=DISABLE, and xmit=DISABLE. While link_control=SCAN_FOR_CARRIER, the PHY shall report link_status=READY if it recognizes 100BASE-T4 link integrity pulses coming from the far end, otherwise it reports link_status=FAIL.

Whenever link_control=DISABLE, the PHY shall report link_status=FAIL and hold the Link Integrity state diagram in the RESET state, while holding rcv=disable and xmit=DISABLE.

While link_control=ENABLE, the PHY shall allow the Link Integrity function to determine if the link is available and, if so, set rcv=ENABLE and xmit=ENABLE.

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23.3.7 PMA_RXERROR.indication

The primitive is generated in the PMA by the PMA Align function to indicate the status of the signal being received from the MDI. The purpose of this primitive is to give the PCS or repeater client an indication of a PMA detectable receive error.

23.3.7.1 Semantics of the service primitive

PMA_RXERROR.indication (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the incoming signal contains a detectable error (ERROR) or not (NO_ERROR).

23.3.7.2 When generated

The PMA shall generate this primitive to indicate whether or not each incoming packet contains a PMA detectable error (23.2.1.4).

23.3.7.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

23.4 PMA functional specifications

The PMA couples messages from a PMA service interface (23.3) to the 100BASE-T4 baseband medium (23.6).

The interface between PCS and the baseband medium is the Medium Dependent Interface (MDI), specified in 23.7.

23.4.1 PMA functions

The PMA sublayer comprises one PMA Reset function and six simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, PMA Carrier Sense, Link Integrity, PMA Align, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. When the PMA is used in conjunction with a PCS, the RESET function may be shared between layers.

The PMA reference diagram, Figure 23–11, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in Figure 23–11. The Management Interface and its functions are specified in Clause 22.

23.4.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occur. These two conditions are power-on and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions. The PMA Reset function sets pma_reset=ON for the duration of its reset function. All state diagrams take the open-ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

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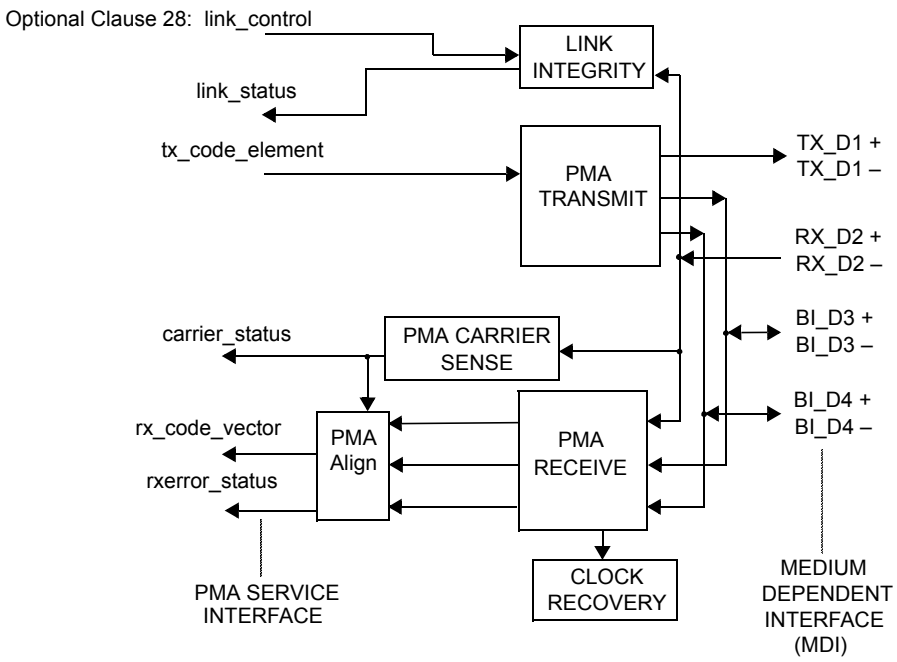


Figure 23–11—PMA reference diagram

23.4.1.2 PMA Transmit function

Except as provided for in the next paragraph, whenever (tx_code_vector=DATA)×(pma_carrier=OFF), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], tx_code_vector[BI_D3], and tx_code_vector[BI_D4], respectively.

Whenever (tx_code_vector=DATA)×(pma_carrier=ON), the PMA shall transmit onto the MDI ternary symbols on pairs TX_D1, BI_D3, and BI_D4 equal to tx_code_vector[TX_D1], CS0, and CS0, respectively, and continue doing so until tx_code_vector=IDLE.

NOTE—This shuts off the transmitters on channels BI_D3 and BI_D4, and keeps them off, in the event of a collision. Shutting off the transmitters prevents overload and saturation of the transmitters, and also reduces the amount of near-end crosstalk present while monitoring for the end of carrier.

Whenever tx_code_vector=IDLE, an idle signal shall be transmitted on pair TX_D1 and silence on pairs BI_D3 and BI_D4. The idle signal consists of periods of silence (times where the differential output voltage remains at 0 mV ± 50 mV) broken by the transmission of link integrity test pulses.

The 100BASE-T4 idle signal is similar to the 10BASE-T idle signal, but with 100BASE-T4 ternary signal levels and a faster repetition rate. The 100BASE-T4 idle signal is called TP_IDL_100. The TP_IDL_100 signal shall be a repeating sequence formed from one 1.2 ms ± 0.6 ms period of silence (the time where the differential voltage remains at 0 mV ± 50 mV) and one link test pulse. Each link test pulse shall be a succession of two ternary symbols having logical values of –1 and 1 transmitted on pair TX_D1 using CS-1 and CS1 as defined in 23.4.3.1. Following a packet, the TP_IDL_100 shall start with a period of silence.

Transmission of TP_IDL_100 may be terminated at any time with respect to the link test pulse. It shall be terminated such that ternary symbols of the subsequent packet are not corrupted, and are not delayed any more than is specified in 23.11.

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For any link test pulse occurring within 20 ternary symbol times of the beginning of a preamble, the zero crossing jitter (as defined in 23.5.1.2.5) of the link test pulse when measured along with the zero crossings of the preamble shall be less than 4 ns p-p.

NOTE—The above condition allows clock recovery implementations that optionally begin fast-lock sequences on part of a link integrity pulse to properly acquire lock on a subsequent preamble sequence.

Regardless of other considerations, when the transmitter is disabled (xmit=DISABLE), the PMA Transmit function shall transmit the TP_IDL_100 signal.

23.4.1.3 PMA Receive function

PMA Receive contains the circuits necessary to convert physically encoded ternary symbols from the physical MDI receive pairs (RX_D2, BI_D3 and BI_D4) into a logical format suitable for the PMA Align function. Each receive pair has its own dedicated PMA Receive circuitry.

The PHY shall receive the signals on the receive pairs (RX_D2, BI_D3, and BI_D4) and translate them into one of the PMA_UNITDATA.indication parameters IDLE, PREAMBLE, or DATA with a ternary symbol error ratio of less than one part in 10^8.

If both pma_carrier=ON and tx_code_vector=DATA, the value of rx_code_vector is unspecified until pma_carrier=OFF.

23.4.1.4 PMA Carrier Sense function

The PMA Carrier Sense function shall set pma_carrier=ON upon reception of the following pattern on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

> Any signal greater than 467 mV, followed by any signal less than –225 mV, followed by any signal greater than 467 mV, all three events occurring within 2 ternary symbol times.

The operation of carrier sense is undefined for signal amplitudes greater than 4.5 V.

See 23.5.1.3.2 for a list of signals defined *not* to set pma_carrier=ON.

After asserting pma_carrier=ON, PMA Carrier Sense shall set pma_carrier=OFF upon receiving either of these conditions:

a) Seven consecutive ternary symbols of value CS0 on pair RX_D2.
b) (tx_code_vector=DATA) has not been true at any time since pma_carrier was asserted, *and* the 6T code group eop1 has been received, properly framed, on any of the lines RX_D2, BI_D4, or BI_D3, *and* enough time has passed to assure passage of all ternary symbols of eop4 across the PMA service interface.

NOTE—Designers may wish to take advantage of the fact that the minimum received packet fragment will include at least 24 ternary symbols of data on pair RX_D2. Therefore, once carrier is activated, it is not necessary to begin searching for seven consecutive zeros until after the 24th ternary symbol has been received. During the time that the first 24 ternary symbols are being received, the near-end crosstalk from pairs BI_D3 and BI_D4, which are switched off during collisions, decays substantially.

While rcv=ENABLE, the PMA CARRIER function shall set carrier_status = pma_carrier.

While rcv≠ENABLE, the PMA CARRIER function shall set carrier_status = OFF.

This function operates independently of the Link Integrity function.

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23.4.1.5 Link Integrity function

Link Integrity provides the ability to protect the network from the consequences of failure of the simplex link attached to RX_D2. While such a failure is present, transfer of data by the Transmit and Receive functions is disabled.

Link Integrity observes the incoming wire pair, RX_D2, to determine whether the device connected to the far end is of type 100BASE-T4. Based on its observations, Link Integrity sets two important internal variables:

a) pma_type variable is set to 100BASE-T4.
b) link_status variable is a parameter sent across the PMA Service interface.

The Link Integrity function shall comply with the state diagram of Figure 23–12.

Four conditions gate the progression of states toward LINK_PASS: (1) reception of at least 31 link integrity test pulses; (2) reception of at least 96 more link integrity test pulses, or reception of carrier; (3) cessation of carrier, if it was present; (4) detection of equals link_control ENABLE.

While the PMA is not in the LINK_PASS state, the Link Integrity function sets rcv=DISABLE and xmit=DISABLE, thus disabling the bit transfer of the Transmit and Receive functions.

If a visible indicator is provided on the PHY to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the PHY is in the LINK_PASS state and off otherwise.

23.4.1.6 PMA Align function

The PMA Align function accepts received ternary symbols from the PMA Receive function, along with pma_carrier. PMA Align is responsible for realigning the received ternary symbols to eliminate the effects of unequal pair propagation time, commonly called pair skew. PMA Align also looks for the SSD pattern to determine the proper alignment of 6T code groups, and then forwards PMA_UNITDATA.indication (DATA) messages to the PCS. The SSD pattern includes referencing patterns on each of the three receive lines that may be used to establish the proper relationship of received ternary symbols (see Figure 23–6).

NOTE—The skew between lines is not expected to change measurably from packet to packet.

At the beginning of each received frame, the PMA Carrier Sense function asserts pma_carrier=ON. During the preamble, the Clock Recovery function begins synchronizing its receive clock. Until clock is synchronized, data coming from the low-level PMA Receive function is meaningless. The PMA Align function is responsible for waiting for the receiver clock to stabilize and then properly recognizing the 100BASE-T4 coded SSD pattern. The PMA Align function shall send PMA_UNITDATA.indication (PREAMBLE) messages to the PCS from the time pma_carrier=ON is asserted until the PMA is ready to transfer the first PMA_UNITDATA.indication (DATA) message. Once the PMA Align function locates a SSD pattern, it begins forwarding PMA_UNITDATA.indication (DATA) messages to the PCS, starting with the first ternary symbol of the first data word on pair BI_D3, as defined in Figure 23–6. This first PMA_UNITDATA.indication (DATA) message shall transfer the following ternary symbols, as specified in the frame structure diagram, Figure 23–6:

rx_code_vector[BI_D3]first ternary symbol of first data code group

rx_code_vector[RX_D2]second ternary symbol prior to start of second data code group

rx_code_vector[BI_D4]fourth ternary symbol prior to start of third data code group

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PMA Align shall continue sending PMA_UNITDATA.indication (DATA) messages until pma_carrier=OFF. While pma_carrier=OFF, PMA Align shall emit PMA_UNITDATA.indication (IDLE) messages.

If no valid SSD pattern is recognized within 22 ternary symbol times of the assertion of pma_carrier=ON, the PMA Align function shall set rxerror_status=ERROR. The PMA Align function is permitted to begin sending PMA_UNITDATA.indication (DATA) messages upon receipt of a partially recognized SSD pattern, but it is required to set rxerror_status=ERROR if the complete SSD does not match perfectly the expected ternary symbol sequence. Rxerror_status shall be reset to NO_ERROR when pma_carrier=OFF.

The PMA Align function is permitted to use the first received packet of at least minimum size after RESET or the transition to LINK_PASS to learn the nominal skew between pairs, adjust its equalizer, or perform any other initiation functions. During this first packet, the PMA Align function shall emit PMA_UNITDATA.indication (PREAMBLE) messages, but may optionally choose to never begin sending PMA_UNITDATA.indication (DATA) messages.

The PMA Align function shall tolerate a maximum skew between any two pairs of 60 ns in either direction without error.

To protect the network against the consequences of mistaken packet framing, the PMA Align function shall detect the following error and report it by setting rxerror_status=ERROR (optionally, those error patterns already detected by codeword_error, dc_balance_error, or eop_error do not also have to be detected by rxerror_status): *In a series of good packets, any one packet that has been corrupted with three or fewer ternary symbols in error causing its sosb 6T code groups on one or more pairs to appear in the wrong location.*

Several approaches are available for meeting this requirement, including, but not limited to, a) comparing the relative positions of sosb 6T code groups on successive packets; b) measuring the time between the first preamble pulse and reception of sosb on each pair; c) counting the number of zero crossings from the beginning of the preamble until sosb; and d) monitoring for exception strings like “11” and “–1–1–1” in conjunction with one or more of the above techniques.

Regardless of other considerations, when the receive function is disabled (rcv=DISABLE), the PMA Align function shall emit PMA_UNITDATA.indication (IDLE) messages and no others.

23.4.1.7 Clock Recovery function

The Clock Recovery function couples to all three receive pairs. It provides a synchronous clock for sampling each pair. While it may not drive the MII directly, the Clock Recovery function is the underlying root source of RX_CLK.

The Clock Recovery function shall provide a clock suitable for synchronously decoding ternary symbols on each line within the bit error tolerance provided in 23.4.1.3. During each preamble, in order to properly recognize the frame delimiting pattern formed by codeword sosb on each pair, the received clock signal must be stable and ready for use in time to decode the following ternary symbols: the 16th ternary symbol of pair RX_D2, the 18th ternary symbol of pair BI_D4, and the 14th ternary symbol of pair BI_D3.

23.4.2 PMA interface messages

The messages between the PMA and PCS are defined above in 23.3, PMA Service Interface. Communication between a repeater unit and PMA also uses the PMA Service Interface. Communication through the MDI is summarized in Tables 23–2 and 23–3.

TP_IDL_100 is defined in 23.4.1.2. The waveforms used to convey CS1, CS0, and CS-1 are defined in 23.5.1.2.

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Table 23–2—MDI signals transmitted by the PHY

Signal	Allowed pair	Meaning
CS1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal voltage level +3.5 V.
CS0	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal voltage level 0 V.
CS-1	TX_D1, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal voltage level –3.5 V.
TP_IDL_100	TX_D1	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

Table 23–3—Signals received at the MDI

Signal	Allowed pair	Meaning
CS1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 1. Nominal transmitted voltage level +3.5 V.
CS0	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol 0. Nominal transmitted voltage level 0 V.
CS-1	RX_D2, BI_D3 BI_D4	A waveform that conveys the ternary symbol –1. Nominal transmitted voltage level –3.5 V.
TP_IDL_100	RX_D2	Idle signal. Indicates transmitter is currently operating at 100 Mb/s.

TP_IDL_100 is defined in 23.4.1.2. The encodings for CS1, CS0, and CS-1 are defined in 23.5.1.2.

Re-timing of CS1, CS0, and CS-1 signals within the PMA is required.

23.4.3 PMA state diagrams

The notation used in the state diagrams follows the conventions of 21.5. Transitions shown without source states are evaluated continuously and take immediate precedence over all other conditions.

23.4.3.1 PMA constants

CS0

A waveform that conveys the ternary symbol 0.

Value: CS0 has a nominal voltage of 0 V. See 23.5.1.2.

CS1

A waveform that conveys the ternary symbol 1.

Value: CS1 has a nominal peak voltage of +3.5 V. See 23.5.1.2.

CS-1

A waveform that conveys the ternary symbol –1.

Value: CS-1 has a nominal peak voltage of –3.5 V. See 23.5.1.2.

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link_100_max

A constant.

Value: Greater than 5.0 ms and less than 7.0 ms.

Used by link_max_timer to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

link_100_min

A constant.

Value: Greater than 0.15 ms and less than 0.45 ms.

Used by cnt_link to detect link test pulses on pair RX_D2 that are too close together to be valid 100BASE-T4 link test pulses.

23.4.3.2 State diagram variables

pma_reset

Causes reset of all PCS functions.

Values: ON and OFF

Set by: PMA Reset

pma_carrier

A version of carrier_status used internally by the PMA sublayer. The variable pma_carrier always functions regardless of the link status. The value of pma_carrier is passed on through the PMA service interface as carrier_status when rcv=ENABLE. At other times, the passage of pma_carrier information to the PMA service interface is blocked.

Values: ON, OFF

Set by: PMA CARRIER

rcv

Controls the flow of data from the PMA to PCS through the PMA_UNITDATA.indication message.

Values: ENABLE (receive is enabled)
DISABLE (the PMA always sends PMA_UNITDATA.indication (IDLE), and carrier_status is set to OFF)

xmit

Controls the flow of data from PCS to PMA through the PMA_UNITDATA.request message.

Values: ENABLE (transmit is enabled)
DISABLE (the PMA interprets all PMA_UNITDATA.request messages as PMA_UNITDATA.request (IDLE). The PMA transmits no data, but continues sending TP_IDL_100).

23.4.3.3 State diagram timers

link_max_timer

A re-triggerable timer.

Values: The condition link_max_timer_done goes true when the timer expires.

Restart when: Timer is restarted for its full duration by every occurrence of either a link test pulse on pair RX_D2 or the assertion of pma_carrier=ON (restarting the timer

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resets the condition link_max_timer_done).

Duration: link_100_max

Used by Link Integrity to detect the absence of 100BASE-T4 link test pulses on pair RX_D2.

23.4.3.4 State diagram counters

cnt_link

Counts number of 100BASE-T4 link test pulses (see 23.5.1.3.1) received on pair RX_D2.

Values: nonnegative integers

Reset to zero: On either of two conditions:

a) While in any state other than LINK_PASS, reset counter to zero if successive link test pulses are received within link_100_min.
b) While in any state, reset to zero if link_max_timer expires.

While in the LINK_PASS state, ignore pulses received within link_100_min (i.e., do not count them).

23.4.3.5 Link Integrity state diagram

The Link Integrity state diagram is shown in Figure 23–12.

23.5 PMA electrical specifications

This clause defines the electrical characteristics of the PHY at the MDI.

The ground reference point for all common-mode tests is the MII ground circuit. Implementations without an MII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

23.5.1 PMA-to-MDI interface characteristics

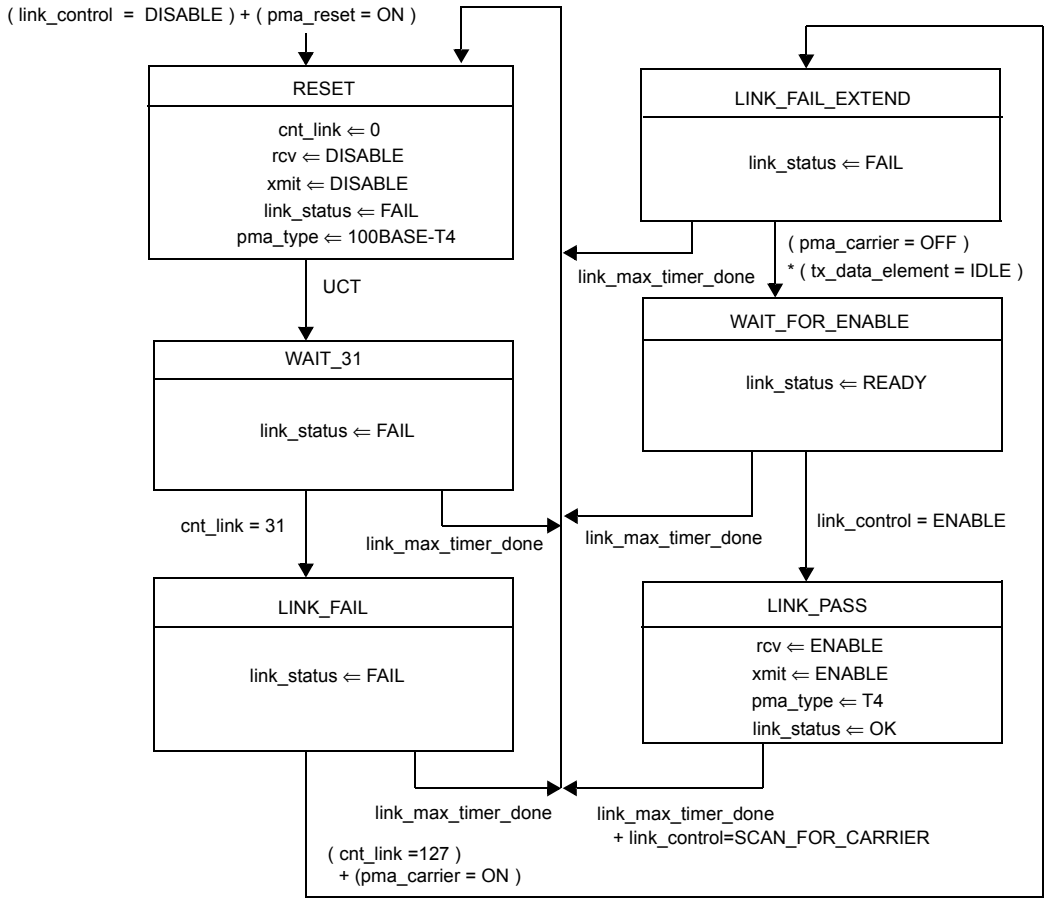
23.5.1.1 Isolation requirement

The PHY shall provide electrical isolation between the DTE, or repeater circuits including frame ground, and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in subclause 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in subclause 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

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NOTE—The variables link_control and link_status are designated as link_control_[T4] and link_status_[T4], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 23–12—Link Integrity state diagram

23.5.1.2 Transmitter specifications

The PMA shall provide the Transmit function specified in 23.4.1.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet requirements of this clause when each transmit output is connected to a differentially connected 100 Ω resistive load.

23.5.1.2.1 Peak differential output voltage

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 -1 0 0 0] (leftmost ternary symbol first), and while observing the differential transmitted output at the MDI, for any pair, with no intervening cable, the absolute value of both positive and negative peaks shall fall within the range of 3.15 V to 3.85 V (3.5 V ± 10%).

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23.5.1.2.2 Differential output templates

While repetitively transmitting the ternary sequence [0 0 1 0 0 0 0 0 -1 0 0 0], and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized transmit template listed in Table 23–4. Portions of this table are represented graphically in Figure 23–13. The entire normalized transmit template shall be scaled by a single factor between 3.15 and 3.85. It is a functional requirement that linear interpolation be used between points. The template time axis may be shifted horizontally to attain the most favorable match. In addition to this simple test pattern, all other pulses, including link integrity pulses and also including the first pulse of each packet preamble, should meet this same normalized transmit template, with appropriate shifting and linear superposition of the CS1 and CS-1 template limits. Transmitters are allowed to insert additional delay in the transmit path in order to meet the first pulse requirement, subject to the overall timing limitations listed in 23.11, Timing summary.

While transmitting the TP_IDL_100 signal, and while observing the transmitted output at the MDI, the observed waveform shall fall within the normalized link pulse template listed in Table 23–4. Portions of this table are represented graphically in Figure 23–14. The entire template shall be scaled by the same factor used for the normalized transmit template test. It is a functional requirement that linear interpolation be used between template points. The template time axis may be shifted horizontally to attain the most favorable match.

After transmitting seven or more consecutive CS0 waveforms during the TP_IDL_100 signal, each pair, as observed using the 100BASE-T4 Transmit Test Filter (23.5.1.2.3) connected to the MDI, shall attain a state within 50 mV of zero.

When the TX_D1, BI_D3, or BI_D4 pair is driven with a repeating pattern (1 -1 1 -1 ...) any harmonic measured at the MDI output shall be at least 27 dB below the fundamental at 12.5 MHz.

NOTE 1—The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementer should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

NOTE 2—The repetitive pattern [0 0 1 0 0 0 0 0 -1 0 0 0] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 73 hex. The repetitive pattern [1 -1 1 -1 1 -1] (leftmost ternary symbol first) may be synthesized using the 8B6T coding rules from a string of repeating data octets with value 92 hex.

The ideal template values may be automatically generated from the following equations:

Laplace transform of
Ideal transmit response $$IdealResponse(s) = \frac{Ideal(s)}{LPF(s)}$$

Where $Ideal(s)$ is a 100% raised cosine system response

Where $LPF(s)$ is a 3-pole Butterworth low pass filter response with –3 dB point at 25 MHz

Convert *IdealResponse(s)* from frequency domain to time domain

Use at least 8 samples per ternary symbol for the conversion

Superimpose alternating positive and negative copies of the ideal time response, separated by 6 ternary symbol times, to form the ideal transmit voltage waveform.

The template limits are formed by offsetting the ideal transmit voltage waveform by plus and minus 6% of its peak.

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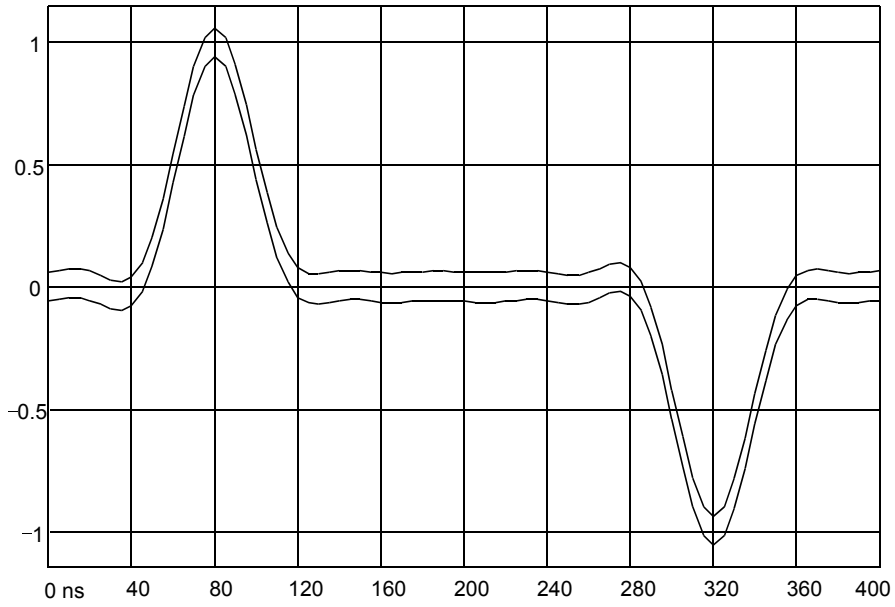


Figure 23–13—Normalized transmit template as measured at MD

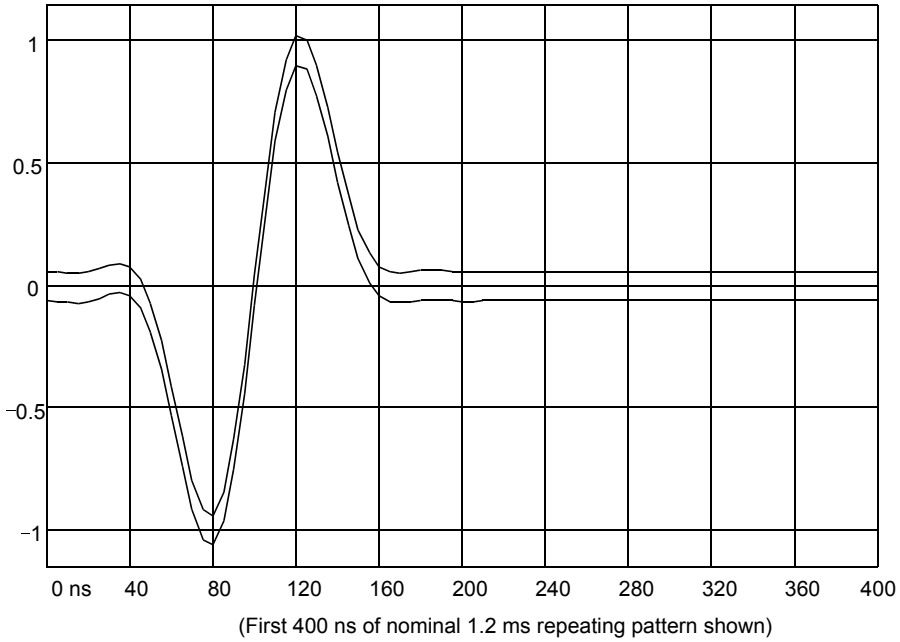


Figure 23–14—Normalized link pulse template as measured at MDI

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Table 23–4—Normalized voltage templates as measured at the MDI

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
0	0.060	–0.061	0.061	–0.060
5	0.067	–0.054	0.056	–0.065
10	0.072	–0.049	0.052	–0.069
15	0.072	–0.049	0.052	–0.069
20	0.063	–0.058	0.058	–0.063
25	0.047	–0.074	0.071	–0.050
30	0.030	–0.091	0.086	–0.035
35	0.023	–0.098	0.094	–0.027
40	0.041	–0.080	0.080	–0.041
45	0.099	–0.022	0.027	–0.094
50	0.206	0.085	–0.076	–0.197
55	0.358	0.237	–0.231	–0.352
60	0.544	0.423	–0.428	–0.549
65	0.736	0.615	–0.640	–0.761
70	0.905	0.784	–0.829	–0.950
75	1.020	0.899	–0.954	–1.075
80	1.060	0.940	–0.977	–1.098
85	1.020	0.899	–0.876	–0.997
90	0.907	0.786	–0.653	–0.774
95	0.744	0.623	–0.332	–0.453
100	0.560	0.439	0.044	–0.077
105	0.384	0.263	0.419	0.298
110	0.239	0.118	0.738	0.617
115	0.137	0.016	0.959	0.838
120	0.077	–0.044	1.060	0.940
125	0.053	–0.068	1.044	0.923
130	0.050	–0.071	0.932	0.811
135	0.057	–0.064	0.759	0.638
140	0.064	–0.057	0.565	0.444
145	0.067	–0.054	0.383	0.262
150	0.065	–0.056	0.238	0.117
155	0.061	–0.060	0.138	0.017
160	0.057	–0.064	0.081	–0.040
165	0.055	–0.066	0.057	–0.064

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Table 23–4—Normalized voltage templates as measured at the MDI *(continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
170	0.056	–0.065	0.054	–0.067
175	0.059	–0.062	0.058	–0.063
180	0.062	–0.059	0.063	–0.058
185	0.064	–0.057	0.064	–0.057
190	0.064	–0.057	0.063	–0.058
195	0.062	–0.059	0.060	–0.061
200	0.060	–0.061	0.058	–0.063
205	0.057	–0.064	0.058	–0.063
210	0.056	–0.065	0.059	–0.062
215	0.058	–0.063	0.060	–0.061
220	0.061	–0.060	0.062	–0.059
225	0.064	–0.057	0.062	–0.059
230	0.066	–0.055	0.062	–0.059
235	0.065	–0.056	0.061	–0.060
240	0.061	–0.060	0.060	–0.061
245	0.054	–0.067	0.060	–0.061
250	0.049	–0.072	0.060	–0.061
255	0.049	–0.072	0.060	–0.061
260	0.058	–0.063	0.061	–0.060
265	0.074	–0.047	0.061	–0.060
270	0.091	–0.030	0.061	–0.060
275	0.099	–0.022	0.061	–0.060
280	0.080	–0.041	0.060	–0.061
285	0.022	–0.099	0.060	–0.061
290	–0.085	–0.206	0.060	–0.061
295	–0.238	–0.359	0.060	–0.061
300	–0.423	–0.544	0.061	–0.060
305	–0.615	–0.736	0.061	–0.060
310	–0.783	–0.904	0.061	–0.060
315	–0.899	-1.020	0.061	–0.060
320	–0.940	-1.061	0.060	–0.061
325	–0.899	-1.020	0.060	–0.061
330	–0.786	–0.907	0.060	–0.061
335	–0.623	–0.744	0.060	–0.061

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Table 23–4—Normalized voltage templates as measured at the MDI *(continued)*

Time, ns	Normalized transmit template, pos. limit	Normalized transmit template, neg. limit	Normalized link template, pos. limit	Normalized link template, neg. limit
340	–0.439	–0.560	0.061	–0.060
345	–0.263	–0.384	0.061	–0.060
350	–0.118	–0.239	0.061	–0.060
355	–0.016	–0.137	0.061	–0.060
360	0.044	–0.077	0.060	–0.061
365	0.068	–0.053	0.060	–0.061
370	0.070	–0.051	0.060	–0.061
375	0.064	–0.057	0.060	–0.061
380	0.057	–0.064	0.061	–0.060
385	0.054	–0.067	0.061	–0.060
390	0.056	–0.065	0.061	–0.060
395	0.060	–0.061	0.061	–0.060
400	0.064	–0.057	0.060	–0.061
405	0.065	–0.056	0.060	–0.061
410	0.064	–0.057	0.060	–0.061
415	0.061	–0.060	0.060	–0.061
420	0.059	–0.062	0.061	–0.060
425	0.058	–0.063	0.061	–0.060
430	0.059	–0.062	0.061	–0.060
435	0.060	–0.061	0.061	–0.060
440	0.061	–0.060	0.060	–0.061
445	0.062	–0.059	0.060	–0.061
450	0.062	–0.059	0.060	–0.061
455	0.061	–0.060	0.060	–0.061
460	0.060	–0.061	0.061	–0.060
465	0.059	–0.062	0.061	–0.060
470	0.060	–0.061	0.061	–0.060
475	0.060	–0.061	0.061	–0.060
480	0.061	–0.060	0.060	–0.061

23.5.1.2.3 Differential output ISI (intersymbol interference)

While observing a pseudo-random 8B6T coded data sequence (with every 6T code group represented at least once) preceded by at least 128 octets and followed by at least 128 octets of data, and while observing the transmitted output through a 100BASE-T4 Transmit Test Filter (one implementation of which is

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depicted in Figure 23–16), the ISI shall be less than 9%. The ISI for this test is defined by first finding the largest of the three peak-to-peak ISI error voltages marked in Figure 23–15 as TOP ISI, MIDDLE ISI, and BOTTOM ISI.

The largest of these peak-to-peak ISI error voltages is then divided by the overall peak-to-peak signal voltage. (The technique of limiting the ratio of worst ISI to overall peak-to-peak voltage at 9% accomplishes the same end as limiting the ratio of worst ISI to nominal peak-to-peak at 10%.)

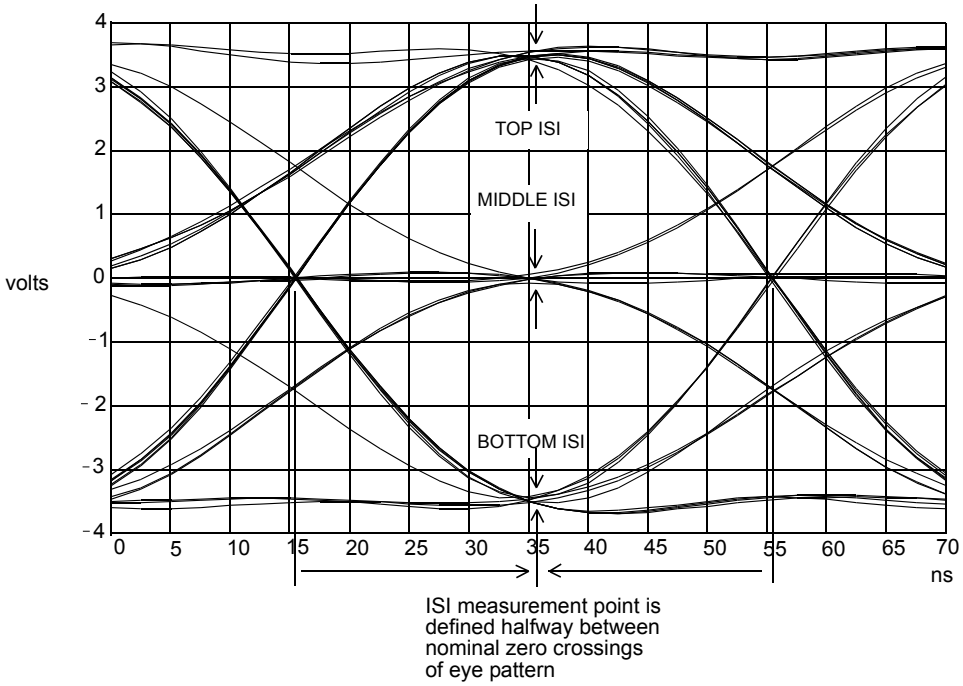


Figure 23–15—Definition of sampling points for ISI measurement

It is a mandatory requirement that the peak-to-peak ISI, and the overall peak-to-peak signal voltage, be measured at a point in time halfway between the nominal zero crossings of the observed eye pattern.

It is a mandatory requirement that the 100BASE-T4 Transmit Test Filter perform the function of a third-order Butterworth filter with its –3 dB point at 25.0 MHz.

One acceptable implementation of a 100BASE-T4 Transmit Test Filter appears in Figure 23–16. That implementation uses the 100BASE-T4 Transmit Test Filter as a line termination. The output of the filter is terminated in 100 Ω. It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed such that the reflection loss of the filter, when driven by a 100 Ω source, exceeds 17 dB across the frequency range 2 to 12.5 MHz.

Equivalent circuits that implement the same overall transfer function are also acceptable. For example, the 100BASE-T4 Transmit Test Filter may be tapped onto a line in parallel with an existing termination. It is a mandatory requirement that such implementations of the 100BASE-T4 Transmit Test Filter be designed with an input impedance sufficiently high that the reflection loss of the parallel combination of filter and 100 Ω termination, when driven by 100 Ω, exceeds 17 dB across the frequency range 2 to 12.5 MHz.

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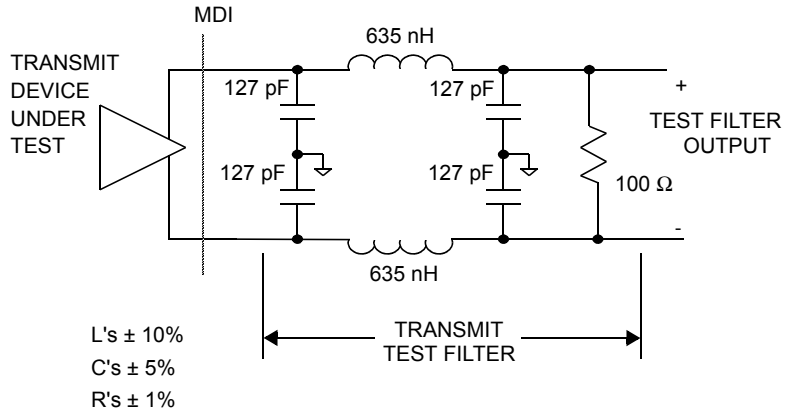


Figure 23–16—Acceptable implementation of transmit test filter

23.5.1.2.4 Transmitter differential output impedance

The differential output impedance as measured at the MDI for each transmit pair shall be such that any reflection due to differential signals incident upon the MDI from a balanced cable having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With every transmitter connected as in Figure 23–17, and while transmitting a repeating sequence of packets as specified in Table 23–5, the amount of droop on any transmit pair as defined in Figure 23–18 during the transmission of eop1 and eop4 shall not exceed 6.0%.

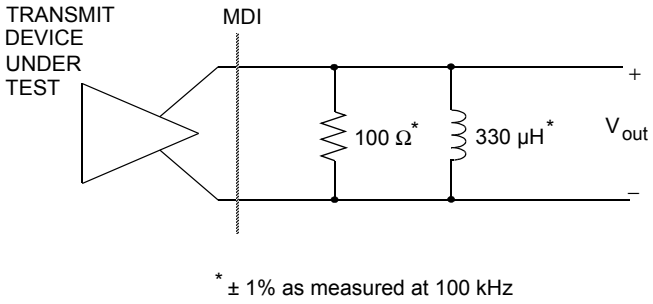


Figure 23–17—Output impedance test setup

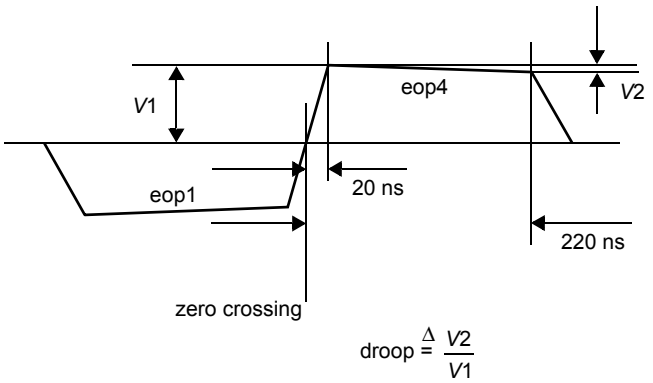


Figure 23–18—Measurement of output droop

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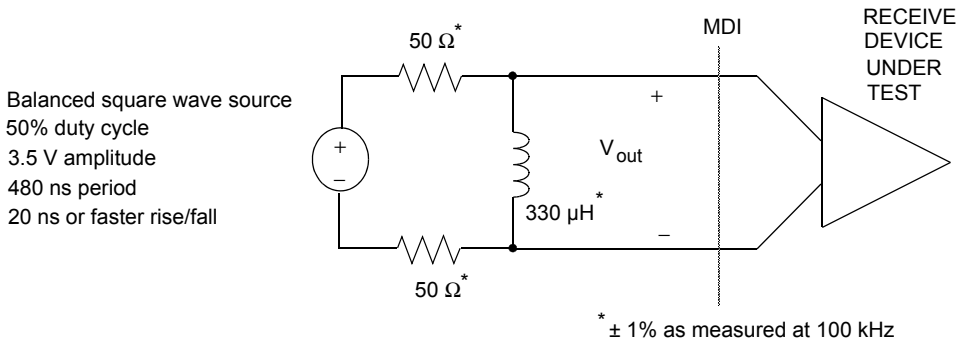


Figure 23–19—Input impedance test setup

Table 23–5—Sequence of packets for droop test

Packet sequence (Transmit this sequence of packets in a repetitive loop)	**Packet length** (Number of data octets)	**Data, hex** (All octets in each packet are the same)
First packet	64	AA
Second packet	65	AA
Third packet	66	AA

23.5.1.2.5 Output timing jitter

While repetitively transmitting a random sequence of valid 8B6T codewords, and while observing the output of a 100BASE-T4 Transmit Test Filter connected at the MDI to any of the transmit pairs as specified in 23.5.1.2.3, the measured jitter shall be no more than 4 ns p-p. For the duration of the test, each of the other transmit pairs shall be connected to either a 100BASE-T4 Transmit Test Filter or a 100 Ω resistive load.

NOTE 1—Jitter is the difference between the actual zero crossing point in time and the ideal time. For various ternary transitions, the zero crossing time is defined differently. For transitions between +1 and –1 or vice versa, the zero crossing point is defined as that point in time when the voltage waveform crosses zero. For transitions between zero and the other values, or from some other value to zero, the zero crossing time is defined as that point in time when the voltage waveform crosses the boundary between logical voltage levels, halfway between zero volts and the logical +1 or logical –1 ideal level.

NOTE 2—The ideal zero crossing times are contained in a set of points $\{t_n\}$ where $t_n = t_0 + n/f$, where n is an integer, and f is in the range 25.000 MHz ± 0.01%. A collection of zero crossing times satisfies the jitter requirement if there exists a pair (t_0, f) such that each zero crossing time is separated from some member of $\{t_n\}$ by no more than 4 ns.

23.5.1.2.6 Transmitter impedance balance

The common-mode to differential-mode impedance balance of each transmit output shall exceed

$$29 - 17\log\left(\frac{f}{10}\right)\text{dB}$$

where f is the frequency (in MHz) over the frequency range 2.0 MHz to 12.5 MHz. The balance is defined as

$$20\log\left(\frac{E_{\text{cm}}}{E_{\text{dif}}}\right)$$

where E_{cm} is an externally applied sine-wave voltage as shown in Figure 23–20.

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NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

23.5.1.2.7 Common-mode output voltage

The implementer should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment. FCC conducted and radiated emissions tests may require that, while transmitting data, the magnitude of the total common-mode output voltage, $E_{cm(out)}$, on any transmit circuit, be less than a few millivolts when measured as shown in Figure 23–21.

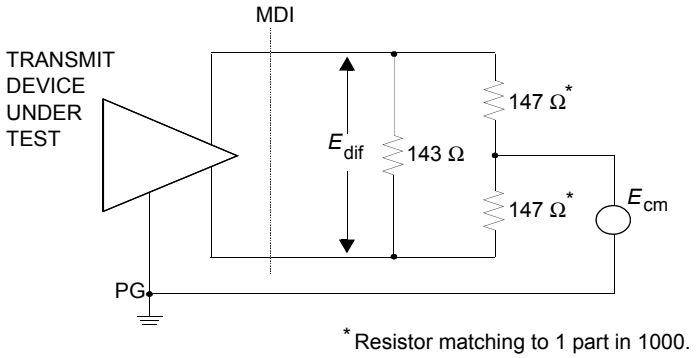


Figure 23–20—Transmitter impedance balance and common-mode rejection test circuit

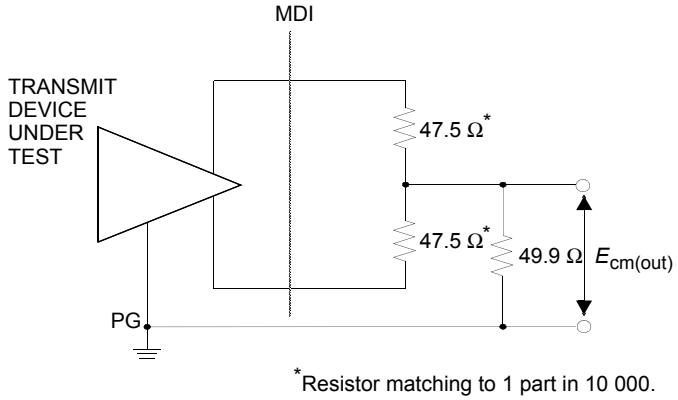


Figure 23–21—Common-mode output voltage test circuit

23.5.1.2.8 Transmitter common-mode rejection

The application of E_{cm} as shown in Figure 23–20 shall not change the differential voltage at any transmit output, E_{dif}, by more than 100 mV for all data sequences while the transmitter is sending data. Additionally, the edge jitter added by the application of E_{cm} shall be no more than 1.0 ns. E_{cm} shall be a 15 V peak 10.1 MHz sine wave.

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23.5.1.2.9 Transmitter fault tolerance

Transmitters, when either idle or nonidle, shall withstand without damage the application of short circuits across any transmit output for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 420 mA.

Transmitters, when either idle or nonidle, shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 23–22). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

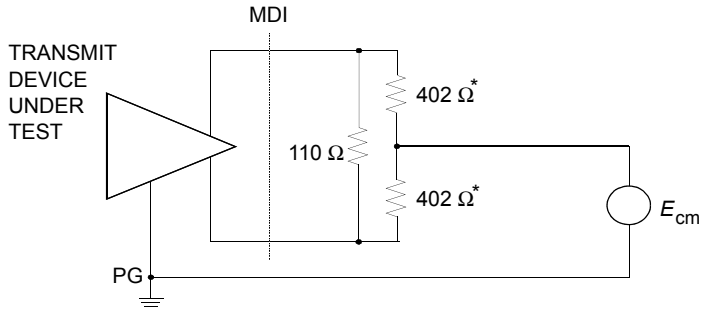


Figure 23–22—Transmitter fault tolerance test circuit

23.5.1.2.10 Transmit clock frequency

The ternary symbol transmission rate on each pair shall be 25.000 MHz ± 0.01%.

23.5.1.3 Receiver specifications

The PMA shall provide the Receive function specified in 23.4.1.3 in accordance with the electrical specifications of this clause. The patch cables and interconnecting hardware used in test configurations shall meet Category 5 specifications as in ISO/IEC 11801: 1995.

The term *worst-case UTP model*, as used in this clause, refers to lumped-element cable model shown in Figure 23–23 that has been developed to simulate the attenuation and group delay characteristics of 100 m of worst-case Category 3 PVC UTP cable.

This constant resistance filter structure has been optimized to best match the following amplitude and group delay characteristics, where the argument f is in hertz, and the argument x is the cable length in meters. For the worst-case UTP model, argument x was set to 100 m, and the component values determined for a best least mean squared fit of both real and imaginary parts of $H(f, x)$ over the frequency range 2 to 15 MHz.

NOTE—This group delay model is relative and does not includes the fixed delay associated with 100 m of Category 3 cable. An additional 570 ns of fixed delay should be added in order to obtain the absolute group delay.

$$PropagationImag(f, x) = j(-10)\sqrt{\frac{f}{10^7}}\left(\frac{x}{100}\right)$$

$$PropagationReal(f, x) = -\left(7.1\sqrt{\frac{f}{10^6}} + 0.70\frac{f}{10^6}\right)\left(\frac{x}{305}\right)$$

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$$H(f,x) = 10^{\frac{PropagationImag(f,x) + PropagationReal(f,x)}{20}}$$

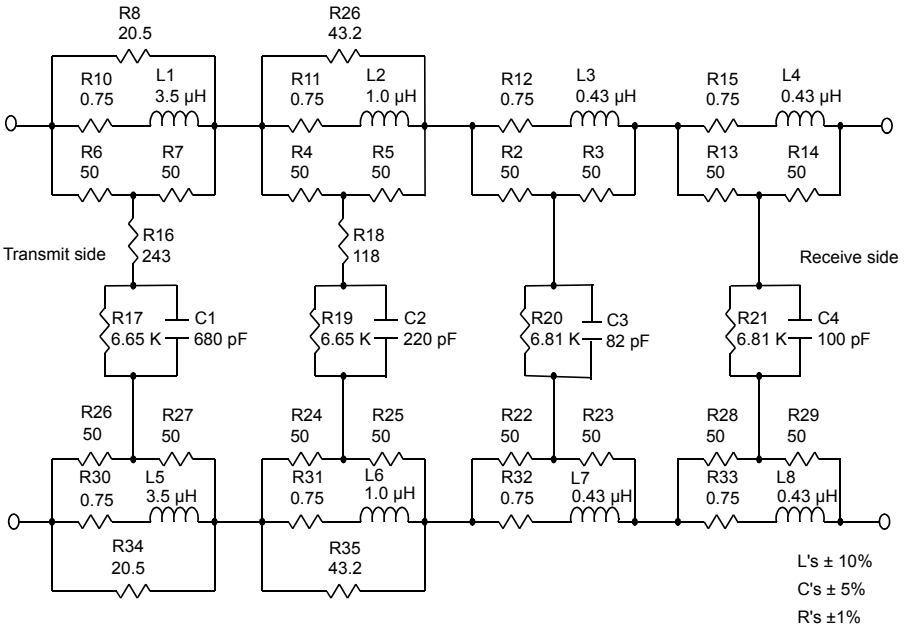


Figure 23–23—Worst-case UTP model

23.5.1.3.1 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the constraints of 23.5.1.2, and have then passed through a worst-case UTP model, shall be correctly translated into one of the PMA_UNITDATA.indication messages and sent to the PCS. In addition, the receiver, when presented with a link test pulse generated according to the requirements of 23.4.1.2 and followed by at least 3T of silence on pair RX_D2, shall accept it as a link test pulse.

Both data and link test pulse receive features shall be tested in at least two configurations: using the worst-case UTP model, and with a connection less than one meter in length between transmitter and receiver.

A receiver is allowed to discard the first received packet after the transition into state LINK_PASS, using that packet for the purpose of fine-tuning its receiver equalization and clock recovery circuits.

NOTE—Implementers may find it practically impossible to meet the requirements of this subclause without using some form of adaptive equalization.

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23.5.1.3.2 Receiver differential noise immunity

The PMA, when presented with 8B6T encoded data meeting the requirements of 23.5.1.3.1, shall translate this data into PMA_UNITDATA.indication (DATA) messages with a bit loss of no more than that specified in 23.4.1.3.

The PMA Carrier Sense function shall *not* set pma_carrier=ON upon receiving any of the following signals on pair RX_D2 at the receiving MDI, as measured using a 100BASE-T4 transmit test filter (23.5.1.2.3):

a) All signals having a peak magnitude less than 325 mV.
b) All continuous sinusoidal signals of amplitude less than 8.7 V peak-to-peak and frequency less than 1.7 MHz.
c) All sine waves of single cycle or less duration, starting with phase 0° or 180°, and of amplitude less than 8.7 V peak-to-peak, where the frequency is between 1.7 MHz and 15 MHz. For a period of 7 BT before and after this single cycle, the signal shall be less than 325 mV.
d) Fast link pulse burst (FLP burst), as defined in Clause 28.
e) The link integrity test pulse signal TP_IDL_100.

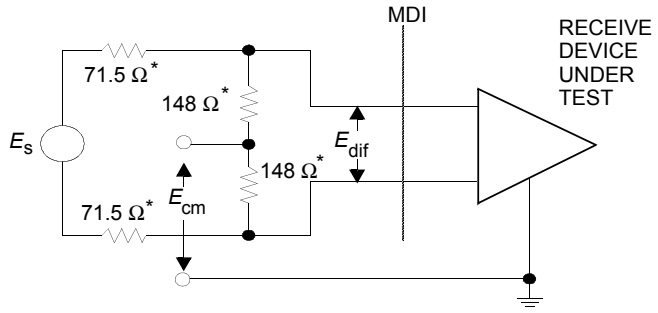
23.5.1.3.3 Receiver differential input impedance

The differential input impedance as measured at the MDI for each receive input shall be such that any reflection due to differential signals incident upon each receive input from a balanced cable having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 12.5 MHz. This return loss shall be maintained at all times when the PHY is fully powered.

With each receiver connected as in Figure 23–19, and with the source adjusted to simulate eop1 and eop4 (50% duty cycle square wave with 3.5 V amplitude, period of 480 ns, and risetime of 20 ns or faster), the amount of droop on each receive pair as defined in Figure 23–18 shall not exceed 6.0%.

23.5.1.3.4 Common-mode rejection

While receiving packets from a compliant 100BASE-T4 transmitter connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indication messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 23.5.1.3.1 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 23–24). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%), connected to each of the receive pairs RX_D2, BI_D3, and BI_D4.



*Resistor matching to 1 part in 1000.

Figure 23–24—Receiver common-mode rejection test circuit

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23.5.1.3.5 Receiver fault tolerance

The receiver shall tolerate the application of short circuits between the leads of any receive input for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity (E_{cm} as indicated in Figure 23–25). The shape of the impulse shall be 0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value), as defined in IEC 60060.

23.5.1.3.6 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a ternary symbol rate within the range 25.000 MHz ± 0.01%.

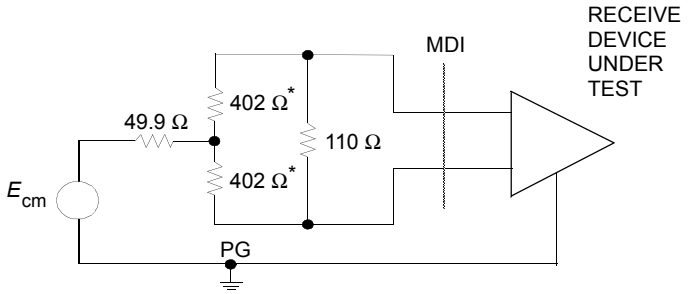


Figure 23–25—Common-mode impulse test circuit

23.5.2 Power consumption

After 100 ms following PowerOn, the current drawn by the PHY shall not exceed 0.75 A when powered through the MII.

The PHY shall be capable of operating from all voltage sources allowed by Clause 22, including those current limited to 0.75 A, as supplied by the DTE or repeater through the resistance of all permissible MII cables.

The PHY shall not introduce extraneous signals on the MII control circuits during normal power-up and power-down.

While in power-down mode the PHY is not required to meet any of the 100BASE-T4 performance requirements.

23.6 Link segment characteristics

23.6.1 Cabling

Cabling and installation practices generally suitable for use with this standard appear in ISO/IEC 11801: 1995. Exceptions, notes, and additional requirements are as follows:

a) 100BASE-T4 uses a star topology. Horizontal cabling is used to connect PHY entities.

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b) 100BASE-T4 is an ISO/IEC 11801: 1995 class C application, with additional installation requirements and transmission parameters specified in 23.6.2 through 23.6.4. The highest fundamental frequency transmitted by 8B6T coding is 12.5 MHz. The aggregate data rate for three pairs using 8B6T coding is 100 Mb/s.
c) 100BASE-T4 shall use four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω.
d) When using Category 3 cable for the link segment, Clause 23 recommends, but does not require, the use of Category 4 or better connecting hardware, patch cords and jumpers. The use of Category 4 or better connecting hardware increases the link segment composite NEXT loss, composite ELFEXT loss and reduces the link segment insertion loss. This lowers the link segment crosstalk noise, which in turn decreases the probability of errors.
e) The use of shielded cable is outside the scope of this standard.

23.6.2 Link transmission parameters

Unless otherwise specified, link segment testing shall be conducted using source and load impedances of 100 Ω.

23.6.2.1 Insertion loss

The insertion loss of a simplex link segment shall be no more than 12 dB at all frequencies between 2 MHz and 12.5 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 23.5.1.2.4 and 23.5.1.3.3.

NOTE—The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as many Fluorinated Ethylene Propylene (FEP), Polytetrafluoroethylene (PTFE), or Perfluoroalkoxy (PFA) plenum-rated cables.

23.6.2.2 Differential characteristic impedance

The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link shall be between 85 Ω and 115 Ω for all frequencies between 2 MHz and 12.5 MHz.

23.6.2.3 Coupling parameters

In order to limit the noise coupled into a simplex link segment from adjacent simplex link segments, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each simplex link segment. In addition, since three simplex links (TX_D1, Bl_D3, and Bl_D4) are used to send data between PHYs and one simplex link (RX_D2) is used to carry collision information as specified in 23.1.4, Multiple-Disturber NEXT loss and Multiple-Disturber ELFEXT loss are also specified.

23.6.2.3.1 Differential Near-End Crosstalk (NEXT) loss

The differential Near-End Crosstalk (NEXT) loss between two simplex link segments is specified in order to ensure that collision information can be reliably received by the PHY receiver. The NEXT loss between each of the three data carrying simplex link segments and the collision sensing simplex link segment shall be at least $24.5 - 15 \times \log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz.

23.6.2.3.2 Multiple-disturber NEXT (MDNEXT) loss

Since three simplex links are used to send data between PHYs and one simplex link is used to carry collision information, the NEXT noise that is coupled into the collision, sensing simplex link segment is from multiple (three) signal sources, or disturbers. The MDNEXT loss between the three data carrying simplex link

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segments and the collision sensing simplex link segment shall be at least $21.4 - 15\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 to 12.5 MHz. Refer to 12.7.3.2 and Annex B.3 Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDNEXT loss for an n-pair cable.

23.6.2.3.3 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of a simplex link segment to meet the BER objective specified in 23.1.2 and the noise specifications of 23.6.3. Far-End Crosstalk (FEXT) noise is the crosstalk noise that appears at the far end of a simplex link segment which is coupled from an adjacent simplex link segment with the noise source (transmitters) at the near end. ELFEXT loss is the ratio of the data signal to FEXT noise at the output of a simplex link segment (receiver input). To limit the FEXT noise from adjacent simplex link segments, the ELFEXT loss between two data carrying simplex link segments shall be greater than $23.1 - 20\times\log_{10}(f/12.5)$ dB (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. ELFEXT loss at frequency f and distance l is defined as

$$\text{ELFEXT\_Loss}(f,l) = 20 \times \log_{10}\left(\frac{V_{pds}}{V_{pcn}}\right) - \text{SLS\_Loss (dB)}$$

where

V_{pds} is the peak voltage of disturbing signal (near-end transmitter)
V_{pcn} is the peak crosstalk noise at the far end of disturbed simplex link segment
SLS_Loss is the insertion loss of the disturbing simplex link segment

23.6.2.3.4 Multiple-disturber ELFEXT (MDELFEXT) loss

Since three simplex links are used to transfer data between PHYs, the FEXT noise that is coupled into an data carrying simplex link segment is from multiple (two) signal sources, or disturbers. The MDELFEXT loss between a data carrying simplex link segment and the other two data carrying simplex link segments shall be greater than $20.9 - 20\times\log_{10}(f/12.5)$ (where f is the frequency in MHz) over the frequency range 2.0 MHz to 12.5 MHz. Refer to 12.7.3.2 and Annex B.3, Example Crosstalk Computation for Multiple Disturbers, for a tutorial and method for estimating the MDELFEXT loss for an n-pair cable.

23.6.2.4 Delay

Since T4 sends information over three simplex link segments in parallel, the absolute delay of each and the differential delay are specified to comply with network round-trip delay limits and ensure the proper decoding by receivers, respectively.

23.6.2.4.1 Maximum link delay

The propagation delay of a simplex link segment shall not exceed 570 ns at all frequencies between 2.0 MHz and 12.5 MHz.

23.6.2.4.2 Maximum link delay per meter

The propagation delay per meter of a simplex link segment shall not exceed 5.7 ns/m at all frequencies between 2.0 MHz and 12.5 MHz.

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23.6.2.4.3 Difference in link delays

The difference in propagation delay, or skew, under all conditions, between the fastest and the slowest simplex link segment in a link segment shall not exceed 50 ns at all frequencies between 2.0 MHz and 12.5 MHz. It is a further functional requirement that, once installed, the skew between all pair combinations due to environmental conditions shall not vary more than ± 10 ns, within the above requirement.

23.6.3 Noise

The noise level on the link segments shall be such that the objective error ratio is met. The noise environment consists generally of two primary contributors: self-induced near-end crosstalk, which affects the ability to detect collisions, and far-end crosstalk, which affects the signal-to-noise ratio during packet reception.

23.6.3.1 Near-End Crosstalk

The MDNEXT (Multiple-Disturber Near-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the crosstalk loss between those pairs and the disturbed pair, RX_D2.

The MDNEXT noise on a link segment shall not exceed 325 mVp.

This standard is compatible with the following assumptions:

a) Three disturbing pairs with 99th percentile pair-to-pair NEXT loss greater than 24.5 dB at 12.5 MHz (i.e., Category 3 cable).
b) Six additional disturbers (2 per simplex link) representing connectors at the near end of the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz (i.e., Category 3 connectors installed in accordance with 23.6.4.1).
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

The MDNEXT noise is defined using three maximum level 100BASE-T4 transmitters sending uncorrelated continuous data sequences while attached to the simplex link segments TX_D1, BI_D3, and BI_D4 (disturbing links), and the noise measured at the output of a filter connected to the simplex link segment RX_D2. (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.3.2 Far-End Crosstalk

The MDFEXT (Multiple-Disturber Far-End Crosstalk) noise on a link segment depends on the level of the disturbing signals on pairs TX_D1, BI_D3, and BI_D4, and the various crosstalk losses between those pairs.

The MDFEXT noise on a link segment shall not exceed 87 mVp.

This standard is compatible with the following assumptions:

a) Two disturbing pairs with 99th percentile ELFEXT (Equal Level Far-End Crosstalk) loss greater than 23 dB at 12.5 MHz.
b) Nine additional disturbers (three per simplex link) representing connectors in the link segment with 99th percentile NEXT loss greater than 40 dB at 12.5 MHz.
c) All disturbers combined according to the MDNEXT Monte Carlo procedure outlined in Appendix A3, Example Crosstalk Computation for Multiple Disturbers.

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The MDFEXT noise is defined using two maximum level 100BASE-T4 transmitters sending uncorrelated continuous data sequences while attached to two simplex link segments (disturbing links) and the noise measured at the output of a filter connected to the far end of a third simplex link segment (disturbed link). Each continuous data sequence is a pseudo-random bit pattern having a length of at least 2047 bits that has been coded according to the 8B6T coding rules in 23.2.1.2. The filter is the 100BASE-T4 Transmit Test Filter specified in 23.5.1.2.3.

23.6.4 Installation practice

23.6.4.1 Connector installation practices

The amount of untwisting in a pair as a result of termination to connecting hardware should be no greater than 25 mm (1.0 in) for Category 3 cables. This is the same value recommended in ISO/IEC 11801: 1995 for Category 4 connectors.

23.6.4.2 Disallow use of Category 3 cable with more than four pairs

Jumper cables, or horizontal runs, made from more than four pairs of Category 3 cable are not allowed.

23.6.4.3 Allow use of Category 5 jumpers with up to 25 pairs

Jumper cables made from up to 25 pairs of Category 5 cable, for the purpose of mass-terminating port connections at a hub, are allowed. Such jumper cables, if used, shall be limited in length to no more than 10 m total.

23.7 MDI specification

This clause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this clause.

23.7.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and figures 1 through 5 of IEC 60603-7: 1990 shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figure 23–26 and Figure 23–27. Table 23-6 shows the assignment of PMA signals to connector contacts for PHYs with and without an internal crossover.

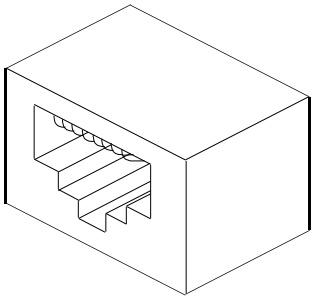


Figure 23–26—MDI connector

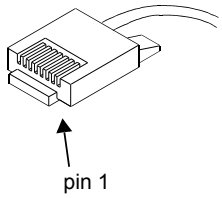


Figure 23–27—Balanced cabling connector

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Table 23-6—MDI connection and labeling requirements

Contact	PHY without internal crossover (recommended for DTE) internal PMA signals	PHY with internal crossover (recommended for repeater) internal PMA signals	MDI labeling requirement
1	TX_D1+	RX_D2+	TX_D1+
2	TX_D1–	RX_D2–	TX_D1–
3	RX_D2+	TX_D1+	RX_D2+
4	BI_D3+	BI_D4+	BI_D3+
5	BI_D3–	BI_D4–	BI_D3–
6	RX_D2–	TX_D1–	RX_D2–
7	BI_D4+	BI_D3+	BI_D4+
8	BI_D4–	BI_D3–	BI_D4–

23.7.2 Crossover function

It is a functional requirement that a crossover function be implemented in every link segment. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the last column of Table 23–4 refer to its own internal circuits (second column). For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 23–4 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol “X”. Internal and external crossover functions are shown in Figure 23–28. The crossover function specified here for pairs TX_D1 and RX_D2 is compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

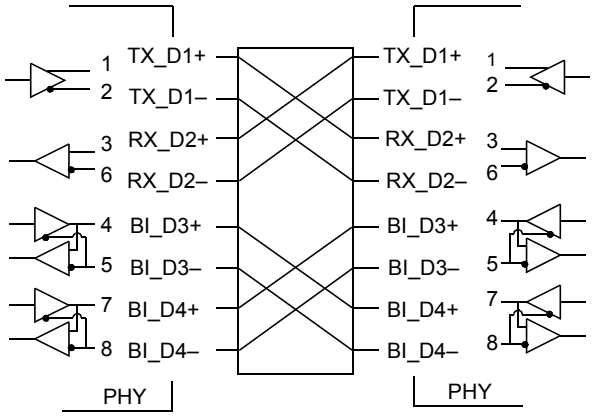
When a link segment connects a DTE to a repeater, it is recommended the crossover be implemented in the PHY local to the repeater. If both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central repeater that the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

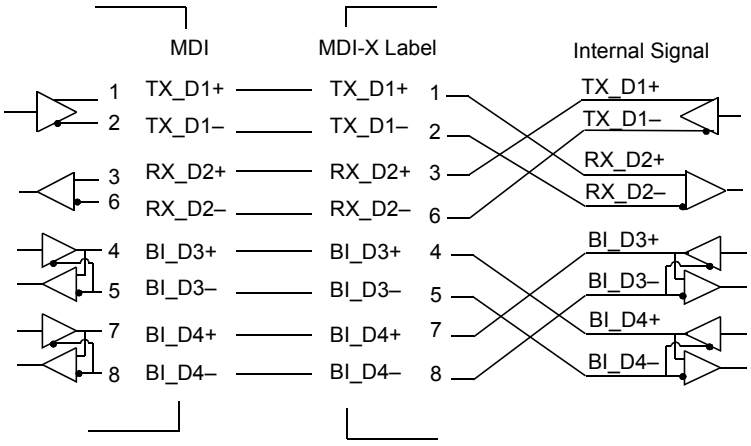
23.8 System considerations

The repeater unit specified in Clause 27 forms the central unit for interconnecting 100BASE-T4 twisted-pair links in networks of more than two nodes. It also provides the means for connecting 100BASE-T4 twisted-pair links to other 100 Mb/s baseband segments. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in Clause 29.

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a) Two PHYs with external crossover function



b) PHY with internal crossover function

Figure 23–28—Crossover function

23.9 Environmental specifications

23.9.1 General safety

All equipment meeting this standard shall conform to IEC 60950: 1991.

23.9.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits
b) Static charge buildup on LAN cables and components
c) High-energy transients coupled onto the LAN cable system

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d) Voltage potential differences between safety grounds to which various LAN components are connected

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

23.9.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

23.9.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING

It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a "doubly insulated, ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

23.9.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cable plant, care be taken to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

23.9.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 100BASE-T4 equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 100BASE-T4 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 100BASE-T4 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

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23.9.3 Environment

23.9.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

23.9.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

23.10 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Any applicable safety warnings

See also 23.7.2.

23.11 Timing summary

23.11.1 Timing references

All MII signals are defined (or corrected to) the DTE end of a zero length MII cable.

NOTE—With a finite length MII cable, TX_CLK appears in the PHY one cable propagation delay *earlier* than at the MII. This advances the transmit timing. Receive timing is retarded by the same amount.

The phrase *adjusted for pair skew*, when applied to a timing reference on a particular pair, means that the designated timing reference has been adjusted by adding to it the difference between the time of arrival of preamble on the latest of the three receive pairs and the time of arrival of preamble on that particular pair.

PMA_UNITDATA.request

Figures 23–29, 23–30, 23–31, and 23–32. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PMA has been given full knowledge and use of the ternary symbols to be transmitted.

PMA_UNITDATA.indication

Figure 23–33. The implementation of this abstract message is not specified. Conceptually, this is the time at which the PCS has been given full knowledge and use of the ternary symbols received.

WAVEFORM

Figure 23–29. Point in time at which output waveform has moved 1/2 way from previous nominal output level to present nominal output level.

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TX_EN

Figure 23–30. First rising edge of TX_CLK following the rising edge of TX_EN.

NOT_TX_EN

Figure 23–31 and Figure 23–32. First rising edge of TX_CLK following the falling edge of TX_EN.

CRS

Figure 23–33. Rising edge of CRS.

CARRIER_STATUS

Figure 23–33. Rising edge of carrier_status.

NOT_CARRIER_STATUS

Figure 23–34. Falling edge of carrier_status.

RX_DV

No figure. First rising edge of RX_CLK following rising edge of RX_DV.

COL

No figure. Rising edge of COL signal at MII.

NOT_COL

No figure. Falling edge of COL signal at MII.

PMA_ERROR

No figure. Time at which rxerror_status changes to ERROR.

23.11.2 Definitions of controlled parameters

PMA_OUT

Figure 23–29. Time between PMA_UNITDATA.request (tx_code_vector) and the WAVEFORM timing reference for each of the three transmit channels TX_D1, BI_D3, or BI_D4.

TEN_PMA

Figure 23–30, Figure 23–31, and Figure 23–32. Time between TX_EN timing reference and MA_UNITDATA.request (tx_code_vector).

TEN_CRS

Figure 23–30. Time between TX_EN timing reference and the loopback of TX_EN to CRS as measured at the CRS timing reference point.

NOT_TEN_CRS

Figure 23–31 and Figure 23–32. Time between NOT_TX_EN timing reference and the loopback of TX_EN to CRS as measured at the NOT_CRS timing reference point. In the event of a collision (COL is raised at any point during a packet) the minimum time for NOT_TEN_CRS may optionally be as short as 0.

RX_PMA_CARRIER

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CARRIER_STATUS timing reference.

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RX_CRS

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the CRS timing reference.

NOTE—The input waveform used for this test is an ordinary T4 preamble, generated by a compliant T4 transmitter. As such, the delay between the first and third pulses of the preamble (which are used by the carrier sense logic) is very nearly 80 ns.

RX_NOT_CRS

For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the first pulse of eop1, and the deassertion of CRS. For a collision fragment, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair TX_D2, which follows the last ternary data symbol received on pair RX_D2, and the deassertion of CRS.

Both are limited to the same value. For a data packet, detection of the six ternary symbols of eopo1 is accomplished in the PCS layer. For a collision fragment, detection of the concluding seven ternary zeros is accomplished in the PMA layer, and passed to the PCS in the form of the carrier_status indication.

FAIRNESS

The difference between RX_NOT_CRS at the conclusion of one packet and RX_CRS on a subsequent packet. The packets used in this test may arrive with an IPG anywhere in the range of 80 to 160.

RX_PMA_DATA

Figure 23–33. Time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the particular PMA_UNITDATA.indication that transfers to the PCS the first ternary symbol of the first 6T code group from receive pair BI_D3.

EOP_CARRIER_STATUS

Figure 23–34. For a data packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of first pulse of eop1 and the NOT_CARRIER_STATUS timing reference.

EOC_CARRIER_STATUS

Figure 23–35. In the case of a colliding packet, the time between the WAVEFORM timing reference, adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_CARRIER_STATUS timing reference.

RX_RXDV

No figure. Time between WAVEFORM timing reference, adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse) and the RX_DV timing reference.

RX_PMA_ERROR

No figure. In the event of a preamble in error, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of that preamble (or first pulse of the preamble preceded by a link test pulse or a partial link test pulse), and the PMA_ERROR timing reference.

RX_COL

No figure. In the event of a collision, the time between the WAVEFORM timing reference adjusted for pair skew, of first pulse of a normal preamble (or first pulse of a preamble preceded by a link test pulse or a partial link test pulse), and the COL timing reference.

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RX_NOT_COL

No figure. In the event of a collision in which the receive signal stops before the locally transmitted signal, the time between the WAVEFORM timing reference adjusted for pair skew, of the ternary symbol on pair RX_D2, which follows the last ternary data symbol received on pair RX_D2 and the NOT_COL timing reference point.

TX_NOT_COL

No figure. In the event of a collision in which the locally transmitted signal stops before the received signal, the time between the NOT_TX_EN timing reference and the loopback of TX_EN to COL as measured at the NOT_COL timing reference point.

TX_SKEW

Greatest absolute difference between a) the waveform timing reference of the first pulse of a preamble as measured on output pair TX_D1; b) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D3; and c) the waveform timing reference of the first pulse of a preamble as measured on output pair BI_D4. Link test pulses, if present during the measurement, must be separated from the preamble by at least 100 ternary symbols.

CRS_PMA_DATA

Time between the timing reference for CARRIER STATUS and the transfer, via PMA_UNITDATA.indication, of the first ternary symbol of the 6T code group marked DATA1 in Figure 23–6.

COL_to_BI_D3/D4_OFF

No figure. In the case of a colliding packet, the time between the WAVE FORM timing reference, adjusted for pair skew, of the first pulse of preamble (or the first pulse of the preamble preceded by a link test pulse or a partial link test pulse) on RX_D2, and the first ternary zero transmitted on BI_D3 and on BI_D4.

NOTE—Subclause 23.4.1.2 mandates that transmission on pairs BI_D3 and BI_D4 be halted in the event of a collision.

23.11.3 Table of required timing values

While in the LINK_PASS state, each PHY timing parameter shall fall within the Low and High limits listed in Table 23–7. All units are in bit times. A bit time equals 10 ns.

Table 23–7—Required timing values

Controlled parameter	Low limit (bits)	High limit (bits)	Comment
PMA_OUT	1	9.5	
TEN_PMA + PMA_OUT	7	17.5	
TEN_CRS	0	+4	
NOT_TEN_CRS	0	36	
RX_PMA_CARRIER	0	15.5	
RX_CRS	0	27.5	
RX_NOT_CRS	0	51.5	

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Table 23–7—Required timing values *(continued)*

Controlled parameter	Low limit (bits)	High limit (bits)	Comment
FAIRNESS	0	28	
RX_PMA_DATA	67	90.5	
EOP_CARRIER_STATUS	51	74.5	
EOC_CARRIER_STATUS	3	50.5	
RX_RXDV	81	114.5	
RX_PMA_ERROR	RX_PMA_DATA	RX_PMA_DATA + 20	Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
RX_COL	0	27.5	SAME AS RX_CRS
RX_NOT_COL	0	51.5	SAME AS RX_NOT_CRS
TX_NOT_COL	0	36	
TX_SKEW	0	0.5	
CRS_PMA_DATA	0	78.5	
COL_to_BI_D3/D4_OFF	0	40	

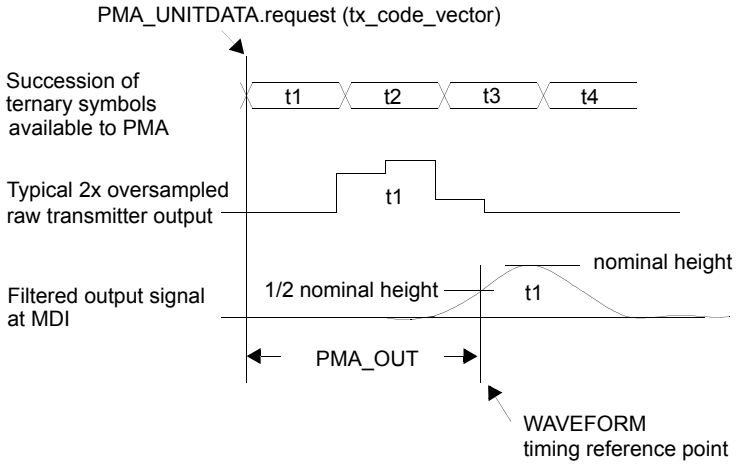


Figure 23–29—PMA TRANSMIT timing while tx_code_vector = DATA

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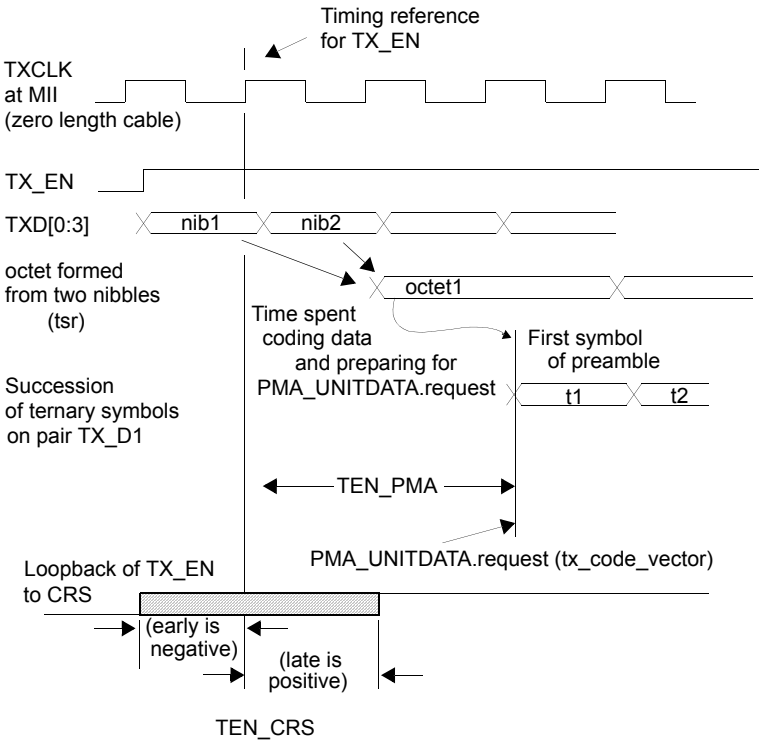


Figure 23–30—PCS TRANSMIT timing at start of packet

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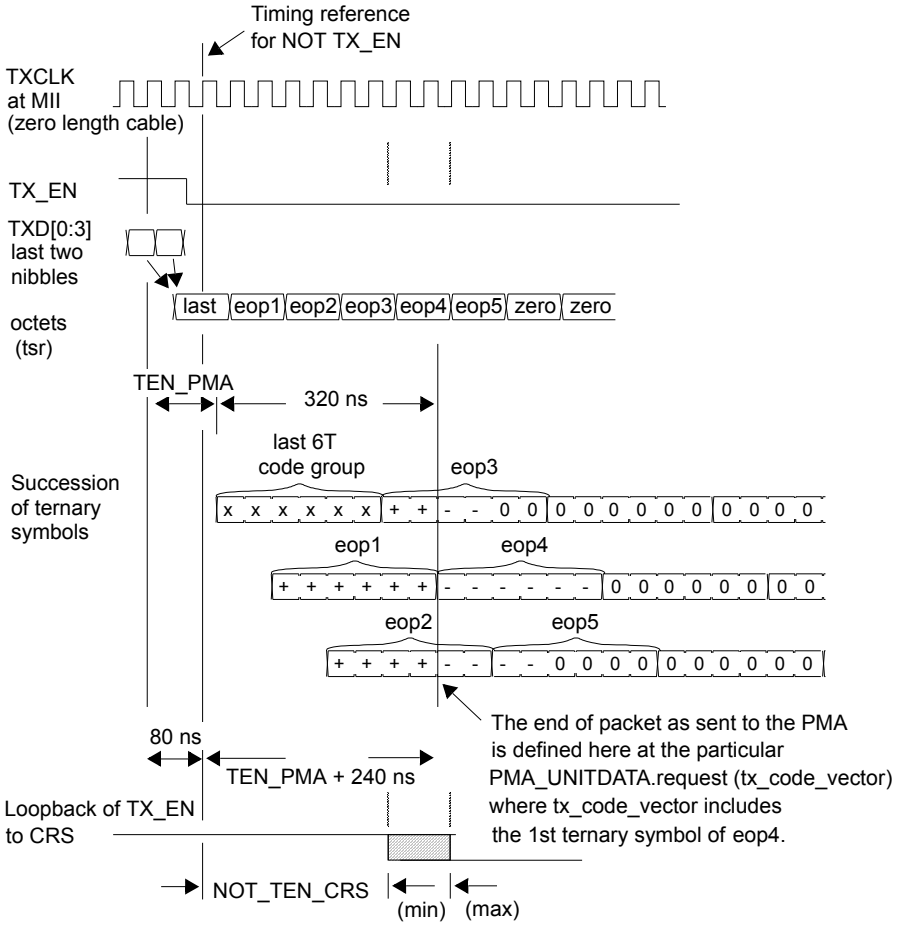


Figure 23–31—PCS TRANSMIT timing end of normal packet

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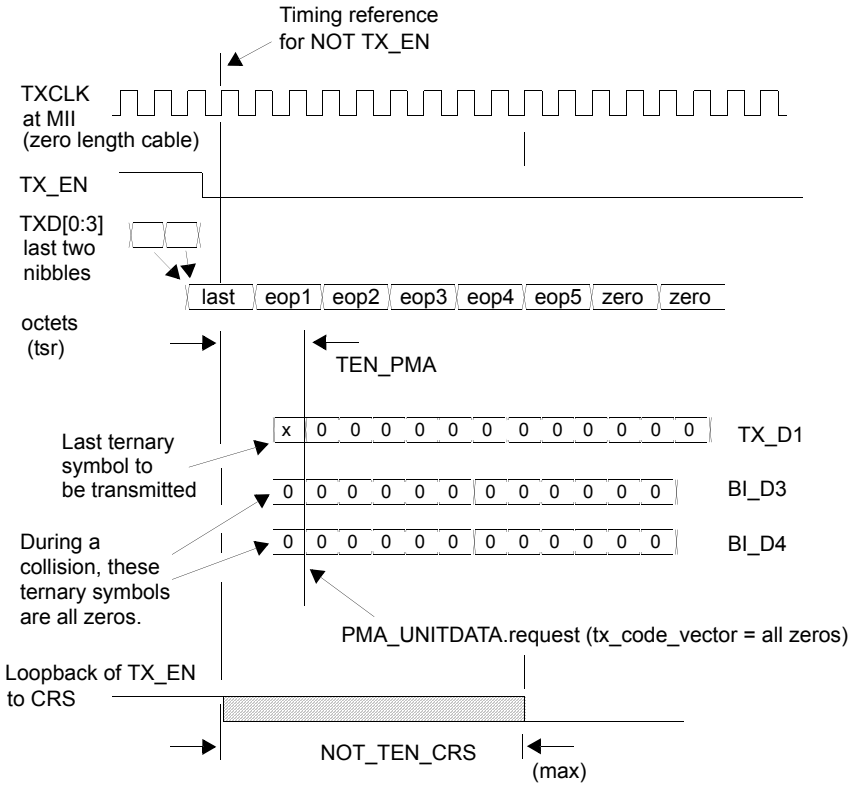


Figure 23–32—PCS TRANSMIT timing end of colliding packet

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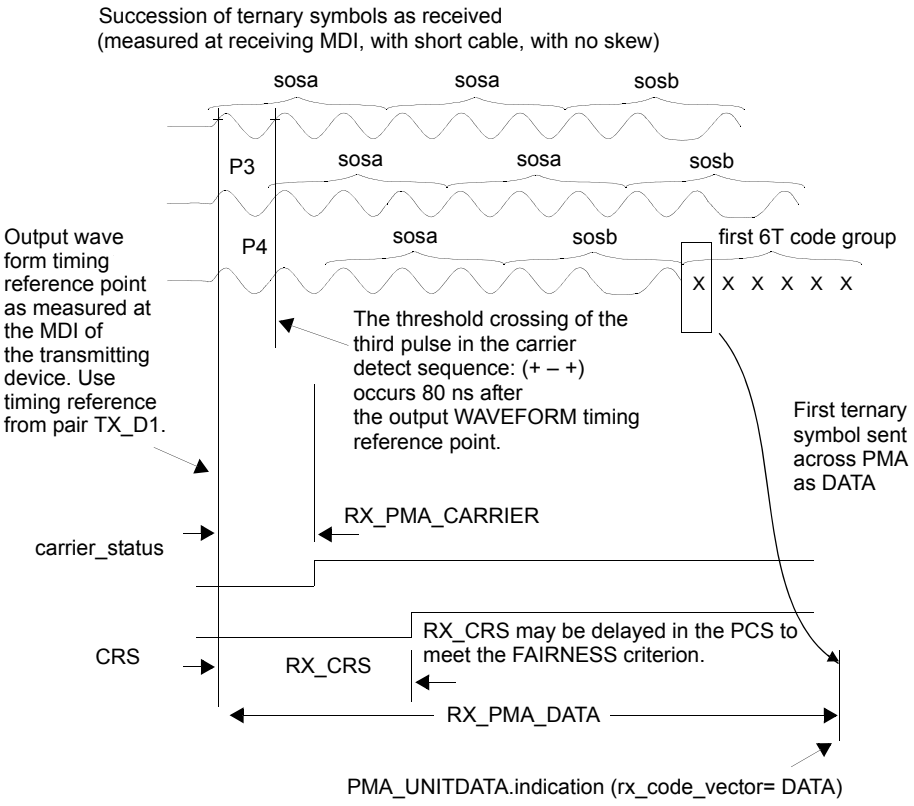
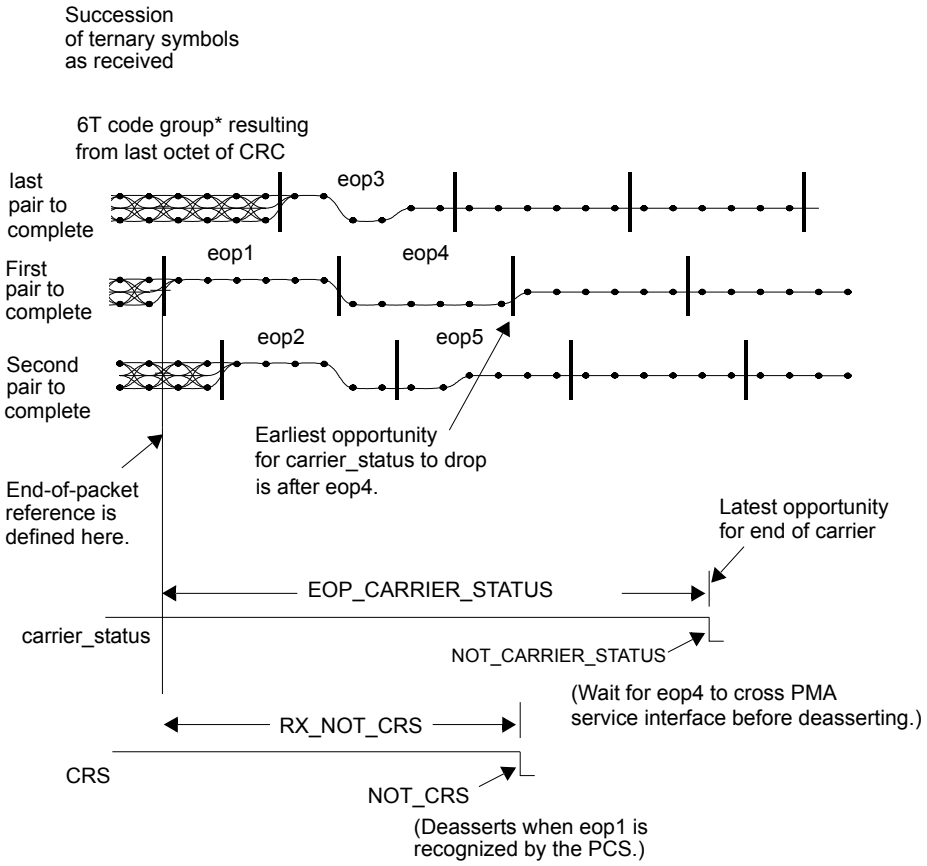


Figure 23–33—PMA RECEIVE timing start of packet

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*RX_DV deasserts after sending the last nibble of this decoded octet across the MII. CRS may deassert prior to that time.

Figure 23–34—PMA RECEIVE timing end of normal packet

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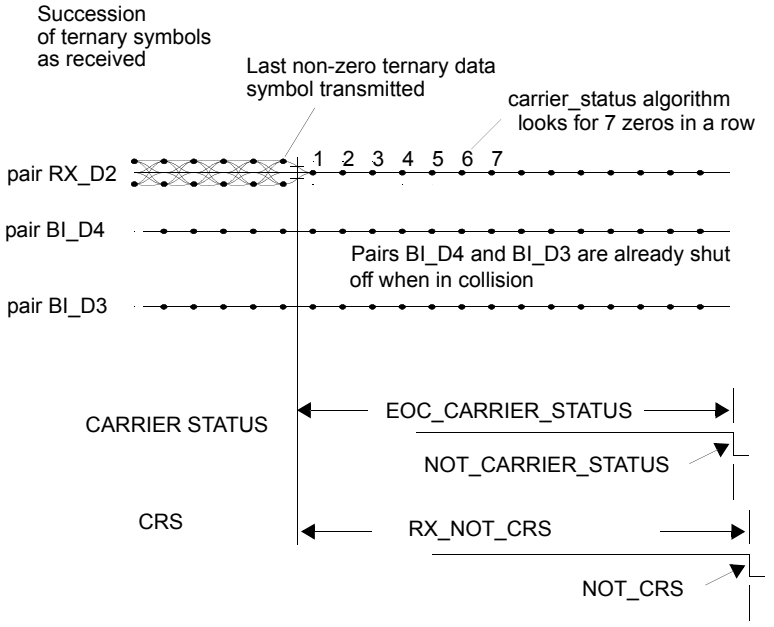


Figure 23–35—PMA RECEIVE timing end of colliding packet

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23.12 Protocol implementation conformance statement (PICS) proforma for Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4[4]

23.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

23.12.2 Identification

23.12.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

23.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2012, Clause 23, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100BASE-T4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2012.)	

Date of Statement	

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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23.12.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*MII	Exposed MII interface	23.1.5.3	O		Devices supporting this option must also support the PCS option
*PCS	PCS functions	23.1.5.2	O		Required for integration with DTE or MII
*PMA	Exposed PMA service interface	23.1.5.2	O		Required for integration into symbol level repeater core
*XVR	Internal wiring crossover	23.7.2	O		Usually implemented in repeater, usually not in DTE
*NWY	Support for optional Auto-Negotiation (Clause 28)	23.1.5.4	O		Required if Auto-Negotiation is implemented
*INS	Installation / cable		O		Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer

23.12.4 PICS proforma tables for the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T4

23.12.4.1 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO-1	Compatibility at the MDI	23.1.5.1	M		

23.12.4.2 PCS Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT-1	PCS Transmit function	23.2.1.2	PCS:M		Complies with state diagram Figure 23–8
PCT-2	Data encoding	23.2.1.2	PCS:M		8B6T with DC balance encoding rules
PCT-3	Order of ternary symbol transmission	Annex 23A	PCS:M		Leftmost symbol of each 6T code group first

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23.12.4.3 PCS Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR1	PCS Receive function	23.2.1.3	PCS:M		Complies with state diagram Figure 23–9
PCR2	Value of RXD<3:0> while RXDV is deasserted	23.2.1.3	PCS:M		All zeros
PCR3	Data decoding	23.2.1.3	PCS:M		8B6T with error detecting rules
PCR4	Value of dc_balance_error, eop_error and codeword_error at times other than those specified in the error detecting rules.	23.2.1.3	PCS:M		OFF
PCR5	Codeword_error indication sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected data nibbles across the MII
PCR6	Dc_balance_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of both affected nibbles across the MII
PCR7	Eop_error sets RX_ER when	23.2.1.3	PCS:M		During transfer of last decoded data nibble across the MII
PCR8	Action taken if carrier_status is truncated due to early deassertion of carrier_status	23.2.1.3	PCS:M		Assert RX_ER, and then deassert RX_DV

23.12.4.4 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	PCS Reset function executed when	23.2.1.1	PCS:M		Power-on, or the receipt of a reset request from the management entity
PCO2	PCS Error Sense function	23.2.1.4	PCS:M		Complies with state diagram Figure 23–10
PCO3	Signaling of RX_ER to MII	23.2.1.4	PCS:M		Before last nibble of Clause 4 MAC frame has passed across MII
PCO4	Timing of rxerror_status	23.2.1.4	PCS:M		Causes RX_ER to appear on the MII no later than last nibble of first data octet
PCO5	PCS Carrier Sense function	23.2.1.5	PCS:M		Controls MII signal CRS according to rules in 23.2.1.5
PCO6	MII signal COL is asserted when	23.2.1.6	PCS:M		Upon detection of a PCS collision
PCO7	At other times COL remains	23.2.1.6	PCS:M		Deasserted
PCO8	Loopback implemented in accordance with 22.2.4.1.2	23.2.2.2	PCS:M		Redundantly specified in 22.2.4.1.2

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23.12.4.4 Other PCS functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PCO9	No spurious signals emitted on the MDI during or after power down	23.2.2.2	M		
PCO10	PMA frame structure	23.2.3	M		Conformance to Figure 23–6
PCO11	PMA_UNITDATA messages	23.2.3	PMA:M		Must have a clock for both directions

23.12.4.5 PCS state diagram variables

Item	Feature	Subclause	Status	Support	Value/Comment
PCS1	Timing of eop adjusted such that the last nibble sent across the MII with RX_DV asserted is	23.2.4.2	PCS:M		Last nibble of last decoded data octet in a packet
PCS2	Transmission of octets on the three transmit pairs	23.2.4.2	PCS:M		Transmission order is: TX_D1, then BI_D3, and then BI_D4
PCS3	Value of tsr during first 16 TX_CLK cycles after TX_EN is asserted	23.2.4.2	PCS:M		sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosa, sosb, sosb, sosb, sosb, sosb, sosb
PCS4	Value of tsr during first 10 TX_CLK cycles after TX_EN is deasserted	23.2.4.2	PCS:M		eop1, eop1, eop2, eop2, eop3, eop3, eop4, eop4, eop5, eop5
PCS5	TX_ER causes transmission of	23.2.4.2	PCS:M		bad_code
PCS6	TX_ER received during the first 16 TX_CLK cycles causes	23.2.4.2	PCS:M		Transmission of **bad_code** during 17th and 18th clock cycles
PCS7	Action taken in event TX_EN falls on an odd nibble boundary	23.2.4.2	PCS:M		Extension of TX_EN by one TX_CLK cycle, and transmission of bad_code
PCS8	Transmission when TX_EN is not asserted	23.2.4.2	PCS:M		zero_code
PCS9	TX_CLK generated synchronous to	23.2.4.2	PCS:M		tw1_timer

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23.12.4.6 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	23.3.1.2	M		
PMS2	Generation of PMA_UNIT-DATA.indication (DATA) messages	23.3.3.2	M		synchronous with data received at the MDI
PMS3	Generation of PMA_CARRIER.indication message	23.3.4.2	M		ON/OFF
PMS4	Generation of PMA_LINK.indication message	23.3.5.2	M		FAIL/READY/OK
PMS5	Link_control defaults on power-on or reset to	23.3.6.2	M		ENABLE
PMS6	Action taken in SCAN_FOR_CARRIER mode	23.3.6.4	NWY:M		Enables link integrity state diagram, but blocks passage into LINK_PASS
PMS7	Reporting of link_status while in SCAN_FOR_CARRRIER mode	23.3.6.4	NWY:M		FAIL / READY
PMS8	Reporting of link_status while in DISABLE mode	23.3.6.4	NWY:M		FAIL
PMS9	Action taken in ENABLE mode	23.3.6.4	NWY:M		enables data processing functions
PMS10	Generation of PMA_RXERROR	23.3.7.2	M		ERROR / NO_ERROR

23.12.4.7 PMA Transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMT1	Transmission while (tx_code_vector=DATA) * (pma_carrier=OFF)	23.4.1.2	M		tx_code_vector[TX_D1] tx_code_vector[BI_D3] tx_code_vector[BI_D4]
PMT2	Transmission from time (tx_code_vector=DATA) * (pma_carrier=ON), until (tx_code_vector=IDLE	23.4.1.2	M		tx_code_vector[TX_D1] CS0 CS0
PMT3	Transmission while tx_code_vector=IDLE	23.4.1.2	M		Idle signal TP_DIL_100
PMT4	Duration of silence between link test pulses	23.4.1.2	M		1.2 ms ± 0.6 ms
PMT5	Link test pulse composed of	23.4.1.2	M		CS-1, CS1 transmitted on TX_D1

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23.12.4.7 PMA Transmit functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PMT6	Following a packet, TP_IDL_100 signal starts with	23.4.1.2	M		Period of silence
PMT7	Effect of termination of TP_IDL_100	23.4.1.2	M		No delay or corruption of subsequent packet
PMT8	Zero crossing jitter of link test pulse	23.4.1.2	M		Less than 4 ns p-p
PMT9	Action taken when xmit=disable	23.4.1.2	M		Transmitter behaves as if tx_code_vector=IDLE

23.12.4.8 PMA Receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMR1	Reception and translation of data with ternary symbol error ratio less than	23.4.1.3	M		One part in 10^8
PMR2	Assertion of pma_carrier=ON upon reception of test signal	23.4.1.4	M		Test signal is a succession of three data values, produced synchronously with a 25 MHz clock, both preceded and followed by 100 symbols of silence. The three values are: 467 mV, –225 mV, and then 467 mV again
PMR3	condition required to turn off pma_carrier	23.4.1.4	M		Either of a) Seven consecutive zeros b) Reception of eop1 per 23.4.1.4
PMR4	Value of carrier_status while rcv=ENABLE	23.4.1.4	M		pma_carrier
PMR5	Value of carrier_status while rcv=DISABLE	23.4.1.4	M		OFF

23.12.4.9 Link Integrity functions

Item	Feature	Subclause	Status	Support	Value/Comment
LIF1	Link Integrity function complies with	23.4.1.5	M		State diagram Figure 23–12

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23.12.4.10 PMA Align functions

Item	Feature	Subclause	Status	Support	Value/Comment
ALN1	Generation of PMA_UNITDATA.indication (PREAMBLE) messages	23.4.1.6	M		
ALN2	Ternary symbols transferred by first PMA_UNITADATA.indication (DATA) message	23.4.1.6	M		rx_code_vector[BI_D3]: first ternary symbol of first data code group rx_code_vector[BI_D2]: two ternary symbols prior to start of second data code group rx_code_vector[BI_D4]: four ternary symbols prior to start of third data code group
ALN3	PMA_UNITDATA.indication (DATA) messages continue until carrier_status=OFF	23.4.1.6	M		
ALN4	While carrier_status=OFF, PMA emits message	23.4.1.6	M		PMA_UNITDATA.indication (IDLE)
ALN5	Failure to recognize SSD generates rxerror_status=ERROR	23.4.1.6	M		
ALN6	Action taken when carrier_status=OFF	23.4.1.6	M		Clear rxerror_status
ALN7	Action taken if first packet is used for alignment	23.4.1.6	M		PMA emits PMA_UNITDATA..indication (PREAMBLE)
ALN8	Tolerance of line skew	23.4.1.6	M		60 ns
ALN9	Detection of misplaced **sosb** 6T code group caused by 3 or fewer ternary symbols in error	23.4.1.6	M		
ALN10	Action taken if **rcv**=disable	23.4.1.6	M		PMA emits PMA_UNITDATA..indication (IDLE)

23.12.4.11 Other PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMO1	PMA Reset function	23.4.1.1	M		
PMO2	Suitable clock recovery	23.4.1.7	M		

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23.12.4.12 Isolation requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ISO1	Values of all components used in test circuits	23.5	M		Accurate to within ±1% unless required otherwise
ISO2	Electrical isolation meets	23.5.1.1	M		1500 V at 50–60 Hz for 60 s per IEC 60950: 1991 *or* 2250 Vdc for 60 s per IEC 60950: 1991 *or* Ten 2400 V pulses per IEC 60060
ISO3	Insulation breakdown during isolation test	23.5.1.1	M		None per IEC 60950: 1991
ISO4	Resistance after isolation test	23.5.1.1	M		At least 2 M Ω

23.12.4.13 PMA electrical requirements

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	Conformance to all transmitter specifications in 23.5.1.2	23.5.1.2	M		
PME2	Transmitter load unless otherwise specified	23.5.1.2	M		100 Ω
PME3	Peak differential output voltage	23.5.1.2.1	M		3.15–3.85 V
PME4	Differential transmit template at MDI	23.5.1.2.2	M		Table 23–2
PME5	Differential MDI output template voltage scaling	23.5.1.2.2	M		3.15– 3.85 V
PME6	Interpolation between points on transmit template	23.5.1.2.2	M		Linear
PME7	Differential link pulse template at MDI	23.5.1.2.2	M		Table 23–2
PME8	Differential link pulse template scaling	23.5.1.2.2	M		Same value as used for differential transmit template scaling
PME9	Interpolation between point on link pulse template	23.5.1.2.2	M		Linear
PME10	State when transmitting seven or more consecutive CS0 during TP_IDL-100 signal	23.5.1.2.2	M		–50 mV to 50 mV
PME11	Limit on magnitude of harmonics measured at MDI	23.5.1.2.2	M		27 dB below fundamental
PME12	Differential output ISI	23.5.1.2.3	M		Less than 9%

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME13	Measurement of ISI and peak-to-peak signal voltage	23.5.1.2.3	M		Halfway between nominal zero crossing of the observed eye pattern
PME14	Transfer function of 100BASE-T4 transmit test filter	23.5.1.2.3	M		Third-order Butterworth filter with –3 dB point at 25.0 MHz
PME15	Reflection loss of 100BASE-T4 transmit test filter and 100 W load across the frequency range 2–12.5 MHz	23.5.1.2.3	M		Exceeds 17 dB
PME16	Differential output impedance	23.5.1.2.4	M		Provide return loss into 100 Ω of 17 dB from 2.0 to 12.5 MHz
PME17	Maintenance of return loss	23.5.1.2.4	M		At all times PHY is fully powered
PME18	Droop as defined in Figure 23–18 during transmission of eop1 and eop4	23.5.1.2.4	M		Less than 6%
PME19	Output timing jitter	23.5.1.2.5	M		No more than 4 ns peak-to-peak
PME20	Measurement of output timing jitter	23.5.1.2.5	M		Other transmit outputs connected to 100BASE-T4 ISI test filter or 100 Ω load
PME21	Minimum transmitter impedance balance	23.5.1.2.6	M		$29 - 17\log\left(\frac{f}{10}\right)$ dB
PME22	Transmitter common-mode rejection; effect of E_{cm} as shown in Figure 23–20 upon E_{dif}	23.5.1.2.8	M		Less than 100 mV
PME23	Transmitter common-mode rejection; effect of E_{cm} as shown in Figure 23–20 upon edge jitter	23.5.1.2.8	M		Less than 1.0 ns
PME24	E_{cm} used for common-mode rejection tests	23.5.1.2.8	M		15 V peak, 10.1 MHz sine wave
PME25	Transmitter faults; response to indefinite application of short circuits	23.5.1.2.9	M		Withstand without damage and resume operation after fault is removed
PME26	Transmitter faults; response to 1000 V common-mode impulse per IEC 60060	23.5.1.2.9	M		Withstand without damage
PME27	Shape of impulse used for common-mode impulse test	23.5.1.2.9	M		0.3/50 μs as defined in IEC 60060
PME28	Ternary symbol transmission rate	23.5.1.2.10	M		25.000 MHz ± 0.01%

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME29	Conformance to all receiver specifications in 23.5.1.3	23.5.1.3	M		
PME30	Action taken upon receipt of differential signals that were transmitted within the constraints of 23.5.1.2 and have passed through worst-case UTP model	23.5.1.3.1	M		Correctly translated into PMA_UNITDATA messages
PME31	Action taken upon receipt of link test pulse	23.5.1.3.1	M		Accept as a link test pulse
PME32	Test configuration for data reception and link test pulse tests	23.5.1.3.1	M		Using worst-case UTP model, and with a connection less than one meter in length
PME33	Bit loss	23.5.1.3.2	M		No more than that specified in 23.5.1.3.1
PME34	Reaction of pma_carrier to signal less than 325 mV peak	23.5.1.3.2	M		Must not set pma_carrier=ON
PME35	Reaction of pma_carrier to continuous sinusoid less than 1.7 MHz	23.5.1.3.2	M		Must not set pma_carrier=ON
PME36	Reaction of pma_carrier to single cycle or less	23.5.1.3.2	M		Must not set pma_carrier=ON
PME37	Reaction of pma_carrier to fast link pulse as defined in Clause 28	23.5.1.3.2	M		Must not set pma_carrier=ON
PME38	Reaction of pma_carrier to link integrity test pulse signal TP_IDL_100	23.5.1.3.2	M		Must not set pma_carrier=ON
PME39	Differential input impedance	23.5.1.3.3	M		Provide return loss into 100 Ω of 17 dB from 2.0 to 12.5 MHz
PME40	Maintenance of return loss	23.5.1.3.3	M		At all times PHY is fully powered
PME41	Droop as defined in Figure 23–18 during reception of test signal defined in Figure 23–19	23.5.1.3.3	M		Less than 6%
PME42	Receiver common-mode rejection; effect of E_{cm} as shown in Figure 23–24	23.5.1.3.4	M		Receiver meets 23.5.1.3.1
PME43	E_{cm} used for common-mode rejection tests	23.5.1.3.4	M		25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns
PME44	Receiver faults; response to indefinite application of short circuits	23.5.1.3.5	M		Withstand without damage and resume operation after fault is removed

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23.12.4.13 PMA electrical requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME45	Receiver faults; response to 1000 V common-mode impulse per IEC 60060	23.5.1.3.5	M		Withstand without damage
PME46	Shape of impulse used for common-mode impulse test	23.5.1.3.5	M		0.3/50 μs as defined in IEC 60060
PME47	Receiver properly receives data have a worst-case ternary symbol range	23.5.1.3.6	M		25.00 MHz ± 0.01%
PME48	Steady-state current consumption	23.5.2	MII:M		0.75 A maximum
PME49	PHY operating voltage range	23.5.2	MII:M		Includes worst voltage available from MII
PME50	Extraneous signals induced on the MII control circuits during normal power-up and power-down	23.5.2	M		None

23.12.4.14 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LNK1	Cable used	23.6.1	INS:M		Four pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω
LNK2	Source and load impedance used for cable testing (unless otherwise specified)	23.6.2	INS:M		100 Ω
LNK3	Insertion loss of simplex link segment	23.6.2.1	INS:M		Less than 12 dB
LNK4	Source and load impedances used to measure cable insertion loss	23.6.2.1	INS:M		Meet 23.5.1.2.4 and 23.5.1.3.3
LNK5	Characteristic impedance over the range 2–12.5 MHz	23.6.2.2	INS:M		85–115 Ω
LNK6	NEXT loss between 2 and 12.5 MHz	23.6.2.3.1	INS:M		Greater than $24.5 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK7	MDNEXT loss between 2 and 12.5 MHz	23.6.2.3.2	INS:M		Greater than $21.4 - 15\log\left(\frac{f}{12.5}\right)$ dB

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23.12.4.14 Characteristics of the link segment *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
LNK8	ELFEXT loss between 2 and 12.5 MHz	23.6.2.3.3	INS:M		Greater than $23.1 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK9	MDELFEXT loss between 2 and 12.5 MHz	23.6.2.3.4	INS:M		Greater than $20.9 - 15\log\left(\frac{f}{12.5}\right)$ dB
LNK10	Propagation delay	23.6.2.4.1	INS:M		Less than 570 ns
LNK11	Propagation delay per meter	23.6.2.4.2	INS:M		Less than 5.7 ns/m
LNK12	Skew	23.6.2.4.3	INS:M		Less than 50 ns
LNK13	Variation in skew once installed	23.6.2.4.3	INS:M		Less than ± 10 ns, within constraint of LNK8
LNK14	Noise level	23.6.3	INS:M		Such that objective error ratio is met
LNK15	MDNEXT noise	23.6.3.1	INS:M		Less than 325 mVp
LNK16	MDFEXT noise	23.6.3.2	INS:M		Less than 87 mVp
LNK17	Maximum length of Category 5, 25-pair jumper cables	23.6.3.2	INS:M		10 m

23.12.4.15 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	23.7.1	M		IEC 60603-7: 1990
MDI2	Connector used on PHY	23.7.1	M		Jack (as opposed to plug)
MDI3	Crossover in every twisted-pair link	23.7.2	INS:M		
MDI4	MDI connector that implements the crossover function	23.7.2	XVR:M		Marked with “X”

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23.12.4.16 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
SAF1	Conformance to safety specifications	23.9.1	M		IEC 60950: 1991
SAF2	Installation practice	23.9.2.1	INS:M		Sound practice, as defined by applicable local codes
SAF3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection	23.9.2.2	M		
SAF4	Care taken during installation to ensure that noninsulated network cable conductors do not make electrical contact with unintended conductors or ground	23.9.2.3	INS:M		
SAF5	Application of voltages specified in 23.9.2.4 does not result in any safety hazard	23.9.2.4	M		
SAF6	Conformance with local and national codes for the limitation of electromagnetic interference	23.9.3.1	INS:M		

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23.12.4.17 Timing requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TIM1	PMA_OUT	23.11.3	PMA:M		1 to 9.5 BT
TIM2	TEN_PMA + PMA_OUT	23.11.3	PCS:M		7 to 17.5 BT
TIM3	TEN_CRS	23.11.3	PCS:M		0 to +4 BT
TIM4	NOT_TEN_CRS	23.11.3	PCS:M		28 to 36 BT
TIM5	RX_PMA_CARRIER	23.11.3	PMA:M		Less than 15.5 BT
TIM6	RX_CRS	23.11.3	PCS:M		Less than 27.5 BT
TIM7	RX_NOT_CRS	23.11.3	PCS:M		0 to 51.5 BT
TIM8	FAIRNESS	23.11.3	PCS:M		0 to 28 BT
TIM9	RX_PMA_DATA	23.11.3	PMA:M		67 to 90.5 BT
TIM10	EOP_CARRIER_STATUS	23.11.3	M		51 to 74.5 BT
TIM11	EOC_CARRIER_STATUS	23.11.3	M		3 to 50.5 BT
TIM12	RX_RXDV	23.11.3	PCS:M		81 to 114.5 BT
TIM13	RX_PMA_ERROR	23.11.3	M		Allowed limits equal the actual RX_PMA_DATA time for the device under test plus from 0 to 20 BT
TIM14	RX_COL	23.11.3	PCS:M		Less than 27.5 BT
TIM15	RX_NOT_COL	23.11.3	PCS:M		Less than 51.5 BT
TIM16	TX_NOT_COL	23.11.3	PCS:M		Less than 36 BT
TIM17	TX_SKEW	23.11.3	M		Less than 0.5 BT
TIM18	CRS_PMA_DATA	23.11.3	PMA:M		Less than 78.5 BT
TIM19	COL_to_BI_D3/4_OFF	23.11.3	PMA:M		Less than 40 BT

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24. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.1 Overview

24.1.1 Scope

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 100 Mb/s Physical Layer implementations, collectively known as 100BASE-X. There are currently two embodiments within this family: 100BASE-TX and 100BASE-FX. 100BASE-TX specifies operation over two pairs of twisted-pair Category 5 cabling. 100BASE-FX specifies operation over two optical fibers. The term 100BASE-X is used when referring to issues common to both 100BASE-TX and 100BASE-FX.

The 100BASE-X may support the capability of Energy-Efficient Ethernet (EEE) as described in Clause 78. When a transmitting station of a link with this capability detects low link utilization, it can request the local PHY transmitter to enter the Low Power Idle (LPI) mode and send appropriate symbols over the link. Upon receiving and decoding those symbols, the link partner's receiver can enter the LPI mode. The transmit and receive paths can enter and exit low power states independently. Energy is conserved by deactivating the corresponding functional blocks of individual path. Only 100BASE-TX supports this optional capability.

100BASE-X leverages the Physical Layer standards of ISO/IEC 9314 and ANSI X3T12 (FDDI) through the use of their Physical Medium Dependent (PMD) sublayers, including their Medium Dependent Interfaces (MDI). For example, ANSI X3.263-1995 (TP-PMD) defines a 125 Mb/s, full duplex signaling system for twisted-pair wiring that forms the basis for 100BASE-TX as defined in Clause 25. Similarly, ISO/IEC 9314-3:1990 defines a system for transmission on optical fiber that forms the basis for 100BASE-FX as defined in Clause 26.

100BASE-X maps the interface characteristics of the FDDI PMD sublayer (including MDI) to the services expected by the CSMA/CD MAC. 100BASE-X can be extended to support any other full duplex medium requiring only that the medium be PMD compliant.

24.1.2 Objectives

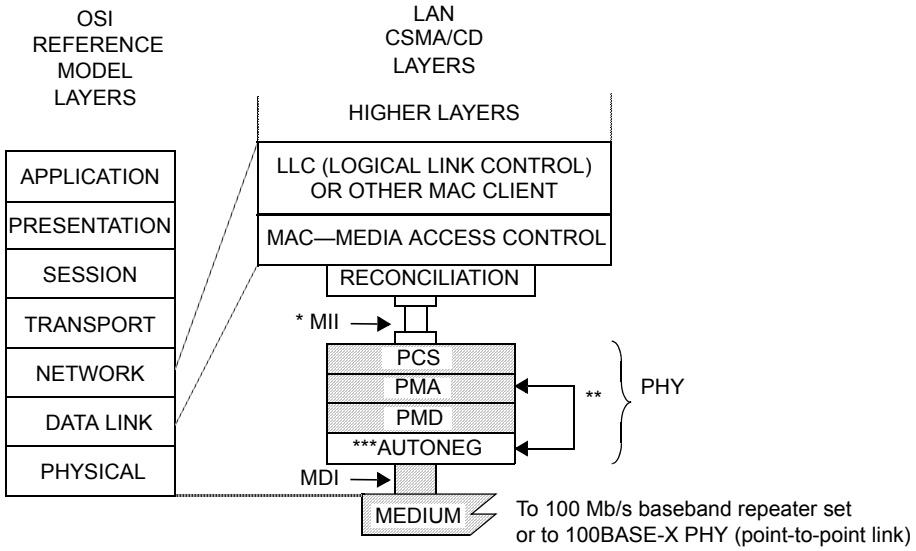
The following are the objectives of 100BASE-X:

a) Support the CSMA/CD MAC in the half duplex and the full duplex modes of operation.
b) Support the 100BASE-T MII, repeater, and optional Auto-Negotiation.
c) Provide 100 Mb/s data rate at the MII.
d) Support cable plants using Category 5 twisted-pair, 150 Ω STP or cabled optical fiber, compliant with ISO/IEC 11801.
e) Allow for a nominal network extent of 200–400 m, including
    1) Unshielded twisted-pair links of 100 m
    2) Two repeater networks of approximately 200 m span
    3) One repeater network of approximately 300 m span (using fiber)
    4) DTE/DTE links of approximately 400 m (half duplex mode using fiber) and 2 km (full duplex mode using multimode fiber.
f) Preserve full duplex behavior of underlying PMD channels.
g) Optionally support EEE through the function of LPI (see Clause 78), available only for 100BASE-TX.

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24.1.3 Relationship of 100BASE-X to other standards

Figure 24–1 depicts the relationships among the 100BASE-X sublayers (shown shaded), other 100BASE-T sublayers, the CSMA/CD MAC, and the IEEE 802.2 LLC.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional.
** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate.
*** AUTONEG is mandatory for EEE capability and optional otherwise.

Figure 24–1—Type 100BASE-X PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

24.1.4 Summary of 100BASE-X sublayers

The following provides an overview of the 100BASE-X sublayers that are embodied in the 100BASE-X Physical sublayer (PHY).[5]

24.1.4.1 Physical Coding Sublayer (PCS)

The PCS interface is the Media Independent Interface (MII) that provides a uniform interface to the Reconciliation sublayer for all 100BASE-T PHY implementations (e.g., 100BASE-X and 100BASE-T4). 100BASE-X, as other 100BASE-T PHYs, is modeled as providing services to the MII. This is similar to the use of an AUI interface.

The 100BASE-X PCS realizes all services required by the MII, including the following:

a) Encoding (decoding) of MII data nibbles to (from) five-bit code-groups (4B/5B).
b) Generating Carrier Sense and Collision Detect indications.

[5] The 100BASE-X PHY should not be confused with the FDDI PHY, which is a sublayer functionally aligned to the 100BASE-T PCS.

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c) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMA.
d) Mapping of Transmit, Receive, Carrier Sense and Collision Detection between the MII and the underlying PMA.
e) Optionally, interpreting and generating MII data signals to enable or disable the LPI mode.

24.1.4.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS and other bit-oriented clients (e.g., repeaters) to support the use of a range of physical media. The 100BASE-X PMA performs the following functions:

a) Mapping of transmit and receive code-bits between the PMA's client and the underlying PMD.
b) Generating a control signal indicating the availability of the PMD to a PCS or other client, also synchronizing with Auto-Negotiation when implemented.
c) Optionally, generating indications of activity (carrier) and carrier errors from the underlying PMD.
d) Optionally, sensing receive channel failures and transmitting the Far-End Fault Indication; and detecting the Far-End Fault Indication.
e) Optionally, receiving and processing LPI control signals from the PCS.
f) Recovery of clock from the NRZI data supplied by the PMD.

24.1.4.3 Physical Medium Dependent (PMD) sublayer

100BASE-X uses the FDDI signaling standards ISO/IEC 9314-3:1990 and ANSI X3.263-1995 (TP-PMD). These signaling standards, called PMD sublayers, define 125 Mb/s, full duplex signaling systems that accommodate multimode optical fiber and twisted-pair cabling. 100BASE-X uses the PMDs specified in these standards with the PMD Service Interface specified in 24.4.1.

The MDI, logically subsumed within the PMD, provides the actual medium attachment, including connectors, for the various supported media.

100BASE-X does not specify the PMD and MDI other than including the appropriate standard by reference along with the minor adaptations necessary for 100BASE-X. Figure 24–2 depicts the relationship between 100BASE-X and the PMDs of ISO/IEC 9314-3:1990 (for 100BASE-FX) and ANSI X3.263-1995 (for 100BASE-TX). The PMDs (and MDIs) for 100BASE-TX and 100BASE-FX are specified in subsequent clauses of this standard.

24.1.4.4 Auto-Negotiation

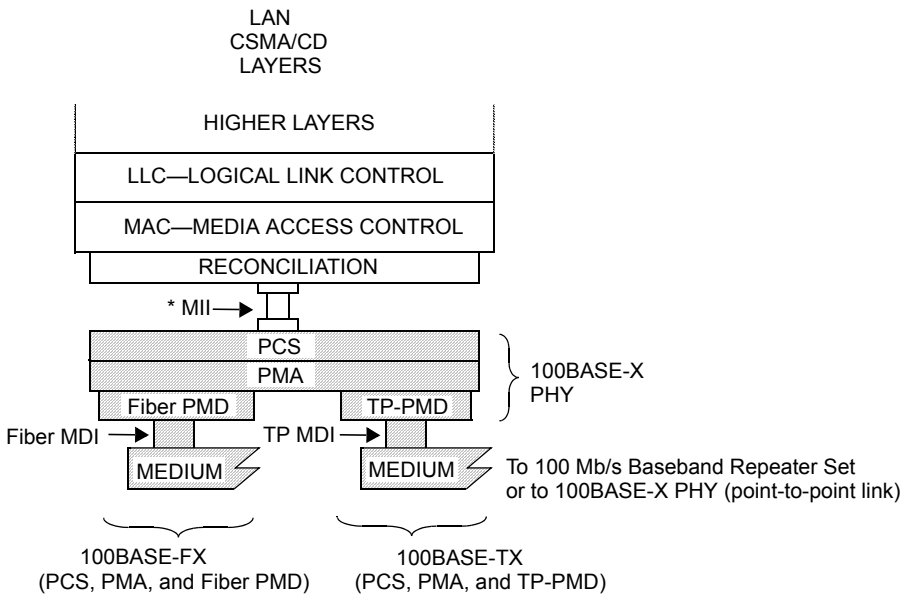
Auto-Negotiation shall be implemented for EEE capability. See Clause 28.

24.1.5 Inter-sublayer interfaces

There are a number of interfaces employed by 100BASE-X. Some (such as the PMA and PMD interfaces) use an abstract service model to define the operation of the interface. The PCS Interface is defined as a set of physical signals, in a medium-independent manner (MII). Figure 24–3 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 100BASE-X.

It is important to note that, while this specification defines interfaces in terms of bits, nibbles, and code-groups, implementations may choose other data path widths for implementation convenience. The only exceptions are: a) the MII, which, when implemented, uses a nibble-wide data path as specified in Clause 22, and b) the MDI, which uses a serial, physical interface.

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MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
Fiber PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR FIBER
TP-PMD = PHYSICAL MEDIUM DEPENDENT SUBLAYER FOR TWISTED PAIRS

NOTE—The PMD sublayers are mutually independent.
* MII is optional.

Figure 24–2—Relationship of 100BASE-X and the PMDs

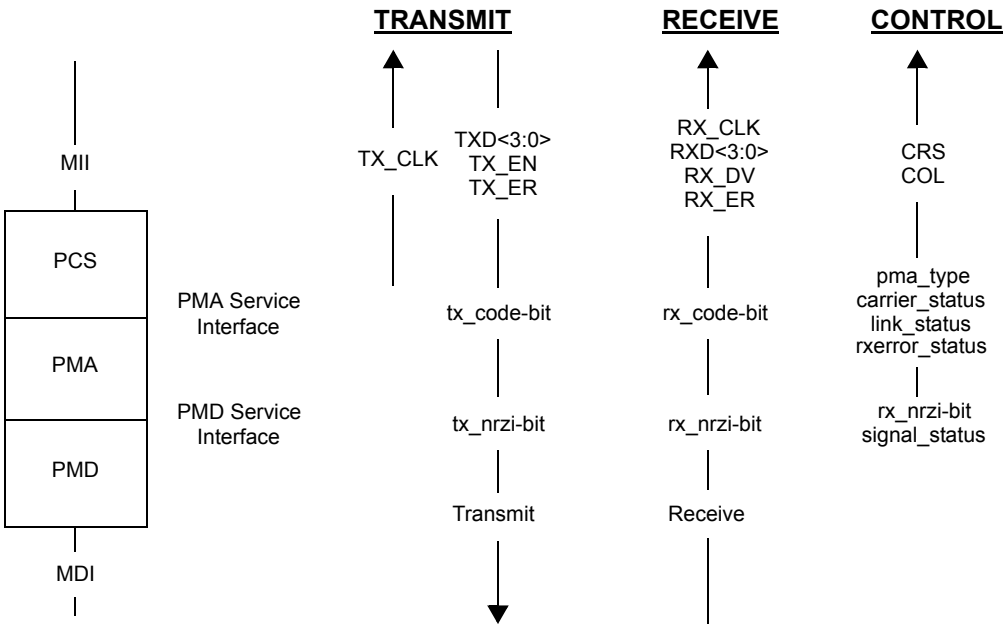


Figure 24–3—Interface mapping

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24.1.6 Functional block diagram

Figure 24–4 provides a functional block diagram of the 100BASE-X PHY. Signals or functions shown with dashed lines are optional.

24.1.7 State diagram conventions

The body of this standard is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5; state diagram timers follow the conventions of 14.2.3.2.

24.2 Physical Coding Sublayer (PCS)

24.2.1 Service Interface (MII)

The PCS Service Interface allows the 100BASE-X PCS to transfer information to and from the MAC (via the Reconciliation sublayer) or other PCS client, such as a repeater. The PCS Service Interface is precisely defined as the Media Independent Interface (MII) in Clause 22.

In this clause, the setting of MII variables to TRUE or FALSE is equivalent, respectively, to “asserting” or “deasserting” them as specified in Clause 22.

24.2.2 Functional requirements

The PCS comprises the Transmit, Receive, and Carrier Sense functions for 100BASE-T. In addition, the collisionDetect signal required by the MAC (COL on the MII) is derived from the PMA code-bit stream. The PCS shields the Reconciliation sublayer (and MAC) from the specific nature of the underlying channel. Specifically for receiving, the 100BASE-X PCS passes to the MII a sequence of data nibbles derived from incoming code-groups, each comprised of five code-bits, received from the medium. Code-group alignment and MAC packet delimiting is performed by embedding special non-data code-groups. The MII uses a nibble-wide, synchronous data path, with packet delimiting being provided by separate TX_EN and RX_DV signals. The PCS provides the functions necessary to map these two views of the exchanged data. The process is reversed for transmit.

The following provides a detailed specification of the functions performed by the PCS, which comprise five parallel processes (Transmit, Transmit Bits, Receive, Receive Bits, and Carrier Sense). Figure 24–4 includes a functional block diagram of the PCS.

The Receive Bits process accepts continuous code-bits via the PMA_UNITDATA.indicate primitive. Receive monitors these bits and generates RXD<3:0>, RX_DV, and RX_ER on the MII, and the internal flag, receiving, used by the Carrier Sense and Transmit processes.

Upon receiving proper code-groups via rx_code_bits from the link partner as described in 24.2.2.1.6, the Receive process may support the LPI function by deactivating all or part of receive functional blocks of the PCS, PMA, and PMD to conserve energy during the low link utilization period, and generate commands through the MII as described in 22.2.2.8. By interacting with the Link Monitor of the PMA, a link failure detection mechanism is included to differentiate two conditions of link failure due to signal off: the loss of channel signal during the normal operation and the loss of refresh signal in the LPI mode.

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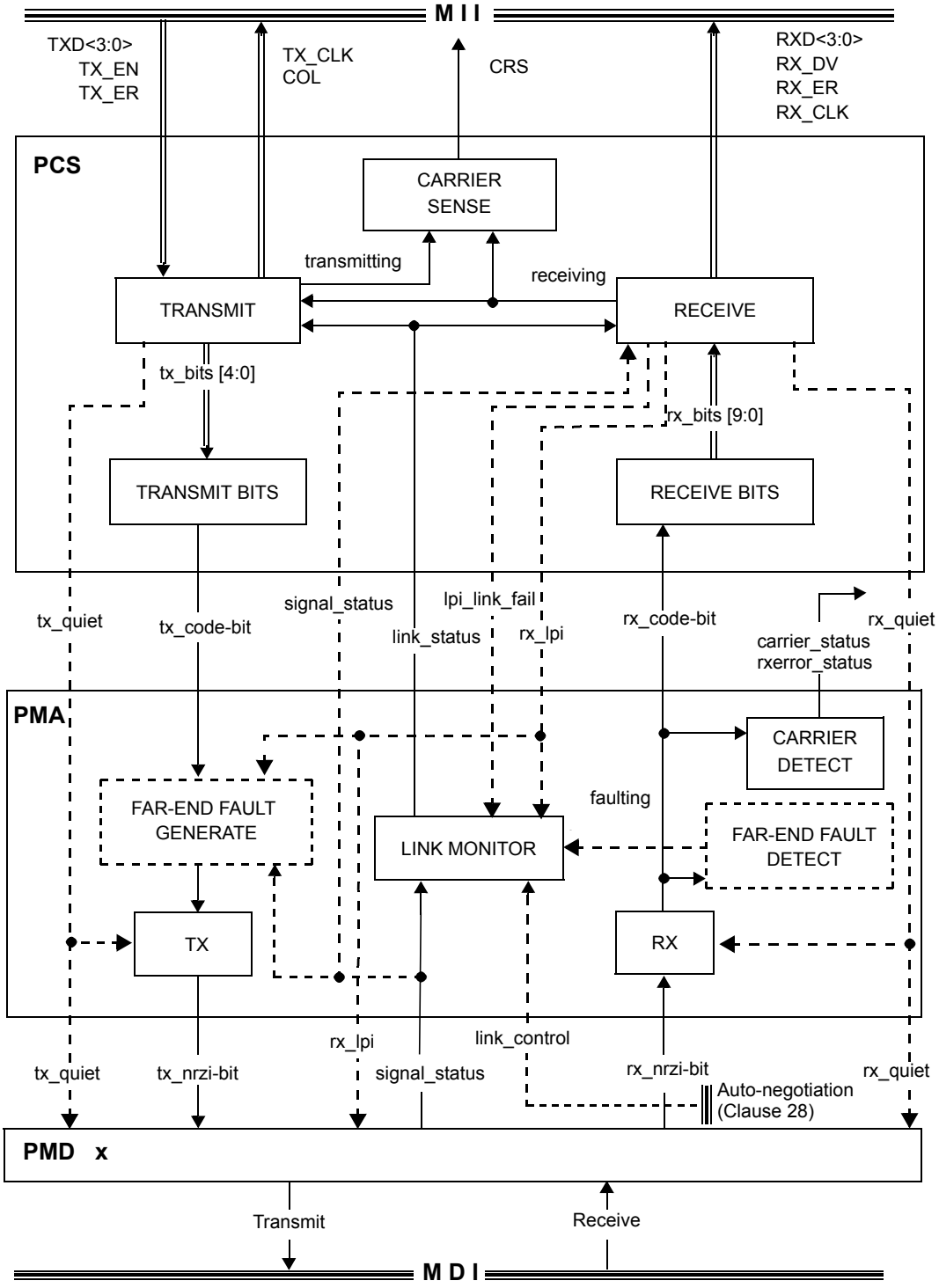


Figure 24–4—Functional block diagram

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The Transmit process generates continuous code-groups based upon the TXD<3:0>, TX_EN, and TX_ER signals on the MII. These code-groups are transmitted by Transmit Bits via the PMA_UNITDATA.request primitive. The Transmit process generates the MII signal COL based on whether a reception is occurring simultaneously with transmission. Additionally, it generates the internal flag, transmitting, for use by the Carrier Sense process.

The Transmit process may support the LPI function by deactivating all or part of the transmit functional blocks of the PCS, PMA, and PMD to conserve energy during the low link utilization period upon receiving the proper command from MII as described in 22.2.2.4. In this mode, the Transmit process is periodically activated to transmit refresh signal through tx_code_bits in order to allow the remote receiver to keep track of the long-term variation of channel characteristics and the clock drift between link partners.

The Carrier Sense process asserts the MII signal CRS when either transmitting or receiving is TRUE. Both the Transmit and Receive processes monitor link_status via the PMA_LINK.indicate primitive, to account for potential link failure conditions.

24.2.2.1 Code-groups

The PCS maps four-bit nibbles from the MII into five-bit code-groups, and vice versa, using a 4B/5B block coding scheme. A code-group is a consecutive sequence of five code-bits interpreted and mapped by the PCS. Implicit in the definition of a code-group is an establishment of code-group boundaries by an alignment function within the PCS Receive process. It is important to note that, with the sole exception of the SSD, which is used to achieve alignment, code-groups are undetectable and have no meaning outside the 100BASE-X physical protocol data unit, called a “stream.”

The coding method used, derived from ISO/IEC 9314-1, provides

a) Adequate codes (32) to provide for all Data code-groups (16) plus necessary control code-groups.
b) Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to effect a 100 Mb/s Physical Layer interface on a 125 Mb/s physical channel as provided by FDDI PMDs.
c) Sufficient transition density to facilitate clock recovery (when not scrambled).

Table 24–1 specifies the interpretation assigned to each five bit code-group, including the mapping to the nibble-wide (TXD or RXD) Data signals on the MII. The 32 code-groups are divided into four categories, as shown.

For clarity in the remainder of this clause, code-group names are shown between /slashes/. Code-group sequences are shown in succession, e.g., /1/2/....

The indicated code-group mapping is identical to ISO/IEC 9314-1:1989, with the following five exceptions:

a) The FDDI term *symbol* is avoided in order to prevent confusion with other 100BASE-T terminology. In general, the term *code-group* is used in its place.
b) The /S/ and /Q/ code-groups are not used by 100BASE-X and are interpreted as INVALID.
c) The /R/ code-group is used in 100BASE-X as the second code-group of the End-of-Stream delimiter rather than to indicate a Reset condition.
d) The /H/ code-group is used to propagate receive errors rather than to indicate the Halt Line State.
e) The /P/ code-group is used to indicate LPI.

24.2.2.1.1 Data code-groups

A Data code-group conveys one nibble of arbitrary data between the MII and the PCS. The sequence of Data code-groups is arbitrary, where any Data code-group can be followed by any other Data code-group. Data code-groups are coded and decoded but not interpreted by the PCS. Successful decoding of Data code-groups depends on proper receipt of the Start-of-Stream delimiter sequence, as defined in Table 24–1.

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Table 24–1—4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
DATA	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
	0 0 0 0 0	P	0 0 0 1	SLEEP; LPI code only for the EEE capability. Otherwise, Invalid code; refer to Table 22–1 and Table 22–2
CONTROL	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

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24.2.2.1.2 Idle code-groups

The Idle code-group (/I/) is transferred between streams. It provides a continuous fill pattern to establish and maintain clock synchronization. Idle code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.3 Control code-groups

The Control code-groups are used in pairs (/J/K/, /T/R/) to delimit MAC packets. Control code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.4 Start-of-Stream delimiter (/J/K/)

A Start-of-Stream delimiter (SSD) is used to delineate the boundary of a data transmission sequence and to authenticate carrier events. The SSD is unique in that it may be recognized independently of previously established code-group boundaries. The Receive function within the PCS uses the SSD to establish code-group boundaries. A SSD consists of the sequence /J/K/.

On transmission, the first 8 bits of the MAC preamble are replaced by the SSD, a replacement that is reversed on reception.

24.2.2.1.5 End-of-Stream delimiter (/T/R/)

An End-of-Stream delimiter (ESD) terminates all normal data transmissions. Unlike the SSD, an ESD cannot be recognized independent of previously established code-group boundaries. An ESD consists of the sequence /T/R/.

24.2.2.1.6 SLEEP code-groups (/P/)

The SLEEP code-group (/P/) is used to delineate the boundary of an LPI sequence and to deliver a refresh signal to maintain clock synchronization and verify the link status. The SLEEP code-groups are emitted from, and interpreted by, the PCS.

24.2.2.1.7 Invalid code-groups

The /H/ code-group indicates that the PCS's client wishes to indicate a Transmit Error to its peer entity. The normal use of this indicator is for repeaters to propagate received errors. Transmit Error code-groups are emitted from the PCS, at the request of the PCS's client through the use of the TX_ER signal, as described in 24.2.4.2.

The presence of any invalid code-group on the medium, including /H/, denotes a collision artifact or an error condition. Invalid code-groups are not intentionally transmitted onto the medium by DTE's. The PCS indicates the reception of an Invalid code-group on the MII through the use of the RX_ER signal, as described in 24.2.4.4.

24.2.2.2 Encapsulation

The 100BASE-X PCS accepts frames from the MAC through the Reconciliation sublayer and MII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 100BASE-X PCS encapsulates the MAC frame (100BASE-X Service Data Unit, SDU) into a Physical Layer stream (100BASE-X Protocol Data Unit, PDU).

Except for the two code-group SSD, data nibbles within the SDU (including the non-SSD portions of the MAC preamble and SFD) are not interpreted by the 100BASE-X PHY. The conversion from a MAC frame to a Physical Layer stream and back to a MAC frame is transparent to the MAC.

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Figure 24–5 depicts the mapping between MAC frames and Physical Layer streams.

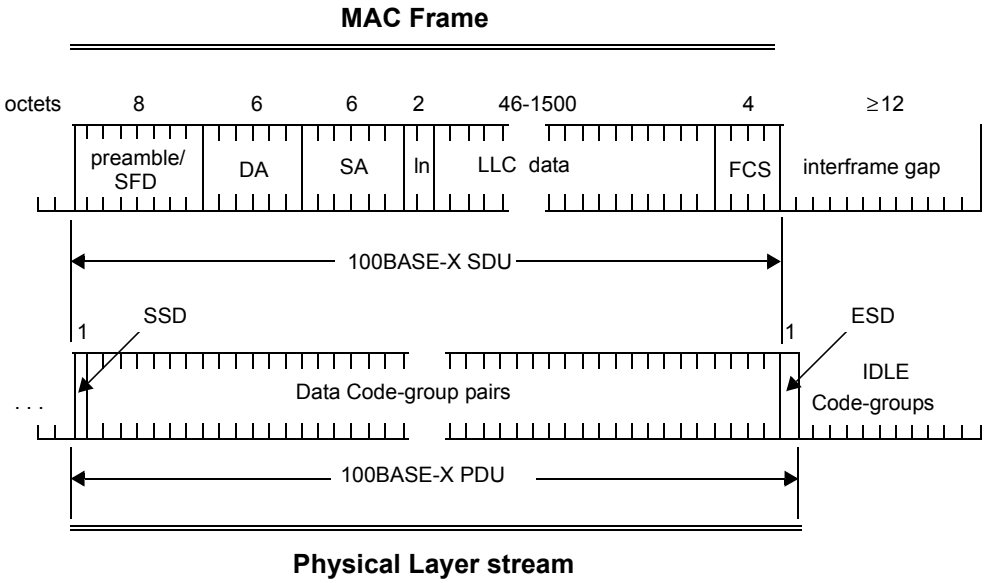


Figure 24–5—PCS encapsulation

A properly formed stream can be viewed as comprising the following three elements:

a) *Start-of-Stream Delimiter.* The start of a Physical Layer stream is indicated by a SSD, as defined in 24.2.2.1. The SSD replaces the first octet of the preamble from the MAC frame and vice versa.
b) *Data Code-groups.* Between delimiters (SSD and ESD), the PCS conveys Data code-groups corresponding to the data nibbles of the MII. These Data code-groups comprise the 100BASE-X Service Data Unit (SDU). Data nibbles within the SDU (including those corresponding to the MAC preamble and SFD) are not interpreted by the 100BASE-X PCS.
c) *End-of-Stream Delimiter.* The end of a properly formed stream is indicated by an ESD, as defined in 24.2.2.1. The ESD is transmitted by the PCS following the deassertion of TX_EN on the MII, which corresponds to the last data nibble composing the FCS from the MAC. It is transmitted during the period considered by the MAC to be the interframe gap (IFG). On reception, ESD is interpreted by the PCS as terminating the SDU.

Between streams, IDLE code-groups are conveyed between the PCS and PMA.

24.2.2.3 Data delay

The PCS maps a non-aligned code-bit data path from the PMA to an aligned, nibble-wide data path on the MII, both for Transmit and Receive. Logically, received bits must be buffered to facilitate SSD detection and alignment, coding translation, and ESD detection. These functions necessitate an internal PCS delay of at least two code-groups. In practice, alignment may necessitate even longer delays of the incoming code-bit stream.

When the MII is present as an exposed interface, the MII signals TX_CLK and RX_CLK, not depicted in the following state diagrams, shall be generated by the PCS in accordance with Clause 22.

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24.2.2.4 Mapping between MII and PMA

Figure 24–6 depicts the mapping of the nibble-wide data path of the MII to the five-bit-wide code-groups (internal to the PCS) and the code-bit path of the PMA interface.

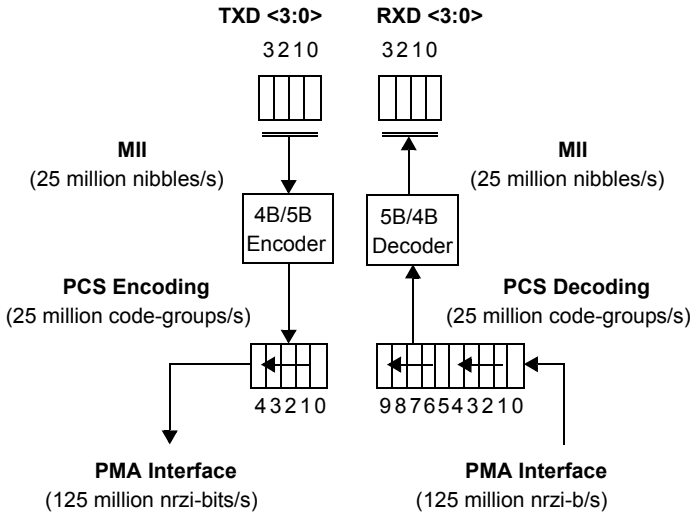


Figure 24–6—PCS reference diagram

Upon receipt of a nibble from the MII, the PCS encodes it into a five-bit code-group, according to 24.2.2.1. Code-groups are serialized into code-bits and passed to the PMA for transmission on the underlying medium, according to Figure 24–6. The first transmitted code-bit of a code-group is bit 4, and the last code-bit transmitted is bit 0. There is no numerical significance ascribed to the bits within a code-group; that is, the code-group is simply a five-bit pattern that has some predefined interpretation.

Similarly, the PCS deserializes code-bits received from the PMA, according to Figure 24–6. After alignment is achieved, based on SSD detection, the PCS converts code-groups into MII data nibbles, according to 24.2.2.1.

24.2.3 State variables

24.2.3.1 Constants

DATA

The set of 16 code-groups corresponding to valid DATA, as specified in 24.2.2.1. (In the Receive state diagram, the set operators $\in$ and $\notin$ are used to represent set membership and non-membership, respectively.)

ESD

The code-group pair corresponding to the End-of-Stream delimiter, as specified in 24.2.2.1.

ESD1

The code-group pair corresponding to the End-of-Stream delimiter, Part 1 (/T/), as specified in 24.2.2.1.

ESD2

The code-group pair corresponding to the End-of-Stream delimiter, Part 2 (/R/), as specified in

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24.2.2.1.

HALT
: The Transmit Error code-group (/H/), as specified in 24.2.2.1.

IDLE
: The IDLE code-group, as specified in 24.2.2.1.

IDLES
: A code-group pair comprised of /I/I/; /I/ as specified in 24.2.2.1.

SSD
: The code-group pair corresponding to the Start-of-Stream delimiter, as specified in 24.2.2.1.

SSD1
: The code-group corresponding to the Start-of-Stream delimiter, Part 1 (/J/), as specified in 24.2.2.1.

SSD2
: The code-group corresponding to the Start-of-Stream delimiter, Part 2 (/K/), as specified in 24.2.2.1.

The following constants are required only for the optional EEE capability:

SLEEP
: The SLEEP code-group (/P/) used by the LPI state delineator, as specified in 24.2.2.1.

TX_LP_IDLE
: A binary value 0001 of transmit nibble-wide Data signals (TXD), together with the deassertion of TX_EN and the assertion of TX_ER on the MII, used to indicate “Assert LPI”, as specified in 22.2.2.

RX_LP_IDLE
: A binary value 0001 of receive nibble-wide Data signals (RXD), together with the deassertion of RX_DV and the assertion of RX_ER on the MII, used to indicate “Assert LPI”, as specified in 22.2.2.

24.2.3.2 Variables

In the following, values for the MII parameters are definitively specified in Clause 22.

COL
: The COL signal of the MII as specified in Clause 22.

CRS
: The CRS signal of the MII as specified in Clause 22.

link_status
: The link_status parameter as communicated by the PMA_LINK.indicate primitive.

  Values: FAIL; the receive channel is not intact
  READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
  OK; the receive channel is intact and enabled for reception

receiving
: A Boolean set by the Receive process to indicate non-IDLE activity (after squelch). Used by the Carrier Sense process, and also interpreted by the Transmit process for indicating a collision.

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Values: TRUE; unsquelched carrier being received
FALSE; carrier not being received

rx_bits [9:0]

A vector of the 10 most recently received code-bits from the PMA as assembled by Receive Bits and processed by Receive. rx_bits [0] is the most recently received (newest) code-bit; rx_bits [9] is the least recently received code-bit (oldest). When alignment has been achieved, it contains the last two code-groups.

rx_code-bit

The rx_code-bit parameter as communicated by the most recent PMA_UNITDATA.indicate primitive (that is, the value of the most recently received code-bit from the PMA).

RX_DV

The RX_DV signal of the MII as specified in Clause 22. Set by the Receive process, RX_DV is also interpreted by the Receive Bits process as an indication that rx_bits is code-group aligned.

RX_ER

The RX_ER signal of the MII as specified in Clause 22.

RXD <3:0>

The RXD <3:0> signal of the MII as specified in Clause 22.

transmitting

A Boolean set by the Transmit Process to indicate a transmission in progress. Used by the Carrier Sense process.

Values: TRUE; the PCS's client is transmitting
FALSE; the PCS's client is not transmitting

tx_bits [4:0]

A vector of code-bits representing a code-group prepared for transmission by the Transmit Process and transmitted to the PMA by the Transmit Bits process.

TX_EN

The TX_EN signal of the MII as specified in Clause 22.

TX_ER

The TX_ER signal of the MII as specified in Clause 22.

TXD <3:0>

The TXD <3:0> signal of the MII as specified in Clause 22.

The following variables are required only for the optional EEE capability:

lpi_link_fail

A Boolean set by the Receive process to control the transition to a Link Down state when in the LPI mode. Used by the Link Monitor process of the PMA as communicated through the PMA_LPILINKFAIL.request primitive.

Values: TRUE; local receiver has detected a link failure status when in the LPI mode
FALSE; local receiver is functioning normally when in the LPI mode

rx_lpi

A Boolean set by the Receive process to indicate the LPI mode. Used by the Link Monitor process of the PMA as communicated through the PMA_RXLPI.request primitive. This parameter is used to alter the signal detection time as shown in Table 25–3. It can also be used to halt the clock RXC of MII as described in Clause 22.

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Values: TRUE; local receiver is in the LPI mode
FALSE; local receiver is in the normal mode

rx_quiet

A Boolean set by the Receive process to indicate a Quiet state of the receiver in the LPI mode as communicated through the PMD_RXQUIET.request primitive. Also may be used to control the power-saving function of various receive blocks (PCS, PMA, and PMD).

Values: TRUE; the local receiver is in the Quiet state
FALSE; the local receiver is not in the Quiet state

tx_quiet

A Boolean set by the Transmit process to indicate a Quiet state of the transmitter in the LPI mode as communicated through the PMD_TXQUIET.request primitive. Also may be used to control the power-saving function of various transmit blocks (PCS, PMA, and PMD).

Values: TRUE; the local transmitter is in the Quiet state
FALSE; the local transmitter is not in the Quiet state

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

24.2.3.3 Functions

nibble DECODE (code-group)

In Receive, this function takes as its argument a five-bit code-group and returns the corresponding MII RXD <3:0> nibble, per Table 24–1.

code-group ENCODE (nibble)

In the Transmit process, this function takes as its argument an MII TXD <3:0> nibble, and returns the corresponding five-bit code-group per Table 24–1.

SHIFTLEFT (rx_bits)

In Receive Bits, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

24.2.3.4 Timers

code-bit_timer

In the Transmit Bits process, the timer governing the output of code-bits from the PCS to the PMA and thereby to the medium with a nominal 8 ns period. This timer shall be derived from a fixed frequency oscillator with a base frequency of 125 MHz ± 0.005% and phase jitter above 20 kHz less than ± 8°.

The following timers are required only for the optional EEE capability:

lpi_link_fail_timer

In the LPI mode, the receiver in Wake state is checking if valid symbols are properly received. This timer defines the maximum time allowed for the PHY between entry into the Wake state and subsequent entry into the Quiet, Sleep, or Idle states before assuming a link failure. The timer shall have a period between 90 μs and 110 μs.

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lpi_rx_ti_timer

In the LPI mode, the receiver can move to the Idle state when it receives consecutive IDLE symbols. In order to distinguish the intended IDLE symbols sent by the link partner from ones falsely decoded during the transition from the Sleep state to the Quiet state before the signal status is deasserted, this receiver timer counts the minimum duration of received IDLE symbols. During this period of time, the receiver stays in an intermediate state. The timer shall have a period between 0.8 μs and 0.9 μs.

lpi_rx_tq_timer

In the LPI mode, this receiver timer counts the maximum duration the PHY stays in the Quiet state before it expects a Refresh signal. If the PHY fails to receive a valid Refresh signal or Wake signal before this timer expires, the receiver shall assume a link failure. The timer shall have a period between 24 ms and 26 ms.

lpi_rx_ts_timer

In the LPI mode, this receiver timer counts the maximum duration the PHY is allowed to stay in the Sleep state before assuming a link failure. The timer shall have a period between 240 μs and 260 μs.

lpi_rx_tw_timer

In the LPI mode, the receiver in the Quiet state is woken up by the receiving signal. This receiver timer counts the expected duration for the PHY to identify if valid SLEEP symbols for the Refresh state or valid IDLES for the Wake state have been properly received. If none of the SLEEP or IDLE symbols are received when the timer expires, the wake error counter as defined in MDIO manageable device (MMD) register 3.22 (see 45.2.3.10) shall be incremented. The timer shall have a period that does not exceed 20.5 μs.

lpi_tx_tq_timer

In the LPI mode, this transmitter timer counts the duration the PHY remains in the Quiet state before it must wake to send a refresh signal. The timer shall have a period between 20 ms and 22 ms.

lpi_tx_ts_timer

In the LPI mode, this transmitter timer counts the duration the PHY is sending continuous SLEEP symbols in the Sleep state before going into the Quiet state. The timer shall have a period between 200 μs and 220 μs.

24.2.3.5 Messages

gotCodeGroup.indicate

A signal sent to the Receive process by the Receive Bits process after alignment has been achieved signifying completion of reception of the next code-group in rx_bits(4:0), with the preceding code-group moved to rx_bits [9:5]. rx_bits [9:5] may be considered as the “current” code-group.

PMA_UNITDATA.indicate (rx_code-bit)

A signal sent by the PMA signifying that the next code-bit from the medium is available in rx_code-bit.

sentCodeGroup.indicate

A signal sent to the Transmit process from the Transmit Bits process signifying the completion of

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transmission of the code-group in tx_bits [4:0].

24.2.4 State diagrams

24.2.4.1 Transmit Bits

Transmit Bits is responsible for taking code-groups prepared by the Transmit process and transmitting them to the PMA using PMA_UNITDATA.request, the frequency of which determines the transmit clock. Transmit deposits these code-groups in tx_bits with Transmit Bits signaling completion of a code-group transmission with sentCodeGroup.indicate.

The PCS shall implement the Transmit Bits process as depicted in Figure 24–7 including compliance with the associated state variables as specified in 24.2.3.

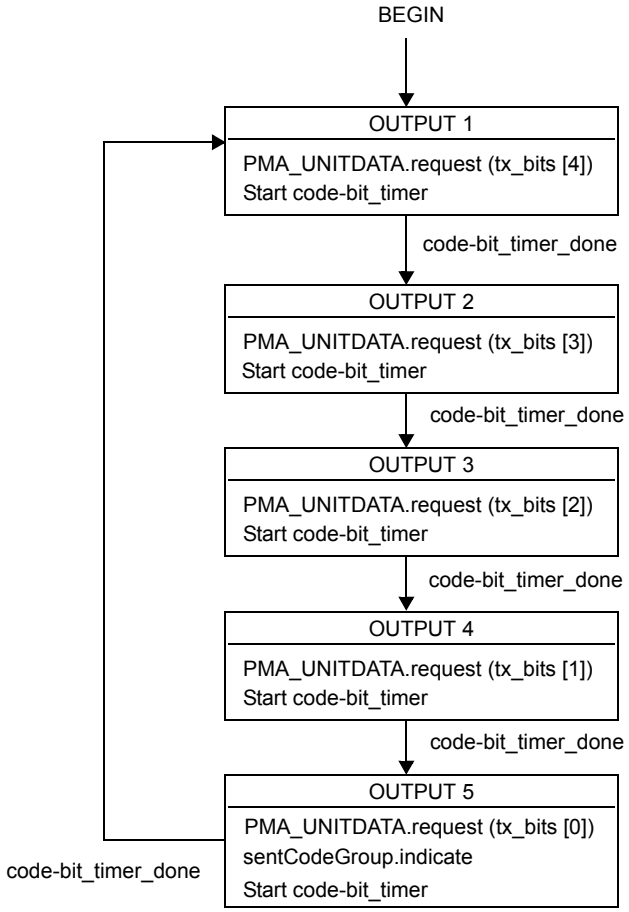


Figure 24–7—Transmit Bits state diagram

24.2.4.2 Transmit

The Transmit process sends code-groups to the PMA via tx_bits and the Transmit Bits process. When initially invoked, and between streams (delimited by TX_EN on the MII), except in the LPI mode for the optional EEE capability, the Transmit process sources continuous Idle code-groups (/I/) to the PMA. Upon the assertion of TX_EN by the MII, the Transmit process passes an SSD (/J/K/) to the PMA, ignoring the TXD<3:0> nibbles during these two code-group times. Following the SSD, each TXD<3:0> nibble is encoded into a five-bit code-group until TX_EN is deasserted. If, while TX_EN is asserted, the TX_ER signal is asserted, the Transmit process passes Transmit Error code-groups (/H/) to the PMA. Following the

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deassertion of TX_EN, an ESD (/T/R/) is generated, after which the transmission of Idle code-groups is resumed by the IDLE state.

If EEE Capability is supported, upon the assertion of LPI on the MII (a binary value 0001 of TXD, together with the deassertion of TX_EN and the assertion of TX_ER, see 22.2.2), the Transmit process enters the LPI mode and starts to source SLEEP (/P/) code-groups to the PMA. In the LPI mode, the Transmit process is controlled by timers to switch between the TX_SLEEP and TX_QUIET states. The Transmit process returns to the IDLE state whenever the MII deasserts LPI.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T.

The indication of link_status ≠ OK by the PMA at any time causes an immediate transition to the IDLE state and supersedes any other Transmit process operations.

The PCS shall implement the Transmit process as depicted in Figure 24–8 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.3 Receive Bits

The Receive Bits process collects code-bits from the PMA interface passing them to the Receive process via rx_bits. rx_bits [9:0] represents a sliding, 10-bit window on the PMA code-bits, with newly received code-bits from the PMA (rx_code-bit) being shifted into rx_bits [0]. This is depicted in Figure 24–9. Bits are collected serially until Receive indicates alignment by asserting RX_DV, after which Receive Bits signals Receive for every five code-bits accumulated. Serial processing resumes with the deassertion of RX_DV.

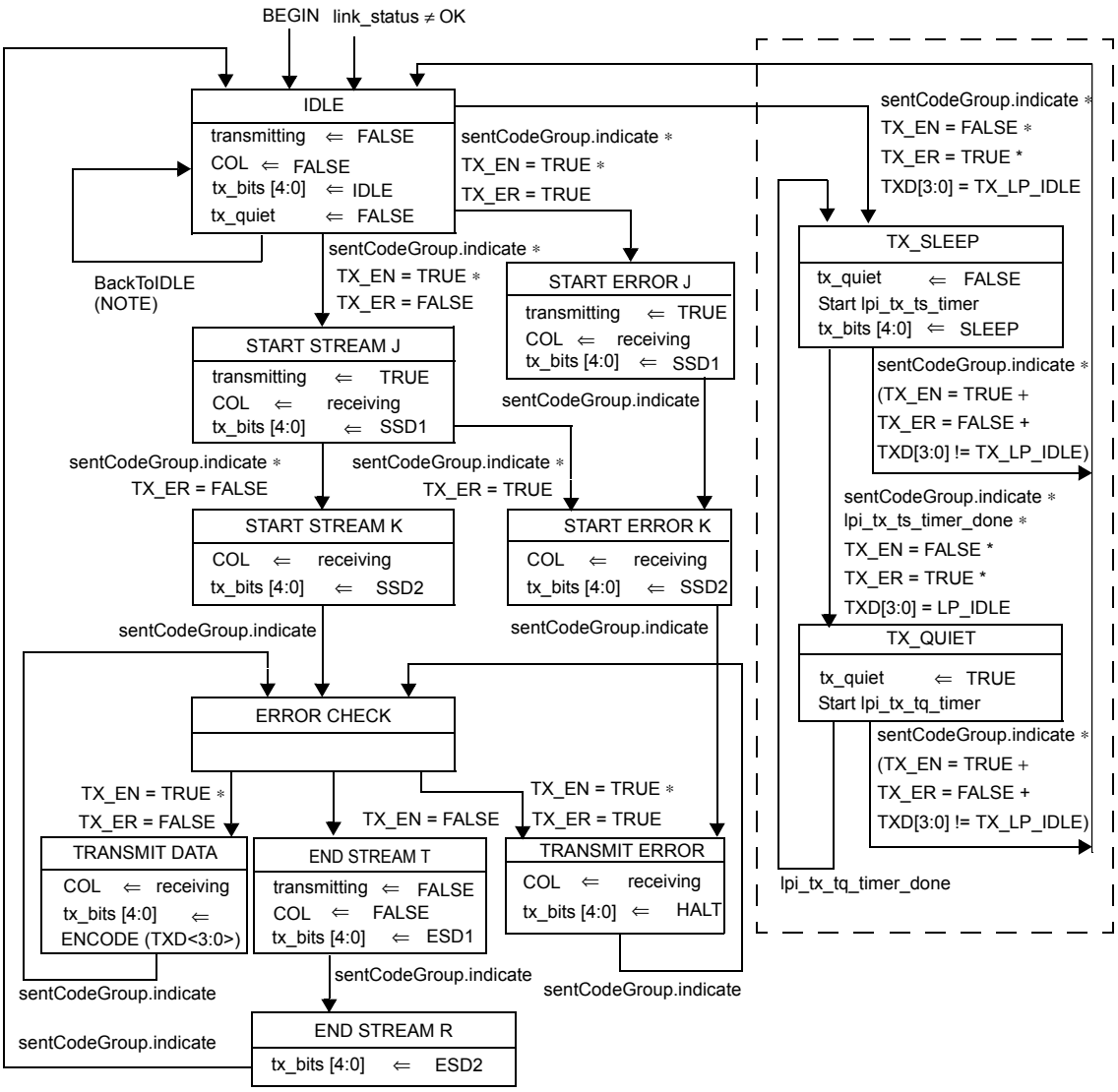
The PCS shall implement the Receive Bits process as depicted in Figure 24–10 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.4 Receive

The Receive process state diagram can be viewed as comprising two sections: prealigned and aligned. In the prealigned states, IDLE, CARRIER DETECT, and IDENTIFY JK, except for the detection of SLEEP code-groups when supporting the optional EEE capability, the Receive process is waiting for an indication of channel activity followed by an SSD. After successful alignment, the incoming code-groups are decoded while waiting for stream termination.

If EEE Capability is supported, when the Receive process successfully aligns and decodes two consecutive SLEEP (/P/) code-groups, it enters the LPI mode and stays in LPI states until either the IDLE code-groups are received, where it leads the Receive process to the IDLE state, or a link failure condition in the LPI mode occurs, where it causes the Receive process to enter the RX_LPI_LINK_FAIL state and eventually move to the IDLE state.

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NOTE 1—BackToIDLE represents the following branch condition:

If the EEE capability is supported,
sentCodeGroup.indicate * TX_EN = FALSE * (TX_E R= FALSE + (TX_ER = TRUE * TXD[3:0] ≠ TX_LP_IDLE))
Otherwise,
sentCodeGroup.indicate * TX_EN = FALSE

NOTE 2—States and state transitions shown within the dashed box are only required for the EEE capability

Figure 24–8—Transmit state diagram

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24.2.4.4.1 Detecting channel activity

In a DTE operating in half duplex mode, the detection of activity on the underlying channel is used both by the MAC (via the MII CRS signal and the Reconciliation sublayer) for deferral purposes, and by the Transmit process for collision detection. Activity, signaled by the assertion of receiving, is indicated by the receipt of two non-contiguous ZEROS within any 10 code-bits of the incoming code-bit stream.

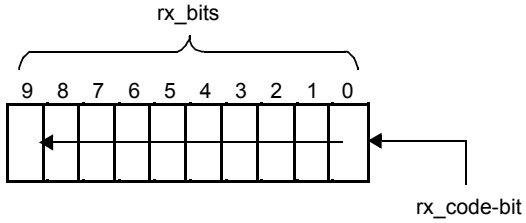


Figure 24–9—Receive Bits reference diagram

24.2.4.4.2 Code-group alignment

After channel activity is detected, the Receive process first aligns the incoming code-bits on code-group boundaries for subsequent data decoding. This is achieved by scanning the rx_bits vector for a SSD (/J/K/). The MII RX_DV signal remains deasserted during this time, which ensures that the Reconciliation sublayer will ignore any signals on RXD <3:0>. Detection of the SSD causes the Receive process to enter the START OF STREAM J state.

Well-formed streams contain SSD (/J/K/) in place of the first eight preamble bits. In the event that something else is sensed immediately following detection of carrier, a False Carrier Indication is signaled to the MII by asserting RX_ER and setting RXD to 1110 while RX_DV remains deasserted. The associated carrier event, as terminated by 10 ONEs, is otherwise ignored.

24.2.4.4.3 Stream decoding

The Receive process substitutes a sequence of alternating ONE and ZERO data-bits for the SSD, which is consistent with the preamble pattern expected by the MAC.

The Receive process then performs the DECODE function on the incoming code-groups, passing decoded data to the MII, including those corresponding to the remainder of the MAC preamble and SFD. The MII signal RX_ER is asserted upon decoding any code-group following the SSD that is neither a valid Data code-group nor a valid stream termination sequence.

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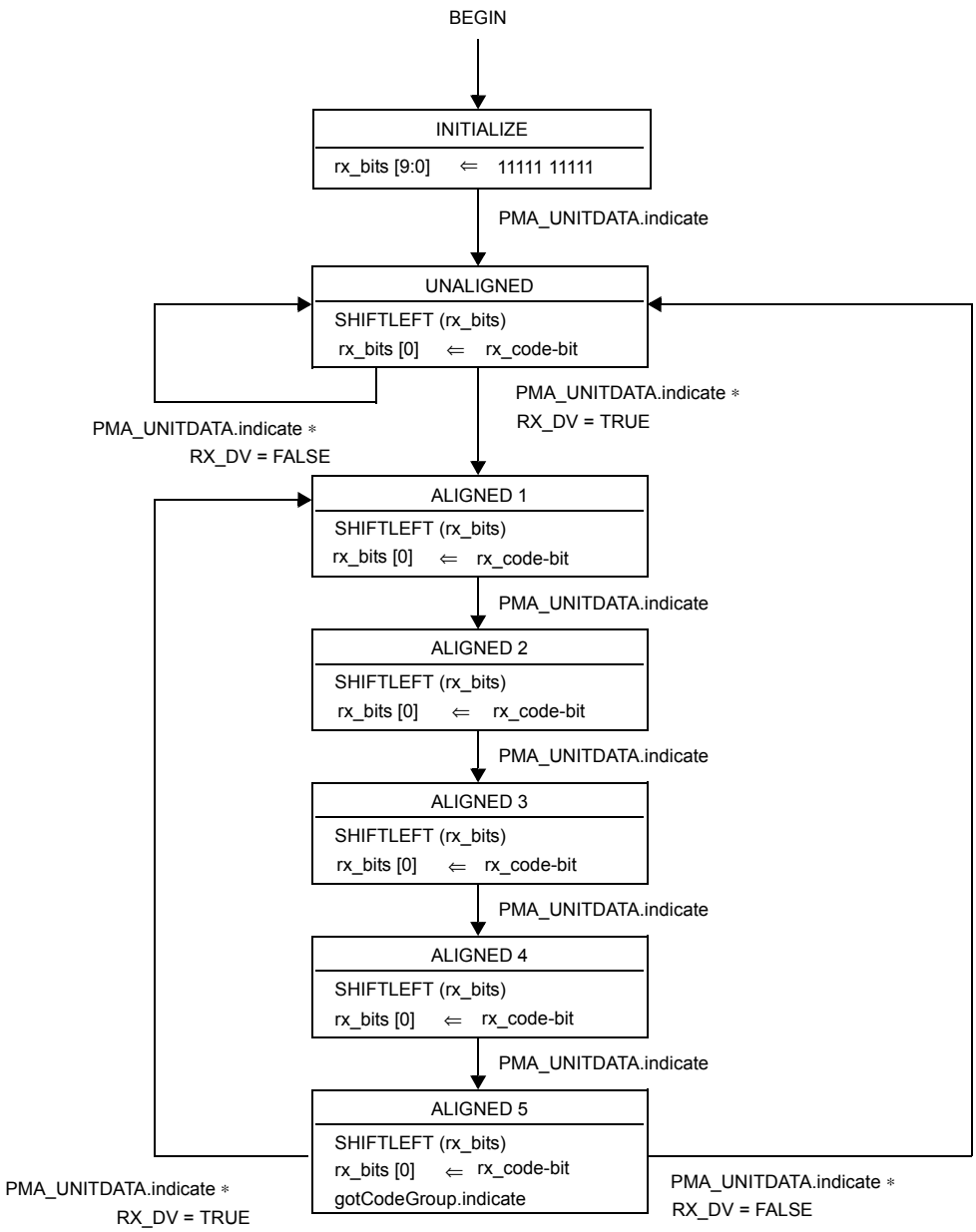
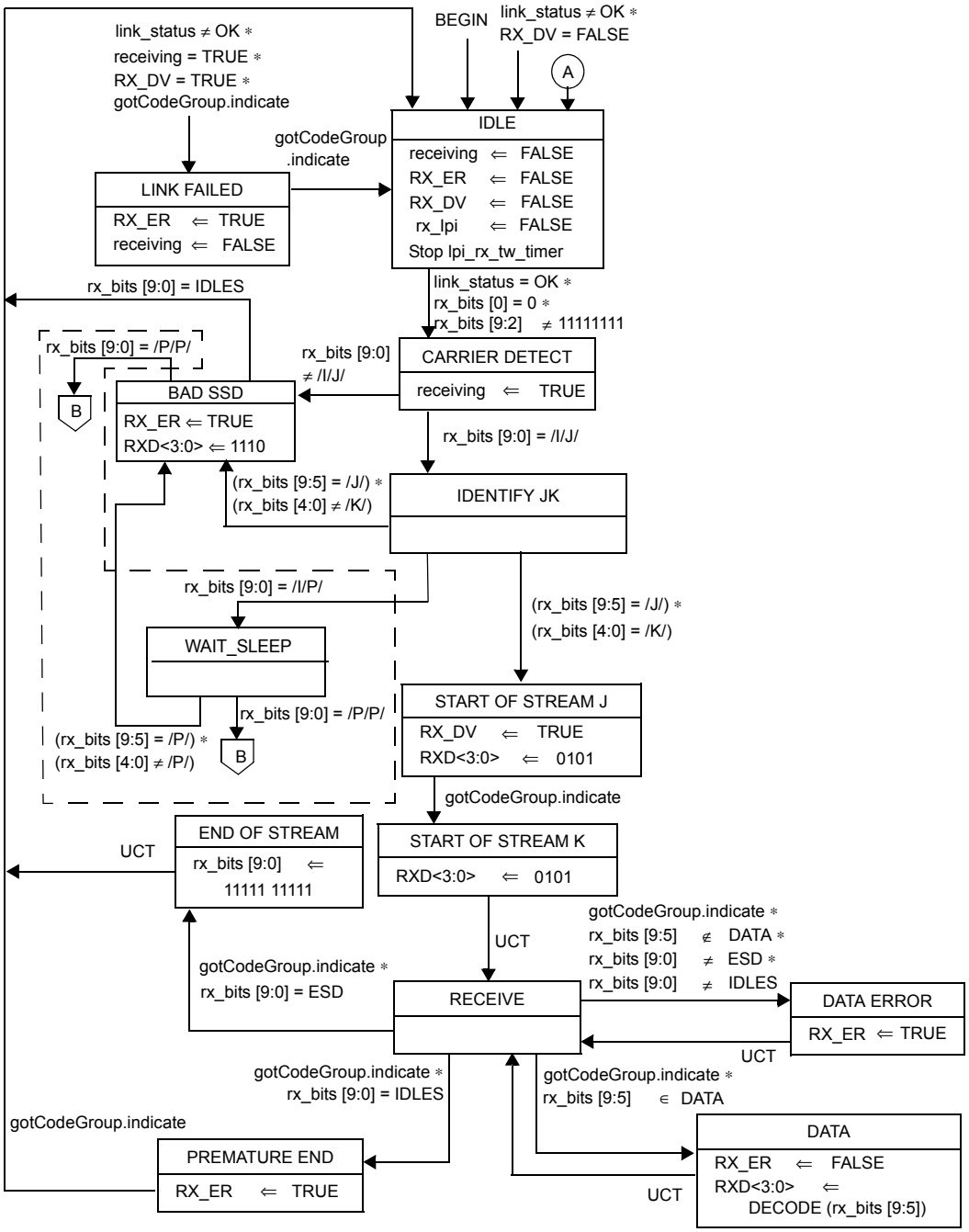


Figure 24–10—Receive Bits state diagram

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24.2.4.4.4 Stream termination

There are two means of effecting stream termination in the Receive process (Figure 24–11 and Figure 24–12) .



NOTE—States and state transitions shown within the dashed box are only required for the EEE capability

Figure 24–11—Receive state diagram, part a

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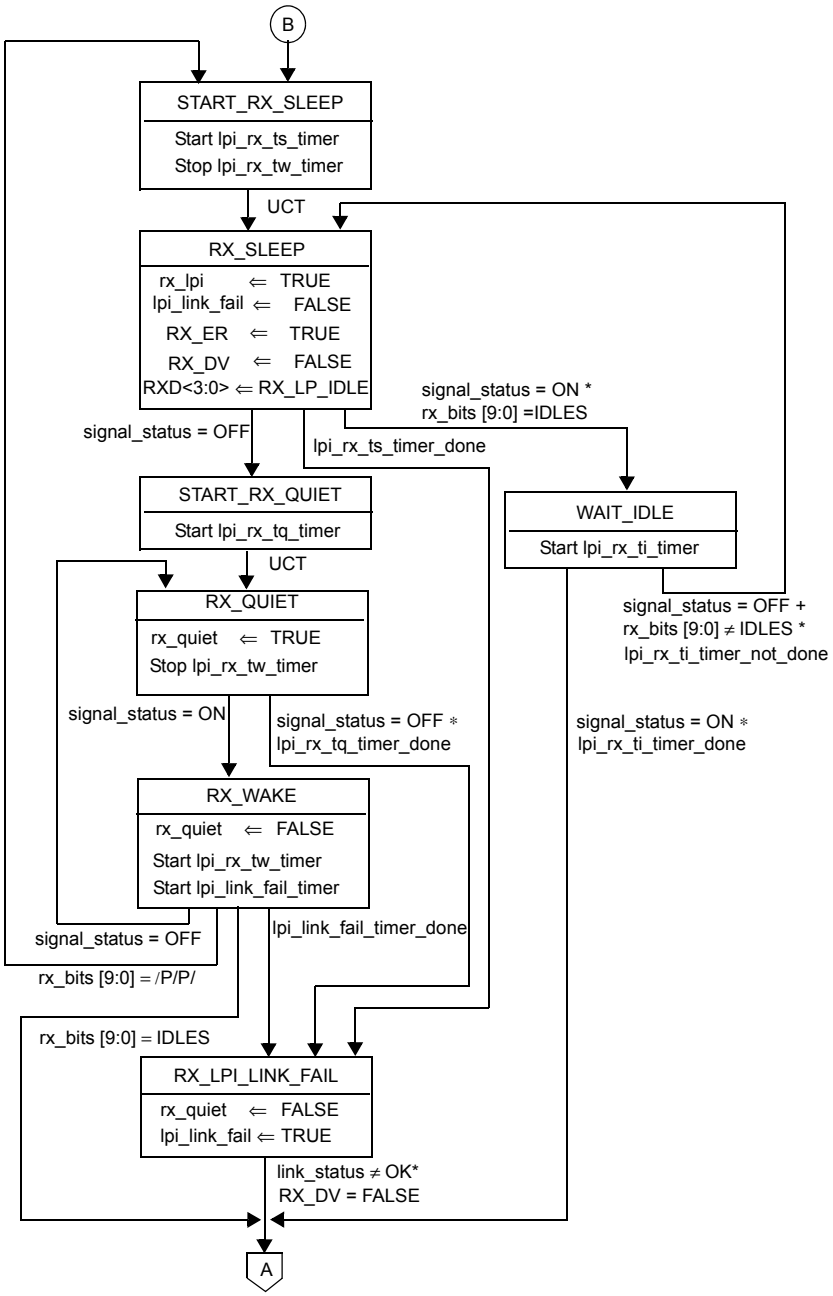


Figure 24–12—Receive state diagram, part b (only required for the EEE capability)

A normal stream termination is caused by detection of an ESD (/T/R/) in the rx_bits vector. In order to preserve the ability of the MAC to properly delimit the FCS at the end of the frame (that is, to avoid incorrect AlignmentErrors in the MAC) the internal signal receiving (and through it, the MII CRS signal, per Clause 22) is deasserted immediately following the last code-bit in the stream that maps to the FCS. Note that the condition link_status ≠ OK during stream reception (that is, when receiving = TRUE) causes an immediate transition to the LINK FAILED state and supersedes any other Receive process operations.

A premature stream termination is caused by the detection of two Idle code-groups (/I/I) in the rx_bits vector prior to an ESD. Note that RX_DV remains asserted during the nibble corresponding to the first five

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contiguous ONEs while RX_ER is signaled on the MII. RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for sufficient time to be detected.

Stream termination causes a transition to the IDLE state.

The PCS shall implement the Receive process as depicted in Figure 24–11 and Figure 24–12 including compliance with the associated state variables as specified in 24.2.3.

24.2.4.5 Carrier Sense

The Carrier Sense process generates the signal CRS on the MII, which (via the Reconciliation sublayer) a MAC operating in half duplex mode uses for deferral. The process operates by performing a logical OR operation on the internal messages receiving and transmitting, generated by the Receive and Transmit processes, respectively.

The PCS shall implement the Carrier Sense process as depicted in Figure 24–13 including compliance with the associated state variables as specified in 24.2.3.

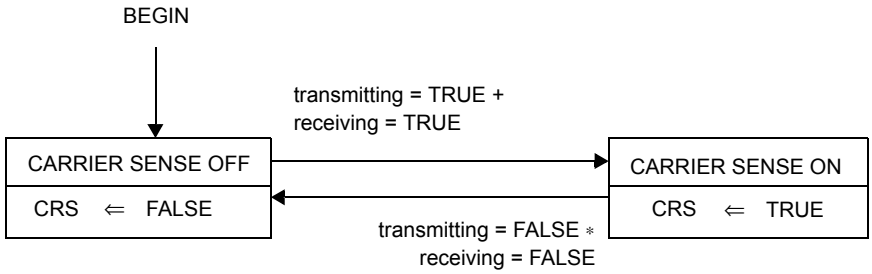


Figure 24–13—Carrier Sense state diagram

24.3 Physical Medium Attachment (PMA) sublayer

24.3.1 Service interface

The following specifies the service interface provided by the PMA to the PCS or another client, such as a repeater. These services are described in an abstract manner and do not imply any particular implementation.

The PMA Service Interface supports the exchange of code-bits between the PCS and/or Repeater entities. The PMA converts code-bits into NRZI format and passes these to the PMD, and vice versa. It also generates additional status indications for use by its client.

The following primitives are defined:

PMA_TYPE.indicate

PMA_UNITDATA.request

PMA_UNITDATA.indicate

PMA_CARRIER.indicate

PMA_LINK.indicate

PMA_LINK.request

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PMA_RXERROR.indicate

PMA_LPILINKFAIL.request

PMA_RXLPI.request

24.3.1.1 PMA_TYPE.indicate

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. The purpose of this primitive is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

24.3.1.1.1 Semantics of the service primitive

PMA_TYPE.indicate (pma_type)

The pma_type parameter for use with a 100BASE-X PMA is “X”.

24.3.1.1.2 When generated

The PMA continuously generates this primitive to indicate the value of pma_type.

24.3.1.1.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.2 PMA_UNITDATA.request

This primitive defines the transfer of data (in the form of code-bits) from the PMA’s client to the PMA.

24.3.1.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_code-bit)

This primitive defines the transfer of data (in the form of code-bits) from the PCS or other client to the PMA. The tx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.2.2 When generated

The PCS or other client continuously sends, at a nominal 125 Mb/s rate, the appropriate code-bit for transmission on the medium.

24.3.1.2.3 Effect of receipt

Upon receipt of this primitive, the PMA generates a PMD_UNITDATA.request primitive, requesting transmission of the indicated code-bit, in NRZI format (tx_nrzi-bit), on the MDI.

24.3.1.3 PMA_UNITDATA.indicate

This primitive defines the transfer of data (in the form of code-bits) from the PMA to the PCS or other client.

24.3.1.3.1 Semantics of the service primitive

PMA_UNITDATA.indicate (rx_code-bit)

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The data conveyed by PMA_UNITDATA.indicate is a continuous code-bit sequence at a nominal 125 Mb/s rate. The rx_code-bit parameter can take one of two values: ONE or ZERO.

24.3.1.3.2 When generated

The PMA continuously sends code-bits to the PCS or other client corresponding to the PMD_UNITDATA.indicate primitives received from the PMD.

24.3.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.4 PMA_CARRIER.indicate

This primitive is generated by the PMA to indicate that a non-squelched, non-IDLE code-bit sequence is being received from the PMD. The purpose of this primitive is to give clients the earliest reliable indication of activity on the underlying continuous-signaling channel.

24.3.1.4.1 Semantics of the service primitive

PMA_CARRIER.indicate (carrier_status)

The carrier_status parameter can take on one of two values, ON or OFF, indicating whether a non-squelched, non-IDLE code-bit sequence (that is, carrier) is being received (ON) or not (OFF).

24.3.1.4.2 When generated

The PMA generates this primitive to indicate a change in the value of carrier_status.

24.3.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.5 PMA_LINK.indicate

This primitive is generated by the PMA to indicate the status of the underlying PMD receive link.

24.3.1.5.1 Semantics of the service primitive

PMA_LINK.indicate (link_status)

The link_status parameter can take on one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled by Auto-Negotiation (READY), intact and enabled (OK), or not intact (FAIL). Link_status is set to FAIL when the PMD sets signal_status to OFF; when Auto-Negotiation (optional) sets link_control to DISABLE; or when Far-End Fault Detect (optional) sets faulting to TRUE. When link_status ≠ OK, then rx_code-bit and carrier_status are undefined.

24.3.1.5.2 When generated

The PMA generates this primitive to indicate a change in the value of link_status.

24.3.1.5.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

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24.3.1.6 PMA_LINK.request

This primitive is generated by the Auto-Negotiation algorithm, when implemented, to allow it to enable and disable operation of the PMA. See Clause 28. When Auto-Negotiation is not implemented, the primitive is never invoked and the PMA behaves as if link_control = ENABLE.

24.3.1.6.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter takes on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE. Auto-Negotiation sets link_control to SCAN_FOR_CARRIER prior to receiving any fast link pulses, permitting the PMA to sense a 100BASE-X signal. Auto-Negotiation sets link_control to DISABLE when it senses an Auto-Negotiation partner (fast link pulses) and must temporarily disable the 100BASE-X PHY while negotiation ensues. Auto-Negotiation sets link_control to ENABLE when full control is passed to the 100BASE-X PHY.

24.3.1.6.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in Clause 28.

24.3.1.6.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4.

24.3.1.7 PMA_RXERROR.indicate

This primitive is generated by the PMA to indicate that an error has been detected during a carrier event.

24.3.1.7.1 Semantics of the service primitive

PMA_RXERROR.indicate (rxerror_status)

The rxerror_status parameter can take on one of two values: ERROR or NO_ERROR, indicating whether the received carrier event contains a detectable error (ERROR) or not (NO_ERROR). A carrier event is considered to be in error when it is not started by a Start-of-Stream Delimiter.

24.3.1.7.2 When generated

The PMA generates this primitive whenever a new, non-squelched carrier event is not started by a Start-of-Stream Delimiter.

24.3.1.7.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.1.8 PMA_LPILINKFAIL.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to control one of the link failure conditions of the Link Monitor in the PMA (see 24.2.4.3 and Figure 24–12).

24.3.1.8.1 Semantics of the service primitive

PMA_LPILINKFAIL.request (lpi_link_fail)

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The lpi_link_fail parameter takes on one of two values, TRUE or FALSE, indicating whether a link failure condition has been set (TRUE) or not (FALSE). The value of TRUE, when in the LPI mode, sets the link_status of the Link Monitor to FAIL (see 24.3.4.4 and Figure 24–15).

24.3.1.8.2 When generated

The PCS generates this primitive to indicate a link failure condition caused by the loss of Refresh signal when in the LPI mode.

24.3.1.8.3 Effect of receipt

This primitive affects operation of the PMA Link Monitor function as described in 24.3.4.4.

24.3.1.9 PMA_RXLPI.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to indicate that the receiver is in the LPI mode (see 24.2.4.3 and Figure 24–12).

24.3.1.9.1 Semantics of the service primitive

PMA_RXLPI.request (rx_lpi)

The rx_lpi parameter takes on one of two values, TRUE or FALSE, indicating whether the receiver is in the LPI mode (TRUE) or not (FALSE).

24.3.1.9.2 When generated

The PCS generates this primitive to indicate the LPI mode.

24.3.1.9.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as described in 24.3.4.4. Other use of receipt of this primitive by the client is unspecified by the PMA sublayer.

24.3.2 Functional requirements

The 100BASE-X PMA comprises the following functions:

a) Mapping of transmit and receive code-bits between the PMA Service Interface and the PMD Service Interface.
b) Link Monitor, which maps the PMD_SIGNAL.indicate primitive to the PMA_LINK.indicate primitive, indicating the availability of the underlying PMD.
c) Carrier Detection, which generates the PMA_CARRIER.indicate and PMA_RXERROR.indicate primitives from inspection of received PMD signals.
d) Far-End Fault (optional), comprised of the Far-End Fault Generate and Far-End Fault Detect processes, which sense receive channel failures and send the Far-End Fault Indication, and sense the Far-End Fault Indication.
e) EEE capability, which disables the Far-End Fault function and modifies the link down condition with the PMA_RXLPI.request primitive.

Figure 24–4 includes a functional block diagram of the PMA.

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24.3.2.1 Far-End fault

Auto-Negotiation provides a Remote Fault capability useful for detection of asymmetric link failures; i.e., channel error conditions detected by the far-end station but not the near-end station. Since Auto-Negotiation is specified only for media supporting eight-pin modular connectors, such as used by 100BASE-TX over twisted pair, Auto-Negotiation's Remote Fault capability is unavailable to other media for which it may be functionally beneficial, such as 100BASE-TX over shielded twisted pair or 100BASE-FX. A remote fault capability for 100BASE-FX is particularly useful due to this medium's applicability over longer distances (making end-station checking inconvenient) and for backbones (in which detection of link failures can trigger redundant systems).

For these reasons, 100BASE-X provides an optional Far-End Fault facility when Auto-Negotiation cannot be used. Far-End Fault shall not be implemented for media capable of supporting Auto-Negotiation.

When no signal is being received, as indicated by the PMD's signal detect function, the Far-End Fault feature permits the station to transmit a special Far-End Fault Indication to its far-end peer. The Far-End Fault Indication is sent only when a physical error condition is sensed on the receive channel. In all other situations, including reception of the Far-End Fault Indication itself, the PMA passes through tx_code-bit. (Note that the Far-End Fault architecture is such that IDLEs are automatically transmitted when the Far-End Fault Indication is detected. This is necessary to re-establish communication when the link is repaired.)

The Far-End Fault Indication is comprised of three or more repeating cycles, each of 84 ONEs followed by a single ZERO. This signal is sent in-band and is readily detectable but is constructed so as to not satisfy the 100BASE-X carrier sense criterion. It is therefore transparent to the PMA's client and to stations not implementing Far-End Fault.

As shown in Figure 24–4, Far-End Fault is implemented through the Far-End Fault Generate, Far-End Fault Detect, and the Link Monitor processes.

The Far-End Fault Generate process, which is interposed between the incoming tx_code-bit stream and the TX process, is responsible for sensing a receive channel failure (signal_status=OFF during the normal operation) and transmitting the Far-End Fault Indication in response. The transmission of the Far-End Fault Indication may start or stop at any time depending only on signal_status. The Far-End Fault shall not be generated when in the LPI mode.

The Far-End Fault Detect process continuously monitors rx_code-bits from the RX process for the Far-End Fault Indication. Detection of the Far-End Fault Indication disables the station by causing the Link Monitor process to deassert link_status, which in turn causes the station to source IDLEs. Far-End Fault detection can also be used by management functions not specified in this clause.

24.3.2.2 Comparison to previous IEEE 802.3 PMAs

Previous IEEE 802.3 PMAs perform the additional functions of SQE Test and Jabber. Neither of these functions is implemented in the 100BASE-X PMA.

SQE Test is provided in other Physical Layers to check the integrity of the Collision Detection mechanism independently of the Transmit and Receive capabilities of the Physical Layer. Since 100BASE-X effects collision detection by sensing receptions that occur during transmissions, collision detection is dependent on the health of the receive channel. By checking the ability to properly receive signals from the PMD, the Link Monitor function therefore functionally subsumes the functions previously implemented by SQE Test.

The Jabber function prevents a DTE from causing total network failure under certain classes of faults. When using mixing media (e.g., coaxial cables or passive optical star couplers), this function must naturally be implemented in the DTE. 100BASE-X requires the use of an active repeater, with one DTE or repeater

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attached to each port. As an implementation optimization, the Jabber function has therefore been moved to the repeater in 100BASE-X.

24.3.2.3 EEE capability

EEE capability, when communicated by the PMA_RXLPI.request primitive, affects the PMA in two ways. It disables the operation of the Far-End Fault processes to ignore the frequent on and off activity of signal_status. It receives link failure detection as communicated by the PMA_LPILINKFAIL.request primitive and changes the Link Monitor process to allow an exit from the LPI mode to a link down state. The EEE capability of the PMA is required only if the PCS supports EEE. If LPI is implemented, the operation of the PMA shall comply with the requirements in this subclause.

24.3.3 State variables

24.3.3.1 Constants

FEF_CYCLES

The number of consecutive cycles (of FEF_ONES ONEs and a single ZERO) necessary to indicate the Far-End Fault Indication. This value is 3.

FEF_ONES

The number of consecutive ONEs to be transmitted for each cycle of the Far-End Fault Indication. This value is 84.

24.3.3.2 Variables

carrier_status

The carrier_status parameter to be communicated by the Carrier Detect process through the PMA_CARRIER.indicate primitive. Carrier is defined as receipt of two noncontiguous ZEROs in 10 code-bits.

Values: ON; carrier is being received
OFF; carrier is not being received

faulting

The faulting variable set by the Far-End Fault Detect process, when implemented, indicating whether or not a Far-End Fault Indication is being sensed. This variable is used by the Link Monitor process to force link_status to FAIL.When Far-End Fault is not implemented, this variable is always FALSE.

Values: TRUE; Far-End Fault Indication is being sensed
FALSE; Far-End Fault Indication is not being sensed

link_control

The link_control parameter as communicated by the PMA_LINK.request primitive. When Auto-Negotiation is not implemented, the value of link_control is always ENABLE. See Clause 28 for a complete definition.

link_status

The link_status parameter as communicated by the Link Monitor process through the PMA_LINK.indicate primitive.

Values: FAIL; the receive channel is not intact

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READY; the receive channel is intact and ready to be enabled by Auto-Negotiation
OK; the receive channel is intact and enabled for reception

r_bits [9:0]

In Carrier Detect, a vector of the 10 most recently received code-bits from the PMD RX process. r_bits [0] is the most recently received (newest) code-bit; r_bits [9] is the least recently received code-bit (oldest). r_bits is an internal variable used exclusively by the Carrier Detect process.

rx_code-bit

The rx_code-bit parameter as delivered by the RX process, which operates in synchronism with the PMD_UNITDATA.indicate primitive. rx_code-bit is the most recently received code-bit from the PMD after conversion from NRZI.

rxerror_status

The rxerror_status parameter to be communicated by the Carrier Detect process through the PMA_RXERROR.indicate primitive.

Values: NO_ERROR; no error detected in the carrier event being received
ERROR; the carrier event being received is in error

signal_status

The signal_status parameter as communicated by the PMD_SIGNAL.indicate primitive.

Values: ON; the quality and level of the received signal is satisfactory
OFF; the quality and level of the received signal is not satisfactory

tx_code-bit_in

In Link Fault Generate, the tx_code-bit parameter as conveyed to the PMA from the PMA client by the PMA_UNITDATA.request.

tx_code-bit_out

In Link Fault Generate, the tx_code-bit parameter to be passed to the TX process. Note that this is called tx_code-bit by the TX process.

The following variables are required only for the optional EEE capability:

lpi_link_fail

The lpi_link_fail parameter is communicated by the PMA_LPILINKFAIL.request primitive. In the LPI mode, this variable is generated by the Receive process of the PCS to control the transition to a Link Down state. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE; local receiver has detected a link failure status when in an LPI state
FALSE; local receiver is functioning normally when in an LPI state

rx_lpi

The rx_lpi parameter is communicated by the PMA_RXLPI.request primitive. This variable is generated by the Receive process of the PCS to indicate the LPI mode. In the absence of the optional EEE capability, the PHY shall operate as if the value of this variable is FALSE.

Values: TRUE; local receiver is in the LPI mode
FALSE; local receiver is in the normal operation mode

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24.3.3.3 Functions

SHIFTLEFT (rx_bits)

In Carrier Detect, this function shifts rx_bits left one bit placing rx_bits [8] in rx_bits [9], rx_bits [7] in rx_bits [8] and so on until rx_bits [1] gets rx_bits [0].

24.3.3.4 Timers

stabilize_timer

An implementation-dependent delay timer between 330 µs and 1000 µs, inclusive, to ensure that the link is stable.

24.3.3.5 Counters

num_cycles

In Link Fault Detect, a counter containing the number of consecutive Far-End Fault cycles currently sensed. This counter gets reset on initialization or when the bit stream fails to qualify as a potential Far-End Fault Indication. It never exceeds FEF_CYCLES.

num_ones

This represents two separate and independent counters: In Link Fault Generate, a counter containing the number of consecutive ONEs already sent during this cycle of the Far-End Fault Indication. In Link Fault Detect, a counter containing the number of consecutive ONEs currently sensed; it gets reset whenever a ZERO is detected or when the bit stream fails to qualify as a potential Far-End Fault Indication. These counters never exceed FEF_ONES.

24.3.3.6 Messages

PMD_UNITDATA.indicate (rx_nrzi-bit)

A signal sent by the PMD signifying that the next nrzi-bit is available from the medium. nrzi-bit is converted (instantaneously) to code-bit by the RX process and used by the Carrier Detect process.

5xPMD_UNITDATA.indicates

In Carrier Detect, this shorthand notation represents repetition of the preceding state five times synchronized with five successive PMD_UNITDATA.indicates.

PMA_UNITDATA.request (tx_code-bit)

A signal sent by the PMA's client signifying that the next nrzi-bit is available for transmission. For this process, the tx_code-bit parameter is interpreted as tx_code-bit_in.

24.3.4 Process specifications and state diagrams

24.3.4.1 TX

The TX process passes data from the PMA's client directly to the PMD. The PMA shall implement the TX process as follows: Upon receipt of a PMA_UNITDATA.request (tx_code-bit), the PMA performs a conversion to NRZI format and generates a PMD_UNITDATA.request (tx_nrzi-bit) primitive with the same logical value for the tx_nrzi-bit parameter. Note that tx_code-bit is equivalent to tx_code-bit_out of the Link Fault Generate process when implemented.

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24.3.4.2 RX

The RX process passes data from the PMD directly to the PMA's client and to the Carrier Detect process. The PMA shall implement the RX process as follows: Upon receipt of a PMD_UNITDATA.indicate (rx_nrzi-bit), the PMA performs a conversion from NRZI format and generates a PMA_UNITDATA.indicate (rx_code-bit) primitive with the same logical value for the rx_code-bit parameter.

24.3.4.3 Carrier detect

The PMA Carrier Detect process provides repeater clients an indication that a carrier event has been sensed and an indication if it is deemed in error. A carrier event is defined as receipt of two non-contiguous ZEROS within any 10 rx_code-bits. A carrier event is in error if it does not start with an SSD. The Carrier Detect process performs this function by continuously monitoring the code-bits being delivered by the RX process, and checks for specific patterns that indicate non-IDLE activity and SSD bit patterns.

The Carrier Detect process collects code-bits from the PMD RX process. r_bits [9:0] represents a sliding, 10-bit window on the code-bit sequence, with newly received code-bits from the RX process being shifted into r_bits [0]. The process shifts the r_bits vector to the left, inserts the newly received code-bit into position 0, and waits for the next PMD.UNITDATA.indicate before repeating the operation. This is depicted in Figure 24–13. The Carrier Detect process monitors the r_bits vector until it detects two noncontiguous ZEROS in the incoming code-bit sequence. This signals a transition of carrier_status from OFF to ON. Each new carrier is further examined for a leading SSD (1100010001) with rxerror_status set to ERROR if it is not confirmed. A pattern of 10 contiguous ONEs in the stream indicates a return to carrier_status = OFF. Code-bit patterns of contiguous ONEs correspond to IDLE code-groups in the PCS, per the encoding specified in 24.2.2.1.

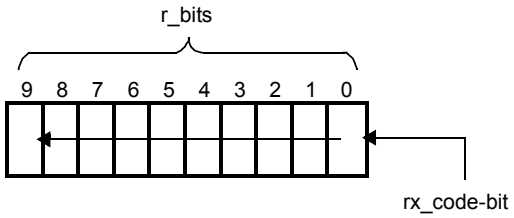


Figure 24–13—Carrier Detect reference diagram

The PMA shall, if it is supporting a repeater, implement the Carrier Detect process as depicted in Figure 24–14 including compliance with the associated state variables as specified in 24.3.3.

24.3.4.4 Link Monitor

The Link Monitor process is responsible for determining whether the underlying receive channel is providing reliable data. Failure of the underlying channel typically causes the PMA's client to suspend normal actions. The Link Monitor process takes advantage of the PMD sublayer's continuously signaled transmission scheme, which provides the PMA with a continuous indication of signal detection on the channel through signal_status as communicated by the PMD_SIGNAL.indicate primitive. It responds to control by Auto-Negotiation, when implemented, which is effected through the link_control parameter of PMA_SIGNAL.request.

The Link Monitor process monitors signal_status, setting link_status to FAIL whenever signal_status is OFF during the normal operation or when Auto-Negotiation sets link_control to DISABLE. If the EEE capability is supported, when the receiver is in the LPI mode, the assertion of lpi_link_fail shall set the link_status to FAIL and eventually brings the receiver out of the LPI mode. The link is deemed to be reliably operating

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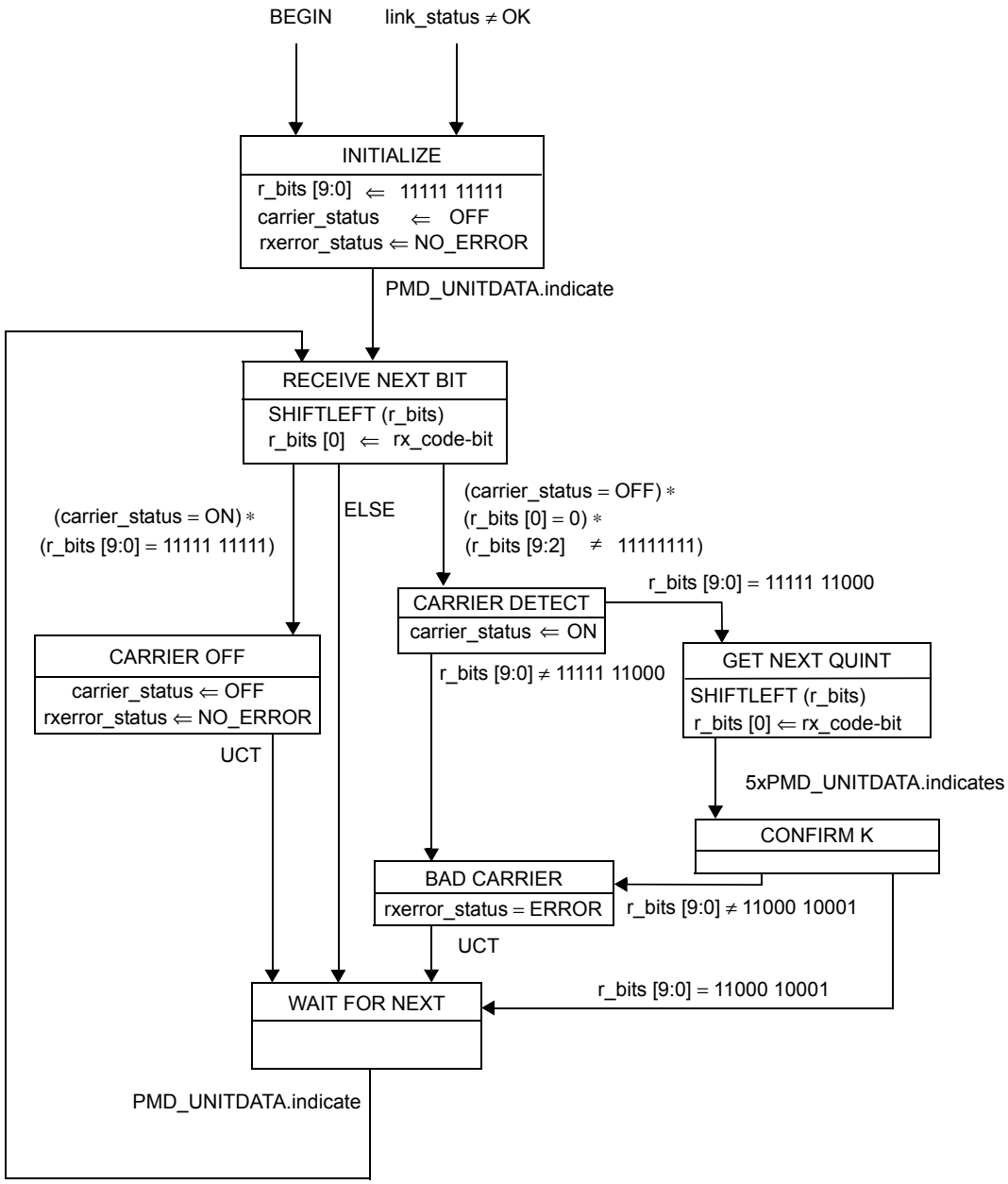
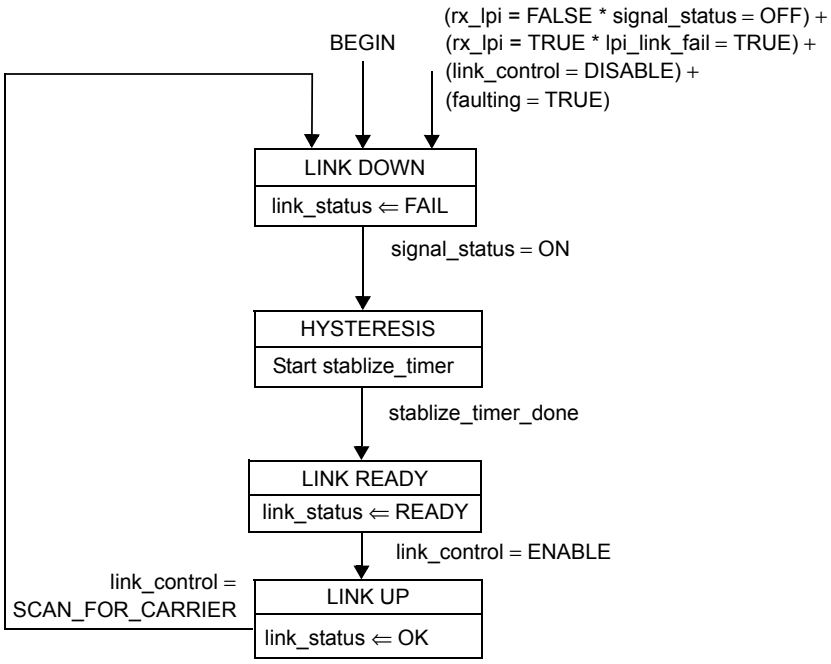


Figure 24–14—Carrier Detect state diagram

when signal_status has been continuously ON for a period of time. This period is implementation dependent but not less than 330 µs or greater than 1000 µs. If so qualified, Link Monitor sets link_status to READY in order to synchronize with Auto-Negotiation, when implemented. Auto-Negotiation permits full operation by setting link_control to ENABLE. When Auto-Negotiation is not implemented, Link Monitor operates with link_control always set to ENABLE.

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The PMA shall implement the Link Monitor process as depicted in Figure 24–15 including compliance with the associated state variables as specified in 24.3.3.



NOTE 1—The variables link_control and link_status are designated as link_control_[TX] and link_status_[TX], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

NOTE 2—The variables rx_lpi and lpi_link_fail are only required for the EEE capability and should be treated as if the value of these two variables is FALSE otherwise.

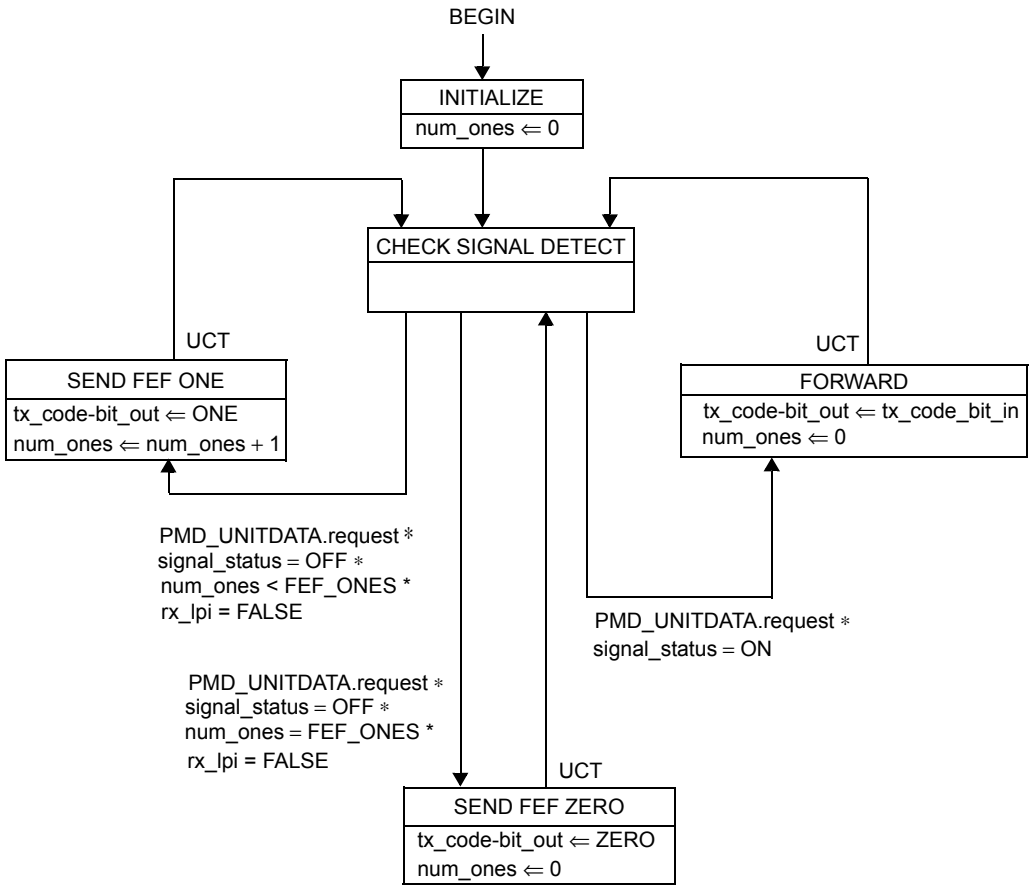
Figure 24–15—Link Monitor state diagram

24.3.4.5 Far-End Fault Generate

Far-End Fault Generate simply passes tx_code-bits to the TX process when signal_status=ON. When signal_status=OFF and not in the LPI mode, it repetitively generates each cycle of the Far-End Fault Indication until signal_status is reasserted.

If Far-End Fault is implemented, the PMA shall implement the Far-End Fault Generate process as depicted in Figure 24–16 including compliance with the associated state variables as specified in 24.3.3.

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NOTE—The variable rx_lpi is only required for the EEE capability and should be treated as if the value of this variable is FALSE otherwise.

Figure 24–16—Far-End Fault Generation state diagram

24.3.4.6 Far-End Fault Detect

Far-End Fault Detect passively monitors the rx_code-bit stream from the RX process for the Far-End Fault Indication. It does so by maintaining counters for the number of consecutive ONEs seen since the last ZERO (num_ones) and the number of cycles of 84 ONEs and a single ZERO (num_cycles). The Far-End Fault Indication is denoted by three or more cycles, each of 84 ONEs and a single ZERO. Note that the number of consecutive ONEs may exceed 84 on the first cycle.

If Far-End Fault is implemented, the PMA shall implement the Far-End Fault Detect process as depicted in Figure 24–17 including compliance with the associated state variables as specified in 24.3.3.

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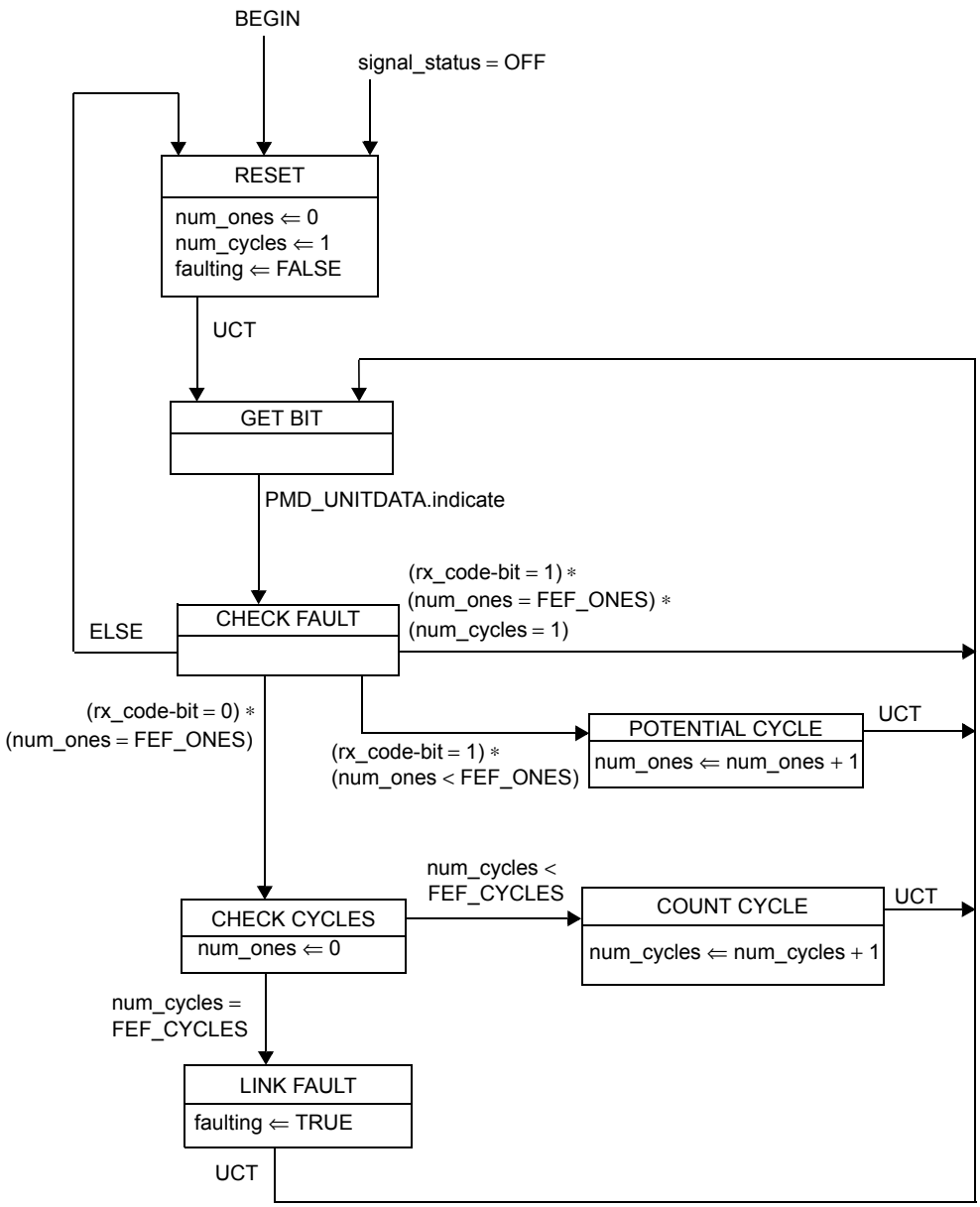


Figure 24–17—Far-End Fault Detect state diagram

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24.4 Physical Medium Dependent (PMD) sublayer service interface

24.4.1 PMD service interface

The following specifies the services provided by the PMD. The PMD is a sublayer within 100BASE-X and may not be present in other 100BASE-T PHY specifications. PMD services are described in an abstract manner and do not imply any particular implementation. It should be noted that these services are functionally identical to those defined in the FDDI standards, such as ISO/IEC 9314-3:1990 and ANSI X3.263-1995, with the following three exceptions:

a) 100BASE-X does not include a Station Management (SMT) function; therefore the PMD-to-SMT interface defined in ISO/IEC 9314-3:1990 and ANSI X3.263-1995.
b) 100BASE-X does not support multiple instances of a PMD in service to a single PMA; therefore, no qualifiers are needed to identify the unique PMD being referenced.
c) 100BASE-X may support LPI for the EEE capability.

There are also *editorial* differences between the interfaces specified here and in the referenced standards, as required by the context of 100BASE-X.

The PMD Service Interface supports the exchange of nrzi-bits between PMA entities. The PMD translates the nrzi-bits to and from signals suitable for the specified medium.

The following primitives are defined:

PMD_UNITDATA.request
PMD_UNITDATA.indicate
PMD_SIGNAL.indicate
PMD_RXQUIET.request
PMD_TXQUIET.request

24.4.1.1 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of nrzi-bits) from the PMA to the PMD.

24.4.1.1.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_nrzi-bit)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of nrzi-bits. The tx_nrzi-bit parameter can take one of two values: ONE or ZERO.

24.4.1.1.2 When generated

The PMA continuously sends, at a nominal 125 Mb/s rate, the PMD the appropriate nrzi-bits for transmission on the medium.

24.4.1.1.3 Effect of receipt

Upon receipt of this primitive, the PMD converts the specified nrzi-bit into the appropriate signals on the MDI.

24.4.1.2 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of nrzi-bits) from the PMD to the PMA.

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24.4.1.2.1 Semantics of the service primitive

PMD_UNITDATA.indicate (rx_nrzi-bit)

The data conveyed by PMD_UNITDATA.indicate is a continuous nrzi-bit sequence. The rx_nrzi-bit parameter can take one of two values: ONE or ZERO.

24.4.1.2.2 When generated

The PMD continuously sends nrzi-bits to the PMA corresponding to the signals received from the MDI.

24.4.1.2.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.3 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signal being received from the MDI.

24.4.1.3.1 Semantics of the service primitive

PMD_SIGNAL.indicate (signal_status)

The signal_status parameter can take on one of two values: ON or OFF, indicating whether the quality and level of the received signal is satisfactory (ON) or unsatisfactory (OFF). When signal_status = OFF, then rx_nrzi-bit is undefined, but consequent actions based on PMD_SIGNAL.indicate, where necessary, interpret rx_nrzi-bit as logic ZERO.

24.4.1.3.2 When generated

The PMD generates this primitive to indicate a change in the value of signal_status.

24.4.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.4 PMD_RXQUIET.request

This primitive is generated by the Receive Process of the PCS only if EEE is supported to indicate that the receiver is in the LPI mode and the line is in the Quiet state (see 24.2.4.3 and Figure 24–12).

24.4.1.4.1 Semantics of the service primitive

PMD_RXQUIET.request(rx_quiet)

The rx_quiet parameter takes on one of two values, TRUE or FALSE, indicating whether the receiver is in the Quiet state (TRUE) or not (FALSE).

24.4.1.4.2 When generated

The PCS generates this primitive to indicate a Quiet state of the transmitter in the LPI mode.

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24.4.1.4.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.5.2. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.1.5 PMD_TXQUIET.request

This primitive is generated by the Transmit Process of the PCS only if EEE is supported to indicate that the transmitter is in the LPI mode and the line is in the Quiet state (see 24.2.4.2 and Figure 24–8).

24.4.1.5.1 Semantics of the service primitive

PMD_TXQUIETrequest(tx_quiet)

The tx_quiet parameter takes on one of two values, TRUE or FALSE, indicating whether the transmitter is in the Quiet state (TRUE) or not (FALSE).

24.4.1.5.2 When generated

The PCS generates this primitive to indicate a Quiet state of the transmitter in the LPI mode.

24.4.1.5.3 Effect of receipt

This primitive affects operation of the PMD function of type 100BASE-TX as described in 25.5.1. Other use of receipt of this primitive by the client is unspecified by the PMD sublayer.

24.4.2 Medium Dependent Interface (MDI)

The MDI, a physical interface associated with a PMD, is comprised of an electrical or optical medium connector. The 100BASE-X MDIs, defined in subsequent clauses, are specified by reference to the appropriate FDDI PMD, such as in ISO/IEC 9314-3:1990 and ANSI X3.263-1995, together with minor modifications (such as connectors and pin-outs) necessary for 100BASE-X.

24.5 Compatibility considerations

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS, PMA, or PMD. However, if an exposed interface is provided to the PCS, it shall comply with the requirements for the MII, as specified in Clause 22.

24.6 Delay constraints

In half duplex mode, proper operation of a CSMA/CD LAN demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY, and repeater implementers must conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

In full duplex mode, predictable operation of the (optional) MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

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MAC constraints are contained in Clause 21. Topological constraints are contained in Clause 29. MAC Control sublayer constraints are contained in Clause 31.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI. Although 100BASE-TX output is scrambled, it is assumed that these measurements are made via apparatuses that appropriately account for this.

24.6.1 PHY delay constraints (exposed MII)

Every 100BASE-X PHY with an exposed MII shall comply with the bit delay constraints specified in Table 24–2 and Table 24–3. These figures apply for all 100BASE-X PMDs.

Table 24–2—Bit delay constraints

a) MDI to MII delay constraints (exposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output	6	14	TX_CLK rising	1st bit of /J/
	MDI input to CRS assert		20	1st bit of /J/	
	MDI input to CRS deassert (aligned)	13	24	1st bit of /T/	
	MDI input to CRS deassert (unaligned)	13	24	1st ONE	
	MDI input to COL assert		20	1st bit of /J/	
	MDI input to COL deassert (aligned)	13	24	1st bit of /T/	
	MDI input to COL deassert (unaligned)	13	24	1st ONE	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS deassert	0	16	TX_CLK rising	

Table 24–3—Bit delay constraints *(continued)*

b) PHY delay constraints (exposed MII, full duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MII ⇔ MDI	TX_EN sampled to MDI output		14	TX_CLK rising	1st bit of /J/
	MDI Input to RX_DV deassert		32	first bit of /T/	RX_CLK rising

24.6.2 DTE delay constraints (unexposed MII)

Every 100BASE-X DTE with no exposed MII shall comply with the bit delay constraints specified in Table 24–4. These figures apply for all 100BASE-X PMDs.

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Table 24–4—DTE delay constraints (unexposed MII, half duplex mode)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MDI	MAC transmit start to MDI output		18		1st bit of /J/
	MDI input to MDI output (worst-case nondeferred transmit)		54	1st bit of /J/	1st bit of /J/
	MDI input to collision detect		28	1st bit of /J/	
	MDI input to MDI output = Jam (worst case collision response)		54	1st bit of /J/	1st bit of jam

24.6.3 Carrier deassertion/assertion constraint (half duplex mode only)

To ensure fair access to the network, each DTE shall, additionally, satisfy the following:

(MAX MDI to MAC Carrier Deassert Detect) – (MIN MDI to MAC Carrier Assert Detect) < 13

24.7 Environmental specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801.

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24.8 Protocol implementation conformance statement (PICS) proforma for Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X[6]

24.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

24.8.2 Identification

24.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

24.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 24, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	

Date of Statement	

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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24.8.2.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*DTE	Supports DTE without MII	24.4	O/1		
*REP	Supports Repeater without MII	24.4	O/1		
*MII	Supports exposed MII interface	24.4	O/1		
*PCS	Implements PCS functions	24.2	REP: O DTE: M MII: M		
PMA	Implements PMA RX, TX and Link Monitor functions	24.3	M		
*LPC	PCS implementation of LPI	24.2	PCS:O		
*LPM	PMA implementation of LPI	24.3	LPC:M		
*NWC	Medium capable of supporting Auto-Negotiation		O		See Clause 28
*FEF	Implements Far-End Fault	24.3.2.1	NWC: X LPM:X		
NWY	Supports Auto-Negotiation (Clause 28)	24.1.4.4	NWC: O LPC:M		See Clause 28

24.8.3 PICS proforma tables for the Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 100BASE-X

24.8.3.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Compliance with MII requirements	24.4	MII:M		See Clause 22
GN2	Environmental specifications	24.7	M		

24.8.3.2 PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PS1	Transmit Bits process	24.2.4.1	PCS:M		
PS2	Transmit process	24.2.4.2	PCS:M		
PS3	Receive Bits process	24.2.4.3	PCS:M		
PS4	Receive process	24.2.4.4	PCS:M		
PS5	Carrier Sense process	24.2.4.5	PCS:M		

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24.8.3.3 PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PA1	TX process	24.3.4.1	M		
PA2	RX process	24.3.4.2	M		
PA3	Carrier Detect process	24.3.2.1	REP: M		
PA4	Link Monitor process	24.3.4.4	M		
PA5	Far-End Fault Generate process	24.3.4.5	FEF: M		
PA6	Far-End Fault Detect process	24.3.4.6	FEF: M		

24.8.3.4 Timing

Item	Feature	Subclause	Status	Support	Value/Comment
TM1	Support for MII signals TX_CLK and RX_CLK	24.2.2.3	MII:M		See Clause 22
TM2	Accuracy of code-bit_timer	24.2.3	M		
TM3	Compliance with PHY bit delay constraints	24.6.1	MII:M REP: O		
TM4	Compliance with DTE bit delay constraints	24.6.2	DTE:M		
TM5	Compliance with Carrier Deassert/Assert Constraint	24.6.3	DTE:M		

24.8.3.5 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
LF1	lpi_rx_ti_timer	24.2.3.4	LPC:M		The timer has a period between 0.8–0.9 μs.
LF2	lpi_rx_tq_timer	24.2.3.4	LPC:M		The timer has a period between 24–26 ms.
LF3	lpi_rx_ts_timer	24.2.3.4	LPC:M		The timer has a period between 240–260 μs.
LF4	lpi_rx_tw_timer	24.2.3.4	LPC:M		The timer has a period that does not exceed 20.5 μs.
LF5	LPI wake error counter	24.2.3.4	LPC:M		Increment the wake error counter for each transition of lpi_rx_tw_timer_done from false to true.

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Item	Feature	Subclause	Status	Support	Value/Comment
LF6	lpi_tx_tq_timer	24.2.3.4	LPC:M		The timer has a period between 20–22 ms.
LF7	link failure caused by lpi_rx-_tq_timer	24.2.3.4	LPC:M		The receiver assumes a link failure if the PHY fails to receive a valid Refresh or Wake signal before the lpi_rx_tq_timer expires.
LF8	lpi_tx_ts_timer	24.2.3.4	LPC:M		The timer has a period between 200–220 μs.
LF9	lpi_link_fail_timer	24.2.3.4	LPC:M		The timer has a period between 90–110 μs.
LF11	lpi_link_fail	24.3.3.2	LPM:M		The PHY operates as if the value of this variable is FALSE in the absence of the optional EEE capability.
LF12	rx_lpi	24.3.3.2	LPM:M		The PHY operates as if the value of this variable is FALSE in the absence of the optional EEE capability.
LF13	link_status affected by lpi_link_fail	24.3.4.4	LPM:M		The assertion of lpi_link_fail sets the link_status to FAIL if the EEE is supported and the receiver is in the LPI mode.

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25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.1 Overview

This clause specifies the 100BASE-X PMD (including MDI) and baseband medium for twisted-pair wiring, 100BASE-TX. In order to form a complete 100BASE-TX Physical Layer, the 100BASE-X PMD (including MDI) shall be integrated with the 100BASE-X PCS and PMA of Clause 24, which are assumed incorporated by reference. As such, the 100BASE-TX PMD shall comply with the PMD service interface specified in 24.4.1.

25.1.1 State diagram conventions

The body of this standard is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. The notation used in the state diagrams follows the conventions of 21.5; state diagram timers follow the conventions of 14.2.3.2.

25.2 Functional specifications

The 100BASE-TX PMD (and MDI) is specified by incorporating the FDDI TP-PMD standard, ANSI X3.263: 1995 (TP-PMD), by reference, with the modifications noted below. This standard provides support for Category 5 twisted pair cabling. For improved legibility in this clause, ANSI X3.263: 1995 (TP-PMD), will henceforth be referred to as TP-PMD.

25.3 General exceptions

The 100BASE-TX PMD is precisely the PMD specified as TP-PMD, with the following general modifications:

a) The Scope and General description discussed in TP-PMD 1 and 5 relate to the use of those standards with an FDDI PHY, ISO/IEC 9314-1:1989, and MAC, ISO/IEC 9314-2:1989. These sections are not relevant to the use of the PMD with 100BASE-X.
b) The Normative references, Definitions and Conventions of TP-PMD 2, 3, and 4 are used only as necessary to interpret the applicable sections of TP-PMD referenced in this clause.
c) The PMD Service Specifications of TP-PMD 6 are replaced by those specified in 24.4.1. The 100BASE-TX PMD Service specification is a proper subset of the PMD Service Specification in TP-PMD.
d) The twisted-pair cabling specifications of TP-PMD 11.1 are replaced by those specified in 25.4.9.
e) 100BASE-TX optionally supports Energy-Efficient Ethernet (EEE), as described in Clause 78, with its Low Power Idle (LPI). Two new service primitives PMD_RXQUIET.request(rx_quiet) (see 24.4.1.4) and PMD_TXQUIET.request(tx_quiet) (see 24.4.1.5) are generated by the PCS to pass the energy saving requests.
f) There are minor terminology differences between this standard and TP-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 25–1.

25.4 Specific requirements and exceptions

The 100BASE-TX PMD (including MDI) shall comply to the requirements of TP-PMD, 7, 8, 9, 10, and 11, and normative Annex A with the exceptions listed below. In TP-PMD, informative annexes B, C, E, G, I, and

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Table 25–1—Interpretation of general FDDI terms and concepts

FDDI term or concept	Interpretation for 100BASE-TX
bypass	<unused>
Connection Management (CMT)	<no comparable entity>
frame	stream
Halt Line State (HLS)	<unused>
hybrid mode	<no comparable entity>
MAC (or MAC-2)	MAC
Master Line State (MLS)	<unused>
maximum frame size = 9000 symbols	maximum stream size = 4018 code-groups
PHY (or PHY-2)	PMA; i.e., PMD client
PHY Service Data Unit (SDU)	stream
PM_SIGNAL.indication (Signal_Detect)	PMD_SIGNAL.indication (signal_status)
PM_UNITDATA.indication (PM_Indication)	PMD_UNITDATA.indication (nrzi-bit)
PM_UNITDATA.request (PM_Request)	PMD_UNITDATA.request (nrzi-bit)
preamble	inter-packet IDLEs
Quiet Line State (QLS)	<unused>
SM_PM_BYPASS.request (Control_Action)	Assume: SM_PM_BYPASS.request(Control_Action = Insert)
SM_PM_CONTROL.request (Control_Action)	Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable)
SM_PM_SIGNAL.indication (Signal_Detect)	<unused>
Station Management (SMT)	<no comparable entity>
symbol	code-group

J, with exceptions listed below, provide additional information useful to PMD sublayer implementers. Where there is conflict between specifications in TP-PMD and those in this standard, those of this standard shall prevail.

25.4.1 Change to 7.2.3.1.1, “Line state patterns”

Descrambler synchronization on the Quiet Line State (QLS), Halt Line State (HLS), and Master Line State (MLS) Line State Patterns cited in TP-PMD 7.2.3.1.1 is optional.

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25.4.2 Change to 7.2.3.3, "Loss of synchronization"

The synchronization error triggered by PH_Invalid as defined in TP-PMD 7.2.3.3a is not applicable.

25.4.3 Change to Table 8-1, "Contact assignments for twisted pair"

100BASE-TX for twisted pair adopts the contact assignments of 10BASE-T. Therefore, the contact assignments shown in TP-PMD Table 8-1 shall instead be as depicted in Table 25–2.

Table 25–2—Twisted-pair MDI contact assignments

Contact	PHY without internal crossover MDI SIGNAL	PHY with internal crossover MDI SIGNAL
1	Transmit +	Receive +
2	Transmit –	Receive –
3	Receive +	Transmit +
4		
5		
6	Receive –	Transmit –
7		
8		

25.4.4 Deletion of 8.3, "Station labelling"

Clause 8.3 of TP-PMD shall not be applied to 100BASE-TX.

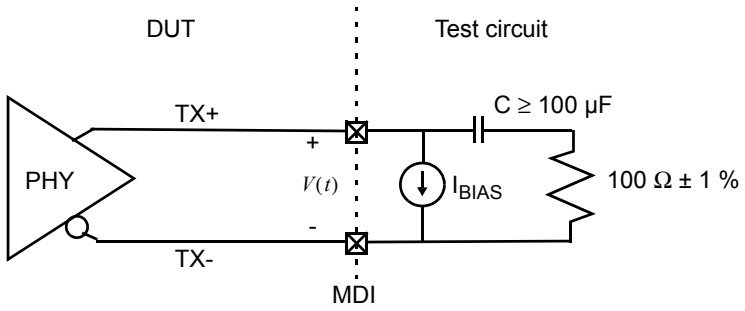
25.4.5 Change to 9.1.7, "Worst case droop of transformer"

A receiver in a Type 2 Endpoint PSE or Type 2 PD (see Clause 33) shall meet the requirements of 25.4.7. A transmitter in a Type 2 Endpoint PSE or Type 2 PD delivering or accepting more than 13.0 W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD, or meet the requirements of 25.4.5.1.

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25.4.5.1 Equivalent system time constant

While transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2, using the test circuit shown in Figure 25–1, the equivalent system time constant, τ, shall be greater than 2.4 μs when calculated using measurement points A and C as shown in Figure 25–2.



DUT = Device under test

NOTE— I_{BIAS} is the current I_{unb} / 2 defined in Clause 33.

Figure 25–1—Type 2 System time constant test circuit

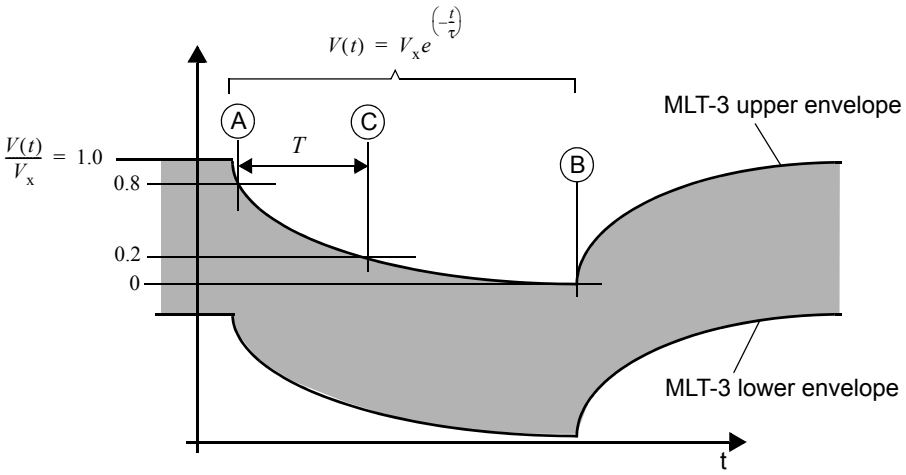


Figure 25–2—Type 2 System time constant measurement

Point B is the point of maximum baseline wander droop, and is the zero point for the vertical axis. Point A, with MDI voltage V_A, is earlier in time from B, with a magnitude that is 80 % of the MLT-3 upper envelope value. Point C, with MDI voltage V_C, is between A and B, with a magnitude that is 20 % of the MLT-3 upper envelope value. The time between A and C is *T*.

These measurements are to be made for the transmitter pair, observing the differential signal output at the MDI with intervening cable, meeting or exceeding the requirements of 25.4.7, less than 1 m long.

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The time constant of the transmitter MDI connected to the test circuit of Figure 25–1 is given by Equation (25–1).

$$\left\{ \tau = \frac{T}{\ln\left(\frac{V_A}{V_C}\right)} = \frac{2L}{R} \right\}_s \qquad (25–1)$$

where

τ	is the effective time constant of the transmitter
T	is the time in seconds from point A to point C as shown in Figure 25–2
V_A	is the MDI voltage at point A
V_C	is the MDI voltage at point C
L	is the open-circuit inductance of the Ethernet isolation transformer for all operating conditions
R	is the 100 Ω termination impedance

25.4.6 Replacement of 8.4.1, “UTP isolation requirements”

A PMD with a MDI that is a PI (see 33.1.3) shall meet the isolation requirements defined in 33.4.1.

A PMD with a MDI that is not a PI shall provide isolation between frame ground and all MDI leads including those not used by the 100BASE-TX PMD.

This electrical isolation shall withstand at least one of the following electrical strength tests.

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
b) 2250 V dc for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 µs (1.2 µs virtual front time, 50 µs virtual time of half value), as defined in IEC 60950-1:2001 Annex N.

There shall be no insulation breakdown, as defined in subclause 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

NOTE—In the case of a PMD with a MDI that is not a PI, these requirements are equivalent to those found in TP-PMD.

25.4.7 Addition to 10.1, “Receiver”

Differential voltage signals generated by a remote transmitter that meets the specifications of Clause 25; passed through a link specified in 25.4.8; and received at the MDI of a 100BASE-TX PMD in a Type 2 Endpoint PSE or a Type 2 PD shall be translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion.

25.4.8 Change to 9.1.9, “Jitter”

The jitter measurement specified in 9.1.9 of TP-PMD may be performed using scrambled IDLEs.

In the LPI mode, jitter shall be measured using scrambled SLEEP code-groups transmitted during the TX_SLEEP state (see Figure 24–8). Total transmit jitter with respect to a continuous unjittered reference shall not exceed 1.4 ns peak-to-peak with the exception that the jitter contributions from the clock transitions

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occurring during the TX_QUIET state and the first 5 μs of the TX_SLEEP state or the first 5 μs of the IDLE state following a TX_QUIET state are ignored. The jitter measurement time period shall be not less than 100 ms and not greater than 1 s.

25.4.9 Cable plant

The twisted-pair cabling specification of TP-PMD 11.1 is replaced by that specified in this subclause. The term "link segment" used in this subclause refers to a duplex channel of two pairs. Specifications for a link segment apply equally to each of the two pairs of a duplex channel. All implementations of the balanced cabling link shall be compatible at the MDI.

25.4.9.1 Cabling system characteristics

The cabling system used to support a 100BASE-TX duplex channel requires two pairs of Category 5 balanced cabling with a nominal impedance of 100 Ω. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995 (Class D).

NOTE—ISO/IEC 11801:2002 provides a specification (Class D) for media that exceeds the minimum requirements of this standard.

25.4.9.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Category 5 link segment of up to 100 m, will provide a reliable medium. The transmission parameters of the link segment include insertion loss, characteristics impedance, return loss, NEXT loss, and external coupled noise.

25.4.9.2.1 Insertion loss

The insertion loss of the link segment shall be less than,

$$\text{Insertion\_Loss}(f) < 2.1f^{0.529} + 0.4/f \qquad \text{(dB)}$$

at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within the link segment.

The insertion loss specification shall be met when the link segment is terminated in 100 Ω.

NOTE—The above equation approximates the insertion loss specification at 20°C for discrete frequencies of Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.9.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 100 MHz.

25.4.9.2.3 Return loss

Each link segment shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 100 MHz.

$$\text{Return\_Loss}(f) \begin{cases} 15 & (1 - 20\ \text{MHz}) \\ 15 - 10\log_{10}(f/20) & (20 - 100\ \text{MHz}) \end{cases} \text{(dB)}$$

where f is the frequency in MHz. The reference impedance shall be 100 Ω.

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25.4.9.2.4 Differential near-end crosstalk (NEXT)

In order to limit the crosstalk at the near end of a duplex channel, the differential pair-to-pair near-end crosstalk (NEXT) loss between the two pairs of a duplex channel shall be at least,

$27.1 - 16.8\log_{10}(f/100)$ (dB)

where f is the frequency over the range of 1 MHz to 100 MHz.

NOTE—The above equation approximates the NEXT loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB-67.

25.4.9.3 Noise environment

The 100BASE-TX noise environment consists of noise from external sources and could impact the objective BER. This noise may consist of sources outside the cabling that couple into the link segment via electric and magnetic fields. In addition noise from adjacent cables, referred to as alien crosstalk, may couple into the link segment. This alien crosstalk is generally present when cables are bound tightly together. To ensure robust operation a 100BASE-TX PHY should operate in the presence of an external noise as specified in 25.4.9.3.1.

25.4.9.3.1 External coupled noise

The differential noise coupled from external sources that is measured at the output of a filter connected to the output of the near end of a disturbed link segment should not exceed 40 mV peak-to-peak. The filter for this measurement is a fifth order Butterworth filter with a 3 dB cutoff at 100 MHz.

25.4.10 Replacement of 11.2, “Crossover function”

Subclause 11.2 of TP-PMD is replaced with the following:

A crossover function compliant with 14.5.2 shall be implemented except that a) the signal names are those used in TP-PMD, and b) the contact assignments for STP are those shown in Table 8-2 of TP-PMD. Note that compliance with 14.5.2 implies a recommendation that crossover (for both UTP and STP) be performed within repeater PHYs.

25.4.11 Change to A.2, “DDJ test pattern for baseline wander measurements”

The length of the test pattern specified in TP-PMD A.2 may be shortened to accommodate feasible 100BASE-X measurements, but shall not be shorter than 3000 code-groups.

NOTE—This pattern is to be applied to the MII. (When applied to the MAC, the nibbles within each byte are to be swapped, e.g., as delivered to the MAC, the test pattern would start, "60 c9 16 ...".)

25.4.12 Change to Annex G, “Stream cipher scrambling function”

An example of a stream cipher scrambling implementation is shown in TP-PMD Annex G. This may be modified to allow synchronization solely on the IDLE sequences between packets.

25.4.13 Change to Annex I, “Common mode cable termination”

The contact assignments shown in TP-PMD Figures I-1 and I-2 shall instead comply with those specified in Table 25–2.

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25.5 EEE capability

TP-PMD does not have an option to support EEE. In order to add this capability to existing TP-PMD specification, the TP-PMD 7.1.2, 7.2.2, 10.1.2, 10.1.3, and Table 4 are modified to incorporate the LPI function. This subclause only applies to the optional EEE capability. If LPI is implemented, the operation of the PMD shall comply with the requirements in this subclause.

25.5.1 Change to TP-PMD 7.1.2 “Encoder”

The Encoder receives the scrambled NRZ data stream from the scrambler (see TP-PMD 7.1.1) and encodes the stream into MLT3 code for presentation to the driver (see TP-PMD 7.1.3). MLT3 coding is similar to NRZI coding, but three instead of two levels are transmitted. The Encoder can be deactivated when in the LPI mode. The PMD Encoder function of the 100BASE-TX with EEE capability is identical to that of the TP-PMD except that the output of the Encoder is set to a value ZERO_VOLTAGE when the transmitter is in the Quiet state of the LPI mode (TX_QUIET, see Figure 24–8).

The PMD in the LPI mode shall implement the Encoder state diagram as depicted in Figure 25–3.

25.5.1.1 State variables

25.5.1.1.1 Variables

encoder_input
: Indicates the value of each scrambled NRZ bit to be encoded.

  Values: ZERO; the NRZ bit from the scrambler has a logical value 0
  ONE; the NRZ bit from the scrambler has a logical value 1

encoder_output
: Indicates the value from the encoder for each MLT-3 encoded bit.

  Values: POSITIVE_VOLTAGE; the output indicates a positive value of voltage to TP-PMD driver
  ZERO_VOLTAGE; the output indicates a zero value of voltage to TP-PMD driver
  NEGATIVE_VOLTAGE; the output indicates a negative value of voltage to TP-PMD driver

tx_quiet
: The tx_quiet parameter as communicated by the PMD_TXQUIET.request (tx_quiet) primitive. This variable is generated by the Transmit process of the PCS to control the power-saving function of the local transmitter. It sets the Encoder state diagram to an initial state of ZERO_V.

  Values: TRUE; the local transmitter is in the Quiet state
  FALSE; the local transmitter is not in the Quiet state

le_flag
: A Boolean set by the Encoder process to indicate whether the last non-zero value of encoder_output was POSITIVE_VOLTAGE. The flag le_flag is set upon entry to the PLUS_V state and is cleared upon entry to the MINUS_V state.

  Values: ONE; the encoder is in the PLUS_V state
  ZERO; the encoder is in the MINUS_V state

25.5.1.1.2 Messages

gotNRZbit.indicate

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A signal sent to the Encoder process by the scrambler after a scrambled NRZ text bit has been generated using recursive linear function by the scrambler from plaintext bit stream and is ready to transmit.

25.5.1.2 State diagram

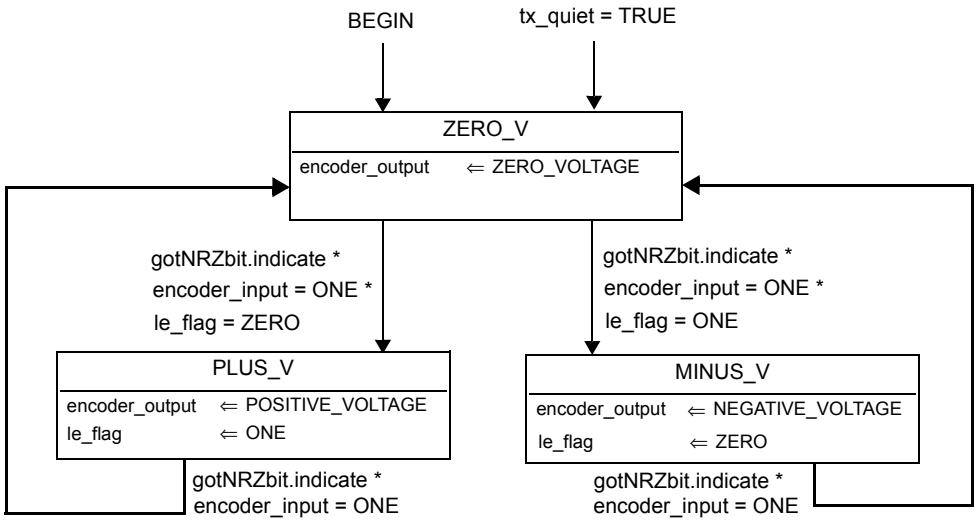


Figure 25–3—Encoder state diagram

25.5.2 Change to TP-PMD 7.2.2 “Decoder”

The Decoder receives the MLT3 encoded bit stream from the receiver (see TP-PMD 7.2.1), and decodes it into a NRZ encoded bit stream for presentation to the descrambler (see TP-PMD 7.2.3). The Decoder can be deactivated when in the LPI mode. The PMD Decoder function of the 100BASE-TX with EEE capability is identical to that of the TP-PMD except that the output of the Decoder is set to a value ZERO when the receiver is in the Quiet state of the LPI mode (RX_QUIET, Figure 24–12).

The PMD in the LPI mode shall implement the Decoder state diagram as depicted in Figure 25–4.

25.5.2.1 State variables

25.5.2.1.1 Variables

decoder_input
: Indicates the value of the MLT-3 encoded bit from the receiver.

  Values: ZERO; the MLT3 bit from the receiver has a logical value 0
  NONZERO; the MLT3 bit from the receiver has a non-zero logical value

decoder_output
: Indicates the value of the NRZ encoded bit.

  Values: ZERO; the output indicates a logical value of 0 to the descrambler
  ONE; the output indicates a logical value of 1 to the descrambler

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rx_quiet

The rx_quiet parameter as communicated by the PMD_RXQUIET.request (rx_quiet) primitive. This variable is generated by the Receive process of the PCS to control the power-saving function of local receiver. It sets the Decoder state diagram to an initial state of ZERO_VALUE.

Values: TRUE; the local receiver is in the Quiet state
FALSE; the local receiver is not in the Quiet state

prev_data

Indicates whether the last value of decoder_input was ZERO or NONZERO.

Values: ZERO; the last value of MLT3 bit of decoder_input has a logical value 0
NONZERO; the last value of MLT3 bit of decoder_input has a non-zero logical value

25.5.2.1.2 Messages

sentNRZbit.indicate

A signal sent to the Decoder process by the descrambler after an NRZ bit from ciphertext bit stream has been processed using recursive linear function and is ready to process the next bit from Decoder.

25.5.2.2 State diagram

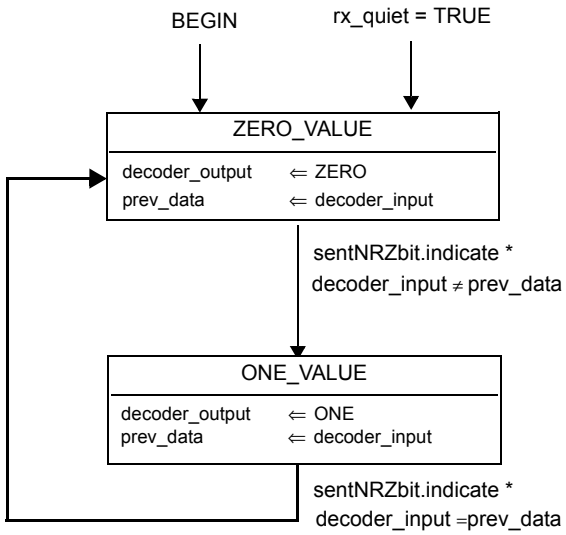


Figure 25–4—Decoder state diagram

25.5.3 Changes to 10.1.1.1 “Signal_Detect assertion threshold”

The TP-PMD 10.1.1.1 is applicable to the normal operation. In the LPI mode, when rx_lpi as communicated by the PMA_RXLPI.request primitive is asserted, Signal_Detect shall be asserted per 25.5.5 for any valid peak-to-peak signal, VSDA, of greater than 400 mV.

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25.5.4 Changes to 10.1.1.2 “Signal_Detect deassertion threshold”

The TP-PMD 10.1.1.2 is applicable to the normal operation. In the LPI mode, when rx_lpi is deasserted, Signal_Detect shall be deasserted per 25.5.6 for any valid peak-to-peak signal, VSDD, of smaller than 200 mV.

25.5.5 Change to 10.1.2 “Signal_Detect timing requirements on assertion”

The TP-PMD 10.1.2 is applicable to the normal operation. In the LPI mode, when rx_lpi is asserted, Signal_Detect output shall be asserted within 5 µs under the same quality requirement of the received signal as in normal operation. The new definition of conditional parameter AS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.5.6 Change to 10.1.3 “Signal_Detect timing requirements on deassertion”

The TP-PMD 10.1.3 is applicable to the normal operation. In the LPI mode, when rx_lpi is asserted, Signal_Detect output shall be deasserted within 5 µs under the same quality requirement of the received signal as in normal operation. The new definition of conditional parameter ANS_Max is inserted in TP-PMD Table 4 as depicted in Table 25–3.

25.5.7 Changes to TP-PMD 10.2 “Transmitter”

For the optional EEE capability, when tx_quiet (as communicated by the PMD_TXQUIET.request primitive) is set to FALSE, the transmitter output shall deliver a signal that exceeds Signal_Detect assertion threshold within 2 µs. The scrambler shall continue to operate for the first 5 µs following tx_quiet = TRUE. Transmit functions may be deactivated after this period. The transmitter shall deliver a fully compliant signal when tx_quiet is set to FALSE less than 5 µs after being set to TRUE. If tx_quiet is set to FALSE more than 5 µs after being set to TRUE, then the transmitter shall deliver a fully compliant signal within 5 µs (see 25.4.8).

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25.5.8 Replace TP-PMD Table 4 “Signal_Detect summary” with Table 25–3

The requirement of signal detection time and threshold are different between the normal operation mode and the LPI mode. In order to share one Signal_Detect, the timing and threshold characteristics may be qualified by LPI signal rx_lpi as communicated by the PMA_RXLPI.request primitive.

Table 25–3—Signal_Detect summary

Characteristic	Minimum	Maximum	Units
Assert time Normal operation mode		1000	µs
Deassert time Normal operation mode		350	µs
Assert time LPI mode		5	µs
Deassert time LPI mode		5	µs
Assert threshold VSDA 100 Ω balanced cable Normal operation mode		1000	mV peak to peak
Deassert threshold VSDD 100 Ω balanced cable Normal operation mode	200		mV peak to peak
Assert threshold VSDA 150 Ω balanced shielded cable Normal operation mode		1225	mV peak to peak
Deassert threshold VSDD 150 Ω balanced shielded cable Normal operation mode	245		mV peak to peak
Assert threshold VSDA LPI mode		400	mV peak to peak
Deassert threshold VSDD LPI mode	200		mV peak to peak

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25.6 Protocol implementation conformance statement (PICS) proforma for Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX[7]

25.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

25.6.2 Identification

25.6.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

25.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2015.)	

Date of Statement	

[7] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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25.6.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*TXU	Supports unshielded twisted pair	25.2	O/1		
TXS	Supports shielded twisted pair	25.2	O/1		
*LPI	Implementation of LPI	25.5	O		

25.6.3.1 DTE Power via MDI major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*PSET2	Type 2 PSE implementation	33.1.4	O	Yes [ ] No [ ]	Optional
*PDT2	Type 2 PD implementation	33.3.2	O	Yes [ ] No [ ]	Optional

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25.6.4 PICS proforma tables for the Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.6.4.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Integrates 100BASE-X PMA and PCS	25.1	M		See Clause 24

25.6.4.2 PMD compliance

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Compliance with 100BASE-X PMD Service Interface	25.1	M		See 24.2.3
PD2	Compliance with ANSI X3.263-1995, 7, 8 (excluding 8.3), 9, 10, 11 and normative annex A, with listed exceptions	25.4 25.4.8	M		
PD3	Precedence over ANSI X3.263-1995	25.4	M		
PD4	MDI contact assignments for twisted pair	25.4.4 25.4.3	TXU: M		
PD5	Compliance with crossover function of 14.5.2 with listed adaptations	25.4.11	M		
PD6	Minimum jitter test pattern length	25.4.12	M		3000 code-groups
PD7	Isolation requirements	25.4.6	M		

25.6.4.3 Characteristics of link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	Implementations of balanced cabling link	25.4.9	M		Compatible at the MDI.
LKS2	100BASE-T links	25.4.9.1	M		Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995 (Class D).

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Item	Feature	Subclause	Status	Support	Value/Comment
LKS3	Insertion loss	25.4.9.2.1	M		As specified in 25.4.9.2.1 at all frequencies from 1 MHz to 100 MHz when link segment is terminated in 100 Ω.
LKS4	Return loss	25.4.9.2.3	M		As specified in 25.4.9.2.3 at all frequencies from 1 MHz to 100 MHz when link segment is terminated in 100 Ω.
LKS5	Differential Near-End Crosstalk (NEXT)	25.4.9.2.4	M		As specified in 25.4.9.2.4 at all frequencies from 1 MHz to 100 MHz.

25.6.4.4 DTE Power via MDI compliance

Item	Feature	Subclause	Status	Support	Value/Comment
DTEP1	Type 2 PD receiver worst-case droop transformer	25.4.5	PDT2:M	Yes [ ] No [ ]	Meet requirements of 25.4.7: differential voltage signals translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion
DTEP2	Type 2 Endpoint PSE receiver worst-case droop transformer	25.4.5	PSET2:M	Yes [ ] No [ ]	Meet requirements of 25.4.7: differential voltage signals translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion
DTEP3	Type 2 PD transmitter worst-case droop transformer while accepting more than 13 W average power	25.4.5	PDT2:M	Yes [ ] No [ ]	Meet OCL requirements of 9.1.7 or requirements in 25.4.5.1
DTEP4	Type 2 Endpoint PSE transmitter worst-case droop transformer while delivering more than 13 W average power	25.4.5	PSET2:M	Yes [ ] No [ ]	Meet OCL requirements in 9.1.7 or requirements in 25.4.5.1
DTEP5	Equivalent system time constant	25.4.5.1	M	Yes [ ] N/A [ ]	Greater than 2.4 μs when calculated using measurement points A and C in Figure 25–2

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25.6.4.5 LPI functions

Item	Feature	Subclause	Status	Support	Value/Comment
LP1	Jitter measurement in the LPI mode	25.4.8	LPI:M	Yes [ ]	1.4 ns peak to peak
LP2	Code-groups used to measure jitter in the LPI mode	25.4.8	LPI:M	Yes [ ]	Scrambled SLEEP code-groups
LP3	Jitter measurement time interval in the LPI mode	25.4.8	LPI:M	Yes [ ]	No less than 100 ms and no greater than 1 s.
LP4	Encoder function in the LPI mode	25.5.1	LPI:M	Yes [ ]	Comply with the state diagram shown in Figure 25–3.
LP5	Decoder function in the LPI mode	25.5.2	LPI:M	Yes [ ]	Comply with the state diagram shown in Figure 25–4.
LP6	Signal_Detect assertion threshold in the LPI mode	25.5.3	LPI:M	Yes [ ]	Minimum 400 mV peak to peak
LP7	Signal_Detect deassertion threshold in the LPI mode	25.5.4	LPI:M	Yes [ ]	Maximum 200 mV peak to peak
LP8	Signal_Detect assertion time in the LPI mode	25.5.5	LPI:M	Yes [ ]	Maximum 5 µs
LP9	Signal_Detect deassertion time in the LPI mode	25.5.6	LPI:M	Yes [ ]	Maximum 5 µs
LP10	Scrambler and transmit functions deactivation time	25.5.7	LPI:M	Yes [ ]	The scrambler and transmit functions continue to operate for the first 5 µs following tx_quiet = TRUE.
LP11	Transmitter output amplitude initial ramp up time	25.5.7	LPI:M	Yes [ ]	The transmitter output delivers a signal that exceeds Signal_Detect assertion threshold within 2 µs when tx_quiet is set to TRUE.
LP12	Transmitter output recovery time after a short Quiet state	25.5.7	LPI:M	Yes [ ]	The transmitter delivers a fully compliant signal promptly if tx_quiet is set to FALSE less than 5 µs after being set to TRUE.
LP13	Transmitter output recovery time after a long Quiet state	25.5.7	LPI:M	Yes [ ]	The transmitter delivers a fully compliant signal within 5 µs if tx_quiet is set to FALSE more than 5 µs after being set to TRUE.

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26. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX

26.1 Overview

This clause specifies the 100BASE-X PMD (including MDI) and fiber optic medium for multimode fiber, 100BASE-FX. In order to form a complete 100BASE-FX Physical Layer it shall be integrated with the 100BASE-X PCS and PMA of Clause 24, which are assumed incorporated by reference. As such, the 100BASE-FX PMD shall comply with the PMD service interface specified in 24.4.1.

26.2 Functional specifications

The 100BASE-FX PMD (and MDI) is specified by incorporating the FDDI PMD standard, ISO/IEC 9314-3:1990, by reference, with the modifications noted below. This standard provides support for two optical fibers. For improved legibility in this clause, ISO/IEC 9314-3:1990 will henceforth be referred to as fiber-PMD.

26.3 General exceptions

The 100BASE-FX PMD is precisely the PMD specified as fiber-PMD, with the following general modifications:

a) The scope and general description discussed in fiber-PMD 1 and 5 relate to the use of those standards with an FDDI PHY, ISO/IEC 9314-1:1989, and MAC, ISO/IEC 9314-2:1989. These clauses are not relevant to the use of the PMD with 100BASE-X.
b) The normative references, definitions, and conventions of fiber-PMD 2, 3, and 4 are used only as necessary to interpret the applicable sections of fiber-PMD referenced in this clause.
c) The PMD Service Specifications of fiber-PMD 6 are replaced by those specified in 24.4.1. The 100BASE-FX PMD Service specification is a proper subset of the PMD service specification in fiber-PMD.
d) There are minor terminology differences between this standard and fiber-PMD that do not cause ambiguity. The terminology used in 100BASE-X was chosen to be consistent with other IEEE 802 standards, rather than with FDDI. Terminology is both defined and consistent within each standard. Special note should be made of the interpretations shown in Table 26–1.

Table 26–1—Interpretation of general FDDI terms and concepts

FDDI term or concept	Interpretation for 100BASE-X
bypass	<unused>
Connection Management (CMT)	<no comparable entity>
frame	stream
Halt Line State (HLS)	<unused>
hybrid mode	<no comparable entity>
MAC (or MAC-2)	MAC
Master Line State (MLS)	<unused>
maximum frame size = 9000 symbols	maximum stream size = 4018 code-groups

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Table 26–1—Interpretation of general FDDI terms and concepts *(continued)*

FDDI term or concept	Interpretation for 100BASE-X
PHY (or PHY-2)	PMA; i.e., PMD client
PHY Service Data Unit (SDU)	stream
PM_SIGNAL.indication (Signal_Detect)	PMD_SIGNAL.indication (signal_status)
PM_UNITDATA.indication (PM_Indication)	PMD_UNITDATA.indication (nrzi-bit)
PM_UNITDATA.request (PM_Request)	PMD_UNITDATA.request (nrzi-bit)
preamble	inter-packet IDLEs
Quiet Line State (QLS)	<unused>
SM_PM_BYPASS.request (Control_Action)	Assume: SM_PM_BYPASS.request (Control_Action = Insert)
SM_PM_CONTROL.request (Control_Action)	Assume: SM_PM_CONTROL.request (Control_Action = Transmit_Enable)
SM_PM_SIGNAL.indication (Signal_Detect)	<unused>
Station Management (SMT)	<no comparable entity>
symbol	code-group

26.4 Specific requirements and exceptions

The 100BASE-FX PMD (including MDI) and baseband medium shall conform to the requirements of fiber-PMD Clauses 8, 9, and 10. In the referenced standard, fiber-PMD, informative Annex A through Annex G provide additional information useful to PMD sublayer implementers. Where there is conflict between specifications in fiber-PMD and those in this standard, those of this standard shall prevail.

26.4.1 Medium Dependent Interface (MDI)

The 100BASE-FX medium dependent interface (MDI) shall conform to one of the following connectors. The recommended alternative is the duplex SC connector.

a) The duplex SC connector as specified in IEC 61754-4 [B25] and IEC 61754-4, Interface 4-2. (See 38.11.3).
b) Media Interface Connector (MIC) as specified in fiber-PMD 7 and Annex F. When the MIC is used, the receptacle shall be keyed as “M”.
c) Optical Medium Connector Plug and Socket (commonly called ST[8] connector) as specified in 15.3.2.

26.4.2 Crossover function

A crossover function shall be implemented in every cable-pair link. The crossover function connects the transmitter of one PHY to the receiver of the PHY at the other end of the cable-pair link. For 100BASE-FX, the crossover function is realized in the cable plant.

[8]ST is a registered trademark of Lucent Technologies.

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26.5 Protocol implementation conformance statement (PICS) proforma for Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX[9]

26.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

26.5.2 Identification

26.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

26.5.3 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 26, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	

Date of Statement	

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26.5.4 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
FSC	Supports duplex SC connector	26.4.1	O/1		Recommended. See IEC 61754-4 [B25] and IEC 61754-4, Interface 4-2. (See 38.11.3).
*FMC	Supports Media Interface Connector (MIC)	26.4.1	O/1		See ISO/IEC 9314-3:1990, 7 and Annex F
FST	Supports Optical Medium Connector Plug and Socket (ST)	26.4.1	O/1		See 15.3.2

26.5.5 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-FX

26.5.5.1 General compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
GN1	Integrates 100BASE-X PMA and PCS	26.1	M		See Clause 24

26.5.5.2 PMD compliance

Item	Feature	Subclause	Status	Support	Value/Comment
PD1	Compliance with 100BASE-X PMD Service Interface	26.1	M		See 24.4.1
PD2	Compliance with ISO/IEC 9314-3:1990 8, 9, and 10	26.4	M		
PD3	Precedence over ISO/IEC 9314-3:1990	26.4	M		
PD4	MIC receptacle keying	26.4.1	FMC: M		“M”
PD5	Crossover function in cable	26.4.2	M		

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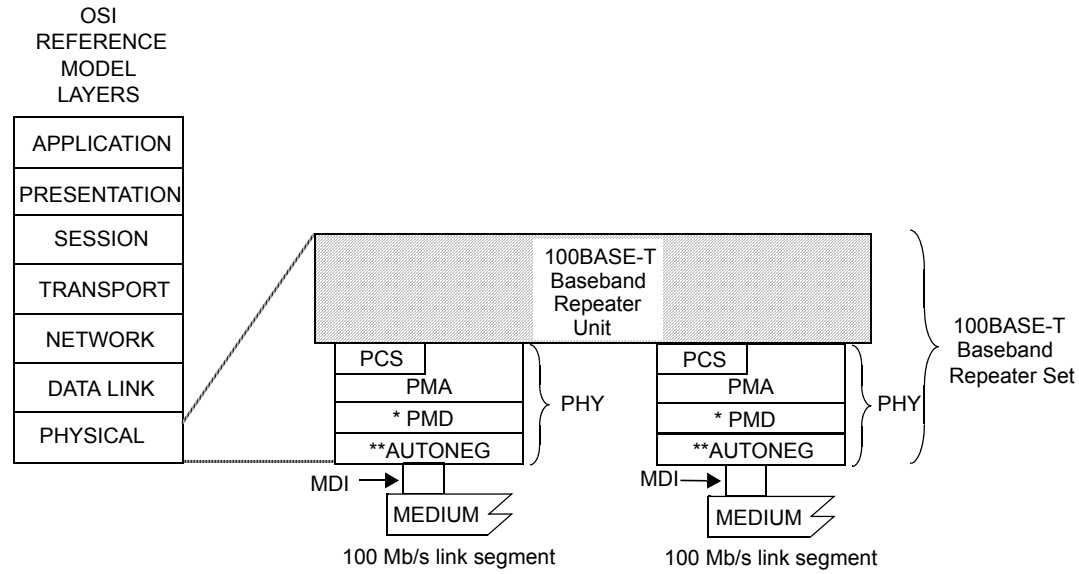
27. Repeater for 100 Mb/s baseband networks

NOTE—This repeater is not recommended for new installations. Since September 2011, maintenance changes are no longer being considered for this clause.

27.1 Overview

27.1.1 Scope

Clause 27 defines the functional and electrical characteristics of a repeater for use with 100BASE-T 100 Mb/s baseband networks. A repeater for any other IEEE 802.3 network type is beyond the scope of this clause. The relationship of this standard to the OSI Reference Model is shown in Figure 27–1. The purpose of the repeater is to provide a simple, inexpensive, and flexible means of coupling two or more segments.



MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* PMD is specified for 100BASE-TX and -FX only; 100BASE-T4 does not use this layer.
Use of MII between PCS and baseband repeater unit is optional.
** AUTONEG is optional.

Figure 27–1—100BASE-T repeater set relationship to the ISO/IEC OSI reference model

27.1.1.1 Repeater set

Repeater sets are an integral part of all 100 Mb/s baseband networks with more than two DTEs and are used to extend the physical system topology by providing a means of coupling two or more segments. Multiple repeater sets are permitted within a single collision domain to provide the maximum connection path length. Segments may be connected directly by a repeater or a pair of repeaters that are, in turn, connected by a inter-repeater link (IRL). Allowable topologies shall contain only one operative signal path between any two

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points on the network. A repeater set is not a station and does not count toward the overall limit of 1024 stations on a network.

A repeater set can receive, and if necessary decode, data from any segment under worst-case noise, timing, and signal amplitude conditions. It retransmits the data to all other segments attached to it with timing, amplitude, and, if necessary, coding restored. The retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. A repeater set also provides a degree of protection to a network by isolating a faulty segment's carrier activity from propagating through the network.

27.1.1.2 Repeater unit

A repeater unit is a subset of a repeater set containing all the repeater-specific components and functions, exclusive of PHY components and functions. A repeater unit connects to the PMA and, if necessary, the PCS sublayers of its PHYs.

27.1.1.3 Repeater classes

Two classes of repeater sets are defined—Class I and Class II.

Class I:

A type of repeater set specified such that in a maximum length segment topology, only one such repeater set may exist between any two DTEs within a single collision domain.

Class II:

A type of repeater set specified such that in a maximum length segment topology, only two such repeater sets may exist between any two DTEs within a single collision domain.

More complex topologies are possible in systems that do not use worst-case cable. See Clause 29 for requirements.

27.1.2 Application perspective

This subclause states the broad objectives and assumptions underlying the specification defined through Clause 27.

27.1.2.1 Objectives

a) Provide physical means for coupling two or more LAN segments at the Physical Layer.
b) Support interoperability of independently developed physical, electrical, and optical interfaces.
c) Provide a communication channel with a mean bit error ratio, at the physical service interface equivalent to that for the attached PHY.
d) Provide for ease of installation and service.
e) Ensure that fairness of DTE access is not compromised.
f) Provide for low-cost networks, as related to both equipment and cabling.
g) Make use of building wiring appropriate for the supported PHYs and telephony wiring practices.

27.1.2.2 Compatibility considerations

All implementations of the repeater set shall be compatible at the MDI. The repeater set is defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the repeater set in an application-dependent manner provided the appropriate PHY specifications are met.

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27.1.2.2.1 Internal segment compatibility

Implementations of the repeater set that contain a MAC layer for network management or other purposes, irrespective of whether they are connected through an exposed repeater port or are internally ported, shall conform to the requirements of Clause 30 on that port if repeater management is implemented.

27.1.3 Relationship to PHY

A close relationship exists between Clause 27 and the PHY clauses, Clause 23 for the 100BASE-T4 PHY and Clause 24 to Clause 26 for the 100BASE-X PHYs, and Clause 32 for the 100BASE-T2 PHY. The PHY's PMA, PCS, and MDI specifications provide the actual medium attachment, including drivers, receivers, and Medium Interface Connectors for the various supported media. The repeater clause does not define a new PHY; it utilizes the existing PHYs complete and without modification.

27.2 PMA interface messages

The messages between the repeater unit and the PMA in the PHY utilizes the PMA service interface defined in 23.3, 24.3, and 32.4.2. The PMA service interface primitives are summarized below:

PMA_TYPE.indication
PMA_UNITDATA.request
PMA_UNITDATA.indication
PMA_CARRIER.indication
PMA_LINK.indication
PMA_RXERROR.indication

27.3 Repeater functional specifications

A repeater set provides the means whereby data from any segment can be received under worst case noise, timing, and amplitude conditions and then retransmitted with timing and amplitude restored to all other attached segments. Retransmission of data occurs simultaneously with reception. If a collision occurs, the repeater set propagates the collision event throughout the network by transmitting a Jam signal. If an error is received by the repeater set, no attempt is made to correct it and it is propagated throughout the network by transmitting an invalid signal.

The repeater set provides the following functional capability to handle data flow between ports:

a) *Signal restoration.* Provides the ability to restore the timing and amplitude of the received signal prior to retransmission.
b) *Transmit function.* Provides the ability to output signals on the appropriate port and encoded appropriately for that port. Details of signal processing are described in the specifications for the PHYs.
c) *Receive function.* Provides the ability to receive input signals presented to the ports. Details of signal processing are described in the specifications for the PHYs.
d) *Data Handling function.* Provides the ability to transfer code-elements between ports in the absence of a collision.
e) *Received Event Handling requirement.* Provides the ability to derive a carrier signal from the input signals presented to the ports.
f) *Collision Handling function.* Provides the ability to detect the simultaneous reception of frames at two or more ports and then to propagate a Jam message to all connected ports.
g) *Error Handling function.* Provides the ability to prevent substandard links from generating streams of false carrier and interfering with other links.
h) *Partition function.* Provides the ability to prevent a malfunctioning port from generating an excessive number of consecutive collisions and indefinitely disrupting data transmission on the network.

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i) *Receive Jabber function.* Provides the ability to interrupt the reception of abnormally long streams of input data.

27.3.1 Repeater functions

The repeater set shall provide the Signal Restoration, Transmit, Receive, Data Handling, Received Event Handling, Collision Handling, Error Handling, Partition, and Receive Jabber functions. The repeater is transparent to all network acquisition activity and to all DTEs. The repeater will not alter the basic fairness criterion for all DTEs to access the network or weigh it toward any DTE or group of DTEs regardless of network location.

The Transmit and Receive functional requirements are specified by the PHY clauses, Clause 23 for 100BASE-T4, Clause 24 to Clause 26 for 100BASE-X, and Clause 32 for 100BASE-T2.

27.3.1.1 Signal restoration functional requirements

27.3.1.1.1 Signal amplification

The repeater set (including its integral PHYs) shall ensure that the amplitude characteristics of the signals at the MDI outputs of the repeater set are within the tolerances of the specification for the appropriate PHY type. Therefore, any loss of signal-to-noise ratio due to cable loss and noise pickup is regained at the output of the repeater set as long as the incoming data is within system specification.

27.3.1.1.2 Signal wave-shape restoration

The repeater set (including its integral PHYs) shall ensure that the wave-shape characteristics of the signals at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any loss of wave-shape due to PHYs and media distortion is restored at the output of the repeater set.

27.3.1.1.3 Signal retiming

The repeater set (including its integral PHYs) shall ensure that the timing of the encoded data output at the MDI outputs of a repeater set are within the specified tolerance for the appropriate PHY type. Therefore, any receive jitter from the media is removed at the output of the repeater set.

27.3.1.2 Data handling functional requirements

27.3.1.2.1 Data frame forwarding

The repeater set shall ensure that the data frame received on a single input port is distributed to all other output ports in a manner appropriate for the PHY type of that port. The data frame is that portion of the packet after the SFD and before the end-of-frame delimiter. The only exceptions to this rule are when contention exists among any of the ports, when the receive port is partitioned as defined in 27.3.1.6, when the receive port is in the Jabber state as defined in 27.3.1.7, or when the receive port is in the Link Unstable state as defined in 27.3.1.5.1. Between unpartitioned ports, the rules for collision handling (see 27.3.1.4) take precedence.

27.3.1.2.2 Received code violations

The repeater set shall ensure that any code violations received while forwarding a packet are propagated to all outgoing segments. These code violations shall be forwarded as received or replaced by bad_code (see 23.2.1.2), /H/ (see 24.2.2.1), or (ESC/0, 0/ESC) (see Figure 32–9) code-groups, as appropriate for the outgoing PHY type. Once a received code violation has been replaced by the bad_code, /H/, or (ESC/0, 0/ESC) code-groups, this substitution shall continue for the remainder of the packet regardless of its content. The only exception to this rule is when contention exists among any of the ports, where the rules for collision handling (see 27.3.1.4) then take precedence.

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27.3.1.3 Received event handling functional requirements

27.3.1.3.1 Received event handling

For all its ports, the repeater set shall implement a function (scarrier_present) that represents a received event. Received events include both the Data Frame and any encapsulation of the Data Frame such as Preamble, SFD, and the code-groups /H/, /J/, /K/, bad_code, eop, /T/, /R/, SSD, ESD, etc. A received event is exclusive of the IDLE pattern. Upon detection of scarrier_present from one port, the repeater set repeats all received signals in the Data Frame from that port to the other port (or ports) as described in Figure 27–2.

27.3.1.3.2 Preamble regeneration

The repeater set shall output preamble as appropriate for the outgoing PHY type followed by the SFD.

27.3.1.3.3 Start-of-packet propagation delay

The start-of-packet propagation delay for a repeater set is the time delay between the start of the packet (see 24.6, 23.11.3, and 32.12.1) on its repeated-from (input) port to the start of the packet on its repeated-to (output) port (or ports). This parameter is referred to as the SOP delay. The maximum value of this delay is constrained by Table 27–2.

27.3.1.3.4 Start-of-packet variability

The start-of-packet variability for a repeater set is defined as the total worst-case difference between start-of-packet propagation delays for successive packets separated by 104 bit times (BT) or less at the same input port. The variability shall be less than or equal to those specified in Table 27–1.

Table 27–1—Start-of-packet variability

Input port type	Variability (BT)
100BASE-FX	7.0
100BASE-TX	7.0
100BASE-T4	8.0
100BASE-T2	8.0

27.3.1.4 Collision handling functional requirements

27.3.1.4.1 Collision detection

The repeater performs collision detection by monitoring all its enabled input ports for received events. When the repeater detects received events on more than one input port, it shall enter a collision state and transmit the Jam message to all of its output ports.

27.3.1.4.2 Jam generation

While a collision is occurring between any of its ports, the repeater unit shall transmit the Jam message to all of the PMAs to which it is connected. The Jam message shall be transmitted in accordance with the repeater state diagram in Figure 27–4 and Figure 27–5.

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27.3.1.4.3 Collision-jam propagation delay

The start-of-collision Jam propagation delay for a repeater set is the time delay between the start of the second packet input signals to arrive at its port and the start of Jam (see 24.6, 23.11, and 32.12.1) out on all ports. This parameter is referred to as the SOJ delay. The delay shall be constrained by Table 27–2. Note that a device defined by two columns in Table 27–2 must meet the performance requirements specified in both columns.

Table 27–2—Start-of-packet propagation and start-of-collision jam propagation delays

Class I repeater	Class II repeater with all ports TX/FX	Class II repeater with any port T4	Class II repeater with any port T2
SOP + SOJ ≤ 140 BT	SOP ≤ 46 BT, SOJ ≤ 46 BT	SOP+SOJ ≤ 67 BT	SOP+SOJ ≤ 90 BT

27.3.1.4.4 Cessation-of-collision Jam propagation delay

The cessation-of-collision Jam propagation delay for a repeater set is the time delay between the end of the packet (see 24.6 and 23.11.3) that creates a state such that Jam should end at a port and the end of Jam (see 24.6 and 23.11.3) at that port. The states of the input signals that should cause Jam to end are covered in detail in the repeater state diagrams. This parameter is referred to as the EOJ delay. The delay shall be constrained by Table 27–3.

Table 27–3—Cessation-of-collision Jam propagation delay

Class I repeater	Class II repeater
EOJ ≤ SOP	EOJ ≤ SOP

27.3.1.5 Error handling functional requirements

27.3.1.5.1 100BASE-X and 100BASE-T2 carrier integrity functional requirements

In 100BASE-TX, 100BASE-FX, and 100BASE-T2 systems, it is desirable that the repeater set protect the network from some transient fault conditions that would disrupt network communications. Potential likely causes of such conditions are DTE and repeater power-up and power-down transients, cabling disconnects, and faulty wiring.

Each 100BASE-TX, 100BASE-FX, and 100BASE-T2 repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–9, to prevent a segment's spurious carrier activity from reaching the repeater unit and hence propagating through the network.

The repeater PMA interface shall count consecutive false carrier events. A false carrier event is defined as a carrier event that does not begin with a valid start of stream delimiter (see 24.2.2.1.4 and 32.3.1.2.3). The count shall be incremented on each false carrier event and shall be reset on reception of a valid carrier event. In addition, each PMA interface shall contain a false carrier timer, which is enabled at the beginning of a false carrier event and reset at the conclusion of such an event. A repeater unit shall transmit the JAM message to all of the PMAs to which it is connected for the duration of the false carrier event or until the duration of the event exceeds the time specified by the false_carrier_timer (see 27.3.2.1.4), whichever is shorter. The JAM message shall be transmitted in accordance with the Repeater state diagram in Figure 27–4 and Figure 27–5. The LINK UNSTABLE condition shall be detected when the False Carrier Count exceeds

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the value FCCLimit (see 27.3.2.1.1) or the duration of a false carrier event exceeds the time specified by the false_carrier_timer. In addition, the LINK UNSTABLE condition shall be detected upon power-up reset.

Upon detection of LINK UNSTABLE, the port shall perform the following:

a) Inhibit sending further messages to the repeater unit.
b) Inhibit sending further output messages from the repeater unit.
c) Continue to monitor activity on that PMA interface.

The repeater shall exit the LINK UNSTABLE condition when one of the following is met:

a1) The repeater has detected no activity (Idle) for more than the time specified by ipg_timer plus idle_timer (see 27.3.2.1.4) on Port X.
b1) A valid carrier event with a duration greater than the time specified by valid_carrier_timer (see 27.3.2.1.4) has been received, preceded by no activity (Idle) for more than the time specified by ipg_timer (see 27.3.2.1.4) on Port X.

27.3.1.5.2 Speed handling

If the PHY has the capability of detecting speeds other than 100 Mb/s, then the repeater set shall have the capability of blocking the flow of non-100 Mb/s signals. The incorporation of 100 Mb/s and 10 Mb/s repeater functionality within a single repeater set is beyond the scope of this standard.

27.3.1.6 Partition functional requirements

In large multisegment networks it may be desirable that the repeater set protect the network from some fault conditions that would disrupt network communications. A potentially likely cause of this condition could be due to a cable fault.

Each repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–8, to prevent a faulty segment's carrier activity from reaching the repeater unit and hence propagating through the network. The repeater PMA interface shall count collisions. The count shall be incremented on each transmission that suffers a collision. The count shall be reset on a carrier event of duration in excess of no_collision_timer (see 27.3.2.1.4) without incurring a collision. If this count reaches the value CCLimit (see 27.3.2.1.1), the Partition condition shall be detected.

Upon detection of Partition, the port shall perform the following:

a) Inhibit sending further input messages to the repeater unit.
b) Continue to output messages from the repeater unit.
c) Continue to monitor activity on that PMA interface.

The repeater shall reset the Partition function when one of the following conditions is met:

a1) On power-up reset.
b1) The repeater has transmitted on the port for a duration in excess of no_collision_timer (see 27.3.2.1.4) without incurring a collision.

NOTE—It is possible that under some network conditions the partition state diagram will partition a port due to normal network collisions rather than a fault condition. It is also possible that some double fault conditions will remain undetected. To reduce the likelihood of these events occurring, the following optional measures, as described in Figure 27–8, are recommended:

a2) The collision count is additionally reset when the repeater has transmitted on the port for a duration in excess of no_collision_timer without detecting a collision.

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b2) The Partition function is additionally reset when the repeater has received activity on the port for a duration in excess of no_collision_timer without detecting a collision.
c2) The Partition condition is additionally detected due to a carrier event of duration in excess of jabber_timer (see 27.3.1.7) in which a collision has occurred.

27.3.1.7 Receive jabber functional requirements

Each repeater PMA interface shall contain a self-interrupt capability, as described in Figure 27–7, to prevent an illegally long reception of data from reaching the repeater unit. The repeater PMA interface shall provide a window of duration jabber_timer bit times (see 27.3.2.1.4) during which the input messages may be passed on to other repeater unit functions. If a reception exceeds this duration, the jabber condition shall be detected.

Upon detection of jabber, the port shall perform the following:

a) Inhibit sending further input messages to the repeater unit.
b) Inhibit sending further output messages from the repeater unit.

The repeater PMA interface shall reset the Jabber function and re-enable data transmission and reception when either one of the following conditions is met:

a1) On power-up reset.
b1) When carrier is no longer detected.

27.3.2 Detailed repeater functions and state diagrams

A precise algorithmic definition is given in this subclause, providing a complete procedural model for the operation of a repeater, in the form of state diagrams. Note that whenever there is any apparent ambiguity concerning the definition of repeater operation, the state diagrams should be consulted for the definitive statement.

The model presented in this subclause is intended as a primary specification of the functions to be provided by any repeater unit. It is important to distinguish, however, between the model and a real implementation. The model is optimized for simplicity and clarity of presentation, while any realistic implementation should place heavier emphasis on such constraints as efficiency and suitability to a particular implementation technology.

It is the functional behavior of any repeater unit implementation that shall match the standard, not the internal structure. The internal details of the procedural model are useful only to the extent that they help specify the external behavior clearly and precisely. For example, the model uses a separate Receive Port Jabber state diagram for each port. However, in actual implementation, the hardware may be shared.

The notation used in the state diagram follows the conventions of 1.2.1. Note that transitions shown without source states are evaluated at the completion of every state and take precedence over other transition conditions.

27.3.2.1 State diagram variables

27.3.2.1.1 Constants

CCLimit

The number of consecutive collisions that must occur before a segment is partitioned.

Values: Positive integer greater than 60.

FCCLimit

The number of consecutive False Carrier events that must occur before a segment is isolated.

Value: 2.

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27.3.2.1.2 Variables

activity(Port designation)

Indicates port activity status. The repeater core effects a summation of this variable received from all its attached ports and responds accordingly.

Values: 0; no frame or packet activity at any port.
1; exactly 1 port of the repeater set has frame or packet activity input.
>1; more than 1 port of the repeater set has frame or packet activity input. Alternately, one or more ports has detected a carrier that is not valid.

all_data_sent

Indicates if all received data frame bits or code-groups from the current frame have been sent. During or after collision the all_data_sent variable follows the inverse of the carrier of port N.

Values: true; all received data frame bits or code-groups have been sent.
false; all received data frame bits or code-groups have not been sent.

begin

The Interprocess flag controlling state diagram initialization values.

Values: true
false

carrier_status(X)

Signal received from PMA; indicates the status of sourced Carrier input at Port X.

Values: ON; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is ON.
OFF; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is OFF.

data_ready

Indicates if the repeater has detected and/or decoded the MAC SFD and is ready to send the received data.

Values: true; the MAC SFD has been detected and/or decoded.
false; the MAC SFD has not been detected nor decoded.

force_jam(X)

Flag from Carrier Integrity state diagram for Port X, which determines whether all ports should transmit Jam.

Values: true; the Carrier Integrity Monitor has determined that it requires all ports be forced to transmit Jam.
false; the Carrier Integrity Monitor has determined that it does not require all ports be forced to transmit Jam.

Default: for T4 ports: false

isolate(X)

Flag from Carrier Integrity state diagram for Port X, which determines whether a port should be enabled or disabled.

Values: true; the Carrier Integrity Monitor has determined the port should be disabled.
false; the Carrier Integrity Monitor has determined the port should be enabled.

jabber(X)

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Flag from Receive Timer state diagram for Port X, which indicates that the port has received excessive length activity.

Values: true; port has exceeded the continuous activity limit.
false; port has not exceeded the continuous activity limit.

link_status(X)

Signal received from PMA; indicates link status for Port X (see 23.3.5, 24.3.1.5, and 32.4.1.3.1).

Values: OK; the link_status parameter of the PMA_LINK.indication primitive for Port X is OK.
READY; the link_status parameter of the PMA_LINK.indication primitive for Port X is READY (for 100BASE-TX and 100BASE-T4).
FAIL; the link_status parameter of the PMA_LINK.indication primitive for Port X is FAIL.

opt(X)

Implementation option. Either value may be chosen for repeater implementation.

Values: true; port will emit the JamT4 pattern in response to collision conditions.
false; port will append Jam pattern after preamble and SFD in response to collision conditions.

OUT(X)

Type of output repeater is sourcing at Port X.

Values: Idle; repeater is transmitting an IDLE pattern as described by 23.4.1.2, 24.2.2.1.2, or 32.3.1.2.3.
In(N); repeater is transmitting rx_code_bit(s) as received from Port (N) except /J/K/ (see 24.3.4.2), or recoded rx_symbol_vector as received from Port (N) except SSD (see 32.3.5.2).
Pream; repeater is sourcing preamble pattern as defined by the PMA or PCS of the port type (see 23.2.1.2, 24.2.2.2, 32.3.1.2, Figure 23–6 and Figure 24–9.)
Data; repeater is transmitting data frame on Port X. This data represents the original MAC source data field, properly encoded for the PHY type (see 23.2.1.2, 24.2.2.2, and 32.3.1.2.3).
Jam; repeater is sourcing well formed arbitrary data encodings, excluding SFD, to the port PMA.
JamX; repeater is sourcing a pattern representing 010101... repetitively on Port X.
JamT4; repeater is sourcing the pattern +-+-... repetitively on Port X.

JamT2; repeater is sending a pattern representing 010101... repetitively on Port X.
SFD; repeater is sourcing the Start Frame Delimiter on Port X encoded as defined by the appropriate PHY (see 23.2.3, Figure 24–9, and 32.3.1.2).
/J/K/; repeater is sourcing the code-groups /J/K/ as defined by the PMA on Port X (see 24.2.2.1.4).
/T/R/; repeater is sourcing the code-groups /T/R/ as defined by the PMA on Port X (see 24.2.2.1.5).

SSD; repeater is sourcing the code-groups SSD as defined by the PMA on Port X (see 32.4.2.5).

ESD; repeater is sourcing the code-groups ESD as defined by the PMA on Port X (see 32.3.1.2.3).
DF; repeater is sourcing the Data Frame of the packet on Port X. These are code elements originating on Port N exclusive of EOP1-5, SOSA and SOSB (see 23.2.3 and 23.2.4).
EOP; repeater is sourcing end of packet delimiter (EOP1-5) as defined by the appropriate PMA on Port X (see 23.2.1.2 and 23.2.4.1).

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bad_code; repeater is sourcing bad_code as defined by the PMA of the transmit port (see 23.2.4.1).
tx_err; repeater is sourcing a transmit error code element, either bad_code (see 23.2.4.1) or the code-group /H/ (see 24.2.2.1), or (ESC/0, 0/ESC) (see Figure 32–12) as appropriate to the outgoing PHY type.

partition(X)

Flag from Partition state diagram for Port X, which determines whether a port receive path should be enabled or disabled.

Values: true; port has exceeded the consecutive collision limit.
false; port has not exceeded the consecutive collision limit.

part_opt(X)

Implementation option. Either value may be chosen for repeater implementation (see 27.3.1.6).

Values: true; port supports the recommended optional measures in the partition state diagram.
false; port does not support the recommended optional measures in the partition state diagram.

rxerror_status(X)

Signal received from PMA; indicates if Port X has detected an error condition from the PMA (see 23.3.7.1, Figure 24–14, and Figure 32–14).The repeater need not propagate this error condition during collision events.

Values: ERROR; the rxerror_status parameter of the PMA_RXERROR.indication primitive for Port X is ERROR.
NO_ERROR; the rxerror_status parameter of the PMA_RXERROR.indication primitive for Port X is NO_ERROR.

RX_ER(X)

Signal received from PCS; indicates if Port X has detected an error condition from the PCS (see 23.2.1.4, 24.2.3.2, 32.3.4.1, Figure 23–10, Figure 24–15, and Figure 32–13). The repeater need not propagate this error condition during collision events.

Values: true; the PCS RX_ER signal for Port X is asserted.
false; the PCS RX_ER signal for Port X is negated.

scarrier_present(X)

Signal received from PMA; indicates the status of sourced Carrier input at Port X.

Values: true; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is ON.
false; the carrier_status parameter of the PMA_CARRIER.indication primitive for Port X is OFF.

source_type(X)

Signal received from PMA; indicates PMA type for Port X. The first port to assert activity maintains the source type status for all transmitting port(s) until activity is deasserted. Repeaters may optionally force nonequality on comparisons using this variable. It must then follow the behavior of the state diagrams accordingly and meet all the delay parameters as applicable for the real implemented port type(s).

Values: FXTX; the pma_type parameter of the PMA_TYPE.indication primitive for Port X is X.
T4; the pma_type parameter of the PMA_TYPE.indication primitive for Port X is T4.
T2; the pma_type parameter of the PMA_TYPE.indication primitive for Port X is T2.

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27.3.2.1.3 Functions

command(X)

A function that passes an inter-process flag to all ports specified by X.

Values: copy; indicates that the repeater core has summed the activity levels of its active ports and is in the ACTIVE state.
collision; indicates that the repeater core has summed the activity levels of its active ports and is in the JAM state.
quiet; indicates that the repeater core has summed the activity levels of its active ports and is in the IDLE state.

port(Test)

A function that returns the designation of a port passing the test condition. For example, port(activity = scarrier_present) returns the designation: X for a port for which scarrier_present = true. If multiple ports meet the test condition, the Port function will be assigned one and only one of the acceptable values.

27.3.2.1.4 Timers

All timers operate in the same fashion. A timer is reset and starts timing upon entering a state where "start x_timer" is asserted. At time "x" after the timer has been started, "x_timer_done" is asserted and remains asserted until the timer is reset. At all other times, "x_timer_not_done" is asserted.

When entering a state where "start x_timer" is asserted, the timer is reset and restarted even if the entered state is the same as the exited state.

The timers used in the repeater state diagrams are defined as follows:

false_carrier_timer

Timer for length of false carrier (27.3.1.5.1) that must be present before the ISOLATION state is entered. The timer is done when it reaches 450 – 500 BT.

idle_timer

Timer for length of time without carrier activity that must be present before the ISOLATION state is exited (27.3.1.5.1). The timer is done when it reaches 33 000 BT ± 25% BT.

ipg_timer

Timer for length of time without carrier activity that must be present before carrier integrity tests (27.3.1.5.1) are re-enabled. The timer is done when it reaches 64 – 86 BT.

jabber_timer

Timer for length of carrier that must be present before the Jabber state (27.3.1.7), and optionally during a collision the Partition state (27.3.1.6), is entered. The timer is done when it reaches 40 000 – 75 000 BT.

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no_collision_timer

Timer for length of packet without collision before the Partition state is exited (27.3.1.6). The timer is done when it reaches 450 – 560 BT.

valid_carrier_timer

Timer for length of valid carrier that must be present before the Isolation state is exited (27.3.1.5.1). The timer is done when it reaches 450 – 500 BT.

27.3.2.1.5 Counters

CC(X)

Consecutive port collision count for Port X. Partitioning occurs on a terminal count of CCLimit being reached.

Values: Non-negative integers up to a terminal count of CCLimit.

FCC(X)

False Carrier Counter for Port X. Isolation occurs on a terminal count of FCCLimit being reached.

Values: Non-negative integers up to a terminal count of FCCLimit.

27.3.2.1.6 Port designation

Ports are referred to by number. Port information is obtained by replacing the X in the desired function with the number of the port of interest. Ports are referred to in general as follows:

X

Generic port designator. When X is used in a state diagram, its value is local to that diagram and not global to the set of state diagrams.

N

Is defined by the Port function on exiting the IDLE or JAM states of Figure 27–2. It indicates a port that caused the exit from these states.

ALL

Indicates all repeater ports are to be considered. All ports shall meet test conditions in order for the test to pass.

ALLXN

Indicates all ports except N should be considered. All ports considered shall meet the test conditions in order for the test to pass.

ANY

Indicates all ports are to be considered. One or more ports shall meet the test conditions in order for the test to pass.

ANYXN

Indicates any port other than N meeting the test conditions shall cause the test to pass.

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27.3.2.2 State diagrams

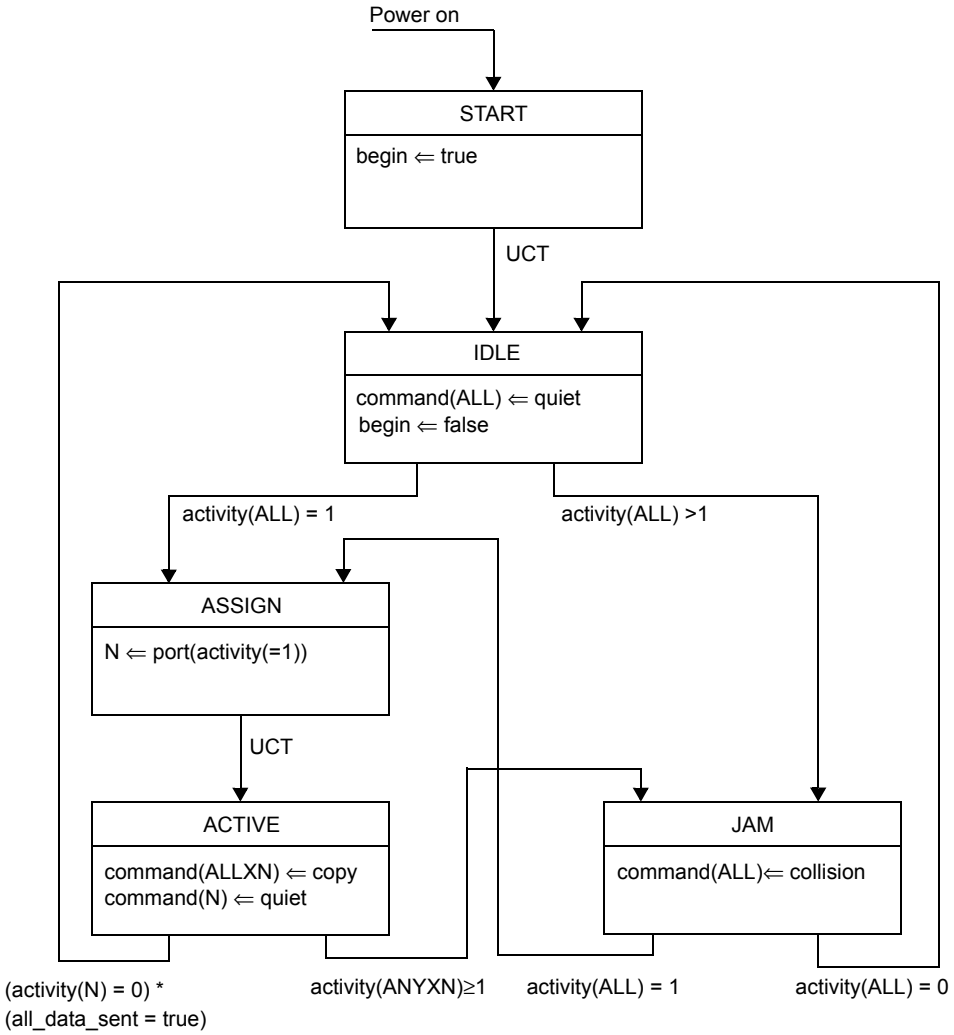


Figure 27–2—Repeater Core state diagram

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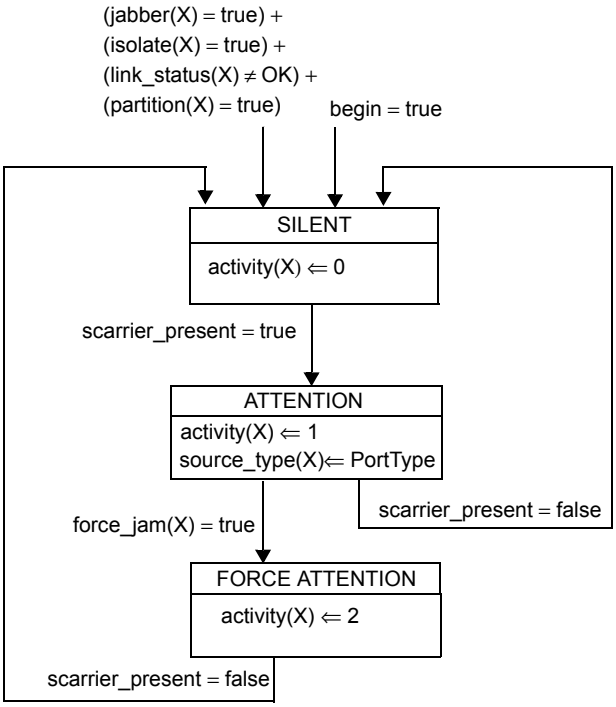


Figure 27–3—Receive state diagram for Port X

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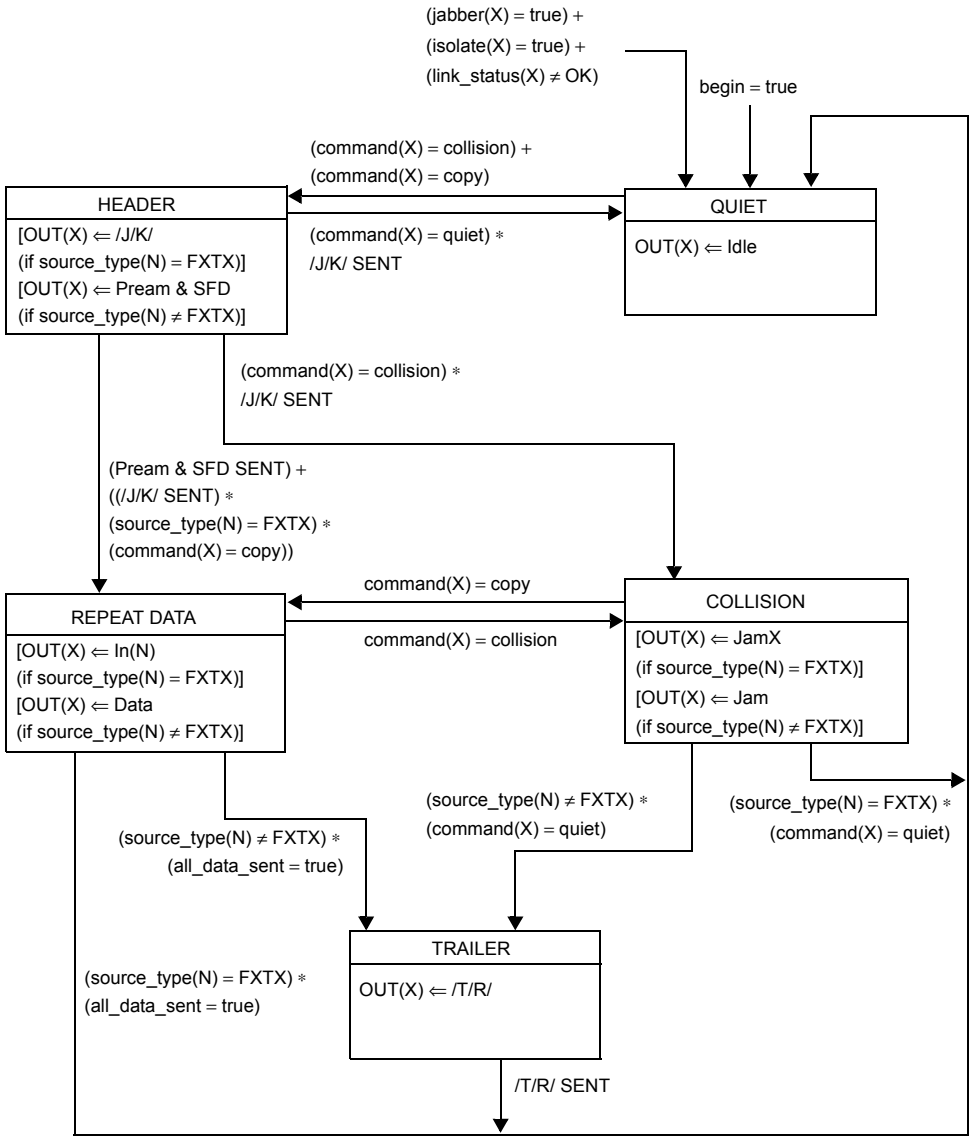


Figure 27–4—100BASE-TX and 100BASE-FX Transmit state diagram for Port X

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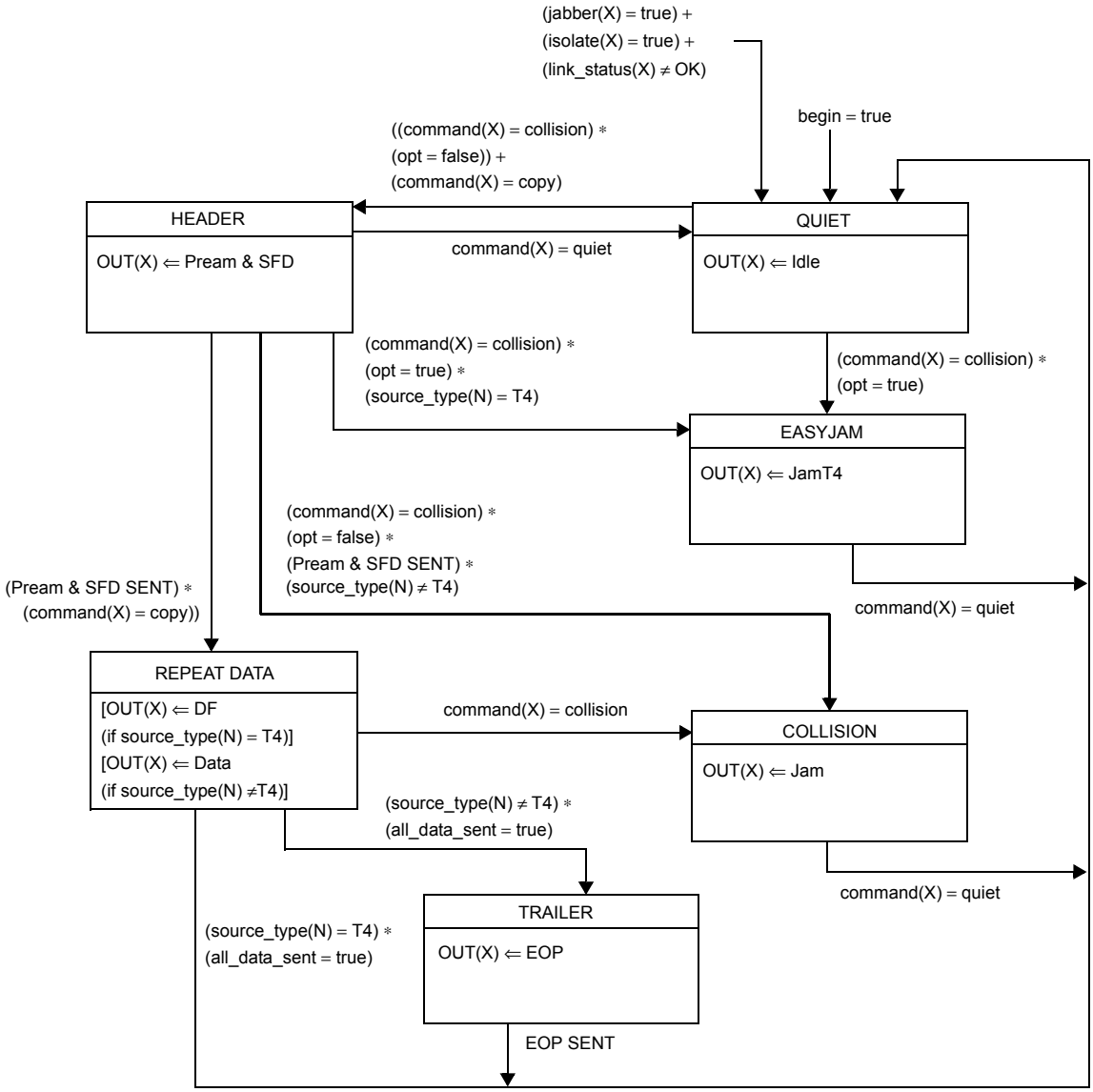


Figure 27–5—100BASE-T4 Transmit state diagram for Port X

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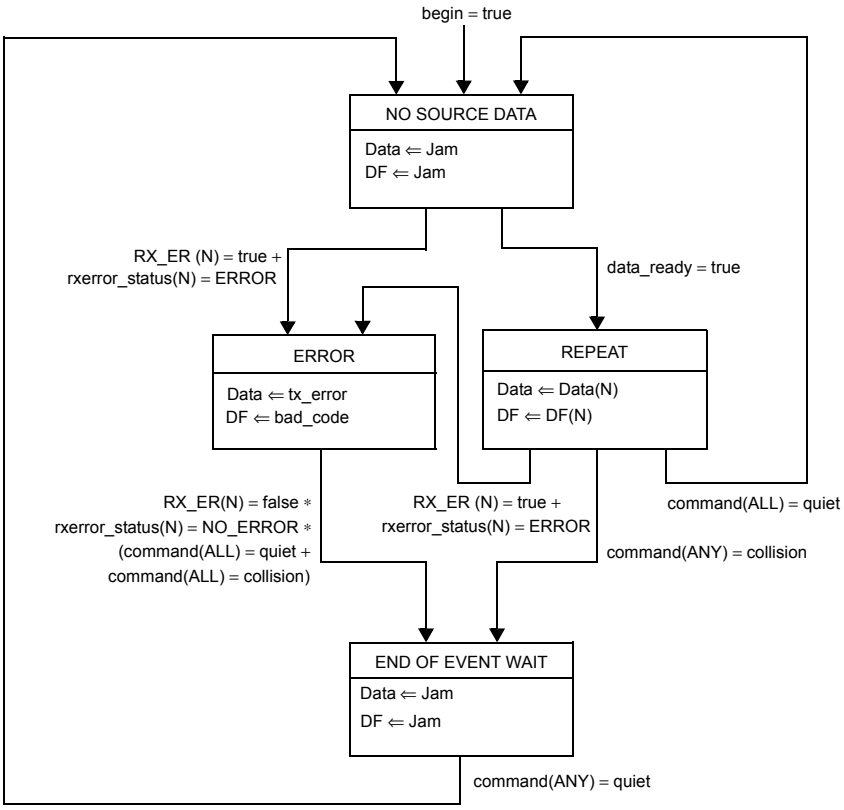


Figure 27–6—Repeater Data Handler state diagram

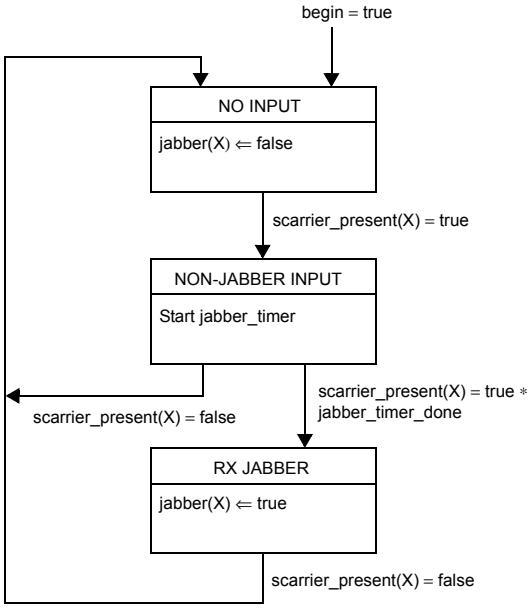


Figure 27–7—Receive Timer state diagram for Port X

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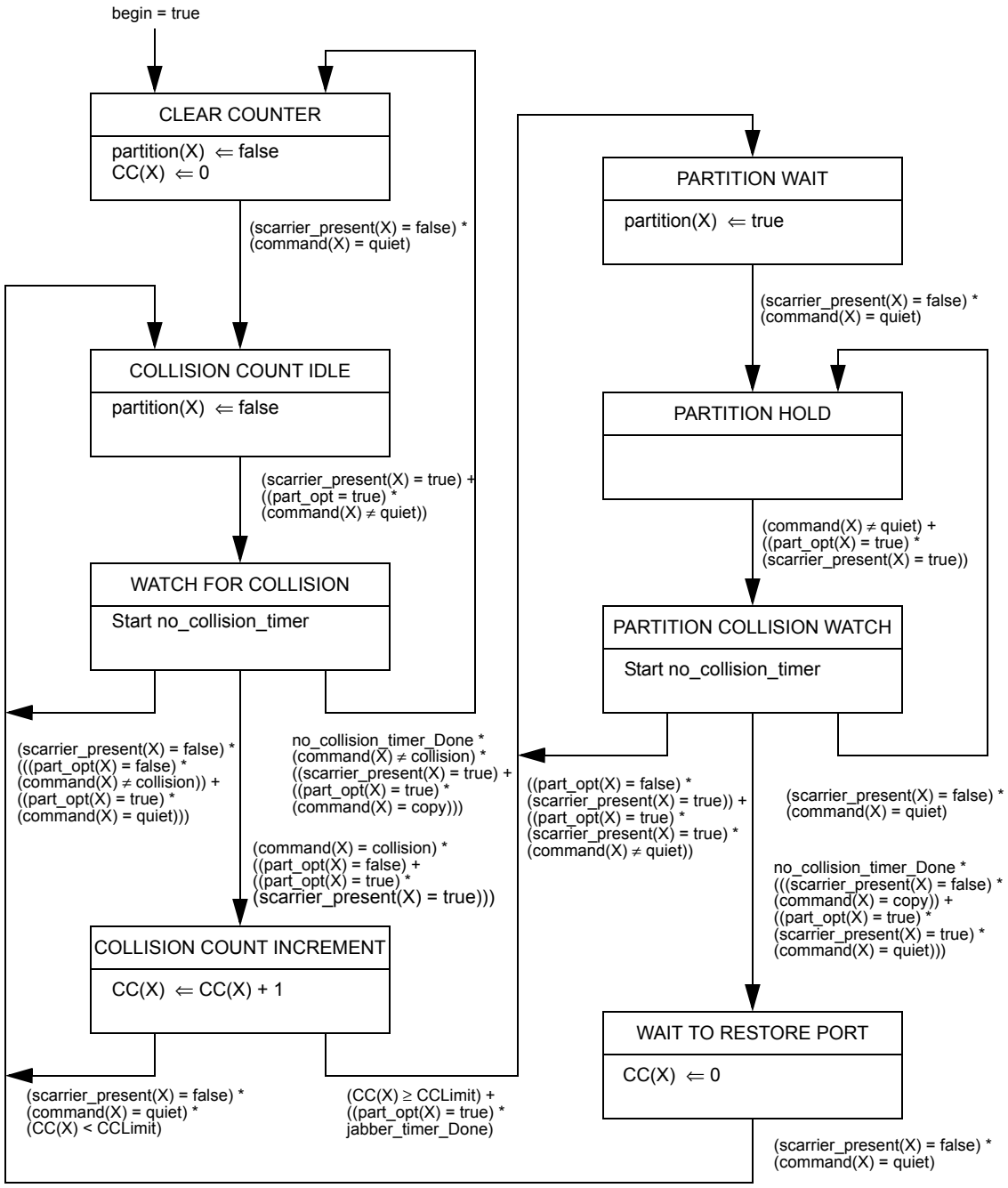


Figure 27–8—Partition state diagram for Port X

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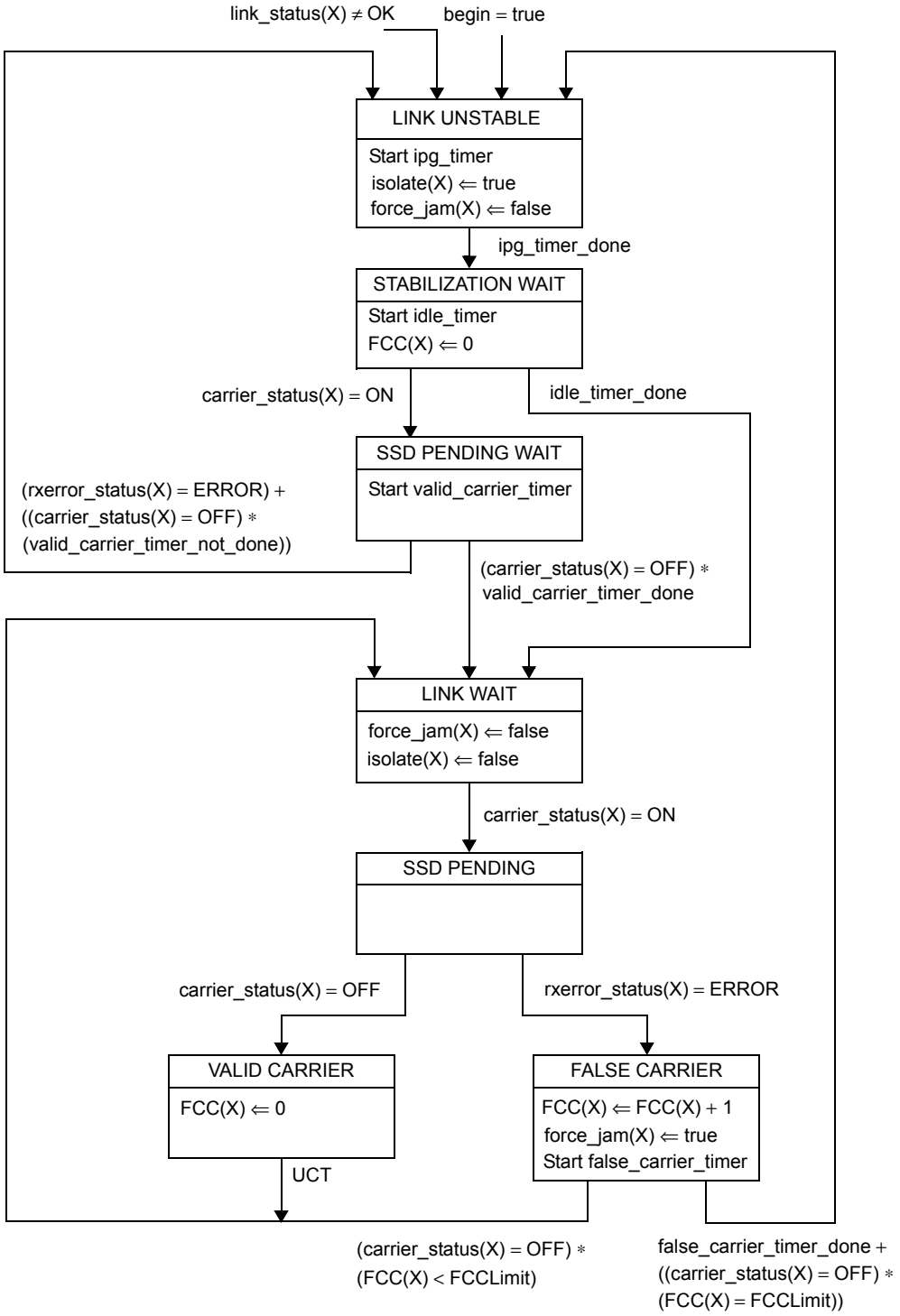


Figure 27–9—100BASE-X/T2 Carrier Integrity Monitor state diagram for Port X

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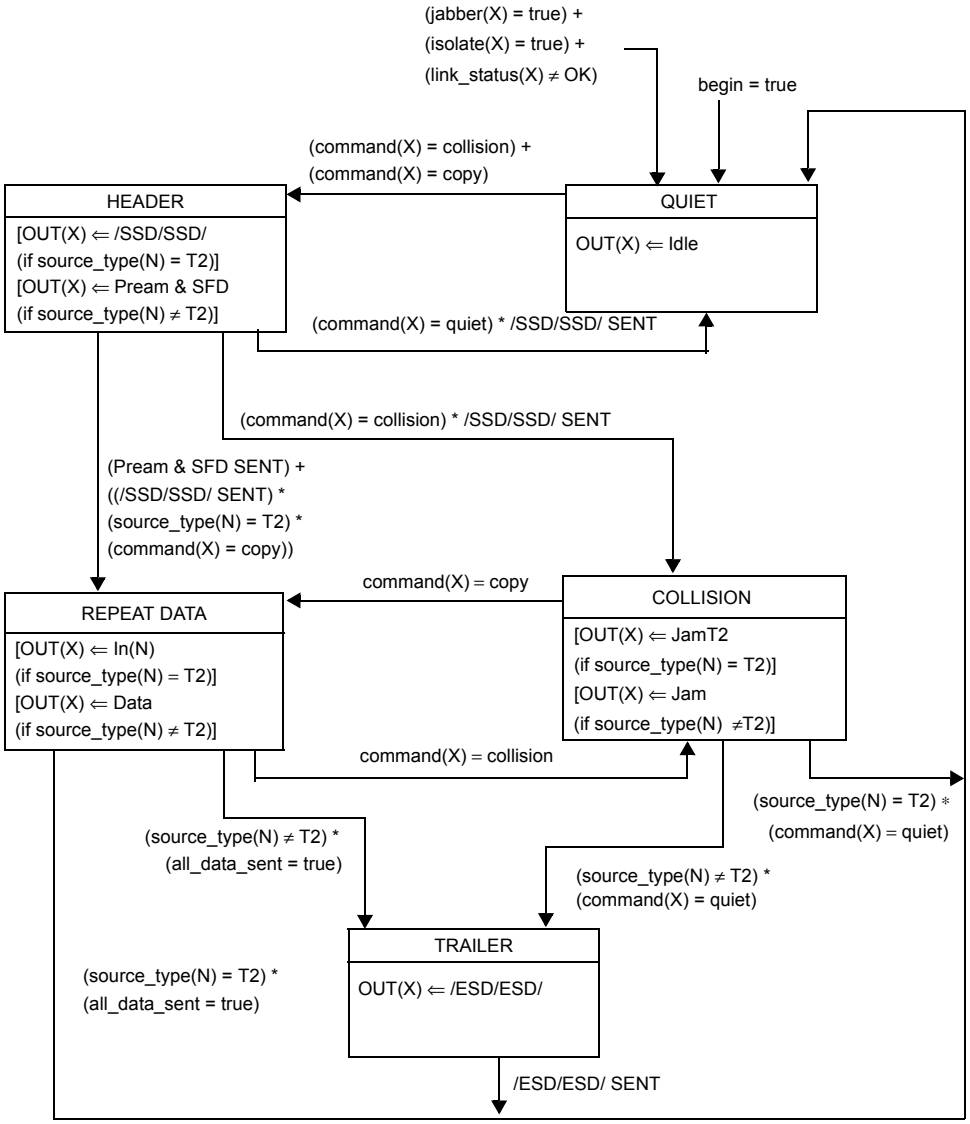


Figure 27–10—100BASE-T2 Transmit state diagram for Port X

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27.4 Repeater electrical specifications

27.4.1 Electrical isolation

Network segments that have different isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of the repeater set.

27.5 Environmental specifications

27.5.1 General safety

All equipment meeting this standard shall conform to IEC 60950-1.

27.5.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this subclause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cables and components.
c) High-energy transients coupled onto the LAN cable system.
d) Voltage potential differences between safety grounds to which the various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 27.5.3.

27.5.2.1 Installation

Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

27.5.2.2 Grounding

The safety ground, or chassis ground for the repeater set, shall be provided through the main ac power cord via the third wire ground as defined by applicable local codes and regulations. It is recommended that an external PHY to the repeater should also be mechanically grounded to the repeater unit through the power and ground signals in the MII connection and via the metal shell and shield of the MII connector if available.

If the MDI connector should provide a shield connection, the shield may be connected to the repeater safety ground. A network segment connected to the repeater set through the MDI may use a shield. If both ends of the network segment have a shielded MDI connector available, then the shield may be grounded at both ends according to local regulations and ISO/IEC 11801:1995, and as long as the ground potential difference between both ends of the network segment is less than 1 V rms. The same rules apply towards an inter-repeater link between two repeaters. Multiple repeaters should reside on the same power main; if not, then it is highly recommended that the repeaters be connected via fiber.

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WARNING

It is assumed that the equipment to which the repeater is attached is properly grounded and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

27.5.2.3 Installation and maintenance guidelines

During installation and maintenance of the cable plant, care should be taken to ensure that uninsulated network cable connectors do not make electrical contact with unintended conductors or ground.

27.5.3 Electrical isolation

There are two electrical power distribution environments to be considered that require different electrical isolation properties:

a) *Environment A*. When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
b) *Environment B*. When a LAN crosses the boundary between separate power distribution systems or the boundary of a single building.

27.5.3.1 Environment A requirements

Attachment of network segments via repeater sets requires electrical isolation of 500 V rms, one-minute withstand, between the segment and the protective ground of the repeater unit.

27.5.3.2 Environment B requirements

The attachment of network segments that cross Environment B boundaries requires electrical isolation of 1500 V rms, one-minute withstand, between each segment and all other attached segments and also the protective ground of the repeater unit.

The requirements for interconnected electrically conducting LAN segments that are partially or fully external to a single building environment may require additional protection against lightning strike hazards. Such requirements are beyond the scope of this standard. It is recommended that the above situation be handled by the use of nonelectrically conducting segments (e.g., fiber optic).

It is assumed that any nonelectrically conducting segments will provide sufficient isolation within that media to satisfy the isolation requirements of Environment B.

27.5.4 Reliability

A two-port repeater set shall be designed to provide a mean time between failure (MTBF) of at least 50 000 hours of continuous operation without causing a communications failure among stations attached to the network medium. Repeater sets with more than two ports shall add no more than 3.46×10^{-6} failures per hour for each additional port.

The repeater set electronics should be designed to minimize the probability of component failures within the repeater electronics that prevent communications among other PHYs on the individual segments. Connectors and other passive components comprising the means of connecting the repeater to the cable should be designed to minimize the probability of total network failure.

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27.5.5 Environment

27.5.5.1 Electromagnetic emission

The repeater shall comply with applicable local and national codes for the limitation of electromagnetic interference.

27.5.5.2 Temperature and humidity

The repeater is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the repeater the operating environmental conditions to facilitate selection, installation, and maintenance.

27.6 Repeater labeling

It is required that each repeater (and supporting documentation) shall be labeled in a manner visible to the user with these parameters:

a) Crossover ports appropriate to the respective PHY should be marked with an X.
b) The repeater set class type should be labeled in the following manner:
    1) Class I: a Roman numeral “I” centered within a circle.
    2) Class II: a Roman numeral “II” centered within a circle.

Additionally, it is recommended that each repeater (and supporting documentation) also be labeled in a manner visible to the user with at least these parameters:

c) Data rate capability in Mb/s
d) Any applicable safety warnings
e) Port type, i.e., 100BASE-TX, 100BASE-T4, or 100BASE-T2
f) Worst-case bit time delays between any two ports appropriate for
    1) Start-of-packet propagation delay
    2) Start-of-collision Jam propagation delay
    3) Cessation-of-collision Jam propagation delay

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27.7 Protocol implementation conformance statement (PICS) proforma for Clause 27, Repeater for 100 Mb/s baseband networks[10]

27.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 27, Repeater for 100 Mb/s baseband networks, shall complete the following protocol implementation conformance statement (PICS) proforma.

27.7.2 Identification

27.7.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

27.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Clause 27, Repeater for 100 Mb/s baseband networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2015.)	

Date of Statement	

[10]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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27.7.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*FXP	Repeater supports 100BASE-FX connections	27.1.2.2	O		
*TXP	Repeater supports 100BASE-TX connections	27.1.2.2	O		
*T4P	Repeater supports 100BASE-T4 connections	27.1.2.2	O		
*T2P	Repeater supports 100BASE-T2 connections	27.1.2.2	O		
*CLI	Repeater meets Class I delays	27.1.1.3	O		
*CLII	Repeater meets Class II delays	27.1.1.3	O		
*PHYS	PHYs capable of detecting non 100BASE-T signals	27.3.1.5.2	O		
*OPF	Partition function supports the recommended optional measures as described	27.3.1.6	O		

In addition, the following predicate name is defined for use when different implementations from the set above have common parameters:

*XP:FXP or TXP

27.7.4 PICS proforma tables for the repeater for 100 Mb/s baseband networks

27.7.4.1 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CC1	100BASE-FX port compatible at the MDI	27.1.2.2	FXP:M		
CC2	100BASE-TX port compatible at the MDI	27.1.2.2	TXP:M		
CC3	100BASE-T4 port compatible at the MDI	27.1.2.2	T4P:M		
CC4	Internal segment compatibility	27.1.2.2.1	M		Internal port meets Clause 30 when repeater management implemented
CC5	100BASE-T2 port compatible at the MDI	27.1.2.2	T2P:M		

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27.7.4.2 Repeater functions

Item	Feature	Subclause	Status	Support	Value/Comment
RF1	Signal Restoration	27.3.1	M		
RF2	Data Handling	27.3.1	M		
RF3	Received Event Handling	27.3.1	M		
RF4	Collision Handling	27.3.1	M		
RF5	Error Handling	27.3.1	M		
RF6	Partition	27.3.1	M		
RF7	Received Jabber	27.3.1	M		

27.7.4.3 Signal Restoration function

Item	Feature	Subclause	Status	Support	Value/Comment
SR1	Output amplitude as required by 100BASE-FX	27.3.1.1.1	FXP:M		
SR2	Output amplitude as required by 100BASE-TX	27.3.1.1.1	TXP:M		
SR3	Output amplitude as required by 100BASE-T4	27.3.1.1.1	T4P:M		
SR4	Output signal wave-shape as required by 100BASE-FX	27.3.1.1.2	FXP:M		
SR5	Output signal wave-shape as required by 100BASE-TX	27.3.1.1.2	TXP:M		
SR6	Output signal wave-shape as required by 100BASE-T4	27.3.1.1.2	T4P:M		
SR7	Output data timing as required by 100BASE-FX	27.3.1.1.3	FXP:M		
SR8	Output data timing as required by 100BASE-TX	27.3.1.1.3	TXP:M		
SR9	Output data timing as required by 100BASE-T4	27.3.1.1.3	T4P:M		
SR10	Output amplitude as required by 100BASE-T2	27.3.1.1.1	T2P:M		
SR11	Output signal wave-shape as required by 100BASE-T2	27.3.1.1.2	T2P:M		
SR12	Output data timing as required by 100BASE-T2	27.3.1.1.3	T2P:M		

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27.7.4.4 Data Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
DH1	Data frames forwarded to all ports except receiving port	27.3.1.2.1	M		
DH2	Data frames transmitted as appropriate for 100BASE-FX	27.3.1.2.1	FXP:M		
DH3	Data frames transmitted as appropriate for 100BASE-TX	27.3.1.2.1	TXP:M		
DH4	Data frames transmitted as appropriate for 100BASE-T4	27.3.1.2.1	T4P:M		
DH5	Code Violations forwarded to all transmitting ports	27.3.1.2.2	M		
DH6	Code Violations forwarded as received	27.3.1.2.2	O.1		
DH7	Received Code Violation forwarded as /H/ or as received	27.3.1.2.2	XP:O.1		
DH8	Received Code Violation forwarded as bad_code or as received	27.3.1.2.2	T4P:O.1		
DH9	Code element substitution for remainder of packet after received Code Violation	27.3.1.2.2	M		
DH10	Data frames transmitted as appropriate for 100BASE-T2	27.3.1.2.1	T2P:M		

27.7.4.5 Receive Event Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
RE1	scarrier_present detect implemented	27.3.1.3.1	M		
RE2	Repeat all received signals	27.3.1.3.1	M		
RE3	Preamble encoded as required by 100BASE-FX	27.3.1.3.2	FXP:M		
RE4	Preamble encoded as required by 100BASE-TX	27.3.1.3.2	TXP:M		
RE5	Preamble encoded as required by 100BASE-T4	27.3.1.3.2	T4P:M		
RE6	Start-of-packet propagation delay, Class I repeater	27.3.1.3.3	CLI:M		
RE7	Start-of-packet propagation delay, Class II repeater	27.3.1.3.3	CLII:M		
RE8	Start-of-packet variability for 100BASE-FX input port	27.3.1.3.4	FXP:M		7.0 BT

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27.7.4.5 Receive Event Handling function *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
RE8	Start-of-packet variability for 100BASE-TX input port	27.3.1.3.4	TXP:M		7.0 BT
RE9	Start-of-packet variability for 100BASE-T4 input port	27.3.1.3.4	T4P:M		8.0 BT
RE10	Preamble encoded as required by 100BASE-T2	27.3.1.3.2	T2P:M		
RE11	Start of packet variability for 100BASE-T2 input port	27.3.1.3.4	T2P:M		8.0 BT

27.7.4.6 Collision Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
CO1	Collision detection	27.3.1.4.1	M		Receive event on more than one port
CO2	Jam generation	27.3.1.4.2	M		Transmit Jam message while collision is detected
CO3	Collision-jam propagation delay, Class I repeater	27.3.1.4.3	CLI:M		SOP + SOJ ≤ 140 BT
CO4	Collision-jam propagation delay, Class II repeater with any port T4	27.3.1.4.3	CLII:M		SOP + SOJ ≤ 67 BT
CO5	Collision-jam propagation delay, Class II repeater, all TX/FX ports	27.3.1.4.3	CLII:M		SOP ≤ 46, SOJ ≤ 46 BT
CO6	Cessation of collision propagation delay, Class I repeater	27.3.1.4.4	CLI:M		EOJ ≤ SOP
CO7	Cessation of collision propagation delay, Class II repeater	27.3.1.4.4	CLII:M		EOJ ≤ SOP
CO8	Collision-jam propagation delay, Class II repeater with any port T2	27.3.1.4.3	CLII * T2P:M		SOP + SOJ ≤ 90 BT

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27.7.4.7 Error Handling function

Item	Feature	Subclause	Status	Support	Value/Comment
EH1	Carrier Integrity function implementation	27.3.1.5.1	XP:M		Self-interrupt of data reception
EH2	False carrier count for Link Unstable detection	27.3.1.5.1	XP:M		False carrier count in excess of FCCLimit
EH3	False carrier count reset	27.3.1.5.1	XP:M		Count reset on valid carrier
EH4	False carrier timer for Link Unstable detection	27.3.1.5.1	XP:M		False carrier of length in excess of false_carrier_timer
EH5	Jam message duration	27.3.1.5.1	XP:M		Equals duration of false carrier event, but not greater than duration of false_carrier_timer
EH6	Link Unstable detection	27.3.1.5.1	XP:M		False Carrier count exceed FCCLimit or False carrier exceeds the false_carrier_timer or power-up reset
EH7	Messages sent to repeater unit in Link Unstable state	27.3.1.5.1	XP:M		Inhibited sending messages to repeater unit
EH8	Messages sent from repeater unit in Link Unstable state	27.3.1.5.1	XP:M		Inhibited sending output messages
EH9	Monitoring activity on PMA interface in Link Unstable state	27.3.1.5.1	XP:M		Continue monitoring activity at PMA interface
EH10	Reset of Link Unstable state	27.3.1.5.1	XP:M		No activity for more than ipg_timer plus idle_timer or Valid carrier event of duration greater than valid_carrier_timer preceded by Idle of duration greater than ipg_timer
EH11	Block flow of non-100 Mb/s signals	27.3.1.5.2	PHYS:M		

27.7.4.8 Partition functions

Item	Feature	Subclause	Status	Support	Value/Comment
PA1	Partition function implementation	27.3.1.6	M		Self-interrupt of data reception
PA2	Collision count for entry into partition state	27.3.1.6	M		Collision count greater than or equal to CCLimit
PA3	Collision counter incrementing	27.3.1.6	M		Count incremented on a collision
PA4	*Collision counter reset*	*27.3.1.6*	*M*		*Count reset on receive activity in excess of no_collision_timer without collision*

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27.7.4.8 Partition functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PA5			OPF:M		Count reset on transmission in excess of no_collision_timer without collision
PA6	Messages sent to repeater unit in Partition state	27.3.1.6	M		Inhibited sending messages to repeater unit
PA7	Messages sent from repeater unit in Partition state	27.3.1.6	M		Continue sending output messages
PA8	Monitoring activity on PMA interface in Partition state	27.3.1.6	M		Continue monitoring activity at PMA interface
PA9	Reset of Partition state	27.3.1.6	M		Power-up reset or transmission in excess of no_collision_timer without collision
PA10			OPF:M		Receive activity in excess of no_collision_timer without collision
PA11	Excessive carrier entry into Partition state	27.3.1.6	OPF:M		Carrier duration in excess of jabber_timer in which a collision occurs

27.7.4.9 Receive Jabber function

Item	Feature	Subclause	Status	Support	Value/Comment
RJ1	Receive Jabber function implementation	27.3.1.7	M		Self-interrupt of data reception
RJ2	Excessive receive duration timer for Receive Jabber detection	27.3.1.7	M		Reception duration in excess of jabber_timer
RJ3	Messages sent to repeater unit in Receive Jabber state	27.3.1.7	M		Inhibit sending input messages to repeater unit
RJ4	Messages sent from repeater unit in Receive Jabber state	27.3.1.7	M		Inhibit sending output messages
RJ5	Reset of Receive Jabber state	27.3.1.7	M		Power-up reset or Carrier no longer detected

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27.7.4.10 Repeater state diagrams

Item	Feature	Subclause	Status	Support	Value/Comment
SD1	Repeater Core state diagram	27.3.2.2	M		Meets the requirements of Figure 27–2
SD2	Receive state diagram for Port X	27.3.2.2	M		Meets the requirements of Figure 27–3
SD3	100BASE-TX and 100BASE-FX Transmit state diagram for Port X	27.3.2.2	XP:M		Meets the requirements of Figure 27–4
SD4	100BASE-T4 Transmit state diagram for Port X	27.3.2.2	T4P:M		Meets the requirements of Figure 27–5
SD5	Repeater Data Handler state diagram	27.3.2.2	M		Meets the requirements of Figure 27–6
SD6	Receive Timer for Port X state diagram	27.3.2.2	M		Meets the requirements of Figure 27–7
SD7	Repeater Partition state diagram for Port X	27.3.2.2	M		Meets the requirements of Figure 27–8
SD8	Carrier Integrity Monitor for Port X state diagram	27.3.2.2	M		Meets the requirements of Figure 27–9
SD9	100BASE-T2 Transmit state diagram for Port X	27.3.2.2	T2P:M		Meets the requirements of Figure 27–10

27.7.4.11 Repeater electrical

Item	Feature	Subclause	Status	Support	Value/Comment
EL1	Port-to-port isolation	27.4.1	M		Satisfies isolation and grounding requirements for attached network segments
EL2	Safety	27.5.1	M		IEC 60950:1991
EL3	Installation practices	27.5.2.1	M		Sound, as defined by local code and regulations
EL4	Grounding	27.5.2.2	M		Chassis ground provided through ac mains cord
EL5	2-port repeater set MTBF	27.5.4	M		At least 50 000 hours
EL6	Additional port effect on MTBF	27.5.4	M		No more than 3.46×10^{-6} increase in failures per hour
EL7	Electromagnetic interference	27.5.5.1	M		Comply with local or national codes

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27.7.4.12 Repeater labeling

Item	Feature	Subclause	Status	Support	Value/Comment
LB1	Crossover ports	27.6	M		Marked with an X
LB2	Class I repeater	27.6	CLI:M		Marked with a Roman numeral I centered within a circle
LB3	Class II repeater	27.6	CLII:M		Marked with Roman numerals II centered within a circle
LB4	Data rate	27.6	O		100 Mb/s
LB5	Safety warnings	27.6	O		Any applicable
LB6	Port types	27.6	O		100BASE-FX or 100BASE-TX or 100BASE-T4 or 100BASE-T2
LB7	Worse-case start-of-packet propagation delay	27.6	O		Value in bit times
LB8	Worse-case start-of-collision-Jam propagation delay	27.6	O		Value in bit times
LB9	Worse-case cessation-of-collision Jam propagation delay	27.6	O		Value in bit times

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28. Physical Layer link signaling for Auto-Negotiation on twisted pair

28.1 Overview

28.1.1 Scope

Clause 28 describes the Auto-Negotiation function that allows a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. The normative definitions for all extensions to Auto-Negotiation and all related register assignments for this standard are documented in Annex 28D.

The objective of the Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. Auto-Negotiation is performed using a modified 10BASE-T link integrity test pulse sequence, such that no packet or upper layer protocol overhead is added to the network devices (see Figure 28–1). Auto-Negotiation does not test the link segment characteristics (see 28.1.4).

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The Auto-Negotiation function allows the devices to switch between the various operational modes in an ordered fashion, permits management to disable or enable the Auto-Negotiation function, and allows management to select a specific operational mode. The Auto-Negotiation function also provides a Parallel Detection function to allow 10BASE-T, 100BASE-TX, and 100BASE-T4 compatible devices to be recognized, even though they may not provide Auto-Negotiation.

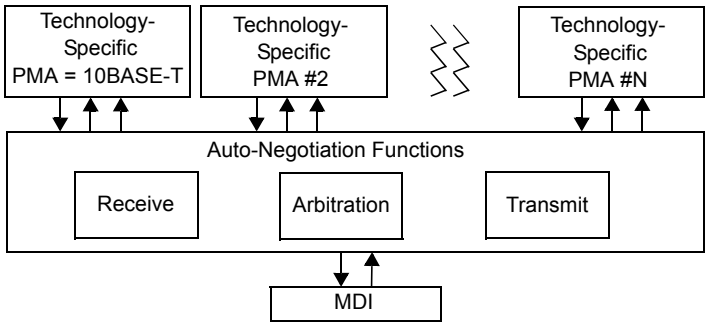


Figure 28–1—High-level model

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced link integrity test pulses that individually meet the 10BASE-T Transmitter Waveform for Link Test Pulse (Figure 14–13). This burst of pulses is referred to as a Fast Link Pulse (FLP) Burst. Each device capable of Auto-Negotiation issues FLP Bursts at power up, on command from management, or due to user interaction. The FLP Burst consists of a series of link integrity test pulses that form an alternating clock/data sequence. Extraction of the data bits from the FLP Burst yields a link codeword that identifies the operational modes supported by the remote device, as well as some information used for the Auto-Negotiation function's handshake mechanism.

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To maintain interoperability with existing 10BASE-T devices, the function also supports the reception of 10BASE-T compliant link integrity test pulses. 10BASE-T link pulse activity is referred to as the Normal Link Pulse (NLP) sequence and is defined in 14.2.1.1. A device that fails to respond to the FLP Burst sequence by returning only the NLP sequence is treated as a 10BASE-T compatible device.

28.1.2 Application perspective/objectives

The Auto-Negotiation function is designed to be expandable and allow IEEE 802.3 compatible devices using an eight-pin modular connector to self-configure a jointly compatible operating mode. Implementation of the Auto-Negotiation function is optional. However, it is highly recommended that this method alone be utilized to perform the negotiation of the link operation.

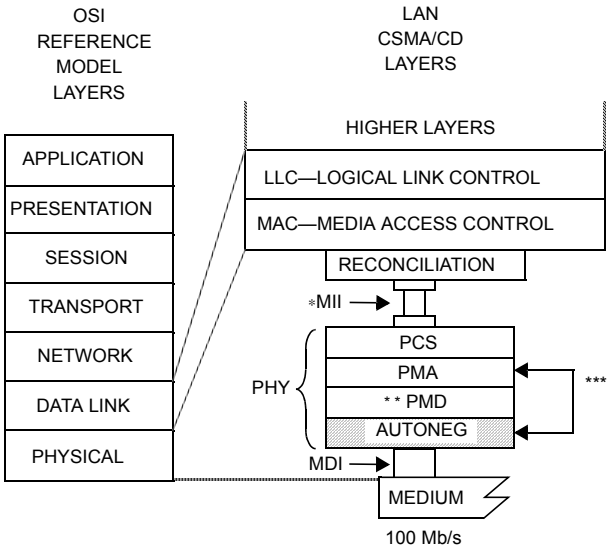
The following are the objectives of Auto-Negotiation:

a) Must interoperate with the IEEE 802.3 10BASE-T installed base.
b) Must allow automatic upgrade from the 10BASE-T mode to the desired "High-Performance Mode."
c) Requires that the 10BASE-T data service is the Lowest Common Denominator (LCD) that can be resolved. A 10BASE-T PMA is not required to be implemented, however. Only the NLP Receive Link Integrity Test function is required.
d) Reasonable and cost-effective to implement.
e) Must provide a sufficiently extensible code space to
    1) Meet existing and future requirements.
    2) Allow simple extension without impacting the installed base.
    3) Accommodate remote fault signals.
    4) Accommodate Link Partner ability detection.
f) Must allow manual or Network Management configuration to override the Auto-Negotiation.
g) Must be capable of operation in the absence of Network Management.
h) Must not preclude the ability to negotiate "back" to the 10BASE-T operational mode.
i) Must operate when
    1) The link is initially electrically connected.
    2) A device at either end of the link is powered up, reset, or a renegotiation request is made.
j) The Auto-Negotiation function may be enabled by automatic, manual, or Network Management intervention.
k) Completes the Base Page Auto-Negotiation function in a bounded time period.
l) Will provide the basis for the link establishment process in future CSMA/CD compatible LAN standards that use an eight-pin modular connector.
m) Must not cause corruption of IEEE 802.3 Layer Management statistics.
n) Operates using a peer-to-peer exchange of information with no requirement for a master device (not master-slave).
o) Must be robust in the UTP cable noise environment.
p) Must not significantly impact EMI/RFI emissions.

28.1.3 Relationship to architectural layering

The Auto-Negotiation function is provided at the Physical Layer of the OSI reference model as shown in Figure 28–2. Devices that support multiple modes of operation may advertise this fact using this function. The actual transfer of information of ability is observable only at the MDI or on the medium. Auto-Negotiation signaling does not occur across either the AUI or MII. Control of the Auto-Negotiation function may be supported through the Management Interface of the MII or equivalent. If an explicit embodiment of the MII is supported, the control and status registers to support the Auto-Negotiation function shall be implemented in accordance with the definitions in Clause 22 and 28.2.4. If a physical embodiment of the MII management is not present, then it is strongly recommended that the implementation provide control and status mechanisms equivalent to those described in Clause 22 and 28.2.4 for manual and/or management interaction.

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MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
AUTONEG = AUTO-NEGOTIATION
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-X only; 100BASE-T4 does not use this layer.
*** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indication.

Figure 28–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

28.1.4 Compatibility considerations

The Auto-Negotiation function is designed to be completely backwards compatible and interoperable with 10BASE-T compliant devices. In order to achieve this, a device supporting the Auto-Negotiation function must provide the NLP Receive Link Integrity Test function as defined in Figure 28–19. The Auto-Negotiation function also supports connection to 100BASE-TX and 100BASE-T4 devices without Auto-Negotiation through the Parallel Detection function. Connection to technologies other than 10BASE-T, 100BASE-TX, or 100BASE-T4 that do not incorporate Auto-Negotiation is not supported.

Implementation of the Auto-Negotiation function is optional. For CSMA/CD compatible devices that use the eight-pin modular connector of IEC 60603-7 and that also encompass multiple operational modes, if a signaling method is used to automatically configure the preferred mode of operation, then the Auto-Negotiation function shall be used in compliance with Clause 28. If the device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities, the device shall implement the Auto-Negotiation function as administered by this specification. All future CSMA/CD implementations that use an eight-pin modular connector shall be interoperable with devices supporting Clause 28. If the implementer of a non-CSMA/CD eight-pin modular device wishes to assure that its operation does not conflict with CSMA/CD devices, then adherence to Clause 28 is recommended.

While this Auto-Negotiation function must be implemented in CSMA/CD compatible devices that utilize the eight-pin modular connector, encompass multiple operational modes, and offer an Auto-Negotiation mechanism, the use of this function does not mandate that the 10BASE-T packet data communication service must exist. A device that employs this function must support the 10BASE-T Link Integrity Test

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function through the NLP Receive Link Integrity Test state diagram. The device may also need to support other technology-dependent link test functions depending on the modes supported. Auto-Negotiation does not perform cable tests, such as detect number of conductor pairs (if more than two pairs are required) or cable performance measurements. Some PHYs that explicitly require use of high-performance cables, may require knowledge of the cable type, or additional robustness tests (such as monitoring CRC or framing errors) to determine if the link segment is adequate.

28.1.4.1 Interoperability with existing 10BASE-T devices

During Auto-Negotiation, FLP Bursts separated by 16 ms ± 8 ms are transmitted. The FLP Burst itself is a series of pulses separated by 62.5 µs ± 7 µs. The timing of FLP Bursts will cause a 10BASE-T device that is in the LINK TEST PASS state to remain in the LINK TEST PASS state while receiving FLP Bursts. An Auto-Negotiation able device must recognize the NLP sequence from a 10BASE-T Link Partner, cease transmission of FLP Bursts, and enable the 10BASE-T PMA, if present. If the NLP sequence is detected and if the Auto-Negotiation able device does not have a 10BASE-T PMA, it will cease transmission of FLP Bursts, forcing the 10BASE-T Link Partner into the LINK TEST FAIL state(s) as indicated in Figure 14–6.

NOTE—Auto-Negotiation does not support the transmission of the NLP sequence. The 10BASE-T PMA provides this function if it is connected to the MDI. In the case where an Auto-Negotiation able device without a 10BASE-T PMA is connected to a 10BASE-T device without Auto-Negotiation, the NLP sequence is not transmitted because the Auto-Negotiation function has no 10BASE-T PMA to enable that can transmit the NLP sequence.

28.1.4.2 Interoperability with Auto-Negotiation compatible devices

An Auto-Negotiation compatible device decodes the base link codeword from the FLP Burst, and examines the contents for the highest common ability that both devices share. Both devices acknowledge correct receipt of each other's base link codewords by responding with FLP Bursts containing the Acknowledge Bit set. After both devices complete acknowledgment, and optionally, Next Page exchange, both devices enable the highest common mode negotiated. The highest common mode is resolved using the priority resolution hierarchy specified in Annex 28B. It may subsequently be the responsibility of a technology-dependent link integrity test function to verify operation of the link prior to enabling the data service.

28.1.4.3 Cabling compatibility with Auto-Negotiation

Provision has been made within Auto-Negotiation to limit the resulting link configuration in situations where the cabling may not support the highest common capability of the two end points. The system administrator/installer must take the cabling capability into consideration when configuring a repeater port's advertised capability. That is, the advertised capability of a hub port should not result in an operational mode that is not compatible with the cabling.

28.2 Functional specifications

The Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PMA type, where more than one PMA type may exist. Management may provide additional control of Auto-Negotiation through the Management function, but the presence of a management agent is not required.

The Auto-Negotiation function shall provide the Auto-Negotiation Transmit, Receive, and Arbitration functions and comply with the state diagrams of Figure 28–16 to Figure 28–19. The Auto-Negotiation function shall provide the NLP Receive Link Integrity Test function and comply with the state diagram of Figure 28–19 if the PHY supports 10BASE-T operation.The Auto-Negotiation functions shall interact with the technology-dependent PMAs through the Technology-Dependent Interface. Technology-dependent PMAs include, but are not limited to, 100BASE-TX and 100BASE-T4. Technology-dependent link integrity test functions shall be implemented and interfaced to only if the device supports the given technology. For example, a 10BASE-T and 100BASE-TX Auto-Negotiation able device must implement and interface to the

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100BASE-TX PMA/link integrity test function, but does not need to include the 100BASE-T4 PMA/Link Integrity Test function. The Auto-Negotiation function shall provide an optional Management function that provides a control and status mechanism.

28.2.1 Transmit function requirements

The Transmit function provides the ability to transmit FLP Bursts. The first FLP Bursts exchanged by the local device and its Link Partner after Power-On, link restart, or renegotiation contain the base link codeword defined in 28.2.1.2. The local device may modify the link codeword to disable an ability it possesses, but will not transmit an ability it does not possess. This makes possible the distinction between local abilities and advertised abilities so that multimode devices may Auto-Negotiate to a mode lower in priority than the highest common local ability.

28.2.1.1 Link pulse transmission

Auto-Negotiation's method of communication builds upon the link pulse mechanism employed by 10BASE-T MAUs to detect the status of the link. Compliant 10BASE-T MAUs transmit link integrity test pulses as a mechanism to determine if the link segment is operational in the absence of packet data. The 10BASE-T NLP sequence is a pulse (Figure 14–13) transmitted every 16 ms ± 8 ms while the data transmitter is idle.

Auto-Negotiation substitutes the FLP Burst in place of the single 10BASE-T link integrity test pulse within the NLP sequence (Figure 28–3). The FLP Burst encodes the data that is used to control the Auto-Negotiation function. FLP Bursts shall not be transmitted when Auto-Negotiation is complete and the highest common denominator PMA has been enabled.

FLP Bursts were designed to allow use beyond initial link Auto-Negotiation, such as for a link monitor type function. However, use of FLP Bursts beyond the current definition for link startup shall be prohibited. Definition of the use of FLP Bursts while in the FLP LINK GOOD state is reserved.

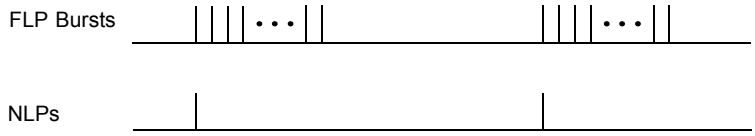


Figure 28–3—FLP Burst sequence to NLP sequence mapping

28.2.1.1.1 FLP burst encoding

All link test pulses in the FLP Burst sequence shall meet the template requirements of Figure 14–13 when measured across each of the test loads defined in Figure 14–12; both with the load connected directly to the TD circuit and with the load connected through all of the cable types and distances supported by the advertised capabilities. A Fast Link Pulse Burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a link pulse and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a link pulse present in an even-numbered pulse position represents a logic one, and a link pulse absent from an even-numbered pulse position represents a logic zero. Clock pulses are differentiated from data pulses by the spacing between pulses as shown in Figure 28–5 and

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enumerated in Table 28–1. An extended FLP Burst contains 97 similarly defined pulse positions with 49 odd-numbered clock pulses and 48 even-numbered data pulses.

Table 28–1—FLP Burst timing summary

	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width (Figure 14–13)		100		ns
T2	Clock Pulse to Clock Pulse	111	125	139	µs
T3	Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	µs
T4	Pulses in a Burst	17 for 16-bit 49 for 48-bit		33 for 16-bit 97 for 48-bit	—
T5	Burst Width		2 for 16-bit 6 for 48-bit		ms
T6	FLP Burst to FLP Burst	8	16	24	ms
T7	Optimized FLP Burst to FLP Burst	8		8.5	ms

The encoding of data using pulses in an FLP Burst is illustrated in Figure 28–4.

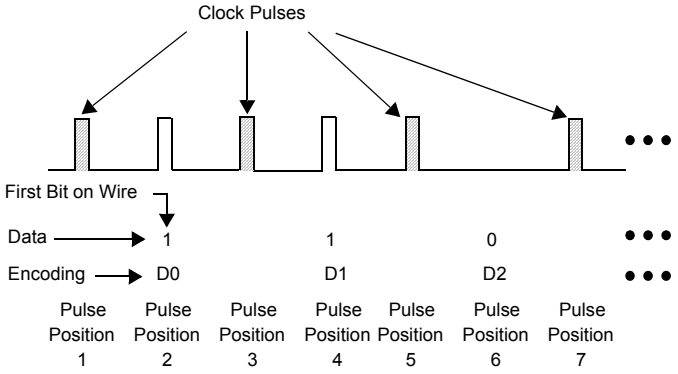


Figure 28–4—Data bit encoding within FLP Bursts

28.2.1.1.2 Transmit timing

The first pulse in an FLP Burst shall be defined as a clock pulse. Clock pulses within an FLP Burst shall be spaced at 125 µs ± 14 µs. If the data bit representation of logic one is to be transmitted, a pulse shall occur 62.5 µs ± 7 µs after the preceding clock pulse. If a data bit representing logic zero is to be transmitted, there shall be no link integrity test pulses within 111 µs of the preceding clock pulse.

The first link pulse in consecutive FLP Bursts shall occur at a 16 ms ± 8 ms interval when using non-optimized FLP Burst to FLP Burst timing, see parameter T6 (Figure 28–6). Devices supporting Extended Next Pages shall use optimized FLP Burst to FLP Burst timing. The first link pulse in consecutive FLP Bursts shall occur at a 8.25 ms ± 0.25 ms interval when using optimized FLP Burst to FLP Burst timing, see parameter T7 (Figure 28–6). Optimized FLP Burst to FLP Burst limits are intended to reduce negotiation time.

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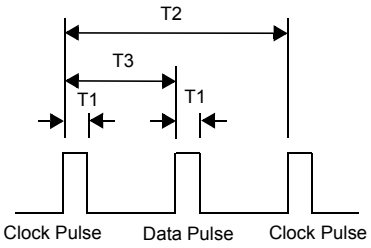


Figure 28–5—FLP Burst pulse-to-pulse timing

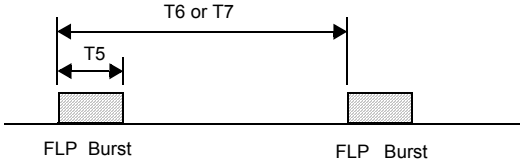


Figure 28–6—FLP Burst to FLP Burst timing

28.2.1.2 Link codeword encoding

The base link codeword (Base Page) transmitted within an FLP Burst shall convey the encoding shown in Figure 28–7. The Auto-Negotiation function may support additional pages using the Next Page function. Encodings for the link codeword(s) used in Next Page exchange are defined in 28.2.3.4. In an FLP Burst, D0 shall be the first bit transmitted.

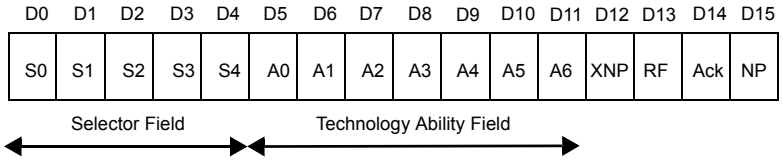


Figure 28–7—Base Page encoding

28.2.1.2.1 Selector Field

Selector Field (S[4:0]) is a five bit wide field, encoding 32 possible messages. Selector Field encoding definitions are shown in Annex 28A. Combinations not specified are reserved for future use. Reserved combinations of the Selector Field shall not be transmitted.

28.2.1.2.2 Technology Ability Field

Technology Ability Field (A[6:0]) is a seven-bit wide field containing information indicating supported technologies specific to the selector field value. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector is described in Annex 28B.2 and in Annex 28D. Multiple technologies may be advertised in the link codeword. A device shall support the data service ability for a technology it advertises.

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It is the responsibility of the Arbitration function to determine the common mode of operation shared by a Link Partner and to resolve multiple common modes.

NOTE—While devices using a Selector Field value other than the IEEE 802.3 Selector Field value are free to define the Technology Ability Field bits, it is recommended that the 10BASE-T bit be encoded in the same bit position as in the IEEE 802.3 selector. A common bit position can be important if the technology using the other selector will ever coexist on a device that also offers a 10BASE-T mode.

28.2.1.2.3 Extended Next Page

Extended Next Page (XNP) is encoded in bit D12 of the base link codeword. The Extended Next Page bit indicates that the local device supports transmission of Extended Next Pages when set to a logic one, and indicates that the local device does not support Extended Next Pages when set to a logic zero. The use of Extended Next Page is orthogonal to the negotiated data rate, medium, or link technology. The Extended Next Page bit is used in accordance with the Extended Next Page function specifications in 28.2.3.4.

When the selector field value is the IEEE Std 802.5v-2001 (withdrawn) value or the IEEE Std 802.9a-1995 (withdrawn) value the Extended Next Page function is not supported and bit D12 is defined as being an additional Technology Ability Field bit A7, extending the Technology Ability Field to be an eight bit wide field (A[7:0]).

28.2.1.2.4 Remote Fault

Remote Fault (RF) is encoded in bit D13 of the base link codeword. The default value is logic zero. The Remote Fault bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the Auto-Negotiation advertisement register (Register 4) is set to logic one, the RF bit in the transmitted base link codeword is set to logic one. When the RF bit in the received base link codeword is set to logic one, the Remote Fault bit in the MII status register (Register 1) will be set to logic one, if the MII management function is present.

The Remote Fault bit shall be used in accordance with the Remote Fault function specifications (28.2.3.5).

28.2.1.2.5 Acknowledge

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its Link Partner's link codeword. The Acknowledge Bit is encoded in bit D14 regardless of the value of the Selector Field or link codeword encoding. If no Next Page information is to be sent, this bit shall be set to logic one in the link codeword after the reception of at least three consecutive and consistent FLP Bursts (ignoring the Acknowledge bit value). If Next Page information is to be sent, this bit shall be set to logic one after the device has successfully received at least three consecutive and matching FLP Bursts (ignoring the Acknowledge bit value), and will remain set until the Next Page information has been loaded into the Auto-Negotiation Next Page transmit register (Register 7). In order to save the current received link codeword, it must be read from the Auto-Negotiation Link Partner ability register (Register 6) before the Next Page of transmit information is loaded into the Auto-Negotiation Next Page transmit register. After the COMPLETE ACKNOWLEDGE state has been entered, the link codeword shall be transmitted six to eight (inclusive) times.

28.2.1.2.6 Next Page

Next Page (NP) is encoded in bit D15 regardless of the Selector Field value or link codeword encoding. Support for transmission and reception of additional link codeword encodings is optional. If Next Page ability is not supported, the NP bit shall always be set to logic zero. If a device implements Next Page ability and wishes to engage in Next Page exchange, it shall set the NP bit to logic one. A device may implement Next Page ability and choose not to engage in Next Page exchange by setting the NP bit to a logic zero. The Next Page function is defined in 28.2.3.4.

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28.2.1.3 Transmit Switch function

The Transmit Switch function shall enable the transmit path from a single technology-dependent PMA to the MDI once a highest common denominator choice has been made and Auto-Negotiation has completed.

During Auto-Negotiation, the Transmit Switch function shall connect only the FLP Burst generator controlled by the Transmit State Diagram, Figure 28–16, to the MDI.

When a PMA is connected to the MDI through the Transmit Switch function, the signals at the MDI shall conform to all of the PHY's specifications.

28.2.2 Receive function requirements

The Receive function detects the NLP sequence using the NLP Receive Link Integrity Test function of Figure 28–19. The NLP Receive Link Integrity Test function will not detect link pass based on carrier sense.

The Receive function detects the FLP Burst sequence, decodes the information contained within, and stores the data in rx_link_code_word[16:1]. The Receive function incorporates a receive switch to control connection to the 100BASE-TX or 100BASE-T4 PMAs in addition to the NLP Receive Link Integrity Test function, excluding the 10BASE-T Link Integrity Test function present in a 10BASE-T PMA. If Auto-Negotiation detects link_status=READY from any of the technology-dependent PMAs prior to FLP Burst detection, the autoneg_wait_timer (28.3.2) is started. If any other technology-dependent PMA indicates link_status=READY when the autoneg_wait_timer expires, Auto-Negotiation will not allow any data service to be enabled and may signal this as a remote fault to the Link Partner using the Base Page and will flag this in the Local Device by setting the Parallel Detection Fault bit (6.4) in the Auto-Negotiation expansion register. If a 10BASE-T PMA exists above the Auto-Negotiation function, it is not permitted to receive MDI activity in parallel with the NLP Receive Link Integrity Test function or any other technology-dependent function.

28.2.2.1 FLP Burst ability detection and decoding

In Figure 28–8 to Figure 28–10, the symbol "t_0=0" indicates the event that caused the timers described to start, and all subsequent times given are referenced from that point. All timers referenced shall expire within the range specified in Table 28–9 in 28.3.2.

The Receive function shall identify the Link Partner as Auto-Negotiation able if it receives 6 to 17 (inclusive) consecutive link pulses that are separated by at least flp_test_min_timer time (5 µs to 25 µs) but less than flp_test_max_timer time (165 µs to 185 µs) as shown in Figure 28–8. The information contained in the FLP Burst that identifies the Link Partner as Auto-Negotiation able shall not be passed to the Arbitration function if the FLP Burst is not complete. The Receive function may use the FLP Burst that identifies the Link Partner as Auto-Negotiation able for ability matching if the FLP Burst is complete. However, it is not required to use this FLP Burst for any purpose other than identification of the Link Partner as Auto-Negotiation able. Implementations may ignore multiple FLP Bursts before identifying the Link Partner as Auto-Negotiation able to allow for potential receive equalization time.

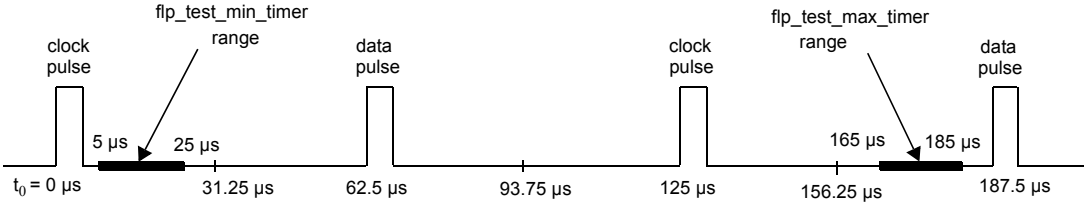


Figure 28–8—FLP detect timers (flp_test_min/max_timers)

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The Receive function captures and decodes link pulses received in FLP Bursts. The first link pulse in an FLP Burst shall be interpreted as a clock link pulse. Detection of a clock link pulse shall restart the data_detect_min_timer and data_detect_max timer. The data_detect_min/max_timers enable the receiver to distinguish data pulses from clock pulses and logic one data from logic zero data, as follows:

a) If, during an FLP Burst, a link pulse is received when the data_detect_min_timer has expired while the data_detect_max_timer has not expired, the data bit shall be interpreted as a logic one (Figure 28–9).
b) If, during an FLP Burst, a link pulse is received after the data_detect_max_timer has expired, the data bit shall be interpreted as a logic zero (Figure 28–9) and that link pulse shall be interpreted as a clock link pulse.

As each data bit is identified it is stored in the appropriate rx_link_code_word[16:1] element.

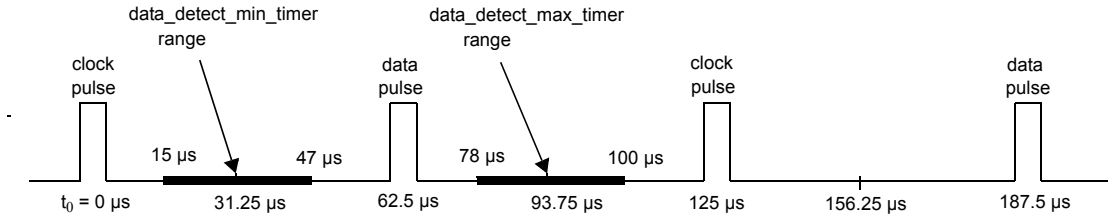
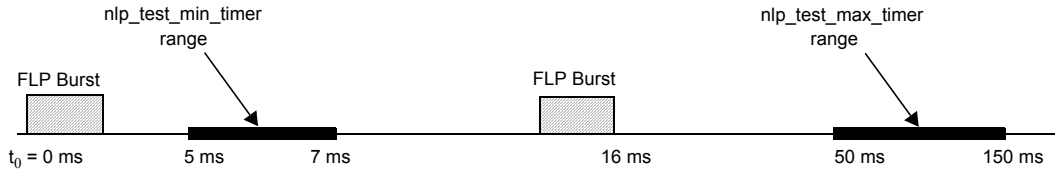


Figure 28–9—FLP data detect timers (data_detect_min/max_timers)

FLP Bursts conforming to the nlp_test_min_timer and nlp_test_max_timer timing as shown in Figure 28–10 shall be considered to have valid separation. The nlp_test_min_timer range for devices that do not support Extended Next Pages is shown in Figure 28–10. The range of nlp_test_min_timer for devices that support Extended Next Pages is specified in 28.3.2.



NOTE—The reference for the starting of the nlp_test_min_timer is from the beginning of the FLP Burst, as shown by t_0, while the reference for the starting of the nlp_test_max_timer is from the expiration of the nlp_test_min_timer.

Figure 28–10—FLP Burst timer (nlp_test_min/max_timers)

28.2.2.2 NLP detection

NLP detection is accomplished via the NLP Receive Link Integrity Test function in Figure 28–19. The NLP Receive Link Integrity Test function is a modification of the original 10BASE-T Link Integrity Test function (Figure 14–6), where the detection of receive activity will not cause a transition to the LINK TEST PASS state during Auto-Negotiation. The NLP Receive Link Integrity Test function also incorporates the Technology-Dependent Interface requirements.

28.2.2.3 Receive Switch function

The Receive Switch function shall enable the receive path from the MDI to a single technology-dependent PMA once a highest common denominator choice has been made and Auto-Negotiation has completed.

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During Auto-Negotiation, the Receive Switch function shall connect both the FLP Burst receiver controlled by the Receive state diagram, Figure 28–17, and the NLP Receive Link Integrity Test state diagram, Figure 28–19, to the MDI. During Auto-Negotiation, the Receive Switch function shall also connect the 100BASE-TX and 100BASE-T4 PMA receivers to the MDI if the 100BASE-TX and/or 100BASE-T4 PMAs are present.

When a PMA is connected to the MDI through the Receive Switch function, the signals at the PMA shall conform to all of the PHY's specifications.

28.2.2.4 Link codeword matching

The Receive function shall generate ability_match, acknowledge_match, and consistency_match variables as defined in 28.3.1.

28.2.3 Arbitration function requirements

The Arbitration function ensures proper sequencing of the Auto-Negotiation function using the Transmit function and Receive function. The Arbitration function enables the Transmit function to advertise and acknowledge abilities. Upon indication of acknowledgment, the Arbitration function determines the highest common denominator using the priority resolution function and enables the appropriate technology-dependent PMA via the Technology-Dependent Interface (28.2.6).

28.2.3.1 Parallel detection function

The Local Device detects a Link Partner that supports Auto-Negotiation by FLP Burst detection. The Parallel Detection function allows detection of Link Partners that support 100BASE-TX, 100BASE-T4, and/or 10BASE-T, but do not support Auto-Negotiation. Prior to detection of FLP Bursts, the Receive Switch shall direct MDI receive activity to the NLP Receive Link Integrity Test state diagram, 100BASE-TX and 100BASE-T4 PMAs, if present, but shall not direct MDI receive activity to the 10BASE-T or any other PMA. If at least one of the 100BASE-TX, 100BASE-T4, or NLP Receive Link Integrity Test functions establishes link_status=READY, the LINK STATUS CHECK state is entered and the autoneg_wait_timer is started. If exactly one link_status=READY indication is present when the autoneg_wait_timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PMA indicating link_status=READY. If a PMA is enabled, the Arbitration function shall set link_control=DISABLE to all other PMAs and indicate that Auto-Negotiation has completed. On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the Link Partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function.

NOTE 1—Native 10BASE-T devices will be detected by the NLP Receive Link Integrity Test function, an integrated part of the Auto-Negotiation function. Hence, Parallel Detection for the 10BASE-T PMA is not required or allowed.

NOTE 2—When selecting the highest common denominator through the Parallel Detection function, only the half-duplex mode corresponding to the selected PMA may automatically be detected.

28.2.3.2 Renegotiation function

A renegotiation request from any entity, such as a management agent, shall cause the Arbitration function to disable all technology-dependent PMAs and halt any transmit data and link pulse activity until the break_link_timer expires (28.3.2). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The Local Device shall resume Auto-Negotiation after the break_link_timer has expired by issuing FLP Bursts with the Base Page valid in tx_link_code_word[16:1].

Once Auto-Negotiation has completed, renegotiation will take place if the Highest Common Denominator technology that receives link_control=ENABLE returns link_status=FAIL. To allow the PMA an

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opportunity to determine link integrity using its own link integrity test function, the link_fail_inhibit_timer qualifies the link_status=FAIL indication such that renegotiation takes place if the link_fail_inhibit_timer has expired and the PMA still indicates link_status=FAIL or link_status=READY.

28.2.3.3 Priority Resolution function

Since a Local Device and a Link Partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PMA enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common to the Local Device and Link Partner that has the highest priority as defined in Annex 28B. This technology is referred to as the Highest Common Denominator, or HCD, technology. If the Local Device receives a Technology Ability Field with a bit set that is reserved, the Local Device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the FLP LINK GOOD CHECK state. In the event that a technology is chosen through the Parallel Detection function, that technology shall be considered the highest common denominator (HCD) technology. In the event that there is no common technology, HCD shall have a value of "NULL," indicating that no PMA receives link_control=ENABLE, and link_status_[HCD]=FAIL.

28.2.3.4 Next Page function

The Next Page function uses the standard Auto-Negotiation arbitration mechanisms to allow exchange of arbitrary pieces of data. Data is carried by optional Next Pages of information, which follow the transmission and acknowledgment procedures used for the base link codeword. Four types of Next Page encodings are defined: Message Pages, Unformatted Pages, extended Message Pages, and extended Unformatted Pages.

A dual acknowledgment system is used. Acknowledge (Ack) is used to acknowledge receipt of the information; Acknowledge 2 (Ack2) is used to indicate that the receiver is able to act on the information (or perform the task) defined in the message.

Next Page operation is controlled by the same three mandatory control bits, Next Page, Extended Next Page, and Acknowledge, used in the base link codeword. Setting the NP bit in the base link codeword to logic one indicates that the device is Next Page able. Setting the Extended Next Page bit in the Base Page link codeword to logic one indicates that the device is Extended Next Page able. If both a device and its Link Partner are Next Page able, then Next Page exchange may occur. If both a device and its Link Partner are Extended Next Page able, then any Next Page exchange that occurs shall use the Extended Next Page encoding. If one or both devices are not Next Page able, then Next Page exchange will not occur and, after the base link codewords have been exchanged, the FLP LINK GOOD CHECK state will be entered. The Toggle bit is used to ensure proper synchronization between the Local Device and the Link Partner.

Next Page exchange occurs after the base link codewords have been exchanged. Next Page exchange consists of using the normal Auto-Negotiation arbitration process to send Next Page messages. Four message encodings are defined: Message Pages, Unformatted Pages, extended Message Pages, and extended Unformatted Pages. Unformatted Pages can be combined to send extended messages. If the Selector Field values do not match, then each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be interpreted. If the Selector Field values match, then the convention governing the use of Message Pages shall be as defined by the Selector Field value definition. Any number of Next Pages may be sent in any order; however, it is recommended that the total number of Next Pages sent be kept small to minimize the link startup time.

Next Page transmission ends when both ends of a link segment set their Next Page bits to logic zero, indicating that neither has anything additional to transmit. It is possible for one device to have more pages to transmit than the other device. Once a device has completed transmission of its Next Page information, it

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shall transmit Message Pages, or extended Message Pages, with Null message codes and the NP bit set to logic zero while its Link Partner continues to transmit valid Next Pages. An Auto-Negotiation able device shall recognize reception of Message Pages, or extended Message Pages, with Null message codes as the end of its Link Partner's Next Page information.

28.2.3.4.1 Next Page encodings

The Next Page shall use the encoding shown in Figure 28–11 and Figure 28–12 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10–D0 shall be encoded as a Message Code Field if the MP bit is logic one and an Unformatted Code Field if MP is set to logic zero.

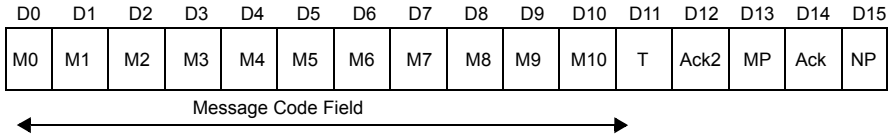


Figure 28–11—Message Page encoding

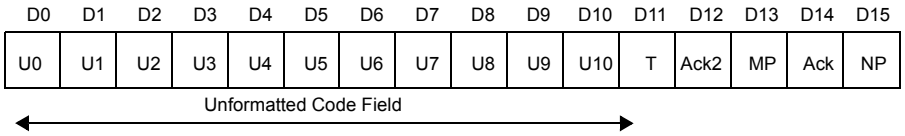


Figure 28–12—Unformatted Page encoding

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28.2.3.4.2 Extended Next Page encodings

Extended Next Pages shall use the encoding shown in Figure 28–13 and Figure 28–14 for the NP, Ack, MP, Ack2, and T bits. The 11-bit field D10:D0 shall be encoded as a Message Code Field if the MP is a logic one and an Unformatted Code Field if the MP bit is set to logic zero.

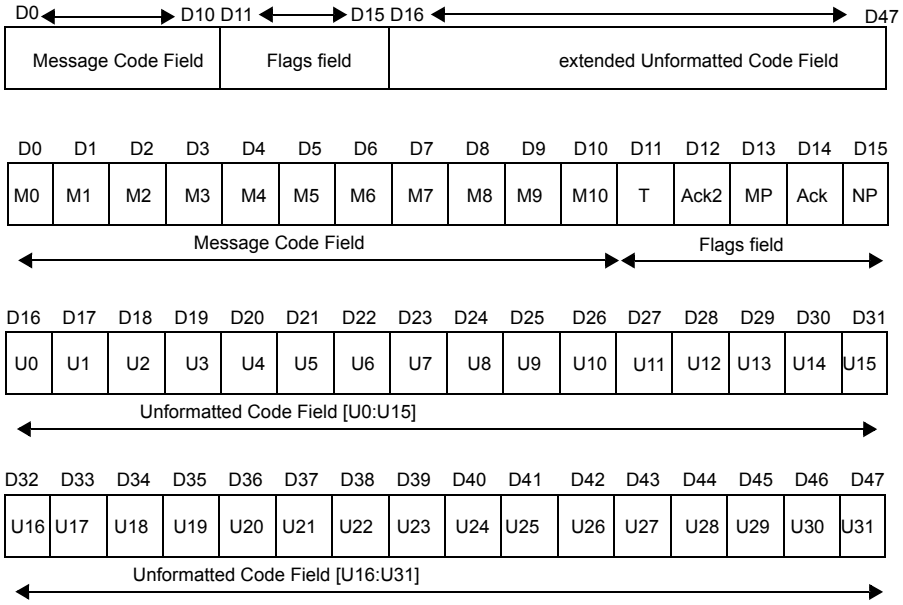


Figure 28–13—Extended Message Page encoding

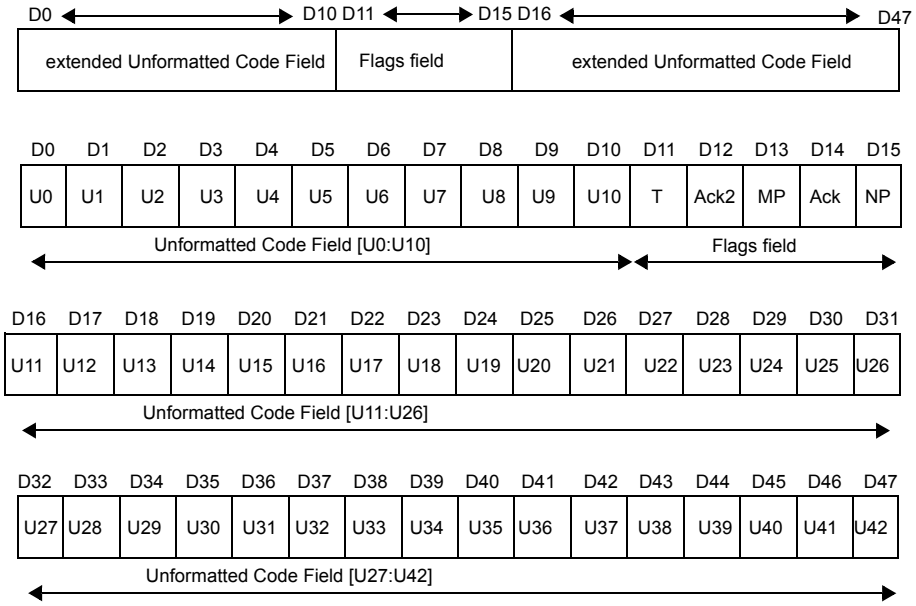


Figure 28–14—Extended Unformatted Page encoding

28.2.3.4.3 Next Page

Next Page (NP) is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. NP shall be set as follows:

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logic zero = last page.
logic one = additional Next Page(s) will follow.

28.2.3.4.4 Acknowledge

As defined in 28.2.1.2.5.

28.2.3.4.5 Message Page

Message Page (MP) is used by the Next Page function to differentiate a Message Page from an Unformatted Page. MP shall be set as follows:

logic zero = Unformatted Page.
logic one = Message Page.

28.2.3.4.6 Acknowledge 2

Acknowledge 2 (Ack2) is used by the Next Page function to indicate that a device has the ability to comply with the message. Ack2 shall be set as follows:

logic zero = cannot comply with message.
logic one = will comply with message.

28.2.3.4.7 Toggle

Toggle (T) is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged link codeword. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base link codeword and, therefore, may assume a value of logic one or zero. The Toggle bit shall be set as follows:

logic zero = previous value of the transmitted link codeword equalled logic one.
logic one = previous value of the transmitted link codeword equalled logic zero.

28.2.3.4.8 Message Page encoding

Message Pages are formatted pages that carry a single predefined message code, which is enumerated in Annex 28C. Two-thousand and forty-eight message codes are available. The allocation of these codes will be controlled by the contents of Annex 28C. If the Message Page bit is set to logic one, then the bit encoding of the link codeword shall be interpreted as a Message Page.

28.2.3.4.9 Message Code Field

Message Code Field (M[10:0]) is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are shown in Annex 28C. Combinations not specified are reserved for future use. Reserved combinations of the Message Code Field shall not be transmitted.

28.2.3.4.10 Unformatted Page encoding

Unformatted Pages carry the messages indicated by Message Pages. Five control bits are predefined, the remaining 11 bits may take on an arbitrary value. If the Message Page bit is set to logic zero, then the bit encoding of the link codeword shall be interpreted as an Unformatted Page.

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28.2.3.4.11 Unformatted Code Field

Unformatted Code Field (U[10:0]) is an eleven bit wide field, which may contain an arbitrary value.

28.2.3.4.12 Extended Unformatted Code Field

The extended Unformatted Code Field is a 32-bit or 43-bit wide field, which may contain an arbitrary value. The field is 32 bits wide in an extended Message Page and 43 bits wide in an extended Unformatted Page.

28.2.3.4.13 Use of Next Pages

a) Both devices must indicate Next Page ability for either to commence exchange of Next Pages.
b) Both devices must indicate Extended Next Page ability for either to commence exchange of Extended Next Pages.
c) If both devices are Next Page able, then both devices shall send at least one Next Page.
d) If both devices are Extended Next Page able, then both devices only transmit Extended Next Pages.
e) Next Page exchange shall continue until neither device on a link has more pages to transmit as indicated by the NP bit. A Message Page with a Null Message Code Field value shall be sent if the device has no other information to transmit.
f) A message code can carry either a specific message or information that defines how following Unformatted Page(s) should be interpreted.
g) If a message code references Unformatted Pages, the Unformatted Pages shall immediately follow the referencing message code in the order specified by the message code.
h) Unformatted Page users are responsible for controlling the format and sequencing for their Unformatted Pages.
i) An Extended Next Page provides a message code and extended Unformatted Code Field. The Message Code Field can carry either a specific message or information that defines how the following extended Unformatted Code Field should be interpreted.

28.2.3.4.14 MII register requirements

The Next Page Transmit register defined in 28.2.4.1.6 shall hold the Next Page to be sent by Auto-Negotiation. Received Next Pages may be stored in the Auto-Negotiation Link Partner ability register.

28.2.3.5 Remote fault sensing function

The Remote Fault function may indicate to the Link Partner that a fault condition has occurred using the Remote Fault bit and, optionally, the Next Page function.

Sensing of faults in a device as well as subsequent association of faults with the Remote Fault bit shall be optional. If the Local Device has no mechanism to detect a fault or associate a fault condition with the received Remote Fault bit indication, then it shall transmit the Remote Fault bit with the value contained in the Auto-Negotiation advertisement register bit (4.13).

A Local Device may indicate it has sensed a fault to its Link Partner by setting the Remote Fault bit in the Auto-Negotiation advertisement register and renegotiating.

If the Local Device sets the Remote Fault bit to logic one, it may also use the Next Page function to specify information about the fault that has occurred. Remote Fault Message Page Codes have been specified for this purpose.

The Remote Fault bit shall remain set until after successful negotiation with the base link codeword, at which time the Remote Fault bit shall be reset to a logic zero. On receipt of a base link codeword with the

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Remote Fault bit set to logic one, the device shall set the Remote Fault bit in the MII status register (1.4) to logic one if the MII management function is present.

28.2.4 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. Where no physical embodiment of the MII exists, an equivalent to MII Registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.

28.2.4.1 Media Independent Interface

The Auto-Negotiation function shall have five dedicated registers:

a) MII control register (Register 0).
b) MII status register (Register 1).
c) Auto-Negotiation advertisement register (Register 4).
d) Auto-Negotiation Link Partner ability register (Register 5).
e) Auto-Negotiation expansion register (Register 6).

If the Next Page function is implemented, the Auto-Negotiation Next Page transmit register (Register 7) shall be implemented.

28.2.4.1.1 MII control register

MII control register (Register 0) provides the mechanism to disable/enable and/or restart Auto-Negotiation. The definition for this register is provided in 22.2.4.1.

The Auto-Negotiation function shall be enabled by setting bit 0.12 to a logic one. If bit 0.12 is set to a logic one, then bits 0.13 and 0.8 shall have no effect on the link configuration, and the Auto-Negotiation process will determine the link configuration. If bit 0.12 is cleared to logic zero, then bits 0.13 and 0.8 will determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

A PHY shall return a value of one in bit 0.9 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process shall be initiated by setting bit 0.9 to a logic one. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitiated. If a PHY reports via bit 1.3 that it lacks the ability to perform Auto-Negotiation, then this bit will have no meaning, and should be written as zero. This bit is self-clearing. The Auto-Negotiation process shall not be affected by clearing this bit to logic zero.

28.2.4.1.2 MII status register

The MII status register (Register 1) includes information about all modes of operations supported by the Local Device's PHY, the status of Auto-Negotiation, and whether the Auto-Negotiation function is supported by the PHY or not. The definition for this register is provided in 22.2.4.2.

When read as a logic one, bit 1.5 indicates that the Auto-Negotiation process has been completed, and that the contents of Registers 4, 5, and 6 are valid. When read as a logic zero, bit 1.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of Registers 4, 5, and 6 are meaningless. A PHY shall return a value of zero in bit 1.5 if Auto-Negotiation is disabled by clearing bit 0.12. A PHY shall also return a value of zero in bit 1.5 if it lacks the ability to perform Auto-Negotiation.

When read as logic one, bit 1.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The Remote Fault bit shall be

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implemented with a latching function, such that the occurrence of a remote fault will cause the Remote Fault bit to become set and remain set until it is cleared. The Remote Fault bit shall be cleared each time Register 1 is read via the management interface, and shall also be cleared by a PHY reset.

When read as a one, bit 1.3 indicates that the PHY has the ability to perform Auto-Negotiation. When read as a logic zero, bit 1.3 indicates that the PHY lacks the ability to perform Auto-Negotiation.

28.2.4.1.3 Auto-Negotiation advertisement register (Register 4) (R/W)

This register contains the Advertised Ability of the PHY. (See Table 28–2). The bit definition for the Base Page is defined in 28.2.1.2. On power-up, before Auto-Negotiation starts, this register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4.11:5) is set based on the values set in the MII status register (Register 1) (1.15:11) or equivalent. See also 28.2.1.2.3 and Annex 28D.

Table 28–2—Advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
4.15	Next Page	See 28.2.1.2	R/W
4.14	Reserved	Write as zero, ignore on read	RO
4.13	Remote Fault	See 28.2.1.2	R/W
4.12	Extended Next Page	See 28.2.1.2	R/W
4.11:5	Technology Ability Field	See 28.2.1.2	R/W
4.4:0	Selector Field	See 28.2.1.2	R/W

[a]RO = Read only, R/W = Read/Write.

Only the bits in the Technology Ability Field that represent the technologies supported by the Local Device may be set. Any of the Technology Ability Field bits that may be set can also be cleared by management before a renegotiation. This can be used to enable management to Auto-Negotiate to an alternate common mode.

The management entity may initiate renegotiation with the Link Partner using alternate abilities by setting the Selector Field (4.4:0) and Technology Ability Field (4.11:5) to indicate the preferred mode of operation and setting the Restart Auto-Negotiation bit (0.9) in the control register (Register 0) to logic one.

Any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a renegotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be examined by software to determine the highest common denominator technology.

28.2.4.1.4 Auto-Negotiation Link Partner ability register (Register 5) (RO)

All of the bits in the Auto-Negotiation Link Partner ability register are read only. A write to the Auto-Negotiation Link Partner ability register shall have no effect.

This register contains the Advertised Ability of the Link Partner's PHY. (See Tables 28–3 and 28–4.) The bit definitions shall be a direct representation of the received link codeword (Figure 28–7). Upon successful completion of Auto-Negotiation, status register (Register 1) Auto-Negotiation Complete bit (1.5) shall be set

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to logic one. If the Next Page function is supported and bit (6.6) in the Auto-Negotiation expansion register (Register 6) is set to logic zero, then the Auto-Negotiation Link Partner ability register may be used to store Link Partner Next Pages. If bit (6.6) in the Auto-Negotiation expansion register (Register 6) is set to logic one, then bit (6.5) determines where the Link Partner Next Pages are stored.

Table 28–3—Link partner ability register bit definitions (Base Page)

Bit(s)	Name	Description	R/W[a]
5.15	Next Page	See 28.2.1.2	RO
5.14	Acknowledge	See 28.2.1.2	RO
5.13	Remote Fault	See 28.2.1.2	RO
5.12	Extended Next Page	See 28.2.1.2	RO
5.11:5	Technology Ability Field	See 28.2.1.2	RO
5.4:0	Selector Field	See 28.2.1.2	RO

[a]RO = Read only.

Table 28–4—Link partner ability register bit definitions (Next Page)

Bit(s)	Name	Description	R/W[a]
5.15	Next Page	See 28.2.3.4	RO
5.14	Acknowledge	See 28.2.3.4	RO
5.13	Message Page	See 28.2.3.4	RO
5.12	Acknowledge 2	See 28.2.3.4	RO
5.11	Toggle	See 28.2.3.4	RO
5.10:0	Message/Unformatted Code Field	See 28.2.3.4	RO

[a]RO = Read only.

The values contained in this register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 1.5 or, if used with Next Page exchange, after the Page Received bit (6.1) has been set to logic one.

NOTE—If this register is used to store Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

28.2.4.1.5 Auto-Negotiation expansion register (Register 6) (RO)

All of the bits in the Auto-Negotiation expansion register are read only; a write to the Auto-Negotiation expansion register shall have no effect. (See Table 28–5.)

Bits 6.15:7 are reserved for future Auto-Negotiation expansion.

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Table 28–5—Expansion register bit definitions

Bit(s)	Name	Description	R/W[a]	Default
6.15:7	Reserved	Write as zero, ignore on read	RO	0
6.6	Receive Next Page Location Able	1 = Received Next Page storage location is specified by bit (6.5) 0 = Received Next Page storage location is not specified by bit (6.5)	RO	—
6.5	Received Next Page Storage Location	1 = Link Partner Next Pages are stored in Register 8 0 = Link Partner Next Pages are stored in Register 5	RO	—
6.4	Parallel Detection Fault	1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected via the Parallel Detection function.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able	RO	0
6.2	Next Page Able	1 = Local Device is Next Page able 0 = Local Device is not Next Page able	RO	0
6.1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO/ LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able	RO	0

[a]RO = Read only, LH = Latching high.

The Receive Next Page Location Able bit (6.6) shall be set to logic one to indicate that the Link Partner Next Page Storage Location bit (6.5) is supported.

The Receive Next Page Storage Location bit (6.5) shall be set to logic one to indicate that the Link Partner's Next Pages are stored in the Auto-Negotiation Link Partner Received Next Page register (Register 8). This bit shall be set to logic zero to indicate that the Link Partner’s Next Pages are stored in the Auto-Negotiation Link Partner ability register (Register 5). It is recommended that all new implementations store the Link Partner’s Next Pages in the Auto-Negotiation Link Partner Received Next Page ability register (Register 8).

NOTE— It is highly recommended that the Link Partner Next Page Storage Location bit (6.5) is supported. If this bit is not supported there is no indication if the Link Partners Next Page is stored in register 5 or register 8.

The Parallel Detection Fault bit (6.4) shall be set to logic one to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires. The Parallel Detection Fault bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

The Link Partner Next Page Able bit (6.3) shall be set to logic one to indicate that the Link Partner supports the Next Page function. This bit shall be reset to logic zero to indicate that the Link Partner does not support the Next Page function.

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The Next Page Able bit (6.2) shall be set to logic one to indicate that the Local Device supports the Next Page function. The Next Page Able bit (6.2) shall be set to logic zero if the Next Page function is not supported.

The Page Received bit (6.1) shall be set to logic one to indicate that a new link codeword has been received and stored in the Auto-Negotiation Link Partner ability register. The Page Received bit shall be reset to logic zero on a read of the Auto-Negotiation expansion register (Register 6).

The Link Partner Auto-Negotiation Able bit (6.0) shall be set to logic one to indicate that the Link Partner is able to participate in the Auto-Negotiation function. This bit shall be reset to logic zero if the Link Partner is not Auto-Negotiation able.

28.2.4.1.6 Auto-Negotiation Next Page transmit register (Register 7) (R/W)

The Auto-Negotiation Next Page Transmit register contains the Next Page link codeword to be transmitted when Next Page ability is supported. (See Table 28–6.) The contents are defined in 28.2.3.4. On power-up, this register shall contain the default value of 2001H, which represents a Message Page with the message code set to Null Message. This value may be replaced by any valid Next Page message code that the device wishes to transmit. Writing to this register shall set mr_next_page_loaded to true.

Table 28–6—Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
7.15	Next Page	See 28.2.3.4	R/W
7.14	Reserved	Write as 0, ignore on read	RO
7.13	Message Page	See 28.2.3.4	R/W
7.12	Acknowledge 2	See 28.2.3.4	R/W
7.11	Toggle	See 28.2.3.4	RO
7.10:0	Message/Unformatted Code field	See 28.2.3.4	R/W

[a]RO = Read only, R/W = Read/Write.

28.2.4.1.7 Auto-Negotiation Link Partner Received Next Page register (Register 8) (RO)

Support for 100BASE-T2 and 1000BASE-T requires support for Next Page and the provision of an Auto-Negotiation Link Partner Received Next Page register (register 8) to store Link Partner Next Pages as shown in Table 28–7. All of the bits in the Auto-Negotiation Link Partner Received Next Page register are read only. A write to the Auto-Negotiation Link Partner Received Next Page register shall have no effect.

The values contained in this register are only guaranteed to be valid after the Page Received bit (6.1) has been set to logical one or once Auto-Negotiation has successfully completed, as indicated by bit 1.5.

NOTE—If this register is used to store multiple Link Partner Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent Link Partner Next Pages.

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Table 28–7—Link Partner Received Next Page register bit definitions

Bit(s)	Name	Description	R/W[a]
8.15	Next Page	see 28.2.3.4	RO
8.14	Acknowledge	see 28.2.3.4	RO
8.13	Message Page	see 28.2.3.4	RO
8.12	Acknowledge 2	see 28.2.3.4	RO
8.11	Toggle	see 28.2.3.4	RO
8.10:0	Message/Unformatted Code Field	see 28.2.3.4	RO

[a]RO = Read only.

28.2.4.1.8 State diagram variable to MII register mapping

The state diagrams of Figures 28–16 to 28–19 generate and accept variables of the form "mr_x," where x is an individual signal name. These variables comprise a management interface that may be connected to the MII management function or other equivalent function. Table 28–8 describes how the MII registers map to the management function interface signals.

Table 28–8—State diagram variable to MII register mapping

State diagram variable	MII register	MDIO register
mr_adv_ability[16:1]	4.15:0 Auto-Negotiation advertisement register	7.16.15:0 AN advertisement register
mr_autoneg_complete	1.5 Auto-Negotiation Complete	7.1.5 Auto-Negotiation Complete
mr_autoneg_enable	0.12 Auto-Negotiation Enable	7.0.12 Auto-Negotiation Enable
mr_lp_adv_ability[16:1]	For Base Page: 5.15:0 Auto-Negotiation link partner ability register For Next Page(s): If 6.6=1 and 6.5=1 then 8.15:0 is Auto-Negotiation link partner Received Next Page register If 6.6=1 and 6.5= 0 then 5.15:0 is Auto-Negotiation link partner ability register If 6.6=0 then 8.15:0 or 5.15:0 is Auto-Negotiation link partner Next Page ability register	7.19.15:0 AN LP Base Page ability register
mr_lp_autoneg_able	6.0 Link Partner Auto-Negotiation able	
mr_lp_np_able	6.3 Link Partner Next Page able	
mr_main_reset	0.15 Reset	7.0.15 Reset
mr_next_page_loaded	Set on write to Auto-Negotiation Next Page Transmit register; cleared by Arbitration state diagram	
mr_np_able	6.2 Next Page able	

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Table 28–8—State diagram variable to MII register mapping *(continued)*

State diagram variable	MII register	MDIO register
mr_np_tx[16:1]	7.15:0 Auto-Negotiation Next Page Transmit Register	7.22.15:0 AN XNP transmit register
mr_np_tx[32:17]	Extended Next Pages not supported by MII register interface	7.23.15:0 Unformatted Code Field 1
mr_np_tx[48:33]	Extended Next Pages not supported by MII register interface	7.24.15:0 Unformatted Code Field 2
mr_page_rx	6.1 Page Received	7.1.6 Page Received
mr_parallel_detection_fault	6.4 Parallel Detection Fault	
mr_restart_negotiation	0.9 Auto-Negotiation Restart	7.0.9 Auto-Negotiation Restart
set if Auto-Negotiation is available	1.3 Auto-Negotiation Ability	7.1.3 Auto-Negotiation Ability

28.2.4.2 Auto-Negotiation managed object class

The Auto-Negotiation Managed Object Class is defined in Clause 30.

28.2.5 Absence of management function

In the absence of any management function, the advertised abilities shall be provided through a logical equivalent of mr_adv_ability[16:1]. A device shall comply with all Next Page function requirements, including the provision of the mr_np_able, mr_lp_np_able, and mr_next_page_loaded variables (or their logical equivalents), in order to permit the NP bit to be set to logic one in the transmitted link codeword.

NOTE—Storage of a valid base link codeword is required to prevent a deadlock situation where negotiation must start again while Next Pages are being transmitted. If a shared transmit register were used, then renegotiation could not occur when Next Pages were being transmitted because the base link codeword would not be available. This requirement can be met using a number of different implementations, including use of temporary registers or register stacks.

28.2.6 Technology-Dependent Interface

The Technology-Dependent Interface is the communication mechanism between each technology's PMA and the Auto-Negotiation function. Auto-Negotiation can support multiple technologies, all of which need not be implemented in a given device. Each of these technologies may utilize its own technology-dependent link integrity test function.

28.2.6.1 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium. The purpose of this primitive is to give the PCS, repeater client, or Auto-Negotiation function a means of determining the validity of received code elements.

28.2.6.1.1 Semantics of the service primitive

PMA_LINK.indication(link_status)

The link_status parameter shall assume one of three values: READY, OK, or FAIL, indicating whether the underlying receive channel is intact and ready to be enabled (READY), intact and enabled (OK), or not

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intact (FAIL). When link_status=FAIL or link_status=READY, the PMA_CARRIER.indication and PMA_UNITDATA.indication primitives are undefined.

28.2.6.1.2 When generated

A technology-dependent PMA and the NLP Receive Link Integrity Test state diagram (Figure 28–19) shall generate this primitive to indicate the value of link_status.

28.2.6.1.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the state diagrams of Figure 28–18.

28.2.6.2 PMA_LINK.request

This primitive is generated by Auto-Negotiation to allow it to enable and disable operation of the PMA.

28.2.6.2.1 Semantics of the service primitive

PMA_LINK.request(link_control)

The link_control parameter shall assume one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

The link_control=SCAN_FOR_CARRIER mode is used by the Auto-Negotiation function prior to receiving any FLP Bursts or link_status=READY indications. During this mode, the PMA shall search for carrier and report link_status=READY when carrier is received, but no other actions shall be enabled.

The link_control=DISABLE mode shall be used by the Auto-Negotiation function to disable PMA processing.

The link_control=ENABLE mode shall be used by Auto-Negotiation to turn control over to a single PMA for all normal processing functions.

28.2.6.2.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagrams of Figure 28–17 and Figure 28–18.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINK.request(DISABLE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINK.request(link_control) is implementation dependent.

28.2.6.2.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the NLP Receive Link Integrity Test state diagram (Figure 28–19) and the receiving technology-dependent link integrity test function, based on the intent specified in the primitive semantics.

28.2.6.3 PMA_LINKPULSE.request

This primitive is generated by Auto-Negotiation to indicate that a valid Link Pulse, as transmitted in compliance with Figure 14–13, has been received.

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28.2.6.3.1 Semantics of the service primitive

PMA_LINKPULSE.request (linkpulse)

The linkpulse parameter shall assume one of two values: TRUE or FALSE.

The linkpulse=FALSE mode shall be used by the Auto-Negotiation function to indicate that the Receive state diagram has performed a state transition.

The linkpulse=TRUE mode shall be used by the Auto-Negotiation function to indicate that a valid Link Pulse has been received.

28.2.6.3.2 When generated

The Auto-Negotiation function shall generate this primitive to indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–17.

Upon power-on or reset, if the Auto-Negotiation function is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request (FALSE) message shall be issued to all technology-dependent PMAs. If Auto-Negotiation is disabled at any time including at power-on or reset, the state of PMA_LINKPULSE.request (linkpulse) is implementation dependent.

28.2.6.3.3 Effect of receipt

The effect of receipt of this primitive shall be governed by the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.3 State diagrams and variable definitions

The notation used in the state diagrams (Figure 28–16 to Figure 28–19) follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set. Variables using the “mr_x” notation do not have state diagram defaults; however, their appropriate initialization conditions when mapped to the MII interface are covered in 28.2.4 and 22.2.4, and Clause 45 MDIO management interface. The variables, timers, and counters used in the state diagrams are defined in 28.3, 14.2.3, and 28.2.6.

Auto-Negotiation shall implement the Transmit state diagram, Receive state diagram, Arbitration state diagram, and NLP Receive Link Integrity Test state diagram as depicted in 28.3. Additional requirements to these state diagrams are made in the respective functional requirements sections. Options to these state diagrams clearly stated as such in the functional requirements sections or state diagrams shall be allowed. In the case of any ambiguity between stated requirements and the state diagrams, the state diagrams shall take precedence.

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The functional reference diagram (Figure 28–15) provides a generic example, illustrated with initial PMA implementations and showing the mechanism for expansion. New PMAs are documented in Annex 28D.

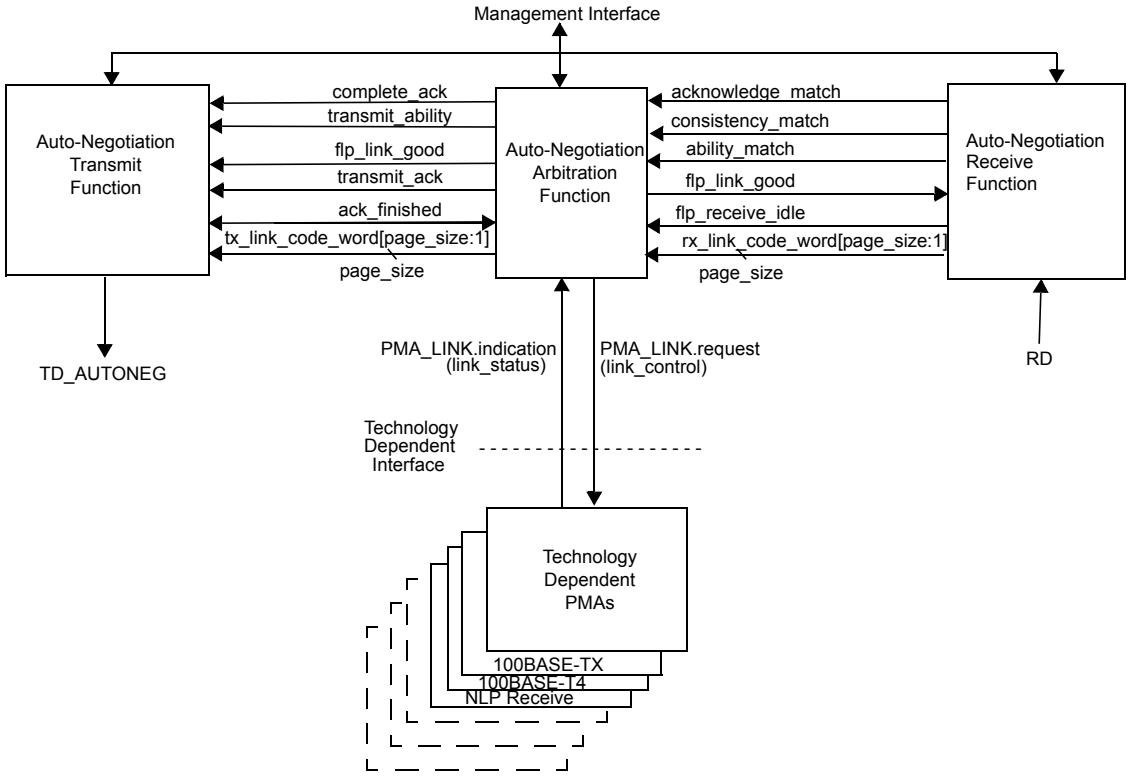


Figure 28–15—Functional reference diagram

28.3.1 State diagram variables

A variable with "_[x]" appended to the end of the variable name indicates a variable or set of variables as defined by "x". "x" may be as follows:

all;	represents all specific technology-dependent PMAs supported in the Local Device and the NLP Receive Link Integrity Test state diagram.
1GigT;	represents that the 1000BASE-T PMA is the signal source.
10GigT;	represents that the 10GBASE-T PMA is the signal source.
HCD;	represents the single technology-dependent PMA chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function. To select 10BASE-T, LIT is used instead of NLP to enable the full 10BASE-T Link Integrity Test function state diagram.
notHCD;	represents all technology-dependent PMAs not chosen by Auto-Negotiation as the highest common denominator technology through the Priority Resolution or Parallel Detection function.
TX;	represents that the 100BASE-TX PMA is the signal source.
T4;	represents that the 100BASE-T4 PMA is the signal source.
NLP;	represents that the NLP Receive Link Integrity Test function is the signal source.
PD;	represents all of the following that are present: 100BASE-TX PMA, 100BASE-T4 PMA, and the NLP Receive Link Integrity Test state diagram.
LIT;	represents the 10BASE-T Link Integrity Test function state diagram is the signal source or

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destination.

Variables with [16:1] appended to the end of the variable name indicate arrays that can be directly mapped to 16-bit registers. For these variables, "[x]" indexes an element or set of elements in the array, where "[x]" may be as follows:

— Any integer.
— Any variable that takes on integer values.
— NP; represents the index of the Next Page bit.
— ACK; represents the index of the Acknowledge bit.
— RF; represents the index of the Remote Fault bit.

Variables of the form "mr_x", where x is a label, comprise a management interface that is intended to be connected to the MII Management function. However, an implementation-specific management interface may provide the control and status function of these bits.

ability_match

Indicates that three consecutive link codewords match, ignoring the Acknowledge bit. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word-match comparison or not.

Values: false; three matching consecutive link codewords have not been received, ignoring the Acknowledge bit (default).
true; three matching consecutive link codewords have been received, ignoring the Acknowledge bit.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

ability_match_word [16:1]

A 16-bit array that contains the last link codeword that caused ability_match = true. For each element in the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

ack_finished

Status indicating that the final remaining_ack_cnt link codewords with the Ack bit set have been transmitted.

Values: false; more link codewords with the Ack bit set to logic one must be transmitted.
true; all remaining link codewords with the Ack bit set to logic one have been transmitted.

acknowledge_match

Indicates that three consecutive link codewords match and have the Acknowledge bit set. Three consecutive words are any three words received one after the other, regardless of whether the word has already been used in a word match comparison or not.

Values: false; three matching and consecutive link codewords have not been received with the Acknowledge bit set (default).
true; three matching and consecutive link codewords have been received with the Acknowledge bit set.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

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base_page

Status indicating that the page currently being transmitted by Auto-Negotiation is the initial link codeword encoding used to communicate the device's abilities.

Values: false; a page other than base link codeword is being transmitted.
true; the base link codeword is being transmitted.

complete_ack

Controls the counting of transmitted link codewords that have their Acknowledge bit set.

Values: false; transmitted link codewords with the Acknowledge bit set are not counted (default).
true; transmitted link codewords with the Acknowledge bit set are counted.

consistency_match

Indicates that the link codeword that caused ability_match to be set is the same as the link codeword that caused acknowledge_match to be set.

Values: false; the link codeword that caused ability_match to be set is not the same as the link codeword that caused acknowledge_match to be set, ignoring the Acknowledge bit value.
true; the link codeword that caused ability_match to be set is the same as the link codeword that caused acknowledge_match to be set, independent of the Acknowledge bit value.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

desire_np

Status indicating that the Local Device desires to engage in Next Page exchange. This information comes from the setting of the NP bit in the base link codeword stored in the Auto-Negotiation advertisement register (Register 4).

Values: false; Next page exchange is not desired.
true; Next page exchange is desired.

flp_link_good

Indicates that Auto-Negotiation has completed.

Values: false; negotiation is in progress (default).
true; negotiation is complete, forcing the Transmit and Receive functions to IDLE.

flp_receive_idle

Indicates that the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

Values: false; the Receive state diagram is not in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state (default).
true; the Receive state diagram is in the IDLE, LINK PULSE DETECT, or LINK PULSE COUNT state.

incompatible_link

Parameter used following Priority Resolution to indicate the resolved link is incompatible with the Local Device settings. A device's ability to set this variable to true is optional.

Values: false; A compatible link exists between the Local Device and Link Partner (default).
true; Optional indication that Priority Resolution has determined no highest common denominator exists following the most recent negotiation.

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NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

link_control

This variable is defined in 28.2.6.2.1.

link_status

This variable is defined in 28.2.6.1.1.

linkpulse

This variable is defined in 28.2.6.3.1.

Values: false; linkpulse is set to false after any Receive State Diagram state transition (default).
true; linkpulse is set to true when a valid Link Pulse is received.

mr_autoneg_complete

Status indicating whether Auto-Negotiation has completed or not.

Values: false; Auto-Negotiation has not completed.
true; Auto-Negotiation has completed.

mr_autoneg_enable

Controls the enabling and disabling of the Auto-Negotiation function.

Values: false; Auto-Negotiation is disabled.
true; Auto-Negotiation is enabled.

mr_adv_ability[16:1]

A 16-bit array that contains the Advertised Abilities link codeword.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_adv_ability[16:1]

A 16-bit array that contains the Link Partner's Advertised Abilities link codeword.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_lp_np_able

Status indicating whether the Link Partner supports Next Page exchange.

Values: false; the Link Partner does not support Next Page exchange.
true; the Link Partner supports Next Page exchange.

mr_np_able

Status indicating whether the Local Device supports Next Page exchange.

Values: false; the Local Device does not support Next Page exchange.
true; the Local Device supports Next Page exchange.

mr_lp_autoneg_able

Status indicating whether the Link Partner supports Auto-Negotiation.

Values: false; the Link Partner does not support Auto-Negotiation.
true; the Link Partner supports Auto-Negotiation.

mr_main_reset

Controls the resetting of the Auto-Negotiation state diagrams.

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Values: false; do not reset the Auto-Negotiation state diagrams.
true; reset the Auto-Negotiation state diagrams.

mr_next_page_loaded

Status indicating whether a new page has been loaded into the Auto-Negotiation Next Page Transmit register (Register 7).

Values: false; a New Page has not been loaded.
true; a New Page has been loaded.

mr_np_tx[page_size:1]

A 16-bit or 48-bit array that contains the new Next Page to transmit.
For each element within the array:

Values: zero; data bit is logical zero.
one; data bit is logical one.

mr_page_rx

Status indicating whether a New Page has been received. A New Page has been successfully received when acknowledge_match=true and consistency_match=true and the link codeword has been written to mr_lp_adv_ability[16:1].

Values: false; a New Page has not been received.
true; a New Page has been received.

mr_parallel_detection_fault

Error condition indicating that while performing Parallel Detection, either flp_receive_idle = false, or zero or more than one of the following indications were present when the autoneg_wait_timer expired. This signal is cleared on read of the Auto-Negotiation expansion register.

1) link_status_ [NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; exactly one of the above three indications was true when the autoneg_wait_timer expired, and flp_receive_idle = true.
true; either zero or more than one of the above three indications was true when the autoneg_wait_timer expired, or flp_receive_idle = false.

mr_restart_negotiation

Controls the entrance to the TRANSMIT DISABLE state to break the link before Auto-Negotiation is allowed to renegotiate via management control.

Values: false; renegotiation is not taking place.
true; renegotiation is started.

np_rx

Flag to hold the value of rx_link_code_word[NP] upon entry to the COMPLETE ACKNOWLEDGE state. This value is associated with the value of rx_link_code_word[NP] when acknowledge_match was last set.

Values zero; local device np_rx bit equals a logical zero.
one; local device np_rx bit equals a logical one.

page_size

Status indicating the size of Next Page that the device is prepared to transmit and receive.

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Values: 16; the device does not support Extended Next Pages or Extended Next Page ability has not been enabled.
48; Extended Next Page ability is supported and has been enabled.

NOTE— This variable is set by this variable definition; it is not set explicitly in the state diagrams. The variable takes on the value of 16 upon entry into the TRANSMIT DISABLE state and is updated upon entry into the NEXT PAGE WAIT state.

power_on

Condition that is true until such time as the power supply for the device that contains the Auto-Negotiation state diagrams has reached the operating region or the device has low power mode set via MII control register bit 0.11.

Values: false; the device is completely powered (default).
true; the device has not been completely powered.

rx_link_code_word[page_size:1]

A 16-bit or 48-bit array that contains the data bits to be received from an FLP Burst.
For each element within the array:

Values: zero; data bit is a logical zero.
one; data bit is a logical one.

single_link_ready

Status indicating that flp_receive_idle = true and only one the of the following indications is being received:

1) link_status_[NLP] = READY
2) link_status_[TX] = READY
3) link_status_[T4] = READY

Values: false; either zero or more than one of the above three indications are true or flp_receive_idle = false.
true; Exactly one of the above three indications is true and flp_receive_idle = true.

NOTE—This variable is set by this variable definition; it is not set explicitly in the state diagrams.

TD_AUTONEG

Controls the signal sent by Auto-Negotiation on the TD_AUTONEG circuit.

Values: idle; Auto-Negotiation prevents transmission of all link pulses on the MDI.
link_test_pulse; Auto-Negotiation causes a single link pulse as defined by Figure 14–13 to be transmitted on the MDI.

toggle_rx

Flag to keep track of the state of the Link Partner's Toggle bit.

Values: 0; Link Partner's Toggle bit equals logic zero.
1; Link Partner's Toggle bit equals logic one.

toggle_tx

Flag to keep track of the state of the Local Device's Toggle bit.

Values: 0; Local Device's Toggle bit equals logic zero.
1; Local Device's Toggle bit equals logic one.

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transmit_ability

Controls the transmission of the link codeword containing tx_link_code_word[page_size:1].

Values: false; any transmission of tx_link_code_word[page_size:1] is halted (default).
true; the transmit state diagram begins sending tx_link_code_word[page_size:1].

transmit_ack

Controls the setting of the Acknowledge bit in the tx_link_code_word[page_size:1] to be transmitted.

Values: false; sets the Acknowledge bit in the transmitted tx_link_code_word[page_size:1] to a logic zero (default).
true; sets the Acknowledge bit in the transmitted tx_link_code_word[page_size:1] to a logic one.

transmit_disable

Controls the transmission of tx_link_code_word[page_size:1].

Values: false; tx_link_code_word[page_size:1] transmission is allowed (default).
true; tx_link_code_word[page_size:1] transmission is halted.

tx_link_code_word[page_size:1]

A 16-bit or 48-bit array that contains the data bits to be transmitted in an FLP Burst. This array may be loaded from mr_adv_ability or mr_np_tx.
For each element within the array:

Values: Zero; data bit is logical zero.
One; data bit is logical one.

28.3.2 State diagram timers

All timers operate in the manner described in 14.2.3.2.

autoneg_wait_timer

Timer for the amount of time to wait before evaluating the number of link integrity test functions with link_status=READY asserted. The autoneg_wait_timer shall expire 500 ms to 1000 ms from the assertion of link_status=READY from the 100BASE-TX PMA, 100BASE-T4 PMA, or the NLP Receive State diagram.

break_link_timer

Timer for the amount of time to wait in order to assure that the Link Partner enters a Link Fail state. The timer shall expire 1200 ms to1500 ms after being started.

data_detect_max_timer

Timer for the maximum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_min_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_max_timer shall expire 78 µs to 100 µs from the last clock pulse.

data_detect_min_timer

Timer for the minimum time between a clock pulse and the next link pulse. This timer is used in conjunction with the data_detect_max_timer to detect whether the data bit between two clock pulses is a logic zero or a logic one. The data_detect_min_timer shall expire 15 µs to 47 µs from the last clock pulse.

flp_test_max_timer

Timer for the maximum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_min_timer to detect whether the Link Partner is transmitting FLP

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Bursts. The flp_test_max_timer shall expire 165 µs to 185 µs from the last link pulse.

flp_test_min_timer
: Timer for the minimum time between two link pulses within an FLP Burst. This timer is used in conjunction with the flp_test_max_timer to detect whether the Link Partner is transmitting FLP Bursts. The flp_test_min_timer shall expire 5 µs to 25 µs from the last link pulse.

interval_timer
: Timer for the separation of a transmitted clock pulse from a data bit. The interval_timer shall expire 55.5 µs to 69.5 µs from each clock pulse and data bit.

link_fail_inhibit_timer
: Timer for qualifying a link_status=FAIL indication or a link_status=READY indication when a specific technology link is first being established. A link will only be considered "failed" if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The link_fail_inhibit_timer shall expire 750 ms to 1000 ms after entering the FLP LINK GOOD CHECK state for devices operating at 10/100/1000 Mb/s. The link_fail_inhibit_timer shall expire 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state for devices operating at 10 Gb/s.

  NOTE—The link_fail_inhibit_timer expiration value must be greater than the time required for the Link Partner to complete Auto-Negotiation after the Local Device has completed Auto-Negotiation plus the time required for the specific technology to enter the link_status=OK state. The maximum time difference between a Local Device and its Link Partner completing Auto-Negotiation is

  (Maximum FLP Burst to FLP Burst separation) × (Maximum number of FLP Bursts needed to complete acknowledgment) = (24 ms) × (8 bursts) = 192 ms.

  For example, 100BASE-T4 requires approximately 460 ms to enter link_status=OK for a total minimum link_fail_inhibit_timer time of 652 ms. The lower bound for the link_fail_inhibit_timer was chosen to provide adequate margin for the current technologies and any future PMAs.

nlp_test_max_timer
: Timer for the maximum time that no FLP Burst may be seen before forcing the receive state diagram to the IDLE state. The nlp_test_max_timer shall expire 50 ms to 150 ms after being started or restarted.

nlp_test_min_timer
: Timer for the minimum time between two consecutive FLP Bursts. The nlp_test_min_timer shall expire 5 ms to 7 ms after being started or restarted for devices that do not support Extended Next Pages, and shall expire 6.75 ms to 7.25 ms after being started or restarted for devices that do support Extended Next Pages.

transmit_link_burst_timer
: Timer for the separation of a transmitted FLP Burst from the next FLP Burst. The transmit_link_burst_timer shall expire 5.7 ms to 22.3 ms after the last transmitted link pulse in an FLP Burst when Extended Next Pages are not supported. When Extended Next Pages are supported, the timer shall expire 5.7 ms to 6.8 ms after the last transmitted link pulse when transmitting 16-bit pages, and shall expire 1.3 ms to 3.1 ms after the last transmitted pulse when transmitting 48-bit pages.

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Table 28–9—Timer min./max. value summary

Parameter	Min.	Typ.	Max.	Units
autoneg_wait_timer	500		1000	ms
break_link_timer	1200		1500	ms
data_detect_min_timer	15		47	µs
data_detect_max_timer	78		100	µs
flp_test_min_timer	5		25	µs
flp_test_max_timer	165		185	µs
interval_timer	55.5	62.5	69.5	µs
link_fail_inhibit_timer (10/100/1000 Mb/s devices)	750		1000	ms
link_fail_inhibit_timer (10 Gb/s devices)	2000		2250	ms
nlp_test_max_timer	50		150	ms
nlp_test_min_timer (no support of Extended Next Pages)	5		7	ms
nlp_test_min_timer (support of Extended Next Pages)	6.75		7.25	ms
transmit_link_burst_timer (no support of Extended Next Pages)	5.7	14	22.3	ms
transmit_link_burst_timer (support of Extended Next Pages when page_size is 16)	5.7	6.25	6.8	ms
transmit_link_burst_timer (support of Extended Next Pages when page_size is 48)	1.3	2.25	3.2	ms

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28.3.3 State diagram counters

flp_cnt

A counter that may take on integer values from 0 to 17. This counter is used to keep a count of the number of FLPs detected to enable the determination of whether the Link Partner supports Auto-Negotiation.

Values: not_done; 0 to 5 inclusive.
done; 6 to 17 inclusive.
init; counter is reset to zero.

remaining_ack_cnt

A counter that may take on integer values from 0 to 8. The number of additional link codewords with the Acknowledge Bit set to logic one to be sent to ensure that the Link Partner receives the acknowledgment.

Values: not_done; positive integers between 0 and 5 inclusive.
done; positive integers 6 to 8 inclusive (default).
init; counter is reset to zero.

rx_bit_cnt

A counter that may take on integer values from 0 to (page_size+1). This counter is used to keep a count of data bits received from an FLP Burst and to ensure that when erroneous extra pulses are received, the first page_size bits are kept while the rest are ignored. When this variable reaches page_size or (page_size+1), enough data bits have been received. This counter does not increment beyond (page_size+1) and does not return to 0 until it is reinitialized.

Values: not_done; 1 to (page_size–1) inclusive.
done; page_size or (page_size+1)
init; counter is reset to zero.
rx_bit_cnt_check; 10 to 17 inclusive.

tx_bit_cnt

A counter that may take on integer values from 1 to (page_size+1). This counter is used to keep a count of data bits sent within an FLP Burst. When this variable reaches (page_size+1), all data bits have been sent.

Values: not_done; 1 to page_size inclusive.
done; (page_size+1).
init; counter is initialized to 1.

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28.3.4 State diagrams

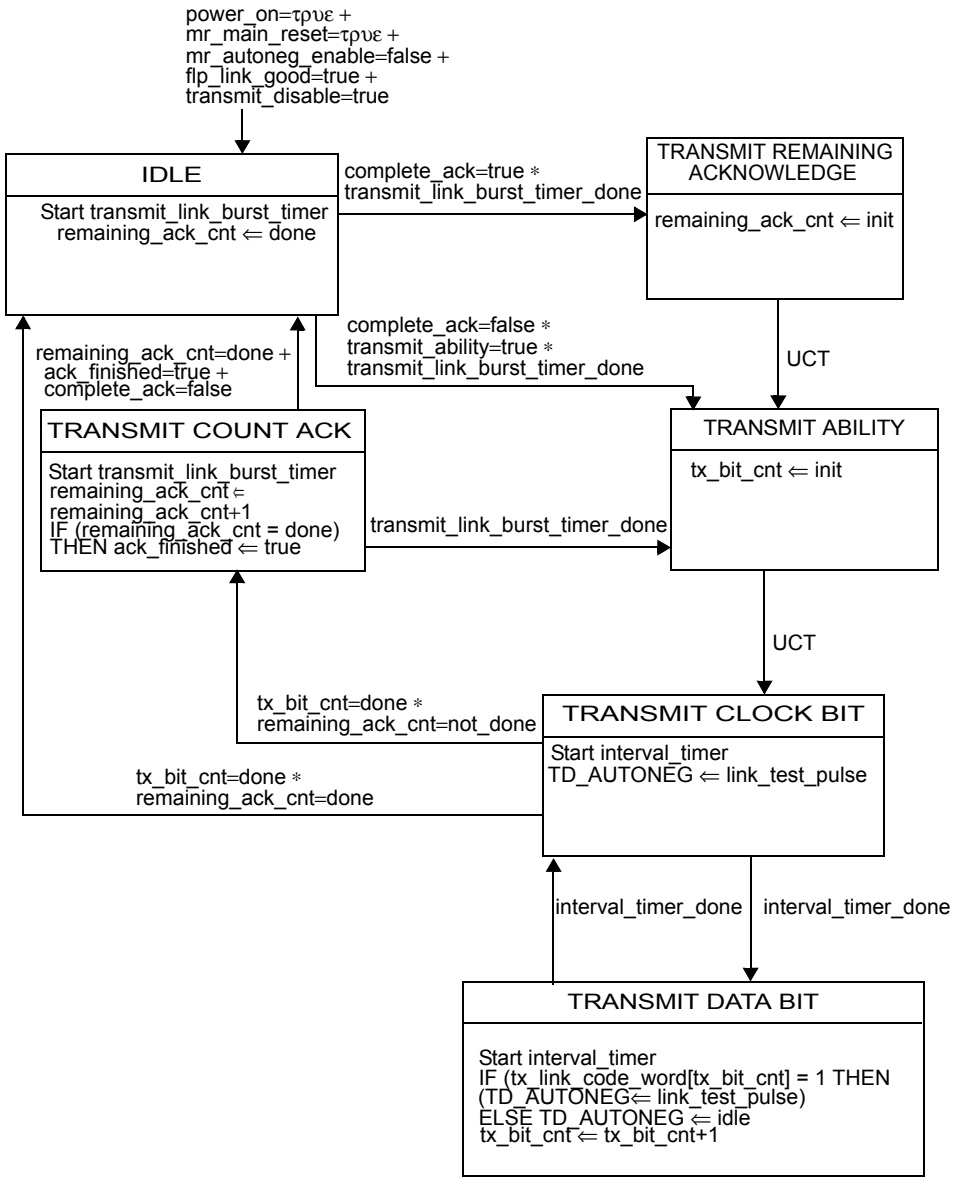


Figure 28–16—Transmit state diagram

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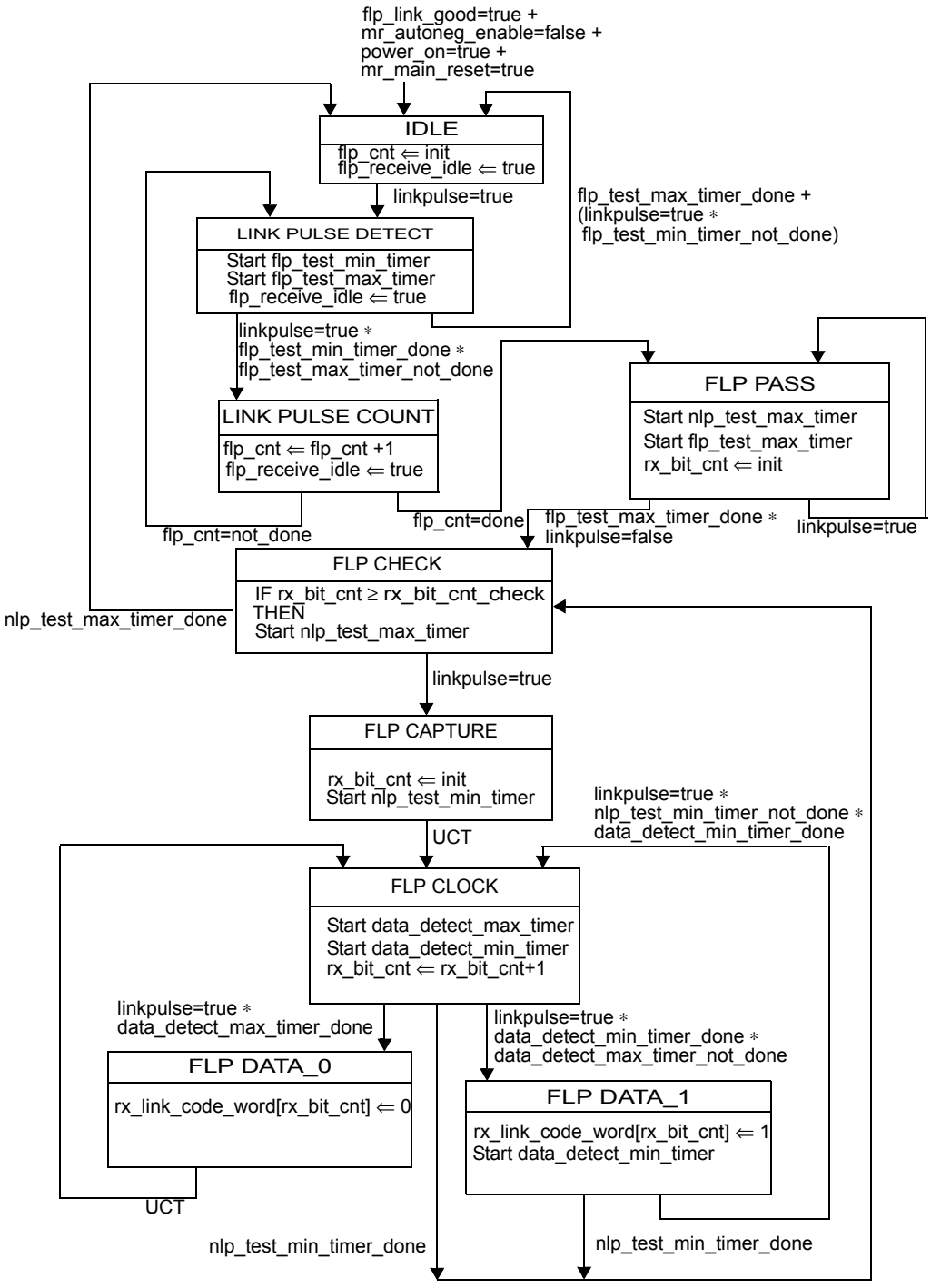
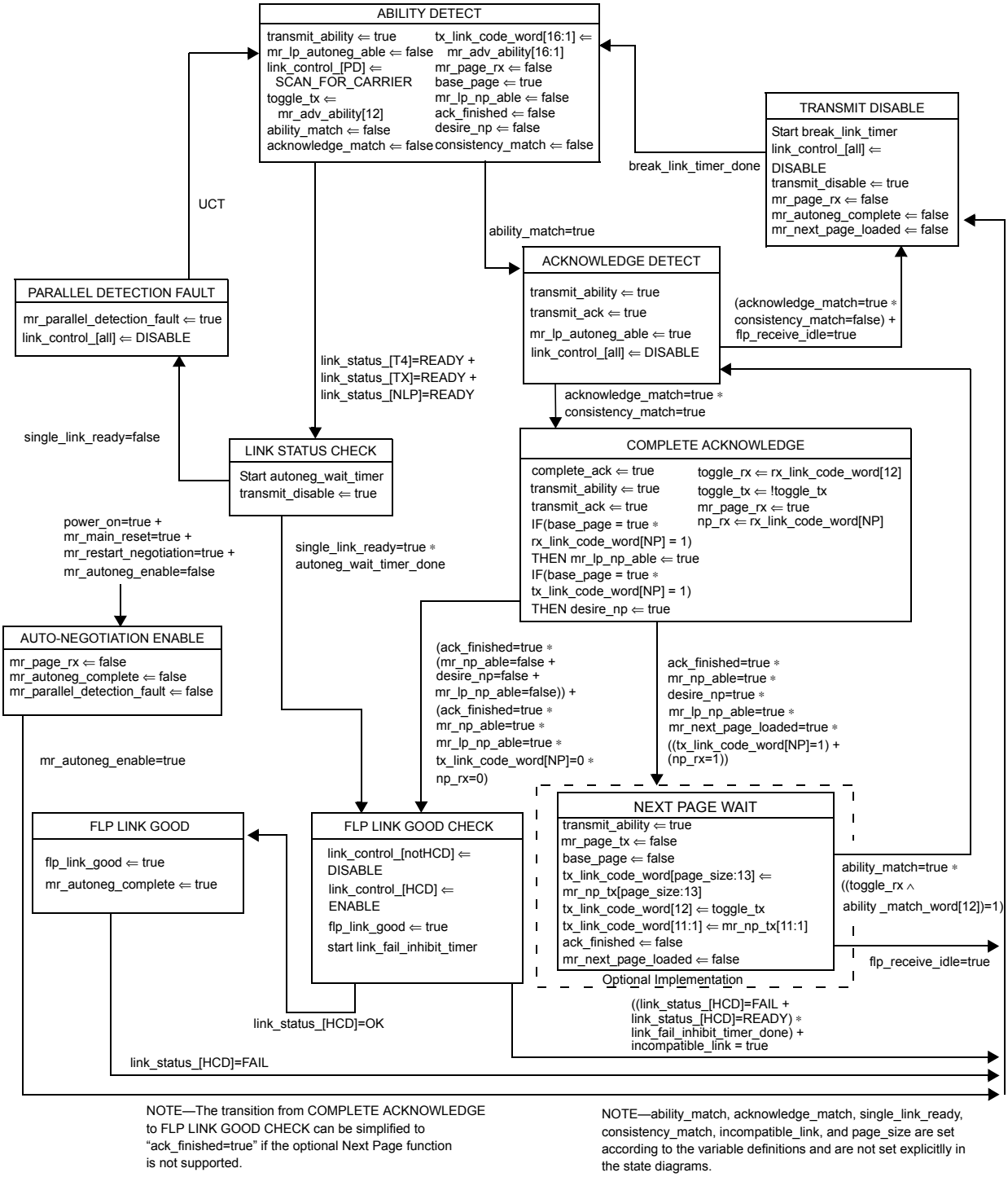


Figure 28–17—Receive state diagram

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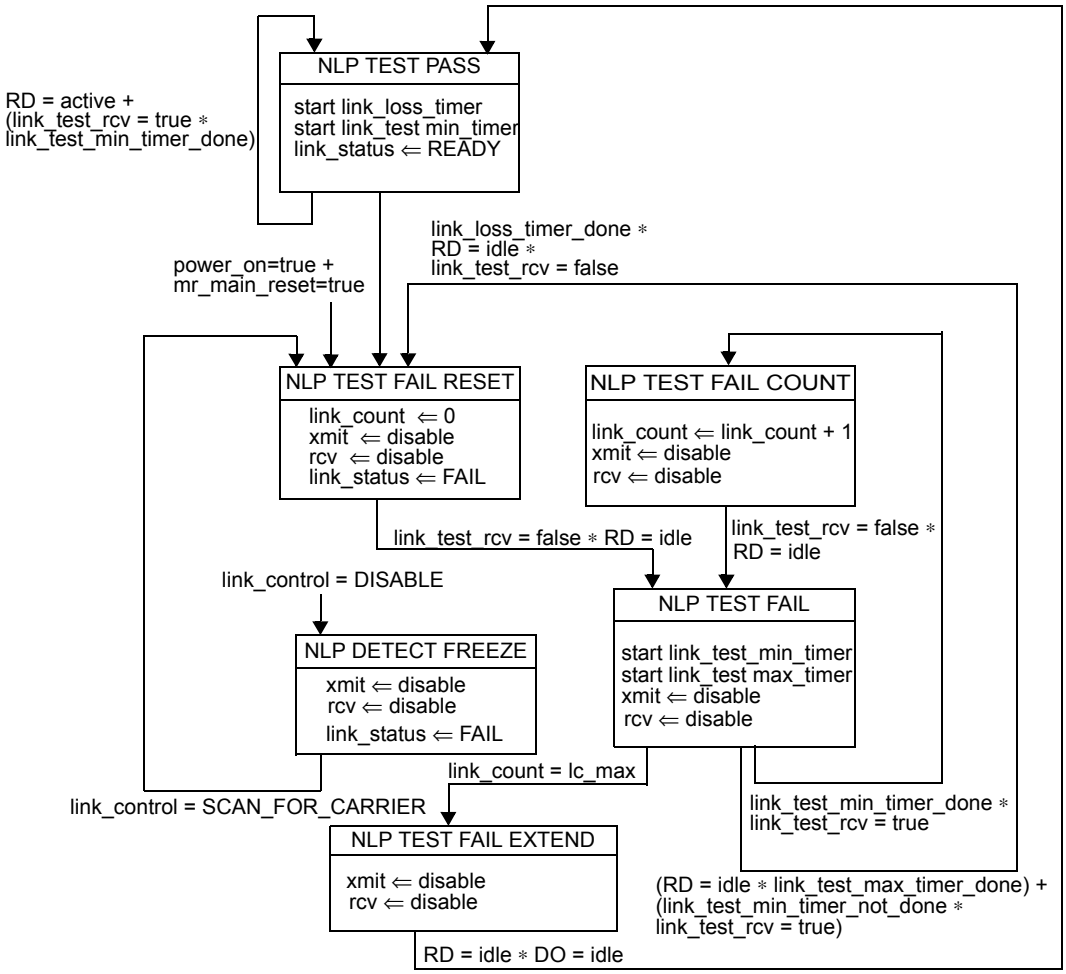


NOTE—The transition from COMPLETE ACKNOWLEDGE to FLP LINK GOOD CHECK can be simplified to "ack_finished=true" if the optional Next Page function is not supported.

NOTE—ability_match, acknowledge_match, single_link_ready, consistency_match, incompatible_link, and page_size are set according to the variable definitions and are not set explicitlly in the state diagrams.

Figure 28–18—Arbitration state diagram

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NOTE—The variables link_control and link_status are viewed as dedicated signals by the NLP Receive Link integrity Test state diagram, but are viewed as link_control_[NLP] and link_status_[NLP] by the Auto-Negotiation Arbitration state diagram, Figure 28–18.

Figure 28–19—NLP Receive Link Integrity Test state diagram

28.4 Electrical specifications

The electrical characteristics of pulses within FLP Bursts shall be identical to the characteristics of NLPs and shall meet the requirements of Figure 14–13.

It is the responsibility of the technology-specific Transmit and Receive functions to interface to the MDI correctly.

NOTE—The requirements relative to the interface to the MDI are specified via the Transmit Switch and Receive Switch functions.

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28.5 Protocol implementation conformance statement (PICS) proforma for Clause 28, Physical Layer link signaling for Auto-Negotiation on twisted pair[11]

28.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 28, Physical Layer link signaling for Auto-Negotiation on twisted pair, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

28.5.2 Identification

28.5.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

28.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Clause 28, Physical Layer link signaling for 10 Mb/s, 100 Mb/s, and 1000 Mb/s Auto-Negotiation on twisted pair
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2015.)	

Date of Statement	

[11] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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28.5.3 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
10BT	Implementation supports a 10BASE-T data service	28.1.2	O		N/A
*NP	Implementation supports Next Page function	28.1.2	O		N/A
*MII	Implementation supports the MII Management Interface	28.1.2	O/1		N/A
MGMT	Implementation supports a non-MII Management Interface	28.1.2	O/1		N/A
*NOM	Implementation does not support management	28.1.2	O/1		N/A
*RF	Implementation supports Remote Fault Sensing	28.2.3.5	O		N/A
*NPSL	Link Partner Next Page Storage Location bit	28.2.4.1.5	O		N/A
*ENP	Implementation supports Extended Next Pages	28.2.3.4.2	O		N/A
*OPT	Implementation supports optimized FLP burst to FLP burst timing	28.2.1.1.2	ENP:M !ENP:O		N/A
*10G	Implementation supports a 10GBASE-T PHY	55	O		N/A

28.5.4 PICS proforma tables for Physical Layer link signaling for Auto-Negotiation on twisted pair

28.5.4.1 Scope

Item	Feature	Subclause	Status	Support	Value/Comment
SC1	MII Management Interface control and status registers	28.1.3	MII:M		Implemented in accordance with the definitions in Clause 22 and 28.2.4
SC2	CSMA/CD compatible devices using an eight-pin modular connector and using a signaling method to automatically configure the preferred mode of operation	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
SC3	Device uses 10BASE-T compatible link signaling to advertise non-CSMA/CD abilities	28.1.4	M		Auto-Negotiation function implemented in compliance with Clause 28
SC4	Future CSMA/CD implementations that use an eight-pin modular connector	28.1.4	M		Interoperable with devices compliant with Clause 28

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28.5.4.2 Auto-Negotiation functions

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	Transmit	28.2	M		Complies with Figure 28–16
AN2	Receive	28.2	M		Complies with Figure 28–17
AN3	Arbitration	28.2	M		Complies with Figure 28–18
AN4	NLP Receive Link Integrity Test	28.2	10BT:M		Complies with Figure 28–19
AN5	Technology-Dependent Interface	28.2	M		Complies with 28.2.6
AN6	Technology-dependent link integrity test	28.2	M		Implemented and interfaced to for those technologies supported by device
AN7	Management	28.2	O		MII based or alternate management

28.5.4.3 Transmit function requirements

Item	Feature	Subclause	Status	Support	Value/Comment
TF1	FLP Burst transmission	28.2.1.1	M		Not transmitted once Auto-Negotiation is complete and highest common denominator PMA has been enabled. Prohibited other than for link start-up
TF2	FLP Burst composition	28.2.1.1.1	M		Pulses in FLP Bursts meet the requirements of Figure 14–13
TF3	FLP Burst pulse definition	28.2.1.1.1	M		Odd-numbered pulse positions represent clock information; even-numbered pulse positions represent data information
TF4	The first pulse in an FLP Burst	28.2.1.1.2	M		Defined as a clock pulse for timing purposes
TF5	FLP Burst clock pulse spacing	28.2.1.1.2	M		Within an FLP Burst, spacing is 125 μs ± 14 μs
TF6	Logic one data bit representation	28.2.1.1.2	M		Pulse transmitted 62.5 μs ± 7 μs after the preceding clock pulse
TF7	Logic zero data bit representation	28.2.1.1.2	M		No link integrity test pulses within 111 μs of the preceding clock pulse
TF8	Consecutive FLP Bursts	28.2.1.1.2	M		The first link pulse in each FLP Burst is separated by 16 ms ± 8 ms
TF9	Consecutive FLP Bursts	28.2.1.1.2	OPT:M		The first link pulse in each FLP Burst is separated by 8.25 ms ± 0.25 ms

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28.5.4.3 Transmit function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
TF10	FLP Burst Base Page	28.2.1.2	M		Conforms to Figure 28–7
TF11	FLP Burst bit transmission order	28.2.1.2	M		Transmission is D0 first to D15 last
TF12	Selector Field values	28.2.1.2.1	M		Only defined values transmitted
TF13	Technology Ability Field values	28.2.1.2.2	M		Implementation supports a data service for each ability set in the Technology Ability Field
TF14	Remote Fault bit	28.2.1.2.4	M		Used in accordance with the Remote Fault function specifications
TF15	Acknowledge bit set, no Next Page to be sent	28.2.1.2.5	M		Set to logic one in the link codeword after the reception of at least three consecutive and consistent FLP Bursts
TF16	Acknowledge bit set, Next Page to be sent	28.2.1.2.5	NP:M		Set to logic one in the transmitted link codeword after the reception of at least three consecutive and consistent FLP Bursts and the current receive link codeword is saved
TF17	Number of link codewords sent with Acknowledge bit set	28.2.1.2.5	M		6 to 8 inclusive after COMPLETE ACKNOWLEDGE state entered
TF18	Device does not implement optional Next Page ability	28.2.1.2.6	M		NP=0 in base link codeword
TF19	Device implements optional Next Page ability and wishes to engage in Next Page exchange	28.2.1.2.6	NP:M		NP=1 in base link codeword
TF20	Transmit Switch function on completion of Auto-Negotiation	28.2.1.3	M		Enables the transmit path from a single technology-dependent PMA to the MDI once the highest common denominator has been selected
TF21	Transmit Switch function during Auto-Negotiation	28.2.1.3	M		Connects FLP Burst generator governed by Figure 28–16 to the MDI
TF22	Signals presented at MDI after connection through Transmit Switch from PMA	28.2.1.3	M		Conform to appropriate PHY specifications

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28.5.4.4 Receive function requirements

Item	Feature	Subclause	Status	Support	Value/Comment
RF1	Timer expiration	28.2.2.1	M		Timer definition in 28.3.2, values shown in Table 28–9
RF2	Identification of Link Partner as Auto-Negotiation able	28.2.2.1	M		Reception of 6 to 17 (inclusive) consecutive link pulses separated by at least flp_test_min_timer time but less than flp_test_max_timer time
RF3	First FLP Burst identifying Link Partner as Auto-Negotiation able	28.2.2.1	M		Data recovered is discarded if FLP Burst is incomplete
RF4	First link pulse in an FLP Burst	28.2.2.1	M		Interpreted as a clock link pulse
RF5	Restart of the data_detect_min_timer and data_detect_max_timer	28.2.2.1	M		Detection of a clock link pulse (Figure 28–9)
RF6	Reception of logic one	28.2.2.1	M		Link pulse received between greater than data_detect_min_timer time and less than data_detect_max_timer time after a clock pulse (Figure 28–9)
RF7	Reception of logic zero	28.2.2.1	M		Link pulse received after greater than data_detect_max_timer time after clock pulse, is treated as clock pulse (Figure 28–9)
RF8	FLP Bursts separation	28.2.2.1	M		Conforms to the nlp_test_min_timer and nlp_test_max_timer timing (Figure 28–10)
RF9	Receive Switch function on completion of Auto-Negotiation	28.2.2.3	M		Enables the receive path from the MDI to a single technology-dependent PMA once the highest common denominator has been selected
RF10	Receive Switch function during Auto-Negotiation	28.2.2.3	M		Connects the MDI to the FLP and NLP receivers governed by Figures 28–17 and 28–19, and to the 100BASE-TX and 100BASE-T4 receivers if present
RF11	Signals presented to PMA after connection through Receive Switch from MDI	28.2.2.3	M		Conform to appropriate PHY specifications
RF12	Generation of ability_match, acknowledge_match, and consistency_match	28.2.2.4	M		Responsibility of Receive function in accordance with 28.3.1

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28.5.4.5 Arbitration functions

Item	Feature	Subclause	Status	Support	Value/Comment
AF1	MDI receive connection during Auto-Negotiation, prior to FLP detection	28.2.3.1	M		Connected to the NLP Receive Link Integrity Test state diagram, and the link integrity test functions of 100BASE-TX and/or 100BASE-T4. Not connected to the 10BASE-T or any other PMA
AF2	Parallel detection operational mode selection	28.2.3.1	M		Set link_control=ENABLE for the single PMA indicating link_status=READY when the autoneg_wait_timer expires
AF3	Parallel detection PMA control	28.2.3.1	M		Set link_control=DISABLE to all PMAs except the selected operational PMA and indicate Auto-Negotiation has completed
AF4	Parallel detection setting of Link Partner ability register	28.2.3.1	M		On transition to the FLP LINK GOOD CHECK state from the LINK STATUS CHECK state the Parallel Detection function shall set the bit in the Link Partner ability register (Register 5) corresponding to the technology detected by the Parallel Detection function
AF5	Response to renegotiation request	28.2.3.2	M		Disable all technology-dependent link integrity test functions and halt transmit activity until break_link_timer expires
AF6	Auto-Negotiation resumption	28.2.3.2	M		Issue FLP Bursts with Base Page valid in tx_link_code_word[16:1] after break_link_timer expires
AF7	Priority resolution	28.2.3.3	M		Single PMA connected to MDI is enabled corresponding to Technology Ability Field bit common to both Local/Link Partner Device and that has highest priority as defined by Annex 28B
AF8	Effect of receipt of reserved Technology Ability Field bit on priority resolution	28.2.3.3	M		Local Device ignores during priority resolution
AF9	Effect of parallel detection on priority resolution	28.2.3.3	M		Local Device considers technology identified by parallel detection as HCD
AF10	Values for HCD and link_status_[HCD] in the event there is no common technology	28.2.3.3	M		HCD=NULL link_status_[HCD]=FAIL

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28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
AF11	Message Page to Unformatted Page relationship for non-matching Selector Fields	28.2.3.4	NP:M		Each series of Unformatted Pages is preceded by an Message Page containing a message code that defines how the following Unformatted Page(s) will be interpreted
AF12	Message Page to Unformatted Page relationship for matching Selector Fields	28.2.3.4	NP:M		Use of Message Pages is specified by the Selector Field value
AF13	Transmission of Null message codes	28.2.3.4	NP:M		Sent with NP=0 on completion of all Next Pages while Link Partner continues to transmit valid Next Page information
AF14	Reception of Null message codes	28.2.3.4	NP:M		Recognized as indicating end of Link Partner's Next Page information
AF15	Next Page encoding	28.2.3.4.1	NP:M		Comply with Figures 28–11 and 28–12 for the NP, Ack, MP, Ack2, and T bits
AF16	Message/Unformatted Code Field	28.2.3.4.1	NP:M		D10-D0 encoded as Message Code Field if MP=1 or Unformatted Code Field if MP=0
AF17	NP bit encoding	28.2.3.4.3	NP:M		Logic 0=last page, logic 1=additional Next Page(s) follow
AF18	Message Page bit encoding	28.2.3.4.5	NP:M		Logic 0=Unformatted Page, logic 1=Message Page
AF19	Ack2 bit encoding	28.2.3.4.6	NP:M		Logic 0=cannot comply with message; logic 1= will comply with message
AF20	Toggle	28.2.3.4.7	NP:M		Takes the opposite value of the Toggle bit in the previously exchanged link codeword
AF21	Toggle encoding	28.2.3.4.7	NP:M		Logic zero = previous value of the transmitted link codeword equalled logic one Logic one = previous value of the transmitted link codeword equalled logic zero
AF22	Message Page encoding	28.2.3.4.8	NP:M		If MP=1, link codeword interpreted as Message Page
AF23	Message Code Field	28.2.3.4.9	NP:M		Combinations not shown in Annex 28C are reserved and may not be transmitted
AF24	Unformatted Page encoding	28.2.3.4.10	NP:M		If MP=0, link codeword interpreted as Unformatted Page

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28.5.4.5 Arbitration functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
AF25	Minimum Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, both send a minimum of one Next Page
AF26	Multiple Next Page exchange	28.2.3.4.13	NP:M		If both devices indicate Next Page able, exchange continues until neither Local/Remote Device has additional information; device sends Next Page with Null message code if it has no information to transmit
AF27	Unformatted Page ordering	28.2.3.4.13	NP:M		Unformatted Pages immediately follow the referencing message code in the order specified by the message code
AF28	Next Page Transmit register	28.2.3.4.14	NP:M		Defined in 28.2.4.1.6
AF29	Next Page receive data	28.2.3.4.14	NP:O		May be stored in Auto-Negotiation Link Partner ability register
AF30	Remote Fault sensing	28.2.3.5	RF:M		Optional
AF31	Transmission of RF bit by Local Device	28.2.3.5	M		If Local Device has no method to set RF bit, it must transmit RF bit with value of RF bit in Auto-Negotiation advertisement register (4.13)
AF32	RF bit reset	28.2.3.5	M		Once set, the RF bit remains set until successful renegotiation with the base link codeword
AF33	Receipt of Remote Fault indication in base link codeword	28.2.3.5	MII:M		Device sets the Remote Fault bit in the MII status register (1.4) to logic one if MII is present
AF34	Extended Next Page exchange	28.2.3.4	ENP:M		If both device and link partner are ENP able, any NP exchange uses Extended Next Pages

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28.5.4.6 Management function requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	Mandatory MII registers for Auto-Negotiation	28.2.4.1	MII:M		Registers 0, 1, 4, 5, 6
MF2	Optional MII register for Auto-Negotiation	28.2.4.1	MII* NP:M		Register 7
MF3	Auto-Negotiation enable	28.2.4.1.1	MII:M		Set control register Auto-Negotiation Enable bit (0.12)
MF4	Manual Speed/Duplex settings	28.2.4.1.1	MII:M		When bit 0.12 set, control register Speed Detection (0.13) and Duplex Mode (0.8) are ignored, and the Auto-Negotiation function determines link configuration
MF5	Control register (Register 0) Restart Auto-Negotiation (0.9) default	28.2.4.1.1	MII:M		PHY returns value of one in 0.9 until Auto-Negotiation has been initiated
MF6	Control register (Register 0) Restart Auto-Negotiation (0.9) set	28.2.4.1.1	MII:M		When 0.9 set, Auto-Negotiation will (re)initiate. On completion, 0.9 will be reset by the PHY device. Writing a zero to 0.9 at any time has no effect
MF7	Control register (Register 0) Restart Auto-Negotiation (0.9) reset	28.2.4.1.1	MII:M		0.9 is self-clearing; writing a zero to 0.9 at any time has no effect
MF8	Status register (Register 1) Auto-Negotiation Complete (1.5) reset	28.2.4.1.2	MII:M		If bit 0.12 reset, or a PHY lacks the ability to perform Auto-Negotiation, (1.5) is reset
MF9	Status register (Register 1) Remote Fault (1.4)	28.2.4.1.2	MII:M		Set by the PHY and remains set until either the status register is read or the PHY is reset
MF10	Advertisement register power on default	28.2.4.1.3	MII:M		Selector field as defined in Annex 28A; Ack=0; Technology Ability Field based on MII status register (1.15:11) or logical equivalent
MF11	Link partner ability register read/write	28.2.4.1.4	MII:M		Read only; write has no effect
MF12	Link partner ability register bit definitions	28.2.4.1.4	MII:M		Direct representation of the received link codeword (Figure 28–7)
MF13	Status register (Register 1) Auto-Negotiation Complete (1.5) set	28.2.4.1.4	MII:M		Set to logic one upon successful completion of Auto-Negotiation
MF14	Auto-Negotiation expansion register (Register 6)	28.2.4.1.5	MII:M		Read only; write has no effect

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28.5.4.6 Management function requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF15	Link Partner Auto-Negotiation Able bit (6.0)	28.2.4.1.5	MII:M		Set to indicate that the Link Partner is able to participate in the Auto-Negotiation function
MF16	Page Received bit (6.1) set	28.2.4.1.5	MII:M		Set to indicate that a new link codeword has been received and stored in the Auto-Negotiation Link Partner ability register
MF17	Page Received bit (6.1) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)
MF18	The Next Page Able bit (6.2) set	28.2.4.1.5	NP* MII:M		Set to indicate that the Local Device supports the Next Page function
MF19	The Link Partner Next Page Able bit (6.3) set	28.2.4.1.5	MII:M		Set to indicate that the Link Partner supports the Next Page function
MF20	Parallel Detection Fault bit (6.4) set	28.2.4.1.5	MII:M		Set to indicate that zero or more than one of the NLP Receive Link Integrity Test function, 100BASE-TX, or 100BASE-T4 PMAs have indicated link_status=READY when the autoneg_wait_timer expires
MF21	Parallel Detection Fault bit (6.4) reset	28.2.4.1.5	MII:M		Reset on a read of the Auto-Negotiation expansion register (Register 6)
MF22	Link Partner Next Page Storage Location bit	28.2.4.1.5	NPSL * MII:M		Indicates location of Link Partner Next Page
MF23	Receive Next Page Location Able bit	28.2.4.1.5	MII:M		Indicates if Link Partner Next Page Storage Location bit is supported.
MF24	Next Page Transmit register default	28.2.4.1.6	NP* MII:M		On power-up, contains value of 2001 H
MF25	Write to Next Page Transmit register	28.2.4.1.6	NP* MII:M		mr_next_page_loaded set to true
MF26	Absence of management function	28.2.5	NOM:M		Advertised abilities provided through a logical equivalent of mr_adv_ability[16:1]
MF27	Next Page support in absence of MII management	28.2.5	NOM:M		Device must provide logical equivalent of mr_np_able, mr_lp_np_able, or mr_next_page_loaded variables in order to set NP bit in transmitted link codeword

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28.5.4.7 Technology-dependent interface

Item	Feature	Subclause	Status	Support	Value/Comment
TD1	PMA_LINK.indication (link_status) values	28.2.6.1.1	M		link_status set to READY, OK or FAIL
TD2	PMA_LINK.indication (link_status) generation	28.2.6.1.2	M		Technology-dependent PMA and NLP Receive Link Integrity Test state diagram (Figure 28–19) responsibility
TD3	PMA_LINK.indication (link_status), effect of receipt	28.2.6.1.3	M		Governed by the state diagram of Figure 28–18
TD4	PMA_LINK.request (link_control) values	28.2.6.1.3	M		link_control set to SCAN_FOR_CARRIER, DISABLE, or ENABLE
TD5	Effect of link_control=SCAN_FOR_CARRIER	28.2.6.2.1	M		PMA to search for carrier and report link_status=READY when carrier is received, but no other actions are enabled
TD6	Effect of link_control=DISABLE	28.2.6.2.1	M		Disables PMA processing
TD7	Effect of link_control=ENABLE	28.2.6.2.1	M		Control passed to a single PMA for normal processing functions
TD8	PMA_LINK.request(link_control) generation	28.2.6.2.2	M		Auto-Negotiation function responsibility in accordance with Figures 28–17 and 28–18
TD9	PMA_LINK.request(link_control) default upon power-on, reset, or release from power-down	28.2.6.2.2	M		link_control = DISABLE state to all technology-dependent PMAs
TD10	PMA_LINK.request(link_control) effect of receipt	28.2.6.2.3	M		Governed by Figure 28–19 and the receiving technology-dependent link integrity test function
TD11	The linkpulse parameter shall	28.2.6.3.1	M		TRUE or FALSE.
TD12	The linkpulse=FALSE shall be used	28.2.6.3.1	M		By the Auto-Negotiation function to indicate that the Receive State Diagram has performed a state transition
TD13	The linkpulse=TRUE shall be used	28.2.6.3.1	M		By the Auto-Negotiation function to indicate that a valid Link Pulse has been received

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28.5.4.7 Technology-dependent interface *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
TD14	The Auto-Negotiation function shall generate linkpulse	28.2.6.3.2	M		To indicate to the PHY how to respond, in accordance with the state diagram of Figure 28–17.
TD15	Upon power-on or reset, if Auto-Negotiation is enabled (mr_autoneg_enable=true) the PMA_LINKPULSE.request(FALSE) message shall be	28.2.6.3.2	M		Issued to all technology-dependent PMAs.
TD16	The effect of the receipt of linkpulse shall be governed	28.2.6.3.3	M		By the receiving technology-dependent PMA function, based on the intent specified in the primitive semantics.

28.5.4.8 State diagrams

Item	Feature	Subclause	Status	Support	Value/Comment
SD1	Adherence to state diagrams	28.3	M		Implement all features of Figures 28–16 to 28–19. Identified options to Figures 28–16 to 28–19 are permitted
SD2	Ambiguous requirements	28.3	M		State diagrams take precedence in defining functional operation
SD3	autoneg_wait_timer	28.3.2	M		Expires 500 ms to 1000 ms after being started
SD4	break_link_timer	28.3.2	M		Expires 1200 ms to 1500 ms after being started
SD5	data_detect_min_timer	28.3.2	M		Expires 15 µs to 47 µs from the last clock pulse
SD6	data_detect_max_timer	28.3.2	M		Expire 78 µs to 100 µs from the last clock pulse
SD7	flp_test_max_timer	28.3.2	M		Expires 165 µs to 185 µs from the last link pulse
SD8	flp_test_min_timer	28.3.2	M		Expires 5 µs to 25 µs from the last link pulse
SD9	interval_timer	28.3.2	M		Expires 55.5 µs to 69.5 µs from each clock pulse and data bit
SD10	link_fail_inhibit_timer (10/100/1000 Mb/s)	28.3.2	!10G:M		Expires 750 ms to 1000 ms after entering the FLP LINK GOOD CHECK state
SD11	link_fail_inhibit_timer (10 Gb/s)	28.3.2	10G:M		Expires 2000 ms to 2250 ms after entering the FLP LINK GOOD CHECK state upon successful master/slave resolution

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28.5.4.8 State diagrams *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
SD12	nlp_test_max_timer	28.3.2	M		Expires 50 ms to 150 ms after being started if not restarted
SD13	nlp_test_min_timer	28.3.2	!ENP:M		Expires 5 ms to 7 ms after being started if not restarted
SD14	nlp_test_min_timer (with Extended Next Page)	28.3.2	ENP:M		Expires 6.75 ms to 7.25 ms after being started if not restarted
SD15	transmit_link_burst_timer (with no optimized timing)	28.3.1	!OPT:M		Expires 5.7 ms to 22.3 ms after the last transmitted link pulse in an FLP Burst
SD16	transmit_link_burst_timer (with optimized timing and 16-bit pages)	28.3.1	OPT:M		Expires 5.7 ms to 6.8 ms after the last transmitted link pulse in an FLP Burst
SD17	transmit_link_burst_timer (with optimized timing and 48-bit pages)	28.3.1	OPT:M		Expires 1.3 ms to 3.2 ms after the last transmitted link pulse in an FLP Burst containing Extended Next Pages

28.5.4.9 Electrical characteristics

Item	Feature	Subclause	Status	Support	Value/Comment
EC1	Pulses within FLP Bursts	28.4	M		Identical to the characteristics of NLPs and meet the requirements of Figure 14–13

28.5.4.10 Auto-Negotiation annexes

Item	Feature	Annex	Status	Support	Value/Comment
AA1	Selector field, S[4:0] values in the link codeword	Annex 28A	M		Identifies base message type as defined by Table 28A–1
AA2	Selector field reserved combinations	Annex 28A	M		Transmission not permitted
AA3	Relative priorities of the technologies supported by the IEEE 802.3 Selector Field value	28B.3	M		Defined in Annex 28B.3
AA4	Relative order of the technologies supported by IEEE 802.3 Selector Field	28B.3	M		Remain unchanged
AA5	Addition of new technology	28B.3	M		Inserted into its appropriate place in the priority resolution hierarchy, shifting technologies of lesser priority lower in priority

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28.5.4.10 Auto-Negotiation annexes *(continued)*

Item	Feature	Annex	Status	Support	Value/Comment
AA6	Addition of vendor-specific technology	28B.3	M		Priority of IEEE 802.3 standard topologies maintained, vendor-specific technologies to be inserted into an appropriate location
AA7	Message Code Field	Annex 28C	NP:M		Defines how following Unformatted Pages (if applicable) are interpreted
AA8	Order of Unformatted Code Fields within extended Pages	Annex 28C	NP:M		Pages to be in order specified by message code
AA9	Message Code Field reserved combinations	Annex 28C	NP:M		Transmission not permitted
AA10	Auto-Negotiation reserved code 1	28C.1	NP:M		Transmission of M10 to M0 equals 0, not permitted
AA11	Null message code	28C.2	NP:M		Transmitted during Next Page exchange when the Local Device has no information to transmit and Link Partner has additional pages to transmit
AA12	Remote Fault Identifier message code	28C.5	NP:M		Followed by single Unformatted Page to identify fault type with types defined in 28C.5
AA13	Organizationally Unique Identifier message code	28C.6	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of OUI or CID (bits 23:13) with MSB in U10; Second Unformatted Page contains next most significant 11 bits of OUI or CID (bits 12:2), with MSB in U10; Third Unformatted Page contains the least significant 2 bits of OUI or CID (bits 1:0) with MSB in U10, bits U8:0 contains user-defined code specific to OUI or CID; Fourth Unformatted Page contains user-defined code specific to OUI or CID

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28.5.4.10 Auto-Negotiation annexes *(continued)*

Item	Feature	Annex	Status	Support	Value/Comment
AA14	PHY Identifier message code	28C.7	NP:M		Followed by 4 Unformatted Pages. First Unformatted Page contains most significant 11 bits of PHY ID (2.15:5) with MSB in U10; Second Unformatted Page contains PHY ID bits 2.4:0 to 3.15:10, with MSB in U10; Third Unformatted Page contains PHY ID bits 3.9:0, with MSB in U10, and U0 contains user-defined code specific to PHY ID; Fourth Unformatted Page contains user-defined code specific to PHY ID
AA15	Auto-Negotiation reserved code 2	28C.8	NP:M		Transmission of M10 to M0 equals 1, not permitted

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28.6 Auto-Negotiation expansion

Auto-Negotiation is designed in a way that allows it to be easily expanded as new technologies are developed. When a new technology is developed, the following things must be done to allow Auto-Negotiation to support it:

a) The appropriate Selector Field value to contain the new technology must be selected and allocated.
b) A Technology bit must be allocated for the new technology within the chosen Selector Field value.
c) The new technology's relative priority within the technologies supported within a Selector Field value must be established.

Code space allocations are enumerated in Annex 28A, Annex 28B, and Annex 28C. Additions and insertions to the annexes are allowed. No changes to existing bits already defined are allowed.

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29. System considerations for multisegment 100BASE-T networks

NOTE—This clause relates to clauses that are not recommended for new installations. This clause is not recommended for new installations. Since March 2012, maintenance changes are no longer being considered for this clause.

29.1 Overview

This clause provides information on building 100BASE-T networks. The 100BASE-T technology is designed to be deployed in both homogenous 100 Mb/s networks and heterogeneous 10/100 Mb/s mixed CSMA/CD networks. Network topologies can be developed within a single 100BASE-T collision domain, but maximum flexibility is achieved by designing multiple collision domain networks that are joined by bridges and/or routers configured to provide a range of service levels to DTEs. For example, a combined 100BASE-T/10BASE-T system built with repeaters and bridges can deliver dedicated 100 Mb/s, shared 100 Mb/s, dedicated 10 Mb/s, and shared 10 Mb/s service to DTEs. The effective bandwidth of shared services is controlled by the number of DTEs that share the service.

Linking multiple 100BASE-T collision domains with bridges maximizes flexibility. Bridged topology designs can provide single bandwidth (Figure 29–1) or multiple bandwidth (Figure 29–2) services.

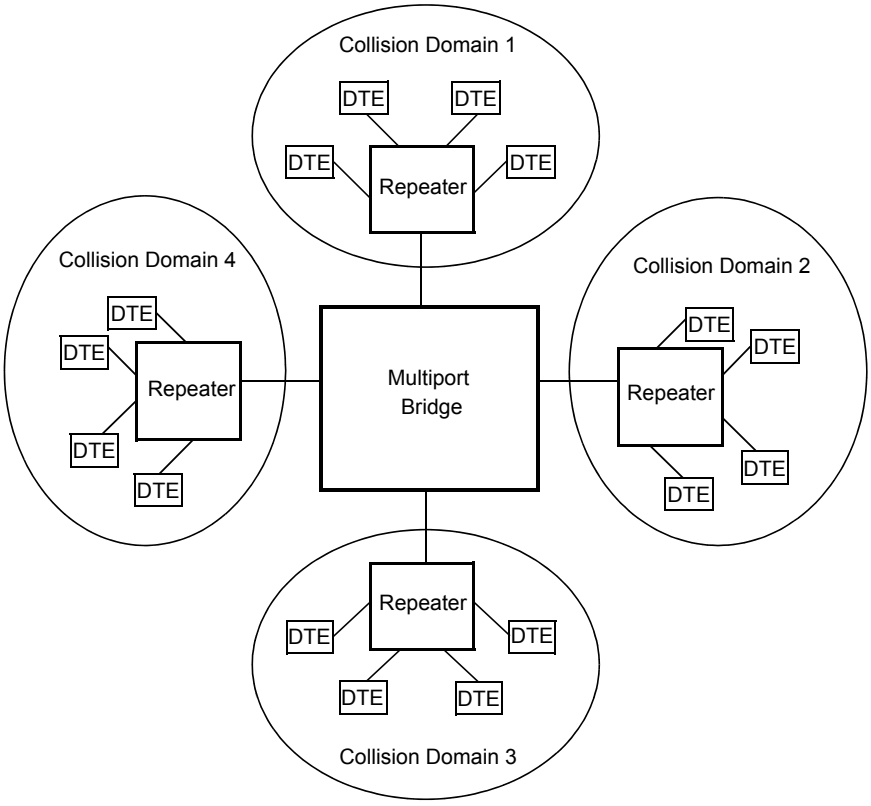


Figure 29–1—100 Mb/s multiple collision domain topology using multiport bridge

Individual collision domains can be linked by single devices (as shown in Figure 29–1 and Figure 29–2) or by multiple devices from any of several transmission systems. The design of multiple-collision-domain networks is governed by the rules defining each of the transmission systems incorporated into the design.

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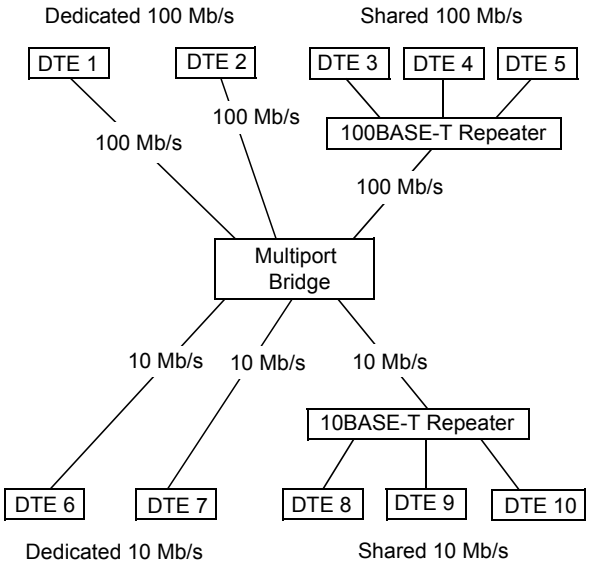


Figure 29–2—Multiple bandwidth, multiple collision domain topology using multiport bridge

The design of shared bandwidth 10 Mb/s collision domains is defined in 13.1 through 13.4; the design of shared bandwidth 100 Mb/s CSMA/CD collision domains is defined in 29.1.1 through 29.3.1.2. The design of 10BASE full duplex LANs is defined in 13.5; the design of full duplex 100BASE-X LANs is defined in 29.4.

29.1.1 Single collision domain multisegment networks

This clause provides information on building 100 Mb/s CSMA/CD multisegment networks within a single collision domain. The proper operation of a CSMA/CD network requires the physical size and number of repeaters to be limited in order to meet the round-trip propagation delay requirements of 4.2.3.2.3 and 4.4.2 and IPG requirements specified in 4.4.2.

This clause provides two network models. Transmission System Model 1 is a set of configurations that have been validated under conservative rules and have been qualified as meeting the requirements set forth above. Transmission System Model 2 is a set of calculation aids that allow those configuring a network to test a proposed configuration against a simple set of criteria that allows it to be qualified. Transmission System Model 2 validates an additional broad set of topologies that are fully functional and do not fit within the simpler, but more restrictive rules of Model 1.

The physical size of a CSMA/CD network is limited by the characteristics of individual network components. These characteristics include the following:

a) Media lengths and their associated propagation time delay
b) Delay of repeater units (start-up, steady-state, and end of event)
c) Delay of MAUs and PHYs (start-up, steady-state, and end of event)
d) Interpacket gap shrinkage due to repeater units
e) Delays within the DTE associated with the CSMA/CD access method
f) Collision detect and deassertion times associated with the MAUs and PHYs

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Table 29–1 summarizes the delays for 100BASE-T media segments. For more detailed information on the delays associated with individual 100BASE-T components, see

MII: Annex 22A
100BASE-T2:32.12
100BASE-T4:23.11
100BASE-TX:24.6
100BASE-FX: ISO/IEC 9314-3:1990
Repeater:27.3

Table 29–1—Delays for network media segments Model 1

Media type	Maximum number of PHYs per segment	Maximum segment length (m)	Maximum medium round-trip delay per segment (BT)
Balanced cable link segment 100BASE-T	2	100	114
Fiber link segment	2	412	412

29.1.2 Repeater usage

Repeaters are the means used to connect segments of a network medium together into a single collision domain. Different signaling systems (i.e., 100BASE-T2, 100BASE-T4, 100BASE-TX, 100BASE-FX) can be joined into a common collision domain using repeaters. Bridges can also be used to connect different signaling systems; however, if a bridge is so used, each system connected to the bridge will be a separate collision domain.

Two types of repeaters are defined for 100BASE-T (see Clause 27). Class I repeaters are principally used to connect unlike physical signaling systems and have internal delays such that only one Class I repeater can reside within a single collision domain when maximum cable lengths are used (see Figure 29–4). Class II repeaters typically provide ports for only one physical signaling system type (e.g., 100BASE-TX but not 100BASE-T4) and have smaller internal delays so that two such repeaters may reside within a given collision domain when maximum cable lengths are used (see Figure 29–6). Cable length can be sacrificed to add additional repeaters in a collision domain (see 29.3).

29.2 Transmission System Model 1

The following network topology constraints apply to networks using Transmission System Model 1.

a) All balanced cable (copper) segments less than or equal to 100 m each.
b) Fiber segments less than or equal to 412 m each.
c) MII cables for 100BASE-T shall not exceed 0.5 m each. When evaluating system topology, MII cable delays need not be accounted for separately. Delays attributable to the MII are incorporated into DTE and repeater component delays.

29.3 Transmission System Model 2

The physical size and number of topological elements in a 100BASE-T network is limited primarily by round-trip collision delay. A network configuration must be validated against collision delay using a net-

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work model. Since there are a limited number of topology models for any 100BASE-T collision domain, the modeling process is quite straightforward and can easily be done either manually or with a spreadsheet.

The model proposed here is derived from the one presented in 13.4. Modifications have been made to accommodate adjustments for DTE, repeater, and cable speeds.

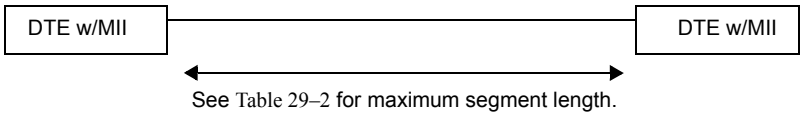


Figure 29–3—Model 1: Two DTEs, no repeater

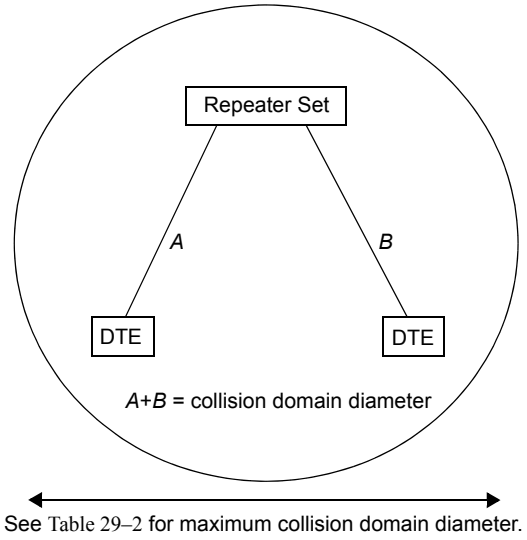


Figure 29–4—Model 1: Single repeater

Table 29–2—Maximum Model 1 collision domain diameter[a]

Model	Balanced cabling (copper)	Fiber	Balanced cabling & fiber (T2 or T4 and FX)	Balanced cabling & fiber (TX and FX)
DTE-DTE (see Figure 29–3)	100	412	NA	NA
One Class I repeater (see Figure 29–4)	200	272	231[a]	260.8[a]
One Class II repeater (see Figure 29–4)	200	320	304[b]	308.8[b]
Two Class II repeaters (see Figure 29–5)	205	228	236.3[c]	216.2[c]

[a]Assumes 100 m of balanced cabling and one fiber link.
[b]This entry included for completeness. It may be impractical to construct a T4 to FX class II repeater.
[c] Assumes 105 m of balanced cabling and one fiber link.

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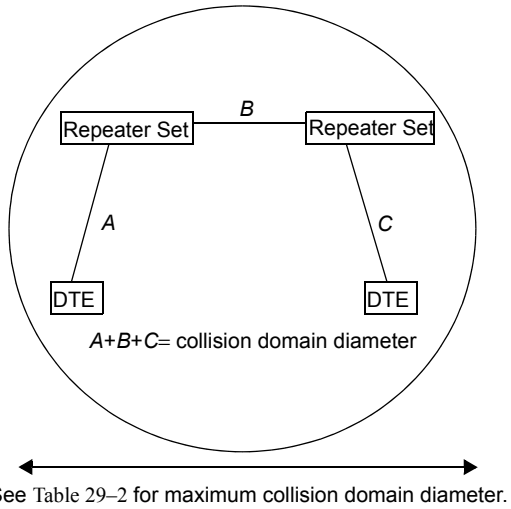


Figure 29–5—System Model 1: Two Class II repeaters

29.3.1 Round-trip collision delay

For a network to be valid, it must be possible for any two DTEs on the network to contend for the network at the same time. Each station attempting to transmit must be notified of the contention by the returned "collision" signal within the "collision window" (see 4.1.2.2 and 5.2.2.1.2). Additionally, the maximum length fragment created must contain less than 512 bits after the start-of-frame delimiter (SFD). These requirements limit the physical diameter (maximum distance between DTEs) of a network. The maximum round-trip delay must be qualified between all pairs of DTEs in the network. In practice this means that the qualification must be done between those that, by inspection of the topology, are candidates for the longest delay. The following network modeling methodology is provided to assist that calculation.

29.3.1.1 Worst-case path delay value (PDV) selection

The worst-case path through a network to be validated shall be identified by examination of aggregate DTE delays, cable delays, and repeater delays. The worst case consists of the path between the two DTEs at opposite ends of the network that have the longest round-trip time. Figure 29–6 and Figure 29–7 show schematic representations of one-repeater and two-repeater paths.

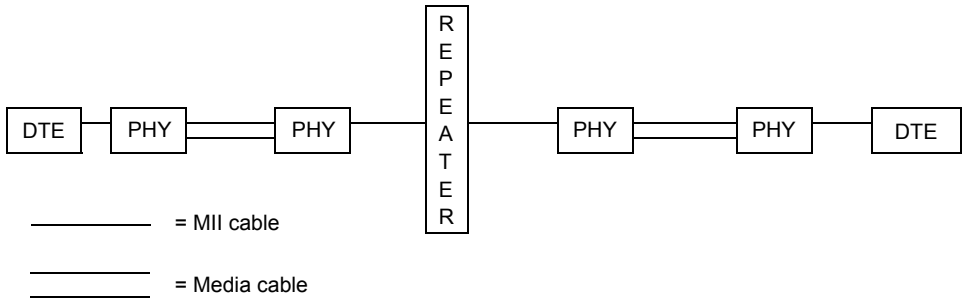


Figure 29–6—System Model 2: Single repeater

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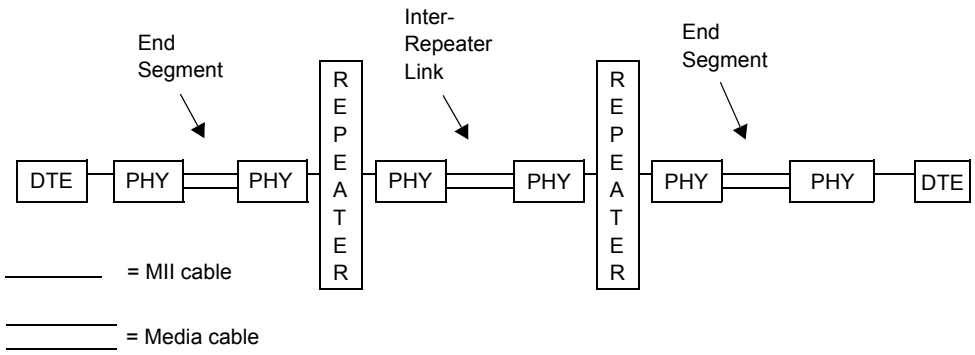


Figure 29–7—System Model 2-2: Two repeaters

29.3.1.2 Worst-case PDV calculation

Once a set of paths is chosen for calculation, each shall be checked for validity against the following formula:

$$PDV = \sum\text{link delays (LSDV)} + \sum\text{repeater delays} + \text{DTE delays} + \text{safety margin}$$

Values for the formula variables are determined by the following method:

a) Determine the delay for each link segment (Link Segment Delay Value, or LSDV), including inter-repeater links, using the formula

$$\text{LSDV} = 2\ (\text{for round-trip delay}) \times \text{segment length} \times \text{cable delay for this segment}$$

NOTE 1—Length is the sum of the cable lengths between the PHY interfaces at the repeater and the farthest DTE for End Segments plus the sum of the cable lengths between the repeater PHY interfaces for Inter-Repeater Links. All measurements are in meters.

NOTE 2—Cable delay is the delay specified by the manufacturer or the maximum value for the type of cable used as shown in Table 29–3. For this calculation, cable delay must be specified in bit times per meter (BT/m). Table 29–4 can be used to convert values specified relative to the speed of light (%c) or nanoseconds per meter (ns/m).

NOTE 3—When actual cable lengths or propagation delays are not known, use the Max delay in bit times as specified in Table 29–3 for copper cables. Delays for fiber should be calculated, as the value found in Table 29–3 will be too large for most applications.

b) Sum together the LSDVs for all segments in the path.

c) Determine the delay for each repeater in the path. If model-specific data are not available from the manufacturer, determine the class of each repeater (I or II) and enter the appropriate default value from Table 29–3.

d) MII cables for 100BASE-T shall not exceed 0.5 m each. When evaluating system topology, MII cable delays need not be accounted for separately. Delays attributable to the MII are incorporated into DTE and repeater component delays.

e) Use the DTE delay value shown in Table 29–3 unless your equipment manufacturer defines a different value.

f) Decide on appropriate safety margin—0 to 5 bit times—for the PDV calculation. Safety margin is used to provide additional margin to accommodate unanticipated delay elements, such as extra-long connecting cable runs between wall jacks and DTEs. (A safety margin of 4 BT is recommended.)

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g) Insert the values obtained through the calculations above into the following formula to calculate the PDV. (Some configurations may not use all the elements of the formula.)

PDV = ∑link delays (LSDV) + ∑repeater delays + DTE delay + safety margin

h) If the PDV is less than 512, the path is qualified in terms of worst-case delay.

i) Late collisions and/or CRC errors are indicators that path delays exceed 512 BT.

Table 29–3—Network component delays, Transmission System Model 2

Component	Round trip delay in bit times per meter	Maximum round trip delay in bit times
Two TX/FX DTEs		100
Two T4 DTEs		138
Two T2 DTEs		96
One T2 or T4 and one TX/FX DTE[a]		127
Cat 3 cabling segment	1.14	114 (100 m)
Cat 4 cabling segment	1.14	114 (100 m)
Cat 5 cabling segment	1.112	111.2 (100 m)
STP cabling segment	1.112	111.2 (100 m)
Fiber optic cabling segment	1.0	412 (412 m)
Class I repeater		140
Class II repeater with all ports TX/FX		92
Class II repeater with any port T4		67
Class II repeater with any port T2		90

[a] Worst-case values are used (TX/FX values for MAC transmit start and MDI input to collision detect; T4 value for MDI input to MDI output).

29.4 Full duplex 100 Mb/s topology limitations

Unlike half duplex CSMA/CD networks, the physical size of full duplex 100 Mb/s CSMA/CD networks is not limited by the round-trip collision propagation delay. Instead, the maximum link length between DTEs is limited only by the signal transmission characteristics of the specific cable, as specified in Table 29–5.

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Table 29–4—Conversion table for cable delays

Speed relative to *c*	ns/m	BT/m
0.4	8.34	0.834
0.5	6.67	0.667
0.51	6.54	0.654
0.52	6.41	0.641
0.53	6.29	0.629
0.54	6.18	0.618
0.55	6.06	0.606
0.56	5.96	0.596
0.57	5.85	0.585
0.58	5.75	0.575
0.5852	5.70	0.570
0.59	5.65	0.565
0.6	5.56	0.556
0.61	5.47	0.547
0.62	5.38	0.538
0.63	5.29	0.529
0.64	5.21	0.521
0.65	5.13	0.513
0.654	5.10	0.510
0.66	5.05	0.505
0.666	5.01	0.501
0.67	4.98	0.498
0.68	4.91	0.491
0.69	4.83	0.483
0.7	4.77	0.477
0.8	4.17	0.417
0.9	3.71	0.371

Table 29–5—Link segment length limits; 100 Mb/s full duplex segments

Cable type	Maximum link segment length
100BASE-TX (UTP, STP per Clause 25)	100 m
100BASE-FX (multimode fiber per Clause 26)	2000 m
100BASE-T2 (UTP per Clause 32)	100 m

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30. Management

30.1 Overview

This clause provides the Layer Management specification for DTEs, repeaters, MAUs, and Midspans based on the CSMA/CD access method. The clause is produced from the ISO framework additions to Clause 5, Layer Management; Clause 19, Repeater Management; and Clause 20, MAU Management. It incorporates additions to the objects, attributes, and behaviours to support 100 Mb/s, 1000 Mb/s and 10 Gb/s, full duplex operation, MAC Control, Link Aggregation, DTE Power via MDI, subscriber access networks, and the Link Layer Discovery Protocol (LLDP) IEEE 802.3 Organizationally Specific TLVs. The objects, attributes, and behaviours to support Link Aggregation are deprecated by IEEE Std 802.1AX-2008.

The layout of this clause takes the same form as 5.1, 5.2, and Clause 19, and Clause 20, although with equivalent subclauses grouped together. It identifies a common management model and framework applicable to IEEE 802.3 managed elements, identifies those elements and defines their managed objects, attributes, and behaviours in a protocol-independent language.

This clause provides the Layer Management specification for DTEs, repeaters, and MAUs based on the CSMA/CD access method. It defines facilities comprised of a set of statistics and actions needed to provide IEEE 802.3 Management services. The information in this clause should be used in conjunction with the Procedural Model defined in 4.2.7 through 4.2.10. The Procedural Model provides a formal description of the relationship between the CSMA/CD Layer Entities and the Layer Management facilities.

This management specification has been developed in accordance with the OSI management architecture as specified in the ISO Management Framework document, ISO/IEC 7498-4:1989. It is independent of any particular management application or management protocol.

The management facilities defined in this standard may be accessed both locally and remotely. Thus, the Layer Management specification provides facilities that can be accessed from within a station or can be accessed remotely by means of a peer-management protocol operating between application entities.

In CSMA/CD no peer management facilities are necessary for initiating or terminating normal protocol operations or for handling abnormal protocol conditions. Since these activities are subsumed by the normal operation of the protocol, they are not considered to be a function of Layer Management and are, therefore, not discussed in this clause.

Implementation of part or all of Layer Management is not a requirement for conformance to any other clause of this standard.

The intent of this standard is to furnish a management specification that can be used by the wide variety of different devices that may be attached to an Ethernet network. Thus, a comprehensive list of management facilities is provided.

The improper use of some of the facilities described in this clause may cause serious disruption of the network. In accordance with ISO management architecture, any necessary security provisions should be provided by the Agent in the Local System Environment. This can be in the form of specific security features or in the form of security features provided by the peer communication facilities.

The device that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds. Because this clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayer combination as a group. Therefore, in this clause, the term MAU will include PMA and PMD sublayers as well as MAUs, except in those instances where it is explicitly restricted to 10 Mb/s.

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30.1.1 Scope

This clause includes selections from Clause 5, Clause 19, and Clause 20. It is intended to be an entirely equivalent specification for the management of 10 Mb/s DTEs, 10 Mb/s baseband repeater units, and 10 Mb/s integrated MAUs. It incorporates additions to the objects, attributes, and behaviours to support subsequent additions to this standard.Implementations of management for DTEs, repeater units, and embedded MAUs should follow the requirements of this clause (e.g., a 10 Mb/s implementation should incorporate the attributes to indicate that it is not capable of 100 Mb/s or 1000 Mb/s operation; half duplex DTE should incorporate the attributes to indicate that it is not capable of full duplex operation, etc.).

For 10 Mb/s ports without integral MAUs, attributes are provided for characteristics observable from the AUI of the connected DTE or repeater. Direct management of AUI MAUs that are external to their respective DTEs or repeaters is beyond the scope of this standard.

The managed objects within this standard are defined in terms of their behaviour, attributes, actions, notifications, and packages in accordance with IEEE 802.1 and ISO standards for network management. Managed objects are grouped into mandatory and optional packages.

This specification is defined to be independent of any particular management application or management protocol. The means by which the managed objects defined in this standard are accessed is beyond the scope of this standard.

30.1.2 Relationship to objects in IEEE 802.1F

The following managed object classes, if supported by an implementation, shall be as specified in IEEE Std 802.1F-1993 (withdrawn): ResourceTypeID, EWMAMetricMonitor.

oResourceTypeID

This object class is mandatory and shall be implemented as defined in IEEE 802.1F. This object is bound to oMAC-Entity, oRepeater, oMidSpan, and oMAU as defined by the NAMEBINDINGs. Note that the binding to oMAU is mandatory only when MII is present. The Entity Relationship Diagrams, Figure 30–3, Figure 30–4, and Figure 30–5 show these bindings pictorially.

oEWMAMetricMonitor

This object class is optional. When implemented, it shall be implemented as defined in IEEE 802.1F, subject to the specific requirements described below. This object is bound to system as defined by the NAMEBINDINGs.

Implementations of IEEE 802.3 Management that support the oEWMAMetricMonitor managed object class are required to support values of granularity period as small as one second. Implementations are required to support at least one sequence of low and high thresholds. The granularity period may be set to equal to the moving time period as a minimal conformant implementation.

30.1.3 Systems management overview

Within the ISO Open Systems Interconnection (OSI) architecture, the need to handle the special problems of initializing, terminating, and monitoring ongoing activities and assisting in their operations, as well as handling abnormal conditions, is recognized. These needs are collectively addressed by the systems management component of the OSI architecture.

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A management protocol is required for the exchange of information between systems on a network. This management standard is independent of any particular management protocol.

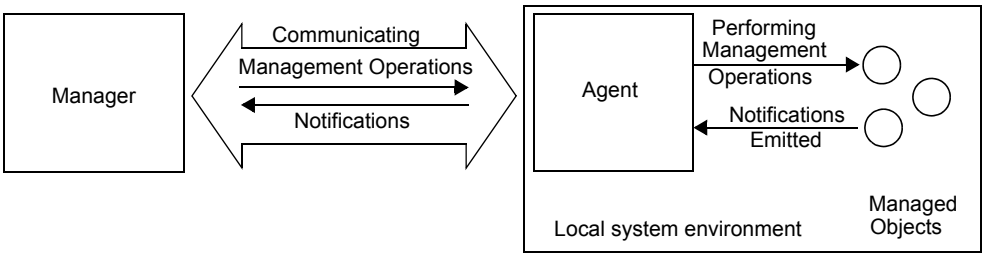
This management standard, in conjunction with the management standards of other layers, provides the means to perform various management functions. IEEE 802.3 Management collects information needed from the MAC and Physical Layers and the devices defined in IEEE 802.3. It also provides a means to exercise control over those elements.

The relationship between the various management entities and the layer entities according to the ISO model is shown in Figure 30–1.

30.1.4 Management model

This standard describes management of DTEs, repeaters, and integrated MAUs in terms of a general model of management of resources within the open systems environment. The model, which is described in ISO/IEC 10040:1992, is briefly summarized here.

Management is viewed as a distributed application modeled as a set of interacting management processes. These processes are executed by systems within the open environment. A managing system executes a managing process that invokes management operations. A managed system executes a process that is receptive to these management operations and provides an interface to the resources to be managed. A managed object is the abstraction of a resource that represents its properties as seen by (and for the purpose of) management. Managed objects respond to a defined set of management operations. Managed objects are also capable of emitting a defined set of notifications. This interaction of processes is shown in Figure 30–1.



NOTE—This figure is drawn from Figure 1 of ISO/IEC 10040:1992, Information technology—Open Systems Interconnection—Systems management overview. In the event of any conflict, the depiction in ISO/IEC 10040:1992 takes precedence.

Figure 30–1—Interaction between manager, agent, and objects

A managed object is a management view of a resource. The resource may be a logical construct, function, physical device, or anything subject to management. Managed objects are defined in terms of four types of elements:

a) *Attributes.* Data-like properties (as seen by management) of a managed object.
b) *Actions.* Operations that a managing process may perform on an object or its attributes.
c) *Notifications.* Unsolicited reports of events that may be generated by an object.
d) *Behaviour.* The way in which managed objects, attributes, and actions interact with the actual resources they model and with each other.

The above items are defined in 30.3 through 30.3.7 of this clause in terms of the template requirements of ISO/IEC 10165-4:1991.

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Some of the functions and resources within IEEE 802.3 devices are appropriate targets for management. They have been identified by specifying managed objects that provide a management view of the functions or resources. Within this general model, the IEEE 802.3 device is viewed as a managed device. It performs functions as defined by the applicable standard for such a device. Managed objects providing a view of those functions and resources appropriate to the management of the device are specified. The purpose of this standard is to define the object classes associated with the devices in terms of their attributes, operations, notifications, and behaviour.

30.2 Managed objects

30.2.1 Introduction

This clause identifies the Managed Object classes for IEEE 802.3 components within a managed system. It also identifies which managed objects and packages are applicable to which components.

All counters defined in this specification are assumed to be wrap-around counters. Wrap-around counters are those that automatically go from their maximum value (or final value) to zero and continue to operate. These unsigned counters do not provide for any explicit means to return them to their minimum (zero), i.e., reset. Because of their nature, wrap-around counters should be read frequently enough to avoid loss of information. When a counter has a maximum increment rate specified at one speed of operation, and that counter is appropriate to a higher speed of operation, then the maximum increment rate at that higher speed of operation is

$$\text{maximum increment rate specified} \times \left(\frac{\text{higher speed of operation in Mb/s}}{\text{specified speed of operation in Mb/s}} \right) \tag{30–1}$$

unless otherwise indicated.

30.2.2 Overview of managed objects

Managed objects provide a means to

— Identify a resource
— Control a resource
— Monitor a resource

30.2.2.1 Text description of managed objects

In case of conflict, the formal behaviour definitions in 30.3, 30.4, 30.5, 30.6, and 30.7 take precedence over the text descriptions in this subclause.

oAggPortDebugInformation

If oAggregator is implemented, a single instance of oAggPortDebugInformation may be contained within oAggregationPort. This managed object class provides optional additional information that can assist with debugging and fault finding in Systems that support Link Aggregation.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAggPortStats

If oAggregator is implemented, a single instance of oAggPortStats may be contained within oAggregationPort. This managed object class

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provides optional additional statistics related to LACP and Marker protocol activity on an instance of an Aggregation Port that is involved in Link Aggregation.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAggregationPort If oAggregator is implemented, oAggregationPort is contained within oAggregator. An instance of this managed object class is present for each Aggregation Port that is part of the aggregation represented by the oAggregator instance. This managed object class provides the basic management controls necessary to allow an instance of an Aggregation Port to be managed, for the purposes of Link Aggregation.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAggregator If implemented, oAggregator is the top-most managed object class of the DTE containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard. The oAggregator managed object class provides the management controls necessary to allow an instance of an Aggregator to be managed.

NOTE—This object is deprecated by IEEE Std 802.1AX-2008.

oAutoNegotiation The managed object of that portion of the containment trees shown in Figure 30–4 and Figure 30–5. The attributes, notifications, and actions defined in 30.6 are contained within the MAU managed object.

oGroup The group managed object class is a view of a collection of repeater ports.

oEXTENSION If implemented, oEXTENSION is contained within oMACControlEntity. The oEXTENSION managed object class provides the management controls necessary to allow an instance of the MAC Control EXTENSION function to be managed.

oLldpXdot3Config The top-most managed object class of the Link Layer Discovery Protocol (LLDP) containment tree shown in Figure 30–6. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oLldpXdot3LocSystemsGroup
If oLldpXdot3Config is implemented, a single instance of oLldpXdot3LocSystemsGroup may be contained within oLldpXdot3Config. This managed object class provides the LLDP local system information.

oLldpXdot3RemSystemsGroup
If oLldpXdot3Config is implemented, a single instance of oLldpXdot3RemSystemsGroup may be contained within oLldpXdot3Config. This managed object class provides the LLDP remote system information.

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oMACControlEntity If implemented, and if oOAM is implemented, a single instance of oMACControlEntity is contained within oOAM. Otherwise, if implemented, and if oAggregator is implemented, oMACControlEntity is contained within oAggregator. Otherwise, if implemented, oMACControlEntity becomes the top-most managed object class of the DTE containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard.

oMACControlFunctionEntity
If implemented, oMACControlFunctionEntity is contained within oMACControlEntity. The oMACControlFunctionEntity managed object class provides the management controls necessary to allow an instance of the MAC Control PAUSE function to be managed.

oMACEntity If oMACControlEntity is implemented, oMACEntity is contained within oMACControlEntity. Otherwise, if oOAM is implemented, oMACEntity is contained within oOAM. Otherwise, if oAggregator is implemented, oMACEntity is contained within oAggregator. Otherwise, oMACEntity becomes the top-most managed object class of the DTE containment tree shown in Figure 30–3. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard.

oMAU The managed object of that portion of the containment trees shown in Figure 30–3 and Figure 30–4. The attributes, notifications, and actions defined in 30.5 are contained within the MAU managed object. Neither counter values nor the value of MAUAdminState is required to be preserved across events involving the loss of power.

oMidSpan The top-most managed object class of the Midspan containment tree shown in Figure 30–5. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oMPCP If implemented, oMPCP is contained within oMACControlEntity. The oMPCP managed object class provides the management controls necessary to allow an instance of the Multipoint MAC Control function to be managed.

oOAM If implemented, and if oAggregator is implemented, oOAM is contained within oAggregator. An instance of this managed object class is present for each Aggregation Port that is part of the aggregation represented by the oAggregator instance. Otherwise, if implemented, oOAM becomes the top-most managed object class of the DTE containment tree shown in Figure 30–3. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this International Standard.

oOMPEmulation If implemented, oOMPEmulation is contained within oMACEntity. The oOMPEmulation managed object class provides the management controls necessary to allow an instance of an OMPEmulation sublayer to be managed.

oPHYEntity If oOMPEmulation is implemented, oPHYEntity is contained within

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oOMPEmulation. Otherwise oPHYEntity is contained within oMACEntity. Many instances of oPHYEntity may coexist within one instance of oMACEntity; however, only one PHY may be active for data transfer to and from the MAC at any one time. oPHYEntity is the managed object that contains the MAU, PAF, and PSE managed objects in a DTE.

oPAF The oPAF managed object class provides the management controls necessary to allow an instance of a PME aggregation function (PAF) to be managed. The PAF managed object class also provides a view of a collection of PMEs.

oPD The managed object of that portion of the containment trees shown in Figure 30–3, Figure 30–4, and Figure 30–5. This managed object class provides the attributes, actions, and notifications required for management by a PSE system.

oPME The oPME managed object class provides the management controls necessary to allow an instance of a PME to be managed. The oPAF managed object contains the PME managed object in a DTE.

oPSE The managed object of that portion of the containment trees shown in Figure 30–3, Figure 30–4, and Figure 30–5. This managed object class provides the attributes, actions, and notifications required for management of a PD system.

oPSEGroup The PSE Group managed object class is a view of a collection of PSEs.

oRepeater The top-most managed object class of the repeater containment tree shown in Figure 30–4. Note that this managed object class may be contained within another superior managed object class. Such containment is expected, but is outside the scope of this standard.

oRepeaterMonitor A managed object class called out by IEEE Std 802.1F-1993. See 30.1.2, oEWMAMetricMonitor.

oRepeaterPort The repeater port managed object class provides a view of the functional link between the data transfer service and a single PMA. The attributes associated with repeater port deal with the monitoring of traffic being handled by the repeater from the port and control of the operation of the port. The Port Enable/Disable function as reported by portAdminState is preserved across events involving loss of power. The oRepeaterPort managed object contains the MAU managed object in a repeater set.

NOTE—Attachment to nonstandard PMAs is outside the scope of this standard.

oResourceTypeID A managed object class called out by IEEE Std 802.1F-1993. It is used within this clause to identify manufacturer, product, and revision of managed components that implement functions and interfaces defined within IEEE 802.3. The Clause 22 MII or Clause 35 GMII specifies two registers to carry PHY Identifier (22.2.4.3.1), which provides succinct information sufficient to support oResourceTypeID.

oTimeSync If implemented, oTimeSync is contained within oPHYEntity. The oTimeSync managed object class provides the controls neccessary to manage the instance of the TimeSync function.

oWIS The managed object of that portion of the containment tree shown in

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Figure 30–3. The attributes defined in 30.8 are contained within the oMAU managed object.

30.2.2.2 Functions to support management

Functions are defined in other clauses that facilitate managed operation. The functions in other clauses that facilitate managed operation are referenced from the text of this management clause.

30.2.2.2.1 DTE MAC sublayer functions

For DTE MACs, with regard to reception-related error statistics a hierarchical order has been established such that when multiple error statuses can be associated with one frame, only one status is returned to the LLC. This hierarchy in descending order is as follows:

— frameTooLong
— alignmentError
— frameCheckError
— lengthError

The counters are primarily incremented based on the status returned to the MAC client; therefore, the hierarchical order of the counters is determined by the order of the status. Frame fragments are not included in any of the statistics unless otherwise stated. In implementing any of the specified actions, receptions and transmissions that are in progress are completed before the action takes effect.

30.2.2.2.2 Repeater functions

The Repeater Port Object class contains seven functions which are defined in this clause and are used to collect statistics on the activity received by the port. The relationship of the functions to the repeater port and to the port attributes is shown in Figure 30–2.

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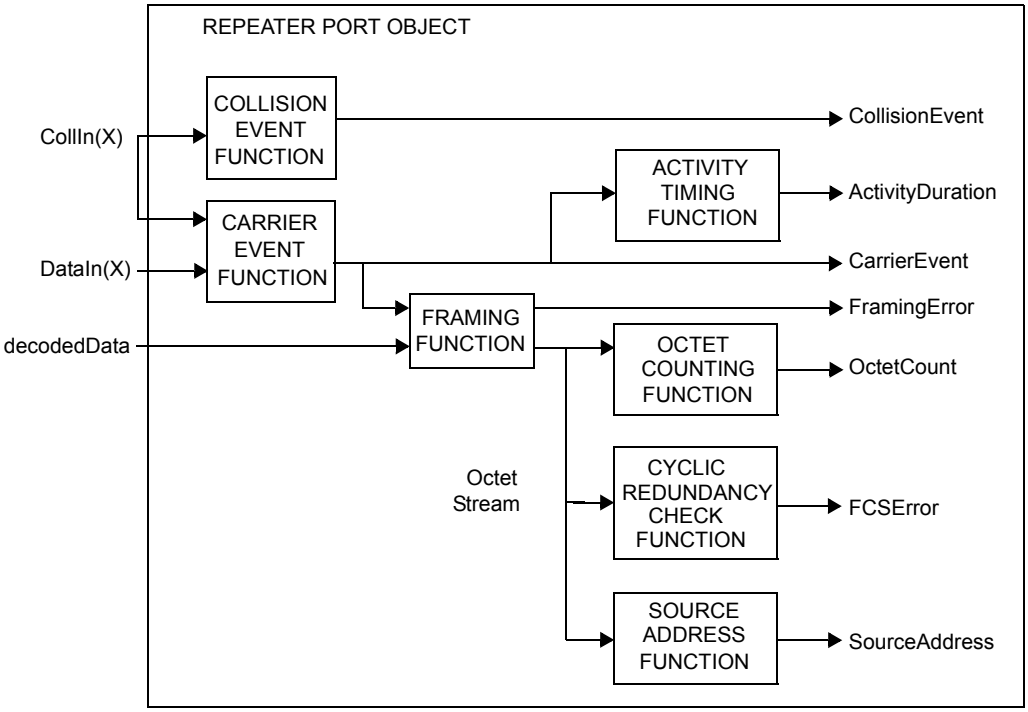


Figure 30–2—Functions relationship

Activity Timing function

The Activity Timing function measures the duration of the assertion of the CarrierEvent signal. For 10 Mb/s repeaters, this duration value must be adjusted by removing the value of Carrier Recovery Time (see 9.5.6.5) to obtain the true duration of activity on the network. The output of the Activity Timing function is the ActivityDuration value, which represents the duration of the CarrierEvent signal as expressed in units of bit times.

Carrier Event function

For 10 Mb/s repeaters the Carrier Event function for port N asserts the CarrierEvent signal when the repeater exits the IDLE state (see Figure 9–2) and the port has been determined to be port N. It deasserts the CarrierEvent signal when, for a duration of at least Carrier Recovery Time (see 9.5.6.5), both the DataIn(N) variable has the value II and the CollIn(N) variable has the value –SQE. The value N is the port assigned at the time of transition from the IDLE state. For 100 and 1000 Mb/s repeaters the Carrier Event function for port N asserts the CarrierEvent signal when the repeater exits the IDLE state of the repeater state diagram (Figure 27–2 and Figure 41–2) and the port has been determined to be port N. The Carrier Event function for Port N deasserts the CarrierEvent signal when the repeater enters the IDLE state of the repeater state diagram (Figure 27–2 and Figure 41–2).

Collision Event function

The Collision Event function asserts the CollisionEvent signal when a

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collision is detected at a repeater port. For a 10 Mb/s repeater port this is indicated by the CollIn(X) variable having the value SQE. For a 100 and 1000 Mb/s repeater port this is indicated by entering the COLLISION COUNT INCREMENT state of the partition state diagram (Figure 27–8 and Figure 41–4). The CollisionEvent signal remains asserted until the assertion of any CarrierEvent signal due to the reception of the following event.

Cyclic Redundancy Check function

The Cyclic Redundancy Check function verifies that the sequence of octets output by the Framing function contains a valid Frame Check Sequence Field. The Frame Check Sequence Field is the last four octets received from the output of the Framing function. The algorithm for generating an FCS from the octet stream is specified in 3.2.9. If the FCS generated according to this algorithm is not the same as the last four octets received from the Framing function, then the FCSError signal is asserted. The FCSError signal is cleared and the Cyclic Redundancy Check function is reinitialized upon the assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

Framing function

The Framing function recognizes the boundaries of an incoming frame by monitoring the CarrierEvent signal and the decoded data stream. Data bits are accepted while the CarrierEvent signal is asserted. The framing function delineates frames by stripping the Start of Packet delimiter (see 35.2.3.6), preamble, Start of frame delimiter, End of Packet delimiter (see 35.2.3.6), and any Carrier Extend from the received data stream. The remaining bits of each frame are aligned along octet boundaries. If there is not an integral number of octets, then FramingError shall be asserted. The FramingError signal is cleared upon the assertion of the CarrierEvent signal due to the reception of the following event. For 1000 Mb/s repeaters, the data stream shall continue until the end of the CarrierEvent signal or upon the recognition of a valid Start of Packet delimiter once the duration of the CarrierEvent is greater than or equal to slotTime. Such a Start of Packet delimiter will begin a new data stream.

Octet Counting function

The Octet Counting function counts the number of complete octets received from the output of the framing function. The output of the octet counting function is the OctetCount value. The OctetCount value is reset to zero upon the assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

Source Address function

The Source Address function extracts octets from the stream output by the framing function. The seventh through twelfth octets shall be extracted from the octet stream and output as the SourceAddress variable. The SourceAddress variable is set to an invalid state upon the

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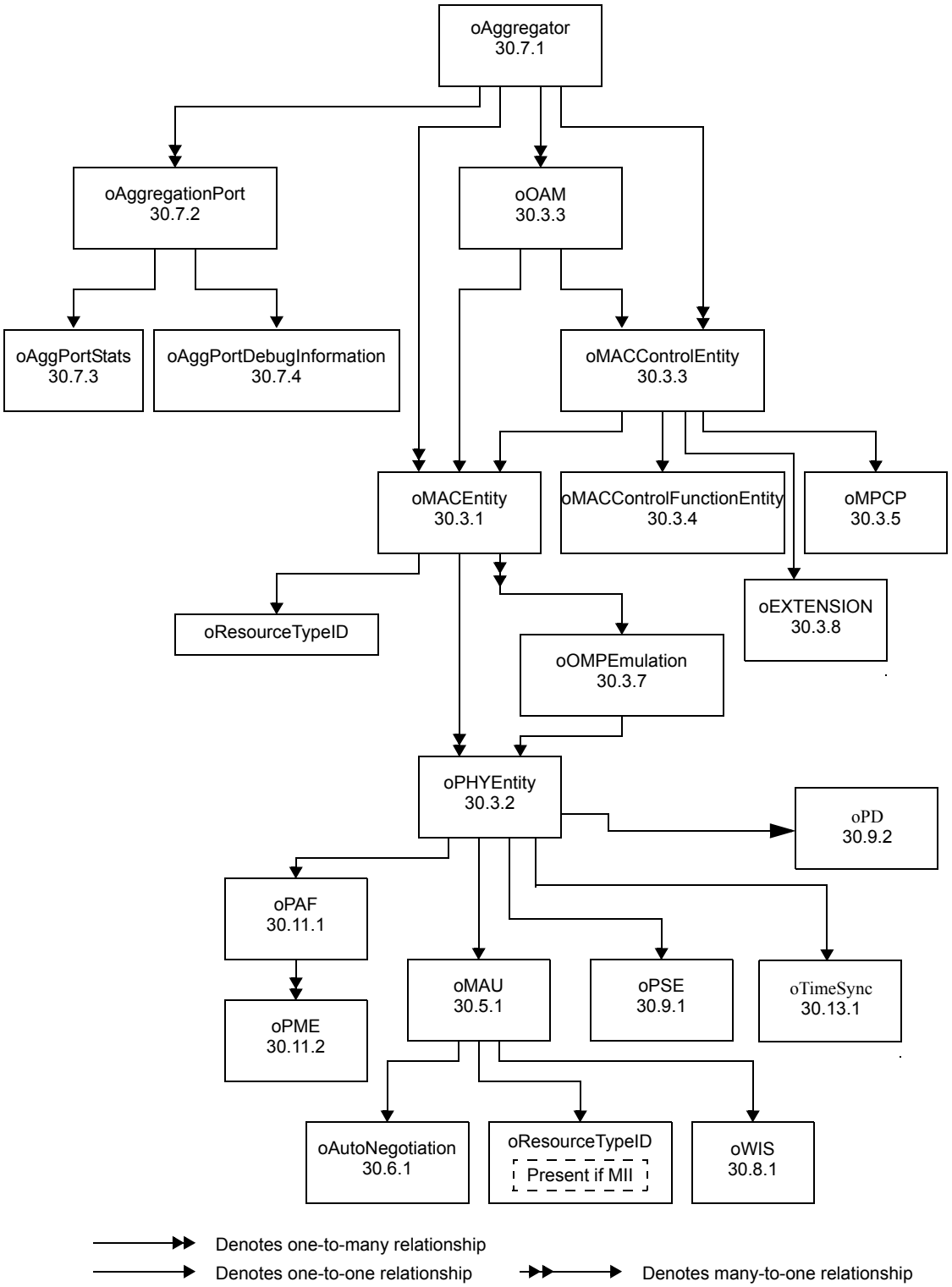
assertion of the CarrierEvent signal due to the reception of the following event and, additionally in the case of a frame burst on a 1000 Mb/s network, upon the recognition of a valid Start of Packet delimiter (see 35.2.3.6), once the duration of the CarrierEvent is greater than or equal to slotTime.

30.2.3 Containment

A containment relationship is a structuring relationship for managed objects in which the existence of a managed object is dependent on the existence of a containing managed object. The contained managed object is said to be the subordinate managed object, and the containing managed object the superior managed object. The containment relationship is used for naming managed objects. The local containment relationships among object classes are depicted in the entity relationship diagrams, Figure 30–3 through Figure 30–6. These figures show the names of the object classes and whether a particular containment relationship is one-to-one, one-to-many or many-to-one. For further requirements on this topic, see IEEE Std 802.1F-1993. PSE management is only valid in a system that provides management at the next higher containment level, that is, either a DTE, repeater or Midspan with management.

MAU management is only valid in a system that provides management at the next higher containment level, that is, either a DTE or repeater with management.

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Note—The objects oAggregator, oAggregationPort, oAggPortStats and oAggPortDebugInformation are deprecated by IEEE Std 802.1AX-2008.

Figure 30–3— DTE System entity relationship diagram

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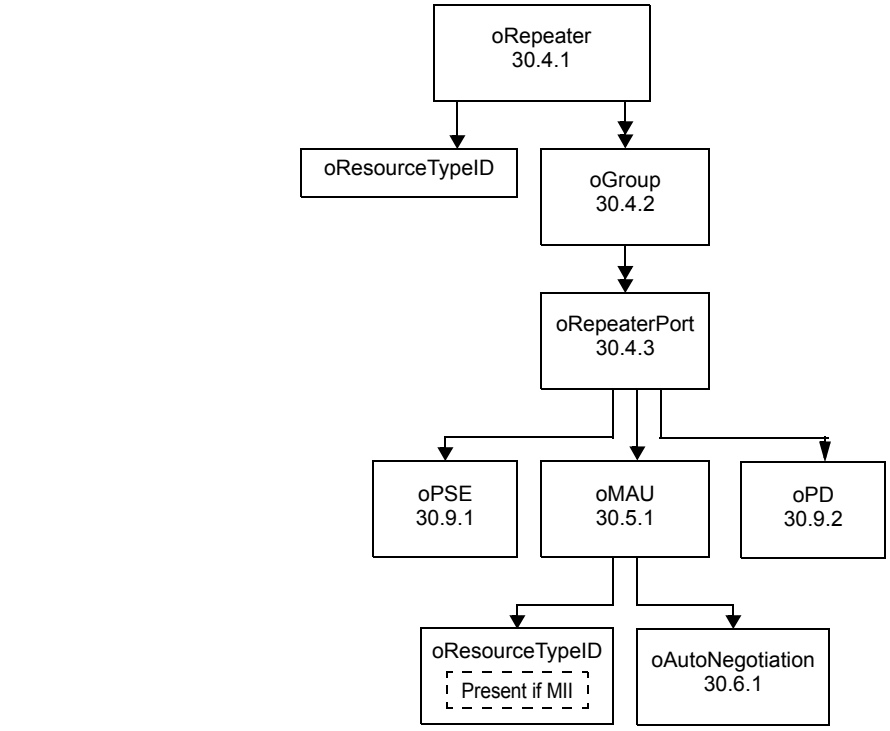


Figure 30–4—Repeater entity relationship diagram

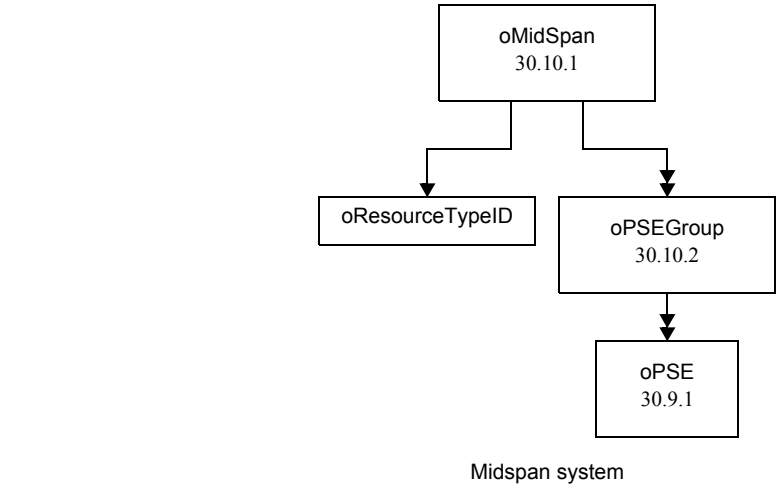


Figure 30–5—Midspan entity relationship diagram

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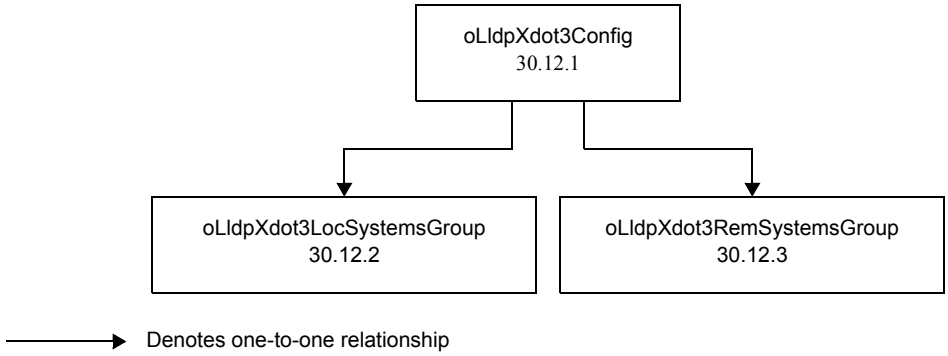


Figure 30–6—Link Layer Discovery Protocol entity relationship diagram

30.2.4 Naming

The name of an individual managed object is hierarchically defined within a managed system. For example, in the context of repeater management, a repeater port might be identified as "repeater 3, group 01, port 13," that is, port 13 of group 01 of a repeater with repeaterID 3 within the managed system.

In the case of MAU management, this will present itself in one of the two forms that are appropriate for a MAU's use, that is, as associated with a CSMA/CD interface of a DTE or with a particular port of a managed repeater. For example, a MAU could be identified as "repeater 3, group 01, port 13, MAU 1" or, that is, the MAU associated with port 13 of group 01 of a repeater with repeaterID 3 within the managed system. Examples of this are represented in the relationship of the naming attributes in the entity relationship diagram, Figure 30–3.

30.2.5 Capabilities

This standard makes use of the concept of *packages* as defined in ISO/IEC 10165-4:1992 as a means of grouping behaviour, attributes, actions, and notifications within a managed object class definition. Packages may either be mandatory, or be conditional, that is to say, present if a given condition is true. Within this standard *capabilities* are defined, each of which corresponds to a set of packages, which are components of a number of managed object class definitions and which share the same condition for presence. Implementation of the appropriate Basic and Mandatory packages is the minimum requirement for claiming conformance to IEEE 802.3 Management. Implementation of an entire optional capability is required in order to claim conformance to that capability. The capabilities and packages for IEEE 802.3 Management are specified in Table 30–1a through Table 30–7.

DTE Management has two packages that are required for management at the minimum conformance configuration—the Basic Package and the Mandatory Package. Systems that implement the optional MAC Control sublayer shall also implement the Basic and Mandatory Packages for the MAC Control Entity managed object class to claim DTE minimum conformance. For systems that include multiple PHY entities per MAC entity and implement the Multiple PHY Package to manage the selection of the active PHY, the optional Recommended Package shall be implemented. Systems that implement the optional Link Aggregation sublayer shall also implement the Basic and Mandatory Packages for the Aggregator and Aggregation Port managed object class to claim minimum DTE conformance.

For managed MAUs, the Basic Package is mandatory; all other packages are optional. For a managed MAU to be conformant to this standard, it shall fully implement the Basic Package. For a MAU to be conformant to an optional package it shall implement that entire package. While nonconformant (reference aMAUType

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= “other”) MAUs may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant MAU and conformant management. MAU Management is optional with respect to all other CSMA/CD Management. If an MII is present then the conditional MII Capability must be implemented. This provides the means to identify the vendor and type of the externally connected device.

There are two distinct aspects of Repeater Management.

The first aspect provides the means to monitor and control the functions of a repeater. These functions include, but are not limited to: identifying a repeater, testing and initializing a repeater, and enabling/ disabling a port. This is encompassed by the mandatory Basic Control Capability.

The second aspect provides the means to monitor traffic from attached segments, and to measure traffic sourced by DTEs connected to these segments. This is done by gathering statistics on packets that enter a repeater and maintaining those statistics on a per port basis. This is encompassed by the optional Performance Monitor Capability. The optional Address Tracking Capability provides the means to identify existence and movement of attached DTEs by their MAC addresses. While nonconformant (reference aRepeaterType = “other”) repeaters may utilize some or all of this clause to specify their management, conformance to this clause requires both a conformant repeater and conformant management.

If link Auto-Negotiation is present and managed, the Auto-Negotiation managed object class shall be implemented in its entirety. All attributes and actions are mandatory.

The 1000 Mb/s Burst Monitor Capability provides additional attributes that relate only to 1000 Mb/s operation, while the 100 Mb/s Monitor Capability has attributes that apply to a mixed 100 and 1000 Mb/s operation. These attributes are provided to complement the counter attributes of the optional packages and capabilities that apply to 10 Mb/s and mixed 10, 100, and 1000 Mb/s implementations. It is recommended that when the 100/1000 Mb/s Monitor Capability or 1000 Mb/s Burst Monitor Capability is implemented, the appropriate complementary counter packages and capabilities are also implemented.

For managed PSEs, the PSE Basic Package is mandatory and the PSE Recommended Package is optional. For managed PDs, the PD Basic Package is mandatory. For a managed PSE to be conformant to this standard, it shall fully implement the PSE Basic Package. For a managed PD to be conformant to this standard, it shall fully implement the PD Basic Package. For a managed PSE to be conformant to the optional Recommended Package it shall implement that entire package. PSE and PD management is optional with respect to all other CSMA/CD management.

For managed Midspans, the Midspan managed object class shall be implemented in its entirety. All attributes and notifications are mandatory. Midspan management is optional with respect to all other CSMA/ CD management.

For LLDP management, the LLDP Basic Package is mandatory. All other LLDP packages are conditional on the IEEE 802.3 Organizationally Specific TLVs supported and the LLDP operating mode (see IEEE Std 802.1AB, Clause 10).

LLDP MAC/PHY Configuration/Status Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “MAC/PHY Configuration/Status” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP MAC/PHY Config/Status Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “MAC/PHY Configuration/Status” and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Power via MDI Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Power via MDI” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Power via MDI Remote Package is mandatory for managed

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entities that support IEEE 802.3 Organizationally Specific TLV named “Power via MDI” and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Link Aggregation Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Link Aggregation” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Link Aggregation Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Link Aggregation” and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Max Frame Size Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named “Max Frame Size” and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Max Frame Size Remote Package is mandatory for managed entities that IEEE 802.3 Organizationally Specific TLV named “Max Frame Size” and are either in LLDP receive only mode or in LLDP transmit and receive mode. (See Table 30–7.)

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Table 30–1a—Capabilities

				DTE								Repeater					MAU						
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oResourceTypeID managed object																							
	aResourceTypeIDName	ATTRIBUTE	GET	X								X									X		
	aResourceInfo	ATTRIBUTE	GET	X								X									X		
oMACEntity managed object class (30.3.1)																							
	aMACID	ATTRIBUTE	GET	X																			
	aFramesTransmittedOK	ATTRIBUTE	GET		X																		
	aSingleCollisionFrames	ATTRIBUTE	GET		X																		
	aMultipleCollisionFrames	ATTRIBUTE	GET		X																		
	aFramesReceivedOK	ATTRIBUTE	GET		X																		
	aFrameCheckSequenceErrors	ATTRIBUTE	GET		X																		
	aAlignmentErrors	ATTRIBUTE	GET		X																		
	aOctetsTransmittedOK	ATTRIBUTE	GET			X																	
	aFramesWithDeferredXmissions	ATTRIBUTE	GET			X																	
	aLateCollisions	ATTRIBUTE	GET			X																	
	aFramesAbortedDueToXSColls	ATTRIBUTE	GET			X																	
	aFramesLostDueToIntMACXmitError	ATTRIBUTE	GET			X																	
	aCarrierSenseErrors	ATTRIBUTE	GET			X																	
	aOctetsReceivedOK	ATTRIBUTE	GET			X																	
	aFramesLostDueToIntMACRcvError	ATTRIBUTE	GET			X																	
	aPromiscuousStatus	ATTRIBUTE	GET-SET			X																	
	aReadMulticastAddressList	ATTRIBUTE	GET			X																	
	aMaxFrameLength	ATTRIBUTE	GET				X																
	aSlowProtocolFrameLimit	ATTRIBUTE	GET				X																
	aMulticastFramesXmittedOK	ATTRIBUTE	GET				X																
	aBroadcastFramesXmittedOK	ATTRIBUTE	GET				X																
	aFramesWithExcessiveDeferral	ATTRIBUTE	GET						X														
	aMulticastFramesReceivedOK	ATTRIBUTE	GET				X																
	aBroadcastFramesReceivedOK	ATTRIBUTE	GET				X																
	aInRangeLengthErrors	ATTRIBUTE	GET				X																
	aOutOfRangeLengthField	ATTRIBUTE	GET				X																
	aFrameTooLongErrors	ATTRIBUTE	GET				X																
	aMACEnableStatus	ATTRIBUTE	GET-SET				X																

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Table 30–1b—Capabilities

				DTE										Repeater					MAU				
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Energy-Efficient Ethernet (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oMACEntity managed object class (con'd.)																							
	aTransmitEnableStatus	ATTRIBUTE	GET-SET				X																
	aMulticastReceiveStatus	ATTRIBUTE	GET-SET				X																
	aReadWriteMACAddress	ATTRIBUTE	GET-SET				X																
	aCollisionFrames	ATTRIBUTE	GET					X															
	aMACCapabilities	ATTRIBUTE	GET		X[1]	X																	
	aDuplexStatus	ATTRIBUTE	GET-SET		X[1]	X																	
	aRateControlAbility	ATTRIBUTE	GET		X																		
	aRateControlStatus	ATTRIBUTE	GET-SET		X																		
	aDeferControlAbility	ATTRIBUTE	GET		X																		
	aDeferControlStatus	ATTRIBUTE	GET-SET		X																		
	acInitializeMAC	ACTION		X																			
	acAddGroupAddress	ACTION				X																	
	acDeleteGroupAddress	ACTION				X																	
	acExecuteSelfTest	ACTION					X																
oPHYEntity managed object class (30.3.2)																							
	aPHYID	ATTRIBUTE	GET	X																			
	aPHYType	ATTRIBUTE	GET	X																			
	aPHYTypeList	ATTRIBUTE	GET	X																			
	aSQETestErrors	ATTRIBUTE	GET			X																	
	aSymbolErrorDuringCarrier	ATTRIBUTE	GET								X												
	aMIIDetect	ATTRIBUTE	GET	X																			
	aPHYAdminState	ATTRIBUTE	GET	X																			
	acPHYAdminControl	ACTION								X													
	aTransmitLPIMicroseconds	ATTRIBUTE	GET									X											
	aReceiveLPIMicroseconds	ATTRIBUTE	GET									X											
	aTransmitLPITransitions	ATTRIBUTE	GET									X											
	aReceiveLPITransitions	ATTRIBUTE	GET									X											

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Table 30–1b—Capabilities *(continued)*

				DTE										Repeater				MAU					
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Energy-Efficient Ethernet (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oMACControlEntity managed object class (30.3.3)																							
	aMACControlID	ATTRIBUTE	GET		X																		
	aMACControlFunctionsSupported	ATTRIBUTE	GET-SET		X																		
	aMACControlFramesTransmitted	ATTRIBUTE	GET			X																	
	aMACControlFramesReceived	ATTRIBUTE	GET			X																	
	aUnsupportedOpcodesReceived	ATTRIBUTE	GET			X																	
	aPFCEnableStatus	ATTRIBUTE	GET		X[2]																		

NOTE 1: The aMACCapabilities and aDuplexStatus attributes are mandatory in systems that can operate in full duplex mode. They are recommended in systems that can operate only in half duplex mode.

NOTE 2: The aPFCenableStatus attribute is mandatory in systems that support the PFC MAC Control Function. It is optional in systems that do not support the PFC MAC Control Function.

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Table 30–1c—Capabilities

			DTE								Repeater					MAU					
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oMACControlFunctionEntity managed object class (30.3.4)																					
aPAUSELinkDelayAllowance	ATTRIBUTE	GET-SET		X																	
aPAUSEMACCtrlFramesTransmitted	ATTRIBUTE	GET			X																
aPAUSEMACCtrlFramesReceived	ATTRIBUTE	GET			X																
oEXTENSION managed object class (30.3.8)																					
aEXTENSIONMACCtrlFramesTrans-	ATTRIBUTE	GET			X																
aEXTENSIONMACCtrlFramesRe-	ATTRIBUTE	GET			X																
oRepeater managed object class (30.4.1)																					
aRepeaterID	ATTRIBUTE	GET									X										
aRepeaterType	ATTRIBUTE	GET									X										
aRepeaterGroupCapacity	ATTRIBUTE	GET									X										
aGroupMap	ATTRIBUTE	GET									X										
aRepeaterHealthState	ATTRIBUTE	GET									X										
aRepeaterHealthText	ATTRIBUTE	GET									X										
aRepeaterHealthData	ATTRIBUTE	GET									X										
aTransmitCollisions	ATTRIBUTE	GET										X									
acResetRepeater	ACTION										X										
acExecuteNonDisruptiveSelfTest	ACTION										X										
nRepeaterHealth	NOTIFICATION										X										
nRepeaterReset	NOTIFICATION										X										
nGroupMapChange	NOTIFICATION										X										
oGroup managed object class (30.4.2)																					
aGroupID	ATTRIBUTE	GET									X										
aGroupPortCapacity	ATTRIBUTE	GET									X										
aPortMap	ATTRIBUTE	GET									X										
nPortMapChange	NOTIFICATION										X										

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Table 30–1d—Capabilities

				DTE							Repeater					MAU						
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	Auto-Negotiation Package (mandatory)
oRepeaterPort managed object class (30.4.3)																							
	aPortID	ATTRIBUTE	GET									X											
	aPortAdminState	ATTRIBUTE	GET									X											
	aAutoPartitionState	ATTRIBUTE	GET									X											
	aReadableFrames	ATTRIBUTE	GET										X										
	aReadableOctets	ATTRIBUTE	GET										X										
	aFrameCheckSequenceErrors	ATTRIBUTE	GET										X										
	aAlignmentErrors	ATTRIBUTE	GET										X										
	aFramesTooLong	ATTRIBUTE	GET										X										
	aShortEvents	ATTRIBUTE	GET										X										
	aRunts	ATTRIBUTE	GET										X										
	aCollisions	ATTRIBUTE	GET										X										
	aLateEvents	ATTRIBUTE	GET										X										
	aVeryLongEvents	ATTRIBUTE	GET										X										
	aDataRateMismatches	ATTRIBUTE	GET										X										
	aAutoPartitions	ATTRIBUTE	GET										X										
	aIsolates	ATTRIBUTE	GET												X								
	aSymbolErrorDuringPacket	ATTRIBUTE	GET												X								
	aLastSourceAddress	ATTRIBUTE	GET											X									
	aSourceAddressChanges	ATTRIBUTE	GET											X									
	aBursts	ATTRIBUTE	GET													X							
	acPortAdminControl	ACTION										X											

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Table 30–1e—Capabilities

			DTE									Repeater					MAU										
			Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	10GBASE-T Operating Margin package (conditional)	Forward Error Correction Package (conditional)	Energy-Efficient Ethernet (optional)	Auto-Negotiation Package (mandatory)	
oMAU managed object class (30.5.1)																											
	aMAUID	ATTRIBUTE	GET													X											
	aMAUType	ATTRIBUTE	GET-SET													X											
	aMAUTypeList	ATTRIBUTE	GET													X											
	aMediaAvailable	ATTRIBUTE	GET													X											
	aLoseMediaCounter	ATTRIBUTE	GET															X									
	aJabber	ATTRIBUTE	GET													X											
	aMAUAdminState	ATTRIBUTE	GET													X											
	aBbMAUXmitRcvSplitType	ATTRIBUTE	GET																X								
	aBroadbandFrequencies	ATTRIBUTE	GET																X								
	aFalseCarriers	ATTRIBUTE	GET																		X						
	aBIPErrorCount	ATTRIBUTE	GET																		X						
	aLaneMapping	ATTRIBUTE	GET																		X						
	aRSFECBIPErrorCount	ATTRIBUTE	GET																		X						
	aRSFECLaneMapping	ATTRIBUTE	GET																		X						
	aIdleErrorCount	ATTRIBUTE	GET																		X						
	aFECAbility	ATTRIBUTE	GET																				X				
	aFECmode	ATTRIBUTE	GET-SET																				X				
	aFECCorrectedBlocks	ATTRIBUTE	GET																				X				
	aFECUncorrectableBlocks	ATTRIBUTE	GET																				X				
	aRSFECBypassAbility	ATTRIBUTE	GET																				X				
	aRSFECIndicationAbility	ATTRIBUTE	GET																				X				
	aRSFECBypassEnable	ATTRIBUTE	GET-SET																				X				
	aRSFECIndicationEnable	ATTRIBUTE	GET-SET																				X				
	aSNROpMarginChnlA	ATTRIBUTE	GET																			X					
	aSNROpMarginChnlB	ATTRIBUTE	GET																			X					
	aSNROpMarginChnlC	ATTRIBUTE	GET																			X					
	aSNROpMarginChnlD	ATTRIBUTE	GET																			X					
	acResetMAU	ACTION															X										
	acMAUAdminControl	ACTION															X										
	nJabber	NOTIFICATION														X											
	aLDFastRetrainCount	ATTRIBUTE	GET																						X		
	aLPFastRetrainCount	ATTRIBUTE	GET																						X		

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Table 30–1e—Capabilities *(continued)*

				DTE									Repeater					MAU									
				Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Array Package (optional)	Excessive Deferral Package (optional)	Multiple PHY Package (optional)	PHY Error Monitor Capability (optional)	Basic Control Capability (mandatory)	Performance Monitor Capability (optional)	Address Tracking Capability (optional)	100/1000 Mb/s Monitor Capability (optional)	1000 Mb/s Burst Monitor Capability (optional)	Basic Package (mandatory)	MAU Control Package (optional)	Media Loss Tracking Package (conditional)	Broadband DTE MAU Package (conditional)	MII Capability (conditional)	PHY Error Monitor Capability (optional)	10GBASE-T Operating Margin package (conditional)	Forward Error Correction Package (conditional)	Energy-Efficient Ethernet (optional)	Auto-Negotiation Package (mandatory)
oAuto-Negotiation managed object class (30.6.1)																											
	aAutoNegID	ATTRIBUTE	GET																								X
	aAutoNegAdminState	ATTRIBUTE	GET																								X
	aAutoNegRemoteSignaling	ATTRIBUTE	GET																								X
	aAutoNegAutoConfig	ATTRIBUTE	GET-SET																								X
	aAutoNegLocalTechnologyAbility	ATTRIBUTE	GET																								X
	aAutoNegAdvertisedTechnologyAbil-	ATTRIBUTE	GET-SET																								X
	aAutoNegReceivedTechnologyAbility	ATTRIBUTE	GET																								X
	aAutoNegLocalSelectorAbility	ATTRIBUTE	GET																								X
	aAutoNegAdvertisedSelectorAbility	ATTRIBUTE	GET-SET																								X
	aAutoNegReceivedSelectorAbility	ATTRIBUTE	GET																								X
	acAutoNegRestartAutoConfig	ACTION																									X
	acAutoNegAdminControl	ACTION																									X
Common Attributes Template																											
	aCMCounter	ATTRIBUTE	GET		X	X	X		X		X		X	X	X			X	X			X					

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Table 30–2—Link Aggregation capabilities

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
oAggregator (30.7.1) NOTE—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggID	ATTRIBUTE	GET	X					
	aAggDescription	ATTRIBUTE	GET		X				
	aAggName	ATTRIBUTE	GET-SET		X				
	aAggActorSystemID	ATTRIBUTE	GET-SET		X				
	aAggActorSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggAggregateOrIndividual	ATTRIBUTE	GET		X				
	aAggActorAdminKey	ATTRIBUTE	GET-SET		X				
	aAggActorOperKey	ATTRIBUTE	GET		X				
	aAggMACAddress	ATTRIBUTE	GET		X				
	aAggPartnerSystemID	ATTRIBUTE	GET		X				
	aAggPartnerSystemPriority	ATTRIBUTE	GET		X				
	aAggPartnerOperKey	ATTRIBUTE	GET		X				
	aAggAdminState	ATTRIBUTE	GET-SET		X				
	aAggOperState	ATTRIBUTE	GET		X				
	aAggTimeOfLastOperChange	ATTRIBUTE	GET		X				
	aAggDataRate	ATTRIBUTE	GET		X				
	aAggOctetsTxOK	ATTRIBUTE	GET			X			
	aAggOctetsRxOK	ATTRIBUTE	GET			X			
	aAggFramesTxOK	ATTRIBUTE	GET		X				
	aAggFramesRxOK	ATTRIBUTE	GET		X				
	aAggMulticastFramesTxOK	ATTRIBUTE	GET				X		
	aAggMulticastFramesRxOK	ATTRIBUTE	GET				X		
	aAggBroadcastFramesTxOK	ATTRIBUTE	GET				X		
	aAggBroadcastFramesRxOK	ATTRIBUTE	GET				X		
	aAggFramesDiscardedOnTx	ATTRIBUTE	GET			X			
	aAggFramesDiscardedOnRx	ATTRIBUTE	GET			X			
	aAggFramesWithTxErrors	ATTRIBUTE	GET			X			

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Table 30–2—Link Aggregation capabilities *(continued)*

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
	aAggFramesWithRxErrors	ATTRIBUTE	GET			X			
	aAggUnknownProtocolFrames	ATTRIBUTE	GET			X			
	aAggLinkUpDownNotificationEnable	ATTRIBUTE	GET-SET		X				
	nAggLinkUpNotification	NOTIFICATION			X				
	nAggLinkDownNotification	NOTIFICATION			X				
	aAggPortList	ATTRIBUTE	GET			X			
	aAggCollectorMaxDelay	ATTRIBUTE	GET-SET		X				
oAggregationPort (30.7.2) NOTE—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggPortID	ATTRIBUTE	GET	X					
	aAggPortActorSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggPortActorSystemID	ATTRIBUTE	GET		X				
	aAggPortActorAdminKey	ATTRIBUTE	GET-SET		X				
	aAggPortActorOperKey	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminSystemPriority	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperSystemPriority	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminSystemID	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperSystemID	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminKey	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperKey	ATTRIBUTE	GET		X				
	aAggPortSelectedAggID	ATTRIBUTE	GET		X				
	aAggPortAttachedAggID	ATTRIBUTE	GET		X				
	aAggPortActorPort	ATTRIBUTE	GET		X				
	aAggPortActorPortPriority	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerAdminPort	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperPort	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminPortPriority	ATTRIBUTE	GET-SET		X				

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Table 30–2—Link Aggregation capabilities *(continued)*

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
	aAggPortPartnerOperPortPriority	ATTRIBUTE	GET		X				
	aAggPortActorAdminState	ATTRIBUTE	GET-SET		X				
	aAggPortActorOperState	ATTRIBUTE	GET		X				
	aAggPortPartnerAdminState	ATTRIBUTE	GET-SET		X				
	aAggPortPartnerOperState	ATTRIBUTE	GET		X				
	aAggPortAggregateOrIndividual	ATTRIBUTE	GET		X				
oAggPortStats (30.7.3) Note—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggPortStatsID	ATTRIBUTE	GET					X	
	aAggPortStatsLACPDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerPDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerResponsePDUsRx	ATTRIBUTE	GET					X	
	aAggPortStatsUnknownRx	ATTRIBUTE	GET					X	
	aAggPortStatsIllegalRx	ATTRIBUTE	GET					X	
	aAggPortStatsLACPDUsTx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerPDUsTx	ATTRIBUTE	GET					X	
	aAggPortStatsMarkerResponsePDUsTx	ATTRIBUTE	GET					X	
oAggPortDebugInformation (30.7.4) Note—This object is deprecated by IEEE Std 802.1AX-2008									
	aAggPortDebugInformationID	ATTRIBUTE	GET						X
	aAggPortDebugRxState	ATTRIBUTE	GET						X
	aAggPortDebugLastRxTime	ATTRIBUTE	GET						X
	aAggPortDebugMuxState	ATTRIBUTE	GET						X
	aAggPortDebugMuxReason	ATTRIBUTE	GET						X
	aAggPortDebugActorChurnState	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChurnState	ATTRIBUTE	GET						X
	aAggPortDebugActorChurnCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChurnCount	ATTRIBUTE	GET						X

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Table 30–2—Link Aggregation capabilities *(continued)*

				DTE					
	Object name	Object type	Operations supported	Basic Package (mandatory)	Mandatory Package (mandatory)	Recommended Package (optional)	Optional Package (optional)	Aggregation Port Statistics (optional)	Aggregation Port Debug Information (optional)
	aAggPortDebugActorSyncTransitionCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerSyncTransitionCount	ATTRIBUTE	GET						X
	aAggPortDebugActorChangeCount	ATTRIBUTE	GET						X
	aAggPortDebugPartnerChangeCount	ATTRIBUTE	GET						X
Common Attributes Template									
	aCMCounter	ATTRIBUTE	GET		X	X	X	X	X

Table 30–3—WIS capabilities

				WIS Basic Package (mandatory)	WIS Recommended Package (optional)
oWIS managed object class (30.8.1)					
	aWISID	ATTRIBUTE	GET	**X**	
	aSectionStatus	ATTRIBUTE	GET	**X**	
	aSectionSESThreshold	ATTRIBUTE	GET-SET		**X**
	aSectionSESs	ATTRIBUTE	GET		**X**
	aSectionESs	ATTRIBUTE	GET		**X**
	aSectionSEFSs	ATTRIBUTE	GET		**X**
	aSectionCVs	ATTRIBUTE	GET		**X**
	aJ0ValueTX	ATTRIBUTE	GET-SET		**X**
	aJ0ValueRX	ATTRIBUTE	GET		**X**
	aLineStatus	ATTRIBUTE	GET	**X**	

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Table 30–3—WIS capabilities

				WIS Basic Package (mandatory)	WIS Recommended Package (optional)
	aLineSESThreshold	ATTRIBUTE	GET-SET		X
	aLineSESs	ATTRIBUTE	GET		X
	aLineESs	ATTRIBUTE	GET		X
	aLineCVs	ATTRIBUTE	GET		X
	aFarEndLineSESs	ATTRIBUTE	GET		X
	aFarEndLineESs	ATTRIBUTE	GET		X
	aFarEndLineCVs	ATTRIBUTE	GET		X
	aPathStatus	ATTRIBUTE	GET	X	
	aPathSESThreshold	ATTRIBUTE	GET-SET		X
	aPathSESs	ATTRIBUTE	GET		X
	aPathESs	ATTRIBUTE	GET		X
	aPathCVs	ATTRIBUTE	GET		X
	aJ1ValueTX	ATTRIBUTE	GET-SET		X
	aJ1ValueRX	ATTRIBUTE	GET		X
	aFarEndPathStatus	ATTRIBUTE	GET	X	
	aFarEndPathSESs	ATTRIBUTE	GET		X
	aFarEndPathESs	ATTRIBUTE	GET		X
	aFarEndPathCVs	ATTRIBUTE	GET		X
Common Attributes Template					
	aCMCounter	ATTRIBUTE	GET		X

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Table 30–4—DTE Power via MDI capabilities

				PSE Basic Package (mandatory)	PSE Recommended Package (optional)	Midspan Basic Capability (mandatory)	PD Basic Package (mandatory)
oResourceTypeID managed object							
	aResourceTypeIDName	ATTRIBUTE	GET			X	
	aResourceInfo	ATTRIBUTE	GET			X	
oMidSpan managed object class (30.10.1)							
	aMidSpanID	ATTRIBUTE	GET			X	
	aMidSpanPSEGroupCapacity	ATTRIBUTE	GET			X	
	aMidSpanPSEGroupMap	ATTRIBUTE	GET			X	
	nMidSpanPSEGroupMapChange	NOTIFICATION				X	
oPSEGroup managed object class (30.10.2)							
	aPSEGroupID	ATTRIBUTE	GET			X	
	aPSECapacity	ATTRIBUTE	GET			X	
	aPSEMap	ATTRIBUTE	GET			X	
	nPSEMapChange	NOTIFICATION				X	
oPSE managed object class (30.9.1)							
	aPSEID	ATTRIBUTE	GET	X			
	aPSEAdminState	ATTRIBUTE	GET	X			
	aPSEPowerPairsControlAbility	ATTRIBUTE	GET	X			
	aPSEPowerPairs	ATTRIBUTE	GET-SET	X			
	aPSEPowerDetectionStatus	ATTRIBUTE	GET	X			
	aPSEPowerClassification	ATTRIBUTE	GET		X		
	aPSEInvalidSignatureCounter	ATTRIBUTE	GET		X		
	aPSEPowerDeniedCounter	ATTRIBUTE	GET		X		
	aPSEOverLoadCounter	ATTRIBUTE	GET		X		
	aPSEShortCounter	ATTRIBUTE	GET		X		
	aPSEMPSAbsentCounter	ATTRIBUTE	GET		X		
	acPSEAdminControl	ACTION		X			
	aPSEActualPower	ATTRIBUTE	GET		X		
	aPSEPowerAccuracy	ATTRIBUTE	GET		X		
	aPSECumulativeEnergy	ATTRIBUTE	GET		X		
oPD managed object class (30.9.2)							
	aPDID	ATTRIBUTE	GET				X
Common Attributes Template							
	aCMCounter	ATTRIBUTE	GET		X		

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Table 30–5—EFM capabilities

				DTE				MAU		PME		
				Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
oMPCP managed object class (30.3.5)												
	aMPCPID	ATTRIBUTE	GET	X								
	aMPCPAdminState	ATTRIBUTE	GET	X								
	aMPCPMode	ATTRIBUTE	GET	X								
	aMPCPLinkID	ATTRIBUTE	GET	X								
	aMPCPRemoteMACAddress	ATTRIBUTE	GET	X								
	aMPCPRegistrationState	ATTRIBUTE	GET	X								
	aMPCPMACCtrlFramesTransmitted	ATTRIBUTE	GET	X								
	aMPCPMACCtrlFramesReceived	ATTRIBUTE	GET	X								
	aMPCPTxGate	ATTRIBUTE	GET	X								
	aMPCPTxRegAck	ATTRIBUTE	GET	X								
	aMPCPTxRegister	ATTRIBUTE	GET	X								
	aMPCPTxRegRequest	ATTRIBUTE	GET	X								
	aMPCPTxReport	ATTRIBUTE	GET	X								
	aMPCPRxGate	ATTRIBUTE	GET	X								
	aMPCPRxRegAck	ATTRIBUTE	GET	X								
	aMPCPRxRegister	ATTRIBUTE	GET	X								
	aMPCPRxRegRequest	ATTRIBUTE	GET	X								
	aMPCPRxReport	ATTRIBUTE	GET	X								
	aMPCPTransmitElapsed	ATTRIBUTE	GET	X								
	aMPCPReceiveElapsed	ATTRIBUTE	GET	X								
	aMPCPRoundTripTime	ATTRIBUTE	GET	X								
	aMPCPDiscoveryWindowsSent	ATTRIBUTE	GET	X								
	aMPCPDiscoveryTimeout	ATTRIBUTE	GET	X								
	aMPCPMaximumPendingGrants	ATTRIBUTE	GET	X								
	aMPCPRecognizedMulticastIDs	ATTRIBUTE	GET	X								
	acMPCPAdminControl	ACTION		X								

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Table 30–5—EFM capabilities *(continued)*

			DTE				MAU		PME		
			Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
oOAM managed object class (30.3.6)											
aMACControlID	ATTRIBUTE	GET		X							
aOAMAdminState	ATTRIBUTE	GET		X							
aOAMDiscoveryState	ATTRIBUTE	GET		X							
aOAMRemoteMACAddress	ATTRIBUTE	GET		X							
aOAMLocalConfiguration	ATTRIBUTE	GET		X							
aOAMRemoteConfiguration	ATTRIBUTE	GET		X							
aOAMLocalPDUConfiguration	ATTRIBUTE	GET		X							
aOAMRemotePDUConfiguration	ATTRIBUTE	GET		X							
aOAMLocalFlagsField	ATTRIBUTE	GET		X							
aOAMRemoteFlagsField	ATTRIBUTE	GET		X							
aOAMLocalRevision	ATTRIBUTE	GET		X							
aOAMRemoteRevision	ATTRIBUTE	GET		X							
aOAMLocalState	ATTRIBUTE	GET		X							
aOAMRemoteState	ATTRIBUTE	GET		X							
aOAMRemoteVendorOUI	ATTRIBUTE	GET		X							
aOAMRemoteVendorSpecificInfo	ATTRIBUTE	GET		X							
aOAMUnsupportedCodesTx	ATTRIBUTE	GET		X							
aUnsupportedOpcodesReceived	ATTRIBUTE	GET		X							
aOAMInformationTx	ATTRIBUTE	GET		X							
aOAMInformationRx	ATTRIBUTE	GET		X							
aOAMUniqueEventNotificationTx	ATTRIBUTE	GET		X							
aOAMDuplicateEventNotificationTx	ATTRIBUTE	GET		X							
aOAMUniqueEventNotificationRx	ATTRIBUTE	GET		X							
aOAMDuplicateEventNotificationRx	ATTRIBUTE	GET		X							
aOAMLoopbackControlTx	ATTRIBUTE	GET		X							
aOAMLoopbackControlRx	ATTRIBUTE	GET		X							
aOAMVariableRequestTx	ATTRIBUTE	GET		X							
aOAMVariableRequestRx	ATTRIBUTE	GET		X							
aOAMVariableResponseTx	ATTRIBUTE	GET		X							
aOAMVariableResponseRx	ATTRIBUTE	GET		X							

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Table 30–5—EFM capabilities *(continued)*

			DTE				MAU		PME		
			Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
aOAMOrganizationSpecificTx	ATTRIBUTE	GET		X							
aOAMOrganizationSpecificRx	ATTRIBUTE	GET		X							
aOAMLocalErrSymPeriodConfig	ATTRIBUTE	GET		X							
aOAMLocalErrSymPeriodEvent	ATTRIBUTE	GET		X							
aOAMLocalErrFrameConfig	ATTRIBUTE	GET		X							
aOAMLocalErrFrameEvent	ATTRIBUTE	GET		X							
aOAMLocalErrFramePeriodConfig	ATTRIBUTE	GET		X							
aOAMLocalErrFramePeriodEvent	ATTRIBUTE	GET		X							
aOAMLocalErrFrameSecsSummaryConfig	ATTRIBUTE	GET		X							
aOAMLocalErrFrameSecsSummaryEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrSymPeriodEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrFrameEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrFramePeriodEvent	ATTRIBUTE	GET		X							
aOAMRemoteErrFrameSecsSummaryEvent	ATTRIBUTE	GET		X							
aFramesLostDueToOAMError	ATTRIBUTE	GET		X							
acOAMAdminControl	ACTION			X							
oOMPEmulation managed object class (30.3.7)											
aOMPEmulationID	ATTRIBUTE	GET			X						
aOMPEmulationType	ATTRIBUTE	GET			X						
aSLDErrors	ATTRIBUTE	GET			X						
aCRC8Errors	ATTRIBUTE	GET			X						
aGoodLLID	ATTRIBUTE	GET				X					
aONUPONcastLLID	ATTRIBUTE	GET				X					
aOLTPONcastLLID	ATTRIBUTE	GET				X					
aBadLLID	ATTRIBUTE	GET				X					
oMAU managed object class (30.5.1)											
aPCSCodingViolation	ATTRIBUTE	GET					X				
aFECAbility	ATTRIBUTE	GET						X			
aFECmode	ATTRIBUTE	GET-SET						X			
aFECCorrectedBlocks	ATTRIBUTE	GET						X			
aFECUncorrectableBlocks	ATTRIBUTE	GET						X			

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Table 30–5—EFM capabilities *(continued)*

			DTE				MAU		PME		
			Multipoint Control Protocol Package (conditional)	Operation Administration Maintenance Package (conditional)	Optical Multipoint Emulation Package (conditional)	Optical Multipoint Emulation Monitor Package (optional)	PCS Code Error Monitor Package (optional)	Forward Error Correction Package (conditional)	Basic Package (mandatory)	PME Aggregation Package (optional)	10P/2B Package (mandatory)
oPAF managed object class (30.11.1)											
aPAFID	ATTRIBUTE	GET							X		
aPhyEnd	ATTRIBUTE	GET							X		
aPHYCurrentStatus	ATTRIBUTE	GET							X		
aPAFSupported	ATTRIBUTE	GET							X		
aPAFAdminState	ATTRIBUTE	GET-SET								X	
aLocalPAFCapacity	ATTRIBUTE	GET								X	
aLocalPMEAvailable	ATTRIBUTE	GET								X	
aLocalPMEAggregate	ATTRIBUTE	GET								X	
aRemotePAFSupported	ATTRIBUTE	GET								X	
aRemotePAFCapacity	ATTRIBUTE	GET								X	
aRemotePMEAggregate	ATTRIBUTE	GET								X	
oPME managed object class (30.11.2)											
aPMEID	ATTRIBUTE	GET									X
aPMEAdminState	ATTRIBUTE	GET-SET									X
aPMEStatus	ATTRIBUTE	GET									X
aPMESNRMgn	ATTRIBUTE	GET									X
aTCCodingViolations	ATTRIBUTE	GET									X
aProfileSelect	ATTRIBUTE	GET-SET									X
aOperatingProfile	ATTRIBUTE	GET									X
aPMEFECCorrectedBlocks	ATTRIBUTE	GET									X
aPMEFECUncorrectableBlocks	ATTRIBUTE	GET									X
aTCCRCErrors	ATTRIBUTE	GET									X
Common Attributes Template											
aCMCounter	ATTRIBUTE	GET	X	X	X	X	X	X		X	X

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Table 30–6—TimeSync Capabilities

				Support for Time Sync(mandatory)
oTimeSync managed object				
	aTimeSyncCapabilityTX	ATTRIBUTE	GET	X
	aTimeSyncCapabilityRX	ATTRIBUTE	GET	X
	aTimeSyncDelayTXmax	ATTRIBUTE	GET	X
	aTimeSyncDelayTXmin	ATTRIBUTE	GET	X
	aTimeSyncDelayRXmax	ATTRIBUTE	GET	X
	aTimeSyncDelayRXmin	ATTRIBUTE	GET	X

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Table 30–7—LLDP capabilities

			LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
oLldpXdot3Config managed object class (30.12.1)													
aLldpXdot3PortConfigTLVsTxEnable	ATTRIBUTE	GET-SET	X										
oLldpXdot3LocSystemsGroup managed object class (30.12.2)													
aLldpXdot3LocPortAutoNegSupported	ATTRIBUTE	GET		X									
aLldpXdot3LocPortAutoNegEnabled	ATTRIBUTE	GET		X									
aLldpXdot3LocPortAutoNegAdvertisedCap	ATTRIBUTE	GET		X									
aLldpXdot3LocPortOperMauType	ATTRIBUTE	GET		X									
aLldpXdot3LocPowerPortClass	ATTRIBUTE	GET				X							
aLldpXdot3LocPowerMDISupported	ATTRIBUTE	GET				X							
aLldpXdot3LocPowerMDIEnabled	ATTRIBUTE	GET				X							
aLldpXdot3LocPowerPairControlable	ATTRIBUTE	GET				X							
aLldpXdot3LocPowerPairs	ATTRIBUTE	GET				X							
aLldpXdot3LocPowerClass	ATTRIBUTE	GET				X							
aLldpXdot3LocLinkAggStatus	ATTRIBUTE	GET						X					
aLldpXdot3LocLinkAggPortId	ATTRIBUTE	GET						X					
aLldpXdot3LocMaxFrameSize	ATTRIBUTE	GET								X			
aLldpXdot3LocPowerType	ATTRIBUTE	GET				X							
aLldpXdot3LocPowerSource	ATTRIBUTE	GET				X							
aLldpXdot3LocPowerPriority	ATTRIBUTE	GET-SET				X							
aLldpXdot3LocPDRequestedPowerValue	ATTRIBUTE	GET				X							
aLldpXdot3LocPSEAllocatedPowerValue	ATTRIBUTE	GET				X							
aLldpXdot3LocResponseTime	ATTRIBUTE	GET				X							
aLldpXdot3LocReady	ATTRIBUTE	GET				X							
aLldpXdot3LocReducedOperationPowerValue	ATTRIBUTE	GET				X							
aLldpXdot3LocTxTwSys	ATTRIBUTE	GET										X	
aLldpXdot3LocTxTwSysEcho	ATTRIBUTE	GET										X	
aLldpXdot3LocRxTwSys	ATTRIBUTE	GET										X	
aLldpXdot3LocRxTwSysEcho	ATTRIBUTE	GET										X	
aLldpXdot3LocFbTwSys	ATTRIBUTE	GET										X	
aLldpXdot3TxDllReady	ATTRIBUTE	GET										X	

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Table 30–7—LLDP capabilities *(continued)*

				LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
	aLldpXdot3RxDllReady	ATTRIBUTE	GET										X	
	aLldpXdot3LocDllEnabled	ATTRIBUTE	GET										X	
	aLldpXdot3LocTxFw	ATTRIBUTE	GET										X	
	aLldpXdot3LocTxFwEcho	ATTRIBUTE	GET										X	
	aLldpXdot3LocRxFw	ATTRIBUTE	GET										X	
	aLldpXdot3LocRxFwEcho	ATTRIBUTE	GET										X	
oLldpXdot3RemSystemsGroup managed object class (30.12.3)														

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Table 30–7—LLDP capabilities *(continued)*

				LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)	LLDP EEE Local Package (optional)	LLDP EEE Remote Package (optional)
	aLldpXdot3RemPortAutoNegSupported	ATTRIBUTE	GET			X								
	aLldpXdot3RemPortAutoNegEnabled	ATTRIBUTE	GET			X								
	aLldpXdot3RemPortAutoNegAdvertisedCap	ATTRIBUTE	GET			X								
	aLldpXdot3RemPortOperMauType	ATTRIBUTE	GET			X								
	aLldpXdot3RemPowerPortClass	ATTRIBUTE	GET					X						
	aLldpXdot3RemPowerMDISupported	ATTRIBUTE	GET					X						
	aLldpXdot3RemPowerMDIEnabled	ATTRIBUTE	GET					X						
	aLldpXdot3RemPowerPairControlable	ATTRIBUTE	GET					X						
	aLldpXdot3RemPowerPairs	ATTRIBUTE	GET					X						
	aLldpXdot3RemPowerClass	ATTRIBUTE	GET					X						
	aLldpXdot3RemLinkAggStatus	ATTRIBUTE	GET							X				
	aLldpXdot3RemLinkAggPortId	ATTRIBUTE	GET							X				
	aLldpXdot3RemMaxFrameSize	ATTRIBUTE	GET									X		
	aLldpXdot3RemPowerType	ATTRIBUTE	GET					X						
	aLldpXdot3RemPowerSource	ATTRIBUTE	GET					X						
	aLldpXdot3RemPowerPriority	ATTRIBUTE	GET					X						
	aLldpXdot3RemPDRequestedPowerValue	ATTRIBUTE	GET					X						
	aLldpXdot3RemPSEAllocatedPowerValue	ATTRIBUTE	GET					X						
	aLldpXdot3RemTxTwSys	ATTRIBUTE	GET											X
	aLldpXdot3RemTxTwSysEcho	ATTRIBUTE	GET											X
	aLldpXdot3RemRxTwSys	ATTRIBUTE	GET											X
	aLldpXdot3RemRxTwSysEcho	ATTRIBUTE	GET											X
	aLldpXdot3RemFbTwSys	ATTRIBUTE	GET											X
	aLldpXdot3RemTxFw	ATTRIBUTE	GET											X
	aLldpXdot3RemTxFwEcho	ATTRIBUTE	GET											X
	aLldpXdot3RemRxFw	ATTRIBUTE	GET											X
	aLldpXdot3RemRxFwEcho	ATTRIBUTE	GET											X

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30.3 Layer management for DTEs

30.3.1 MAC entity managed object class

This subclause formally defines the behaviours for the oMACEntity managed object class attributes, actions, and notifications.

30.3.1.1 MAC entity attributes

30.3.1.1.1 aMACID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMACID is assigned so as to uniquely identify a MAC among the subordinate managed objects of the containing object.;

30.3.1.1.2 aFramesTransmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.3 aSingleCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are involved in a single collision, and are subsequently transmitted successfully. This counter is incremented when the result of a transmission is reported as transmitOK and the attempt value is 2. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.4 aMultipleCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 11 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are involved in more than one collision and are subsequently transmitted

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successfully. This counter is incremented when the TransmitStatus is reported as transmitOK and the value of the attempts variable is greater than 2 and less or equal to attemptLimit. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.5 aFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received (receiveOK). This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the ReceiveStatus is reported as receiveOK. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.6 aFrameCheckSequenceErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of receive frames that are an integral number of octets in length and do not pass the FCS check. This does not include frames received with frame-too-long, or frame-too-short (frame fragment) error. This counter is incremented when the ReceiveStatus is reported as frameCheckError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

NOTE—Coding errors detected by the Physical Layer for speeds above 10 Mb/s will cause the frame to fail the FCS check.;

30.3.1.1.7 aAlignmentErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are not an integral number of octets in length and do not pass the FCS check. This counter is incremented when the ReceiveStatus is reported as alignmentError. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3). This counter will not increment for group encoding schemes encoding greater than 4 bits per group.;

30.3.1.1.8 aOctetsTransmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s

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BEHAVIOUR DEFINED AS:

A count of data and padding octets of frames that are successfully transmitted. This counter is incremented when the TransmitStatus is reported as transmitOK. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.9 aFramesWithDeferredXmissions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames whose transmission was delayed on its first attempt because the medium was busy. This counter is incremented when the Boolean variable deferred has been asserted by the TransmitLinkMgmt function (4.2.8). Frames involved in any collisions are not counted. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.10 aLateCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of the times that a collision has been detected later than one slotTime from the start of the packet transmission. A late collision is counted twice, i.e., both as a collision and as a lateCollision. This counter is incremented when the lateCollisionCount variable is nonzero. The actual update is incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.11 aFramesAbortedDueToXSColls

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 3255 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of the frames that, due to excessive collisions, are not transmitted successfully. This counter is incremented when the value of the attempts variable equals attemptLimit during a transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.12 aFramesLostDueToIntMACXmitError

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

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A count of frames that would otherwise be transmitted by the station, but could not be sent due to an internal MAC sublayer transmit error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

30.3.1.1.13 aCarrierSenseErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of times that the carrierSense variable was not asserted or was deasserted during the transmission of a frame without collision. This counter is incremented when the carrierSenseFailure flag is true at the end of transmission. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.14 aOctetsReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of data and padding octets in frames that are successfully received. This does not include octets in frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented when the result of a reception is reported as a receiveOK status. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.15 aFramesLostDueToIntMACRcvError

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that would otherwise be received by the station, but could not be accepted due to an internal MAC sublayer receive error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

30.3.1.1.16 aPromiscuousStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET operation returns the value “true” for promiscuous mode enabled, and “false” otherwise.

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Frames without errors received solely because this attribute has the value “true” are counted as frames received correctly; frames received in this mode that do contain errors update the appropriate error counters.

A SET operation to the value “true” provides a means to cause the LayerMgmtRecognizeAddress function to accept frames regardless of their destination address.

A SET operation to the value “false” causes the MAC sublayer to return to the normal operation of carrying out address recognition procedures for station, broadcast, and multicast group addresses (LayerMgmtRecognizeAddress function).;

30.3.1.1.17 aReadMulticastAddressList

ATTRIBUTE

APPROPRIATE SYNTAX:
SEQUENCE OF MAC addresses

BEHAVIOUR DEFINED AS:
The current multicast address list.;

30.3.1.1.18 aMulticastFramesXmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of frames that are successfully transmitted, as indicated by the status value transmitOK, to a group destination address other than broadcast. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.19 aBroadcastFramesXmittedOK

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of the frames that were successfully transmitted as indicated by the TransmitStatus transmitOK, to the broadcast address. Frames transmitted to multicast addresses are not broadcast frames and are excluded. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2).;

30.3.1.1.20 aFramesWithExcessiveDeferral

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 412 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

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A count of frames that deferred for an excessive period of time. This counter may only be incremented once per LLC transmission. This counter is incremented when the excessDefer flag is set. The actual update occurs in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode and also when connected to a PHY utilizing the MAC-PHY Rate Matching defined in 61.2.1.1.;

30.3.1.1.21 aMulticastFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received and are directed to an active nonbroadcast group address. This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.22 aBroadcastFramesReceivedOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that are successfully received and are directed to the broadcast group address. This does not include frames received with frame-too-long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error. This counter is incremented as indicated by the receiveOK status, and the value in the destinationField. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.23 aInRangeLengthErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC frames received with a Length/Type field (see 3.2.6) value between the minimum MAC client data size that does not require padding and maxBasicDataSize (see 4.2.7.1) inclusive, that does not match the number of data octets received. The counter also increments for frames whose Length/Type field value is less than the minimum allowed MAC client data size that does not require padding and the number of data octets received is greater than the minimum MAC client data size that does not require padding. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.24 aOutOfRangeLengthField

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC frames received with a Length/Type field value that is greater than maxBasicDataSize (see 4.2.7.1). The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).

NOTE—Before IEEE Std 802.3x-1997, this counter was incremented by frames containing "Type" fields. Due to the modification to legitimize "Type" fields, such frames will now increment aFramesReceivedOK and this counter may only increment with a Length/Type field value that is between maxBasicDataSize and minTypeValue, exclusive (see 4.2.7.1 and 4.2.9).;

30.3.1.1.25 aFrameTooLongErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 815 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC frames received that exceed maxFrameSizeLimit (see 4.2.7.1). This counter is incremented when the status of a frame reception is frameTooLong. The actual update occurs in the LayerMgmtReceiveCounters procedure (5.2.4.3).;

30.3.1.1.26 aMACEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if MAC sublayer is enabled and false if disabled. This is accomplished by setting or checking the values of the receiveEnabled and transmitEnabled variables. Setting to true provides a means to cause the MAC sublayer to enter the normal operational state at idle. The PLS is reset by this operation (see 7.2.2.2.1). This is accomplished by setting receiveEnabled and transmitEnabled to true.

Setting to false causes the MAC sublayer to end all transmit and receive operations, leaving it in a disabled state. This is accomplished by setting receiveEnabled and transmitEnabled to false.;

30.3.1.1.27 aTransmitEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if transmission is enabled and false otherwise. This is accomplished by setting or checking the value of the transmitEnabled variable.

Setting this to true provides a means to enable MAC sublayer frame transmission (TransmitFrame function). This is accomplished by setting transmitEnabled to true.

Setting this to false will inhibit the transmission of further frames by the MAC sublayer (TransmitFrame function). This is accomplished by setting transmitEnabled to false.;

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30.3.1.1.28 aMulticastReceiveStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
True if multicast receive is enabled, and false otherwise. Setting this to true provides a means to cause the MAC sublayer to return to the normal operation of multicast frame reception. Setting this to false will inhibit the reception of further multicast frames by the MAC sublayer.;

30.3.1.1.29 aReadWriteMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
Read the MAC station address or change the MAC station address to the one supplied (RecognizeAddress function). Note that the supplied station address shall not have the group bit set and shall not be the null address.;

30.3.1.1.30 aCollisionFrames

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of 32 generalized nonresettable counters. Each counter has a maximum increment rate of 13 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A histogram of collision activity. The indices of this array (1 to attemptLimit – 1) denote the number of collisions experienced in transmitting a frame. Each element of this array contains a counter that denotes the number of frames that have experienced a specific number of collisions. When the TransmitStatus is reported as transmitOK and the value of the attempts variable equals n, then collisionFrames[n–1] counter is incremented. The elements of this array are incremented in the LayerMgmtTransmitCounters procedure (5.2.4.2). The contents of this attribute are undefined for MAC entities operating in full duplex mode.;

30.3.1.1.31 aMACCapabilities

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE that meets the requirements of the description below:

half duplex	Capable of operating in half duplex mode
full duplex	Capable of operating in full duplex mode

BEHAVIOUR DEFINED AS:
This indicates the duplex capabilities of the MAC.;

30.3.1.1.32 aDuplexStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

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An ENUMERATED VALUE that has one of the following entries:

half duplex	Half duplex mode
full duplex	Full duplex mode
unknown	Duplex status unknown

BEHAVIOUR DEFINED AS:

A GET operation returns the current mode of operation of the MAC entity, either half duplex, full duplex, or unknown. A SET operation changes the mode of operation of the MAC entity to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.;

30.3.1.1.33 aRateControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

"True" for operating speeds above 1000 Mb/s where Rate Control through lowering the average data rate of the MAC sublayer, with frame granularity, is supported (see 4.2.3.2.2), and "false" otherwise.;

30.3.1.1.34 aRateControlStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

rate control off	Rate control mode disabled
rate control on	Rate control mode enabled
unknown	Rate control mode unknown

BEHAVIOUR DEFINED AS:

A GET operation returns the current Rate Control mode of operation of the MAC sublayer.

A SET operation changes the mode of operation of the MAC sublayer to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.

This attribute maps to the variable ifsStretchMode (see 4.2.7.2).;

30.3.1.1.35 aDeferControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

The enumeration "true" is returned when the interframe spacing is accomplished within the MAC sublayer (see 4A.2.3.2.3), the enumeration "false" is returned otherwise.;

30.3.1.1.36 aDeferControlStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

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An ENUMERATED VALUE that has one of the following entries:

unknown	defer control mode unknown
defer control off	defer control mode disabled
defer control on	defer control mode enabled

BEHAVIOUR DEFINED AS:

A GET operation returns the current Defer Control mode of operation of the MAC. A SET operation changes the mode of operation of the MAC sublayer to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.

This attribute maps to the variable deferenceMode (see 4A.2.7.2).;

30.3.1.1.37 aMaxFrameLength

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

unknown	Frame length capability unknown
basicFrame	Capable of supporting maxBasicFrameSize (1518 octet frames)
qTaggedFrame	Capable of supporting maxBasicFrameSize + qTagPrefixSize (1522 octet frames)
envelopeFrame	Capable of supporting maxEnvelopeFrameSize (2000 octet frames)

BEHAVIOUR DEFINED AS:

This indicates the MAC frame length at which the aFramesTooLong counter is incremented.

30.3.1.1.38 aSlowProtocolFrameLimit

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The maximum number of Slow Protocol frames of a given subtype that can be transmitted in a one-second period. The default value is 10.;

30.3.1.2 MAC entity actions

30.3.1.2.1 acInitializeMAC

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

This action provides a means to call the Initialize procedure (4.2.7.4). This action also results in the initialization of the PLS.;

30.3.1.2.2 acAddGroupAddress

ACTION

APPROPRIATE SYNTAX:

MACAddress

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BEHAVIOUR DEFINED AS:

Add the supplied multicast group address to the address recognition filter (RecognizeAddress function).;

30.3.1.2.3 acDeleteGroupAddress

ACTION

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

Delete the supplied multicast group address from the address recognition filter (RecognizeAddress function).;

30.3.1.2.4 acExecuteSelfTest

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

Execute a self-test and report the results (success or failure). The actual mechanism employed to carry out the self-test is not defined in this standard. If PHY loopback is accessible through a Clause 22 MII, Clause 35 GMII, or Clause 45 MDIO interface, then this action shall also invoke a data integrity test using PHY loopback, returning to normal operation on completion of the test. In the case of a Clause 45 MDIO Interface where multiple loopbacks are available, the loopback in the MMD closest to the MDI should be used.;

30.3.2 PHY device managed object class

This subclause formally defines the behaviours for the oPHYEntity managed object class attributes, actions and notifications. Management of that portion of the physical sublayer whose physical containment within the DTE is optional is outside the scope of this clause.

30.3.2.1 PHY device attributes

30.3.2.1.1 aPHYID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aPHYID is assigned so as to uniquely identify a PHY, i.e., Physical Layer among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992 [SMI], Definition of management information).;

30.3.2.1.2 aPhyType

ATTRIBUTE

APPROPRIATE SYNTAX:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected

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2BASE-TL	Clause 61 0.5 Mb/s to 5.5 Mb/s 64/65-octet
10 Mb/s	Clause 7 10 Mb/s Manchester
10PASS-TS	Clause 61 2.5 Mb/s to 100 Mb/s 64/65-octet
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 or subclause 66.1 100 Mb/s 4B/5B
100BASE-T2	Clause 32 100 Mb/s PAM5X5
1000BASE-X	Clause 36 or subclause 66.2 1000 Mb/s 8B/10B
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5
10GBASE-X	Clause 48 10 Gb/s 4 lane 8B/10B
10GBASE-R	Clause 49 10 Gb/s 64B/66B
10GBASE-W	Clause 49 10 Gb/s 64B/66B and Clause 50 WIS
10GBASE-T	Clause 55 10 Gb/s DSQ128
10GBASE-PR	Clause 76 10/10G-EPON 10 Gb/s 64B/66B
10/1GBASE-PRX	Clause 76 10/1G-EPON 10 Gb/s 64B/66B downstream and 1 Gb/s 8B/10B upstream
40GBASE-R	Clause 82 40 Gb/s multi-PCS lane 64B/66B
100GBASE-R	Clause 82 100 Gb/s multi-PCS lane using 2-level PAM
100GBASE-P	Clause 82 100 Gb/s multi-PCS lane using >2-level PAM

BEHAVIOUR DEFINED AS:

A read-only value that identifies the PHY type. The enumeration of the type is such that the value matches the clause number of this International Standard that specifies the particular PHY. The value of this attribute maps to the value of aMAUType. The enumeration “none” can only occur in a standard implementation where an MII exists and there is nothing connected. However, the attribute aMIIDetect should be used to determine whether an MII exists or not.;

30.3.2.1.3 aPhyTypeList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

other	Undefined
unknown	Initializing, true state or type not yet known
none	MII present and nothing connected
2BASE-TL	Clause 61 0.5 Mb/s to 5.5 Mb/s 64/65-octet
10 Mb/s	Clause 7 10 Mb/s Manchester
10PASS-TS	Clause 61 2.5 Mb/s to 100 Mb/s 64/65-octet
100BASE-T4	Clause 23 100 Mb/s 8B/6T
100BASE-X	Clause 24 or subclause 66.1 100 Mb/s 4B/5B
100BASE-T2	Clause 32 100 Mb/s PAM5X5
1000BASE-X	Clause 36 or subclause 66.2 1000 Mb/s 8B/10B
1000BASE-T	Clause 40 1000 Mb/s 4D-PAM5
10GBASE-X	Clause 48 10 Gb/s 4 lane 8B/10B
10GBASE-R	Clause 49 10 Gb/s 64B/66B
10GBASE-W	Clause 49 10 Gb/s 64B/66B and Clause 50 WIS
10GBASE-T	Clause 55 10 Gb/s DSQ128
10GBASE-PR	Clause 76 10/10G-EPON 10 Gb/s 64B/66B
10/1GBASE-PRX	Clause 76 10/1G-EPON 10 Gb/s 64B/66B downstream and 1 Gb/s 8B/10B upstream
40GBASE-R	Clause 82 40 Gb/s multi-PCS lane 64B/66B
100GBASE-R	Clause 82 100 Gb/s multi-PCS lane using 2-level PAM
100GBASE-P	Clause 82 100 Gb/s multi-PCS lane using >2-level PAM

BEHAVIOUR DEFINED AS:

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A read-only list of the possible types that the PHY could be, identifying the ability of the PHY. If Clause 28, Clause 37, or Clause 73 Auto-Negotiation is present, then this attribute will map to the local technology ability or advertised ability of the local device.;

NOTE—At 10 Gb/s the ability of the PMD must be taken into account when reporting the possible types that the PHY could be.;

30.3.2.1.4 aSQETestErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of times that the SQE_TEST_ERROR was received. The SQE_TEST_ERROR is set in accordance with the rules for verification of the SQE detection mechanism in the PLS Carrier Sense function (see 7.2.4.6). The SQE test function is not a part of 100 or 1000 Mb/s PHY operation, and so SQETestErrors will not occur in 100 or 1000 Mb/s PHYs. The contents of this attribute are undefined for full duplex operation.;

30.3.2.1.5 aSymbolErrorDuringCarrier

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second for 100 Mb/s implementations

BEHAVIOUR DEFINED AS:

For 100 Mb/s operation it is a count of the number of times when valid carrier was present and there was at least one occurrence of an invalid data symbol (see 23.2.1.4, 24.2.2.1.7, and 32.3.4.1).
For half duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than slotTime (see 4.2.4), and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” or “Carrier Extend Error” on the GMII (see Table 35–2).
For full duplex operation at 1000 Mb/s, it is a count of the number of times the receiving media is non-idle (a carrier event) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Data reception error” on the GMII (see Table 35–2).
For operation at 10 Gb/s, 40 Gb/s, and 100 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Receive Error” on the XGMII (see Table 46–4), the XLGMII, or the CGMII (see Table 81–3).
At all speeds this counter shall be incremented only once per valid CarrierEvent and if a collision is present this counter shall not increment.;

30.3.2.1.6 aMIIDetect

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
unknown
present, nothing connected

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present, connected
absent

BEHAVIOUR DEFINED AS:

An attribute of the PhyEntity managed object class indicating whether an MII connector is physically present, and if so whether it is detectably connected as specified in 22.2.2.14.;

30.3.2.1.7 aPhyAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:

A disabled PHY neither transmits nor receives. The PHY shall be explicitly enabled to restore operation. The acPhyAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across DTE reset including loss of power. Only one PHY per MAC can be enabled at any one time. Setting a PHY to the enabled state using the action acPhyAdminControl will result in all other instances of PHY (indicated by PhyID) instantiated within the same MAC to be disabled. If a Clause 22 MII or Clause 35 GMII is present then setting this attribute to "disabled" will result in electrical isolation as defined in 22.2.4.1.6, Isolate; and setting this attribute to "enabled" will result in normal operation as defined in 22.2.4.1.5, Power down; and 22.2.4.1.6, Isolate. For all MMDs that provide a Clause 45 MDIO Interface within the PHY, setting this attribute to "enabled" will result in the MMD Low-power bit being set for normal operation. MMDs that support Low Power are the PMA/PMD MMD (see 45.2.1.1.2 and 45.2.1.2.5), the WIS MMD (see 45.2.2.1.3 and 45.2.2.2.3), the PCS MMD (see 45.2.3.1.3 and 45.2.3.2.8), the PHY XS MMD (see 45.2.4.1.3 and 45.2.4.2.8) and the DTE XS MMD (see 45.2.5.1.3 and 45.2.5.2.8).;

30.3.2.1.8 aTransmitLPIMicroseconds

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 000 000 counts per second

BEHAVIOUR DEFINED AS:

A count reflecting the amount of time that the LPI_REQUEST parameter has the value ASSERT. The request is indicated to the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

30.3.2.1.9 aReceiveLPIMicroseconds

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 000 000 counts per second

BEHAVIOUR DEFINED AS:

A count reflecting the amount of time that the LPI_INDICATION parameter has the value ASSERT. The indication reflects the state of the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

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30.3.2.1.10 aTransmitLPITransitions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 000 counts per second at 100 Mb/s; 90 000 counts per second at 1000 Mb/s; and 230 000 counts per second at 10 Gb/s

BEHAVIOUR DEFINED AS:

A count of occurrences of the transition from state LPI_DEASSERTED to state LPI_ASSERTED of the LPI transmit state diagram is the RS. The state transition corresponds to the assertion of the LPI_REQUEST parameter. The request is indicated to the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

30.3.2.1.11 aReceiveLPITransitions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 000 counts per second at 100 Mb/s; 90 000 counts per second at 1000 Mb/s; and 230 000 counts per second at 10 Gb/s

BEHAVIOUR DEFINED AS:

A count of occurrences of the transition from DEASSERT to ASSERT of the LPI_INDICATE parameter. The indication reflects the state of the PHY according to the requirements of the RS (see 22.7, 35.4, 46.4).;

30.3.2.2 PHY device actions

30.3.2.2.1 acPhyAdminControl

ACTION

APPROPRIATE SYNTAX:

Same as aPortAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to alter aPhyAdminState. Setting a PHY to the enabled state will result in all other instances of PHY being disabled.;

30.3.3 MAC control entity object class

This subclause formally defines the behaviours for the oMACControlEntity managed object class attributes.

30.3.3.1 aMACControlID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aMACControlID is assigned so as to uniquely identify a MAC Control entity among the subordinate managed objects of the containing object.;

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30.3.3.2 aMACControlFunctionsSupported

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

PAUSE	PAUSE command implemented
MPCP	MPCP implemented
PFC	PFC implemented
EXTENSION	EXTENSION MAC Control frame supported

BEHAVIOUR DEFINED AS:

A read-write list of the possible MAC Control functions implemented within the device. Each function implemented will have an associated MAC Control Function Entity object class.;

30.3.3.3 aMACControlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer.;

30.3.3.4 aMACControlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3.;

30.3.3.5 aUnsupportedOpcodesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames received that contain an opcode from Table 31A–1 that is not supported by the device. This counter is incremented when a ReceiveFrame function call returns a valid frame with a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, and with an opcode for a function that is not supported by the device.;

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30.3.3.6 aPFCEnableStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:

A read-only value that indicates whether PFC MAC Control operation is enabled. The value enabled indicates that operation of PFC MAC Control is enabled and operation of PAUSE MAC Control is disabled. The value disabled indicates that transmission and reception of PFC MAC Control is not enabled and PAUSE MAC Control may operate if it has been enabled through another mechanism.;

NOTE 1—aPFCEnableStatus is read-only to avoid the risk of it being set to a conflicting value with enablement of PFC in the MAC Control Client. It is intended that an implementation locally sets the value to enabled when the MAC Control Client has PFC enabled for any priority and to disabled when the MAC Control Client has PFC disabled for all priorities.

NOTE 2—There is no mechanism in this Clause to enable and disable PAUSE transmit and receive for PHYs without autonegotiation. IEEE Std 802.3.1 provides dot3PauseAdminMode to enable and disable PAUSE in the absence of autonegotiation.

30.3.4 PAUSE entity managed object class

This subclause formally defines the behaviours for the oMACControlFunctionEntity managed object class attributes.

30.3.4.1 aPAUSELinkDelayAllowance

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET operation returns the value, in bits, of the allowance made by the PAUSE MAC Control entity for round-trip propagation delay of the full duplex link. A SET operation changes the value of the allowance made by the PAUSE MAC Control entity for round-trip propagation delay of the full duplex link to the indicated value, in bits.;

30.3.4.2 aPAUSEMACCtrlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of PAUSE frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer with an opcode indicating the PAUSE operation.;

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30.3.4.3 aPAUSEMACCtrlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, and (2) an opcode indicating the PAUSE operation.;

30.3.5 MPCP managed object class

This subclause formally defines the behaviours for the oMPCP managed object class attributes and actions.

30.3.5.1 MPCP Attributes

30.3.5.1.1 aMPCPID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMPCPID is assigned so as to uniquely identify an MPCP entity among the subordinate managed objects of the containing object.;

30.3.5.1.2 aMPCPAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64 or Clause 77 is enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled”, the interface acts as it would if it had no Multipoint MAC Control sublayer. The operational state of the Multipoint MAC Control sublayer can be changed using the acMPCPAdminControl action.;

30.3.5.1.3 aMPCPMode

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
OLT
ONU

BEHAVIOUR DEFINED AS:

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A read-only value that identifies the operational mode of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64 and Clause 77 operates as an OLT when this attribute has the enumeration “OLT”. When this attribute has the enumeration “ONU”, the interface acts as an ONU.;

30.3.5.1.4 aMPCPLinkID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only value that identifies the Logical Link identity (LLID) associated with the MAC port as specified in 65.1.3.2.2 or 76.2.6.1.3.2, as appropriate.;

30.3.5.1.5 aMPCPRemoteMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A read-only value that identifies the source_address parameter of the last MPCPDU passed to MAC Control.

This value is updated on reception of a valid frame with (1) a destinationField equal to the reserved multicast address for MAC Control specified in 31A, (2) lengthOrType field value equal to the reserved Type for MAC Control as specified in 31A, (3) an opcode value reserved for one of MPCP messages, as specified in 31A.;

30.3.5.1.6 aMPCPRegistrationState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:

unregistered	unregistered
registering	registering with link-partner
registered	registered with a link-partner

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of an individual instance of Multipoint MAC Control. When this attribute has the enumeration “unregistered” the interface is ready for registering a link partner. When this attribute has the enumeration “registering” the interface is in the process of registering a link-partner. When this attribute has the enumeration “registered” the interface has an established and operational link-partner.

NOTE—This attribute may be used by layer management mechanisms or OAM client to obtain the status of logical links in P2MP networks. Specifically, in implementations where the OAM sublayer is interfaced with Multipoint MAC Control, theOAM_CTRL.request (local_link_status) primitive specified in 57.2.5.3 should be mapped to this attribute as follows:

When the value of this attribute changes from “registering” to “registered”, an OAM_CTRL.request primitive with parameter local_link_status = OK is generated.

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When the value of this attribute changes from “registered” to “unregistered”, an OAM_CTRL.request primitive with parameter local_link_status = FAIL is generated.;

30.3.5.1.7 aMPCPMACCtrlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of MPCP frames passed to the MAC sublayer for transmission.

Increment counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating an MPCP frame.;

30.3.5.1.8 aMPCPMACCtrlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of MPCP frames passed by the MAC sublayer to the MAC Control sublayer.

Increment counter by one when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, and (2) an opcode indicating an MPCP frame.;

30.3.5.1.9 aMPCPTxGate

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a GATE MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a GATE MPCPDU.;

30.3.5.1.10 aMPCPTxRegAck

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_ACK MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated

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within the MAC Control sublayer with an opcode indicating a REGISTER_ACK MPCPDU.;

30.3.5.1.11 aMPCPTxRegister

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a REGISTER MPCPDU.;

30.3.5.1.12 aMPCPTxRegRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_REQ MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a REGISTER_REQ MPCPDU.;

30.3.5.1.13 aMPCPTxReport

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REPORT MPCP frames transmission occurs.

Increment the counter by one when a MA_CONTROL.request service primitive is generated within the MAC Control sublayer with an opcode indicating a REPORT MPCPDU.;

30.3.5.1.14 aMPCPRxGate

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a GATE MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the reserved multicast address for MAC Control specified in 31A, or unique physical address associated with this station, (2) a lengthOrType field value equal to the

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reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a GATE MPCPDU.;

30.3.5.1.15 aMPCPRxRegAck

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_ACK MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the reserved multicast address for MAC Control specified in 31A, (2) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REGISTER_ACK MPCPDU.;

30.3.5.1.16 aMPCPRxRegister

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the unique physical address associated with this station, (2) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REGISTER MPCPDU.;

30.3.5.1.17 aMPCPRxRegRequest

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REGISTER_REQ MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the reserved multicast address for MAC Control specified in 31A, (2) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REGISTER_REQ MPCPDU.;

30.3.5.1.18 aMPCPRxReport

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000

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counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of the number of times a REPORT MPCP frames reception occurs.

Increment the counter by one when a ReceiveFrame function call returns a valid frame with: (1) a destinationField equal to the reserved multicast address for MAC Control specified in 31A, (2) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, (3) an opcode indicating a REPORT MPCPDU.;

30.3.5.1.19 aMPCPTransmitElapsed

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A read-only value that reports the interval from last MPCP frame transmission in increments of 16 ns. The value returned shall be (interval from last MPCP frame transmission in ns)/16, where this value exceeds (2^{32}–1) the value (2^{32}–1) shall be returned.;

30.3.5.1.20 aMPCPReceiveElapsed

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A read-only value that reports the interval from last MPCP frame reception in increments of 16 ns. The value returned shall be (interval from last MPCP frame reception in ns)/16, where this value exceeds (2^{32}–1) the value (2^{32}–1) shall be returned.;

30.3.5.1.21 aMPCPRoundTripTime

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A read-only value that reports the MPCP round trip time in increments of 16 ns. The value returned shall be (round trip time in ns)/16, where this value exceeds (2^{16}–1) the value (2^{16}–1) shall be returned. This value is only defined for an OLT. The contents of this attribute are undefined for an ONU.;

30.3.5.1.22 aMPCPDiscoveryWindowsSent

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of discovery windows generated. The counter is incremented by one for each generated discovery window.;

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30.3.5.1.23 aMPCPDiscoveryTimeout

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:
A count of the number of times a discovery time-out occurs. The counter is incremented by one for each discovery processing state diagram reset resulting from time-out waiting for message arrival.;

30.3.5.1.24 aMPCPMaximumPendingGrants

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only value that indicates the maximum number of grants an ONU can store. The maximum number of grants an ONU can store has a range of 0 to 255.;

30.3.5.1.25 aMPCPRecognizedMulticastIDs

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of INTEGERS

BEHAVIOUR DEFINED AS:
A An array of read-only values that identify the multicast Logical Link identities (LLID) associated with the MAC port as specified in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate.; These values are only defined for an ONU. The contents of this attribute are undefined for an OLT.;

30.3.5.2 MPCP Actions

30.3.5.2.1 acMPCPAdminControl

ACTION

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
This action provides a means to alter aMPCPAdminState.;

30.3.6 OAM object class

This subclause formally defines the behaviours for the oOAM managed object class attributes.

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30.3.6.1 OAM Attributes

30.3.6.1.1 aOAMID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aOAMID is assigned so as to uniquely identify an OAM entity among the subordinate managed objects of the containing object.;

30.3.6.1.2 aOAMAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the OAM sublayer.

An interface which can provide the OAM sublayer functions specified in Clause 57 will be enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled” the interface will act as it would if it had no OAM sublayer. The operational state of the OAM sublayer can be changed using the acOAMAdminControl action.;

30.3.6.1.3 aOAMMode

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

passive	passive OAM mode
active	active OAM mode

BEHAVIOUR DEFINED AS:
A GET operation returns the current mode of the OAM sublayer entity (see 57.2.9), either “passive” or “active.” A SET operation changes the mode of operation of the OAM entity to the indicated value. A SET operation shall have no effect on a device whose mode cannot be changed through management or that can only operate in a single mode.;

30.3.6.1.4 aOAMDiscoveryState

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
link fault
active send local
passive wait
send local remote
send local remote ok
send any

BEHAVIOUR DEFINED AS:

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A read-only value that identifies the current state of the OAM Discovery function. The enumerations match the states within the Discovery state diagram Figure 57–5.;

30.3.6.1.5 aOAMRemoteMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
The value of the source_address parameter of the last OAMPDU passed by the OAM subordinate sublayer to the OAM sublayer.

This value is updated on reception of a valid frame with (1) a destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3.;

30.3.6.1.6 aOAMLocalConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (5)]

BEHAVIOUR DEFINED AS:
A string of five bits corresponding to the OAM Configuration field (see Table 57–8) in the most recently transmitted Information OAMPDU.;

The first bit corresponds to the OAM Mode bit in the OAM Configuration field. The second bit corresponds to the Unidirectional Support bit in the OAM Configuration field. The third bit corresponds to the Remote Loopback Support bit in the OAM Configuration field. The fourth bit corresponds to the Link Events bit in the OAM Configuration field. The fifth bit corresponds to the Variable Retrieval bit in the OAM Configuration field.;

30.3.6.1.7 aOAMRemoteConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (5)]

BEHAVIOUR DEFINED AS:
A string of five bits corresponding to the OAM Configuration field (see Table 57–8) in the most recently received Information OAMPDU.

The first bit corresponds to the OAM Mode bit in the OAM Configuration field. The second bit corresponds to the Unidirectional Support bit in the OAM Configuration field. The third bit corresponds to the Remote Loopback Support bit in the OAM Configuration field.The fourth bit corresponds to the Link Events bit in the OAM Configuration field. The fifth bit corresponds to the Variable Retrieval bit in the OAM Configuration field.

This value is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAM

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code equals the OAM Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.8 aOAMLocalPDUConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An eleven bit value corresponding to the Maximum OAMPDU Size value within the OAMPDU Configuration field (see Table 57–9) in the most recently transmitted OAMPDU.;

30.3.6.1.9 aOAMRemotePDUConfiguration

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An eleven bit value corresponding to the Maximum OAMPDU Size value within the OAMPDU Configuration field (see Table 57–9) in the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAM code equals the OAM Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.10 aOAMLocalFlagsField

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (7)]

BEHAVIOUR DEFINED AS:
A string of seven bits corresponding to the Flags field (see Table 57–3) in the most recently transmitted OAMPDU.

The first bit corresponds to the Link Fault bit in the Flags field. The second bit corresponds to the Dying Gasp bit in the Flags field. The third bit corresponds to the Critical Event bit in the Flags field. The fourth bit corresponds to the Local Evaluating bit in the Flags field. The fifth bit corresponds to the Local Stable bit in the Flags field. The sixth bit corresponds to the Remote Evaluating bit in the Flags field. The seventh bit corresponds to the Remote Stable bit in the Flags field.;

30.3.6.1.11 aOAMRemoteFlagsField

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (7)]

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BEHAVIOUR DEFINED AS:

A string of seven bits corresponding to the Flags field (see Table 57–3) in the most recently received OAMPDU.

The first bit corresponds to the Link Fault bit in the Flags field. The second bit corresponds to the Dying Gasp bit in the Flags field. The third bit corresponds to the Critical Event bit in the Flags field. The fourth bit corresponds to the Local Evaluating bit in the Flags field. The fifth bit corresponds to the Local Stable bit in the Flags field. The sixth bit corresponds to the Remote Evaluating bit in the Flags field. The seventh bit corresponds to the Remote Stable bit in the Flags field.

This value is updated on reception of a valid frame with (1) a destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAM code equals one of the codes as specified in Table 57–4.;

30.3.6.1.12 aOAMLocalRevision

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of the Revision field (see 57.5.2.1) in the Local Information TLV of the most recently transmitted Information OAMPDU.;

30.3.6.1.13 aOAMRemoteRevision

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of the Revision field (see 57.5.2.1) in the Local Information TLV of the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.14 aOAMLocalState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (3)]

BEHAVIOUR DEFINED AS:

A string of three bits corresponding to the State field (see Table 57–7) of the most recently transmitted Information OAMPDU. The first and second bits corresponds to the Parser Action bits in the State field. The third bit corresponds to the Multiplexer Action bit in the State field.;

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30.3.6.1.15 aOAMRemoteState

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (3)]

BEHAVIOUR DEFINED AS:
A string of three bits corresponding to the State field (see Table 57–7) of the most recently received Information OAMPDU. The first and second bits corresponds to the Parser Action bits in the State field. The third bit corresponds to the Multiplexer Action bit in the State field.

This value is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.16 aOAMRemoteVendorOUI

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of the OUI/CID field (see Table 57–10) of the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) a OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

30.3.6.1.17 aOAMRemoteVendorSpecificInfo

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of the Vendor Specific Information field (see Table 57–11) of the most recently received Information OAMPDU.

This value is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equal to the Information code as specified in Table 57–4, (5) the frame contains a Local Information TLV (see 57.5.2.1).;

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30.3.6.1.18 aOAMUnsupportedCodesTx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:
A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that are not supported by the device. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code for a function that is not supported by the device.;

30.3.6.1.19 aOAMUnsupportedCodesRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:
A count of OAMPDUs received that contain an OAM code from Table 57–4 that are not supported by the device. This counter is incremented on reception of a valid frame with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) an OAMPDU code for a function that is not supported by the device.;

30.3.6.1.20 aOAMInformationTx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:
A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the OAM Information code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU code indicating an Information OAMPDU.;

30.3.6.1.21 aOAMInformationRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:
A count of OAMPDUs received that contain the OAM Information code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in

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Table 57A–3, (4) the OAMPDU code equals the OAM Information code and is supported by the device.;

30.3.6.1.22 aOAMUniqueEventNotificationTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Event Notification code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is not equal to the Sequence Number field of the last transmitted Event Notification OAMPDU.;

30.3.6.1.23 aOAMDuplicateEventNotificationTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Event Notification code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is equal to the Sequence Number field of the last transmitted Event Notification OAMPDU.;

30.3.6.1.24 aOAMUniqueEventNotificationRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of the OAMPDUs received that contain the Event Notification code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is not equal to the Sequence Number field of the last received Event

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Notification OAMPDU and is supported by the device.;

30.3.6.1.25 aOAMDuplicateEventNotificationRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of the OAMPDUs received that contain the Event Notification code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Event Notification code, (5) the Sequence Number field is equal to the Sequence Number field of the last received Event Notification OAMPDU.;

30.3.6.1.26 aOAMLoopbackControlTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Loopback Control code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating a Loopback Control OAMPDU.;

30.3.6.1.27 aOAMLoopbackControlRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Loopback Control code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Loopback Control code and is supported by the device.;

30.3.6.1.28 aOAMVariableRequestTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

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BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Variable Request code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating a Variable Request OAMPDU.;

30.3.6.1.29 aOAMVariableRequestRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Variable Request code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Variable Request code and is supported by the device.;

30.3.6.1.30 aOAMVariableResponseTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Variable Response code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating a Variable Response OAMPDU.;

30.3.6.1.31 aOAMVariableResponseRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Variable Response code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Variable Response code and is supported by the device.;

30.3.6.1.32 aOAMOrganizationSpecificTx

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of Organization Specific OAMPDUs passed to the OAM subordinate sublayer for transmission that contain the Organization Specific code specified in Table 57–4. This counter is incremented when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAM code indicating an Organization Specific OAMPDU.;

30.3.6.1.33 aOAMOrganizationSpecificRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of Slow_Protocol_Frames as defined in 57A.2.

BEHAVIOUR DEFINED AS:

A count of OAMPDUs received that contain the Organization Specific code specified in Table 57–4. This counter is incremented on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) a Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) the OAMPDU code equals the Organization Specific code and is supported by the device.;

30.3.6.1.34 aOAMLocalErrSymPeriodConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER

BEHAVIOUR DEFINED AS:

The first integer is an eight-octet value indicating the duration of the Errored Symbol Period Event (see 57.5.3.1) window, in terms of symbols.
The second integer is an eight-octet value indicating the number of errored symbols in the period that must be met or exceeded in order for the Errored Symbol Period Event to be generated.;

30.3.6.1.35 aOAMLocalErrSymPeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Symbol Window field
The third INTEGER represents the Errored Symbol Threshold field
The fourth INTEGER represents the Errored Symbols field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently transmitted Errored Symbol Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the

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OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Symbol Period Event value as specified in Table 57–12.;

30.3.6.1.36 aOAMLocalErrFrameConfig

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of two instances of the type INTEGER

BEHAVIOUR DEFINED AS:
The first integer is a two-octet value indicating the duration of the Errored Frame Event (see 57.5.3.2) window, in terms of number of 100 ms intervals. The second integer is a four-octet value indicating the number of errored frames in the period that must be met or exceeded in order for the Errored Frame Event to be generated.;

30.3.6.1.37 aOAMLocalErrFrameEvent

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:
A sequence of six integers corresponding to the respective fields in the most recently transmitted Errored Frame Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Frame Event value as specified in Table 57–12.;

30.3.6.1.38 aOAMLocalErrFramePeriodConfig

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of two instances of the type INTEGER

BEHAVIOUR DEFINED AS:
The first integer is a four-octet value indicating the duration of the Errored Frame Period Event (see 57.5.3.3) window, in terms of the number of frames in the window.

The second integer is a four-octet value indicating the number of errored frames in the period that must be met or exceeded in order for the Errored Frame Period Event to be generated.;

30.3.6.1.39 aOAMLocalErrFramePeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

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A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently transmitted Errored Frame Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Frame Period Event value as specified in Table 57–12.;

30.3.6.1.40 aOAMLocalErrFrameSecsSummaryConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER

BEHAVIOUR DEFINED AS:

The first integer is a two-octet value indicating the duration of the Errored Frame Seconds Summary Event (see 57.5.3.4) window, in terms of number of 100 ms intervals. The second integer is a two-octet value indicating the number of errored frame seconds in the period that must be met or exceeded in order for the Errored Frame Seconds Summary Event to be generated.;

30.3.6.1.41 aOAMLocalErrFrameSecsSummaryEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Seconds Summary Window field
The third INTEGER represents the Errored Frame Seconds Summary Threshold field
The fourth INTEGER represents the Errored Frame Seconds Summary field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently transmitted Errored Frame Seconds Summary Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated when a CTL:OAMI.request service primitive is generated within the OAM sublayer with an OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4 and Event TLV Type field equal to the Errored Frame Seconds Summary Event value as specified in Table 57–12.;

30.3.6.1.42 aOAMRemoteErrSymPeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

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A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Symbol Window field
The third INTEGER represents the Errored Symbol Threshold field
The fourth INTEGER represents the Errored Symbols field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently received Errored Symbol Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Symbol Period Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.43 aOAMRemoteErrFrameEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently received Errored Frame Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Frame Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.44 aOAMRemoteErrFramePeriodEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

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A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Window field
The third INTEGER represents the Errored Frame Threshold field
The fourth INTEGER represents the Errored Frames field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently received Errored Frame Period Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Frame Period Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.45 aOAMRemoteErrFrameSecsSummaryEvent

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of six instances of the type INTEGER
The first INTEGER represents the Event Time Stamp field
The second INTEGER represents the Errored Frame Seconds Summary Window field
The third INTEGER represents the Errored Frame Seconds Summary Threshold field
The fourth INTEGER represents the Errored Frame Seconds Summary field
The fifth INTEGER represents the Error Running Total field
The sixth INTEGER represents the Event Running Total field

BEHAVIOUR DEFINED AS:

A sequence of six integers corresponding to the respective fields in the most recently received Errored Frame Seconds Summary Event TLV in an Event Notification OAMPDU (see 57.4.3.2).

This sequence is updated on reception of a valid frame, with (1) destinationField equal to the reserved multicast address for Slow_Protocols specified in Table 57A–1, (2) lengthOrType field value equal to the reserved Type for Slow_Protocols as specified in Table 57A–2, (3) Slow_Protocols subtype value equal to the subtype reserved for OAM as specified in Table 57A–3, (4) OAMPDU Code field value equal to the Event Notification code as specified in Table 57–4, (5) an Event TLV Type field equal to the Errored Frame Seconds Summary Event value as specified in Table 57–12.

If more than one Event TLV of the same Event Type is present within an Event Notification OAMPDU, the Event with the most recent timestamp should be used.;

30.3.6.1.46 aFramesLostDueToOAMError

ATTRIBUTE

APPROPRIATE SYNTAX:

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Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames that would otherwise be transmitted by the OAM sublayer, but could not be due to an internal OAM sublayer transmit error. If this counter is incremented, then none of the other counters in this section are incremented. The exact meaning and mechanism for incrementing this counter is implementation dependent.;

30.3.6.2 OAM Actions

30.3.6.2.1 acOAMAdminControl

ACTION

APPROPRIATE SYNTAX:

Same as aPortAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to alter aOAMAdminState.;

30.3.7 OMPEmulation managed object class

This subclause formally defines the behaviours for the oOMPEmulation managed object class attributes.

30.3.7.1 OMPEmulation Attributes

30.3.7.1.1aOMPEmulationID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aOAMID is assigned so as to uniquely identify an OMPEmulation entity among the subordinate managed objects of the containing object.;

30.3.7.1.2aOMPEmulationType

ATTRIBUTE

APPROPRIATE SYNTAX:

A ENUMERATION that meets the requirements of the description below:

unknown	initializing, true state or type not yet known
OLT	sublayer operating in OLT mode
ONU	sublayer operating in ONU mode

BEHAVIOUR DEFINED AS:

A read only value that indicates that mode of operation of the Reconciliation Sublayer for Point to Point Emulation (see 65.1.3.1 or 76.2.6.1.1, as appropriate).;

30.3.7.1.3aSLDErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000

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counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames received that do not contain a valid SLD field as defined in 65.1.3.3.1or 76.2.6.1.3.1, as appropriate.;

30.3.7.1.4aCRC8Errors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:

A count of frames received that contain a valid SLD field, as defined in 65.1.3.3.1or 76.2.6.1.3.1, as appropriate, but do not pass the CRC-8 check as defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate.;

30.3.7.1.5aGoodLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames received that contain a valid SLD field in an OLT, as defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate, and pass the CRC-8 check, as defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate.;

30.3.7.1.6aONUPONcastLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames received that: 1) contain a valid SLD field in an ONU, 2) meet the rules for frame acceptance, and 3) pass the CRC-8 check. The SLD is defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate. The rules for LLID acceptance are defined in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate. The CRC-8 check is defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate.;

30.3.7.1.7aOLTPONcastLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames received that contain a valid SLD field in an OLT, as defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate, passes the CRC-8 check, as defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate, and the frame meets the rule for acceptance defined in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate.;

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30.3.7.1.8aBadLLID

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 500 000 counts per second at 1000 Mb/s.

BEHAVIOUR DEFINED AS:

A count of frames received that contain a valid SLD field in an OLT, and pass the CRC-8 check, but are discarded due to the LLID check. The SLD is defined in 65.1.3.3.1 or 76.2.6.1.3.1, as appropriate. The CRC-8 check is defined in 65.1.3.3.3 or 76.2.6.1.3.3, as appropriate. The LLID check is defined in 65.1.3.3.2 or 76.2.6.1.3.2, as appropriate.;

30.3.8 EXTENSION entity managed object class

This subclause formally defines the behaviours for the oEXTENSION managed object class attributes.

30.3.8.1 aEXTENSIONMACCtrlFramesTransmitted

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:

A count of EXTENSION frames passed to the MAC sublayer for transmission. This counter is incremented when a MA_CONTROL.request primitive is generated within the MAC Control sublayer with an opcode indicating the EXTENSION operation.;

30.3.8.2 aEXTENSIONMACCtrlFramesReceived

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 600 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:

A count of MAC Control frames passed by the MAC sublayer to the MAC Control sublayer. This counter is incremented when a ReceiveFrame function call returns a valid frame with: (1) a lengthOrType field value equal to the reserved Type for 802.3_MAC_Control as specified in 31.4.1.3, and (2) an opcode indicating the EXTENSION operation.;

30.3.8.3 aEXTENSIONMACCtrlStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries: enabled disabled

BEHAVIOUR DEFINED AS:

A read-write value that identifies the current (when read) or target (when set) operational state of the EXTENSION MAC Control function (when read), as specified in Annex 31C.;

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30.4 Layer management for 10, 100, and 1000 Mb/s baseband repeaters

30.4.1 Repeater managed object class

This subclause formally defines the behaviours for the oRepeater managed object class, attributes, actions, and notifications.

30.4.1.1 Repeater attributes

30.4.1.1.1 aRepeaterID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aRepeaterID is assigned so as to uniquely identify a repeater among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992 [SMI], Definition of management information).;

30.4.1.1.2 aRepeaterType

ATTRIBUTE

APPROPRIATE SYNTAX:
An INTEGER that meets the requirements of the following description:

9	10 Mb/s Baseband
271	100 Mb/s Baseband, Class I
272	100 Mb/s Baseband, Class II
41	1000 Mb/s Baseband
other	See 30.2.5
unknown	Initializing, true state or type not yet known

BEHAVIOUR DEFINED AS:
Returns a value that identifies the CSMA/CD repeater type. The enumeration of the type is such that the value matches the clause number of the standard that specifies the particular repeater, with further numerical identification for the repeater classes within the same clause.;

30.4.1.1.3 aRepeaterGroupCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aRepeaterGroupCapacity is the number of groups that can be contained within the repeater. Within each managed repeater, the groups are uniquely numbered in the range from 1 to aRepeaterGroupCapacity.

Some groups may not be present in a given repeater instance, in which case the actual number of groups present is less than aRepeaterGroupCapacity. The number of groups present is never greater than aRepeaterGroupCapacity.;

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30.4.1.1.4 aGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of units that are viewed by group managed objects. The length of the bitstring is "aRepeaterGroupCapacity" bits. The first bit relates to group 1. A "1" in the bitstring indicates presence of the group, "0" represents absence of the group.;

30.4.1.1.5 aRepeaterHealthState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries:

other	undefined or unknown
ok	no known failures
repeaterFailure	known to have a repeater related failure
groupFailure	known to have a group related failure
portFailure	known to have a port related failure
generalFailure	has a failure condition, unspecified type

BEHAVIOUR DEFINED AS:
The aRepeaterHealthState attribute indicates the operational state of the repeater. The aRepeaterHealthData and aRepeaterHealthText attributes may be consulted for more specific information about the state of the repeater's health. In case of multiple kinds of failures (e.g., repeater failure and port failure), the value of this attribute shall reflect the highest priority in the following order:
repeater failure
group failure
port failure
general failure;

30.4.1.1.6 aRepeaterHealthText

ATTRIBUTE

APPROPRIATE SYNTAX:
A PrintableString, 255 characters max

BEHAVIOUR DEFINED AS:
The aRepeaterHealthText attribute is a text string that provides information relevant to the operational state of the repeater. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.

The contents are vendor specific.;

30.4.1.1.7 aRepeaterHealthData

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING, 0–255

BEHAVIOUR DEFINED AS:

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The aRepeaterHealthData attribute is a block of data octets that provides information relevant to the operational state of the repeater. The encoding of this data block is vendor dependent. Repeater vendors may use this mechanism to provide detailed failure information or instructions for problem resolution.;

30.4.1.1.8 aTransmitCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater, the counter increments every time the repeater state diagram enters the TRANSMIT COLLISION state from any state other than ONE PORT LEFT (Figure 9–2). For a Clause 27 repeater, the counter increments every time the Repeater Core state diagram enters the JAM state as a result of Activity(ALL) > 1 (Figure 27–2). For a Clause 41 repeater, the counter increments every time the Repeater Unit state diagram enters the JAM state (Figure 41–2).

NOTE—Some non-collision events such as false carriers will cause the repeater unit to enter the JAM state and increment this counter.;

30.4.1.2 Repeater actions

30.4.1.2.1 acResetRepeater

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

This causes a transition to the START state of Figure 9–2 for a Clause 9 repeater, to the START state of Figure 27–2 for a Clause 27 repeater, or to the START state of Figure 41–2 for a Clause 41 repeater. The repeater performs a disruptive self-test that has the following characteristics:

1. The components are not specified
2. The test resets the repeater but without affecting management information about the repeater
3. The test does not inject packets onto any segment
4. Packets received during the test may or may not be transferred
5. The test does not interfere with management functions

This causes a nRepeaterReset notification to be sent.;

30.4.1.2.2 acExecuteNonDisruptiveSelfTest

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

The repeater performs a vendor-specific, non-disruptive self-test that has the following characteristics:

1. The components are not specified
2. The test does not change the state of the repeater or management information about the repeater
3. The test does not inject packets onto any segment
4. The test does not prevent the transfer of any packets

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5. Completion of the test causes a nRepeaterHealth to be sent.;

30.4.1.3 Repeater notifications

30.4.1.3.1 nRepeaterHealth

NOTIFICATION

APPROPRIATE SYNTAX:

A SEQUENCE of three data types. The first is mandatory, the following two are optional. The first is the value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData

BEHAVIOUR DEFINED AS:

This notification conveys information related to the operational state of the repeater. See the aRepeaterHealthState, aRepeaterHealthText, and aRepeaterHealthData attributes for descriptions of the information that is sent.

The nRepeaterHealth notification is sent only when the health state of the repeater changes. The nRepeaterHealth notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included. The nRepeaterHealth notification is not sent as a result of powering up a repeater.;

30.4.1.3.2 nRepeaterReset

NOTIFICATION

APPROPRIATE SYNTAX:

A SEQUENCE of three data types. The first is mandatory, the following two are optional. The first is the value of the attribute aRepeaterHealthState. The second is the value of the attribute aRepeaterHealthText. The third is the value of the attribute aRepeaterHealthData

BEHAVIOUR DEFINED AS:

This notification conveys information related to the operational state of the repeater. The nRepeaterReset notification is sent when the repeater is reset as the result of a power-on condition or upon completion of the acResetRepeater action. The nRepeaterReset notification shall contain repeaterHealthState. repeaterHealthData and repeaterHealthText may or may not be included.;

30.4.1.3.3 nGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:

BITSTRING

BEHAVIOUR DEFINED AS:

This notification is sent when a change occurs in the group structure of a repeater. This occurs only when a group is logically removed from or added to a repeater. The nGroupMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aGroupMap attribute.;

30.4.2 Group managed object class

This subclause formally defines the behaviours for the oGroup managed object class, attributes, actions, and notifications.

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30.4.2.1 Group attributes

30.4.2.1.1 aGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique within the repeater. The value of aGroupID is assigned so as to uniquely identify a group among the subordinate managed objects of the containing object (oRepeater). This value is never greater than aRepeaterGroupCapacity.;

30.4.2.1.2 aGroupPortCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aGroupPortCapacity is the number of ports contained within the group. Valid range is 1–1024. Within each group, the ports are uniquely numbered in the range from 1 to aGroupPortCapacity. Some ports may not be present in a given group instance, in which case the actual number of ports present is less than aGroupPortCapacity. The number of ports present is never greater than aGroupPortCapacity.;

30.4.2.1.3 aPortMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
A string of bits that reflects the current configuration of port managed objects within this group. The length of the bitstring is “aGroupPortCapacity” bits. The first bit relates to group 1. A “1” in the bitstring indicates presence of the port, “0” represents absence of the port.;

30.4.2.2 Group notifications

30.4.2.2.1 nPortMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the port structure of a group. This occurs only when a port is logically removed from or added to a group. The nPortMapChange notification is not sent when powering up a repeater. The value of the notification is the updated value of the aPortMap attribute.;

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30.4.3 Repeater port managed object class

This subclause formally defines the behaviours for the oRepeaterPort managed object class, attributes, actions, and notifications.

30.4.3.1 Port attributes

30.4.3.1.1 aPortID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique in the group. It is assumed that ports are partitioned into groups that also have IDs. The value of aPortID is assigned so as to uniquely identify a repeater port among the subordinate managed objects of the containing object (oGroup). This value can never be greater than aGroupPortCapacity.;

30.4.3.1.2 aPortAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries:
disabled
enabled

BEHAVIOUR DEFINED AS:
A disabled port neither transmits nor receives. The port shall be explicitly enabled to restore operation. The acPortAdminControl action provides this ability. The port enable/disable function as reported by this attribute is preserved across repeater reset including loss of power. aPortAdminState takes precedence over auto-partition and functionally operates between the auto-partition mechanism and the AUI/PMA, PCS/PMA, or GMII/PCS as applicable. For a Clause 9 and Clause 27 repeater, the port auto-partition is reinitialized upon acPortAdminControl taking the value “enabled.” For a Clause 41 repeater, the port auto-partition, receive jabber and carrier integrity functions are reinitialized upon acPortAdminControl taking the value “enabled.”;

30.4.3.1.3 aAutoPartitionState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE LIST that has the following entries:
autoPartitioned
notAutoPartitioned

BEHAVIOUR DEFINED AS:
The aAutoPartitionState flag indicates whether the port is currently partitioned by the repeater’s auto-partition protection. The conditions that cause port partitioning are specified in partition state diagram in Clause 9, Clause 27, and Clause 41. They are not differentiated here. A Clause 27 and Clause 41 repeater port partitions on entry to the PARTITION WAIT state of the partition state diagram (Figure 27–8 and Figure 41–4).;

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30.4.3.1.4 aReadableFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

A representation of the total frames of valid frame length. Increment counter by one for each frame whose OctetCount is greater than or equal to minFrameSize and for which the FCSError and CollisionEvent signals are not asserted, and for which the attribute aFramesTooLong has not been incremented. Additionally, for 1000 Mb/s repeaters, this count shall only be incremented for frames which are received within a CarrierEvent which has a ActivityDuration of greater than or equal to (slotTime + JamSize) BT (see 4.4.2).

NOTE—This statistic provides one of the parameters necessary for obtaining the packet error ratio.;

30.4.3.1.5 aReadableOctets

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 240 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by OctetCount for each frame which has been determined to be a readable frame.

NOTE—This statistic provides an indicator of the total data transferred.;

30.4.3.1.6 aFrameCheckSequenceErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame with the FCSError signal asserted and the FramingError and CollisionEvent signals deasserted and whose OctetCount is greater than or equal to minFrameSize and for which the attribute aFramesTooLong has not been incremented.;

30.4.3.1.7 aAlignmentErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame with the FCSError and FramingError signals asserted and CollisionEvent signal deasserted and whose OctetCount is greater than or equal to minFrameSize and for which the attribute aFramesTooLong has not been incremented. If aAlignmentErrors is incremented then the aFrameCheckSequenceErrors attribute shall not be incremented for the same

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frame. This counter will not increment for 8 bit wide group encoding schemes.;

30.4.3.1.8 aFramesTooLong

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 815 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each frame whose OctetCount is greater than maxFrameSizeLimit (see 4.2.7.1 and 4.4.2). If aFrameTooLong is counted then neither the aAlignmentErrors nor the aFrameCheckSequenceErrors attribute shall be incremented for the frame.

30.4.3.1.9 aShortEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent with ActivityDuration less than ShortEventMaxTime. In the 10 Mb/s case ShortEventMaxTime is greater than 74 BT and less than 82 BT. ShortEventMaxTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state diagram. In the 100 Mb/s case ShortEventMaxTime is 84 bits (21 nibbles), and for the 1000 Mb/s case ShortEventMaxTime is 72 bits (9 octets).

NOTE 1—shortEvents may indicate externally generated noise hits which will cause the repeater to transmit Runts to its other ports, or propagate a collision (which may be late) back to the transmitting DTE and damaged frames to the rest of the network.

NOTE 2—implementers may wish to consider selecting the ShortEventMaxTime towards the lower end of the allowed tolerance range to accommodate bit losses suffered through physical channel devices not budgeted for within this standard.

NOTE 3—Note also that the significance of this attribute is different in 10, 100, and 1000 Mb/s collision domains. Clause 9 repeaters perform fragment extension of short events which would be counted as runts on the interconnect ports of other repeaters. Clause 27 repeaters do not perform fragment extension. Clause 41 repeaters support one repeater per collision domain and do not perform fragment extension.;

30.4.3.1.10 aRunts

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

Increment counter by one for each CarrierEvent that meets one of the following two conditions. Only one test need be made. a) The ActivityDuration is greater than ShortEventMaxTime and less than ValidPacketMinTime and the CollisionEvent signal is deasserted. b) The OctetCount is less than 64, the ActivityDuration is greater than ShortEventMaxTime, and the CollisionEvent signal is deasserted. For 10 and 100 Mb/s repeaters, ValidPacketMinTime is greater than or equal to

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552 BT and less than 565 BT. A CarrierEvent greater than or equal to 552 BT but less than 565 BT may or may not be counted as a runt. At 10 Mb/s an event whose length is greater than 74 BT but less than 82 BT shall increment either the aShortEvents attribute or the aRunts attribute, but not both. ValidPacketMinTime has tolerances included to provide for circuit losses between a conformance test point at the AUI and the measurement point within the state diagram.
For 1000 Mb/s repeaters, ValidPacketMinTime is 4136 BT.

NOTE—Runts usually indicate collision fragments, a normal network event. In certain situations associated with large diameter networks a percentage of runts may exceed ValidPacketMinTime.;

30.4.3.1.11 aCollisions

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

This counter increments for any CarrierEvent signal on any port in which the CollisionEvent signal on this port is asserted.;

30.4.3.1.12 aLateEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 75 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater port this counter increments for each CarrierEvent in which the CollIn(X) variable transitions to the value SQE (see 9.6.6.2) while the ActivityDuration is greater than the LateEventThreshold. For a Clause 27 and Clause 41 repeater port this counter increments for each CarrierEvent in which the CollisionEvent signal assertion occurs while the ActivityDuration is greater than the LateEventThreshold. In both cases such a CarrierEvent is counted twice, as both an aCollision and as an aLateEvent.
For 10 and 100 Mb/s repeaters, the LateEventThreshold is greater than 480 BT and less than 565 BT. LateEventThreshold has tolerances included to permit an implementation to build a single threshold to serve as both the LateEventThreshold and ValidPacketMinTime threshold. For 1000 Mb/s repeaters, the LateEventThreshold is equal to ValidPacketMinTime.;

30.4.3.1.13 aVeryLongEvents

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 250 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:

For a Clause 9 repeater port this counter increments for each CarrierEvent whose ActivityDuration is greater than the MAU Jabber Lockup Protection timer TW3 (see 9.6.1, 9.6.5). For a Clause 27 and Clause 41 repeater port this counter increments on entry to the RX JABBER state of the receive timer state diagram (Figure 27–7 and Figure 41–3). Other counters may be incremented as appropriate.;

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30.4.3.1.14 aDataRateMismatches

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter

BEHAVIOUR DEFINED AS:
Increment counter by one for each frame received by this port that meets all of the conditions required by only one of the following three measurement methods:

Measurement method A, which is valid for 10 and 100 Mb/s operation only: a) The CollisionEvent signal is not asserted. b) The ActivityDuration is greater than ValidPacketMinTime. c) The received frequency (data rate) is detectably mismatched from the local transmit frequency.

Measurement method B, which is valid for 10 and 100 Mb/s operation only: a) The CollisionEvent signal is not asserted. b) The OctetCount is greater than 63. c) The received frequency (data rate) is detectably mismatched from the local transmit frequency.

Measurement method C, which is valid for 1000 Mb/s operation only: The received frequency (data rate) is detectably mismatched from the local transmit frequency.

The exact degree of mismatch is vendor specific and is to be defined by the vendor for conformance testing. When this event occurs, other counters whose increment conditions were satisfied may or may not also be incremented, at the implementer's discretion.

NOTE—Whether or not the repeater was able to maintain data integrity is beyond the scope of this standard.;

30.4.3.1.15 aAutoPartitions

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter

BEHAVIOUR DEFINED AS:
Increment counter by one for each time that the repeater has automatically partitioned this port. The conditions that cause a Clause 9 repeater port to partition are specified in the partition state diagram in Clause 9. They are not differentiated here. A Clause 27 and Clause 41 repeater port partitions on entry to the PARTITION WAIT state of the partition state diagram (Figure 27–8 and Figure 41–4).;

30.4.3.1.16 aIsolates

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 400 counts per second at 100 Mb/s

BEHAVIOUR DEFINED AS:
Increment counter by one each time that the repeater port automatically isolates as a consequence of false carrier events. The conditions that cause a port to automatically isolate are as defined by the transition from the FALSE CARRIER state to the LINK UNSTABLE state of the carrier integrity state diagram (Figure 27–9 and Figure 41–5).

NOTE—Isolates do not affect the value of aPortAdminState.;

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30.4.3.1.17 aSymbolErrorDuringPacket

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second for 100 Mb/s implementations

BEHAVIOUR DEFINED AS:
A count of the number of times when valid length packet was received at the port and there was at least one occurrence of an invalid data symbol. This can increment only once per valid CarrierEvent. A collision presence at any port of the repeater containing port N, will not cause this attribute to increment.;

30.4.3.1.18 aLastSourceAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
The Source Address of the last readable Frame received by this port.;

30.4.3.1.19 aSourceAddressChanges

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 15 000 counts per second at 10 Mb/s

BEHAVIOUR DEFINED AS:
Increment counter by one each time that the aLastSourceAddress attribute has changed.

NOTE—This may indicate whether a link is connected to a single DTE or another multi-user segment.;

30.4.3.1.20 aBursts

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 235 000 counts per second at 1000 Mb/s

BEHAVIOUR DEFINED AS:
This counter is valid for 1000 Mb/s operation only. This counter increments by one for each CarrierEvent with ActivityDuration greater than or equal to slotTime during which the CollisionEvent signal has not been asserted. Note that this counter will not increment for a 10 or 100 Mb/s port as packet bursting is not supported at these speeds.;

30.4.3.2 Port actions

30.4.3.2.1 acPortAdminControl

ACTION

APPROPRIATE SYNTAX:

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Same as aPortAdminStateBEHAVIOUR DEFINED AS:
This action provides a means to alter aPortAdminState. For a Clause 9 and Clause 27 repeater it should exert a BEGIN on the Partitioning state diagram (Figure 9–6 and Figure 27–8) upon taking the value "enabled." For a Clause 41 repeater it shall exert a BEGIN on the receive timer, partition, and carrier integrity state diagrams (Figure 41–3, Figure 41–4, and Figure 41–5) upon taking the value "enabled.";

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

This subclause formally defines the behaviours for the oMAU managed object class, attributes, actions, and notifications.

The sublayer that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds. Because this clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayers as a group. Therefore in this clause, the term MAU will include PMA and PMD sublayers, as well as MAUs, except in those instances where it is explicitly restricted to 10 Mb/s.

30.5.1.1 MAU attributes

30.5.1.1.1 aMAUID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMAUID is assigned so as to uniquely identify a MAU among the subordinate managed objects of the containing object.;

30.5.1.1.2 aMAUType

ATTRIBUTE

APPROPRIATE SYNTAX:
A GET-SET ENUMERATION that meets the requirements of the following description:

global	undefined
other	See 30.2.5
unknown	Initializing, true state or type not yet known
AUI	no internal MAU, view from AUI
2BASE-TL	Voice grade twisted-pair cabling PHY as specified in Clause 61 and 63
10BASE5	Thick coax MAU as specified in Clause 8
FOIRL	FOIRL MAU as specified in 9.9
10BASE2	Thin coax MAU as specified in Clause 10
10BROAD36	Broadband DTE MAU as specified in Clause 11
10BASE-T	Twisted-pair cabling MAU as specified in Clause 14, duplex mode unknown
10BASE-THD	Twisted-pair cabling MAU as specified in Clause 14, half duplex mode
10BASE-TFD	Twisted-pair cabling MAU as specified in Clause 14, full duplex mode
10PASS-TS	Voice grade twisted-pair cabling PHY as specified in Clause 61 and 62
10BASE-FP	Passive fiber MAU as specified in Clause 16
10BASE-FB	Synchronous fiber MAU as specified in Clause 17

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10BASE-FL	Asynchronous fiber MAU as specified in Clause 18, duplex mode unknown
10BASE-FLHD	Asynchronous fiber MAU as specified in Clause 18, half duplex mode
10BASE-FLFD	Asynchronous fiber MAU as specified in Clause 18, full duplex mode
100BASE-T4	Four-pair Category 3 twisted-pair cabling as specified in Clause 23
100BASE-TX	Two-pair Category 5 twisted-pair cabling as specified in Clause 25, duplex mode unknown
100BASE-TXHD	Two-pair Category 5 twisted-pair cabling as specified in Clause 25, half duplex mode
100BASE-TXFD	Two-pair Category 5 twisted-pair cabling as specified in Clause 25, full duplex mode
100BASE-BX10D	One single-mode fiber OLT PHY as specified in Clause 58
100BASE-BX10U	One single-mode fiber ONU PHY as specified in Clause 58
100BASE-FX	X fiber over PMD as specified in Clause 26, duplex mode unknown
100BASE-FXHD	X fiber over PMD as specified in Clause 26, half duplex mode
100BASE-FXFD	X fiber over PMD as specified in Clause 26, full duplex mode
100BASE-LX10	Two fiber PHY as specified in Clause 58
100BASE-T2	Two-pair Category 3 twisted-pair cabling as specified in Clause 32, duplex mode unknown
100BASE-T2HD	Two-pair Category 3 twisted-pair cabling as specified in Clause 32, half duplex mode
100BASE-T2FD	Two-pair Category 3 twisted-pair cabling as specified in Clause 32, full duplex mode
1000BASE-X	X PCS/PMA as specified in Clause 36 over undefined PMD, duplex mode unknown
1000BASE-BX10D	One single-mode fiber OLT PHY as specified in Clause 59
1000BASE-BX10U	One single-mode fiber ONU PHY as specified in Clause 59
1000BASE-XHD	X PCS/PMA as specified in Clause 36 over undefined PMD, half duplex mode
1000BASE-XFD	X PCS/PMA as specified in Clause 36 over undefined PMD, full duplex mode
1000BASE-LX	X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-LXHD	X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-LXFD	X fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-LX10	Two fiber 10 km PHY as specified in Clause 59
1000BASE-PX10-D	One single-mode fiber OMP OLT PHY, as specified in Clause 60, supporting a distance of at least 10 km, and a split of at least 1:16
1000BASE-PX10-U	One single-mode fiber OMP ONU PHY, as specified in Clause 60, supporting a distance of at least 10 km, and a split of at least 1:16
1000BASE-PX20-D	One single-mode fiber OMP OLT PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:16
1000BASE-PX20-U	One single-mode fiber OMP ONU PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:16
1000BASE-PX30-D	One single-mode fiber OMP OLT PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:32
1000BASE-PX30-U	One single-mode fiber OMP ONU PHY, as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:32
1000BASE-PX40-D	One single-mode fiber OMP OLT PHY as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:64
1000BASE-PX40-U	One single-mode fiber OMP ONU PHY as specified in Clause 60, supporting a distance of at least 20 km, and a split of at least 1:64

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1000BASE-SX	X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-SXHD	X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-SXFD	X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-CX	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown
1000BASE-CXHD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode
1000BASE-CXFD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full duplex mode
1000BASE-KX	X PCS/PMA over an electrical backplane PMD as specified in Clause 70
1000BASE-T	Four-pair Category 5 twisted-pair cabling PHY as specified in Clause 40, duplex mode unknown
1000BASE-THD	Four-pair Category 5 twisted-pair cabling PHY as specified in Clause 40, half duplex mode
1000BASE-TFD	Four-pair Category 5 twisted-pair cabling PHY as specified in Clause 40, full duplex mode
10GBASE-X	X PCS/PMA as specified in Clause 48 over undefined PMD
10GBASE-LX4	X fiber over 4 lane 1310nm optics as specified in Clause 53
10GBASE-CX4	X copper over 8 pair 100-Ohm balanced cable as specified in Clause 54
10GBASE-KX4	X PCS/PMA over an electrical backplane PMD as specified in Clause 71
10GBASE-R	R PCS/PMA as specified in Clause 49 over undefined PMD
10GBASE-ER	R fiber over 1550nm optics as specified in Clause 52
10GBASE-LR	R fiber over 1310nm optics as specified in Clause 52
10GBASE-SR	R fiber over 850nm optics as specified in Clause 52
10GBASE-LRM	R fiber over 1310 nm optics as specified in Clause 68
10GBASE-KR	R PCS/PMA over an electrical backplane PMD as specified in Clause 72
10GBASE-W	W PCS/PMA as specified in Clause 49 and 50 over undefined PMD
10GBASE-EW	W fiber over 1550nm optics as specified in Clause 52
10GBASE-LW	W fiber over 1310nm optics as specified in Clause 52
10GBASE-SW	W fiber over 850nm optics as specified in Clause 52
10GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 55
10/1GBASE-PRX-D1	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-D2	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-D3	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-D4	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream OLT PHY as specified in Clause 75
10/1GBASE-PRX-U1	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10/1GBASE-PRX-U2	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10/1GBASE-PRX-U3	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10/1GBASE-PRX-U4	One single-mode fiber 10.3125 GBd continuous downstream / 1.25 GBd burst mode upstream ONU PHY as specified in Clause 75
10GBASE-PR-D1	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-D2	One single-mode fiber 10.3125 GBd continuous downstream / burst

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	mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-D3	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-D4	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream OLT PHY as specified in Clause 75
10GBASE-PR-U1	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 75
10GBASE-PR-U3	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 75
10GBASE–PR–U4	One single-mode fiber 10.3125 GBd continuous downstream / burst mode upstream ONU PHY as specified in Clause 75
40GBASE-R	Multi-lane PCS as specified in Clause 82 over undefined PMA/PMD
40GBASE-KR4	40GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 84
40GBASE-CR4	40GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 85
40GBASE-SR4	40GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 86
40GBASE-LR4	40GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with long reach, as specified in Clause 87
40GBASE-ER4	40GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with extended reach, as specified in Clause 87
40GBASE-FR	40GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 89
100GBASE-R	Multi-lane PCS as specified in Clause 82 over undefined 100GBASE-R or 100GBASE-P PMA/PMD
100GBASE-CR4	100GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 92
100GBASE-KR4	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 93
100GBASE-KP4	100GBASE-P PCS/PMA over an electrical backplane PMD as specified in Clause 94
100GBASE-CR10	100GBASE-R PCS/PMA over 10 lane shielded copper balanced cable PMD as specified in Clause 85
100GBASE-SR4	100GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 95
100GBASE-SR10	100GBASE-R PCS/PMA over 10 lane multimode fiber PMD as specified in Clause 86
100GBASE-LR4	100GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with long reach, as specified in Clause 88
100GBASE-ER4	100GBASE-R PCS/PMA over 4 WDM lane single mode fiber PMD, with extended reach, as specified in Clause 88
802.9a	Integrated services MAU as specified in IEEE Std 802.9a-1995 (withdrawn)

BEHAVIOUR DEFINED AS:

Returns a value that identifies the internal MAU type. If an AUI is to be identified to access an external MAU, the type “AUI” is returned. A SET operation to one of the possible enumerations indicated by aMAUTypeList will force the MAU into the new operating mode. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the mode force bits specified in 22.2.4.1. If a Clause 45 MDIO Interface is present, then this will map to the PCS type selection bit(s) in the 10G WIS Control 2 register specified in 45.2.2.6.6, the PCS Control 2 register specified in 45.2.3.6.1, the PMA/PMD type selection bits in the PMA/PMD Control 2 register specified in 45.2.1.6, the PMA/PMD control 1 register specified in 45.2.1.1, and the PCS control 1 register

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45.2.3.1. If Clause 28, Clause 37, or Clause 73 Auto-Negotiation is operational, then this will change the advertised ability to the single enumeration specified in the SET operation, and cause an immediate link renegotiation. A change in the MAU type will also be reflected in aPHYType.

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 10GBASE-X, 10GBASE-R, 10GBASE-W, 40GBASE-R, and 100GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.3 aMAUTypeList

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of ENUMERATIONS that match the syntax of aMAUType

BEHAVIOUR DEFINED AS:

A GET attribute that returns the possible types that the MAU could be, identifying the ability of the MAU. This attribute maps to aPHYTypeList.;

30.5.1.1.4 aMediaAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
available	link or light normal, loopback normal
available reduced	link normal, reduced bandwidth, applies only to 2BASE-TL and 10PASS-TS
not available	link loss or low light, no loopback
remote fault	remote fault with no detail
invalid signal	invalid signal, applies only to 10BASE-FB
remote jabber	remote fault, reason known to be jabber
remote link loss	remote fault, reason known to be far-end link loss
remote test	remote fault, reason known to be test
ready	at least one PME available, applies only to 2BASE-TL and 10PASS-TS
offline	offline, applies only to Clause 37 Auto-Negotiation
auto neg error	Auto-Negotiation Error, applies only to Clause 37 Auto-Negotiation
PMD link fault	PMD/PMA receive link fault
WIS frame loss	WIS loss of frame, applies only to 10GBASE-W
WIS signal loss	WIS loss of signal, applies only to 10GBASE-W
PCS link fault	PCS receive link fault
excessive BER	PCS Bit Error Ratio monitor reporting excessive error ratio
DXS link fault	DTE XGXS receive link fault, applies only to XAUI
PXS link fault	PHY XGXS transmit link fault, applies only to XAUI

BEHAVIOUR DEFINED AS:

If the MAU is a 10 Mb/s link or fiber type (FOIRL, 10BASE-T, 10BASE-F), then this is equivalent to the link test fail state/low light function. For an AUI, 10BASE2, 10BASE5, or 10BROAD36 MAU, this indicates whether or not loopback is detected on the DI circuit. The value of this attribute persists between packets for MAU types AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP.

At power-up or following a reset, the value of this attribute will be “unknown” for AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP MAUs. For these MAUs loopback will be tested on each transmission during which no collision is detected. If DI is receiving *input* when DO returns

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to IDL after a transmission and there has been no collision during the transmission, then loopback will be detected. The value of this attribute will only change during noncollided transmissions for AUI, 10BASE2, 10BASE5, 10BROAD36, and 10BASE-FP MAUs.

For 100BASE-T2 and 100BASE-T4 PHYs the enumerations match the states within the respective link integrity state diagrams, Figure 32-16 and Figure 23–12. For 100BASE-TX, 100BASE-FX, 100BASE-LX10 and 100BASE-BX10 PHYs the enumerations match the states within the link integrity state diagram Figure 24–15. Any MAU that implements management of Clause 28 or Clause 73 Auto-Negotiation will map remote fault indication to MediaAvailable "remote fault." Any MAU that implements management of Clause 37 Auto-Negotiation will map the received RF1 and RF2 bits as specified in Table 37–3, as follows. Offline maps to the enumeration "offline," Link_Failure maps to the enumeration "remote fault" and Auto-Negotiation Error maps to the enumeration "auto neg error."

The enumeration "remote fault" applies to 10BASE-FB remote fault indication, the 100BASE-X far-end fault indication and nonspecified remote faults from a system running Clause 28 Auto-Negotiation. The enumerations "remote jabber", "remote link loss", or "remote test" should be used instead of "remote fault" where the reason for remote fault is identified in the remote signaling protocol.

Where a Clause 22 MII or Clause 35 GMII is present, a one in the remote fault bit (22.2.4.2.11) maps to the enumeration "remote fault," a zero in the link status bit (22.2.4.2.13) maps to the enumeration "not available." The enumeration "not available" takes precedence over "remote fault."

For 40 Gb/s and 100 Gb/s the enumerations map to value of the link_fault variable (see 81.3.4) within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46–11) as follows: the value OK maps to the enumeration "available", the value Local Fault maps to the enumeration "not available" and the value Remote Fault maps to the enumeration "remote fault."

For 2BASE-TL and 10PASS-TS PHYs, the enumeration "unknown" maps to the condition where the PHY is initializing, the enumeration "ready" maps to the condition where at least one PME is available and is ready for handshake, the enumeration "available" maps to the condition where, at the PCS, at least one PME is operationally linked, the enumeration "not available" maps to the condition where the PCS is not operationally linked, the enumeration "available reduced" maps to the condition where a link fault is detected at the receive direction by one or more PMEs in the aggregation group and the enumeration "PMD link fault" maps to the condition where a link fault is detected at the receive direction by all of the PMA/PMDs in the aggregation group.

For 10 Gb/s the enumerations map to value of the link_fault variable within the Link Fault Signaling state diagram (Figure 46–11) as follows: the value OK maps to the enumeration "available", the value Local Fault maps to the enumeration "not available" and the value Remote Fault maps to the enumeration "remote fault". The enumeration "PMD link fault", "WIS frame loss", "WIS signal loss", "PCS link fault", "excessive BER" or "DXS link fault" should be used instead of the enumeration "not available" where the reason for the Local Fault state can be identified through the use of the Clause 45 MDIO Interface. Where multiple reasons for the Local Fault state can be identified only the highest precedence error should be reported. This precedence in descending order is as follows: "PXS link fault", "PMD link fault", "WIS frame loss", "WIS signal loss", "PCS link fault", "excessive BER", "DXS link fault".

Where a Clause 45 MDIO interface is present a zero in the PMA/PMD Receive link status bit (45.2.1.2.4) maps to the enumeration "PMD link fault", a one in the LOF status bit (45.2.2.10.4) maps to the enumeration "WIS frame loss", a one in the LOS status bit (45.2.2.10.5) maps to the enumeration "WIS signal loss", a zero in the PCS Receive link status bit (45.2.3.2.7) maps to the enumeration "PCS link fault", a one in the 10/40/100GBASE-R PCS Latched high BER status bit (45.2.3.14.2) maps to the enumeration "excessive BER", a zero in the DTE XS receive link status bit (45.2.5.2.7) maps to the enumeration "DXS link fault" and a zero in the PHY XS transmit link status bit (45.2.4.2.7) maps to the enumeration "PXS link fault".;

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30.5.1.1.5 aLoseMediaCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 counts per second

BEHAVIOUR DEFINED AS:

Counts the number of times that the MediaAvailable attribute changes from the enumeration "available" to any other enumeration. Mandatory for MAU type "AUI," optional for all others.;

30.5.1.1.6 aJabber

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two indications. The first, JabberFlag, consists of an ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
normal	state is true or normal
fault	state is false, fault, or abnormal

The second, jabberCounter, is a generalized nonresettable counter. This counter has a maximum increment rate of 40 counts per second

BEHAVIOUR DEFINED AS:

If the MAU is in the JABBER state, the jabberFlag portion of the attribute is set to the "fault" value. The jabberCounter portion of the attribute is incremented each time the flag is set to the "fault" value. This attribute returns the value "other" for type AUI. Note that this counter will increment for a 10 Mb/s baseband and broadband MAUs only.;

30.5.1.1.7 aMAUAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
operational	powered and connected
standby	inactive but on
shutdown	similar to power down

BEHAVIOUR DEFINED AS:

A MAU in management state "standby" forces DI and CI to idle and the media transmitter to idle or fault, if supported. The management state "standby" only applies to link type MAUs. The state of MediaAvailable is unaffected. A MAU or AUI in the management state "shutdown" assumes the same condition on DI, CI and the media transmitter as if it were powered down or not connected. For an AUI, this management state will remove power from the AUI. The MAU may return the value "undefined" for Jabber and MediaAvailable attributes when it is in this management state. A MAU in the management state "operational" is fully functional, and operates and passes signals to its attached DTE or repeater port in accordance with its specification.;

30.5.1.1.8 aBbMAUXmitRcvSplitType

ATTRIBUTE

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APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
single	single-cable system
dual	dual-cable system, offset normally zero

BEHAVIOUR DEFINED AS:

Returns a value that indicates the type of frequency multiplexing/cabling system used to separate the transmit and receive paths for the 10BROAD36 MAU. All other types return “undefined.”;

30.5.1.1.9 aBroadbandFrequencies

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances of the type INTEGER.

The first INTEGER represents the Transmitter Carrier Frequency. The value of its INTEGER represents the frequency of the carrier divided by 250 kHz.

The second INTEGER represents the Translation Offset Frequency. The value of its INTEGER represents the frequency of the offset divided by 250 kHz

BEHAVIOUR DEFINED AS:

Returns a value that indicates the transmit carrier frequency and translation offset frequency in MHz/4 for the 10BROAD36 MAU. This allows the frequencies to be defined to a resolution of 250 kHz.;

30.5.1.1.10 aFalseCarriers

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 160 000 counts per second under maximum network load, and 10 counts per second under zero network load, for 100 Mb/s implementations. This counter has a maximum increment rate of 1 600 000 counts per second under maximum network load, and 100 000 counts per second under zero network load, for 1000 Mb/s implementations

BEHAVIOUR DEFINED AS:

A count of the number of false carrier events during IDLE in 100BASE-X and 1000BASE-X links. This counter does not increment at the symbol rate. For 100BASE-X, it can increment after a valid carrier completion at a maximum rate of once per 100 ms until the nextCarrierEvent. For 1000BASE-X, it can increment after a valid carrier completion at a maximum rate of once per 10 μs until the next CarrierEvent.

NOTE—The increased increment rate for this attribute at 1000 Mb/s relative to its increment rate at 100 Mb/s has been provided to improve its use as an indication of line quality.;

30.5.1.1.11 aBIPErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 10 000 counts per second for 40 Gb/s implementations and 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

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For 40/100GBASE-R PHYs and 100GBASE-P PHYS, an array of BIP error counters. The counters do not increment for other PHY types. The indices of this array (0 to n – 1) denote the PCS lane number where n is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane. Increment the counter by one for each BIP error detected during alignment marker removal in the PCS for the corresponding lane.
If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the BIP error counters (see 45.2.3.44 and 45.2.3.45).;

30.5.1.1.12 aLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:
For 40/100GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to n – 1) denote the service interface lane number where n is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.
If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the Lane mapping registers (see 45.2.3.46 and 45.2.3.47).;

30.5.1.1.13 aIdleErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This attribute takes the eight-bit value from the 100BASE-T2 Status register (MII management register 10) bits 7:0 “Idle Error Count” as described in 100BASE-T2, 32.5.3.2.6 and 40.5.;

30.5.1.1.14 aPCSCodingViolation

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 25 000 000 counts per second for 100 Mb/s implementations and 125 000 000 counts per second for 1000 Mb/s implementations.

BEHAVIOUR DEFINED AS:
For 100 Mb/s operation it is a count of the number of events that cause the PHY to indicate “Data reception with errors” on the MII (see Table 22–2). For 1000 Mb/s operation it is a count of the number of events that cause the PHY to indicate “Data reception error” or “Carrier Extend Error” on the GMII (see Table 35–1). The contents of this attribute is undefined when FEC is operating.;

30.5.1.1.15 aFECAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
supported	FEC supported

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not supported FEC not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional FEC sublayer for forward error correction (see 65.2 and Clause 74) or supports the Clause 91 mandatory RS-FEC.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC capability register (see 45.2.8.2 or 45.2.1.92).;

30.5.1.1.16 aFECmode

ATTRIBUTE

APPROPRIATE SYNTAX:

A ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
disabled	FEC disabled
enabled	FEC enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the optional FEC sublayer for forward error correction (see 65.2 and Clause 74).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. When Clause 73 Auto-Negotiation is enabled for a PHY supporting Clause 74 FEC a SET operation is not allowed and a GET operation maps to the variable FEC_enable in Clause 74.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC control register (see 45.2.8.3) for 1000BASE-PX or FEC enable bit in BASE-R FEC control register (see 45.2.1.93).;

30.5.1.1.17 aFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/40/100GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for multiple FEC lanes. Each element of this array contains a count of corrected FEC blocks for that FEC sublayer instance.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.8.5 and 45.2.1.94 for 10GBASE-R, 45.2.3.39 for 10GBASE-PR and 10/

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1GBASE-PRX, 45.2.1.116 for BASE-R, and 45.2.1.103 for RS-FEC).;

30.5.1.1.18 aFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/40/100GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for multiple FEC lanes. Each element of this array contains a count of corrected FEC blocks for that FEC sublayer instance.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC uncorrectable blocks counter(s) (see 45.2.8.6 and 45.2.1.95 for 10GBASE-R, 45.2.3.40 for 10GBASE-PR and 10/1GBASE-PRX, 45.2.1.117 for BASE-R, and 45.2.1.104 for RS-FEC).;

30.5.1.1.19 aSNROpMarginChnlA

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel A for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel A register (see 45.2.1.66).;

30.5.1.1.20 aSNROpMarginChnlB

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current SNR operating margin measured at the slicer input for channel B for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel B register (see 45.2.1.67).;

30.5.1.1.21 aSNROpMarginChnlC

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel C for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel C register (see 45.2.1.68).;

30.5.1.1.22 aSNROpMarginChnlD

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current SNR operating margin measured at the slicer input for channel D for the 10GBASE-T PMA. It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute maps to the SNR operating margin channel D register (see 45.2.1.69).;

30.5.1.1.23 aEEESupportList

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE of ENUMERATIONS that match the syntax of aMAUType

BEHAVIOUR DEFINED AS:
A read-only list of the possible PHY types for which the underlying system supports Energy-Efficient Ethernet (EEE) as defined in Clause 78. If Clause 28 or Clause 73 Auto-Negotiation is present, then this attribute will map to the local technology ability or advertised ability of the local device;

30.5.1.1.24 aLDFastRetrainCount

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per second

BEHAVIOUR DEFINED AS:
A count of the number of 10GBASE-T fast retrains initiated by the local device. The indication reflects the state of the PHY event counter (see 45.2.1.79.2 and 55.4.5.1.).;

30.5.1.1.25 aLPFastRetrainCount

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per second

BEHAVIOUR DEFINED AS:
A count of the number of 10GBASE-T fast retrains initiated by the link partner. The indication reflects the state of the PHY event counter (see 45.2.1.79.1 and 55.4.5.1.).;

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30.5.1.1.26 aRSFECBIPErrorCount

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 100GBASE-R and 100GBASE-P PHYs, an array of BIP error counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the PCS lane number where N is the number of PCS lanes in use. Each element of this array contains a count of BIP errors for that PCS lane.

Increment the counter by one for each BIP error detected during alignment marker removal in the PCS for the corresponding lane.

If a Clause 45 MDIO Interface is present, then this attribute maps to the BIP error counters (see 45.2.1.108 and 45.2.1.109).;

30.5.1.1.27 aRSFECLaneMapping

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of INTEGERs.

BEHAVIOUR DEFINED AS:

For 100GBASE-R and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to N – 1) denote the service interface lane number where N is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.

If a Clause 45 MDIO Interface is present, then this attribute maps to the Lane mapping registers (see 45.2.1.110 and 45.2.1.111).;

30.5.1.1.28 aRSFECBypassAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	FEC bypass ability supported
not supported	FEC bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC bypass ability (see 91.5.3.3).

If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.102).;

30.5.1.1.29 aRSFECIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	FEC error indication bypass ability supported

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not supported	FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC error indication bypass ability (see 91.5.3.3).

If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC status register (see 45.2.1.102).;

30.5.1.1.30 aRSFECBypassEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	FEC bypass disabled
enabled	FEC bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC bypass function (see 91.5.3.3).

A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.

If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.101).;

30.5.1.1.31 aRSFECIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	FEC error indication bypass disabled
enabled	FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function (see 91.5.3.3).

A GET operation returns the current mode of operation of the RS-FEC. A SET operation changes the mode of operation of the RS-FEC to the indicated value.

If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.1.101).;

30.5.1.2 MAU actions

30.5.1.2.1 acResetMAU

ACTION

APPROPRIATE SYNTAX:

None required

BEHAVIOUR DEFINED AS:

Resets the MAU in the same manner as would a power-off, power-on cycle of at least 0.5 s duration. During the 0.5 s DO, DI, and CI should be idle.;

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30.5.1.2.2 acMAUAdminControl

ACTION

APPROPRIATE SYNTAX:
The same as used for aMAUAdminState

BEHAVIOUR DEFINED AS:
Executing an acMAUAdminControl action causes the MAU to assume the aMAUAdminState attribute value of one of the defined valid management states for control input. The valid inputs are “standby,” “operational,” and “shutdown” state (see the behaviour definition bMAUAdminState for the description of each of these states) except that a “standby” action to a mixing type MAU or an AUI will cause the MAU to enter the “shutdown” management state.;

30.5.1.3 MAU notifications

30.5.1.3.1 nJabber

NOTIFICATION

APPROPRIATE SYNTAX:
The same as used for aJabber

BEHAVIOUR DEFINED AS:
The notification is sent whenever a managed 10 Mb/s baseband or broadband MAU enters the JABBER state.;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

This subclause formally defines the behaviours for the oAuto-Negotiation managed object class, attributes, actions, and notifications.

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.1 aAutoNegID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aAutoNegID is assigned so as to uniquely identify an Auto-Negotiation managed object among the subordinate managed objects of the containing object.;

30.6.1.1.2 aAutoNegAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:

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An interface which has Auto-Negotiation signaling ability will be enabled to do so when this attribute is in the enabled state. If disabled then the interface will act as it would if it had no Auto-Negotiation signaling.;

30.6.1.1.3 aAutoNegRemoteSignaling

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
detected
notdetected

BEHAVIOUR DEFINED AS:

The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts, /C/ ordered sets (see 36.2.4.10) or DME signals (see 73.5) were received from the remote end.;

30.6.1.1.4 aAutoNegAutoConfig

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
other
configuring
complete
disabled
parallel detect fail

BEHAVIOUR DEFINED AS:

Indicates whether Auto-Negotiation signaling is in progress or has completed. The enumeration "parallel detect fail" maps to a failure in parallel detection as defined in 28.2.3.1 or 73.7.4.1.;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE that meets the requirements of the description below:

global	Reserved for future use
other	See 30.2.5
unknown	Initializing, true state or type not yet known
10BASE-T	10BASE-T half duplex as defined in Clause 14
10BASE-TFD	Full duplex 10BASE-T as defined in Clause 14 and Clause 31
100BASE-T4	100BASE-T4 half duplex as defined in Clause 23
100BASE-TX	100BASE-TX half duplex as defined in Clause 25
100BASE-TXFD	Full duplex 100BASE-TX as defined in Clause 25 and Clause 31
FDX PAUSE	PAUSE operation for full duplex links as defined in Annex 31B
FDX APAUSE	Asymmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX SPAUSE	Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
FDX BPAUSE	Asymmetric and Symmetric PAUSE operation for full duplex links as defined in Clause 37, Annex 28B, and Annex 31B
100BASE-T2	100BASE-T2 half duplex as defined in Clause 32

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100BASE-T2FD	Full duplex 100BASE-T2 as defined in Clause 31 and Clause 32
1000BASE-X	1000BASE-X half duplex as specified in Clause 36
1000BASE-XFD	Full duplex 1000BASE-X as specified in Clause 31 and Clause 36
1000BASE-T	1000BASE-T half duplex PHY as specified in Clause 40
1000BASE-TFD	Full duplex 1000BASE-T PHY as specified in Clause 31 and as specified in Clause 40
Rem Fault1	Remote fault bit 1 (RF1) as specified in Clause 37
Rem Fault2	Remote fault bit 2 (RF2) as specified in Clause 37
10GBASE-T	10GBASE-T PHY as specified in Clause 55
1000BASE-KXFD	Full duplex 1000BASE-KX as specified in Clause 70
10GBASE-KX4FD	Full duplex 10GBASE-KX4 as specified in Clause 71
10GBASE-KRFD	Full duplex 10GBASE-KR as specified in Clause 72
40GBASE-KR4	40GBASE-KR4 as specified in Clause 84
40GBASE-CR4	40GBASE-CR4 as specified in Clause 85
100GBASE-CR10	100GBASE-CR10 as specified in Clause 85
100GBASE-CR4	100GBASE-CR4 as specified in Clause 92
100GBASE-KR4	100GBASE-KR4 as specified in Clause 93
100GBASE-KP4	100GBASE-KP4 as specified in Clause 94
Rem Fault	Remote fault bit (RF) as specified in Clause 73
FEC Capable	FEC ability as specified in Clause 73 (see 73.6.5) and Clause 74
FEC Requested	FEC requested as specified in Clause 73 (see 73.6.5) and Clause 74
isoethernet	IEEE Std 802.9 ISLAN-16T

BEHAVIOUR DEFINED AS:

This indicates the technology ability of the local device, as defined in Clause 28, Clause 37, and Clause 73.

30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalTechnologyAbility

BEHAVIOUR DEFINED AS:

This GET-SET attribute maps to the technology ability of the local device, as defined in Clause 28 and Clause 37.

NOTE—This will in every case cause temporary link loss during link renegotiation. If set to a value incompatible with aAutoNegReceivedTechnologyAbility, link negotiation will not be successful and will cause permanent link loss.;

30.6.1.1.7 aAutoNegReceivedTechnologyAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegLocalTechnologyAbility

BEHAVIOUR DEFINED AS:

Indicates the advertised technology ability of the remote hardware. For Clause 28 Auto-Negotiation, this attribute maps to the Technology Ability Field of the last received Auto-Negotiation link codeword(s). For Clause 37 Auto-Negotiation, this attribute maps to bits D0-D13 of the received Config_Reg Base Page (see 37.2.1). For Clause 73 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 73.6).;

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30.6.1.1.8 aAutoNegLocalSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
A SEQUENCE that meets the requirements of the description on http://www.ieee802.org/3/selectors/selectors.html.

BEHAVIOUR DEFINED AS:
This indicates the value of the selector field of the local hardware. The Selector Field is defined in 28.2.1.2.1 for Clause 28 Auto-Negotiation and 73.6.1 for Clause 73 Auto- Negotiation. The enumeration of the Selector Field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration “ethernet”.;

30.6.1.1.9 aAutoNegAdvertisedSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
Same as aAutoNegLocalSelectorAbility

BEHAVIOUR DEFINED AS:
In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector Field of the Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 73 Auto-Negotiation link codeword (see 73.6.1). A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration “ethernet”.

NOTE—This will in every case cause temporary link loss during link renegotiation. If set to a value incompatible with aAutoNegReceivedSelectorAbility, link negotiation will not be successful and will cause permanent link loss.;

30.6.1.1.10 aAutoNegReceivedSelectorAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
Same as aAutoNegLocalSelectorAbility

BEHAVIOUR DEFINED AS:
In the case of Clause 28 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware. It maps to the Message Selector Field of the last received Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector Field of the last received Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration “ethernet”.;

30.6.1.2 Auto-Negotiation actions

30.6.1.2.1 acAutoNegRestartAutoConfig

ATTRIBUTE

APPROPRIATE SYNTAX:
None required

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BEHAVIOUR DEFINED AS:

Forces Auto-Negotiation to begin link renegotiation. Has no effect if Auto-Negotiation signaling is disabled.;

30.6.1.2.2 acAutoNegAdminControl

ATTRIBUTE

APPROPRIATE SYNTAX:

Same as aAutoNegAdminState

BEHAVIOUR DEFINED AS:

This action provides a means to turn Auto-Negotiation signaling on or off.;

30.7 Management for Link Aggregation

Subclause 30.7 is deprecated by IEEE Std 802.1AX-2008.

30.7.1 Aggregator managed object class

This subclause formally defines the behaviours for the oAggregator managed object class, attributes, and notifications.

Some of the attributes that are part of the definition of the oAggregator managed object class are derived by summing counter values from attributes of other objects; e.g., to generate a count of received frames for the Aggregator, the individual value for each Aggregation Port contributes to the sum. Where calculations of this form are used, the values that contribute to the Aggregator's attributes are *increments* in the values of the component attributes, not their absolute values. As any individual Aggregation Port is potentially only temporarily attached to its current Aggregator, the count values it contributes to the Aggregator's counters are the increments in its values that it has experienced during the period of time that it has been attached to that Aggregator.

The counter values defined for the Aggregator have been formulated as far as possible to make the Aggregator behave like an individual IEEE 802.3 MAC. The counts of frames received and transmitted are formulated to reflect the counts that would be expected by the MAC Client; they do not include frames transmitted and received as part of the operation of LACP or the Marker protocol, only frames that pass through the interface between the MAC Client and the Aggregator. However, as LACP and the Marker protocol are, as far as the individual MACs are concerned, part of their MAC Client, the RX/TX counters for the individual MACs will reflect both control and data traffic. As counts of errors at the port level cannot always be cleanly delineated between those that occurred as a result of aggregation activity and those that did not, no attempt has been made to separate these aspects of the port error counts. Therefore, there is not necessarily a direct correspondence between the individual MAC counters and the corresponding derived counters at the Aggregator level.

It should also be noted that the counters defined for the Aggregator include values that can only apply to half duplex links. This is consistent with the approach taken in Link Aggregation that a link that can only operate as an individual link is nonetheless considered as being attached to an Aggregator. This simplifies the modelling of managed objects for links that can operate in either half or full duplex, and ensures a consistent presentation of the attributes regardless of the type of links attached to the Aggregator.

NOTE—The operation of autonegotiation may mean that a given link can operate in full duplex or half duplex, depending upon the capabilities of the device(s) connected to it. Keeping the management view the same regardless of a link's current mode of operation allows a consistent management approach to be taken across all types of links.

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30.7.1.1 Aggregator attributes

30.7.1.1.1 aAggID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The unique identifier allocated to this Aggregator by the local System. This attribute identifies an Aggregator instance among the subordinate managed objects of the containing object. This value is read-only.

30.7.1.1.2 aAggDescription

ATTRIBUTE

APPROPRIATE SYNTAX:
A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:
A human-readable text string containing information about the Aggregator. This string could include information about the distribution algorithm in use on this Aggregator; for example, “Aggregator 1, Dist Alg=Dest MAC address.” This string is read-only. The contents are vendor specific.;

30.7.1.1.3 aAggName

ATTRIBUTE

APPROPRIATE SYNTAX:
A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:
A human-readable text string containing a locally significant name for the Aggregator. This string is read-write.;

30.7.1.1.4 aAggActorSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-write MAC address value used as a unique identifier for the System that contains this Aggregator.

NOTE—From the perspective of the Link Aggregation mechanisms described in Clause 43, only a single combination of Actor’s System ID and System Priority are considered, and no distinction is made between the values of these parameters for an Aggregator and the port(s) that are associated with it (i.e., the protocol is described in terms of the operation of aggregation within a single System). However, the managed objects provided for the Aggregator and the port both allow management of these parameters. The result of this is to permit a single piece of equipment to be configured by management to contain more than one System from the point of view of the operation of Link Aggregation. This may be of particular use in the configuration of equipment that has limited aggregation capability (see 43.6).;

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30.7.1.1.5 aAggActorSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-write value indicating the priority value associated with the Actor's System ID.;

30.7.1.1.6 aAggAggregateOrIndividual

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value indicating whether the Aggregator represents an Aggregate ("TRUE") or an Individual link ("FALSE").;

30.7.1.1.7 aAggActorAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the Key for the Aggregator. The administrative Key value may differ from the operational Key value for the reasons discussed in 43.6.2. This is a 16-bit read-write value. The meaning of particular Key values is of local significance.;

30.7.1.1.8 aAggActorOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current operational value of the Key for the Aggregator. The administrative Key value may differ from the operational Key value for the reasons discussed in 43.6.2. This is a 16-bit read-only value. The meaning of particular Key values is of local significance.;

30.7.1.1.9 aAggMACAddress

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-only value carrying the individual MAC address assigned to the Aggregator.;

30.7.1.1.10 aAggPartnerSystemID

ATTRIBUTE

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APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-only MAC address value consisting of the unique identifier for the current protocol Partner of this Aggregator. A value of zero indicates that there is no known Partner. If the aggregation is manually configured, this System ID value will be a value assigned by the local System.;

30.7.1.1.11 aAggPartnerSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-only value that indicates the priority value associated with the Partner's System ID. If the aggregation is manually configured, this System Priority value will be a value assigned by the local System.;

30.7.1.1.12 aAggPartnerOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current operational value of the Key for the Aggregator's current protocol Partner. This is a 16-bit read-only value. If the aggregation is manually configured, this Key value will be a value assigned by the local System.;

30.7.1.1.13 aAggAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
up
down

BEHAVIOUR DEFINED AS:
This read-write value defines the administrative state of the Aggregator. A value of "up" indicates that the operational state of the Aggregator (aAggOperState) is permitted to be either up or down. A value of "down" forces the operational state of the Aggregator to be down. Changes to the administrative state affect the operational state of the Aggregator only, not the operational state of the Aggregation Ports that are attached to the Aggregator. A GET operation returns the current administrative state. A SET operation changes the administrative state to a new value.;

30.7.1.1.14 aAggOperState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:
up
down

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BEHAVIOUR DEFINED AS:

This read-only value defines the operational state of the Aggregator. The operational state is "up" if one or more of the Aggregation Ports that are attached to the Aggregator are collecting, or both collecting and distributing, and if the value of aAggAdminState for the Aggregator is also "up." If none of the Aggregation Ports that are attached to the Aggregator are collecting and/or distributing, or if there are no Aggregation Ports attached to this Aggregator, then the operational state is "down." An operational state of "up" indicates that the Aggregator is available for use by the MAC Client; a value of "down" indicates that the Aggregator is not available for use by the MAC Client.;

30.7.1.1.15 aAggTimeOfLastOperChange

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aTimeSinceSystemReset (Annex F.2.1) at the time the interface entered its current operational state. If the current state was entered prior to the last re-initialization of the local network management subsystem, then this object contains a value of zero. This value is read-only.;

30.7.1.1.16 aAggDataRate

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The current data rate, in bits per second, of the aggregate link. The value is calculated as N times the data rate of a single link in the aggregation, where N is the number of active links. This attribute is read-only.;

30.7.1.1.17 aAggOctetsTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data and padding octets transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include octets transmitted by the Aggregator in frames that carry LACPDUs or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.18 aAggOctetsRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 230 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data and padding octets received by this Aggregator, from the Aggregation Ports

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that are (or have been) members of the aggregation. The count does not include octets received in frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.19 aAggFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.20 aAggFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.21 aAggMulticastFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation, to a group destination address other than the broadcast address. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.22 aAggMulticastFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the data frames received by this Aggregator, from the Aggregation Ports that are (or

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have been) members of the aggregation, that were addressed to an active group address other than the broadcast address. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.23 aAggBroadcastFramesTxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the broadcast data frames transmitted by this Aggregator on all Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames transmitted by the Aggregator that carry LACP or Marker PDUs (30.7.3.1.7, 30.7.3.1.8, 30.7.3.1.9). However, it includes frames discarded by the Distribution function of the Aggregator (30.7.1.1.25). This value is read-only.;

30.7.1.1.24 aAggBroadcastFramesRxOK

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of the broadcast data frames received by this Aggregator, from the Aggregation Ports that are (or have been) members of the aggregation. The count does not include frames that carry LACP or Marker PDUs (30.7.3.1.2, 30.7.3.1.3, 30.7.3.1.4), illegal or unknown protocol frames (30.7.3.1.5, 30.7.3.1.6), or frames discarded by the Collection function of the Aggregator (30.7.1.1.26). This value is read-only.;

30.7.1.1.25 aAggFramesDiscardedOnTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames requested to be transmitted by this Aggregator that were discarded by the Distribution function of the Aggregator when conversations are re-allocated to different ports, due to the requirement to ensure that the conversations are flushed on the old ports in order to maintain proper frame ordering (43A.3), or discarded as a result of excessive collisions by ports that are (or have been) members of the aggregation. This value is read-only.;

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30.7.1.1.26 aAggFramesDiscardedOnRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames, received on all ports that are (or have been) members of the aggregation, that were discarded by the Collection function of the Aggregator as they were received on ports whose Collection function was disabled. This value is read-only.;

30.7.1.1.27 aAggFramesWithTxErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames requested to be transmitted by this Aggregator that experienced transmission errors on ports that are (or have been) members of the aggregation. This count does not include frames discarded due to excess collisions. This value is read-only.;

30.7.1.1.28 aAggFramesWithRxErrors

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames discarded on reception by all ports that are (or have been) members of the aggregation, or that were discarded by the Collection function of the Aggregator, or that were discarded by the Aggregator due to the detection of an illegal Slow Protocols PDU (30.7.3.1.6). This value is read-only.;

30.7.1.1.29 aAggUnknownProtocolFrames

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 16 000 counts per second for a single 10 Mb/s aggregation.

BEHAVIOUR DEFINED AS:

A count of data frames discarded on reception by all ports that are (or have been) members of the aggregation, due to the detection of an unknown Slow Protocols PDU (30.7.3.1.5). This value is read-only.;

30.7.1.1.30 aAggPortList

ATTRIBUTE

APPROPRIATE SYNTAX:

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A SEQUENCE OF INTEGERs that match the syntax of aAggPortID.

BEHAVIOUR DEFINED AS:

The value of this read-only attribute contains the list of Aggregation Ports that are currently attached to the Aggregator. An empty list indicates that there are no Aggregation Ports attached. Each integer value in the list carries an aAggPortID attribute value (30.7.2.1.1).;

30.7.1.1.31 aAggLinkUpDownNotificationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:

When set to "enabled," Link Up and Link Down notifications are enabled for this Aggregator. When set to "disabled," Link Up and Link Down notifications are disabled for this Aggregator. This value is read-write.;

30.7.1.1.32 aAggCollectorMaxDelay

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of this 16-bit read-write attribute defines the maximum delay, in tens of microseconds, that may be imposed by the Frame Collector between receiving a frame from an Aggregator Parser, and either delivering the frame to its MAC Client or discarding the frame (see 43.2.3.1.1).;

30.7.1.2 Aggregator Notifications

30.7.1.2.1 nAggLinkUpNotification

NOTIFICATION

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

When aAggLinkUpDownNotificationEnable is set to "enabled," a Link Up notification is generated when the Operational State of the aggregator changes from "down" to "up." When aAggLinkUpDownNotificationEnable is set to "disabled," no Link Up notifications are generated. The notification carries the identifier of the Aggregator whose state has changed.;

30.7.1.2.2 nAggLinkDownNotification

NOTIFICATION

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

When aAggLinkUpDownNotificationEnable is set to "enabled," a Link Down notification is generated when the Operational State of the aggregator changes from "up" to "down." When aAggLinkUpDownNotificationEnable is set to "disabled," no Link Down notifications are

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generated. The notification carries the identifier of the Aggregator whose state has changed.;

30.7.2 Aggregation Port managed object class

This subclause formally defines the behaviours for the oAggregationPort managed object class attributes.

30.7.2.1 Aggregation Port Attributes

30.7.2.1.1 aAggPortID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The unique identifier allocated to this Aggregation Port by the local System. This attribute identifies an Aggregation Port instance among the subordinate managed objects of the containing object. This value is read-only.

30.7.2.1.2 aAggPortActorSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A 2-octet read-write value used to define the priority value associated with the Actor's System ID.;

30.7.2.1.3 aAggPortActorSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:
MACAddress

BEHAVIOUR DEFINED AS:
A 6-octet read-only MAC address value that defines the value of the System ID for the System that contains this Aggregation Port.;

30.7.2.1.4 aAggPortActorAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the Key for the Aggregation Port. This is a 16-bit read-write value. The meaning of particular Key values is of local significance.;

30.7.2.1.5 aAggPortActorOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

The current operational value of the Key for the Aggregation Port. This is a 16-bit read-only value. The meaning of particular Key values is of local significance.;

30.7.2.1.6 aAggPortPartnerAdminSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A 2-octet read-write value used to define the administrative value of priority associated with the Partner's System ID. The assigned value is used, along with the value of aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.7 aAggPortPartnerOperSystemPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A 2-octet read-only value indicating the operational value of priority associated with the Partner's System ID. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminSystemPriority if there is no protocol Partner.;

30.7.2.1.8 aAggPortPartnerAdminSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

A 6-octet read-write MACAddress value representing the administrative value of the Aggregation Port's protocol Partner's System ID. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminKey, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.9 aAggPortPartnerOperSystemID

ATTRIBUTE

APPROPRIATE SYNTAX:

MACAddress

BEHAVIOUR DEFINED AS:

A 6-octet read-only MACAddress value representing the current value of the Aggregation Port's protocol Partner's System ID. A value of zero indicates that there is no known protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminSystemID if there is no protocol Partner.;

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30.7.2.1.10 aAggPortPartnerAdminKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the Key for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminPort, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.11 aAggPortPartnerOperKey

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current operational value of the Key for the protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminKey if there is no protocol Partner. This is a 16-bit read-only value.;

30.7.2.1.12 aAggPortSelectedAggID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The identifier value of the Aggregator that this Aggregation Port has currently selected. Zero indicates that the Aggregation Port has not selected an Aggregator, either because it is in the process of detaching from an Aggregator or because there is no suitable Aggregator available for it to select. This value is read-only.;

30.7.2.1.13 aAggPortAttachedAggID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The identifier value of the Aggregator that this Aggregation Port is currently attached to. Zero indicates that the Aggregation Port is not currently attached to an Aggregator. This value is read-only.;

30.7.2.1.14 aAggPortActorPort

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The port number locally assigned to the Aggregation Port. The port number is communicated in

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LACPDUs as the Actor_Port. This value is read-only.;

30.7.2.1.15 aAggPortActorPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The priority value assigned to this Aggregation Port. This 16-bit value is read-write.;

30.7.2.1.16 aAggPortPartnerAdminPort

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the port number for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, and aAggPortPartnerAdminPortPriority, in order to achieve manually configured aggregation.;

30.7.2.1.17 aAggPortPartnerOperPort

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The operational port number assigned to this Aggregation Port by the Aggregation Port's protocol Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminPort if there is no protocol Partner. This 16-bit value is read-only.;

30.7.2.1.18 aAggPortPartnerAdminPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The current administrative value of the port priority for the protocol Partner. This is a 16-bit read-write value. The assigned value is used, along with the value of aAggPortPartnerAdminSystemPriority, aAggPortPartnerAdminSystemID, aAggPortPartnerAdminKey, and aAggPortPartnerAdminPort, in order to achieve manually configured aggregation.;

30.7.2.1.19 aAggPortPartnerOperPortPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

The priority value assigned to this Aggregation Port by the Partner. The value of this attribute may contain the manually configured value carried in aAggPortPartnerAdminPortPriority if there is no protocol Partner. This 16-bit value is read-only.;

30.7.2.1.20 aAggPortActorAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the administrative values of Actor_State (43.4.2) as transmitted by the Actor in LACPDUs. The first bit corresponds to bit 0 of Actor_State (LACP_Activity), the second bit corresponds to bit 1 (LACP_Timeout), the third bit corresponds to bit 2 (Aggregation), the fourth bit corresponds to bit 3 (Synchronization), the fifth bit corresponds to bit 4 (Collecting), the sixth bit corresponds to bit 5 (Distributing), the seventh bit corresponds to bit 6 (Defaulted), and the eighth bit corresponds to bit 7 (Expired). These values allow administrative control over the values of LACP_Activity, LACP_Timeout, and Aggregation. This attribute value is read-write.;

30.7.2.1.21 aAggPortActorOperState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the current operational values of Actor_State (43.4.2) as transmitted by the Actor in LACPDUs. The bit allocations are as defined in 30.7.2.1.20. This attribute value is read-only.;

30.7.2.1.22 aAggPortPartnerAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the current administrative value of Actor_State for the protocol Partner. The bit allocations are as defined in 30.7.2.1.20. This attribute value is read-write. The assigned value is used in order to achieve manually configured aggregation.;

30.7.2.1.23 aAggPortPartnerOperState

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (1..8)]

BEHAVIOUR DEFINED AS:

A string of 8 bits, corresponding to the current values of Actor_State in the most recently received LACPDU transmitted by the protocol Partner. The bit allocations are as defined in 30.7.2.1.20. In the absence of an active protocol Partner, this value may reflect the manually configured value aAggPortPartnerAdminState. This attribute value is read-only.;

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30.7.2.1.24 aAggPortAggregateOrIndividual

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value indicating whether the Aggregation Port is able to Aggregate ("TRUE") or is only able to operate as an Individual link ("FALSE").;

30.7.3 Aggregation Port Statistics managed object class

This subclause formally defines the behaviours for the oAggPortStats managed object class attributes.

30.7.3.1 Aggregation Port Statistics attributes

30.7.3.1.1 aAggPortStatsID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
This read-only attribute identifies an Aggregation Port Statistics object instance among the subordinate managed objects of the containing object. The value allocated to this attribute shall be the same as the containing oAggregationPort managed object.;

30.7.3.1.2 aAggPortStatsLACPDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:
The number of valid LACPDUs received on this Aggregation Port. This value is read-only.;

30.7.3.1.3 aAggPortStatsMarkerPDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:
The number of valid Marker PDUs received on this Aggregation Port. This value is read-only.;

30.7.3.1.4 aAggPortStatsMarkerResponsePDUsRx

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

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BEHAVIOUR DEFINED AS:

The number of valid Marker Response PDUs received on this Aggregation Port. This value is read-only.;

30.7.3.1.5 aAggPortStatsUnknownRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 counts per second.

BEHAVIOUR DEFINED AS:

The number of frames received that either

— Carry the Slow Protocols Ethernet Type value (43B.4), but contain an unknown PDU, or

— Are addressed to the Slow Protocols group MAC Address (43B.3), but do not carry the Slow Protocols Ethernet Type. This value is read-only.;

30.7.3.1.6 aAggPortStatsIllegalRx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 50 counts per second.

BEHAVIOUR DEFINED AS:

The number of frames received that carry the Slow Protocols Ethernet Type value (43B.4), but contain a badly formed PDU or an illegal value of Protocol Subtype (43B.3). This value is read-only.;

30.7.3.1.7 aAggPortStatsLACPDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of LACPDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.3.1.8 aAggPortStatsMarkerPDUsTx

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of Marker PDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.3.1.9 aAggPortStatsMarkerResponsePDUsTx

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

The number of Marker Response PDUs transmitted on this Aggregation Port. This value is read-only.;

30.7.4 Aggregation Port Debug Information managed object class

This subclause formally defines the behaviours for the oAggPortDebugInformation managed object class attributes.

30.7.4.1 Aggregation Port Debug Information attributes

30.7.4.1.1 aAggPortDebugInformationID

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

This read-only attribute identifies an LACP Debug Information object instance among the subordinate managed objects of the containing object. The value allocated to this attribute shall be the same as the containing oAggregationPort managed object.;

30.7.4.1.2 aAggPortDebugRxState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
current
expired
defaulted
initialize
lacpDisabled
portDisabled

BEHAVIOUR DEFINED AS:

This attribute holds the value “current” if the Receive state machine for the Aggregation Port is in the CURRENT state, “expired” if the Receive state machine is in the EXPIRED state, “defaulted” if the Receive state machine is in the DEFAULTED state, “initialize” if the Receive state machine is in the INITIALIZE state, “lacpDisabled” if the Receive state machine is in the LACP_DISABLED state, or “portDisabled” if the Receive state machine is in the PORT_DISABLED state. This value is read-only.;

30.7.4.1.3 aAggPortDebugLastRxTime

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The value of aTimeSinceSystemReset (F.2.1) when the last LACPDU was received by this

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Aggregation Port. This value is read-only.;

30.7.4.1.4 aAggPortDebugMuxState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
detached
waiting
attached
collecting
distributing
collecting_distributing

BEHAVIOUR DEFINED AS:

This attribute holds the value “detached” if the Mux state machine (43.4.15) for the Aggregation Port is in the DETACHED state, “waiting” if the Mux state machine for the Aggregation Port is in the WAITING state, “attached” if the Mux state machine for the Aggregation Port is in the ATTACHED state, “collecting” if the Mux state machine for the Aggregation Port is in the COLLECTING state, “distributing” if the Mux state machine for the Aggregation Port is in the DISTRIBUTING state, and “collecting_distributing” if the Mux state machine for the Aggregation Port is in the COLLECTING_DISTRIBUTING state. This value is read-only.;

30.7.4.1.5 aAggPortDebugMuxReason

ATTRIBUTE

APPROPRIATE SYNTAX:

A PrintableString, 255 characters max.

BEHAVIOUR DEFINED AS:

A human-readable text string indicating the reason for the most recent change of Mux machine state. This value is read-only.;

30.7.4.1.6 aAggPortDebugActorChurnState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
noChurn
churn

BEHAVIOUR DEFINED AS:

The state of the Actor Churn Detection machine (43.4.17) for the Aggregation Port. A value of “noChurn” indicates that the state machine is in either the NO_ACTOR_CHURN or the ACTOR_CHURN_MONITOR state, and “churn” indicates that the state machine is in the ACTOR_CHURN state. This value is read-only.;

30.7.4.1.7 aAggPortDebugPartnerChurnState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:
noChurn

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churn

BEHAVIOUR DEFINED AS:

The state of the Partner Churn Detection machine (43.4.17) for the Aggregation Port. A value of "noChurn" indicates that the state machine is in either the NO_PARTNER_CHURN or the PARTNER_CHURN_MONITOR state, and "churn" indicates that the state machine is in the PARTNER_CHURN state. This value is read-only.;

30.7.4.1.8 aAggPortDebugActorChurnCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor Churn state machine has entered the ACTOR_CHURN state. This value is read-only.;

30.7.4.1.9 aAggPortDebugPartnerChurnCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner Churn state machine has entered the PARTNER_CHURN state. This value is read-only.;

30.7.4.1.10 aAggPortDebugActorSyncTransitionCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Actor's Mux state machine (43.4.15) has entered the IN_SYNC state. This value is read-only.;

30.7.4.1.11 aAggPortDebugPartnerSyncTransitionCount

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:

Count of the number of times the Partner's Mux state machine (43.4.15) has entered the IN_SYNC state. This value is read-only.;

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30.7.4.1.12 aAggPortDebugActorChangeCount

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:
Count of the number of times the Actor's perception of the LAG ID for this Aggregation Port has changed. This value is read-only.;

30.7.4.1.13 aAggPortDebugPartnerChangeCount

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 5 counts per second.

BEHAVIOUR DEFINED AS:
Count of the number of times the Partner's perception of the LAG ID (43.3.6.1) for this Aggregation Port has changed. This value is read-only.;

30.8 Management for WAN Interface Sublayer (WIS)

30.8.1 WIS managed object class

This subclause formally defines the behaviours for the oWIS managed object class and attributes.

30.8.1.1 WIS attributes

The attributes in 30.8.1.1.1 through 30.8.1.1.28 may be used, possibly in conjunction with other attributes, to derive various system performance monitoring parameters and information.

30.8.1.1.1 aWISID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aWISID is assigned so as to uniquely identify a WIS among the subordinate managed objects of the containing object.;

30.8.1.1.2 aSectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A string of 2 bits corresponding to the Section Status (50.3.2.5). The first bit corresponds to the Loss of Signal flag and maps to the LOS bit in the WIS Status 3 register. The second bit corresponds to the Loss of Frame flag and maps to the LOF bit in the WIS Status 3 register. If a

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Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10.;

30.8.1.1.3 aSectionSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET operation returns the value for *x* for Section SES definition (30.8.1.1.4). A SET operation changes the value for *x* for Section SES definition. After reset (or power-off, power-on cycle), *x* for Section SES returns to the default value 8554.

NOTE—8554 is selected to reflect the number of Section BIP-8 Errors that would occur with a random bit error ratio of 1×10^{-6} (see Annex 50A).;

30.8.1.1.4 aSectionSESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Section BIP-8 Errors (50.3.2.5) or one or more Section Defects, i.e., the LOS flag (50.3.2.5) was equal to 1 or the LOF flag (50.3.2.5) was equal to 1, where *x* is the Section SES threshold defined by aSectionSESThreshold (30.8.1.1.3).;

30.8.1.1.5 aSectionESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Section BIP-8 Errors (50.3.2.5) or one or more Section Defects, i.e., the LOS flag (50.3.2.5) was equal to 1 or the LOF flag (50.3.2.5) was equal to 1.;

30.8.1.1.6 aSectionSEFSs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in a "Severely Errored Framing Second" (SEFS), i.e., a second containing one or more SEF events (50.3.2.5).;

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30.8.1.1.7 aSectionCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 64 000 counts per second.

BEHAVIOUR DEFINED AS:

For every received B1 octet, increment counter by the number of detected Section BIP-8 Errors (50.3.2.5).;

30.8.1.1.8 aJ0ValueTX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

BEHAVIOUR DEFINED AS:

An 16 octet value defining the transmitter's Section Trace message as defined in 50.3.2.3. The first octet of the string is transmitted first, and the last octet is transmitted last. A SET operation changes the Section Trace message value. A GET operation returns the current Section Trace message value. The default transmitter's Section Trace message is the hexadecimal value 89, followed by 15 NULL characters, the hexadecimal value 00. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J0 transmit registers specified in 45.2.2.18.;

30.8.1.1.9 aJ0ValueRX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

BEHAVIOUR DEFINED AS:

An 16 octet value indicating the received Section Trace message as defined in 50.3.2.4. The first octet in this string was received first, and the last octet received last. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J0 receive registers specified in 45.2.2.19.;

30.8.1.1.10 aLineStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A string of 2 bits reflecting the Line status (50.3.2.5). The first bit corresponds to the Line Alarm Indication Signal flag and maps to the AIS-L bit. The second bit corresponds to the Line Remote Defect Indication flag and maps to the RDI-L bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.11 aLineSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:

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INTEGER

BEHAVIOUR DEFINED AS:

A GET operation returns the value for *x* for Line SES definition (30.8.1.1.12). A SET operation changes the value for x for Line SES definition. After WIS reset (or power-off, power-on cycle), *x* for Line SES returns to the default value 9835.;

NOTE—9835 is selected to reflect the number of Line BIP Errors that would occur with a random bit error ratio of 1×10^{-6} (see Annex 50A).;

30.8.1.1.12 aLineSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Line BIP Errors (50.3.2.5) or an AIS-L defect was present, i.e., the AIS-L flag (50.3.2.5) was equal to 1, where *x* is the Line SES threshold defined by aLineSESThreshold (30.8.1.1.11).;

30.8.1.1.13 aLineESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Line BIP Errors (50.3.2.5) or an AIS-L defect was present, i.e., the AIS-L flag (50.3.2.5) was equal to 1.;

30.8.1.1.14 aLineCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 12 288 000 counts per second at 10 Gb/s.

BEHAVIOUR DEFINED AS:

For every received WIS frame (50.3.2), increment counter by the number of detected Line BIP Errors (50.3.2.5).;

30.8.1.1.15 aFarEndLineSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Far End Line BIP Errors (50.3.2.5) or an RDI-L defect was present, i.e., the RDI-L flag (50.3.2.5) was equal to 1, where *x* is the Line SES threshold defined by aLineSESThreshold (30.8.1.1.11).;

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30.8.1.1.16 aFarEndLineESs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:
Increment counter by one in an "Errored Second" (ES), i.e., a second that had one or more Far End Line BIP Errors (50.3.2.5) or an RDI-L defect was present, i.e., the RDI-L flag (50.3.2.5) was equal to 1.;

30.8.1.1.17 aFarEndLineCVs

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 040 000 counts per second at 10 Gb/s.

BEHAVIOUR DEFINED AS:
For every received WIS frame (50.3.2), increment counter by the number of reported Far End Line BIP Errors (50.3.2.5).;

30.8.1.1.18 aPathStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (4)]

BEHAVIOUR DEFINED AS:
A string of 4 bits corresponding to the Path Status (50.3.2.5). The first bit corresponds to the Loss of Pointer flag and maps to the LOP-P bit, the second bit corresponds to the Alarm Indication Signal and maps to the AIS-P bit, the third bit corresponds to the Path Label Mismatch flag and maps to the PLM-P bit and the fourth bit corresponds to the Path Loss of Cell Delineation flag and maps to the LCD-P bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.19 aPathSESThreshold

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET operation returns the value for *x* for Path SES definition (30.8.1.1.20). A SET operation changes the value for *x* for Path SES definition. After reset (or power-off, power-on cycle), *x* for Path SES is set to the default value 2400.

NOTE—2400 is selected to reflect the point where 30% of all SPEs have a Path Block Error (see Annex 50A).;

30.8.1.1.20 aPathSESs

ATTRIBUTE

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APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a "Severely Errored Second" (SES), i.e., a second that had *x* or more Path Block Errors (Annex 50A) or one or more Path Defects, i.e., the LOP-P flag (50.3.2.5) was equal to 1, the AIS-P flag (50.3.2.5) was equal to 1, the PLM-P flag (50.3.2.5) was equal to 1, or the LCD-P flag (50.3.2.5) was equal to 1, where *x* is the Path SES threshold defined by aPathSESThreshold (30.8.1.1.19).;

30.8.1.1.21 aPathESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an Errored Second (ES), i.e., a second that had one or more Path Block Errors (Annex 50A) or one or more Path Defects, i.e., the LOP-P flag (50.3.2.5) was equal to 1, the AIS-P flag (50.3.2.5) was equal to 1, the PLM-P flag (50.3.2.5) was equal to 1, or the LCD-P flag (50.3.2.5) was equal to 1.;

30.8.1.1.22 aPathCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 8000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one for every received B3 indicating a Path Block Error (Annex 50A).;

30.8.1.1.23 aJ1ValueTX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

BEHAVIOUR DEFINED AS:

An 16 octet value defining the transmitter's Path Trace message as defined in 50.3.2.1. The first octet of the string is transmitted first, and the last octet is transmitted last. A SET operation changes the Path Trace message value. A GET operation returns the current Path Trace message value. The default transmitter's Path Trace message is the hexadecimal value 89, followed by 15 NULL characters, the hexadecimal value 00. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J1 transmit registers specified in 45.2.2.12.;

30.8.1.1.24 aJ1ValueRX

ATTRIBUTE

APPROPRIATE SYNTAX:

OCTET STRING, 15

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BEHAVIOUR DEFINED AS:

An 16 octet value indicating the received Path Trace message as defined in 50.3.2.4. The first octet in this string was received first, and the last octet received last. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS J1 receive registers specified in 45.2.2.13.;

30.8.1.1.25 aFarEndPathStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A string of 2 bits corresponding to the Far End Path Status (50.3.2.5). The first bit corresponds to the Far End Path Label Mismatch/Path Loss of Cell Delineation flag and maps to the Far End PLM-P/LCD-P bit, and the second bit corresponds to the Far End Path Alarm Indication Signal/ Path Loss of Pointer flag and maps to the Far End AIS-P/LOP-P bit. If a Clause 45 MDIO Interface to the WIS is present, then this attribute will map to the WIS Status 3 register specified in 45.2.2.10;

30.8.1.1.26 aFarEndPathSESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in a “Severely Errored Second” (SES), i.e., a second that had *x* or more Far End Path Block Errors or one or more Far End Path Defects reported in the Far End PLM-P/ LCD-P, AIS-P, and LOP-P bits (50.3.2.5), where *x* is the Path SES threshold defined by aPathSESThreshold (30.8.1.1.19).;

30.8.1.1.27 aFarEndPathESs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1 count per second independent of speed of operation.

BEHAVIOUR DEFINED AS:

Increment counter by one in an “Errored Second” (ES), i.e., a second that had one or more Far End Path Block Errors or one or more Far End Path Defects reported in the Far End PLM-P/LCD-P, AIS-P, and LOP-P bits (50.3.2.5).;

30.8.1.1.28 aFarEndPathCVs

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 8000 counts per second.

BEHAVIOUR DEFINED AS:

Increment counter by one for each received G1 octet indicating a Far End Path Block Error

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reported in REI-P (50.3.2.5).;

30.9 Management for DTE Power via MDI

30.9.1 PSE managed object class

This subclause formally defines the behaviours for the oPSE managed object class attributes and actions.

30.9.1.1 PSE attributes

30.9.1.1.1 aPSEID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPSEID is assigned so as to uniquely identify a PSE among the subordinate managed objects of the containing object.;

30.9.1.1.2 aPSEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

enabled	PSE functions enabled
disabled	PSE functions disabled

BEHAVIOUR DEFINED AS:
A read-only value that identifies the operational state of the PSE functions. An interface which can provide the PSE functions specified in Clause 33 will be enabled to do so when this attribute has the enumeration “enabled.” When this attribute has the enumeration “disabled” the interface will act as it would if it had no PSE function. The operational state of the PSE function can be changed using the acPSEAdminControl action. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Enable bit specified in 33.5.1.1.5.;

30.9.1.1.3 aPSEPowerPairsControlAbility

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
Indicates the ability to control which PSE Pinout Alternative (see 33.2.3) is used for PD detection and power. When “true” the PSE Pinout Alternative used can be controlled through the aSectionSESs attribute. When “false” the PSE Pinout Alternative used cannot be controlled through the aSectionSESs attribute. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control Ability bit specified in 33.5.1.2.12;

30.9.1.1.4 aPSEPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

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An ENUMERATED VALUE that has one of the following entries:

signal	PSE Pinout Alternative A
spare	PSE Pinout Alternative B

BEHAVIOUR DEFINED AS:

A read-write value that identifies the supported PSE Pinout Alternative specified in 33.2.3. A GET operation returns the PSE Pinout Alternative in use. A SET operation changes the PSE Pinout Alternative used to the indicated value only if the attribute aSectionSESThreshold is "true." If the attribute aSectionSESThreshold is "false" a SET operation has no effect.

The enumeration "signal" indicates that PSE Pinout Alternative A is used for PD detection and power. The enumeration "spare" indicates that PSE Pinout Alternative B is used for PD detection and power. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Pair Control bits specified in 33.5.1.1.4.;

30.9.1.1.5 aPSEPowerDetectionStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

disabled	PSE disabled
searching	PSE searching
deliveringPower	PSE delivering power
test	PSE test mode
fault	PSE fault detected
otherFault	PSE implementation specific fault detected

BEHAVIOUR DEFINED AS:

A read-only value that indicates the current status of the PD Detection function specified in 33.2.5.

The enumeration "disabled" indicates that the PSE State diagram (Figure 33–9) is in the state DISABLED. The enumeration "deliveringPower" indicates that the PSE State diagram is in the state POWER_ON. The enumeration "test" indicates that the PSE State diagram is in the state TEST_MODE. The enumeration "fault" indicates that the PSE State diagram is in the state TEST_ERROR. The enumeration "otherFault" indicates that the PSE State diagram is in the state IDLE due to the variable error_condition = true. The enumeration "searching" indicates the PSE State diagram is in a state other than those listed above. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PSE Status bits specified in 33.5.1.2.11.

NOTE—A derivative attribute may wish to apply a delay to the use of the "deliveringPower" enumeration as the PSE state diagram will enter then quickly exit the POWER_ON state if a short-circuit or overcurrent condition is present when power is first applied.;

30.9.1.1.6 aPSEPowerClassification

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

class0	Class 0 PD
class1	Class 1 PD
class2	Class 2 PD
class3	Class 3 PD
class4	Class 4 PD

BEHAVIOUR DEFINED AS:

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A read-only value that indicates the PD Class of a detected PD as specified in 33.2.6.1.

This value is only valid while a PD is being powered, that is the attribute aLineSESThreshold reporting the enumeration “deliveringPower.” If a Clause 22 MII or Clause 35 GMII is present, then this will map to the PD Class bits specified in 33.5.1.2.10.;

30.9.1.1.7 aPSEInvalidSignatureCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9) enters the state SIGNATURE_INVALID. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Invalid Signature bit specified in 33.5.1.2.6.;

30.9.1.1.8 aPSEPowerDeniedCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9) enters the state POWER_DENIED. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Power Denied bit specified in 33.5.1.2.4.;

30.9.1.1.9 aPSEOverLoadCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9) enters the state ERROR_DELAY_OVER. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Overload bit specified in 33.5.1.2.8.;

30.9.1.1.10 aPSEShortCounter

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:

This counter is incremented when the PSE state diagram (Figure 33–9) enters the state ERROR_DELAY_SHORT. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the Short Circuit bit specified in 33.5.1.2.7.;

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30.9.1.1.11 aPSEMPSAbsentCounter

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 2 counts per second.

BEHAVIOUR DEFINED AS:
This counter is incremented when the PSE state diagram (Figure 33–9) transitions directly from the state POWER_ON to the state IDLE due to tmpdo_timer_done being asserted. If a Clause 22 MII or Clause 35 GMII is present, then this will map to the MPS Absent bit specified in 33.5.1.2.9.;

30.9.1.1.12 aPSEActualPower

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating present (actual) power being supplied by the PSE as measured at the MDI in milliwatts. The behaviour is undefined if the state of aPSEPowerDetectionStatus is anything other than deliveringPower. The sampling frequency and averaging is vendor-defined.;

30.9.1.1.13 aPSEPowerAccuracy

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
An integer value indicating the accuracy associated with aPSEActualPower in +/- milliwatts.;

30.9.1.1.14 aPSECumulativeEnergy

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. The counter has a maximum increment rate of 100000 per second.

BEHAVIOUR DEFINED AS:
A count of the cumulative energy supplied by the PSE as measured at the MDI in millijoules.;

30.9.1.2 PSE actions

30.9.1.2.1 acPSEAdminControl

ACTION

APPROPRIATE SYNTAX:
Same as aSectionStatus

BEHAVIOUR DEFINED AS:
This action provides a means to alter aSectionStatus.;

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30.9.2 PD managed object class

This subclause formally defines the behaviours for the oPD managed object class attributes.

30.9.2.1 PD attributes

30.9.2.1.1 aPDID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPDID is assigned so as to uniquely identify a PD Power via MDI classification local system among the subordinate managed objects of the containing object.;

30.10 Layer management for Midspan

30.10.1 Midspan managed object class

This subclause formally defines the behaviours for the oMidSpan managed object class, attributes, and notifications.

30.10.1.1 Midspan attributes

30.10.1.1.1 aMidSpanID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aMidSpanID is assigned so as to uniquely identify a Midspan device among the subordinate managed objects of system (systemID and system are defined in ISO/IEC 10165-2:1992 [SMI]).;

30.10.1.1.2 aMidSpanPSEGroupCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aMidSpanPSEGroupCapacity is the number of PSE groups that can be contained within the Midspan device. Within each managed Midspan device, the PSE groups are uniquely numbered in the range from 1 to aMidSpanPSEGroupCapacity.

Some PSE groups may not be present in a given Midspan instance, in which case the actual number of PSE groups present is less than aMidSpanPSEGroupCapacity. The number of PSE groups present is never greater than aMidSpanPSEGroupCapacity.;

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30.10.1.1.3 aMidSpanPSEGroupMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A string of bits which reflects the current configuration of PSE groups that are viewed by PSE group managed objects. The length of the bitstring is "aMidSpanPSEGroupCapacity" bits. The first bit relates to PSE group 1. A "1" in the bitstring indicates presence of the PSE group, "0" represents absence of the PSE group.;

30.10.1.2 Midspan notifications

30.10.1.2.1 nMidSpanPSEGroupMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE group structure of a Midspan device. This occurs only when a PSE group is logically removed from or added to a Midspan device. The nMidSpanPSEGroupMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aMidSpanPSEGroupMap attribute.;

30.10.2 PSE Group managed object class

This subclause formally defines the behaviours for the oPSEGroup managed object class, attributes, actions, and notifications.

30.10.2.1 PSE Group attributes

30.10.2.1.1 aPSEGroupID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique within the Midspan device. The value of aPSEGroupID is assigned so as to uniquely identify a PSE group among the subordinate managed objects of the containing object (oMidSpan). This value is never greater than aMidSpanPSEGroupCapacity.;

30.10.2.1.2 aPSECapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The aPSECapacity is the number of PSEs contained within the PSE group. Valid range is 1–1024. Within each PSE group, the PSEs are uniquely numbered in the range from 1 to aPSECapacity. Some PSEs may not be present in a given PSE group instance, in which case the actual number of

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PSEs present is less than aPSECapacity. The number of PSEs present is never greater than aPSECapacity.;

30.10.2.1.3 aPSEMap

ATTRIBUTE

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
A string of bits that reflects the current configuration of PSE managed objects within this PSE group. The length of the bitstring is “aPSECapacity” bits. The first bit relates to PSE 1. A “1” in the bitstring indicates presence of the PSE, “0” represents absence of the PSE.;

30.10.2.2 PSE Group notifications

30.10.2.2.1 nPSEMapChange

NOTIFICATION

APPROPRIATE SYNTAX:
BitString

BEHAVIOUR DEFINED AS:
This notification is sent when a change occurs in the PSE structure of a PSE group. This occurs only when a PSE is logically removed from or added to a PSE group. The nPSEMapChange notification is not sent when powering up a Midspan device. The value of the notification is the updated value of the aPSEMap attribute.;

30.11 Layer Management for Physical Medium Entity (PME)

30.11.1 PAF managed object class

This subclause formally defines the behaviours for the oPAF managed object class attributes.

30.11.1.1 PAFAttributes

30.11.1.1.1 aPAFID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aTCID is assigned so as to uniquely identify a PAF among the subordinate managed objects of the containing object.

30.11.1.1.2 aPhyEnd

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value that has one of the following entries:

subscriber	subscriber mode of operation
office	office mode of operation

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BEHAVIOUR DEFINED AS:

A read-only value that indicates the subtype of the PHY (see 61.1). The enumeration “subscriber” indicates the PHY is operating as a -R subtype, the enumeration “office” indicates the PHY is operating as a -O subtype.;

30.11.1.1.3 aPHYCurrentStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:

noPMEAssigned	no PME assigned in case of PME aggregation
lossOfFraming	one or more PME in aggregation indicates Loss of Framing
lossOfSignal	one or more PME in aggregation indicates Loss of Signal
lossOfPower	one or more PME in aggregation indicates Loss of Power
configInitFailure	configuration initialization failure
noPeerPMEPresent	one or more PME in aggregation indicates no peer PME present
snrMarginViolation	one or more PME in aggregation indicates SNR Margin Violation
lineAttenViolation	one or more PME in aggregation indicates Loop Attenuation Violation

BEHAVIOUR DEFINED AS:

This read-only value indicates the current operational state of the PHY (see 62.3.4.8 and 63.2.2.3).

The enumeration “noPMEAssigned” indicates that the PAF is enabled but that there are no PMEs available for aggregation (no modems assigned), the enumeration “lossOfFraming” indicates one or more PMEs in the aggregation are reporting loss of framing, the enumeration “lossOfSignal” indicates one or more PMEs in the aggregation are reporting loss of signal, the enumeration “lossOfPower” indicates one or more PMEs in the aggregation are reporting loss of power, the enumeration “configInitFailure” indicates configuration initialization failure, the enumeration “noPeerPMEPresent” indicates one or more PMEs in the aggregation are reporting that there was no handshake message/tones send by the remote end during initialization, the enumeration “snrMarginViolation” indicates one or more PMEs in the aggregation are reporting a SNR margin violation and the enumeration “lineAttenViolation” indicates one or more PMEs in the aggregation are reporting a loop attenuation violation.;

30.11.1.1.4 aPAFSupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the TPS-TC supports the PME aggregation function (see 61.2.2). A TPS-TC that can perform PME aggregation on the available PMEs shall return the enumeration “true”. A TPS-TC that is incapable of PME aggregation shall return the enumeration “false”.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the PAF available bit in the 10P/2B capability register (see 45.2.3.25.1).;

30.11.1.1.5 aPAFAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:

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enabled
disabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the state of the PME aggregation function (see 61.2.2). When "disabled", PME aggregation will not be performed, when "enabled", PME aggregation will be performed when the link is Up, even on a single PME. As changing the state of the PME aggregation function is a traffic disruptive operation this can only occur when the link is down.

A GET operation returns the current state of the PME aggregation function. A SET operation changes the state of the PME aggregation function to the indicated value only if the attribute aPAFSupported is "true" and the link is down. If the attribute aPAFSupported is "false", or the link is not down, a SET operation has no effect.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the PAF enable bit in the 10P/2B capability register (see 45.2.3.26.3).;

30.11.1.1.6 aLocalPAFCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:

The aLocalPAFCapacity is the number of PMEs that can be aggregated by the PME aggregation function (PAF) of the PHY. Valid range is 1–32. Within each PHY, the PMEs are uniquely numbered in the range from 1 to aLocalPAFCapacity. Some PMEs may not be present in a given PHY instance, in which case the actual number of PMEs present is less than aLocalPAFCapacity. The number of PMEs present is never greater than aLocalPAFCapacity.;

30.11.1.1.7 aLocalPMEAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (32)]

BEHAVIOUR DEFINED AS:

A string of bits that indicates which PMEs are currently available for aggregation by the PME aggregation function (PAF) of the PHY (see 61.1.5.3) and therefore reflects the current configuration of PME managed objects within this PAF. The length of the bitstring is "aLocalPAFCapacity" bits. The first bit relates to PME[0]. A "1" in the bitstring indicates the PME is present and is available to the PAF for aggregation. A "0" in the bitstring indicates the PME is absent and not available to the PAF for aggregation.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the 10P/2B PME available register (see 45.2.3.27).;

30.11.1.1.8 aLocalPMEAggregate

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (32)]

BEHAVIOUR DEFINED AS:

A string of bits that indicates which PMEs are in an active aggregation in the PHY. The length of

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the bitstring is “aLocalPAFCapacity” bits. The first bit relates to PME[0]. A “1” in the bitstring indicates the PME is in an active aggregation. A “0” in the bitstring indicates the PME is not in an active aggregation.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the 10P/2B PME available registers (see 45.2.3.28).;

30.11.1.1.9 aRemotePAFSupported

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:

unknown	initializing, true state not yet know
supported	PAF supported
not supported	PAF not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the link-partner PHY supports the PME aggregation function (see 61.2.2). When the link-partner PHY can perform PME aggregation on its available PMEs the enumeration “supported” shall be returned. When the link-partner PHY is incapable of PME aggregation the enumeration “not supported” shall be returned.

If a Clause 45 MDIO Interface to the local PCS is present, then this attribute will map to the Remote PAF supported bit in the 10P/2B capability register (see 45.2.3.25.2).;

30.11.1.1.10 aRemotePAFCapacity

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

The aRemotePAFCapacity indicates the number of PME that can be aggregated by the PME aggregation function (PAF) of the link-partner PHY. Valid range is 1–32. Within the link-partner PHY, the PMEs are uniquely numbered in the range from 1 to aRemotePAFCapacity. Some PMEs may not be present in a given PHY instance, in which case the actual number of PMEs present is less than aRemotePAFCapacity. The number of PMEs present is never greater than aRemotePAFCapacity.;

30.11.1.1.11 aRemotePMEAggregate

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (32)]

BEHAVIOUR DEFINED AS:

A string of bits that indicates which PMEs are in an active aggregation in the link-partner PHY. The length of the bitstring is “aRemotePAFCapacity” bits. The first bit relates to PME[0]. A “1” in the bitstring indicates the PME is in an active aggregation. A “0” in the bitstring indicates the PME is not in an active aggregation.

If a Clause 45 MDIO Interface to the local PCS is present, then this attribute will map to the 10P/2B PME available registers (see 45.2.6.10).;

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30.11.2 PME managed object class

This subclause formally defines the behaviours for the oPME managed object class attributes.

30.11.2.1 PME Attributes

30.11.2.1.1 aPMEID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A value unique within the PAF. The value of aPMEID is assigned so as to uniquely identify a PME among the subordinate managed objects of the containing object (oPAF). This value is never greater than aLocalPAFCapacity.;

30.11.2.1.2 aPMEAdminState

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has the following entries:
enabled
disabled

BEHAVIOUR DEFINED AS:
A read-write value that indicates the state of the PME. The enumeration “disabled” indicates that the PME is disabled, the enumeration “enabled” indicates that the PME is enabled.
A GET operation returns the current state of the PME. A SET operation changes the state of the PME to the indicated value. The PME is enabled and link initialization initiated when the a SET operation is performed with the value “enabled” when the current value is “disabled”. A SET operation performed with the value “enabled” when the current value is already “enabled” will have shall have no effect.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the PMA/PMD link control register (see 45.2.1.11).;

30.11.2.1.3 aPMEStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
A ENUMERATED VALUE that has the following entries:

down not ready	link is down, not ready
down ready	link is down, ready
initializing	link is initializing
10PASS-TS	link is up as 10PASS-TS
2BASE-TL	link is up as 2BASE-TL

BEHAVIOUR DEFINED AS:
A read-only value that indicates the PME status. The enumeration “not ready” indicates that the link is down and handshake tones are not being received from a link partner, the enumeration “ready” indicates that the link is down and that handshake tones are being received from a link partner, the enumeration “initializing” indicates that the link is initializing, the enumeration “10PASS-TS” indicates that the link is up and the remote PHY is a 10PASS-TS PHY and the

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enumeration “2BASE-TL” indicates that the link is up and the remote PHY is a 2BASE-TL PHY.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the PMA/PMD link status register (see 45.2.1.16.4).;

30.11.2.1.4 aPMESNRMgn

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only value that indicates the PME current signal-to-noise ratio (SNR) Margin (see 62.3.4.7 and 63.2.2.3) with respect to the received signal in increments of dB rounded down to the nearest dB.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the 10P/2B RX SNR margin register (see 45.2.1.20).;

30.11.2.1.5 aTCCodingViolations

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 19 230 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:
A count of 64/65-octet encapsulation error. Increment the counter by one for each 64/65-octet encapsulation error detected by the 64/65-octet receive function (see Figure 61–19).;

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the TC coding violations register (see 45.2.6.12).;

30.11.2.1.6 aProfileSelect

ATTRIBUTE

APPROPRIATE SYNTAX:
SEQUENCE of the type INTEGER

BEHAVIOUR DEFINED AS:
A SEQUENCE of read-write values that indicates the operating profile numbers (see 62A.3.7 and 63A.4) of the PME. A 2BASE-TL PME supports a maximum of six values, 10PASS-TS PME can only support one. The operating profile can only be changed in a PME that is operating within a -O PHY subtype (see 61.1). As changing the operating profile is a traffic disruptive operation this can only occur when the link is down.

A GET operation returns the current operating profile number(s). A SET operation changes the operating profile to the indicated profile number only if the attribute aPHYEnd is “office” and the link is down. If the attribute aPHYEnd is “subscriber”, or the link is not down, a SET operation has no effect. If all values are zero, the PME operation is defined via the Clause 45 register settings (Table 45–42 and Table 45–43) rather than a specific profile.

NOTE 1—The profile selected by a particular value is different for 10PASS-TS and 2BASE-TL PHY types.

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NOTE 2—For a 2BASE-TL PHY six profiles per region can be chosen for handshake (see 61.4) and the one with the highest data rate will be used.;

30.11.2.1.7 aOperatingProfile

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of two instances, the first instances PMEProfileState is an ENUMERATED VALUE that has the following entries:

no link	link is down
match	link up using a profile
no match	link up not using a profile
activate failure	link activate failure

The second instances is an INTEGER

BEHAVIOUR DEFINED AS:

The ProfileState portion of the attribute is a read-only value that indicates the state of the operating profile. The enumeration “no link” indicates that the link is down, the enumeration “match” indicates that the link is up and achieved operating parameters match a defined complete profile (63A.3 and Table 63A–1), the enumeration “no match” indicates that the link is up but the achieved operating parameters do not match a defined complete profile and the enumeration “activate failure” indicates that the link failed to come up in any of the selected profiles.

The integer portion of the attribute is a read-only value that indicates the operating profile number. This value is only valid when the ProfileState portion of the attribute is “match”;

30.11.2.1.8 aPMEFECCorrectedBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:

For a 10PASS-TS PME, a count of corrected FEC blocks. This counter will not increment for other PHY types.

Increment the counter by one for each received block that is corrected by the FEC function in the PME.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the 10P FEC correctable errors (see 45.2.1.26).;

30.11.2.1.9 aPMEFECUncorrectableBlocks

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 10 000 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:

For a 10PASS-TS PME, a count of uncorrectable FEC blocks. This counter will not increment for other PME types.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC

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function in the PME.

If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute will map to the 10P FEC uncorrectable errors counter (see 45.2.1.27).;

30.11.2.1.10 aTCCRCErrors

ATTRIBUTE

APPROPRIATE SYNTAX:
Generalized nonresettable counter. This counter has a maximum increment rate of 19 230 counts per second for 10 Mb/s implementations.

BEHAVIOUR DEFINED AS:
A count of TC-CRC errors.

Increment the counter by one for each TC-CRC error detected by the 64/65-octet receive function (see 61.3.3 and Figure 61–19).;

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the TC CRC error register (see 45.2.6.11).;

30.12 Layer Management for Link Layer Discovery Protocol (LLDP)

30.12.1 LLDP Configuration managed object class

This subclause formally defines the behaviours for the oLldpXdot3Config managed object class attributes.

30.12.1.1 LLDP Configuration attributes

30.12.1.1.1 aLldpXdot3PortConfigTLVsTxEnable

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
A read-write string of 6 bits indicating, for each of the IEEE 802.3 optional LLDP TLVs, if transmit is enabled on the local LLDP agent by the network management. A "1" in the bitstring indicates transmit of the TLV is enabled, "0" indicates transmit of the TLV is disabled. The value of this attribute is preserved across reset including loss of power.

The first bit indicates if the MAC/PHY configuration/status TLV transmit is enabled, the second bit indicates if the Power via MDI TLV transmit is enabled, the third bit indicates if the deprecated Link Aggregation TLV transmit is enabled, the fourth bit indicates if the Maximum Frame Size TLV transmit is enabled, the fifth bit indicates if the EEE TLV is enabled, and the sixth bit indicates if the EEE Fast Wake TLV is enabled.;

30.12.2 LLDP Local System Group managed object class

This subclause formally defines the behaviours for the oLldpXdot3LocSystemsGroup managed object class attributes.

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30.12.2.1 LLDP Local System Group attributes

30.12.2.1.1 aLldpXdot3LocPortAutoNegSupported

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the given port (associated with the local system) supports Auto-negotiation.;

30.12.2.1.2 aLldpXdot3LocPortAutoNegEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether port Auto-negotiation is enabled on the given port associated with the local system.;

30.12.2.1.3 aLldpXdot3LocPortAutoNegAdvertisedCap

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A read-only 2-octet value that contains the value (bitmap) of the ifMauAutoNegCapAdvertisedBits object (defined in IETF RFC 4836) which is associated with the given port on the local system.;

30.12.2.1.4 aLldpXdot3LocPortOperMauType

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only 32-bit integer value that indicates the operational MAU type of the given port on the local system.

This object contains an integer value derived from the list position of the corresponding dot3MauType as listed in IETF RFC 4836 (or subsequent revisions) and is equal to the last number in the respective dot3MauType Object Identifier (OID).

For example, if the ifMauType object is dot3MauType1000BaseTHD which corresponds to {dot3MauType 29}, the numerical value of this field is 29. For MAU types not listed in IETF RFC 4836 (or subsequent revisions), the value of this field shall be set to zero.;

30.12.2.1.5 aLldpXdot3LocPowerPortClass

ATTRIBUTE

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APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has one of the following entries:

pClassPSE	PSE
pClassPD	PD

BEHAVIOUR DEFINED AS:

A read-only value that identifies the port Class of the given port associated with the local system.;

30.12.2.1.6 aLldpXdot3LocPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the local system.;

30.12.2.1.7 aLldpXdot3LocPowerMDIEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the local system.;

30.12.2.1.8 aLldpXdot3LocPowerPairControlable

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A read-only Boolean value derived from the value of pethPsePortPowerPairsControlAbility object (defined in IETF RFC 3621) and used to indicate whether the pair selection can be controlled on the given port associated with the local system.;

30.12.2.1.9 aLldpXdot3LocPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aPSEPowerPairs

BEHAVIOUR DEFINED AS:

A read-only the value that contains the value of the pethPsePortPowerPairs object (defined in IETF RFC 3621) which is associated with the given port on the local system.;

30.12.2.1.10 aLldpXdot3LocPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aPSEPowerClassification

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BEHAVIOUR DEFINED AS:

A read-only the value that contains the value of the pethPsePortPowerClassifications object (defined in IETF RFC 3621) which is associated with the given port on the local system.;

30.12.2.1.11 aLldpXdot3LocLinkAggStatus

ATTRIBUTE

APPROPRIATE SYNTAX:

BITSTRING

BEHAVIOUR DEFINED AS:

The bitmap value which contains the link aggregation capabilities and the current aggregation status of the link (see 79.3.3.1).;

30.12.2.1.12 aLldpXdot3LocLinkAggPortId

ATTRIBUTE

APPROPRIATE SYNTAX:

The same as used for aAggPortID

BEHAVIOUR DEFINED AS:

This object contains the IEEE 802.3 aggregated port identifier, aAggPortID (see 30.7.2.1.1), derived from the ifNumber of the ifIndex for the port component in link aggregation.

If the port is not in link aggregation state and/or it does not support link aggregation, this value should be set to zero.;

30.12.2.1.13 aLldpXdot3LocMaxFrameSize

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

An integer value indicating the maximum supported frame size in octets on the given port of the local system.;

30.12.2.1.14 aLldpXdot3LocPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD. A PSE shall set this bit to indicate a PSE. A PD shall set this bit to indicate a PD.;

30.12.2.1.15 aLldpXdot3LocPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

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BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating the power sources of the local system. A PSE indicates whether it is being powered by a primary power source; a backup power source; or unknown. A PD indicates whether it is being powered by a PSE and locally; by a PSE only; or unknown.;

30.12.2.1.16 aLldpXdot3LocPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:

A GET attribute that returns the priority of a PD system. For a PSE, this is the priority that the PSE assigns to the PD. For a PD, this is the priority that the PD requests from the PSE.
A SET operation changes the priority of the PD system to the indicated value.;

30.12.2.1.17 aLldpXdot3LocPDRequestedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value. For a PD, it is the power value that the PD has currently requested from the remote system. PD requested power value is the maximum input average power the PD ever draws under this power allocation if accepted. For a PSE, it is the power value that the PSE mirrors back to the remote system. This is the PD requested power value that was used by the PSE to compute the power it has currently allocated to the remote system. The PD requested power value is encoded according to Equation (79–1), where *X* is the decimal value of aLldpXdot3LocPDRequestedPowerValue.;

30.12.2.1.18 aLldpXdot3LocPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value. For a PSE, it is the power value that the PSE has currently allocated to the remote system. The PSE allocated power value is the maximum input average power that the PSE wants the PD to ever draw under this allocation if it is accepted. For a PD, it is the power value that the PD mirrors back to the remote system. This is the PSE allocated power value that was used by the PD to compute the power that it has currently requested from the remote system. The PSE allocated power value is encoded according to Equation (79–2), where *X* is the decimal value of aLldpXdot3LocPSEAllocatedPowerValue.;

30.12.2.1.19 aLldpXdot3LocResponseTime

ATTRIBUTE

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APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the response time in seconds of the local system. For a PD, it is the maximum time required to update the value of attribute aLldpXdot3LocPDRequestedPowerValue when the remote system requests the PD to change its max power draw. For a PSE, it is the maximum time required to update the value of attribute aLldpXdot3LocPDRequestedPowerValue when the remote system requests of the PSE a new power value.;

30.12.2.1.20 aLldpXdot3LocReady

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:

FALSE:	Local system has not completed initialization of the Data Link Layer classification engine and is not ready to receive/transmit an LLDPDU containing a Power via MDI TLV.
TRUE:	Local system has initialized the Data Link Layer classification engine and is ready to receive/transmit an LLDPDU containing a Power via MDI TLV.

BEHAVIOUR DEFINED AS:
A GET operation returns the initialization status of the Data Link Layer classification engine on the local system.;

30.12.2.1.21 aLldpXdot3LocReducedOperationPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the reduced operation power value. For a PD, it is a power value that is lower than the currently requested power value. This reduced operation power value represents a power state in which the PD could continue to operate, but with less functionality than at the current PD requested power value. The PSE could optionally use this information in the event that the PSE subsequently requests a lower PD power value than the PD requested power value. For a PSE, it is a power value that the PSE could ask the PD to move to if the PSE wants the PD to move to a lower power state. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17). The default value for this field is the hexadecimal value FFFF.;

30.12.2.1.22 aLldpXdot3LocTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system can support in the transmit direction. This attribute maps to the variable LocTxSystemValue as defined in 78.4.2.3;

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30.12.2.1.23 aLldpXdot3LocTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable LocTxSystemValueEcho as defined in 78.4.2.3;

30.12.2.1.24 aLldpXdot3LocRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is requesting in the receive direction. This attribute maps to the variable LocRxSystemValue as defined in 78.4.2.3;

30.12.2.1.25 aLldpXdot3LocRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable LocRxSystemValueEcho as defined in 78.4.2.3;

30.12.2.1.26 aLldpXdot3LocFbTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of the fallback $T_{w\_sys\_tx}$ that the local system is advertising to the remote system. This attribute maps to the variable LocFbSystemValue as defined in 78.4.2.3;

30.12.2.1.27 aLldpXdot3TxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:

FALSE:	Local system has not completed initialization of the EEE transmit Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.

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TRUE: Local system has initialized the EEE transmit Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:

A GET operation returns the initialization status of the EEE transmit Data Link Layer management function on the local system.;

30.12.2.1.28 aLldpXdot3RxDllReady

ATTRIBUTE

APPROPRIATE SYNTAX:

A BOOLEAN value:

FALSE: Local system has not completed initialization of the EEE receive Data Link Layer management function and is not ready to receive/transmit an LLDPDU containing a EEE TLV.

TRUE: Local system has initialized the EEE receive Data Link Layer management function and is ready to receive/transmit an LLDPDU containing a EEE TLV.

BEHAVIOUR DEFINED AS:

A GET operation returns the initialization status of the EEE receive Data Link Layer management function on the local system.;

30.12.2.1.29 aLldpXdot3LocDllEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:

A BOOLEAN value:

FALSE: Local system has not completed auto-negotiation with a link partner that has indicated at least one EEE capability.

TRUE: Local system has completed auto-negotiation with a link partner that has indicated at least one EEE capability.

BEHAVIOUR DEFINED AS:

A GET operation returns the status of the EEE capability negotiation on the local system.;

30.12.2.1.30 aLldpXdot3LocTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system can support in the transmit direction. This attribute maps to the variable LocTxSystemFW as defined in 78.4.2.3;

30.12.2.1.31 aLldpXdot3LocTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

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A GET attribute that returns the value of LPI_FW that the remote system is advertising that it can support in the transmit direction and is echoed by the local system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable LocTxSystemFWEcho as defined in 78.4.2.3;

30.12.2.1.32 aLldpXdot3LocRxFw

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the local system is requesting in the receive direction. This attribute maps to the variable LocRxSystemFW as defined in 78.4.2.3;

30.12.2.1.33 aLldpXdot3LocRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of LPI_FW that the remote system is advertising that it is requesting in the receive direction and is echoed by the local system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable LocRxSystemFWEcho as defined in 78.4.2.3;

30.12.3 LLDP Remote System Group managed object class

This subclause formally defines the behaviours for the oLldpXdot3RemSystemsGroup managed object class attributes.

30.12.3.1 LLDP Remote System Group attributes

30.12.3.1.1 aLldpXdot3RemPortAutoNegSupported

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the given port (associated with the remote system) supports Auto-negotiation.;

30.12.3.1.2 aLldpXdot3RemPortAutoNegEnabled

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether port Auto-negotiation is enabled on the given port associated with the remote system.;

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30.12.3.1.3 aLldpXdot3RemPortAutoNegAdvertisedCap

ATTRIBUTE

APPROPRIATE SYNTAX:
OCTET STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A read-only 2-octet value that contains the value (bitmap) of the ifMauAutoNegCapAdvertisedBits object (defined in IETF RFC 4836) which is associated with the given port on the remote system.;

30.12.3.1.4 aLldpXdot3RemPortOperMauType

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A read-only 32-bit integer value that indicates the operational MAU type of the given port on the remote system.

This object contains an integer value derived from the list position of the corresponding dot3MauType as listed in IETF RFC 4836 (or subsequent revisions) and is equal to the last number in the respective dot3MauType OID.

For example, if the ifMauType object is dot3MauType1000BaseTHD which corresponds to {dot3MauType 29}, the numerical value of this field is 29. For MAU types not listed in IETF RFC 4836 (or subsequent revisions), the value of this field shall be set to zero.;

30.12.3.1.5 aLldpXdot3RemPowerPortClass

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED VALUE that has one of the following entries:

pClassPSE	PSE
pClassPD	PD

BEHAVIOUR DEFINED AS:
A read-only value that identifies the port Class of the given port associated with the remote system.;

30.12.3.1.6 aLldpXdot3RemPowerMDISupported

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to indicate whether the MDI power is supported on the given port associated with the remote system.;

30.12.3.1.7 aLldpXdot3RemPowerMDIEnabled

ATTRIBUTE

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APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value used to identify whether MDI power is enabled on the given port associated with the remote system.;

30.12.3.1.8 aLldpXdot3RemPowerPairControlable

ATTRIBUTE

APPROPRIATE SYNTAX:
BOOLEAN

BEHAVIOUR DEFINED AS:
A read-only Boolean value is derived from the value of pethPsePortPowerPairsControlAbility object (defined in IETF RFC 3621) and is used to indicate whether the pair selection can be controlled on the given port associated with the remote system.;

30.12.3.1.9 aLldpXdot3RemPowerPairs

ATTRIBUTE

APPROPRIATE SYNTAX:
The same as used for aPSEPowerPairs

BEHAVIOUR DEFINED AS:
A read-only the value that contains the value of the pethPsePortPowerPairs object (defined in IETF RFC 3621) which is associated with the given port on the remote system.;

30.12.3.1.10 aLldpXdot3RemPowerClass

ATTRIBUTE

APPROPRIATE SYNTAX:
The same as used for aPSEPowerClassification

BEHAVIOUR DEFINED AS:
A read-only the value that contains the value of the pethPsePortPowerClassifications object (defined in IETF RFC 3621) which is associated with the given port on the remote system.;

30.12.3.1.11 aLldpXdot3RemLinkAggStatus

ATTRIBUTE

APPROPRIATE SYNTAX:
BITSTRING

BEHAVIOUR DEFINED AS:
The bitmap value which contains the link aggregation capabilities and the current aggregation status of the link (see 79.3.3.1).;

30.12.3.1.12 aLldpXdot3RemLinkAggPortId

ATTRIBUTE

APPROPRIATE SYNTAX:
The same as used for aAggPortID

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BEHAVIOUR DEFINED AS:

This object contains the IEEE 802.3 aggregated port identifier, aAggPortID (see 30.7.2.1.1), derived from the ifNumber of the ifIndex for the port component in link aggregation.

If the port is not in link aggregation state and/or it does not support link aggregation, this value should be set to zero.;

30.12.3.1.13 aLldpXdot3RemMaxFrameSize

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

An integer value indicating the maximum supported frame size in octets on the given port of the remote system.;

30.12.3.1.14 aLldpXdot3RemPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating whether the remote system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD.;

30.12.3.1.15 aLldpXdot3RemPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:

BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:

A GET attribute that returns a bit string indicating the power sources of the remote system. When the remote system is a PSE, it indicates whether it is being powered by a primary power source; a backup power source; or unknown. When the remote system is a PD, it indicates whether it is being powered by a PSE and locally; locally only; by a PSE only; or unknown.;

30.12.3.1.16 aLldpXdot3RemPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:

A GET operation returns the priority of the PD system received from the remote system. For a PSE, this is the priority that the remote system requests from the PSE. For a PD, this is the priority that the remote system has assigned to the PD.;

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30.12.3.1.17 aLldpXdot3RemPDRequestedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value that was used by the remote system to compute the power value that is has currently allocated to the PD. For a PSE, it is the PD requested power value received from the remote system. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17).;

30.12.3.1.18 aLldpXdot3RemPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value received from the remote system. For a PSE, it is the PSE allocated power value that was used by the remote system to compute the power value that it has currently requested from the PSE. For a PD, it is the PSE allocated power value received from the remote system. The definition and encoding of PSE allocated power value is the same as described in aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18).;

30.12.3.1.19 aLldpXdot3RemTxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system can support in the transmit direction. This attribute maps to the variable RemTxSystemValue as defined in 78.4.2.3;

30.12.3.1.20 aLldpXdot3RemTxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable RemTxSystemValueEcho as defined in 78.4.2.3;

30.12.3.1.21 aLldpXdot3RemRxTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

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BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the remote system is requesting in the receive direction. This attribute maps to the variable RemRxSystemValue as defined in 78.4.2.3;

30.12.3.1.22 aLldpXdot3RemRxTwSysEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of $T_{w\_sys\_tx}$ that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable RemRxSystemValueEcho as defined in 78.4.2.3;

30.12.3.1.23 aLldpXdot3RemFbTwSys

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of fallback $T_{w\_sys\_tx}$ that the remote system is advertising. This attribute maps to the variable RemFbSystemValue as defined in 78.4.2.3;

30.12.3.1.24 aLldpXdot3RemTxFw

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the remote system can support in the transmit direction. This attribute maps to the variable RemTxSystemFW as defined in 78.4.2.3;

30.12.3.1.25 aLldpXdot3RemTxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system is advertising that it can support in the transmit direction as echoed by the remote system under the control of the EEE DLL receiver state diagram. This attribute maps to the variable RemTxSystemFWEcho as defined in 78.4.2.3;

30.12.3.1.26 aLldpXdot3RemRxFw

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

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BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the remote system is requesting in the receive direction. This attribute maps to the variable RemRxSystemFW as defined in 78.4.2.3;

30.12.3.1.27 aLldpXdot3RemRxFwEcho

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

A GET attribute that returns the value of LPI_FW that the local system is advertising that it is requesting in the receive direction as echoed by the remote system under the control of the EEE DLL transmitter state diagram. This attribute maps to the variable RemRxSystemFWEcho as defined in 78.4.2.3;

30.13 Management for oTimeSync entity

If the optional TimeSync function is implemented, then the oTimeSync managed object class shall be implemented in its entirety. All attributes of this managed object class are mandatory. TimeSync management is optional with respect to all other CSMA/CD management.

30.13.1 TimeSync entity managed object class

This subclause formally defines the behaviours for the oTimeSync managed object class attributes.

30.13.1.1 aTimeSyncCapabilityTX

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if the TimeSync capability is supported in the transmit path and false otherwise.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute is equal to the logical OR operation over the values stored in the following instantiated MDIO registers (for each MMD, in case of multiple instances) 1.1800.1, 2.1800.1, 3.1800.1, 4.1800.1, 5.1800.1, and 6.1800.1 (see 45.2.1.128, 45.2.2.20, 45.2.3.48, 45.2.4.12, 45.2.5.12, 45.2.6.14, respectively).

30.13.1.2 aTimeSyncCapabilityRX

ATTRIBUTE

APPROPRIATE SYNTAX:

BOOLEAN

BEHAVIOUR DEFINED AS:

True if the TimeSync capability is supported in the receive path and false otherwise.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute is equal to the logical OR operation over the values stored in the following instantiated MDIO registers (for each MMD, in case of multiple instances) 1.1800.0, 2.1800.0, 3.1800.0, 4.1800.0, 5.1800.0, and 6.1800.0 (see 45.2.1.128, 45.2.2.20, 45.2.3.48, 45.2.4.12, 45.2.5.12, 45.2.6.14, respectively).

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30.13.1.3 aTimeSyncDelayTXmax

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The maximum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute represents the maximum transmit path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

— for PMA/PMD: 1.1801 and 1.1802, see 45.2.1.129
— for WIS: 2.1801 and 2.1802, see 45.2.2.21
— for PCS: 3.1801 and 3.1802, see 45.2.3.49
— for PHY XS: 4.1801 and 4.1802, see 45.2.4.13
— for DTE XS: 5.1801 and 5.1802, see 45.2.5.13
— for TC: 6.1801 and 6.1802, see 45.2.6.15

30.13.1.4 aTimeSyncDelayTXmin

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The minimum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute represents the minimum transmit path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

— for PMA/PMD: 1.1803 and 1.1804, see 45.2.1.129
— for WIS: 2.1803 and 2.1804, see 45.2.2.21
— for PCS: 3.1803 and 3.1804, see 45.2.3.49
— for PHY XS: 4.1803 and 4.1804, see 45.2.4.13
— for DTE XS: 5.1803 and 5.1804, see 45.2.5.13
— for TC: 6.1803 and 6.1804, see 45.2.6.15

30.13.1.5 aTimeSyncDelayRXmax

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The maximum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute represents the maximum receive path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

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— for PMA/PMD: 1.1805 and 1.1806, see 45.2.1.130
— for WIS: 2.1805 and 2.1806, see 45.2.2.22
— for PCS: 3.1805 and 3.1806, see 45.2.3.50
— for PHY XS: 4.1805 and 4.1806, see 45.2.4.14
— for DTE XS: 5.1805 and 5.1806, see 45.2.5.14
— for TC: 6.1805 and 6.1806, see 45.2.6.16

30.13.1.6 aTimeSyncDelayRXmin

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The minimum data delay as specified in 90.7, expressed in units of ns.
If a Clause 45 MDIO Interface to to PMA/PMD, WIS, PCS, PHY XS, DTE XS and/or TC is present, then the value stored in this attribute represents the minimum receive path data delay values, consisting of the sum of the values of the registers in the instantiated sublayers (for each MMD, in case of multiple instances):

— for PMA/PMD: 1.1807 and 1.1808, see 45.2.1.130
— for WIS: 2.1807 and 2.1808, see 45.2.2.22
— for PCS: 3.1807 and 3.1808, see 45.2.3.50
— for PHY XS: 4.1807 and 4.1808, see 45.2.4.14
— for DTE XS: 5.1807 and 5.1808, see 45.2.5.14
— for TC: 6.1807 and 6.1808, see 45.2.6.16

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31. MAC Control

31.1 Overview

This clause specifies an optional MAC Control sublayer (MAC Control) for use with the CSMA/CD MAC. MAC Control provides for real-time control and manipulation of MAC sublayer operation. This clause specifies a generalized architecture and protocol for MAC Control. Specific implementations of control functions using this protocol are specified in the normative annexes to this clause. The MAC Control protocol is specified such that it can support new functions to be implemented and added to this standard in the future.

Non-realtime, or quasistatic control (e.g., configuration of MAC operational parameters) is provided by Layer Management.

Operation of the MAC Control sublayer is transparent to the CSMA/CD MAC.

The body of this clause and its associated annexes contain state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram shall prevail. The notation used in the state diagrams follows the conventions of 21.5.

31.2 Layer architecture

The MAC Control sublayer is a client of the CSMA/CD MAC. Figure 31–1 depicts the architectural positioning of the MAC Control sublayer with respect to the CSMA/CD MAC and the MAC Control client. MAC Control clients may include the Bridge Relay Entity, LLC, or other applications.

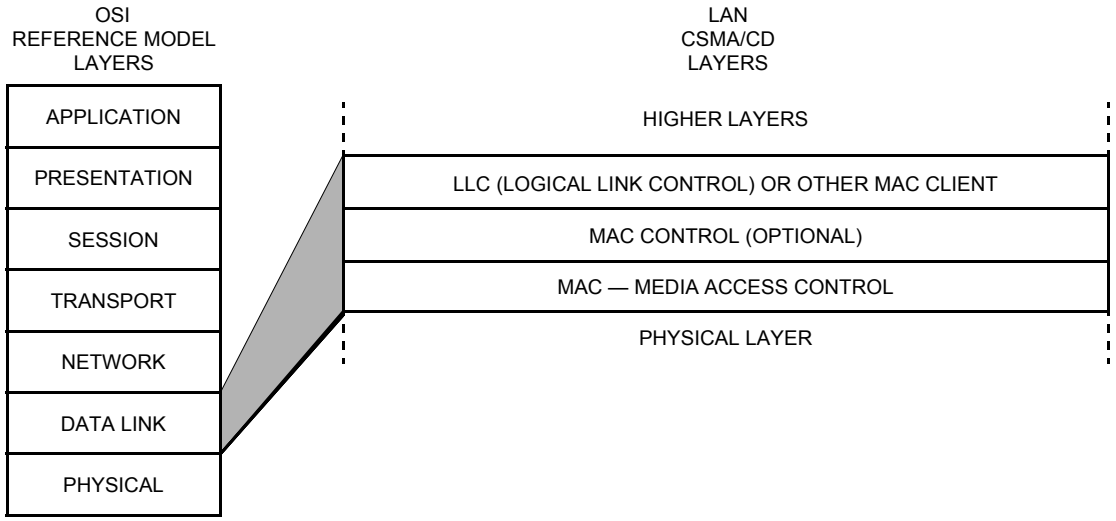


Figure 31–1—Architectural positioning of MAC Control sublayer

31.3 Support by interlayer interfaces

This subclause describes how the MAC Control sublayer uses the MAC service interface specified in Clause 2. The optional MAC Control sublayer is inserted between the MAC sublayer and its MAC client. The MAC Control sublayer uses the MAC service interface to interface to the MAC client and to the MAC.

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Figure 31–2 depicts the usage of interlayer interfaces by the MAC Control sublayer. Devices that implement the MAC Control sublayer shall support the MAC service primitives, MA_CONTROL.request and MA_-CONTROL.indication, as specified in this clause.

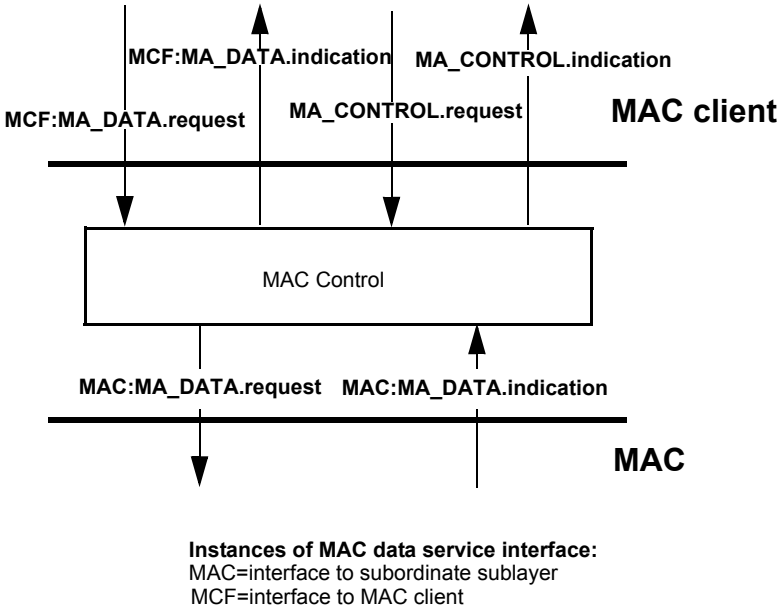


Figure 31–2—MAC Control sublayer support of interlayer service interfaces

Clients of the MAC Control sublayer may generate either MCF:MA_CONTROL.request or MCF:MA_-DATA.request primitives. MA_CONTROL.request primitives generated by MAC clients are interpreted by the MAC Control sublayer, and may result in the generation of MAC:MA_DATA.request calls to the MAC sublayer, or other actions as necessary to support the requested MAC Control sublayer function. Based upon the state of the MAC Control sublayer, MCF:MA_DATA.request primitives may cause the immediate generation of a MAC:MA_DATA.request call to the MAC sublayer, or be delayed, discarded, or modified in order to perform the requested MAC Control function.

All MAC frames validly received by the CSMA/CD MAC are passed to the MAC Control sublayer for interpretation. If the MAC frame is destined for the MAC client, the MAC Control sublayer generates an MCF:MA_DATA.indication primitive, providing complete transparency for normal data exchange between MAC clients. If the MAC frame is destined for the MAC Control sublayer entity, it is interpreted and acted on internal to the MAC Control sublayer. This may result in state changes within the MAC Control sublayer, the generation of MA_CONTROL.indication primitives, or other actions as necessary to support the MAC Control sublayer function. MAC Control sublayer functions shall always sink MAC Control frames.

In the MAC:MA_DATA.indication primitive, MAC frames destined for the MAC Control sublayer (MAC Control frames) are distinguished from MAC frames destined for MAC clients by a unique Length/Type field identifier.

The MAC Control sublayer generates MA_CONTROL.indication primitives to its client, signaling the current value of internal state variables. Each MAC Control function implemented may have its own function-specific state indications.

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31.3.1 MA_CONTROL.request

Implementation of the MA_CONTROL.request primitive is mandatory.

31.3.1.1 Function

This primitive defines the transfer of control commands from a MAC client entity to the local MAC Control sublayer entity.

31.3.1.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_CONTROL.request      (
                        destination_address,
                        opcode,
                        request_operand_list
                        )
```

The destination_address parameter may specify either an individual or a group MAC entity address. It must contain sufficient information to create the DA field that is prepended to the MAC frame by the local MAC sublayer entity. The opcode specifies the control operation requested by the MAC client entity. The request_operand_list is an opcode-specific set of parameters.

The valid opcodes and their respective meanings are defined in Annex 31A.

31.3.1.3 When generated

This primitive is generated by a MAC client whenever it wishes to use the services of the optional MAC Control sublayer entity.

31.3.1.4 Effect of receipt

The effect of receipt of this primitive by the MAC Control sublayer is opcode-specific. (See Annex 31A.)

31.3.2 MA_CONTROL.indication

Implementation of the MA_CONTROL.indication primitive is mandatory.

31.3.2.1 Function

This primitive defines the transfer of control status indications from the MAC Control sublayer entity to the MAC client entity.

31.3.2.2 Semantics of the service primitive

The semantics of the primitive are as follows:

```
MA_CONTROL.indication       (
                            opcode,
                            indication_operand_list
                            )
```

The elements of the indication_operand_list are opcode-specific, and specified in Annex 31A.

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31.3.2.3 When generated

The MA_CONTROL.indication is generated by the MAC Control sublayer under conditions specific to each MAC Control operation.

31.3.2.4 Effect of receipt

The effect of receipt of this primitive by the MAC client is not specified in this clause. See the list of MAC control functions in Annex 31A.

31.4 MAC Control frames

MAC Control frames comprise MAC client data for the CSMA/CD MAC, as specified in Clause 3. They are encapsulated by the CSMA/CD MAC; that is, they are prepended by a Preamble and Start-of-Frame delimiter and appended by an FCS.

MAC Control frames are distinguished from other MAC frames only by their Length/Type field identifier.

31.4.1 MAC Control frame format

For any particular implementation of this standard, MAC Control frames are fixed length, containing minFrameSize–32 bits. The underlying MAC prepends the Preamble and Start-of-Frame delimiter fields, and appends the FCS. Figure 31–3 depicts the MAC Control frame format.

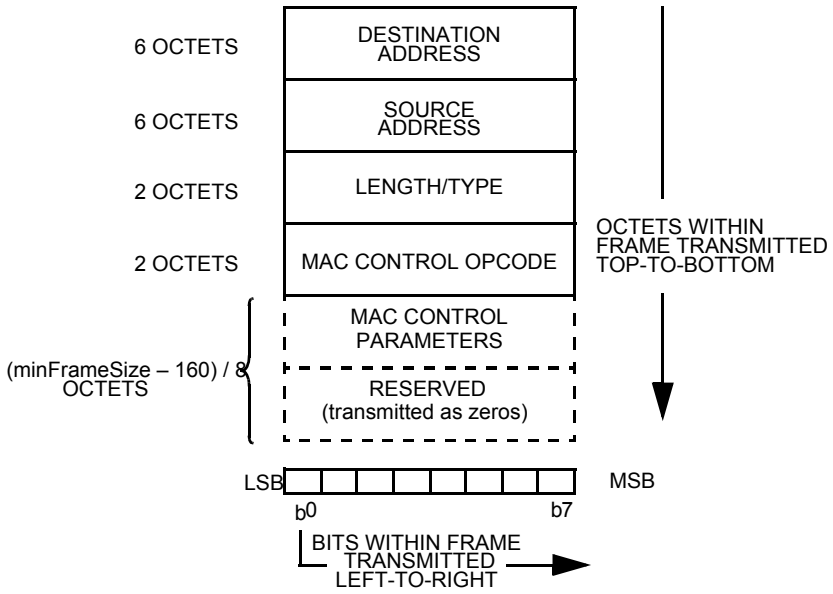


Figure 31–3—MAC Control frame format

31.4.1.1 Destination Address field

The Destination Address field of a MAC Control frame contains the 48-bit address of the station(s) for which the frame is intended. It may be an individual or multicast (including broadcast) address. Permitted values for the Destination Address field may be specified separately for each MAC Control opcode in the annexes to Clause 31.

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31.4.1.2 Source Address field

The Source Address field of a MAC Control frame contains the 48-bit individual address of the station sending the frame.

31.4.1.3 Length/Type field

The Length/Type field of a MAC Control frame is a 2-octet field that shall contain the hexadecimal value: 88-08. This value carries the Ethertype interpretation (see 3.2.6), and has been universally assigned for MAC Control of CSMA/CD LANs.

31.4.1.4 MAC Control Opcode field

The MAC Control Opcode field shall contain a 2-octet operation code indicating the MAC Control function. It defines the semantics of the MAC Control Parameters field specified in 31.4.1.5. Annex 31A contains the list of defined MAC Control opcodes and interpretations.

A MAC Control frame shall contain exactly one MAC Control opcode.

31.4.1.5 MAC Control Parameters field

The MAC Control Parameters field shall contain MAC Control opcode-specific parameters. This field may contain none, one, or more parameters as defined by the MAC Control Opcode. The opcode-specific semantics of the MAC Control Parameters field are defined in the normative annex specifying each MAC Control function.

The MAC Control Parameters field shall contain an integral number of octets. The length of the MAC Control Parameters field varies from a minimum of zero, to a maximum of minFrameSize –160 bits. See 4.2.3.3 for a discussion of minFrameSize.

31.4.1.6 Reserved field

The Reserved field is used when the MAC Control parameters do not fill the fixed length MAC Control frame. The size of the Reserved field, if any, is determined by the size of the MAC Control Parameters field supplied by MAC Control and the minimum frame size parameter of the particular implementation.

The length of Reserved field required for a MAC Control Parameters field that is n octets long is [minFrameSize – $(8 \times n + 160)$] bits. See 4.2.3.3 for a discussion of minFrameSize. The Reserved field is transmitted as all zeros.

31.5 Opcode-independent MAC Control sublayer operation

The MAC passes to the MAC Control sublayer all valid MAC frames via the MA_DATA.indication primitive. Invalid MAC frames are not passed to the MAC Control sublayer (see 3.4).

31.5.1 Frame parsing and data frame reception

Upon receipt, the MAC Control sublayer parses the incoming MAC frame to determine whether it is destined for the MAC client (data frame) or for a specific function within the MAC Control sublayer entity itself (MAC Control frame). MAC Control frames with a length of minFrameSize and a supported opcode field are interpreted and acted upon by the MAC Control sublayer.

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A MAC frame that does not contain the unique Length/Type field specified in 31.4.1.3 is a data frame. The receipt of a data frame results in the generation of a MCF:MA_DATA.indication primitive by the MAC Control sublayer, with its parameters identical to the MAC:MA_DATA.indication primitive.

NOTE—For Length/Type field values in the range between maxBasicDataSize and minTypeValue, the behavior of the RemovePad function in the underlying MAC sublayer is unspecified. Frames with Length/Type field values in this range may or may not be passed up by the MAC sublayer.

MAC Control frames with a length greater than minFrameSize and a supported opcode field may be either discarded, or truncated to minFrameSize, interpreted, and acted upon. Unsupported MAC Control frames are discarded. Discarded frames are neither interpreted nor acted upon by the MAC Control sublayer.

31.5.2 Control frame reception

Validly received MAC Control frames are further parsed to determine the opcode. The location of the opcode within a valid MAC Control frame and its format are specified in 31.4.1.4 and Figure 31–3. If the MAC Control sublayer entity supports the function requested by the specified opcode, it interprets and acts upon the MAC Control frame in an opcode- and request_operand-specific manner. (See Annex 31A.) This action may change the state of the MAC Control sublayer, affecting its behavior with respect to data transmission requests by the MAC client, future control frame receptions, or control indications to the MAC client.

If the MAC Control sublayer entity does not support the function requested by the specified opcode, it discards the MAC Control frame. The discard of a frame in this manner may be reported to network management.

31.5.3 Opcode-independent MAC Control receive state diagram

The MAC Control sublayer shall implement the Receive state diagram specified in this subclause.

31.5.3.1 Constants

802.3_MAC_Control
: The 16-bit Length/Type field value reserved for CSMA/CD MAC Control usage, specified in 31.4.1.3.

31.5.3.2 Variables

receiveEnabled
: A Boolean set by Network Management to indicate that the station is permitted to receive from the network.

  Values: true; Receiver is enabled by management
  false; Receiver is disabled by management

DA
: The destination address field parsed from the received frame.

SA
: The source address field parsed from the received frame.

lengthOrType
: The lengthOrType field parsed from the received frame.

data
: The data payload field parsed from the received frame.

fcs
: The fcs field parsed from the received frame.

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fcsPresent
: A Boolean set by the MAC sublayer. See 4.3.2.

mac_service_data_unit
: The concatenation of lengthOrType, data.

ReceiveStatus
: Indicates the status of the received frame. See 4.3.2.

opcode
: The MAC Control opcode field parsed from the received frame.

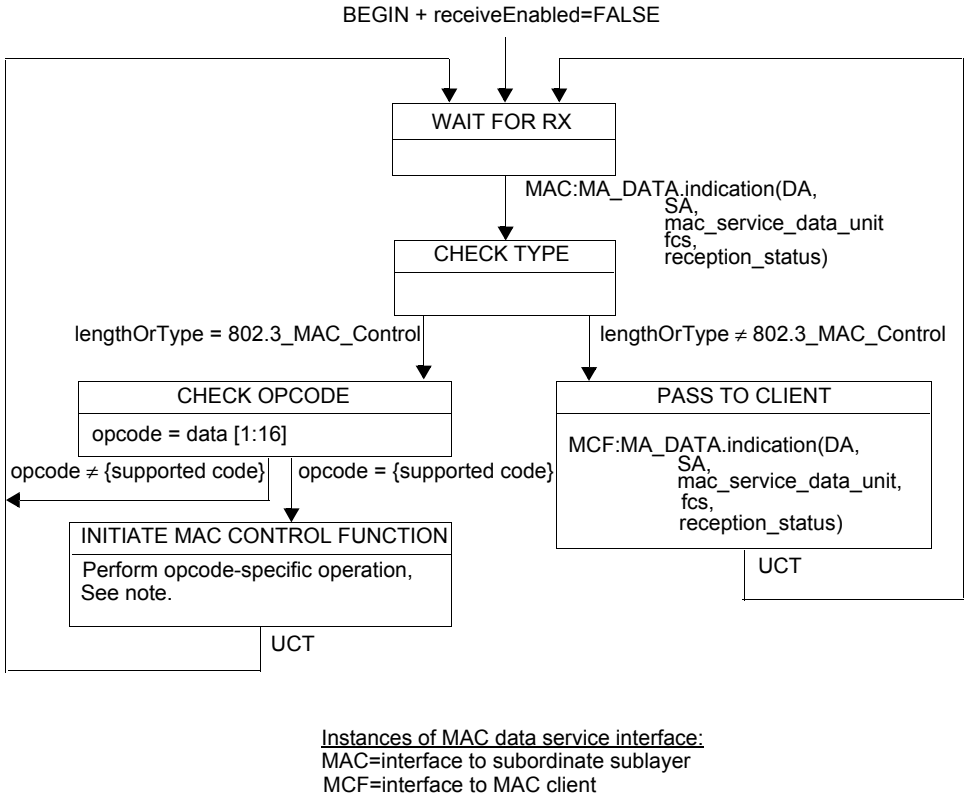
31.5.3.3 Messages

MA_DATA.indication

The service primitive used to pass a validly received MAC frame between the MAC and the MAC Control sublayers, or between the MAC Control sublayer and the MAC client. When generated by the MAC sublayer, this message is used by the MAC Control Receive state diagram as the condition for transition between WAIT FOR RX and CHECK TYPE states. While in the PASS TO CLIENT state, the MAC Control Receive state diagram generates this message to the MAC client.

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31.5.3.4 Opcode-independent MAC Control Receive state diagram



NOTE—The opcode-specific operation (see Annex 31A) is launched as a parallel process by the MAC Control sublayer, and not as a synchronous function. Progress of the generic MAC Control Receive state diagram (as shown in this figure) is not implicitly impeded by the launching of the opcode-specific function.

Figure 31–4—Generic MAC Control Receive state diagram

The functions performed in the INITIATE MAC CONTROL FUNCTION state are opcode-specific (see Annex 31A).

31.6 Compatibility requirements

An instantiation of the MAC Control sublayer is not required to implement all valid control functions specified in Annex 31A.

31.7 MAC Control client behavior

The MAC Control sublayer uses the services of the underlying connectionless-mode MAC sublayer to exchange both Data and Control frames. The MAC Control sublayer does not provide any mechanism for recovery from lost, discarded, damaged, or delayed frames. It is the responsibility of the MAC Control client to implement mechanisms for dealing with lost, discarded, damaged, and delayed frames, if necessary.

Since implementation of the MAC Control sublayer is optional, a MAC Control client cannot assume the existence of a MAC Control sublayer entity in a peer DTE.

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31.8 Protocol implementation conformance statement (PICS) proforma for Clause 31, MAC Control[12]

31.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 31, the optional MAC Control sublayer, shall complete the following PICS proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31.8.2 Identification

31.8.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-201x, Clause 31, MAC Control
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-201x.)	

Date of Statement	

[12] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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31.8.3 PICS proforma for MAC Control frames

31.8.3.1 Support by interlayer interfaces

Item	Feature	Subclause	Value/Comment	Status	Support
SI1	Support for MAC service primitives, MA_-CONTROL.request and MA_CON-TROL.indication	31.3	Required	M	Yes [ ]

31.8.3.2 MAC Control frame format

Item	Feature	Subclause	Value/Comment	Status	Support
FF1	Length/Type field	31.4.1.3	2-octet field containing 88-08	M	Yes [ ]
FF2	MAC Control opcode	31.4.1.4	2-octet operation code	M	Yes [ ]
FF3	Number of opcodes	31.4.1.4	1	M	Yes [ ]
FF4	MAC Control parameters	31.4.1.5	MAC Control Parameter field as described	M	Yes [ ]

31.8.3.3 Opcode-independent MAC Control sublayer operation

Item	Feature	Subclause	Value/Comment	Status	Support
SD1	Generic MAC Control receive state diagram	31.5.3	Meets requirements of Figure 31–4	M	Yes [ ]
SD2	MAC Control frame action	31.3	Sink MAC Control frames	M	Yes [ ]

31.8.3.4 Control opcode assignments

Item	Feature	Subclause	Value/Comment	Status	Support
COA1	Opcode values and interpretations	31A	Reserved opcodes not used	M	Yes [ ]

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32. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2

NOTE—This PHY is not recommended for new installations. Since September 2003, maintenance changes are no longer being considered for this clause.

32.1 Overview

The 100BASE-T2 PHY is one of the 100BASE-T family of high-speed CSMA/CD network specifications. The 100BASE-T2 Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and baseband medium specifications are aimed at users who want 100 Mb/s performance over basic data grade Category 3 twisted-pair cabling systems. 100BASE-T2 signaling requires two pairs of Category 3 cabling, or cabling with better transfer characteristics than Category 3, installed according to ISO/IEC 11801, as specified in 32.7. This type of cabling, and the connectors used with it, are simple to install and reconfigure.

This clause defines the type 100BASE-T2 PCS, type 100BASE-T2 PMA sublayer, and type 100BASE-T2 Medium Dependent Interface (MDI). Together, the PCS and the PMA sublayer comprise a 100BASE-T2 Physical Layer (PHY). Control actions needed for correct PHY operations are specified by the 100BASE-T2 PHY Control function. Provided in this document are full functional, electrical, and mechanical specifications for the type 100BASE-T2 PHY Control function, PCS, PMA, and MDI. This clause also specifies the baseband medium used with 100BASE-T2.

The objectives of 100BASE-T2 are as follows:

a) To support the CSMA/CD MAC;

b) To support the 100BASE-T Media Independent Interface (MII), repeater, and Auto-Negotiation;

c) To support full duplex operations (Clause 31);

d) To provide 100 Mb/s data rate at the MII;

e) To provide for operating over two pairs of Category 3, 4, or 5 balanced twisted-pair cabling systems installed in accordance with ISO/IEC 11801, as specified in 32.7, at distances up to 100 m;

f) To support operation of other applications on adjacent pairs;

g) To allow for a nominal network extent of 200 m including

   1) Balanced cabling links of 100 m to support both half duplex and full duplex operation and

   2) Two-repeater networks of approximately 200 m span;

h) To provide a communication channel with a symbol error ratio of less than one part in 10^{10} at the PMA service interface.

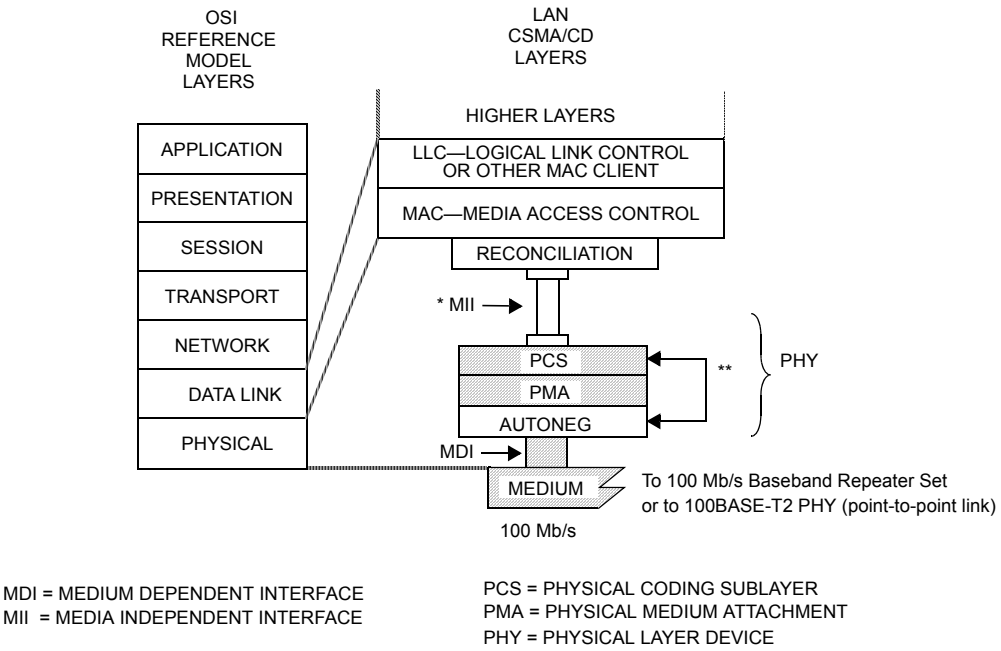
32.1.1 Relation of 100BASE-T2 to other standards

Relations between the 100BASE-T2 PHY and the ISO/IEC Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 32–1. The PHY layers shown in Figure 32–1 connect one Clause 4 Media Access Control (MAC) layer to a Clause 27 repeater. This clause also discusses other variations of the basic configuration shown in Figure 32–1. This whole clause builds on Clauses 1, 2, 3, 4, 21, 22, 27, 28, 29, and 30 of this standard.

32.1.2 Operation of 100BASE-T2

The 100BASE-T2 PHY employs dual-duplex baseband transmission over two wire pairs BI_DA and BI_DB, whereby the aggregate data rate of 100 Mb/s is achieved by transmission at a modulation rate of

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NOTE 1—* MII is optional.

NOTE 2—** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indication.

Figure 32–1—Type 100BASE-T2 PHY relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

25 MBd over each wire pair in each direction simultaneously (full duplex transmission), as shown in Figure 32–2. Transmitted symbols are selected from the two-dimensional 5 × 5 symbol constellation illustrated in Figure 32–3. Redundancy in the 5 × 5 constellation allows specific encoding rules to be employed to represent MII data streams, an idle mode or control signals as sequences of two-dimensional symbols. Each two-dimensional symbol can be viewed as a pair (A_n, B_n) of one-dimensional quinary symbols taken from the set {–2, –1, 0, +1, +2}. Five-level Pulse Amplitude Modulation is employed for transmission over each wire pair (PAM 5 × 5). The modulation rate of 25 MBd matches the MII clock rate of 25 MHz. The corresponding symbol period is 40 ns. This specification permits the use of Category 3, 4, or 5 balanced cabling, installed according to ISO/IEC 11801, as defined in 32.7.

A 100BASE-T2 PHY can be configured either as a *master* PHY or as a *slave* PHY. The master-slave relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 28, 32.5, Annex 28C, and 32.5.2). The master PHY uses an external clock to determine the timing of transmitter and receiver operations. The slave PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations, i.e., it performs loop timing, as illustrated in Figure 32–2. In a DTE to repeater connection, the repeater is typically set to be master and the DTE is typically set to be slave.

The following subclauses summarize the PCS, PMA, and PHY Control sections of this document. Figure 32–4 shows the division of responsibilities between the PCS, the PMA sublayer, and the PHY Control function.

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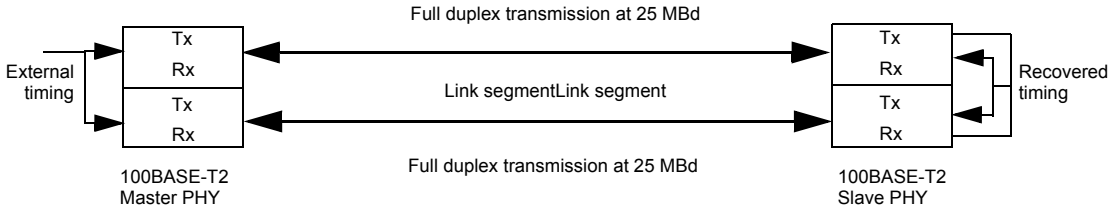


Figure 32–2—100BASE-T2 topology

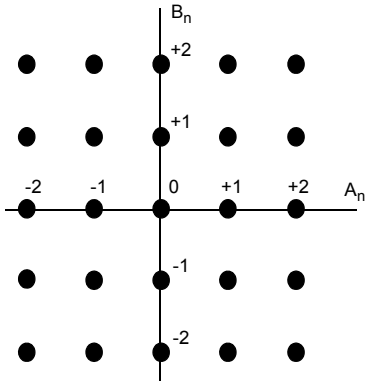


Figure 32–3—PAM5×5 symbol constellation

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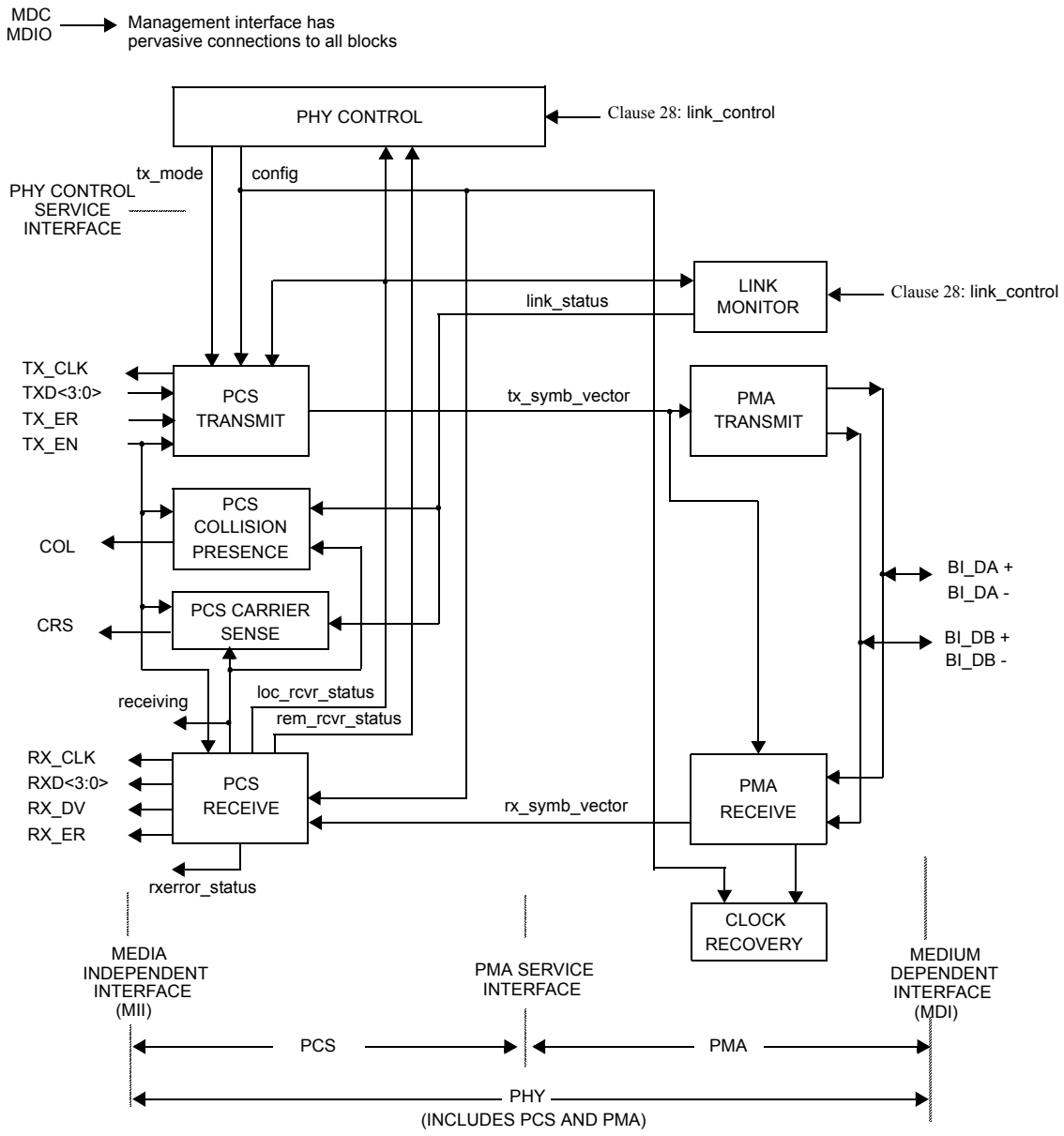


Figure 32–4—Division of responsibilities between 100BASE-T2 PCS, PMA, and PHY Control

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32.1.2.1 Physical coding sublayer (PCS)

The 100BASE-T2 PCS couples an MII, as described in Clause 22, to a PMA sublayer.

The functions performed by the PCS comprise the generation of continuous quinary symbol sequences to be transmitted over each wire pair. During *data mode*, i.e., when a data stream from the MII is transmitted, the four bits representing the TXD<3:0> data nibble are scrambled by a side-stream scrambler and encoded into a pair of quinary symbols. During *idle mode*, i.e., between transmission of consecutive data streams, the sequences of quinary symbols are generated with an encoding rule that differs from the encoding rule used in data mode. Through this technique, sequences of arbitrary quinary symbols that represent data can easily be distinguished from sequences that represent the idle mode. Furthermore, idle mode encoding takes into account the information of whether the local PHY is operating reliably or not and allows conveying this information to the remote station. A transition from the idle to the data mode is signaled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive pairs of quinary symbols. Similarly, the end of a data stream transmission is signaled by inserting an End-of-Stream delimiter that also consists of a pattern of two consecutive pairs of quinary symbols. Further patterns are reserved for signaling a transmit error during transmission of a data stream.

PCS Receive processes pairs of quinary symbols provided by the PMA. It detects the beginning and the end of streams of data and, during the reception of a data stream, descrambles and decodes the received quinary symbol pairs into nibbles RXD<3:0> that are passed to the MII. PCS Receive also detects errors in the received sequences and signals them to the MII. Furthermore, the PCS contains a PCS Carrier Sense function, a PCS Collision Presence function, and a management interface.

The PCS functions and state diagrams are specified in 32.3. The signals provided by the PCS at the MII conform to the interface requirements of Clause 22. The PCS interfaces to PHY Control and to the PMA are abstract message-passing interfaces specified in 32.2 and 32.4, respectively.

32.1.2.2 PMA sublayer

The PMA couples messages from the PMA service interface onto the balanced cabling physical medium. The PMA provides dual-duplex communications at 25 MBd over two pairs of balanced cabling up to 100 m in length.

The PMA Transmit function comprises two independent transmitters to generate five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB, as described in 32.4.1.1.2.

The PMA Receive function comprises two independent receivers for five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB, as described in 32.4.1.1.3. The receivers are responsible for acquiring clock, and providing quinary symbol pairs to the PCS as defined by the PMA_UNITDATA.indication message. The PMA also contains functions for Link Monitor.

PMA functions and state diagrams are specified in 32.4. PMA electrical specifications are given in 32.6.

32.1.2.3 PHY Control function

PCS and PMA sublayer operations are controlled via signals generated by the PHY Control function. PHY Control does not itself represent a sublayer but rather a logical grouping of the control functions necessary for proper operations of a 100BASE-T2 transceiver.

PHY Control determines whether the PHY should operate in a normal state, where packets can be exchanged over the link segment, or whether the PHY should be forced to send quinary symbol sequences that represent the idle mode. The latter occurs when either one of the PHYs, or both PHYs, that share a link segment are not operating reliably.

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The PHY Control function and state diagram are specified in 32.2, prior to introducing the PCS and PMA functional specifications. The PHY Control interface to the PCS and PMA sublayer is an abstract message-passing interface also specified in 32.2.

32.1.3 Application of 100BASE-T2

32.1.3.1 Compatibility considerations

All implementations of the balanced cabling link shall be compatible at the MDI. The PCS, PMA, and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided the MDI and MII specifications are met.

32.1.3.2 Incorporating the 100BASE-T2 PHY into a DTE

When the PHY is incorporated within the physical bounds of a DTE, conformance to the MII is optional, provided that the observable behavior of the resulting system is identical to that of a system with a full MII implementation. For example, an integrated PHY may incorporate an interface between PCS and MAC that is logically equivalent to the MII, but does not have the full output current drive capability called for in the MII specification.

32.1.3.3 Use of 100BASE-T2 PHY for point-to-point communication

The 100BASE-T2 PHY, in conjunction with the MAC specified in Clause 1 through Clause 4 (including parameterized values in 4.4.2 to support 100 Mb/s operation) may be used at both ends of a link for point-to-point applications between two DTEs. Such a configuration does not require a repeater. In this case each PHY may connect through an MII to its respective DTE. Optionally, either PHY (or both PHYs) may be incorporated into the DTEs without an exposed MII.

32.1.3.4 Auto-Negotiation requirement

Full Auto-Negotiation, as specified in Clause 28, shall be included in all compliant implementations.

32.1.4 State diagram conventions

The body of this clause and its associated annexes contain state diagrams, including definitions of variables, constants and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram shall prevail. The notation used in the state diagrams follows the conventions of 21.5.

32.2 PHY Control functional specifications and service interface

32.2.1 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY in a mode of operation during which packets can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 32–5.

During Auto-Negotiation, PHY Control ensures that the transmitter is disabled. When the Auto-Negotiation process asserts link_control=ENABLE, PHY Control enters the TRAINING state. During training, PHY Control enforces transmission in the idle mode by setting tx_mode=SEND_I and the PHY transmits sequences of quinary symbols encoded with the parameter loc_rcvr_status=NOT_OK. When the PHY achieves successful training and establishes proper receiver operations, PCS Receive asserts the parameter loc_rcvr_status=OK, and PCS Transmit conveys this information to the link partner via idle transmission.

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The criterion for assertion of the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver or detecting errors during reception of symbol streams that represent the idle mode. Upon observation that the remote PHY also operates reliably (rem_rcvr_status=OK), the normal mode of operation is entered where transmission of packets over the link segment can take place.

The normal mode of operation corresponds to the SEND IDLE OR DATA state, where PHY Control asserts tx_mode=SEND_N. In this state, when no packets have to be sent, idle mode transmission takes place. Encoding of quinary symbols is realized with the parameter loc_rcvr_status = OK.

If during the normal mode of operation unsatisfactory receiver operations is detected (loc_rcvr_status=NOT_OK), transmission of the current packet, if any, is completed and PHY Control enters the TRAINING state.

Whenever a PHY that operates reliably detects unsatisfactory operation of the remote PHY (rem_rcvr_status=NOT_OK), it enters the SEND IDLE state where tx_mode=SEND_I is asserted and idle transmission takes place. In this state, encoding is performed with the parameter loc_rcvr_status=OK. As soon as the remote PHY signals satisfactory receiver operation (rem_rcvr_status=OK), the SEND IDLE OR DATA state is entered. Note that if in the SEND IDLE state loc_rcvr_status takes the value NOT_OK transition to the TRAINING state occurs.

PHY Control may force the transmit scrambler state to be initialized to a random value by requesting the execution of the PCS Reset function defined in 32.3.1.1.

32.2.2 PHY Control Service interface

The following specifies the services provided by PHY Control. These services are described in an abstract manner and do not imply any particular implementation.

The following primitives are defined:

PHYC_CONFIG.indication
PHYC_TXMODE.indication
PHYC_RXSTATUS.request
PHYC_REMRXSTATUS.request

The parameter link_control is identical to the link_control parameter defined for the PMA Service interface in 32.4.2.4.

32.2.2.1 PHYC_CONFIG.indication

Each PHY in a 100BASE-T2 link is configured as a master PHY or as a slave PHY. Master/slave configuration is determined during Auto-Negotiation (see 32.5). The result of this negotiation is provided to PHY Control.

32.2.2.1.1 Semantics of the primitive

PHYC_CONFIG.indication (config)

PHYC_CONFIG.indication specifies to PCS and PMA Clock Recovery via the parameter config whether the PHY must operate as a master PHY or as a slave PHY. The parameter config can take on one of two values of the form:

MASTER This value is continuously asserted when the PHY must operate as a master PHY.

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SLAVE This value is continuously asserted when the PHY must operate as a slave PHY.

32.2.2.1.2 When generated

PHY Control shall generate PHYC_CONFIG.indication messages synchronously with every MII TX_CLK cycle.

32.2.2.1.3 Effect of receipt

Upon reception of this primitive, PCS and PMA Clock Recovery shall perform their functions in master or slave configuration according to the value assumed by the parameter config.

32.2.2.2 PHYC_TXMODE.indication

The transmitter in a 100BASE-T2 link normally sends over the two pairs quinary symbols that can represent an MII data stream or the idle mode.

32.2.2.2.1 Semantics of the primitive

PHYC_TXMODE.indication (tx_mode)

PHYC_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of quinary symbols the PCS should be transmitting. The parameter tx_mode can take on one of two values of the form:

SEND_N This value is continuously asserted when transmission of sequences of quinary symbols representing an MII data stream or the idle mode is to take place.

SEND_I This value is continuously asserted in case transmission of sequences of quinary symbols representing the idle mode is to take place.

32.2.2.2.2 When generated

PHY Control shall generate PHYC_TXMODE.indication messages synchronously with every MII TX_CLK cycle.

32.2.2.2.3 Effect of receipt

Upon receipt of this primitive, the PCS shall perform its Transmit function as described in 32.3.1.2.

32.2.2.3 PHYC_RXSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the receive link for the local PHY. The parameter loc_rcvr_status conveys to PHY Control and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by PCS Transmit encoding functions.

32.2.2.3.1 Semantics of the primitive

PHYC_RXSTATUS.request (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK This value is asserted and remains true during reliable operation of the receive link for

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the local PHY.

NOT_OK This value is asserted whenever operation of the receive link for the local PHY is unreliable.

32.2.2.3.2 When generated

PCS Receive shall generate PHYC_RXSTATUS.request messages synchronously with signals received at the MDI. It shall prevent that the value of the parameter loc_rcvr_status is modified while TX_EN=1 in order to avoid that a transition from data to idle mode or from idle to data mode occurs while a packet is being presented to the PCS at the MII.

32.2.2.3.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2.5 and 32.4.1.3.3.

32.2.2.4 PHYC_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link as communicated by the remote PHY. The parameter rem_rcvr_status conveys to PHY Control the information on whether reliable operation of the remote PHY is detected or not.

32.2.2.4.1 Semantics of the primitive

PHYC_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK The receive link for the remote PHY is operating reliably.

NOT_OK Reliable operation of the receive link for the remote PHY is not detected.

32.2.2.4.2 When generated

The PCS shall generate PHYC_REMRXSTATUS.request messages synchronously with signals received at the MDI.

32.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2.5.

32.2.3 State diagram variables

link_control
: See 32.4.1.3.1.

link_status
: See 32.4.1.3.1.

loc_rcvr_status
: Variable set by the PCS Receive function to indicate correct or incorrect operation of the receive link for the local PHY.

  Values: OK: the receive link for the local PHY is operating reliably,
  NOT_OK: operation of the receive link for the local PHY is not reliable.

pma_reset
: Allows reset of all PMA functions.

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Values: ON and OFF

Set by: PMA Reset

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

Values: OK: the receive link for the remote PHY is operating reliably,
NOT_OK: reliable operation of the receive link for the remote PHY is not detected.

tx_mode

PCS Transmit shall send quinary symbols according to the value assumed by this variable.

Values: SEND_N: transmission of sequences of quinary symbols representing an MII data stream, the idle mode, or control signals shall take place,
SEND_I: transmission of sequences of quinary symbols representing the idle mode shall take place.

32.2.4 State diagram timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

maxwait_timer

A timer used to measure the amount of time during which a receiver dwells in the TRAINING state. The timer shall expire 2500 ms to 3000 ms after entering the TRAINING state.

minwait_timer

A timer used to measure the amount of time during which a receiver waits in the SEND IDLE OR DATA, the TRAINING, or the SEND IDLE state before being allowed to leave the current state. The timer shall expire 128T = 5.12 μs after being started.

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32.2.5 PHY Control state diagram

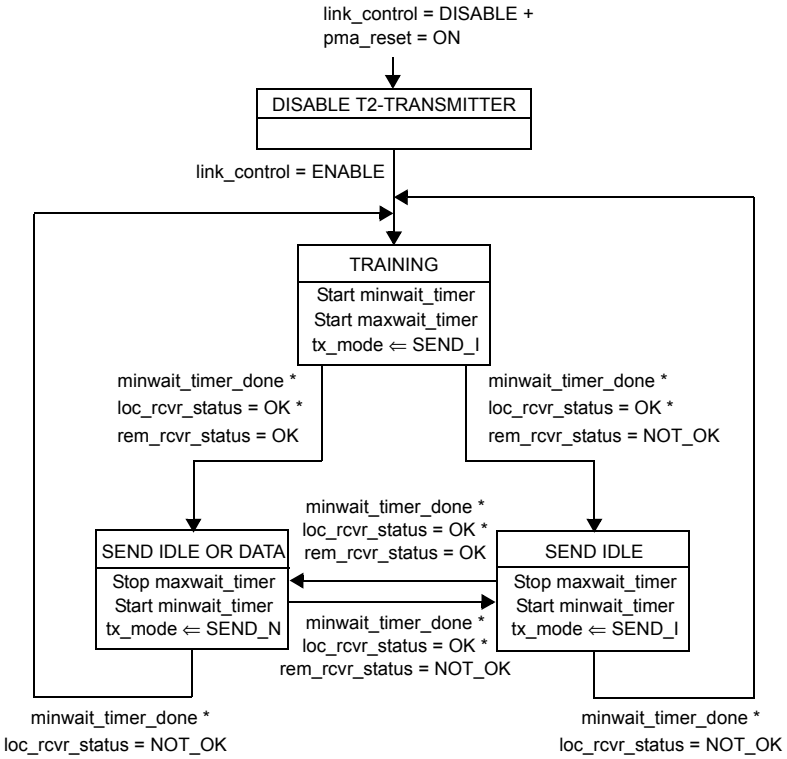


Figure 32–5—PHY Control state diagram

32.3 PCS functional specifications

The PCS comprises one PCS Reset function and four simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit, PCS Receive, PCS Carrier Sense, and PCS Collision Presence. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 32–5, shows how the four operating functions relate to the messages of the PCS-PMA and the PCS-PHY Control interfaces. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive, and are not shown in Figure 32–5. The management functions are specified in Clause 30. See also Figure 32–7, which presents a block diagram helpful for understanding the definitions of PCS Transmit function variables, and Figure 32–11, which defines the structure of frames passed from PCS to PMA.

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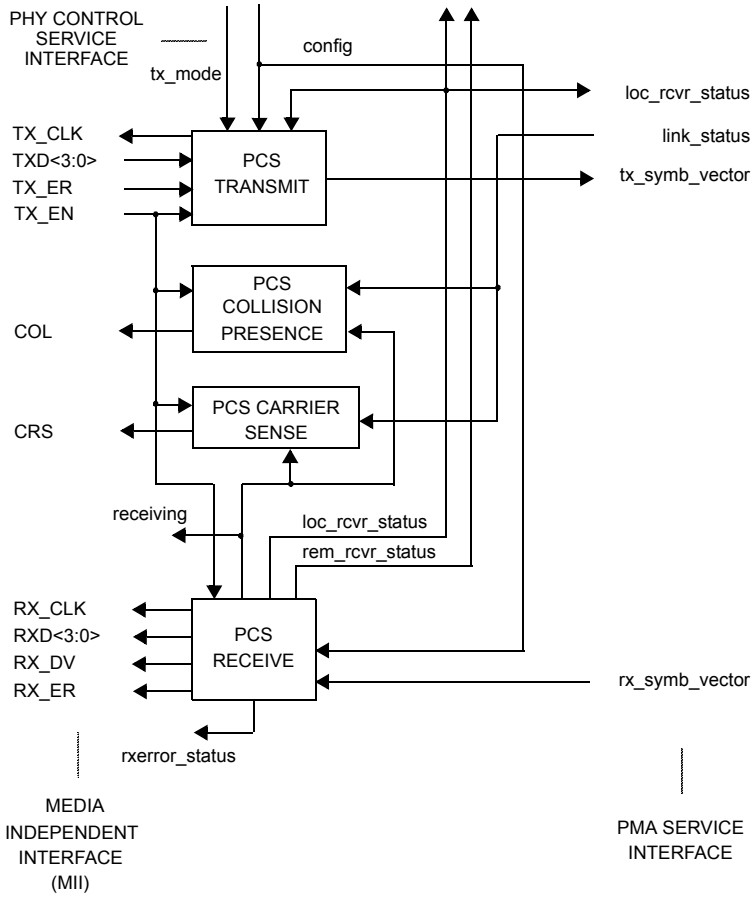


Figure 32-6—PCS reference diagram

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32.3.1 PCS functions

32.3.1.1 PCS Reset function

The PCS Reset function shall be executed any time one of three conditions occurs. These three conditions are "power on," the receipt of a request for reset from the management entity, and the receipt of a request for reset from PHY Control. PCS Reset initializes all PCS functions. PCS Reset sets pcs_reset = ON for the duration of its Reset function. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

32.3.1.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 32–12.

In normal mode of operation, the tx_mode parameter, which is transferred from PHY Control to the PCS via the PHYC_TXMODE.indication message, assumes the value tx_mode=SEND_N, and the PCS Transmit function generates at each symbol period pairs of quinary symbols that represent data or the idle mode. A symbol period T is equal to 40 ns. A time index n, where n is an integer, is introduced to establish a temporal relationship between different symbol periods. The tx_symb_vector parameter at time n is a two-element vector of quinary symbols (A_n, B_n) that is transferred to the PMA via PMA_UNITDATA.request. The PMA shall transmit symbols A_n and B_n over wire pairs BI_DA and BI_DB, respectively. During transmission of data, the four bits representing the TXD<3:0> data nibble are scrambled by the OCS using a side-stream scrambler then encoded into a pair of quinary symbols and transferred to the PMA. The idle mode is signaled by a sequence of pairs of quinary symbols that are also generated using the side-stream transmit scrambler. However, the encoding rules by which the quinary symbols are obtained are different for the data and the idle modes. This allows, at the receiver, sequences of quinary symbol pairs that represent data to be distinguished from sequences of quinary symbol pairs that represent the idle mode. A transition from the idle mode to the data mode is signalled by inserting a Start-of-Stream delimiter that consists of a pattern of two consecutive pairs of quinary symbols. Similarly, the end of transmission of data is signalled by an End-of-Stream delimiter that also consists of a pattern of two consecutive pairs of quinary symbols. Further patterns are reserved for signaling the assertion of TX_ER within a stream of data.

If tx_mode = SEND_I is asserted, PCS Transmit generates sequences of symbol pairs (A_n, B_n) according to the encoding rule in idle mode. Idle mode encoding takes into account the value of the parameter loc_rcvr_status. By this mechanism, a PHY indicates during idle transmission the status of its own receiver to the link partner.

The PCS Transmit reference diagram is shown in Figure 32–7. PCS encoding involves the generation of the three-bit words Sa_n[2:0], Sb_n[2:0], Ta_n[2:0], and Tb_n[2:0], from which the pairs of quinary symbols (A_n, B_n) are obtained. The three-bit words Sa_n[2:0] and Sb_n[2:0] are determined first, as explained in 32.3.1.2.2, from sequences of random binary symbols derived from the transmit side-stream scrambler. The generation of Ta_n[2:0] and Tb_n[2:0] and the quinary symbols A_n and B_n is given in 32.3.1.2.3. The physical structure represented in Figure 32–7 is not required. Implementers are free to construct any logical devices having functionality identical to that described by the following specifications and the PCS Transmit state diagram.

32.3.1.2.1 Side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PHY Control function via the PHYC_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ

$$g_M(x) = 1 + x^{13} + x^{33}$$

as transmitter side-stream scrambler generator polynomial. If config = SLAVE, PCS Transmit shall employ

$$g_S(x) = 1 + x^{20} + x^{33}$$

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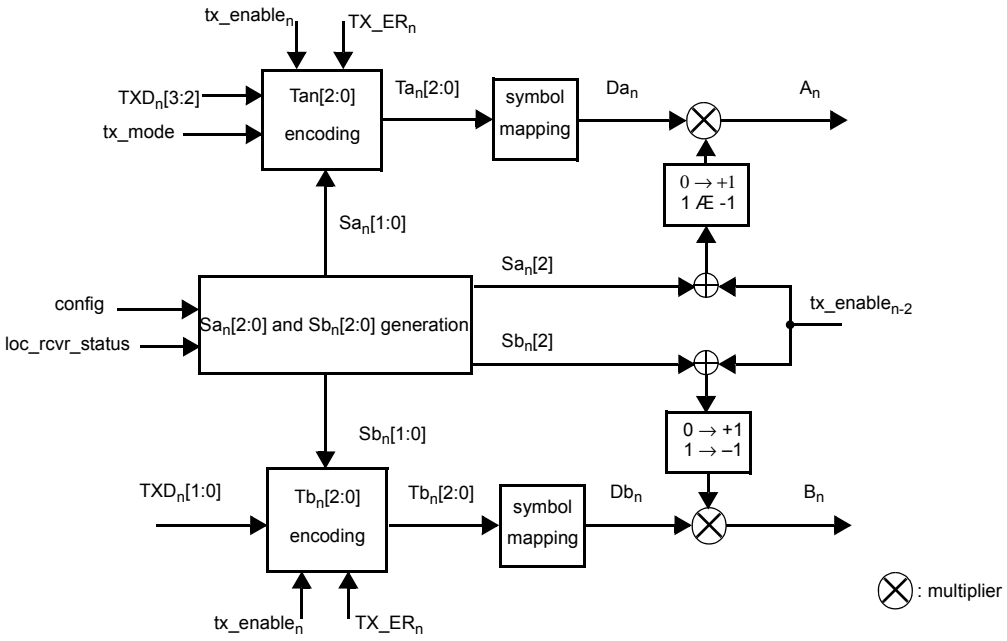
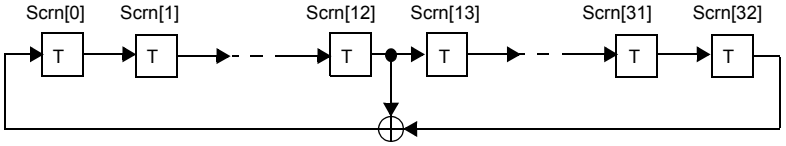
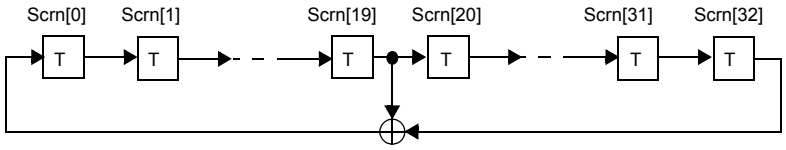


Figure 32–7—PCS Transmit reference diagram

as transmitter side-stream scrambler generator polynomial. The implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 32–8. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are randomly set. The generation of the random bits is left to the implementer.



a) Side-stream scrambler employed by the master PHY



b) Side-stream scrambler employed by the slave PHY

Figure 32–8—Realization of side-stream scramblers by linear feedback shift registers

32.3.1.2.2 Generation of bits $Sa_n[2:0]$ and $Sb_n[2:0]$

PCS Transmit encoding rules are based on the generation, at time n, of the four bits Sx_n, Sy_n, $Sa_n[2]$, and $Sb_n[2]$. These four bits are mutually uncorrelated and also uncorrelated with the bit $Scr_n[0]$ in data and idle

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modes. For both master and slave PHYs, they are obtained by the same linear combinations of bits stored in the transmit scrambler shift register delay line. The four bits are elements of the same maximum-length shift register sequence of length $2^{33} - 1$ as $Scr_n[0]$, but shifted in time. The associated delays are all large and different, such that there is no apparent correlation among the five bits $Scr_n[0]$, Sx_n, Sy_n, $Sa_n[2]$, and $Sb_n[2]$. The bits Sx_n and Sy_n are given by

$$Sx_n = Scr_n[3] \oplus Scr_n[8]$$

$$Sy_n = Scr_n[4] \oplus Scr_n[6]$$

where $\oplus$ denotes the XOR logic operator. Four bits $X_n[1:0]$ and $Y_n[1:0]$ are obtained by

$$X_n[0] = \begin{cases} Sx_n & \text{if } \{n - n_0 = 0 \text{ (mod 2) or loc\_rcvr\_status = OK }\} \\ Sx_n \oplus 1 & \text{else} \end{cases}$$

$$X_n[1] = X_n[0] \oplus 1$$

$$Y_n[0] = \begin{cases} Sy_n & \text{if } n - n_0 = 0 \text{ (mod 2)} \\ Sy_{n-1} \oplus 1 & \text{else} \end{cases}$$

$$Y_n[1] = Y_n[0]$$

where n_0 denotes the time index of the last transmitter side-stream scrambler reset.

The bits San[2:0] and Sbn[2:0] are given by

$$Sa_n[2] = Scr_n[1] \oplus Scr_n[5]$$

$$Sa_n[1:0] = \begin{cases} X_n[1:0] & \text{if } Scr_n[0] = 1 \\ Y_n[1:0] & \text{else} \end{cases}$$

$$Sb_n[2] = Scr_n[2] \oplus Scr_n[12]$$

$$Sb_n[1:0] = \begin{cases} Y_n[1:0] & \text{if } Scr_n[0] = 1 \\ X_n[1:0] & \text{else} \end{cases}$$

32.3.1.2.3 Generation of sequences A_n and B_n

If tx_mode = SEND_N, the PCS Transmit function generates sequences A_n and B_n that represent either a stream of data or an idle mode. If tx_mode = SEND_I, idle transmission is enforced. The encoding rule is determined by the value of the signal tx_enable_n, given by

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$$\text{tx\_enable}_n = \begin{cases} TX\_EN_n & \text{if tx\_mode = SEND\_N} \\ 0 & \text{else} \end{cases}$$

where TX_EN_n represents the MII signal TX_EN at time n. If $tx\_enable_n = 1$, transmission of a stream of data takes place. As illustrated in Figure 32–11, the definition of a Start-of-Stream Delimiter ("SSD") is related to the condition $SSD_n = (tx\_enable_n) * (! tx\_enable_{n-2}) = 1$, where "*" and "!" denote the logic AND and NOT operators, respectively. For the generation of "SSD", PCS Transmit replaces the first two nibbles of the preamble in a data stream with the symbols defined below. Similarly, the definition of an End-of-Stream Delimiter (ESD) is related to the condition $ESD_n = (! tx\_enable) * (tn\_enable_{n-2}) = 1$. This occurs during the first two symbol periods after transmission of the last nibble of a data stream.

The symbols A_n and B_n are obtained from the three-bit words $Ta_n[2:0]$ and $Tb_n[2:0]$ whose definitions in the data and the idle modes are given below.

Data mode (tx_enable_n=1):

Definition of "SSD":

$Ta_n[2:0] = [1, 0, 0]$

$Tb_n[2:0] = [!tx\_enable_{n-1}, tx\_enable_{n-2}, tx\_enable_{n-2}]$

A most significant bit $Ta_n[2]=1$ or $Tb_n[2]=1$ results in the transmission of a symbol that can be interpreted as an ESC symbol.

Encoding of data nibbles:

$$Ta_n[2:0] = [0,(Sa_n[1] \oplus TXD_n[3]),(Sa_n[0] \oplus TXD_n[2] \oplus 1)]$$

$$Tb_n[2:0] = [0, (Sb_n[1] \oplus TXD_n[1]),(Sb_n[0] \oplus TXD_n[0] \oplus 1)]$$

where $TXD_n[3:0]$ denotes the data nibble TXD[3:0] at time n.

Encoding of error indication:

If $TX\_ER_n=1$ is asserted, where TX_ER_n denotes the value of the signal TX_ER at time n, error indication is signaled by means of the ESC and 0 symbols. The encoding rule is given by

$$Ta_n[2:0] = [(Sa_n[1] \oplus Sa_n[0]),0,0]$$

$$Tb_n[2:0] = [(Sb_n[1] \oplus Sb_n[0]),0,0]$$

Idle mode (tx_enable_n=0):

Definition of "ESD":

$Ta_n[2:0] = [1, 0, 0]$

$Tb_n[2:0] = [tx\_enable_{n-1}, !tx\_enable_{n-2}, !tx\_enable_{n-2}]$

Encoding in the idle mode:

$$Ta_n[2:0] = [0,Sa_n[1],Sa_n[0]]$$

$$Tb_n[2:0] = [0,Sb_n[1],Sb_n[0]]$$

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The mapping of $Ta_n[2:0]$ and $Tb_n[2:0]$ into quinary symbols Da_n and Db_n is given in Figure 32–9. This mapping ensures that the symbols representing data are Gray coded. The quinary symbols A_n and B_n are obtained from Da_n and Db_n by

Symbol mapping	
Ta/Tb	Da/Db
000	0
001	+1
010	-1
011	-2
100 (ESC)	+2

Idle or data	
Da_n:	0, +1, -1, or -2
Db_n:	0, +1, -1, or -2

Data stream delimiters	
Da_n: ESC	Dan+1: ESC
Db_n: ESC	Dbn+1: 0

Error indication	
Da_n: ESC	Da_n: 0
or	
Db_n: 0	Db_n: ESC

Figure 32–9—Symbol mapping and encoding rule summary

$$A_n = \begin{cases} Da_n & \text{if } \text{Sa}_n[2] \oplus \text{tx\_enable}_{n-2} = 0 \\ -Da_n & \text{else} \end{cases}$$

$$B_n = \begin{cases} Db_n & \text{if } \text{Sb}_n[2] \oplus \text{tx\_enable}_{n-2} = 0 \\ -Db_n & \text{else} \end{cases}$$

With the rules defined in this subclause, if in idle mode a transmitted symbol on one wire pair belongs to the set {–2,0,+2}, the symbol on the other wire pair belongs to the set {–1,+1}. Moreover, one of the quinary symbols that are transmitted at time $2(n–n_0)$ and $2(n–n_0)+1$ is guaranteed to be either +2 or –2. Both in data and idle modes, the symbol sequences on each wire pair can be modeled as sequences of independent and identically distributed quinary symbols. The symbol constellations and symbol probabilities for these two modes are shown in Figure 32–10. The average symbol energy is the same in data and idle modes.

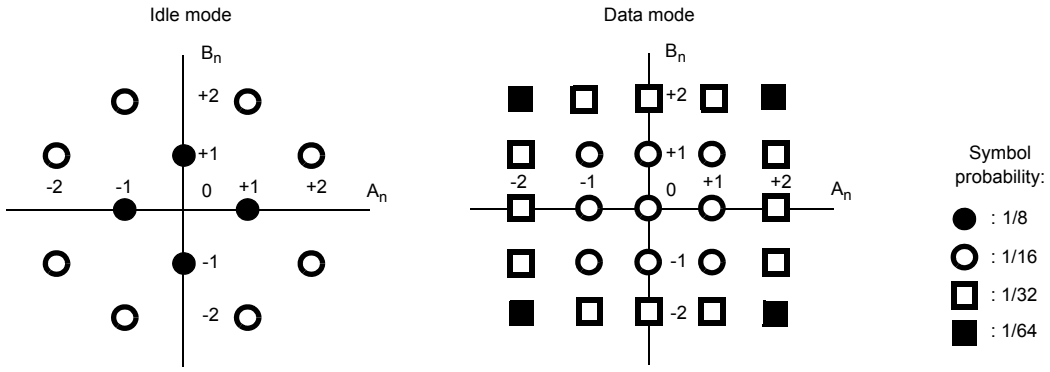


Figure 32–10—Symbol constellations in idle and data modes

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32.3.1.3 PCS Receive function

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 32–13.

The PCS Receive function accepts pairs of detected quinary symbols provided by the PMA Receive function via the parameter rx_symb_vector. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. For example, the property that in the idle mode if A_n belongs to the set {–2,0,+2} then B_n belongs to the set {–1,+1}, and vice versa, can be used to acquire the correct state for the receiver side-stream descrambler, and to determine which detected quinary symbol was transmitted on wire pair BI_DA and which on wire pair BI_DB. Also, correct polarity of the detected quinary symbols can reliably be obtained by ensuring in the idle mode that the encoding rule holds whenever a –2 symbol is received. PCS Receive generates the sequence of vectors of two quinary symbols (RA_n, RB_n) and indicates the reliability of receiver operations by setting the parameter loc_rcvr_status to OK (logic high) or NOT_OK (logic low). The sequence (RA_n, RB_n) is processed to generate the signals RXD<3:0>, RX_DV, and RX_ER, which are presented to the MII. PCS Receive detects the transmission of a stream of data from the remote station and conveys this information to the PCS Carrier Sense and PCS Collision Presence functions via the parameter receiving.

32.3.1.3.1 Receiver descrambler polynomials

For side-stream descrambling, the master PHY shall employ the receiver descrambler generator polynomial $g'_M(x) = 1 + x^{20} + x^{33}$, and the slave PHY shall employ the receiver descrambler generator polynomial $g'_S(x) = 1 + x^{13} + x^{33}$.

32.3.1.3.2 Decoding of quinary symbols

At the beginning of a stream of data, PCS Receive detects “SSD” and asserts the signal RX_DV. Detection of “SSD” is achieved by processing two consecutive vectors ($RA_{n–1}$, $RB_{n–1}$) and (RA_n, RB_n) at each time n. Upon detection of “SSD,” PCS Receive also assigns the value TRUE to the parameter receiving that is provided to the PCS Carrier Sense and Collision Presence functions.

Table 32–1 shows the mapping of symbols RA_n and RB_n into two-bit words Qa_n[1:0] and Qb_n[1:0] that are descrambled and decoded to generate nibbles of data RXD[3:0].

Table 32–1—Inverse quinary symbol mapping

RA_n/RB_n	$Qa_n[1:0]/Qb_n[1:0]$
0	00
+1	01 or 10
–1	01 or 10
± 2	11

The mapping shown in Table 32–1 corresponds to the inverse of the encoding function employed by PCS Transmit. For example, a symbol $A_n = +1$ is generated by Ta_n[1:0] being equal to “01” or “10.” Hence, in the above table the value of Qa_n[1:0] for $RA_n = +1$ is specified as being equal to “01 or 10.” Similarly for other entries in the table.

During reception of a stream of data, PCS Receive checks that the symbols RA_n and RB_n follow the encoding rule defined in 32.3.1.2 whenever they assume values ± 2. PCS Receive processes two consecutive vectors at each time n to detect “ESD.” Upon detection of “ESD,” PCS Receive deasserts the signal RX_DV, and assigns the value FALSE to the parameter receiving. If a violation of the encoding rules is detected, PCS

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Receive asserts the signal RX_ER for at least one symbol period. During reception of an idle sequence, PCS Receive checks that the symbols RA_n and RB_n follow the encoding rule defined in 32.3.1.2.

32.3.1.4 PCS Carrier Sense function

The PCS Carrier Sense function shall conform to the PCS Carrier Sense state diagram in Figure 32–14.

The PCS Carrier Sense function controls the MII signal CRS according to the rules presented in this clause. While link_status = OK, CRS is asserted whenever receiving=TRUE or TX_EN=1.

32.3.1.5 PCS Collision Presence function

A PCS collision is defined as the simultaneous occurrence of TX_EN=1 and the assertion of the parameter receiving=TRUE while link_status=OK. While a PCS collision is detected, the MII signal COL shall be asserted. At other times COL shall remain deasserted.

32.3.2 PCS interfaces

32.3.2.1 PCS–MII interface signals

The signals in Table 32–2 are formally defined in 22.2.2. Jabber detection as specified in 22.2.4.2.12 is not required by this standard.

Table 32–2—MII interface signals

Signal name	Meaning	Subclause
TX_CLK	Transmit clock	22.2.2.1
RX_CLK	Receive clock	22.2.2.2
TX_EN	Frames transmit data	22.2.2.3
TXD<3:0>	Transmit data	22.2.2.4
TX_ER	Forces transmission of illegal code	22.2.2.5
RX_DV	Frames receive SFD and DATA	22.2.2.7
RXD<3:0>	Receive data	22.2.2.8
RX_ER	Receive error indication	22.2.2.10
CRS	Non-idle medium indication	22.2.2.11
COL	Collision indication	22.2.2.12
MDC	Management data clock	22.2.2.13
MDIO	Management data	22.2.2.14

32.3.2.2 PCS–management entity signals

The management interface has pervasive connections to all functions. Operation of the management control lines MDC and MDIO, and requirements for managed objects inside the PCS and PMA, are specified in Clause 22 and Clause 30, respectively.

No spurious signals shall be emitted onto the MDI when the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when external power is first applied to the PHY.

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32.3.3 Frame structure

Frames passed from the PCS to the PMA sublayer shall have the structure shown in Figure 32–11. This figure shows the temporal relationship between the signals tx_enable$_n$, and TXD[3:0] and the sequences of quinary symbol pairs (A_n, B_n) in correspondence of transitions from the idle mode to transmission of data and vice versa. Time proceeds from left to right in the figure.

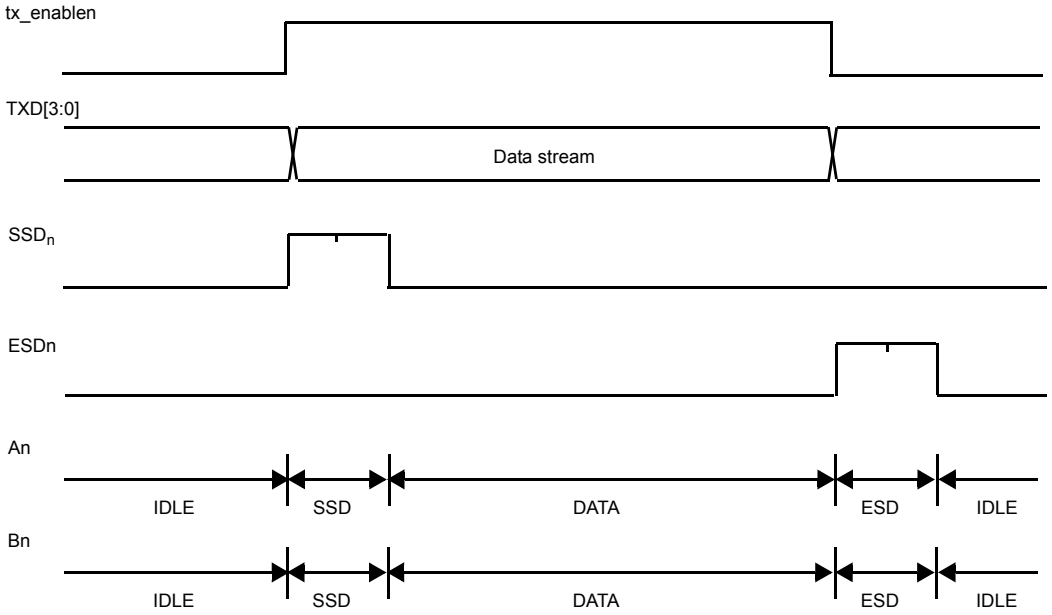


Figure 32–11—PCS sublayer to PMA sublayer frame structure

32.3.4 State variables

32.3.4.1 Variables

COL

The COL signal of the MII as specified in Clause 22.

config

The config parameter set by PHY Control and passed to the PCS via the PHYC_CONFIG.indication primitive.
Values: MASTER and SLAVE.

CRS

The CRS signal of the MII as specified in Clause 22.

DATA

A sequence of vectors of two quinary symbols corresponding to valid data, as specified in 32.3.1.2.

ESD

Two consecutive vectors of two quinary symbols corresponding to the End-of-Stream delimiter, as specified in 32.3.1.2.

IDLE

A sequence of vectors of two quinary symbols generated in idle mode, as specified in 32.3.1.2.

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link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK, READY, and FAIL

loc_rcvr_status

The loc_rcvr_status parameter generated by PCS Receive.
Values: OK and NOT_OK

pcs_reset

The pcs_reset parameter set by the PCS Reset function.
Values: ON and OFF

(RA_n, RB_n)

The vector of the two correctly aligned most recently received quinary symbols generated by PCS Receive.

receiving

The receiving parameter generated by the PCS Receive function.
Values: TRUE and FALSE

rxerror_status

The rxerror_status parameter set by the PCS Receive function. Although this variable is set by PCS Receive, it achieves the same function as the variable rxerror_status of Clause 24 that is set by PMA and communicated through the PMA_RXERROR.indication primitive.
Values: ERROR and NO_ERROR

RX_DV

The RX_DV signal of the MII as specified in Clause 22.

RX_ER

The RX_ER signal of the MII as specified in Clause 22.

rx_symb_vector

A vector of two quinary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: SYMB_PAIR

RXD[3:0]

The RXD<3:0> signal of the MII as specified in Clause 22.

SSD

Two consecutive vectors of two quinary symbols corresponding to the Start-of-Stream delimiter, as specified in 32.3.1.2.

tx_enable

The tx_enable parameter generated by PCS Transmit as specified in 32.3.1.2.3.

TX_ER

The TX_ER signal of the MII as specified in Clause 22.

tx_mode

The tx_mode parameter set by PHY Control and passed to the PCS via the

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PHYC_TXMODE.indication primitive.
Values: SEND_N and SEND_I

tx_symb_vector

A vector of two quinary symbols generated by the PCS Transmit function and passed to the PMA via the PMA_UNITDATA.request primitive.
Value: SYMB_PAIR

32.3.4.2 Timer

symb_timer

A continuous free-running timer. The condition symb_timer_done becomes true upon timer expiration.

Restart time: Immediately after expiration; timer restart resets the condition symb_timer_done.

Duration: 40 ns nominal.

TX_CLK shall be generated synchronously with symb_timer (see tolerance required for TX_CLK in 32.6.1.2.6). In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done.

32.3.4.3 Messages

PMA_UNITDATA.indication (rx_symb_vector)
A signal sent by PMA Receive indicating that a vector of two quinary symbols is available in rx_symb_vector.

PMA_UNITDATA.request (tx_symb_vector)
A signal sent to PMA Transmit indicating that a vector of two quinary symbols is available in tx_symb_vector.

32.3.5 State diagrams

32.3.5.1 PCS Transmit

PCS Transmit sends vectors of two quinary symbols to the PMA via the tx_symb_vector parameter. In normal mode of operation, between streams indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes an “SSD” of two consecutive vectors of two quinary symbols to the PMA replacing the preamble bits of a stream of data during these two symbol periods. Following the “SSD,” each TXD<3:0> nibble is encoded into a vector of two quinary symbols until tx_enable is deasserted. If, while tx_enable is asserted, the TX_ER signal is also asserted, PCS Transmit passes to the PMA vectors indicating a transmit error. Note that if the signal TX_ER is asserted while “SSD” is being sent, the transmission of the error condition is delayed until transmission of “SSD” has been completed. Following the deassertion of tx_enable, an “ESD” of two consecutive vectors of two quinary symbols is generated, after which the transmission of a sequence indicating the idle mode is resumed.

Collision detection is implemented by noting the occurrence of carrier receptions during transmissions, following the model of 10BASE-T. The PCS shall implement the Transmit process as depicted in Figure 32–12 including compliance with the associated state variables as specified in 32.3.4.

32.3.5.2 PCS Receive

PCS Receive accepts vectors of two quinary symbols from the PMA via the rx_symb_vector parameter. After correct receiver operation has been achieved, the loc_rcvr_status parameter assumes the value OK, and PCS

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Receive continuously checks that the received sequence satisfies the encoding rule used in idle mode. As soon as a violation is detected, PCS Receive asserts the parameter receiving and determines whether the violation is due to reception of "SSD" or to a receiver error by examining the last two received vectors (RA_{n-1}, RB_{n-1}) and (RA_n, RB_n). In the first case, during the two symbol periods corresponding to "SSD," PCS Receive replaces "SSD" by preamble bits. Following "SSD," the signal RX_DV is asserted and each received vector is decoded into a data nibble RXD<3:0> until "ESD" is detected. Deassertion of RX_DV and transition to the IDLE state take place upon detection of "ESD". The signal RX_ER is asserted if a receiver error occurs before proper stream termination. In the second case, the signal RX_ER is asserted and the parameter rxerror_status assumes the value ERROR. Deassertion of RX_DV and transition to the IDLE state (rxerror_status=NO_ERROR) takes place upon detection of a sequence generated in idle mode.

A premature stream termination is caused by the detection of four consecutive vectors satisfying the encoding rule used in idle mode prior to the detection of "ESD", provided that the first vector is not a valid data vector. Note that RX_DV remains asserted during the symbol periods corresponding to the first three idle vectors, while RX_ER=TRUE is signaled on the MII. The signal RX_ER is also asserted in the LINK FAILED state, which ensures that RX_ER remains asserted for at least one symbol period. The PCS shall implement the Receive process as depicted in Figure 32–13 including compliance with the associated state variables as specified in 32.3.4.

The parameters receiving and rxerror_status are communicated to the PCS's clients by the following primitives:

PCS_CARRIER.indication (carrier_status)
: A signal generated by PCS Receive to indicate reception of non-idle quinary symbols. The purpose of this primitive is to give clients indication of activity on the underlying continuous-signaling channel.

PCS_RXERROR.indication (rxerror_status)
: A signal generated by PCS Receive to indicate a reception of non-idle symbols that does not start with "SSD."

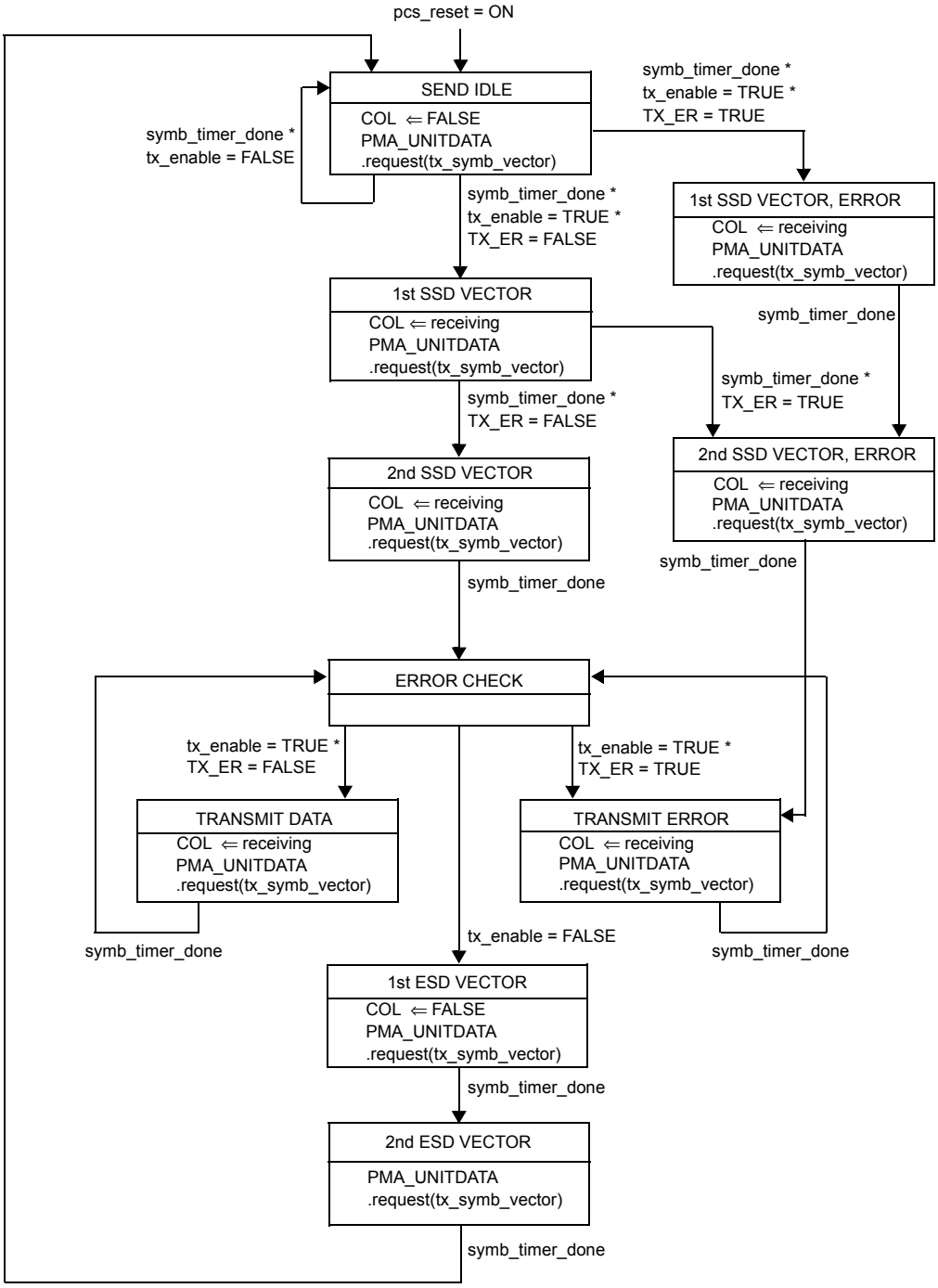
32.3.5.3 PCS Carrier Sense

The PCS Carrier Sense process generates the signal CRS on the MII, which the MAC uses via the Reconciliation sublayer for frame receptions and for deferral. The process operates by performing logical operations on TX_EN and receiving. The PCS shall implement the Carrier Sense process as depicted in Figure 32–14 including compliance with the associated state variables as specified in 32.3.4.

32.3.6 PCS electrical specifications

The interface between PCS, PMA and PHY Control is an abstract message-passing interface, having no specified electrical properties. Electrical characteristics of the signals passing between the PCS and MII may be found in Clause 22.

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NOTE—The generation of PMA_UNITDATA.request(tx_symb_vector) depends on the parameters config, tx_mode, and loc_rcvr_status as defined in 32.3.1.2 and is not shown explicitly in the state diagram.

Figure 32–12—PCS Transmit state diagram

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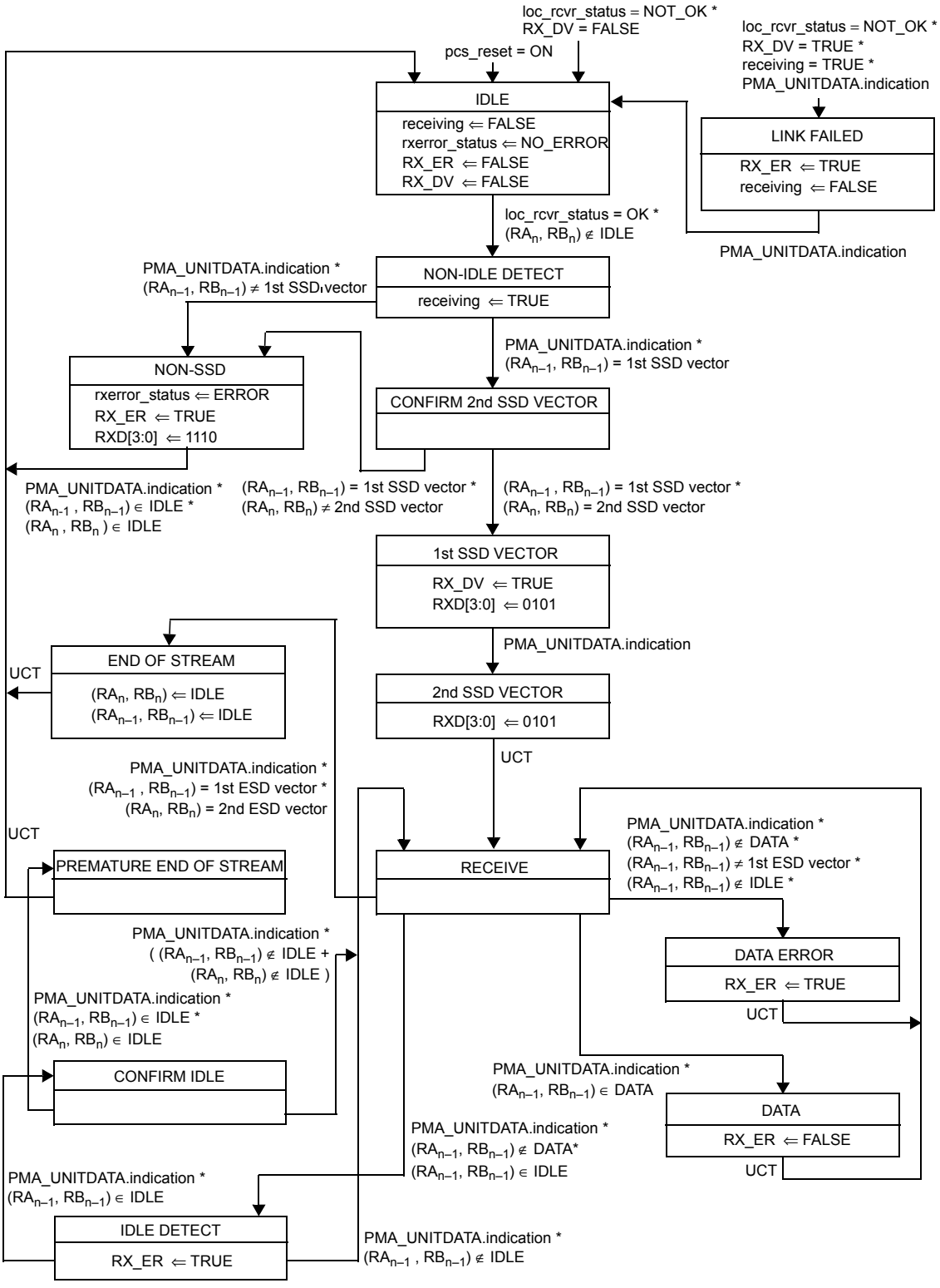


Figure 32–13—PCS Receive state diagram

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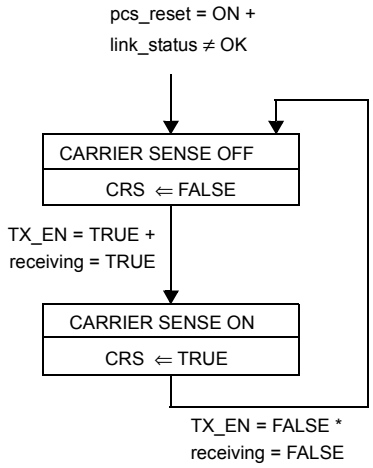


Figure 32–14—PCS Carrier Sense state diagram

32.4 PMA functional specifications and service interface

32.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 32.4.2 to the 100BASE-T2 baseband medium, specified in 32.7. The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), specified in 32.8.

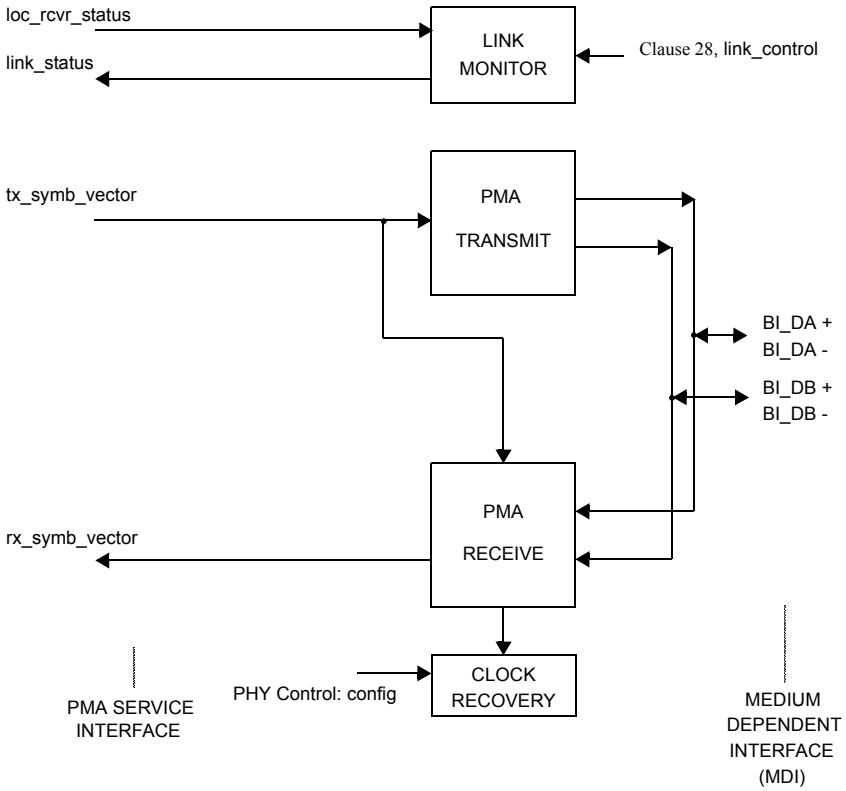


Figure 32–15—PMA reference diagram

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32.4.1.1 PMA functions

The PMA sublayer comprises one PMA Reset function and four simultaneous and asynchronous operating functions. The PMA operating functions are PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function. The Reset function may be shared between PMA and PCS sublayers.

The PMA reference diagram, Figure 32–15, shows how the operating functions relate to the messages of the PMA Service interface, PHY Control Service interface, and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive, and are not shown in Figure 32–15. The management interface and its functions are specified in Clause 22.

32.4.1.1.1 PMA Reset function

The PMA Reset function shall be executed any time either of two conditions occurs. These two conditions are "power on" and the receipt of a reset request from the management entity. The PMA Reset function initializes all PMA functions and forces Auto-Negotiation to be executed. The PMA Reset function sets pma_reset = ON for the duration of its reset function. All state diagrams take the open ended pma_reset branch upon execution of the PMA Reset function. The reference diagrams do not explicitly show the PMA Reset function.

32.4.1.1.2 PMA Transmit function

The PMA Transmit function comprises two independent transmitters to generate five-level pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB], respectively. The two transmitters shall be driven by the same transmit clock. The signals generated by PMA Transmit will follow the mathematical description given in 32.4.1.2.1, and shall comply with the electrical specifications given in 32.6.

32.4.1.1.3 PMA Receive function

The PMA Receive function comprises two independent receivers for quinary pulse-amplitude modulated signals on each of the two pairs BI_DA and BI_DB. PMA Receive contains the circuits necessary to detect quinary symbol sequences from the signals received at the MDI over receive pairs BI_DA and BI_DB and present these sequences to the PCS Receive function. The signals received at the MDI are described mathematically in 32.4.1.2.2. The PHY shall translate the signals received on pairs BI_DA and BI_DB into the PMA_UNITDATA.indication parameter rx_symb_vector with a symbol error ratio of less than one part in 10^{10}.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization, suppression of cyclo-stationary interference signals created by alien near-end crosstalk sources, and echo and self near-end crosstalk cancellation. The sequence of quinary transmitted symbols tx_symb_vector is needed to perform echo and self near-end crosstalk cancellation.

32.4.1.1.4 Link Monitor function

Link Monitor determines the status of the underlying receive channel. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Auto-Negotiation process notifies Link Monitor whether the device connected to the far end is of type 100BASE-T2. Based on this and other information, Link Monitor sets two important internal variables:

a) The pma_type variable that indicates whether the remote station is of type 100BASE-T2 or not,
b) The link_status variable that is sent across the PMA Service interface.

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The Link Monitor function shall comply with the state diagram of Figure 32-16.

Upon power-on, reset, or release from power-down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and sends during this period fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 100BASE-T2 station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

32.4.1.1.5 Clock Recovery function

The Clock Recovery function couples to both receive pairs. It provides a synchronous clock for sampling the signals on the two pairs.

The Clock Recovery function shall provide a clock suitable for synchronous signal sampling on each line so that the symbol error ratio indicated in 32.4.1.1.3 is achieved. The received clock signal must be stable and ready for use when training has been completed (loc_rcvr_status=OK).

32.4.1.2 PMA interface messages

The messages between the PMA, PCS, and PHY Control are defined in 32.4.2, PMA Service Interface. Communication through the MDI is summarized below.

32.4.1.2.1 MDI signals transmitted by the PHY

The quinary symbols to be transmitted by the PMA on the two pairs BI_DA and BI_DB are denoted by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB], respectively. Five-level Pulse Amplitude Modulation over each pair (PAM5×5) is the modulation scheme employed in 100BASE-T2. It is the function of PMA Transmit to generate on each pair a pulse-amplitude modulated signal of the form

$$s(t) = \sum_k a_k h_1(t - kT)$$

where a_k represents the quinary symbol from the set {–2, –1, 0, +1, +2} to be transmitted at time kT, and $h_1(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 32.6.

32.4.1.2.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise:

$$r(t) = \sum_k a_k h_2(t - kT) + w(t)$$

In this equation, $h_2(t)$ denotes the impulse response of the overall channel from the transmit side up to the MDI at the receive side, and $w(t)$ is a term that includes the contribution of various noise sources. The two signals received on pair BI_DA and BI_DB shall be processed within the PMA Receive function to yield the quinary received symbols rx_symb_vector[BI_DA] and rx_symb_vector[BI_DB].

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32.4.1.3 PMA state diagram

32.4.1.3.1 State diagram variables

link_control
: The link_control parameter as communicated by the PMA_LINK.request primitive.
Values: See 32.4.2.4.

link_status
: The link_status parameter as communicated by the Link Monitor function through the PMA_LINK.indication primitive.
Values: See 32.4.2.5.

loc_rcvr_status
: The loc_rcvr_status parameter as communicated by the PMA_RXSTATUS.request primitive.
Values: See 32.2.2.3.1.

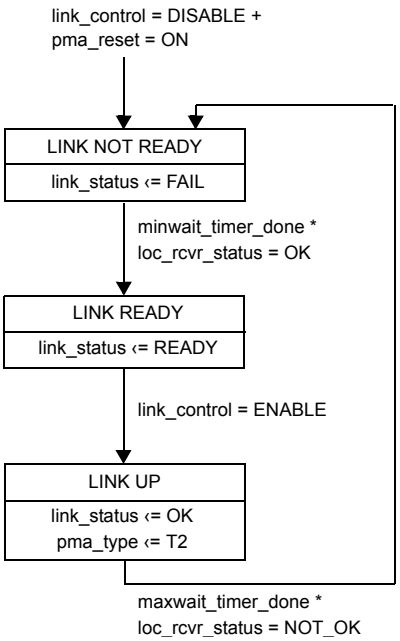
pma_reset
: Allows reset of all PMA functions.
Values: ON and OFF
Set by: PMA Reset

32.4.1.3.2 Timers

maxwait_timer
: Values: See 32.2.4.

minwait_timer
: Values: See 32.2.4.

32.4.1.3.3 Link Monitor state diagram



NOTE—The variables link_control and link_status are designated as link_control_[T2] and link_status_[T2], respectively, by the Auto-Negotiation Arbitration state diagram (Figure 28–18).

Figure 32-16—Link Monitor state diagram

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32.4.2 PMA service interface

This subclause specifies the services provided by the PMA. These services are described in an abstract manner and do not imply any particular implementation. The PMA Service Interface supports the exchange of symbol vectors, status indications, and control signals between the PMA, the PCS, and PHY Control. The following primitives are defined:

PMA_TYPE.indication
PMA_UNITDATA.request
PMA_UNITDATA.indication
PMA_LINK.request
PMA_LINK.indication
PMA_CARRIER.indication
PMA_RXERROR.indication

The parameter config is passed from PHY Control to the PMA via the primitive PHYC_CONFIG.indication. The definition of this parameter is given for the PHY Control Service interface in 32.2.2.1 and is not repeated here for the PMA Service interface.

32.4.2.1 PMA_TYPE.indication

This primitive is generated by the PMA to indicate the nature of the PMA instantiation. Its purpose is to allow clients to support connections to the various types of 100BASE-T PMA entities in a generalized manner.

32.4.2.1.1 Semantics of the service primitive

PMA_TYPE.indication (pma_type)

The pma_type parameter for use with the 100BASE-T2 PMA is T2.

32.4.2.1.2 When generated

The PMA shall continuously generate this primitive to indicate the value of pma_type.

32.4.2.1.3 Effect of receipt

The client uses the value of pma_type to define the semantics of the primitives defined at the PMA service interface.

32.4.2.2 PMA_UNITDATA.request

This primitive defines the transfer of pairs of quinary symbols in the form of the tx_symb_vector parameter from the PCS to the PMA. The quinary symbols are obtained in the PCS Transmit function using the encoding rules defined in 32.3.1.2 to represent MII data streams, an idle mode, or other sequences.

32.4.2.2.1 Semantics of the service primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission using 100BASE-T2 signaling, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over each of the two transmit pairs BI_DA and BI_DB. The tx_symb_vector parameter takes on the form:

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SYMB_PAIR A vector of two quinary symbols, one for each of the two transmit pairs BI_DA and BI_DB. Each quinary symbol may take on one of the values –2, –1, 0, +1 or +2.

The quinary symbols that are elements of tx_symb_vector are called, according to the pair on which each will be transmitted, tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB].

32.4.2.2.2 When generated

The PCS generates PMA_UNITDATA.request (SYMB_PAIR) synchronously with every MII TX_CLK cycle.

32.4.2.2.3 Effect of receipt

Upon receipt of this primitive, the PMA transmits on the MDI the signals corresponding to the indicated quinary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pairs BI_DA and BI_DB.

32.4.2.3 PMA_UNITDATA.indication

This primitive defines the transfer of pairs of quinary symbols in the form of the rx_symb_vector parameter from the PMA to the PCS.

32.4.2.3.1 Semantics of the service primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception of PAM5×5 signals using 100BASE-T2 signaling, the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on each of the two receive pairs BI_DA and BI_DB. The rx_symbol_vector parameter takes on the form:

SYMB_PAIR A vector of two quinary symbols, one for each of the two receive pairs BI_DA and BI_DB. Each quinary symbol may take on one of the values –2, –1, 0, +1 or +2.

The quinary symbols that are elements of rx_symb_vector are called, according to the pair upon which each symbol was received, rx_symbol_vector[BI_DA] and rx_symb_vector[BI_DB].

32.4.2.3.2 When generated

The PMA shall generate PMA_UNITDATA.indication (SYMB_PAIR) messages synchronously with signals received at the MDI.

32.4.2.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

32.4.2.4 PMA_LINK.request

This primitive allows the Auto-Negotiation algorithm to enable and disable operation of the PMA.

32.4.2.4.1 Semantics of the service primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of three values: SCAN_FOR_CARRIER, DISABLE, or ENABLE.

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SCAN_FOR_CARRIER	Used by the Auto-Negotiation algorithm prior to receiving any fast link pulses. During this mode the PMA reports link_status=FAIL. PHY processes are disabled.
DISABLE	Set by the Auto-Negotiation algorithm in the event fast link pulses are detected. *PHY processes are disabled.* This allows the Auto-Negotiation algorithm to determine how to configure the link.
ENABLE	Used by Auto-Negotiation to turn control over to the PHY for data processing functions.

32.4.2.4.2 When generated

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm issues the message PMA_LINK.request (SCAN_FOR_CARRIER).

32.4.2.4.3 Effect of receipt

While link_control=SCAN_FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=FAIL. While link_control=ENABLE, PHY Control determines the operations to be performed by the PHY.

32.4.2.5 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium. This primitive informs the PCS, PHY Control and the Auto-Negotiation algorithm about the status of the underlying link.

32.4.2.5.1 Semantics of the service primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of three values: FAIL, READY, or OK.

FAIL	No valid link established.
READY	Training completed after Auto-Negotiation.
OK	The Link Monitor function indicates that a valid 100BASE-T2 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

32.4.2.5.2 When generated

The PMA shall generate this primitive to indicate the value of link_status in compliance with the state diagrams given in Figure 32-16.

32.4.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 32.2 and 32.3.

32.4.2.6 PMA_CARRIER.indication

This primitive is identical to PCS_CARRIER.indication defined in 32.3.5.2. It is not explicitly shown in the PMA reference diagram.

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32.4.2.7 PMA_RXERROR.indication

This primitive is identical to PCS_RXERROR.indication defined in 32.3.5.2. It is not explicitly shown in the PMA reference diagram.

32.4.2.8 PMA_RXSTATUS.request

This primitive allows the Link Monitor to determine via the parameter loc_rcvr_status generated by the PCS Receive function whether reliable receiver operations are established. The parameter loc_rcvr_status is also passed from the PCS Receive function to the PHY Control Service interface via the primitive PHYC_RXSTATUS.request. The definition of this parameter is given for the PHY Control Service interface in 32.2.2.3 and is not repeated here for the PMA Service interface.

32.5 Management functions

100BASE-T2 makes extensive use of the management functions provided by the Media Independent Interface (Clause 22) and the communication and self-configuration functions provided by Auto-Negotiation (Clause 28.)

In addition to the provision of MII Registers 0, 1, 4, 5, 6, and 7, it is required that implementations that support 100BASE-T2 also provide equivalents to MII Registers 8, 9, and 10 (Clause 22). Register 8 is used to provide the Auto-Negotiation Link Partner NEXT Page Register, Register 9 is used to provide the MASTER-SLAVE Control Register, and Register 10 is used to provide the MASTER-SLAVE Status Register. These registers are used to configure PHYs for testing, to manually configure PHYs for MASTER-SLAVE negotiation, to store the contents of Next Pages during the Auto-Negotiation process, and to store information reporting the results of the master/slave configuration process as described in the next subclause.

32.5.1 100BASE-T2 Use of Auto-Negotiation and MII Registers 8, 9, and 10

On power-up, before Auto-Negotiation starts, the Auto-Negotiation Advertisement register shall have the following configuration: The Selector Field (4.4:0) is set to an appropriate code as specified in Annex 28A. The Acknowledge bit (4.14) is set to logic zero. The Technology Ability Field (4:9:5) is set based on the values set in the MII Status Register (Register 1) (1.15:11) or equivalent and (4.11:10) is set based on the values set in the MII Status Register (Register 1) (1.10:9) or equivalent.

When Auto-Negotiation begins, 100BASE-T2 implementations send an Auto-Negotiation Base Page with bit D15 set to logical one to indicate that a Next Page follows (see 28.2.1.2.)

The Base Page is followed by a formatted Next Page containing the 100BASE-T2 Technology Ability Message Code (7), which indicates that two Unformatted Next Pages containing the 100BASE-T2 Technology Ability fields follow (see Table 28C–1.)

Two Unformatted Next Pages are sent using the 100BASE-T2 Technology Ability fields shown in Table 32–6 Register 8 will be used to store the transmitted information while it is being processed as described below.

Bit U0 of page 1 shall be copied from MII Register 4.10 to indicate 100BASE-T2FD advertised ability.

Bit U1 of page 1 shall be copied from MII Register 4.11 to indicate 100BASE-T2HD advertised ability.

Bit U2 of page 1 shall be copied from MASTER-SLAVE control register 9.10 to indicate that the PHY device is a repeater port or DTE for 100BASE-T2.

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Bits U3 and U4 shall be copied from MASTER-SLAVE control register (bits 9.12 and 9.11) for use by the MASTER-SLAVE negotiation process as described below.

Bits U5-U10 of page 1 and U0-U9 of page 2 shall be used to define the seed used for the MASTER-SLAVE negotiation process described as follows.

Using the information described above, the PHY performs a MASTER-SLAVE configuration process as defined in 32.5.4.3. This process is conducted at the entrance to the FLP LINK GOOD CHECK state shown Auto-Negotiation Arbitration State Diagram (Figure 28–18.)

If the local device detects that both the local device and the remote device are of the same type (either repeater or DTE) and that both have generated the same random seed, it sets the Ack2 bit of Register 8 to logical zero and generates and transmits a new random seed for MASTER-SLAVE negotiation.

The MASTER-SLAVE configuration process returns one of the three following outcomes.

Successful: Bit 10:15 of the MASTER-SLAVE Status Register is set to logical zero and bit 10.14 is set to logical one. 100BASE-T2 returns control to Auto-Negotiation (at the entrance to the FLP LINK GOOD CHECK state in Figure 28–18) and passes the value of MASTER or SLAVE to PHYC_CONFIG.indication (see 32.2.2.)

Unsuccessful: link_status_T2 is set to FAIL and Auto-Negotiation restarts (see Figure 28–18.)

Fault detected: (This happens when both end stations are set for manual configuration and both are set to MASTER or both are set to SLAVE.) Bit 10.15 of the MASTER-SLAVE Status Register is set to logical one to indicate that a manual configuration fault has been detected and bit 10.14 is set to logical one to indicate that MASTER-SLAVE resolution completed with a fault. Because the MASTER-SLAVE relationship was not established, link_status_T2 is set to FAIL, causing Auto-Negotiation to restart.

32.5.2 Management functions

The management interface specified in Clause 22 provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface. The register definition specifies a basic register set with an extension mechanism.

100BASE-T2 requires the basic register set that consists of two registers referred to as the Control Register (Register 0) and the Status Register (Register 1) and of some PHY-specific registers. The detailed definitions of these registers are given in 22.2.4.

The full set of management registers is listed in Table 22–6 and 100BASE-T2 PHY specific registers are given in Table 32–3.

Table 32–3—100BASE-T2 Control and Status registers

Register address	Register name	Basic/Extended
9	MASTER-SLAVE Control register	E
10	MASTER-SLAVE Status register	E

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32.5.3 PHY specific registers for 100BASE-T2

Some of the extended registers (registers with addresses 2 to 15) are used as PHY specific registers as described in 22.2.4.3. A 100BASE-T2 PHY shall use register addresses 9 and 10 for its control and status functions. The bits in the 100BASE-T2 Control register are used to place the PHY into several possible test modes and to determine the MASTER-SLAVE relationship during Auto-Negotiation. The bits in the 100BASE-T2 Status register are used to report the MASTER-SLAVE relationship determined during Auto-Negotiation, the local and remote receiver status, and provide an idle error counter.

32.5.3.1 100BASE-T2 Control register (Register 9)

Register 9 shall provide the following values for 100BASE-T2. The assignment of bits in the register is shown in Table 32–4. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 32–4—100BASE-T2 Control register (MII management Register 9) bit definition

Bit(s)	Name	Description	R/W
9.15:14	Transmitter test mode	Default bit values are “00”	R/W
9.13	Receiver test mode	Default bit value is “0”	R/W
9.12	MASTER-SLAVE Manual Configuration Enable	1 = Enable MASTER-SLAVE Manual Configuration value 0 = Disable MASTER-SLAVE Manual Configuration value (default)	R/W
9.11	MASTER-SLAVE Manual Configuration Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.12 is set to logical one. 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.12 is set to logical one.	R/W
9.10	T2_Repeater/DTE bit	1 = Repeater device port 0 = DTE device	R/W
9.9:0	Reserved		

32.5.3.1.1 Transmitter test mode

For a PHY with 100BASE-T2 capability, the PHY shall be placed in transmitter test mode 1 operation (described in 32.6.1.2.1) when bit 9.15 is set to logical zero and bit 9.14 is set to logical one. When bit 9.15 is set to logical one and bit 9.14 is set to logical zero, the PHY shall be placed in transmitter test mode 2 operation as described in 32.6.1.2.1. When bit 9.15 is set to logical one and bit 9.14 is set to logical one, the PHY shall be placed in the transmitter test mode 3 operation as described in 32.6.1.2.1.

The default value for bits 9.15:14 are all zero.

32.5.3.1.2 Receive test mode

The PHY shall be placed in the receiver test mode as described in 32.6.1.3.2 when the bit 9.13 is set to logical one.

The default value for bit 9.13 is zero.

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32.5.3.1.3 MASTER-SLAVE Manual Configuration Enable

The MASTER-SLAVE relationship is established during Auto-Negotiation via either automatic MASTER-SLAVE configuration or manual configuration. If bit 9.12 is set to logical zero, then the MASTER-SLAVE configuration negotiation function will determine the PHY configuration. If bit 9.12 is set to logical one, then manual MASTER-SLAVE configuration is enabled, using 9.11 to specify the value. (Usage of this bit is further described in 32.5.3.1.)

The default value of bit 9.12 is zero.

32.5.3.1.4 MASTER-SLAVE Manual Configuration Value

MASTER-SLAVE Manual configuration is enabled by setting bit 9.12 to logical one. When manual configuration mode is enabled, setting bit 9.11 to logical one configures the PHY as MASTER, and setting bit 9.11 to logic zero configures the PHY as SLAVE during MASTER-SLAVE negotiation process and shall be used to report the result of the MASTER-SLAVE configuration resolution for that PHY. Detailed description of the use of this bit in MASTER-SLAVE configuration resolution is provided in 32.5.3.1.

The default value of bit 9.11 is zero.

32.5.3.1.5 T2_Repeater/DTE Bit

Bit 9.10 shall be set to logical zero if the PHY is a DTE device and shall be set to a logical one if the PHY is a repeater device port (usage of this bit is described in 32.5.2.)

32.5.3.1.6 Reserved bits

Bits 9.9:0 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

32.5.3.2 100BASE-T2 Status register (Register 10)

Register 10 shall provide the following values for 100BASE-T2. The assignment of bits in the register is shown in Table 32–5. The default value for each bit of the register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 32–5—100BASE-T2 Status register (MII management Register 10) bit definition

Bit(s)	Name	Description	R/W[a]
10.15	MASTER-SLAVE manual configuration fault	1 = MASTER-SLAVE manual configuration fault detected 0 = No MASTER-SLAVE manual configuration fault detected	RO/SC
10.14	MASTER-SLAVE configuration resolution complete	1 = MASTER-SLAVE configuration resolution has completed 0 = MASTER-SLAVE configuration resolution has not completed	RO
10.13	Local Receiver Status	1 = Local Receiver OK 0 = Local Receiver not OK	RO
10.12	Remote Receiver Status	1 = Remote Receiver OK 0 = Remote Receiver not OK	RO
10.11:8	Reserved		
10.7:0	Idle Error Count	Idle Error count	RO/SC

[a]R/W = Read/Write, SC = Self Clearing, RO = Read Only

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32.5.3.2.1 MASTER-SLAVE Manual Configuration Fault

When read as a logical one, bit 10.15 indicates that a MASTER-SLAVE Manual Configuration Fault condition has been detected. The type of fault as well as the criteria and method of fault detection is PHY specific. The MASTER-SLAVE Manual Configuration Fault bit shall be implemented with a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until it is cleared. The MASTER-SLAVE Manual Configuration Fault bit shall be cleared each time Register 10 is read via the management interface and shall also be cleared by a 100BASE-T2 PMA reset.

For 100BASE-T2, this fault condition will occur when both PHYs are forced to be MASTER or SLAVE at the same time using bits 9.12 and 9.11. Bit 10.15 should be set via the MASTER-SLAVE Configuration Resolution function described in 32.5.4.

32.5.3.2.2 MASTER-SLAVE Configuration Resolution Complete

When read as a logical one, bit 10.14 indicates that the MASTER-SLAVE Resolution process has been completed and that the contents of Registers 9 and 10 related to MASTER-SLAVE are valid. When read as a logic zero, bit 10.14 indicates that the MASTER-SLAVE Configuration Resolution process has not been completed and that the contents of Registers 9 and 10 which are related to MASTER-SLAVE resolution are invalid. Bit 10.14 should be set via the MASTER-SLAVE Configuration Resolution function described in 32.5.4.

32.5.3.2.3 Local Receiver Status

Bit 10.13 indicates the status of the local receiver. Local receiver status is defined by the value of the loc_rcvr_status variable described in 32.2.3.

32.5.3.2.4 Remote Receiver Status

Bit 10.12 indicates the status of the remote receiver. Remote receiver status is defined by the value of the rem_rcvr_status variable described in 32.2.3.

32.5.3.2.5 Reserved bits

Bit 10.11:8 are reserved for future standardization. They shall be written as zero and shall be ignored when read; however, a PHY shall return the value zero in these bits.

32.5.3.2.6 Idle Error count

Bits 10.7:0 indicate the Idle Error count, where 10.7 is the most significant bit. During normal operation these bits contain a cumulative count of the errors detected when the receiver is receiving idles and the PHY Control parameter tx_mode is equal to SEND_N (indicating that both local and remote receiver status have been detected to be OK). When the PHY has receiver test mode (bit 9.13) enabled, these bits contain a cumulative count of the errors detected at all times when the local receiver status is OK. These bits are reset to all zeros when the error count is read by the management function or upon execution of the PCS Reset function and they are held at all ones in case of overflow (see 30.5.1.1.13).

32.5.4 Changes and additions to Auto-Negotiation (Clause 28)

32.5.4.1 Change to 28.2.4.1.3 (Auto-Negotiation Advertisement register)

For implementations which support 100BASE-T2, the Technology Ability Field (4:9:5) is set based on the values set in the MII Status Register (Register 1) (1.15:11) or equivalent and (4.11:10) is set based on the

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values set in the MII Status Register (Register 1) (1.10:9) or equivalent. Use of Register 4 is defined in 28.2.4.1.3.

32.5.4.2 Use of Auto-Negotiation Next Page codes for 100BASE-T2 PHYs

For a PHY capable of 100BASE-T2 transmission, during Auto-Negotiation the Base Page will be followed by a Next Page with a message code containing the 100BASE-T2 Technology Ability Message Code (7) as shown in Table 28C–1. This Message Next Page indicates that two Unformatted Message Next Pages will follow which contain the 100BASE-T2 Technology Ability Fields as described in Table 32–6.

Table 32–6—Bit assignments for Unformatted Next Pages containing 100BASE-T2 Technology Ability Field

Bit	Technology	MII register bit/source
PAGE 1		
U0	100BASE-T2 Half Duplex (1 = Half Duplex and 0 = no Half Duplex)	MII Register 4.10
U1	100BASE-T2 Full Duplex (1=Full Duplex and 0 = no Full Duplex)	MII Register 4.11
U2	100BASE-T2 Repeater/DTE bit (1 = Repeater and 0 = DTE)	MII Register 9.10 (MASTER-SLAVE Control register)
U3	100BASE-T2 MASTER-SLAVE Manual Configuration Enable (1 = Manual Configuration Enable); intended to be used for manual selection in a particular MASTER-SLAVE mode. To be used in conjunction with bit U4	MII Register 9.12 (MASTER-SLAVE Control register)
U4	100BASE-T2 MASTER-SLAVE Manual Configuration value 1 = MASTER and 0 = SLAVE. This bit is ignored if U3 = 0.	MII Register 9.11 (MASTER-SLAVE Control register)
U5	100BASE-T2 MASTER-SLAVE Seed Bit 0 (SB0) (LSB)	MASTER-SLAVE seed value (15.0)
U6	100BASE-T2 MASTER-SLAVE Seed Bit 1 (SB1)	
U7	100BASE-T2 MASTER-SLAVE Seed Bit 2 (SB2)	
U8	100BASE-T2 MASTER-SLAVE Seed Bit 3 (SB3)	
U9	100BASE-T2 MASTER-SLAVE Seed Bit 4 (SB4)	
U10	100BASE-T2 MASTER-SLAVE Seed Bit 5 (SB5)	
PAGE 2		
U0	100BASE-T2 MASTER-SLAVE Seed Bit 6 (SB6)	
U1	100BASE-T2 MASTER-SLAVE Seed Bit 7 (SB7)	
U2	100BASE-T2 MASTER-SLAVE Seed Bit 8 (SB8)	
U3	100BASE-T2 MASTER-SLAVE Seed Bit 9 (SB9)	
U4	100BASE-T2 MASTER-SLAVE Seed Bit 10 (SB10)	
U5	100BASE-T2 MASTER-SLAVE Seed Bit 11 (SB11)	
U6	100BASE-T2 MASTER-SLAVE Seed Bit 12 (SB12)	
U7	100BASE-T2 MASTER-SLAVE Seed Bit 13 (SB13)	
U8	100BASE-T2 MASTER-SLAVE Seed Bit 14 (SB14)	
U9	100BASE-T2 MASTER-SLAVE Seed Bit 15 (SB15)	
U10	unused	

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32.5.4.3 MASTER-SLAVE Configuration Resolution

Since both PHYs that share a link segment are capable of being MASTER or SLAVE, a prioritization scheme exists to ensure that the correct mode is chosen. The MASTER-SLAVE relationship shall be determined during Auto-Negotiation using Table 32–7 with the 100BASE-T2 Technology Ability Next Page bit values specified in Table 32–7 and information received from the link partner.

Table 32–7—100BASE-T2 MASTER-SLAVE Configuration Resolution table

Local Device Type	Remote Link Partner Type	Resolution Function result	
		Local Device	Remote Link Partner
DTE (U2=0 & U3=0) or Manual SLAVE (U3=1 & U4=0)	Repeater (U2=1 & U3=0) or Manual MASTER (U3=1 & U4=1)	SLAVE	MASTER
Repeater (U2=1 & U3=0)	Manual MASTER (U3=1 & U4=1)		
Manual SLAVE (U3=1 & U4=0)	DTE (U2=0 & U3=0)		
Repeater (U2=1 & U3=0) or Manual MASTER (U3=1 & U4=1)	DTE (U2=0 & U3=0) or Manual SLAVE (U3=1 & U4=0)	MASTER	SLAVE
DTE (U2=0 & U3=0)	Manual Slave (U3=1 & U4=0)		
Manual Master (U3=1 & U4=1)	Repeater (U2=1 & U3=0)		
Repeater (U2=1 & U3=0)	Repeater (U2=1 & U3=0)	PHY with higher seed value is the MASTER. If the seeds are equal, the MASTER-SLAVE resolution is unsuccessful, set link_status_T2=FAIL, causing Auto-Negotiation to restart.	
DTE (U2=0 & U3=0)	DTE (U2=0 & U3=0)		
Manual SLAVE (U3=1 & U4=0)	Manual SLAVE (U3=1 & U4=0)	Fault detected Set link_status_T2=FAIL, forcing Auto-Negotiation to restart.	
Manual MASTER (U3=1 & U4=1)	Manual MASTER (U3=1 & U4=1)		

The rationale for this hierarchy is straightforward. A 100BASE-T2 repeater has higher priority than a DTE to become the MASTER. In the case where both devices are of the same type, e.g., both devices are Repeaters, the device with the higher MASTER-SLAVE seed bits (SB0..SB15), where SB15 is the MSB, becomes the MASTER and the device with the lower seed value becomes the SLAVE. In case both devices have the same seed value, both should assert link_status_T2=FAIL (as defined in 28.3.1) and restart Auto-Negotiation. Successful completion of the MASTER-SLAVE resolution shall be treated as MASTER-SLAVE configuration resolution complete and the 100BASE-T2 Status Register bit 10.14 shall be set to logical one.

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The method of generating a random seed is left to the implementer. The generated random seeds should belong to a sequence of independent, identically distributed integer numbers with a uniform distribution in the range of 0 to 65535. The algorithm used to generate the integer should be designed to minimize the correlation between the number generated by any two devices at any given time. A seed counter shall be provided to track the number of seed attempts. The seed counter shall be set to zero at start-up and shall be incremented each time a seed is generated. A MASTER-SLAVE resolution fault shall be declared if resolution is not reached after the generation of seven seeds.

The MASTER-SLAVE Manual Configuration Enable bit (control register bit 9.12) is used to manually set a device to become the MASTER or the SLAVE. In case both devices are manually set to become the MASTER or the SLAVE, this condition shall be flagged as a MASTER-SLAVE Manual Configuration fault condition, thus the MASTER-SLAVE Manual Configuration fault bit (status register bit 10.15) shall be set to logical one. The MASTER-SLAVE Manual Configuration fault condition shall be treated as MASTER-SLAVE configuration resolution complete and status register bit 10.14 shall be set to logical one. In this case, link_status_T2 will be set to FAIL, because the MASTER-SLAVE relationship was not resolved. This will force Auto-Negotiation to restart after the link_fail_inhibit_timer has expired. Determination of MASTER-SLAVE values occur on the entrance to the FLP LINK GOOD CHECK state (Figure 28–18) when the highest common denominator (HCD) technology is 100BASE-T2. The resulting MASTER-SLAVE value is used by the 100BASE-T2 PHY control (32.2.2.1).

32.6 PMA electrical specifications

This clause defines the electrical characteristics of the PHY at the MDI.

The ground reference point for all common-mode tests is the MII ground circuit. Implementations without an MII use the chassis ground. The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

32.6.1 PMA-to-MDI interface characteristics

32.6.1.1 Isolation requirement

The PHY shall provide electrical isolation between the DTE or repeater circuits, including frame ground and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50–60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

32.6.1.2 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 32.4.1.1.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

The tolerance on the poles of the test filters used in this clause shall be ±1%.

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32.6.1.2.1 Transmitter test modes

Since the 100BASE-T2 PCS employs scrambling, synchronization of data at the MII to the scrambled state is virtually impossible. Therefore a special transmit test mode shall be required to allow for testing of the transmitter waveform. Additionally, a test mode for measuring transmitter output jitter is also required.

For a PHY with a MII interface, these modes shall be enabled by setting bits 9.14 and 9.15 (MASTER-SLAVE Control Register) of the MII Management register set as shown in Table 32–8. These test modes shall only change the data symbols provided to the transmitter circuitry and may not alter the electrical characteristics of the transmitter. A PHY without an MII shall provide a means to provide these functions. The vendor shall provide a means to enable these modes for conformance testing.

Table 32–8—MII management register set

Bit 9.15	Bit 9.14	Mode
0	0	Normal operation
0	1	TX Test mode 1—waveform test
1	0	TX Test mode 2—jitter test
1	1	TX Test mode 3—idle

When transmit test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols (A_n and B_n of 32.3.1.2.3) continually from both transmitters:

{{+2 followed by 127 0 symbols}, {-2 followed by 127 0 symbols},{+1 followed by 127 0 symbols}, {–1 followed by 127 0 symbols}, {16 +2 symbols, 16 –2 symbols followed by 224 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the transmit test mode is enabled. A typical transmitter output is shown below in Figure 32–17. The transmitter shall time the transmitted symbols from a 25.000 MHz ± 0.01% clock.

When transmit test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+2,–2} repeatedly on both channels. The transmitter shall time the transmitted symbols from a 25.000 MHz ± 0.01% clock.

When transmit test mode 3 is enabled, the PHY shall transmit idle data compliant with the idle signaling specified in 32.3 with loc_rcvr_status=OK.

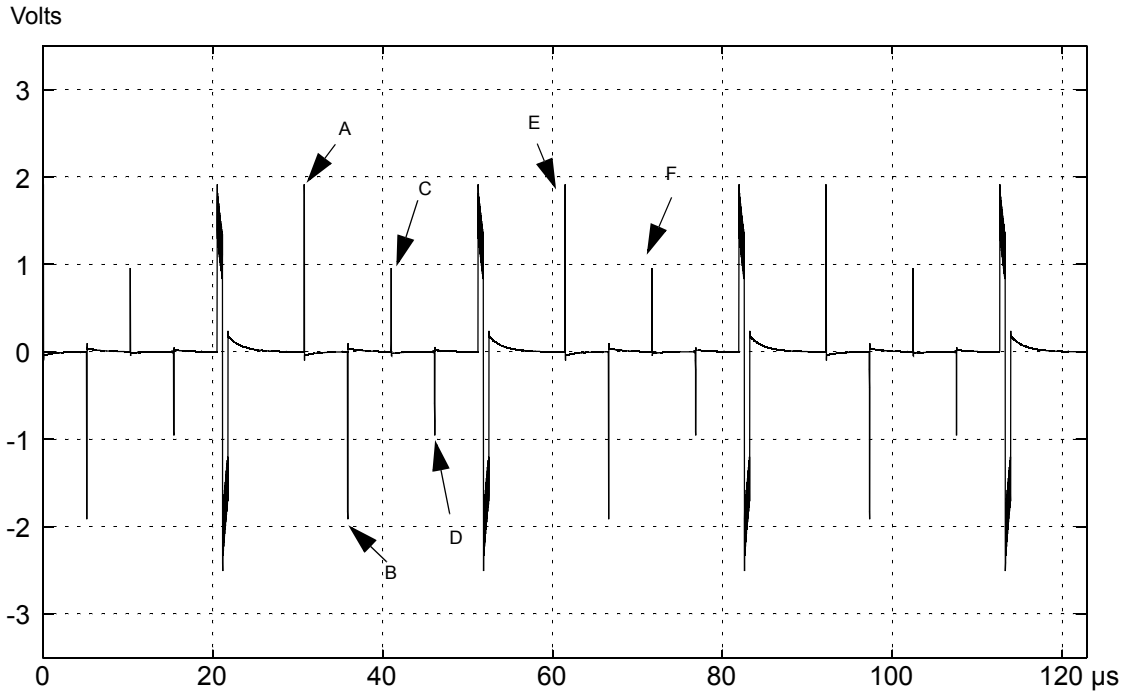
32.6.1.2.2 Peak differential output voltage and level distortion

When in transmit test mode 1 and observing the differential signal output at the MDI terminated in 100 Ω, preprocessed by the high pass filter defined below, for each pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 32–17 shall fall within 1.71 V to 1.91 V (1.81 V ± 0.5 dB).

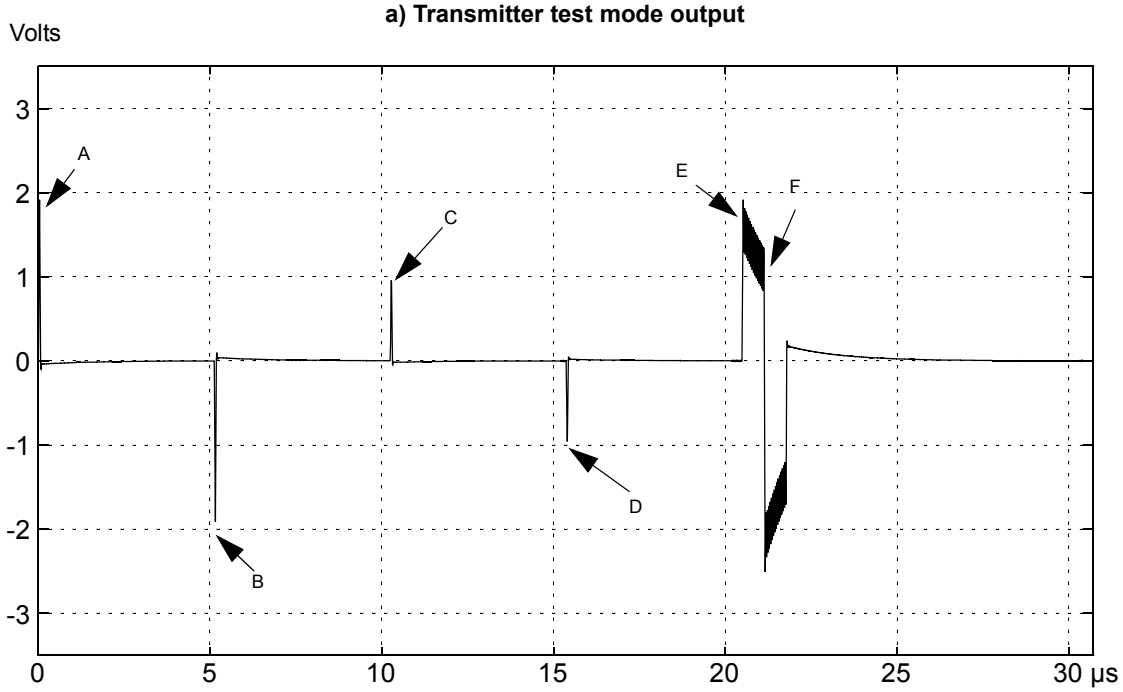
The absolute value of the peak of the waveforms at points A and B shall differ by less than 1%.

The absolute value of the peak of the waveform at points C and D as defined in Figure 32–17 shall differ from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.

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a) Transmitter test mode output



b) Expanded view of partial cycle of transmitter test mode output

Figure 32–17—Example transmitter test mode transmitter

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The preprocessing filter shall have the following transfer function:[13]

$$H_{\text{preprocess}}(f) = \frac{\mathrm{j}f}{\mathrm{j}f + 200 \times 10^3} \quad f \text{ in Hz}$$

32.6.1.2.3 Maximum output droop

When in transmit test mode 1 and observing the differential signal output at the MDI, for either pair, with no intervening cable, the peak value of the waveform at point F as defined in Figure 32–17 shall be greater than 70.5% of the peak value of the waveform at point E. A preprocessing filter is not used for this measurement.

32.6.1.2.4 Differential output templates

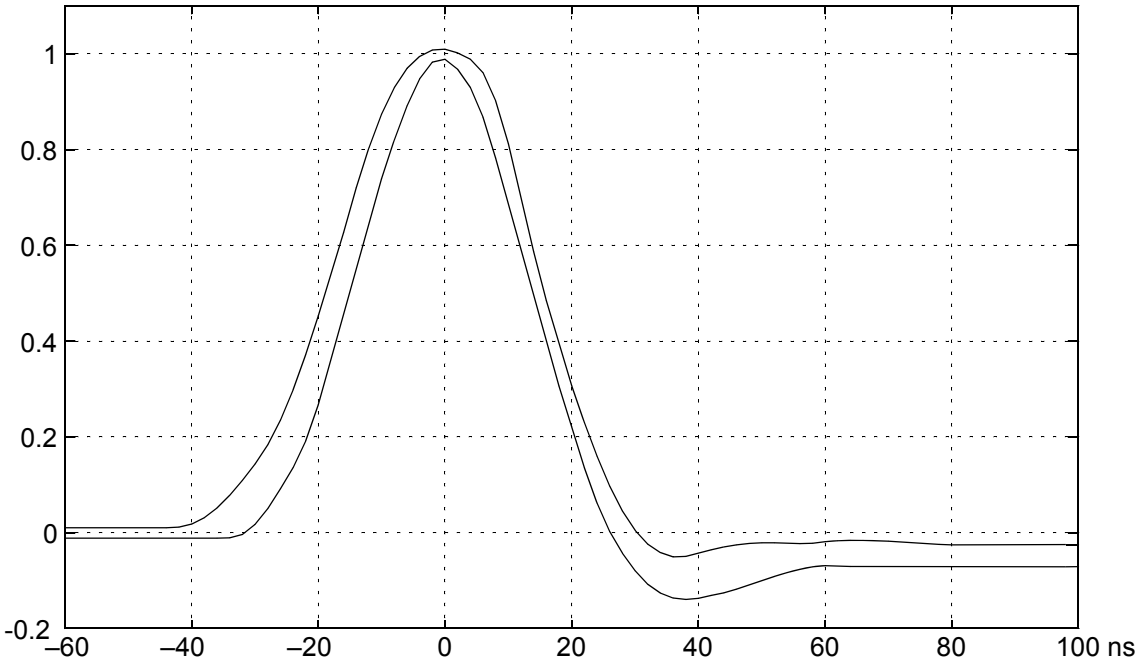
The transmitter differential output voltage shall be measured at the output of the high pass preprocessing filter defined in 32.6.1.2.2, with no intervening cables. The voltage waveforms A, B, C and D defined in Figure 32–17, after normalization by their respective peak values, shall lie within the time domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–9. The waveforms may be shifted in time as appropriate to fit within the template.

Additionally, the magnitude in dB of the Fourier transform of the preprocessed waveforms A, B, C and D shall lie within the frequency domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–9. The time span of the waveforms so processed shall be –80 ns to +2000 ns with the 0 ns point of the waveform aligned as for the time domain mask shown in Figure 32–18 and the magnitude of the Fourier transform should be normalized so that the maximum value is at 0 dB.[14]

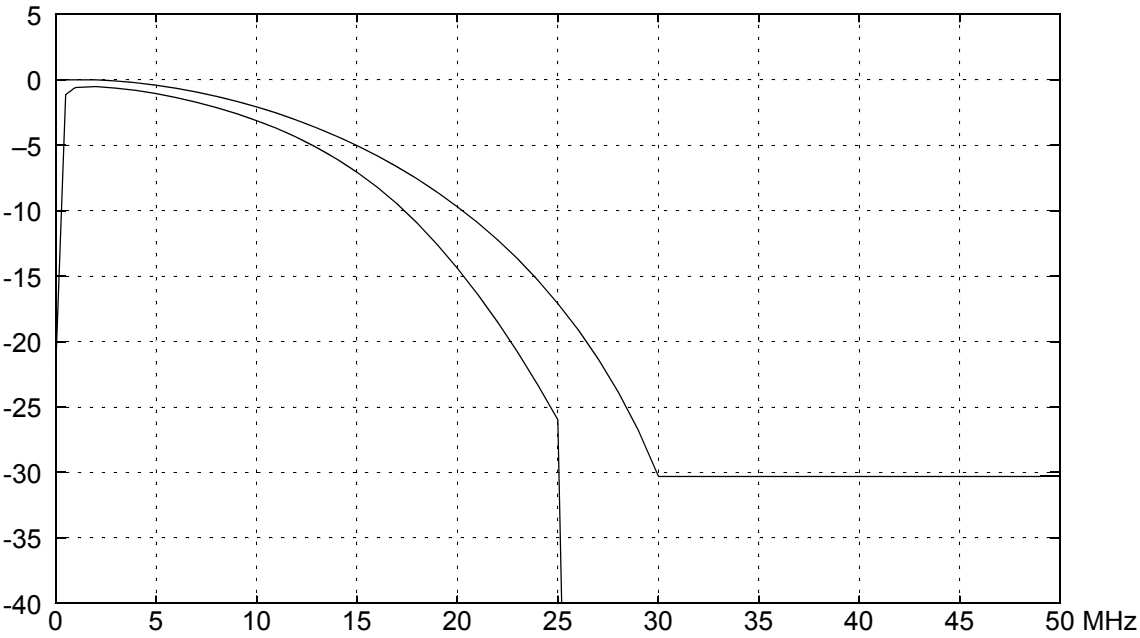
[13]"j" denotes the positive square root of –1.

[14]A sampling rate of 100 MHz is adequate to generate the frequency domain mask.

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a) Normalized time domain transmit template



b) Normalized frequency domain transmit template

NOTE—The frequency domain transmit template is not intended to address electromagnetic radiation limits.

Figure 32–18—Normalized transmit templates as measured at MDI through preprocessing filter

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Table 32–9—Normalized time domain voltage template

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
–60	0.010	–0.011	22	0.230	0.136
–58	0.010	–0.011	24	0.160	0.062
–56	0.010	–0.011	26	0.097	0.002
–54	0.010	–0.011	28	0.045	–0.042
–52	0.010	–0.011	30	0.005	–0.079
–50	0.010	–0.011	32	–0.024	–0.108
–48	0.010	–0.011	34	–0.042	–0.126
–46	0.010	–0.011	36	–0.051	–0.136
–44	0.010	–0.011	38	–0.050	–0.139
–42	0.012	–0.011	40	–0.043	–0.137
–40	0.018	–0.011	42	–0.036	–0.131
–38	0.031	–0.011	44	–0.030	–0.126
–36	0.052	–0.011	46	–0.025	–0.118
–34	0.078	–0.011	48	–0.023	–0.109
–32	0.109	–0.004	50	–0.021	–0.100
–30	0.143	0.017	52	–0.021	–0.091
–28	0.184	0.050	54	–0.022	–0.084
–26	0.235	0.092	56	–0.023	–0.077
–24	0.298	0.136	58	–0.022	–0.071
–22	0.372	0.192	60	–0.019	–0.069
–20	0.453	0.268	62	–0.017	–0.070
–18	0.538	0.360	64	–0.016	–0.070
–16	0.627	0.461	66	–0.016	–0.071
–14	0.720	0.558	68	–0.017	–0.071
–12	0.804	0.650	70	–0.018	–0.071
–10	0.874	0.739	72	–0.020	–0.071
–8	0.930	0.820	74	–0.021	–0.071
–6	0.969	0.891	76	–0.023	–0.071
–4	0.995	0.948	78	–0.024	–0.070
–2	1.008	0.982	80	–0.026	–0.070
0	1.009	0.988	82	–0.025	–0.070

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Table 32–9—Normalized time domain voltage template *(continued)*

Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit	Time, ns	Normalized transmit time domain template, upper limit	Normalized transmit time domain template, lower limit
2	1.002	0.967	84	–0.025	–0.070
4	0.989	0.930	86	–0.025	–0.071
6	0.961	0.868	88	–0.025	–0.071
8	0.902	0.782	90	–0.025	–0.072
10	0.812	0.685	92	–0.025	–0.072
12	0.703	0.585	94	–0.025	–0.072
14	0.587	0.489	96	–0.025	–0.071
16	0.485	0.396	98	–0.025	–0.071
18	0.394	0.306	100	–0.025	–0.071
20	0.307	0.221			

Table 32–10—Normalized frequency domain amplitude spectrum template

Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB	Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB
0.1	0.00	–17.88	22	–12.24	–18.52
0.2	0.00	–13.49	23	–13.70	–20.84
0.3	0.00	–9.09	24	–15.31	–23.32
0.4	0.00	–4.70	25	–17.09	–25.97
0.5	0.00	–1.13	26	–19.08	
0.6	0.00	–1.01	27	–21.31	
0.7	0.00	–0.90	28	–23.84	
0.8	0.00	–0.78	29	–26.78	
0.9	0.00	–0.66	30	–30.29	
1	0.00	–0.59	31	–30.29	
2	–0.00	–0.52	32	–30.29	
3	–0.08	–0.63	33	–30.29	
4	–0.23	–0.82	34	–30.29	

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Table 32–10—Normalized frequency domain amplitude spectrum template *(continued)*

Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB	Frequency, MHz	Normalized transmit frequency domain template, upper limit, dB	Normalized transmit frequency domain template, lower limit, dB
5	–0.42	–1.06	35	–30.29	
6	–0.65	–1.36	36	–30.29	
7	–0.93	–1.71	37	–30.29	
8	–1.26	–2.12	38	–30.29	
9	–1.64	–2.59	39	–30.29	
10	–2.07	–3.12	40	–30.29	
11	–2.55	–3.72	41	–30.29	
12	–3.08	–4.40	42	–30.29	
13	–3.67	–5.17	43	–30.29	
14	–4.31	–6.05	44	–30.29	
15	–5.03	–7.06	45	–30.29	
16	–5.80	–8.20	46	–30.29	
17	–6.65	–9.50	47	–30.29	
18	–7.58	–10.96	48	–30.29	
19	–8.59	–12.59	49	–30.29	
20	–9.70	–14.39	50	–30.29	
21	–10.91	–16.37			

32.6.1.2.5 Transmitter timing jitter

When in transmit test mode 2, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI shall be less than 0.5 ns.

32.6.1.2.6 Transmit clock frequency

The quinary symbol transmission rate on each pair shall be 25.000 MHz ± 0.01%.

32.6.1.3 Receiver electrical specifications

The PMA shall provide the Receive function specified in 32.4.1.1.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall meet or exceed ISO/IEC 11801, Category 3 specifications.

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32.6.1.3.1 Test channel

To perform the Receiver Alien NEXT Tolerance test and Receiver timing jitter test described in this clause, a test channel including transmitter, cabling and NEXT models is required. This test channel is shown conceptually in Figure 32–19.

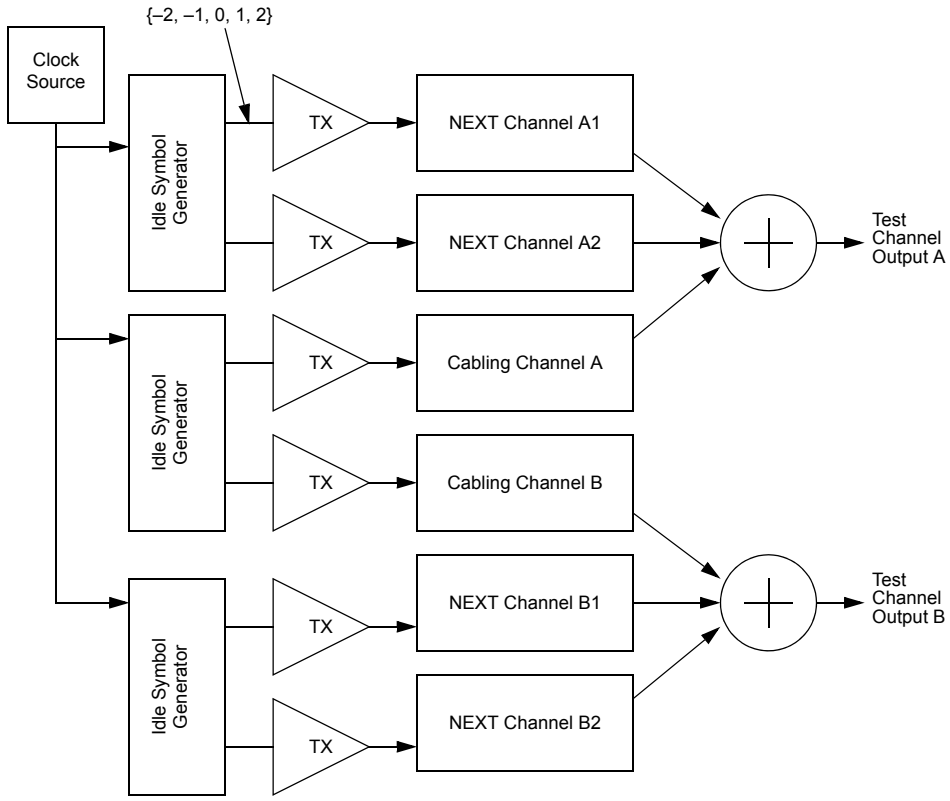


Figure 32–19—Conceptual diagram of test channel

The combined responses of the TX block and NEXT or cabling channel blocks shall be those defined in Table 32–8. The responses of Table 32–10 are shown in Figure 32–20. The responses represent the response of the test channel to isolated "1" symbols in a stream of "0" symbols at the input to the transmitter blocks. The test channel may also include a first order high pass filter with 3 dB cutoff frequency of less than 100 kHz in addition to the tabulated responses. The output impedance of the test channel shall be consistent with 32.6.1.4.1. The idle symbol generator outputs shall be conformant with the idle signaling specified in 32.3 with loc_rcvr_status=OK. The clock source shall result in a quinary symbol transmission rate conformant with 32.6.1.2.6. The peak-to-peak jitter on the clock source shall be less than 0.2 ns.

The test channel may be implemented in any fashion consistent with the above specifications and with the further constraint that the ratio of the squared error between the implemented NEXT channel symbol responses and the specified NEXT channel symbol responses to the energy in the specified NEXT channel symbol responses shall be less than 5% and the energy of the implemented NEXT channel symbol responses and the energy of the specified NEXT channel symbol responses shall differ by less than ± 0.25 dB. If digital filters are used to generate the channel characteristics, care must be taken to ensure that the signal to quantization noise at the channel output is greater than 35 dB.

The NEXT channel impulse responses defined in Table 32–11 have been developed to simulate the attenuation and phase characteristics of worst case 100BASE-T2 alien NEXT.

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The cabling attenuation and group delay characteristics used to derive the cable symbol responses specified in Table 32–8 at 0 m and 100 m are obtained from the following worst-case model of the cabling attenuation. The model includes 1.2 dB of flat loss simulating three worst-case Category 3 connectors. The group delay of the model is relative and does not include the fixed delay associated with 100 m of Category 3 cabling. An additional 570 ns of fixed delay should be added in order to obtain the absolute group delay; however, it is not necessary to add this fixed delay to the test channel.

$$\gamma(f) = -(1.537\times10^{-6}\sqrt{\pi f} + j1.537\times10^{-6}\sqrt{\pi f} + 44.5\times10^{-12}2\pi f)$$

$$H(f, l) = e^{\gamma(f)l}10^{-1.2/20}$$

f in Hz

Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model

Time (µs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.000	4.23e-06	1.48e-03	1.62e-05	1.19e-05	–5.05e-06	3.70e-05
0.004	–4.87e-06	1.55e-03	–5.97e-05	1.67e-05	6.71e-05	2.02e-05
0.008	–6.84e-06	1.62e-03	–8.19e-05	1.15e-05	9.78e-05	1.20e-05
0.012	–1.28e-05	1.69e-03	–3.79e-05	7.58e-06	6.43e-05	1.50e-05
0.016	3.56e-06	1.77e-03	4.53e-05	–1.47e-05	1.52e-06	6.51e-06
0.020	6.97e-06	1.86e-03	1.40e-04	–1.73e-05	–9.59e-05	–8.16e-06
0.024	1.68e-05	1.96e-03	1.86e-04	3.46e-05	–2.01e-04	–3.64e-05
0.028	8.73e-06	2.07e-03	1.07e-04	1.67e-04	–2.67e-04	–8.81e-05
0.032	–1.98e-05	2.19e-03	–2.56e-04	3.80e-04	–1.52e-04	–2.18e-04
0.036	–2.24e-05	2.33e-03	–1.10e-03	5.84e-04	3.94e-04	–5.53e-04
0.040	–2.95e-05	2.48e-03	–2.53e-03	7.54e-04	1.49e-03	–1.14e-03
0.044	3.65e-05	2.64e-03	–4.46e-03	8.74e-04	3.09e-03	–1.95e-03
0.048	7.11e-05	2.83e-03	–6.54e-03	9.73e-04	4.89e-03	–2.83e-03
0.052	6.30e-05	3.04e-03	–8.29e-03	1.13e-03	6.41e-03	–3.56e-03
0.056	–1.42e-04	3.27e-03	–9.25e-03	1.38e-03	7.24e-03	–3.97e-03
0.060	–4.49e-04	3.53e-03	–9.04e-03	1.93e-03	6.96e-03	–3.84e-03
0.064	–2.89e-04	3.87e-03	–7.53e-03	2.90e-03	5.37e-03	–3.06e-03
0.068	–2.72e-04	4.22e-03	–4.73e-03	4.32e-03	2.51e-03	–1.69e-03
0.072	–3.87e-04	4.55e-03	–9.82e-04	5.95e-03	–1.15e-03	–5.29e-05
0.076	–1.39e-04	5.09e-03	3.14e-03	7.23e-03	–4.72e-03	1.19e-03
0.080	4.92e-04	5.83e-03	6.98e-03	7.68e-03	–7.33e-03	1.50e-03
0.084	1.50e-03	6.70e-03	9.98e-03	6.90e-03	–8.27e-03	5.20e-04
0.088	9.97e-04	7.69e-03	1.19e-02	4.74e-03	–7.36e-03	–1.68e-03

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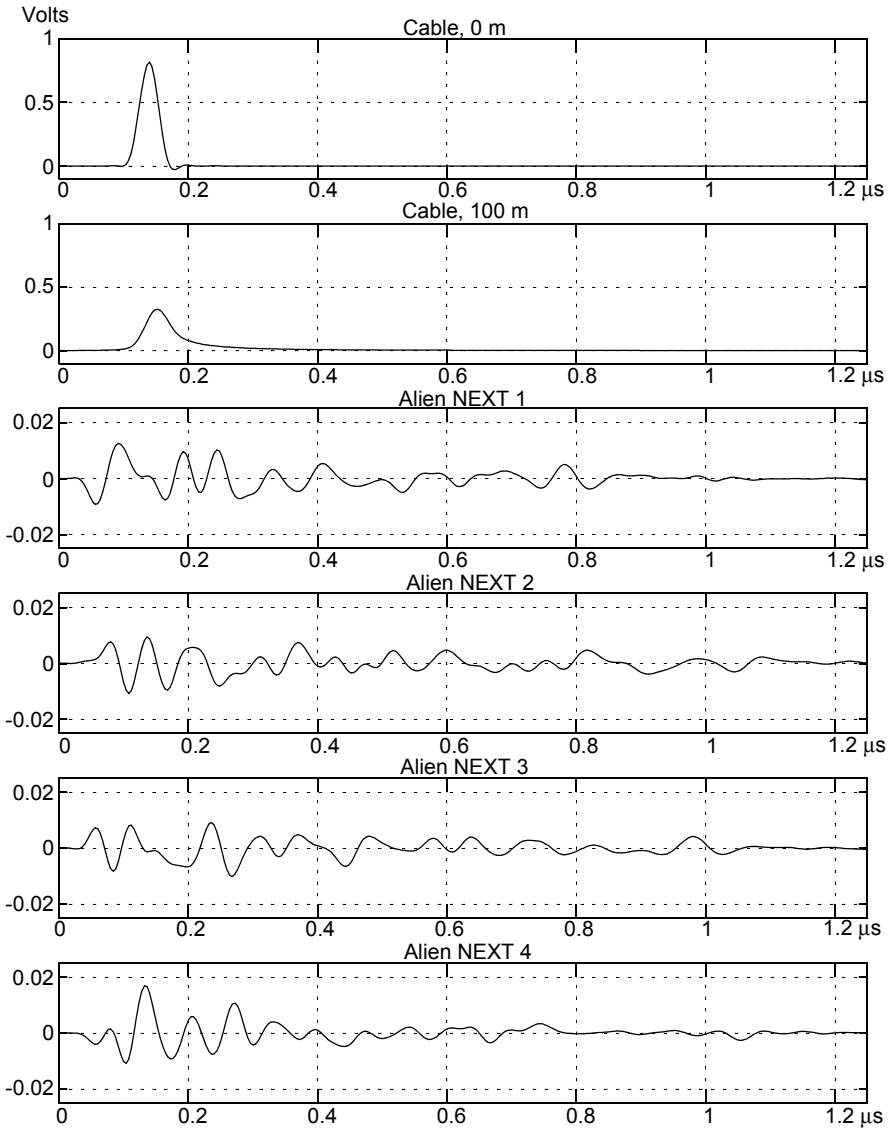


Figure 32–20—Test channel responses

Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (µs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.092	–1.45e-03	8.81e-03	1.26e-02	1.43e-03	–4.82e-03	–4.65e-03
0.096	–3.84e-03	1.04e-02	1.22e-02	–2.63e-03	–1.17e-03	–7.77e-03
0.100	–1.58e-03	1.27e-02	1.10e-02	–6.60e-03	2.75e-03	–1.01e-02
0.104	1.30e-02	1.64e-02	9.20e-03	–9.57e-03	6.05e-03	–1.08e-02
0.108	4.64e-02	2.27e-02	7.06e-03	–1.08e-02	7.97e-03	–9.32e-03
0.112	1.05e-01	3.30e-02	4.91e-03	–9.84e-03	8.20e-03	–5.54e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.116	1.95e-01	4.93e-02	3.07e-03	–7.06e-03	7.00e-03	–2.20e-04
0.120	3.14e-01	7.28e-02	1.72e-03	–3.05e-03	4.92e-03	5.68e-03
0.124	4.54e-01	1.04e-01	9.15e-04	1.34e-03	2.63e-03	1.10e-02
0.128	5.95e-01	1.42e-01	6.23e-04	5.31e-03	6.32e-04	1.50e-02
0.132	7.15e-01	1.84e-01	6.67e-04	8.16e-03	–7.36e-04	1.69e-02
0.136	7.93e-01	2.28e-01	8.34e-04	9.39e-03	–1.30e-03	1.66e-02
0.140	8.15e-01	2.68e-01	7.62e-04	8.84e-03	–1.25e-03	1.44e-02
0.144	7.77e-01	3.01e-01	1.20e-04	6.66e-03	–9.31e-04	1.08e-02
0.148	6.83e-01	3.21e-01	–1.23e-03	3.32e-03	–8.01e-04	6.60e-03
0.152	5.49e-01	3.27e-01	–3.18e-03	–5.48e-04	–1.13e-03	2.50e-03
0.156	3.96e-01	3.20e-01	–5.26e-03	–4.29e-03	–1.86e-03	–1.22e-03
0.160	2.50e-01	3.01e-01	–6.94e-03	–7.31e-03	–2.84e-03	–4.34e-03
0.164	1.30e-01	2.73e-01	–7.68e-03	–9.17e-03	–3.84e-03	–6.80e-03
0.168	4.47e-02	2.40e-01	–7.12e-03	–9.59e-03	–4.72e-03	–8.47e-03
0.172	–5.75e-03	2.06e-01	–5.15e-03	–8.55e-03	–5.39e-03	–9.25e-03
0.176	–2.72e-02	1.75e-01	–1.95e-03	–6.26e-03	–5.80e-03	–9.17e-03
0.180	–2.85e-02	1.49e-01	1.90e-03	–3.26e-03	–6.01e-03	–8.19e-03
0.184	–1.82e-02	1.28e-01	5.60e-03	–1.83e-04	–6.13e-03	–6.35e-03
0.188	–5.94e-03	1.11e-01	8.37e-03	2.37e-03	–6.29e-03	–3.77e-03
0.192	2.81e-03	9.82e-02	9.58e-03	4.08e-03	–6.50e-03	–7.34e-04
0.196	6.25e-03	8.84e-02	9.06e-03	5.05e-03	–6.67e-03	2.21e-03
0.200	5.54e-03	8.06e-02	6.92e-03	5.49e-03	–6.65e-03	4.54e-03
0.204	3.70e-03	7.39e-02	3.66e-03	5.66e-03	–6.24e-03	5.81e-03
0.208	1.64e-03	6.80e-02	6.86e-05	5.68e-03	–5.26e-03	5.91e-03
0.212	5.59e-05	6.26e-02	–3.01e-03	5.52e-03	–3.62e-03	4.88e-03
0.216	–1.02e-03	5.77e-02	–4.83e-03	5.16e-03	–1.33e-03	2.95e-03
0.220	–1.53e-03	5.34e-02	–4.97e-03	4.40e-03	1.42e-03	4.48e-04
0.224	–9.73e-04	4.96e-02	–3.46e-03	3.07e-03	4.28e-03	–2.25e-03
0.228	–3.20e-04	4.63e-02	–6.22e-04	1.04e-03	6.85e-03	–4.71e-03
0.232	2.89e-05	4.33e-02	2.90e-03	–1.55e-03	8.65e-03	–6.56e-03
0.236	1.73e-04	4.06e-02	6.35e-03	–4.20e-03	9.24e-03	–7.53e-03
0.240	1.33e-04	3.83e-02	8.95e-03	–6.40e-03	8.35e-03	–7.48e-03
0.244	1.39e-04	3.62e-02	1.02e-02	–7.73e-03	5.99e-03	–6.40e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.248	9.80e-05	3.42e-02	9.77e-03	–8.11e-03	2.56e-03	–4.30e-03
0.252	4.22e-05	3.25e-02	7.90e-03	–7.70e-03	–1.34e-03	–1.35e-03
0.256	–2.56e-06	3.08e-02	4.95e-03	–6.76e-03	–5.02e-03	2.14e-03
0.260	–3.84e-05	2.93e-02	1.50e-03	–5.62e-03	–7.91e-03	5.67e-03
0.264	–2.83e-05	2.80e-02	–1.85e-03	–4.58e-03	–9.67e-03	8.59e-03
0.268	–2.41e-05	2.67e-02	–4.54e-03	-3.89e-03	–1.01e-02	1.04e-02
0.272	–8.46e-06	2.55e-02	–6.29e-03	–3.61e-03	–9.30e-03	1.08e-02
0.276	4.04e-07	2.44e-02	–7.13e-03	–3.62e-03	–7.62e-03	9.78e-03
0.280	4.91e-06	2.34e-02	–7.25e-03	–3.70e-03	–5.51e-03	7.51e-03
0.284	1.01e-05	2.24e-02	–6.97e-03	–3.61e-03	–3.40e-03	4.44e-03
0.288	3.79e-06	2.15e-02	–6.54e-03	–3.18e-03	–1.47e-03	1.18e-03
0.292	2.18e-06	2.07e-02	–6.11e-03	–2.37e-03	2.01e-04	–1.65e-03
0.296	–2.23e-06	1.99e-02	–5.78e-03	–1.23e-03	1.62e-03	–3.54e-03
0.300	–1.74e-06	1.92e-02	–5.43e-03	6.10e-05	2.78e-03	–4.28e-03
0.304	4.33e-07	1.85e-02	–4.87e-03	1.26e-03	3.62e-03	–3.93e-03
0.308	2.19e-07	1.79e-02	–3.88e-03	2.10e-03	4.14e-03	–2.74e-03
0.312	1.40e-06	1.73e-02	–2.42e-03	2.37e-03	4.25e-03	–1.08e-03
0.316	–5.61e-07	1.67e-02	–7.17e-04	1.97e-03	3.87e-03	6.99e-04
0.320	–4.40e-07	1.62e-02	9.57e-04	9.16e-04	2.95e-03	2.25e-03
0.324	–4.37e-07	1.56e-02	2.28e-03	–5.89e-04	1.53e-03	3.34e-03
0.328	–3.68e-08	1.51e-02	3.07e-03	–2.20e-03	–8.99e-05	3.92e-03
0.332	9.92e-07	1.47e-02	3.23e-03	–3.52e-03	–1.59e-03	4.04e-03
0.336	5.29e-07	1.43e-02	2.74e-03	–4.19e-03	–2.63e-03	3.85e-03
0.340	5.69e-07	1.38e-02	1.73e-03	–4.00e-03	–3.00e-03	3.44e-03
0.344	–1.87e-07	1.34e-02	4.38e-04	–2.97e-03	–2.62e-03	2.85e-03
0.348	–3.47e-07	1.31e-02	–8.80e-04	–1.22e-03	–1.53e-03	2.11e-03
0.352	–9.04e-08	1.27e-02	–2.04e-03	9.56e-04	5.06e-05	1.27e-03
0.356	8.10e-08	1.24e-02	–3.01e-03	3.22e-03	1.79e-03	3.65e-04
0.360	5.29e-07	1.20e-02	–3.78e-03	5.22e-03	3.32e-03	–5.53e-04
0.364	3.23e-07	1.17e-02	–4.36e-03	6.64e-03	4.36e-03	–1.41e-03
0.368	1.82e-07	1.14e-02	–4.67e-03	7.34e-03	4.82e-03	–2.03e-03
0.372	–6.93e-08	1.11e-02	–4.60e-03	7.31e-03	4.75e-03	–2.26e-03
0.376	–1.46e-07	1.09e-02	–4.11e-03	6.65e-03	4.31e-03	–1.98e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.380	6.66e-08	1.06e-02	–3.17e-03	5.50e-03	3.64e-03	–1.29e-03
0.384	1.71e-07	1.03e-02	–1.84e-03	4.02e-03	2.88e-03	–3.97e-04
0.388	3.12e-07	1.01e-02	–2.24e-04	2.44e-03	2.18e-03	4.68e-04
0.392	1.95e-07	9.86e-03	1.51e-03	9.58e-04	1.59e-03	1.07e-03
0.396	5.86e-08	9.64e-03	3.13e-03	–2.37e-04	1.17e-03	1.30e-03
0.400	–2.48e-08	9.43e-03	4.40e-03	–1.02e-03	8.60e-04	1.08e-03
0.404	–3.03e-08	9.22e-03	5.16e-03	–1.34e-03	5.83e-04	4.43e-04
0.408	1.02e-07	9.02e-03	5.37e-03	–1.16e-03	2.87e-04	–4.57e-04
0.412	1.68e-07	8.83e-03	5.08e-03	–5.37e-04	-8.75e-05	–1.43e-03
0.416	1.93e-07	8.64e-03	4.41e-03	4.06e-04	–5.80e-04	–2.27e-03
0.420	1.20e-07	8.46e-03	3.49e-03	1.39e-03	–1.26e-03	–2.94e-03
0.424	3.01e-08	8.29e-03	2.45e-03	2.10e-03	–2.18e-03	–3.47e-03
0.428	5.52e-09	8.12e-03	1.40e-03	2.28e-03	–3.31e-03	–3.92e-03
0.432	2.95e-08	7.96e-03	4.39e-04	1.83e-03	–4.53e-03	–4.33e-03
0.436	1.05e-07	7.80e-03	–4.02e-04	8.46e-04	–5.62e-03	–4.64e-03
0.440	1.40e-07	7.65e-03	–1.11e-03	–4.79e-04	–6.34e-03	–4.79e-03
0.444	1.27e-07	7.51e-03	–1.71e-03	–1.86e-03	–6.51e-03	–4.72e-03
0.448	7.69e-08	7.37e-03	–2.18e-03	–2.95e-03	–6.01e-03	–4.34e-03
0.452	2.73e-08	7.23e-03	–2.53e-03	–3.49e-03	–4.88e-03	–3.66e-03
0.456	2.59e-08	7.10e-03	–2.75e-03	–3.31e-03	–3.20e-03	–2.68e-03
0.460	5.54e-08	6.97e-03	–2.83e-03	–2.57e-03	–1.24e-03	–1.56e-03
0.464	9.74e-08	6.85e-03	–2.80e-03	–1.60e-03	7.13e-04	–5.10e-04
0.468	1.11e-07	6.73e-03	–2.65e-03	–7.72e-04	2.36e-03	2.70e-04
0.472	8.93e-08	6.61e-03	–2.40e-03	–3.48e-04	3.50e-03	6.40e-04
0.476	5.48e-08	6.49e-03	–2.08e-03	–3.49e-04	4.12e-03	6.10e-04
0.480	3.08e-08	6.39e-03	–1.72e-03	–6.97e-04	4.26e-03	2.42e-04
0.484	3.87e-08	6.28e-03	–1.36e-03	–1.18e-03	4.05e-03	–3.37e-04
0.488	6.37e-08	6.17e-03	–1.02e-03	–1.52e-03	3.61e-03	–9.74e-04
0.492	8.60e-08	6.07e-03	–7.22e-04	–1.45e-03	3.03e-03	–1.52e-03
0.496	8.68e-08	5.98e-03	–5.08e-04	–7.85e-04	2.45e-03	–1.85e-03
0.500	6.64e-08	5.88e-03	–4.43e-04	4.01e-04	1.89e-03	–1.94e-03
0.504	4.41e-08	5.79e-03	–6.03e-04	1.84e-03	1.38e-03	–1.81e-03
0.508	3.47e-08	5.70e-03	–1.02e-03	3.19e-03	9.06e-04	–1.54e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.512	4.54e-08	5.61e-03	–1.69e-03	4.14e-03	4.56e-04	–1.20e-03
0.516	6.35e-08	5.52e-03	–2.55e-03	4.57e-03	6.45e-05	–7.70e-04
0.520	7.41e-08	5.44e-03	–3.47e-03	4.40e-03	–2.43e-04	–2.64e-04
0.524	6.88e-08	5.36e-03	–4.30e-03	3.69e-03	–4.49e-04	3.11e-04
0.528	5.25e-08	5.28e-03	–4.86e-03	2.59e-03	–5.97e-04	9.07e-04
0.532	3.91e-08	5.20e-03	–4.98e-03	1.30e-03	–7.31e-04	1.46e-03
0.536	3.76e-08	5.13e-03	–4.57e-03	4.15e-05	–8.65e-04	1.90e-03
0.540	4.78e-08	5.05e-03	–3.67e-03	–1.04e-03	–9.88e-04	2.14e-03
0.544	5.97e-08	4.98e-03	–2.47e-03	–1.87e-03	–1.04e-03	2.11e-03
0.548	6.32e-08	4.91e-03	–1.16e-03	–2.42e-03	–9.79e-04	1.74e-03
0.552	5.59e-08	4.84e-03	4.24e-05	–2.70e-03	–7.35e-04	1.07e-03
0.556	4.40e-08	4.78e-03	9.93e-04	–2.70e-03	–2.60e-04	2.15e-04
0.560	3.68e-08	4.71e-03	1.60e-03	–2.43e-03	4.47e-04	–6.81e-04
0.564	3.90e-08	4.65e-03	1.85e-03	–1.93e-03	1.33e-03	–1.46e-03
0.568	4.74e-08	4.59e-03	1.86e-03	–1.22e-03	2.25e-03	–2.02e-03
0.572	5.44e-08	4.53e-03	1.78e-03	–3.47e-04	3.03e-03	–2.28e-03
0.576	5.40e-08	4.47e-03	1.74e-03	6.36e-04	3.49e-03	–2.22e-03
0.580	4.68e-08	4.41e-03	1.79e-03	1.66e-03	3.55e-03	–1.86e-03
0.584	3.86e-08	4.36e-03	1.86e-03	2.66e-03	3.17e-03	–1.27e-03
0.588	3.55e-08	4.30e-03	1.85e-03	3.54e-03	2.41e-03	–5.17e-04
0.592	3.92e-08	4.25e-03	1.67e-03	4.23e-03	1.41e-03	2.65e-04
0.596	4.55e-08	4.19e-03	1.23e-03	4.64e-03	3.37e-04	9.51e-04
0.600	4.89e-08	4.14e-03	5.18e-04	4.74e-03	-6.03e-04	1.45e-03
0.604	4.65e-08	4.09e-03	–4.25e-04	4.50e-03	–1.23e-03	1.72e-03
0.608	4.03e-08	4.04e-03	–1.43e-03	3.96e-03	–1.42e-03	1.79e-03
0.612	3.52e-08	3.99e-03	–2.30e-03	3.21e-03	–1.13e-03	1.73e-03
0.616	3.46e-08	3.95e-03	–2.85e-03	2.33e-03	–4.11e-04	1.62e-03
0.620	3.84e-08	3.90e-03	–2.96e-03	1.44e-03	6.15e-04	1.56e-03
0.624	4.26e-08	3.86e-03	–2.66e-03	6.40e-04	1.76e-03	1.61e-03
0.628	4.37e-08	3.81e-03	–2.01e-03	1.25e-05	2.81e-03	1.78e-03
0.632	4.06e-08	3.77e-03	–1.16e-03	–4.14e-04	3.60e-03	2.01e-03
0.636	3.58e-08	3.72e-03	–2.62e-04	–6.60e-04	4.00e-03	2.11e-03
0.640	3.29e-08	3.68e-03	5.11e-04	–7.79e-04	3.95e-03	1.94e-03

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.644	3.37e-08	3.64e-03	1.04e-03	–8.48e-04	3.47e-03	1.38e-03
0.648	3.69e-08	3.60e-03	1.32e-03	–9.56e-04	2.68e-03	4.76e-04
0.652	3.95e-08	3.56e-03	1.38e-03	–1.17e-03	1.71e-03	–6.44e-04
0.656	3.91e-08	3.52e-03	1.32e-03	–1.52e-03	7.06e-04	–1.80e-03
0.660	3.60e-08	3.48e-03	1.24e-03	–1.97e-03	–2.19e-04	–2.78e-03
0.664	3.25e-08	3.45e-03	1.22e-03	–2.47e-03	–1.02e-03	–3.39e-03
0.668	3.12e-08	3.41e-03	1.34e-03	–2.93e-03	–1.66e-03	–3.51e-03
0.672	3.26e-08	3.38e-03	1.58e-03	–3.22e-03	–2.14e-03	–3.12e-03
0.676	3.51e-08	3.34e-03	1.92e-03	–3.27e-03	–2.45e-03	–2.36e-03
0.680	3.64e-08	3.31e-03	2.26e-03	–3.01e-03	–2.58e-03	–1.40e-03
0.684	3.52e-08	3.27e-03	2.53e-03	–2.48e-03	–2.54e-03	–4.72e-04
0.688	3.24e-08	3.24e-03	2.67e-03	–1.77e-03	–2.30e-03	2.96e-04
0.692	3.01e-08	3.21e-03	2.66e-03	–1.04e-03	–1.85e-03	8.20e-04
0.696	2.98e-08	3.17e-03	2.47e-03	–4.69e-04	–1.20e-03	1.07e-03
0.700	3.13e-08	3.14e-03	2.17e-03	–1.76e-04	–4.09e-04	1.10e-03
0.704	3.31e-08	3.11e-03	1.78e-03	–2.25e-04	4.27e-04	9.85e-04
0.708	3.34e-08	3.08e-03	1.38e-03	–6.12e-04	1.21e-03	8.49e-04
0.712	3.19e-08	3.05e-03	9.74e-04	–1.24e-03	1.87e-03	7.97e-04
0.716	2.96e-08	3.02e-03	5.40e-04	–1.94e-03	2.35e-03	8.91e-04
0.720	2.83e-08	2.99e-03	4.50e-05	–2.52e-03	2.66e-03	1.15e-03
0.724	2.86e-08	2.96e-03	–5.39e-04	–2.82e-03	2.80e-03	1.56e-03
0.728	2.99e-08	2.94e-03	–1.21e-03	–2.76e-03	2.82e-03	2.06e-03
0.732	3.10e-08	2.91e-03	–1.93e-03	–2.34e-03	2.78e-03	2.56e-03
0.736	3.07e-08	2.88e-03	–2.63e-03	–1.64e-03	2.70e-03	2.99e-03
0.740	2.91e-08	2.86e-03	–3.19e-03	–8.03e-04	2.59e-03	3.27e-03
0.744	2.75e-08	2.83e-03	–3.49e-03	2.08e-05	2.40e-03	3.36e-03
0.748	2.68e-08	2.80e-03	–3.41e-03	6.61e-04	2.08e-03	3.25e-03
0.752	2.74e-08	2.78e-03	–2.90e-03	9.96e-04	1.62e-03	2.96e-03
0.756	2.85e-08	2.75e-03	–1.98e-03	9.72e-04	1.01e-03	2.54e-03
0.760	2.89e-08	2.73e-03	–7.19e-04	6.06e-04	3.03e-04	2.04e-03
0.764	2.83e-08	2.71e-03	7.27e-04	–1.29e-05	–4.51e-04	1.55e-03
0.768	2.69e-08	2.68e-03	2.19e-03	–7.52e-04	–1.17e-03	1.09e-03
0.772	2.57e-08	2.66e-03	3.49e-03	–1.45e-03	–1.76e-03	6.97e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.776	2.55e-08	2.64e-03	4.45e-03	–1.95e-03	–2.16e-03	3.84e-04
0.780	2.62e-08	2.61e-03	4.96e-03	–2.13e-03	–2.35e-03	1.50e-04
0.784	2.70e-08	2.59e-03	4.94e-03	–1.91e-03	–2.33e-03	–9.21e-06
0.788	2.70e-08	2.57e-03	4.41e-03	–1.30e-03	–2.16e-03	–1.09e-04
0.792	2.62e-08	2.55e-03	3.43e-03	–3.53e-04	–1.88e-03	–1.67e-04
0.796	2.50e-08	2.53e-03	2.14e-03	7.94e-04	–1.52e-03	–1.97e-04
0.800	2.43e-08	2.51e-03	6.97e-04	1.99e-03	–1.11e-03	–2.12e-04
0.804	2.44e-08	2.48e-03	–7.29e-04	3.07e-03	–6.76e-04	–2.16e-04
0.808	2.50e-08	2.46e-03	–1.98e-03	3.92e-03	–2.42e-04	–2.11e-04
0.812	2.55e-08	2.44e-03	–2.95e-03	4.47e-03	1.71e-04	–1.93e-04
0.816	2.52e-08	2.43e-03	–3.56e-03	4.69e-03	5.47e-04	–1.58e-04
0.820	2.44e-08	2.41e-03	–3.79e-03	4.59e-03	8.49e-04	–1.06e-04
0.824	2.35e-08	2.39e-03	–3.68e-03	4.24e-03	1.04e-03	–4.15e-05
0.828	2.31e-08	2.37e-03	–3.29e-03	3.71e-03	1.09e-03	3.17e-05
0.832	2.34e-08	2.35e-03	–2.72e-03	3.10e-03	9.78e-04	1.09e-04
0.836	2.38e-08	2.33e-03	–2.02e-03	2.46e-03	7.26e-04	1.89e-04
0.840	2.40e-08	2.31e-03	–1.28e-03	1.85e-03	3.61e-04	2.70e-04
0.844	2.36e-08	2.29e-03	–5.54e-04	1.30e-03	–7.48e-05	3.50e-04
0.848	2.29e-08	2.28e-03	9.66e-05	8.67e-04	–5.29e-04	4.35e-04
0.852	2.22e-08	2.26e-03	6.28e-04	5.63e-04	–9.51e-04	5.28e-04
0.856	2.21e-08	2.24e-03	1.02e-03	3.91e-04	–1.30e-03	6.25e-04
0.860	2.24e-08	2.23e-03	1.26e-03	3.27e-04	–1.54e-03	7.05e-04
0.864	2.27e-08	2.21e-03	1.35e-03	3.18e-04	–1.67e-03	7.38e-04
0.868	2.27e-08	2.19e-03	1.32e-03	3.13e-04	–1.71e-03	7.00e-04
0.872	2.22e-08	2.18e-03	1.20e-03	2.49e-04	–1.65e-03	5.79e-04
0.876	2.15e-08	2.16e-03	1.06e-03	6.50e-05	–1.54e-03	3.86e-04
0.880	2.11e-08	2.15e-03	9.49e-04	–2.75e-04	–1.39e-03	1.42e-04
0.884	2.11e-08	2.13e-03	9.05e-04	–7.77e-04	–1.23e-03	–1.19e-04
0.888	2.14e-08	2.11e-03	9.32e-04	–1.40e-03	–1.08e-03	–3.50e-04
0.892	2.16e-08	2.10e-03	1.01e-03	–2.06e-03	–9.51e-04	–5.12e-04
0.896	2.14e-08	2.08e-03	1.10e-03	–2.69e-03	–8.58e-04	–5.74e-04
0.900	2.09e-08	2.07e-03	1.17e-03	–3.22e-03	–8.19e-04	–5.37e-04
0.904	2.04e-08	2.06e-03	1.17e-03	–3.60e-03	–8.53e-04	–4.30e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
0.908	2.02e-08	2.04e-03	1.07e-03	–3.81e-03	–9.70e-04	–2.86e-04
0.912	2.02e-08	2.03e-03	8.84e-04	–3.86e-03	–1.17e-03	–1.38e-04
0.916	2.05e-08	2.01e-03	6.43e-04	–3.76e-03	–1.43e-03	–3.73e-06
0.920	2.05e-08	2.00e-03	4.00e-04	–3.57e-03	–1.72e-03	1.07e-04
0.924	2.03e-08	1.99e-03	2.04e-04	–3.32e-03	–2.00e-03	1.97e-04
0.928	1.98e-08	1.97e-03	8.04e-05	–3.05e-03	–2.21e-03	2.83e-04
0.932	1.94e-08	1.96e-03	3.54e-05	–2.77e-03	–2.31e-03	3.84e-04
0.936	1.93e-08	1.95e-03	6.11e-05	–2.49e-03	–2.25e-03	5.12e-04
0.940	1.94e-08	1.93e-03	1.19e-04	–2.19e-03	–2.02e-03	6.60e-04
0.944	1.96e-08	1.92e-03	1.68e-04	–1.87e-03	–1.61e-03	7.99e-04
0.948	1.95e-08	1.91e-03	1.69e-04	–1.51e-03	–1.04e-03	8.98e-04
0.952	1.92e-08	1.90e-03	1.12e-04	–1.11e-03	–3.35e-04	9.23e-04
0.956	1.88e-08	1.88e-03	3.20e-05	–6.75e-04	4.63e-04	8.56e-04
0.960	1.86e-08	1.87e-03	–3.29e-05	–2.21e-04	1.31e-03	6.88e-04
0.964	1.85e-08	1.86e-03	–3.97e-05	2.28e-04	2.16e-03	4.27e-04
0.968	1.86e-08	1.85e-03	3.82e-05	6.47e-04	2.94e-03	1.05e-04
0.972	1.87e-08	1.84e-03	2.03e-04	1.01e-03	3.58e-03	–2.35e-04
0.976	1.86e-08	1.82e-03	4.37e-04	1.30e-03	4.03e-03	–5.42e-04
0.980	1.83e-08	1.81e-03	6.79e-04	1.50e-03	4.23e-03	–7.76e-04
0.984	1.80e-08	1.80e-03	8.54e-04	1.61e-03	4.14e-03	–9.10e-04
0.988	1.78e-08	1.79e-03	8.92e-04	1.65e-03	3.77e-03	–9.27e-04
0.992	1.78e-08	1.78e-03	7.59e-04	1.61e-03	3.13e-03	–8.27e-04
0.996	1.79e-08	1.77e-03	4.78e-04	1.51e-03	2.31e-03	–6.23e-04
1.000	1.79e-08	1.76e-03	9.92e-05	1.35e-03	1.38e-03	–3.43e-04
1.004	1.77e-08	1.75e-03	–3.03e-04	1.14e-03	4.42e-04	–2.81e-05
1.008	1.74e-08	1.74e-03	–6.46e-04	8.71e-04	–4.26e-04	2.80e-04
1.012	1.72e-08	1.73e-03	–8.64e-04	5.31e-04	–1.16e-03	5.35e-04
1.016	1.71e-08	1.71e-03	–9.09e-04	1.17e-04	–1.71e-03	6.95e-04
1.020	1.71e-08	1.70e-03	–7.85e-04	–3.71e-04	–2.06e-03	7.20e-04
1.024	1.72e-08	1.69e-03	–5.39e-04	–9.22e-04	–2.21e-03	5.83e-04
1.028	1.71e-08	1.68e-03	–2.39e-04	–1.51e-03	–2.20e-03	2.80e-04
1.032	1.69e-08	1.67e-03	4.62e-05	–2.08e-03	–2.04e-03	–1.70e-04
1.036	1.67e-08	1.66e-03	2.68e-04	–2.58e-03	–1.78e-03	–7.21e-04

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
1.040	1.65e-08	1.66e-03	3.93e-04	–2.92e-03	–1.45e-03	–1.31e-03
1.044	1.65e-08	1.65e-03	4.08e-04	–3.07e-03	–1.08e-03	–1.86e-03
1.048	1.65e-08	1.64e-03	3.24e-04	–2.97e-03	–6.97e-04	–2.29e-03
1.052	1.65e-08	1.63e-03	1.64e-04	-2.62e-03	-3.38e-04	-2.53e-03
1.056	1.64e-08	1.62e-03	–2.93e-05	–2.04e-03	–2.07e-05	–2.54e-03
1.060	1.62e-08	1.61e-03	–2.24e-04	–1.30e-03	2.39e-04	–2.32e-03
1.064	1.60e-08	1.60e-03	–3.91e-04	–4.72e-04	4.34e-04	–1.91e-03
1.068	1.59e-08	1.59e-03	–5.13e-04	3.49e-04	5.60e-04	–1.37e-03
1.072	1.59e-08	1.58e-03	–5.79e-04	1.08e-03	6.21e-04	–7.75e-04
1.076	1.59e-08	1.57e-03	–5.84e-04	1.66e-03	6.27e-04	–2.13e-04
1.080	1.59e-08	1.56e-03	–5.35e-04	2.04e-03	5.90e-04	2.42e-04
1.084	1.57e-08	1.56e-03	–4.46e-04	2.24e-03	5.24e-04	5.43e-04
1.088	1.55e-08	1.55e-03	–3.40e-04	2.26e-03	4.42e-04	6.80e-04
1.092	1.54e-08	1.54e-03	–2.40e-04	2.14e-03	3.58e-04	6.70e-04
1.096	1.53e-08	1.53e-03	–1.64e-04	1.95e-03	2.82e-04	5.53e-04
1.100	1.53e-08	1.52e-03	–1.21e-04	1.72e-03	2.23e-04	3.73e-04
1.104	1.53e-08	1.51e-03	–1.09e-04	1.48e-03	1.90e-04	1.72e-04
1.108	1.53e-08	1.51e-03	–1.19e-04	1.27e-03	1.85e-04	–1.10e-05
1.112	1.51e-08	1.50e-03	–1.38e-04	1.09e-03	2.03e-04	–1.51e-04
1.116	1.49e-08	1.49e-03	–1.54e-04	9.49e-04	2.33e-04	–2.31e-04
1.120	1.48e-08	1.48e-03	–1.57e-04	8.36e-04	2.60e-04	–2.52e-04
1.124	1.48e-08	1.47e-03	–1.42e-04	7.46e-04	2.72e-04	–2.18e-04
1.128	1.48e-08	1.47e-03	–1.14e-04	6.77e-04	2.53e-04	–1.33e-04
1.132	1.48e-08	1.46e-03	–8.40e-05	6.30e-04	1.95e-04	–6.35e-06
1.136	1.47e-08	1.45e-03	–6.31e-05	6.05e-04	9.72e-05	1.50e-04
1.140	1.45e-08	1.44e-03	–5.84e-05	5.99e-04	–2.78e-05	3.12e-04
1.144	1.44e-08	1.44e-03	–7.04e-05	6.01e-04	–1.58e-04	4.51e-04
1.148	1.43e-08	1.43e-03	–9.63e-05	6.02e-04	–.69e-04	5.45e-04
1.152	1.43e-08	1.42e-03	–1.29e-04	5.87e-04	–3.41e-04	5.76e-04
1.156	1.43e-08	1.42e-03	–1.60e-04	5.43e-04	–3.62e-04	5.36e-04
1.160	1.42e-08	1.41e-03	–1.81e-04	4.58e-04	–3.29e-04	4.30e-04
1.164	1.41e-08	1.40e-03	–1.83e-04	3.30e-04	–2.48e-04	2.72e-04
1.168	1.40e-08	1.39e-03	–1.65e-04	1.72e-04	–1.35e-04	9.19e-05

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Table 32–11—Coefficients for worst-case channel and T2 Alien NEXT model *(continued)*

Time (μs)	Cable 0 m	Cable 100 m	Alien NEXT 1	Alien NEXT 2	Alien NEXT 3	Alien NEXT 4
1.172	1.39e-08	1.39e-03	–1.28e-04	4.95e-06	–1.13e-05	–7.86e-05
1.176	1.38e-08	1.38e-03	–7.75e-05	–1.48e-04	1.02e-04	–2.10e-04
1.180	1.38e-08	1.37e-03	–1.90e-05	–2.62e-04	1.90e-04	–2.83e-04
1.184	1.38e-08	1.37e-03	4.03e-05	-3.19e-04	2.48e-04	-2.93e-04
1.188	1.37e-08	1.36e-03	9.40e-05	–3.07e-04	2.73e-04	–2.43e-04
1.192	1.36e-08	1.35e-03	1.37e-04	–2.28e-04	2.68e-04	–1.50e-04
1.196	1.35e-08	1.35e-03	1.66e-04	–9.21e-05	2.37e-04	–3.64e-05
1.200	1.34e-08	1.34e-03	1.80e-04	7.95e-05	1.86e-04	7.45e-05
1.204	1.34e-08	1.34e-03	1.79e-04	2.63e-04	1.22e-04	1.62e-04
1.208	1.34e-08	1.33e-03	1.62e-04	4.36e-04	5.03e-05	2.17e-04
1.212	1.33e-08	1.32e-03	1.27e-04	5.81e-04	–2.48e-05	2.37e-04
1.216	1.33e-08	1.32e-03	7.69e-05	6.83e-04	–9.88e-05	2.28e-04
1.220	1.32e-08	1.31e-03	1.24e-05	7.35e-04	–1.66e-04	2.01e-04
1.224	1.31e-08	1.30e-03	–6.03e-05	7.34e-04	–2.22e-04	1.66e-04
1.228	1.30e-08	1.30e-03	–1.36e-04	6.87e-04	–2.61e-04	1.35e-04
1.232	1.29e-08	1.29e-03	–2.14e-04	6.00e-04	–2.84e-04	1.13e-04
1.236	1.29e-08	1.29e-03	–2.89e-04	4.86e-04	–2.93e-04	1.02e-04
1.240	1.29e-08	1.28e-03	–3.66e-04	3.57e-04	–2.97e-04	9.58e-05
1.244	1.29e-08	1.27e-03	–4.41e-04	2.30e-04	–3.00e-04	9.07e-05
1.248	1.29e-08	1.27e-03	–5.17e-04	1.15e-04	–3.10e-04	7.92e-05

32.6.1.3.2 Receiver test mode

To facilitate the testing of the receiver in the presence of synchronous 100BASE-T2 alien NEXT, a special receiver test mode shall be required to allow for receiver alien NEXT tolerance and jitter testing. For a PHY with an MII, this mode shall be enabled by setting bit 9.13 (MASTER-SLAVE Control register) of the MII management register set to a 1. A PHY without an MII shall provide a means to enable this test mode. This mode shall not be overridden except by clearing bit 9.13 or resetting the PHY.

When the receive test mode is enabled, the receiver shall configure itself in SLAVE mode, continually attempt to bring its receiver up until successful receiver operation is achieved and transmit symbols in idle mode. For a PHY with an MII, when the receiver is properly detecting the received data (loc_rcvr_status=OK), it shall set bit 10.13 of the MII management register to 1 and reset the error count in bits 10.0 through 10.7 (MSB) to zero. The error count shall be incremented for every symbol error detected in the received idle sequence (where rem_rcvr_status is assumed to be OK). Upon loss of proper data reception, the receiver shall clear bit 10.13. A PHY without an MII shall provide a means to realize this function. The vendor shall provide a means to enable this mode for conformance testing.

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32.6.1.3.3 Receiver differential input signals

Differential signals received on the receive inputs that were transmitted within the specifications given in 32.6.1.2, and have then passed through a link as defined in 32.7, shall be translated into one of the PMA_UNITDATA.indication messages with an symbol error ratio less than 10^{-10} and sent to the PCS after link bring-up.

Performance shall be tested in at least two configurations: using a 100 m link segment conformant to 32.7 and with a link segment less than 1 m in length between transmitter and receiver.

32.6.1.3.4 Receiver Alien NEXT tolerance

Differential signals received from the test channel defined in 32.6.1.3.1 shall be detected with a symbol error ratio less than 10^{-8} when the PHY is in receiver test mode for the following combinations of channel and worst-case alien NEXT responses, as shown in Table 32-13.

Table 32-13—Receiver Alien NEXT test cases

Case	Cable channels	NEXT Channels			
		A1	A2	B1	B2
1	0 m	Alien NEXT 1	Alien NEXT 3	Alien NEXT 4	Alien NEXT 2
2	0 m	Alien NEXT 1	Alien NEXT 4	Alien NEXT 3	Alien NEXT 2
3	100 m	Alien NEXT 1	Alien NEXT 3	Alien NEXT 4	Alien NEXT 2
4	100 m	Alien NEXT 1	Alien NEXT 4	Alien NEXT 3	Alien NEXT 2

NOTE—Implementers will find it practically impossible to meet the requirements of this subclause without using some form of adaptive equalization and cyclostationary interference suppression.

32.6.1.3.5 Receiver timing jitter

For the test channels described below, the peak-to-peak value of RX_CLK zero-crossing jitter shall be less than 1.3 ns after the receiver is properly receiving the data and has set bit 9.13 of the MII management register set to 1. When the jitter waveform on RX_CLK is filtered by a high pass filter having the transfer function below,[15] the peak-to-peak value of the resulting filtered timing jitter shall be less than 0.8 ns.

Test channels:

Channels 1–4 are the test channels described in 32.6.1.3.1 with the four combinations of worst-case channel and alien NEXT responses tabulated in 32.6.1.3.4.

Channels 5–6 are the test channels described in 32.6.1.3.1 with the combinations of worst-case channel and alien NEXT responses tabulated in cases 1 and 2 of 32.6.1.3.4 plus the addition of 100 m of Category 3 compliant cable between the test channel fixture and the PHY under test.

$$H_{\text{jitterfilter}}(f) = \frac{jf}{jf + 1000} \qquad f \text{ in Hz}$$

The RX_CLK of the MII shall be made available for this test. A PHY without an MII shall provide an equivalent clock.

[15] "j" denotes the positive square root of –1.

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32.6.1.3.6 Common-mode noise rejection

While receiving packets from a compliant 100BASE-T2 transmitter, connected to all MDI pins, a receiver shall send the proper PMA_UNITDATA.indication messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 32.6.1.3.3 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 32–21). E_{cm} shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%-80%), connected to each of the pairs (BI_DA+, BI_DA-) and (BI_DB+, BI_DB-).

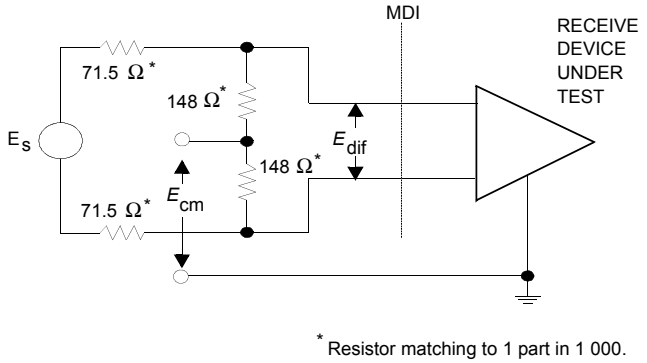


Figure 32–21—Receiver common-mode noise rejection test circuit

32.6.1.3.7 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a 5-level symbol rate within the range 25.000 MHz ± 0.01%.

32.6.1.4 MDI Specifications

32.6.1.4.1 MDI differential impedance

The differential impedance as measured at the MDI for each transmit/receive channel shall be such that any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω is at least 17 dB below the incident signal over the frequency range 2.0 MHz to 6.5 MHz and at least 12.9–20 $\log_{10}(f/10)$ dB over the frequency range 6.5 MHz to 25 MHz (f in MHz). This return loss shall be maintained at all times when the PHY is transmitting data.

32.6.1.4.2 MDI impedance balance

Over the frequency range 2.0 MHz to 25.0 MHz, the common-mode to differential-mode impedance balance of each channel of the MDI shall exceed

$$29 - 17\log\left(\frac{f}{10}\right) \text{ dB}$$

where f is the frequency in MHz when the transmitter is transmitting idle mode data (transmit test mode 3).

The balance is defined as

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$$20\log\left(\frac{E_{cm}}{E_{dif}}\right)$$

where E_{cm} is an externally applied sine wave voltage as shown in Figure 32–22 and E_{dif} is the resulting waveform due only to the applied sine wave and not the transmitted data.[16]

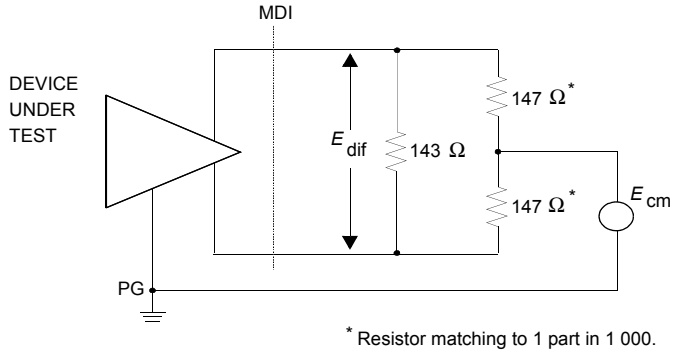


Figure 32–22—MDI impedance balance test circuit

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

32.6.1.4.3 MDI common-mode output voltage

The implementer should consider any applicable local, national, or international regulations. Driving balanced cable pairs with high-frequency common-mode voltages may cause radiated emissions that may result in interference to other equipment. FCC conducted and radiated emissions tests may require that the magnitude of the total common-mode output voltage, E_{cm_out}, on any transmit circuit, when measured as shown in Figure 32–23, be less than a few millivolts when transmitting data.

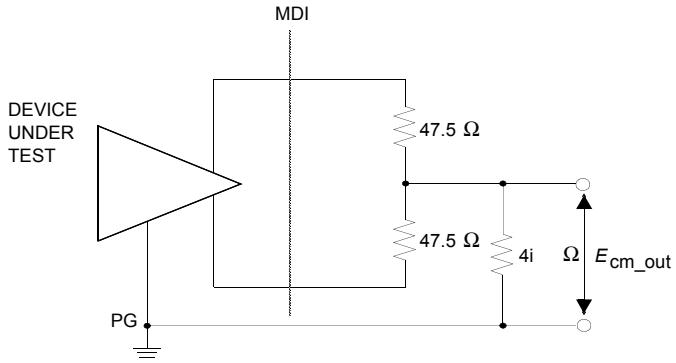


Figure 32–23—Common-mode output voltage test circuit

NOTE—The balance of the test equipment (such as the matching of the test resistors) must be insignificant relative to the balance requirements.

[16]Triggered averaging can be used to separate the component due to the applied common-mode sine wave from the transmitted data component.

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32.6.1.4.4 MDI fault tolerance

Transmitters and receivers shall withstand without damage the application of short circuits across any MDI port for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters shall withstand without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity (as indicated in Figure 32–24). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.

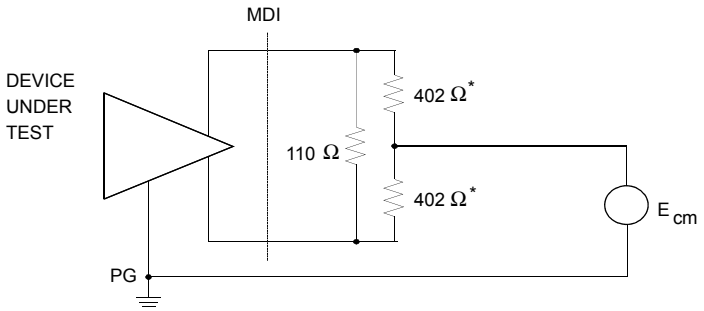


Figure 32–24—MDI fault tolerance test circuit

32.6.2 Power consumption

After 100 ms following PowerOn, the current drawn by the PHY shall not exceed 1.0 A when powered through the MII.

The PHY shall be capable of operating from all voltage sources allowed by Clause 22, including those current limited to 1.0 A, as supplied by the DTE or repeater through the resistance of all permissible MII cabling.

The PHY shall not introduce extraneous signals on the MII control circuits during normal power-up and power-down.

While in power-down mode, the PHY is not required to meet any of the 100BASE-T2 performance requirements.

32.7 Link segment characteristics

100BASE-T2 employs a dual duplex transmission system, i.e., two full duplex channels are used simultaneously to transmit data. The use of the term *link segment* in this clause refers to two duplex channels and the specifications for a link segment apply individually to each of the two duplex channels. Furthermore, the term duplex channel will be used to refer a single channel of the dual duplex link segment.

100BASE-T2 is designed to allow use of the pairs of the cabling other than the two used for the full duplex channels of the 100BASE-T2 service. Services supported for use in the other pairs are as follows:

a) 100BASE-T2
b) 10BASE-T
c) Digital phone services compliant with the ITU-T Recommendation I.430 and ANSI T1.605 and T1.601

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32.7.1 Cabling

Cabling and installation practices generally suitable for use with this standard appear in ISO/IEC 11801. Exceptions, notes, and additional requirements are as listed below.

a) 100BASE-T2 uses a star topology. Balanced cabling is used to connect PHY entities.
b) 100BASE-T2 is an ISO 11801 class C application, with additional installation requirements and transmission parameters specified in 32.7.2–32.7.4. The width of the PAM5 × 5 transmit spectrum is approximately 25 MHz (as shown in Figure 32–19). The aggregate data rate for two pairs using PAM5 × 5 coding is 100 Mb/s.
c) 100BASE-T2 shall use 2 pairs of balanced cabling, Category 3 or better, with a nominal characteristic impedance of 100 Ω.
d) When using Category 3 cabling for the link segment, Clause 32 recommends, but does not require, the use of Category 4 or better connecting hardware, patch cords and jumpers. The use of Category 4 or better connecting hardware increases the link segment composite NEXT loss, composite ELFEXT loss and reduces the link segment insertion loss. This lowers the link segment crosstalk noise which in turn decreases the probability of errors.
e) The use of shielding is outside the scope of this standard.
f) The use of other cabling systems is discussed in Annex 32A.

32.7.2 Link transmission parameters

Unless otherwise specified, link segment testing shall be conducted using source and load impedances of 100 Ω.

The tolerance on the poles of the test filter used in this clause shall be ± 1%.

32.7.2.1 Insertion loss

The insertion loss of a link segment shall be no more than 14.6 dB at all frequencies between 2 and 16 MHz. This consists of the attenuation of the balanced cabling pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the link segment. The insertion loss specification shall be met when the link segment is terminated in source and load impedances that satisfy 32.6.1.4.1.

NOTE—The loss of PVC-insulated cabling exhibits significant temperature dependence. At temperatures greater than 40 ^{o}C, it may be necessary to use a less temperature-dependent cabling, such as many Fluorinated Ethylene Propylene (FEP), Polytetrafluoroethylene (PTFE), or Perfluoroalkoxy (PFA) plenum-rated cabling.

32.7.2.2 Differential characteristic impedance

The cable used in the links shall meet the requirements for characteristic impedance specified in ISO/IEC 11801. Connecting hardware shall meet the return loss requirements for connecting hardware specified in ISO/IEC 11801.

32.7.2.3 Coupling parameters

In order to limit the noise coupled into a duplex channel from an adjacent duplex channel, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. In addition, since two dual-duplex connections may co-exist in a 4-pair cabling and a receiver on a duplex channel will be disturbed by crosstalk from one to three other duplex (or simplex) channels, Multiple-Disturber NEXT loss and Multiple-Disturber ELFEXT loss are also specified. When a 10BASE-T service is used within the same cabling, a restriction on the allowable NEXT loss to Insertion Loss (NIR) of the cabling is required and is specified in 32.7.2.3.5.

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32.7.2.3.1 Differential near-end crosstalk (NEXT) loss

The differential Near-End Crosstalk (NEXT) loss between the two duplex channels of a link segment is specified in order to limit the crosstalk noise at the near end of a link segment to meet the symbol error ratio objective specified in 32.1 and the noise specifications of 32.7.3. The NEXT loss between the two duplex channels of a link segment shall be at least $19.3 - 16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2 MHz to 16 MHz.

32.7.2.3.2 Multiple-disturber NEXT (MDNEXT) loss

Since two dual duplex applications (connections) may exist in a 4-pair cabling system, a received signal may be disturbed by multiple alien NEXT signals. The MDNEXT loss between each link segment duplex channel and the two alien data carrying duplex channels shall be at least $19.0 - 16.6\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2.0 MHz to 16 MHz. MDNEXT is computed as the power sum of the individual NEXT losses. This specification is consistent with two disturbers, each with a NEXT loss of at least $22.0 - 16.6\log_{10}(f/16)$.

NOTE—Since the self NEXT noise from the other duplex channel of a connection can be cancelled using digital signal processing techniques whereas the alien NEXT noise from an alien connection can not be cancelled in the same fashion, the self NEXT noise is treated differently than the alien NEXT noise and is not included in the MDNEXT calculation.

32.7.2.3.3 Equal level far-end crosstalk loss (ELFEXT)

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk noise at the far end of a link segment to meet the symbol error ratio objective specified in 32.1 and the noise specifications of 32.7.3. Far-End Crosstalk (FEXT) noise is the crosstalk noise that appears at the far end of one of the duplex channels which is coupled from one of the duplex channels with the noise source (transmitters) at the near end. ELFEXT loss is the ratio of the data signal to FEXT noise at the far end output of a duplex channel. To limit the FEXT noise from an adjacent duplex channel, the ELFEXT loss between each duplex channel shall be greater than $20.9 - 20\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2 MHz to16 MHz. ELFEXT loss at frequency f and distance l is defined as

$$ELFEXT\_Loss(f,l) = 20\log_{10}(V\text{pds}/V\text{pcn}) - SLS\_Loss(\text{dB})$$

where Vpds = peak voltage of disturbing signal (near-end transmitter), Vpcn = peak crosstalk noise at far-end of disturbed channel, and SLS_Loss = insertion loss of the disturbing channel.

32.7.2.3.4 Multiple-disturber ELFEXT (MDELFEXT) loss

Since two duplex channels are used to transfer data between PHYs and two connections can exist in a 4-pair cabling, the FEXT noise that is coupled into a data carrying duplex channel is from one to three disturbers. The MDELFEXT loss between a duplex channel and the other data carrying duplex channels shall be greater than $19.9 - 20\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2 MHz to 16 MHz.This specification is consistent with three disturbers, one with a FEXT loss of at least $20.9 - 20\log_{10}(f/16)$ and two with a FEXT loss of at least $27.0 - 20\log_{10}(f/16)$.

MDELNEXT is computed as the power sum of the individual FEXT losses.

32.7.2.3.5 10BASE-T NEXT loss to insertion loss ratio requirement

The objective of this specification is to support the coexistence of a 100BASE-T2 link segment and a 10BASE-T link segment in a 4-pair cable. When a 100BASE-T2 link segment operates in the same 4-pair cable with a 10BASE-T link segment, each 100BASE-T2 duplex channel will receive alien NEXT noise signals from the 10BASE-T link segment. To ensure reliable operation, a minimum signal-to-noise ratio must

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be maintained. This minimum signal-to-noise ratio is assured by meeting the following NEXT loss to insertion loss ratio (NIR).

NIR is defined by the following equation:

$$NIR\ (\text{dB}) = (AdjustedNEXTLoss - InsertionLoss_{6\ \text{MHz}})$$

where $InsertionLoss_{6\ \text{MHz}}$ is the maximum of the insertion loss at 6 MHz of the two duplex channels of the 100BASE-T2 link segment and *AdjustedNEXTLoss* is determined by the following algorithm:

AdjustedNEXTLoss Algorithm

Step 1. Measure the NEXT loss as a function of frequency over the range 1 MHz to 16 MHz for each of the six pair combinations between the four pairs of the cabling. The maximum spacing in frequency of the samples shall be 250 kHz.

Step 2. Add $16.6\log_{10}(f/16)$ to the NEXT loss measurements (where f is frequency in MHz) to normalize the NEXT loss as a function of frequency.

Step 3. Determine the minimum value of the normalized NEXT loss across the frequency range over all pair combinations. The minimum value is the AdjustedNEXTLoss.

The NIR shall be greater than 19.4 dB.

32.7.2.4 Delay

Since 100BASE-T2 sends information over two duplex channels in parallel, the propagation delay of each channel and the difference in delay are specified to comply with network round-trip delay of the two channels and ensure proper decoding by receivers, respectively.

32.7.2.4.1 Maximum link delay

The propagation delay of a link segment shall not exceed 5.7 ns/m at all frequencies between 2 MHz and 25 MHz.

32.7.2.4.2 Difference in link delays

The difference in propagation delay, or skew, under all conditions, between the two duplex channels of a link segment shall not exceed 90 ns at all frequencies between 2 MHz and 25 MHz. It is a further functional requirement that, once installed, the skew between the duplex links due to environmental conditions shall not vary more than ± 20 ns, within the above requirement.

32.7.3 Noise

The noise level on the link segments shall be such that the cabling noise requirements which follow are met. The noise environment consists generally of a main contributor, self-induced and alien near-end crosstalk noise, and a lessor contributor, far-end crosstalk noise.

The noise environment for 100BASE-T2 can consist of the following elements:

a) Echo from the local transmitter on the same pair (duplex channel). Echo is caused by the hybrid used to achieve simultaneous bidirectional transmission of data in the T2 system and by impedance mismatches in the link segment. It is practically impossible to achieve robust performance without using echo cancellation to reduce this noise to a small residual. Echo cancellation is possible since the symbols transmitted from the disturbing local transmitter are available to the cancellation processor.

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b) Near-end crosstalk (NEXT) noise from the local transmitter on the other pair (duplex channel) of the link segment. This is often referred to as self NEXT noise since the source is from the same link segment. NEXT noise cancellation is typically used to reduce this noise to a small residual. NEXT noise cancellation is possible since the symbols transmitted from the disturbing local transmitter are available to the cancellation processor.

c) Far-end crosstalk (FEXT) noise from the remote transmitters on the other pair (duplex channel) of the link segment. This is often referred to as self FEXT noise since the source is from the same link segment. Self FEXT noise can not be cancelled in the same way as echo and self NEXT noise since the symbols from the remote transmitter are not immediately available; however, in the link configurations used for 100BASE-T2, self FEXT noise is much smaller than self NEXT noise and can generally be neglected.[17]

d) Noise from non-idealities in the duplex channels, transmitters and receivers; for example, DAC/ADC non-linearity, electrical noise (shot and thermal) and non-linear channel characteristics.

e) Noise from sources outside the cabling which couple into the link segment via electric and magnetic fields.

f) Noise from services in adjacent wire pairs in the same cable sheath. These services generate near- and far-end crosstalk and are often referred to as alien NEXT noise and alien FEXT noise since the sources are not from the link segment of the disturbed duplex channel. Since the transmitted symbols from an alien NEXT noise source are not available to the PHY of the disturbed duplex channel, it is not possible to cancel the alien NEXT noise as can be done for self NEXT noise. If the alien NEXT noise is from a 100BASE-T2 transceiver, a technique termed cyclostationary interference suppression can be used to suppress the alien NEXT noise. It will be practically impossible achieve reliable operation in the presence of alien NEXT noise meeting the limits of the specifications in subclause 32.6 without using some form of cyclostationary interference suppression. 10BASE-T can not be suppressed and therefore an additional constraint has been placed on the link (see subclause 32.7.2.3.5) to ensure adequate signal to noise levels for reliable performance. Digital phone services compliant with the ITU-T Recommendation I.430 and ANSI T1.605 and T1.601 also can not be suppressed but produce substantially smaller crosstalk than 10BASE-T and thus do not require any additional constraints on the link.

100BASE-T2 supports three types of service in adjacent pairs of the same cable: 100BASE-T2, 10BASE-T, and digital phone service compliant with the ISDN-BR U and S/T interfaces. Analog phone service is not supported since the noise generated during off-hook transitions and ringing source from older PBX equipment can cause bit errors to occur.

NOTE—Due to the use of noise cancellation, cyclostationary interference suppression and the use of adaptive equalization, there is no meaningful way to add up the noises at the input to the receiver into an overall noise level and simulation of a design is required to determine the contribution of each source to the final error at the symbol decision point.

32.7.3.1 Near-end crosstalk noise

The MDNEXT (Multiple-Disturber Near-End Crosstalk) noise on a duplex channel from an alien connection depends on the signal spectrum on the alien channels and the crosstalk between the alien channels and the disturbed channel.

The MDNEXT noise on each duplex link of a link segment shall not exceed 182 mVp.

This specification is compatible with the following assumptions:

[17]Additionally, FEXT noise may be suppressed to some degree via cyclostationary interference suppression; however, in the presence of alien NEXT noise, the equalizer will be primarily suppressing the alien NEXT noise.

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a) Two disturbing alien pairs with a NEXT loss greater than 22.0 dB at 16 MHz
b) All disturbers combined on a power sum basis

The MDNEXT noise is the noise measured at the output of a filter connected to the output of the near end of a disturbed link segment using maximum level 100BASE-T2 transmitters attached to the near end of an alien disturbing link segment. Each continuous transmit signal is generated by a transceiver in idle mode meeting the data scrambling and encoding rules in 32.3, e.g., a transmitter in transmit test mode 3.

32.7.3.2 Far-end crosstalk noise

The MDFEXT (Multiple-Disturber Far-End Crosstalk) noise on a duplex channel depends on the signal spectrum on the disturbing channels and the various crosstalk losses between those channels and the disturbed channel.

The MDFEXT noise on a link segment shall not exceed 54.4 mVp.

This specification is compatible with the following assumptions:

a) One disturbing pair with ELFEXT (Equal Level Far-End Crosstalk) loss greater than 20.9 dB at 16 MHz
b) Two additional disturbers with ELFEXT (Equal Level Far-End Crosstalk) loss greater than 27.0 dB at 16 MHz
c) All disturbers combined on a power sum basis

The MDFEXT noise is the noise measured at the output of a filter connected to the output of the far end of a disturbed link segment using maximum level 100BASE-T2 transmitters attached to the near end of the other duplex channel of the link segment and both duplex channels of an alien disturbing link segment. Each continuous transmit signal is generated by a transceiver in idle mode meeting the data scrambling and encoding rules in 32.3, e.g., a transmitter in transmit test mode 3.

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 23 MHz.

32.7.3.3 External coupled noise

Noise coupled from external sources, measured at the output of a filter connected to the output of the near end of a disturbed link segment shall not exceed 25 mV peak.[18]

The filter is a 5th order Butterworth filter with a 3 dB cutoff at 23 MHz.

32.7.4 Installation practice

32.7.4.1 Connector installation practices

The amount of untwisting in a pair as a result of termination to connecting hardware should be no greater than 25 mm (1.0 in.) for Category 3 cabling. This is the same value recommended in ISO/IEC 11801 for Category 4 connectors.

32.7.4.2 Restrictions on use of Category 3 cabling with more than four pairs

Jumper cabling, or horizontal runs, made from more than four pairs of Category 3 cabling shall not be used.

[18]This assumes the link has worst-case attenuation and alien NEXT and that the noise has the worst possible properties. In the absence of alien NEXT the tolerance to external noise sources is substantially increased. Tolerance to stationary noise such as continuous wave interference from AM radio can be substantially higher since the equalizer can notch out frequencies with poor signal-to-noise ratios. Tolerance to isolated impulse noise events is also typically much higher and dependent on the shape of the impulse.

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32.7.4.3 Restrictions on use of Category 5 cabling with up to 25 pairs

Cables made from up to 25 pairs of Category 5 cable are allowed. Such cables, if used, shall be limited in length to no more than 90 m total. The services in the cable shall be limited to any combination 100BASE-T2, 10BASE-T and digital phone services compliant with the ITU-T Recommendation I.430 and ANSI T1.605 and T1.601 interfaces up to a total of 12 services in the cable.

32.8 MDI specification

This subclause defines the MDI. The link topology requires a crossover function between PMAs. Implementation and location of this crossover are also defined in this subclause.

32.8.1 MDI connectors

Eight-pin connectors meeting the requirements of section 3 and Figures 1–4 of IEC 60603-7, Detail Specification for Connectors, 8-Way shall be used as the mechanical interface to the balanced cabling. The plug connector shall be used on the balanced cabling and the jack on the PHY. These connectors are depicted (for informational use only) in Figures 32–25 and 32–26. Table 32–14 shows the assignment of PMA signals to connector contacts for PHYs.

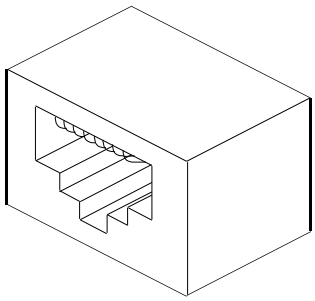


Figure 32–25—MDI connector

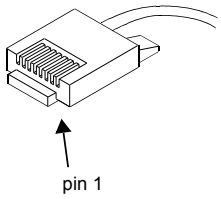


Figure 32–26—Balanced cabling connector

32.8.2 Crossover function

Although the crossover function is not required for successful operation of 100BASE-T2, it is a functional requirement that a crossover function be implemented in every link segment to support the operation of Auto-Negotiation. The crossover function connects the transmitters of one PHY to the receivers of the PHY at the other end of the link segment. Crossover functions may be implemented internally to a PHY or elsewhere in the link segment. For a PHY that does not implement the crossover function, the MDI labels in the last column of Table 32–14 refer to its own internal circuits (second column). For PHYs that do implement the internal crossover, the MDI labels in the last column of Table 32–14 refer to the internal circuits of the remote PHY of the link segment. Additionally, the MDI connector for a PHY that implements the crossover function shall be marked with the graphical symbol X. The crossover function specified here is compatible with the crossover function specified in 14.5.2 for pairs TD and RD.

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Table 32–14—Assignment of PMA signals to MDI pin-outs

Contact	PHY without internal crossover (100BASE-T2 operation)	PHY with internal crossover (Auto-Negotiation operation)	MDI labeling requirement
1	BI_DA+	BI_DB+	BI_DA+
2	BI_DA-	BI_DB-	BI_DA-
3	BI_DB+	BI_DA+	BI_DB+
4	Not used	Not used	
5	Not used	Not used	
6	BI_DB-	BI_DA-	BI_DB-
7	Not used	Not used	
8	Not used	Not used	

When a link segment connects a DTE to a repeater, it is recommended the crossover be implemented in the PHY local to the repeater. If both PHYs of a link segment contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the PHYs. When both PHYs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central repeater that the PHY furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

32.9 System considerations

The repeater unit specified in Clause 27 forms the central unit for interconnecting 100BASE-T2 twisted-pair links in networks of more than two nodes. It also provides the means for connecting 100BASE-T2 balanced cabling links to other 100 Mb/s baseband segments. The proper operation of a CSMA/CD network requires that network size be limited to control round-trip propagation delay as specified in Clause 29.

When operated in Full Duplex mode where CSMA/CD requirements do not apply, 100BASE-T2 balanced cabling links are limited to 100 m as per ISO/IEC 11801.

32.10 Environmental specifications

32.10.1 General safety

All equipment meeting this standard shall conform to IEC 60950.

32.10.2 Network safety

This clause sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits
b) Static charge buildup on LAN cabling and components

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c) High-energy transients coupled onto the LAN cabling system
d) Voltage potential differences between safety grounds to which various LAN components are connected

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network.

32.10.2.1 Installation

It is a mandatory functional requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

32.10.2.2 Grounding

Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.

WARNING

It is assumed that the equipment to which the PHY is attached is properly grounded, and not left floating nor serviced by a "doubly insulated, ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety, are beyond the scope of this standard.

32.10.2.3 Installation and maintenance guidelines

It is a mandatory functional requirement that, during installation and maintenance of the cabling plant, care be taken to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

32.10.2.4 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 100BASE-T2 equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an AC component and a DC component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The DC component is 56 Vdc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 100BASE-T2 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE—Wiring errors may impose telephony voltages differentially across 100BASE-T2 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

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32.10.3 Environment

32.10.3.1 Electromagnetic emission

The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

32.10.3.2 Temperature and humidity

The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the PHY the operating environmental conditions to facilitate selection, installation, and maintenance.

32.10.4 Cabling specifications

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801.

32.11 PHY labeling

It is recommended that each PHY (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Data rate capability in Mb/s
b) Power level in terms of maximum current drain (for external PHYs)
c) Port type (i.e., 100BASE-T2)
d) Any applicable safety warnings

See also 32.8.2.

32.12 Delay constraints

Proper operation of a CSMA/CD LAN, operating in half duplex mode, demands that there be an upper bound on the propagation delays through the network. This implies that MAC, PHY and repeater implementers must conform to certain delay minima and maxima, and that network planners and administrators conform to constraints regarding the cabling topology and concatenation of devices. MAC constraints are contained in Clause 21. Topological constraints are contained in Clause 29. In the full duplex mode of operation, DTEs are not required to conform to the constraints specified in this clause.

The reference point for all MDI measurements is the peak point of the mid-cell transition corresponding to the reference code-bit, as measured at the MDI. Although 100BASE-T2 output is scrambled, it is assumed that these measurements are made via apparatuses that appropriately account for this.

32.12.1 PHY delay constraints (exposed MII)

Every 100BASE-T2 PHY with an exposed MII shall comply with the bit delay constraints specified in Table 32–15. These figures apply for all 100BASE-T2 PMDs.

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Table 32–15—MDI to MII delay constraints (exposed MII)

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MII ⇔ MDI	TX_EN Sampled to MDI Output	7	9	TX_CLK rising	1st symbol of SSD
	MDI input to CRS assert		25	1st symbol of SSD	
	MDI input to CRS deassert		29	1st ONE	
	MDI input to COL assert		25	1st symbol of SSD	
	MDI input to COL deassert		29	1st symbol of SSD	
	TX_EN sampled to CRS assert	0	4	TX_CLK rising	
	TX_EN sampled to CRS deassert	0	16	TX_CLK rising	

32.12.2 DTE delay constraints (unexposed MII)

Every 100BASE-T2 DTE with no exposed MII shall comply with the bit delay constraints specified in Table 32–16. These figures apply for all 100BASE-T2 PMDs.

Table 32–16—DTE delay constraints (unexposed MII)

Sublayer Measurement Points	Event	Min (bits)	Max (bits)	Input Timing Reference	Output Timing Reference
MAC ⇔ MDI	MAC transmit start to MDI output		13		1st symbol of SSD
	MDI input to MDI output (worst-case non-deferred transmit)		50	1st symbol of SSD	1st symbol of SSD
	MDI input to collision detect		33	1st symbol of SSD	
	MDI input to MDI output = Jam (worst-case collision response)		50	1st symbol of SSD	1st symbol of SSD

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32.13 Protocol implementation conformance statement (PICS) proforma for Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2[19]

The supplier of a protocol implementation that is claimed to conform to Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2, shall complete the following protocol implementation conformance statement (PICS) proforma.

Instructions for interpreting and filling out the PICS proforma may be found in Clause 21.

32.13.1 Identification

32.13.1.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1— Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

32.13.1.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Clause 32, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T2
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exceptions items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2015.)	

Date of Statement	

[19] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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32.13.2 Major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*MII	Exposed MII interface	32.1.3.2	O	Yes [ ] No [ ]	Devices supporting this option must also support the PCS option.
PC	PHY Control functions	32.2	M	Yes [ ]	Required for proper operation of the PHY.
*PCS	PCS functions	32.3	O	Yes [ ] No [ ]	Required for integration with DTE or MII.
*PMA	Exposed PMA service interface	32.4.2	O	Yes [ ] No [ ]	Required for integration into symbol level repeater core.
NWY	Support for Auto-Negotiation (Clause 28)	32.1.3.4	M	Yes [ ]	Required
*INS	Installation/cabling	32.7.4	O	Yes [ ] No [ ]	Items marked with INS include installation practices and cabling specifications not applicable to a PHY manufacturer.

32.13.3 Compatibility considerations

Item	Feature	Subclause	Status	Support	Value/Comment
CCO1	Compatibility at the MDI	32.1.3.1	M	Yes [ ]	
CCO2	Auto-Negotiation required	32.1.3.4	M	Yes [ ]	
CCO3	State diagrams prevail	32.1.4	M	Yes [ ]	In discrepancy between text and state diagram.

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32.13.4 PHY control function

Item	Feature	Subclause	Status	Support	Value/Comment
PC01	PHY Control shall	32.2.1	M	Yes [ ]	Comply with the state diagram descriptions given in Figure 32–5.
PC02	PHY Control shall	32.2.2.1.2	M	Yes [ ]	Generate PHYC_CONFIG.indication messages synchronously with every MII TX_CLK cycle.
PC03	Upon receipt of the PHYC_CONFIG primitive, PCS Transmit and PMA Clock Recovery shall	32.2.2.1.3	M	Yes [ ]	Perform their functions in master or slave configuration according to the value of the parameter config.
PC04	PHY Control shall	32.2.2.2.2	M	Yes [ ]	Generate PHYC_LOCRXSTATUS.indication messages synchronously with every MII TX_CLK cycle.
PC05	Upon reception of the PHYC_LOCRXSTATUS.indication primitive, PCS Transmit shall	32.2.2.2.3	M	Yes [ ]	Perform its function according to the value assumed by the parameter loc_cvr_status.
PC06	PHY Control shall	32.2.2.3.2	M	Yes [ ]	Generate PHYC_TXMODE.indication messages synchronously with every MII TX_CLK cycle.
PC07	Upon receipt of the PHYC_TXMODE.indication primitive, the PCS shall	32.2.2.3.3	M	Yes [ ]	Perform its Transmit function as described in 32.3.1.2.
PC8	The PCS shall	32.2.2.3.2	M	Yes [ ]	Generate PHYC_RXSTATUS.request messages synchronously with signals received at the MDI.
PC9	The PCS shall	32.2.2.4.2	M	Yes [ ]	Generate PHYC_REMRXSTATUS.request messages synchronously with signals received at the MDI.
PC10	PCS Transmit shall	32.2.3	M	Yes [ ]	Send quinary symbols according to the value assumed by tx_mode.
PC11	When tx_mode assumes the value of SEND_N	32.2.3	M	Yes [ ]	Transmission of sequences of quinary symbols representing an MII data stream, the idle mode, or control sequences shall take place.
PC12	When tx_mode assumes the value of SEND_I	32.2.3	M	Yes [ ]	Transmission of sequences of quinary symbols representing the idle mode shall take place.

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32.13.5 Physical Coding Sublayer (PCS) or Physical Medium Attachment (PMA) sublayer

32.13.5.1 PCS transmit functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCT01	The PCS shall	32.3.5.1	M	Yes [ ]	Implement the Transmit process as depicted in Figure 32–12 including compliance with the associated state variables specified in 32.3.4.
PCT02	PCS Transmit function shall	32.3.1.2	M	Yes [ ]	Conform to the PCS Transmit state diagram in Figure 32–12.
PCT03	If the parameter config provided to the PCS by the PHY Control function via the PHY-C_CONFIG.indication message assumes the value MASTER, PCS Transmit shall	32.3.1.2.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with MASTER in 32.3.1.2.1.
PCT04	If the parameter config provided to the PCS by the PHY Control function via the PHY-C_CONFIG.indication message assumes the value SLAVE, PCS Transmit shall	32.3.1.2.1	M	Yes [ ]	Employ the transmitter side-stream scrambler generator polynomial specified for use with SLAVE in 32.3.1.2.1.
PCT05	Transmission of quinary symbol pairs over wire pairs	32.3.1.2	M	Yes [ ]	Symbols A_n and B_n are transmitted over BI_DA and BI_DB respectively.

32.13.5.2 PCS receive functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCR01	The PCS shall	32.3.5.2	M	Yes [ ]	Implement the Receive process as depicted in Figure 32–13 including compliance with the associated state variables as specified in 32.3.4.
PCR02	PCS Receive function shall	32.3.1.3	M	Yes [ ]	Conform to the PCS Receive state diagram shown in Figure 32–13.
PCR03	For side-stream descrambling, the MASTER PHY shall employ	32.3.1.3.1	M	Yes [ ]	The receiver scrambler generator polynomial specified for MASTER operation in 32.3.1.3.1.
PCR04	For side-stream descrambling, the SLAVE PHY shall employ	32.3.1.3.1	M	Yes [ ]	The receiver scrambler generator polynomial specified for SLAVE operation in 32.3.1.3.1.

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32.13.5.3 Other PCS functions

Item	Feature	Subclause	Status	Support	Value/Comment
PCO1	The PCS Reset function shall	32.3.1.1	M	Yes [ ]	Be executed any time “power on,” receipt of a request for reset from the management entity, or receipt of a request for reset from the PHY Control occur.
PCO2	THE PCS shall	32.3.1.4	M	Yes [ ]	Implement the PCS Carrier Sense function shown in Figure 32–14.
PCO3	PCS Carrier Sense function shall	32.3.5.3	M	Yes [ ]	Comply with the PCS Carrier Sense state diagram shown in Figure 32–14 including compliance with the associated state variables specified in 32.3.4.
PCO4	MII COL signal shall be asserted while	32.3.1.5	M	Yes [ ]	A PCS collision is being detected.
PCO5	The MII signal COL shall remain deasserted.	32.3.1.5	M	Yes [ ]	A PCS collision is not being detected.
PCO6	No spurious PCS management entity signals shall be emitted onto the MDI while the PHY is held in power down mode as defined in 22.2.4.1.5, independently of the value of TX_EN, or when released from power down mode, or when power is first applied to the PHY.	32.3.2.2	M	Yes [ ]	
PCO7	Frames passed from the PCS to the PMA sublayer shall	32.3.3	M	Yes [ ]	Have the structure shown in Figure 32–11.
PCO8	TX_CLK shall be generated	32.3.4.2	M	Yes [ ]	Synchronously with symb_timer with tolerance as specified in 32.6.1.2.6.

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32.13.5.4 PMA functions

Item	Feature	Subclause	Status	Support	Value/Comment
PMF1	PMA Reset function shall be executed	32.4.1.1.1	M	Yes [ ]	At power on and upon receipt of a reset request from the management entity.
PMF2	PMA transmit shall continuously transmit	32.3.1.2	M	Yes [ ]	Onto the MDI pulses modulated by the quinary symbols given by tx_symb_vector[BI_DA] and tx_symb_vector[BI_DB] respectively.
PMF3	The two transmitters shall be driven by the same transmit clock.	32.4.1.1.2	M	Yes [ ]	
PMF4	PMA Transmit function will follow	32.4.1.1.2	M	Yes [ ]	The mathematical description given in 32.4.1.2.1.
PMF5	PMA Transmit shall comply with	32.4.1.1.2	M	Yes [ ]	The electrical specifications given in 32.6.
PMF6	PMA Receive function shall translate	32.4.1.1.3	M	Yes [ ]	The signals received on pairs BI_DA and BI_DB into the PMA_UNITDATA.indication parameter rx_symb_vector with a symbol error ratio of less than one part in 10^{10}.
PMF7	The Link Monitor function shall	32.4.1.1.4	M	Yes [ ]	Comply with the state diagram shown in Figure 32–17.
PMF8	Clock Recovery function shall provide	32.4.1.1.5	M	Yes [ ]	A clock suitable for synchronous signal sampling on each line so that the symbol error ratio indicated in 32.4.1.1.3 is achieved.
PMF9	The waveform obtained at the MDI shall comply with	32.4.1.2.1	M	Yes [ ]	The electrical specifications given in 32.6.
PMF10	The two signals received on pair BI_DA and BI_DB shall be processed within the PMA Receive function to yield	32.4.1.2.2	M	Yes [ ]	The quinary received symbols rx_symb_vector[BI_DA] and rx_symb_vector[BI_DB].

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32.13.5.5 PMA service interface

Item	Feature	Subclause	Status	Support	Value/Comment
PMS1	Continuous generation of PMA_TYPE	32.4.1.2.2	M	Yes [ ]	
PMS2	Generation of PMA_UNIT-DATA.indication (SYM-B_PAIR) messages	32.4.2.3.2	M	Yes [ ]	Synchronous with data received at the MDI.
PMS3	The PMA shall generate	32.4.2.5.2	M	Yes [ ]	PMA_LINK.indication to indicate the value of link_status.
PMS4	Effect of receipt of PMA_LINK.request messages	32.4.2.4.3	M	Yes [ ]	While link_control=SCAN_-FOR_CARRIER or link_control=DISABLE, the PMA shall report link_status=fail; while link_control=ENABLE, PHY determines operations to be performed by the PHY.

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32.13.5.6 Management functions

Item	Feature	Subclause	Status	Support	Value/Comment
MF1	A 100BASE-T2 PHY shall	32.5	M	Yes [ ]	Use register addresses 9 and 10 for its control and status functions.
MF2	Register 9 shall	32.5.3.1	M	Yes [ ]	Provide values as specified in Table 32–4.
MF3	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 1 when bit 9.15 is set to logic zero and bit 9.14 is set to logic one.
MF4	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 2 when bit 9.15 is set to logic one and bit 9.14 is set to logic zero.
MF5	A PHY with 100BASE-T2 capability shall	32.5.3.1.1	M	Yes [ ]	Be placed in transmitter test mode 3 when bit 9.15 is set to logic one and bit 9.14 is set to logic one.
MF6	A PHY with 100BASE-T2 capability shall	32.5.3.1.2	M	Yes [ ]	Be placed in receiver test mode when bit 9.13 is set to logic one.
MF7	MASTER-SLAVE configuration negotiation will determine PHY configuration if	32.5.3.1.3	M	Yes [ ]	Bit 9.12 is set to logic zero.
MF8	Manual MASTER-SLAVE configuration will be set manually using bit 9.11 to set the value if	32.5.3.1.3	M	Yes [ ]	Bit 9.12 is set to logic one.
MF9	Bit 9.11 shall be used to report the results of manual MASTER-SLAVE configuration.	32.5.3.1.4	M	Yes [ ]	
MF10	Bit 9.10 shall	32.5.3.1.5	M	Yes [ ]	Be set to logic zero if the PHY is a DTE device and be set to logic one if the PHY is a repeater device port.
MF11	Bits 9.9:0 shall	32.5.3.1.6	M	Yes [ ]	Be set to logic zero.
MF12	Bits 9.9:0 shall be ignored when read	32.5.3.1.6	M	Yes [ ]	
MF13	A PHY shall return a value of zero for bits 9.9:0.	32.5.3.1.6	M	Yes [ ]	
MF14	Register 10 shall	32.5.3.1.2	M	Yes [ ]	Be used as shown in Table 32–5.
MF15	Bits 10.11:8 shall	32.5.3.2.5	M	Yes [ ]	Be set to logic zeros by default.
MF16	The MASTER-SLAVE Manual Configuration Fault bit shall be implemented	32.5.3.2.1	M	Yes [ ]	With a latching function, such that the occurrence of a MASTER-SLAVE Manual Configuration Fault will cause the MASTER-SLAVE Manual Configuration Fault bit to be set and remain set until cleared.

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32.13.5.6 Management functions *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
MF17	The MASTER-SLAVE Manual Configuration Fault bit shall be cleared	32.5.3.2.1	M	Yes [ ]	Each time register 10 is read by the management interface.
MF18	The MASTER-SLAVE Management Configuration Fault bit shall also be cleared by	32.5.3.2.1	M	Yes [ ]	A 100BASE-T2 PMA reset.
MF19	Bits 10:11:8 shall	32.5.3.2.5	M	Yes [ ]	Be ignored when read.
MF20	A PHY shall return a value of zero for bits10.11:8.	32.5.3.2.5	M	Yes [ ]	

32.13.5.7 100BASE-T2 specific Auto-Negotiation requirements

Item	Feature	Subclause	Status	Support	Value/Comment
AN1	Base Page will be followed with	32.5.4.2	M	Yes [ ]	A Next Page with a message code containing the 100BASE-T2 Technology Ability Message Code (7).
AN2	Message Next Page shall be followed with	32.5.4.2	M	Yes [ ]	Unformatted Message Next Page containing the 100BASE-T2 Technology Ability Fields as described in Table 32–6.
AN3	MASTER-SLAVE relationship shall be determined by	32.5.4.3	M	Yes [ ]	Using Table 32–7with the 100BASE-T2 Technology Ability Next Page bit values specified in Table 32–6.
AN4	A seed counter shall be provided to	32.5.4.3	M	Yes [ ]	Track the generation of seeds.
AN5	At start-up, the seed counter shall be set to	32.5.4.3	M	Yes [ ]	Zero.
AN6	The seed counter shall be incremented	32.5.4.3	M	Yes [ ]	Every time a new random seed is sent.
AN7	Maximum seed attempts before declaring a MASTER_SLAVE configuration Resolution Fault	32.5.4.3	M	Yes [ ]	Seven.
AN8	During MASTER_SLAVE configuration, the device with the lower seed value shall	32.5.4.3	M	Yes [ ]	Become the SLAVE.

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32.13.5.7 100BASE-T2 specific Auto-Negotiation requirements *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
AN9	Both PHYs set in manual mode to be either MASTER or SLAVE shall be treated as	32.5.4.3	M	Yes [ ]	MASTER-SLAVE resolution fault (Failure) condition
AN10	MASTER-SLAVE resolution fault (failure) condition shall result in	32.5.4.3	M	Yes [ ]	MASTER-SLAVE Configuration Resolution Fault bit (10.15) to be set
AN11	MASTER-SLAVE Configuration resolution fault condition shall be treated as	32.5.4.3	M	Yes [ ]	MASTER-SLAVE Configuration Resolution complete

32.13.5.8 PMA electrical specifications

Item	Feature	Subclause	Status	Support	Value/Comment
PME1	The value of all components in test circuits shall be accurate to within	32.6	M	Yes [ ]	±1%.
PME2	The PHY shall provide electrical isolation between	32.6.1.1	M	Yes [ ]	The DTE or repeater circuits including frame ground, and all MDI leads.
PME3	PHY-provided electrical separation shall withstand at least one of three electrical strength tests	32.6.1.1	M	Yes [ ]	a) 1500 V rms at 50–60Hz for 60 s, applied as specified in section 5.3.2 of IEC 60950. b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950. c) a sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs. (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60950.
PME4	There shall be no insulation breakdown as defined in Section 5.3.2 of IEC 60950, during the test.	32.6.1.1	M	Yes [ ]	
PME5	The resistance after the test shall be at least	32.6.1.1	M	Yes [ ]	2 MΩ, measured at 500 Vdc.
PME6	The PMA shall provide the Transmit function specified in 32.4.1.1.2 in accordance with the electrical specifications of this clause.	32.6.1.2	M	Yes [ ]	

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME7	Where a load is not specified, the transmitter shall meet all the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.	32.6.1.2	M	Yes [ ]	
PME8	The tolerance on the poles of the test filters used in 32.6 shall be	32.6.1.2	M	Yes [ ]	±1%
PME9	A special transmit test mode shall be required to allow for testing of the transmitter waveform	32.6.1.2.1	M	Yes [ ]	
PME10	A test mode for measuring transmitter output jitter is required.	32.6.1.2.1	M	Yes [ ]	
PME11	For a PHY with a MII interface, the transmit test mode shall be enabled by	32.6.1.2.1	M	Yes [ ]	Setting bit 9.15 and 9.14 (MASTER-SLAVE Control register) of the MII management register set as shown in Table 32–6.
PME12	These test modes shall only change the data symbols provided to the transmitter circuitry and may not alter the electrical characteristics of the transmitter	32.6.1.2.1	M	Yes [ ]	
PME13	When transmit test mode 1 is enabled, the PHY shall transmit	32.6.1.2.1	M	Yes [ ]	The sequence of data symbols specified in 32.6.1.2.1 continuously from both transmitters.
PME14	When in test mode 1, the transmitter shall time the transmitted symbols	32.6.1.2.1	M	Yes [ ]	From a 25.000 MHz ± 0.01% clock.
PME15	When test mode 2 is enabled, the PHY shall transmit	32.6.1.2.1	M	Yes [ ]	The data symbol sequence {+2,–2} repeatedly on both channels.
PME16	When in test mode 2, the transmitter shall time the transmitted symbols	32.6.1.2.1	M	Yes [ ]	From a 25.000 MHz ± 0.01% clock.
PME17	A PHY without a MII shall provide a means to enter this test mode.	32.6.1.2.1	M	Yes [ ]	
PME18	The vendor shall	32.6.1.2.1	M	Yes [ ]	Provide a means to enable these modes for testing.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME19	When in transmit test mode 1 and observing the differential signal output at the MDI, terminated in 100 Ω, preprocessed by the high pass filter defined below, for either pair, with no intervening cable, the absolute value of the peak of the waveform at points A and B as defined in Figure 32–18 shall fall within	32.6.1.2.2	M	Yes [ ]	The range of 1.71V to 1.91 V (1.81 V ± 0.5 dB).
PME20	The absolute value of the peak of the waveforms at points A and B shall	32.6.1.2.2	M	Yes [ ]	Differ by less than 2%.
PME21	The absolute value of the peak of the waveform at points C and D as defined in Figure 32–18 shall differ	32.6.1.2.2	M	Yes [ ]	From 0.5 times the average of the absolute values of the peaks of the waveform at points A and B by less than 2%.
PME22	The preprocessing filter shall have	32.6.1.2.2	M	Yes [ ]	The transfer function specified in 32.6.1.2.2.
PME23	When in transmit test mode 1 and observing the differential transmitted output at the MDI, for either pair, with no intervening cabling, the peak value of the waveform at point F as defined in Figure 32–17 shall be	32.6.1.2.3	M	Yes [ ]	Greater than 70.5% of the peak value of the waveform at point E. A preprocessing filter is not used for this measurement.
PME24	The transmitter differential output voltage shall be measured at the output of the high pass filter defined in 32.6.1.2.2 with no intervening cables.	32.6.1.2.4	M	Yes [ ]	
PME25	The voltage waveforms at points A, B, C and D as defined in Figure 32–17,when normalized by their respective peak values, shall	32.6.1.2.4	M	Yes [ ]	Lie within the time domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–6
PME26	The magnitude in dB of the Fourier transform of the waveforms at points A, B, C and D shall	32.6.1.2.4	M	Yes [ ]	Lie within the transmit frequency domain template defined in Figure 32–18 and the piecewise linear interpolation between the points in Table 32–7.
PME27	The time span of the waveforms so processed shall be	32.6.1.2.4	M	Yes [ ]	–80 ns to +2000 ns with the 0 ns point of the waveform aligned as for the time domain mask shown in Figure 32–18 and the magnitude of the Fourier transform should be normalized so that the maximum value is at 0 dB.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME28	When in transmit mode 2, the peak-to-peak jitter of the zero crossings of the differential signal output at the MDI shall	32.6.1.2.5	M	Yes [ ]	Be less than 0.5 ns.
PME29	The quinary symbol transmission rate on each pair shall be	32.6.1.2.6	M	Yes [ ]	25.000 MHz ± 0.01%.
PME30	The PMA shall provide	32.6.1.3	M	Yes [ ]	The Receive function specified in 32.4.1.3 in accordance with the electrical specifications of this clause.
PME31	The patch cabling and interconnecting hardware used in test configurations shall	32.6.1.3	M	Yes [ ]	Meet or exceed ISO/IEC 11801 Category 3 specifications.
PME32	The combined responses of the test fixture TX block and NEXT or cabling channel blocks shall be	32.6.1.3.1	M	Yes [ ]	Those defined in Table 32–8.
PME33	The output impedance of the test channel shall be	32.6.1.3	M	Yes [ ]	Consistent with 32.6.1.4.1.
PME34	The idle symbol generator outputs shall be	32.6.1.3	M	Yes [ ]	Conformant with the idle signaling specified in 32.3 with loc_rcvr_status=OK.
PME35	The clock source shall	32.6.1.3	M	Yes [ ]	Result in a quinary symbol transmission rate conformant with 32.6.1.2.6.
PME36	The jitter on the clock source shall be	32.6.1.3	M	Yes [ ]	Less than 0.2 ns.
PME37	The test channel implementation shall ensure that the ratio of the squared error between the implemented NEXT channel symbol responses and the specified NEXT channel symbol responses to the energy in the specified NEXT channel symbol responses shall be	32.6.1.3	M	Yes [ ]	Less than 5%.
PME38	The test channel implementation shall ensure that the energy of the implemented NEXT channel impulse responses and the energy of the specified NEXT channel impulse responses shall	32.6.1.3	M	Yes [ ]	Differ by less than ±0.25 dB.
PME39	A special receiver test mode shall be required to allow for receiver alien NEXT tolerance and jitter testing.	32.6.1.3.2	M	Yes [ ]	
PME40	For a PHY with a MII interface, this mode shall be enabled by	32.6.1.3.2	M	Yes [ ]	Setting bit 9.13 (MASTER-SLAVE Control Register) of the MII management register set to a 1.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME41	A PHY without an MII shall provide	32.6.1.3.2	M	Yes [ ]	A means to enable this test mode.
PME42	This mode shall not be overridden except by	32.6.1.3.2	M	Yes [ ]	Clearing bit 9.13 or resetting the PHY.
PME43	When the receive test mode is enabled, the receiver shall	32.6.1.3.2	M	Yes [ ]	Configure itself in SLAVE mode, continually attempt to bring its receiver up until successful receiver operation is achieved and transmit symbols in idle mode.
PME44	For a PHY with a MII interface, when the receiver is properly detecting the received data, it shall set	32.6.1.3.2	M	Yes [ ]	Bit 10.13 of the MII management register set to 1 and reset the error count in bit 10.0–10.7 (MSB) to zero.
PME45	The error count shall be incremented	32.6.1.3.2	M	Yes [ ]	For every symbol error detected in the received idle sequence.
PME46	Upon loss of proper data reception, the receiver shall	32.6.1.3.2	M	Yes [ ]	Clear bit 10.13.
PME47	A PHY without an MII shall provide	32.6.1.3.2	M	Yes [ ]	A means to provide the functions defined in PME43 through PME46.
PME48	The vendor shall provide a means to enable this mode for conformance testing.	32.6.1.3.2	M	Yes [ ]	
PME49	Differential signals received on the receive inputs that were transmitted within the constraints of 32.6.1.2, and have then passed through a link as defined in 32.7, shall be translated into	32.6.1.3.3	M	Yes [ ]	One of the PMA_UNITDATA.indication messages with an bit error ratio less than 10^{-10} and sent to the PCS after link bring-up.
PME50	Performance shall be tested	32.6.1.3.3	M	Yes [ ]	In at least two configurations: using a 100 m link segment conformant to 32.7 and with a link segment less than one meter in length between transmitter and receiver.
PME51	Differential signals received from the test channel defined in 32.6.1.3.1 shall be detected	32.6.1.3.4	M	Yes [ ]	With a symbol error ratio less than 10^{-10} when the PHY is in receiver test mode for the combinations of channel and worst-case alien NEXT responses specified in 32.6.1.2.
PME52	In the test configuration described in 32.6.1.3.1 and for all combinations of worst-case channel and alien NEXT coefficients tabulated in 32.6.1.3.4, the peak-to-peak value of the RX_CLK zero-crossing jitter shall be less than	32.6.1.3.5	M	Yes [ ]	1.3 ns after the receiver is properly receiving the data and has set bit 9.13 of the MII management register set to 1.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME53	When the jitter waveform is filtered by a high pass filter having the transfer function specified in 32.6.1.3.4, the peak-to-peak value of the jitter waveform shall be less than	32.6.1.3.5	M	Yes [ ]	0.8 ns.
PME54	The RX_CLK of the MII shall be made available for the receiver jitter test specified in 32.6.1.3.5.	32.6.1.3.5	M	Yes [ ]	
PME55	A PHY without an MII shall provide an equivalent to the MII RX-CLK clock for the receiver jitter test specified in 32.6.1.3.5.	32.6.1.3.5	M	Yes [ ]	
PME56	While receiving packets from a compliant 100BASE-T2 transmitter connected to all MDI pins, a receiver shall send the	32.6.1.3.6	M	Yes [ ]	Proper PMA_UNITDATA.indication messages to the PCS for any differential input signal E_s that results in a signal E_{dif} that meets 32.6.1.3.3 even in the presence of common-mode voltages E_{cm} (applied as shown in Figure 32–21).
PME57	E_{cm} shall be	32.6.1.3.6	M	Yes [ ]	A 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%), connected to each of the pairs BI_DA+, BI_DA-, BI_DB+ and BI_DB-.
PME58	The receive feature shall properly receive	32.6.1.3.7	M	Yes [ ]	Incoming data with a 5-level symbol rate within the range 25.000 MHz ± 0.01%.
PME59	The differential impedance as measured at the MDI for each transmit/receive channel shall be such that	32.6.1.4.1	M	Yes [ ]	Any reflection due to differential signals incident upon the MDI from a balanced cabling having an impedance of 100 Ω is at least 17 dB below the incident signal, over the frequency range of 2.0 MHz to 25.0 MHz and at least $12.9–20\log_{10}(f/10)$ dB over the frequency range 6.5 MHz to 25 MHz (f in MHz).
PME60	This return loss shall be maintained	32.6.1.4.1	M	Yes [ ]	At all times when the PHY is transmitting data.
PME61	The common-mode to differential-mode impedance balance of each transmit output shall exceed	32.6.1.4.2	M	Yes [ ]	The value specified by the equations specified in 32.6.1.2.6 over the range 2.0–25.0 MHz.

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32.13.5.8 PMA electrical specifications *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
PME62	Transmitters and receivers shall tolerate	32.6.1.4.4	M	Yes [ ]	The application of short circuits between the leads of any receive input for an indefinite period of time without damage.
PME63	Transmitters and receivers shall resume	32.6.1.4.4	M	Yes [ ]	Normal operation after such faults are removed.
PME64	The magnitude of the current through the short circuit specified in PME62 shall not exceed	32.6.1.4.4	M	Yes [ ]	300 mA.
PME65	Transmitters shall withstand without damage	32.6.1.4.4	M	Yes [ ]	A 1000 V common-mode impulse of either polarity (E_{cm} as indicated in Figure 32–24).
PME66	The shape of the impulse shall be	32.6.1.4.4	M	Yes [ ]	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060.
PME67	After 100 ms following PowerOn, the current drawn by the PHY shall not exceed	32.6.2	M	Yes [ ]	1.0 A when powered through the MII.
PME68	The PHY shall	32.6.2	M	Yes [ ]	Be capable of operating from all voltage sources allowed by Clause 22, including those current limited to1.0 A, as supplied by the DTE or repeater through the resistance of all permissible MII cabling.
PME69	The PHY shall not introduce	32.6.2	M	Yes [ ]	Extraneous signals on the MII control circuits during normal power-up and power-down.

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32.13.5.9 Characteristics of the link segment

Item	Feature	Subclause	Status	Support	Value/Comment
LKS1	100BASE-T2 links shall use	32.7.1	M	Yes [ ]	2 pair of balanced cabling, CAT 3 or better, with a nominal impedance of 100 Ω.
LKS2	Unless otherwise specified, link segment testing shall be conducted using	32.7.2	M	Yes [ ]	Source and load impedances of 100 Ω
LKS3	The tolerance on the poles of the test filter used in this section shall be	32.7.2	M	Yes [ ]	± 1%.
LKS4	The insertion loss of a link segment shall be no more than	32.7.2.1	M	Yes [ ]	14.6 dB at all frequencies between 2 and 16 MHz.
LKS5	The insertion loss specification shall be met when	32.7.2.1	M	Yes [ ]	The link segment is terminated in source and load impedances that satisfy 32.6.1.4.1.
LKS6	The magnitude of the differential characteristic impedance of a 3 m segment of balanced cabling pair used in a link shall be	32.7.2.2	M	Yes [ ]	Between 85 and 115 Ω for all frequencies between 2 and 16 MHz.
LKS7	The NEXT loss between each of the two duplex channels of a link segment shall be	32.7.2.3.1	M	Yes [ ]	At least $19.3–16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS8	The NEXT loss between link segments of two different connections shall be	32.7.2.3.1	M	Yes [ ]	At least $22.0 –16.6\log_{10}(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS9	The MDNEXT loss between a link segment and the two alien data carrying channels shall be	32.7.2.3.2	M	Yes [ ]	At least $19.0–16.6\log_{10}(f/16)$ dB (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS10	To limit the FEXT noise from an adjacent channel, the ELFEXT loss between channels shall be	32.7.2.3.3	M	Yes [ ]	Greater than $20.9–20\log_{10}(f/16)$ dB as defined in 32.7.2.3.3
LKS11	The MDELFEXT loss between a duplex channel and the other data carrying duplex channels shall be	32.7.2.3.4	M	Yes [ ]	Greater than $19.9–20\log10(f/16)$ (where f is the frequency in MHz) over the frequency range 2.0 to 16 MHz.
LKS12	The maximum spacing of the frequency in the sample shall be	32.7.2.3.5	M	Yes [ ]	250 kHz.

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32.13.5.9 Characteristics of the link segment *(continued)*

Item	Feature	Subclause	Status	Support	Value/Comment
LKS13	When 10BASE-T service is used in adjacent pairs, the channel shall provide	32.7.2.3.5	M	Yes [ ]	A NEXT loss to Insertion loss Ratio (NIR) greater than 19.4 dB.
LKS14	The propagation delay of a link segment shall not exceed	32.7.2.4.1	M	Yes [ ]	5.7 ns/meter at all frequencies between 2.0–25.0 MHz.
LKS15	The difference in propagation delay, or skew, under all conditions, between the fastest and the slowest channel in a link segment shall not exceed	32.7.2.4.2	M	Yes [ ]	50 ns at all frequencies between 2.0–25.0 MHz.
LKS16	Once installed, the skew between pairs due to environmental conditions shall not vary	32.7.2.4.2	M	Yes [ ]	More than ± 10 ns.
LKS17	The noise level on the link segments shall be such that	32.7.3	M	Yes [ ]	The objective error ratio is met.
LKS18	The MDNEXT noise on a link segment shall not exceed	32.7.3.1	M	Yes [ ]	182 mVp.
LKS19	The MDFEXT noise on a link segment shall not exceed	32.7.3.2	M	Yes [ ]	54.4 mVp.
LKS20	Cables made from up to 25 pairs of Category 5 cabling, if used, shall be limited in length to no more than	32.7.4.3	O	Yes [ ]	90 m total.
LKS21	The services in 25 pair Category 5 cabling shall be limited to any combination of 100BASE-T2, 10BASE-T and digital phone service compliant with the ISDN-BR U and S/T interfaces up to a total of 12 services in the cable.	32.7.4.3	M	Yes [ ]	
LKS22	Jumper cabling, or horizontal runs, made from more than 4 pairs of Category 3 cabling shall not be used	32.7.4.3	M	Yes [ ]	

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32.13.5.10 MDI requirements

Item	Feature	Subclause	Status	Support	Value/Comment
MDI1	MDI connector	32.8.1	M	Yes [ ]	8-Way connector as per IEC 60603-7.
MDI2	Connector used on cabling	32.8.1	M	Yes [ ]	Plug.
MDI3	Connector used on PHY	32.8.1	M	Yes [ ]	Jack (as opposed to plug).
MDI4	AN MDI connector for the PHY that implements the crossover function shall be marked	32.8.2	M	Yes [ ]	With the graphical symbol "X".

32.13.5.11 General safety and environmental requirements

Item	Feature	Subclause	Status	Support	Value/Comment
ENV1	Conformance to safety specifications	32.10.1	M	Yes [ ]	IEC 60950.
ENV2	Installation practice	32.10.2.1	M	Yes [ ]	Sound practice, as defined by applicable local codes.
ENV3	Any safety grounding path for an externally connected PHY shall be provided through the circuit ground of the MII connection.	32.10.2.2	M	Yes [ ]	
ENV4	Care taken during installation to ensure that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.	32.10.2.3	M	Yes [ ]	
ENV5	Application of voltages specified in 32.10.2.4 does not result in any safety hazard.	32.10.2.4	M	Yes [ ]	
ENV6	Conformance with local and national codes for the limitation of electromagnetic interference.	32.10.3.1	M	Yes [ ]	
ENV7	All equipment subject to this clause shall conform to	32.10.4	M	Yes [ ]	The requirements of 14.7 and the applicable sections of ISO/IEC 11801.

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32.13.5.12 Timing requirements exposed MII

Item	Feature	Subclause	Status	Support	Value/Comment
TME1	TX-EN (sampled to MDI output)	32.12.1	M	Yes [ ]	7–9 bit times
TME2	MDI input to CRS assert	32.12.1	M	Yes [ ]	25 bit times
TME3	MDI input to CRS deassert	32.12.1	M	Yes [ ]	29 bit times
TME4	MDI input to COL assert	32.12.1	M	Yes [ ]	25 bit times
TME5	MDI input to COL deassert	32.12.1	M	Yes [ ]	29 bit times
TME6	TX_EN sampled to CRS assert	32.12.1	M	Yes [ ]	0–4 bit times
TME7	TX_EN sampled to CRS deassert	32.12.1	M	Yes [ ]	0–16 bit times

32.13.5.13 Timing requirements unexposed MII

Item	Feature	Subclause	Status	Support	Value/Comment
TMU1	MAC transmit start to MDI output	32.12.2	M	Yes [ ]	13 bit times
TMU2	MDI input to MDI output (worst-case non-deferred transmit)	32.12.2	M	Yes [ ]	50 bit times
TMU3	MDI input to collision detect	32.12.2	M	Yes [ ]	33 bit times
TMU4	MDI input to MDI output = Jam (worst-case collision response)	32.12.2	M	Yes [ ]	50 bit times

32.13.5.14 Timing requirements: carrier assertion/deassertion constraint

Item	Feature	Subclause	Status	Support	Value/Comment
TMC1	Each DTE shall satisfy the relationship	36.5.3	M	Yes [ ]	(MAX MDI to MAC Carrier Deassert Detect)–(MIN MDI to MAC Carrier Assert Detect).

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33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

33.1 Overview

This clause defines the functional and electrical characteristics of two optional power (non-data) entities, a Powered Device (PD) and Power Sourcing Equipment (PSE), for use with the MAU defined in Clause 14 and the PHYs defined in Clause 25 and Clause 40. These entities allow devices to draw/supply power using the same generic cabling as is used for data transmission.

DTE powering is intended to provide a 10BASE-T, 100BASE-TX, or 1000BASE-T device with a single interface to both the data it requires and the power to process this data. This clause specifies the following:

a) A power source to add power to the 100 Ω balanced cabling system
b) The characteristics of a powered device's load on the power source and the structured cabling
c) A protocol allowing the detection of a device that requests power from a PSE
d) Methods to classify devices based on their power needs
e) A method for powered devices and power sourcing equipment to dynamically negotiate and allocate power
f) A method for scaling supplied power back to the detect level when power is no longer requested or required

The importance of item c) above should not be overlooked. Given the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected to a 100 Ω balanced cabling system, and the possible consequences of applying power to such devices, the protocol to distinguish compatible devices and non-compatible devices is important to prevent damage to non-compatible devices.

The detection and powering algorithms are likely to be compromised by cabling that is not point-to-point, resulting in unpredictable performance and possibly damaged equipment.

This clause differentiates between the two ends of the powered portion of the link, defining the PSE and the PD as separate but related devices.

33.1.1 Objectives

The following are objectives of Power via MDI:

a) *Power*—A PD designed to the standard, and within its range of available power, can obtain both power and data for operation through the MDI and therefore needs no additional connections.

b) *Safety*—A PSE designed to the standard does not introduce non-SELV (Safety Extra Low Voltage) power into the wiring plant.

c) *Compatibility*—Clause 33 utilizes the MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification. Type 1 operation adds no significant requirements to the cabling. Type 2 operation requires ISO/IEC 11801:1995 Class D or better cabling and a derating of the cabling maximum ambient operating temperature. The clause does not address the operation of 10GBASE-T. For 10GBASE-T operation, the channel model specified in Clause 55 needs to be met without regard to DTE Power via MDI presence or operation.

d) *Simplicity*—The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, or 1000BASE-T.

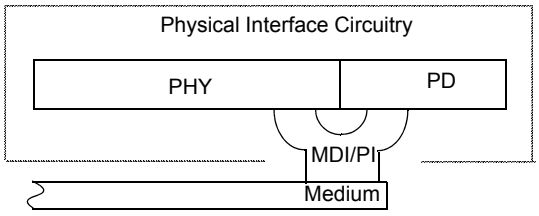
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33.1.2 Compatibility considerations

All implementations of PD and PSE systems shall be compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of Clause 33 where appropriate. Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

33.1.3 Relationship of DTE Power via MDI to the IEEE 802.3 Architecture

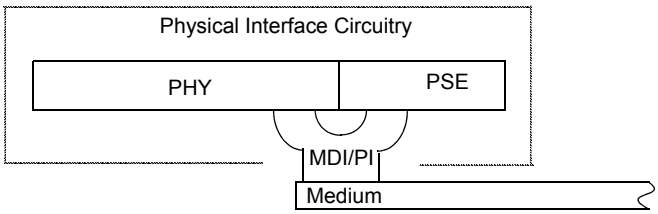
DTE Power via MDI comprises an optional non-data entity. As a non-data entity, it does not appear in a depiction of the OSI Reference Model. Figure 33–1 depicts the positioning of DTE Power via MDI in the case of the PD.



MDI = Medium Dependent Interface
PD = Powered Device
PHY = Physical Layer Device
PI = Power Interface

Figure 33–1—DTE Power via MDI powered device relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

Figure 33–2 and Figure 33–3 depict the positioning of DTE Power via MDI in the cases of the Endpoint PSE and the Midspan PSE, respectively.



MDI = Medium Dependent Interface
PHY = Physical Layer Device
PI = Power Interface
PSE = Power Sourcing Equipment

Figure 33–2—DTE Power via MDI Endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

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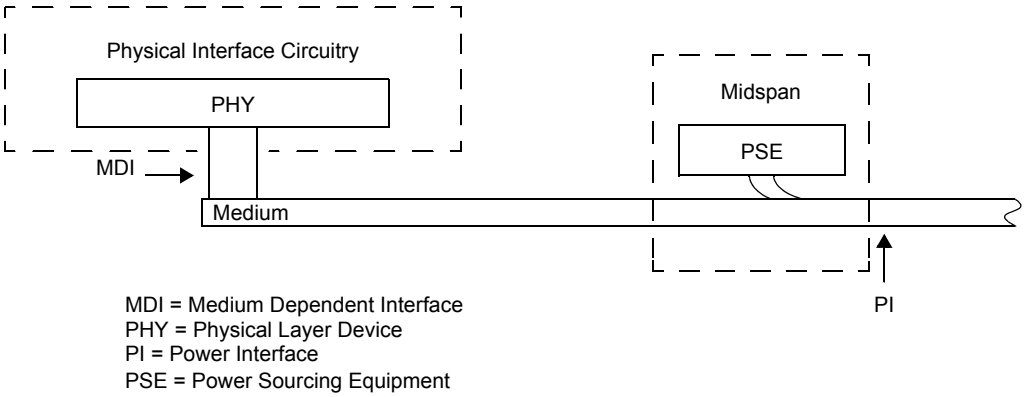


Figure 33–3—DTE Power via MDI Midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

The Power Interface (PI) is the generic term that refers to the mechanical and electrical interface between the PSE or PD and the transmission medium.

In an Endpoint PSE and in a PD, the PI is encompassed within the MDI.

PSE power interface specifications that are defined at the MDI apply to an Endpoint PSE. They may or may not apply to a Midspan PSE PI.

33.1.4 Type 1 and Type 2 system parameters

A power system, consisting of a single PSE, link segment, and a single PD, defined as either Type 1 or Type 2, has certain basic parameters defined according to Table 33–1. These parameters define not only certain performance characteristics of the system, but are also used in calculating the various electrical characteristics of PSEs and PDs as described in 33.2 and 33.3.

Table 33–1—Type 1 and Type 2 system parameters

Parameter	Symbol	Units	Type 1 value	Type 2 value	Additional information
Nominal highest DC current per pair	I_{Cable}	A	0.350	0.600	
Channel maximum DC pair loop resistance	R_{Ch}	Ω	20.0	12.5	
Minimum cable type			twisted-pair cabling per 14.4 and 14.5[a]	Class D	See 33.1.4.1, 33.1.4.2

[a]Class D recommended.

I_{Cable} is the current on one twisted pair in the multi-twisted pair cable. Two twisted pairs are required to source I_{Cable}—one carrying (+ I_{Cable}) and one carrying (– I_{Cable}), from the perspective of the PI.

It should be noted that the cable references use "DC loop resistance," which refers to a single conductor. This clause uses "DC pair loop resistance," which refers to a pair of conductors in parallel. Therefore, R_{Ch} is related to, but not equivalent to, the "DC loop resistance" called out in the cable references.

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33.1.4.1 Type 2 cabling requirement

Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995 with the additional requirement that channel DC loop resistance shall be 25 Ω or less. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA-568-C.2; or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A.

Under worst-case conditions, Type 2 operation requires a 10 °C reduction in the maximum ambient operating temperature of the cable when all cable pairs are energized at I_{Cable} (see Table 33–1), or a 5 °C reduction in the maximum ambient operating temperature of the cable when half of the cable pairs are energized at I_{Cable}. Additional cable ambient operating temperature guidelines for Type 2 operation are provided in ISO/IEC TR 29125 [B48][20] and TIA TSB-184 [B60].

33.1.4.2 Type 1 and Type 2 channel requirement

Type 1 and Type 2 operation requires that the resistance unbalance shall be 3% or less. Resistance unbalance is a measure of the difference between the two conductors of a twisted pair in the 100 Ω balanced cabling system. Resistance unbalance is defined as in Equation (33–1):

$$\left.\frac{(R_{max} - R_{min})}{(R_{max} + R_{min})} \times 100 \right\}_{\%} \tag{33–1}$$

where

R_{max} is the resistance of the channel conductor with the highest resistance
R_{min} is the resistance of the channel conductor with the lowest resistance

33.2 Power sourcing equipment (PSE)

The PSE is the portion of the end station or midspan equipment that provides the power to a single PD. The PSE's main functions are as follows:

— To search the link section for a PD
— To supply power to the detected PD through the link section
— To monitor the power on the link section
— To remove power when no longer requested or required, returning to the searching state

An unplugged link section is one instance when power is no longer required. In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD.

A PSE is electrically specified at the point of the physical connection to the cabling.

33.2.1 PSE location

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater or midspan. A PSE that is coincident with the DTE/Repeater is an "Endpoint PSE." A PSE that is located within a link segment that is distinctly separate from and between the MDIs is a "Midspan PSE." The requirements of this document shall apply equally to Endpoint and Midspan PSEs unless the requirement contains an explicit statement that it applies to only one implementation. The location of

[20]The numbers in brackets correspond to those of the bibliography in Annex A.

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Alternative A and Alternative B Endpoint PSEs and Midspan PSEs are illustrated in Figure 33–4, Figure 33–5, Figure 33–6, and Figure 33–7.

PSEs can be compatible with 10BASE-T, 100BASE-TX, and/or 1000BASE-T. PSEs may support either Alternative A, Alternative B, or both.

33.2.2 Midspan PSE types

There are two types of Midspan PSEs defined.

10BASE-T/100BASE-TX Midspan PSE:
: A Midspan PSE that results in a link that can support only 10BASE-T and 100BASE-TX operation (see Figure 33–6). Note that this limitation is due to the presence of the Midspan PSE whether it is supplying power or not.

1000BASE-T Midspan PSE:
: A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see Figure 33–7).

NOTE—See 33.4.9.2 for Alternative A Midspan PSEs.

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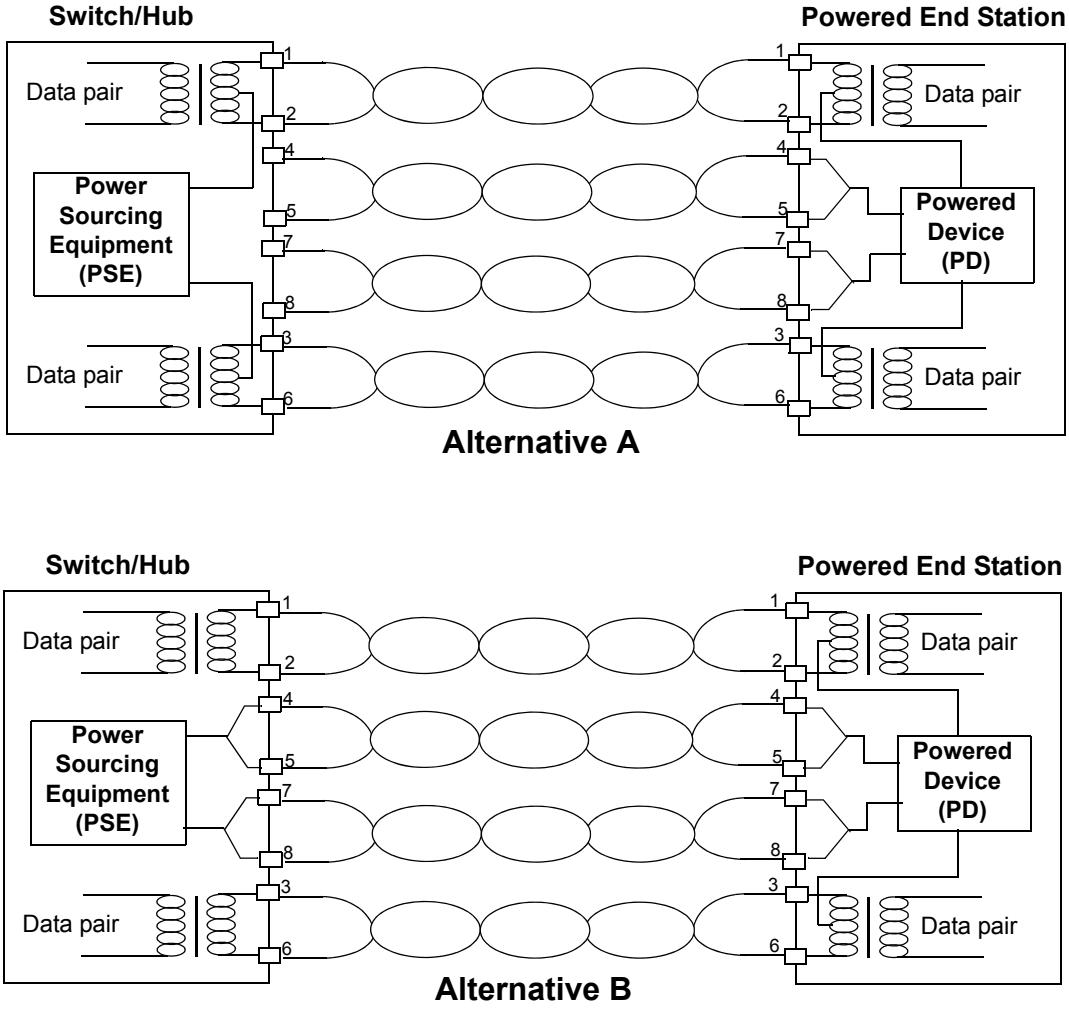


Figure 33–4—10BASE-T/100BASE-TX Endpoint PSE location overview

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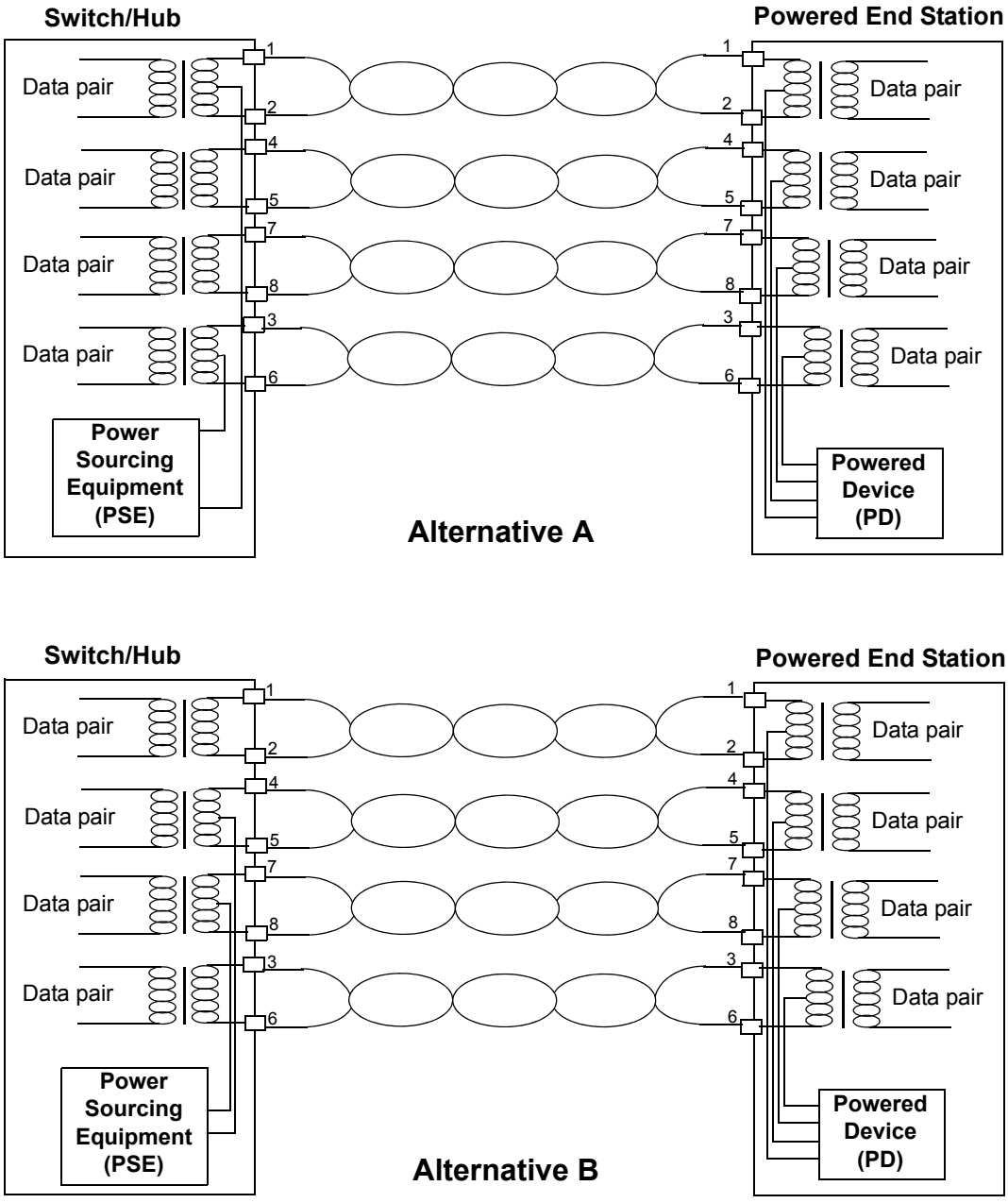


Figure 33–5—1000BASE-T Endpoint PSE location overview

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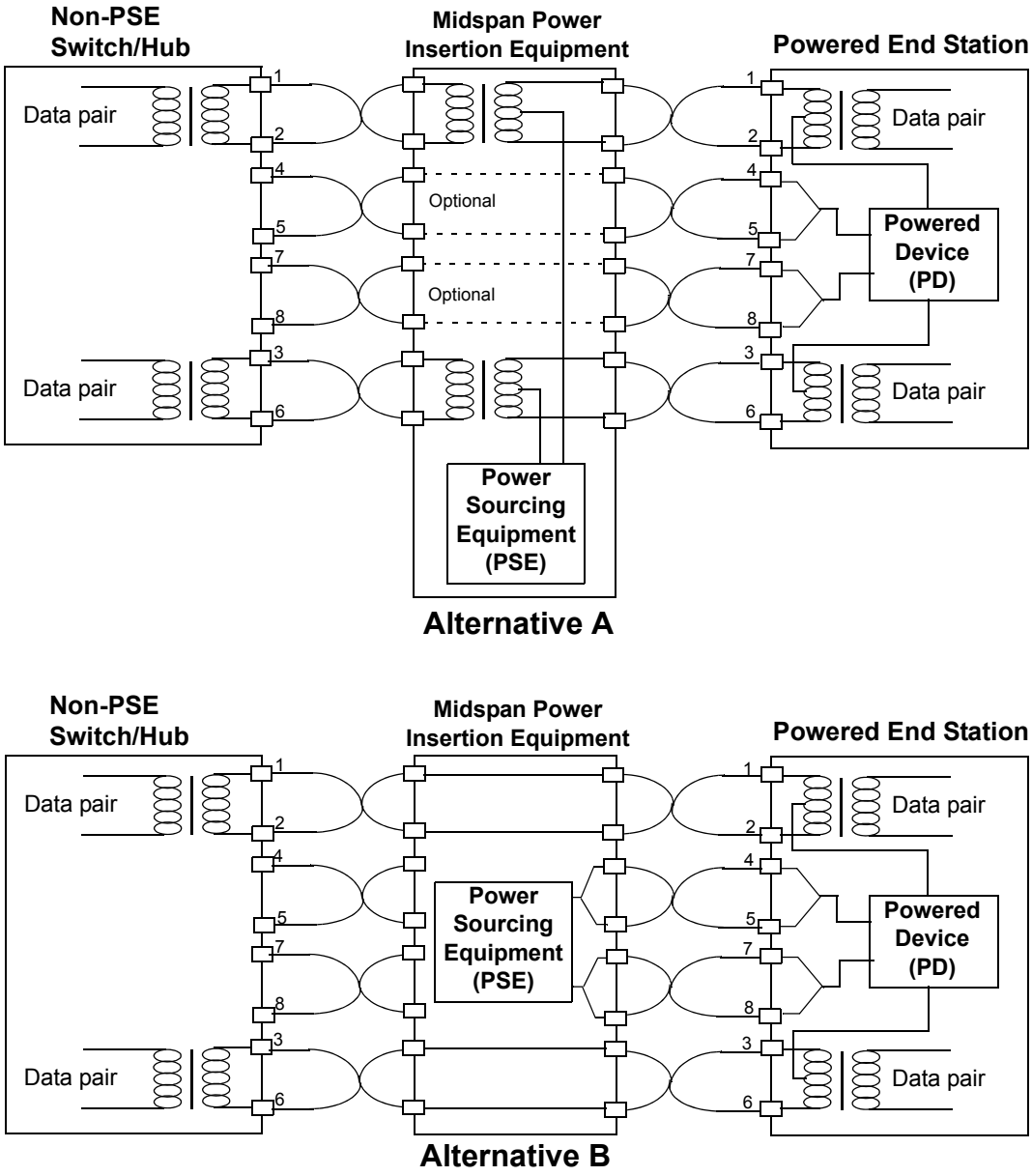


Figure 33–6—10BASE-T/100BASE-TX Midspan PSE location overview

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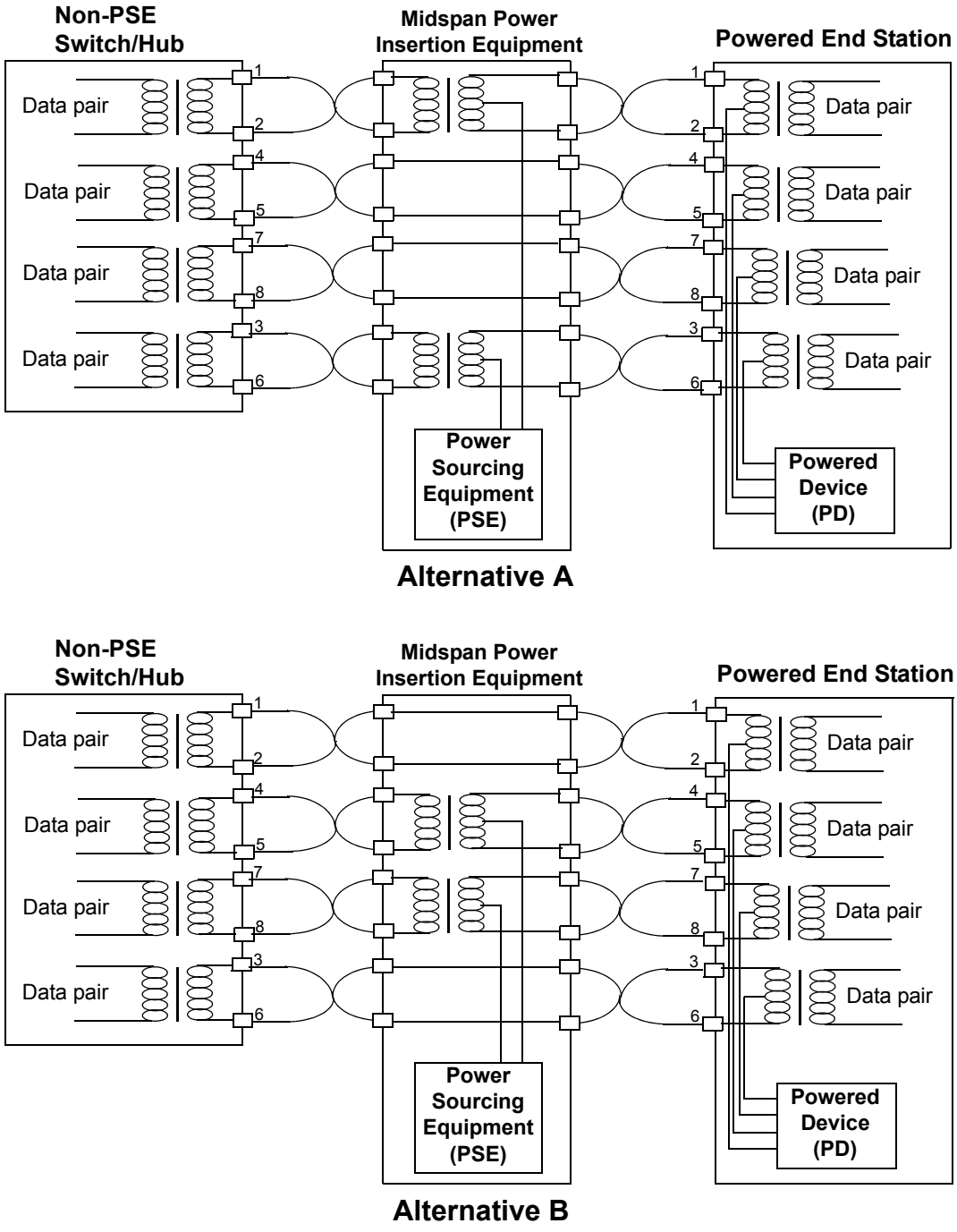


Figure 33–7—1000BASE-T Midspan PSE location overview

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33.2.3 PI pin assignments

A PSE device may provide power via one of two valid four-wire connections. In each four-wire connection, the two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 33–8, in conjunction with Table 33–2, illustrates the valid alternatives.

Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

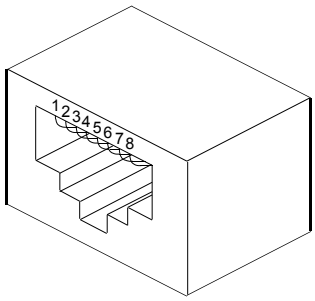


Figure 33–8—PD and PSE eight-pin modular jack

For the purposes of data transfer, the type of PSE data port is relevant to the far-end PD, and in some cases, to the cabling system between them. Therefore, Alternative A matches the positive voltage to the transmit pair of the PSE. PSEs that use automatically-configuring MDI/MDI-X ("Auto MDI-X") ports may choose either polarity choice associated with Alternative A configurations. For further information on the placement of MDI vs. MDI-X, see 14.5.2.

A PSE shall implement Alternative A, Alternative B, or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously.

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33.2.4 PSE state diagrams

The PSE shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10.

33.2.4.1 Overview

Detection, classification, and power turn-on timing shall meet the specifications in Table 33–4, Table 33–10, and Table 33–11.

If power is to be applied, the PSE turns on power after a valid detection in less than T_{pon} as specified in Table 33–11. If the PSE cannot supply power within T_{pon}, it initiates and successfully completes a new detection cycle before applying power.

It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 33.2.1), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

A PSE performing detection using Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE backs off for at least T_{dbo} as specified in Table 33–11 before attempting another detection. During this backoff, the PSE shall not apply a voltage greater than V_{Off} to the PI.

If a PSE performing detection using Alternative B detects an open circuit (see 33.2.5.5) on the link section, then that PSE may optionally omit the detection backoff.

If a PSE performing detection using Alternative A detects an invalid signature, it should complete a second detection in less than T_{dbo} min after the beginning of the first detection attempt. This allows an Alternative A PSE to complete a successful detection cycle prior to an Alternative B PSE present on the same link section that may have caused the invalid signature.

NOTE—A Type 1 PSE performing detection using Alternative A may need to have its DTE powering ability disabled when it is attached to the same link segment as a Type 2 Midspan PSE performing detection using Alternative B. This allows the Midspan PSE to successfully complete a detection cycle.

33.2.4.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.2.4.3 Constants

The PSE state diagrams use the following constants:

PSE_TYPE
A constant indicating the type of the PSE
Values:1: Type 1 PSE
2: Type 2 PSE

33.2.4.4 Variables

The PSE state diagrams use the following variables:

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class_num_events

A variable indicating the number of classification events performed by the PSE. A variable that is set in an implementation-dependent manner.

Values:0: PSE does not perform Physical Layer classification.
1: PSE performs 1-Event Physical Layer classification.
2: PSE performs 2-Event Physical Layer classification.

error_condition

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 33–11 and that require the PSE not to source power. These error conditions are different from those monitored by the state diagrams in Figure 33–10.

Values:FALSE:No fault indication.
TRUE:A fault indication exists.

I_{Inrush}

Output current during POWER_UP (see Table 33–11 and Figure 33–13).

I_{Port}

Output current (see 33.2.7.6).

legacy_powerup

This variable is provided for PSEs that monitor the PI voltage output and use that information to indicate the completion of PD inrush current during POWER_UP operation. Using only the PI voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed T_{Inrush} period is recommended. A variable that is set in an implementation-dependent manner.

Values:TRUE:The PSE supports legacy power up; this value is not recommended.
FALSE:The PSE does not support legacy power up. It is highly recommended that new equipment use this value.

mr_mps_valid

The PSE monitors either the DC or AC Maintain Power Signature (MPS, see 33.2.9.1). This variable indicates the presence or absence of a valid MPS.

Values:FALSE:If monitoring both components of the MPS, the DC component of MPS is absent or the AC component of MPS is absent. If monitoring only one component of MPS, that component of MPS is absent.
TRUE: If monitoring both components of the MPS, the DC component of MPS and the AC component of MPS are both present. If monitoring only one component of MPS, that component of MPS is present.

mr_pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values:A: The PSE uses PSE pinout Alternative A.
B: The PSE uses PSE pinout Alternative B.

mr_pse_enable

A control variable that selects PSE operation and test functions. This variables is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent functions.

Values:disable: All PSE functions disabled (behavior is as if there was no PSE functionality). This value corresponds to MDIO register bits 11.1:0 = '00'.
enable: Normal PSE operation. This value corresponds to MDIO register bits 11.1:0 = '01'.
force_power:Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = '10'.

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option_detect_ted

This variable indicates if detection can be performed by the PSE during the ted_timer interval.

Values:FALSE:Do not perform detection during ted_timer interval.

TRUE:Perform detection during ted_timer interval.

option_vport_lim

This optional variable indicates if V_{PSE} is out of the operating range during normal operating state.

Values:FALSE:V_{PSE} is within the V_{Port_PSE} operating range as defined in Table 33–11.

TRUE:V_{PSE} is outside of the V_{Port_PSE} operating range as defined in Table 33–11.

ovld_detected

A variable indicating if the PSE output current has been in an overload condition (see 33.2.7.6) for at least T_{CUT} of a one second sliding time.

Values:FALSE:The PSE has not detected an overload condition.

TRUE:The PSE has detected an overload condition.

pd_dll_power_type

A control variable output by the PSE power control state diagram (Figure 33–27) that indicates the type of PD as advertised through Data Link Layer classification.

Values:1: PD is a Type 1 PD (default)

2: PD is a Type 2 PD

pi_powered

A variable that controls the circuitry that the PSE uses to power the PD.

Values:FALSE:The PSE is not to apply power to the link (default).

TRUE:The PSE has detected a PD, classified it if applicable, and determined the PD is to be powered; or power is being forced on in TEST_MODE.

power_applied

A variable indicating that the PSE has begun steady state operation by having asserted pi_powered, completed the ramp of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 33.2.7.5.

Values:FALSE:The PSE is either not applying power or has begun applying power but is still in POWER_UP.

TRUE:The PSE has begun steady state operation.

power_not_available

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values:FALSE:PSE is capable to continue to source power to a PD.

TRUE:PSE is no longer capable of sourcing power to a PD.

pse_available_power

This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.

Values:0: Class 1

1: Class 2

2: Class 0 and Class 3

3: Class 4

pse_dll_capable

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 33.6. This variable is provided by a management interface that may be mapped to the PSE Control register Data Link Layer Classification Capability bit (11.5), as described below, or other equivalent functions. A variable that is set in an implementation-dependent manner.

Values:FALSE:The PSE's Data Link Layer classification capability is not enabled.

TRUE:The PSE's Data Link Layer classification capability is enabled.

pse_dll_enabled

A variable indicating whether the Data Link Layer classification mechanism is enabled. See 33.6.

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Values:FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

pse_ready
Variable that is asserted in an implementation-dependent manner to probe the link segment.
Values:FALSE:PSE is not ready to probe the link segment.
TRUE:PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid signature is detected due to the delay it introduces between detection attempts (see 33.2.4.1).

pse_reset
Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.
Values:FALSE:Do not reset the PSE state diagram.
TRUE:Reset the PSE state diagram.

pse_skips_event2
The PSE can choose to bypass a portion of the classification state flow. A variable that is set in an implementation-dependent manner.
Values:FALSE:The PSE does not bypass MARK_EV1.
TRUE:The PSE does bypass MARK_EV1.

short_detected
A variable indicating if the PSE output current has been in a short circuit condition for T_{LIM} within a sliding window (see 33.2.7.7).
Values:FALSE:The PSE has not detected a short circuit condition.
TRUE:The PSE has detected qualified short circuit condition.

temp_var
A temporary variable used to store the value of the state variable mr_pd_class_detected.

PSEs shall meet at least one of the allowable variable definition permutations described in Table 33–3.

Table 33–3—Allowed PSE variable definition permutations

PSE Type	Variables	
	class_num_events	**pse_dll_capable**
Type 2	2	FALSE
		TRUE
	1	TRUE
Type 1	1	FALSE
		TRUE
	0	FALSE
		TRUE

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33.2.4.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where “stop x_timer” is asserted.

tcle1_timer
: A timer used to limit the first classification event time in 2-Event classification; see T_{CLE1} in Table 33–10.

tcle2_timer
: A timer used to limit the second classification event time in 2-Event classification; see T_{CLE2} in Table 33–10.

tdbo_timer
: A timer used to regulate backoff upon detection of an invalid signature; see T_{dbo} in Table 33–11.

tdet_timer
: A timer used to limit an attempt to detect a PD; see T_{det} in Table 33–11.

ted_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_done.

tinrush_timer
: A timer used to monitor the duration of the inrush event; see T_{Inrush} in Table 33–11.

tme1_timer
: A timer used to limit the first mark event time in 2-Event classification; see T_{ME1} in Table 33–10.

tme2_timer
: A timer used to limit the second mark event time in 2-Event classification; see T_{ME2} in Table 33–10.

tmpdo_timer
: A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 33–11.

tpdc_timer
: A timer used to limit the classification time; see T_{pdc} in Table 33–10.

tpon_timer
: A timer used to limit the time for power turn-on; see T_{pon} in Table 33–11.

33.2.4.6 Functions

do_classification
: This function returns the following variables:

  pd_requested_power: This variable indicates the power class requested by the PD. A Type 1 PSE that measures a Class 4 signature assigns that PD to Class 0. See 33.2.6.

  Values:
  - 0: Class 1
  - 1: Class 2
  - 2: Class 0 or Class 3
  - 3: Class 4

  mr_pd_class_detected: The class of the PD associated with the PD classification signature; see Table 33–7 and 33.2.6.

  Values:
  - 0: Class 0
  - 1: Class 1
  - 2: Class 2
  - 3: Class 3
  - 4: Class 4

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do_detection

This function returns the following variables:

signature:

This variable indicates the presence or absence of a PD.

Values: open_circuit:The PSE has detected an open circuit. This value is optionally returned by a PSE performing detection using Alternative B.
valid: The PSE has detected a PD requesting power.
invalid: Neither open_circuit, nor valid PD detection signature has been found.

mr_valid_signature:

This variable indicates that the PSE has detected a valid signature.

Values: FALSE: No valid signature detected.
TRUE: Valid signature detected.

do_mark

This function produces the classification mark event voltage. This function does not return any variables.

set_parameter_type

This function is used by a Type 2 PSE to evaluate the type of PD connected to the link based on Physical Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements defined in Table 33–11 are set to values corresponding to either a Type 1 or Type 2 PSE. This function returns the following variable:

parameter_type: A variable used by a Type 2 PSE to pick between Type 1 and Type 2 PI electrical requirement parameter values defined in Table 33–11.

Values: 1: Type 1 PSE parameter values (default)
2: Type 2 PSE parameter values

When a Type 2 PSE powers a Type 2 PD, the PSE may choose to assign a value of '1' to parameter_type if mutual identification is not complete (see 33.2.6) and shall assign a value of '2' to parameter_type if mutual identification is complete.

When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type} (see Table 33–11).

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33.2.4.7 State diagrams

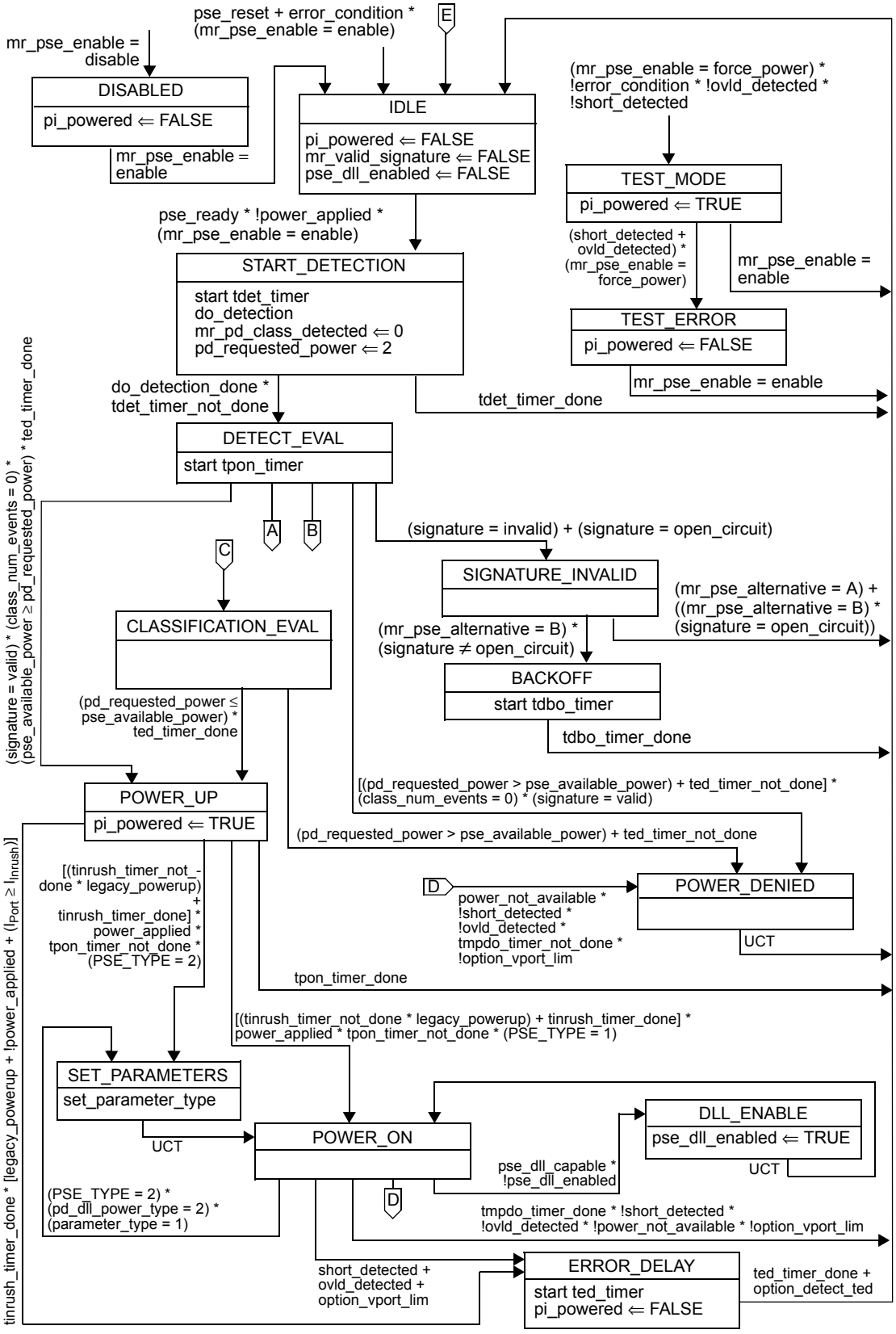


Figure 33–9—PSE state diagram

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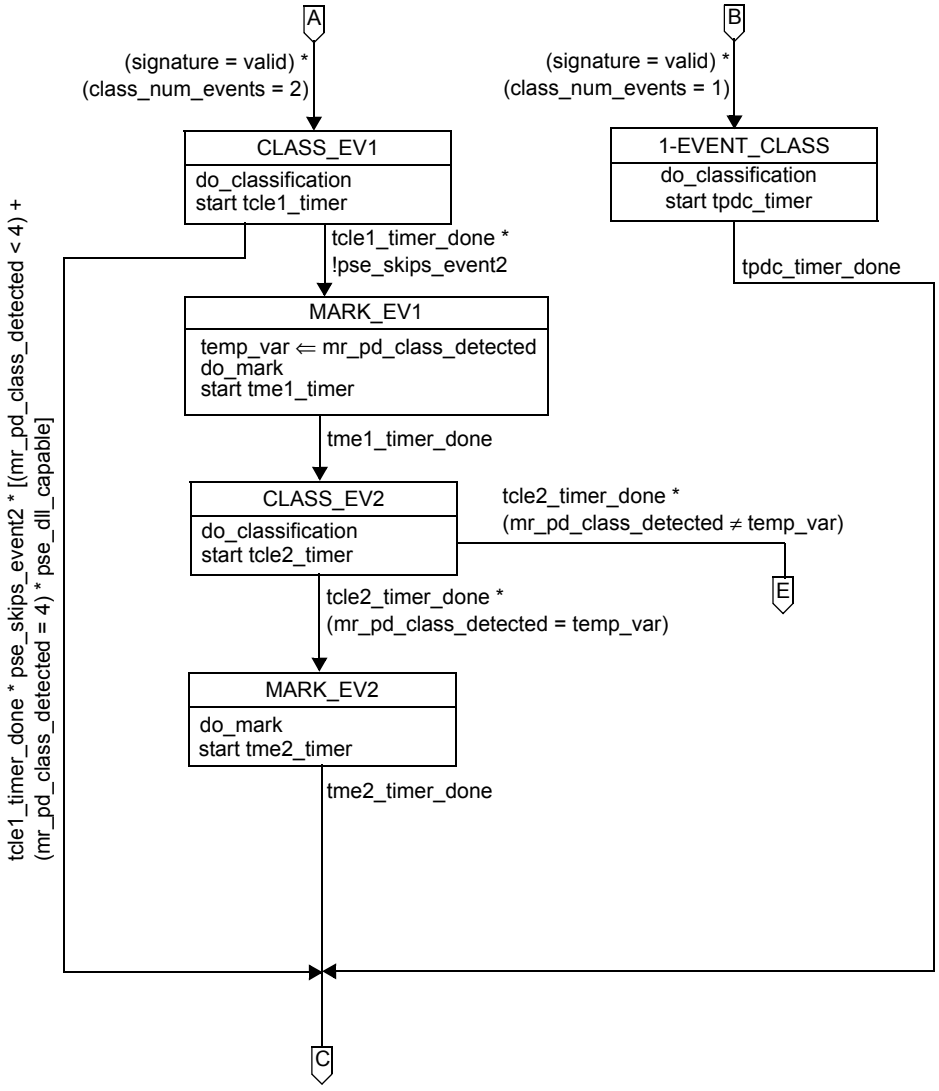


Figure 33–9—PSE state diagram *(continued)*

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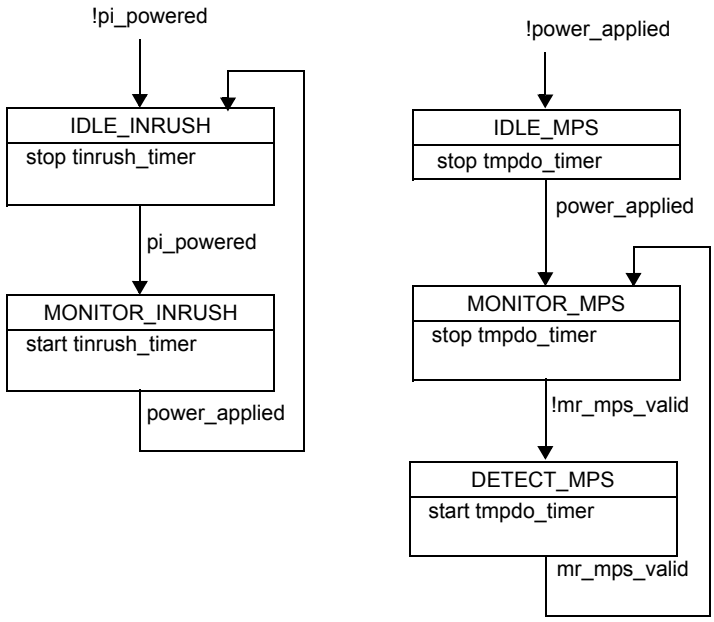


Figure 33–10—PSE monitor inrush and monitor MPS state diagrams

33.2.5 PSE detection of PDs

In any operational state, the PSE shall not apply operating power to the PI until the PSE has successfully detected a PD requesting power.

The PSE probes the link section in order to detect a valid PD detection signature. The PSE PI is connected to a PD through a link segment. In the following subclauses, the link is not called out to preserve clarity.

The PSE is not required to continuously probe to detect a PD signature. The period of time when a PSE is not attempting to detect a PD signature is implementation dependent. Also, a PSE may successfully detect a PD but then opt not to power the detected PD.

The PSE shall turn on power only on the same pairs as those used for detection.

33.2.5.1 PSE detection validation circuit

The PSE shall detect the PD by probing via the PSE PI. The PSE shall present a non-valid PD detection signature as defined in Table 33–15 when probed in either polarity by another PSE. An illustrative embodiment of a detection circuit is shown in Figure 33–11.

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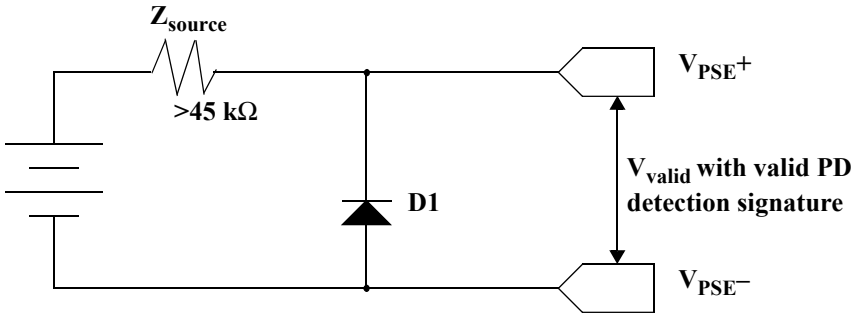


Figure 33–11—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation but restricts the PSE detection circuit to the first quadrant is shown in Figure 33–12.

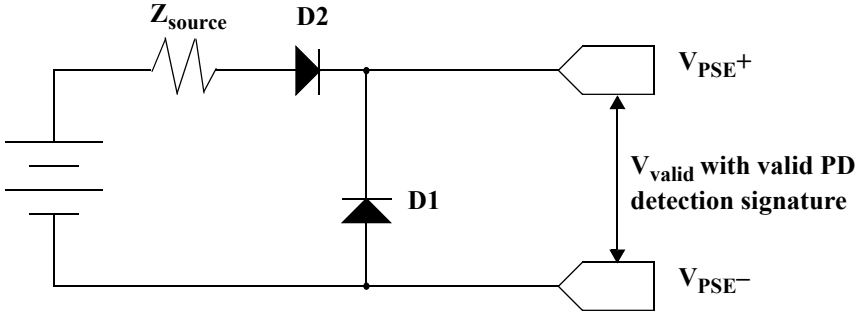


Figure 33–12—Alternative PSE detection source

In Figure 33–11 and Figure 33–12, the diode D1 presents a non-valid PD detection signature for a reversed voltage PSE to PSE connection.

The open circuit voltage and short circuit current shall meet the specifications in Table 33–4. The PSE shall not be damaged by up to 5 mA backdriven current over the range of V_{oc} as specified in Table 33–4. Output capacitance shall be as specified in Table 33–11.

Table 33–4—PSE PI detection state electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{oc}	V		30.0	In detection state only
2	Short circuit current	I_{sc}	A		0.005	In detection state only
3	Valid test voltage	V_{valid}	V	2.80	10.0	—
4	Voltage difference between test points	ΔV_{test}	V	1.00		—
5	Slew rate	V_{slew}	V/μs		0.100	—

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33.2.5.2 Detection probe requirements

The detection voltage at the PSE PI shall be within the V_{valid} voltage range (as specified in Table 33–4) with a valid PD detection signature connected (as specified in Table 33–14).

In evaluating the presence of a valid PD, the PSE shall make at least two measurements with V_{PSE} values that create at least a ΔV_{test} difference as specified in Table 33–4. An effective resistance is calculated from two voltage/current measurements made during the detection process.

The resistance is calculated with Equation (33–2):

$$R = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \quad (33–2)$$

where

V_1 and V_2 are the first and second voltage measurements made at the PSE PI, respectively
I_1 and I_2 are the first and second current measurements made at the PSE PI, respectively
R is the effective resistance

Attached PI capacitance may be determined using these measurements and the port RC time-constant charging characteristics.

NOTE—Settling time before voltage or current measurement: the voltage or current measurement should be taken after V_{PSE} has settled to within 1% of its steady state condition with a valid PD detection signature connected (as specified in Table 33–14).

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than V_{slew} as specified in Table 33–4.

33.2.5.3 Detection criteria

A PSE shall accept as a valid signature a link section with both of the following characteristics between the powering pairs with an offset voltage up to V_{os} max and an offset current up to I_{os} max, as specified in Table 33–5:

a) Signature resistance R_{good}, and
b) Parallel signature capacitance C_{good}.

Table 33–5—Valid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Accept signature resistance	R_{good}	kΩ	19.0	26.5	—
2	Accept signature capacitance	C_{good}	µF		0.150	—
3	Signature offset voltage tolerance	V_{os}	V	0	2.00	—
4	Signature offset current tolerance	I_{os}	µA	0	12.0	—

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CAUTION

In a multiport system, the implementer should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents.

33.2.5.4 Rejection criteria

The PSE shall reject link sections as having an invalid signature, when those link sections exhibit any of the following characteristics between the powering pairs, as specified in Table 33–6:

a) Resistance less than or equal to R_{bad} min, or
b) Resistance greater than or equal to R_{bad} max, or
c) Capacitance greater than or equal to C_{bad} min.

A PSE may accept or reject a signature resistance in the band between R_{good} min and R_{bad} min, and in the band between R_{good} max and R_{bad} max. A PSE may accept or reject a parallel signature capacitance in the band between C_{good} max and C_{bad} min.

In instances where the resistance and capacitance meet the detection criteria, but one or both of the offset tolerances are exceeded, the detection behavior of the PSE is undefined.

Table 33–6—Invalid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Reject signature resistance	R_{bad}	kΩ	15.0	33.0	—
2	Reject signature capacitance	C_{bad}	µF	10.0		—
3	Open circuit resistance	R_{open}	MΩ	0.500		—

33.2.5.5 Open circuit criteria

If a PSE that is performing detection using Alternative B (see 33.2.3) determines that the impedance at the PI is greater than R_{open} as defined in Table 33–4, it may optionally consider the link to be open circuit and omit the tdbo_timer interval.

33.2.6 PSE classification of PDs and mutual identification

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a Type 2 PD to differentiate Type 1 PSEs from Type 2 PSEs. Additionally, mutual identification allows Type 2 PSEs to differentiate between Type 1 and Type 2 PDs. PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices.

There are two forms of classification: Physical Layer classification and Data Link Layer classification.

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Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto the PI and the PD responds with a current representing a limited number of power classifications. Based on the response of the PD, the minimum power level at the output of the PSE is P_{Class} as shown in Equation (33–3). Physical Layer classification encompasses two methods, known as 1-Event Physical Layer classification (see 33.2.6.1) and 2-Event Physical Layer classification (see 33.2.6.2).

The minimum power output by the PSE for a particular PD class is defined by Equation (33–3). Alternatively, PSE implementations may use $V_{PSE} = V_{Port\_PSE}$ min and $R_{Chan} = R_{Ch}$ max to arrive at over-margined values as shown in Table 33–7.

$$P_{Class} = \left\{ V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) \right\}_W \quad (33–3)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4.426
R_{Chan} is the channel DC pair loop resistance
P_{Class_PD} is the PD's power classification (see Table 33–18)

Table 33–7—Physical Layer power classifications (P_{Class})

Class	Minimum power levels at output of PSE (P_{Class})
0	15.4 Watts
1	4.00 Watts
2	7.00 Watts
3	15.4 Watts
4	P_{Type} as defined in Table 33–11
NOTE 1—This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33–18. NOTE 2—Data Link Layer classification takes precedence over Physical Layer classification.	

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see 33.6) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation.

A PSE shall meet one of the allowable classification permutations listed in Table 33–8.

Subsequent to successful detection, a Type 1 PSE may optionally classify a PD using 1-Event Physical Layer classification. Valid classification results are Classes 0, 1, 2, 3, and 4, as listed in Table 33–7. If a Type 1 PSE does not implement classification, then the Type 1 PSE shall assign all PDs to Class 0. A Type 1 PSE may optionally implement Data Link Layer classification.

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Table 33–8—PSE and PD classification permutations

Permutations			PSE allowed?	PD allowed?
PSE/PD Type	Physical Layer classification	Data Link Layer classification		
Type 2	2-Event	No	Yes	No
		Yes	Yes	Yes
	1-Event	No	No	No
		Yes	Yes	No
	None	No	No	No
		Yes	No	No
Type 1	2-Event	No	No	Yes
		Yes	No	Yes
	1-Event	No	Yes	Yes
		Yes	Yes	Yes
	None	No	Yes	No
		Yes	Yes	No

Subsequent to successful detection, all Type 2 PSEs perform classification using at least one of the following: 2-Event Physical Layer classification; 2-Event Physical Layer classification and Data Link Layer classification; or 1-Event Physical Layer classification and Data Link Layer classification.

If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall either return to the IDLE state or assign the PD to Class 0; a Type 2 PSE shall return to the IDLE state.

33.2.6.1 PSE 1-Event Physical Layer classification

When 1-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a single classification event—1-EVENT_CLASS—as defined in the state diagram in Figure 33–9.

The PSE shall provide to the PI V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–10. Polarity shall be the same as defined for V_{Port_PSE} in 33.2.3 and timing specifications shall be as defined by T_{pdc} in Table 33–10.

The PSE shall measure the resultant I_{Class} and classify the PD based on the observed current according to Table 33–9. All measurements of I_{Class} shall be taken after the minimum relevant class event timing in Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the measured I_{Class} is within the range of I_{Class_LIM}, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2 PSE shall return to the IDLE state.

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33.2.6.2 PSE 2-Event Physical Layer classification

When 2-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a series of classification and mark events—CLASS_EV1, MARK_EV1, CLASS_EV2, and MARK_EV2—as defined in the state diagram in Figure 33–9.

The PSE in the state CLASS_EV1 shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{CLE1} in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV1, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV2, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE2} timing specification, as defined in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME2} in Table 33–10.

The mark event states, MARK_EV1 and MARK_EV2, commence when the PI voltage falls below V_{Class} min and end when the PI voltage exceeds V_{Class} min. The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 33–17.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min as defined in Table 33–10, a Type 2 PSE shall return to the IDLE state. The class events shall meet the I_{Class_LIM} current limitation. The mark events shall meet the I_{Mark_LIM} current limitation. All measurements of I_{Class} shall be taken after the minimum relevant class event timing of Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for V_{Port_PSE} in 33.2.3. The PSE shall complete 2-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI to go below V_{Mark} min. If the PSE returns to the IDLE state, it shall maintain the PI voltage at V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle.

If the result of the first class event is Class 4, the PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the result of the first class event is any of Classes 0, 1, 2, or 3, the PSE treats the PD as a Type 1 PD and may omit the subsequent mark and class events and classify the PD according to the result of the first class event.

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Table 33–9—PD classification

Measured I_{Class}	Classification
0 mA to 5.00 mA	Class 0
> 5.00 mA and < 8.00 mA	May be Class 0 or 1
8.00 mA to 13.0 mA	Class 1
> 13.0 mA and < 16.0 mA	Either Class 1 or 2
16.0 mA to 21.0 mA	Class 2
> 21.0 mA and < 25.0 mA	Either Class 2 or 3
25.0 mA to 31.0 mA	Class 3
> 31.0 mA and < 35.0 mA	Either Class 3 or 4
35.0 mA to 45.0 mA	Class 4
> 45.0 mA and < 51.0 mA	Either Class 4 or invalid class

NOTE—A Type 1 PSE may ignore I_{Class} and report Class 0.

Table 33–10—PSE Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	1- or 2-Event	Additional information
1	Class event voltage	V_{Class}	V	15.5	20.5	1, 2	
2	Class event current limitation	I_{Class_LIM}	A	0.051	0.100	1, 2	
3	Mark event voltage	V_{Mark}	V	7.00	10.0	2	
4	Mark event current limitation	I_{Mark_LIM}	A	0.005	0.100	2	
5	1st class event timing	T_{CLE1}	ms	6.00	30.0	2	
6	1st mark event timing	T_{ME1}	ms	6.00	12.0	2	
7	2nd class event timing	T_{CLE2}	ms	6.00	30.0	2	
8	2nd mark event timing	T_{ME2}	ms	6.00		2	Time from end of detection until power-on is limited by 33.2.7.12.
9	Classification reset voltage	V_{Reset}	V	0	2.80	2	
10	Classification reset timing	T_{Reset}	ms	15.0		2	
11	1-Event Physical Layer classification timing	T_{pdc}	ms	6.00	75.0	1	

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33.2.7 Power supply output

PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9 continued, and Figure 33–10. When the PSE provides power to the PI, it shall conform with Table 33–11.

Table 33–11 limits show values that support worst-case operating limits. These ranges may be narrowed when additional information is known and applied in accordance with this specification.

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
1	Output voltage in the POWER_ON state	V_{Port_PSE}	V	44.0	57.0	1	See 33.2.7.1.
				50.0	57.0	2	
2	Voltage transient below V_{Port_PSE} min	K_{Tran_lo}	%		7.6	2	See 33.2.7.2.
3	Power feeding ripple and noise:						
	f < 500 Hz		V_{pp}		0.500	1, 2	See 33.2.7.3.
	500 Hz to 150 kHz				0.200		
	150 kHz to 500 kHz				0.150		
	500 kHz to 1 MHz				0.100		
4	Continuous output current capability in POWER_ON state	I_{Con}	A	P_{Class} / V_{Port_PSE}		1, 2	See 33.2.7.4.
5	Output current in POWER_UP state	I_{Inrush}	A	0.400	See info	1, 2	See 33.2.7.5. Max value defined by Figure 33–13.
6	Inrush time	T_{Inrush}	s	0.050	0.075	1, 2	See 33.2.7.5
7	Overload current detection range	I_{CUT}	A	P_{Class} / V_{Port_PSE}	I_{LIM}	1,2	Optional limit; see 33.2.7.6, Table 33–7.
8	Overload time limit	T_{CUT}	s	0.050	0.075	1, 2	See 33.2.7.7.
9	Output current – at short circuit condition	I_{LIM}	A	0.400	See info	1	See 33.2.7.7. Max value defined by Figure 33–14.
				1.14 × I_{Cable}		2	
10	Short circuit time limit	T_{LIM}	s	0.050	See info	1	See 33.2.7.7.
				0.010		2	
11	Continuous output power capability in POWER_ON state	P_{Con}	W	P_{Class}		1, 2	See 33.2.7.10, Table 33–7.
12	PSE Type power minimum	P_{Type}	W	I_{Cable} × (V_{Port_PSE} min)		1, 2	See 33.1.4.
13	Power turn on time	T_{pon}	s		0.400	1, 2	See 33.2.7.12.

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Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
14	Turn on rise time	T_{Rise}	µs	15.0		1, 2	From 10 % to 90 % of the voltage difference at the PI in POWER_ON state from the beginning of POWER_UP.
15	Turn off time	T_{Off}	s		0.500	1, 2	See 33.2.7.8.
16	Turn off voltage	V_{Off}	V		2.80	1, 2	See 33.2.7.9.
17	DC MPS current	I_{Hold}	A	0.005	0.010	1, 2	See 33.2.9.1.2.
18	PD Maintain Power Signature dropout time limit	T_{MPDO}	s	0.300	0.400	1, 2	See 33.2.9.
19	PD Maintain Power Signature time for validity	T_{MPS}	s	0.060		1, 2	See 33.2.9.
20	Current unbalance	I_{unb}	A		3 % × I_{Cable}	1	See 33.2.7.11, 33.4.8. NOTE—For practical implementations, it is recommended that Type 1 PSEs support Type 2 I_{unb} requirements.
					3 % × I_{Peak}	2	
21	Alternative B detection backoff time	T_{dbo}	s	2.00		1, 2	
22	Output capacitance during detection state	C_{out}	µF		0.520	1, 2	
23	Detection timing	T_{det}	s		0.500	1, 2	Time to complete detection of a PD.
24	Error delay timing	T_{ed}	s	0.750		1, 2	Delay before PSE may attempt subsequent powering after power removal because of error condition.

33.2.7.1 Output voltage in the POWER_ON state

The specification for V_{Port_PSE} in Table 33–11 shall be met with a (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min load step at a rate of change of at least 15 mA/µs. The voltage transients as a result of load changes up to 35 mA/µs shall be limited to 3.5 V/µs max.

A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the V_{Port_PSE} specification.

33.2.7.2 Voltage transients

A Type 2 PSE shall maintain an output voltage no less than K_{Tran_lo} below V_{Port_PSE} min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 33.2.7.7.

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Transients less than 30 µs in duration may cause the voltage at the PI to fall more than K_{Tran_lo}. The minimum PD input capacitance allows the PD to operate for any input voltage transient lasting less than 30 µs. Transients lasting more than 250 µs shall meet the V_{Port_PSE} specification.

33.2.7.3 Power feeding ripple and noise

The specification for power feeding ripple and noise in Table 33–11 shall be met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min for PSEs at static operating V_{Port_PSE}. The limits are meant to preserve data integrity. To meet EMI standards, lower values may be needed. For higher frequencies, see 33.4.4 and 33.4.5.

33.2.7.4 Continuous output current capability in the POWER_ON state

In addition to I_{Con} as specified in Table 33–11, the PSE shall support the following AC current waveform parameters, while within the operating voltage range of V_{Port_PSE}:

I_{Peak} minimum for T_{CUT} minimum and 5 % duty cycle minimum, where

$$I_{Peak} = \left\{ \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4(R_{Chan})(P_{Peak\_PD})}}{2(R_{Chan})} \right\}_A \quad (33\text{–}4)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4.426

R_{Chan} is the channel loop resistance as defined in 33.1.4; this parameter has a worst-case value of R_{Ch}, defined in Table 33–1

P_{Peak_PD} is the peak power a PD may draw for its class; see Table 33–18

33.2.7.5 Output current in POWER_UP mode

POWER_UP mode occurs between the PSE's transition to the POWER_UP state and either the expiration of T_{Inrush} or the conclusion of PD inrush currents (see 33.3.7.3). However, for practical implementations, it is recommended that the POWER_UP mode persist for the complete duration of T_{Inrush}, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

The PSE shall limit the maximum current sourced at the PI during POWER_UP. The maximum inrush current sourced by the PSE shall not exceed the PSE inrush template in Figure 33–13.

a) During POWER_UP, for PI voltages between 0 V and 10 V, the minimum I_{Inrush} requirement is 5 mA.
b) During POWER_UP, for PI voltages between 10 V and 30 V, the minimum I_{Inrush} requirement is 60 mA.
c) During POWER_UP, for PI voltages above 30 V, the minimum I_{Inrush} requirement is as specified in Table 33–11.
d) For Type 1 PSE, measurement of minimum I_{Inrush} requirement to be taken after 1 ms to allow startup transients. A Type 2 PSE that uses 1-Event physical layer classification, and requires the 1 ms settling time, shall power up a class 4 PD as if it used 2-Event physical layer classification.

The PSE inrush template, I_{PSEIT}, is defined by the following segments:

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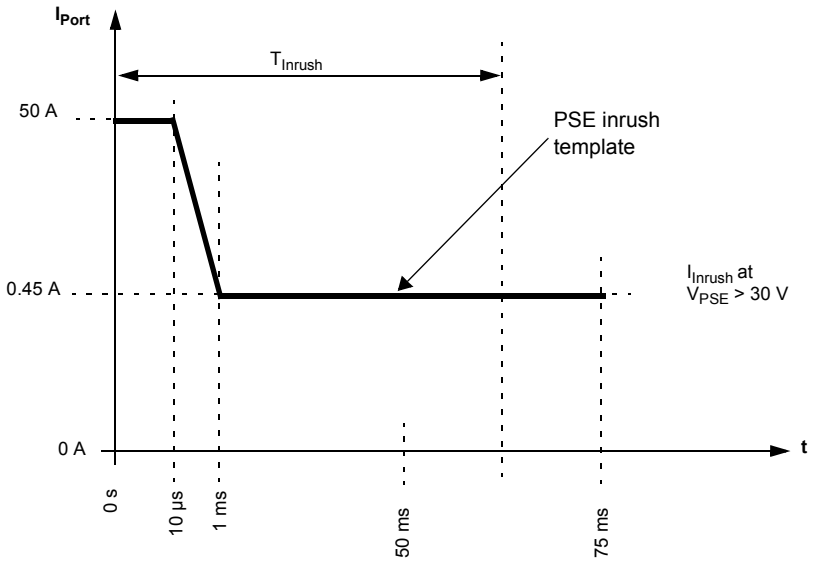


Figure 33–13—I_{Inrush} current and timing limits in POWER_UP state

$$I_{\mathrm{PSEIT}}(t) = \begin{cases} 50.0 & \text{for } 0 < t < 10.0\times10^{-6} \\ 50.0 - \dfrac{(t - 10.0\times10^{-6}) \times 49.6}{0.990\times10^{-6}} & \text{for } 10.0\times10^{-6} \le t < 0.001 \\ 0.450 & 0.001 \le t < 0.075 \end{cases} \quad (33\text{–}5)$$

where

t is the time in seconds

33.2.7.6 Overload current

If I_{Port}, the current supplied by the PSE to the PI, exceeds I_{CUT} for longer than T_{CUT}, the PSE may remove power from the PI. The cumulative duration of T_{CUT} is measured with a sliding window of at least 1 second width.

The I_{CUT} threshold may equal the I_{Peak} value determined by Equation (33–4).

33.2.7.7 Output current—at short circuit condition

A PSE may remove power from the PI if the PI current meets or exceeds the "PSE lowerbound template" in Figure 33–14. Power shall be removed from the PI of a PSE before the PI current exceeds the "PSE upperbound template" in Figure 33–14.

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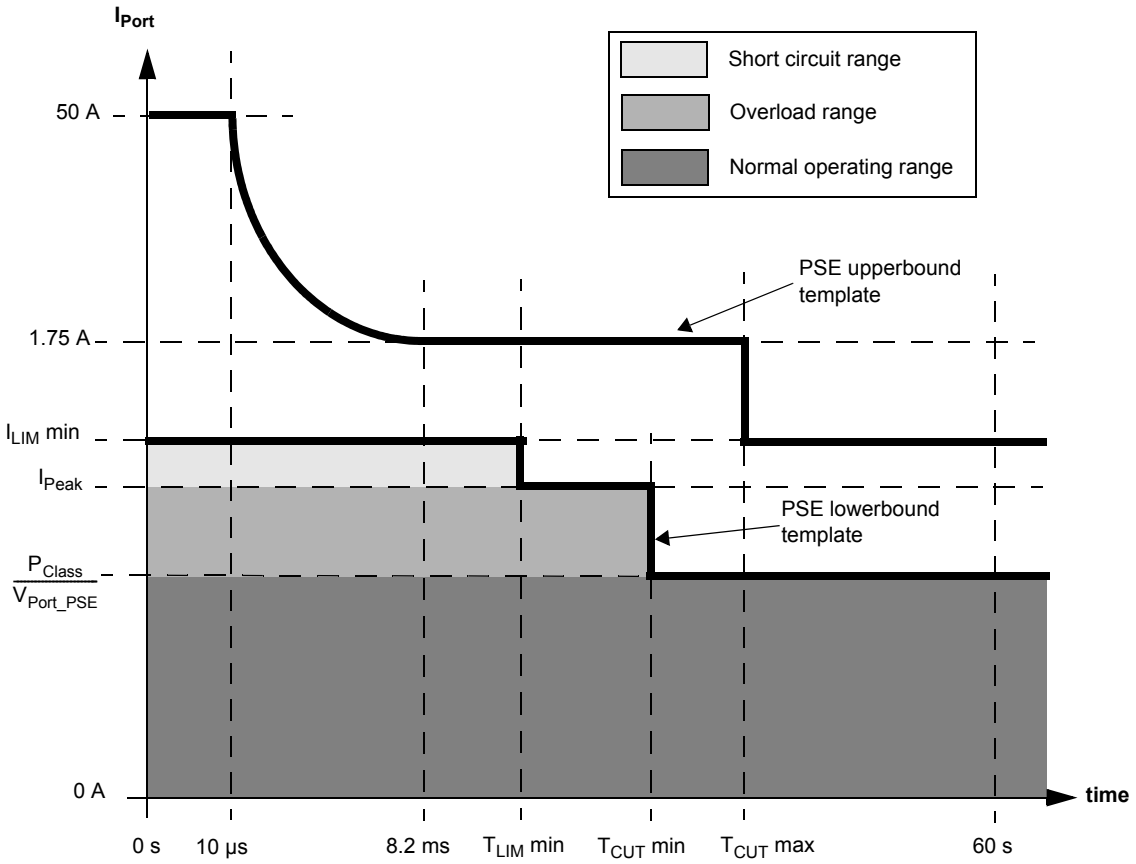


Figure 33–14—POWER_ON state PI operating current templates

The maximum value of I_{LIM} is the PSE upperbound template described by Equation (33–6) and Figure 33–14.

The PSE upperbound template, I_{PSEUT}, is defined by the following segments:

$$I_{\mathrm{PSEUT}}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for } (0 \le t < 10.0\times10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10.0\times10^{-6} \le t < 8.20\times10^{-3}) \\ 1.75 & \text{for } \left(8.20\times10^{-3} \le t < T_{\mathrm{cutmax}}\right) \\ I_{\mathrm{limmin}} & \text{for } (T_{\mathrm{cutmax}} \le t) \end{array} \right\}_{\mathrm{A}} \qquad (33\text{–}6)$$

where

t	is the duration in seconds that the PSE sources I_{Port}
K	is 0.025 A^2s, an energy limitation constant for the port current when it is not in steady state normal operation
T_{cutmax}	is T_{CUT} max, as defined in Table 33–11
I_{limmin}	is I_{LIM} min, as defined in Table 33–11

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The PSE shall limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI. The cumulative duration of T_{LIM} may be measured with a sliding window.

The PSE lowerbound template, I_{PSELT}, is defined by the following segments:

$$I_{PSELT}(t) = \left\{ \begin{array}{ll} I_{LIMmin} & \text{for } (0 \le t < T_{limmin}) \\ I_{Peak} & \text{for } (T_{limmin} \le t < T_{cutmin}) \\ \dfrac{P_{Class}}{V_{PSE}} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_{A} \quad (33\text{–}7)$$

where

I_{LIMmin} is the I_{LIM} min value for the PSE (see Table 33–11)
t is the duration that the PI sources I_{Port}
T_{limmin} is T_{LIM} min as defined in Table 33–11
T_{cutmin} is T_{CUT} min, as defined in Table 33–11
I_{Peak} is I_{Peak}, as defined in Equation (33–4)
P_{Class} is P_{Class}, as defined in Table 33–7
V_{PSE} is the voltage at the PSE PI

If a short circuit condition is detected, power removal from the PI shall begin within T_{LIM} as specified in Table 33–11. If I_{Port} exceeds the PSE lowerbound template, the PSE output voltage may drop below V_{Port_PSE} min.

33.2.7.8 Turn off time

The specification for T_{Off} in Table 33–11 shall apply to the discharge time from V_{Port_PSE} to V_{Off} with a test resistor of 320 kΩ attached to the PI. In addition, it is recommended that the PI be discharged when turned off. T_{Off} starts when V_{PSE} drops 1 V below the steady-state value after the pi_powered variable is cleared (see Figure 33–9). T_{Off} ends when $V_{PSE} \le V_{Off}$ max. The PSE remains in the IDLE state as long as the average voltage across the PI is V_{Off}. The IDLE state is the state when the PSE is not in detection, classification, or normal powering states.

33.2.7.9 Turn off voltage

The specification for V_{Off} in Table 33–11 shall apply to the PI voltage in the IDLE State.

33.2.7.10 Continuous output power capability in POWER_ON state

P_{Class} is the class power defined in 33.2.6 and Equation (33–3), or PSE allocated power (as defined in 79.3.2.6) added to the channel power loss.

P_{Con} is valid over the range of V_{Port_PSE} defined in Table 33–11. Measurement of P_{Con} should be averaged using any sliding window with a width of 1 s.

A PSE may remove power from a PD that causes the PSE to source more than P_{Class}.

33.2.7.11 Current unbalance

The specification for I_{unb} in Table 33–11 shall apply to the current unbalance between the two conductors of a power pair over the current load range.

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Type 2 Endpoint PSEs shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).

33.2.7.12 Power turn on time

The specification for T_{pon} in Table 33–11 applies to the PSE power up time for a PD after completion of detection. If power is not applied as specified, a new detection cycle is initiated (see 33.2.4.1).

33.2.7.13 PSE stability

When connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33A for PSE design guidelines for stable operation.

33.2.8 Power supply allocation

A PSE does not initiate power provision to a link if the PSE is unable to provide the maximum power level requested by the PD based on the PD's class.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

See 33.6 for a description of Data Link Layer classification.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

33.2.9 PSE power removal

Figure 33–10 shows the PSE monitor state diagrams. These state diagrams monitor for inrush current and the absence of the Maintain Power Signature (MPS).

If any of these conditions exist for longer than its related time limit, the power is removed from the PI.

33.2.9.1 PSE Maintain Power Signature (MPS) requirements

The MPS consists of two components, an AC MPS component and a DC MPS component.

The PSE shall monitor either the DC MPS component, the AC MPS component, or both.

33.2.9.1.1 PSE AC MPS component requirements

A PSE that monitors the AC MPS component shall meet the "AC Signal parameters" and "PSE PI voltage during AC disconnect detection" parameters in Table 33–12.

A PSE shall consider the AC MPS component to be present when it detects an AC impedance at the PI equal to or lower than $|Z_{ac1}|$ as defined in Table 33–12.

A PSE shall consider the AC MPS component to be absent when it detects an AC impedance at the PI equal to or greater than $|Z_{ac2}|$ as defined in Table 33–12. Power shall be removed from the PI when AC MPS has been absent for a time duration greater than T_{MPDO}.

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A PSE may consider the AC MPS component to be either present or absent when it detects a AC impedance between the values $|Z_{ac1}|$ max and $|Z_{ac2}|$ min.

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if I_{Port} is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if I_{Port} is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of I_{Hold}.

Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when I_{Port} is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every $T_{MPS} + T_{MPDO}$, as defined in Table 33–11. This allows a PD to minimize its power consumption.

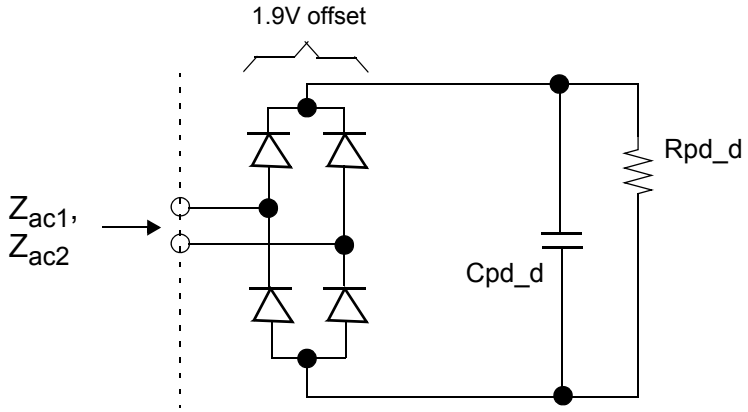
Table 33–12—PSE PI parameters for AC disconnect-detection function

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC signal parameters					
1a	PI probing AC voltage	V_open	V_{pp}	1.90	10% of the average value of V_{Port_PSE} within the limits of Table 33–11	Includes noise, ripple, etc. V_open is the AC voltage across the PI when the PD is not connected to the PI and before the detection of this condition by the PSE.
		V_open1	V_p		30.0 V, $V_{PSE} \leq$ 44.0 V	V_open1 is the AC voltage across the PI when the PD is not connected to the PI and after the detection of this condition by the PSE and the removal of power from the PI.
1b	AC probing signal frequency	F_p	kHz		0.500	
1c	AC probing signal slew rate	SR	V/µs		0.100	Positive or negative.
	AC source output impedance					
2a	Source output current during the operation of the AC disconnect detection function	I_sac	mA		5.00	During operation of the AC disconnect detection function.
2b	PSE PI impedance during PD detection when measured at the PSE PI	R_rev	kΩ	45.0		Specified in 33.2.5.1 and Figure 33–11. Shown here to clarify the difference in PI impedance during the signature detection function.
	PSE PI voltage during AC disconnect detection					
3a	PI AC voltage when PD is connected	V_{CLOSE}	V_{pp}			See Table 33–11, item 3.

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Table 33–12—PSE PI parameters for AC disconnect-detection function *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
3b	PI voltage when PD is disconnected	V_{PSE}	V_p		60.0	
	AC Maintain Power Signature					
4a	Valid impedance	$\lvert Z_{ac1} \rvert$	kΩ		27.0	F_p = 5 Hz, Testing voltage >2.5 V. See Figure 33–15.
4b	Invalid impedance	$\lvert Z_{ac2} \rvert$	kΩ	1980		See Figure 33–15.



NOTE—Rpd_d and Cpd_d are specified in Table 33–19. Cpd_d may be located either in parallel with Z_{ac1} or as shown above.

Figure 33–15—Z_{ac1} and Z_{ac2} definition as indicated in Table 33–12

33.3 Powered devices (PDs)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PI. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

33.3.1 PD PI

The PD shall be capable of accepting power on either of two sets of PI conductors. The two conductor sets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–8 in conjunction with Table 33–13 illustrates the two power modes.

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Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_{P}, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

The PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

33.3.2 PD type descriptions

PDs can be categorized as either Type 1 or Type 2.

Type 1 PDs implement a minimum of 1-Event Physical Layer classification and advertise a 1-Event class signature of 0, 1, 2, or 3.

Type 2 PDs implement both 2-Event Physical Layer classification (see 33.3.5.2) and Data Link Layer classification (see 33.6) and advertise a 2-Event class signature of 4.

The maximum power a PD expects to draw from a PSE is P_{Class_PD} max as defined in Table 33–18.

A Type 2 PD that does not successfully observe a 2-Event Physical Layer classification or Data Link Layer classification shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementer.

Type 2 PDs shall meet the requirements of 25.4.5 in the presence of (I_{unb} / 2).

33.3.3 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 33–16.

33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

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33.3.3.2 Constants

The PD state diagram uses the following constants:

V_{Reset_th}
: Reset voltage threshold (see Table 33–17)

V_{Mark_th}
: Mark event voltage threshold (see Table 33–17)

class_sig
: PD classification, one of either 0, 1, 2, 3, or 4 (see Table 33–16)

33.3.3.3 Variables

The PD state diagram uses the following variables:

mdi_power_required
: A control variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.
Values:FALSE:PD functionality is disabled.
TRUE:PD functionality is enabled.

pd_2-event
: A control variable indicating whether the PD presents a 2-Event class signature.
Values:FALSE:PD does not present a 2-Event class signature.
TRUE:PD does present a 2-Event class signature.

pd_dll_capable
: This variable indicates whether the PD implements Data Link Layer classification.
Values:FALSE:The PD does not implement Data Link Layer classification.
TRUE:The PD does implement Data Link Layer classification.

pd_dll_enabled
: A variable indicating whether the Data Link Layer classification mechanism is enabled.
Values:FALSE:Data Link Layer classification is not enabled.
TRUE:Data Link Layer classification is enabled.

pd_max_power
: A control variable indicating the max power that the PD may draw from the PSE. See power classifications in Table 33–18.
Values:0: PD may draw Class 0 power
1: PD may draw Class 1 power
2: PD may draw Class 2 power
3: PD may draw Class 3 power
4: PD may draw Class 4 power

pd_reset
: An implementation-specific control variable that unconditionally resets the PD state diagram to the OFFLINE state.
Values:FALSE:The device has not been reset (default).
TRUE:The device has been reset.

power_received
: An indication from the circuitry that power is present on the PD's PI.
Values:FALSE:The input voltage does not meet the requirements of V_{Port_PD} in Table 33–18.
TRUE:The input voltage meets the requirements of V_{Port_PD}.

present_class_sig
: Controls presenting the classification signature (see 33.3.5) by the PD.

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Values:FALSE:The PD classification signature is not to be applied to the link.
TRUE:The PD classification signature is to be applied to the link.

present_det_sig
Controls presenting the detection signature (see 33.3.4) by the PD.
Values:FALSE:A non-valid PD detection signature is to be applied to the link.
TRUE:A valid PD detection signature is to be applied to the link.

present_mark_sig
Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD.
Values:FALSE:The PD does not present mark event behavior.
TRUE:The PD does present mark event behavior.

present_mps
Controls applying MPS (see 33.3.8) to the PD's PI.
Values:FALSE:The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE:The MPS is to be applied to the PD's PI.

pse_dll_power_type
A control variable output by the PD power control state diagram (Figure 33–28) that indicates the type of PSE by which the PD is being powered.
Values:1: The PSE is a Type 1 PSE (default).
2: The PSE is a Type 2 PSE.

pse_power_type
A control variable that indicates to the PD the type of PSE by which it is being powered.
Values:1: The PSE is a Type 1 PSE.
2: The PSE is a Type 2 PSE.

V_{PD}
Voltage at the PD PI as defined in 1.4.425.

33.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer
A timer used to prevent the Type 2 PD from drawing more than inrush current during the PSE's inrush period; see T_{delay} in Table 33–18.

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33.3.3.5 State diagrams

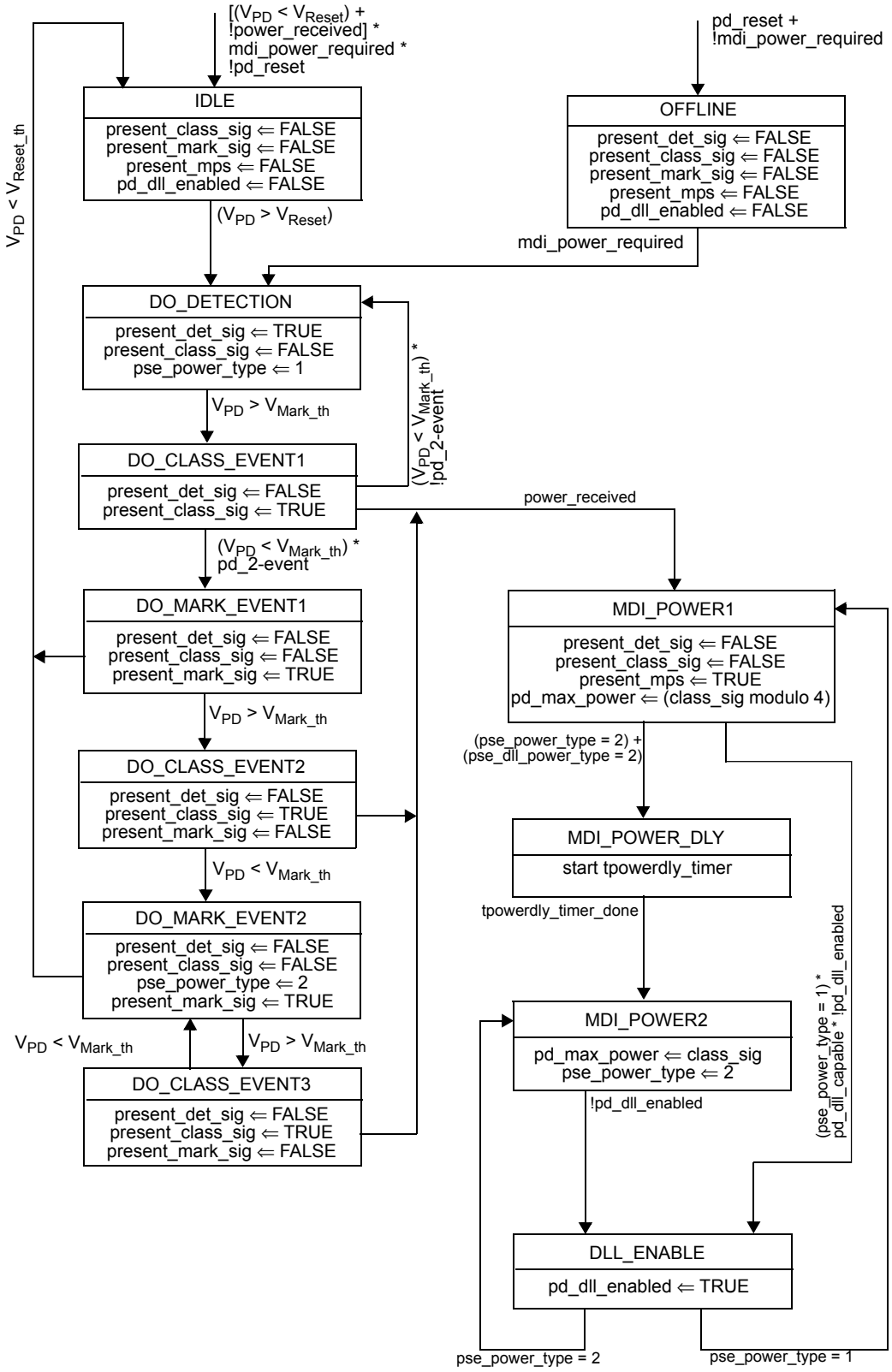


Figure 33–16—PD state diagram

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NOTE 1—DO_CLASS_EVENT3 creates a defined behavior for a Type 2 PD that is brought into the classification range repeatedly.

NOTE 2—In general, there is no requirement for a PD to respond with a valid classification signature for any DO_CLASS_EVENT duration less than T_{class}.

33.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature while it is in a state where it accepts power via the PI, but is not powered via the PI per Figure 33–16.

A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 33–16.

A Type 2 PD presents a non-valid detection signature when in a mark event state per Figure 33–16.

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive V_{PD} and Negative V_{PD} of PD Mode A and PD Mode B as defined in 33.3.1. When a PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power.

A PD may or may not present a valid detection signature when in the IDLE state.

The detection signature is a resistance calculated from two voltage/current measurements made during the detection process.

$$R_{\text{detect}} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \tag{33–8}$$

where

V_1 and V_2	are the first and second voltage measurements made at the PD PI, respectively
I_1 and I_2	are the first and second current measurements made at the PD PI, respectively
R_{detect}	is the effective resistance

A valid PD detection signature shall have the characteristics of Table 33–14.

A non-valid detection signature shall have one or both of the characteristics in Table 33–15.

A PD that presents a signature outside of Table 33–14 is non-compliant, while a PD that present the signature of Table 33–15 is assured to fail detection.

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Table 33–14—Valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
R_{detect} (at any 1 V or greater chord within the voltage range conditions)	2.70 V to 10.1 V	23.7	26.3	kΩ
V offset	See Figure 33–17	0	1.90	V
Voltage at the PI	I_{Port} = 124 μA	2.70		V
Input capacitance	2.70 V to 10.1 V	0.050	0.120	μF
Series input inductance	2.70 V to 10.1 V		0.100	mH

Table 33–15—Non-valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Range of values	Unit
R_{detect}	V < 10.1 V	Either greater than 45.0 or less than 12.0	kΩ
Input capacitance	V < 10.1 V	Greater than 10.0	μF

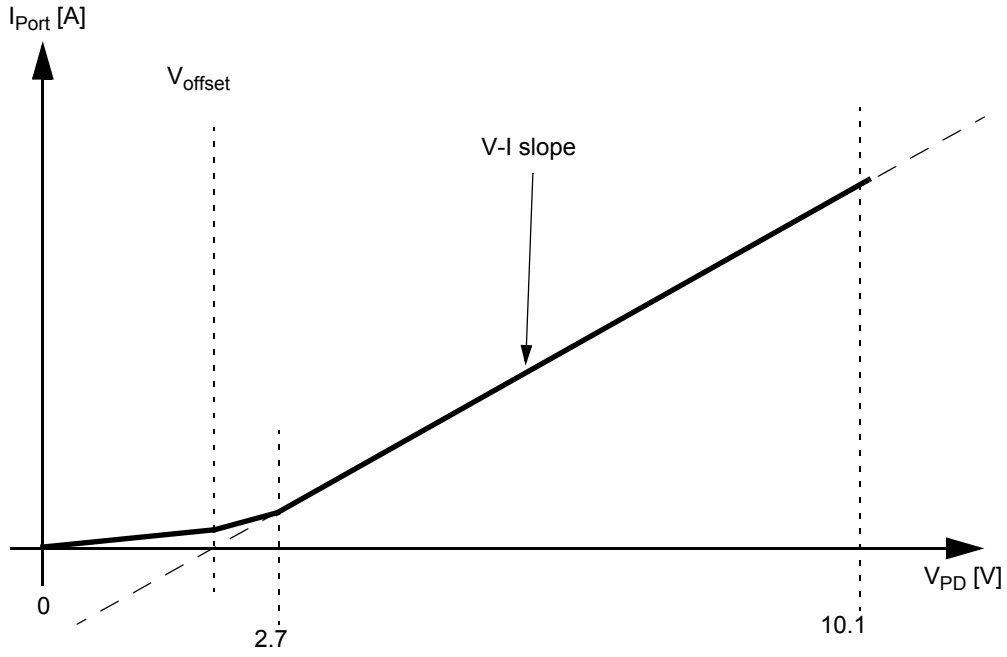


Figure 33–17—Valid PD detection signature offset

33.3.5 PD classifications

See 33.2.6 for a general description of classification mechanisms.

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A PD may be classified by the PSE based on the Physical Layer classification information, Data Link Layer classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used to establish mutual identification between Type 2 PSEs and Type 2 PDs.

The method of classification depends on the type of the PD and the type of the attached PSE.

A PD shall meet at least one of the allowable classification permutations listed in Table 33–8.

A Type 1 PD may implement any of the class signatures in 33.3.5 and 33.6.

Type 2 PDs implement both 2-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6).

PD classification behavior conforms to the state diagram in Figure 33–16.

33.3.5.1 PD 1-Event class signature

Class 0 is the default for PDs. However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3.

The PD is classified based on power. The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes.

PDs implementing a 2-Event class signature shall return Class 4 in accordance with the maximum power draw, P_{Class_PD}, as specified in Table 33–18. Since 1-Event classification is a subset of 2-Event classification, Type 2 PDs respond to 1-Event classification with a Class 4 signature. Type 1 PDs may choose to implement a 2-Event class signature and return Class 0, 1, 2, or 3 in accordance with the maximum power draw, P_{Class_PD}. The Type 2 PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

In addition to a valid detection signature, PDs shall provide the characteristics of a classification signature as specified in Table 33–16. A PD shall present one, and only one, classification signature during classification.

Table 33–16—Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5 V to 20.5 V	0	4.00	mA
Current for Class 1	14.5 V to 20.5 V	9.00	12.0	mA
Current for Class 2	14.5 V to 20.5 V	17.0	20.0	mA
Current for Class 3	14.5 V to 20.5 V	26.0	30.0	mA
Current for Class 4	14.5 V to 20.5 V	36.0	44.0	mA

33.3.5.2 PD 2-Event class signature

PDs implementing a 2-Event class signature shall return a Class 4 classification signature in accordance with the maximum power draw, P_{Class_PD}, as specified by Table 33–18. The PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

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Until successful 2-Event Physical Layer classification or Data Link Layer classification has completed, a Type 2 PD's pse_power_type state variable is set to '1.' A Type 2 PD shall conform to the electrical requirements as defined by Table 33–18 for the type defined in its pse_power_type state variable.

Table 33–17—2-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Class event voltage	V_{Class}	V	14.5	20.5	
2	Mark event voltage	V_{Mark}	V	6.90	10.1	
3	Mark event current	I_{Mark}	mA	0.250	4.00	See 33.3.5.2.1
4	Mark event threshold	V_{Mark_th}	V	10.1	14.5	See 33.3.5.2.1
5	Classification reset threshold	V_{Reset_th}	V	2.81	6.90	See 33.3.5.2.1
6	Classification reset voltage	V_{Reset}	V	0	2.81	See 33.3.5.2.1

33.3.5.2.1 Mark Event behavior

When the PD is presenting a mark event signature as shown in the state diagram of Figure 33–16, the PD shall draw I_{Mark} as defined in Table 33–17 and present a non-valid detection signature as defined in Table 33–15.

The PD shall not exceed the I_{Mark} current limits when voltage at the PI enters the V_{Mark} specification as defined in Table 33–17.

V_{Mark_th} is the PI voltage threshold at which the PD implementing 2-Event class signature transitions into and out of the DO_CLASS_EVENT1 or DO_CLASS_EVENT2 states as shown in Figure 33–16.

The PD shall draw I_{Mark} until the PD transitions from a DO_MARK_EVENT state to the IDLE state.

V_{Reset_th} is the PI voltage threshold at which the PD implementing 2-Event class signature transitions from a DO_MARK_EVENT state to the IDLE state as shown in Figure 33–16.

33.3.6 PSE Type identification

A Type 2 PD shall identify the PSE Type as either Type 1 or Type 2 (see Figure 33–16).

The default value of pse_power_type is 1. After a successful 2-Event Physical Layer classification or Data Link Layer classification has completed, the pse_power_type is set to 2.

The PD resets the pse_power_type to '1' when the PD enters the DO_DETECTION state.

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33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage	V_{Port_PD}	V	37.0	57.0	1	See 33.3.7.1, Table 33–1
				42.5	57.0	2	
2	Transient operating input voltage	V_{Tran_lo}	V	36.0		2	For time duration defined in 33.2.7.2
3	Input voltage range during overload	$V_{Overload}$	V	36.0	57.0	1	See 33.3.7.4, Table 33–1
				41.4	57.0	2	
4	Input average power, Class 0 and Class 3	P_{Class_PD}	W		13.0	1	See 33.3.7.2, Table 33–1
	Input average power, Class 1				3.84	1	
	Input average power, Class 2				6.49	1	
	Input average power, Class 4				25.5	2	
5	Input inrush current	I_{Inrush_PD}	A		0.400	1, 2	Peak value—See 33.3.7.3
6	Inrush to operating state delay	T_{delay}	s	0.080		2	See 33.3.7.3
7	Peak operating power, Class 0 and Class 3	P_{Peak_PD}	W		14.4	1	See 33.3.7.4
	Peak operating power, Class 1				5.00	1	
	Peak operating power, Class 2				8.36	1	
	Peak operating power, Class 4				$1.11 \times P_{Class\_PD}$	2	
8	Input current transient (absolute value)		mA/µs		4.70	1, 2	See 33.3.7.5
9	PI capacitance during MDI_POWER states	C_{Port}	µF	5.00		1, 2	See 33.3.7.6, 33.3.7.3

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Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
10	Ripple and noise, < 500 Hz		V_{PP}		0.500	1, 2	See 33.3.7.7. Balanced source impedance: R_{Ch}
	Ripple and noise, 500 Hz to 150 kHz				0.200		
	Ripple and noise, 150 kHz to 500 kHz				0.150		
	Ripple and noise, 500 kHz to 1 MHz				0.100		
11	a) PD Power supply turn on voltage	V_{On}	V		42.0	1, 2	See 33.3.7.1
	b) PD power supply turn off voltage	V_{Off}	V	30.0		1, 2	
12	PD classification stability time	T_{class}	s		0.005		See 33.3.7.8
13	Backfeed voltage	V_{bfd}	V		2.80		See 33.3.7.9

33.3.7.1 Input voltage

The specification for V_{Port_PD} in Table 33–18 is for the input voltage range after startup (see 33.3.7.3), and accounts for loss in the cabling plant. Note, $V_{PD} = V_{PSE} - (R_{Chan} \times I_{Port})$.

The PD shall turn on at a voltage less than or equal to V_{On}. After the PD turns on, the PD shall stay on over the entire V_{Port_PD} range. The PD shall turn off at a voltage less than V_{Port_PD} minimum and greater than or equal to V_{Off}.

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by V_{Port_PSE} min to V_{Port_PSE} max (as defined in Table 33–11) with a series resistance within the range of valid Channel Resistance.

33.3.7.2 Input average power

The maximum average power, P_{Class_PD} in Table 33–18 or PDMaxPowerValue in 33.6.3.3, is calculated over a 1 second interval. PDs may dynamically adjust their maximum required operating power below P_{Class_PD} as described in 33.6.

NOTE—Average power is calculated using any sliding window with a width of 1 s.

33.3.7.2.1 System stability test conditions during startup and steady state operation

When the PD is fed by V_{Port_PSE} min to V_{Port_PSE} max with R_{Ch} (as defined in Table 33–1) in series, P_{Port_PD} shall be defined as shown in Equation (33–9):

$$P_{Port\_PD} = \{V_{Port\_PD} \times I_{Port}\}_W \quad (33–9)$$

where

P_{Port_PD} is the average input power at the PD PI

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V_{Port_PD} is the static input voltage at the PD PI
I_{Port} is the input current, either DC or RMS

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{Port_PD} requirements as defined in Table 33–18, and ending when C_{Port} is charged to 99% of its final value. This period should be less than T_{Inrush} min per Table 33–11.

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} starts when V_{PD} crosses the PD power supply turn on voltage, V_{On}. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from I_{Inrush} to I_{LIM}.

Input inrush current at startup is limited by the PSE if $C_{Port} < 180$ µF, as specified in Table 33–11.

If $C_{Port} \geq 180$ µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max is satisfied.

33.3.7.4 Peak operating power

$V_{Overload}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, the peak power shall not exceed P_{Class_PD} max for more than T_{CUT} min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed P_{Peak} max.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max.

The RMS, DC and ripple current shall be bounded by Equation (33–10):

$$I_{Port} = \left\{ \sqrt{(I_{Port\_dc})^2 + (I_{Port\_ac})^2} \right\}_A \quad (33–10)$$

where
I_{Port} is the RMS input current
I_{Port_dc} is the DC component of the input current
I_{Port_ac} is the RMS value of the AC component of the input current

The maximum I_{Port} value for all operating V_{Port_PD} range shall be defined by the following equation:

$$I_{portmax} = \left\{ \frac{P_{Class\_PD}}{V_{Port\_PD}} \right\}_A \quad (33–11)$$

where
$I_{portmax}$ is the maximum DC and RMS input current
V_{Port_PD} is the static input voltage at the PD PI
P_{Class_PD} is the maximum power, P_{Class_PD} max, as defined in Table 33–18

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Peak power, P_{Peak_PD}, for Class 4 is based on Equation (33–12), which approximates the ratiometric peak powers of Class 0 through Class 3. This equation may be used to calculate peak operating power for P_{Peak_PD} values obtained via Data Link Layer classification.

$$P_{Peak\_PD} = \{1.11 \times P_{Class\_PD}\}_W \quad (33–12)$$

where

P_{Peak_PD} is the peak operating power
P_{Class_PD} is the input average power

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

33.3.7.5 Peak transient current

When the input voltage at the PI is static and in the range of V_{Port_PD} defined by Table 33–18, the transient current drawn by the PD shall not exceed 4.70 mA/μs in either polarity. This limitation applies after inrush has completed (33.3.7.3) and before the PD has disconnected.

Under normal operating conditions when there are no transients applied at the PD PI, the PD shall operate below the PD upperbound template defined in Figure 33–18.

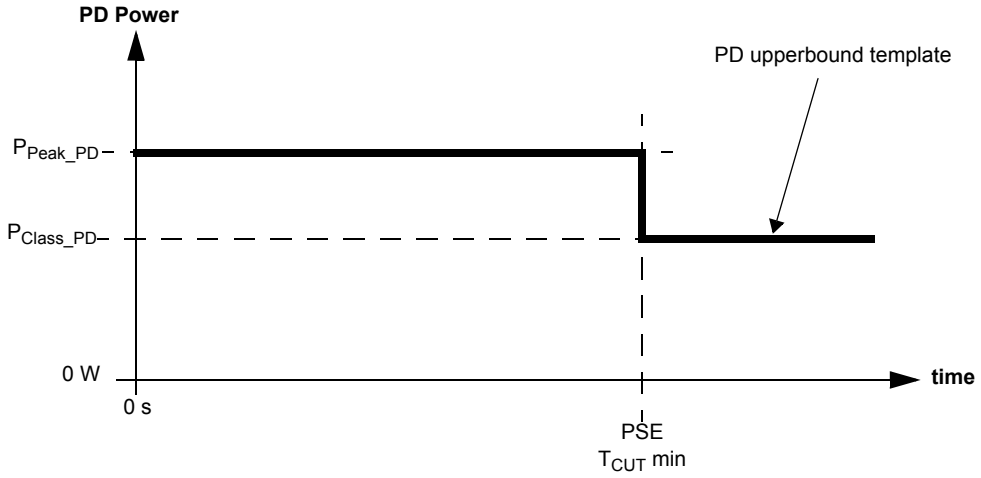


Figure 33–18—PD static operating mask

The PD upperbound template in Figure 33–18, P_{PDUT}, is described by Equation (33–13):

$$P_{PDUT}(t) = \left\{ \begin{array}{l} P_{Peak\_PD} \text{ for } (0 \le t < T_{cutmin}) \\ P_{Class\_PD} \text{ for } (T_{cutmin} \le t) \end{array} \right\}_W \quad (33–13)$$

where

t is the duration in seconds that the PD sinks I_{Port}
P_{Peak_PD} is the peak operating power, P_{Peak_PD} max, as defined in Table 33–18
P_{Class_PD} is the maximum power, P_{Class_PD} max, as defined in Table 33–18
T_{cutmin} is T_{CUT} min, as defined in Table 33–11

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During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least T_{LIM} min as defined in Table 33–11.

33.3.7.6 PD behavior during transients at the PSE PI

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after T_{LIM} min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.

A Type 2 PD shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance is R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI I_{LIM} per Equation (33–14).

The current limit at the MDI (MDI I_{LIM}) is defined by Equation (33–14):

$$\{pse_{\mathrm{ILIMmin}}\}_{\mathrm{mA}} < \{mdi_{\mathrm{ILIM}}\}_{\mathrm{mA}} \leq \{pse_{\mathrm{ILIMmin}}\}_{\mathrm{mA}} + 5.00 \quad (33\text{–}14)$$

where

pse_{ILIMmin} is the PSE I_{LIM} min as defined in Table 33–11
mdi_{ILIM} is the current limit at the MDI (MDI I_{LIM})

33.3.7.7 Ripple and noise

The specification for ripple and noise in Table 33–18 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range of V_{Port_PD}, and over the range of input power of the device.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 33–11, item 3.

Limits are provided to preserve data integrity. To meet EMI standards, lower values may be needed.

The system designer is advised to assume the worst-case condition in which both PSE and PD generate the maximum noise allowed by Table 33–11 and Table 33–18, which may cause a higher noise level to appear at the PI than the standalone case as specified by this clause.

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33.3.7.8 PD classification stability time

Following a valid detection and a rising voltage transition from V_{valid} to V_{Class}, the PD Physical Layer classification signature shall be valid within T_{class} as specified in Table 33–18 and remain valid for the duration of the classification period.

33.3.7.9 Backfeed voltage

When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kΩ load resistor connected shall not exceed V_{bfd} max as specified in Table 33–18. When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode B according to Table 33–13, the voltage measured across the PI for Mode A with a 100 kΩ load resistor connected shall not exceed V_{bfd} max.

33.3.8 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS shall be both:

a) Current draw equal to or above the minimum input current (I_{Port_MPS} min) as specified in Table 33–19 for a minimum duration of 75 ms followed by an optional MPS dropout for no longer than 250 ms, and
b) Input impedance with resistive and capacitive components as defined in Table 33–19.

A PD that does not maintain the MPS components in a) and b) above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.

Powered PDs that no longer require power shall remove both components a) and b) of the MPS. To cause PSE power removal, the impedance of the PI should rise above Z_{ac2} as specified in Table 33–12.

Table 33–19—PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input current	I_{Port_MPS}	A	0.010		See 33.3.8
2	Input resistance	R_{pd_d}	kΩ		26.3	
3	Input capacitance	C_{pd_d}	μF	0.050		See Table 33–12

NOTE—A PD with $C_{port} > 180$ μF may not be able to meet the I_{Port_MPS} specification in Table 33–19 during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.

33.4 Additional electrical specifications

This clause defines additional electrical specifications for both the PSE and PD. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 33.4 are consistent with the requirements of the 10BASE-T MAU and the 100BASE-TX and 1000BASE-T PHYs.

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33.4.1 Isolation

PDs and PSEs shall provide isolation between all accessible external conductors, including frame ground (if any), and all MDI leads including those not used by the PD or PSE. Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector. Accessible external conductors are specified in subclause 6.2.1 b) of IEC 60950-1:2001.

This electrical isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
b) 2250 V dc for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
c) An impulse test consisting of a 1500 V, 10/700 µs waveform, applied 10 times, with a 60 s interval between pulses. The shape of the impulses shall be 10/700 µs (10 µs virtual front time, 700 µs virtual time of half value), as defined in IEC 60950-1:2001 Annex N.

There shall be no insulation breakdown, as defined in subclause 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

33.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

— **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
— **Environment B:** When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

33.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

A multiport NID complying with Environment A requirements does not require electrical power isolation between link segments.

An Environment A PSE shall switch the more negative conductor. It is allowable to switch both conductors.

33.4.1.1.2 Environment B requirements

The attachment of network segments that cross Environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

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For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.6, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strikes or other hazards. Protection requirements for such hazards are beyond the scope of this standard. Guidance on these requirements may be found in Section 6 of IEC 60950-1:2001, as well as any local and national codes related to safety.

33.4.2 Fault tolerance

Each wire pair of the PI, when it is also an MDI (e.g., an Endpoint PSE or PD), shall meet the fault tolerance requirements of the appropriate specifying clause. (See 14.3.1.2.7, 25.4, and 40.8.3.4.) When a PI is not an MDI (e.g., a Midspan PSE), the PSE PI shall meet the fault tolerance requirements of this subclause.

The PSE PI shall withstand without damage the application of short circuits of any wire to any other wire within the cable for an indefinite period of time. The magnitude of the current through such a short circuit shall not exceed I_{LIM} max as defined in Table 33–11.

Each wire pair shall withstand, without damage, a 1000 V common-mode impulse applied at E_{cm} of either polarity. The shape of the impulse shall be (0.3/50) μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060, where E_{cm} is an externally applied AC voltage as shown in Figure 33–19.

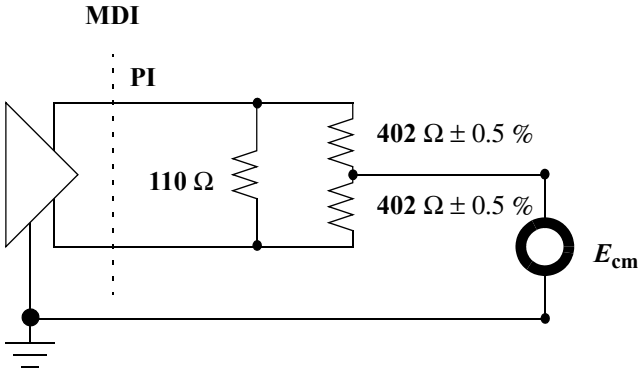


Figure 33–19—PI fault tolerance test circuit

33.4.3 Impedance balance

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed:

$$\left\{29.0 - 17.0 \times \log_{10}\left(\frac{f}{10.0}\right)\right\}_{\text{dB}} \tag{33–15}$$

where

f is the frequency in MHz from 1.00 MHz to 20.0 MHz for a 10 Mb/s MAU

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$$\left\{34.0 - 19.2 \times \log_{10}\left(\frac{f}{50.0}\right)\right\}_{\text{dB}} \tag{33–16}$$

where

f is the frequency in MHz from 1.00 MHz to 100. MHz for a 100 Mb/s or greater PHY

The impedance balance is defined as shown in Equation (33–17):

$$\left\{20.0 \times \log_{10}\left(\frac{E_{\text{cm}}}{E_{\text{dif}}}\right)\right\}_{\text{dB}} \tag{33–17}$$

where

E_{cm} is an externally applied sinusoidal voltage as shown in Figure 33–20

E_{dif} is the voltage of the resulting waveform due only to the applied sine wave measured as shown in Figure 33–20

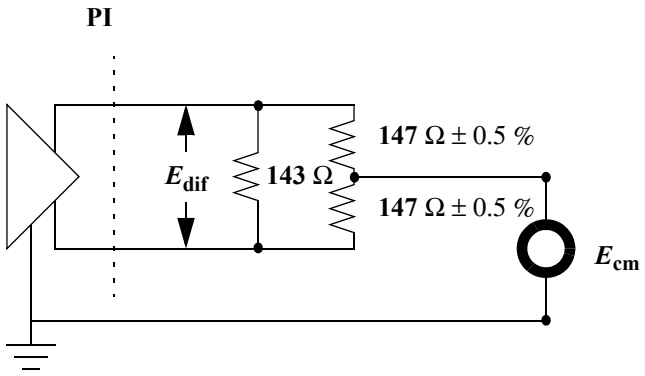


Figure 33–20—PI impedance balance test circuit

33.4.4 Common-mode output voltage

The magnitude of the common-mode AC output voltage measured according to Figure 33–21 and Figure 33–22 at the transmit PI while transmitting data and with power applied, $E_{\text{cm\_out}}$, shall not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater. The frequency of the measurement shall be from 1 MHz to 100 MHz.

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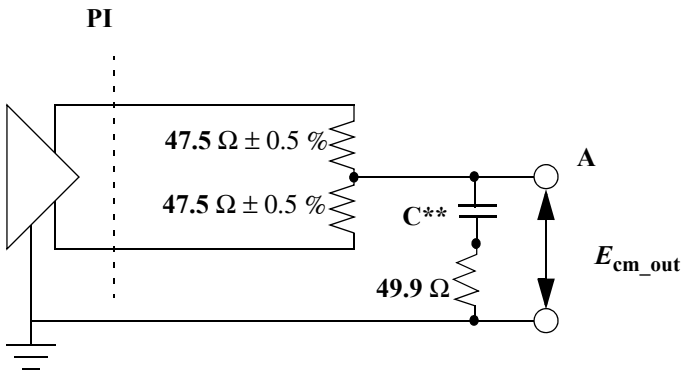


Figure 33–21—Common-mode output voltage test

The common-mode AC output voltage shall be measured while the PHY is transmitting data, the PSE or PD is operating with the following PSE load or PD source:

1) For a PSE, the PI that supplies power is terminated as illustrated in Figure 33–22. The PSE load, R, in Figure 33–22 is adjusted so that the PSE output current, I_{out}, is 10 mA and then 350 mA, while measuring E_{cm_out} on the PI.
2) For a PD, the PI that requires power shall be terminated as illustrated in Figure 33–22. V_{source} in Figure 33–22 is adjusted to 36 Vdc and 57 Vdc, while measuring E_{cm_out} on the PI.

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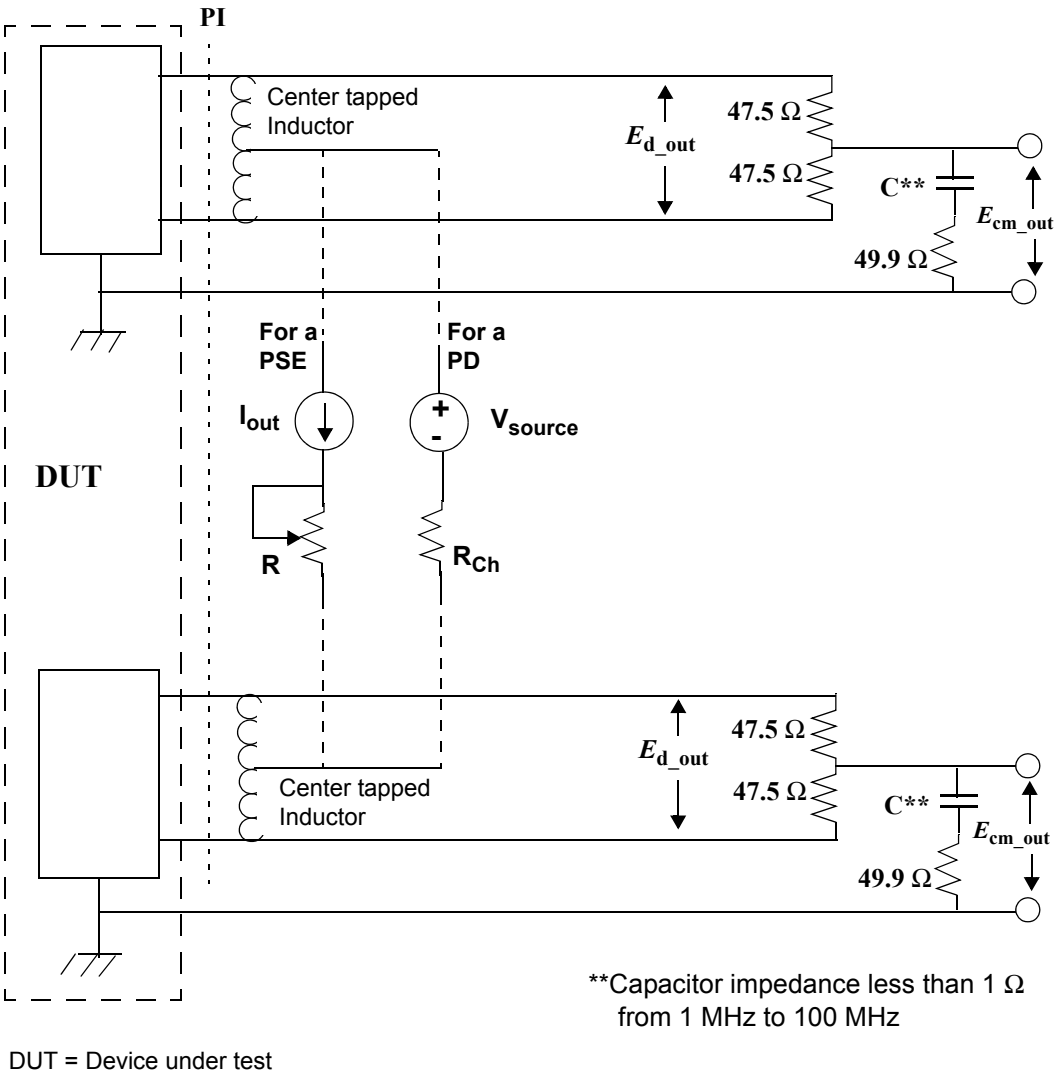


Figure 33–22—PSE and PD terminations for common-mode output voltage test

NOTE—The implementer should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

33.4.5 Pair-to-pair output noise voltage

The pair-to-pair output noise voltage (see Figure 33–23) is limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the power supply (Table 33–11, item 3) or from any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

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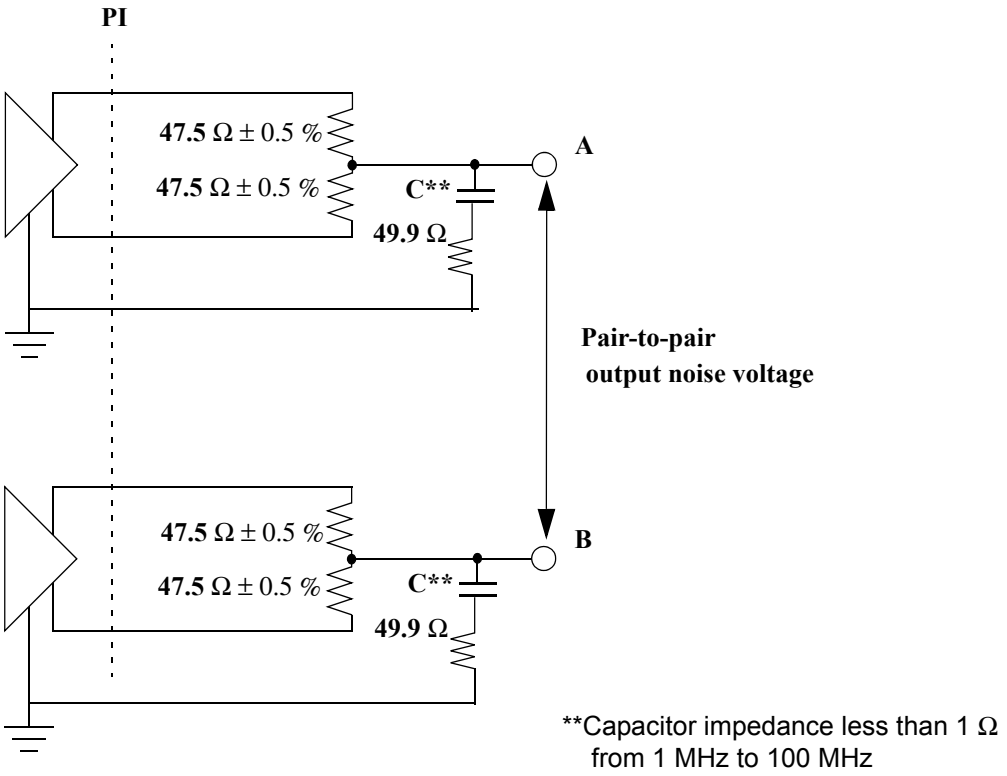


Figure 33–23—Pair-to-pair output noise voltage test

33.4.6 Differential noise voltage

The coupled noise, E_{d_out} in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4, item 1) and item 2).

33.4.7 Return loss

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY. In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75 Ω. The common-mode termination is affected by the presence of the power supply, and this should be considered to determine proper termination.

33.4.8 100BASE-TX transformer droop

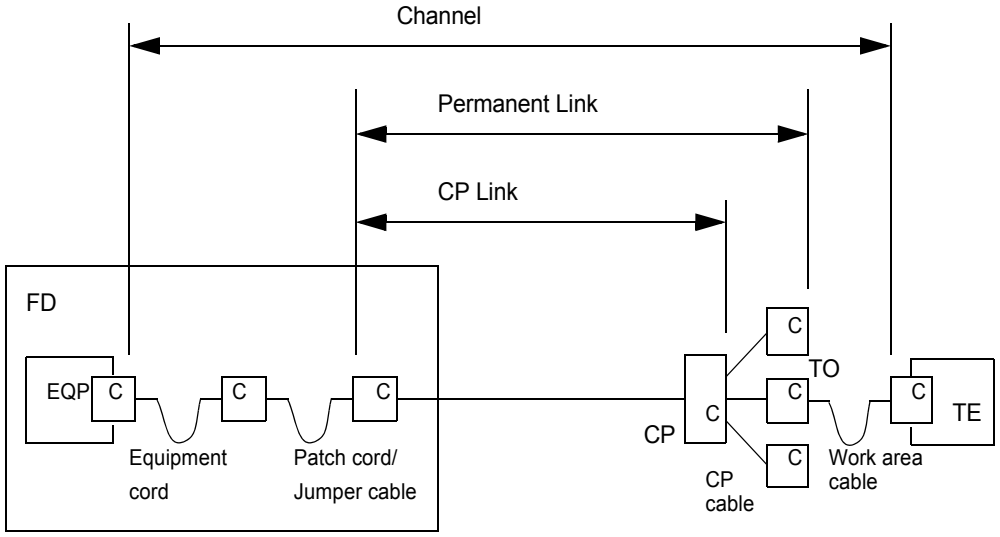
100BASE-TX systems may contain a legacy PHY receiver that expects to be connected to a PHY transmitter with 350 μH open circuit inductance (OCL). Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1 I_{unb} (see Table 33–11) or meet 33.4.9.2.

100BASE-TX Type 2 Endpoint PSEs and 100BASE-TX Type 2 PDs shall meet the requirements of Clause 25 in the presence of (I_{unb}/2).

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33.4.9 Midspan PSE device additional requirements

The cabling specifications for 100 Ω balanced cabling are described in ISO/IEC 11801-2002. Cable conforming to ANSI/TIA-568-C.2 also meets these requirements. Some cable category specifications that only appear in earlier editions are also supported. The configuration of "channel" and "permanent link" is defined in Figure 33–24. Type 2 Midspan PSE cabling system requirements are specified in 33.1.4.1.



FD = floor distributor; EQP = equipment; C = connection (mated pair);
CP = consolidation point; TO = telecommunications outlet;
TE = terminal equipment

Figure 33–24—Floor distributor channel configuration

ISO/IEC 11801 defines in 5.6.1 two types of Equipment interface to the cabling system: "Interconnect model" and the "cross-connect model." An equivalent "Interconnect model" and "cross-connect model" can be found in ANSI/TIA-568-C.0, 4.2. See Figure 33–25.

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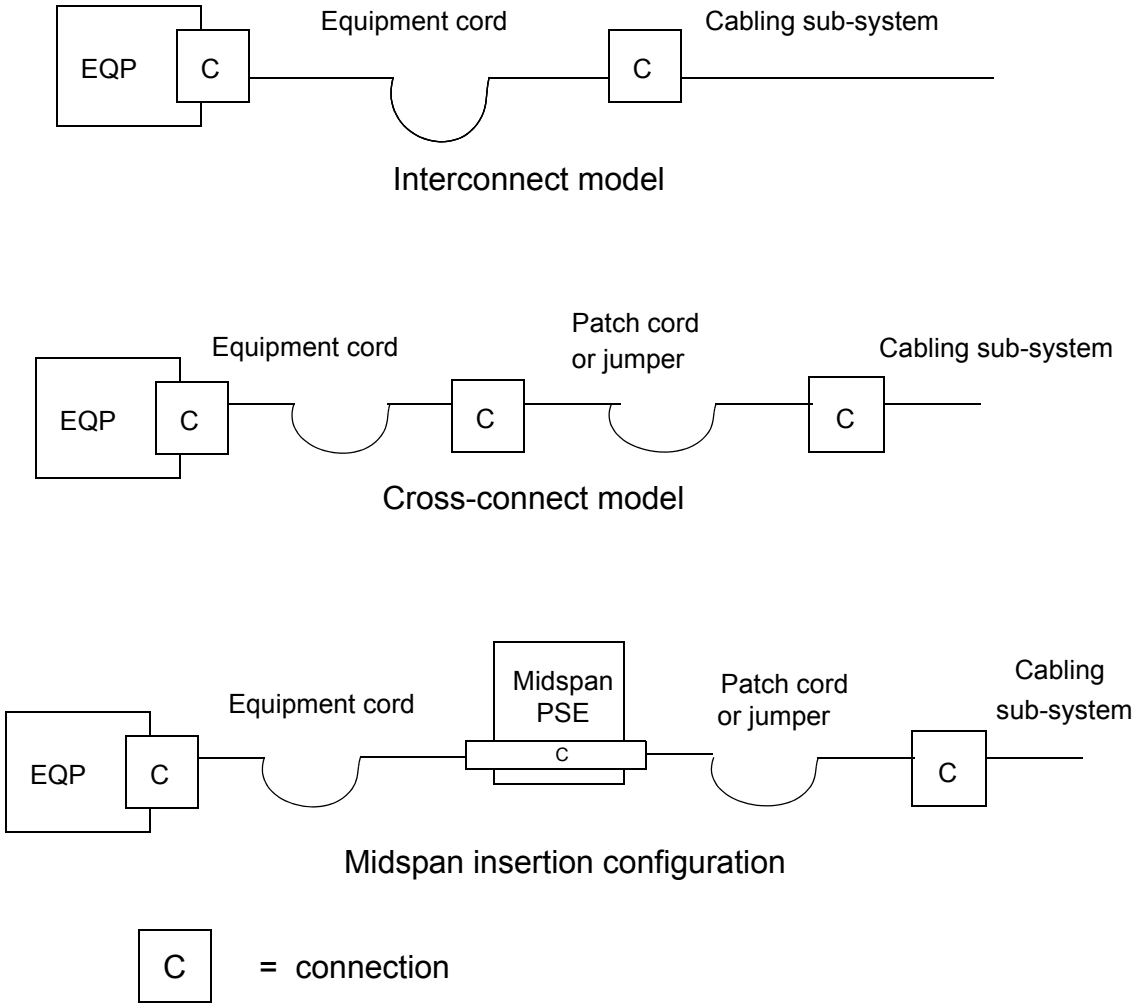


Figure 33–25—Interconnect model, cross-connect model, and midspan insertion configuration

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

a) If the existing FD configuration is of the "Interconnect model" type, the Midspan PSE can be added, provided it does not increase the length of the resulting "channel" to more than specified 100 m as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

b) If the existing FD configuration is of the "Cross-connect model" type, the Midspan PSE needs to be installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the length of the resulting "channel" to more than specified 100 m as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

Configurations with the Midspan PSE in the cabling channel shall not alter the transmission requirements of the "permanent link." A Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.

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The requirements for the two pair Category 5 channel are found in 25.4.9. The specification of Midspan PSE operation on a two pair cable is beyond the scope of this document.

NOTE—Appropriate terminations may be applied to the interrupted pairs on both sides of the Midspan device.

33.4.9.1 "Connector" or "telecom outlet" Midspan PSE device transmission requirements

The Midspan PSE equipment to be inserted as "connector" or "telecom outlet" shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO 11801:2002 or ANSI/TIA-568-C.2 for connecting hardware.

There are four types of Midspan PSEs defined with respect to transmission requirements:

1) 10BASE-T/100BASE-TX connector or telecom outlet Midspan PSE
2) 10BASE-T/100BASE-TX work area or equipment cable Midspan PSE
3) 1000BASE-T connector or telecom outlet Midspan PSE
4) 1000BASE-T work area of equipment cable Midspan PSE

33.4.9.1.1 Near End Crosstalk (NEXT)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. However, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXTconn\}_{\text{dB}} \geq 40.0 - 20.0 \times \log_{10}\left(\frac{f}{100}\right) \quad (33\text{–}18)$$

where

NEXTconn	is the Near End Crosstalk loss
f	is the frequency expressed in MHz

33.4.9.1.2 Insertion loss

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. Insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–19) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. However, for frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB.

$$\{ILconn\}_{\text{dB}} \leq 0.040 \times \sqrt{f} \quad (33\text{–}19)$$

where

ILconn	is the insertion loss
f	is the frequency expressed in MHz

33.4.9.1.3 Return loss

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss for Midspan PSE devices shall meet or exceed the values specified in Table 33–20 when measured for the transmit and receive pairs from 1 MHz to 100 MHz.

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Table 33–20—Connector return loss

Frequency	Return loss
1 MHz ≤ f < 20 MHz	23 dB
20 MHz ≤ f ≤ 100 MHz	14 dB

33.4.9.1.4 Work area or equipment cable Midspan PSE

Replacing the work area or equipment cable with a cable that includes a Midspan PSE should not alter the requirements of the cable. This cable shall meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2 for insertion loss, NEXT, and return loss for the transmit and receive pairs.

33.4.9.2 Midspan signal path requirements

An Alternative A Midspan PSE transfer function gain shall be greater than that expressed by Equation (33–20) for the frequency range from 0.1 MHz to 1 MHz, at the pins of the PI used as 100BASE-TX transmit pins.

$$\left\{ -0.100 + 37.5 \times \log_{10}\left(\frac{22.4 \times f}{\sqrt{1.00 + 521 \times f^2}} \right) \right\} \text{dB} \qquad (33\text{–}20)$$

where

f is the frequency expressed in MHz.

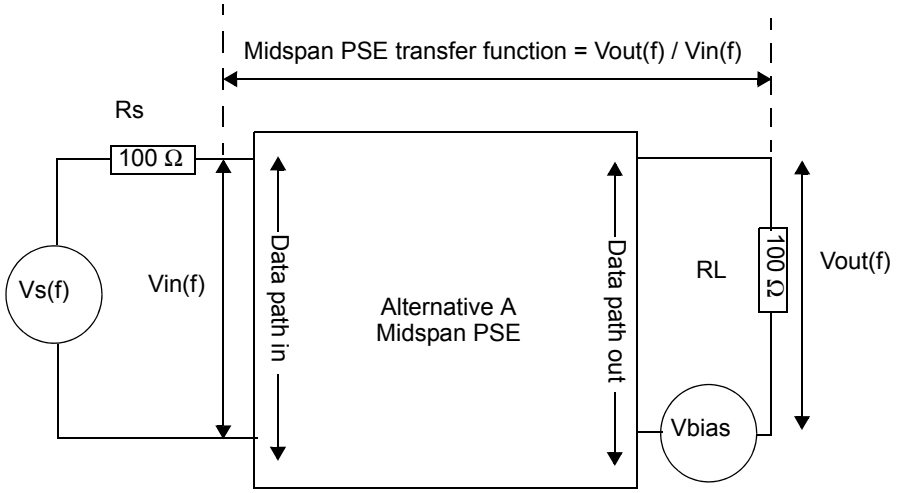
The requirements shall be met with a DC bias current, I_{bias}, between 0 mA and (I_{unb}/2) mA (I_{unb} is defined in Table 33–11).

33.4.9.2.1 Alternative A Midspan PSE signal path transfer function

The transfer function is measured by applying a test signal to the Midspan PSE signal input through a source impedance of 100 Ω ± 1 %. The Midspan PSE signal input and output may be connected to a 0.5 m maximum length of cable, meeting the requirements of 25.4.9, terminated with 100 Ω ± 1 %.

The transfer function is defined from the output termination to the Midspan PSE input. See Figure 33–26.

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Vin(f) is the sine wave signal to be used to measure the Midspan PSE transfer function.
Vbias is the DC offset voltage to be applied in series with RL in order to generate I_{bias}.
Vout(f) is the Midspan PSE response to Vin(f).
Some test equipment may require isolation between measurement ports.

Figure 33–26—Measurement setup for Alternative A Midspan PSE transfer function

33.5 Management function requirements

If the PSE is implemented with a management interface described in 22.2.4 or 45.2 (MDIO), then the management access shall use the PSE register definitions shown in 33.5.1. Where no physical embodiment of the Clause 22 or Clause 45 management is supported, equivalent management capability shall be provided. Managed objects corresponding to PSE and PD control parameters and states are described in Clause 30.

33.5.1 PSE registers

A PSE implementing either Clause 22 or Clause 45 management interface shall use register address 11 for its control and register address 12 for its status functions. The full set of management registers is listed in Table 22–6.

Some of the bits within registers are defined as latching high (LH). When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

33.5.1.1 PSE Control register (Register 11) (R/W)

The assignment of bits in the PSE Control register is shown in Table 33–21. The default value for each bit of the PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

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Table 33–21—PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
11.15:6	Reserved	Ignore when read	RO
11.5	Data Link Layer Classification Capability	1 = Data Link Layer classification capability enabled 0 = Data Link Layer classification capability disabled	R/W
11.4	Enable Physical Layer Classification	1 = Physical Layer classification enabled 0 = Physical Layer classification disabled	R/W
11.3:2	Pair Control	(11.3) (11.2) 1 1 = Reserved 1 0 = PSE pinout Alternative B 0 1 = PSE pinout Alternative A 0 0 = Reserved	R/W
11.1:0	PSE Enable	(11.1) (11.0) 1 1 = Reserved 1 0 = Force Power Test Mode 0 1 = PSE Enabled 0 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

33.5.1.1.1 Reserved bits (11.15:6)

Bits 11.15:6 are reserved for future standardization. They shall not be affected by writes and shall return a value of zero when read. For compatibility with future use of reserved bits and registers, if the management entity writes to a reserved bit, it should use a value of zero. If it reads a reserved bit, it should ignore the results.

33.5.1.1.2 Data Link Layer Classification capability (11.5)

Bit 11.5 controls a PSEs capability of performing Data Link Layer classification as specified in 33.6.

A PSE that does not support Data Link Layer classification shall ignore writes to bit 11.5 and shall return a value of zero when read. A PSE that supports Data Link Layer classification, but does not allow the capability to be disabled, shall ignore writes to bit 11.5 and shall return a value of one when read.

A PSE that supports Data Link Layer classification and supports the ability to enable and disable it shall enable Data Link Layer classification by setting bit 11.5 to one and disable it by setting bit 11.5 to zero.

33.5.1.1.3 Enable Physical Layer classification (11.4)

Bit 11.4 controls Physical Layer classification as specified in 33.2.6. A PSE that indicates support for Physical Layer classification in register 12.13 may also provide the option of disabling Physical Layer classification through bit 11.4.

A PSE that does not support Physical Layer classification shall ignore writes to bit 11.4 and shall return a value of zero when read. A PSE that supports Physical Layer classification, but does not allow the function to be disabled, shall ignore writes to bit 11.4 and shall return a value of one when read.

The Physical Layer classification function shall be enabled by setting bit 11.4 to one and disabled by setting bit 11.4 to zero.

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33.5.1.1.4 Pair Control (11.3:2)

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.1. A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits. Provision of this option is indicated through the Pair Control Ability (12.0) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative.

When read as '01', bits 11.3:2 indicate that only PSE Pinout Alternative A is supported by the PSE. When read as '10', bits 11.3:2 indicate that only PSE Pinout Alternative B is supported by the PSE.

Where the option of controlling the PSE Pinout Alternative through these bits is provided, setting bits 11.3:2 to '01' shall force the PSE to use only PSE Pinout Alternative A and setting bits 11.3:2 to '10' shall force the PSE to use only PSE Pinout Alternative B.

If bit 12.0 is one, writing to these register bits shall set mr_pse_alternative to the corresponding value: '01' = A and '10' = B. The combinations '00' and '11' for bits 11.3:2 are reserved and will never be assigned. Reading bits 11.3:2 returns an unambiguous result of '01' or '10' that may be used to determine the presence of the PSE Control register.

33.5.1.1.5 PSE enable (11.1:0)

The PSE function shall be disabled by setting bit 11.1 to zero and bit 11.0 to zero. When the PSE function is disabled, the MDI shall function as it would if it had no PSE function. The PSE function shall be enabled by setting bits 11.1 to a zero and 11.0 to a one. When bit 11.1 is a one, and bit 11.0 is a zero, a test mode is enabled. This test mode supplies power without regard to PD detection.

Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power. The combination '11' for bits 11.1:0 has been reserved for future use.

CAUTION

Test mode may damage connected non-PD, legacy, twisted pair Ethernet devices, or other non-Ethernet devices, especially in split application wiring schemes.

33.5.1.2 PSE Status register (Register 12) (R/W)

The assignment of bits in the PSE Status register is shown in Table 33–22.

Table 33–22—PSE Status register bit definitions

Bit(s)	Name	Description	R/W[a]
12.15	PSE Type Electrical Parameters	1 = PSE is using Type 2 PSE electrical parameters 0 = PSE is using Type 1 PSE electrical parameters	RO
12.14	Data Link Layer Classification Enabled	1 = Data Link Layer classification is enabled 0 = Data Link Layer classification is not supported or is not enabled	RO
12.13	Physical Layer Classification Supported	1 = PSE supports Physical Layer classification 0 = PSE does not support Physical Layer classification	RO

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Table 33–22—PSE Status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
12.12	Power Denied or Removed	1 = Power has been denied or removed due to fault 0 = Power has not been denied or removed	RO/ LH
12.11	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
12.10	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
12.9	Short Circuit	1 = Short circuit condition detected 0 = No short circuit condition detected	RO/ LH
12.8	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
12.7	MPS Absent	1 = MPS absent condition detected 0 = No MPS absent condition detected	RO/ LH
12.6:4	PD Class	(12.6) (12.5) (12.4) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Invalid Class 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Class 0	RO
12.3:1	PSE Status	(12.3) (12.2) (12.1) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = implementation-specific fault 1 0 0 = Test error 0 1 1 = Test mode 0 1 0 = Delivering power 0 0 1 = Searching 0 0 0 = Disabled	RO
12.0	Pair Control Ability	1 = PSE pinout controllable by Pair Control bits 0 = PSE Pinout Alternative fixed	RO

[a]RO = Read Only, LH = Latched High

33.5.1.2.1 PSE Type electrical parameters (12.15)

When read as a zero, bit 12.15 indicates that the PSE is operating with Type 1 PSE electrical parameters. When read as a one, bit 12.15 indicates that the PSE is operating with Type 2 PSE electrical parameters. This bit shall be set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. This bit shall be set to one when the PSE state diagram sets set_parameter_type to 2.

33.5.1.2.2 Data Link Layer Classification Enabled (12.14)

When read as a one, bit 12.14 indicates the PSE supports Data Link Layer classification as defined in 33.2.6 and that it is enabled. When read as a zero, bit 12.14 indicates that the PSE lacks support for Data Link Layer classification or that Data Link Layer classification is not enabled. If supported, the Data Link Layer classification may be enabled or disabled through the state diagram variable pse_dll_enabled (see 33.2.4.4).

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This bit shall be set to one when the PSE state diagram (Figure 33–9) sets true the state variable pse_dll_enabled. This bit shall be set to zero when the PSE state diagram sets false the state variable pss_dll_enabled.

33.5.1.2.3 Physical Layer Classification Supported (12.13)

When read as a one, bit 12.13 indicates that the PSE supports Physical Layer classification as defined in 33.2.6. When read as a zero, bit 12.13 indicates that the PSE lacks support for Physical Layer classification. If supported, the function may be enabled or disabled through the Enable Physical Layer Classification bit (11.4).

33.5.1.2.4 Power Denied or Removed (12.12)

When read as a one, bit 12.12 indicates that power has been denied or has been removed due to a fault condition. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the states 'POWER_DENIED' or 'ERROR_DELAY.' The Power Denied bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.5 Valid Signature (12.11)

When read as a one, bit 12.11 indicates that a valid signature has been detected. This bit shall be set to one when mr_valid_signature transitions from FALSE to TRUE. The Valid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.6 Invalid Signature (12.10)

When read as a one, bit 12.10 indicates that an invalid signature has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'SIGNATURE_INVALID'. The Invalid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.7 Short Circuit (12.9)

When read as a one, bit 12.9 indicates that a short circuit condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'ERROR_DELAY.' The Short Circuit bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.8 Overload (12.8)

When read as a one, bit 12.8 indicates that an overload condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'ERROR_DELAY_OVER'. The Overload bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.9 MPS Absent (12.7)

When read as a one, bit 12.7 indicates that an MPS Absent condition has been detected. The MPS Absent bit shall be set to one when the PSE state diagram (Figure 33–9) transitions directly from the state POWER_ON to IDLE due to tmpdo_timer_done being asserted. The MPS Absent bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.10 PD Class (12.6:4)

Bits 12.6:4 report the PD Class of a detected PD as specified in 33.2.5 and 33.2.6. The value in this register is valid while a PD is connected, i.e., while the PSE Status (12.3:1) bits are reporting "delivering power." The combinations '110' and '111' for bits 12.6:4 have been reserved for future use.

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33.5.1.2.11 PSE Status (12.3:1)

Bits 12.3:1 report the current status of the PSE. When read as ‘000’, bits 12.3:1 indicate that the PSE state diagram (Figure 33–9) is in the state DISABLED. When read as ‘010’, bits 12.3:1 indicate that the PSE state diagram is in the state POWER_ON. When read as ‘011’, bits 12.3:1 indicate that the PSE state diagram is in the state TEST_MODE. When read as ‘100’, bits 12.3:1 indicate that the PSE state diagram is in the state TEST_ERROR. When read as ‘101’, bits 12.3:1 indicate that the PSE state diagram is in the state IDLE due to the variable error_condition = true. When read as ‘001’, bits 12.3:1 indicate that the PSE state diagram is in a state other than those listed above.

The combinations ‘111’ and ‘110’ for bits 12.3:1 have been reserved for future use.

33.5.1.2.12 Pair Control Ability (12.0)

When read as a one, bit 12.0 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a zero, bit 12.0 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

33.6 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. Type 2 PDs that require more than 13.0 W support Data Link Layer classification (see 33.3.5). Data Link Layer classification is optional for all other devices.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

33.6.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-2009; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2; and shall support the control state diagrams defined in 33.6.3.

33.6.2 Data Link Layer classification timing requirements

A Type 2 PSE shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable pse_dll_enabled (33.2.4.4, 33.6.3.3).

A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable pse_dll_ready (33.6.3.3).

All Type 1 PDs that implement Data Link Layer classification and Type 2 PDs shall set the state variable pd_dll_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enabled (33.3.3.3, 33.6.3.3).

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the “PSE allocated power value” field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the “PD requested power value” field is different from the previously communicated value.

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Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the "PD requested power value" field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the "PSE allocated power value" field is different from the previously communicated value.

33.6.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively. PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–27. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–28.

33.6.3.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.6.3.2 Constants

PD_DLLMAX_VALUE

This value is derived from pd_max_power variable (33.3.3.3) described as follows:

pd_max_power	PD_DLLMAX_VALUE
0	130
1	39
2	65
3	130
4	255

PD_INITIAL_VALUE

This value is derived as follows from the pd_max_power (33.3.3.3) variable used in the PD state diagram (Figure 33–16):

pd_max_power	PD_INITIAL_VALUE
0	≤ 130
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255

PSE_INITIAL_VALUE

This value is derived as follows from parameter_type and the mr_pd_class_detected (33.2.4.6) variable used in the PSE state diagram (Figure 33–9):

parameter_type	mr_pd_class_detected	PSE_INITIAL_VALUE
1	0	130
1	1	39
1	2	65
1	3	130
1	4	130
2	4	255

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33.6.3.3 Variables

The PSE power control state diagram (Figure 33–27) and PD power control state diagram (Figure 33–28) use the following variables:

MirroredPDRequestedPowerValue
: The copy of PDRequestedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17). Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of MirroredPDRequestedPowerValue.
Values:0 through 255

MirroredPDRequestedPowerValueEcho
: The copy of PDRequestedPowerValueEcho that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17).

MirroredPSEAllocatedPowerValue
: The copy of PSEAllocatedPowerValue that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18). Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of MirroredPSEAllocatedPowerValue.
Values:0 through 255

MirroredPSEAllocatedPowerValueEcho
: The copy of PSEAllocatedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18).

PDRequestedPowerValueEcho
: This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).
Values:0 through 255

PDMaxPowerValue
: Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.7.2) the PD ever draws under the current power allocation. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PDMaxPowerValue.

PDRequestedPowerValue
: Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.7.2) the PD requests. This power value is encoded according to Equation (79–1), where *X* is the decimal value of PDRequestedPowerValue. This variable is mapped from the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).
Values:0 through PD_DLLMAX_VALUE

PSEAllocatedPowerValue
: Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.7.2) the PD ever draws. The power value for a PSE is the maximum input average power the PD may ever draw. This power value is encoded according to Equation (79–2), where *X* is the decimal value of PSEAllocatedPowerValue. This variable is mapped from the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).
Values:0 through 255

PSEAllocatedPowerValueEcho
: This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).
Values:0 through 255

TempVar
: A temporary variable used to store Power Value. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1) or Equation (79–2), where *X* is the decimal value of TempVar.

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local_system_change
: An implementation-specific control variable that indicates that the local system wants to change the allocated power value. In a PSE, this indicates it is going to change the power allocated to the PD. In a PD, this indicates it is going to request a new power allocation from the PSE.
Values:FALSE:The local system does not wants to change the power allocation.
TRUE:The local system wants to change the power allocation.

parameter_type
: A control variable output by the PSE state diagram (Figure 33–9) used by a Type 2 PSE to choose operation with Type 1 or Type 2 PSE output PI electrical requirement parameter values defined in Table 33–11.
Values: 1: Type 1 PSE parameter values (default).
2: Type 2 PSE parameter values.

pd_dll_enabled
: A variable output by the PD state diagram (Figure 33–16) to indicate if the PD Data Link Layer classification mechanism is enabled.
Values: FALSE:PD Data Link Layer classification is not enabled.
TRUE:PD Data Link Layer classification is enabled.

pd_dll_power_type
: A control variable that indicates the type of PD that is connected to the PSE as advertised through Data Link Layer classification.
Values: 1: PD is a Type 1 PD (default).
2: PD is a Type 2 PD.

pd_dll_ready
: An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
Values:FALSE:Data Link Layer classification has not completed initialization.
TRUE:Data Link Layer classification has completed initialization.

pse_dll_enabled
: A variable output by the PSE state diagram (Figure 33–9) to indicate if the PSE Data Link Layer classification mechanism is enabled.
Values: FALSE:PSE Data Link Layer classification is not enabled.
TRUE:PSE Data Link Layer classification is enabled.

pse_dll_power_type
: A control variable that indicates the type of the PSE by which the PD is being powered.
Values: 1: PSE is a Type 1 PSE (default).
2: PSE is a Type 2 PSE.

pse_dll_ready
: An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).
Values:FALSE:Data Link Layer classification has not completed initialization.
TRUE:Data Link Layer classification has completed initialization.

pse_power_type
: A control variable output by the PD state diagram (Figure 33–16) to indicate the type of PSE by which it is being powered.

A summary cross-references between the DTE Power via MDI classification local and remote object class attributes and the PSE and PD power control state diagrams, including the direction of the mapping, is provided in Table 33–23.

33.6.3.4 Functions

pse_power_review
: This function evaluates the power allocation or budget of the PSE based on local system changes. The function returns the following variables:

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PSE_NEW_VALUE:

The new max power value that the PSE expects the PD to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of PSE_NEW_VALUE.

pd_power_review

This function evaluates the power requirements of the PD based on local system changes and/or changes in the PSE allocated power value. The function returns the following variables:

PD_NEW_VALUE:

The new max power value that the PD wants to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PD_NEW_VALUE.

Table 33–23—Attribute to state diagram variable cross-reference

Entity	Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class			
PSE	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValueEcho
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValue
	aLldpXdot3LocReady	⇐	pse_dll_ready
PD	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValue
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValueEcho
	aLldpXdot3LocReady	⇐	pd_dll_ready
oLldpXdot3RemSystemsGroup Object Class			
PSE	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValue
	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValueEcho
	aLldpXdot3RemPowerType Value[a] 11 01	 ⇒ ⇒	pd_dll_power_type Value[a] 01 10
PD	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValue
	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValueEcho
	aLldpXdot3RemPowerType Value[a] 10 00	 ⇒ ⇒	pse_dll_power_type Value[a] 01 10

[a]Other value combinations mapping from aLldpXdot3RemPowerType to pd_dll_power_type or pse_dll_power_type are not possible.

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33.6.3.5 State diagrams

The general state change procedure for PSEs is shown in Figure 33–27.

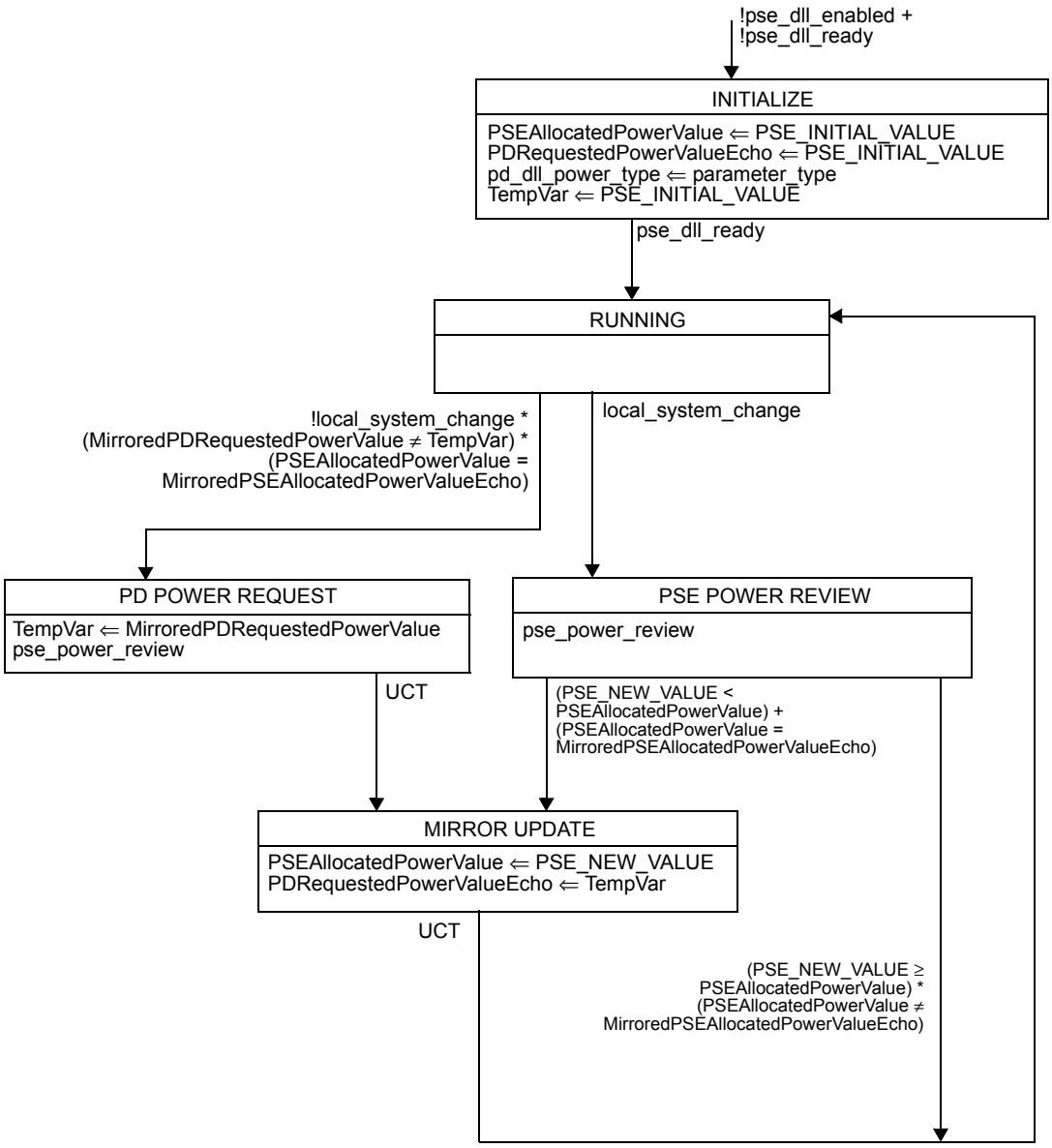


Figure 33–27—PSE power control state diagram

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The general state change procedure for PDs is shown in Figure 33–28.

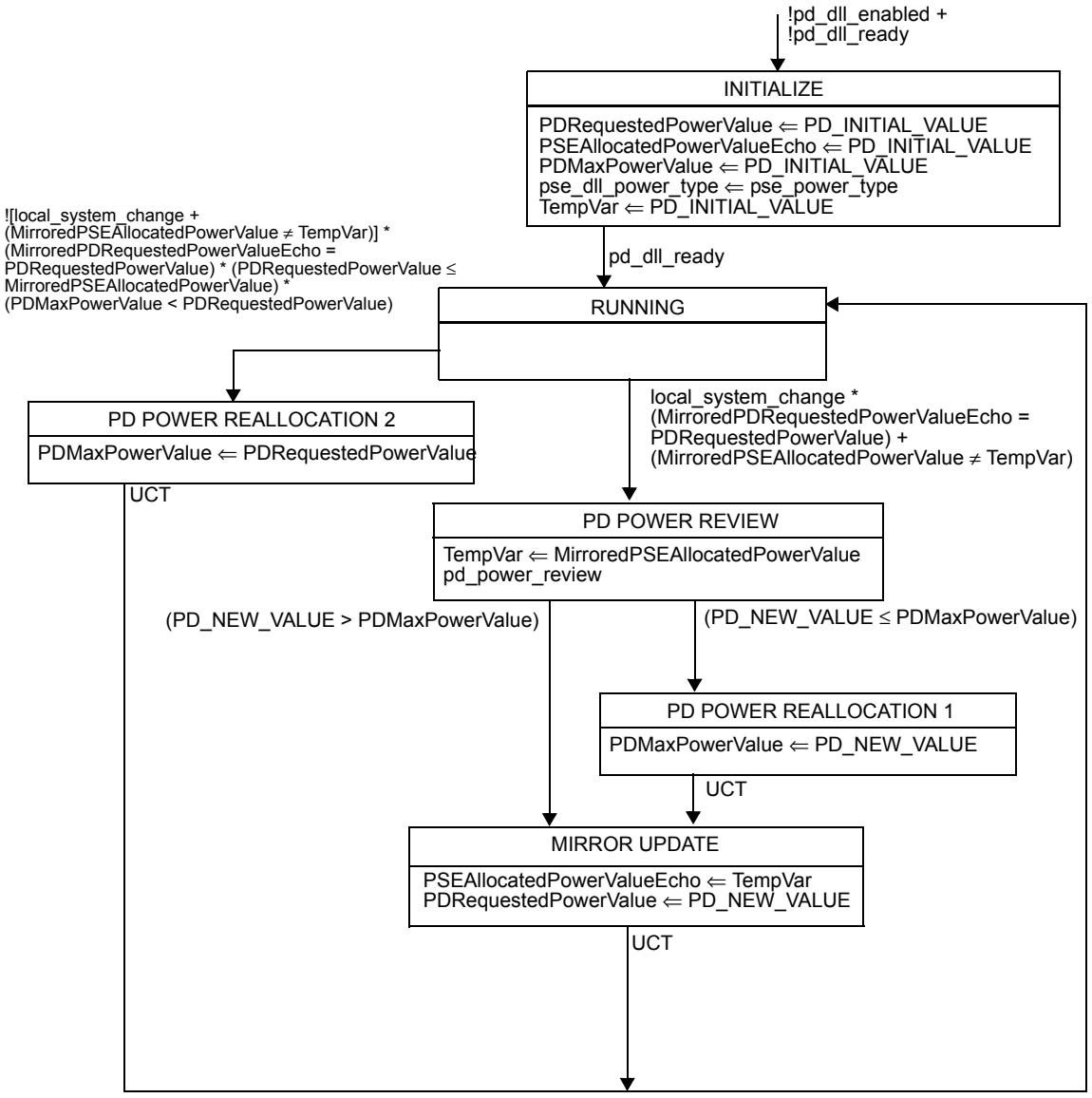


Figure 33–28—PD power control state diagram

33.6.4 State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) in the oLldpXdot3RemSystemsGroup object class

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to the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object class. This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The state diagrams describe the behavior above.

33.6.4.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of MirroredPSEAllocatedPowerValueEcho. When the PSE is not in sync with the PD, the PSE is only allowed to decrease its power allocation.

During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the local_system_change is asserted and the PSE enters the PSE POWER REVIEW state, where a new power allocation value, PSE_NEW_VALUE, is computed. If the PSE is in sync with the PD or if PSE_NEW_VALUE is smaller than PSEAllocatedPowerValue, it enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

If the PSE sees a change to the previously stored MirroredPDRequestedPowerValue, it recognizes a request by the PD to change its power allocation. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new power allocation value, PSE_NEW_VALUE, is computed. It then enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

33.6.4.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue matches the value of MirroredPDRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the RUNNING state. If the PD sees a change to the previously stored MirroredPSEAllocatedPowerValue or local_system_change is asserted by the PD so as to change its power allocation, it enters the PD POWER REVIEW state. In this state, the PD evaluates the change and generates an updated power value called PD_NEW_VALUE. If PD_NEW_VALUE is less than PDMaxPowerValue, it updates PDMaxPowerValue in the PD POWER REALLOCATION 1 state. The PD finally enters the MIRROR UPDATE state where PD_NEW_VALUE is assigned to PDRequestedPowerValue. It also updates PSEAllocatedPowerValueEcho and returns to the RUNNING state.

In the above flow, if PD_NEW_VALUE is greater than PDMaxPowerValue, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD

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POWER REALLOCATION 2 state. In this state, the PD assigns PDMaxPowerValue to PDRequestedPowerValue and returns to the RUNNING state.

33.7 Environmental

33.7.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1. In particular, the PSE shall be classified as a Limited Power Source in accordance with IEC 60950-1.

Equipment shall comply with all applicable local and national codes related to safety.

33.7.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to verify compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to verify that the intended safety features are not negated during installation of a new network or during modification of an existing network.

33.7.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to verify that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

33.7.4 Patch panel considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers' specifications to verify compliance with the appropriate requirements.

33.7.5 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to a PSE or PD. Other than voice signals, the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc, applied to the line through a balanced 400 Ω source impedance. Ringing voltage is a composite signal consisting of an AC component and a DC component. The

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AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 Ω source resistance. The DC component is 56 Vdc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Application of any of the above voltages to the PI of a PSE or a PD shall not result in any safety hazard.

33.7.6 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

33.7.7 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are beyond the scope of this standard.

33.7.8 Labeling

It is recommended that the PSE or PD (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Power classification and power level in terms of maximum current drain over the operating voltage range, 36 V to 57 V, applies for PD only
b) Port type (e.g., 100BASE-TX, TIA Category, or ISO Class)
c) Any applicable safety warnings
d) “PSE” or “PD” as appropriate
e) Type (e.g., “Type 1” or “Type 2”)

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33.8 Protocol implementation conformance statement (PICS) proforma for Clause 33, DTE Power via MDI[21]

33.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 33, DTE Power via MDI, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

33.8.2 Identification

33.8.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

33.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Clause 33, DTE Power via MDI
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3-2015.)	
Date of Statement	

[21] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

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33.8.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDT2	Type 2 PD implementation	33.3.2	PD is Type 2	O	Yes [ ] No [ ]
*PDCL	PD Classification	33.3.5	PD supports classification	PDT2:M	Yes [ ] No [ ]
*PDCL2	Implementation supports 2-Event class signature	33.3.5	PD supports 2-Event class signature	PDT2:M	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PD supports Data Link Layer classification	PDT2:M	Yes [ ] No [ ]

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33.8.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PSET1	Type 1 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*PSET2	Type 2 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.1	PSE implemented as a midspan device	O/1	Yes [ ] No [ ]
*MIDA	Alternative A Midspan PSE	33.2.2	Midspan PSE implements Alternative A	MID:O:2	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.5	Optional	O	Yes [ ] No [ ]
*CL	Implementation supports Physical Layer classification	33.2.6	Optional	O/1	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PSE supports Data Link Layer classification	O	Yes [ ] No [ ]
*1EPLC	Implementation supports 1-Event Physical Layer classification	33.2.6.1	Optional	O	Yes [ ] No [ ]
*2EPLC	Implementation supports 2-Event Physical Layer classification	33.2.6.2	Optional	O	Yes [ ] No [ ]
*PA	Power Allocation	33.2.8	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability—PSE supports the option to control which PSE Pinout is used	33.5.1.1.5	Optional	O	Yes [ ] No [ ]
*AC	Monitor AC MPS	33.2.9.1.1	PSE monitors for AC MPS	O.3	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.9.1.2	PSE monitors for DC MPS	O.3	Yes [ ] No [ ]

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33.8.3 PICS proforma tables for DTE Power via MDI

33.8.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility considerations.	33.1.2	PDs and PSEs compatible at their PIs	M	Yes [ ]
COM2	Type 2 operation cabling	33.1.4.1	DC loop resistance 25 Ω or less. Requirement satisfied by category 5e components (cables, cords, and connectors)	M	Yes [ ]
COM3	Resistance unbalance	33.1.4.2	3 % or less	M	Yes [ ]

33.8.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location	33.2.1	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated	M	Yes [ ]
PSE2	Alternative A and Alternative B	33.2.3	Implement either Alternative A or Alternative B or both but not operate on same link segment simultaneously	M	Yes [ ] N/A [ ]
PSE3	PSE behavior	33.2.4	In accordance with state diagrams shown in Figure 33–9, Figure 33–9 continued, and Figure 33–10	M	Yes [ ]
PSE4	Detection, classification, and turn on timing	33.2.4.1	In accordance with Table 33–4, Table 33–10, and Table 33–11	M	Yes [ ]
PSE5	Backoff voltage	33.2.4.1	Not greater than V_{Off}	M	Yes [ ]
PSE6	PSE variable definition permutations	33.2.4.4	Meet at least one allowable definition described in Table 33–3	M	Yes [ ]
PSE7	Type 2 PSE mutual identification	33.2.4.6	When powering a Type 2 PD, assigns a value of '2' to parameter_type if mutual identification is complete	PSET2: M	Yes [ ] N/A [ ]
PSE8	Type 2 PSE powering a Type 1 PD	33.2.4.6	Meets the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type}	PSET2: M	Yes [ ] N/A [ ]
PSE9	Applying power	33.2.5	Not until a PD requesting power has been successfully detected	M	Yes [ ]
PSE10	Power pairs	33.2.5	Power supplied on the same pairs as those used for detection	M	Yes [ ]
PSE11	Detecting PDs	33.2.5.1	Performed via the PSE PI	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE12	PSE presents non-valid signature	33.2.5.1	As defined in Table 33–15	M	Yes [ ]
PSE13	Open circuit voltage and short circuit current	33.2.5.1	Meet specifications for V_{oc} and I_{sc} in Table 33–4	M	Yes [ ]
PSE14	Backdriven current	33.2.5.1	Not be damaged by up to 5 mA over the range of V_{Port_PSE}	M	Yes [ ]
PSE15	Output capacitance	33.2.5.1	C_{out} in Table 33–11	M	Yes [ ]
PSE16	Detection voltage with a valid PD signature connected	33.2.5.2	Meets V_{valid} in Table 33–4	M	Yes [ ]
PSE17	Detection voltage measurements	33.2.5.2	At least two that create at least ΔV_{test} difference	M	Yes [ ]
PSE18	Control slew rate when switching detection voltages	33.2.5.2	Less than V_{slew} in Table 33–4	M	Yes [ ]
PSE19	Accept as a valid signature	33.2.5.3	R_{good} and C_{good}, with up to V_{os} max and I_{os} max as defined in Table 33–5	M	Yes [ ]
PSE20	Reject as an invalid signature	33.2.5.4	Resistance less than R_{bad} min, resistance greater than R_{bad} max, or capacitance greater than C_{bad} min	M	Yes [ ]
PSE21	Classification permutations	33.2.6	Meet one allowable permutation in Table 33–8	M	Yes [ ]
PSE22	Type 1 PSE does not implement Physical Layer classification	33.2.6	Assign all PDs to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE23	Type 1 PSE failure to complete classification	33.2.6	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE24	Type 2 PSE failure to complete classification	33.2.6	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE25	Provide V_{Class} for 1-Event Physical Layer classification	33.2.6.1	Limited to I_{Class_LIM} as defined by Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE26	Classification polarity for 1-Event Physical Layer classification	33.2.6.1	Same as V_{Port_PSE}	1EPLC: M	Yes [ ] N/A [ ]
PSE27	Classification timing for 1-Event Physical Layer classification	33.2.6.1	In accordance with T_{pdc} in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE28	Measurement result of 1-Event Physical Layer classification I_{Class}	33.2.6.1	Classify PD according to observed current based on Table 33–9	1EPLC: M	Yes [ ] N/A [ ]
PSE29	Measurement timing of 1-Event Physical Layer classification I_{Class}	33.2.6.1	Measurement taken after the minimum relevant class event timing in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE30	Class 4 result for 1-Event Physical Layer classification with a Type 1 PSE	33.2.6.1	Assign the PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE31	Type 1 PSE 1-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE32	Type 2 PSE 1-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE33	In the CLASS_EV1 and CLASS_EV2 states, provide V_{Class}	33.2.6.2	As defined in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE34	Classification timing in CLASS_EV1 state	33.2.6.2	In accordance with T_{CLE1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE35	In the CLASS_EV1 and CLASS_EV2 states, measurement result I_{Class}	33.2.6.2	Classify PD according to Table 33–9	2EPLC: M	Yes [ ] N/A [ ]
PSE36	In the MARK_EV1 and MARK_EV2 states, provide V_{Mark}	33.2.6.2	In accordance with Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE37	Classification timing in MARK_EV1	33.2.6.2	In accordance with T_{ME1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE38	Classification timing in CLASS_EV2 state	33.2.6.2	In accordance with T_{CLE2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE39	Classification timing in MARK_EV2 state	33.2.6.2	In accordance with T_{ME2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE40	Type 2 PSE 2-Event Physical Layer classification if I_{Class} is greater than or equal to I_{Class_LIM} min	33.2.6.2	Returns to IDLE state	2EPLC: M	Yes [ ] N/A [ ]
PSE41	Current limitation during class events	33.2.6.2	Meet I_{Class_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE42	Current limitation during mark events	33.2.6.2	Meet I_{Mark_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE43	Measurement timing of 2-Event Physical Layer classification I_{Class}	33.2.6.2	Taken after the minimum relevant class event timing in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE44	Class event and mark event voltages polarity	33.2.6.2	Same as V_{Port_PSE}	2EPLC: M	Yes [ ] N/A [ ]
PSE45	Voltage level at PI when transition to POWER_ON state	33.2.6.2	Completes 2-Event classification and transitions to POWER_ON with PI voltage greater than or equal to V_{Mark} min	2EPLC: M	Yes [ ] N/A [ ]
PSE46	Return to IDLE state	33.2.6.2	Maintains PI voltage at V_{Reset} for at least T_{Reset} min before starting new detection cycle	2EPLC: M	Yes [ ] N/A [ ]
PSE47	Power supply output	33.2.7	When the PSE provides power to the PI, conforms with Table 33–11	M	Yes [ ]
PSE48	Load regulation	33.2.7.1	Met with (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min load step at a rate of change of at least 15 mA/µs max	M	Yes [ ]
PSE49	Voltage transients	33.2.7.1	Limited to 3.5 V/µs max for load changes up to 35 mA/µs	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE50	Voltage transients (30 µs to 250 µs)	33.2.7.2	No less than K_{Tran_lo} below V_{Port_PSE} min and meet requirements of 33.2.7.7.	PSET2: M	Yes [ ]
PSE51	Voltage transients (greater than 250 µs)	33.2.7.2	Meet V_{Port_PSE} specification	M	Yes [ ]
PSE52	Power feeding ripple and noise	33.2.7.3	Met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min at static operating V_{Port_PSE}	M	Yes [ ]
PSE53	AC current waveform parameters	33.2.7.4	I_{Peak} minimum equals Equation (33–4) for T_{CUT} minimum and 5% duty cycle minimum.	M	Yes [ ]
PSE54	Inrush current limit	33.2.7.5	PSE limits the maximum current sourced at the PI	M	Yes [ ]
PSE55	Inrush current template	33.2.7.5	Current sourced does not exceed the PSE inrush template in Figure 33–13	M	Yes [ ]
PSE56	Short circuit condition	33.2.7.7	Remove power from PI before I_{PSEUT} is exceeded. Equation (33–6) and Figure 33–14.	M	Yes [ ]
PSE57	Short circuit current and time	33.2.7.7	In accordance with I_{LIM} and T_{LIM} in Table 33–11	M	Yes [ ]
PSE58	Short circuit power removal	33.2.7.7	Begins within T_{LIM} in Table 33–11	M	Yes [ ]
PSE59	Turn off time	33.2.7.8	Applies to the discharge time from V_{Port_PSE} to V_{Off} with a test resistor of 320 kΩ attached to the PI.	M	Yes [ ]
PSE60	Turn off voltage	33.2.7.9	Applies to the PI voltage in the IDLE state	M	Yes [ ]
PSE61	Current unbalance	33.2.7.11	Applies to the two conductors of a power pair over the current load range in accordance with I_{unb} in Table 33–11.	M	Yes [ ]
PSE62	Type 2 PSEs in the presence of (I_{unb} / 2)	33.2.7.11	Meet the requirements of 25.4.5	PSET2: M	Yes [ ]
PSE63	Power allocation	33.2.8	Not be based solely on historical data of power consumption of the attached PD	PA:M	Yes [ ] N/A [ ]
PSE64	PSE monitoring AC MPS component	33.2.9.1.1	Meets “AC Signal parameters” and “PSE PI voltage during AC disconnect detection” parameters in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE65	PSE AC MPS component present	33.2.9.1.1	When AC impedance at the PI is equal to or lower than $\|Z_{ac1}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE66	PSE AC MPS component absent	33.2.9.1.1	When AC impedance at the PI equal to or greater than $\|Z_{ac2}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSE67	Power removal	33.2.9.1.1	When AC MPS has been absent for a time duration greater than T_{MPDO}	AC:M	Yes [ ] N/A [ ]
PSE68	PSE DC MPS component present	33.2.9.1.2	I_{Port} is greater than or equal to I_{Hold} max for at least T_{MPS} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE69	PSE DC MPS component absent	33.2.9.1.2	I_{Port} is less than or equal to I_{Hold} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE70	Power removal	33.2.9.1.2	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M	Yes [ ] N/A [ ]
PSE71	Not remove power	33.2.9.1.2	When the DC current is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every $T_{MPS} + T_{MPDO}$	DC:M	Yes [ ] N/A [ ]

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33.8.3.3 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	33.3.1	On either set of PI conductors	M	Yes [ ]
PD2	Polarity insensitive	33.3.1	Both Mode A and Mode B per Table 33–13	M	Yes [ ]
PD3	Source power	33.3.1	The PD does not source power on its PI	M	Yes [ ]
PD4	Voltage tolerance	33.3.1	Withstand 0 V to 57 V at the PI indefinitely without permanent damage	M	Yes [ ]
PD5	Underpowered Type 2 PD	33.3.2	If PD does not successfully observe 2-Event Physical Layer classification or Data Link Layer classification, conforms to Type 1 PD power restrictions and provides the user with an active indication if underpowered	PDT2:M	Yes [ ] N/A [ ]
PD6	Current unbalance	33.3.2	Type 2 PDs meet the requirements of 25.4.5 in presence of (I_{unb}/2)	PDT2:M	Yes [ ] N/A [ ]
PD7	PD behavior	33.3.3	According to state diagram shown in Figure 33–16	M	Yes [ ]
PD8	Valid and non-valid detection signatures	33.3.4	Presented between positive V_{PD} and negative V_{PD} on each set of pairs defined in 33.3.1	M	Yes [ ]
PD9	Non-valid detection signature	33.3.4	When powered, present an invalid signature on the set of pairs not drawing power	M	Yes [ ]
PD10	Valid detection signature	33.3.4	Characteristics defined in Table 33–14	M	Yes [ ]
PD11	Non-valid detection signature	33.3.4	Exhibit one or both of the characteristics described in Table 33–15	M	Yes [ ]
PD12	PD classifications	33.3.5	Meets at least one permutation listed in Table 33–8	PDCL:M	Yes [ ]
PD13	PD implementing 2-Event class signature	33.3.5.1	Returns Class 4	PDCL2:M	Yes [ ] N/A [ ]
PD14	Type 2 PD classification behavior	33.3.5.1	Conforms to electrical specifications in Table 33–17	PDT2:M	Yes [ ] N/A [ ]
PD15	Classification signature	33.3.5.1	As defined in Table 33–16	PDCL:M	Yes [ ] N/A [ ]
PD16	Classification signature	33.3.5.1	One classification signature during classification	PDCL:M	Yes [ ] N/A [ ]
PD17	2-Event class signature	33.3.5.2	Class 4 in accordance with the maximum power draw as specified in Table 33–18	PDCL2:M	Yes [ ] N/A [ ]
PD18	2-Event class signature behavior	33.3.5.2	As defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD19	Type 2 PD electrical requirements	33.3.5.2	As defined by Table 33–18 of the Type defined in its pse_power_type state variable	PDT2:M	Yes [ ] N/A [ ]
PD20	Mark event current and 2-Event class signature	33.3.5.2.1	Draw I_{Mark} and present a non-valid detection signature as defined in Table 33–15	PDCL2:M	Yes [ ] N/A [ ]
PD21	Mark event current limits	33.3.5.2.1	Not exceed I_{Mark} when voltage at the PI enters V_{Mark} as defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]
PD22	PD current draw	33.3.5.2.1	I_{Mark} until the PD transitions from DO_MARK_EVENT state to the IDLE state	PDCL2:M	Yes [ ] N/A [ ]
PD23	PSE identification	33.3.6	Identify as Type 1 or Type 2 (see Figure 33–16)	PDT2:M	Yes [ ]
PD24	PD power supply	33.3.7	Operate within the characteristics in Table 33–18	M	Yes [ ]
PD25	PD turn on voltage	33.3.7.1	PD turns on at a voltage less than or equal to V_{On}	M	Yes [ ]
PD26	PD stay on voltage	33.3.7.1	Stay on for all voltages in the range of V_{Port_PD}	M	Yes [ ]
PD27	PD turn off voltage	33.3.7.1	Turn off at a voltage less than V_{Port_PD} min and greater than V_{Off}	M	Yes [ ]
PD28	Startup oscillations	33.3.7.1	Shall turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]
PD29	P_{Port_PD} definition	33.3.7.2.1	When PD is fed by V_{Port_PD} min to V_{Port_PD} max with R_{Ch} (as defined in Table 33–1) in series	M	Yes [ ]
PD30	Type 2 PD input inrush current	33.3.7.3	With pse_power_type state set to 2 prior to power-on, operate as a Type 1 PD for at least T_{delay} min	PDT2:M	Yes [ ] N/A [ ]
PD31	Input inrush current	33.3.7.3	Limited by the PD if C_{port} is greater than or equal to 180 μF so that I_{Inrush_PD} max is satisfied.	M	Yes [ ]
PD32	Peak power	33.3.7.4	Not to exceed P_{Class_PD} max for more than T_{CUT} min and 5% duty cycle	M	Yes [ ]
PD33	Peak operating power	33.3.7.4	Not to exceed P_{Peak} max	M	Yes [ ]
PD34	RMS, DC, and ripple current	33.3.7.4	Bounded by Equation (33–10)	M	Yes [ ]
PD35	Maximum I_{Port} for all operating V_{Port_PD}	33.3.7.4	Defined by Equation (33–11)	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PD36	Peak transient current	33.3.7.5	Not to exceed 4.70 mA/μs in either polarity	M	Yes [ ]
PD37	Specifications for I_{PDUT}	33.3.7.5	Operate below upperbound template defined in Figure 33–18	M	Yes [ ]
PD38	Behavior during transients at the PSE PI	33.3.7.6	As specified in 33.3.7.6	M	Yes [ ]
PD39	Ripple and noise	33.3.7.7	As specified in Table 33–18 for the common-mode and/or differential pair-to-pair noise at the PD PI	M	Yes [ ]
PD40	Ripple and noise specification	33.3.7.7	For all operating voltages in the range defined by V_{Port_PD} in Table 33–18	M	Yes [ ]
PD41	Ripple and noise presence	33.3.7.7	Operates in the presence of ripple and noise generated by the PSE that appears at the PD PI	M	Yes [ ]
PD42	Classification stability	33.3.7.8	Class signature valid within T_{class} and remains valid for the duration of the classification period	M	Yes [ ]
PD43	Backfeed voltage	33.3.7.9	Mode A and Mode B per 33.3.7.9	M	Yes [ ]
PD44	Maintain power signature	33.3.8	PD provides a valid MPS at the PI as defined in 33.3.8	M	Yes [ ]
PD45	No longer require power	33.3.8	Remove both components of the Maintain Power Signature	M	Yes [ ]

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33.8.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Conductor isolation	33.4.1	Provided between accessible external conductors including frame ground and all MDI leads	M	Yes [ ]
EL2	Strength tests for electrical isolation	33.4.1	Withstand at least one of the electrical strength tests specified in 33.4.1	M	Yes [ ]
EL3	Insulation breakdown	33.4.1	No breakdown of insulation during electrical isolation tests	M	Yes [ ]
EL4	Isolation resistance	33.4.1	At least 2 MΩ, measured at 500 Vdc after electrical isolation tests	M	Yes [ ]
EL5	Isolation and grounding requirements	33.4.1	Conductive link segments that have different requirements have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL6	Environment A requirements for multiple instances of PSE and/or PD	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL7	Environment A requirement	33.4.1.1.1	Switch more negative conductor	M	Yes [ ] N/A [ ]
EL8	Environment B requirements for multiple instances of PSE and/or PD	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL9	Fault tolerance for PIs encompassed within the MDI	33.4.2	Meet requirements of the appropriate specifying clause	!MID:M	Yes [ ] N/A [ ]
EL10	Fault tolerance for PSE PIs not encompassed within an MDI	33.4.2	Meet the requirements of 33.4.2	M	Yes [ ] N/A [ ]
EL11	Common-mode fault tolerance	33.4.2	Each wire pair withstands without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity	M	Yes [ ]
EL12	The shape of the impulse for item common-mode fault tolerance	33.4.2	0.3/50 µs (300 ns virtual front time, 50 µs virtual time of half value)	M	Yes [ ]
EL13	Common-mode to differential-mode impedance balance for transmit and receive pairs	33.4.3	Exceeds Equation (33–15) for 10 Mb/s PHYs and Equation (33–16) for 100Mb/s or greater PHYs	M	Yes [ ]
EL14	Common-mode AC output voltage	33.4.4	Magnitude while transmitting data and with power applied does not exceed 50 mV peak when operating at 10 Mb/s and 50 mV peak-to-peak when operating at 100 Mb/s or greater	M	Yes [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
EL15	Frequency range for common-mode AC output voltage measurement	33.4.4	From 1 MHz to 100 MHz	M	Yes [ ]
EL16	Common-mode AC output voltage measurement	33.4.4	While the PHY is transmitting data, the PSE or PD is operating, and with the enumerated PSE load or PD source	M	Yes [ ]
EL17	Noise from an operating PSE or PD to the differential transmit and receive pairs	33.4.6	Does not exceed 10 mV peak-to-peak measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4	M	Yes [ ]
EL18	Return loss requirements	33.4.7	Specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY	M	Yes [ ]
EL19	100BASE-TX Type 2 Endpoint PSE and PD channel unbalance	33.4.8	Meet requirements of Clause 25 in the presence of (I_{unb}/2)	M	Yes [ ] N/A [ ]

33.8.3.5 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	Short circuit fault tolerance	33.4.2	Any wire pair withstands any short circuit to any other pair for an indefinite amount of time	M	Yes [ ]
PSEEL2	Magnitude of short circuit current	33.4.2	Does not exceed I_{LIM} max	M	Yes [ ]
PSEEL3	Limitation of electromagnetic interference.	33.4.5	PSE complies with applicable local and national codes	M	Yes [ ]
PSEEL4	Alternative A Type 2 Midspan PSEs that support 100BASE-TX	33.4.8	Enforce channel unbalance currents less than or equal to Type 1 Iunb (see Table 33–11) or meet 33.4.9.2.	MIDA: M	Yes [ ] N/A [ ]
PSEEL5	Insertion of Midspan at FD	33.4.9	Comply with the guidelines specified in 33.4.9 items a) and b)	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”	33.4.9	Installation of a Midspan PSE does not increase the length to more than 100 m as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]
PSEEL7	Configurations with Midspan PSE	33.4.9	Not alter transmission requirements of the “permanent link”	MID:M	Yes [ ] N/A [ ]
PSEEL8	DC continuity in power injecting pairs	33.4.9	Does not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL9	Midspan PSE inserted as a “connector” or “telecom outlet”	33.4.9.1	Meet transmission parameters NEXT, insertion loss, and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE NEXT	33.4.9.1.1	Meet values detemined by Equation (33–18) from 1 MHz to 100 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE Insertion Loss	33.4.9.1.2	Meet values determined by Equation (33–19) from 1 MHz to 100 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE Return Loss	33.4.9.1.3	Meet or exceed values in Table 33–20 for transmit and receive pairs from 1 MHz to 100 MHz	MID:M	Yes [ ] N/A [ ]
PSEEL13	Work area or equipment cable Midspan PSE	33.4.9.1.4	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 or ANSI/TIA-568-C.2 for insertion loss, NEXT, and return loss for transmit and receive pairs	MID:M	Yes [ ] N/A [ ]
PSEEL14	Alternative A Midspan PSE signal path requirements	33.4.9.2	Exceed transfer function gain expressed in Equation (33–20) from 0.10 MHz to 1 MHz at the pins of the PI used as 100BASE-TX transmit pins	MIDA: M	Yes [ ] N/A [ ]
PSEEL15	Alternative A Midspan PSE signal path requirements bias current	33.4.9.2	Met with DC bias current between 0 mA and (I_{unb}/2)	MIDA: M	Yes [ ] N/A [ ]

33.8.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD common-mode test requirement	33.4.4	The PIs that require power terminated as illustrated in Figure 33–22	M	Yes [ ]

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33.8.3.7 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability	33.5	Access to register definitions defined in 33.5.1 via interface described in 22.2.4 or 45.2 or equivalent	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers	33.5.1	Register address 11 for control functions and register address 12 for status functions	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH)	33.5.1	Remain high until read via the management interface	MAN:M	Yes [ ] N/A [ ]
MF4	Latching register bit after read	33.5.1	Assumes a value based on the current state of the condition it monitors	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:6)	33.5.1.1.1	Not affected by writes and return a value of zero when read	MAN:M	Yes [ ] N/A [ ]
MF6	Data Link Layer classification not supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of zero when read	MAN* !DLLC:M	Yes [ ] N/A [ ]
MF7	Data Link Layer classification supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of one when function cannot be disabled	MAN* DLLC:M	Yes [ ] N/A [ ]
MF8	Enable/disable Data Link Layer classification capability	33.5.1.1.2	Capability enabled by setting bit 11.5 to one and disabled by setting bit 11.5 to zero	MAN* DLLC:M	Yes [ ] N/A [ ]
MF9	Physical Layer classification not supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of zero when read	MAN* !CL:M	Yes [ ] N/A [ ]
MF10	Physical Layer classification supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of one when function cannot be disabled	MAN* CL:M	Yes [ ] N/A [ ]
MF11	Enable/disable Physical Layer classification	33.5.1.1.3	Function enabled by setting bit 11.4 to one and disabled by setting bit 11.5 to zero	MAN* CL:M	Yes [ ] N/A [ ]
MF12	Pair Control Ability not supported	33.5.1.1.4	Ignore writes to bits 11.3:2	MAN* !PCA:M	Yes [ ] N/A [ ]
MF13	Writes to 11.3:2 when Pair Control Ability not supported	33.5.1.1.4	Return the value that reports the supported PSE Pinout Alternative	MAN* !PCA:M	Yes [ ] N/A [ ]
MF14	Bits 11.3:2 set to '01'	33.5.1.1.4	Forces the PSE to use Alternative A	MAN* PCA:M	Yes [ ] N/A [ ]
MF15	Bits 11.3:2 set to '10'	33.5.1.1.4	Forces the PSE to use Alternative B	MAN* PCA:M	Yes [ ] N/A [ ]
MF16	Pair control ability bit (12.0)	33.5.1.1.4	A value of one sets the mr_pse_alternative variable	MAN* PCA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF17	PSE function disabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a '00', also the MDI shall function as it would if it had no PSE function	MAN:M	Yes [ ] N/A [ ]
MF18	PSE function enabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a '01'	MAN:M	Yes [ ] N/A [ ]
MF19	PSE enable bits (11.1:0)	33.5.1.1.5	Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power	MAN:M	Yes [ ] N/A [ ]
MF20	PSE Type electrical parameters bit (12.15)	33.5.1.2.1	Set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. Set to one when set_parameter_type is set to 2	MAN:M	Yes [ ] N/A [ ]
MF21	Data Link Layer classification enabled bit (12.14)	33.5.1.2.2	Set to one when the PSE state diagram sets true pse_dll_enabled. Set to zero when the PSE state diagram sets false pss_dll_enabled	MAN:M	Yes [ ] N/A [ ]
MF22	Power denied bit (12.12)	33.5.1.2.4	A value of one indicates power has been denied or removed due to an error condition	MAN:M	Yes [ ] N/A [ ]
MF23	Power denied bit implementation	33.5.1.2.4	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF24	Valid signature bit (12.11)	33.5.1.2.5	One indicates a valid signature has been detected. Set to one when mr_valid_signature transitions from FALSE to TRUE.	MAN:M	Yes [ ] N/A [ ]
MF25	Valid signature bit implementation	33.5.1.2.5	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF26	Invalid signature bit (12.10)	33.5.1.2.6	One indicates an invalid signature has been detected. Set to one entering SIGNATURE_INVALID state	MAN:M	Yes [ ] N/A [ ]
MF27	Invalid signature bit implementation	33.5.1.2.6	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF28	Short circuit bit (12.9)	33.5.1.2.7	Bit indicates a short circuit condition has been detected. Set to one entering ERROR_DELAY state.	MAN:M	Yes [ ] N/A [ ]
MF29	Short circuit bit implementation	33.5.1.2.7	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF30	Overload bit (12.8)	33.5.1.2.8	Bit indicates an overload condition has been detected. Set to one when entering the ERROR_DELAY_OVER state	MAN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MF31	Overload bit implementation	33.5.1.2.8	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF32	MPS absent bit (12.7)	33.5.1.2.9	Bit indicates an MPS Absent condition has been detected. Set to one when transitions directly from POWER_ON to IDLE state when $\overline{\text{MPS}}$ is absent for a duration greater than T_{MPDO} as specified in 33.2.9	MAN:M	Yes [ ] N/A [ ]
MF33	MPS Absent bit implementation	33.5.1.2.9	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]

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33.8.3.8 Data Link Layer classification requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLL1	Reserved fields	33.6	Reserved fields in Power via MDI TLV transmitted as zeroes and ignored upon receipt	M	Yes [ ] N/A [ ]
DLL2	Data Link Layer classification standards compliance	33.6.1	Meet mandatory parts of IEEE Std 802.1AB-2009	DLLC:M	Yes [ ] N/A [ ]
DLL3	TLV frame definitions	33.6.1	Meet requirements for Type, Length, and Value (TLV) defined in 79.3.2	DLLC:M	Yes [ ] N/A [ ]
DLL4	Control state diagrams	33.6.1	Meet state diagrams defined in 33.6.3	DLLC:M	Yes [ ] N/A [ ]
DLL5	Type 2 PSE LLDPDU	33.6.2	Transmitted within 10 seconds of Data Link Layer classification being enabled as indicated by pse_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL6	Type 1 PSE LLDPDU	33.6.2	Transmitted when Data Link Layer classification is ready as indicated by pse_dll_ready	DLLC:M	Yes [ ] N/A [ ]
DLL7	PD Data Link Layer classification ready	33.6.2	Set state variable pd_dll_ready within 5 min of Data Link Layer classification being enabled as indicated by pd_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL8	PD requested power value change	33.6.2	LLDPDU with updated “PSE allocated power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL9	PSE allocated power value change	33.6.2	LLDPDU with updated “PD requested power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL10	PSE power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–27	DLLC:M	Yes [ ] N/A [ ]
DLL11	PD power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–28	DLLC:M	Yes [ ] N/A [ ]

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33.8.3.9 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	33.7.1	Conforms to IEC 60950-1:2001	M	Yes [ ]
ES2	PSE classified as a limited power source	33.7.1	In accordance with IEC 60950-1:2001	M	Yes [ ]
ES3	Safety	33.7.1	Comply with all applicable local and national codes	M	Yes [ ]
ES4	Telephony voltages	33.7.5	Application thereof described in 33.7.5 not result in any safety hazard	M	Yes [ ]
ES5	Limitation of electromagnetic interference	33.7.6	PD and PSE powered cabling comply with applicable local and national codes	M	Yes [ ]

33.8.3.10 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	33.7.1	Limited Power Source in accordance with IEC 60950-1:2001	M	Yes [ ]

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NOTE—The remaining annexes in the standard are numbered in correspondence to their associated clauses; e.g., Annexes 22A, 22B, 22C, and 22D correspond to Clause 22.

Annex 22A

(informative)

MII output delay, setup, and hold time budget

22A.1 System model

The discussion of signal timing characteristics that follows will refer to the system model depicted in Figure 22A–1, Figure 22A–2, and Figure 22A–3. This system model can be applied to each of the three application environments defined in 22.2.1.

Figure 22A–1 depicts a simple system model in which the MII is used to interconnect two integrated circuits on the same circuit assembly. In this model the Reconciliation sublayer comprises one integrated circuit, and the PHY comprises the other. A Reconciliation sublayer or a PHY may actually be composed of several separate integrated circuits. The system model in Figure 22A–1 includes two unidirectional signal transmission paths, one from the Reconciliation sublayer to the PHY and one from the PHY to the Reconciliation sublayer. The path from the Reconciliation sublayer to the PHY is separated into two sections, labeled A1 and B1. The path from the PHY to the Reconciliation sublayer is separated into two sections, labeled C1 and D1.

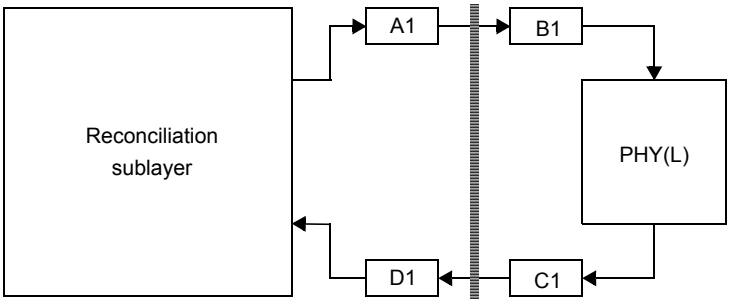


Figure 22A–1—Model for integrated circuit to integrated circuit connection

Figure 22A–2 depicts a system model for the case where the MII is used to interconnect two circuit assemblies. The circuit assemblies may be physically connected in a motherboard/daughterboard arrangement, or they may be physically connected with the cable defined in 22.4.5 and the line interface connector defined in 22.6. The system model in Figure 22A–2 includes two unidirectional signal transmission paths, one from the Reconciliation sublayer to the PHY and one from the PHY to the Reconciliation sublayer. The path from the Reconciliation sublayer to the PHY is separated into two sections, labeled A2 and B2. The path from the PHY to the Reconciliation sublayer is separated into two sections, labeled C2 and D2.

Figure 22A–3 depicts a system model in which the MII is used to interconnect both integrated circuits and circuit assemblies. This system model allows for separate signal transmission paths to exist between the Reconciliation sublayer and a local PHY(L), and between the Reconciliation sublayer and a remote PHY(R). The unidirectional paths between the Reconciliation sublayer and the PHY(L) are composed of sections A1,

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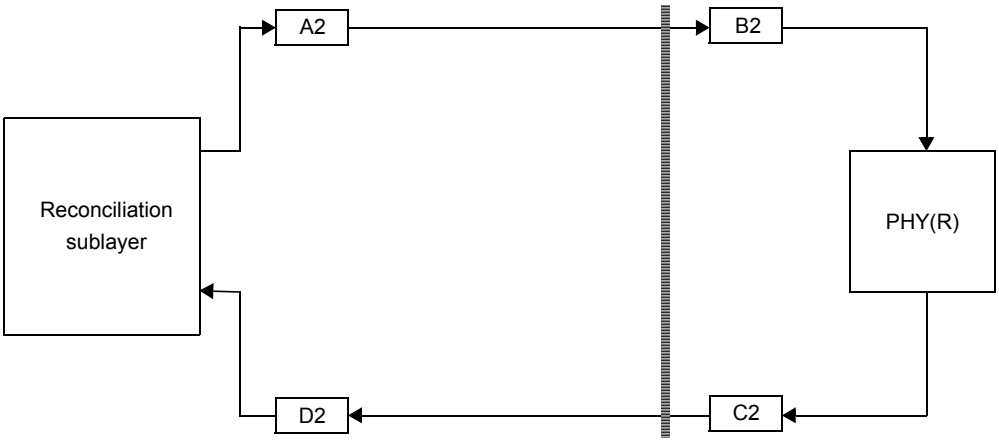


Figure 22A–2—Model for circuit assembly to circuit assembly connection

B1, C1, and D1. The unidirectional paths between the Reconciliation sublayer and the remote PHY(R) are composed of sections A2, B2, C2, and D2.

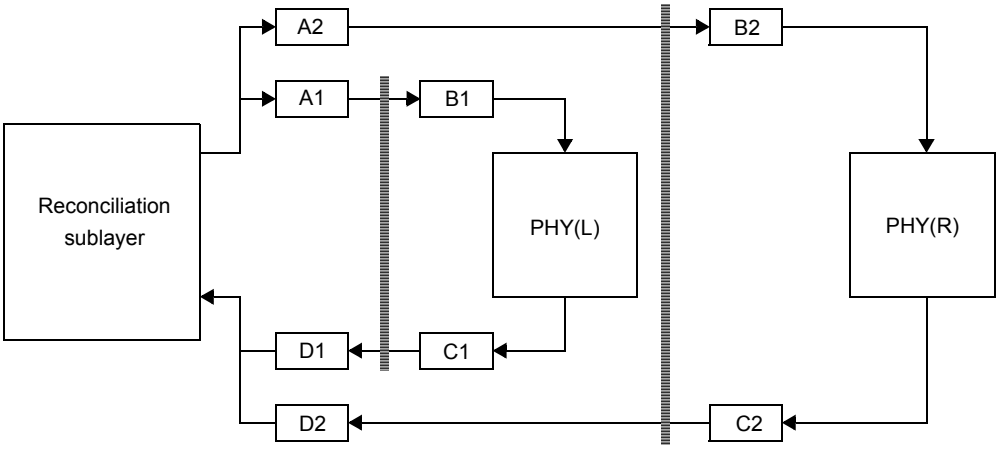


Figure 22A–3—Combined model

Each of these system models assumes a set of common timing and electrical characteristics that shall be met at the input and output ports of the Reconciliation sublayer and PHY devices. The characteristics of the signal transmission paths are identified for each of the sections A1, B1, C1, D1, A2, B2, C2, and D2.

22A.2 Signal transmission path characteristics

The signal transmission path characteristics are specified for each of the path sections defined in 22A.1. The characteristics for these sections are specified so as to allow sections A1, B1, C1, and D1 to be implemented in the form of printed circuit board traces, while sections A2, B2, C2, and D2 may be implemented with a combination of printed circuit board traces and wire conductors in a cable assembly.

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The signal transmission path characteristics are stated in terms of their maximum delay and their characteristic impedance. These values are summarized in Table 22A–1.

Table 22A–1—Signal transmission path characteristics

Section	Maximum delay (ns)	Impedance (Ω)
A1, D1	5	68 ± 15%
B1, C1	2.5	68 ± 15%
A2, D2	5	68 ± 10%
B2, C2	2.5	68 ± 10%

The driver characteristics specified in 22.4.3, the receiver characteristics specified in 22.4.4, and the signal transmission path characteristics specified in Table 22A–1 can be applied to the system models shown in Figure 22A–1 or Figure 22A–2. The combination of loads presented in Figure 22A–3 cannot be adequately driven by an output buffer that meets the driver characteristics specified in 22.4.3 while being sampled by an input buffer that meets the receiver characteristics specified in 22.4.4.

To address the system model depicted in Figure 22A–3, it is permissible to incorporate an additional stage of buffering into path sections A1, A2, D1, and D2, provided that the resulting maximum delay characteristic for those path sections does not exceed the value stated in Table 22A–1. The delay characteristic for transmission path sections A2 and D2 includes an allowance for the delay that results from the presence of a lumped capacitive load at the end of the path. For a transmission path section with a characteristic impedance Z_o, with a lumped capacitive load C_L, this delay is nominally Z_oC_L. In the case of a maximum transmission path section impedance of 78 Ω with a lumped load of 8 pF, the nominal delay is 0.6 ns. Thus the allowable delay for a buffer inserted into transmission path section A2 or D2 is 4.4 ns.

22A.3 Budget calculation

A recommended timing budget is shown in Table 22A–2. This budget assumes that the combined system model shown in Figure 22A–3 represents a worst case.

Table 22A–2—Round-trip delay budget

Description	Incremental delay (ns)	Cumulative delay (ns)
TX_CLK output at PHY(R)	0.0	0.0
Transmission path section C2	2.5	2.5
Transmission path section D2	5.0	7.5
Clock to output in Reconciliation sublayer	15.0	22.5

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Table 22A–2—Round-trip delay budget *(continued)*

Description	Incremental delay (ns)	Cumulative delay (ns)
Transmission path section A2	5.0	27.5
Transmission path section B2	2.5	30.0
Setup time at PHY(R)	10.0	40.0

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Annex 22B

(informative)

MII driver ac characteristics

22B.1 Implications of CMOS ASIC processes

For MII drivers that drive rail to rail, such as those commonly used in CMOS ASICs (complimentary metal oxide semiconductor application-specific integrated circuits), the ac characteristic performance requirements of 22.4.3.2 can be met if the V_{oh} vs. I_{oh} and V_{ol} vs. I_{ol} dc characteristics of the driver stay within the unshaded areas of Figure 22B–1.

The variation in output resistance of a field effect transistor (FET) due to variations in supply voltage, temperature, and process may require that a resistance be placed in series with the output of the FETs to meet this specification. The series resistance can be part of the driver circuit, or external to the driver. If the series resistance is not part of the driver circuit, the driver vendor shall specify the value of series resistance required to meet the specification. A series resistor used to meet this specification is conceptually part of the driver regardless of whether it is physically internal or external to the driver.

The propagation delay of the path between the driver and an external series resistor used to meet the specification shall not exceed 10% of the 10–90% rise/fall time of the driver.

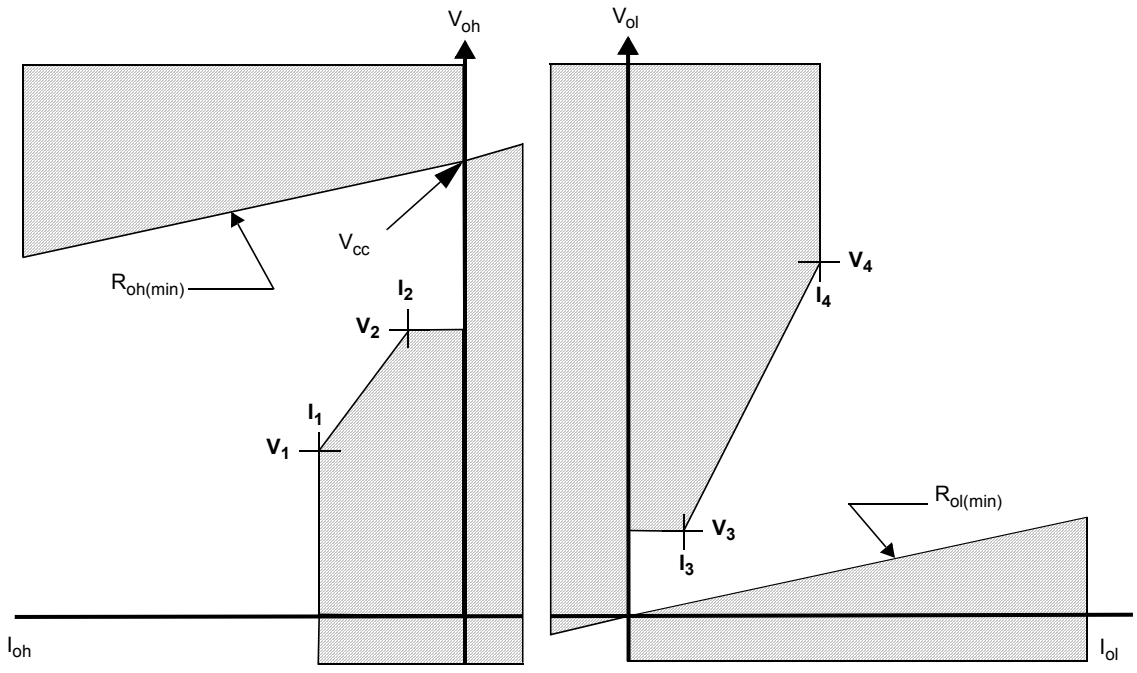


Figure 22B–1—Driver output V–I curve

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22B.2 $R_{o(min)}$ and V, I values for operation from 5 V ± 10% supply

Referring to Figure 22B–1, $R_{oh(min)}$ and $R_{ol(min)}$ both equal 40 Ω, and the values for the V-I points on the curve are given in Table 22B–1 for MII drivers that drive rail to rail from a +5 V ± 10% power supply.

Table 22B–1—Values for driver output V-I curve (5 V supply)

V–I point	I (mA)	V (V)
I_1, V_1	–20	1.10
I_2, V_2	–4	2.4
I_3, V_3	4	0.40
I_4, V_4	43	3.05

22B.3 $R_{o(min)}$ and V, I values for operation from 3.3 V ± 0.3 V supply

Referring to Figure 22B–1, $R_{oh(min)}$ and $R_{ol(min)}$ both equal 33 Ω, and the values for the V–I points on the curve are given in Table 22B–2 for MII drivers that drive rail to rail from a +3.3 V ± 0.3 V power supply.

Table 22B–2—Values for driver output V-I curve (3.3 V supply)

V-I point	I (mA)	V (V)
I_1,V_1	–20	1.10
I_2,V_2	–4	2.4
I_3,V_3	4	0.40
I_4,V_4	26	2.10

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Annex 22C

(informative)

Measurement techniques for MII signal timing characteristics

22C.1 Measuring timing characteristics of source terminated signals

The measurement of timing relationships between MII signals at the MII connector is complicated by the use of driver output impedance to control transmission line reflections on point-to-point transmission paths passing through the connector. The voltage waveforms on point-to-point transmission paths can be different at the MII connector and at the end of the paths. A clean transition (or step) from one logic state to the other at the end of a point to point path can appear as two half-steps at the MII connector.

To eliminate ambiguity as to where on a two half-step state transition to measure timing, all timing measurements on point-to-point transmission paths will be at the end of the path. In some cases, an end of path must be artificially created.

22C.2 Measuring timing characteristics of transmit signals at the MII

The timing of TX_EN, TX_ER, and TXD<3:0> relative to TX_CLK at the MII connector is measured as follows.

Use the time base for TX_CLK as a timing reference. Break the TX_CLK path at the MII connector, forcing the TX_CLK point-to-point transmission path to end at the connector. Measure when the rising edge of TX_CLK passes through $V_{ih(min)}$ at the MII connector. Call this time T_{clk}. Reconnect the TX_CLK path at the MII connector and break the paths of TX_EN, TX_ER, and TXD<3:0> at the MII connector, forcing the paths to end at the connector. Measure when TX_EN, TX_ER, and TXD<3:0> exit the switching region at the MII connector. Call these times T_{en}, T_{er}, and $T_{<3:0>}$, respectively.

The timing relationships at the MII connector for TX_EN, TX_ER, and TXD<3:0> relative to TX_CLK are met if ($T_{en} - T_{clk}$), ($T_{er} - T_{clk}$), ($T_3 - T_{clk}$), ($T_2 - T_{clk}$), ($T_1 - T_{clk}$), and ($T_0 - T_{clk}$), respectively, meet the timing relationships specified in 22.3.1.

22C.3 Measuring timing characteristics of receive signals at the MII

The timing of RX_DV, RX_ER, and RXD<3:0> relative to RX_CLK at the MII connector is measured as follows.

Break the paths of RX_CLK, RX_DV, RX_ER, and RXD<3:0> at the MII connector, forcing the paths to end at the connector. Measure when RX_DV, RX_ER, and RXD<3:0> exit the switching region at the MII connector relative to when the rising edge of RX_CLK passes through $V_{il(max)}$). Also measure when RX_DV, RX_ER, and RXD<3:0> reenter the switching region relative to when the rising edge of RX_CLK passes through $V_{ih(min)}$.

The timing relationships at the MII connector for RX_DV, RX_ER, and RXD<3:0> relative to RX_CLK are met if the times measured in the previous step meet the timing relationships specified in 22.3.2.

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22C.4 Measuring timing characteristics of MDIO

The MDIO and MDC signal timing characteristics cannot be measured using the techniques defined for the transmit and receive signals since MDIO and MDC may connect a single station management entity to multiple PHY devices. The MDIO and MDC timing characteristics are measured with a PHY connected to the MII connector. The signal timing characteristics for MDC and MDIO must be met over the range of conditions which occur when from one to 32 PHYs are connected to an STA. When 32 PHYs are connected to an STA, the total capacitance can be as large as 390 pF on MDC, and as large as 470 pF on MDIO.

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Annex 22D

(informative)

Clause 22 access to Clause 45 MMD registers

Clause 22 provides access to registers in a Clause 45 MMD using Registers 13 and 14. This informative annex provides users with some insight how these registers can be utilized to access Clause 45 MMD registers. Accesses to Registers 13 and 14, for the purpose of accessing registers in a Clause 45 MMD, should be performed atomically to avoid the chance of another process changing the Function, DEVAD or address fields within the MMD. This is the same requirement of Clause 45 accesses.

22D.1 Write operation

To write a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

a) To Register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD;
b) To Register 14, write the desired address value to the MMD's address register;
c) To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the desired MMD;
d) To Register 14, write the content of the MMD's selected register.

Step a) and Step b) can be skipped if the MMD's address register was previously configured.

22D.2 Read operation

To read a Clause 45 register using the Clause 22 access mechanism, perform the following accesses using the appropriate PHY address for the PHY of interest:

a) To Register 13, write the Function field to 00 (address) and DEVAD field to the device address value for the desired MMD;
b) To Register 14, write the desired address value to the MMD's address register;
c) To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value for the desired MMD;
d) From Register 14, read the content of the MMD's selected register.

Step a) and Step b) can be skipped if the MMD's address register was previously configured.

22D.3 MMD address operations

22D.3.1 Address

While the Function field contains the value 00 (address):

a) subsequent writes to Register 14 continue to rewrite MMD DEVAD's address register;
b) subsequent reads from Register 14 continue to reread MMD DEVAD's address register.

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22D.3.2 Data, no post increment

While the Function field contains the value 01 (Data, no post increment):

a) subsequent writes to Register 14 continue to rewrite the data register selected by the value in MMD DEVAD's address register;
b) subsequent reads from Register 14 continue to reread the data register selected by the value in MMD DEVAD's address register.

22D.3.3 Data, post increment on reads and writes

While the Function field contains the value 10 (Data, post increment on reads and writes):

a) subsequent writes to Register 14 write the next higher addressed data register selected by the value in MMD DEVAD's address register, i.e. MMD DEVAD's address register is incremented after each access;
b) subsequent reads from Register 14 read the next higher addressed data register selected by the value in MMD DEVAD's address register, i.e. MMD DEVAD's address register is incremented after each access.

22D.3.4 Data, post increment on writes only

While the Function field contains the value 11 (Data, post increment on writes only):

a) subsequent writes to Register 14 write the next higher addressed data register selected by the value in MMD DEVAD's address register, i.e. MMD DEVAD's address register is incremented after each access;
b) subsequent reads from Register 14 continue to reread the data register selected by the value in MMD DEVAD's address register.

This Function enables a read-modify-write capability for successively addressed registers within a MMD.

22D.4 PHY Coexistence and bus conflict avoidance

There are multiple levels of coexistence on the MDIO bus:

a) PHYs accessible via the Clause 22 access mechanism can coexist on the same bus using different PHY address values;
b) Ports accessible via the Clause 45 access mechanism can coexist on the same bus using different port address values;
c) PHYs accessible via the Clause 22 access mechanism can coexist on the same bus with ports accessible via the Clause 45 access mechanism, even with identical PHY/port address values due to the different ST (start of frame) encodings of the frame structures (see 45A.3 and 45A.4, which discuss the need for protocol aware voltage translators for this type of coexistence);
d) MMDs accessible via the Clause 45 access mechanism with the same port address can coexist on the same bus using different device address values.

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Annex 23A

(normative)

6T codewords

The *leftmost* ternary symbol of each 6T Code group shown in Table 23A–1 (broken into 23A–1a and 23A–1b for pagination) shall be transmitted *first.* The *leftmost* nibble of each data octet is the *most significant.*

Table 23A–1a—100BASE-T4 8B6T code table

Data octet	6T code group	Data octet	6T code group	Data octet	6T code group	Data octet	6T code group
00	+ - 0 0 + -	20	0 0 - + + -	40	+ 0 + 0 0 -	60	0 - 0 + + 0
01	0 + - + - 0	21	- - + 0 0 +	41	+ + 0 0 - 0	61	0 0 - + 0 +
02	+ - 0 + - 0	22	+ + - 0 + -	42	+ 0 + 0 - 0	62	0 - 0 + 0 +
03	- 0 + + - 0	23	+ + - 0 - +	43	0 + + 0 - 0	63	- 0 0 + 0 +
04	- 0 + 0 + -	24	0 0 + 0 - +	44	0 + + 0 0 -	64	- 0 0 + + 0
05	0 + - - 0 +	25	0 0 + 0 + -	45	+ + 0 - 0 0	65	0 0 - 0 + +
06	+ - 0 - 0 +	26	0 0 - 0 0 +	46	+ 0 + - 0 0	66	0 - 0 0 + +
07	- 0 + - 0 +	27	- - + + + -	47	0 + + - 0 0	67	- 0 0 0 + +
08	- + 0 0 + -	28	- 0 - + + 0	48	0 0 0 + 0 0	68	- + - + + 0
09	0 - + + - 0	29	- - 0 + 0 +	49	0 0 0 - + +	69	- - + + 0 +
0A	- + 0 + - 0	2A	- 0 - + 0 +	4A	0 0 0 + - +	6A	- + - + 0 +
0B	+ 0 - + - 0	2B	0 - - + 0 +	4B	0 0 0 + + -	6B	+ - - + 0 +
0C	+ 0 - 0 + -	2C	0 - - + + 0	4C	0 0 0 - + 0	6C	+ - - + + 0
0D	0 - + - 0 +	2D	- - 0 0 + +	4D	0 0 0 - 0 +	6D	- - + 0 + +
0E	- + 0 - 0 +	2E	- 0 - 0 + +	4E	0 0 0 + - 0	6E	- + - 0 + +
0F	+ 0 - - 0 +	2F	0 - - 0 + +	4F	0 0 0 + 0 -	6F	+ - - 0 + +
10	+ 0 + - - 0	30	+ - 0 0 - +	50	+ 0 + - - +	70	- + + 0 0 0
11	+ + 0 - 0 -	31	0 + - - + 0	51	+ + 0 - + -	71	+ - + 0 0 0
12	+ 0 + - 0 -	32	+ - 0 - + 0	52	+ 0 + - + -	72	+ + - 0 0 0
13	0 + + - 0 -	33	- 0 + - + 0	53	0 + + - + -	73	0 0 + 0 0 0
14	0 + + - - 0	34	- 0 + 0 - +	54	0 + + - - +	74	- 0 + 0 0 0
15	+ + 0 0 - -	35	0 + - + 0 -	55	+ + 0 + - -	75	0 - + 0 0 0
16	+ 0 + 0 - -	36	+ - 0 + 0 -	56	+ 0 + + - -	76	+ 0 - 0 0 0
17	0 + + 0 - -	37	- 0 + + 0 -	57	0 + + + - -	77	0 + - 0 0 0
18	0 + - 0 + -	38	- + 0 0 - +	58	+ + + 0 - -	78	0 - - + + +
19	0 + - 0 - +	39	0 - + - + 0	59	+ + + - 0 -	79	- 0 - + + +
1A	0 + - + + -	3A	- + 0 - + 0	5A	+ + + - - 0	7A	- - 0 + + +
1B	0 + - 0 0 +	3B	+ 0 - - + 0	5B	+ + 0 - - 0	7B	- - 0 + + 0
1C	0 - + 0 0 +	3C	+ 0 - 0 - +	5C	+ + 0 - - +	7C	+ + - 0 0 -
1D	0 - + + + -	3D	0 - + + 0 -	5D	+ + 0 0 0 -	7D	0 0 + 0 0 -
1E	0 - + 0 - +	3E	- + 0 + 0 -	5E	- - + + + 0	7E	+ + - - - +
1F	0 - + 0 + -	3F	+ 0 - + 0 -	5F	0 0 - + + 0	7F	0 0 + - - +

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Table 23A–1b—100BASE-T4 8B6T code table

Data octet	6T code group	Data octet	6T code group	Data octet	6T code group	Data octet	6T code group
80	+ - + 0 0 -	A0	0 - 0 + + -	C0	+ - + 0 + -	E0	+ - 0 + + -
81	+ + - 0 - 0	A1	0 0 - + - +	C1	+ + - + - 0	E1	0 + - + - +
82	+ - + 0 - 0	A2	0 - 0 + - +	C2	+ - + + - 0	E2	+ - 0 + - +
83	- + + 0 - 0	A3	- 0 0 + - +	C3	- + + + - 0	E3	- 0 + + - +
84	- + + 0 0 -	A4	- 0 0 + + -	C4	- + + 0 + -	E4	- 0 + + + -
85	+ + - - 0 0	A5	0 0 - - + +	C5	+ + - - 0 +	E5	0 + - - + +
86	+ - + - 0 0	A6	0 - 0 - + +	C6	+ - + - 0 +	E6	+ - 0 - + +
87	- + + - 0 0	A7	- 0 0 - + +	C7	- + + - 0 +	E7	- 0 + - + +
88	0 + 0 0 0 -	A8	- + - + + -	C8	0 + 0 0 + -	E8	- + 0 + + -
89	0 0 + 0 - 0	A9	- - + + - +	C9	0 0 + + - 0	E9	0 - + + - +
8A	0 + 0 0 - 0	AA	- + - + - +	CA	0 + 0 + - 0	EA	- + 0 + - +
8B	+ 0 0 0 - 0	AB	+ - - + - +	CB	+ 0 0 + - 0	EB	+ 0 - + - +
8C	+ 0 0 0 0 -	AC	+ - - + + -	CC	+ 0 0 0 + -	EC	+ 0 - + + -
8D	0 0 + - 0 0	AD	- - + - + +	CD	0 0 + - 0 +	ED	0 - + - + +
8E	0 + 0 - 0 0	AE	- + - - + +	CE	0 + 0 - 0 +	EE	- + 0 - + +
8F	+ 0 0 - 0 0	AF	+ - - - + +	CF	+ 0 0 - 0 +	EF	+ 0 - - + +
90	+ - + - - +	B0	0 - 0 0 0 +	D0	+ - + 0 - +	F0	+ - 0 0 0 +
91	+ + - - + -	B1	0 0 - 0 + 0	D1	+ + - - + 0	F1	0 + - 0 + 0
92	+ - + - + -	B2	0 - 0 0 + 0	D2	+ - + - + 0	F2	+ - 0 0 + 0
93	- + + - + -	B3	- 0 0 0 + 0	D3	- + + - + 0	F3	- 0 + 0 + 0
94	- + + - - +	B4	- 0 0 0 0 +	D4	- + + 0 - +	F4	- 0 + 0 0 +
95	+ + - + - -	B5	0 0 - + 0 0	D5	+ + - + 0 -	F5	0 + - + 0 0
96	+ - + + - -	B6	0 - 0 + 0 0	D6	+ - + + 0 -	F6	+ - 0 + 0 0
97	- + + + - -	B7	- 0 0 + 0 0	D7	- + + + 0 -	F7	- 0 + + 0 0
98	0 + 0 - - +	B8	- + - 0 0 +	D8	0 + 0 0 - +	F8	- + 0 0 0 +
99	0 0 + - + -	B9	- - + 0 + 0	D9	0 0 + - + 0	F9	0 - + 0 + 0
9A	0 + 0 - + -	BA	- + - 0 + 0	DA	0 + 0 - + 0	FA	- + 0 0 + 0
9B	+ 0 0 - + -	BB	+ - - 0 + 0	DB	+ 0 0 - + 0	FB	+ 0 - 0 + 0
9C	+ 0 0 - - +	BC	+ - - 0 0 +	DC	+ 0 0 0 - +	FC	+ 0 - 0 0 +
9D	0 0 + + - -	BD	- - + + 0 0	DD	0 0 + + 0 -	FD	0 - + + 0 0
9E	0 + 0 + - -	BE	- + - + 0 0	DE	0 + 0 + 0 -	FE	- + 0 + 0 0
9F	+ 0 0 + - -	BF	+ - - + 0 0	DF	+ 0 0 + 0 -	FF	+ 0 - + 0 0

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Annex 23B

(informative)

Noise budget

Worst-case values for noise effects in the 100BASE-T4 system are as shown in Tables 23B–1 and 23B–2.

Table 23B–1—Carrier presence analysis

Received signal peak amplitude (min.)	792 mVp
NEXT noise	325 mVp

Table 23B–2—Far-end signal analysis

Received signal peak amplitude (min.)	796 mVp
Baseline wander	14 mVp
ISI	80 mVp
Reflections	60 mVp
FEXT noise	87 mVp

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Annex 23C

(informative)

Use of cabling systems with a nominal differential characteristic impedance of 120 Ω

The 100BASE-T4 standard specifies only the use of 100 Ω link segments for conformance. Since ISO/IEC 11801: 1995 also recognizes 120 Ω cabling, this informative annex specifies the conditions for using cabling systems with a nominal characteristic impedance of 120 Ω by 100BASE-T4 conformant stations.

The use of cables with a characteristic impedance outside the range specified in 23.6 will generally increase the mismatching effects in the link components, inducing additional noise in the received signals.

In particular, the use of a homogeneous link segment having a characteristic impedance of 120 Ω ±15 Ω over the frequency band 1 to 16 MHz may add up to 1.4% of additional noise to the signals at the input of the receivers (worst-case short-length link segment).

Therefore, in order to keep the overall noise (MDFEXT + reflections) at the same value as for a 100 Ω link segment when using a 120 Ω link segment, the minimum ELFEXT loss requirement for the cable must be increased by 2 dB (i.e., from 23 dB to 25 dB at 12.5 MHz, see 23.6.3.2). Accordingly, the MDFEXT noise requirement shall be decreased from 87 mV peak to 69 mV peak. In practice, this means that cables rated category 4 or higher, as specified in ISO/IEC 11801: 1995, are required when 120 Ω cables are used with 100BASE-T4 compliant PMDs.

NOTE 1—The use of 100 Ω cords at end points in conjunction with 120 Ω premises cabling may be tolerated provided that all the components of the link are of Category 5, as defined in ISO/IEC 11801: 1995.

NOTE 2—The use of 100 Ω cords at any intermediate cross-connect points on 120 Ω links as well as the use of 120 Ω cords in conjunction with 100 Ω premises cabling is not allowed since it would result in worst-case jitter greater than that allowed in this standard.

CAUTION

Users of this annex are further advised to check with the manufacturer of the particular 100BASE-T4 couplers they intend to use with a 120 Ω link to see whether those couplers can operate correctly on cables with Z_c as high as 120 Ω ± 15 Ω.

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Annex 27A

(normative)

Repeater delay consistency requirements

Proper operation of the network requires that repeaters do not cause the interpacket gap (IPG) to disappear by propagating the end of any carrier event to different output ports with greatly different delay times. Maximum port-to-port delays have been assigned as absolute delays to meet requirements for detection of collision within a slot time and limiting the length of collision fragments to less than minimum frame size. To avoid specification of minimum input-to-output propagation time as absolute values that reduce implementation flexibility, these delays are instead implied by imposing a triangular delay inequality relationship.

Consider three ports {A, B, C}. Using the notation SOP(xy) to mean the start-of-packet delay for an input at port x to resulting output on port y, repeaters shall achieve this relationship for all groups of three ports within a repeater set:

SOP(AC) < SOP(AB) + SOP(BC)

Following a frame transmitted by node A that propagates to nodes B and C, this constraint ensures that node B cannot complete an IPG timer and initiate a transmission that arrives at node C before node C has also advanced its own IPG timer sufficiently that a pending frame can contend for access to the network.

There is a second delay consistency requirement, one that relates to jam propagation by repeaters. Using a notation similar to that above, SOJ(xy) stands for the start-of-jam propagation delay from port x to port y and EOJ(xy) for the end-of-jam delay between same two ports.

To ensure proper detection of collisions and avoid generation of fragments that exceed minimum frame size, maximum values have been imposed on SOJ and EOJ delays through repeaters. No specific minima have been specified as all delays less than the maxima meet the collision detection and fragment length criteria. To prevent the jam pattern from shrinking excessively as it propagates through repeaters, repeaters shall meet this relationship between all pairs of ports:

EOJ(AB) >= SOJ(AB) – 4 bit times

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Annex 28A

(normative)

Selector Field definitions

The Selector Field, S[4:0] in the link codeword, shall be used to identify the type of message being sent by Auto-Negotiation. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Selector Field uses a 5-bit binary encoding, which allows 32 messages to be defined. All unspecified combinations are reserved. Reserved combinations shall not be transmitted.

Table 28A–1—Selector Field value mappings

S4	S3	S2	S1	S0	Selector description
0	0	0	0	0	Reserved for future Auto-Negotiation development
0	0	0	0	1	IEEE Std 802.3
0	0	0	1	0	IEEE Std 802.9a-1995 (withdrawn)
0	0	0	1	1	IEEE Std 802.5v-2001 (withdrawn)
0	0	1	0	0	IEEE Std 1394
0	0	1	0	1	INCITS
0	0	1	1	X	Reserved for future Auto-Negotiation development[a]
0	1	X	X	X	Reserved for future Auto-Negotiation development
1	X	X	X	X	Reserved for future Auto-Negotiation development

[a]For up-to-date information on the allocation of Auto-Negotiation Selector Fields see http://www.ieee802.org/3/selectors/selectors.html

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Annex 28B

(normative)

IEEE 802.3 Selector Base Page definition

This annex provides the Technology Ability Field bit assignments, Priority Resolution table, and Message Page transmission conventions relative to the IEEE 802.3 Selector Field value within the Base Page encoding.

As new IEEE 802.3 LAN technologies are developed, a reserved bit in the Technology Ability field may be assigned to each technology by the standards body.

The new technology will then be inserted into the Priority Resolution hierarchy and made a part of the Auto-Negotiation standard. The relative hierarchy of the existing technologies will not change, thus providing backward compatibility with existing Auto-Negotiation implementations.

It is important to note that the reserved bits are required to be transmitted as logic zeros. This guarantees that devices implemented using the current priority table will be forward compatible with future devices using an updated priority table.

28B.1 Selector field value

The value of the IEEE 802.3 Selector Field is S[4:0] = 00001.

28B.2 Technology Ability Field bit assignments

The Technology bit field consists of bits D5 through D11 (A0–A6, respectively) in the IEEE 802.3 Selector Base Page. Table 28B–1 summarizes the bit assignments.

Note that the order of the bits within the Technology Ability Field has no relationship to the relative priority of the technologies.

Setting Bit A5 or Bit A6 indicates that the DTE has implemented both the optional MAC control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium. The encoding of Bits A5 and A6 is specified in Table 28B–2.

Table 28B–1—Technology Ability Field bit assignments

Bit	Technology	Minimum cabling requirement
A0	10BASE-T	Two-pair Category 3
A1	10BASE-T full duplex	Two-pair Category 3
A2	100BASE-TX	Two-pair Category 5
A3	100BASE-TX full duplex	Two-pair Category 5
A4	100BASE-T4	Four-pair Category 3
A5	PAUSE operation for full duplex links	Not applicable
A6	Asymmetric PAUSE operation for full duplex Links	Not applicable

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Table 28B–2—Pause encoding

PAUSE (A5)	ASM_DIR (A6)	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. The ASM_DIR bit indicates that asymmetric PAUSE is supported. The value of the PAUSE bit when the ASM_DIR bit is set indicates the direction the PAUSE frames are supported for flow across the link. Asymmetric PAUSE configuration results in independent enabling of the PAUSE receive and PAUSE transmit functions as defined by Annex 31B. See 28B.3 regarding PAUSE configuration resolution.

28B.3 Priority resolution

Since two devices may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

a) 10GBASE-T full duplex
b) 1000BASE-T full duplex
c) 1000BASE-T
d) 100BASE-T2 full duplex
e) 100BASE-TX full duplex
f) 100BASE-T2
g) 100BASE-T4
h) 100BASE-TX
i) 10BASE-T full duplex
j) 10BASE-T

The rationale for this hierarchy is straightforward. 10BASE-T is the lowest common denominator and therefore has the lowest priority. Full duplex solutions are always higher in priority than their half duplex counterparts. 1000BASE-T has a higher priority than 100 Mb/s technologies. 100BASE-T2 is ahead of 100BASE-TX and 100BASE-T4 because 100BASE-T2 runs across a broader spectrum of copper cabling and can support a wider base of configurations. 100BASE-T4 is ahead of 100BASE-TX because 100BASE-T4 runs across a broader spectrum of copper cabling. The relative order of the technologies specified herein shall not be changed. As each new technology is added, it shall be inserted into its appropriate place in the list, shifting technologies of lesser priority lower in priority. If a vendor-specific technology is implemented, the priority of all IEEE 802.3 standard technologies shall be maintained, with the vendor specific technology inserted at any appropriate priority location.

NOTE—Refer to 28.2.1.2.3 for resolution of Extended Next Pages.

The use of the PAUSE operation for full duplex links (as indicated by bits A5 and A6) is orthogonal to the negotiated data rate, medium, or link technology. The setting of these bits indicates the availability of additional DTE capability when full duplex operation is in use. The PAUSE function shall be enabled according to Table 28B–3 only if the highest common denominator is a full duplex technology. There is no priority resolution associated with the PAUSE operation.

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Table 28B–3—Pause resolution

Local device		Link partner		Local device resolution	Link partner resolution
PAUSE	**ASM_DIR**	**PAUSE**	**ASM_DIR**		
0	0	Don’t care	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	0	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE transmit Disable PAUSE receive	Enable PAUSE receive Disable PAUSE transmit
1	0	0	Don’t care	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	Don’t care	1	Don’t care	Enable PAUSE Transmit and Receive	Enable PAUSE Transmit and Receive
1	1	0	0	Disable PAUSE Transmit and Receive	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE receive Disable PAUSE transmit	Enable PAUSE transmit Disable PAUSE receive

28B.4 Message Page transmission convention

Each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be used.

Next Page message codes should be allocated globally across Selector Field values so that meaningful communication is possible between technologies using different Selector Field values.

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Annex 28C

(normative)

Next Page Message Code field definitions

The Message Code Field of a message page used in Next Page exchange shall be used to identify the meaning of a message. The following table identifies the types of messages that may be sent. As new messages are developed, this table will be updated accordingly.

The Message Code Field uses an 11-bit binary encoding that allows 2048 messages to be defined. All message codes not specified shall be reserved for IEEE use or allocation. Devices that have negotiated Extended Next Page support transmit Extended Next Pages but not other Next Pages.

Extended Next Pages are used to transmit Extended Next Page message codes and the subsequent Extended Next Pages and extended Unformatted Pages. In addition, Extended Next Pages may be used to transmit multiple Message Pages and Unformatted Pages in the following manner. The Message Code Field is mapped to bits M0:10 of the extended Message Page, and the first two Unformatted Code Fields associated with the Message Code Field value are mapped to bits U0:U10 and U16:U26, respectively, of the extended Message Page. Additional Unformatted Code Fields would be mapped to bits U0:U42 of subsequent extended Unformatted Pages. Any unused bits in the Extended Next Pages are transmitted as zero and ignored by the receiver.

If more than two Unformatted Code fields are required by a message code, then additional Unformatted Code Fields are transmitted in the extended Unformatted Pages immediately following the extended Message Page. Up to three Unformatted Code Fields can be transmitted in each extended Unformatted Page, the first in bits U0:10, the second in bits U11:21, and the third in bits U27:37.

When a message code requires the transmission of one or more extended Unformatted Pages, due to the number of Unformatted Code Fields it defines, the Unformatted Code Fields in the extended Message and extended Unformatted Pages shall be in the order specified by the message code.

Table 28C–1—Message code field values

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
0	0	0	0	0	0	0	0	0	0	0	0	Reserved for future Auto-Negotiation use
1	0	0	0	0	0	0	0	0	0	0	1	Null Message
2	0	0	0	0	0	0	0	0	0	1	0	One UP with Technology Ability Field follows
3	0	0	0	0	0	0	0	0	0	1	1	Two UPs with Technology Ability Field follow
4	0	0	0	0	0	0	0	0	1	0	0	One UP with Binary coded Remote fault follows
5	0	0	0	0	0	0	0	0	1	0	1	Organizationally Unique Identifier Tagged Message
6	0	0	0	0	0	0	0	0	1	1	0	PHY Identifier Tag Code

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Table 28C–1—Message code field values *(continued)*

Message code	M 10	M 9	M 8	M 7	M 6	M 5	M 4	M 3	M 2	M 1	M 0	Message code description
7	0	0	0	0	0	0	0	0	1	1	1	100BASE-T2 Technology message code. 100BASE-T2 Ability Page to follow using Unformatted Next Page
8	0	0	0	0	0	0	0	1	0	0	0	1000BASE-T Technology message code. Two 1000BASE-T Ability Pages to follow using Unformatted Next Pages.
9	0	0	0	0	0	0	0	1	0	0	1	10GBASE-T/1000BASE-T Technology message code (Extended Next Page)
10	0	0	0	0	0	0	0	1	0	1	0	EEE Technology Message Code. EEE capability to follow using Unformatted Next Page.
11	0	0	0	0	0	0	0	1	0	1	1	Organizationally Unique Identifier Tagged Message (Extended Next Page)
12.....	0	0	0	0	0	0	0	1	1	0	0	Reserved for future Auto-Negotiation use
.....2047	1	1	1	1	1	1	1	1	1	1	1	Reserved for future Auto-Negotiation use

28C.1 Message code 0—Auto-Negotiation reserved code 1

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.2 Message code 1—Null Message code

The Null Message code shall be transmitted during Next Page exchange when the Local Device has no further messages to transmit and the Link Partner is still transmitting valid Next Pages. See 28.2.3.4 for more details.

28C.3 Message code 2—Technology Ability extension code 1

This message code is reserved for future expansion of the Technology Ability Field and indicates that a defined user code with a specific Technology Ability Field encoding follows.

28C.4 Message code 3—Technology Ability extension code 2

This message code is reserved for future expansion of the Technology Ability Field and indicates that two defined user codes with specific Technology Ability Field encodings follow.

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28C.5 Message code 4—Remote fault number code

This message code shall be followed by a single user code whose encoding specifies the type of fault that has occurred. The following user codes are defined:

0: RF Test
This code can be used to test Remote Fault operation.
1: Link Loss
2: Jabber
3: Parallel Detection Fault
This code may be sent to identify when bit 6.4 is set.

28C.6 Message code 5—Organizationally Unique Identifier (OUI) tag code

The OUI Tagged Message shall consist of a single message code of 0000 0000 0101 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the OUI or CID (bits 23:13) with the most significant bit in bit 10 of the user code. The second user code shall contain the next most significant 11 bits of the OUI or CID (bits 12:2) with the most significant bit in bit 10 of the user code. The third user code shall contain the remaining least significant 2 bits of the OUI or CID (bits 1:0) with the most significant bit in bit 10 of the user code. Bits 8:0 of the third user code contain a user-defined user code value that is specific to the OUI or CID transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the OUI or CID transmitted.

For example, assume that a manufacturer's IEEE-assigned OUI/CID value is AC-DE-48 and the manufacturer-selected user-defined user code associated with the OUI/CID is $1100\,1110\,0001\,1111\,1100_2$. The message code values generated from these two numbers is encoded into four message codes, as specified in Figure 28C–1. For clarity, the position of the global broadcast *g* is illustrated.

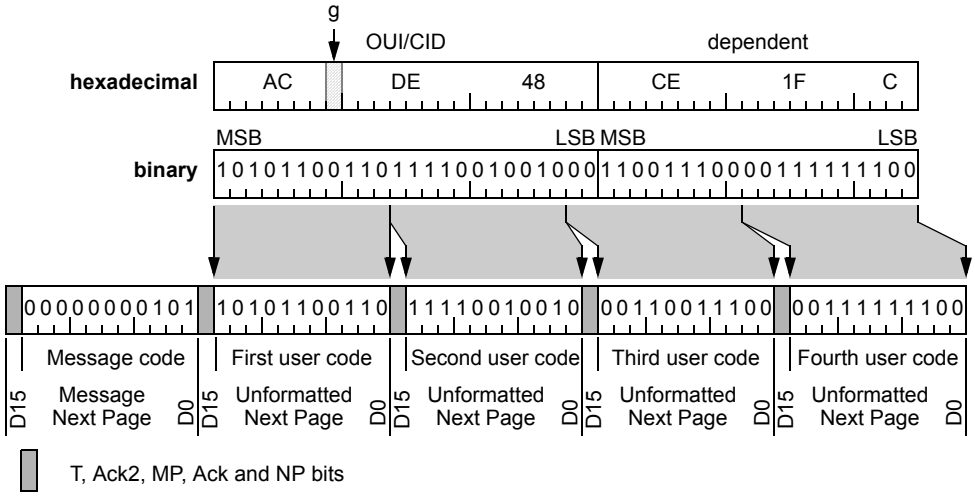


Figure 28C–1—Message code 5 sequence

NOTE—Figure 28C–1 shows the order Next Pages are transmitted, with the first transmitted Next Page shown in the leftmost position. While Figure 28–11 and Figure 28–12 use the convention that the most significant bit (i.e., the last bit to be transmitted) is the rightmost bit, Figure 28C–1 uses the opposite convention, i.e., the most significant bit of each page is shown in the leftmost position. This is a pictorial difference only; there is no difference in the actual order of bits transmitted.

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Devices that negotiate the use of Extended Next Page messages may use this message encapsulated within the Extended Next Page message as described in Annex 28C, however it is recommended that devices use message code 11 for Extended Next Page OUI tagged messages.

28C.7 Message code 6—PHY identifier tag code

The PHY ID tag code message shall consist of a single message code of 0000 0000 0110 followed by four user codes defined as follows. The first user code shall contain the most significant 11 bits of the PHY ID (2.15:5) with the most significant bit in bit 10 of the user code. The second user code shall contain bits 2.4:0 to 3.15:10 of the PHY ID with the most significant bit in bit 10 of the user code. The third user code shall contain bits 3.9:0 of the PHY ID with the most significant bit in bit 10 of the user code. Bit 0 in the third user code shall contain a user-defined user code value that is specific to the PHY ID transmitted. The fourth and final user code shall contain a user-defined user code value that is specific to the PHY ID transmitted.

28C.8 Message code 2047—Auto-Negotiation reserved code 2

This code is reserved for future Auto-Negotiation function enhancements. Devices shall not transmit this code.

28C.9 Message code 7—100BASE-T2 technology message code

Clause 32 (100BASE-T2) uses Next Page message code 7 to indicate that T2 implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two Unformatted Next Pages which contain information defined in 32.5.4.2.

28C.10 Message code 8—1000BASE-T technology message code

Clause 40 (1000BASE-T) uses Next Page message code 8 to indicate that 1000BASE-T implementations will follow the transmission of this page [the initial, Message (formatted) Next Page] with two Unformatted Next Pages that contain information defined in 40.5.1.2.

28C.11 Message code 9—10GBASE-T and 1000BASE-T technology message code

Clause 55 (10GBASE-T) uses Extended Next Page message code 9 to indicate that 10GBASE-T and 1000BASE-T abilities are contained within this Extended Next Page. The Next Page that contains this information is defined in 55.6.1. This page shall not be sent if Extended Next Page mode is disabled.

28C.12 Message code 10—EEE technology message code

Multiple clauses use Next Page message code 10 to indicate that EEE technology messages will follow the transmission of this page [the initial, Message (formatted) Next Page] with one Unformatted Next Page. The contents of the unformatted code field bits (U10:U0) shall be as defined in 45.2.7.13.

EEE capability negotiation is defined in 78.3.

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28C.13 Message code 11—Organizationally Unique Identifier Tagged Message (Extended Next Page)

Devices that negotiate the use of Extended Next Page messages may use the Extended Next Page OUI Tagged Message. This shall consist of a single message code of 000 0000 1011 and bits U23-U0 of the unformatted code field shall contain the OUI or CID (with most significant bit of the OUI or CID in U23, the second most significant bit in U22, etc.). Bits U31-U24 contain user-defined data. If the Next Page flag is set, the message page shall be followed by an unformatted Extended Next Page containing user-defined data.

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Annex 28D

(normative)

Description of extensions to Clause 28 and associated annexes

28D.1 Introduction

This annex is to be used to document extensions and modifications to Clause 28 required by IEEE 802.3 clauses and other standards that use Auto-Negotiation and that were approved after July 1995. It provides a single location to define such extensions and modifications without changing the basic contents of Clause 28.

Subclause 28D.2 lists those clauses and standards that require extensions to Clause 28 and provides pointers to the subclauses where those extensions are listed.

28D.2 Extensions to Clause 28

28D.2.1 Extensions required for Clause 31 (full duplex)

Clause 31 (full duplex) requires the use of Auto-Negotiation. Extensions to Clause 28 and associated annexes required for the correct operation of full duplex are shown in 28D.3.

28D.2.2 Extensions required for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) requires the use of Auto-Negotiation. Extensions to Clause 28 required for correct operation of 100BASE-T2 are shown in 28D.4.

28D.3 Extensions for Clause 31

Full duplex requires the use of bit A5 in the Technology Ability Field of the IEEE 802.3 Selector Base Page. (This bit is also defined as MII bit 4.10.) This bit was previously defined as “reserved for future technology.”

Bit	Technology	Minimum cabling requirement
A5	PAUSE operation for full duplex links	Not applicable

Bit A5 (PAUSE operation for full duplex links) signifies that the DTE has implemented both the optional MAC Control sublayer and the PAUSE function as specified in Clause 31 and Annex 31B. This capability is significant only when the link is configured for full duplex operation, regardless of data rate and medium.

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28D.4 Extensions for Clause 32 (100BASE-T2)

Clause 32 (100BASE-T2) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 32.5.

Auto-Negotiation is mandatory for 100BASE-T2 (32.1.3.4).

100BASE-T2 introduces the concept of MASTER and SLAVE to define DTEs and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER/SLAVE status (32.5.4.3).

100BASE-T2 uses unique Next Page transmit and receive registers (MII Registers 8, 9, and 10) in conjunctions with Auto-Negotiation. These registers are in addition to Registers 0–7 as defined in 28.2.4 (32.5.2).

100BASE-T2 use of Auto-Negotiation generates information which is stored in configuration and status bits defined for the MASTER-SLAVE Control register (MII Register 9) and the MASTER-SLAVE Status register (MII Register 10).

100BASE-T2 requires an ordered exchange of Next Page messages (32.5.1).

100BASE-T2 parameters are configured based on information provided by the ordered exchange of Next Page messages.

100BASE-T2 adds new message codes to be transmitted during Auto-Negotiation (32.5.4.2).

100BASE-T2 adds 100BASE-T2 full duplex and half duplex capabilities to the priority resolution table (28B.3) and MII Status Register (22.2.4.2).

T2 is defined as a valid value for “x” in 28.3.1 (e.g., link_status_T2). T2 represents that the 100BASE-T2 PMA is the signal source.

28D.5 Extensions required for Clause 40 (1000BASE-T)

Clause 40 (1000BASE-T) makes special use of Auto-Negotiation and requires additional MII registers. This use is summarized below. Details are provided in 40.5.

a) Auto-Negotiation is mandatory for 1000BASE-T (see 40.5.1).
b) 1000BASE-T requires an ordered exchange of Next Page messages (see 40.5.1.2), or optionally an exchange of an Extended Next Page message
c) 1000BASE-T parameters are configured based on information provided by the exchange of Next Page messages.
d) 1000BASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status (see 40.5.2).
e) 1000BASE-T transmits and receives Next Pages for exchange of information related to MASTER-SLAVE operation. The information is specified in MII registers 9 and 10 (see 32.5.2 and 40.5.1.1), which are required in addition to registers 0-8 as defined in 28.2.4.
f) 1000BASE-T adds new message codes to be transmitted during Auto-Negotiation (see 40.5.1.3).
g) 1000BASE-T adds 1000BASE-T full duplex and half duplex capabilities to the priority resolution table (see 28B.3) and MII Extended Status Register (see 22.2.2.4).
h) 1000BASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_1GigT.) 1GigT represents that the 1000BASE-T PMA is the signal source.

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i) 1000BASE-T supports Asymmetric Pause as defined in Annex 28B.

28D.6 Extensions required for Clause 55 (10GBASE-T)

Clause 55 (10GBASE-T) makes special use of Auto-Negotiation and requires additional MDIO registers. This use is summarized below. Details are provided in 55.6.

a) Auto-Negotiation is mandatory for 10GBASE-T.
b) Extended Next Page support is mandatory for 10GBASE-T.
c) 10GBASE-T requires an exchange of an Extended Next Page message.
d) 10GBASE-T parameters are configured based on information provided by the exchange of an Extended Next Page message.
e) 10GBASE-T uses MASTER and SLAVE to define PHY operations and to facilitate the timing of transmit and receive operations. Auto-Negotiation is used to provide information used to configure MASTER-SLAVE status.
f) 10GBASE-T transmits and receives an Extended Next Page for exchange of information related to MASTER-SLAVE operation. The information is specified in 45.2.7.
g) 10GBASE-T adds new message codes to be transmitted during Auto-Negotiation.
h) 10GBASE-T adds 10GBASE-T full duplex capabilities to the priority resolution table (see 28B.3).
i) 10GBASE-T is defined as a valid value for “x” in 28.3.1 (e.g., link_status_10GigT.) 10GigT represents that the 10GBASE-T PMA is the signal source.
j) 10GBASE-T supports Asymmetric Pause as defined in Annex 28B.

28D.7 Extensions required for Energy-Efficient Ethernet (Clause 78)

Energy-Efficient Ethernet (Clause 78) makes use of Auto-Negotiation and requires additional MDIO registers. Auto-negotiation is mandatory for all EEE PHYs that support LPI. Details are provided in 78.3.

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Annex 29A

(informative)

DTE and repeater delay components

29A.1 DTE delay

Round-trip DTE delay = MAC transmit start to MDI output
+ MDI input to MDI output (worst case, nondeferred)
+ MDI input to collision detect

NOTE 1—Refer to Clause 23, Clause 24, Clause 25, and Clause 26.

NOTE 2—Worst-case values are used for the one T4 and one TX/FX value shown in Table 29–3. (TX/FX values for MAC transmit start and MDI input to collision detect; T4 value for MDI input to MDI output.)

29A.2 Repeater delay

Repeater delay= SOP (start-of-packet propagation delay)
+ SOJ (start-of-jam propagation delay)

NOTE—Refer to Clause 27.

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Annex 29B

(informative)

Recommended topology documentation

It is strongly recommended that detailed records documenting the topology components of 100BASE-T networks be prepared and maintained to facilitate subsequent modification. Proper 100BASE-T topology design requires an accurate knowledge of link segment and hub parameters to ensure proper operation of single and multisegment, single collision domain networks. Link segment documentation is site-specific and requires careful documentation. It is recommended that the information shown in Table 29B–1 be collected for each link segment and archived for future reference. Hub performance parameters may be obtained from manufacturer documentation.

Table 29B–1—Recommended link segment documentation

	Horizontal wiring (wiring closet, from punch-down block to end station wall plate)	**MII cable(s)**	**Wiring closet patch cord**	**End station connecting cable**
Length				
Type (e.g., Category 3)				
Cable manufacturer				
Cable code/id (from manufacturer)				
Cable delay (in bit times per meter)				

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Annex 30A

(normative)

GDMO specification for IEEE 802.3 managed object classes

NOTE—The GDMO specification was moved to IEEE Std 802.3.1-2011.

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Annex 30B

(normative)

GDMO and ASN.1 definitions for management

NOTE—The GDMO specification was moved to IEEE Std 802.3.1-2011 Clause C.1 Common attributes template.

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Annex 30C

(normative)

SNMP MIB definitions for Link Aggregation

NOTE—The SNMP for Link Aggregation specification was moved to IEEE Std 802.1AX-2008.

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Annex 31A

(normative)

MAC Control opcode assignments

Table 31A–1 shows the currently defined opcode values and interpretations:

Table 31A–1—MAC Control opcodes

Opcode (Hexadecimal)	MAC Control function	Specified in	Value/Comment	Timestamp[a]
00-00	Reserved			
00-01	PAUSE	Annex 31B	Requests that the recipient stop transmitting non-control frames for a period of time indicated by the parameters of this function.	No
00-02	GATE	Clause 64, Clause 77	Request that the recipient allow transmission of frames at a time, and for a period of time indicated by the parameters of this function.	Yes
00-03	REPORT	Clause 64, Clause 77	Notify the recipient of pending transmission requests as indicated by the parameters of this function.	Yes
00-04	REGISTER_REQ	Clause 64, Clause 77	Request that the station be recognized by the protocol as participating in a gated transmission procedure as indicated by the parameters of this function.	Yes
00-05	REGISTER	Clause 64, Clause 77	Notify the recipient that the station is recognized by the protocol as participating in a gated transmission procedure as indicated by the parameters of this function.	Yes
00-06	REGISTER_ACK	Clause 64, Clause 77	Notify the recipient that the station acknowledges participation in a gated transmission procedure.	Yes
00-07 through 01-00	Reserved			
01-01	PFC	Annex 31D and IEEE Std 802.1Q	Requests that the recipient stop transmissions in the priorities indicated in the parameters of the function for a period of time also indicated in the parmeters.	No
01-02 through FF-FD	Reserved			
FF–FE	EXTENSION	Annex 31C	This frame is used for Organization–Specific Extension. Upon reception of this message, the MAC Control generates MA_CONTROL.Indication informing the MAC Control Client to perform the relevant action.	No
FF-FF	Reserved			

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[a]The timestamp field is generated by MAC Control and is not exposed through the client interface.

Opcodes are transmitted high-order octet first. Within each octet, bits are transmitted least-significant bit first. Reserved opcodes shall not be used by MAC Control sublayer entities.

Table 31A–2 through Table 31A–9 show the elements and semantics of the indication_operand_list for MA_CONTROL.indication primitives for each currently defined opcode value in Table 31A–1:

Table 31A–2—PAUSE MAC Control indications

PAUSE (opcode 0x0001)		
indication_operand_list element	**Value**	**Interpretation**
pause_status	paused	Indicates that the PAUSE function is inhibiting transmission of data frames by the MAC client.
	not_paused	Indicates that the PAUSE function is not inhibiting transmission of data frames by the MAC client.

Table 31A–3—GATE MAC Control indications

GATE (opcode 0x0002)		
indication_operand_list element	**Value**	**Interpretation**
start	32 bit	Time when transmission should be initiated.
length	16 bit	Interval of time during which transmission is allowed.
status	arrive	Indicates that a grant has been received for future activation.
	active	Indicates that the GATE function is allowing transmission of frames.
	deactive	Indicates that the GATE function is inhibiting transmission of frames.
force_report	true	The OLT expects the ONU to transmit a REPORT message during the transmission opportunity identified by start and length fields.
	false	The OLT does not request the ONU to transmit a REPORT message during the transmission opportunity identified by start and length fields.
discovery	true	This grant is reserved for use during discovery.
	false	This grant is not reserved for use by the discovery process, and is available for use by all traffic.
discoveryInformation[a]	16 bits	See Table 77–3 for the internal structure of the discoveryInformation field.

[a]Only present in 10G–EPON GATE MAC Control indication (Clause 77).

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Table 31A–4—REPORT MAC Control indications

REPORT (opcode 0x0003)		
indication_operand_list element	**Value**	**Interpretation**
RTT	32 bit	Indicates the calculated round trip time for the station, as calculated following the REPORT message reception.
n	Integer	Indicates the number of queue status reports present
report_list	valid[8]	Indicates whether the corresponding status element is present when set to true.
	status[8]	Indicates amount of data waiting in the corresponding queue including the associated transmission overhead.

Table 31A–5—REGISTER_REQ MAC Control indications

REGISTER_REQ (opcode 0x0004)		
indication_operand_list element	**Value**	**Interpretation**
status	incoming	Indicates that a station is requesting recognition.
	retry	Indicates that the station should reattempt registration.
flags	register	Indicates that the station is requesting to register.
	deregister	Indicates that the station is requesting to deregister.
pending_grants	Integer	Indicates the maximal number of future GATES that can be stored by the GATE function.
RTT	32 bit	Indicates the calculated round trip time for the station, as calculated following the REGISTER_REQ message reception.
laserOnTime[a]	8 bits	Indicates the Laser On Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.
laserOffTime[a]	8 bits	Indicates the Laser Off Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.
discoveryInformation[a]	16 bits	See Table 77–7 for the internal structure of the discoveryInformation field.

[a]Only present in 10G–EPON REGISTER_REQ MAC Control indication (Clause 77).

Table 31A–6—REGISTER MAC Control indications

REGISTER (opcode 0x0005)		
indication_operand_list element	**Value**	**Interpretation**
SA	48 bit	MAC address of OLT to which registration is being performed.
ID	16 bit	LLID assigned by the OLT for use by the ONU.

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Table 31A–6—REGISTER MAC Control indications *(continued)*

REGISTER (opcode 0x0005)		
indication_operand_list element	**Value**	**Interpretation**
status	accepted	Indicates that the requested registration is successful.
	denied	Indicates that the requested registration attempt is denied by the higher-layer-entity.
	deregistered	Indicates that the ONU has been deregistered, i.e., the associated LLID has been deallocated.
	reregistered	Indicates that the ONU is explicitly asked to re-register.
laserOnTime[a]	8 bits	Indicates the Laser On Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.
laserOffTime[a]	8 bits	Indicates the Laser Off Time characteristic for the given ONU transmitter, expressed in the units of time_quanta.

[a]Only present in 10G–EPON REGISTER MAC Control indication (Clause 77).

Table 31A–7—REGISTER_ACK MAC Control indications

REGISTER_ACK (opcode 0x0006)		
indication_operand_list element	**Value**	**Interpretation**
SA	48 bit	MAC address of ONU to which registration is being performed.
ID	16 bit	Indicates the LLID allocated to the ONU.
status	accepted	Indicates the station has been recognized as participating in gated transmission.
	denied	Indicates the station has been excluded from participating in gated transmission.
	reset	Indicates the station has been requested to resubmit a registration request.
	deregistered	Indicates that the station will no longer be participating in gated transmission.
RTT	32 bit	Indicates the calculated round trip time for the station, as calculated following the REGISTER_ACK message reception.

Table 31A–8—EXTENSION MAC Control indications

EXTENSION (opcode 0xFFFE)		
indication_operand_list element	**Value**	**Interpretation**
OUI	24 bits	Organizationally-Unique Identifier (OUI) or Company ID (CID) that determines the format and semantics of the Value field and its subfields, if any are defined.
Value	Variable	Organization-specific value, distinguished by the OUI or CID.

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Table 31A–9—PFC MAC Control indications

PFC (opcode 0x0101)		
indication_operand_list element	**Value**	**Interpretation**
priority_enable_vector	2 octets	The most significant octet is reserved (i.e., set to zero on transmission and ignored on receipt). Each bit of the least significant octet indicates if the corresponding field in the time_vector parameter is valid. The bits of the least significant octet are named e[0] (the least significant bit) to e[7] (the most significant bit). Bit e[n] refers to Priority n. For each e[n] bit set to one, the corresponding time[n] value is valid. For each e[n] bit set to zero, the corresponding time[n] value is invalid.
time_vector	a list of eight 2-octet unsigned integers	A list of eight 2-octet fields named time[0] to time[7]. The eight time[n] values are always present regardless of the value of the corresponding e[n] bit. Each time[n] field is a 2-octet, unsigned integer containing the length of time for which the receiving station is requested to inhibit transmission of data frames associated with Priority n. The field is transmitted most significant octet first, and least significant octet second. The time[n] fields are transmitted sequentially, with time[0] transmitted first and time[7] transmitted last. Each time[n] value is measured in units of pause_quanta, equal to the time required to transmit 512 bits of a frame at the data rate of the MAC. Each time[n] field can assume a value in the range of 0 to 65 535 pause_quanta.

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Annex 31B

(normative)

MAC Control PAUSE operation

31B.1 PAUSE description

The PAUSE operation is used to inhibit transmission of data frames for a specified period of time. A MAC Control client wishing to inhibit transmission of data frames from another station on the network generates a MA_CONTROL.request primitive specifying:

a) The globally assigned 48-bit multicast address 01-80-C2-00-00-01,
b) The PAUSE opcode,
c) A request_operand indicating the length of time for which it wishes to inhibit data frame transmission. (See 31B.2.)

The PAUSE operation cannot be used to inhibit transmission of MAC Control frames.

PAUSE frames shall only be sent by DTEs configured to the full duplex mode of operation.

The globally assigned 48-bit multicast address 01-80-C2-00-00-01 has been reserved for use in MAC Control PAUSE frames for inhibiting transmission of data frames from a DTE in a full duplex mode IEEE 802.3 LAN. IEEE 802.1D-conformant bridges will not forward frames sent to this multicast destination address, regardless of the state of the bridge's ports, or whether or not the bridge implements the MAC Control sublayer. To allow generic full duplex flow control, stations implementing the PAUSE operation shall instruct the MAC (e.g., through layer management) to enable reception of frames with destination address equal to this multicast address.

NOTE—By definition, an IEEE 802.3 LAN operating in full duplex mode comprises exactly two stations, thus there is no ambiguity regarding the destination DTE's identity. The use of a well-known multicast address relieves the MAC Control sublayer and its client from having to know, and maintain knowledge of, the individual 48-bit address of the other DTE in a full duplex environment.

When MAC Control PFC operation (see Annex 31D and IEEE Std 802.1Q) has been enabled, MAC Control PAUSE operation shall be disabled.

31B.2 Parameter semantics

The PAUSE opcode takes the following request_operand:

pause_time
: A 2-octet, unsigned integer containing the length of time for which the receiving station is requested to inhibit data frame transmission. The field is transmitted most-significant octet first, and least-significant octet second. The pause_time is measured in units of pause_quanta, equal to 512 bit times of the particular implementation (see 4.4). The range of possible pause_time is 0 to 65535 pause_quanta.

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31B.3 Detailed specification of PAUSE operation

The state machines in 31B.3 follow the conventions in 21.5. (See 25.1.1 for an example statement. That also covers the timer conventions from 14 which apply here.)

31B.3.1 Transmit operation

Upon receipt of a MA_CONTROL.request primitive containing the PAUSE opcode from a MAC client, the MAC Control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with the following parameters:

a) The destination_address is set equal to the destination_address parameter of the MA_CONTROL.request primitive. This parameter is currently restricted to the value specified in 31B.1.
b) The source_address is set equal to the 48-bit individual address of the station.
c) The length/type field (i.e., the first two octets) within the mac_service_data_unit parameter is set to the IEEE 802.3 MAC Control Ethertype value assigned in 31.4.1.3.
d) The remainder of the mac_service_data_unit is set equal to the concatenation of the PAUSE opcode encoding (see Annex 31A), the pause_time request_operand specified in the MA_CONTROL.request primitive, and a field containing zeros of the length specified in 31.4.1.6.
e) The frame_check_sequence is omitted.

Upon receipt of a data transmission request from the MAC client through the MCF:MA_DATA.request primitive, if the transmission of data frames has not been inhibited due to reception of a valid MAC Control frame specifying the PAUSE operation and a non-zero pause_time, the MAC Control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with its parameters identical to the MCF:MA_DATA.indication primitive.

31B.3.2 Transmit state diagram for PAUSE operation

It is not required that an implementation be able to transmit PAUSE frames. MAC Control sublayer entities that transmit PAUSE frames shall implement the Transmit state diagram specified in this subclause.

31B.3.2.1 Constants

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31B.1 (a).

802.3_MAC_Control
: The 16 bit Ethertype field assignment for 802.3 MAC Control specified in 31.4.1.3.

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

31B.3.2.2 Variables

transmitEnabled
: A Boolean set by network management to indicate that the station is permitted to transmit on the network.
: Values: true; Transmitter is enabled by management
false; Transmitter is disabled by management

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transmission_in_progress
: A Boolean used to indicate to the Receive state diagram that a MAC:MA_DATA.request service primitive call is pending.
  Values: true; transmission is in progress
  false; transmission is not in progress

n_quanta_tx
: An integer indicating the number of pause_quanta that the transmitter of a PAUSE frame is requesting that the receiver pause.

pause_timer_Done
: A Boolean set by the MAC Control PAUSE Operation Receive state diagram to indicate the expiration of a pause_timer initiated by reception of a MAC Control frame with a PAUSE opcode.
  Values: true; The pause_timer has expired.
  false; The pause_timer has not expired.

pause_mac_service_data_unit
: The concatenation of IEEE 802.3_MAC_Control, pause_command, n_quanta_tx, zeros.

31B.3.2.3 Functions

None

31B.3.2.4 Timers

pause_timer
: The timer governing the inhibition of transmission of data frames (see 31.5.1) from a MAC Client by the PAUSE function.

31B.3.2.5 Messages

MA_CONTROL.request
: The service primitive used by a client to request a MAC Control sublayer function with the specified request_operands.

MCF:MA_DATA.request
: The service primitive used by a client to request MAC data transmission with the specified parameters.

MAC:MA_DATA.request
: The service primitive issued by the MAC Control sublayer to transmit a MAC frame with the specified parameters. The action invoked is not considered to end until the transmission of the frame by the MAC has concluded and the ability of the MAC control layer to determine this is implementation dependent.

31B.3.2.6 Transmit state diagram for PAUSE operation

Figure 31B–1 depicts the Transmit state diagram for a MAC Control sublayer entity implementing the PAUSE operation.

31B.3.3 Receive operation

The opcode-independent MAC Control sublayer Receive state diagram accepts and parses valid frames received from the MAC sublayer. MAC Control sublayer entities that implement the PAUSE operation shall implement the Receive state diagram specified in this subclause. The functions specified in this subclause are performed upon receipt of a valid Control frame containing the PAUSE opcode, and define the function called by the INITIATE MAC CONTROL FUNCTION state of Figure 31–4. (See 31.5.3.)

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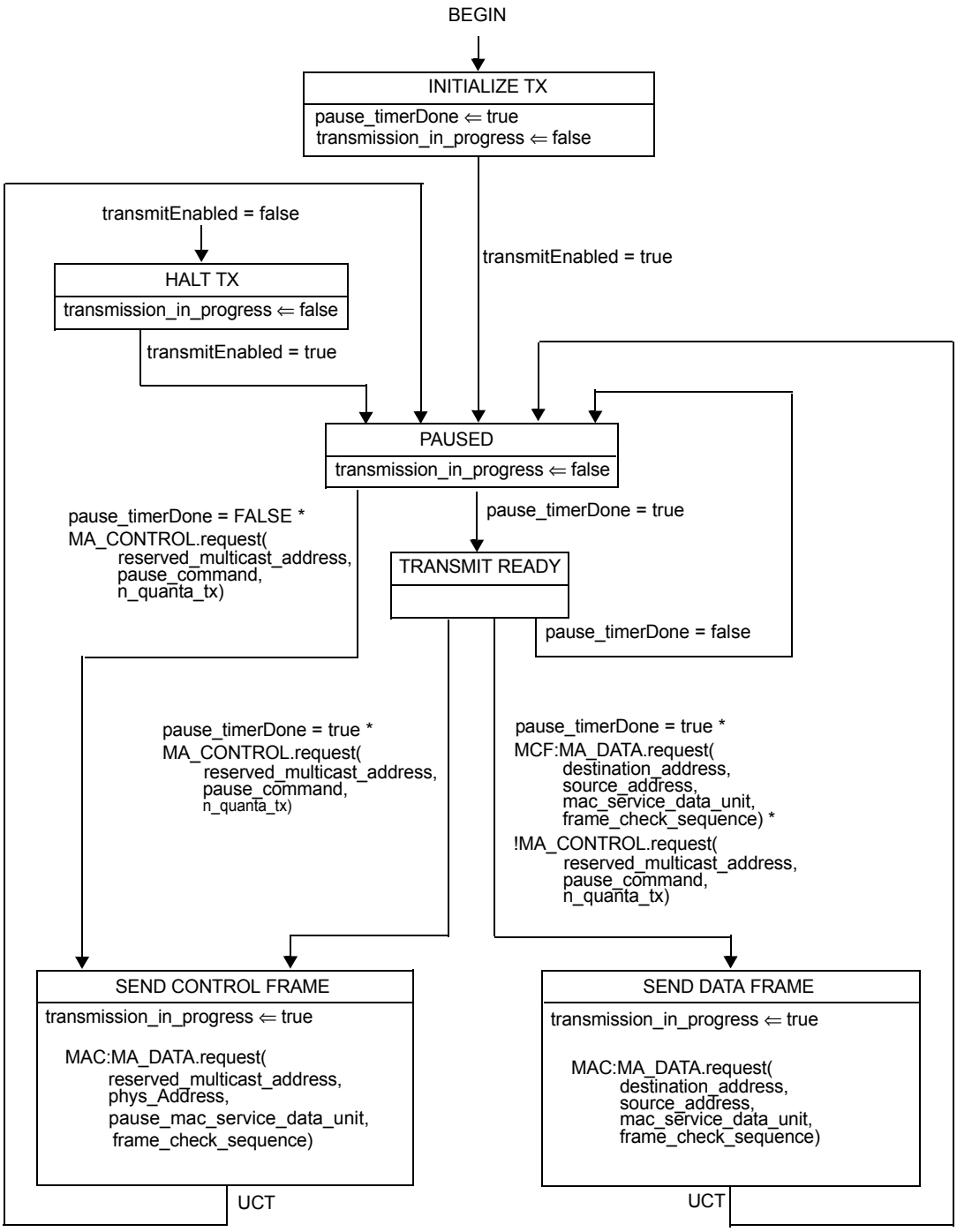


Figure 31B–1—PAUSE Operation Transmit state diagram

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Upon receipt of a valid MAC Control frame with the opcode indicating PAUSE and the destination address indicating either: (1) the reserved multicast address specified in 31B.1, or (2) the unique physical address associated with this station, the MAC Control sublayer starts a timer for the length of time specified by the pause_time request_operand in the Control frame (see 31B.2). The value of the variable pause_timer_Done is set to false upon the setting of the pause_timer to a non-zero value by the MAC Control PAUSE Operation Receive state diagram. The value of the variable pause_timer_Done is set to true when the timer value reaches zero (i.e., the timer expires). If the received PAUSE operation indicates a pause_timer value of zero, the value of pause_timer_Done is set to true immediately.

The receipt of a valid MAC Control frame with the opcode indicating PAUSE and the destination address indicating the reserved multicast address specified in 31B.1 or the unique physical address associated with this station will cause the pause_timer to be set according to the pause_time request_operand in the newly received frame, regardless of the current setting of the pause_timer, i.e., new PAUSE operations override earlier PAUSE operations.

31B.3.4 Receive state diagram for PAUSE operation

31B.3.4.1 Constants

pause_quantum
: The unit of measurement for pause time specified in 31B.2

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31B.1 (a).

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

31B.3.4.2 Variables

n_quanta_rx
: An integer used to extract the number of pause_quanta to set the pause_timer from the dataParam of the received MAC frame.

opcode
: The opcode parsed from the received MAC frame.

DA
: The destination address from the MAC:MA_DATA.indication service primitive.

data
: The data payload parsed from the received MAC frame.

transmission_in_progress
: A Boolean used by the Transmit state diagram to indicate that a MAC:MA_DATA.request service primitive call is pending.

  Values: true; transmission is in progress
  false; transmission is not in progress

31B.3.4.3 Timers

pause_timer
: The timer governing the inhibition of transmission of data frames.

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31B.3.4.4 Receive state diagram (INITIATE MAC CONTROL FUNCTION) for PAUSE operation

Figure 31B–2 depicts the INITIATE MAC CONTROL FUNCTION for the PAUSE operation. (See 31.5.3.)

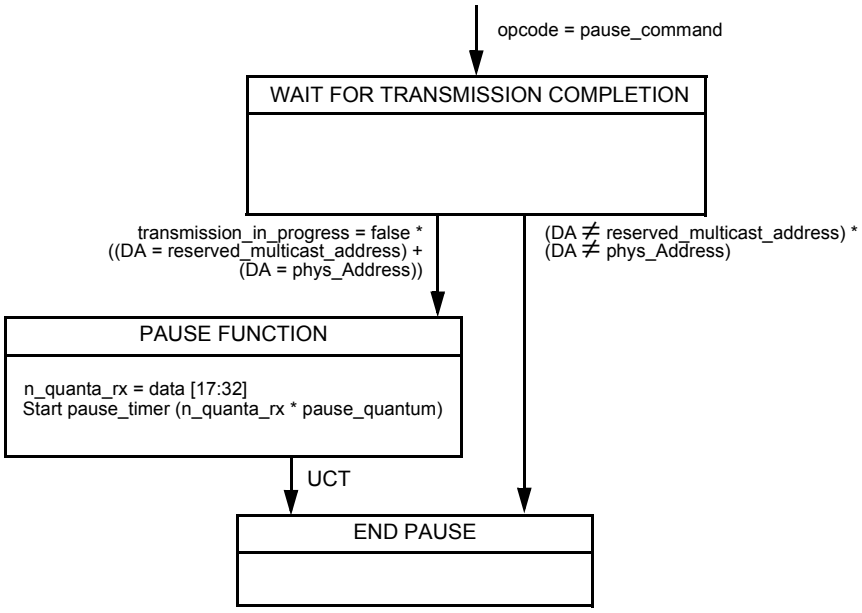


Figure 31B–2—PAUSE Operation Receive state diagram

31B.3.5 Status indication operation

MAC Control sublayer entities that implement the PAUSE operation shall implement the Indication state diagram specified in this subclause.

The PAUSE function sets the pause_status variable to one of two values: paused or not_paused, and indicates this to its client through the MA_CONTROL.indication primitive.

31B.3.6 Indication state diagram for pause operation

31B.3.6.1 Constants

pause_command
: The 2-octet encoding of the PAUSE command, as specified in Annex 31A.

31B.3.6.2 Variables

pause_status
: Used to indicate the state of the MAC Control sublayer for the PAUSE operation. It takes one of two values: paused or not_paused.

pause_timer_Done
: A Boolean set by the MAC Control PAUSE Operation Receive state diagram to indicate the expiration of a pause_timer initiated by reception of a MAC Control frame with a PAUSE opcode.

Values: true; The pause_timer has expired.
false; The pause_timer has not expired.

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31B.3.6.3 Messages

MA_CONTROL.indication

The service primitive used to indicate the state of the MAC Control sublayer to its client.

31B.3.6.4 Indication state diagram for PAUSE operation

Figure 31B–3 depicts the Indication State Diagram for a MAC Control sublayer implementing the PAUSE operation.

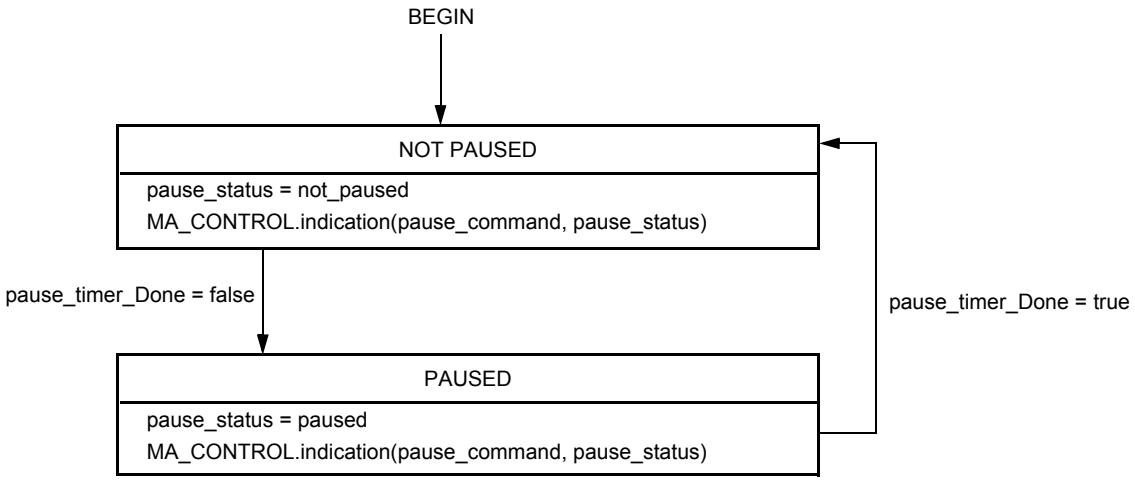


Figure 31B–3—PAUSE Operation Indication state diagram

31B.3.7 Timing considerations for PAUSE operation

In a full duplex mode DTE, it is possible to receive PAUSE frames asynchronously with respect to the transmission of MAC frames. For effective flow control, it is necessary to place an upper bound on the length of time that a DTE can transmit data frames after receiving a valid PAUSE frame with a non-zero pause_time request_operand.

Reception of a PAUSE frame shall not affect the transmission of a MAC frame that has been submitted by the MAC Control sublayer to the underlying MAC (i.e., the MAC:MA_DATA.request service primitive is synchronous, and is never interrupted).

At operating speeds of 100 Mb/s or less, a station that implements an exposed MII, shall not begin to transmit a (new) frame (assertion of TX_EN at the MII, see 22.2.2.3) more than one pause_quantum after the reception of a valid PAUSE frame (deassertion of RX_DV at the MII, see 22.2.2.7) that contains a nonzero value of pause_time. Stations that do not implement an exposed MII, shall measure this time at the MDI, with the timing specification increased to one pause_quantum + 64 BT.

At an operating speed of 1000 Mb/s, a station shall not begin to transmit a (new) frame more than two pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 10 Gb/s, a station with a 10GBASE-T PHY shall not begin to transmit a (new) frame more than 74 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI. A station using any other 10 Gb/s PHY shall not begin to transmit a (new) frame more than 60 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

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At operating speeds of 40 Gb/s, a station shall not begin to transmit a (new) frame more than 118 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 100 Gb/s, a station shall not begin to transmit a (new) frame more than 394 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

In addition to DTE and MAC Control delays, system designers should take into account the delay of the link segment when designing devices that implement the PAUSE operation.

The PAUSE response time may be verified by demonstrating that no more than max_overrun bytes of frame data are sent by the station after reception of a valid PAUSE frame that contains a non-zero value of pause_time. The value of max_overun is defined for the following operating speeds, where frame_length is the maximum frame length transmitted by the station during the test:

10 Gb/s (using 10GBASE-T) - max_overrun = 4736 + frame_length.

10 Gb/s (not using 10GBASE-T) - max_overrun = 3840 + frame_length.

40 Gb/s - max_overrun = 7552 + frame_length.

100 Gb/s - max_overrun = 25216 + frame_length.

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31B.4 Protocol implementation conformance statement (PICS) proforma for MAC Control PAUSE operation[22]

31B.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31B, MAC Control PAUSE operation, shall complete the following PICS proforma in addition to the PICS of Clause 31.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31B.4.2 Identification

31B.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31B.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Annex 31B, MAC Control PAUSE operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2015)	

Date of Statement	

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31B.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PST	Support for transmit of PAUSE frames	31B.3.2	N/A	O	Yes [ ] No [ ]
*MIIa	At operating speeds of 100 Mb/s or less, MII connection exists and is accessible for test.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIb	At operating speeds of 100 Mb/s or less, MII connection does not exist or is not accessible for test.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIc	At operating speeds of 1000 Mb/s	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIId	At operating speeds of 10 Gb/s with PHY types other than 10GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIe	At operating speeds of 10 Gb/s with PHY types of 10GBASE-T.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIf	At operating speeds of 40 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]
*MIIg	At operating speeds of 100 Gb/s.	31B.3.7	N/A	O	Yes [ ] No [ ]

31B.4.4 PAUSE command requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PCR1	Duplex mode of DTE	31B.1	Full duplex	M	Yes [ ]
PCR2	Reception of frames with destination address equal to the multicast address 01-80-C2-00-00-01	31B.1	Enabled	M	Yes [ ]
PCR3	PAUSE operation on PFC enable	31B.1	Disabled	PFC: M	Yes [ ]

31B.4.5 PAUSE command state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PSD1	Transmit state diagram for PAUSE operation	31B.3.2	Meets requirements of Figure 31B–1	PST: M	N/A [ ] M:Yes [ ]
PSD2	Receive state diagram for PAUSE operation	31B.3.4	Meets requirements of Figure 31B–2	M	Yes [ ]
PSD3	Indication state diagram for PAUSE operation	31B.3.6	Meets requirements of Figure 31B–3	M	Yes [ ]

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31B.4.6 PAUSE command MAC timing considerations

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	Effect of PAUSE frame on a frame already submitted to underlying MAC	31B.3.7	Has no effect	M	Yes [ ]
	Delay from receiving valid PAUSE command, with non-zero value for pause_time, to cessation of transmission	31B.3.7	Measured as described		
TIM2	Measurement point for station with MII		Delay at MII ≤ one pause_quantum	MIIa: M	N/A [ ] M: Yes [ ]
TIM3	Measurement point for station without MII at 100 Mb/s or less		Delay at MDI ≤ one pause_quantum + 64 BT	MIIb: M	N/A [ ] M: Yes [ ]
TIM4	Measurement point for station at 1000 Mb/s		Delay at MDI ≤ two pause_quanta	MIIc: M	N/A [ ] M: Yes [ ]
TIM5	Measurement point for station at 10 Gb/s with PHY types other than 10GBASE-T		Delay at MDI ≤ 60 pause_quanta	MIId: M	N/A [ ] M: Yes [ ]
TIM6	Measurement point for station at 10Gb/s with PHY type of 10GBASE-T		Delay at MDI ≤ 74 pause_quanta	MIIe: M	N/A [ ] M: Yes [ ]
TIM7	Measurement point for station at 40 Gb/s		Delay at MDI ≤ 118 pause_quanta	MIIf: M	N/A [ ] M: Yes [ ]
TIM8	Measurement point for station at 100 Gb/s		Delay at MDI ≤ 394 pause_quanta	MIIg: M	N/A [ ] M: Yes [ ]

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Annex 31C

(normative)

MAC Control organization specific extension operation

31C.1 Organization specific extension description

The extension operation is used to provide a standardized means for other organizations, to define their own MAC Control protocols outside the scope of this standard. The requirements defined in Clause 31 apply to these protocols.

31C.2 Transmission of Extension MAC Control frame

Upon receipt of a MA_CONTROL.request primitive containing the EXTENSION opcode from a MAC client, the MAC control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with the following parameters:

a) The destination_address is set equal to the destination_address parameter of the MA_CONTROL.request primitive. This parameter is currently restricted to either the value 01–80–C2–00–00–01 or to the 48 bit individual address of the destination station.
b) The source_address is set equal to the 48 bit individual address of the station.
c) The length/type field (i.e., the first two octets) within the mac_service_data_unit parameter is set to the IEEE 802.3 MAC Control Ethertype value assigned in 31.4.1.3.
d) The remainder of the mac_service_data_unit is set to the concatenation of the Extension Opcode, Organizationally Unique Identifier (OUI) or Company ID (CID)[23] assigned to the organization by the IEEE, and the organization-specific data.
e) The frame_check_sequence is omitted.

MAC Control sublayer entities that transmit or receive EXTENSION frames shall pass them through without additional processing.

31C.3 Receive operation

The opcode–independent MAC Control sublayer Receive state diagram accepts and parses valid frames received from the MAC sublayer. MAC Control sublayer entities that implement the EXTENSION operation shall implement the Receive state diagram specified in this subclause. The functions specified in this subclause are performed upon receipt of a valid Control frame containing the EXTENSION opcode and define the function called by the INITIATE MAC CONTROL FUNCTION state of Figure 31–4 (see 31.5.3).

[23]Details defining the format of OUIs and CIDs can be found in IEEE Std 802-2014. Interested applicants should contact the IEEE Standards Department, Institute of Electrical and Electronics Engineers, http://standards.ieee.org/develop/regauth/, 445 Hoes Lane, Piscataway, NJ 08854, USA.

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31C.3.1 Receive state diagram (INITIATE MAC CONTROL FUNCTION) for EXTENSION operation

Figure 31C–2 depicts the INITIATE MAC CONTROL FUNCTION for the EXTENSION operation (see 31.5.3). Upon reception of EXTENSION frames, the frame is sent to the MAC CONTROL client.

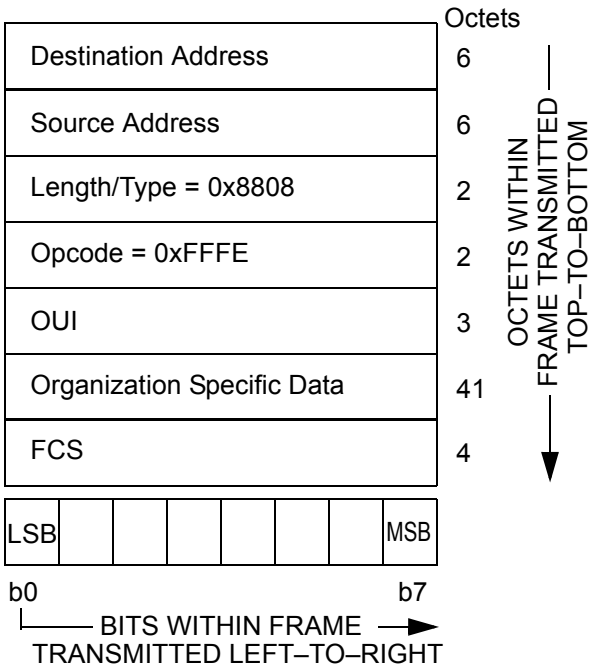


Figure 31C–1—MAC Control EXTENSION Frame

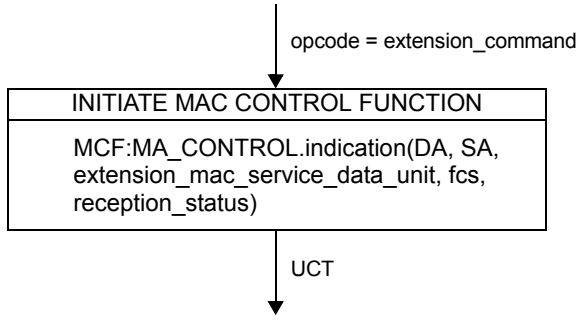


Figure 31C–2—EXTENSION receive function

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31C.4 Protocol implementation conformance statement (PICS) proforma for MAC Control organization specific extension operation[24]

31C.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31A, MAC Control organization specific extension operation, shall complete the following PICS proforma in addition to the PICS of Clause 31.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31C.4.2 Identification

31C.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31C.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Annex 31A, MAC Control organization specific extension operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2015)	

Date of Statement	

31C.4.3 EXTENSION command state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
ESD1	Receive state diagram for EXTENSION operation	31C.3	Meets requirements of Figure 31C–2	M	Yes [ ]

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Annex 31D

(normative)

MAC Control PFC operation

31D.1 PFC description

The Priority-based Flow Control (PFC) operation is used to inhibit transmission of data frames on one or more priorities for a specified period of time. The behavior of a MAC Control client supporting PFC operation is specified in IEEE Std 802.1Q. A MAC Control client wishing to inhibit transmission of data frames from the link partner generates a MA_CONTROL.request primitive specifying:

a) The globally assigned 48-bit multicast address 01-80-C2-00-00-01,
b) The PFC opcode,
c) A request_operand list with two operands: priority_enable_vector and time_vector. (See 31D.2)

Unlike the MAC Control PAUSE operation, the inhibition of frames for the PFC operation occurs in the MAC Control client. Upon receiving a PFC frame, the only action in MAC Control is to generate a MA_CONTROL.indication primitive with the indication_operand list specified in Table 31A–9.

The PFC operation does not inhibit transmission of MAC Control frames.

PFC operation shall not be enabled on DTEs configured to the half-duplex mode of operation. PFC is intended for use over full-duplex point-to-point links. Use on shared media such as EPON is out of the scope of this standard.

The globally assigned 48-bit multicast address 01-80-C2-00-00-01 has been reserved for use in MAC Control frames. Bridges conformant to IEEE Std 802.1D or IEEE Std 802.1Q will not forward frames sent to this multicast destination address, regardless of the state of the bridge's ports, and whether or not the bridge implements the MAC Control sublayer. To allow PFC full duplex flow control, stations implementing the PFC operation shall instruct the MAC (e.g., through layer management) to enable reception of frames with destination address equal to this multicast address.

NOTE—By definition, an IEEE 802.3 LAN operating in full duplex mode comprises exactly two stations, thus there is no ambiguity regarding the destination DTE's identity. The use of a well-known multicast address relieves the MAC Control sublayer and its client from having to know, and maintain knowledge of, the individual 48-bit address of the other DTE in a full duplex environment.

31D.2 Parameter semantics

The PFC opcode takes the following request_operand_list:

priority_enable_vector:

A 2-octet vector. The most significant octet is reserved (i.e., set to zero on transmission and ignored on receipt). Each bit of the least significant octet indicates if the corresponding field in the time_vector parameter is valid. The bits of the least significant octet are named e[0] (the least significant bit) to e[7] (the most significant bit). Bit e[n] refers to Priority n. For each e[n] bit set to one, the corresponding time[n] value is valid. For each e[n] bit set to zero, the corresponding time[n] value is invalid.

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time_vector:

A list of eight 2-octet fields named time[0] to time[7]. The eight time[n] values are always present regardless of the value of the corresponding e[n] bit. Each time[n] field is a 2-octet, unsigned integer containing the length of time for which the receiving station is requested to inhibit transmission of data frames associated with Priority n. The field is transmitted most significant octet first, and least significant octet second. The time[n] fields are transmitted sequentially, with time[0] transmitted first and time[7] transmitted last. Each time[n] value is measured in units of pause_quanta, equal to the time required to transmit 512 bits of a frame at the data rate of the MAC. Each time[n] field can assume a value in the range of 0 to 65 535 pause_quanta.

31D.3 PFC transmit

The state machines in 31D.3 follow the conventions in 21.5. (See 25.1.1 for an example statement. That also covers the timer conventions from 14 which apply here.)

Upon receipt of a MA_CONTROL.request primitive containing the PFC opcode from a MAC client, the MAC Control sublayer calls the MAC sublayer MAC:MA_DATA.request service primitive with the following parameters:

a) The destination_address is set equal to the destination_address parameter of the MA_CONTROL.request primitive. This parameter is currently restricted to the value specified in 31D.1.
b) The source_address is set equal to the 48-bit individual address of the station.
c) The length/type field (i.e., the first two octets) within the mac_service_data_unit parameter is set to the IEEE 802.3 MAC Control Ethertype value assigned in 31.4.1.3.
d) The remainder of the mac_service_data_unit is set equal to the concatenation of the PFC opcode encoding (see Annex 31A), the priority_enable_vector and the time_vector specified in the MA_CONTROL.request primitive, and a field containing zeros of the length specified in 31.4.1.6.
e) The frame_check_sequence is omitted.

Figure 31D–1 depicts the MAC Control PFC Frame transmitted in response to an MA_Control.request primitive with the PFC opcode.

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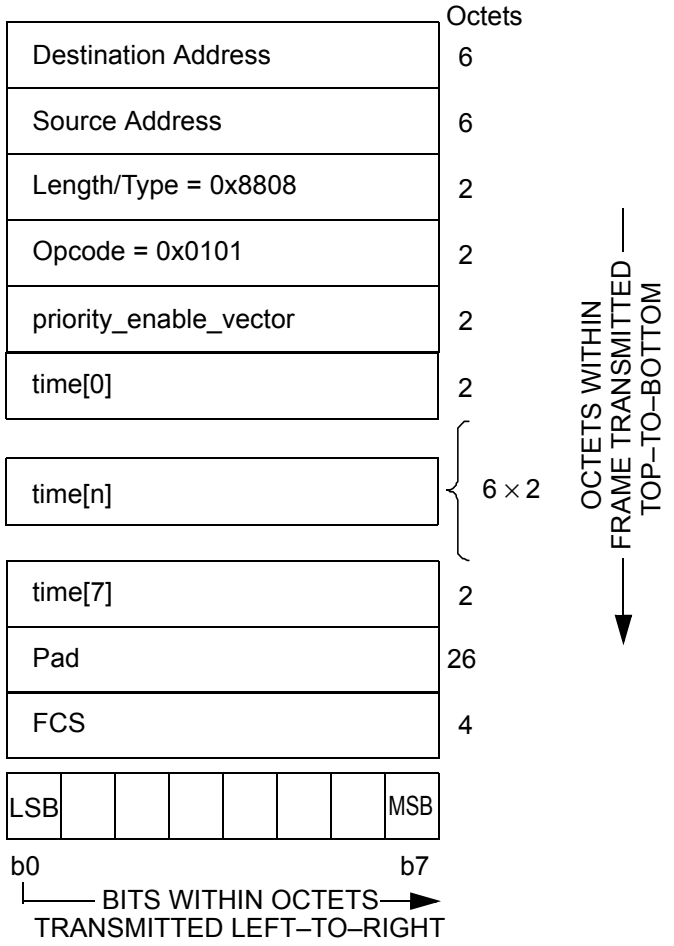


Figure 31D–1—MAC Control EXTENSION Frame

31D.4 Transmit state diagram for PFC operation

MAC Control sublayer entities that transmit PFC frames shall implement the Transmit state diagram specified in this subclause.

31D.4.1 Constants

pfc_command
: The 2-octet encoding of the PFC opcode, as specified in Annex 31A.

phys_Address
: A 48-bit value, equal to the unicast address of the station implementing the MAC Control sublayer.

reserved_multicast_address
: The 48-bit address specified in 31D.1 (a).

802.3_MAC_Control
: The 16 bit Ethertype field assignment for 802.3 MAC Control specified in 31.4.1.3.

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31D.4.2 Variables

transmitEnabled
: A Boolean set by network management to indicate that the station is permitted to transmit on the network.
Values: true; Transmitter is enabled by management
false; Transmitter is disabled by management

pfc_operand_list
: The priority_enable_vector and time_vector from the MA_CONTROL.request.

pfc_mac_service_data_unit
: The concatenation of IEEE 802.3_MAC_Control, pfc_command, priority_enable_vector, time_vector, zeros.

31D.4.3 Messages

MA_CONTROL.request
: The service primitive used by a client to request a MAC Control sublayer function with the specified request_operands.

MCF:MA_DATA.request
: The service primitive used by a client to request MAC data transmission with the specified parameters.

MAC:MA_DATA.request
: The service primitive issued by the MAC Control sublayer to transmit a MAC frame with the specified parameters. The action invoked is not considered to end until the transmission of the frame by the MAC has concluded and the ability of the MAC control layer to determine this is implementation dependent.

31D.4.4 Transmit state diagram for PFC operation

Figure 31B–1 depicts the Transmit state diagram for a MAC Control sublayer entity implementing the PFC operation.

31D.5 PFC receive

The opcode-independent MAC Control sublayer Receive state diagram accepts and parses valid frames received from the MAC sublayer. The functions specified in this subclause are performed upon receipt of a valid Control frame containing the PFC opcode, and define the function called by the INITIATE MAC CONTROL FUNCTION state of Figure 31–4. (See 31.5.3.) Upon receipt of a valid MAC Control frame with the opcode indicating PFC and the destination address indicating the reserved multicast address specified in 31D.1, the MAC Control sublayer generates the MA_CONTROL.indication to the MAC Control Client.

31D.6 Receive state diagram for PFC operation

MAC Control sublayer entities that transmit PFC frames shall implement the Receive state diagram specified in this subclause.

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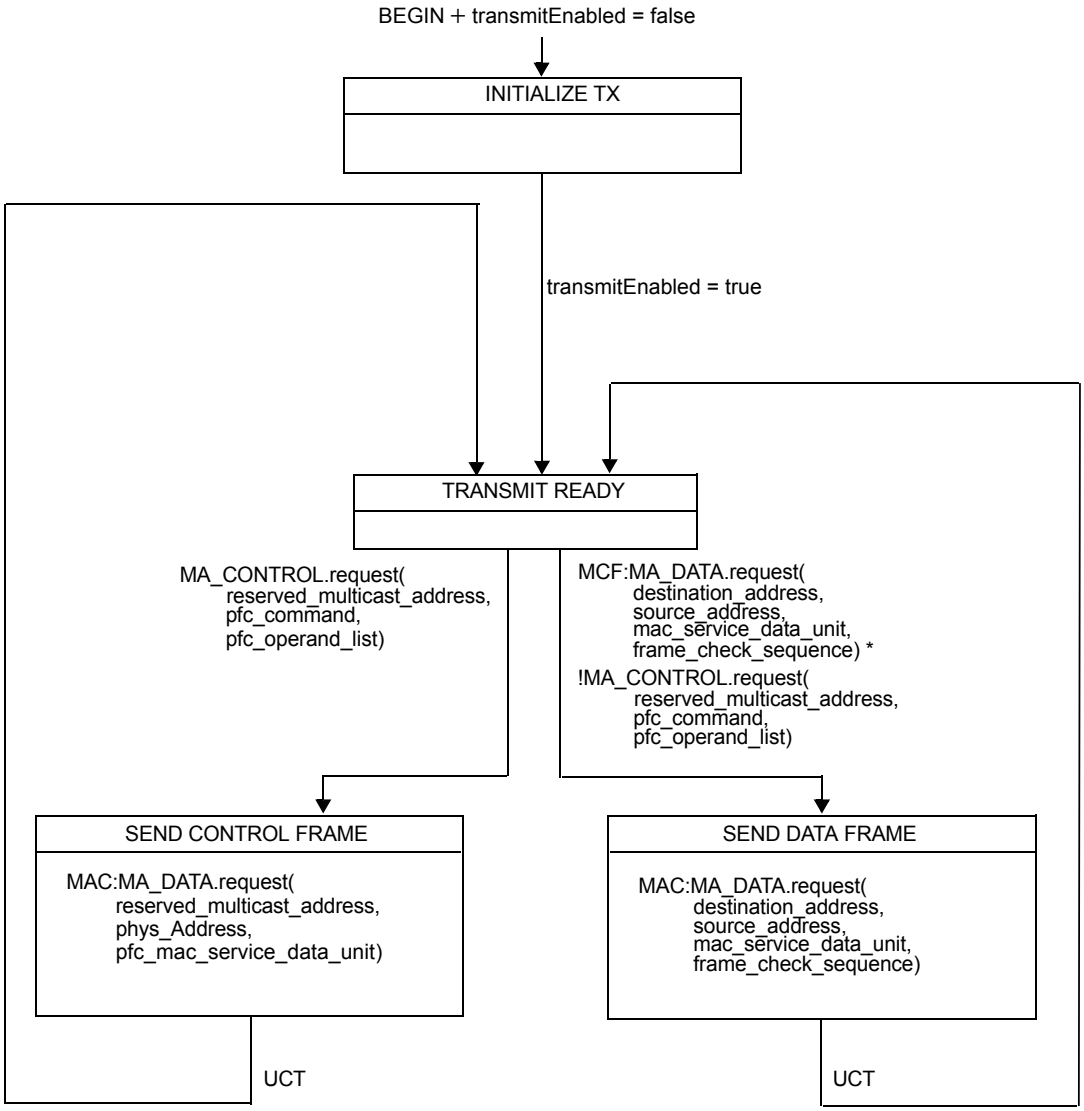


Figure 31D–2—PFC Operation Transmit state diagram

31D.6.1 Constants

pfc_command
: The 2-octet encoding of the PFC opcode, as specified in Annex 31A.

reserved_multicast_address
: The 48-bit address specified in 31D.1 (a).

31D.6.2 Variables

opcode
: The opcode parsed from the received MAC frame.

DA
: The destination address from the MAC:MA_DATA.indication service primitive.

pfc_operand_list
: The priority_enable_vector and time_vector parsed from the received frame.

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31D.6.3 Receive state diagram (INITIATE MAC CONTROL FUNCTION) for PFC operation

Figure 31B–2 depicts the INITIATE MAC CONTROL FUNCTION for the PFC operation. (See 31.5.3.)

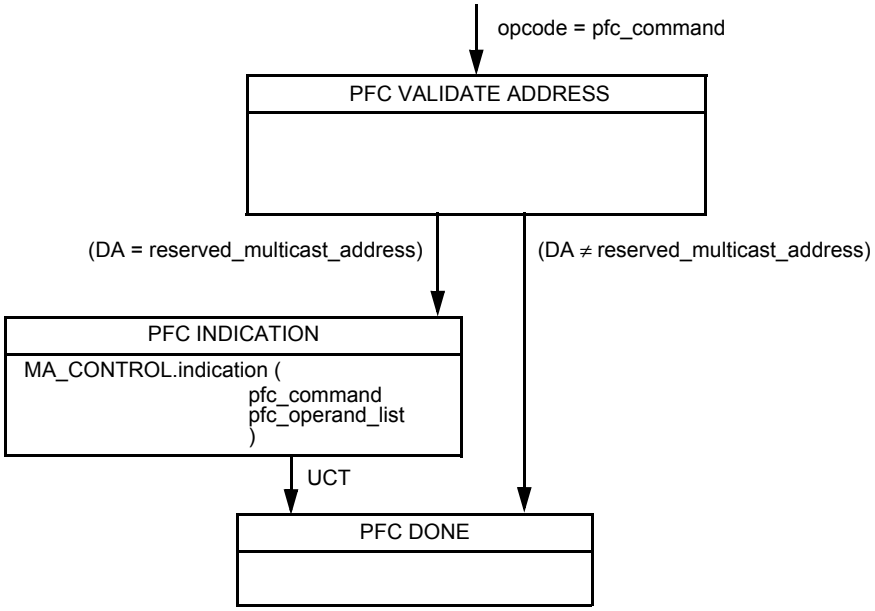


Figure 31D–3—PFC Operation Receive state diagram

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31D.7 Protocol implementation conformance statement (PICS) proforma for MAC Control PFC operation[25]

31D.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31D, MAC Control PFC operation, shall complete the following PICS proforma in addition to the PICS of Clause 31.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

31D.7.2 Identification

31D.7.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

31D.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-2015, Annex 31D, MAC Control PFC operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; The answer Yes means that the implementation does not conform to IEEE Std 802.3-2015)	

Date of Statement	

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31D.7.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
PFC	Support for transmit and reception of PFC frames	31D.3 and 31D.5	N/A	M	Yes [ ]

31D.7.4 PFC command requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PFC1	Duplex mode of DTE	31D.1	Full duplex	M	Yes [ ]
PFC2	Reception of frames with destination address equal to the multicast address 01-80-C2-00-00-01	31D.1	Enabled	M	Yes [ ]

31D.7.5 PFC command state diagram requirements

Item	Feature	Subclause	Value/Comment	Status	Support
PSDT	Transmit state diagram for PFC operation	31D.4	Meets requirements of Figure 31D–2	M	Yes [ ]
PSDR	Receive state diagram for PFC operation	31D.6	Meets requirements of Figure 31D–3	M	Yes [ ]

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Annex 32A

(informative)

Use of cabling systems with nominal differential characteristic impedance of 120 Ω or 150 Ω

The 100BASE-T2 standard specifies only the use of 100 Ω link segments for conformance. Since ISO/IEC 11801: 1995 also recognizes 120 Ω and 150 Ω cabling, this informative annex specifies the conditions for using cabling systems with nominal characteristic impedances of 120 Ω and 150 Ω by 100BASE-T2 conformant stations.

The use of cabling with a characteristic impedance outside the range specified in 32.7.2.2 will generally increase the mismatching effects in the link components if directly coupled to the PHY without a impedance transforming balun and results in the following consequences:

a) Increased echo due primarily to poorer hybrid performance
b) Increased cabling attenuation roughness due to increased reflections
c) Increased transmitter launch amplitude
d) Possible non-linearities in transmitter

The effect of increased echo and reflection is more than compensated by use of Category 4 or higher 120 Ω cabling or 150 Ω cabling consistent with ISO/IEC 11801 specifications. The increased transmitter launch level will not be an additional noise or EMC problem on these quality cabling. Manufacturers intending to support a direct connection of 120 Ω or 150 Ω cabling to the 100BASE-T2 PHY must ensure that the transmitters can tolerate the impedance without additional non-linearity.

If baluns are used instead of a direct connection, care must be taken to ensure that the corner frequencies of the baluns do not substantially interfere with the 100BASE-T2 signals. In practice, a lower corner frequency less than 100 kHz and an upper corner frequency greater than 30 MHz should be adequate for use with Category 4 or higher 120 Ω cabling or 150 Ω cabling consistent with ISO/IEC 11801 specifications.

CAUTION

Users of the present annex are further advised to check with the manufacturer of the particular 100BASE-T2 devices they intend to use with a 120 Ω or 150 Ω link whether those devices can operate correctly on cabling with Zc as high as 120 Ω ± 15 Ω and 150 Ω ± 15 Ω.

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Annex 33A

(informative)

PSE-PD stability

33A.1 Recommended PSE design guidelines and test setup

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (Zo_port), the cable impedance (Zc), the PD input port circuitry impedance (Zpd_cir) and the PD EMI output filter impedance (Z_emi) should be lower than the PD power supply input impedance (Zin_ps_pd). This subclause focuses on the PSE part.

Port output impedance consists of two parts:

a) PSE power supply output impedance (Zo_ps), which is a function of the load (P_{Port}), and
b) Series elements (Z_ser) that connect the PSE power supply output to the port.

Therefore, the total Port output impedance during normal powering mode is Zo_port=Zo_ps+Z_ser.

In order to maintain PSE-PD stability, the following guidelines apply:

c) Zo_ps max = 0.3 Ω at frequencies up to 100 kHz at $P_{port} = P_{Type}$ as defined in Table 33–11.
   Zo_ps can be extracted from Z_{port} by measuring V_{Port} / I_{Port} (with an external power dynamic analyzer system) as a function of frequency and subtracting from Z_{port} the value of Zser (f = DC) which is limited by the value of Zser at DC (low frequency).
d) If Zo_ps < Zo_ser and V_{Port} is kept to V_{Port} min and V_{Port} max as defined in Table 33–11 during dynamic load changes from 10 Hz to 100 kHz, then the value of Zo_ps is not limited.

Compliance to the above requirements should be made by measuring the port output impedance from 10 Hz to 100 kHz with a load of P_{Type} as defined in Table 33–11 at short cable length, or by presenting simulation results.

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See Figure 1 for the PSE-PD system impedance allocation.

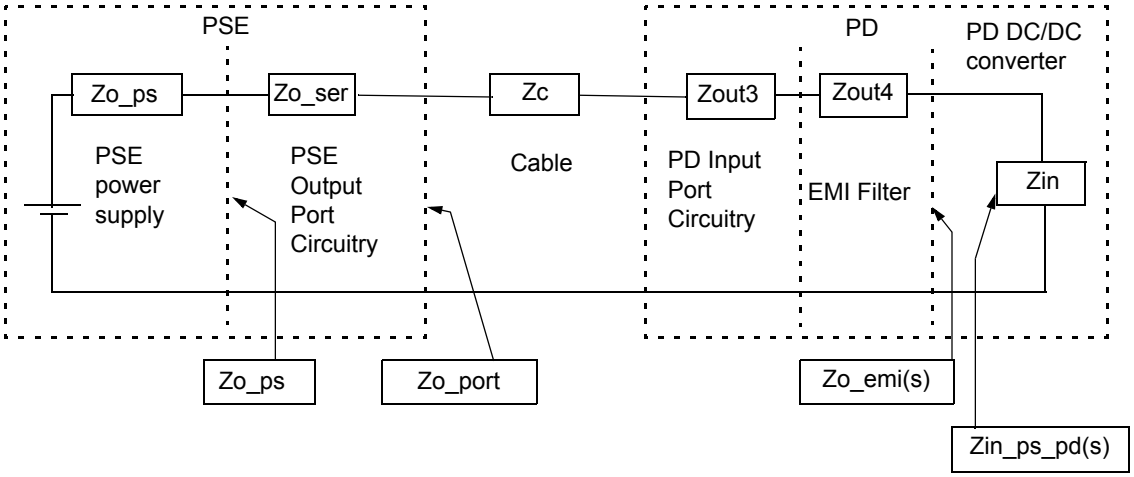


Figure 33A–1—PSE-PD system impedance allocation

See Figure 33A–2 for the test setup and Figure 33A–3 for the test requirements.

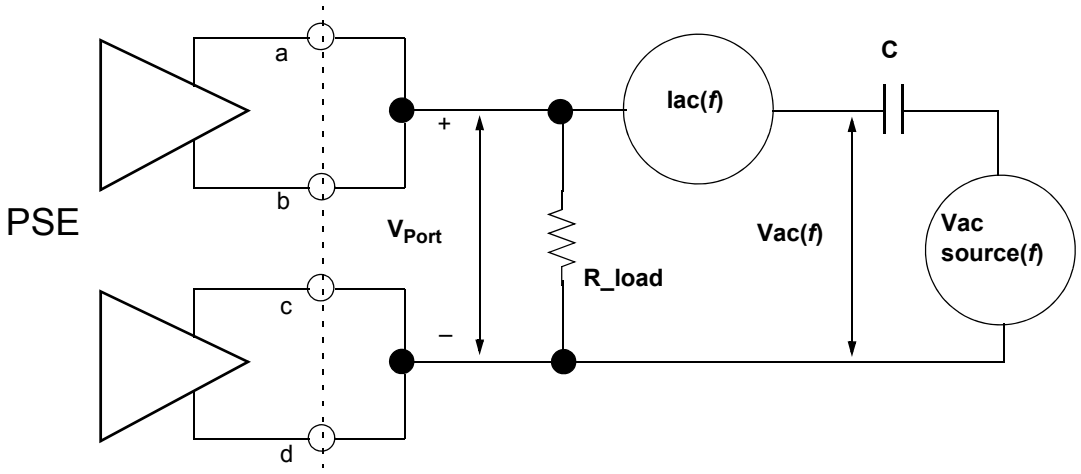


Figure 33A–2—Test setup for measuring Zo_port

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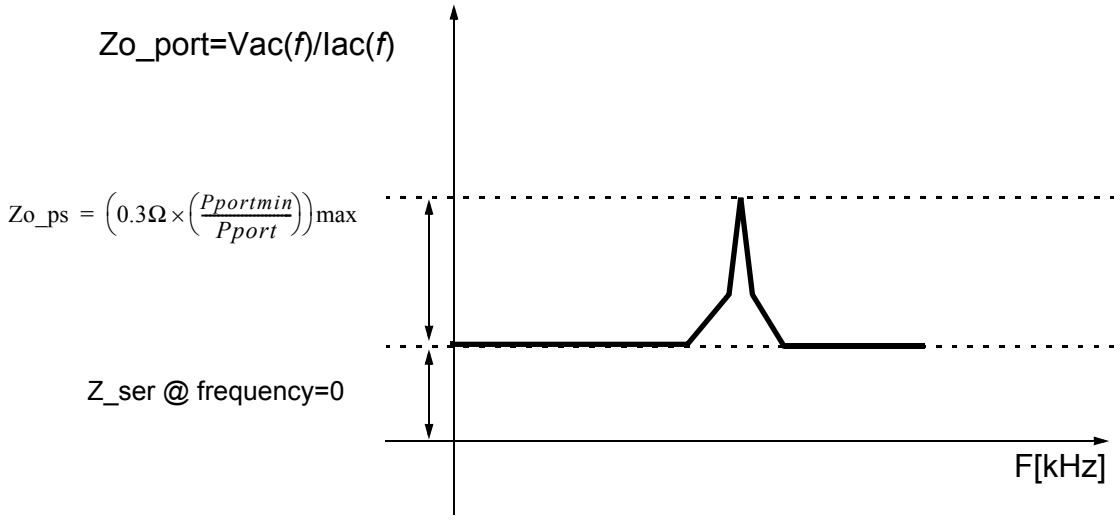


Figure 33A–3—Test requirements for measuring Zo_port

33A.2 Recommended PD design guidelines

PD port input impedance consists of the following two parts:

a) PD port input circuits including the EMI filter (Zin_ser), and
b) PD power supply input impedance (Zin_ps_pd), which is fed by the output of the EMI filter (Zo_emi).

In order to maintain stability with the PSE, the PD power supply input impedance (Zin_ps_pd) should be higher than the output impedance of the total network including the PD EMI output filter impedance fed by the cable (MDI) output impedance, which is fed by the PSE port output impedance.

The worst-case scenario is when the cable (MDI) length is zero (in terms of lower damping factor).

The access to the PD input power supply is not possible through the PD port for evaluating the various impedances and derivation of the above parameters. Because of this, measuring the PD input impedance is a complicated task and the following guidelines should be followed by the PD vendor:

c) The PD power supply input impedance (Zin_ps_pd) at max load of $P_{port} = P_{Port}$ max as defined in Table 33–18 should be higher than 30 Ω at any frequency up to the PD power supply crossover frequency. If the PD power supply is consuming less than $P_{port} = P_{Port}$ max as defined in Table 33–18, then Zin_ps_pd min = $30 \times P_{Port}$ max / P_{port}.
d) The PD power supply EMI filter output impedance should be Zo_emi = 2.7 Ω max. If the PD power supply is consuming less than $P_{port} = P_{Port}$ max, then Zo_emi = $2.7 \times P_{Port}$ max / P_{port}.

See Figure 33A–1 for the PSE-PD system impedance allocation.

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