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(54) **MULTI-LEVEL AMPLITUDE SIGNALING RECEIVER**

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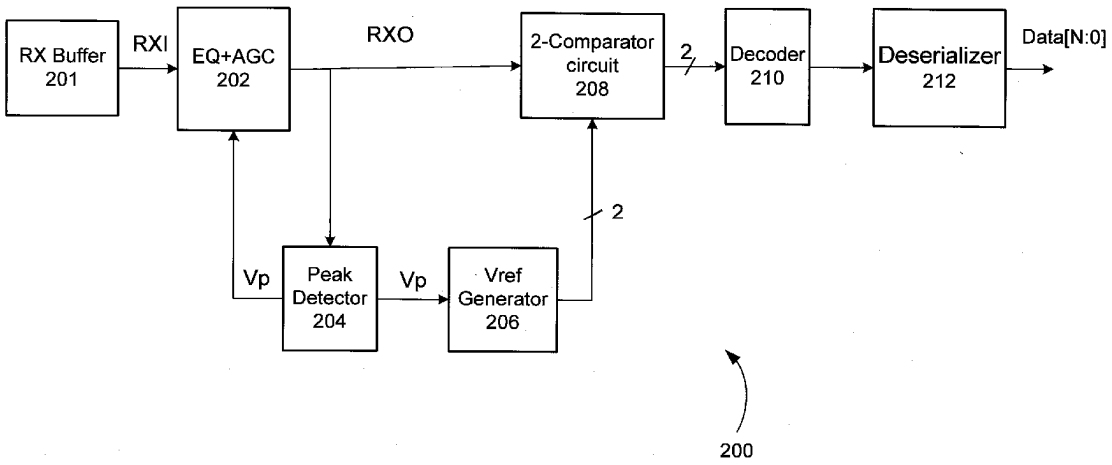
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(52) **U.S. Cl.**

USPC **375/219**; 375/317

(57) **ABSTRACT**

One embodiment relates to a receiver circuit for multi-level amplitude signaling which includes at least three amplitude levels for each symbol period. The receiver circuit includes a peak detector, a reference voltage generator, and a comparator circuit. The peak detector is arranged to detect a peak voltage of the multi-level amplitude signal, and the reference voltage generator uses the peak voltage to generate multiple reference voltages. The comparator circuit uses the multiple reference voltages to detect an amplitude level of the multi-level amplitude signal. Other embodiments and features are also disclosed.



Amphenol Exhibit 1016
Amphenol v. Credo

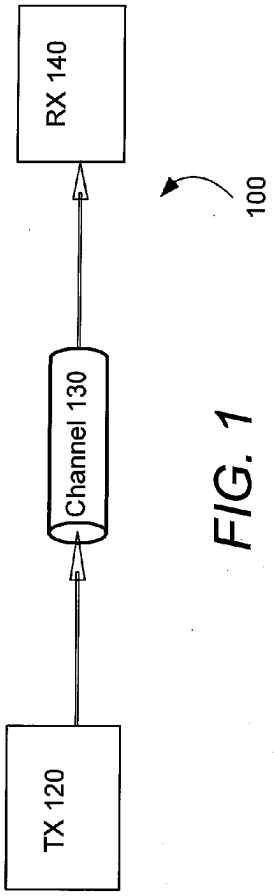

TX 120
Channel 130
RX 140
100

FIG. 1

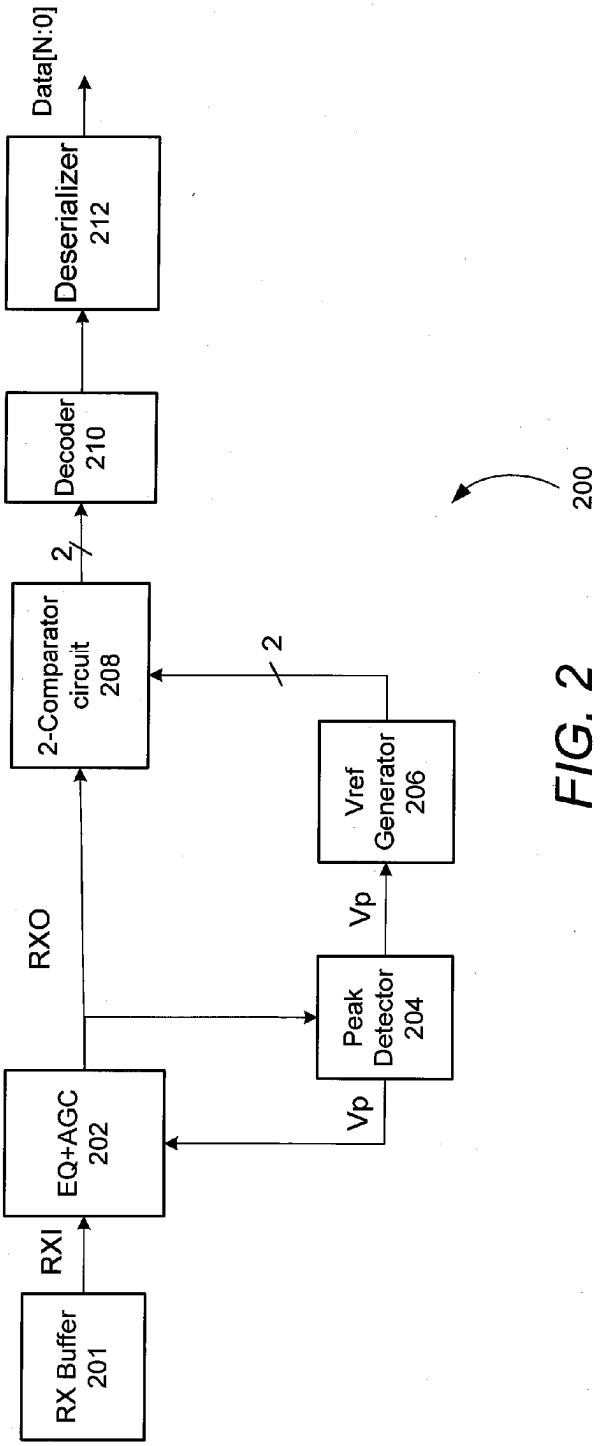

RX Buffer 201
RXI
EQ+AGC 202
RXO
Peak Detector 204
Vp
Vp
Vref Generator 206
2
2-Comparator circuit 208
2
Decoder 210
Deserializer 212
Data[N:0]
200

FIG. 2

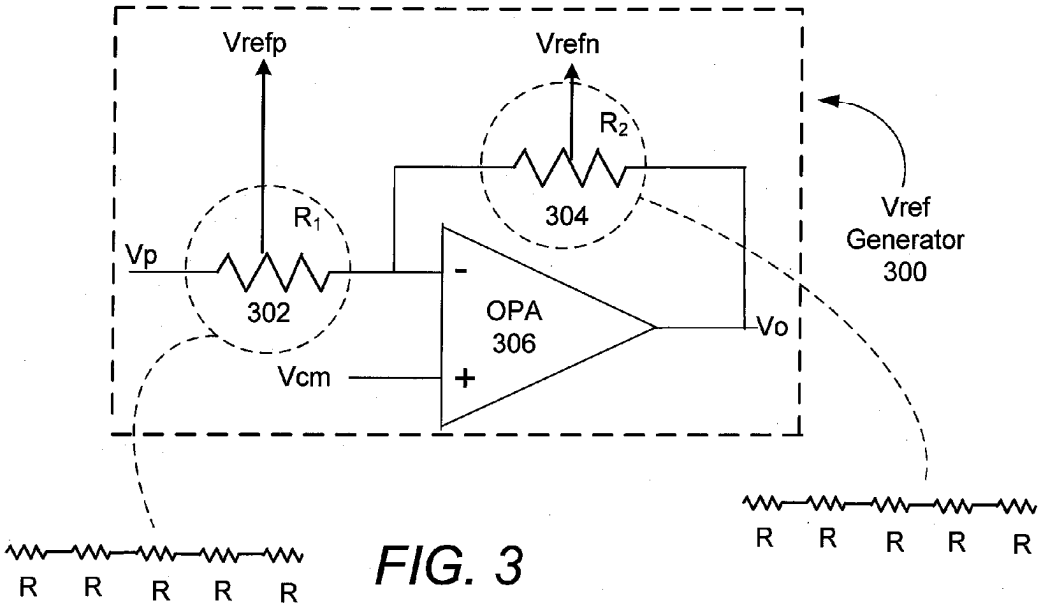

Vrefp
Vrefn
R2
304
R1
Vp
302
OPA
306
Vo
Vcm
Vref
Generator
300
R R R R R
R R R R R

FIG. 3

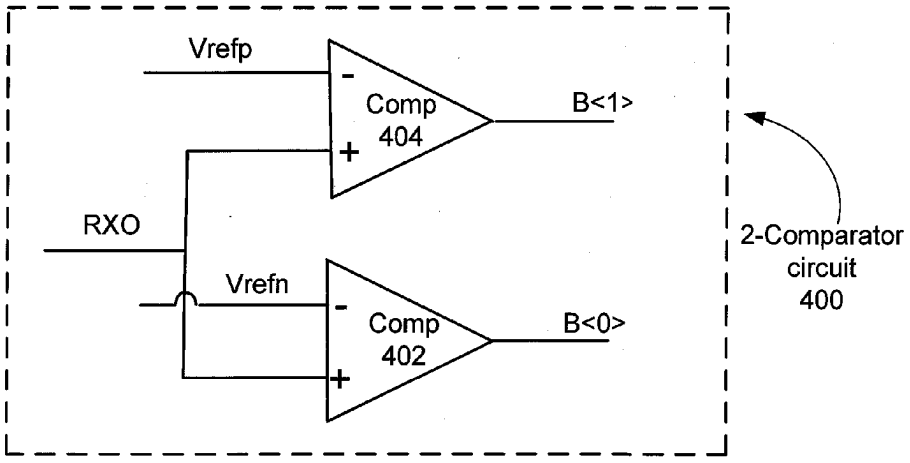

Vrefp
Comp
404
B<1>
RXO
Vrefn
Comp
402
B<0>
2-Comparator
circuit
400

FIG. 4

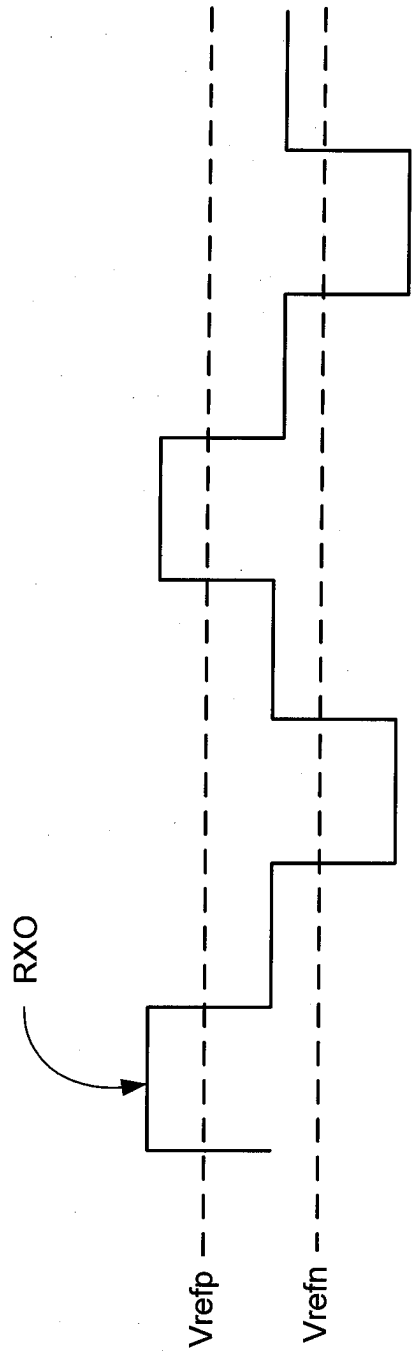


FIG. 5

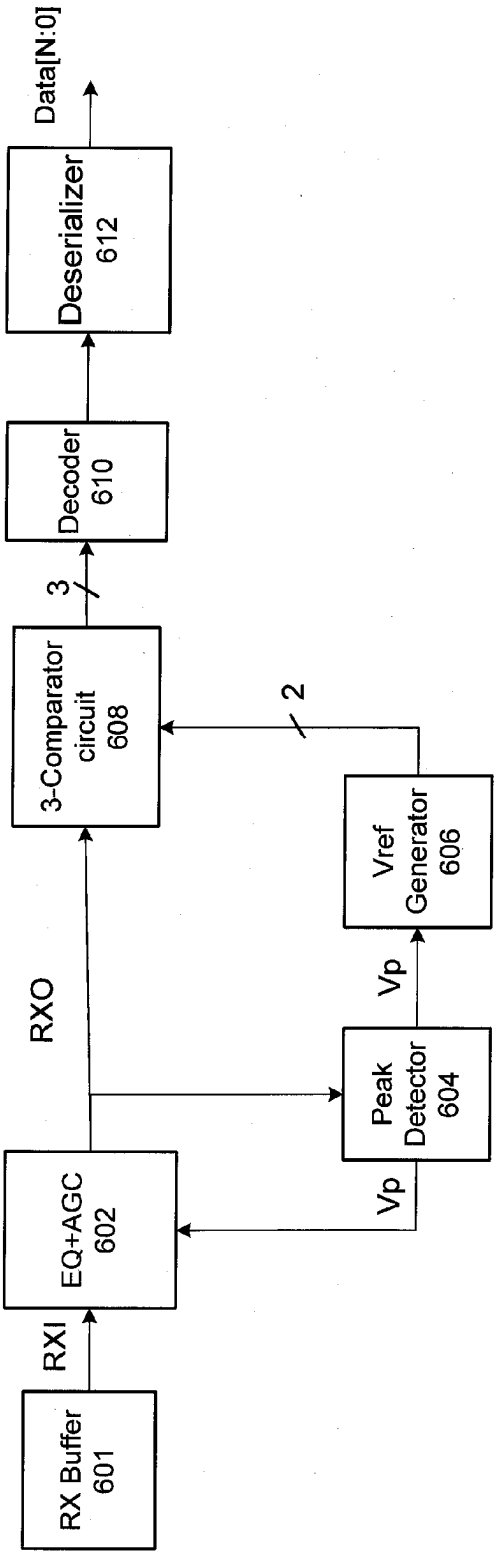

Data[N:0]
Deserializer 612
Decoder 610
3
3-Comparator circuit 608
2
Vref Generator 606
Vp
Peak Detector 604
Vp
RXO
EQ+AGC 602
RXI
RX Buffer 601
600

FIG. 6

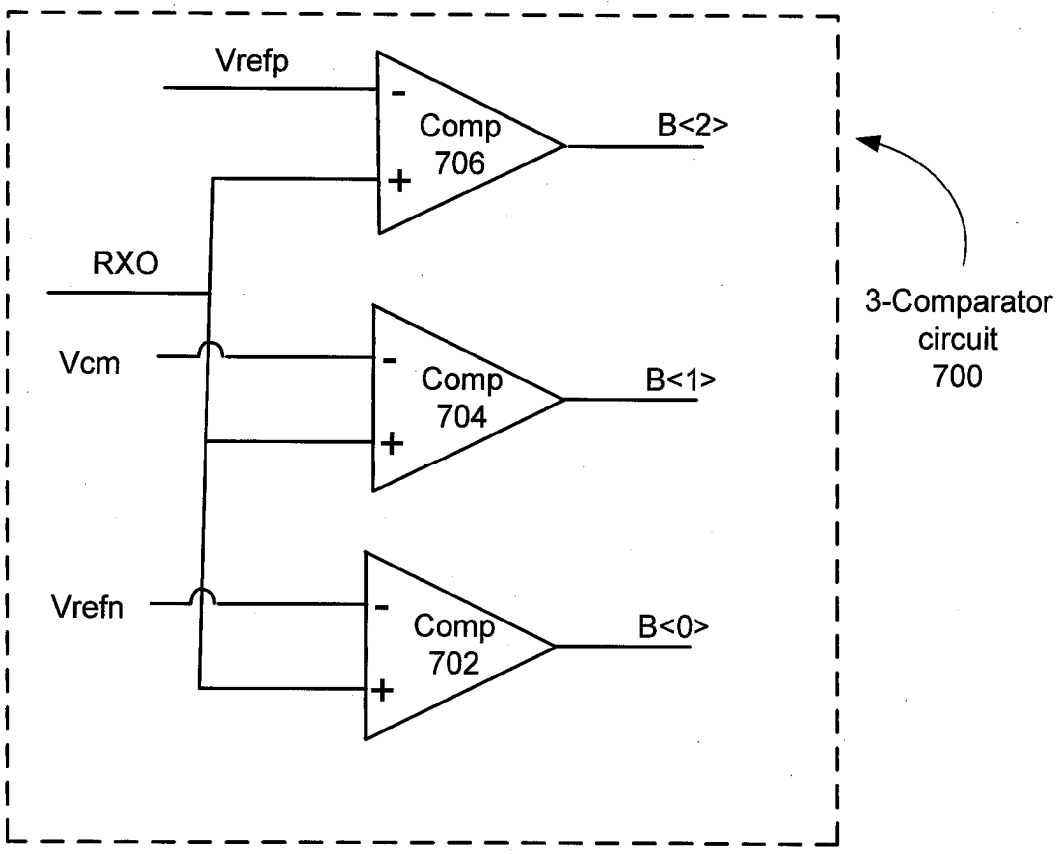

Vrefp
Comp
706
B<2>
RXO
Vcm
Comp
704
B<1>
Vrefn
Comp
702
B<0>
3-Comparator
circuit
700

FIG. 7

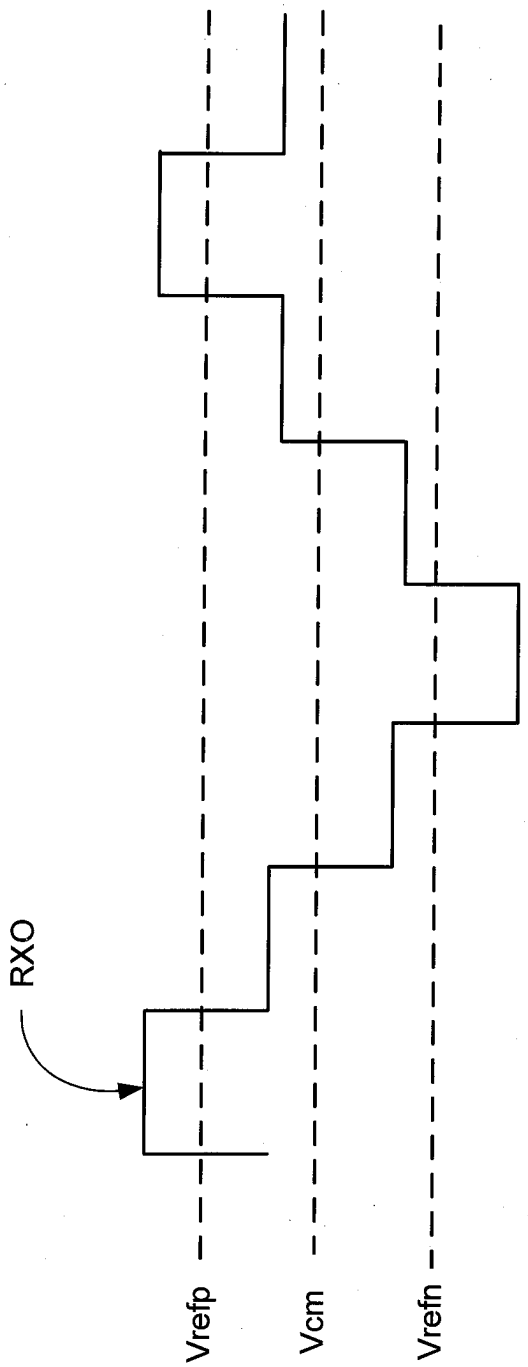


FIG. 8

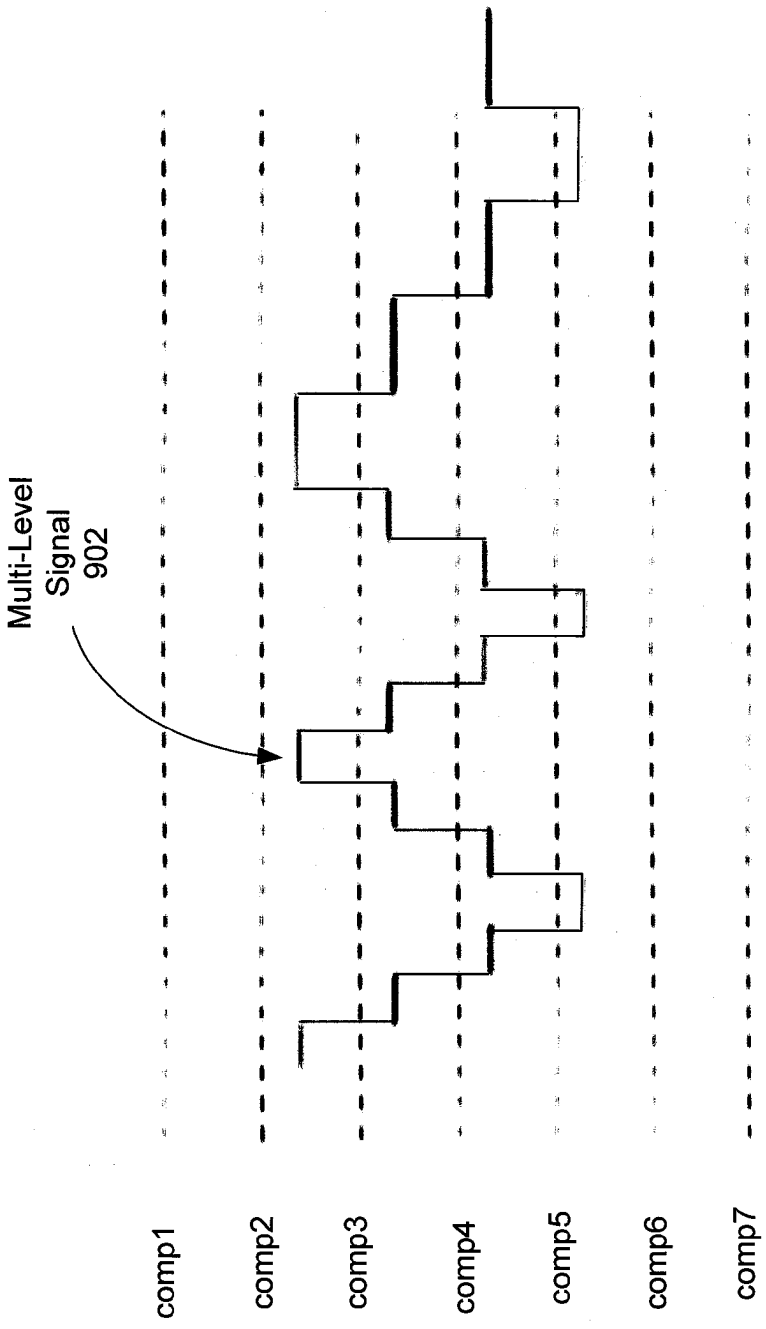


FIG. 9
(Conventional)

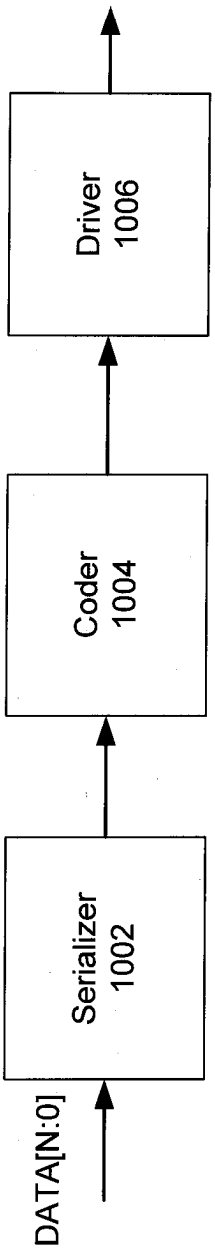


FIG. 10

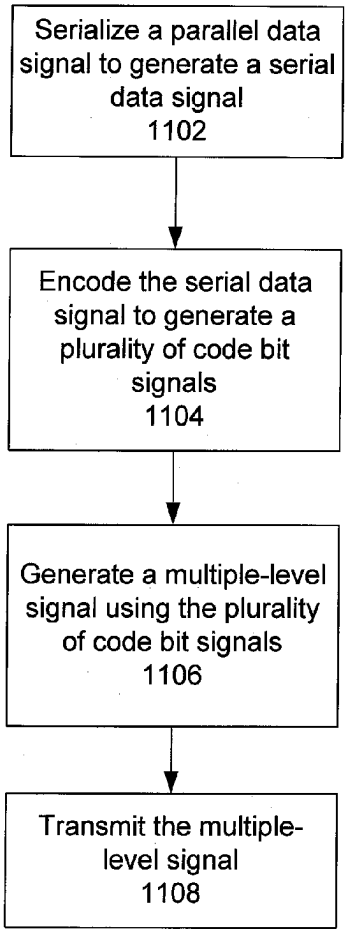


FIG. 11A 1100

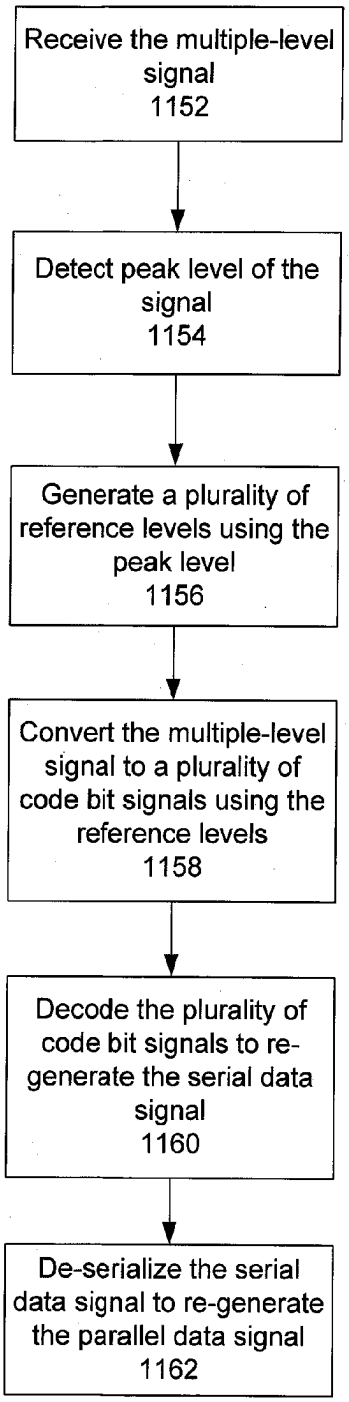


FIG. 11B 1150

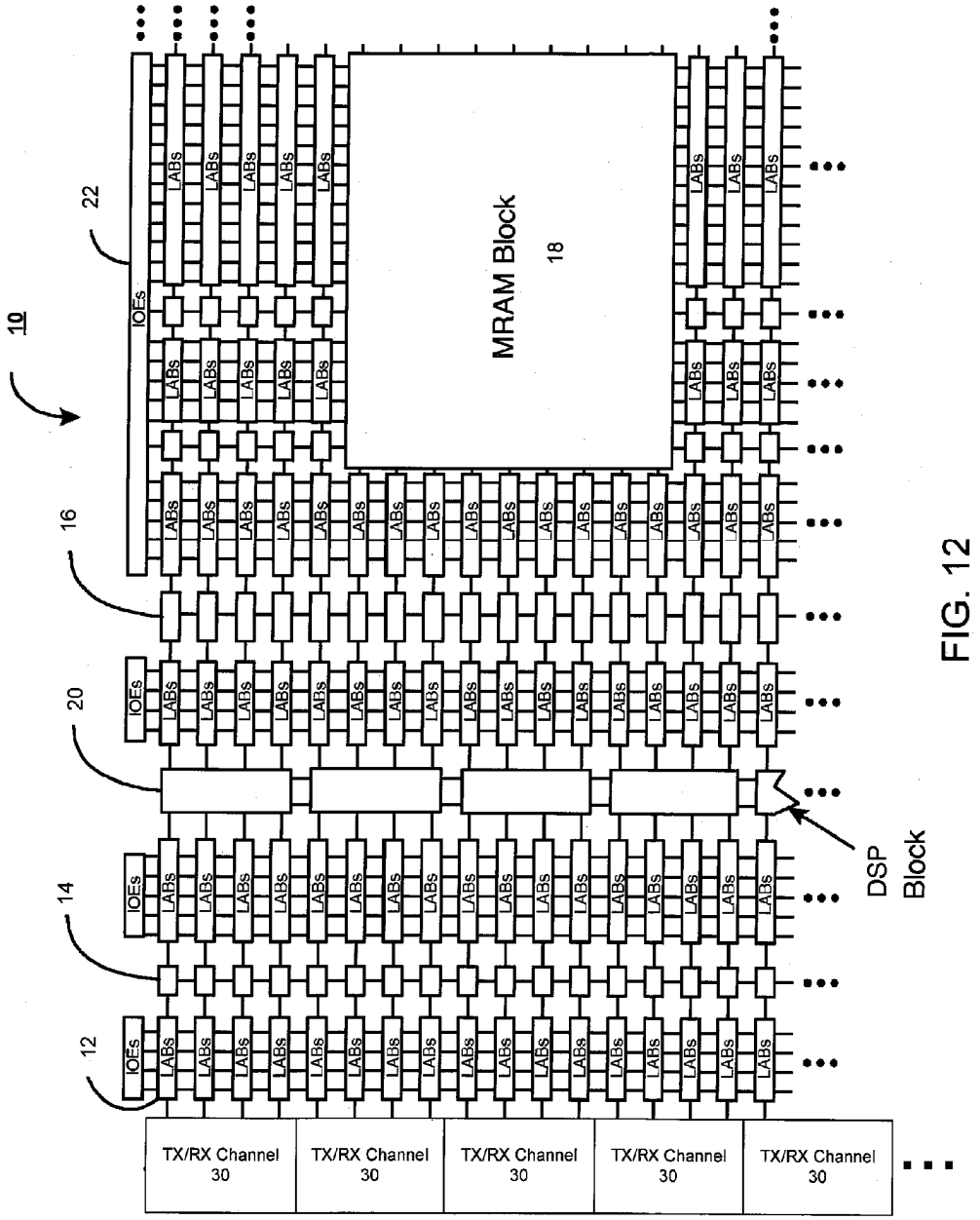

10
22
16
20
14
12
IOEs
LABs
MRAM Block
18
DSP
Block
TX/RX Channel
30

FIG. 12

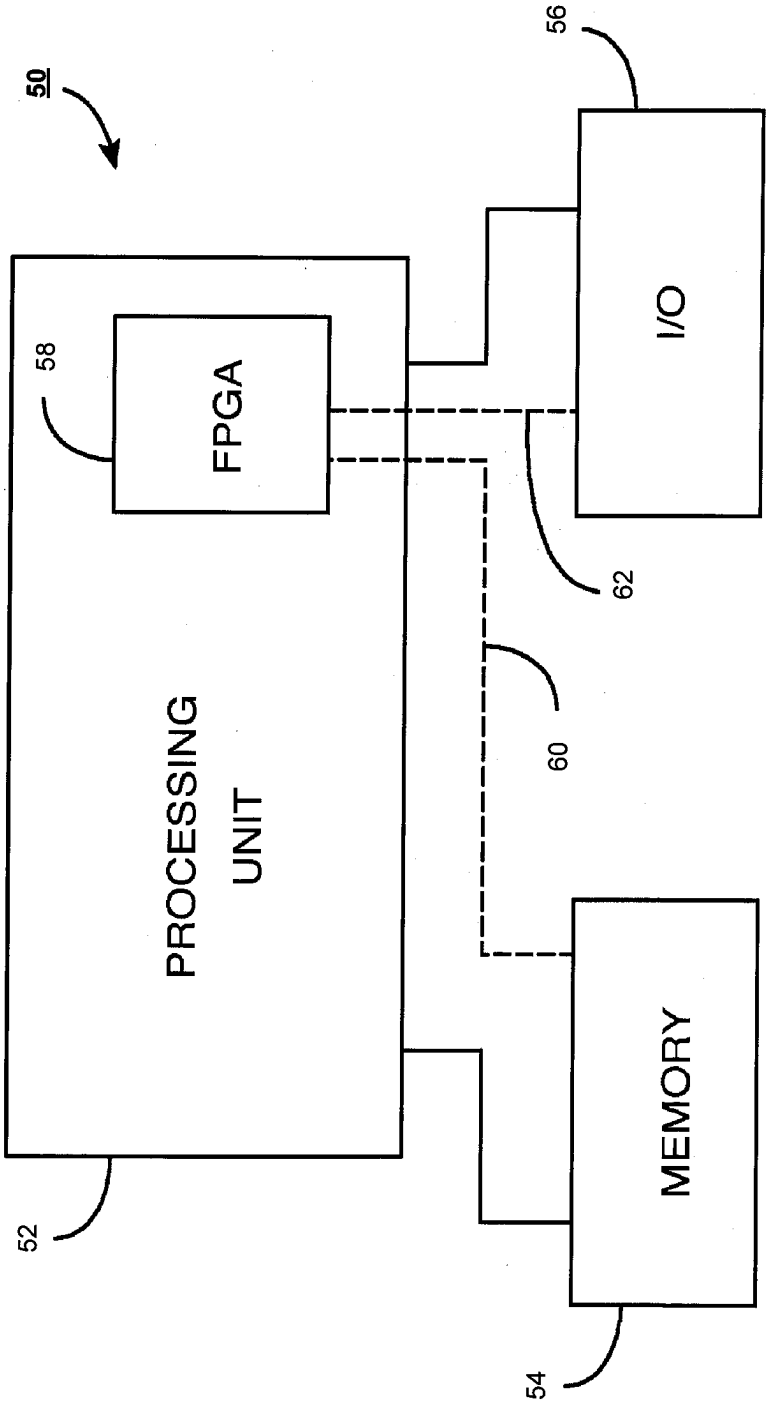


FIG. 13

MULTI-LEVEL AMPLITUDE SIGNALING RECEIVER

BACKGROUND

[0001] 1. Technical Field

[0002] The present invention relates generally to data communications. More particularly, the present invention relates to circuitry for high-speed data links.

[0003] 2. Description of the Background Art

[0004] High-speed data links are used to communicate data between devices in a system. Serial interface protocols have been developed at increasingly fast data rates for such high-speed links. Currently, the data signal for most high-speed serial links use just two voltage levels (amplitudes) to convey information: a high level and a low level. The high level may be interpreted as a logical one, and the low level may be interpreted as a logical zero. Such signaling is sometimes referred to as "non-return-to-zero" (NRZ) data signaling. In NRZ signaling, one symbol provides one bit of information within one unit interval (UI).

[0005] Instead of using just two levels, multi-level amplitude signaling uses several (at least three) distinct voltage levels. Such multi-level amplitude signaling, which is sometimes referred to as pulse amplitude modulation (PAM) signaling, communicates more than one bit of information per symbol. Hence, for the same symbol rate, PAM signaling provides a higher effective data rate than NRZ signaling.

[0006] Unfortunately, transceiver complexity generally increases if, instead of NRZ signaling, PAM signaling is implemented. For example, a high-speed analog-to-digital converter (ADC) circuit is typically implemented at the front end of the receiver to digitize the PAM signal. However, such a high-speed ADC circuit generally requires a relatively large area to implement and typically consumes a large amount of power.

SUMMARY

[0007] One embodiment relates to a receiver circuit for multi-level amplitude signaling which includes at least three amplitude levels for each symbol period. The receiver circuit includes a peak detector, a reference voltage generator, and a comparator circuit. The peak detector is arranged to detect a peak voltage of the multi-level amplitude signal, and the reference voltage generator uses the peak voltage to generate multiple reference voltages. The comparator circuit uses the multiple reference voltages to detect an amplitude level of the multi-level amplitude signal.

[0008] Another embodiment relates to a method of receiving a multi-level amplitude signal which includes at least three amplitude levels for each symbol period. A peak voltage of the multi-level amplitude signal is detected, and multiple reference voltages which depend on the peak voltage are generated. The multi-level amplitude signal is compared against the plurality of reference voltages to detect an amplitude level.

[0009] Another embodiment relates to an integrated circuit which includes a pulse amplitude modulation receiver. The receiver includes at least a peak detector, a reference voltage generator, and a comparator circuit The peak detector is arranged to detect a peak voltage of a transmitted pulse amplitude modulation signal which includes at least three amplitude levels for each symbol period. The reference voltage generator is arranged to generate a plurality of reference voltages which depend on the peak voltage. The comparator circuit is arranged to compare the pulse amplitude modulation signal against the plurality of reference voltages to detect an amplitude level.

[0010] Other embodiments and features are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1** is a high-level diagram of a communication link in accordance with an embodiment of the invention.

[0012] FIG. **2** is a block diagram depicting a PAM-3 signaling receiver in accordance with an embodiment of the invention.

[0013] FIG. **3** depicts reference voltage generator circuit which may be used by a receiver in accordance with an embodiment of the invention.

[0014] FIG. **4** depicts a 2-comparator circuit which may be used by a three-level signaling receiver in accordance with an embodiment of the invention.

[0015] FIG. **5** shows an example PAM-3 signal and two reference levels that may be generated and used by a receiver circuit in accordance with an embodiment of the invention.

[0016] FIG. **6** is a block diagram depicting a PAM-4 signaling receiver in accordance with an embodiment of the invention.

[0017] FIG. **7** depicts a three-comparator circuit may be used by a PAM-4 signaling receiver in accordance with an embodiment of the invention.

[0018] FIG. **8** shows an example PAM-4 signal and three reference levels that may be generated and used by a receiver circuit in accordance with an embodiment of the invention.

[0019] FIG. **9** shows an example PAM-4 signal and seven reference levels that may be used by a conventional receiver circuit.

[0020] FIG. **10** is a block diagram of a multi-level amplitude signaling transmitter in accordance with an embodiment of the invention.

[0021] FIG. **11**A is a flow chart of a method of transmitting a multi-level amplitude signal in accordance with an embodiment of the invention.

[0022] FIG. **11**B is a flow chart of a method of receiving a multi-level amplitude signal in accordance with an embodiment of the invention.

[0023] FIG. **12** is a simplified partial block diagram of a field programmable gate array that may be arranged or configured to include one or more of the circuits disclosed herein in accordance with an embodiment of the invention.

[0024] FIG. **13** is a block diagram of an exemplary digital system that may employ a multi-level signaling data link in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

[0025] The present disclosure provides an innovative receiver architecture for PAM signaling that substantially reduces the receiver complexity. In accordance with an embodiment of the invention, the receiver architecture automatically aligns a number of slicing voltage levels to minimize the number of required samplers.

[0026] FIG. **1** is a high-level diagram of a communication link **100** in accordance with an embodiment of the invention. As shown in FIG. **1**, a communication link **100** is generally composed of a transmitter (TX) **120**, a receiver (RX) **140**, and a communication channel **130** that is used to communicate

signals between the transmitter and the receiver. The channel **130** may include one or more lanes.

[0027] As relevant to the present disclosure, the communication link **100** may utilize multi-level signaling to increase the effective data rate of the link **100**. Such multi-level signaling uses three or more voltage levels to communicate information.

[0028] In PAM signaling, information is encoded in the amplitude of a series of signal pulses. PAM-M signaling refers to PAM signaling where the amplitude of each signal pulse may be at one of M voltage levels. For example, in PAM-3 signaling, the amplitude of each signal pulse may be at one of three voltage levels, such as, for instance: −3 volts; 0 volts; or +3 volts. As another example, in PAM-4 signaling, the amplitude of each signal pulse may be at one of four voltage levels, such as, for instance: −3 volts; −1 volt; +1 volt; or +3 volts. NRZ signaling is essentially PAM-2 signaling. Note that, while embodiments involving PAM-3 and PAM-4 signaling are described in detail below, the receiver architecture disclosed herein may be applied in general to PAM-M signaling, where M is three or more.

[0029] FIG. **2** is a block diagram depicting a PAM-3 signaling receiver **200** in accordance with an embodiment of the invention. As shown, the receiver **200** may include a receiver buffer (RX Buffer) **201**, an equalizer and automatic gain control (EQ+AGC) circuit **202**, a peak detector **204**, a voltage reference generator (Vref generator) **206**, a 2-comparator circuit **208**, a decoder **210**, and a deserializer **212**.

[0030] The RX Buffer **201** may be arranged to receive a PAM-3 signal which has been transmitted over a communication channel **130** and to output a buffered PAM-3 signal (RXI). The RXI signal may be input into the EQ+AGC circuit **202**. After equalizing and adjusting the gain of the signal, the EQ+AGC circuit **202** may output an equalized and gain-adjusted PAM-3 signal (the RXO signal).

[0031] The RXO signal may be input to both the peak detector **204** and the 2-Comparator circuit **208**. The peak detector **204** may be arranged to output a peak voltage (Vp) signal which corresponds to a peak voltage of the RXO signal. The peak detector **204** may be implemented, for example, using on-chip signal quality monitoring circuitry which may be referred to as EYE Monitor circuitry. As shown, the Vp signal may be output to both the Vref generator **206** and the EQ+AGC circuit **202**. The EQ+AGC circuit **202** may use the Vp signal in its adjustment of the signal gain.

[0032] The Vref generator **206** may be arranged to utilize the Vp signal to generate multiple reference voltage levels. In this case, two reference voltage levels may be generated by the Vref generator **206**. One embodiment of the Vref generator **206** is described below in relation to FIG. **3**.

[0033] The 2-comparator circuit **208** may be arranged to use the reference voltage levels from the Vref generator **206** as slicing levels for the PAM-3 signal. A two-bit signal that indicates the comparison results may be output from the 2-comparator circuit **208**. One embodiment of the **2**-comparator circuit **208** is described below in relation to FIG. **4**.

[0034] The 2-bit signal from the 2-comparator circuit **208** may be received by the decoder **210**. The decoder **210** may be arranged to decode the 2-bit signal so as to re-generate the serial binary data signal from the transmitter. The serial binary data signal may be received by the deserializer **212**. The deserializer **212** may be arranged to convert the serial binary data signal to parallel binary data signals (shown as Data[N:0]).

[0035] In contrast to a conventional PAM signaling receiver, the receiver **200** in FIG. **2** does not include an ADC circuit at the front end. Instead, two slicing voltage levels are automatically generated using the peak detector **204** and the Vref generator **206**, and the 2-comparator circuit **208** and the decoder **210** are used to demodulate and decode the signal.

[0036] FIG. **3** depicts a reference voltage generator circuit (Vref generator) **300** which may be used by a receiver in accordance with an embodiment of the invention. The Vref generator **300** in FIG. **3** may be used as the Vref Generator **206** for the receiver **200** in FIG. **2**. As shown in FIG. **3**, the Vref generator **300** may include an inverting amplifier circuit which is formed using a first resistor ladder **302** having an end-to-end resistance R_1, a second resistor ladder **304** having an end-to-end resistance R_2, and an operational amplifier (OPA) circuit **306**.

[0037] The first resistor ladder **302** may be arranged between a peak voltage Vp input and the negative input terminal of the OPA **306**. The second resistor ladder **304** may be arranged between the negative input terminal and the output terminal of the OPA **306**. The positive input terminal of the OPA **306** may be connected to a common mode voltage Vcm. The output terminal of the OPA **306** may provide an output voltage signal $Vo=-(R_2/R_1)\,Vp+Vcm\,(R_1+R_2)/R_1$. If Vcm is zero volts (ground) and $R_1=R_2$, then $Vo=-Vp$.

[0038] The first resistor ladder **302** may include multiple resistor elements R in series, and a first (positive) reference voltage (Vrefp) may be obtained from a node between two adjacent resistor elements R in the ladder. The node in the ladder which outputs Vrefp may be programmably selected during configuration of the receiver. In this case, due to the negative terminal of the OPA **306** being effectively driven to Vcm, the voltage level for Vrefp may be programmably selected to be a voltage level in a range between Vp and Vcm.

[0039] Similarly, the second resistor ladder **304** may also include multiple resistor elements R in series, and a second (negative) reference voltage (Vrefn) may be obtained from a node between two adjacent resistor elements R in the ladder. The node in the ladder which outputs Vrefn may be programmably selected during configuration of the receiver. In this case, due to the negative terminal of the OPA **306** being effectively driven to Vcm, the voltage level for Vrefn may be programmably selected to be a voltage level in a range between Vcm and Vo.

[0040] While the example resistor ladders shown in FIG. **3** each have five resistor elements, the number of resistor elements may be any number. For example, a larger number of resistor elements may be included in a resistor ladder to increase the granularity at which a reference voltage may be programmably selected. Furthermore, the resistance of the resistor elements R in a ladder may be the same, or may vary, depending on the implementation.

[0041] FIG. **4** depicts a 2-comparator circuit **400** which may be used by a three-level signaling receiver in accordance with an embodiment of the invention. The 2-comparator circuit **400** in FIG. **4** may be used as the 2-comparator circuit **208** for the receiver **200** in FIG. **2**.

[0042] A first comparator **402** may be arranged to compare each symbol in the RXO signal (the equalized and gain-adjusted PAM-3 signal from the EQ+ADC circuit **202**) against the Vrefn signal (the negative reference voltage from the Vref generator **206**). The output of the first comparator **402** may be a first code bit signal B<**0**> which depends on the result of the comparison. For example, B<**0**> may be high

(logical one) if RXO is higher than Vrefn at the time of the comparison and may be low (logical zero) if RXO is lower than Vrefn at the time of the comparison.

[0043] A second comparator **404** may be arranged to compare each symbol in the RXO signal against the Vrefp signal (the positive reference voltage from the Vref generator **206**). The output of the second comparator **404** may be a second code bit signal B<**1**> which depends on the result of the comparison. For example, B<**1**> may be high (logical one) if RXO is higher than Vrefp at the time of the comparison and may be low (logical zero) if RXO is lower than Vrefp at the time of the comparison.

[0044] The two-bit code signal (including B<**0**> and B<**1**>) indicates an amplitude level for each symbol in the PAM-3 signal. For example, if B<**0**> and B<**1**> are both low, then the amplitude may be indicated to be at a low level. If B<**0**> and B<**1**> are both high, then the amplitude may be indicated to be at a high level. Finally, if B<**0**> is high and B<**1**> is low, then the amplitude may be indicated to be at a middle level.

[0045] FIG. **5** shows an example PAM-3 signal (RXO) and two reference levels (Vrefn and Vrefp) that may be generated and used by a receiver circuit in accordance with an embodiment of the invention. As seen, the RXO signal may transition between three amplitude levels: a low level below Vrefn; a high level above Vrefp; and a middle level between Vrefn and Vrefp.

[0046] FIG. **6** is a block diagram depicting a PAM-4 signaling receiver in accordance with an embodiment of the invention. As shown, the receiver **600** may include a receiver buffer (RX Buffer) **601**, an equalizer and automatic gain control (EQ+AGC) circuit **602**, a peak detector **604**, a voltage reference generator (Vref generator) **606**, a **3**-comparator circuit **608**, a decoder **610**, and a deserializer **612**.

[0047] The RX Buffer **601** may be arranged to receive a PAM-4 signal which has been transmitted over a communication channel **130** and to output a buffered PAM-4 signal (RXI). The RXI signal may be input into the EQ+AGC circuit **602**. After equalizing and adjusting the gain of the signal, the EQ+AGC circuit **602** may output an equalized and gain-adjusted PAM-4 signal (the RXO signal).

[0048] The RXO signal may be input to both the peak detector **604** and the 3-Comparator circuit **608**. The peak detector **604** may be arranged to output a peak voltage (Vp) signal which corresponds to a peak voltage of the RXO signal. The peak detector **604** may be implemented, for example, using EYE Monitor circuitry. As shown, the Vp signal may be output to both the Vref generator **606** and the EQ+AGC circuit **602**. The EQ+AGC circuit **602** may use the Vp signal in its adjustment of the signal gain.

[0049] The Vref generator **606** may be arranged to utilize the Vp signal to generate multiple reference voltage levels. In this case, two reference voltage levels may be generated by the Vref generator **606**. One embodiment of the Vref generator **606** is described above in relation to FIG. **3**.

[0050] The 3-comparator circuit **608** may be arranged to use the two reference voltage levels from the Vref generator **606** and the common mode voltage level (Vcm) as slicing levels for the PAM-4 signal. A three-bit signal that indicates the comparison results may be output from the 3-comparator circuit **608**. One embodiment of the 3-comparator circuit **608** is described below in relation to FIG. **7**.

[0051] The 3-bit signal from the 3-comparator circuit **608** may be received by the decoder **610**. The decoder **610** may be arranged to decode the 3-bit signal so as to re-generate the serial binary data signal from the transmitter. The serial binary data signal may be received by the deserializer **612**. The deserializer **612** may be arranged to convert the serial binary data signal to parallel binary data signals (shown as Data[N:0]).

[0052] In contrast to a conventional PAM signaling receiver, the receiver **600** in FIG. **6** does not include an ADC circuit at the front end. Instead, three slicing voltage levels are automatically generated using the peak detector **604** and the Vref generator **606**, and the 3-comparator circuit **608** and the decoder **610** are used to demodulate and decode the signal.

[0053] FIG. **7** depicts a 3-comparator circuit **700** which may be used by a PAM-4 receiver in accordance with an embodiment of the invention. The 3-comparator circuit **700** in FIG. **7** may be used as the 3-comparator circuit **608** for the receiver **600** in FIG. **6**.

[0054] A first comparator **702** may be arranged to compare each symbol in the RXO signal (the equalized and gain-adjusted PAM-4 signal from the EQ+ADC circuit **602**) against the Vrefn signal (the negative reference voltage from the Vref generator **606**). The output of the first comparator **702** may be a first code bit signal B<**0**> which depends on the result of the comparison. For example, B<**0**> may be high (logical one) if RXO is higher than Vrefn at the time of the comparison and may be low (logical zero) if RXO is lower than Vrefn at the time of the comparison.

[0055] A second comparator **704** may be arranged to compare each symbol in the RXO signal against the Vcm signal (the common mode voltage). The output of the second comparator **704** may be a second code bit signal B<**1**> which depends on the result of the comparison. For example, B<**1**> may be high (logical one) if RXO is higher than Vcm at the time of the comparison and may be low (logical zero) if RXO is lower than Vcm at the time of the comparison.

[0056] A third comparator **706** may be arranged to compare each symbol in the RXO signal against the Vrefp signal (the positive reference voltage from the Vref generator **606**). The output of the third comparator **704** may be a third code bit signal B<**2**> which depends on the result of the comparison. For example, B<**2**> may be high (logical one) if RXO is higher than Vrefp at the time of the comparison and may be low (logical zero) if RXO is lower than Vrefp at the time of the comparison.

[0057] The three-bit code signal (including B<**0**>, B<**1**>, and B<**2**>) indicates an amplitude level for each symbol in the PAM-4 signal. For example, if B<**0**> is low, then the amplitude may be indicated to be at a lowest level, while if B<**2**> is high, then the amplitude may be indicated to be at a highest level. Else, if B<**0**> is high and B<**2**> is low, then the amplitude may be indicated to be at a second lowest level if B<**1**> is low and may be indicated to be at a second highest level if B<**1**> is high.

[0058] FIG. **8** shows an example PAM-4 signal and three reference levels that may be generated and used by a receiver circuit in accordance with an embodiment of the invention. As seen, the RXO signal may transition between four amplitude levels: a lowest level below Vrefn; a second lowest level above Vrefn and below Vcm; a second highest level above Vcm and below Vrefp; and a highest level above Vrefp. Advantageously, the automatic alignment of the reference levels to slice the PAM-4 signal allows for a minimal number of comparators to be used.

[0059] In contrast, FIG. **9** shows an example PAM-4 signal and seven reference levels (comp**1** through comp**7**) that may

be used by a conventional receiver circuit. For a conventional receiver, the reference levels are not automatically aligned to slice the PAM-4 signal. As such, a greater number of comparators are needed to ensure that the reference levels can accurately distinguish between the different levels of the PAM-4 signal.

[0060] In accordance with an embodiment of the invention, FIG. **10** is a block diagram of a multi-level amplitude signaling transmitter **1000**, while FIG. **11**A shows a flow chart of a method of transmitting a multi-level amplitude signal. As shown in FIG. **10**, the transmitter **1000** may include a serializer **1002**, a coder **1004**, and a driver **1006**. The serializer **1002** receives parallel data signals (DATA[N:0]) to be transmitted over a communication channel **130** to a receiver **140**. The serializer **1002** serializes **1102** the parallel data signal to generate a serial data signal which is output to the coder **1004**. The coder **1004** may be arranged to encode **1104** the serial data signal so as to generate a plurality of code bit signals. The driver **1006** may be arranged to generate **1106** a multi-level amplitude signal based on the code bit signals and transmit **1108** the multi-level amplitude signal via the communication channel **130** to the receiver **140**.

[0061] A method of receiving **1150** a multi-level amplitude signal is shown in FIG. **11**B in accordance with an embodiment of the invention. As shown, the mutli-level amplitude signal may be received, and a peak level of the signal may be detected **1154**. Using the peak level of the multi-level amplitude signal, a plurality of reference levels may be generated **1156**.

[0062] In accordance with an embodiment of the invention, the reference levels may be generated **1156** in a manner such that they are automatically aligned. The alignment is such that the multi-level amplitude signal may be sliced in a robust way into distinct levels. The alignment may be achieved automatically by the detection of the peak voltage and by using a reference voltage generator which has been previously programmed to generate slicing voltages that are appropriate for the particular multi-level amplitude signal being received.

[0063] The multi-level amplitude signal may then be converted **1158** to a plurality of code bit signals using the reference levels, and the plurality of code bit signals may be decoded **1160** to generate the serial data signal. Finally, the serial data signal may be de-serialized **1162** to re-generate the parallel data signal which was transmitted.

[0064] FIG. **12** is a simplified partial block diagram of a field programmable gate array (FPGA) **10** that may be arranged or configured to include one or more of the circuits disclosed herein in accordance with an embodiment of the invention. It should be understood that embodiments of the present invention may be used in numerous types of integrated circuits, including FPGAs, programmable logic devices (PLDs), complex programmable logic devices (CPLDs), programmable logic arrays (PLAs), digital signal processors (DSPs) and application specific integrated circuits (ASICs).

[0065] FPGA **10** includes within its "core" a two-dimensional array of programmable logic array blocks (or LABs) **12** that are interconnected by a network of column and row interconnect conductors of varying length and speed. LABs **12** include multiple (e.g., ten) logic elements (or LEs). An LE is a programmable logic block that provides for efficient implementation of user defined logic functions. An FPGA has numerous logic elements that can be configured to implement various combinatorial and sequential functions. The logic elements have access to a programmable interconnect structure. The programmable interconnect structure can be programmed to interconnect the logic elements in almost any desired configuration.

[0066] FPGA **10** may also include a distributed memory structure including random access memory (RAM) blocks of varying sizes provided throughout the array. The RAM blocks include, for example, blocks **14**, blocks **16**, and block **18**. These memory blocks can also include shift registers and FIFO buffers. FPGA **10** may further include digital signal processing (DSP) blocks **20** that can implement, for example, multipliers with add or subtract features.

[0067] Input/output elements (IOEs) **22** located, in this example, around the periphery of the chip support numerous single-ended and differential input/output standards. Each **10**E **22** is coupled to an external terminal (i.e., a pin) of FPGA **10**. A transceiver (TX/RX) channel array may be arranged as shown, for example, with each TX/RX channel circuit **30** being coupled to several LABs. A TX/RX channel circuit **30** may include, among other circuitry, the receiver circuitry described herein.

[0068] It is to be understood that FPGA **10** is described herein for illustrative purposes only and that the present invention can be implemented in many different types of PLDs, FPGAs, and ASICs.

[0069] FIG. **13** is a block diagram of an exemplary digital system **50** that may employ multi-level amplitude signaling in accordance with an embodiment of the invention. As shown, system **50** may include an FPGA as one of several components.

[0070] System **50** may be, for example, a programmed digital computer system, digital signal processing system, specialized digital switching network, or other processing system. System **50** may be designed for a wide variety of applications such as telecommunications systems, automotive systems, control systems, consumer electronics, personal computers, Internet communications and networking, and others. Further, system **50** may be provided on a single board, on multiple boards, or within multiple enclosures.

[0071] As shown, system **50** includes a processing unit **52**, a memory unit **54**, and an input/output (I/O) unit **56** interconnected together by one or more buses. According to this exemplary embodiment, FPGA **58** is embedded in processing unit **52**. FPGA **58** may serve many different purposes within the system **50**. FPGA **58** may, for example, be a logical building block of processing unit **52**, supporting its internal and external operations. FPGA **58** is programmed to implement the logical functions necessary to carry on its particular role in system operation. FPGA **58** can be specially coupled to memory **54** through connection **60** and to I/O unit **56** through connection **62**.

[0072] Processing unit **52** may direct data to an appropriate system component for processing or storage, execute a program stored in memory **54**, receive and transmit data via I/O unit **56**, or other similar function. Processing unit **52** may be a central processing unit (CPU), microprocessor, floating point coprocessor, graphics coprocessor, hardware controller, microcontroller, field programmable gate array programmed for use as a controller, network controller, or any type of processor or controller. Furthermore, in many embodiments, there is often no need for a CPU.

[0073] For example, instead of a CPU, one or more FPGAs **58** may control the logical operations of the system. As another example, FPGA **58** acts as a reconfigurable processor

that may be reprogrammed as needed to handle a particular computing task. Alternately, FPGA **58** may itself include an embedded microprocessor. Memory unit **54** may be a random access memory (RAM), read only memory (ROM), fixed or flexible disk media, flash memory, tape, or any other storage means, or any combination of these storage means.

[0074] In the above description, numerous specific details are given to provide a thorough understanding of embodiments of the invention. However, the above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise forms disclosed. One skilled in the relevant art will recognize that the invention can be practiced without one or more of the specific details, or with other methods, components, etc.

[0075] In other instances, well-known structures or operations are not shown or described in detail to avoid obscuring aspects of the invention. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. These modifications may be made to the invention in light of the above detailed description.

What is claimed is:

1. A receiver circuit for multi-level amplitude signaling, the receiver circuit comprising:
- a peak detector for detecting a peak voltage of a multi-level amplitude signal which includes at least three amplitude levels for each symbol period;
- a reference voltage generator for generating a plurality of reference voltages at least partially in response to the peak voltage; and
- a comparator circuit which uses the plurality of reference voltages to detect an amplitude level of the multi-level amplitude signal.

2. The receiver circuit of claim **1**, wherein a number of comparators in the comparator circuit is less than a number of amplitude levels in the multi-level amplitude signal.

3. The receiver circuit of claim **2**, wherein the multi-level amplitude signal comprises a three-level pulse amplitude modulated (PAM-3) signal, and wherein the comparator circuit comprises less than three comparators.

4. The receiver circuit of claim **2**, wherein the multi-level amplitude signal comprises a four-level pulse amplitude modulated (PAM-4) signal, and wherein the comparator circuit comprises less than four comparators.

5. The receiver circuit of claim **1**, wherein the reference voltage generator comprises an inverting amplifier that includes at least one resistor ladder.

6. The receiver circuit of claim **5**, wherein a reference voltage is obtained from a node in the resistor ladder.

7. The receiver circuit of claim **6**, wherein selection of the node is programmable.

8. A method of receiving a multi-level amplitude signal, the method comprising:
- detecting a peak voltage of a multi-level amplitude signal which includes at least three amplitude levels for each symbol period;
- generating a plurality of reference voltages at least partially responsive to the peak voltage; and
- comparing the multi-level amplitude signal against the plurality of reference voltages to detect an amplitude level.

9. The method of claim **8**, wherein the comparing is performed by a number of comparators that is less than a number of amplitude levels in the multi-level amplitude signal.

10. The method of claim **9**, wherein the multi-level amplitude signal comprises a three-level pulse amplitude modulated (PAM-3) signal, and wherein the comparator comparing is performed by less than three comparators.

11. The method of claim **9**, wherein the multi-level amplitude signal comprises a four-level pulse amplitude modulated (PAM-4) signal, and wherein the comparing is performed by less than four comparators.

12. The method of claim **8**, wherein the plurality of reference voltages are generated using an inverting amplifier that includes at least one resistor ladder.

13. The method of claim **12**, further comprising:
- obtaining a reference voltage from a node in the resistor ladder.

14. An integrated circuit comprising:
- a pulse amplitude modulation receiver which includes
  - a peak detector arranged to detect a peak voltage of a transmitted pulse amplitude modulation signal which includes at least three amplitude levels for each symbol period,
  - a reference voltage generator arranged to generate a plurality of reference voltages which depend on the peak voltage, and
  - a comparator circuit arranged to compare the pulse amplitude modulation signal against the plurality of reference voltages to detect an amplitude level.

15. The integrated circuit of claim **14**, further comprising:
- a transmitter which includes
  - a serializer arranged to convert a parallel data signal to a serial data signal,
  - a coder arranged to encode the serial data signal so as to generate a plurality of code bits, and
  - a driver arranged to use the plurality of code bits to generate a pulse amplitude modulation signal for transmission.

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