

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

AMPHENOL CORPORATION,
Petitioner,

v.

CREDO TECHNOLOGY GROUP LTD.,
Patent Owner

Case IPR2025-00835
U.S. Patent No. 10,877,233

PATENT OWNER'S REQUEST FOR DISCRETIONARY DENIAL

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LIST OF EXHIBITS

- Ex-2001 Order No. 6: Setting Procedural Schedule, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, issued May 19, 2025
- Ex-2002 September 1, 2023 Letter re Credo Technology Group, Ltd.’s Intellectual Property
- Ex-2003 USPTO, “FAQs for Interim Processes for PTAB Workload Management,” *available at* <https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management>
- Ex-2004 “Credo Introduces PAM4 DSP for High Performance Data Centers and Enterprise Networks,” March 17, 2021, <https://credosemi.com/credo-introduces-pam4-dsp-for-high-performance-data-centers-and-enterprise-networks/>
- Ex-2005 “AEC Applications,” <https://credosemi.com/products/hiwire-aec/applications/>
- Ex-2006 “Credo Introduces 800G HiWire ZeroFlap AECs to Support AI Backend Networks,” October 10, 2024, *available at* https://s205.q4cdn.com/511065572/files/doc_news/2024/10/credo-introduces-800g-hiwire-zeroflap-aecs-to-support-ai-backend-networks.pdf
- Ex-2007 Respondents’ Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025
- Ex-2008 Exhibit A-1, 233 Patent Invalidity Chart (Lugthart414), Respondents’ Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025

- Ex-2009 Exhibit A-2, 233 Patent Invalidity Chart (Lugthart431), Respondents' Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025
- Ex-2010 Exhibit A-4, 233 Patent Invalidity Chart (DS110DF111), Respondents' Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025
- Ex-2011 Exhibit A-5, 233 Patent Invalidity Chart (DS125DF410), Respondents' Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025
- Ex-2012 Exhibit A-6, 233 Patent Invalidity Chart (DS250DF410), Respondents' Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025
- Ex-2013 U.S. Pat. No. 10,148,414 ("Lugthart414")
- Ex-2014 Exhibit A-7, 233 Patent Invalidity Chart (DS250DF810), Respondents' Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025
- Ex-2015 Exhibit A-12, 233 Patent Invalidity Chart (Gorecki617), Respondents' Initial Invalidity Contentions, *In the Matter of Certain Active Electrical Cables and Components Thereof*, Inv. No. 337-TA-1446, served June 26, 2025
- Ex-2016 Bert Reiser & Ruthie Wu, Why the International Trade Commission is such an appealing forum for patent disputes," *Reuters* (June 11, 2025), <https://www.reuters.com/legal/legalindustry/why-international-trade-commission-is-such-an-appealing-forum-patent-disputes-2025-06-11/>

- Ex-2017 United States International Trade Commission, Section 337
Statistics: Average Length of Investigations, Updated
4/11/2025,
[https://www.usitc.gov/intellectual_property/337_statistics_aver
age_length_investigations.htm](https://www.usitc.gov/intellectual_property/337_statistics_average_length_investigations.htm)
- Ex-2018 Non-Final Office Action Dated September 9, 2020 issued in
Application No. 16/541,094
- Ex-2019 U.S. Pat. No. 9,337,993 (“Lugthart993”)
- Ex-2020 U.S. Pat. No. 7,401,985 (“Aronson985”)

I. INTRODUCTION

Credo is an American innovator. Its patented technologies power the next generation of energy-efficient data center interconnects. The subject patent of this IPR proceeding—U.S. Pat. No. 10,877,233 (“the ’233 patent”)—is one of three patents asserted in a pending Section 337 investigation before the International Trade Commission (ITC) (Inv. No. 337-TA-1446). These patents are not abstract ideas or litigation assets; they are the foundation of Credo’s HiWire® active electrical cable (AEC) products. The patents were obtained through careful and transparent examination by the Office. Credo is thereby asserting its patents rights after having built real products around this domestic innovation.

The ITC Investigation underscores the stakes associated with these patents and the urgency of their enforcement. Credo is seeking exclusionary relief to protect its core technology from infringement by competitors, including, among others, Petitioner Amphenol. This case is advancing quickly—the ITC has instituted the investigation and is proceeding toward an evidentiary hearing on the merits. Even under the most conservative timeline comparison, the Commission is expected to issue a Final Determination on October 15, 2026, **before** the Final Written Decision is expected on November 12, 2026 (“FWD Date”). The ITC will therefore have adjudicated validity of the subject patent before the PTAB reaches the FWD Date, resulting in judicial inefficiency. Meanwhile, the underlying legal

and factual issues before the ITC and the PTAB are the same. The patents are the same. The parties are the same. And the asserted prior art and challenged claims are virtually identical.¹ *Fintiv* therefore supports discretionary denial.

Beyond *Fintiv*, this proceeding presents precisely the situation the Office's leadership envisioned when the Stewart Memo² was issued in March 2025. That memo reaffirmed the Acting Director's authority to deny institution not only to prevent inefficient use of the Board's resources, but also to protect the integrity of the patent system as a whole. That integrity depends on the reasonable expectations of patent owners who play by the rules, prosecute diligently, disclose truthfully, and invest in commercialization.

Credo did all of this. It earned its patents under a well-functioning patent examination process before the Office. It also built a domestic industry around the

¹ Amphenol's preliminary invalidity contentions before the ITC include references with different patent numbers, but have near-identical disclosures to references included in its IPR grounds (each of which are similarly relied upon by Amphenol for addressing invalidity). See §IV.A.4, *infra* (addressing *Fintiv* factor 4).

² Memorandum to All PTAB Judges from Coke Morgan Stewart, Acting Secretary of Commerce for Intellectual Property, Regarding the Interim Processes for PTAB Workload Management (March 26, 2025) ("Stewart Memo").

patents. And now, it is using those patents productively in a good-faith enforcement campaign. Amphenol, for its part, is simply recycling the same pool of decade-old prior art—repackaged, recombined, and re-litigated—to gum up the gears of that enforcement effort.

This scenario is not what IPR was designed to enable. And it is what discretionary denial was designed to prevent. The PTAB’s resources are not appropriate to adjudicate issues the party seeking review (i.e., petitioner) sought to litigate elsewhere.³ The PTAB is a component of a balanced and efficient patent system, entrusted with the authority to decline review when institution would undermine—not promote—fairness, efficiency, and technological progress. Institution denial of the subject proceeding under § 314(a) advances these objectives and is necessary to protect the role of the PTAB as a partner in a functional U.S. patent system. Adoption of the bifurcated process reflects a clear policy shift toward protecting patent owner expectations and avoiding duplicative proceedings—precisely the situation presented here.

³ The issues before the ITC and the PTAB pertaining to the ’233 patent are nearly identical (same prior art, claims at-issue). Despite this overlap, Amphenol has not filed a stipulation or otherwise pursued any narrowing. See §IV.A.4, *infra* (addressing *Fintiv* factor 4).

II. CREDO'S PATENTED TECHNOLOGY

The application that issued as the '233 patent was filed on November 27, 2019, and issued on December 29, 2020. Credo is the original assignee and owner of the '233 patent. The patent was neither recently-acquired nor dormant. Instead, it arose directly from Credo's own research and development into active electrical cable (AEC) technology, i.e., high-speed Ethernet cables with integrated digital signal-processing electronics.

The '233 patent also protects Credo's AEC products. It embodies critical features of the AEC products that improve cable performance, such as advanced transmitter and receiver equalization, adaptive equalization, and retiming. *See* Ex-1035, 5-12⁴ (summarizing the technology and products at issue and the asserted patents).

The '233 patent is critically important to Credo by virtue of its protection of AEC products offered by Credo. These products have led to meaningful commercial uses, such "high-performance serial connectivity solutions for the Hyperscale data center, 5G carrier, enterprise networking, artificial intelligence, and high-performance computing markets." Ex-2004; *see also* Ex-2005 ("The

⁴ Unless otherwise indicated, citations to page numbers in this Request refer to page numbers specified in the corresponding document.

demand for cloud computing, instant data streaming, and emerging applications including 5G, AI, and machine learning have pushed Hyperscale, enterprise and edge data centers to accelerate the deployment of 400G and 800G networks”).

By 2024, Credo reported “millions of units” of AEC products deployed at tier-1 hyperscaler customers. *See* Ex-2006. The AEC products have won industry awards and play a significant role in modern data center architectures. *Id.* Credo’s senior VP of product noted that the company “invented AECs” based on years of engineering and has invested tens of millions of dollars developing this pioneering technology. *Id.* Credo’s long-term investment and active marketing underscore how these patents are central to Credo’s business, not idle paper patents. Indeed, Credo’s overall solutions portfolio explicitly includes AEC cables alongside its semiconductor integrated circuit (IC) products. Protecting these patented AEC innovations is strategically vital for Credo’s competitive position in high-speed connectivity.

III. LEGAL STANDARDS

A. Discretionary Denial Under 35 U.S.C. § 314(a)

Instituting or denying a petition under §314(a) “is a matter committed to the Patent Office’s discretion.” *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (under §314(a) “the PTO is permitted, but never compelled, to institute an

IPR proceeding”). In *NHK*, the Board used its discretion to deny institution under §314(a) because the parallel district court proceeding was scheduled to end before the FWD deadline and “Petitioner assert[ed] the same prior art and arguments” in that parallel proceeding. *NHK Spring Co Ltd v. Intri Plex Technologies Inc.*, IPR2018-00752, Pap. 8, at 19-20 (Sep. 10, 2019).

Fintiv articulated six factors (*infra* §V.A) to consider in determining whether to exercise discretion to deny institution based on a parallel district court or ITC proceeding. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Pap. 11, at 5-6 (Mar. 20, 2020) (“*Fintiv*”). The factors are evaluated by taking “a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Id.*

The Office has also made clear that “the Board will apply the *Fintiv* factors when there is a parallel proceeding at the International Trade Commission (‘ITC’).” Boalick Memo, at 2.⁵ Further, “the Board is more likely to deny institution where the ITC’s projected final determination date is earlier than the Board’s deadline to issue a final written decision...” *Id.*

⁵ Memorandum, Guidance on USPTO’s rescission of “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (Mar. 24, 2025), at 2 (“Boalick Memo”)

B. Recent USPTO Guidance

The Stewart Memo specified a bifurcated approach for considering discretionary denial, and further identified additional considerations for discretionary denial:

- Whether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims;
- Whether there have been changes in the law or new judicial precedent issued since issuance of the claims that may affect patentability;
- The strength of the unpatentability challenge;
- The extent of the petition’s reliance on expert testimony;
- Settled expectations of the parties, such as the length of time the claims have been in force;
- Compelling economic, public health, or national security interests; and
- Any other considerations bearing on the Director’s discretion

As explained below, denial is warranted under 35 U.S.C. § 314(a) based on these additional factors. Credo has developed settled expectations and yet there is no sufficient justification for institution. *See* §IV.B.1, *infra*. Furthermore,

Amphenol’s contentions in its Petition rely on expert testimony to gap-fill prior art disclosures in addressing limitation [1.f]. *See* §IV.B.2, *infra*. Thus, institution denial is appropriate under these circumstances to “improve PTAB efficiency,

maintain PTAB capacity to conduct AIA proceedings, . . . and promote consistent application of discretionary considerations in the institution of AIA proceedings.”

Stewart Memo, 3.

IV. DISCRETIONARY FACTORS FAVOR INSTITUTION DENIAL

A. The *Fintiv* Factors Weigh In Favor Of Discretionary Denial

The Petition should be denied institution because (i) at least factors 1-5 support discretionary denial; and (ii) the Petition does not provide a strong meritorious challenge (factor 6).

1. Factor 1—The ITC Investigation Will Not Be Stayed

No stay has been requested in the ITC investigation. And if one were, the stay is unlikely to be granted. Ex-2016, 2 (“discovery proceeds at a more expedited pace in the ALJ setting, and ITC proceedings are **rarely stayed**”) (emphasis added). The ITC is under a congressional mandate to conclude its investigations and make determinations “at the earliest practicable time.” 19 U.S.C. § 1337(b)(1). The ITC typically does not stay its proceedings based on a pending IPR.

2. Factor 2—The ITC’s Projected Final Determination Date Is Earlier Than the FWD Deadline

The projected statutory deadline for issuing a FWD in this proceeding is November 12, 2026 (“FWD Date”). By contrast, the Commission is expected to

issue a Final Determination on October 15, 2026. Thus, the ITC is scheduled to complete its investigation around 19 months after the March 13, 2025 filing date of the ITC complaint. This schedule is more conservative than the ITC's average length of investigations in the past 10 years. *See* Ex-2017 (average length for Fiscal Years 2014 to 2024 never reached 19 months). Further, in the first two quarters of Fiscal Year 2025 ("FY2025"), the average length of Section 337 investigations was 18.04 and 18.2 months, respectively, resulting in an average length of 18.12 months over the first half of 2025. *See* Ex-2017. Based on this average statistic for FY2025, the ITC Investigation would be expected to complete in September 2026—a month earlier than the scheduled completion date.

As such, it is unlikely that the FWD in this proceeding will issue before the ITC completes its investigation. *See Caihong Display Devices Co. Ltd v. Corning, Inc.*, IPR2025-00439, Pap. 18, at 2 (Jul. 10, 2025) ("*Caihong*") (finding that "it is unlikely that a final written decision in this proceeding will issue before the final determination in the ITC investigation" because "the projected final written decision due date for this proceeding is September 10, 2026" and "the target date for completion is August 7, 2026"); *see also* Boalick Memo, 2 ("[I]nstituting an IPR or a PGR where the ITC has set a target date for completing its investigation (i.e., the full Commission's final determination) to occur earlier than the Board's deadline to issue a final written decision in a challenge involving the same patent

claims means that multiple tribunals may be adjudicating validity at the same time, which may increase duplication and expenses for the parties and the tribunals”).

Fintiv factor 2 therefore weighs in favor of denial. *See Biofrontera Inc. v. Sun Pharmaceutical Industries, Inc.*, IPR2025-00287, Pap. 10 (Jul. 2, 2025) (Director discretionary decision denying institution based on a parallel ITC investigation scheduled to complete before FWD); *see also Ringconn LLC, v. Ouraring, Inc.*, PGR2025-00018, Pap. 11 (Jun. 25, 2025) (same); *see also Ultrahuman Healthcare SP LLC et al. v. Ouraring Inc.*, IPR2025-00411, Pap. 12 (Jun. 25, 2025) (same).

As discussed in §IV.A.4, *infra*, the ITC Investigation also presents overlapping issues with the IPRs, including Amphenol’s reliance on substantially the same prior art and arguments. Amphenol has not filed a stipulation or otherwise narrowed its invalidity positions before the ITC in a manner that prevents duplication. Thus, the Commission’s early resolution will directly address the asserted grounds of unpatentability in this proceeding. If the Board were to proceed, it would not be providing an efficient alternative to litigation but rather a second, duplicative review of issues already adjudicated.

3. *Factor 3—Fact Discovery And Expert Reports Will Complete Before A Decision On Institution*

Factor 3 weighs in favor of discretionary denial because the parties will have committed significant resources to the ITC Investigation by the time this

proceeding reaches a Decision on Institution (DI), and that investment will only increase materially if the proceeding progresses to a final written decision (by November 2026).

The deadline for issuing the DI is November 12, 2025. By that time, the parties to the ITC Investigation will have already: (i) exchanged proposed claim constructions (July 28, 2025), (ii) completed fact discovery (September 12, 2025), and (iii) exchanged initial expert reports (October 1, 2025) and rebuttal expert reports (October 31, 2025). Indeed, expert discovery will be complete by November 14, 2025—only two days after the expected DI. Ex-2001, 2.

In practical terms, the ITC investigation will be well past the halfway point and approaching expert discovery cut-off by the time the PTAB even considers institution. *Caihong*, at 2 (finding that “there has been meaningful investment” in a parallel ITC investigation because the parties will “have exchanged expert reports” and “complete fact discovery before a decision on institution is due”); *Arashi Visionus LLC v. GoPro Inc.*, IPR2025-00017, Pap. 11, at 11 (Apr. 28, 2025).

If this proceeding is instituted, the parties’ investment in the ITC Investigation will only materially increase by the FWD Date. The evidentiary hearing in the ITC Investigation is scheduled to be completed the week of January 20, 2026—over 10 months before the FWD. Ex-2001, 3. Further, an initial

determination in the ITC Investigation is scheduled to issue on June 15, 2026

(roughly five months before FWD) and the target date for completion of the ITC

Investigation is October 15, 2026 (roughly a month before FWD). Ex-2001, 2.

4. *Factor 4—Complete Overlap Exists Between The Petition And The ITC Investigation And Amphenol Has Not Stipulated Otherwise*

Amphenol relies on the same prior art disclosures to address the same claims of the '233 patent (claims 1-20) before the ITC and the PTAB. *Compare* Ex-2007, 48, *and* Pet., 2. This overlap is summarized in the table below with respect to prior art that Amphenol applies as primary references in each forum.

Preliminary Invalidity Contentions (ITC)			IPR Grounds (PTAB)		
Claims	Reference	Exhibit	Claims	Reference	Exhibit
1-20	Lugthart414	Ex-2013	1-20 (Grounds 1, 2)	Lugthart706	Ex-1005
1-5, 8-12, 14, 16-19	Gorecki617	Ex-1006	1-20 (Grounds 1, 2)	Gorecki617	Ex-1006
7, 14, 20	IEEE Std. 802.3-2015	Ex-1007- Ex1012	7, 14, 20 (Ground 2)	IEEE Std. 802.3-	Ex-1007- Ex1012

				2015	
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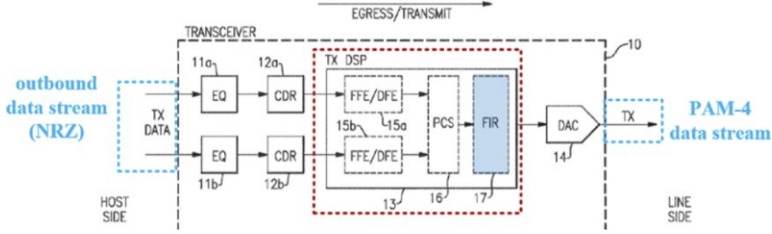
a) Amphenol Applied The Same Disclosure From Near-Identical Lugthart References Before The ITC And The PTAB

Amphenol applied U.S. Pat. No. 10,148,414 (Lugthart414; Ex-2013) in its preliminary invalidity contentions before the ITC, which has nearly-identical disclosures to U.S. Pat. No. 9,882,706 (Lugthart706; Ex-1005) applied in Grounds 1 and 2 of the Petition.

Lugthart414 and Lugthart706 have near-identical prior art disclosures. Each of their 32 figures are identical (FIGS. 1A-1D, 2A, 2B, 3A-3C, 4A, 4B, 5, 6A, 6B, 7A, 7B, 8, 9A, 9B, 10, 11, 12A, 12B, 13A-13C, 14-16, 17A, 17B, 18). And as to their written description, a side-by-side review confirms no meaningful difference in technical substance. Amphenol's contentions confirm this overlap, since they rely on the ***same disclosures*** found in each reference in addressing key claim limitations. Indeed, in addressing claim 1, Amphenol's invalidity contentions based on Lugthart414 and its IPR grounds based on Lugthart706 include the same 8 annotated figures. *Compare* Ex-2008, 2-14, *and* Pet., 19-35. To illustrate, below are excerpts from relevant portions of Amphenol's claim chart based on Lugthart414 (Ex-2008) and its Petition based on Lugthart706 (Ex-1005) addressing limitation [1.f]:

Amphenol's Preliminary Invalidity Contentions Based on Lugthart'414 in the ITC

1[f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in non-volatile memories.	Lugthart '414 discloses and/or renders obvious this limitation. Pre-Equalization Lugthart '414 discloses the subject matter of claim limitation 1[f] because the transceivers 107a/b of the combination provide “adaptive and configurable signal conditioning features such as... output pre-emphasis” on the TX signals transported by conductive lines 111 (e.g., electrical transit signals). <i>See, e.g.</i>, Lugthart '414 at 16:17-22, 23:64-24:7, 29:25-30, Figs. 1A, 2A. An ordinarily skilled artisan understood that “pre-emphasis” and “pre-equalization” have the same meaning. <i>See, e.g.</i>, U.S. Patent No. 8,787,430 at 2:39-41 (describing a “technique for combating ISI... known as ‘pre-emphasis’, or pre-equalization”); <i>see also</i> U.S. Patent No. 9,806,812 at 7:54-55; U.S. Patent No. 9,137,063 at 3:24-27; 9,152,257 at 5:4-8. Transceivers 107a/107b provide pre-equalization in DSP 13 using finite impulse response (FIR) filter 17. FIR filter 17 is a transmit filter because DAC 14 converts the FIR 17 output to an analog signal that is transmitted on the line side. <i>See, e.g.</i>, Lugthart '414 at 23:19-23, 23:64-24:7, Fig. 1A (annotated detail below).
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Claim 1	Lugthart '414
	 The FIR filter 17 “perform[s] emphasis on the signal to compensate for channel losses,” e.g., it pre-equaliz[es] the electrical transit signal. <i>See</i> Lugthart '414 at 23:67-24:2. The FIR filter 17 forwards conditioned signals to DAC 14 for transmission over cable 110 and conductive lines 111. <i>See, e.g., id.</i> at 8:23-26, 16:17-22, 23:64-24:7, Figs. 1A, 2A. The TX signals transmitted on the cable’s conductive lines are electrical transit signals. The FIR filter 17 tap coefficients are transmit filter coefficient values. The '233 Patent states that “equalization parameters may include filter coefficient values for pre-equalizer filters[.]” <i>See</i> '233 Patent at 5:45-48, 8:19-30 (during training adaptation adjusts filter coefficient values). Lugthart '414 explains that FIR filter 17 can be “a five tap FIR filter with tap coefficients S5.3, S7.3, S8.3, S7.3, S5.3” (<i>see</i> Lugthart '414 at 22:19-23). To the extent that this limitation is not disclosed, either explicitly or inherently, by Lugthart '414, this limitation is obvious to a person of ordinary skill in the art based on (1) Lugthart '414 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this limitation as detailed in the Cover Pleading, this Exhibit, and/or invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading or in this Exhibit.

Ex-2008, 13-14 (excerpted)

Amphenol's IPR Ground Based on Lugthart706 in the PTAB

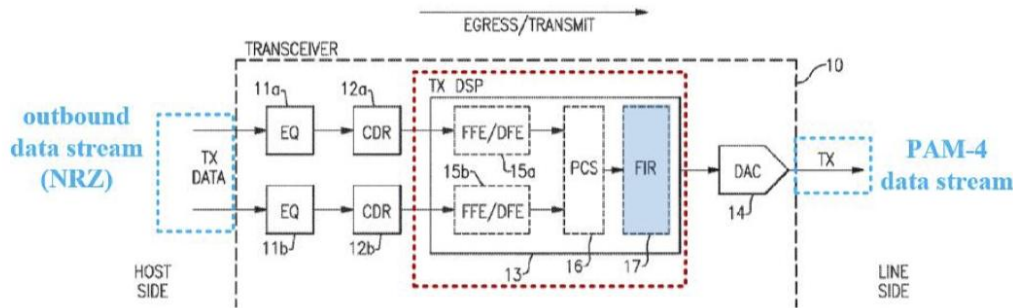
e. Limitation [1.f]

1.f	the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.
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i. pre-equalization

Lugthart+Gorecki meets [1.f] because Lugthart-706's transceivers 107a/b provide "adaptive and configurable signal conditioning features such as... ***output pre-emphasis***" on the TX signals transported by conductive lines 111 (e.g., *electrical transit signals, supra* §VI.D.1.c ([1.c])). Lugthart-706, Figs. 1A, 2A, 16:11-15, 23:59-24:2, 29:23-28; Min, ¶164. POSAs understood that "pre-emphasis" and "pre-equalization" have the same meaning. Min, ¶164; Raghavan, 2:39-41 (describing a "technique for combating ISI... known as 'pre-emphasis', or pre-equalization"); Schmidt, 7:54-55; Zerbe-063, 3:24-27; McCall, 5:4-8.

Transceivers 107a/107b provide pre-equalization in DSP 13 using finite impulse response (FIR) filter 17. FIR filter 17 is a *transmit filter* because DAC 14 converts the FIR 17 output to an analog signal that is transmitted on the line side. Lugthart-706, Fig. 1A (annotated detail below), 23:13-17, 23:59-24:2; Min, ¶165.



FIR filter 17 “perform[s] emphasis on the signal to compensate for channel losses,” e.g., it *pre-equaliz[es]* the *electrical transit signal*. Lugthart-706, 23:62-64; Min, ¶166. FIR filter 17 forwards conditioned signals to DAC 14 for transmission over cable 110 and conductive lines 111. Lugthart-706, Figs. 1A, 2A, 8:19-22, 16:11-15, 23:59-24:2; Min, ¶166. The TX signals transmitted on the cable’s conductive lines are *electrical transit signals*. Min, ¶166.

The filter 17 tap coefficients are *transmit filter coefficient values*. Min, ¶167. The ’233 Patent states that “equalization parameters may include filter coefficient values for pre-equalizer filters[.]” EX1001, 5:45-48, 8:15-26 (during training adaptation adjusts filter coefficient values); Min, ¶167. Lugthart-706 explains that FIR filter 17 can be “a five tap FIR filter with tap coefficients S5.3, S7.3, S8.3, S7.3, S5.3,” Lugthart-706, 22:12-16, while Gorecki-617 provides that “tap weights or coefficients (values) may be determined or controlled[.]” Gorecki-617, 6:56-57; Min, ¶167.

Pet., 33-34

As shown above, in addressing the “pre-equalization” recited in limitation [1.f], Amphenol relies on the same (1) identical annotated figure from Lugthart414 and

Lugthart706, (2) the same prior art disclosures (e.g., Lugthart414, 16:17-22, 12:64-24:7, 29:25-30, Figs. 1A, 2A; Lugthart706, 16:11-15, 23:59-24:2, 29:23-28, Figs. 1A, 2A), and (3) the same disclosed elements (e.g., transceivers 107a/b) within that disclosure. Examples of one of the cited portions of Lugthart414 and Lugthart706 are reproduced below:

In various implementations, the cable **110** of FIG. 2A and/or the cable **115** of FIG. 2B can include one or more electrical conducting lines **111** that can transport electrical signals between the first electronic device **101a** and the
15 second electronic device **101b**. However, the teachings herein are also applicable to other configurations, such as configurations in which data is communicated optically between transceivers.

In various implementations, the cable **110** of FIG. 2A and/or the cable **115** of FIG. 2B can include one or more
20 electrical conducting lines **111** that can transport electrical signals between the first electronic device **101a** and the second electronic device **101b**. However, the teachings herein are also applicable to other configurations, such as configurations in which data is communicated optically
25 between transceivers.

Ex-1005 (Lugthart706), 16:11-18 (left); Ex-2013 (Lugthart414), 16:17-25 (right)

Amphenol's strategy reflects a deliberate attempt to use prior art references with different patent numbers to avoid discretionary denial.

b) Amphenol Applied The Same Disclosure From Gorecki617 (Ex-1006) Before The ITC And The PTAB

Amphenol relied upon the same Gorecki617 reference (U.S. Pat. No. 7,233,617) before the ITC and the PTAB. See Ex-2015 (Exhibit A-12 to Amphenol's preliminary invalidity contentions, with invalidity contentions with respect to Gorecki617), 268-69, 299; Pet., 10-54 (IPR Ground based on Lugthart706-Gorecki617).

The overlap is further confirmed by Amphenol's reliance on the same prior art disclosure from Gorecki617 in its invalidity positions in each forum. In

addressing claim 1, Amphenol's invalidity contentions based on Gorecki617 and its IPR ground based on Gorecki617 each cite to disclosure in column 7, lines 18 to 33 relating to storage of information in ROM or EEPROM. *Compare* Ex-2015, 268-269, *and* Pet., 35. To illustrate, below are excerpts from relevant portions of Amphenol's claim chart based on Gorecki617 (Ex-2015) and its Petition based on Gorecki617 addressing limitation [1.f]:

Amphenol's Preliminary Invalidity Contentions Based on Gorecki617 in the ITC

	<i>U.S. Patent No. 7,233,617 to Gorecki</i> Gorecki discloses that “tap weights or coefficients (values) may be determined or controlled[.]” <i>See</i> Gorecki at 6:56-57. Gorecki discloses the storing of filter coefficient values in EEPROM, and use those values to set filter coefficients to provide pre-equalization. <i>See</i> Gorecki at 7:18-33 (“[I]nformation representative of... the coefficients of the tap(s)... may be stored... in... for example... ROM or EEPROM. In this way, the transmitter may access the memory to retrieve the necessary information during start-up/power-up, initialization or re-initialization.”). An EEPROM [electrically erasable programmable read-only memory] is non-volatile memory. <i>See, e.g.,</i> U.S. Patent App. Pub. No. 2015/0106536 at [0081] (“nonvolatile memory can include... electrically erasable PROM (EEPROM)”; U.S. Patent No. 8,000,176 at 2:53-54 (“EEPROM is a non-volatile memory”); U.S. Patent App. Pub. No. 2005/0013317 at [0012] (“non-
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INVESTIGATION NO. 337-TA-1446
RESPONDENTS' INITIAL INVALIDITY CONTENTIONS

– 268 –

Claim 1	Disclosure
	volatile memory may include... an EEPROM”). The L-G combination teaches programming the coefficients of the FIR filter 17 using the values stored in non-volatile EEPROM to pre-equalize the TX signal in transceiver 107a and 107b.

Ex-2015, 268-69

Amphenol's IPR Ground Based on Gorecki617 in the PTAB

ii. **non-volatile memory**

Lugthart+Gorecki uses Gorecki-617's teaching to store filter coefficient values in EEPROM, and use those values to set filter coefficients to provide pre-equalization. Gorecki-617, 7:18-33 (“[I]nformation representative of... *the coefficients of the tap(s)*... may be *stored... in... for example... ROM or EEPROM*. In this way, the transmitter *may access the memory to retrieve the necessary information* during start-up/power-up, initialization or re-initialization.”); Min, ¶168. An EEPROM [electrically erasable programmable read-only memory] is non-volatile memory. EX1051 (“Lauby”), [0081] (“nonvolatile memory can include... electrically erasable PROM (EEPROM)”); EX1032 (“Bakx”), 2:53-54 (“EEPROM is a non-volatile memory”); EX1047 (“Lindsay”), [0012] (“non-volatile memory may include... an EEPROM”); Min, ¶¶120, 168. Lugthart+Gorecki uses Gorecki-617's teaching to program filter 17 coefficients using the values stored in non-volatile EEPROM to pre-equalize the TX signal in transceiver 107a and 107b, thus meeting [1.f]. *Supra* §VI.C (combination); Min, ¶¶168-169.

Pet., 35

c) Amphenol Applied The Same Disclosure From The Same IEEE Std. 802.3-2015 Standard Before The ITC And The PTAB

Amphenol relied upon the same IEEE Std. 802.3-2015 standard before the ITC and the PTAB. See Ex-2015 (Exhibit A-12 to Amphenol's preliminary

invalidity contentions, with invalidity contentions with respect to IEEE Std. 802.3-2015), 497-98; Pet., 55-60 (IPR Ground based on Lugthart706-Gorecki617- IEEE Std. 802.3-2015).

The overlap is further confirmed by Amphenol's reliance on the same prior art disclosure from IEEE Std. 802.3-2015 in its invalidity positions in each forum. In addressing claim 7, Amphenol's invalidity contentions based on IEEE Std. 802.3-2015 and its IPR ground based on IEEE Std. 802.3-2015 include the same key disclosures. *Compare* Ex-2015, 497-98, *and* Pet., 59-60. To illustrate, below are excerpts from relevant portions of Amphenol's claim chart based on IEEE Std. 802.3-2015 and its Petition based on IEEE Std. 802.3-2015 addressing claim 7:

Amphenol's Preliminary Invalidity Contentions Based on IEEE Std. 802.3-2015 in the ITC

	<i>IEEE 802.3-2015</i> The IEEE 802.3-2015 standard discloses setting transmit filter coefficients to disable pre-equalization. As was known, an ordinarily skilled artisan would have disabled pre-equalization "if not needed to consume minimum power while satisfying the performance or margin objective" for a system. <i>See</i> U.S. Patent No. 9,137,063 to Zerbe at 27:24-37. Thus, for instances where signal transmission between host devices using the active cable meets performance objectives without pre-equalization of the multi-lane data streams provided to the first and second host interface ports, a user would disable those pre-equalization based on the IEEE 802.3-2015 standard.
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Claim 7	Disclosure
	72.6.10.3.4 Functions COEFF_UPDATE(coefficient, preset, initialize, inc, dec) Returns an updated coefficient based on the contents of the coefficient update field in the training frame. Sets a fixed coefficient value, or adds, or subtracts from the current coefficient value to create the updated coefficient. If multiple actions are requested in the coefficient update field, then the priority is: 1) preset 2) initialize 3) inc/dec Values: preset; If preset is TRUE then the function returns the coefficient value equivalent to no equalization [$c(-1)$ and $c(1)$ coefficients are set to zero, $c(0)$ set to maximum]. initialize; If initialize is TRUE, then the function returns the coefficient value such that the transmit output meets the conditions defined in 72.6.10.4.2. inc; If inc is TRUE then the function returns (coefficient + step). dec; If dec is TRUE then the function returns (coefficient – step). The requirements for the value of step are defined in 72.7.1.10 and Table 72–7. IEEE 802.3-2015, Section 5 at 480.

Ex-2009, 9

Amphenol’s IPR Ground Based on IEEE Std. 802.3-2015 in the PTAB

Lugthart+Gorecki+802.3 uses the 802.3 teaching to set transmit filter coefficients to disable pre-equalization. As was known in the art, a POSA would have disabled pre-equalization “if not needed to consume minimum power while satisfying the performance or margin objective” for a system. Zerbe-063, 27:24-37; Min, ¶249. Thus, for use-cases where signal transmission between host devices using the active cable meets performance objectives *without* FIR filters 27a/27b pre-equalizing the RX DATA signal transmitted into electronic device 101a/101b, a user would disable the pre-equalization at filters 27a/27b in Lugthart+Gorecki+802.3. *Supra* §VII.B (combination); Min, ¶249.

Pet., 59-60

d) Amphenol Has Not Narrowed Issues Between The PTAB
And The ITC

As explained above, Amphenol's invalidity theories in the ITC and the PTAB are identical. This results in inefficient use of judicial resources in each. And yet, Amphenol has taken no action to reduce this overlap. As of the filing of this request, Amphenol has not filed any stipulation with the ITC or otherwise narrowed the issues. *Fintiv* factor 4 therefore weighs in favor of discretionary denial.

Any effort by Amphenol to later narrow the issues would also be ineffective. Each of the IPR grounds in the Petition apply prior art that is included in Amphenol's invalidity contentions (Lugthart706, Gorecki617, IEEE Std. 802.3-2015). This duplication makes Amphenol's IPR grounds distinguishable from those implicated in *Samsung*, where institution was granted with a parallel ITC investigation. *See Samsung Electronics Co Ltd v. SiOnyx LLC*, IPR2024-01431, Pap. 21, at 14-16 (Apr. 10, 2025) ("*Samsung*"). There, institution was premised on the petitioner's withdrawal of specific IPR grounds raised before the ITC, thereby removing all overlap with the ITC Investigation. *Id.*, 14-15. In other words, in *Samsung*, institution was premised on the petitioner avoiding overlap by withdrawing IPR grounds from consideration by the ITC.

Finally, any stipulation subsequently submitted by Amphenol should be

deemed late. The Office has made clear that timely filing of a stipulation for consideration in discretionary denial briefing is one month from the Notice of Filing Date Accorded (NOFDA). In this instance, the NOFDA issued on May 12, 2025, which resulted in a stipulation deadline on June 12, 2025. Amphenol failed to file any stipulation by that date. Based on recent USPTO guidance, a stipulation should be filed “as soon as practicable, so that a patent owner may address the impact of the stipulation.” Ex-2003, 5. Amphenol chose not to pursue any stipulation as of the filing date of this request, foreclosing the opportunity for Credo to assess the impact on discretionary denial.

5. *Factor 5—Parties Involved In This IPR And The ITC Investigation Overlap*

Factor 5 weighs in favor of denying institution because the parties in the parallel litigation are the same. *See* Pet., x-xi; *Fintiv II*, 15 (“Because the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial.”).

6. *Factor 6—The Petition Fails To Demonstrate That One Or More of the Claims Are Unpatentable*

Factor 6 weighs in favor of denying institution because the merits of the Petition are weak. As will be explained in Patent Owner’s Preliminary Response

(POPR),⁶ the Petition fails to establish that the challenged claims would have been obvious over the various combinations of references in Grounds 1 and 2. Weak merits are further demonstrated by Amphenol’s over-reliance on expert testimony (*see* §IV.B.2, *infra*) and presentation of prior art analyses previously considered and deemed by the Examiner as not material to patentability (*see* §IV.C, *infra*), each of which establish distinct bases for discretionary denial.

B. Additional Factors Set Forth In The Stewart Memo Support Discretionary Denial

1. *Settled Expectations And Patent Maturity Further Reinforce Discretionary Denial*

While “there is no bright-line rule on when settled expectations become settled, in general, the longer the patent has been in force, the more settled expectations should be.” *Dabico Airport Solutions Inc v. HydraFacial LLC et al.*, IPR2025-00408, Pap. 21, at 3 (Jun. 18, 2025). Here, Credo has invested in, relied on, and commercialized the challenged patents for half a decade—destabilizing them now undercuts the certainty that the patent system is meant to foster. The

⁶ Credo asks the Acting Director to consider the merits briefing presented in the POPR when considering *Fintiv* factor 6. *See* Ex-2003, 7 (“when filing a brief for discretionary denial, a patent owner may direct attention to an anticipated POPR and evidence for a discussion of the merits.”)

challenged patents have been enforced and licensed as part of a publicly disclosed patent portfolio. *See* Ex-1035. As noted in §II, *supra*, claimed inventions in the '233 patent protect Credo's AEC products, which are relied upon by (a) customers, including major data center operators, and (b) domestic industry partners. *See* Ex-2004; Ex-2005; Ex-2006. The claims have also been unchallenged for more than four years, indicating market acceptance and long-term reliance.

Further, Amphenol's prior knowledge of the '233 patent, coupled with a failure to seek early review, is an independent ground for discretionary denial under §314(a). *See, e.g., iRhythm Inc et al. v. Welch Allyn Inc.*, IPR2025-00363, Pap. 10, at 2-3 (Jun. 6, 2025) ("*iRhythm*") (finding that "settled expectations favor denial of institution" because of "Petitioner's awareness of Patent Owner's applications and failure to seek early review of the patents").

Here, Amphenol was made aware of the '233 patent on September 1, 2023—more than a year prior to filing its Petition in April 2025. *See* Ex-2002. This lengthy delay undermines any claim of prejudice and strongly supports the denial of institution based on Credo's "settled expectations." In *iRhythm*, "discretionary denial of institution [was] appropriate" because Patent Owner's settled expectations were found to outweigh "[s]everal arguments weigh[ing] against discretionary denial, e.g., "that a final written decision [in the PTAB] proceeding will issue before the district court trial" (*Fintiv* factor 2), "little

investment by the parties in the district court proceeding” (*Fintiv* factor 3), and “a high likelihood of a stay if an *inter partes* review is instituted” (*Fintiv* factor 1). *iRhythm*, at 1. As explained in §IV.A, *supra*, the *Fintiv* factors are even more favorable such that there is no indication that Credo’s settled expectations are outweighed.

Further, Amphenol has not demonstrated why institution is justified. There is no persuasive reason the Board should now review the challenged claims of the ’233 patent. As discussed in §II, *infra*, this is not an instance where “a patent may have been in force for years but may not have been commercialized, asserted, marked, licensed, or otherwise applied in a petitioner’s particular technology space, if at all.” *Zepp Health Corp v. Slyde Analytics LLC*, IPR2025-00327, Pap. 12, 2-3 (Jun. 26, 2025). To the contrary, Credo expressly marked its rights and asserted the ’233 patent by providing Amphenol with actual notice of its infringement in September 2023. *See* Ex-2002. There is also no “significant change in law ... since the patent issued” and, thus, Amphenol cannot show “how [a] change in law directly bears on the patentability of the challenged claims.” *Id.* Thus, based on the absence of this information, the Office should be “disinclined to disturb” the settled expectations that Credo has developed for the ’233 patent. *Id.*, 3.

Finally, the ’233 patent also supports technology that helps decarbonize U.S.

infrastructure by reducing energy consumption. Weakening this patent through the PTAB, as pursued by Amphenol, serves no public purpose. *See* Ex-1001, 1:25-40. They also enable lower-power, lower-cost data centers (energy efficiency is a national priority). *See id.* Credo is a U.S.-based innovator asserting its patent rights. The ITC proceeding already promotes national trade policy and patent enforcement.

2. *Amphenol's Contentions For Limitation [1.f] Rely On Expert Testimony To Fill Gaps in Third Party Evidence*

Amphenol's IPR ground against claim 1 (Ground 1) relies on Gorecki617 to address limitation [1.f] of claim 1.⁷ *See* Pet., 35. And yet, Amphenol's contentions with respect to Gorecki617 in relation to limitation [1.f] (specifically, "transmit filter coefficient values stored in nonvolatile memories") reveal reliance on expert testimony to gap-fill prior art disclosures. Indeed, as will be explained in the POPR, the proposed combination of Lugthart706 and Gorecki617 fails to disclose or suggest limitation [1.f], rendering Amphenol's contentions substantively

⁷ This reliance creates a separate and distinct basis for discretionary denial under § 325(d) because the relied-upon disclosures from Lugthart706 were previously presented to the Office and specifically considered by the Examiner in original prosecution. *See* §IV.C, *infra*.

defective (beyond the type of expert testimony reliance that separately warrants institution denial).

More specifically, Amphenol effectively concedes the primary reference (Lugthart706) lacks express or inherent disclosure to satisfy the “transmit filter coefficient values stored in nonvolatile memories” recited in the limitation [1.f]. *See* Pet., 35. Amphenol is therefore forced to rely on a hypothetical configuration outside Lugthart706’s disclosure that, in its view, “uses Gorecki-617’s teaching to store filter coefficient values in EEPROM, and use those values to set filter coefficients to provide pre-equalization.” Pet., 35. Amphenol then purports that this hypothetical configuration satisfies limitation [1.f] because, according to Amphenol, the proposed combination “uses Gorecki-617’s teaching to program filter 17 coefficients using the values stored in non-volatile EEPROM to pre-equalize the TX signal in transceiver 107a and 107b.” *Id.* In other words, in attempting to address the elements recited in [1.f] (including the “filter coefficient values stored in nonvolatile memories”), Amphenol’s contentions fill gaps in Lugthart706’s disclosure by relying on expert testimony to combine functionality with Gorecki617. *Id.* This amounts to over-reliance because (1) Amphenol’s contentions fail to explain why “[a] POSA would have had reasons to configure the transmit filters of Lugthart-706 based on Gorecki-617’s approach of using coefficients stored in non-volatile memory” (Pet., 15), and (2) the corresponding

testimony from a declaration from Dr. Min (“Min Declaration”) merely parrots the arguments included in the Petition. As will be explained in greater detail in the forthcoming POPR, this reliance is also substantively defective since neither the Petition nor the Min Declaration sufficiently address how a POSITA would have relied upon the disclosures of third-party evidence (e.g., Lugthart706, Gorecki617) to arrive at the hypothetical configuration that Amphenol’s contentions require to achieve satisfaction of limitation [1.f].

Below is a chart showing a comparison of Amphenol’s contentions with respect to the “filter coefficient values stored in nonvolatile memories” recited in limitation [1.f] and declaration testimony from Dr. Min cited for evidentiary support:

Amphenol's Contentions (Pet., 35)	Cited Testimony From Min Declaration (Ex-1003, ¶¶68-69)
ii. non-volatile memory Lugthart+Gorecki uses Gorecki-617's teaching to store filter coefficient values in EEPROM, and use those values to set filter coefficients to provide pre-equalization. Gorecki-617, 7:18-33 ("[I]nformation representative of... <i>the coefficients of the tap(s)</i>... may be <i>stored</i>... <i>in... for example... ROM or EEPROM</i>. In this way, the transmitter <i>may access the memory to retrieve the necessary information</i> during start-up/power-up, initialization or re-initialization."); Min, ¶168. An EEPROM [electrically erasable programmable read-only memory] is non-volatile memory. EX1051 ("Lauby"), [0081] ("nonvolatile memory can include... electrically erasable PROM (EEPROM)"); EX1032 ("Bakx"), 2:53-54 ("EEPROM is a non-volatile memory"); EX1047 ("Lindsay"), [0012] ("non-volatile memory may include... an EEPROM"); Min, ¶¶120, 168. Lugthart+Gorecki uses Gorecki-617's teaching to program filter 17 coefficients using the values stored in non-volatile EEPROM to pre-equalize the TX signal in transceiver 107a and 107b, thus meeting [1.f]. <i>Supra</i> §VI.C (combination); Min, ¶¶168-169.	(2) non-volatile memory 168. Lugthart+Gorecki uses Gorecki-617's teaching to store filter coefficient values in non-volatile memory ("NVM"), which can include EEPROM and the like such as flash memory, and use those values to set filter coefficients to provide pre-equalization. Hsu-140, 3:42-4:2; Gorecki-617, 7:18-33 ("[I]nformation representative of... <i>the coefficients of the tap(s)</i> may be <i>stored</i>... <i>in... for example... ROM or EEPROM</i>. In this way, the transmitter <i>may access the memory to retrieve the necessary information</i> during start-up/power-up, initialization or re-initialization."); <i>supra</i> §VI.A.2 (discussing NVM as described in Gorecki-617). Lugthart+Gorecki uses Gorecki-617's teaching to program filter 17 coefficients using the values stored in NVM to pre-equalize the TX signal in transceiver 107a and 107b, thus meeting [1.f]. <i>Supra</i> §VI.A.3 (combination). 169. Thus, it is my opinion that Lugthart+Gorecki meets [1.f].

Tellingly, Amphenol's contentions for the "filter coefficient values stored in nonvolatile memories" of limitation [1.f] is limited to one page. *See* Pet., 35. As explained above, it cites to a single paragraph from Gorecki617 (7:18-33), and relies exclusively on testimony from the Min Declaration. The cited testimony also parrots the contentions in the Petition. For instance, like the Petition, paragraph 168 of the Min Declaration provides a conclusory allegation that the hypothetical configuration of Lugthart706 required to satisfy the "filter coefficient values stored in nonvolatile memories" of limitation [1.f] would have used "Gorecki-617's teaching to store filter coefficient values in non-volatile memory."

Ex-1003, ¶168.

To the extent that Amphenol argues its contentions for [1.f] incorporate-by-reference prior analysis regarding the proposed Lugthart706+Gorecki617 combination in Section VI.C of the Petition, its position still demands reliance on expert testimony. In that section of the Petition (Pet., 15-18), Amphenol contends “[a] POSA would have had reasons to configure the transmit filters of Lugthart-706 based on Gorecki-617’s approach of using coefficients stored in non-volatile memory.” Pet., 15.

That is, Amphenol’s reliance on the Lugthart706+Gorecki617 combination to address limitation [1.f] requires Gorecki617 to have disclosed storage of parameters in non-volatile memory and further suggested a configuration in which “the transmit filters of Lugthart-706” are specifically stored in its disclosed non-volatile memory. But the Petition fails to explain how Gorecki617 supports this proposition. Amphenol’s application of the Lugthart706+Gorecki617 combination to limitation [1.f] thereby requires reliance on expert testimony. And yet, the testimony cited in pages 15-18 of the Petition (i.e., paragraphs 124-131 of the Min Declaration) fails to substantiate key assertions, and in any event, largely parrots the analysis in the Petition. For example, paragraph 125 of the Min Declaration includes the following conclusory statement without any further analysis or explanation or corroboration with secondary evidence: “[a] POSA would have had

reasons to configure the transmit filters of Lugthart-706 based on Gorecki-617's approach of using coefficients stored in nonvolatile memory." Ex-1003, ¶125.

C. 35 U.S.C. § 325(d) Also Weighs In Favor of Discretionary Denial

Amphenol also relitigates the same issues that were resolved during original examination of the '233 patent—in particular, patentability of limitation [1.f], which the Examiner specifically deemed allowable over substantially the same prior art disclosures that Amphenol now applies in both grounds of its Petition.

Amphenol advances a single ground against claim 1:

Ground	References	Claims
1	Lugthart-706, Gorecki-617	1-6, 8-13, 15-19
2	Lugthart-706, Gorecki-617, IEEE Std. 802.3-2015	7, 14, 20

Pet., 4

As discussed below, each of the relied-upon disclosures from Lugthart706 were previously presented to, and considered by, the Examiner in original examination. Moreover, prior art disclosures from Gorecki617 relied upon by Amphenol are cumulative over other prior art considered by the examiner (e.g., Aronson985), leaving no other prior art disclosures to establish a “new” patentability analysis.

Amphenol also relies on Gorecki617 to remedy the defects of Lugthart706 with respect to limitation [1.f]. Amphenol admits the same, since it fails to cite to any teaching from Lugthart706 in addressing the “filter coefficient values stored in nonvolatile memories” in limitation [1.f]. Pet., 35. But, as explained in §IV.C.2(c)(2), *infra*, the cited portion of Gorecki617 applied to limitation [1.f] is analogous to disclosures previously presented to the Office during original examination.⁸

The Petition therefore fails to present a new patentability analysis with respect to limitation [1.f] that was not previously before the Office. Worse, it fails to identify with particularity how the cited portions of Gorecki617 sufficiently disclose limitation [1.f] or render it obvious, failing to meet Amphenol’s burden to demonstrate material error. Despite Amphenol’s arguments to the contrary, exercise of discretion under 325(d) is appropriate.

⁸ The “filter coefficient values stored in nonvolatile memories” was recited in original claim 1 (Ex-2001, 67) and identified by the Examiner to be allowable following consideration of prior art cited by the applicant in two IDS submissions (*see id.*, 113, 154). Thus, the file history reflects limitation [1.f] as having been material to patentability with respect to the prior art of record.

1. *Relevant Prosecution*

Prosecution of the application that issued as the '233 patent involved consideration of Lugthart706 (applied in all IPR grounds). As discussed in §IV.C.2, *infra*, Lugthart706 has the same underlying disclosure as U.S. Pat. No. 9,337,993 (“Lugthart993”), which was before the Office during original examination. Pet., 4 (identifying IPR grounds based on Lugthart706) and Ex-1002, 193 (IDS citing Non-Final Office Action issued in Application No. 16/541,094, which applied Lugthart993).

As to Gorecki617, Amphenol’s reliance on its disclosure is exclusively focused on limitation [1.f], which the file history demonstrates was deemed allowable over the prior art of record twice during original examination. Ex-1002, 113 (first Notice of Allowance), 154 (second Notice of Allowance). That is, Amphenol’s relied-upon disclosures from Gorecki617 for limitation [1.f] are cumulative over prior art previously considered—and dismissed—by the Examiner in relation to this limitation (i.e., Aronson985).

Further, the disclosures of Lugthart706 (relied upon in the Petition) and

Lugthart993 are largely identical.⁹ Unsurprisingly, Amphenol downplays the examiner's consideration of Lugthart993 because of its critical significance to the *Advanced Bionics* framework. This includes the following:

- Lugthart993 was presented to, and considered by, the Examiner via citation to a September 9, 2020 Non-Final Office Action issued in U.S. App. No. 16/541,094 (Ex-2018) (*see* Ex-2001, 166)
- Disclosure present in Lugthart993 is critical to Amphenol's invalidity theories because it is relied upon in both IPR grounds
- The file history confirms analysis by the Examiner yielded identification of claim features now recited in limitation [1.f] as to have resulted in allowance (Ex-1002, 113, 154)

Thus, presentation of Lugthart993 during original examination is pertinent to whether the analysis presented in the Petition was previously considered by the Office. And, it relates to the very limitation deemed allowable from that examination (limitation [1.f]).

⁹ Amphenol attempts to disqualify Lugthart993 as previously presented prior art because "Neither PO nor the Office made Lugthart-993 of-record." In doing so, Amphenol not only misunderstands 37 C.F.R. §1.98(a)(1) and MPEP 609.05(a), but misstates their relevance to 325(d). *See* §IV.C.2(b), *infra*.

In effect, Amphenol seeks to use the PTAB's resources to address an already-answered question: whether the prior art discloses or suggests elements recited limitation [1.f]. But the Examiner's patentability analysis already confirms that this disclosure is not material to the patentability of limitation [1.f]. And the Petition's cryptic reliance on its disclosure only confirms it.

Below is an overview of key milestones occurring during original examination:

Date	Event	Relevance	Excerpt from Ex-1002
11/27/2019	Applicant submits first IDS	Listed 8 documents, including U.S. Pat. No. 7,401,985 ("Aronson985")	6-8
10/15/2020	Examiner issues first Notice of Allowance	Indicated all original claims (claims 1-20) are allowable Emphasized the feature of "first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories" as not taught or suggested in the prior art of record. (Ex-1002, 113)	107-115
10/15/2020	Examiner indicates consideration of references cited in first IDS	Affirmative consideration of Aronson985 cited in first IDS	122-124
10/21/2020	Applicant submits second IDS	Listed 5 non-patent documents, including a Non-Final Office Action issued in Application No. 16/541,094 (which cited a single prior art	137-139

		reference, U.S. Pat. No. 9,337,993, or “Lugthart993”) (<i>see</i> Ex-2019)	
10/21/2020	Applicant files Request for Continued Examination (RCE)		134-135
11/2/2020	Examiner indicates consideration of references cited in second IDS	Affirmative consideration of Non-Final Office Action issued in App. No. 16/541,094 and Lugthart993 (<i>see</i> Ex-1002, 166; <i>see also</i> Ex-2019).	165-167
11/6/2020	Examiner issues second Notice of Allowance	Notice noted “[n]o change is seen from the notice of allowance issued October 15, 2020” (Ex-1002, 154) MPEP 2001.06(b) cited and noted “individuals covered by 37 CFR 1.56 cannot assume that the examiner of a particular application is necessarily aware of other applications which are ‘material to patentability’ of the application in question, but must instead bring such other applications to the attention of the examiner” (Ex-1002, 153) Further, the Notice noted “if a particular inventor has different applications pending which disclose similar subject matter but claim patentably indistinct inventions, the existence of other applications must be disclosed to the examiner of each of the involved applications.” <i>Id.</i> Moreover, “the prior art references from one application must be made of record in another subsequent application if such prior art	146-156

		references are ‘material to patentability’ of the subsequent application.” <i>Id.</i> (citing <i>Dayco Prod.</i> , 329 F.3d at 1369, 66 USPQ2d at 1808).	
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2. *Advanced Bionics, First Prong—Amphenol’s Relied-Upon Prior Art Disclosures Material To Patentability Were Previously Presented To The Office*

The first prong of *Advanced Bionics* is met because Amphenol’s relied-upon prior disclosures for addressing limitation [1.f] in Ground 1 were effectively previously presented to the Office during original examination. Specifically, Amphenol’s relied-upon prior disclosures from Lugthart706 is nearly identical to those from Lugthart933. Moreover, Amphenol’s relied-upon prior art disclosures from Gorecki617 are cumulative over those present in Aronson985. Thus, Amphenol’s proposed combination of Lugthart706 and Gorecki617 is not “new” because it relies on the same types of prior art disclosures to address the very limitation that resulted in allowance (i.e., limitation [1.f]).

a) A Signed IDS Represents Sufficient Prior Consideration For Satisfaction for *Advanced Bionics*, First Prong

As discussed below, the disclosures of Lugthart993 and Aronson985 were previously presented to the Office via IDS submissions by the applicant, which is relevant to the first prong of the *Advanced Bionics* framework. *Advanced Bionics*, 8 (explaining that previously presented prior art includes “art provided to the

Office by the applicant, such as **on an Information Disclosure Statement (IDS)**, in the prosecution history of the challenged patent”) (emphasis added); *see also Ecto World, LLC v. RAI Strategic Holdings, Inc.*, IPR2024-01280, Pap. 13, at 4 (May 19, 2025) (“*Ecto World*”) (precedential as to § A) (“[c]hallenging the claims using the same prior art that was previously presented on an IDS is sufficient to satisfy the first part of the *Advanced Bionics* framework”); *Ivantis, Inc. v. Sight Sciences, Inc.*, IPR2022-01530, Pap. 14, at 17 (Mar. 27, 2023) (“[T]here is no requirement that Examiner needs to rely on a reference in a rejection during prosecution in order for the reference to be ‘considered’ during prosecution.”).

Indeed, the Board has frequently held that a signed IDS is sufficient evidence to show consideration by the Examiner. *See, e.g., Palo Alto Networks, Inc. v. Centripetal Networks, Inc.*, IPR2021-01156, Pap. 10, at 13-14 (Jan. 24, 2022) (rejecting argument that “the first part of the *Advanced Bionics* framework is not met because [the prior art was] not substantively discussed or applied in a rejection during prosecution” because “[u]nder the Board’s precedent in *Advanced Bionics*, however, ‘[p]reviously presented art includes . . . art provided to the Office by an applicant, such as on an [IDS]’”) (quoting *Advanced Bionics* at 7-8) (alterations in original); *Eyenovia, Inc. v. Sydnexus*, IPR2022-00963, Pap. 7, at 10-11 (Nov. 8, 2022) (Because “references appear in the references cited section of the [challenged] patent and were identified in Information Disclosure Statements

(‘IDSs’) during prosecution[,] ... these references were ‘previously presented’ for the purposes of assessing the application of discretion under 35 U.S.C. § 325(d).”); *BMW of N. Am., LLC v. Stragent, LLC*, IPR2021-00419, Pap. 14, at 12-13 (July 19, 2021) (exercising discretion to deny institution under § 325(d) in part because relied-upon prior art was cited on an IDS), *reh’g denied*, Pap. 21, at 5 (Mar. 21, 2022); *Vovomart (HK) Enters. Co. v. Office Kick, Inc.*, PGR2022-00048, Pap. 14, at 9 (Jan. 12, 2013), *reh’g denied*, Pap. 16 (Mar. 9, 2023) (same); *Microsoft Corp. v. AlmondNet, Inc.*, IPR2022-01319, Pap. 9, at 8, 10 (Jan. 30, 2023) (same), POP request denied, Pap. 13 (Mar. 24, 2023), *reh’g denied*, Pap. 14 (Apr. 23, 2023).

As discussed in further detail below, the file history reveals that elements recited in limitation [1.f] led to allowance and that the Examiner considered prior art references cited on IDS submissions in relation to these elements. The Examiner’s evaluation reflects careful consideration (especially in view of the modest number of total references presented on each IDS reference).

b) Lugthart993 Was Previously Presented To The Office

Amphenol attempts to inoculate Lugthart706 from the *Advanced Bionics* framework by arguing a reference with nearly-identical disclosure—Lugthart933 (Ex-2019)—was not made “of-record.” Pet., 64 (fn 2) (citing 37 C.F.R. §1.98(a)(1) and MPEP 609.05(a)). This allegation is both factually and legally flawed.

(1) Amphenol Oversimplifies The File History

Amphenol overlooks the number of documents cited in the relevant IDS (“October 21, 2020 IDS”) and the number of prior art references applied in the relevant cited document—each of which suggest it was reasonable for the Examiner to have identified Lugthart993 and consider its disclosure as a result. The October 21, 2020 IDS cited a total of *five* documents, including a Non-Final Office Action issued in U.S. App. No. 16/541,094 (“the ’094 Office Action”). Ex-1002, 137-139. The ’094 Office Action included prior art rejections based on a *single* prior art reference, i.e., Lugthart993:

Application/Control Number: 16/541,094
Art Unit: 2633

Page 3

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

6. Claims 1-4, 14 and 15 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Lugthart et al. (US 9,337,993).

Ex-2018, 3

8. Claims 19-21 are rejected under 35 U.S.C. 103 as being unpatentable over Lugthart et al. (US 9,337,993).

Ex-2018, 8

Moreover, Lugthart993 was the only reference cited in the ’094 Office Action:

Notice of References Cited	Application/Control No. 16/541,094	Applicant(s)/Patent Under Reexamination LAM et al.	
	Examiner TED M WANG	Art Unit 2633	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9337993-B1	05-2016	Lugthart; Marcel Louis	H04L7/0054	1/1
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)

Notice of References Cited

Part of Paper No. 20200831

Ex-2018, 16

Thus, because the '094 Office Action was cited amongst five documents in the October 21, 2020 IDS and only applied Lugthart993, no excessive burden would have been placed on the Examiner in identifying and evaluating Lugthart993. Presentation of the '094 Office Action in the October 21, 2020 IDS therefore reflects presentation of Lugthart993 (i.e., the only prior art reference applied in the '094 Office Action). Indeed, it would have been reasonable for the Examiner to conclude that another examiner's analysis of Lugthart993 to similar claims of a co-pending application warrants separate consideration of Lugthart993.

Moreover, the manner in which the Examiner indicated consideration of references cited in the October 21, 2020 IDS further suggests awareness of Lugthart993. On November 2, 2020, the Examiner initialized each and every one of five references identified in the October 21, 2020 IDS:

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16698935
	Filing Date	2019-11-27
	First Named Inventor	Yifei DAI
	Art Unit	2883
	Examiner Name	Jordan, Andrew
	Attorney Docket Number	20160.0038.NPUS00

/AJ/	1	Ex Parte Quayle Action received March 11, 2020 for U.S. Application no. 16/539,910
/AJ/	2	Notice of Allowance received June 4, 2020 for U.S. Application no. 16/539,910
/AJ/	3	Restriction Requirement received May 1, 2020 for U.S. Application no. 16/541,094
/AJ/	4	Non Final Office Action received September 9, 2020 for U.S. Application no. 16/541,094
/AJ/	5	Notification of Reopening of Prosecution Due to Consideration of Information Disclosure Statement Filed After Mailing of a Notice of Allowance received October 5, 2020 for U.S. Application no. 16/539,910

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE	
Examiner Signature	/ANDREW JORDAN/ (11/02/2020)
Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Ex-1002, 166 (annotated)

There is no indication from the file history that the Examiner did not consider the substance of the documents cited in the October 21, 2020 IDS. To suggest otherwise, as Amphenol purports, runs contrary to the *Advanced Bionics* framework reflecting “a commitment to defer to previous Office evaluations of the

evidence of record unless material error is shown.” *Advanced Bionics*, 9. Indeed, as explained in §IV.C.3, *infra*, Amphenol fails to demonstrate material error to justify a lack of deference to the Examiner’s evaluation of the documents cited in the October 21, 2020 IDS.

Moreover, the file history demonstrates that the October 21, 2020 IDS was diligently submitted in relation to prosecution in co-pending applications. Applicant submitted the October 21, 2020 IDS after already receiving a first Notice of Allowance on October 15, 2020 (Ex-1002, 107-115), and after already submitting another IDS on November 27, 2019 (*id.*, 6-8). Further, the notification date of the ’094 Office Action is September 9, 2020, i.e., the ’094 Office Action issued within the intervening time frame of applicant’s first IDS submission (on November 27, 2019) and the Examiner’s first Notice of Allowance (on October 15, 2020). Ex-2018, 1. Despite this timing, Applicant made the Examiner aware of the ’094 Office Action in **six days** of the Notice of Allowance being issued. Unlike *Ecto World*, which implicated “applicant’s tacit refusal to identify references in response to the Examiner’s request,” the applicant here acted proactively to ensure the Examiner was made aware of documents potentially material to patentability. *Ecto World*, at 7.

(2) Amphenol's Allegations Regarding Lugthart993
Lack Legal Foundation

Amphenol's reliance on 37 C.F.R. §1.98(a)(1) and MPEP 609.05(a) to support its assertion that Lugthart993 was not made "of-record" is also misguided. To start, neither expressly support the broad proposition that a prior art reference cited in an Office Action cited on an IDS submission is not relevant to prior consideration of the prior art reference under the *Advanced Bionics* framework.

Instead, 37 C.F.R. §1.98(a)(1) (reproduced below) specifies the requirements for the contents of an IDS:

§ 1.98 Content of information disclosure statement.

CROSS REFERENCE

Link to an amendment published at [89 FR 92008](#), Nov. 20, 2024.

(a) Any information disclosure statement filed under § 1.97 shall include the items listed in paragraphs (a)(1) through (4) of this section.

(1) A list of all patents, publications, applications, or other information submitted for consideration by the Office. U.S. patents and U.S. patent application publications must be listed in a section separately from citations of other documents. Each page of the list must include:

(i) The application number of the application in which the information disclosure statement is being submitted;

(ii) A column that provides a space, next to each document to be considered, for the examiner's initials; and

(iii) A heading that clearly indicates that the list is an information disclosure statement.

See <https://www.ecfr.gov/current/title-37/chapter-I/subchapter-A/part-1/subpart-B/subject-group-ECFR2896c671410fb75/section-1.98>

Similarly, MPEP 609.05(a) offers guidance regarding recommended actions if a patent examiner believes information on an IDS submission is not compliant with

37 CFR 1.97 and 37 CFR 1.98. Under these circumstances, MPEP 609.05(a) provides the following guidance:

The examiner should write “not considered” on an information disclosure statement where none of the information listed complies with the requirements, e.g., the format requirements of 37 CFR 1.98(a)(1) are not met. If none of the information listed on a PTO/SB/08 form is considered, a diagonal line or “X” should also be drawn across the form and the form made of record in the application file. The examiner will inform applicant that the information has not been considered and the reasons why by using form paragraphs 6.49 through 6.49.10. If the improper citation appears as part of another paper, e.g., an amendment, which may be properly entered and considered, the portion of the paper which is proper for consideration will be considered.

Again, there is no indication from the file history of the '233 patent that the Examiner deemed the '094 Office Action to lack compliance with 37 C.F.R. §1.98(a)(1). The Examiner also provided no indication that the '094 Office Action was “not considered” based on the guidance specified in MPEP 609.05(a). As noted in the previous section, the Examiner instead indicated the opposite by initialing each of the five references cited on the October 21, 2020 IDS submission. This reflects affirmative consideration of the '094 Office Action (and, by extension, Lugthart993 as the only prior art reference applied within it). Ex-1002,

166. Amphenol's allegation that "[n]either PO nor the Office made Lugthart-993 of-record" plainly misapplies 37 C.F.R. §1.98(a)(1) and MPEP 609.05(a).

Ecto World further confirms this point. In this decision, the Acting Director clarified that § 325(d) warrants consideration of "the volume of the references submitted to the Office during examination and any application information or assistance regarding the relevance of reference." *Ecto World*, at 6-7. This comports with recognition in *Advanced Bionics* that "the question of whether proffered art or arguments are 'the same or substantially the same' as art or arguments previously presented to the Office is a **highly factual inquiry**." *Advanced Bionics*, at 7 (emphasis added).

As explained in the previous section, the facts, as reflected in the file history of the '233 patent, demonstrate that the Examiner could have reasonably identified Lugthart993 based on the corresponding citation to the Office Action in October 21, 2020 IDS submission. The October 21, 2020 IDS cited a total of **five references**, and the '094 Office Action applied Lugthart993 as the only prior art reference. Ex-1002, 166; *see also* Ex-2018, 16. This IDS submission is therefore "the size of a typical IDS," which "contain fewer than 25 references." *Ecto World*, 7 (fn 3). And, the IDS submission is also unlike the IDS submission at-issue in *Ecto World*, which was a "1000-reference IDS." *Id.*

c) Relied-Upon Prior Art Disclosures In Ground 1
(Lugthart706, Gorecki617) Were Previously Presented
To The Office

(1) Amphenol's Relied-Upon Disclosures from
Lugthart706 Are Nearly Identical to Lugthart7933

As discussed in §IV.C.2(b), *supra*, Lugthart993 was previously presented to the Office in original examination through citation of the '094 Office Action in the October 21, 2020 IDS. *See* Ex-1002, 166; *see also* Ex-2018, 16.

The disclosures of Lugthart706 (applied in Amphenol's IPR grounds) and Lugthart993 are largely identical in terms of technical substance. More importantly, every portion of the Lugthart706 disclosure that Amphenol cites to in addressing, for instance, claim 1 is literally present, word-for-word in Lugthart993. These relied-upon portions of Lugthart706 include 3:31-34, 6:65-67, 7:8-27, 8:8-60, 9:10-55, 13:13-57, 14:7-53, 15:42-52, 15:59-63, 16:11-20, 19:2-6, 22:12-16, 23:13-17, 23:59-24:2, 29:23-28, 30:23-55, 33:3-8, and Figures 1A-1D, 2A, 6A. *See* Pet., 19-35. And, as shown in the table below, each of these portions is literally present in Lugthart933:

Amphenol's Relied-Upon Disclosure From Lugthart706 (Ex-1005)	Corresponding Disclosure in Lugthart993 (Ex-2019)
According to an additional aspect, a communication device includes a host interface including at least two inputs for receiving signals from a host device at a total data rate of at least 40 Gbit/s. The communication device can further include host-side analog-to-digital converter (ADC) circuitry configured to digitize the received signals to generate at least two digital data channels each having a first data rate. The device can also include a digital signal processor configured to digitally condition the at least two digital data channels and multi-level encode the at least two digital data channels to generate a reduced number of one or more multiplexed digital data channels that each have a second data rate higher than the first data rate. The device may also include line-side digital-to-analog converter (DAC) circuitry configured to convert the multiplexed one or more digital data channels into one or more differential output signals. In addition, the device can include a line interface comprising one or more differential outputs each configured to transmit a corresponding one of the differential output signals onto corresponding paired differential cables. The egress path may be configured to deliver the one or more differential output signals onto the paired differential cables such that the line interface operates at a total data rate of at least 40 Gbit/s. 3:31-54	According to an additional aspect, a communication device includes a host interface including at least two inputs for receiving signals from a host device at a total data rate of at least 40 Gbit/s. The communication device can further include host-side analog-to-digital converter (ADC) circuitry configured to digitize the received signals to generate at least two digital data channels each having a first data rate. The device can also include a digital signal processor configured to digitally condition the at least two digital data channels and multi-level encode the at least two digital data channels to generate a reduced number of one or more multiplexed digital data channels that each have a second data rate higher than the first data rate. The device may also include line-side digital-to-analog converter (DAC) circuitry configured to convert the multiplexed one or more digital data channels into one or more differential output signals. In addition, the device can include a line interface comprising one or more differential outputs each configured to transmit a corresponding one of the differential output signals onto corresponding paired differential cables. The egress path may be configured to deliver the one or more differential output signals onto the paired differential cables such that the line interface operates at a total data rate of at least 40 Gbit/s. 3:22-44
65 A high-speed communication link can include a cable and a pair of transceivers provided at respective ends of the cable. The cable can be implemented in a wide variety of ways. For example, in certain configurations, the cable can correspond to an electrical cable including one or more pairs of differential micro coaxial cables or conductors. However, other configurations are possible, such as implementations in which the cable is implemented as an optical cable. 6:65-7:5	A high-speed communication link can include a cable and a pair of transceivers provided at respective ends of the cable. The cable can be implemented in a wide variety of ways. For example, in certain configurations, the cable can correspond to an electrical cable including one or more pairs of differential micro coaxial cables or conductors. However, other configurations are possible, such as implementations in which the cable is implemented as an optical cable. 6:51-58

In certain configurations, the transceivers can implement a serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable. The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the transceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts. 7:6-33	In certain configurations, the transceivers can implement a 60 serializer/deserializer (SerDes) function. For example, in certain implementations each transceiver can be a full duplex multiplexer and re-timer capable of receiving multiple (e.g., 2, 4, or more) signals from a host via a host-side interface. The transceiver multiplexes the received signals for transmission 65 via a line-side interface over the cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved via multi-level modulation encoding, for example. In one non-limiting embodiment, each transceiver is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission over the cable. The transceiver can also be configurable in different operational modes. For instance, depending on the mode, the transceiver can handle different numbers of host-side data streams having variable data rates. In one embodiment, the transceiver operates in a first operational mode to translate two host-side 10 20 Gbit/s NRZ data streams into a single PAM-4 40 Gbit/s stream on the line side, and vice versa. In a second operational mode, the transceiver translates four host-side 10 Gbps NRZ data streams into a single PAM-4 40 Gbit/s stream on the line-side, and vice versa. Such flexibility allows the trans- 15 ceiver to be employed in a variety of different contexts, such as in both consumer and data center contexts. 6:59-7:17
The transceiver 10 of FIG. 1A illustrates one example of a transceiver which can include one or more of the features disclosed herein. However, the teachings herein are applicable to other systems or apparatus, including, for example, other configurations of transceivers. As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA). 8:8-32	The transceiver 10 of FIG. 1A illustrates one example of a transceiver which can include one or more of the features disclosed herein. However, the teachings herein are applicable to other systems or apparatus, including, for example, other configurations of transceivers. As shown in FIG. 1A, the first and second transmit path equalizers 11a, 11b include inputs that receive host side transmit data (TX DATA) and outputs electrically connected to inputs of the first and second transmit path CDR circuits 12a, 12b, respectively. The first and second transmit path CDR circuits 12a, 12b further include outputs electrically connected to inputs of the transmit path DSP 13. The transmit path DAC 14 includes an input electrically connected to an output of the transmit path DSP 13 and an output that generates a line side transmit signal (TX). The receive path equalizer 21 includes an input that receives a line side receive signal (RX), and an output electrically connected to an input of the receive path CDR circuit 22. The receive path CDR circuit 22 further includes an output electrically connected to an input of the receive path DSP 23. The receive path DSP 23 further includes outputs electrically connected to inputs of the first and second receive path DACs 24a, 24b. The first and second receive path DACs 24a, 24b further include outputs that generate host side receive data (RX DATA). 7:63-8:14

The transceiver 10 can be used to support data transfer between various electronic devices, such as computing devices, storage devices, and/or peripheral devices. For example, the transceiver 10 can communicate with one or more additional transceivers using a wide variety of communications interface standards, including, for example, Thunderbolt Gen1/Gen2, USB 2.0/3.0, or IEEE 1394b. In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side. 8:33-60	The transceiver 10 can be used to support data transfer between various electronic devices, such as computing devices, storage devices, and/or peripheral devices. For example, the transceiver 10 can communicate with one or more additional transceivers using a wide variety of communications interface standards, including, for example, Thunderbolt Gen1/Gen2, USB 2.0/3.0, or IEEE 1394b. In certain configurations, the transceiver 10 can implement a serializer/deserializer (SerDes) function or operation. For example, in one embodiment, the transceiver 10 can operate as a full duplex multiplexer and re-timer capable of receiving multiple (for example, 2, 4, or more) signals from a host via a host-side interface. Additionally, the transceiver 10 can multiplex the received host-side transmit signals for transmission via a line-side interface over a cable utilizing a reduced number of channels. The multiplexing reduces cabling cost and complexity, and can be achieved, for example, via multi-level modulation encoding. In one non-limiting example, an egress/transmit path of the transceiver 10 is capable of receiving dual 20 Gbit/s non-return-to-zero (NRZ) signals on the host side and multiplexing these signals into a single 40 Gbit/s signal via four level pulse amplitude modulation (PAM-4) for transmission to the line side over the cable. Conversely, an ingress/receive path of the transceiver in such an example is capable of receiving a single 40 Gbit/s PAM-4 signal on the line side and de-multiplexing this signal into dual 20 Gbit/s NRZ signals for communication to the host side. 8:15-41
The receive path equalizer 21 can be used to provide signal equalization to compensate for transmission line losses on the line side, and the first and second transmit path equalizers 11a, 11b can be used to provide signal equalization to compensate for transmission line losses on the host side. For example, in certain implementations, an equalizer can be used to compensate for high-frequency signal loss by boosting high frequency components of a signal relative to low frequency components of the signal, thereby improving signal fidelity. In certain configurations, an equalizer can also be used for balancing amplitude and/or frequency characteristics associated with non-inverted and inverted components of a differential signal. In one embodiment, the transmit path equalizers 11a, 11b and/or the receive path equalizer 21 are implemented as continuous-time linear equalizers (CTLEs). The receive path CDR circuit 22 and the first and second transmit CDR circuits 12a, 12b can be used to perform clock and data recovery operations. For example, the receive path CDR circuit 22 can receive a data stream from the receive path equalizer 21, and can sample the data stream using a sampling clock signal. Additionally, the receive path CDR circuit 22 can control the sampling clock signal's frequency and phase to align the sampling clock signal relative to transitions in the data stream. Similarly, the first and second transmit path CDR circuits 12a, 12b can recover data in data streams generated by the first and second transmit path equalizers 11a, 11b, respectively. 9:10-37	The receive path equalizer 21 can be used to provide signal equalization to compensate for transmission line losses on the line side, and the first and second transmit path equalizers 11a, 11b can be used to provide signal equalization to compensate for transmission line losses on the host side. For example, in certain implementations, an equalizer can be used to compensate for high-frequency signal loss by boosting high frequency components of a signal relative to low frequency components of the signal, thereby improving signal fidelity. In certain configurations, an equalizer can also be used for balancing amplitude and/or frequency characteristics associated with non-inverted and inverted components of a differential signal. In one embodiment, the transmit path equalizers 11a, 11b and/or the receive path equalizer 21 are implemented as continuous-time linear equalizers (CTLEs). The receive path CDR circuit 22 and the first and second transmit CDR circuits 12a, 12b can be used to perform clock and data recovery operations. For example, the receive path CDR circuit 22 can receive a data stream from the receive path equalizer 21, and can sample the data stream using a sampling clock signal. Additionally, the receive path CDR circuit 22 can control the sampling clock signal's frequency and phase to align the sampling clock signal relative to transitions in the data stream. Similarly, the first and second transmit path CDR circuits 12a, 12b can recover data in data streams generated by the first and second transmit path equalizers 11a, 11b, respectively.

	8:58-9:18
The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible. The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.	The receive path DSP 23 can be used to process the data recovered by the receive path CDR circuit 22, and the transmit path DSP 13 can be used to process the data recovered by the first and second transmit path CDR circuits 12a, 12b. In the illustrated configuration, the receive path DSP 23 includes a feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 25, a physical coding sublayer (PCS) block 26, a first finite impulse response (FIR) filter 27a, and a second FIR filter 27b. Additionally, the transmit path DSP 13 includes a first FFE/DFE block 15a, a second FFE/DFE block 15b, a PCS block 16, and a FIR filter 17. Although one example of DSP blocks for receive path and transmit path DSPs has been provided, other configurations are possible. The illustrated receive path and transmit path DSPs can aid in conditioning and recovering received signals and in processing and generating signals associated with various communication interface standards or signaling protocols. For example, the transmit path DSP 13 can be used to filter and/or otherwise condition received signals, and to process and combine multiple recovered data streams to generate a serialized or multiplexed output signal having a desired modulation format. For example, in one embodiment, transmit path DSP 13 can filter or otherwise recover and condition the received signal, and to process the received signal to output a digital signal of a desired format or encoding, such as PAM-4, NRZ, duobinary, differential phase-shift keying (DPSK), and/or phase-shift keying (PSK). Additionally, the receive path DSP 23 can be used to process (for example, filter or otherwise recover and condition) data recovered by the receive path CDR circuit 22, and to deserialize the data to generate output signals having a desired modulation format for host side transmission.
9:38-10:3	9:19-51

Although FIGS. 1A-1D illustrate various examples of transceivers, the teachings herein are applicable to other systems or apparatus, including, for example, other configurations of transceivers. A wide variety of electrical and optical transceiver configurations supporting different data rates are possible. Here are some non-limiting examples:

- A 40 Gbit/s re-timer that re-times four host-side 10 Gbit/s NRZ lanes into four re-timed line-side 10 Gbit/s NRZ lanes.
- A 40 Gbit/s transceiver that multiplexes four host-side 10 Gbit/s NRZ lanes into a single 40 Gbit/s PAM-4 line-side lane.
- A 50 Gbit/s transceiver that multiplexes two 25 Gbit/s host-side NRZ lanes into a single PAM-4 50 Gbit/s line-side lane.
- A 100 Gbit/s transceiver that multiplexes four host-side 25 Gbit/s NRZ lanes into two 50 Gbit/s PAM-4 line-side lanes.
- A 100 Gbit/s transceiver that multiplexes four host-side 25 Gbit/s NRZ lanes into two 50 Gbit/s PAM-4 line-side lanes.
- A 100 Gbit/s transceiver that multiplexes four host-side 25 Gbit/s NRZ lanes into a single 100 Gbit/s PAM-4 line-side lanes.
- A 200 Gbit/s re-timer that re-times eight host-side 25 Gbit/s NRZ lanes into eight re-timed line-side 25 Gbit/s NRZ lanes.
- A 200 Gbit/s transceiver that multiplexes eight host-side 25 Gbit/s NRZ lanes into four 50 Gbit/s line-side PAM-4 lanes.
- A 400 Gbit/s transceiver that multiplexes sixteen 25 Gbit/s host-side NRZ lanes into eight 50 Gbit/s PAM-4 line-side lanes.
- A 400 Gbit/s transceiver that converts eight 50 Gbit/s PAM-4 host-side lanes into four 100 Gbit/s PAM-4 line-side lanes.

13:13-47

Although FIGS. 1A-1D illustrate various examples of transceivers, the teachings herein are applicable to other systems or apparatus, including, for example, other configurations of transceivers. A wide variety of electrical and optical transceiver configurations supporting different data rates are possible. Here are some non-limiting examples:

- A 40 Gbit/s re-timer that re-times four host-side 10 Gbit/s NRZ lanes into four re-timed line-side 10 Gbit/s NRZ lanes.
- A 40 Gbit/s transceiver that multiplexes four host-side 10 Gbit/s NRZ lanes into a single 40 Gbit/s PAM-4 line-side lane.
- A 50 Gbit/s transceiver that multiplexes two 25 Gbit/s host-side NRZ lanes into a single PAM-4 50 Gbit/s line-side lane.
- A 100 Gbit/s transceiver that multiplexes four host-side 25 Gbit/s NRZ lanes into two 50 Gbit/s PAM-4 line-side lanes.
- A 100 Gbit/s transceiver that multiplexes four host-side 25 Gbit/s NRZ lanes into two 50 Gbit/s PAM-4 line-side lanes.
- A 100 Gbit/s transceiver that multiplexes four host-side 25 Gbit/s NRZ lanes into a single 100 Gbit/s PAM-4 line-side lanes.
- A 200 Gbit/s re-timer that re-times eight host-side 25 Gbit/s NRZ lanes into eight re-timed line-side 25 Gbit/s NRZ lanes.
- A 200 Gbit/s transceiver that multiplexes eight host-side 25 Gbit/s NRZ lanes into four 50 Gbit/s line-side PAM-4 lanes.
- A 400 Gbit/s transceiver that multiplexes sixteen 25 Gbit/s host-side NRZ lanes into eight 50 Gbit/s PAM-4 line-side lanes.
- A 400 Gbit/s transceiver that converts eight 50 Gbit/s PAM-4 host-side lanes into four 100 Gbit/s PAM-4 line-side lanes.

12:56-13:24

While only the egress/transmit direction of data transmission is referred to in the above examples, it will be appreciated that the transceivers have both egress/transmit and ingress/receive paths. For instance, each of the transceivers described above as implementing a multiplexing function in the egress/transmit direction will be capable of performing a corresponding demultiplexing function in the ingress/receive direction to generate the appropriate number of host-side lanes, as described herein. Any of the above transceivers can be used to support either optical or electrical signal transmission. While the above examples are provided for the purposes of illustration, a wide variety of other configurations including those supporting additional data rates are possible. For instance, various implementations can be capable of operation at one or more of 20 Gbit/s, 25 Gbit/s, 28 Gbit/s, 32 Gbit/s, 40 Gbit/s, 50 Gbit/s, 56 Gbit/s, 64 Gbit/s, 100 Gbit/s, 112 Gbit/s, 128 Gbit/s, 200 Gbit/s, 224 Gbit/s, 256 Gbit/s, 400 Gbit/s, and 448 Gbit/s, and/or be capable of operation at data rates greater than any of these amounts, or rates between any of the foregoing rates. Listed data rates in some cases may correspond to effective payload data rates, not including certain overhead. For instance, a device with a listed data rate of 50 Gbit/s may actually be capable of a total data rate of 56 Gbit/s including 6 Gbit/s of overhead. 13:48-14:6	While only the egress/transmit direction of data transmission is referred to in the above examples, it will be appreciated that the transceivers have both egress/transmit and ingress/receive paths. For instance, each of the transceivers described above as implementing a multiplexing function in the egress/transmit direction will be capable of performing a corresponding demultiplexing function in the ingress/receive direction to generate the appropriate number of host-side lanes, as described herein. Any of the above transceivers can be used to support either optical or electrical signal transmission. While the above examples are provided for the purposes of illustration, a wide variety of other configurations including those supporting additional data rates are possible. For instance, various implementations can be capable of operation at one or more of 20 Gbit/s, 25 Gbit/s, 28 Gbit/s, 32 Gbit/s, 40 Gbit/s, 50 Gbit/s, 56 Gbit/s, 64 Gbit/s, 100 Gbit/s, 112 Gbit/s, 128 Gbit/s, 200 Gbit/s, 224 Gbit/s, 256 Gbit/s, 400 Gbit/s, and 448 Gbit/s, and/or be capable of operation at data rates greater than any of these amounts, or rates between any of the foregoing rates. Listed data rates in some cases may correspond to effective payload data rates, not including certain overhead. For instance, a device with a listed data rate of 50 Gbit/s may actually be capable of a total data rate of 56 Gbit/s including 6 Gbit/s of overhead. 13:25-48
FIG. 2A is a schematic diagram of a high-speed point-to-point communication system 100 according to one embodiment. The communication system 100 includes a first electronic device 101a and a second electronic device 101b electrically connected to one another via a cable 110. The communication system 100 of FIG. 2A illustrates an implementation of a high-speed communication link between first and second electronic devices 101a, 101b, which can also be referred to herein as host devices. In various implementations, the first and second electronic devices 101a and 101b can include one or more of a mobile computing device (e.g., a smart phone or a tablet), a personal computing device (e.g., a laptop, a desktop, a notebook), a workstation, a supercomputer, a peripheral device (e.g., a mouse, a keyboard, a joystick, a digital camera, a video camera, a webcam, a monitor, a display device, a speaker, a microphone, a printer, a scanner, a gaming system, an internet router, a hub, a network router, a port expansion device, an electronic switching device, a printed circuit board, a storage device (e.g., an external hard drive), an input/output interface device (e.g., read/write device, DVD player), a voice-over-IP device, etc. 14:7-28	FIG. 2A is a schematic diagram of a high-speed point-to-point communication system 100 according to one embodiment. The communication system 100 includes a first electronic device 101a and a second electronic device 101b electrically connected to one another via a cable 110. The communication system 100 of FIG. 2A illustrates an implementation of a high-speed communication link between first and second electronic devices 101a, 101b, which can also be referred to herein as host devices. In various implementations, the first and second electronic devices 101a and 101b can include one or more of a mobile computing device (e.g., a smart phone or a tablet), a personal computing device (e.g., a laptop, a desktop, a notebook), a workstation, a supercomputer, a peripheral device (e.g., a mouse, a keyboard, a joystick, a digital camera, a video camera, a webcam, a monitor, a display device, a speaker, a microphone, a printer, a scanner, a gaming system, an internet router, a hub, a network router, a port expansion device, an electronic switching device, a printed circuit board, a storage device (e.g., an external hard drive), an input/output interface device (e.g., read/write device, DVD player), a voice-over-IP device, etc. 13:49-14:2

FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111. Although FIG. 2A illustrates a configuration including the conductive lines 111, in other configurations the conductive lines 111 can be omitted in favor of communication using an optical cable. The first and second transceiver assemblies 105a, 105b can be implemented in a variety of ways. For example, the first and second transceiver assemblies include first and second transceivers 107a, 107b, respectively, which can be implemented using, for example, any of the embodiments of transceivers described earlier with respect to FIGS. 1A-1D. 14:29-53	FIG. 2A illustrates an embodiment in which the cable 110 is an active cable including actively powered componentry for improving performance of the cable 110. Thus, the cable 110 shown in FIG. 2A includes one or more conductive lines 111 as well as first and second transceiver assemblies 105a, 105b positioned at either end of the conductive lines 111. For example, the first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111. Additionally, the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111. Although FIG. 2A illustrates a configuration including the conductive lines 111, in other configurations the conductive lines 111 can be omitted in favor of communication using an optical cable. The first and second transceiver assemblies 105a, 105b can be implemented in a variety of ways. For example, the first and second transceiver assemblies include first and second transceivers 107a, 107b, respectively, which can be implemented using, for example, any of the embodiments of transceivers described earlier with respect to FIGS. 1A-1D. 14:3-26
In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP). 15:36-52	In various implementations, the packaging can have a design and a form factor similar to the packaging defined by an existing interface standard (e.g., Thunderbolt Gen1/Gen2 or USB 2.0/3.0), although the packaging can have some other form factor. The packaging can comprise materials suitable for electronic and computer interfaces, such as plastic, metal or a composite material. Each of the transceiver assemblies 105a and 105b has an input port that is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable. The input port can include a connector similar to connectors of existing interface standards, including, but not limited to, Thunderbolt, USB 2.0/3.0, small form-factor pluggable (SFP), enhanced small form-factor pluggable (SFP+), and/or quad small form-factor pluggable (QSFP). 15:8-23
More than two electronic devices (e.g., 3, 4, 5, 6, or more devices) can be daisy chained together in some cases through the use of additional cables and transceivers. In one such example, the first electronic device 101a is a laptop or other personal computer, the second electronic device 101b is a television or other display device, and a third electronic device is a disk drive or other storage device. The television has a second port (not shown) configured to accept a connector of a third transceiver (not shown). The third transceiver is connected via a second cable (not shown) to a port on the hard disk drive.	More than two electronic devices (e.g., 3, 4, 5, 6, or more devices) can be daisy chained together in some cases through the use of additional cables and transceivers. In one such example, the first electronic device 101a is a laptop or other personal computer, the second electronic device 101b is a television or other display device, and a third electronic device is a disk drive or other storage device. The television has a second port (not shown) configured to accept a connector of a third transceiver (not shown). The third transceiver is connected via a second cable (not shown) to a port on the hard disk drive.

15:53-63	15:24-34
In various implementations, the cable 110 of FIG. 2A and/or the cable 115 of FIG. 2B can include one or more electrical conducting lines 111 that can transport electrical signals between the first electronic device 101a and the second electronic device 101b. However, the teachings herein are also applicable to other configurations, such as configurations in which data is communicated optically between transceivers. The conducting lines 111 can include metal (e.g., copper) conductors, for example. In some implementations, the conducting lines 111 can alternatively or additionally include one or more other types of conductors, such as one or more optical fibers that can transport optical signals. As indicated, the conducting lines 111 in alternative embodiments are not housed within a cable, and can instead reside on a PCB or other substrate.	In various implementations, the cable 110 of FIG. 2A and/or the cable 115 of FIG. 2B can include one or more electrical conducting lines 111 that can transport electrical signals between the first electronic device 101a and the second electronic device 101b. However, the teachings herein are also applicable to other configurations, such as configurations in which data is communicated optically between transceivers. The conducting lines 111 can include metal (e.g., copper) conductors, for example. In some implementations, the conducting lines 111 can alternatively or additionally include one or more other types of conductors, such as one or more optical fibers that can transport optical signals. As indicated, the conducting lines 111 in alternative embodiments are not housed within a cable, and can instead reside on a PCB or other substrate.
16:11-26	15:48-63
Micro coaxial cables can exhibit relatively stable and reliable data transmission, support relatively high speeds, and have a relatively low-profile form factor as compared to other types of cabling. Other types of coaxial cables can have similar advantages and can be used in certain embodiments. For example, a cable can include twinaxial cables ("Twinax"), where each Twinax cable includes two inner conductors instead of a single inner conductor. In such cases, the two inner conductors can be configured to implement differential signaling.	Micro coaxial cables can exhibit relatively stable and reliable data transmission, support relatively high speeds, and have a relatively low-profile form factor as compared to other types of cabling. Other types of coaxial cables can have similar advantages and can be used in certain embodiments. For example, a cable can include twinaxial cables ("Twinax"), where each Twinax cable includes two inner conductors instead of a single inner conductor. In such cases, the two inner conductors can be configured to implement differential signaling.
18:65-19:6	18:31-40
In some arrangements, the recovered digital clock and data signals from the CDR circuits 12a-12b are input to the DSP 13 for further processing. The DSP 13 can include one or more digital filters (e.g., a finite impulse response (FIR) filter), one or more delay blocks, a feed-forward equalizer (FFE) and/or decision feedback equalizer (DFE) and/or one or more first-in-first-out (FIFO) buffers and can generally be configured to condition and multiplex the digital data signal to a multiplexed signal at a higher bit-rate than the bit-rate of the incoming differential signals. The DSP 13 can include one or more FIR filters (e.g., a five tap FIR filter with tap coefficients S5.3, S7.3, S8.3, S7.3, S5.3) to generate symbol sequence for the multiplexed signal corresponding to a desired modulation format.	In some arrangements, the recovered digital clock and data signals from the CDR circuits 12a-12b are input to the DSP 13 for further processing. The DSP 13 can include one or more digital filters (e.g., a finite impulse response (FIR) filter), one or more delay blocks, a feed-forward equalizer (FFE) and/or decision feedback equalizer (DFE) and/or one or more first-in-first-out (FIFO) buffers and can generally be configured to condition and multiplex the digital data signal to a multiplexed signal at a higher bit-rate than the bit-rate of the incoming differential signals. The DSP 13 can include one or more FIR filters (e.g., a five tap FIR filter with tap coefficients S5.3, S7.3, S8.3, S7.3, S5.3) to generate symbol sequence for the multiplexed signal corresponding to a desired modulation format.
22:3-17	21:33-46

In the illustrated configuration, the DSP 13 of the egress path includes a first feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 15a, a second FFE/DFE block 15b, a PCS block 16, and a finite impulse response (FIR) filter 17. Additionally, in the illustrated configuration, the DSP 23 in the ingress path includes an FFE/DFE block 25, a PCS block 26, a first FIR filter 27a, and a second FIR filter 27b. Thus, the DSP 23 can include componentry implementing similar functionality to the componentry in the egress path. 23:13-23	In the illustrated configuration, the DSP 13 of the egress path includes a first feed-forward equalizer and/or decision feedback equalizer (FFE/DFE) block 15a, a second FFE/DFE block 15b, a PCS block 16, and a finite impulse response (FIR) filter 17. Additionally, in the illustrated configuration, the DSP 23 in the ingress path includes an FFE/DFE block 25, a PCS block 26, a first FIR filter 27a, and a second FIR filter 27b. Thus, the DSP 23 can include componentry implementing similar functionality to the componentry in the egress path. 22:41-50
The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies. 23:59-24:2	The FIR filter 17 can include one or more finite impulse response (FIR) filters, and is generally configured to receive the multiplexed signal, condition the signal, and forward the processed signal to the DAC 14. For example, FIR filters can be used to perform emphasis on the signal to compensate for channel losses. Although illustrated as including the FIR filters, the DSP 13 can include additional processing componentry that can be used to further process signals. For example, the DSP 13 can be used to perform a de-emphasis function, e.g., to compensate for losses in the channel that are larger at certain (e.g., higher) frequencies. 23:20-30
Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC). 29:23-28	Various implementations of the transceiver can serve as a fully rate and channel adaptive transceiver for a wide range of signals from the electronic devices. Various implementations of the transceivers also include adaptive and configurable signal conditioning features such as an integrated continuous time linear equalizer (CTLE), output pre-emphasis, self-adaptive digital equalization, by-passable forward error correction (FEC). 28:40-47

20 FIG. 6A is a flowchart that illustrates an example method 300 of multiplexing at least two input analog differential signals received from an electronic device to a multiplexed analog differential signals. The method 300 includes receiving at least two input analog differential signals from an electronic device, as shown in block 301. The method 300 further includes converting each input analog differential signal to a digital signal, as shown in block 302. An analog to digital converter (ADC) can be used to convert the input analog differential signal to a digital signal. The method 300 further includes recovering digital clock and digital data signals from the converted digital signal, as shown in block 303. In various implementations, a first ADC is used to digitize the received data signal, and a second, lower resolution ADC is used for clock recovery. For instance, the second ADC may be at least a 2-bit ADC and the first ADC may be at least a 3-bit ADC. In various implementations the first ADC is at least a 6-bit ADC or is at least a 7-bit ADC. The method 300 further includes conditioning and multiplexing the digital data signal, as shown in block 304. The conditioning and multiplexing the data signal can be performed in the digital domain using digital signal processing. Programmable chip sets, physical coding sublayer (PCS) blocks, FPGAs, FIR filters can be used to condition and multiplex the digital data signal. As discussed above, conditioning the data signals can include equalizing the data signals to reduce the effects of ISI, framing, error correction, scrambling, etc. The method 300 includes converting the multiplexed digital signal to an analog differential signal having a suitable modulation format at a higher data rate than the input analog differential signal and output the multiplexed analog differential signal into a cable, as shown in block 305. The multiplexed analog differential signal can be an M-level pulse PAM signal (e.g., a 4-level PAM signal), an NRZ modulated signal or a signal with any other suitable modulation format. 30:20-55	FIG. 6A is a flowchart that illustrates an example method 300 of multiplexing at least two input analog differential signals received from an electronic device to a multiplexed analog differential signals. The method 300 includes receiving at least two input analog differential signals from an electronic device, as shown in block 301. The method 300 further includes converting each input analog differential signal to a digital signal, as shown in block 302. An analog to digital converter (ADC) can be used to convert the input analog differential signal to a digital signal. The method 300 further includes recovering digital clock and digital data signals from the converted digital signal, as shown in block 303. In various implementations, a first ADC is used to digitize the received data signal, and a second, lower resolution ADC is used for clock recovery. For instance, the second ADC may be at least a 2-bit ADC and the first ADC may be at least a 3-bit ADC. In various implementations the first ADC is at least a 6-bit ADC or is at least a 7-bit ADC. The method 300 further includes conditioning and multiplexing the digital data signal, as shown in block 304. The conditioning and multiplexing the data signal can be performed in the digital domain using digital signal processing. Programmable chip sets, physical coding sub-layer (PCS) blocks, FPGAs, FIR filters can be used to condition and multiplex the digital data signal. As discussed above, conditioning the data signals can include equalizing the data signals to reduce the effects of ISI, framing, error correction, scrambling, etc. The method 300 includes converting the multiplexed digital signal to an analog differential signal having a suitable modulation format at a higher data rate than the input analog differential signal and output the multiplexed analog differential signal into a cable, as shown in block 305. The multiplexed analog differential signal can be an M-level pulse PAM signal (e.g., a 4-level PAM signal), an NRZ modulated signal or a signal with any other suitable modulation format. 29:38-30:5
In some embodiments, the CDR circuit is included in a transceiver, such that the transceiver achieves relatively fast clock recovery with reduced latency. For example, the CDR circuits can operate in ingress paths and/or egress paths of the transceivers described herein. In one embodiment, a CDR circuit provides clock and data recovery to an input signal provide to the transceiver from a host device. In another embodiment, a CDR circuit provides clock and data recovery to an input signal received over a cable from another transceiver. 32:66-33:8	In some embodiments, the CDR circuit is included in a transceiver, such that the transceiver achieves relatively fast clock recovery with reduced latency. For example, the CDR circuits can operate in ingress paths and/or egress paths of the transceivers described herein. In one embodiment, a CDR circuit provides clock and data recovery to an input signal provide to the transceiver from a host device. In another embodiment, a CDR circuit provides clock and data recovery to an input signal received over a cable from another transceiver. 32:14-23

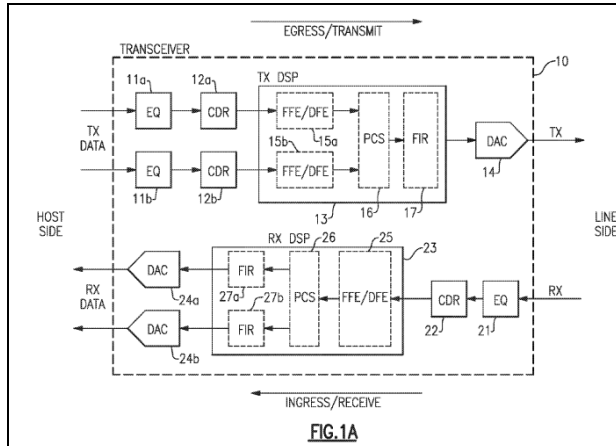


Figure 1A

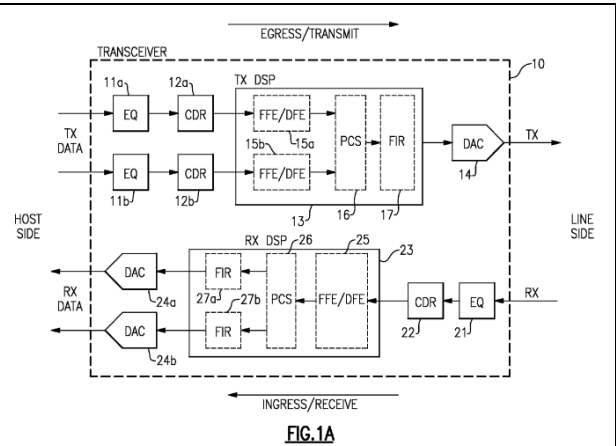


Figure 1A

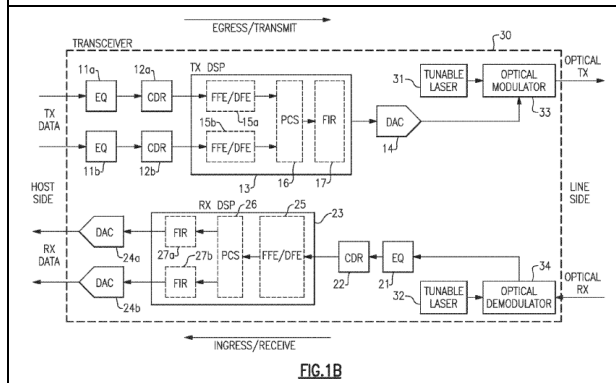


Figure 1B

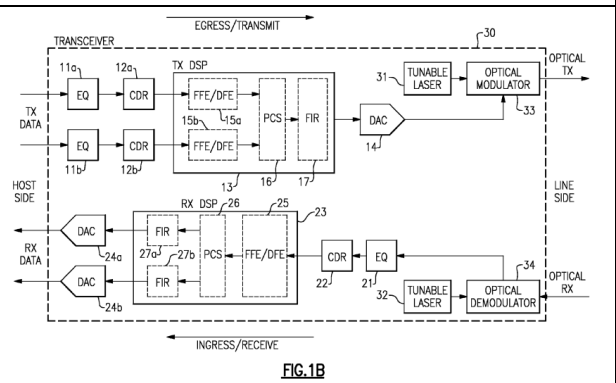


Figure 1B

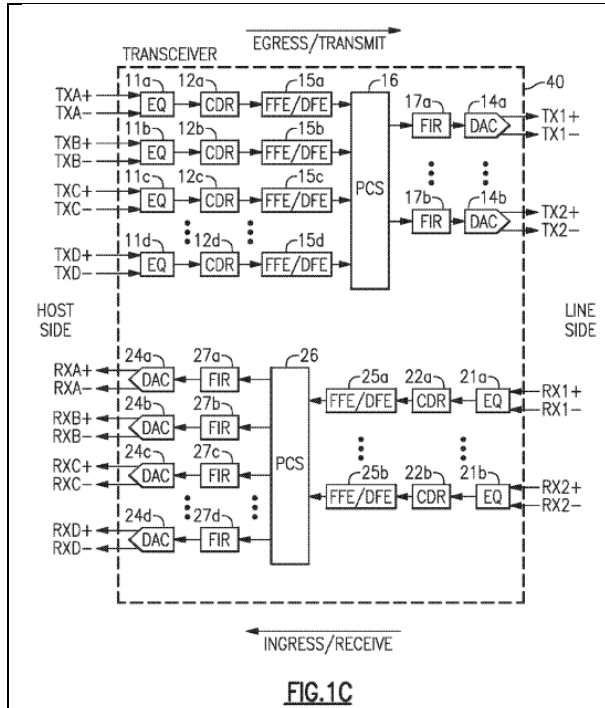


Figure 1C

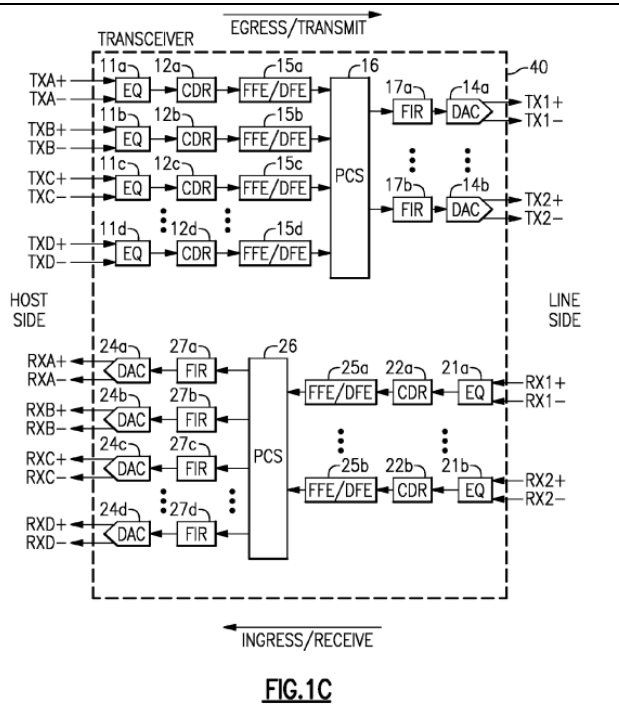


Figure 1C

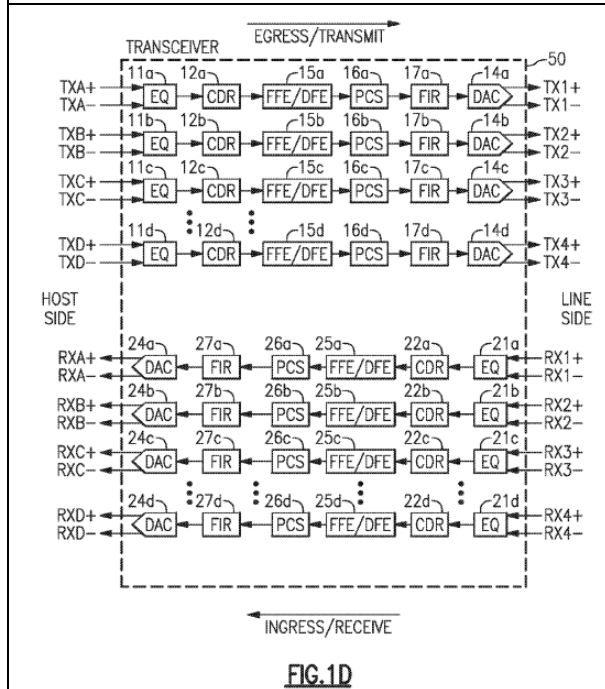


Figure 1D

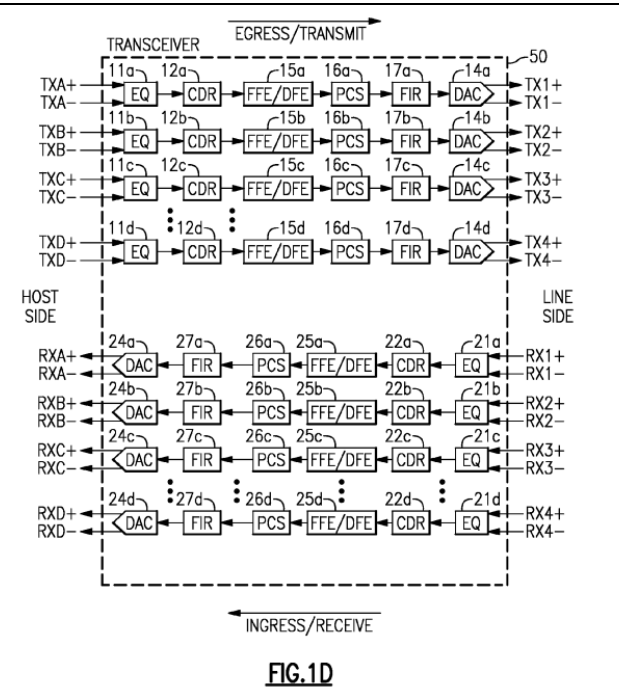


Figure 1D

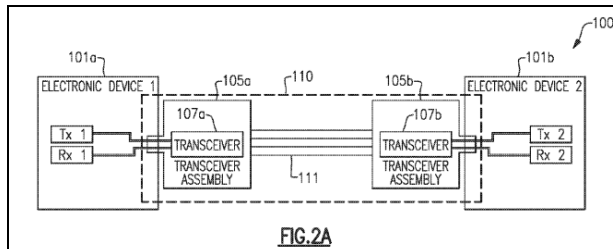


Figure 2A

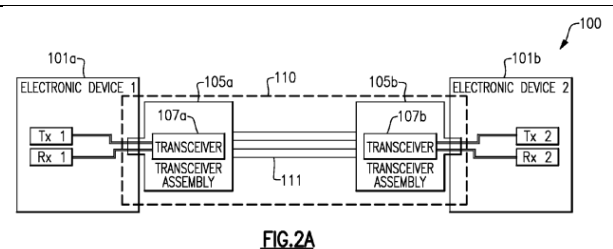


Figure 2A

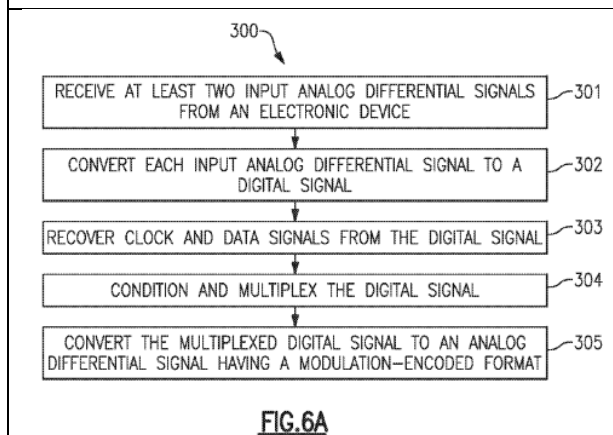


Figure 6A

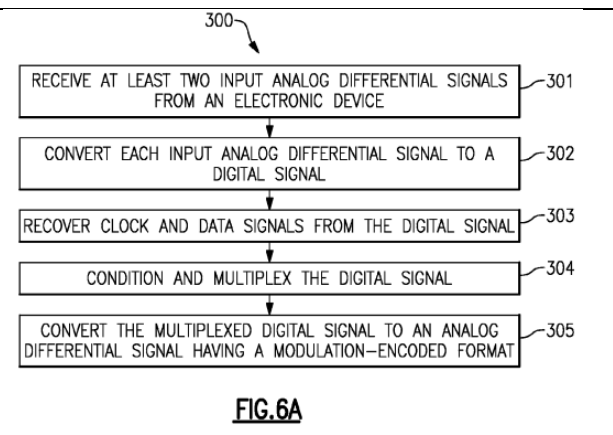


Figure 6A

Given the extensive similarity shown above, Amphenol's unsurprisingly asserts that "nothing in Lugthart-993 is relevant to the *Advanced Bionics* analysis." Pet., 64 (fn 8). Amphenol's reliance on Lugthart706 is a blatant attempt to avoid § 325(d).

(2) Amphenol's Relied-Upon Disclosures From
Gorecki617 Are Cumulative To Aronson985

While Gorecki617 itself was not cited in original examination, the disclosure relied upon by Amphenol to address limitation [1.f] is cumulative over other prior art disclosures previously considered in relation to this limitation. That disclosure

was presented to the Office in the form of Aronson985, which was cited in an IDS submission by the applicant on November 27, 2019 (Ex-1002, 6-8) and considered by the Examiner by October 15, 2020 (*id.*, 122-24). Following this consideration, the Examiner issued a first Notice of Allowance on October 15, 2020 emphasizing the features now recited in limitation [1.f]:

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

The prior art does not teach or suggest

first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories as set forth in the claimed combination of independent claim(s) 1, 8, and 15.

Applicant's other applications are seen as providing the closest prior art. However, while limited by the enabling disclosure of the specification as originally filed and the confines of teachings and substance therein, Applicant's active Ethernet cable appears to have elements new to the art.

Ex-1002, 113 (emphasis added)

After a second IDS submission on October 21, 2020, the Examiner issued a second Notice of Allowance finding the same features to be allowable over the prior art of record. Ex-1002, 154. Thus, the file history demonstrates that the Examiner found elements recited in limitation [1.f] (e.g., “transmit filter coefficient values stored in nonvolatile memories”) to be allowable over the prior art of record. The Examiner reached this finding subsequent to affirmative consideration of Aronson985. The

allowance thereby reflects evaluation of the Aronson985 disclosure in relation to elements recited in limitation [1.f] and a determination that the Aronson985 disclosure does not disclose or suggest these elements.

Amphenol's relied-upon disclosure from Gorecki617 are analogous to those from Aronson985 in terms of technical substance based on their relevance to limitation [1.f]. More importantly, the portion of Gorecki617 that Amphenol cites to in addressing limitation [1.f] (7:18-33) involves similar types of disclosures present in Aronson985 relating to EEPROM memory. *See Pet.*, 35. This is shown in the table below:

Amphenol's Relied-Upon Disclosure From Gorecki617 (Ex-1006)	Analogous Disclosure in Aronson985 (Ex-2020)
In another embodiment, the positions of the tap(s), the coefficients of the tap(s), and/or the pulse durations of the tap(s) may be pre-programmed or pre-set, for example, by permanently, semi-permanently or temporarily (i.e., until re-programmed) storing information which is representative of the positions of the tap(s), the coefficients of the tap(s), and/or the pulse durations of the tap(s) in an SRAM, DRAM, ROM, PROM, EPROM, EEPROM or the like (e.g., configuring the state of a certain pin or pins on the package). In this embodiment of the present invention, the information representative of the positions of the tap(s), the coefficients of the tap(s) and/or the pulse durations of the tap(s) may be stored or in, for example an SRAM, DRAM, ROM or EEPROM. In this way, the transmitter may access the memory to retrieve the necessary information during start-up/power-up, initialization or re-initialization. 7:18-33	The low speed serial data interface may be configured for use in control of the first electro-optical transducer, may be part of a system for the transmission of out of band data, may be configured to read or write data to nonvolatile memory in the optics portion of the cable, and/or may be used for one or more functions selected from the following list: serial identifier codes, customer security codes. Customer security codes could be provided to specifically allow only host qualified implementations of the cable and to detect outright counterfeit parts. Diagnostic information, which would be dynamically updated in volatile memory could be provided over the same serial interface. The serial interface may also be used for factory setup of the device to load non-volatile data to an internal EEPROM, FLASH memory or set of fusible links in the laser driver and/or receiver IC. The serial interface may be any serial interface, whether not existing (such as SPI interface or I2C interface) or whether to be developed in the future. 12:17-35 The amount of gain can be adjusted at factory setup individually to match the particular length of the characteristics of the copper cabling. 14:1-3

In practical terms, Amphenol relies on similar disclosures relating to EEPROM found in each reference, rendering the overlap highly relevant for § 325(d) purposes. Specifically, Aronson985 describes “factory setup of the [active] device to load non-volatile data to an internal EEPROM, FLASH memory ... in the laser driver and/or receiver IC,” where “[the device] provides preemphasis to the high frequency content of the transmitted signal to overcome the larger loss on the cable of these high frequencies.” Ex-2020, 12:29-31. Gorecki617 similarly describes “storing information” in an “EEPROM,” and Amphenol relies on this disclosure to address limitation [1.f]. *See* Pet., 35 (citing Gorecki617, 7:18-33).

Further, as discussed below, the Examiner’s lack of patentability rejections based on Aronson985 does not reflect material error. *See* §IV.C.3, *infra*. Rather, the lack of rejections represents a consistent pattern of the Examiner indicating the lack of relevance to the feature ultimately deemed allowable over the prior art of record—limitation [1.f].

(3) The Proposed Lugthart706+Gorecki617
Combination Does Not Justify Additional Review

As discussed above, the disclosures of each of Lugthart706 and Gorecki617 were previously-presented to the Office during original examination via consideration of Lugthart993 and Aronson985. In combining their teachings in Ground 1, Amphenol merely relies on Gorecki617 to remedy defects in

Lugthart706 with respect to the “filter coefficient values stored in nonvolatile memories” recited in limitation [1.f]. Specifically, according to Amphenol, “Lugthart+Gorecki uses Gorecki-617’s teaching to store filter coefficient values in EEPROM, and use those values to set filter coefficients to provide pre-equalization.” Pet., 35 (citing Gorecki617, 7:18-33). But, as explained in §IV.C.3(b)(2), *infra* (and more specifically in the POPR), Gorecki617 fails to disclose or suggest limitation [1.f], making Amphenol’s proposed Lugthart706+Gorecki617 combination not “new” to warrant further consideration by the PTAB.

3. *Advanced Bionics, Second Prong—Amphenol Failed To Demonstrate Material Error*

The second prong of *Advanced Bionics* is met because Amphenol fails to meet its burden in demonstrating material error. Like the petitioner in *Ecto World*, Amphenol relies on “generalized statements as to the strength of its Petition fail to identify sufficiently a material error.” *Ecto World*, 6. Indeed, the key citations within the single paragraph it devoted to addressing the *Advanced Bionics*, second prong are internal citations to other sections of the Petition. Pet., 66. (citing “§§IV.C, VI.D.1.e ([1.f]), VI.D.7.c ([8.f]), and VI.D.12.d ([15.c])” and “§§VI.D.1 (claim 1), VI.D.7 (claim 8), and VI.D.12 (claim 15)”). This lack of specificity effectively suggests “the Board should have scoured the Petition to cobble together

an argument under the second part of *Advanced Bionics*.” *Ecto World*, 6 (fn 2).

And, because Amphenol broadly concludes “the Examiner materially erred in allowing the Challenged Claims at least” without identifying the specific type of error, the Petition “improperly shift[ed] Petitioner’s burden to demonstrate material error onto the Board.” *Id.*

Moreover, to the extent that Amphenol contends that the Examiner materially erred based on not applying a reference cited on an IDS, the Petition fails to put forth the requisite analysis. *Ecto World*, 5 (clarifying that “a petitioner must provide an analysis even when the asserted prior art is on an IDS, but the Examiner did not apply the reference”). Specifically, the Petition was required to “explain, with reference to *Becton Dickinson* factors (c), (e), and (f), how the Examiner erred in overlooking the prior art.” *Id.* The Petition’s § 325(d) analysis failed to address *Becton Dickinson* factors (c), (e), and (f) entirely. *See Pet.*, 64-66.

Finally, Amphenol’s allegation that “Gorecki-617 teaches the subject matter in Limitations [1.f], [8.f], and [15.c] that the Examiner identified as missing in the prior art and a reason for allowance” is both procedurally and substantively defective. *See Pet.*, 66. On procedure, this allegation does not by itself establish that “no reasonable examiner could have found otherwise” (i.e., rejecting limitation [1.f] over the teachings of the prior art of record). *Ecto World*, 6; *see also Advanced Bionics*, 9 (“If reasonable minds can disagree regarding the purported

treatment of the art or arguments, it cannot be said that the Office erred in a manner material to patentability”). Because the Petition failed to address teachings of any of the prior art references cited in original examination, it similarly failed to demonstrate any material error.

On substance, as will be explained in greater detail in the POPR, the Petition’s analysis of limitation [1.f] also does not demonstrate material error, and Amphenol fails to explain how the Lugthart706-Gorecki617 combination satisfies its requirements. *See* Pet., 35. For instance, the combination involves teachings from divergent technologies—Lugthart706’s active cable systems and Gorecki617’s backplane environments—without any reasoned basis or motivation for the proposed combination. In particular, the Petition fails to address how Gorecki617’s backplane-based filter coefficients would be stored in a distributed, cable-based system where the transceivers are embedded and potentially inaccessible after manufacture. Nor does it account for the thermal, electrical, and mechanical constraints unique to active cables. These implementation differences raise questions regarding feasibility and operability. Notably, the Petition fails to address how a POSITA would have incorporated Gorecki617’s slower, static memory approach for a backplane environment into Lugthart706’s dynamic, active cable system.

V. CONCLUSION

For the reasons set forth above, Credo requests discretionary denial of the Petition.

Respectfully submitted,

Date: July 14, 2025

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24, the undersigned hereby certifies that the word count for the foregoing Patent Owner's Request for Discretionary Denial totals 9,283, which is less than the 14,000 limit.

Respectfully submitted,

Date: July 14, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e)(4), the undersigned certifies that on July 14, 2025, a complete and entire copy of this Patent Owner's Request for Discretionary Denial and all supporting exhibits were provided via email, to the Petitioner, by serving the correspondence address of record as follows:

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