UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

Before The Honorable Cameron R. Elliot
Administrative Law Judge

In the Matter of **CERTAIN ACTIVE ELECTRICAL CABLES AND COMPONENTS THEREOF**	**Investigation No. 337-TA-1446**

RESPONDENTS' INITIAL CONTENTIONS

CREDO 2007
Amphenol v. Credo
IPR2025-00835

TABLE OF CONTENTS

1. INTRODUCTION 1

2. LEGAL STANDARDS 3

35 U.S.C. § 101 3

Ineligible Subject Matter 3

Priority Date 5

Law of Anticipation 6

Law of Obviousness 7

35 U.S.C. § 112 10

Written Description and Enablement 10

Indefiniteness 11

3. RESPONDENTS' SOURCES OF INFORMATION REGARDING SECTION 101 ELIGIBILITY, SECTIONS 102-103 INVALIDITY, SECTION 112 INVALIDITY, AND UNENFORCEABILITY 12

4. THE '233 PATENT 14

Priority Date 14

Subject Matter Eligibility Grounds Under 35 U.S.C. § 101 14

Identification of Asserted Claims That Are Ineligible Under Section 101 16

Factual and Legal Basis for Subject Matter Ineligibility 18

All of the Asserted Claims Are Substantially Similar—Represented by Claim 1—for Purposes of Section 101 Analysis 43

Invalidity Grounds Under 35 U.S.C. §§ 102 and 103 47

Level of Ordinary Skill in the Art 55

Obviousness and Motivation to Combine 55

Secondary Considerations 94

Invalidity Grounds Under 35 U.S.C. § 112 94

Lack of Written Description and/or Enablement 95

Indefiniteness 96

Inequitable Conduct 102

Improper Inventorship 102

5. THE ’252 PATENT 103

Priority Date 103

Subject Matter Eligibility Grounds Under 35 U.S.C. § 101 103

Identification of Asserted Claims That Are Ineligible Under Section 101 105

Factual and Legal Basis for Subject Matter Ineligibility 107

All of the Asserted Claims Are Substantially Similar—Represented by Claim 1—for Purposes of Section 101 Analysis 130

Invalidity Grounds Under 35 U.S.C. §§ 102 and 103 133

Level of Ordinary Skill in the Art 139

Obviousness and Motivation to Combine 140

Secondary Considerations 268

Invalidity Grounds Under 35 U.S.C. § 112 268

Lack of Written Description and/or Enablement 269

Indefiniteness 271

Inequitable Conduct 275

Improper Inventorship 276

6. THE ’111 PATENT 276

Priority Date 276

Subject Matter Eligibility Grounds Under 35 U.S.C. § 101 277

Identification of Asserted Claims That Are Ineligible Under § 101 279

Factual and Legal Basis for Subject Matter Ineligibility 281

All of the Asserted Claims Are Substantially Similar—Represented by Claim 1—for Purposes of Section 101 Analysis 295

Invalidity Grounds Under 35 U.S.C. §§ 102 and 103 296

Level of Ordinary Skill in the Art 302

Obviousness and Motivation to Combine 303

Secondary Considerations 360

Invalidity Grounds Under 35 U.S.C. § 112 361

Lack of Written Description and/or Enablement 362

Indefiniteness 363

Inequitable Conduct 365

Improper Inventorship 366

7. CONCLUSION 367

Pursuant to Commission Rules 210.29 and 210.30, the ALJ's Ground Rules (Order No. 2), and the Procedural Schedule (Order No. 6), Respondents Amphenol Corporation ("Amphenol"), Molex, LLC ("Molex"), and TE Connectivity Corporation ("TE Connectivity") (collectively, "Respondents"), by and through their undersigned counsel, hereby submit the following Initial Contentions.

1. INTRODUCTION

These Initial Contentions, while based on diligent inquiry and investigation by Respondents, necessarily reflect only the current state of Respondents' knowledge, understanding, and belief based upon those facts and information presently and specifically known to Respondents at this time. Discovery is ongoing, the purported inventors have not yet been deposed, and Respondents have yet to receive Complainants' infringement and domestic industry technical prong contentions, including the manner in which Complainants purport to apply the limitations of the Asserted Claims to the Respondents' respective Accused Products. Respondents reserve the right to amend or supplement these Initial Contentions as discovery progresses including in response to, among other things, information learned in fact and/or expert discovery including identification of additional prior art, Complainants' positions on infringement, domestic industry technical prong, claim construction, and/or invalidity, the ALJ's rulings, and in the event Complainants are permitted to revise infringement or domestic industry theories.

These Initial Contentions address the following Asserted Claims (both for alleged infringement and technical domestic industry) of U.S. Patent No. 10,877,233 (the "'233 Patent"); U.S. Patent No. 11,012,252 (the "'252 Patent"); and U.S. Patent No. 11,032,111 (the "'111 Patent") (collectively, the "Asserted Patents"):

	Claims Asserted for Infringement	Claims Asserted for Domestic Industry
’233 Patent	1–20 (independent claims 1, 8, 15)	1–20 (independent claims 1, 8, 15)
’252 Patent	1–14 (independent claims 1, 6, 11)	1–14 (independent claims 1, 6, 11)
’111 Patent	1–19 (independent claims 1, 8, 11, 16)	1–19 (independent claims 1, 8, 11, 16)

Respondents’ Initial Contentions are not an admission that Respondents’ respective Accused Products or Complainants’ alleged domestic industry products are covered by any Asserted Claim or claim limitation. Complainants continue to have the burden of proof on infringement and domestic industry. To the extent that prior art cited for a particular limitation discloses functionality or structure that is the same or similar in some respects to the alleged functionality or structure of Respondents’ respective Accused Products that may be set forth in Complainants’ forthcoming infringement contentions or the domestic industry products that may be set forth in Complainants’ forthcoming domestic industry contentions, Respondents do not concede that those claim limitations are in fact met by those products.

Respondents are currently unaware of the extent, if any, to which Complainants will contend that the limitations of the Asserted Claims are not disclosed in the prior art identified by Respondents. To the extent that Complainants make such contentions, Respondents may identify and rely on other prior art.

Further, discovery is still underway, witnesses remain to be deposed, and claim construction exchanges have not yet taken place. Respondents’ Initial Contentions may thus be modified, amended, and/or supplemented in accordance with the Ground Rules (Order No. 2), the Procedural Schedule in this Investigation (Order No. 6), pursuant to 19 C.F.R. § 210.27(f), in response to Complainants’ validity contentions and any supplements or amendments thereto, based

on Respondents' further investigation, or as may be warranted in light of ongoing discovery. To the extent positions are provided herein in the alternative or under multiple constructions, those positions should not be construed as an admission that such construction is proper.

Respondents maintain their contentions that certain claim terms are indefinite, as noted below for each Asserted Patent. For purposes of these Initial Contentions only, however, Respondents' attached Appendices treat such claim terms as not indefinite. Respondents do not waive any contention regarding indefiniteness by proceeding in this manner.

Citations in these contentions to the first page of a produced document that comprises multiple pages constitute a citation to the entire document.

2. LEGAL STANDARDS

35 U.S.C. § 101

Ineligible Subject Matter

Section 101 lists four broad categories of patent-eligible subject matter but is subject to "an important implicit exception" that "[l]aws of nature, natural phenomena, and abstract ideas," which form the "basic tools of scientific and technological work," are not eligible for patent protection. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 573 U.S. 208, 216 (2014) (internal quotation marks omitted). "The 'abstract ideas' category embodies 'the longstanding rule that an idea of itself is not patentable.'" *Id.* at 209 (quoting *Gottschalk v. Benso*n, 409 U.S. 63, 67 (1972) (quoting *Rubber-Tip Pencil Co. v. Howard*, 87 U.S. 498 (1874)). "[M]erely presenting the results of abstract processes of collecting and analyzing information, without more (such as identifying a particular tool for presentation), is abstract as an ancillary part of such collection and analysis." *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1354 (Fed. Cir. 2016).

Alice set forth a two-step inquiry. "First, we determine whether the ***claims*** at issue are directed to one of those patent-ineligible concepts." *Id.* at 217 (emphasis added). In making this inquiry, the claims "must be considered as a whole." *Alice*, 573 U.S. at 218 n.3 (quoting *Diamond v. Diehr*, 450 U.S. 175, 188 (1981)). Section 101 is supposed to "prevent patenting of claims that abstractly cover results where 'it matters not by what process or machinery the result is accomplished.'" *McRo Inc. v. Bandai Namco Games Am. Inc.*, 837 F.3d 1299, 1312 (Fed. Cir. 2016). In analyzing step one, courts consider "whether the claims in the patent focus on a specific means or method, or are instead directed to a result or effect that itself is the abstract idea and merely invokes generic process and machinery." *Two-Way Media Ltd. v. Comcast Cable Commc'ns, LLC*, 874 F.3d 1329, 1337 (Fed. Cir. 2017); *see also Free Stream Media Corp. v. Alphonso Inc.*, 996 F.3d 1355, 1363 (Fed. Cir. 2021).

If the claims recite an abstract idea, the second step requires a "search for an 'inventive concept'—an element or combination of elements that is 'sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the [ineligible concept] itself.'" *Id.* at 218 (quoting *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 566 U.S. 66, 73 (2016)). "A claim that recites an abstract idea must include 'additional features' to ensure 'that the claim is more than a drafting effort designed to monopolize the abstract idea.'" *Id.* at 221 (quoting *Mayo*, 566 U.S. at 78) (alterations omitted). The recited "additional features must be more than well-understood, routine, conventional activity." *Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 1335, 1339 (Fed. Cir. 2013) (internal quotations omitted).

Application of an abstract idea using "conventional and well understood techniques" does not "supply an inventive concept." *BSG Tech. LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1290–91 (Fed. Cir. 2018); *see also Baggage Airline Guest Servs., Inc. v. Roadie. Inc.,* 351 F. Supp. 3d 753,

761 (D. Del. 2019), *aff'd*, 2019 WL 5703890 (Fed. Cir. Nov. 5, 2019) (finding that "reciting generic computer functions and the use of generic computer elements to achieve a more efficient way of 'coordinating and monitoring baggage delivery'" is not an inventive concept). A "critical difference" exists between "patenting a particular concrete solution to a problem" and "attempting to patent the abstract idea of a solution to the problem in general," because the overbroad functional claiming of the latter "purport[s] to monopolize every potential solution to the problem." *BSG*, 899 F.3d at 1290–91. Further, claims are subject matter ineligible if "[w]hat is claimed is simply a generic environment in which to carry out the abstract idea." *Yu v. Apple Inc.*, 1 F.4th 1040, 1043 (Fed. Cir. 2021).

Priority Date

Complainant bears the burden of proving its claims are entitled to the asserted priority date. For a patent to claim priority from the filing date of its provisional application, it must satisfy 35 U.S.C. § 119(e)(1), which requires that the written description of the provisional adequately support the claims of the non-provisional application. *New Railhead Mfg., L.L.C. v. Vermeer Mfg. Co.*, 298 F.3d 1290, 1294 (Fed. Cir. 2002); 35 U.S.C. § 119(e)(1) (2006) ("An application for patent filed under section 111(a) or section 363 of this title for an invention ***disclosed in the manner provided by the first paragraph of section 112*** of this title in a provisional application filed under section 111(b) of this title, by an inventor or inventors named in the provisional application, shall have the same effect, as to such invention, as though filed on the date of the provisional application filed under section 111(b) of this title[.]") (emphases added). "In other words, the specification of the *provisional* must 'contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms,' 35 U.S.C. § 112 ¶ 1, to enable an ordinarily skilled artisan to practice the invention *claimed* in the

non-provisional application." *New Railhead Mfg.*, 298 F.3d at 1294 (emphases in original); *see also Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The purpose of the written description requirement is broader than to merely explain how to "make and use;" the applicant must also convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention. That is, the disclosure must show he had invented each feature that is included as a claim limitation. The adequacy of the written description (*i.e.*, the disclosure) is measured from the face of the application, and the written description requirement is not satisfied if one of ordinary skill in the art must first make the patented invention before he can ascertain the claimed features of that invention. *New Railhead Mfg.*, 298 F.3d at 1295.

Law of Anticipation

A patent claim is anticipated if each and every element of the claim was disclosed in a single prior art reference. *See SRI Int'l, Inc. v. Internet Sec. Sys., Inc.*, 511 F.3d 1186, 1192 (Fed. Cir. 2008) ("A [patent] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.").

To be anticipated, each element of a patent claim may be disclosed by a prior art reference either expressly or inherently. *SRI*, 511 F.3d at 1192. An element of a patent claim is inherent in a prior art reference if the element must necessarily be present. *See Schering Corp. v. Geneva Pharms.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003) ("[A] prior art reference may anticipate without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference…. [A] court may consult artisans of ordinary skill to ascertain their understanding about subject matter disclosed by the prior art, including features

inherent in the prior art."). "Inherency, however, may not be established by probabilities or possibilities." *Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1325, 1332 (Fed. Cir. 2010).

Law of Obviousness

A patent may not issue where "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103. That is, the claimed invention must be nonobvious. The legal test to determine the question of obviousness is expansive and flexible, and there is "need for caution in granting a patent based on the combination of elements found in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415 (2007). The Supreme Court's *KSR* decision established the proper analysis for obviousness. *Id.* The Court loosened the standard for showing the obviousness of combining prior art references by overturning the Federal Circuit's teaching-suggestion-motivation test as too rigid and narrow and reaffirming the Graham factors. *Id.* at 415, 419–21.

In place of the teaching-suggestion-motivation test, the Court held that a more expansive and flexible approach should be applied. *Id.* at 415. "Obviousness is a question of law based on underlying findings of fact." *In re Kubin*, 561 F.3d 1351, 1355 (Fed. Cir. 2009). The underlying factual inquiries are: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; (3) the level of ordinary skill in the pertinent art; and (4) secondary considerations of non-obviousness. *See KSR*, 550 U.S. at 399 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966)).

In defining the obviousness standard, the Supreme Court stressed that "the results of ordinary innovation are not the subject of exclusive rights under the patent laws. Were it otherwise patents might stifle, rather than promote, the progress of useful arts." *KSR*, 550 U.S. at 427; *see*

also id. at 402 ("Granting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, for patents combining previously known elements, deprive prior inventions of their value or utility."). The Court also emphasized that its long-standing precedents confirm that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* at 416–417 (citing *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 62 (1969); *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273, 282 (1976); *United States v. Adams*, 383 U.S. 39, 50–51 (1966)). Thus, the operative question when assessing whether a claimed invention would have been obvious is "whether the improvement is more than the predictable use of prior art elements according to their established functions." *KSR*, 550 U.S. at 417. Notably, "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." *Id.* at 421. Indeed, beyond simple cases that merely require the combination of two prior art references, "a person of ordinary skill [often] will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420.

It is sufficient that a combination of limitations was "obvious to try" holding that, "[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." *Id.* at 421. "In that instance the fact that a combination was obvious to try might show that it was obvious under § 103." *Id.* All of the following rationales recognized in *KSR* support a finding of obviousness with respect to each of the obviousness combinations disclosed herein:

(1) Combining prior art limitations according to known methods to yield predictable results;

(2) Simple substitution of one known limitation for another to obtain predictable results;

(3) Use of known technique to improve similar devices (methods, or products) in the same way;

(4) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(5) "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(6) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

(7) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

Certain of these rationales are discussed with greater specificity below, but all apply, and the lack of a more specific discussion of some should not be taken to imply or admit that others do not also apply as the discussion below is intended to provide further explanation regarding certain of the specific rationales.

The rationale to combine prior-art references can come from a variety of sources and is not limited to the prior art itself or the specific problem the patentee was trying to solve. *Id.* at 420. Furthermore, the Supreme Court's expansive approach in *KSR* encourages, rather than restricts, the use of common sense when addressing obviousness. *Id.* at 421. The references themselves need

not provide a specific hint or suggestion of the alteration needed to arrive at the claimed invention; the analysis "may include recourse to logic, judgment, and common sense available to the person of ordinary skill that do not necessarily require explication in any reference or expert opinion." *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1329 (Fed. Cir. 2009). And the "reason, suggestion, or motivation to combine may be found explicitly or implicitly: 1) in the prior art references themselves; 2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved…." *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 665 (Fed. Cir. 2000).

35 U.S.C. § 112

Written Description and Enablement

The inventor must describe the invention so that the public will know what it is and that he or she has truly made the claimed invention. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 736 (2002) ("These [ ] requirements must be satisfied before issuance of the patent, for exclusive patent rights are given in exchange for disclosing the invention to the public. What is claimed by the patent application must be the same as what is disclosed in the specification. . ." (internal citations omitted)). To satisfy the written description requirement, the patent "must 'clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed.'" *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (*en banc*) (quoting *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1562–63 (Fed. Cir. 1991)); *see Kao Corp. v. Unilever U.S., Inc.*, 441 F.3d 963 967–68 (Fed. Cir. 2006). "[E]nough [of the invention] must be included to convince a person of skill in the art that the inventor possessed the invention . . ." *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005). "[T]he

hallmark of written description is disclosure." *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). "[I]t is the specification itself that must demonstrate possession." *Id.* at 1352.

Section 112, ¶ 1, also requires a patent to be enabled and describe "the manner and process of making and using [the claimed invention], in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same." 35 U.S.C. § 112, ¶ 1 (pre-AIA); *see also* 35 U.S.C. § 112(a) (AIA). Claims are not enabled when, at the effective filing date of the patent, a POSA could not practice their full scope without undue experimentation. *See Wyeth & Cordis Corp. v. Abbott Labs*., 720 F.3d 1380, 1384 (Fed. Cir. 2013). In addition, the scope of enablement must be commensurate with the full scope of the claim. *Id*. at 1384–85; *see also AK Steel Corp. v. Sollac and Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003). "Enabling the full scope of each claim is 'part of the quid pro quo of the patent bargain.'" *Id*. The Federal Circuit has provided several factors that may be utilized in determining whether a disclosure would require undue experimentation: (1) the quantity of experimentation necessary; (2) the amount of direction or guidance disclosed in the patent; (3) the presence or absence of working examples in the patent; (4) the nature of the alleged invention; (5) the state of the prior art; (6) the relative skill of those in the art; (7) the predictability of the art; and (8) the breadth of the claims. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988).

Indefiniteness

Section 112, ¶ 2, requires that "one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112 ¶ 2 (pre-AIA); *see also* 35 U.S.C. § 112(b) (AIA). "[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform,

with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). "Indefiniteness must be proven by clear and convincing evidence." *Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017).

Section 112, ¶ 4, states that "a claim in dependent form shall contain a reference to a claim previously set forth and then specify *a further limitation* of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference *all the limitations of the claim to which it refers*." 35 U.S.C. § 112 ¶ 4 (pre-AIA) (emphasis added); *see also* 35 U.S.C. § 112(d) (AIA). "A dependent claim that contradicts, rather than narrows, the claim from which it depends is invalid." *Multilayer Stretch Cling Film Holdings, Inc. v. Berry Plastics Corp.*, 831 F.3d 1350, 1362 (Fed. Cir. 2016); *see also, e.g.*, *Pfizer, Inc. v. Ranbaxy Lab'ys Ltd.*, 457 F.3d 1284, 1291 (Fed. Cir. 2006) (where independent claim and dependent claim "deal with non-overlapping subject matter," the dependent claim is invalid).

3. RESPONDENTS' SOURCES OF INFORMATION REGARDING SECTION 101 ELIGIBILITY, SECTIONS 102-103 INVALIDITY, SECTION 112 INVALIDITY, AND UNENFORCEABILITY.

As discussed below, Respondents have provided claim charts in support of their Initial Contentions. When considering citations in Respondents' invalidity claim charts:

- Citations to a particular structure or set of structures in a given figure should be understood as also referring to all identical, parallel, correlating, or corresponding sets of structures in other figures in the prior art or its text. Such citations should further be understood as referring to any alternative embodiments disclosed in the prior art for the cited structure or sets of structures.

- Citations to a particular structure or set of structures in a given figure should be understood as also referring to the text in the prior art that describes, explains, or elucidates upon the cited structure(s) or the given figure.

- Citations to text in prior art should be understood as also referring to any figures, structures, or embodiments described therein.

- The fact that certain entries in the charts may include citations to multiple alternative structures in the prior art should not be construed to mean that for points for which only a single citation is provided, the above points do not apply. Further, the fact that certain sections or pages of the prior art are cited for a given claim limitation should not be construed to mean that other sections or pages do not contain additional disclosures or suggestions of the same claim limitation.

Furthermore, in addition to the references cited in Respondents' claim charts, Respondents may rely on any of the patents or publications deriving from applications in the respective claimed priority chains of the Asserted Patents; materials listed on the faces of the Asserted Patents and related patents; materials incorporated by reference in the charted references; admitted prior art in the specifications of the Asserted Patents and related patents; the prosecution histories of the Asserted Patents and related patents; references cited in any USPTO (including PTAB) proceedings related to the Asserted Patents or related patents; any references known to an inventor, prosecution counsel, Complainants, or any affiliated party; and the references cited in any invalidity contentions that have been or will be submitted in any action or proceedings involving the Asserted Patents or related patents. A product in a charted reference should be understood as a contention that both the reference itself and the identified product independently invalidate the claims.

Respondents may also rely on deposition testimony of an inventor, deposition testimony of prosecution counsel, expert testimony, and any additional prior art located or developed during the course of discovery. Respondents may rely on additional documents or materials relating to system prior art addressed in these Initial Contentions. Respondents may rely on any of the materials in these Initial Contentions to demonstrate a motivation to combine. Respondents may also rely on deposition testimony of an inventor, deposition testimony of prosecution counsel, and/or expert testimony to further explain the prior art and to, for example, demonstrate a motivation to combine.

Respondents may also rely on (i) foreign counterparts of U.S. patents identified in its invalidity claim charts; (ii) U.S. counterparts of foreign patents and foreign patent applications identified in its invalidity claim charts; and (iii) U.S. and foreign patents and patent applications corresponding to articles and publications identified in its invalidity claim charts. Respondents may rely on uncited portions of the identified prior art, rely on other references (irrespective of whether such references themselves qualify as prior art) to show the state of the art, and/or rely on expert testimony to provide context to, or aid in understanding, the cited portions of the identified prior art.

4. THE ’233 PATENT

Priority Date

Complainants have yet to satisfy their burden of proving that any of the Asserted Claims of the ’233 Patent are entitled to a priority date prior to the filing date of its application, November 27, 2019. Because Complainants have not shown that any of the Asserted Claims of the ’233 Patent were conceived or reduced to practice, actually or constructively, prior to the filing date of the ’233 Patent, none of the Asserted Claims of the ’233 Patent are entitled to a date of invention that is earlier than the filing date, November 27, 2019.

Subject Matter Eligibility Grounds Under 35 U.S.C. § 101

As shown in Exhibits A-1 through A-12, each of the limitations of the Asserted Claims of the ’233 Patent, individually and in combination with the other elements of each claim, were well understood, routine, and conventional in the industry at the time. Exhibits A-1 through A-12 cite a number of prior art references as evidence of the description of the industry at the relevant time and how the various claim elements were well understood, routine, and conventional (alone and in combination). The prior art references referred to are exemplary only.

The information provided in prior art references and cited herein and in Appendices should not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Respondents claim construction disclosures will be provided according to the procedural schedule. Nothing contained in these Initial Contentions should be understood or deemed to be an express or implied admission or contention with respect to the absence of factual disputes relating to patent ineligibility, the absence of a need for construction of any terms in an Asserted Claim, any proper construction of any terms in an Asserted Claim, or alleged infringement of that claim. There is no claim construction issue or factual issue that precludes the Administrative Law Judge finding that the claims of the Asserted Patents are patent-ineligible.

Respondents also reserve the right to rely upon expert testimony as evidence of the description of the industry at the relevant time and how the various claim elements were well understood, routine, and conventional (alone and in combination). Respondents also further incorporate by reference the discussion below providing the exemplary legal and factual bases supporting its Section § 101 contentions. *See infra*.

Furthermore, to the extent the listed prior art discloses and describes particular products that were publicly known and/or in public use, in addition to each publication itself serving to demonstrate that the Asserted Claims of the ’233 Patent were well understood, routine, and conventional at the time of filing, the various products described in the publications also serve to demonstrate that the Asserted Claims of the ’233 Patent were well understood, routine, and conventional at the time of filing.

Respondents also reserve the right to rely upon foreign counterparts of the references identified in these Initial Contentions, U.S. counterparts of foreign patents and foreign patent

applications identified in these Initial Contentions, U.S. and foreign patents and patent applications corresponding to articles and publications identified in these Initial Contentions, issued patents corresponding to published patent applications identified in these Initial Contentions, published patent applications corresponding to issued patents identified in these Initial Contentions, and any systems, products, or prior inventions related to any of the references identified in these Initial Contentions.

As discussed below, the limitations of the Asserted Claims of the ’233 Patent recite cables comprised of generic and conventional hardware components, such as non-volatile memory, registers, pre-equalization filters, post-equalization filters, retimers, microcontrollers, and electrical conductors, and the cables and the components therein are used in their known and expected manner. The cables can also comprise software-based functions implemented by firmware stored in the memory and/or the microcontrollers, and the software-based functions are generic and conventional as well (*e.g.*, storing data (e.g., coefficients) to/from memory).

Identification of Asserted Claims That Are Ineligible Under Section 101

’233 Patent Claim	Exception to Eligibility	Factual and Legal Basis	Representative Claim[1]
1	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

[1] Claims 8 and 15 are substantially equivalent in scope to claim 1, therefore claim 1 can be used as representative of claims 8 and 15 for purposes of these Contentions. Claims 2–7, 9–14, and 16–20 have additional limitations that do nothing to make these claims valid under Section 101 and therefore claim 1 can be used as representative of all Asserted Claims for purposes of these Contentions. *See, e.g., Content Extraction,* 776 F.3d at 1349 (affirming that a specific claim is “representative, because all the claims are ‘substantially similar and linked to the same abstract idea’”). Moreover, as discussed below, each of the Asserted Claims of the ’233 Patent fails to satisfy Section 101 irrespective of whether claim 1 is representative.

’233 Patent Claim	Exception to Eligibility	Factual and Legal Basis	Representative Claim[1]
2	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
3	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
4	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
5	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
6	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
7	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
8	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
9	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
10	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
11	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
12	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

’233 Patent Claim	Exception to Eligibility	Factual and Legal Basis	Representative Claim[1]
13	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
14	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
15	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
16	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
17	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
18	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
19	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
20	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

Factual and Legal Basis for Subject Matter Ineligibility

***Alice* Step One: The Asserted Claims Are Directed to The Abstract Idea of Transferring and Converting Data**

Representative Independent Claim 1

Representative claim 1 of the ’233 patent recites as follows:

1. A cable that comprises:

[a] a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;

[b] a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and

[c] electrical connectors connecting the first and second DRR device to convey electrical signals therebetween,

[d] the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and

[e] the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,

[f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

'233 patent, claim 1.

The plain language of claim 1 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of exchanging data between first and second host ports and first and second DRR devices via connector plugs; converting between electrical transit signals and multi-lane data streams; and pre-equalization of electrical transit signals using coefficient values stored in nonvolatile memory. Claim 1 does not specify any non-conventional ways of exchanging data streams, conveying electrical signals, converting signals, or performing pre-equalization. In addition, claim 1 does not provide any new algorithms or methods or techniques for accomplishing these tasks. In effect, claim 1 claims a computer-implemented method of converting and conveying data, and the Federal Circuit has "consistently held that similar claims reciting the collection, transfer, and publishing of data are directed to an abstract idea." *Cellspin Soft, Inc. v. Fitbit, Inc.*, 927 F.3d 1306, 1315 (Fed. Cir. 2019) (citing *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016); *In re TLI Commc'ns. Patent Litig.*, 823 F.3d 607, 610–12 (Fed. Cir. 2016)). *See also Adaptive Streaming Inc. v. Netflix, Inc.*, 836 F.App'x 900, 903 (Fed. Cir. 2020) ("We have

held that the ideas of encoding and decoding image data and of converting formats, including when data is received from one medium and sent along through another, are by themselves abstract ideas, and accordingly conclude that claims focused on those general ideas governing basic communication practices, not on any more specific purported advance in implementation ,were directed to abstract ideas."); *Interval Licensing LLC v. AOL, Inc.*, 896 F.3d 1335, 1344 (Fed. Cir. 2019) ("We have recognized that 'information as such is an intangible' and that collecting, analyzing, and displaying that information, without more, is an abstract idea") (cleaned up).

Claim 1 requires the functional result of "exchang[ing]," "convey[ing]," "converting," and "pre-equaliz[ing]," data, but fails to do so in a non-abstract way as it does not sufficiently describe how to achieve these results in a non-abstract way. *See, e.g.*, *Two-Way Media Ltd. v. Comcast Cable Commc'ns., LLC*, 847 F.3d 1329, 1338–39 (Fed. Cir. 2017) (holding that "claim 1 manipulates data but fails to do so in a non-abstract way," because "[t]he claim requires the functional result of 'converting,' 'routing,' 'controlling,' 'monitoring,' and 'accumulating records,' but does not sufficiently describe how to achieve these results in a non-abstract way."); *RecogniCorp LLC v. Nintendo Co., Ltd.*, 855 F.3d 1322, 1326–27 (Fed. Cir. 2017) ("standard encoding and decoding" is "an abstract concept long utilized to transmit information," and "[a] process that started with data, added an algorithm, and ended with a new form of data was directed to an abstract idea"); *Adaptive Stream Inc. v. Netflix, Inc.*, 836 F.App'x 900, 903 (Fed. Cir. 2020) ("We have held that the ideas of encoding and decoding image data and of converting formats, including when data is received from one medium and sent along through another, are by themselves abstract ideas."); *Entropic Commc'ns., LLC v. DISH Network Corp.*, 767 F.Supp.3d 1043, 1058 (C.D. Cal. 2025) ("Sending and receiving data, even in the context of a communication network, is abstract."). Claim 1 is only directed to the aspirational end-result that, somehow,

conversion and pre-equalization occurs. *See also TriDim Innovations LLC v. Amazon.com, Inc.*, 207 F.Supp.3d 1073, 1080 (N.D. Cal. 2016) ("Much like the unpatentable subject matter in TLI Communications, the claims in question here are defined only in terms of their functions . .") (citing *In re TLI*, 823 F.3d at 613); *Affinity Labs of Tex., LLC v. Amazon.com, Inc.*, 838 F.3d 1266, 1269–70 (Fed. Cir. 2016) ("The purely functional nature of the claim confirms that it is directed to an abstract idea . ."); *Elec. Power Grp.*, 830 F.3d at 1354 (ineligible claims provided no "particular . inventive technology for performing those functions").

Turning to the claim language itself, elements 1[a]-[b] are directed to exchanging data between first and second host ports and first and second DRR devices via connector plugs, however, there is no recitation of how the data stream exchange is accomplished that would be indicative of an inventive technological improvement. Additionally, hardware for performing data recovery and remodulation was generic at least as of the '233 patent's November 27, 2019 filing date, *see, e.g.*, A-1–12, and no specific type of data recovery and remodulation hardware are recited in these elements. These elements are abstract because they describe generic devices (first and second DRR devices) configured to perform an abstract process (data exchange) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations (2 DRR Devices connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the November 27, 2019 filing date of the '233 patent, active optical cables (which use an optical link between two DRR-type devices that interfaced with host ports) were in common usage, and those cables used DRR-type devices to exchange data streams with host machines. *See, e.g.*, A-1–12.

Element 1[c] merely adds the requirement that there are electrical conductors connecting the DRRs to convey electrical signals therebetween. These elements do not disclose any improved

function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, conveying electrical signals via conductors were conventional and well-known techniques. *See, e.g.*, A-1–12.

Elements 1[d]-[e] are directed to converting between electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) and the inbound/outbound data streams, however, there is no recitation of how the DRRs’ conversion of the electrical transit signals and data streams is accomplished that would be indicative of an inventive technological improvement. Additionally, hardware for performing data conversion was generic as of the ’233 patent’s November 27, 2019 filing date, *see, e.g.*, A-1–12, and no specific types of data conversion hardware are recited by these claimed elements. These elements are abstract because they describe generic devices (first and second DRR devices) configured to perform an abstract process (implied mathematical algorithm for signal conversion) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations (2 DRR devices connected by a cable) recited therein that improve technology or solve a technical problem in a novel way, and there are no inventive concepts recited in the claim language directed to the conversion between undefined data streams and electrical transit signals. These elements do not disclose any improved function of a computer or other technology, nor do it solve a specific technological problem (e.g., data conversion) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, active optical cables (which used an optical link between two DRR-type devices that interfaced with host ports) were in common usage, and those cables used DRR-type devices that converted data streams into optical signals, and vice-versa. *See, e.g.*, A-1–12.

Element 1[f] is directed to the pre-equalization of electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) using coefficient values stored in the nonvolatile memory. The pre-equalization occurs after the data stream has been converted into electrical transit signals to be conveyed through the conductors. However, there is no recitation as to how the first or second DRR devices perform the recited pre-equalization that would be indicative of an inventive technological improvement, and using coefficients stored in nonvolatile memory was generic as of the '233 patent's November 27, 2019 filing date. *See, e.g.*, A-1–12. Additionally, hardware for performing pre-equalization was also generic as of the '233 patent's November 27, 2019 filing date, *see, e.g.*, A-1–12, and no specific types of pre-equalization hardware are recited in this claim element. This element is abstract because it describes generic devices (first and second DRR devices) configured to perform an abstract process (implied mathematical algorithm for pre-equalization) without specifying sufficiently concrete or inventive technical improvements; there are no specific, non-generic components or configurations (2 DRR devices connected by a cable) recited therein that improve technology or solve a technical problem in a novel way; and there are no inventive concepts recited in the claim language directed to the pre-equalization of electrical transit signals. The claim element does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., pre-equalization) in a novel way. As of the November 27, 2019 filing date of the '233 patent, pre-equalization of data signals being conveyed across conductors was a well-known signal conditioning technique. *See, e.g.*, A-1–12.

Although Respondents believe that independent claim 1 of the '233 patent is representative of all Asserted Claims of the '233 patent (all asserted claims recite the same abstract idea with

immaterial and conventional variations), out of an abundance of caution, Respondents will discuss the remaining asserted independent and dependent claims here.

Dependent Claim 2

Dependent claim 2 of the ’233 Patent recites as follows:

> 2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.

’233 patent, claim 2.

The additional limitations recited in dependent claim 2 merely adds a first controller to configure the first DRR in response to a power-on event and retrieve the transmit filter coefficient values from nonvolatile memory. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, configuring a DRR using a controller in response to a power-on event and retrieving transmit filter coefficient values from nonvolatile memory were conventional and well-known techniques. *See, e.g.*, A-1–12. In sum, claim 2 only recites abstract ideas, as the additional limitations of claim 2 are neither in isolation nor combined render claim 2 patent eligible.

Dependent Claim 3

Dependent claim 3 of the ’233 Patent recites as follows:

> 3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

’233 patent, claim 3.

The additional limitations recited in dependent claim 3 merely add the requirement that the DRRs use transmit coefficient values each time power is supplied to the plugs. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific

technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, having DRRs use transmit filter coefficient values each time power is supplied were conventional and well-known techniques. *See, e.g.*, A-1–12. In sum, claim 3 only recites abstract ideas, as the additional limitations of claim 3 are neither in isolation nor combined render claim 3 patent eligible.

Dependent Claim 4

Dependent claim 4 of the ’233 Patent recites as follows:

> 4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

’233 patent, claim 4.

The additional limitations recited in dependent claim 4 merely adds the requirement that the transmit filter coefficient values are determined in stored in nonvolatile memory after the cable is assembled. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, storing and determining filter coefficient values in nonvolatile memory after cable assembly were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 4 only recites abstract ideas, as the additional limitations of claim 4 are neither in isolation nor combined render claim 4 patent eligible.

Dependent Claim 5

Dependent claim 5 of the ’233 Patent recites as follows:

> 5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in nonvolatile memories.

’233 patent, claim 5.

The additional limitations recited in dependent claim 5 merely recite additional equalization parameters, which, as stated for claim 1, are abstract. Claim 5 is directed to the post-equalization of electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) using coefficient values stored in the nonvolatile memory. The post-equalization occurs before the received electrical transit signals are converted into the data stream (i.e., receiver-based). There is no recitation of how the first or second DRR devices perform the recited post-equalization that would be indicative of an inventive technological improvement, and using coefficients stored in a nonvolatile memory was generic as of the November 27, 2019 filing date of the ’233 patent. *See, e.g.*, A-1–12. Additionally, hardware for performing post-equalization was also generic as of the November 27, 2019 filing date of the ’233 patent, *see, e.g.*, A-1–12, and no specific types of post-equalization hardware are recited in the claimed invention. This element is abstract because it describes generic devices (first and second DRR devices) configured to perform an abstract process (implied mathematical algorithm for post-equalization) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or configurations (2 DRR devices connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. This claim element does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., post-equalization) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, post-equalization of data signals being conveyed across conductors was a well-known signal conditioning technique. *See, e.g.*, A-1–12.

Dependent Claim 6

Dependent claim 6 of the ’233 Patent recites as follows:

> The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

’233 patent, claim 6.

The additional limitations recited in dependent claim 6 merely add the requirement that the electrical conductors are twin-axial conductors carrying electrical transit signals in differential form. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, twin-axial conductors carrying electrical transit signals in differential form were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 6 only recites abstract ideas, as the additional limitations of claim 6 are neither in isolation nor combined render claim 6 patent eligible.

Dependent Claim 7

Dependent claim 7 of the ’233 Patent recites as follows:

> The cable of claim 1, wherein the first and second DRR device do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

’233 patent, claim 7.

The additional limitations recited in dependent claim 7 merely add the requirement that the DRR devices do not perform pre-equalization of multi-lane data streams. However, there is no recitation as to how the first or second DRR devices do not perform the recited pre-equalization that would be indicative of an inventive technological improvement. Additionally, hardware that did no perform pre-equalization was generic as of the ’233 patent’s November 27, 2019 filing date. *See, e.g.*, A-1–12. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, not pre-equalizing multi-lane data streams were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 7 only recites abstract ideas,

as the additional limitations of claim 7 are neither in isolation nor combined render claim 7 patent eligible.

Independent Claim 8

Independent claim 8 recites as follows:

8. A cable manufacturing method that comprises:

[a] connecting a first connector plug to a first data recover and re-modulation (DRR) device that exchanges multi-lane data streams with a first host interface port via the first connector plug;

[b] connecting a second connector plug to a second DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;

[c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween.

[d] the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and

[e] the second DRR device converting between said electrical transit signals and said multi-lane data streams for the second host interface port,

[f] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

’233 patent, claim 8.

Like claim 1, the plain language of claim 8 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of exchanging data between first and second host ports and first and second DRR devices via connector plugs; converting between electrical transit signals and multi-lane data streams; and pre-equalization of electrical transit signals using coefficient values stored in nonvolatile memory.

Elements 8[a]-[b] are directed to exchanging data between first and second host ports and first and second DRR devices via connector plugs, however, there is no recitation of how the data stream exchange is accomplished that would be indicative of an inventive technological

improvement. Additionally, hardware for performing data recovery and remodulation was generic as of the November 27, 2019 filing date of the ’233 patent and not specific type of data recovery and remodulation hardware is recited in these claim elements. *See, e.g.*, A-1–12. As of the November 27, 2019 filing date of the ’233 patent, active optical cables (which used an optical link between two DRR-type devices that interfaced with host ports) were in common usage, and those cables used DRR-type devices to exchange data streams with host machines. *See, e.g.*, A-1–12.

Element 8[c] merely adds the requirement that there are electrical conductors connecting the DRRs to convey electrical signals therebetween. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, conveying electrical signals via conductors were conventional and well-known techniques. *See, e.g.*, A-1–12.

Elements 8[d]-[e] are directed to the conversion between electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) and the inbound/outbound data streams, however, there is no recitation of how the DRRs’ conversion of the electrical transit signals and data streams is accomplished that would be indicative of an inventive technological improvement. Additionally, hardware for performing data conversion was generic as of the November 27, 2019 filing date of the ’233 patent, *see, e.g.*, A-1–12, and no specific types of data conversion hardware are recited in these elements. These elements are abstract because they describe generic devices (first and second DRR devices) configured to perform an abstract process (implied mathematical algorithm for signal conversion) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or configurations (2 DRR devices connected by a cable) recited therein that improve technology or solve a technical problem in a novel way, and there are no inventive concepts recited in the claim

language directed to the conversion between undefined data streams and electrical transit signals. These elements do not disclose any improved function of a computer or other technology, nor do it solve a specific technological problem (e.g., data conversion) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, active optical cables (which used an optical link between two DRR-type devices that interfaced with host ports) were in common usage, and those cables used DRR-type devices that converted data streams into optical signals, and vice-versa. *See, e.g.*, A-1–12.

Element 8[f] is directed to the pre-equalization of electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) using coefficient values stored in the nonvolatile memory. The pre-equalization occurs after the data stream has been converted into electrical transit signals to be conveyed through the conductors. However, there is no recitation of how the first or second DRR devices perform the recited pre-equalization that would be indicative of an inventive technological improvement, and using coefficients stored in nonvolatile memory was generic as of the ’233 patent’s November 27, 2019 filing date. *See, e.g.*, A-1–12. Additionally, hardware for performing pre-equalization is generic as of the ’233 patent’s November 27, 2019 filing date, *see, e.g.*, A-1–12, and no specific types of pre-equalization hardware are recited in this claim element. This element is abstract because it describes a generic device (first and second DRR devices) configured to perform an abstract process (implied mathematical algorithm for pre-equalization) without specifying sufficiently concrete or inventive technical improvements; there are no specific, non-generic components or configurations (2 DRR devices connected by a cable) recited therein that improve technology or solve a technical problem in a novel way; and there are no inventive concepts recited in the claim language directed to the pre-equalization of electrical transit signals. The claim limitation does not disclose any improved function of a computer or

other technology, nor does it solve a specific technological problem (e.g., pre-equalization) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, pre-equalization of data signals being conveyed across conductors was a well-known signal conditioning technique. *See, e.g.*, A-1–12.

Dependent Claim 9

Dependent claim 9 of the ’233 Patent recites as follows:

> 9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.

’233 patent, claim 9.

The additional limitations recited in dependent claim 9 merely adds a first controller to configure the first DRR in response to a power-on event and retrieve the transmit filter coefficient values from nonvolatile memory. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, configuring a DRR using a controller in response to a power-on event and retrieving transmit filter coefficient values from nonvolatile memory were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 9 only recites abstract ideas, as the additional limitations of claim 9 are neither in isolation nor combined render claim 9 patent eligible.

Dependent Claim 10

Dependent claim 10 of the ’233 Patent recites as follows:

> 10. The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

’233 patent, claim 10.

The additional limitations recited in dependent claim 10 merely add the requirement that the DRRs use transmit coefficient values each time power is supplied to the plugs. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, having DRRs use transmit filter coefficient values each time power is supplied were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 10 only recites abstract ideas, as the additional limitations of claim 10 are neither in isolation nor combined render claim 10 patent eligible.

Dependent Claim 11

Dependent claim 11 of the ’233 Patent recites as follows:

> 11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.

’233 patent, claim 11.

The additional limitations recited in dependent claim 11 merely adds the requirement that the transmit filter coefficient values are determined in stored in nonvolatile memory after the cable is assembled. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, storing and determining filter coefficient values in nonvolatile memory after cable assembly were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 11 only recites abstract ideas, as the additional limitations of claim 11 are neither in isolation nor combined render claim 11 patent eligible.

Dependent Claim 12

Dependent claim 12 of the ’233 Patent recites as follows:

> 12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

’233 patent, claim 12.

The additional limitations recited in dependent claim 12 merely recite additional equalization parameters, which, as stated for claim 1, are abstract. Claim 12 is directed to the post-equalization of electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) using coefficient values stored in the nonvolatile memory. The post-equalization occurs before the received electrical transit signals are converted into the data streams (i.e., receiver based). There is no recitation of how the first or second DRR devices perform the recited post-equalization that would be indicative of an inventive technological improvement, and using coefficients stored in a nonvolatile memory was generic as of the November 27, 2019 filing date of the ’233 patent. *See, e.g.*, A-1–12. Additionally, hardware for performing post-equalization was generic as of the November 27, 2019, *see, e.g.*, A-1–12, and no specific types of post-equalization hardware are recited in the claimed invention. This element is abstract because it describes a generic device (first and second DRR devices) configured to perform an abstract process (implied mathematical algorithm for post-equalization) without specifying sufficiently concrete or inventive technical improvements; there are no specific non-generic components or configurations (2 DRR devices connected by a cable) recited therein that improve technology or solve a technical problem in a novel way; and there are not inventive concepts recited in the claim language directed to the conversion between undefined data streams and electrical transit signals. This claim element does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., post-equalization) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, post-equalization of data signals being conveyed across conductors was a well-known signal conditioning technique. *See, e.g.*, A-1–12.

Dependent Claim 13

Dependent claim 13 of the ’233 Patent recites as follows:

> 13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.

’233 patent, claim 13.

The additional limitations recited in dependent claim 13 add the requirement that the electrical conductors are twin-axial conductors carrying electrical transit signals in differential form. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, twin-axial conductors carrying electrical transit signals in differential form were well-known techniques. *See, e.g.*, A-1–12. In sum, claim 13 only recites abstract ideas, as the additional limitations of claim 13 are neither in isolation nor combined render claim 13 patent eligible.

Dependent Claim 14

Dependent claim 14 of the ’233 Patent recites as follows:

> 14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

’233 patent, claim 14.

The additional limitations recited in dependent claim 14 merely add the requirement that the DRR devices do not perform pre-equalization of multi-lane data streams. However, there is no recitation as to how the first or second DRR devices do not perform the recited pre-equalization that would be indicative of an inventive technological improvement. Additionally, hardware that did no perform pre-equalization was generic as of the ’233 patent’s November 27, 2019 filing date. *See, e.g.*, A-1–12. These elements do not disclose any improved function of a computer or other

technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, not pre-equalizing multi-lane data streams were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 14 only recites abstract ideas, as the additional limitations of claim 14 are neither in isolation nor combined render claim 14 patent eligible.

Independent Claim 15

Independent claim 15 of the ’233 Patent recites as follows:

15. A communications method that comprises:

[a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and

[b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,

[c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.

’233 patent, claim 15.

Like claim 1, the plain language of claim 15 establishes that it is directed to a patent ineligible concept, namely the abstract idea of exchanging data between first and second host ports and first and second DRR devices via connector plugs; converting between electrical signals and multi-lane data streams; and pre-equalization of electrical transit signals using coefficient values stored in nonvolatile memory.

Turning to the claim language itself, element 15[a] is directed to the conversion between electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) and the inbound/outbound data streams, however, there is no recitation of how the first DRR

conversion of the electrical transit signals or data streams is accomplished that would be indicative of an inventive technological improvement. Additionally, hardware for performing data conversion is generic as of the November 27, 2019 filing date of the ’233 patent, *see, e.g.*, A-1–12, and no specific types of data conversion hardware are recited in this claim element. This claim element is abstracted because it describes a generic device (first DRR device) configured to perform an abstract process (implied mathematical algorithm for signal conversion) without specifying sufficiently concrete or inventive technical improvements; there are no specific, non-generic components or configurations (2 DRR devices connected by cable) recited therein that improve technology or solve a technical problem in a novel way; and there are no inventive concepts recited in the claim language directed to the conversion between undefined data streams and electrical transit signals. The claim language does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., data conversion) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, active optical cables (which used an optical link between two DRR-type devices that interfaced with host ports) were in common usage, and those cables used DRR-type devices that converted data streams into optical cables, and vice-versa. *See, e.g.*, A-1–12.

Element 15[b] is directed to the conversion between electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) and the inbound/outbound data streams, however, there is no recitation of how the second DRR conversion of the electrical transit signal or data streams are accomplished that would be indicative of an inventive technological improvement. Additionally, hardware for performing data conversion is generic as of the November 27, 2019 filing date of the ’233 patent, *see, e.g.*, A-1–12, and no specific types of data conversion hardware are recited in the claimed element. This claim element is abstract because it

describes a generic device (second DRR device) configured to perform an abstract process (implied mathematical algorithm for signal conversion) without specifying sufficiently concrete or inventive technical improvements; there are no specific, non-generic components or configurations (2 DRR devices connected by cable) recited therein that improve technology or solve a technical problem in a novel way; and there are no inventive concepts recited in the claim language directed to the conversion between undefined data streams and electrical transit signals. The claim element does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., data conversion) in a novel way. As of the November 27, 2019 filing of the ’233 patent, active optical cables (which used an optical link between two DRR-type devices that interface with host ports) were in common usage, and those cables used DRR-type devices that converted data streams into optical signals, and vice-versa.

Element 15[c] is directed to the pre-equalization of electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) using coefficient values stored in the nonvolatile memory. The pre-equalization occurs after the data stream has been converted into electrical transit signals to be conveyed through the conductors. However, there is no recitation of how the first or second DRR devices perform the recited pre-equalization that would be indicative of an inventive technological improvement, and using coefficients stored in nonvolatile memory was generic as of the ’233 patent’s November 27, 2019 filing date. Additionally, hardware for performing pre-equalization was also generic as of the ’233 patent’s November 27, 2019 filing date, *see, e.g.*, A-1–12, and no specific types of pre-equalization hardware are recited in this claim element. This element is abstract because it describes a generic device (first and second DRR devices) configured to perform an abstract process (implied mathematical algorithm for pre-equalization) without specifying sufficiently concrete or inventive technical improvements; there

are no specific, non-generic components or configurations (2 DRR devices connected by cable) recited therein that improve technology or solve a technical problem in a novel way; and there are no inventive concepts recited in the claim language directed to the pre-equalization of electrical transit signals. This claim element does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., data conversion) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, pre-equalization of data signals being conveyed across conductors was a well-known signal conditioning technique.

Dependent Claim 16

Dependent claim 16 of the ’233 Patent recites as follows:

> 16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.

’233 patent, claim 16.

The additional limitations recited in dependent claim 16 merely add the requirement that controllers configure the DRRs in response to a power-on event and retrieve transmit filter coefficient values from internal nonvolatile memory. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, having controllers to configure DRRs in response to a power-on event and retrieve transmit filter values from internal nonvolatile memory were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 16 only recites abstract ideas, as the additional limitations of claim 16 are neither in isolation nor combined render claim 16 patent eligible.

Dependent Claim 17

Dependent claim 17 of the ’233 Patent recites as follows:

> 17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

’233 patent, claim 17.

The additional limitations recited in dependent claim 17 merely add the requirement that the DRRs use transmit coefficient values each time power is supplied to the plugs. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, having DRRs use transmit filter coefficient values each time power is supplied were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 17 only recites abstract ideas, as the additional limitations of claim 17 are neither in isolation nor combined render claim 17 patent eligible.

Dependent Claim 18

Dependent claim 18 of the ’233 Patent recites as follows:

> 18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

’233 patent, claim 18.

The additional limitations recited in dependent claim 18 merely add he requirement that the transmit filter coefficient values are determined in stored in nonvolatile memory after the cable is assembled. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, storing and determining filter coefficient values in nonvolatile memory after cable assembly were conventional well-known techniques. *See, e.g.*, A-

1–12. In sum, claim 18 only recites abstract ideas, as the additional limitations of claim 18 are neither in isolation nor combined render claim 18 patent eligible.

Dependent Claim 19

Dependent claim 19 of the ’233 Patent recites as follows:

> 19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

’233 patent, claim 19.

The additional limitations recited in dependent claim 19 merely recite additional equalization parameters, which, as stated for claim 1, are abstract. Claim 19 is directed to the post-equalization of electrical transit signals (i.e., signals traversing the electrical conductors between the DRRs) using coefficient values stored in the nonvolatile memory. The post-equalization occurs before the received electrical transit signals are converted into data streams (i.e., receiver based). There is no recitation of how the first or second DRR devices perform the recited post-equalization that would be indicative of inventive technological improvement, and using coefficients stored in nonvolatile memory was generic as off the November 27, 2019 filing date of the ’233 patent. *See, e.g.*, A-1–12. Additionally, hardware for performing post-equalization was also generic as of the November 27, 2019 filing date of the ’233 patent, *see, e.g.*, A-1–12 and no specific types of post-equalization hardware are recited in the claim element. This element is abstract because it describes a generic device (first DRR device) configured to perform an abstract process (implied mathematical algorithm for post-equalization) without specifying sufficiently concrete or inventive technical improvements; there are no specific, non-generic components or configurations (2 DRR devices connected by cable) recited therein that improve technology or solve a technical problem in a novel way; and there are no inventive concepts recited in the claim language directed to the conversion between undefined data streams and electrical transit signals. This claim element

does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., post-equalization) in a novel way. As of the November 27, 2019 filing date of the ’233 patent, post-equalization of data signals being conveyed across conductors was a well-known signal conditioning technique.

Dependent Claim 20

Dependent claim 20 of the ’233 Patent recites as follows:

> The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

’233 patent, claim 20.

The additional limitations recited in dependent claim 20 merely add the requirement that the DRR devices do not perform pre-equalization of multi-lane data streams. However, there is no recitation as to how the first or second DRR devices do not perform the recited pre-equalization that would be indicative of an inventive technological improvement. Additionally, hardware that did no perform pre-equalization was generic as of the ’233 patent’s November 27, 2019 filing date. *See, e.g.*, A-1–12. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the November 27, 2019 filing date of the ’233 patent, not pre-equalizing multi-lane data streams were conventional well-known techniques. *See, e.g.*, A-1–12. In sum, claim 20 only recites abstract ideas, as the additional limitations of claim 20 are neither in isolation nor combined render claim 20 patent eligible.

***Alice* Step Two: The Asserted Claims Contain No “Inventive Concept” Sufficient to Render Them Patent Eligible**

As noted above, the second step of a Section 101 analysis under *Alice* requires the consideration of each claim element “both individually and ‘as an ordered combination’ to

determine" whether there are additional elements present in the claim that 'transform the nature of the claim' into a patent-eligible application." *Alice*, 573 U.S. at 217 (quotation omitted).

The Asserted Claims of the '233 patent merely invoke well-understood, routine, and conventional software methods and techniques to achieve the multiple abstract ideas interspersed throughout the Asserted Claims. The claims directed to exchanging data between first and second host ports and first and second DRR devices via connector plugs; converting between electrical transit signals and multi-lane data streams; and pre-equalization of electrical transit signals using coefficient values stored in nonvolatile memory, which is well-known to one of ordinary skill in the art. *See, e.g.*, A-1–12. As the Federal Circuit has held, "claims are not saved from abstraction merely because they recite components more specific than a generic computer." *BSG Tech LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1286 (Fed. Cir. 2018). As discussed in detail in the preceding Section, the Asserted Claims of the '233 patent lack any of the inventive hallmarks found in other patents found to be patent eligible.

As noted earlier, the Asserted Claims of the '233 patent provide no technological solution to the purported problems but instead simply disclose the abstract idea of exchanging and converting data, which moreover would have been well-known to one of ordinary skill in the art. As noted at the beginning of this section, the second step of a Section 101 analysis under *Alice* requires the consideration of the claim elements "as an ordered combination" to determine whether there are additional elements present in the claim that "transform the nature of the claim" into a patent-eligible application." *Alice*, 134 S. Ct. at 2347 (quotation omitted). However, the method claims' order of claim elements transfer the claim int patent-eligible material. To the contrary, the order of claim elements is conventional in the sense that a user would normally connect the DRR devices to the host ports and connect the DRRs to themselves via a cable prior to any data transfer

or conversion. The claims do not disclose anything different than the common and conventional practice of connecting two devices with an active electrical cable to that will transfer data therebetween. The order of the claim elements does not disclose any software and/or hardware technological advancement.

All of the Asserted Claims Are Substantially Similar—Represented by Claim 1—for Purposes of Section 101 Analysis

All the Asserted Claims of the ’233 Patent are directed to patent-ineligible abstract ideas. Where claims are “substantially similar and linked to the same abstract idea,” courts may look to representative claims in a Section 101 analysis. *Content Extraction and Trans. v. Wells Fargo Bank,* 776 F.3d 1343, 1349 (Fed. Cir. 2014). Here, claim 1 of the ’233 Patent is representative of all Asserted Claims of the ’233 Patent, as the remaining claims recite the same abstract idea with immaterial and conventional variations.

Asserted independent claims 1, 8, and 15 recite nearly the same subject matter with only minor variations for purposes of Section 101 analysis. As discussed above, claim 1 is directed to the abstract idea of a cable exchanging and converting data. Claims 8 and 15 recite the same subject matter written as method claims.

The asserted dependent claims add additional limitations, but those additional limitations do not impart patent eligibility. Instead, the dependent claims add further variations on abstract ideas that are not technological advancements. *See, e.g.*, *Universal Secure Registry LLC v. Apple Inc.*, 10 F.4th 1342, 1357 (Fed. Cir. 2021).

As noted above, dependent claim 2 adds a first controller which configures the first DRR already recited in independent claim 1. As noted previously, dependent claim 2 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive

concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 3 merely adds the requirement that the DRRs use transmit coefficient values each time power is supplied to the plugs. As noted previously, dependent claim 3 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 4 merely adds the requirement that the transmit filter coefficient values are determined in stored in nonvolatile memory after the cable is assembled. As noted previously, dependent claim 4 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 5 merely adds the requirement of the DRRs employing receiver-based equalization of the electrical transit signals, which, as discussed above, is an abstract idea that is not patent-eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 6 merely adds the requirement that the electrical conductors are twin-axial conductors carrying electrical transit signals in differential form. As noted previously, dependent claim 6 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and is simply another layer of abstraction on top of an already abstract idea (i.e., exchanging and converting data).

Dependent claim 7 merely adds the requirement that the DRRs do not perform pre-equalization of the multi-lane data streams provided to the host interface ports. As noted previously, dependent claim 7 recites conventional and well-known subject matter, (*see, e.g.*, A-

1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 9 adds a first controller which configures the first DRR already recited in independent claim 8. As noted previously, dependent claim 9 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 10 merely adds the requirement that the DRRs use transmit coefficient values each time power is supplied to the plugs. As noted previously, dependent claim 10 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 11 merely adds the requirement that the transmit filter coefficient values are determined in stored in nonvolatile memory after the cable is assemble. As noted previously, dependent claim 11 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 12 merely adds the requirement of the DRRs employing receiver-based equalization of the electrical transit signals, which, as discussed above, is an abstract idea that is not patent-eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 13 merely adds the requirement that the electrical conductors are twin-axial conductors carrying electrical transit signals in differential form. As noted previously, dependent claim 13 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and

does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 14 merely adds the requirement that the DRRs do not perform pre-equalization of the multi-lane data streams provided to the host interface ports. As noted previously, dependent claim 14 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 16 merely adds the requirement that controllers configure the DRRs in response to a power-on event and retrieve transmit filter coefficient values from internal nonvolatile memory. As noted previously, dependent claim 16 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 17 merely adds the requirement that the DRRs use transmit coefficient values each time power is supplied to the plugs. As noted previously, dependent claim 17 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 18 merely adds the requirement that the transmit filter coefficient values are determined in stored in nonvolatile memory after the cable is assembled. As noted previously, dependent claim 18 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 19 merely adds the requirement of the DRRs employing receiver-based equalization of the electrical transit signals, which, as discussed above, is an abstract idea that is not patent-eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 20 merely adds the DRRs do not perform pre-equalization of the multi-lane data streams provided to the host interface ports. As noted previously, dependent claim 20 recites conventional and well-known subject matter, (*see, e.g.*, A-1–12) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Notably, there are no specific instructions or limitations in the specification concerning how these claim limitations must be carried out, other than a description of the idea, non-specific examples of how the idea may be carried out, and the instructions to apply it to the conventional technological environment. *See Alice*, 573 U.S. at 220–21. Thus, as with claim 1, none of the asserted dependent claims provide particular requirements as to how the claimed steps are to be performed, nor do they recite anything other than conventional components that are used in conventional ways.

Accordingly, claim 1 of the ’233 Patent is representative for purposes of the Section 101 analysis, and any differences amongst claims 2–20 are insubstantial with respect to eligibility, as each of the claims in the ’233 Patent are drawn to the same abstract idea of data exchange and conversion using generic components and configurations. *Alice*, 573 U.S. at 225; *see also Content Extraction*, 776 F.3d at 1348.

Invalidity Grounds Under 35 U.S.C. §§ 102 and 103

Respondents attach, as Appendix A to its Initial Contentions, claim charts showing examples of how the cited references anticipate and/or render obvious the Asserted Claims of the

’233 Patent under at least AIA 35 U.S.C. §§ 102 and 103 either expressly or inherently as understood by a person having ordinary skill in the art, or based on Complainants’ apparent interpretation of the claims.

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
A-1	U.S. Patent No. 10,148,414 (“Lugthart ’414”)	December 4, 2018 (Issued) October 19, 2017 (Published)	June 30, 2017
A-2	U.S. Patent Pub. No. US20170302431A1 (“Lugthart ’431”)	October 19, 2017 (Published)	June 30, 2017
A-3	U.S. Patent No. 8,516,238 (“Cornelius”)	Aug. 20, 2013 (Issued)	June 30, 2011
A-4	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“TI DS110DF111”)	No later than June 2015 (Published and On Sale)	
A-5	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer (“DS125DF410”)	No later than February 2018 (Published and On Sale)	
A-6	Texas Instruments – DS250DF410 25 Gbps Multi-Rate 4-Channel Retimer (“DS250DF410”)	No later than October 2019 (Published and On Sale)	
A-7	Texas Instruments – DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer (“DS250DF810”)	No later than October 2019 (Published and On Sale)	
A-8	U.S. Patent No. 9,270,500 (“Vijayaraghavan”)	Feb. 23, 2016 (Issued)	Dec. 13, 2013
A-9	U.S. Patent No. 8,499,103 (“Carter”)	July 30, 2013 (Issued)	April 20, 2010
A-10	U.S. Patent No. 8,312,302 (“Baker”) which incorporates Cornelius	Nov. 13, 2012 (Issued)	June 30, 2011
A-11	Amphenol SMP9 Active Electric Cable Product	Prior to 2018 (On Sale)	
A-12	Common Management Interface Specification for 8X/16X Pluggable Transceivers Rev 3.0 (“CMIS”)	September 18, 2018 (Published)	
A-12	A 4-32 Gb/s Bidirectional Link With 3-Tap FFE/6-Tap DFE and Collaborative CDR in 22 nm CMOS, IEEE Journal of	December 2014 (Published)	

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
	Solid-State Circuits, Volume 49, No. 12. ("Musah")		
A-12	A 12.5-Gbps, 7-bit Transmit DAC with 4-Tap LUT-based Equalization in 0.13um CMOS ("Chung")	September 21, 2008 (Published)	
A-12	U.S. Patent 10,659,337 ("Riani")	May 19, 2020	August 28, 2018
A-12	A 40-Gb/s Quarter Rate SerDes Transmitter and Receiver Chipset in 65 nm CMOS, IEEE Journal of Solid-State Circuits, Volume 52, No. 11 ("Zheng")	November 2017 (Published)	
A-12	U.S. Patent No. 7,233,617 ("Gorecki")	April 15, 2004 (Published)	April 10, 2003
A-12	IEEE 802.3-2015 - IEEE Standard for Ethernet	March 4, 2016 (Published)	
A-12	U.S. Patent 9,337,993 ("Lugthart '993")	May 10, 2016 (Issued)	December 23, 2014
A-12	U.S. Patent 8,891,670 ("Ishaug")	Nov. 18, 2014 (Published)	November 9, 2012
A-12	U.S. Patent 8,867,928 ("Piehler")	Oct. 21, 2014 (Published)	May 16, 2011
A-12	U.S. Patent 6,879,641 ("Unger")	April 12, 2005 (Published)	June 13, 2002
A-12	U.S. Patent Application 2013/0073749 ("Tremblay")	March 21, 2013 (Published)	February 22, 2011

The attached claim charts identify specific examples of disclosures that teach or suggest a given claim limitation. These identifications should be understood to be exemplary; the charts do not necessarily indicate every location within a particular prior art reference where a claim limitation may be disclosed or suggested. Respondents and their expert witnesses may rely on other portions of the prior art.

To the extent Complainants contend that any reference identified above does not anticipate the Asserted Claims, it would have been obvious over that primary reference alone or to combine or modify the primary references with concepts from other prior art, such as the other references identified and as explained herein and in Exhibits A-01 – A-12.

In particular, for each limitation of the Asserted Claims that Complainants contend is not met by a particular reference, Respondents contend that the limitation (and claim as a whole) is obvious based on a combination of that particular reference with (1) any other reference disclosing the limitation, (2) any admitted prior art, as explained in the background of each patent or discussed in the file history, (3) any other reference identified in Exhibits A-01 – A-12, as disclosing that limitation, and/or (4) the knowledge of a person of ordinary skill in the art and/or any of the references and concepts discussed herein regarding the relevant background and state of the art. Respondents' obviousness grounds for each dependent claim incorporate the obviousness grounds for the claims from which the dependent claim depends in addition to any obviousness grounds identified in the charts for the dependent claim. To the extent that individual Exhibits A-01 – A-12 include specific combination of prior art, Respondents' contentions are not limited only to those particular combinations, as such combinations are merely exemplary and are meant to be inclusive of the combinations expressed herein and in the other Appendices to these contentions.

The suggested obviousness combinations discussed herein are not to be construed to suggest that any reference included in the combinations is not anticipatory. Further, to the extent that Complainants contend that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, Defendants reserve the right to identify other prior art references that, when combined with the anticipatory prior art, would render the claims obvious despite an allegedly missing limitation. Defendants will further specify the motivations to combine the prior art, including through reliance on expert testimony, at the appropriate later stage of this Investigation.

In addition to the combinations of Exhibits A-01 – A-12, at least the following exemplary combinations would have been obvious to a POSITA:

- Lugthart ’414 in view of Gorecki;
- Lugthart ’414 in view of Gorecki and IEEE 802.3 Section 5;
- Lugthart 431 in view of TI DS110DF111, or TI DS125DF410, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or any combination therein;
- TI DS110DF111 in view of Lugthart 431, or TI DS125DF410, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or any combination therein;
- TI DS125DF410 in view of Lugthart 431, or TI DS110DF111, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or any combination therein;
- TI DS250DF410 in view of Lugthart 431, or TI DS110DF111, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or any combination therein;
- TI DS250DF810 in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or TI DS250DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or any combination therein;
- Vijayaraghavan in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or any combination therein;
- Carter in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Vijayaraghavan, or Cornelius, or Musah, or Riani, or Zheng, or any combination therein;

- Cornelius in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Musah, or Riani, or Zheng, or any combination therein;
- Baker in view of Lugthart 431/414/993, Ishaug, Piehler, Gorecki, Tremblay, and/or Unger, or TI DS110DF111, or TI DS125DF410, or TI DS250DF410, or TI DS250DF810, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Musah, or Riani, or Zheng, or any combination therein.

For each specified combination, Respondents rely on the references herein, as well as the knowledge of a person of ordinary skill in the art, including that which will be discussed through expert discovery. Although Respondents provide exemplary disclosures and motivations to combine below, Respondents will present expert opinion in accordance with the procedural schedule. Respondents reserve the right to supplement or modify the anticipation and obviousness grounds in response to, for example, Complainants' positions regarding the scope and meaning of the Asserted Claims taken in this Investigation, before the PTAB, or during prosecution of pending matters related to the Asserted Patents, claim construction determinations made in this Investigation or other proceedings involving the Asserted Patents, updates or changes to Complainants' infringement and/or technical domestic industry positions, and materials later obtained during discovery, including from Complainant or in response to any third party subpoenas.

Respondents reserve the right to rely on the prior art references identified in connection with any of the other Asserted Patents in connection with the '233 Patent. In addition, Respondents hereby cite the following additional references as being relevant to the subject matter claimed in the '233 Patent. Respondents are producing concurrently herewith a number of such references

that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Respondents reserve the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103 (including as evidence of motivation to combine or reasonable expectation of success), as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Complainant may take regarding the scope of the Asserted Claims, and/or based on the Court's claim construction (once issued), Respondents reserve the right to revise these contentions and to rely on these references to prove the invalidity of the '233 Patent in a manner consistent with this ALJ's Ground Rules.

- U.S. Patent No. 5,452,333
- U.S. Patent No. 6,975,140
- U.S. Patent No. 7,570,708
- U.S. Patent No. 7,762,727
- U.S. Patent No. 8,000,176
- U.S. Patent No. 8,787,430
- U.S. Patent No. 8,990,654
- U.S. Patent No. 9,137,063
- U.S. Patent No. 9,152,257
- U.S. Patent No. 9,172,578
- U.S. Patent No. 9,178,542
- U.S. Patent No. 9,806,812
- U.S. Patent Application Publication No. 2005/0013317
- U.S. Patent Application Publication No. 2005/0078758

- U.S. Patent Application Publication No. 2013/0195155
- U.S. Patent Application Publication No. 2014/0075076
- U.S. Patent Application Publication No. 2014/0119425
- U.S. Patent Application Publication No. 2014/0281068
- U.S. Patent Application Publication No. 2015/0106536
- SFP-DD MSA, "SFP-DD Hardware Specification for SFP Double Density 2X Pluggable Transceiver," SFP-DD Rev 3.0 (April 10, 2019)
- SFF-8436 Specification for QSFP+ 4X 10 Gb/s Pluggable Transceiver, Rev. 4.9 (Aug. 31, 2018)
- Pavan Kumar Hanumolu, *et al*., "Equalizers for High-Speed Serial Links," International Journal of High Speed Electronics and Systems, vol. 15, no. 2, 2005, pp. 429-458
- DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer Datasheet, SNLS482B, Texas Instruments Incorporated (January 2017)
- Proakis, John G., DIGITAL COMMUNICATION, McGraw-Hill, 4th Edition, 2000, pp. 583-635
- Liu, Jin and Xiaofeng Lin, "Equalization in high-speed communication systems." IEEE Circuits and Systems Magazine, vol. 4, no. 2, 2004, pp. 4-17
- Hsieh, Ming-ta and Gerald E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery," IEEE Circuits and Systems Magazine, vol. 8, no. 4, 2008, pp. 45-57
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section One
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Two
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Three
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Four
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Five
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Six

Level of Ordinary Skill in the Art

To assess the level of ordinary skill of a POSITA, the following factors can be considered: (i) the type of problems encountered in the art; (ii) the prior solutions to those problems; (iii) the rapidity at which innovations are made; (iv) the sophistication of the technology; and (v) the level of education of active workers in the relevant field.

Based on the foregoing, Respondents contend that a POSITA for the ’233 Patent as of November 27, 2019 would have had a Bachelor of Science in electrical or computer engineering with at least three years of experience in high-speed digital communication systems. A higher level of education may substitute for less experience.

Obviousness and Motivation to Combine

Motivations to combine with a reasonable expectation of success, as well as the general state of the art, may be found in a variety of places including in the references defined above and the specification of the ’233 Patent. For example, each piece of prior art relates to the design and/or structure and/or function of active cable devices. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine any one piece of identified prior art with any other identified piece of prior art with a reasonable expectation of success. For at least this reason, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein so as to practice the Asserted Claims and there was a motivation in the art to make such a combination. A POSITA would have also had a reasonable belief that such combinations would have been successful.

Motivations to combine various prior art references with a reasonable expectation of success are present in the references themselves, the common knowledge of one of ordinary skill in the art, the prior art as a whole, or the nature of the problems allegedly addressed by the ’233

Patent. Further reasons to combine the references identified in these charts with a reasonable expectation of success include the nature of the problem being solved, the express, implied, and/or inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed towards methods and systems for the design and/or structure and/or function of communication devices that such combinations would have yielded predictable results, and the fact that such combinations would have represented known alternatives to a person of ordinary skill in the art.

In *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 550 U.S. 398, 416 (2007); *see also id.* at 401 ("[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions."). In particular, a patent is obvious where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill are not in material dispute, and the obviousness of the claim is apparent in light of these factors." *Id.* at 427. The Supreme Court explained that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 401.

Moreover, the Supreme Court recognized that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. *Id*. at 402 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp."). When a person of ordinary skill uses an identified, predictable solution

to solve a problem, "it is likely the product not of innovation but of ordinary skill and common sense." *Id*. at 402-03.

In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. at 417. If a person of ordinary skill can implement a predictable variation, § 103 bars its patentability. *Id*. The rationale to combine or modify prior art references is significantly stronger when references seek to solve similar problems, come from the same field, and correspond well with one another. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

The references share commonalities in terms of their general subject matter as well as the types of equipment, products, systems, and/or methods used. Further, the prior art references explicitly or implicitly reference other prior art references, share common authors or inventors, were published in the same journals, were compiled by a common author of a compilation or reference book, were presented at the same conferences, and/or were developed at common companies, schools, or organizations which would motivate one of skill in the art to combine them. Additionally, the references, and any products, devices, or processes described in the references, existed and/or were invented in the same time period providing further motivation for combination.

These disclosures are provided without prejudice to any arguments or objections concerning the relevance of motivation to combine in connection with any invalidity contentions. Respondents reserve the right to further specify the motivations to combine the prior art in response to positions that Complainant may take later in this Investigation and as discovery proceeds. Respondents may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. Moreover, Respondents

reserve the right to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the ’233 Patent.

One or more combinations of the prior art references identified in Exhibits A-1 through A-12 would have been obvious because these references would have been combined using a simple substitution of one known, equivalent element for another to obtain predictable results and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Exhibits A-1 through A-12 would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

All the Asserted Claims are directed to an active cable. Such technology was widely known before the alleged priority date of the ’233 Patent, as evidenced by the references in Exhibits A-1 through A-12. *See, e.g.*, Exs. A-1 (Lugthart ’414); A-2 (Lugthart ’431); A-3 (Cornelius); A-4 (TI DS110DF111); A-5 (TI DS125DF410); A-6 (TI DS250DF410); A-7 (TI DS250DF810); A-8 (Vijayaraghavan); A-9 (Carter); A-10 (Baker incorporating Cornelius); A-11 (SMP9 Cable); A-12 (Secondary References).

The prior art references provide motivations to combine because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in an active cable device could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the ’233 Patent.

Additional motivations to combine specific references are discussed below.

4.1.1.1. Exemplary Motivations to Combine for the ’233 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references described in Exhibits A-01 – A-12, or any reference disclosed above with a reasonable expectation of success, to perform the teachings of signal conditioning functionalities, including data recovery, re-modulation, and pre-equalization, in a cable used for high-speed data communications. The ’233 patent recognizes that active cables containing certain data processing functionality were well known in the art prior to the priority date of the ’233 patent. *See* ’233 patent at 1:6-36.

For example, a person of ordinary skill in the art would have been motivated to combine U.S. Patent No. 10,148,414 (“Lugthart ’414”) with U.S. Patent No. 7,233,617 (“Gorecki”) to render obvious claims 1–6, 8–13, and 15–19 and would have reasonable expected such combination to be successful.

Lugthart ’414 was filed on June 30, 2017, was published October 19, 2017, was issued on December 12, 2018, and claims domestic priority to at least U.S. Patent Application No.

14,581,979 filed on December 23, 2014. Lugthart '414 qualifies as prior art under 35 U.S.C. § 102(a)(1) (AIA) and 35 U.S.C. § 102(a)(2) (AIA).

Lugthart '414 discloses an "active cable" that "includes… first and second transceiver assemblies 105a, 105b positioned at either end of… conductive lines 111." *See* Lugthart '414 at 14:32-37, Fig. 2A (below).

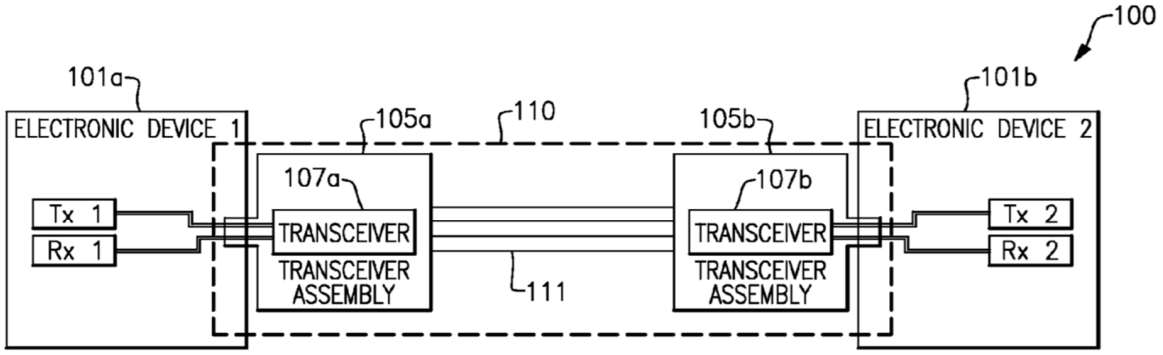
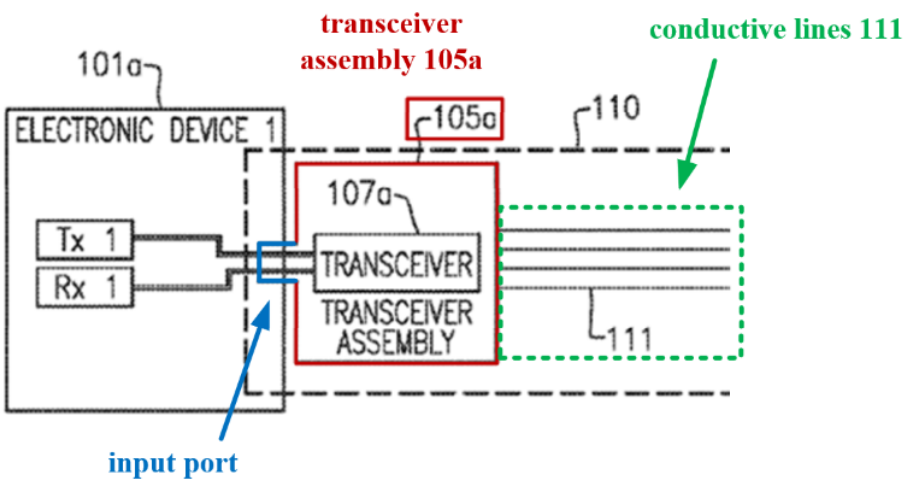


FIG.2A

The electronic components of an active cable improve signal quality. *See, e.g.*, Lugthart '414 at 14:32-34. The transceiver assemblies 105a, 105b include transceivers 107a, 107b, respectively. *See id*. at 14:50-56, Fig. 2A. Each transceiver assembly has a "host side" electrically connected to a host (termed an "electronic device") and a "line side" electrically connected to one end of the cable's conductive lines 111. *See id*. at 14:36-45, Fig. 2A (annotated detail below).



Each transceiver assembly's input port comprises a connector, such as an industry standard SFP or QSFP connector, that "is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable." *See id.* at 15:49-59, Figs. 2A, 17A, 17B, 18.

The transceivers 107a/107b of Lugthart '414 can perform pre-equalization (which Lugthart '414 calls pre-emphasis) on signals transmitted over the cable's conductive lines 111, as well as on signals transmitted to electronic devices 101a/101b. *See, e.g., id.* at 23:67-24:2, 29:25-30.

Figure 1A's transceiver 10 illustrates one embodiment of Figure 2A's pluggable module transceiver 107a/107b. *See, e.g., id.* at 14:50-56.

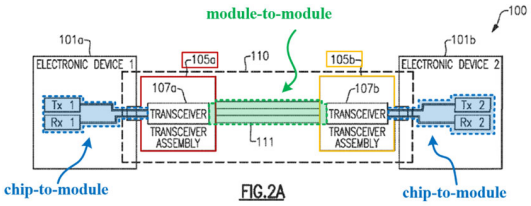


FIG.2A

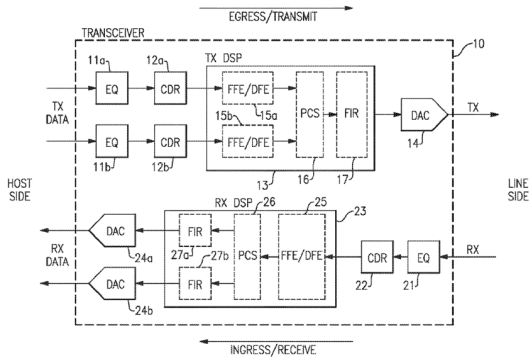


FIG.1A

Transceiver 10's "EGRESS/TRANSMIT" path through DSP 13 performs digital signal processing, including retiming, on the multi-lane TX DATA signal before transmitting the TX signal over conductive lines 111. *See, e.g., id*. at 16:4-10, 21:42-49, Figs. 1A, 2A. The finite impulse response (FIR) filter 17 is a transmit filter that performs pre-emphasis on the re-timed TX signal transmitted over conductive lines 111. *See, e.g., id*. at 16:17-22, 29:25-30.

Lugthart '414 configures FIR filters using "tap coefficients," and the filters "perform emphasis on the signal to compensate for channel losses." *See id*. at 22:19-23, 23:64-24:7. "Pre-emphasis" and "pre-equalization" were used interchangeably in the art. *See, e.g.*, U.S. Patent No. 8,787,430 at 2:39-41 (describing a "technique for combating ISI [inter-symbol interference]… known as 'pre-emphasis', or pre-equalization"); *see also* U.S. Patent No. 9,806,812 at 7:54-55; U.S. Patent No. 9,137,063 at 3:24-27; U.S. Patent No. 9,152,257 at 5:4-8. The purpose of pre-equalization is to compensate for anticipated channel distortion on a transmitted signal.

On the "INGRESS/RECEIVE" path, the DSP 23 performs digital signal processing on signal RX received from the cable before that signal is transmitted to the host (electronic device 101a/101b in Figure 2A). *See, e.g.*, Lugthart '414 at 8:30-36, 9:42-55, Fig. 1A. The DSP 23 includes FIR filters 27a/27b. *See, e.g.*, *id*. at 9:42-50. The DSP 23 uses these FIR filters for "adaptive and configurable signal conditioning features such as… output pre-emphasis" on the signal transmitted to the host. *See, e.g.*, *id*. at 9:56-59, 29:25-30. In one exemplary embodiment, Lugthart '414 describes a five-tap FIR 17 and 27a/27b. *See, e.g.*, *id*. at 22:19-23.

Gorecki was filed on April 10, 2003, was published on April 15, 2004, and claims domestic priority to U.S. Patent Application No. 10/269,446 filed on October 11, 2002. Gorecki qualifies as prior art under 35 U.S.C. § 102(a)(1) (AIA) and 35 U.S.C. § 102(a)(2) (AIA).

Gorecki describes systems and methods for transmitter equalization (*e.g.*, "pre-emphasis equalization" or pre-equalization) by FIR transmit filters in high-speed digital communication systems, including cables. *See, e.g.*, Gorecki at Abstract, 1:15-17, 1:59-2:11, 19:61-66. Gorecki explains that it was known to digitally equalize data, thus implementing FIR filters in digital signal processing, before converting the equalized signals to analog. *See, e.g., id*. at 16:40-46.

Gorecki describes storing FIR filter tap coefficients in non-volatile memory ("NVM") including writable NVM (*e.g.*, "ROM, PROM, EPROM, EEPROM or the like"). *See, e.g., id*. at 7:18-43, 10:37-51, 17:41-51. EEPROM is electrically erasable programmable read only memory that is rewritable Flash memory was another well-known rewritable non-volatile memory (e.g., "EEPROM or the like") conventionally used with transmit FIR filters *See, e.g.*, U.S. Patent No. 6,975,140 at 3:42-4:2 ("Any type of NVRAM can be used as the rewritable non-volatile storage, so long as [it] is of the type suitable for integration on an integrated circuit.").

Gorecki's filter taps are programmable. *See, e.g.,* Gorecki at 3:42-45. "In this way, the transmitter may access the memory to retrieve the necessary information during start-up/power-up, initialization or re-initialization." *See, e.g., id*. at 7:31-33. Gorecki describes a "controller" that adjusts equalizer tap coefficients by distributing filter coefficient values from its non-volatile memory to a transmitter to implement FIR filter taps "within the equalization circuitry." *See, e.g., id*. at 7:9-17.

Gorecki also explains the filter coefficients stored in its non-volatile memory can be "re-programmed." *See, e.g., id*. at 7:18-26, 20:41-43 (claim 2, "pre-programmed [tap] coefficient… is… re-programmed"). The filter coefficients can also be "fine-tuned" using adaptive algorithms. *See, e.g., id*. at 7:50-61, 10:26-51.

Although Lugthart ’414 describes multi-tap transmit filters (FIR 17) and their implementation, Lugthart ’414 does not explain in detail how to set the transmit filter coefficients and thus leaves the implementation details to the ordinarily skilled artisan. *See, e.g.*, Lugthart ’414 at 22:19-23 (describing five-tap filter), Fig. 2A.

An ordinarily skilled artisan would have had multiple reasons to configure the transmit filters disclosed in Lugthart ’414 in view of the approach of using coefficients stored in non-volatile memory, as taught by Gorecki, and would have reasonably expected that such a configuration would work. *First*, Gorecki is directed to “enhancing the performance of high-speed digital communications through a communications channel.” *See* Gorecki at 1:15-17, 6:4-5, 19:61-66. Gorecki further explains that “[t]he extent of equalization introduced by the circuitry, however, may vary between equalization circuitry of each transmitter in the high-speed digital communication system.” *See id*. at 8:66-9:2. For each transmitter, “the amount of equalization may be adjusted or controlled by… changing the coefficients of the taps[.]” *See id*. at 9:37-40. The equalizers are “configured to introduce compensation that is ideally the inverse of the effects caused by the communications channel.” *See id*. at 9:8-10. Gorecki achieves this result by storing and loading equalization parameters, including transmit filter coefficient values, from “ROM, PROM, EPROM, EEPROM or the like” (i.e., non-volatile memory). *See id*. at 7:25. Thus, an ordinarily skilled artisan would have understood that “performance of high-speed digital communications” could be enhanced by using transmit filter coefficient values stored in non-volatile memories.

Second, having a transmitter being able to “access the memory” to retrieve the filter coefficient values and program an equalizer (including setting pre-equalizer filter taps) with those values when Lugthart ’414 ’s transceiver is powered up, initialized, or re-initialized was a

conventional and convenient technique for setting filter coefficients while persisting the coefficient values for use as power to the AEC transceiver was cycled. *See, e.g.*, Gorecki at 7:18-42. An ordinarily skilled artisan would have understood that the controller disclosed in Gorecki distributes, to a transmitter, coefficients used for filter taps, and that would have been a conventional technique to implement that transmitter's memory access and setting programmable FIR filter taps. *See, e.g.*, Gorecki at 7:1-17; U.S. Patent No. 6,975,140 at 4:25-38, 9:54-62; U.S. Patent App. Pub. No. 2014/0119425 at [0049]-[0050] (programmable equalizer 56 includes on-board microcontroller 68 that sets equalizer parameters after power-up using values stored in non-volatile memory 70), Fig. 6 (micro-controller 68, EEPROM 70).

Third, provisioning the transceiver disclosed in Lugthart '414 with pre-set filter coefficient values in non-volatile memory would have allowed setting an active cable with initial coefficient values determined at manufacture and/or default pre-set coefficient values for various chip-to-module channel models for host devices that could be used with the active cable.

The resulting Lugthart-Gorecki combination would have combined familiar elements (Lugthart '414 's equalizer and FIR filters with Gorecki's controller, EEPROM or the like, and techniques for programming filter coefficient values from such memory) according to known methods (as demonstrated by Gorecki) yielding no more than predictable results. *KSR Int'l v. Teleflex*, 550 U.S. 398, 416 (2007). The Lugthart-Gorecki combination would have arranged known elements with each performing the same function it had been known to perform. *KSR*, 550 U.S. at 417. An ordinarily skilled artisan would have recognized that the coefficient storage and filter programming techniques disclosed in Gorecki could improve equalization circuitry disclosed in Lugthart '414 in the same manner that those techniques improved the equalization circuitry of Gorecki. *KSR*, 550 U.S. at 417.

An ordinarily skilled artisan would have had a reasonable expectation of success combining Lugthart with Gorecki because the combination used (1) known components with (2) known filter programming and (3) non-volatile coefficient value storage techniques, all of which were within an ordinarily skilled artisan's abilities, and these techniques were conventionally used for pre-equalization. *See, e.g.*, Gorecki at 6:39-67, 7:18-49, 16:40-46 (describing digital pre-equalization); *see also* Lugthart '414 at 8:37-43, 15:35-57, 22:19-23, 29:7-21. As Hsu explains, for example, "[f]lash memory is a non-volatile random access memory (NVRAM) suitable for use as the rewriteable non-volatile storage to store updated control information for operating the FIR transmitter. … Any type of NVRAM can be used as the rewriteable non-volatile storage, so long as such NVRAM is of the type suitable for integration on an integrated circuit chip." *See* U.S. Patent No. 6,975,140 at 3:42-4:3.

As another example, a person of ordinary skill in the art would have been motivated to combine U.S. Patent No. 10,148,414 ("Lugthart '414") with U.S. Patent No. 7,233,617 ("Gorecki") and the IEEE 802.3-2015 - Standard for Ethernet Section 5 ("802.3-2015, Section 5") with a reasonable expectation of success to render obvious claims 7, 14, and 20.

Lugthart '414 and Gorecki have been discussed *supra*.

IEEE 802.3-2015 was published on March 4, 2016.[2] IEEE 802.3-2015 qualifies as prior art under 35 U.S.C. § 102(a)(1) (AIA).

IEEE 802.3-2015 ("802.3-2015") is the 2015 IEEE Standard for Ethernet and comprises six sections provided as Sections 1 through Section 6. *See, e.g.*, 802.3-2015, Section 1 at 21-22 (introduction and identifying sections); *see also id*. at 54 ("This standard defines Ethernet local area, access and metropolitan area networks."). The IEEE 802.3-2015 standard was adopted on

[2] *See* https://ieeexplore.ieee.org/servlet/opac?punumber=7428774.

September 3, 2015 and published March 4, 2016. *See, e.g.*, 802.3-2015, Section 1. The IEEE 802.3-2015 standard is applicant admitted prior art. *See, e.g.*, '233 Patent at 1:6-24, 6:33-45.

The standard defines a three-tap transmit filter for pre-equalization in electrical backplanes (*e.g.*, 10GBASE-KR).[3] *See, e.g.*, 802.3-2015, Section 5 at 490, Fig. 72-11 ("Transmit equalizer example" with taps c(-1), c(0), and c(1)). The same three-tap transmit filter is used for pre-equalization in a chip-to-module link. *See, e.g.*, 802.3-2015, Section 6 at Fig. 85-3 ("Transmit equalizer functional model" below); *see also id*. at 225 ("The 40GBASE-CR4 and 100GBASE-CR10 transmit function includes programmable equalization to compensate for the frequency-dependent loss of the channel and facilitate data recovery at the receiver. … The requirements for the 40GBASE-CR4 and 100GBASE-CR10 transmit equalizer are intended to be similar to the requirements for 10GBASE-KR specified in 72.7.1.10."); *see also id*. at Fig. 92-7, 416 (same transmit filter model for 100GBASE-CR4).[4]

[3] 10GBASE-KR is the "IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane." *See, e.g.*, 802.3-2015, Section 1 at 71 (Definitions §1.4.34).

[4] 40GBASE-CR4 is the IEEE 802.3 Physical Layer specification for 40 Gb/s using 40GBASE-R encoding over four lanes of shielded balanced copper cabling. *See, e.g.*, 802.3-2015, Section 1 at 73 (Definitions §1.4.67). 100GBASE-CR4 and 100GBASE-CR10 are the specifications for 100 Gb/s using 100GBASE-R encoding over four (CR4) and ten (CR10) lanes, respectively, of shielded balanced copper cabling (*See, e.g.*, 802.3-2015, Section 1 at 72 (Definitions "§1.4.53 100GBASE-CR4," "§1.4.54 100GBASE-CR10").

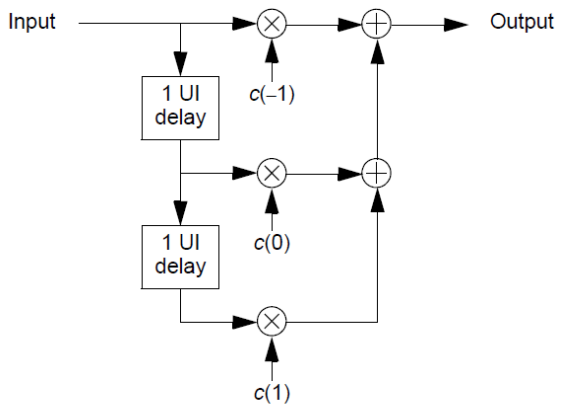


Figure 85–3—Transmit equalizer functional model

Setting the first and third tap coefficient values (*e.g.*, c(-1) and c(1)) to 0, and the second tap coefficient value (e.g., c(0)) to "maximum," passes the input signal without equalization. *See* 802.3-2015, Section 5 at 480 ("If preset is TRUE then the function returns ***the coefficient value equivalent to no equalization*** [c(–1) and c(1) coefficients are set to zero, c(0) set to maximum]."). In other words, the IEEE 802.3-2015 standard specifically defines transmit filter tap settings that disable pre-equalization.

An ordinarily skilled artisan would have had multiple reasons to use the disclosures of IEEE 802.3-2015 to disable transmit equalization in the Lugthart-Gorecki combination (*see supra*) because it was known that disabling filter taps could minimize transceiver power consumption where signal quality was achievable without transmit pre-equalization. An ordinarily skilled artisan would have known that disabling a filter tap would have the same effect as setting a filter tap coefficient value to zero as taught in IEEE 802.3-2015. For example, Zerbe describes transmit pre-equalization and explains that "the FIRs of the transmitter… can be modified to support modes in which… taps can be disabled if not needed to consume minimum power while satisfying the performance or margin objective…. Through a combination of enabling or disabling Tx and Rx DFE taps… the overall system power can be minimized while maintaining adequate margins." *See* U.S. Patent No. 9,137,063 at 27:15-43. An ordinarily skilled artisan would have known that

disabling transmit pre-equalization was a conventional functionality for a transceiver. *See, e.g.*, DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer Datasheet, SNLS482B, Texas Instruments Inc. (January 2017) at 37, Table 14 (describing hexadecimal channel register 1E setting for "Raw Data" in which "FIR filter will not function"); *see also* Gorecki at 18:3-17 (explaining "the leading and/or trailing taps may be 'turned off' or disabled"). Furthermore, an ordinarily skilled artisan would have known that the five-tap transmit filter pre-equalization functionality of Lugthart '414 could be disabled through choice of tap coefficient values in the same manner as the Ethernet Standard taught for its three-tap transmit filter (*e.g.*, by setting certain taps to zero while maximizing the central tap).

The resulting Lugthart-Gorecki-IEEE 802.3 combination provides a mechanism for disabling transmit pre-equalization in FIR 17 and 27a/27b of Lugthart '414. An ordinarily skilled artisan would have disabled pre-equalization in FIR 17 and/or FIR 27a/27b of the Lugthart-Gorecki-IEEE 802.3 combination to reduce power consumption where pre-equalization was not needed to meet signal quality requirements.

Thus, the Lugthart-Gorecki-IEEE 802.3 combination would have combined familiar elements according to known methods yielding no more than predictable results *KSR*, 550 U.S., 416 The combination would have used (1) known methods (disabling FIR filters when pre-equalization was unnecessary) to solve a (2) known problem (reducing power consumption), and (3) would have improved the transceivers and system power consumption of the Lugthart-Gorecki combination in the same way that it improved power consumption in U.S. Patent No. 9,137,063 to Zerbe. *KSR*, 550 U.S. at 417.

An ordinarily skilled artisan would have had a reasonable expectation of success combining Lugthart with Gorecki and IEEE 802.3-2015 because setting filter coefficient values

that disabled pre-equalization in transmit filters was known and described in the Ethernet Standard and other prior art discussed above. The prior art discussed above demonstrates that disabling pre-equalization in transmit filters was within the abilities of an ordinarily skilled artisan. The technique of disabling pre-equalization was conventional for providing lower power mode in transceiver components.

To the extent that it is determined that any of these references do not disclose "a cable," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches using pre-equalization coefficients that are stored in a non-volatile memory. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[pre], claim 8[pre]). For example, a POSITA would have been motivated to incorporate any of the above references with the embodiments of at least each of Musah, Carter, Cornelius, Lugthart 431, Vijayaraghavan, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, and/or any combinations therein where they disclose an embodiment that comprises a cable. *See* Exs. A-2-A-9, A-12. As a specific example, Lugthart 431 discloses an active cable that includes actively powered componentry for improving the performance of the cable. Ex. A-2. As another specific example, Musah discloses an 8-lane cable between a plug receptacles on a pair of devices. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of

success to enable data communications between a pair of host devices. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[f], claim 8[pre]). Implementing an embodiment that comprises a cable form factor would require nothing more than the application of a known solution (using a cable configured to connect a pair of devices for data communications), according to its established function (using the cable for data communications), yielding a predictable result (data communications). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[c], claim 8[c], claim 15[a]). For example, a POSITA would have been motivated to incorporate any of the above references with the embodiments of at least each of Musah, Carter, Cornelius, Lugthart 431, Vijayaraghavan, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, and/or any combinations therein where they disclose using

electrical conductors to convey electrical signals between a pair of devices. *See* Exs. A-2-A-9, A-12. As a specific example, Lugthart 431 discloses a cable that includes conducting lines that can include metal (e.g., copper) conductors. Ex. A-2. As another specific example, Musah discloses an 8-lane cable between a plug receptacles on a pair of devices. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to enable data communications between a pair of devices. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[c], claim 8[c], claim 15[a]). Using electrical conductors between a pair of devices would require nothing more than the application of a known solution (using electrical conductors (e.g., a cable) configured to connect a pair of devices for data communications), according to its established function (using the electrical conductors for data communications), yielding a predictable result (data communications). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a conversion between electrical transit signals and inbound and outbound multi-lane data streams for the first host interface port in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches

converting between electrical transit signals and inbound and outbound multi-lane data streams for the first host interface port. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[d], claim 8[d], claim 15[a]). For example, a POSITA would have been motivated to incorporate any of the above references with the embodiments of at least each of Musah, Carter, Cornelius, Lugthart 431, Vijayaraghavan, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, and/or any combinations therein where they disclose converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port. *See* Exs. A-2-A-9, A-12. As a specific example, Lugthart 431 discloses transceiver devices for converting electrical signals between a host side and a line side of a cable. Ex. A-2. As another specific example, TI DS110DF111, TI DS125DF410, TI DS250DF410, and TI DS250DF810 all each also disclose transceiver devices for converting electrical signals between a host side and a line side of a cable. Exs. A-4-A-7. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to enable data communications between a pair of devices. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[d], claim 8[d], claim 15[a]). Converting between electrical transit signals and inbound and outbound multi-lane data streams for the first host interface port would require nothing more than the application of a known solution (using electrical conductors (e.g., a cable) configured to connect a pair of devices for data communications), according to its established function (processing electrical transit signals that are transmitted via the electrical conductors for data communications), yielding a predictable result (data communications). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices providing preequalization of the electrical transit signals using transmit filter

coefficient values stored in nonvolatile memories," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such preequalization of electrical transit signals using transmit filter coefficient values stored in nonvolatile memories in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches using pre-equalization coefficients that are stored in a non-volatile memory. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[f], claim 8[f], claim 15[c]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of CMIS, Musah, Chung, or Zheng where they disclose transmit filter coefficient values stored in nonvolatile memories, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, Vijayaraghavan, Carter, Cornelius, and/or any combinations therein. *See* Exs. A-2-A-9, A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 1[f], claim 8[f], claim 15[c]). Indeed, the storage of transmit filter coefficient values in nonvolatile memory is but one of a finite number of known, predicable solutions to implement preequalization. Implementing preequalization by using transmit filter coefficient values stored in nonvolatile memory would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function

(using the stored coefficients for preequalization), yielding a predictable result (preequalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "a first controller that configures the first DRR device in response to a power-on event" and "the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a controller that configures the first DRR device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches a controller that configures the first DRR device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 2, claim 9, claim 16[c][d]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of CMIS, Musah, or Zheng, where they disclose configuring a device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, Vijayaraghavan, Carter, Cornelius, and/or any combinations therein. *See* Exs. A-2-A-9, A-12. As a specific

example, CMIS discloses configuring its memory map with filter coefficients in response to a power-up event. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 2, claim 9, claim 16[c][d]). Indeed, providing transmit filter coefficient values from a nonvolatile memory in response to a power-on event is but one of a finite number of known, predicable solutions to implement preequalization. Implementing preequalization by using controller that configures the DRR device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (obtaining the stored coefficients for preequalization in response to detecting a power-on event), yielding a predictable result (preequalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a configuration where the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs in view

of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches a configuration where the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 3, claim 10, claim 17). For example, a POSITA would have been motivated to incorporate the embodiments at least each of CMIS, Musah, Chung, or Zheng, where they disclose devices that are programmed to use the transmit coefficient values each time power is supplied, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, Vijayaraghavan, Carter, Cornelius, and/or any combinations therein. *See* Exs. A-2-A-9, A-12. As a specific example, CMIS discloses configuring its memory map with filter coefficients in response to a power-up event. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 3, claim 10, claim 17). Indeed, programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs is but one of a finite number of known, predicable solutions to implement preequalization. Implementing preequalization by programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end

connector plugs), yielding a predictable result (preequalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a configuration where the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches a configuration where the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 4, claim 11, claim 18). For example, a POSITA would have been motivated to incorporate the embodiments at least each of CMIS, Musah, Chung, Zheng, where they disclose transmit filter coefficient values that are determined and stored in the nonvolatile memories after assembly of the cable, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, Vijayaraghavan, Carter, Cornelius, and/or any combinations therein. *See* Exs. A-2-A-9, A-12. As a specific example, CMIS discloses configuring or updating its memory map with filter coefficients before or during operation, which occurs after the assembly of the cable. Ex. A-

12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 4, claim 11, claim 18). Indeed, the determination and storage of transmit filter coefficient values in nonvolatile memory after the assembly of a cable is but one of a finite number of known, predicable solutions to implement preequalization. Implementing preequalization by using transmit filter coefficient values that are determined and stored in nonvolatile memory after the assembly of a cable would thus require nothing more than the application of a known solution (providing a nonvolatile memory), according to its established function (determining and storing coefficients for preequalization in the nonvolatile memory after the cable is assembled and operational), yielding a predictable result (stored transmit filter coefficient values for preequalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, Baker, Ishaug, Piehler, Unger, Tremblay-740, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a configuration where the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values

stored in the nonvolatile memories in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Baker, Ishaug, Piehler, Unger, Tremblay-740, or Zheng, each of which a configuration where the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 5, claim 12, claim 19). For example, a POSITA would have been motivated to incorporate the embodiments at least each of CMIS, Musah, Chung, Zheng, where they disclose employing receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, Vijayaraghavan, Carter, Cornelius, and/or any combinations therein. *See* Exs. A-2-A-9, A-12. As a specific example, Lugthart 431 discloses a receiver-based equalizer that are configured to equalize electrical transit signals using coefficient values stored in the nonvolatile memories. Ex. A-2. As another specific example, TI DS110DF111, TI DS125DF410, TI DS250DF410, and TI DS250DF810 all each also disclose a receiver-based equalizer that are configured to equalize electrical transit signals using coefficient values stored in the nonvolatile memories. Exs. A-4-A-7. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 5, claim 12, claim 19). Indeed, employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories is but one of a finite number of known, predicable solutions to implement equalization. Implementing receiver-based equalization of the electrical transit signals

using coefficient values stored in the nonvolatile memories would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (using the stored coefficients for equalization), yielding a predictable result (equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Baker, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such electrical conductors comprising twin-axial conductors that carry each of the electrical transit signals in differential form in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Baker, or Zheng, each of which teaches electrical conductors comprising twin-axial conductors that carry each of the electrical transit signals in differential form. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 6, claim 13). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so. For example, a POSITA would have been motivated to incorporate the embodiments at least each of Musah, Chung, Riani, or Zheng, where they disclose electrical conductors comprising twin-axial conductors that carry each of the electrical transit signals in differential form, with the embodiments of at least Lugthart 431,

TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, Vijayaraghavan, Carter, Cornelius, and/or any combinations therein. *See* Exs. A-2-A-9, A-12. As a specific example, Riani discloses using twin-axial conductors that carry each of the electrical transit signals in differential form. Ex, A-12. As another specific example, TI DS110DF111, TI DS125DF410, TI DS250DF410, and TI DS250DF810 all each also disclose using twin-axial conductors that carry each of the electrical transit signals in differential form. Exs. A-4-A-7. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the signal to noise ratio of transmitted signals for data communications. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 6, claim 13). Indeed, using twin-axial conductors that carry each of the electrical transit signals in differential form is but one of a finite number of known, predicable solutions to implement data communications. Implementing data communications by using twin-axial conductors that carry each of the electrical transit signals in differential form would thus require nothing more than the application of a known solution (configuring twin-axial conductors that carry each of the electrical transit signals in differential form between a pair of devices), according to its established function (using the twin-axial conductors configured to carry each of the electrical transit signals in differential form for data communications), yielding a predictable result (data communications). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, Zheng, or any

combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a configuration where the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, CMIS, Chung, Vijayaraghavan, Carter, Cornelius, Musah, Riani, or Zheng, each of which teaches using a configuration where the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 7, claim 14, claim 20). For example, a POSITA would have been motivated to incorporate the embodiments at least each of CMIS, Musah, Riani, or Zheng, where they disclose transmit filter coefficient values stored in nonvolatile memories, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, TI DS250DF410, TI DS250DF810, Vijayaraghavan, Carter, Cornelius, and/or any combinations therein. *See* Exs. A-2-A-9, A-12. As a specific example, CMIS discloses selectively enabling pre-equalization (i.e., selectively not performing) of the multi-lane data streams provided to the first and second host interface ports. Ex. A-12. As another specific example, TI DS110DF111, TI DS125DF410, TI DS250DF410, and TI DS250DF810 all each also disclose selectively enabling pre-equalization (i.e., selectively not performing) of the multi-lane data streams provided to the first and second host interface ports. Exs. A-4-A-7. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-2-A-9, A-12 (claim 7, claim 14, claim 20). Not performing pre-equalization of the multi-lane data streams provided to

the first and second host interface ports would require nothing more than the application of a known solution (providing the ability to selectively perform pre-equalization of the multi-lane data streams), according to its established function (selectively performing pre-equalization of the multi-lane data streams), yielding a predictable result (selective preequalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

Similarly, a POSITA would have been motivated to combine Baker in view of either Lugthart 431/414/993, Ishaug, Piehler, Unger, Gorecki-617, Tremblay-740 (A-12), or a combination thereof, with a reasonable expecation of success. These references are in the same field of invention and have compatible and complementary teachings. A POSITA would have also been motivated to additionally combine Baker with Cornelius-705 or Cornelius-238 with a reasonable expecation of success because Baker expressly points to the teachings of those references to explain how to implement its invention.

It would have been obvious to apply the pre-equalization techniques taught by Lugthart 431/414/993, Ishaug, Piehler, Unger, Gorecki-617, and Tremblay-740 to Baker's active cable with a reasonable expectation of success. As discussed above, pre-equalization techniques are well known to have been applied to active cables. Lugthart 431/414/993, Ishaug, Piehler, Unger, Tremblay-740 each teach pre-equalization. See, e.g., Exhibits A-2-A-9, A-12 (claim 1[f], claim 8[f], claim 15[c]). These references are all in the same field of invention. A POSITA would understand that transmitter-side pre-equalization improves signal integrity by compensating for channel-induced distortion, including inter-symbol interference (ISI) and high-frequency attenuation. A POSITA would have been motivated by the growing demand for higher data rates, longer cable lengths, and improved signal integrity without burdening host devices. Thus,

integrating pre-equalization in the transmitters of active cables would have been a predictable solution with a reasonable expectation of success. Indeed, the storage of transmit filter coefficient values in nonvolatile memory is but one of a finite number of known, predicable solutions to implement preequalization. Implementing preequalization by using transmit filter coefficient values stored in nonvolatile memory would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (using the stored coefficients for preequalization), yielding a predictable result (preequalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined one of the above references does not disclose configuring "the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring" it would have been obvious in further view of Ishaug with a reasonable expectation of success. Ishaug disclosing configuring predistortion circuitry at power up. Ishaug at 4:51-5:54. It would have been obvious to modify the teachings of any of the above recited references to include Ishaug's teaching of power-on configuration. Implementing Ishaug's teaching of power-on configuration would require nothing more than the application of a known solution (power-on configuration), according to its established function, yielding a predictable result. Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined Baker does not disclose configuring "the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form" it would have been obvious in further view of Lugthart-414/434/993, for the

reasons discussed above, with a reasonable expectation of success. Lugthart-414/434/993 disclose twin-axial conductors that carry differential signals. See e.g., Lugthart-993 at Fig. 3a. Twin-axial conductors that carry each of the electrical transit signals in differential form were commonly used in active cables at the time of the alleged invention. It would have been obvious to modify the teachings of any of the above recited references to use twin-axial conductors carrying differential signals. Implementing twin-axial conductors would require nothing more than applying a known solution (twin-axial conductors), according to their established function, yielding a predictable result. Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with Gorecki, CMIS, Chung, Musah, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such pre-equalization of electrical transit signals using transmit filter coefficient values stored in nonvolatile memories in view of the teachings of at least the knowledge of a POSITA and/or one or more of Gorecki, CMIS, Chung, Musah, or Zheng, each of which teaches using pre-equalization coefficients that are stored in a non-volatile memory. *See, e.g.*, Exhibits A-11 – A-12 (claim 1[f], claim 8[f], claim 15[c]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Gorecki, CMIS, Musah, Chung, or Zheng where they disclose transmit filter coefficient values stored in nonvolatile memories, with the embodiments of the SMP9 Cable. *See* Exs. A-11 – A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation

of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-11 – A-12 (claim 1[f], claim 8[f], claim 15[c]), Indeed, the storage of transmit filter coefficient values in nonvolatile memory is but one of a finite number of known, predicable solutions to implement pre-equalization. Implementing pre-equalization by using transmit filter coefficient values stored in nonvolatile memory would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (using the stored coefficients for pre-equalization), yielding a predictable result (pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "a first controller that configures the first DRR device in response to a power-on event" and "the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with Gorecki, CMIS, Chung, Musah, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a controller that configures the first DRR device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event in view of the teachings of at least the knowledge of a POSITA and/or one or more of Gorecki, CMIS, Chung, Musah, Zheng, each of which teaches a controller that configures the first DRR device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event. *See, e.g.*, Exhibits A-11 – A-12 (claim 2, claim 9, claim 16[c][d]). For example, a POSITA would have been motivated to

incorporate the embodiments at least each of Gorecki, CMIS, Musah, or Zheng, where they disclose configuring a device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event, with the embodiments of the SMP9 Cable, and/or any combinations therein. *See* Exs. A-11 – A-12. As a specific example, CMIS discloses configuring its memory map with filter coefficients in response to a power-up event. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A11 – A-12 (claim 2, claim 9, claim 16[c][d]). Indeed, providing transmit filter coefficient values from a nonvolatile memory in response to a power-on event is but one of a finite number of known, predicable solutions to implement pre-equalization. Implementing pre-equalization by using controller that configures the DRR device with transmit filter coefficient values from an internal nonvolatile memory in response to a power-on event would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (obtaining the stored coefficients for pre-equalization in response to detecting a power-on event), yielding a predictable result (pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with Gorecki, CMIS, Chung, Musah, Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to

modify the teachings of any of the above recited references to include such a configuration where the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs in view of the teachings of at least the knowledge of a POSITA and/or one or more of Gorecki, CMIS, Chung, Musah, or Zheng, each of which teaches a configuration where the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs. *See, e.g.*, Exhibits A-11 – A-12 (claim 3, claim 10, claim 17). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Gorecki, CMIS, Chung, Musah, or Zheng, where they disclose devices that are programmed to use the transmit coefficient values each time power is supplied, with the embodiments of the SMP9 Cable. *See* Exs. A-11 – A-12. As a specific example, CMIS discloses configuring its memory map with filter coefficients in response to a power-up event. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-11 – A-12 (claim 3, claim 10, claim 17). Indeed, programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs is but one of a finite number of known, predicable solutions to implement pre-equalization. Implementing pre-equalization by programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs),

yielding a predictable result (pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with Gorecki, CMIS, Chung, Musah, and Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a configuration where the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Gorecki, CMIS, Chung, Musah, and Zheng, each of which teaches a configuration where the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable. *See, e.g.*, Exhibits A-11 – A-12 (claim 4, claim 11, claim 18). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Gorecki, CMIS, Musah, Chung, or Zheng, where they disclose transmit filter coefficient values that are determined and stored in the nonvolatile memories after assembly of the cable, with the embodiments of the SMP9 Cable. *See* Exs. A-11 – A-12. As a specific example, CMIS discloses configuring or updating its memory map with filter coefficients before or during operation, which occurs after the assembly of the cable. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-11 – A-12 (claim 4, claim 11, claim 18). Indeed, the determination and storage

of transmit filter coefficient values in nonvolatile memory after the assembly of a cable is but one of a finite number of known, predicable solutions to implement pre-equalization. Implementing pre-equalization by using transmit filter coefficient values that are determined and stored in nonvolatile memory after the assembly of a cable would thus require nothing more than the application of a known solution (providing a nonvolatile memory), according to its established function (determining and storing coefficients for pre-equalization in the nonvolatile memory after the cable is assembled and operational), yielding a predictable result (stored transmit filter coefficient values for pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with Gorecki, CMIS, Chung, Musah, and Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a configuration where the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories in view of the teachings of at least the knowledge of a POSITA and/or one or more of Gorecki, CMIS, Chung, Musah, and Zheng, each of which a configuration where the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories. *See, e.g.*, Exhibits A-11 – A-12 (claim 5, claim 12, claim 19). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Gorecki, CMIS,

Musah, Chung, or Zheng, where they disclose employing receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories, with the embodiments of the SMP9 Cable. *See* Exs. A-11 – A-12. As a specific example, Lugthart 431 discloses a receiver-based equalizer that are configured to equalize electrical transit signals using coefficient values stored in the nonvolatile memories. Ex. A-2. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-11 – A-12 (claim 5, claim 12, claim 19). Indeed, employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories is but one of a finite number of known, predicable solutions to implement equalization. Implementing receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories would thus require nothing more than the application of a known solution (storing coefficients in nonvolatile memory), according to its established function (using the stored coefficients for equalization), yielding a predictable result (equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with Gorecki, CMIS, Musah, Chung, or Zheng, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such a configuration where

the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports in view of the teachings of at least the knowledge of a POSITA and/or one or more of Gorecki, CMIS, Musah, Chung, or Zheng, each of which teaches using a configuration where the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports. *See, e.g.*, Exhibits A-11 – A-12 (claim 7, claim 14, claim 20). For example, a POSITA would have been motivated to incorporate the embodiments at least each of CMIS, Musah, Riani, or Zheng, where they disclose transmit filter coefficient values stored in nonvolatile memories, with the embodiments of the SMP9 Cable. *See* Exs. A-211 – A-12. As a specific example, CMIS discloses selectively enabling pre-equalization (i.e., selectively not performing) of the multi-lane data streams provided to the first and second host interface ports. Ex. A-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to improve the repeatability and efficiency of providing transmit filter coefficient values to equalizers for improving the signal to noise ratio of transmitted signals. *See, e.g.*, Exhibits A-11 – A-12 (claim 7, claim 14, claim 20). Not performing pre-equalization of the multi-lane data streams provided to the first and second host interface ports would require nothing more than the application of a known solution (providing the ability to selectively perform pre-equalization of the multi-lane data streams), according to its established function (selectively performing pre-equalization of the multi-lane data streams), yielding a predictable result (selective pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such a combination and would have had a reasonable expectation of success in doing so.

Complainant has yet to indicate a belief that any of the prior art references do not supply any of the claim limitations. Respondents' motivations to combine the prior art to supply other

limitations may be amended or supplemented in view of Complainant's contentions regarding the missing limitations in the prior art references.

Secondary Considerations

Respondents are not aware of any secondary-considerations evidence demonstrating non-obviousness of the Asserted Claims of the '233 Patent. Complainant has not produced any documents related to secondary considerations, nor has Complainant identified any such secondary considerations, let alone demonstrated a nexus between any such considerations and the alleged inventions of the Asserted Claims of the '233 Patent.

As discussed in Appendix A, the prior art references confirm that the Asserted Claims of the '233 Patent would have been obvious to a POSITA before the earliest possible priority date. Respondents reserve the right to supplement or modify these factors to address any evidence or arguments later identified by Complainants.

Invalidity Grounds Under 35 U.S.C. § 112

Subject to Respondents' reservation of rights above, Respondents identify their grounds of invalidity for the '233 Patent based on lack of enablement, written description, and indefiniteness pursuant to 35 U.S.C. §§ 112(a) and (b) below. The terms recited below are invalid based on lack of enablement, written description, and indefiniteness pursuant to 35 U.S.C. §§ 112(a) and (b) under any scope of the claim terms. If, however, an overbroad construction is applied, at least under the overbroad constructions that Complainants appear to be applying to the Asserted Claims of the '233 Patent, which go beyond (and are not adequately described or enabled by) the purported inventions allegedly disclosed in the '233 Patent, the claims are invalid for that additional reason. Specifically, to the extent that Complainants assert that the Asserted Claims of the '233 Patent are so broad as to cover the Respondents' respective Accused Products and alleged domestic industry

products, or to the extent that they may eventually be construed so broadly, such an interpretation or construction would render the Asserted Claims of the ’233 Patent invalid for failure to meet the requirements of 35 U.S.C. § 112. A more detailed discussion of Respondents’ written description, enablement, and indefiniteness defenses will be set forth in Respondents’ expert report(s) on invalidity.

Lack of Written Description and/or Enablement

The ’233 Patent does not provide sufficient written description to establish that the applicants were in possession of the alleged inventions recited in certain of the Asserted Claims at the time the ’233 Patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that “reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus.

The specification of the ’233 Patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the Asserted Claims without undue experimentation. To the extent the following limitations are definite, the application that became the ’233 Patent fails to sufficiently describe or enable them as required:

Term	Relevant Claim(s)	Basis
“the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories”	1–7	The patent does not describe and there is insufficient disclosure to allow a POSITA to make and use a device “providing pre-equalization of the electric transit signals”.
“the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories”	8–14	

Term	Relevant Claim(s)	Basis
"the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories"	15–20	
"electrical conductors connecting the first and second DRR devices to convey electrical transit signals therebetween" "connecting electrical conductors to the first and second DRR devices to convey electrical transit signals therebetween," "conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; …. Conveyed by electrical conductors to the first DRR device"	1–7 8–14 15–20	The patent does not describe and there is insufficient disclosure to allow a POSITA to make and use a device having "electrical conductors" to connect the first and second DRR devices and to convey electrical transit signals therebetween.

Indefiniteness

Certain of the Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the Asserted Claims are indefinite in whole, in part or in combination:

Term	Relevant Claim(s)	Basis
"carry each of the electrical transit signals in differential form"	6	The claims, read in light of the specification and prosecution history, fail to inform, with reasonable certainty, what "differential form" means.

Term	Relevant Claim(s)	Basis
"a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug" "a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug"	1, 8, 15	The claims, read in light of the specification and prosecution history, fail to inform, with reasonable certainty, what the term "re-modulation" means. The term "modulation" is used in the specification in multiple contexts. For example, the specification states that "receiver 400 receives an analog electrical signal (CH_IN) and supplies it to an optional low noise amplifier." *See* 233 Patent at 7:42-45. The Specification continues to state that, after passing through a CTLE and FFE, a "decision feedback equalizer (DFE) 404 operates on the filtered signal to correct for trailing ISI an detect each transmitted channel bit or symbol, thereby producing a demodulated digital data stream." *See* 233 Patent at 7:45-58. Thereafter, the specification further states that the "symbols or data blocks are placed on the digital receive bus (RXD) for remodulation and transmission by a transmitter to the remote end of the channel." 233 Patent at 7:64-67. In other contexts, however, the 233 Patent discusses modulation with respect to the type of modulation scheme employed (e.g., PAM4 or NRZ). *See* 233 Patent at 4:24-45. The 233 Patent specifically contemplates that the "DRR devices may provide format conversion by , e.g., converting 1 lane of PAM4 symbols into 2

Term	Relevant Claim(s)	Basis
		lanes of NRZ symbols, and vice versa." 233 Patent at 4:43-45. Given the inconsistent use of the term in the specification and the lack of guidance in the claims, the claims of the 233 patent are indefinite, as they fail to provide reasonable certainty as to the meaning of the term "re-modulation."
"a first data recovery and re-modulation (DRR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug"	1	Claim 1 is an apparatus claim that purports to be directed to "A cable" comprising multiple elements. This limitation, however, requires the step of "*exchanges* inbound and outbound multi-lane data streams" and thus injects a method step into an apparatus claim. The inclusion of this step within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
"a second DRR device that exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and"	1	Claim 1 is an apparatus claim that purports to be directed to "A cable" comprising multiple elements. This limitation, however, requires the step of "*exchanges* inbound and outbound multi-lane data streams" and thus injects a method step into an apparatus claim. The inclusion of this step within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*,

Term	Relevant Claim(s)	Basis
		Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
"the first DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the first host interface port, and"	1	Claim 1 is an apparatus claim that purports to be directed to "A cable" comprising multiple elements. This limitation, however, requires the step of "*converting* between said electrical transit signals and said inbound and outbound multi-land data streams" and thus injects a method step into an apparatus claim. The inclusion of this step within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
"the second DRR device converting between said electrical transit signals and said inbound and outbound multi-lane data streams for the second host interface port,"	1	Claim 1 is an apparatus claim that purports to be directed to "A cable" comprising multiple elements. This limitation, however, requires the step of "*converting* between said electrical transit signals and said inbound and outbound multi-land data streams" and thus injects a method step into an apparatus claim. The inclusion of this step within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
"the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories."	1	Claim 1 is an apparatus claim that is directed to "A cable" comprising multiple elements. This limitation, however, requires the steps of "*providing* pre-equalization of the electrical

Term	Relevant Claim(s)	Basis
		transit signals" and doing so "*using* transmit filter coefficient values stored in nonvolatile memory" and thus injects method steps into an apparatus claim. The inclusion of these steps within an apparatus claim would not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
"2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring."	2	Claim 2 is an apparatus claim that is directed to "The cable of claim 1." The additional limitations of this claim, however, requires the steps of "*configures* the first DRR device in response to a power-on event" and "*retrieving* the transmit filter coefficient values from the nonvolatile memories" and thus injects method steps into an apparatus claim. The inclusion of these steps within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.	4	Claim 4 is an apparatus claim that is directed to "The cable of claim 3." The additional limitations of this claim, however, require the steps of "the transmit filter coefficient values are *determined* and *stored* in in the nonvolatile memories *after* assembly of the cable" and thus injects method steps into an apparatus claim.

Term	Relevant Claim(s)	Basis
		The inclusion of these steps within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.	5	Claim 5 is an apparatus claim that is directed to "The cable of claim 4." The additional limitations of this claim, however, require the step of the "first and second DRR devices *employ* receiver-based equalization of the electrical transit signals *using* coefficient values stored in the nonvolatile memories" and thus injects a method step into an apparatus claim. The inclusion of this step within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	7	Claim 7 is an apparatus claim that is directed to "The cable of claim 1." The additional limitations of this claim, however, requires the step of the "DRR devices *do not perform* pre-equalization" and thus injects a method step into an apparatus claim. The inclusion of this step within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings,*

Term	Relevant Claim(s)	Basis
		L.L.C. v. Amazon.com, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).

Inequitable Conduct

Discovery is ongoing regarding the enforceability of the ’233 Patent. To date, Complainants have refused to disclose any prior art known to Complainants, those involved in prosecution, or known to the inventors, outside of what is identified in the prosecution history and what was disclosed to it by third parties in litigation.

In view of Complainants’ continued obstruction to relevant discovery, Respondents reserve the right to amend or supplement these contentions as discovery progresses including in response to, among other things, information learned in fact and/or expert discovery including identification of additional prior art, Complainants’ positions on priority, infringement, claim construction, and/or invalidity, the Court’s rulings, including on claim construction, changes in the Respondents’ respective Accused Products, and in the event Complainants are permitted to revise infringement or domestic industry theories.

Improper Inventorship

Complainants have yet to provide discovery concerning each named inventor’s participation, involvement, and contribution to the conception and reduction to practice of the alleged invention, including the dates of such participation, involvement, and contribution to the conception and reduction to practice on an element-by-element basis. *See, e.g.*, Respondents’ Common Interrogatory No. 27. Respondents reserve their rights to contend, based on further discovery, that the Asserted Claims of the ’233 Patent are invalid and/or unenforceable due to misjoinder of one or more inventors, nonjoinder of one or more inventors, or derivation of the claimed inventions from another.

5. THE ’252 PATENT

Priority Date

Complainants have yet to satisfy its burden of proving that any of the Asserted Claims of the ’252 Patent are entitled to a priority date prior to the filing date of its application, August 13, 2019. Because Complainants have not shown that Chinese Application No. CN201910155535.9 (“’535.9 Application”) provides written description support for the Asserted Claims, Complainants are not entitled to the priority date of March 1, 2019, the filing date of that application. Additionally, because Complainants have not shown that any of the Asserted Claims of the ’252 Patent were conceived or reduced to practice, actually or constructively, prior to the filing date of the ’252 Patent, none of the Asserted Claims of the ’252 Patent are entitled to a date of invention that is earlier than the filing date, August 13, 2019. Respondents reserve the right to supplement and amend its Initial Contentions should Complainants subsequently identify alleged support for its claimed priority date.

The ’535.9 Application does not support any of the Asserted Claims of the ’252 Patent. For example, at a minimum, the ’535.9 Application does not disclose:

- “wherein cable dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters,” (claims 7–10);

Subject Matter Eligibility Grounds Under 35 U.S.C. § 101

As shown in Exhibits B-1 through B-11, each of the limitations of the Asserted Claims of the ’252 Patent, individually and in combination with the other elements of each claim, were well

understood, routine, and conventional in the industry at the time. Exhibits B-1 through B-11 cite a number of prior art references as evidence of the description of the industry at the relevant time and how the various claim elements were well understood, routine, and conventional (alone and in combination). The prior art references referred to are exemplary only.

The information provided in prior art references and cited herein and in Exhibits B-1 through B-11 should not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Respondents' claim construction disclosures will be provided according to the procedural schedule. Nothing contained in these Initial Contentions should be understood or deemed to be an express or implied admission or contention with respect to the absence of factual disputes relating to patent ineligibility, the absence of a need for construction of any terms in an Asserted Claim, any proper construction of any terms in an Asserted Claim, or alleged infringement of that claim. There is no claim construction issue or factual issue that precludes the Administrative Law Judge finding that the claims of the Asserted Patents are patent-ineligible.

Respondents also reserve the right to rely upon expert testimony as evidence of the description of the industry at the relevant time and how the various claim elements were well understood, routine, and conventional (alone and in combination). Respondents also further incorporate by reference the discussion below providing the exemplary legal and factual bases supporting its Section § 101 contentions. *See infra*.

Furthermore, to the extent the listed prior art discloses and describes particular products that were publicly known and/or in public use, in addition to each publication itself serving to demonstrate that the Asserted Claims of the '252 Patent were well understood, routine, and conventional at the time of filing, the various products described in the publications also serve to

demonstrate that the Asserted Claims of the ’252 Patent were well understood, routine, and conventional at the time of filing.

Respondents also reserve the right to rely upon foreign counterparts of the references identified in these Initial Contentions, U.S. counterparts of foreign patents and foreign patent applications identified in these Initial Contentions, U.S. and foreign patents and patent applications corresponding to articles and publications identified in these Initial Contentions, issued patents corresponding to published patent applications identified in these Initial Contentions, published patent applications corresponding to issued patents identified in these Initial Contentions, and any systems, products, or prior inventions related to any of the references identified in these Initial Contentions.

As discussed below, the limitations of the Asserted Claims of the ’252 Patent recite cables comprised of generic and conventional hardware components, such as non-volatile memory, registers, pre-equalization filters, post-equalization filters, retimers, microcontrollers, and electrical conductors, and the cables and the components therein are used in their known and expected manner. The cables can also comprise software-based functions implemented by firmware stored in the memory and/or the microcontrollers, and the software-based functions are generic and conventional as well (*e.g.*, storing data (e.g., coefficients) to/from memory).

Identification of Asserted Claims That Are Ineligible Under Section 101

’252 Patent Claim	Exception to Eligibility	Factual and Legal Basis	Representative Claim[5]
1	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

[5] Claims 6 and 11 are substantially equivalent in scope to claim 1, therefore claim 1 can be used as representative of claims 6 and 11 for purposes of these Contentions. Claims 2–5, 7–10, and 12–

’252 Patent Claim	Exception to Eligibility	Factual and Legal Basis	Representative Claim[5]
2	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
3	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
4	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
5	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
6	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
7	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
8	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
9	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
10	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

14 have additional limitations that do nothing to make these claims valid under Section 101 and therefore claim 1 can be used as representative of all Asserted Claims for purposes of these Contentions. *See, e.g., Content Extraction,* 776 F.3d at 1349 (affirming that a specific claim is “representative, because all the claims are ‘substantially similar and linked to the same abstract idea’”). Moreover, as discussed in below, each of the Asserted Claims of the ’252 Patent fails to satisfy Section 101 irrespective of whether claim 1 is representative.

’252 Patent Claim	Exception to Eligibility	Factual and Legal Basis	Representative Claim[5]
11	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
12	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
13	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
14	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

Factual and Legal Basis for Subject Matter Ineligibility

***Alice* Step One: The Asserted Claims Are Directed to The Abstract Idea of Transferring and Converting Data**

Representative Independent Claim 1

Representative claim 1 of the ’252 Patent recites as follows:

1. An active Ethernet cable that comprises:

[a] electrical conductors connected between a first connector and a second connector,

[b] each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable,

[c] each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream,

[d] the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, and

[e] the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal.

'252 patent, claim 1.

The plain language of claim 1 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of converting and exchanging data between hosts. Claim 1 does not specify any non-conventional ways of converting and exchanging data. In addition, claim 1 does not provide any new algorithms or methods or techniques for doing so. In effect, claim 1 claims a computer-implemented method of converting and conveying data, and the Federal Circuit has "consistently held that similar claims reciting the collection, transfer, and publishing of data are directed to an abstract idea." *Cellspin Soft, Inc. v. Fitbit, Inc.*, 927 F.3d 1306, 1315 (Fed. Cir. 2019) (citing *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016); *In re TLI Commc'ns. Patent Litig.*, 823 F.3d 607, 610–12 (Fed. Cir. 2016)). *See also Adaptive Streaming Inc. v. Netflix, Inc.*, 836 F.App'x 900, 903 (Fed. Cir. 2020) ("We have held that the ideas of encoding and decoding image data and of converting formats, including when data is received from one medium and sent along through another, are by themselves abstract ideas, and accordingly conclude that claims focused on those general ideas governing basic communication practices, not on any more specific purported advance in implementation ,were directed to abstract ideas."); *Interval Licensing LLC v. AOL, Inc.*, 896 F.3d 1335, 1344 (Fed. Cir. 2019) ("We have recognized that 'information as such is an intangible' and that collecting, analyzing, and displaying that information, without more, is an abstract idea") (cleaned up).

Claim 1 requires the functional result of "conveying," "provid[ing]," "recover[ing]," and "remodulat[ing]," data, but fails to so in a non-abstract way as it does not sufficiently describe how to achieve these results in a non-abstract way. *See, e.g.*, *Two-Way Media Ltd. v. Comcast Cable Commc'ns., LLC*, 847 F.3d 1329, 1338–39 (Fed. Cir. 2017) (holding that "claim 1 manipulates

data but fails to do so in a non-abstract way," because "[t]he claim requires the functional result of 'converting,' 'routing,' 'controlling,' 'monitoring,' and 'accumulating records,' but does not sufficiently describe how to achieve these results in a non-abstract way."); *RecogniCorp LLC v. Nintendo Co., Ltd.*, 855 F.3d 1322, 1326–27 (Fed. Cir. 2017) ("standard encoding and decoding" is "an abstract concept long utilized to transmit information," and "[a] process that started with data, added an algorithm, and ended with a new form of data was directed to an abstract idea"); *Adaptive Stream Inc. v. Netflix, Inc.*, 836 F.App'x 900, 903 (Fed. Cir. 2020) ("We have held that the ideas of encoding and decoding image data and of converting formats, including when data is received from one medium and sent along through another, are by themselves abstract ideas."); *Entropic Commc'ns., LLC v. DISH Network Corp.*, 767 F.Supp.3d 1043, 1058 (C.D. Cal. 2025) ("Sending and receiving data, even in the context of a communication network, is abstract."). Claim 1 is only directed to the aspirational end-result that, somehow, these steps occur. *See also TriDim Innovations LLC v. Amazon.com, Inc.*, 207 F.Supp.3d 1073, 1080 (N.D. Cal. 2016) ("Much like the unpatentable subject matter in TLI Communications, the claims in question here are defined only in terms of their functions . .") (citing *In re TLI*, 823 F.3d at 613); *Affinity Labs of Tex., LLC v. Amazon.com, Inc.*, 838 F.3d 1266, 1269–70 (Fed. Cir. 2016) ("The purely functional nature of the claim confirms that it is directed to an abstract idea . ."); *Elec. Power Grp.*, 830 F.3d at 1354 (ineligible claims provided no "particular . inventive technology for performing those functions").

Turning to the claim language itself, element 1[a] merely adds the requirement that there are electrical conductors connecting the first and second connectors. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the '252 patent's August 13, 2019 filing date and

March 1, 2019 claimed priority date, connecting two connectors with electrical conductors was a conventional and well-known technique. *See, e.g.*, Exs. B-1 – B-11.

Element 1[b] is directed to exchanging data between host devices and the first and second connectors, however, there is no recitation of how the data stream exchange is accomplished that would be indicative of an inventive technological improvement. Additionally, hardware for performing data transfer was generic at least as of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of data recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform an abstract process (data exchange) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Element 1[c] is directed to performing clock and data recovery on electrical input signals to convert it into an electrical transit signal to be conveyed across the electrical connectors, however, there is no recitation of how the clock and data recovery nor conversion is accomplished that would be indicative of any technological improvement. Additionally, hardware for performing clock and data recovery and remodulation was generic at least as of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of recovery and remodulation hardware are recited in these elements. These are abstract

because they describe generic devices (first and second connectors) configured to perform abstract processes (clock and data recovery, remodulation) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Element 1[d] is directed to performing clock and data recovery on the electrical transit signals to convert them into the outbound data stream to be conveyed to the host port, however, there is no recitation of how the clock and data recovery nor conversion is accomplished that would be indicative of any technological improvement. Additionally, hardware for performing clock and data recovery and remodulation was generic at least as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform abstract processes (clock and data recovery, remodulation) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Element 1[f] merely adds the requirement that fixed, cable-independent, equalization parameters are used for the remodulation of the transit data stream and the clock and data recovery performed on the electrical input signal. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way, As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, using fixed, cable-independent, equalization parameters for remodulation of the transit data stream and the clock and data recovery performed on the electrical input signal were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11.

Although Respondents believe that independent claim 1 of the ’252 patent is representative of all Asserted Claims of the ’233 patent (all asserted claims recite the same abstract idea with immaterial and conventional variations), out of an abundance of caution, Respondents will discuss the remaining asserted independent and dependent claims here.

Dependent Claim 2

Dependent claim 2 of the ’252 Patent recites as follows:

> 2. The active Ethernet cable of claim 1, wherein the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal.

’252 patent, claim 2.

The additional limitations recited in dependent claim 2 merely recite additional equalization parameters, which, as stated for claim 1, are abstract. Claim 2 is directed to equalization, however, there is no recitation of how the equalization is performed that would be indicative of an inventive technological improvement, and employing cable-dependent equalization parameters for the remodulation of the inbound data stream and clock and data recovery performed on electrical transit signals was generic as of the ’252 patent’s August 13,

2019 filing date and March 1, 2019 claimed priority date. *See, e.g.*, Exs. B-1 – B-11. Additionally, hardware performing equalization with cable-dependent parameters for the remodulation of the inbound data stream and clock and data recovery performed on electrical transit signals was also generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific types of equalization hardware are recited in the claimed invention. This element is abstract because it describes generic devices configured to perform an abstract process (implied mathematical algorithm of equalization) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or steps recited therein that improve technology or solve a technical problem in a novel way. This claim does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., equalization) in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, equalization of signals conveyed across conductors using adaptively updated parameters was a well-known signal conditioning technique. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 3

Dependent claim 3 of the ’252 Patent recites as follows:

> 3. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable.

’252 patent, claim 3.

The additional limitations recited in dependent claim 3 merely recite additional equalization parameters, which, as stated for claims 1 and 2, are abstract. Claim 3 is directed to equalization, however, there is no recitation of how the equalization is performed that would be indicative of an inventive technological improvement, and using equalization parameters that adapt during usage of the cable as generic as of the ’252 patent’s August 13, 2019 filing date and

March 1, 2019 claimed priority date. *See, e.g.*, Exs. B-1 – B-11. Additionally, hardware performing equalization with adaptively updated parameters was also generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific types of equalization hardware are recited in the claimed invention. This element is abstract because it describes generic devices configured to perform an abstract process (implied mathematical algorithm of equalization with adaptively updated parameters) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or steps recited therein that improve technology or solve a technical problem in a novel way. This claim does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., equalization) in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, equalization of signals conveyed across conductors using adaptively updated parameters was a well-known signal conditioning technique. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 4

Dependent claim 4 of the ’252 Patent recites as follows:

> 4. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable.

’252 patent, claim 4.

The additional limitations recited in dependent claim 4 merely adds the requirement that the equalization parameters are fixed during normal usage and are determined during manufacturing-testing of the cable. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, having

fixed equalization parameters that were determined during manufacturing-testing were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11. In sum, claim 4 only recites abstract ideas, as the additional limitations of claim 4 are neither in isolation nor combined render claim 4 patent eligible.

Dependent Claim 5

Dependent claim 5 of the ’252 Patent recites as follows:

> 5. The active Ethernet cable of claim 4, wherein the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd.

’252 patent, claim 5.

The additional limitations recited in dependent claim 5 merely adds the requirement that the data streams each have a per-lane symbol rate in excess of 50 GBd. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, having fixed equalization parameters that were determined during manufacturing-testing were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11. Indeed, the requirement that the data streams “each have a per-lane symbol rate in excess of 50 GBd” is conventional and well-known and no different than the speeds contemplated in the IEEE 802.3 Ethernet standard. *See, e.g.*, ’252 patent, 1:5-22. In sum, claim 5 only recites abstract ideas, as the additional limitations of claim 5 are neither in isolation nor combined render claim 5 patent eligible.

Independent Claim 6

Independent claim 6 of the ’252 Patent recites as follows:

> 6. A communications method that comprises, in a network cable having conductor pairs electrically connecting a first connector to a second connector:

[a] receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device;

[b] performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream;

[c] re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs;

[d] receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device;

[e] performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream;

[f] re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs;

[g] performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream;

[h] re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device;

[i] performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream; and

[j] re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device,

[k] wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.

’252 patent, claim 6.

Like claim 1, the plain language of claim 6 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of converting and exchanging data between hosts.

Elements 6[a], 6[d] are directed to exchanging data between host devices and first and second connectors, however, there is no recitation of how the data stream exchange is accomplished that would be indicative of an inventive technological improvement. Additionally,

hardware for performing data transfer was generic at least as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of data recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform an abstract process (data exchange) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Elements 6[b]-[c], 6[e]-[f], are directed to performing clock and data recovery on electrical input signals to convert it into an electrical transit signal to be conveyed across the electrical connectors, however, there is no recitation of how the clock and data recovery nor conversion is accomplished that would be indicative of any technological improvement. Additionally, hardware for performing clock and data recovery and remodulation was generic at least as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform abstract processes (clock and data recovery,) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019

claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Elements 6[g]-[j] are directed to performing clock and data recovery on the electrical transit signals to convert them into the outbound data stream to be conveyed to the host port, however, there is no recitation of how the clock and data recovery nor conversion is accomplished that would be indicative of any technological improvement. Additionally, hardware for performing clock and data recovery and remodulation was generic at least as of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform abstract processes (clock and data recovery, remodulation) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Element 6[k] merely adds the requirement that fixed, cable-independent, equalization parameters are used for the remodulation of the transit data stream and the clock and data recovery performed on the electrical input signal. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way, As of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, using

fixed, cable-independent, equalization parameters for remodulation of the transit data stream and the clock and data recovery performed on the electrical input signal were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 7

Dependent claim 7 of the ’252 Patent recites as follows:

> 7. The communication method of claim 6, wherein cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters.

’252 patent, claim 7.

The additional limitations recited in dependent claim 7 merely recite additional equalization parameters, where, as stated for claim 6, are abstract. Claim 7 is directed to equalization, however, there is no recitation of how the equalization is performed that would be indicative of an inventive technological improvement, and employing cable-dependent equalization parameters for the remodulation of the inbound data stream and clock and data recovery performed on electrical transit signals was generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date. *See, e.g.*, Exs. B-1 – B-11. Additionally, hardware performing equalization with cable-dependent parameters for the remodulation of the inbound data stream and clock and data recovery performed on electrical transit signals was also generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific types of equalization hardware are recited in the claimed invention. This element is abstract because it describes generic devices configured to perform an abstract process (implied mathematical algorithm of equalization) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or steps recited therein that improve technology or solve a technical problem in a

novel way. This claim does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., equalization) in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, equalization of signals conveyed across conductors using adaptively updated parameters was a well-known signal conditioning technique. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 8

Dependent claim 8 of the ’252 Patent recites as follows:

> 8. The communication method of claim 7, wherein said cable-dependent equalization parameters are adaptively updated.

’252 patent, claim 8.

The additional limitations recited in dependent claim 8 merely recite additional equalization parameters, which, as stated for claims 6 and 7, are abstract. Claim 8 is directed to equalization, however, there is no recitation of how the equalization is performed that would be indicative of an inventive technological improvement, and using adaptively updated equalization parameters was generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date. *See, e.g.*, Exs. B-1 – B-11. Additionally, hardware performing equalization with adaptively updated parameters was also generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific types of equalization hardware are recited in the claimed invention. This element is abstract because it describes a generic method to perform an abstract process (implied mathematical algorithm of equalization with adaptively updated parameters) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or steps recited therein that improve technology or solve a technical problem in a novel way. This claim does not disclose any improved function of a computer or other technology, nor does it solve a

specific technological problem (e.g., equalization) in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, equalization of signals conveyed across conductors using adaptively updated parameters was a well-known signal conditioning technique. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 9

Dependent claim 9 of the ’252 Patent recites as follows:

> 9. The communication method of claim 7, wherein said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable.

’252 patent, claim 9.

The additional limitations recited in dependent claim 9 merely adds the requirement that the equalization parameters are fixed during normal usage and are determined during manufacturing-testing of the cable. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, having fixed equalization parameters that were determined during manufacturing-testing were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11. In sum, claim 4 only recites abstract ideas, as the additional limitations of claim 9 are neither in isolation nor combined render claim 4 patent eligible.

Dependent Claim 10

Dependent claim 10 of the ’252 Patent recites as follows:

> 10. The communication method of claim 9, wherein the first inbound data stream has a per-lane symbol rate in excess of 50 GBd.

’252 patent, claim 10.

The additional limitations recited in dependent claim 10 merely adds the requirement that the data streams each have a per-lane symbol rate in excess of 50 GBd. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, having fixed equalization parameters that were determined during manufacturing-testing were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11. Indeed, the requirement that the data streams “each have a per-lane symbol rate in excess of 50 GBd” is conventional and well-known and no different than the speeds contemplated in the IEEE 802.3 Ethernet standard. *See, e.g.*, ’252 patent, 1:5-22. In sum, claim 5 only recites abstract ideas, as the additional limitations of claim 10 are neither in isolation nor combined render claim 5 patent eligible.

Independent Claim 11

Independent claim 11 of the ’252 Patent recites as follows:

11. A cable manufacturing method that comprises:

[a] connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver;

[b] packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device; and

[c] packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device,

[d] the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams,

[e] configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and

[f] each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals.

'252 patent, claim 11.

Like claim 1, the plain language of claim 11 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of converting and exchanging data between hosts.

Element 1[a] merely adds the requirement that the first and second transceivers are connected with conductors such that electrical transit signals can be transported therebetween. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, connecting two transceivers with electrical conductors such that they can exchange electrical transit signals therebetween was a conventional and well-known technique. *See, e.g.*, Exs. B-1 – B-11.

Elements 11[b]-[c] merely adds the requirement that the first and second transceivers are packaged into first and second connectors, respectively, and that the connectors exchange data with host ports, however, there is no recitation of how the data exchange is accomplished that would be indicative of an inventive technological improvement. Additionally, hardware for performing data transfer was generic at least as of the '252 patent's August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of data recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform an abstract process (data exchange) without specifying sufficiently concrete or inventive technological improvements;

and there are no specific, non-generic components or configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Element 11[d] is directed to performing clock and data recovery on electrical input signals to convert it into an electrical transit signal to be conveyed across the electrical connectors, however, there is no recitation of how the clock and data recovery nor conversion is accomplished that would be indicative of any technological improvement. Additionally, hardware for performing clock and data recovery and remodulation was generic at least as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform abstract processes (clock and data recovery, remodulation) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Element 11[e] is directed to performing clock and data recovery on the electrical transit signals to convert them into the outbound data stream to be conveyed to the host port, however,

there is no recitation of how the clock and data recovery nor conversion is accomplished that would be indicative of any technological improvement. Additionally, hardware for performing clock and data recovery and remodulation was generic at least as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific type of recovery and remodulation hardware are recited in these elements. These are abstract because they describe generic devices (first and second connectors) configured to perform abstract processes (clock and data recovery, remodulation) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic configurations (2 connectors connected by a cable) recited therein that improve technology or solve a technical problem in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, active optical cables (which use an optical link between two connectors that interfaced with host ports) were in common usage, and those cables used connectors to exchange data streams with host machines. *See, e.g.*, Exs. B-1 – B-11.

Element 11[f] merely adds the requirement that fixed, cable-independent, equalization parameters are used for the remodulation of the transit data stream and the clock and data recovery performed on the electrical input signal. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way, As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, using fixed, cable-independent, equalization parameters for remodulation of the transit data stream and the clock and data recovery performed on the electrical input signal were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 12

Dependent claim 12 of the ’252 Patent recites as follows:

> 12. The cable manufacturing method of claim 11, wherein the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals.

’252 patent, claim 12.

The additional limitations recited in dependent claim 12 merely recite additional equalization parameters, which, as stated for claim 11, are abstract. Claim 12 is directed to equalization, however, there is no recitation of how the equalization is performed that would be indicative of an inventive technological improvement, and employing cable-dependent equalization parameters for the remodulation of the inbound data stream and clock and data recovery performed on electrical transit signals was generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date. *See, e.g.*, Exs. B-1 – B-11. Additionally, hardware performing equalization with cable-dependent parameters for the remodulation of the inbound data stream and clock and data recovery performed on electrical transit signals was also generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific types of equalization hardware are recited in the claimed invention. This element is abstract because it describes generic devices configured to perform an abstract process (implied mathematical algorithm of equalization) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or steps recited therein that improve technology or solve a technical problem in a novel way. This claim does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., equalization) in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, equalization of signals conveyed across conductors using adaptively updated parameters was a well-known signal conditioning technique. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 13

Dependent claim 13 of the ’252 Patent recites as follows:

> 13. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation.

’252 patent, claim 13.

The additional limitations recited in dependent claim 13 merely recite additional equalization parameters, which, as stated for claims 11 and 12, are abstract. Claim 13 is directed to equalization, however, there is no recitation of how the equalization is performed that would be indicative of an inventive technological improvement, and using equalization parameters that adapt during usage of the cable as generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date. *See, e.g.*, Exs. B-1 – B-11. Additionally, hardware performing equalization with adaptively updated parameters was also generic as of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, *see, e.g.*, Exs. B-1 – B-11, and no specific types of equalization hardware are recited in the claimed invention. This element is abstract because it describes generic devices configured to perform an abstract process (implied mathematical algorithm of equalization with adaptively updated parameters) without specifying sufficiently concrete or inventive technical improvements; and there are no specific, non-generic components or steps recited therein that improve technology or solve a technical problem in a novel way. This claim does not disclose any improved function of a computer or other technology, nor does it solve a specific technological problem (e.g., equalization) in a novel way. As of the ’252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, equalization of signals conveyed across conductors using adaptively updated parameters was a well-known signal conditioning technique. *See, e.g.*, Exs. B-1 – B-11.

Dependent Claim 14

Dependent claim 14 of the ’252 Patent recites as follows:

> 14. The cable manufacturing method of claim 12, wherein the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters.

’252 patent, claim 14.

The additional limitations recited in dependent claim 14 merely recite additional 14 merely adds the requirement that the transceivers use preset cable-dependent equalization parameters which are determined during testing. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the 252 patent’s August 13, 2019 filing date and March 1, 2019 claimed priority date, using preset cable-dependent equalization parameters which are determined during testing were conventional and well-known techniques. *See, e.g.*, Exs. B-1 – B-11. In sum, claim 14 only recites abstract ideas, as the additional limitations of claim 4 are neither in isolation nor combined render claim 14 patent eligible.

***Alice* Step Two: The Asserted Claims Contain No “Inventive Concept” Sufficient to Render Them Patent Eligible**

As noted above, the second step of a Section 101 analysis under *Alice* requires the consideration of each claim element “both individually and ‘as an ordered combination’ to determine” whether there are additional elements present in the claim that ‘transform the nature of the claim’ into a patent-eligible application.” *Alice*, 573 U.S. at 217 (quotation omitted).

The Asserted Claims of the ’252 patent merely invoke well-understood, routine, and conventional software methods and techniques to achieve the multiple abstract ideas interspersed throughout the Asserted Claims. The claims directed to exchanging data between first and second

host ports and first and second connectors that convert and exchange data therebetween, which is well-known to one of ordinary skill in the art. *See, e.g.*, Exs. B-1 – B-11. As the Federal Circuit has held, "claims are not saved from abstraction merely because they recite components more specific than a generic computer." *BSG Tech LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1286 (Fed. Cir. 2018). As discussed in detail in the preceding Section, the Asserted Claims of the '252 patent lack any of the inventive hallmarks found in other patents found to be patent eligible.

As noted earlier, the Asserted Claims of the '252 patent provide no technological solution to the purported problems but instead simply disclose the abstract idea of exchanging and converting data, which moreover would have been well-known to one of ordinary skill in the art. As noted at the beginning of this section, the second step of a Section 101 analysis under *Alice* requires the consideration of the claim elements "as an ordered combination" to determine whether there are additional elements present in the claim that "transform the nature of the claim" into a patent-eligible application." *Alice*, 134 S. Ct. at 2347 (quotation omitted). However, the method claims' order of claim elements transfer the claim int patent-eligible material. To the contrary, the order of claim elements is conventional in the sense that a user would normally connect the transceivers together and package them within the connectors prior to any data transfer or conversion. The claims do not disclose anything different than the common and conventional practice of connecting two devices with an active electrical cable to that will transfer data therebetween. The order of the claim elements does not disclose any software and/or hardware technological advancement.

All of the Asserted Claims Are Substantially Similar—Represented by Claim 1—for Purposes of Section 101 Analysis

All the Asserted Claims of the ’252 Patent are directed to patent-ineligible abstract ideas. Where claims are “substantially similar and linked to the same abstract idea,” courts may look to representative claims in a Section 101 analysis. *Content Extraction*, 776 F.3d at 1349; *see also Phoenix Licensing, L.L.C. v. Consumer Cellular, Inc.*, No. 2:16-cv-152-JRG-RSP, 2017 WL 1065938, at *8-9 (E.D. Tex. Mar. 8, 2017), *report and recommendation adopted*, 2017 WL 1177988 (Mar. 30, 2017) (invalidating 974 claims after analyzing only a few “representative claims” where other claims were “substantially similar” and “linked to the same abstract idea”). Here, claim 1 of the ’252 Patent is representative of all Asserted Claims of the ’252 Patent, as the remaining claims recite the same abstract idea with immaterial and conventional variations.

Asserted independent claims 1, 6, and 11 recite nearly the same subject matter with only minor variations for purposes of Section 101 analysis. As discussed above, claim 1 is directed to the abstract idea of a cable exchanging and converting data. Claims 6 and 11 merely recite the same subject matter written as method claims.

The asserted dependent claims add additional limitations, but those additional limitations do not impart patent eligibility. Instead, the dependent claims add further variations on abstract ideas that are not technological advancements. *See, e.g.*, *Universal Secure Registry LLC v. Apple Inc.*, 10 F.4th 1342, 1357 (Fed. Cir. 2021).

As noted above, dependent claim 2 merely adds the requirement that the transceivers employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data streams and the clock and data recovery performed on the electrical transit signal,

which, as discussed above, is an abstract idea that is not patent eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 3 merely adds the requirement that the equalization parameters adapt during usage of the cable, which, as discussed above, is an abstract idea that is not patent eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 4 merely adds the requirement that the equalization parameters are fixed during normal usage and are determined during manufacturing-testing of the cable. As noted previously, dependent claim 4 recites conventional and well-known subject matter, (*see, e.g.*, Exs. B-1 – B-11) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 5 merely adds the requirement that the data streams each have a per-lane symbol rate in excess of 50 GBd. As noted previously, dependent claim 5 recites conventional and well-known subject matter, (*see, e.g.*, Exs. B-1 – B-11) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 7 merely adds the requirement that the transceivers employ cable-dependent equalization parameters for at least one of the remodulation of the inbound data streams and the clock and data recovery performed on the electrical transit signal. As noted previously, dependent claim 7 recites conventional and well-known subject matter, (*see, e.g.*, Exs. B-1 – B-11) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 8 merely adds the requirement that the cable-dependent equalization parameters are adaptively updated, which, as discussed above, is an abstract idea that is not patent eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 9 merely adds the requirement that the cable-dependent equalization parameters are fixed during normal usage and that they are determined during manufacturing-testing of the cable. As noted previously, dependent claim 9 recites conventional and well-known subject matter, (*see, e.g.*, Exs. B-1 – B-11) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 10 merely adds the requirement that the data streams each have a per-lane symbol rate in excess of 50 GBd. As noted previously, dependent claim 10 recites conventional and well-known subject matter, (*see, e.g.*, Exs. B-1 – B-11) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Dependent claim 12 merely adds the requirement that the transceivers employ cable-dependent equalization parameters for generating the electrical transit signals and for clock and data recovery, which, as discussed above, is an abstract idea that is not patent eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 13 merely adds the requirement that the transceivers adapt the cable-dependent equalization parameters during operation, which, as discussed above, is an abstract idea that is not patent eligible and is simply another layer of abstraction on top of an already abstract idea.

Dependent claim 14 merely adds the requirement that the transceivers are configured to use preset cable-dependent equalization parameters during operation that the cable-dependent equalization parameters are determined during testing. As noted previously, dependent claim 14 recites conventional and well-known subject matter, (*see, e.g.*, Exs. B-1 – B-11) and does not contain an inventive concept that would suffice to transform the abstract subject matter (i.e., exchanging and converting data) into an eligible application of the abstract idea.

Notably, there are no specific instructions or limitations in the specification concerning how these claim limitations must be carried out, other than a description of the idea, non-specific examples of how the idea may be carried out, and the instructions to apply it to the conventional technological environment. *See Alice*, 573 U.S. at 220–21. Thus, as with claim 1, none of the asserted dependent claims provide particular requirements as to how the claimed steps are to be performed, nor do they recite anything other than conventional components that are used in conventional ways.

Accordingly, claim 1 of the ’252 Patent is representative for purposes of the Section 101 analysis, and any differences amongst claims 2–14 are insubstantial with respect to eligibility, as each of the claims in the ’252 Patent are drawn to the same abstract idea of data exchange and conversion using generic components and configurations. *Alice*, 573 U.S. at 225; *see also Content Extraction*, 776 F.3d at 1348.

Invalidity Grounds Under 35 U.S.C. §§ 102 and 103

Respondents attach, as Appendix B to its Initial Contentions, claim charts showing examples of how the cited references anticipate and/or render obvious the Asserted Claims of the ’252 Patent under at least AIA 35 U.S.C. §§ 102 and 103 either expressly or inherently as

understood by a person having ordinary skill in the art, or based on Complainants' apparent interpretation of the claims.

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
B-1	U.S. Patent No. 10,148,414 ("Lugthart '414")	October 19, 2017 (Published)	June 30, 2017
B-2	U.S. Patent App. Pub. No. 2013/0115803 ("Tang")	May 9, 2013 (Published)	November 9, 2011
B-3	U.S. Patent App. Pub. No. 2017/0302431 ("Lugthart 431")	October 19, 2017 (Published)	June 30, 2017
B-4	U.S. Patent No. 8,516,238 ("Cornelius")	January. 5, 2012 (Published)	June 30, 2011
B-5	(Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer ("TI DS110DF111"))	June 2015 (Published)	N/A
B-6	Texas Instruments – DS125DF410 Low-Power Multi-Rate Quad Channel Retimer ("TI DS125DF410")	February 2018 (Published)	N/A
B-7	U.S. Patent No. 9,270,500 ("Vijayaraghavan")	February 23, 2016 (Issued)	December 13, 2013
B-8	U.S. Patent No. 8,499,103 ("Carter")	July 30, 2013 (Issued)	April 20, 2010
B-9	U.S. Patent Pub. US 2019-0028262A1 ("Kobayashi")	January 24, 2019 (Published)	August 31, 2018
B-10	Amphenol SMP9 Active Electric Cable Product ("SMP9 Cable"))	2017 (Manufactured)	N/A
B-11	Collected Secondary References	Prior to March 1, 2019	Prior to March 1, 2019

The attached claim charts identify specific examples of disclosures that teach or suggest a given claim limitation. These identifications should be understood to be exemplary; the charts do not necessarily indicate every location within a particular prior art reference where a claim limitation may be disclosed or suggested. Respondents and their expert witnesses may rely on other portions of the prior art.

To the extent Complainants contend that any reference identified above does not anticipate the Asserted Claims, it would have been obvious over that primary reference alone or to combine

or modify the primary references with concepts from other prior art, such as the other references identified and as explained herein and in Exhibits B-1 – B-11.

In particular, for each limitation of the Asserted Claims that Complainants contend is not met by a particular reference, Respondents contend that the limitation (and claim as a whole) is obvious based on a combination of that particular reference with (1) any other reference disclosing the limitation, (2) any admitted prior art, as explained in the background of each patent or discussed in the file history, (3) any other reference identified in Exhibits B-1 – B-11, as disclosing that limitation, and/or (4) the knowledge of a person of ordinary skill in the art and/or any of the references and concepts discussed herein regarding the relevant background and state of the art. Respondents' obviousness grounds for each dependent claim incorporate the obviousness grounds for the claims from which the dependent claim depends in addition to any obviousness grounds identified in the charts for the dependent claim. To the extent that individual Exhibits B-1 – B-11 include specific combination of prior art, Respondents' contentions are not limited only to those particular combinations, as such combinations are merely exemplary and are meant to be inclusive of the combinations expressed herein and in the other Appendices to these contentions.

The suggested obviousness combinations discussed herein are not to be construed to suggest that any reference included in the combinations is not anticipatory. Further, to the extent that Complainants contend that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, Defendants reserve the right to identify other prior art references that, when combined with the anticipatory prior art, would render the claims obvious despite an allegedly missing limitation. Defendants will further specify the motivations to combine the prior art, including through reliance on expert testimony, at the appropriate later stage of this Investigation.

In addition to the combinations of Exhibits B-1 – B-11, at least the following exemplary combinations would have been obvious to a POSITA:

- Lugthart ’414 in view of Aronson
- Tang in view of Texas Instruments DS125DF1610 (B-n) or Aronson
- Lugthart 431 in view of TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or Lusted, or Yin, or Yu, or Ikeda, or Norimatsu
- TI DS110DF111 in view of Lugthart 431, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or Lusted, or Yin, or Yu, or Ikeda, or Norimatsu
- TI DS125DF410 in view of Lugthart 431, or TI DS110DF111, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng , or Lusted, or Yin, or Yu , or Ikeda, or Norimatsu
- Vijayaraghavan in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or Lusted, or Yin, or Yu, or Ikeda, or Norimatsu
- Carter in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Cornelius, or Musah, or Riani, or Zheng, or Lusted, or Yin, or Yu, or Ikeda, or Norimatsu
- Cornelius in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Musah, or Riani, or Zheng, or Lusted, or Yin, or Yu, or Ikeda, or Norimatsu

- Kobayashi in view of Lusted or Yu or Yin or Ikeda or Norimatsu or TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng

For each specified combination, Respondents rely on the references herein, as well as the knowledge of a person of ordinary skill in the art, including that which will be discussed through expert discovery. Although Respondents provide exemplary disclosures and motivations to combine below, Respondents will present expert opinion in accordance with the procedural schedule. Respondents reserve the right to supplement or modify the anticipation and obviousness grounds in response to, for example, Complainants' positions regarding the scope and meaning of the Asserted Claims taken in this Investigation, before the PTAB, or during prosecution of pending matters related to the Asserted Patents, claim construction determinations made in this Investigation or other proceedings involving the Asserted Patents, updates or changes to Complainants' infringement and/or technical domestic industry positions, and materials later obtained during discovery, including from Complainants or in response to any third party subpoenas.

Respondents reserve the right to rely on the prior art references identified in connection with any of the other Asserted Patents in connection with the '252 Patent. In addition, Respondents hereby cite the following additional references as being relevant to the subject matter claimed in the '252 Patent. Respondents are producing concurrently herewith a number of such references that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Respondents reserve the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103 (including as evidence of motivation to

combine or reasonable expectation of success), as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Complainants may take regarding the scope of the Asserted Claims, and/or based on the Court's claim construction (once issued), Respondents reserve the right to revise these contentions and to rely on these references to prove the invalidity of the '252 Patent in a manner consistent with this ALJ's Ground Rules.

- U.S. Patent No. 5,452,333
- U.S. Patent No. 5,856,980
- U.S. Patent No. 6,055,269
- U.S. Patent No. 6,147,826
- U.S. Patent No. 6,621,862
- U.S. Patent No. 7,239,665
- U.S. Patent No. 8,787,430
- U.S. Patent Application Publication No. 2006/0045176
- U.S. Patent Application Publication No. 2010/0210142
- U.S. Patent Application Publication No. 2010/0232492
- U.S. Patent Application Publication No. 2011/0228821
- U.S. Patent Application Publication No. 2013/0280955
- U.S. Patent Application Publication No. 2014/0281067
- U.S. Patent Application Publication No. 2017/0187463
- U.S. Patent Application Publication No. 2020/0194911
- SFF-8436 Specification for QSFP+ 4X 10 Gb/s Pluggable Transceiver Rev 4.9, SFF Committee (August 31, 2018)
- SFF-8642 Specification for MINI MULTILANE SERIES: SHIELDED INTEGRATED CONNECTOR, Rev 2.7, SFF Committee (February 26, 2010)

- SFF-8432 Specification for SFP+ Module and Cage, Rev 5.2a, SFF Committee (November 30, 2018)
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section One
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Two
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Three
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Four
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Five
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Six
- Texas Instruments Application Report SNLA225, "Selecting TI SigCon Devices for SFF-8431 SFP+ Applications." Texas Instruments Inc. (June 2014) (available at https://web.archive.org/web/20151031185909/https://www.ti.com/lit/an/snla225/snla225.pdf)
- Proakis, John G., DIGITAL COMMUNICATION, McGraw-Hill, 4th Edition, 2000, pp. 583-635
- Hanumolu, P. K. *et al*., "Equalizers for High-Speed Serial Links." International Journal of High Speed Electronics and Systems, vol. 15, no. 2, 2005, pp. 429-458
- Liu, Jin and Xiaofeng Lin, "Equalization in high-speed communication systems," IEEE Circuits and Systems Magazine, vol. 4, no. 2, 2004, pp. 4-17
- Hsieh, Ming-ta and Gerald E. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery," IEEE Circuits and Systems Magazine, vol. 8, no. 4, 2008, pp. 45-57

Level of Ordinary Skill in the Art

To assess the level of ordinary skill of a POSITA, the following factors can be considered: (i) the type of problems encountered in the art; (ii) the prior solutions to those problems; (iii) the rapidity at which innovations are made; (iv) the sophistication of the technology; and (v) the level of education of active workers in the relevant field.

Based on the foregoing, Respondents contend that a POSITA for the '252 Patent as of August 13, 2019 (as well as March 1, 2019) would have had a Bachelor of Science in electrical or

computer engineering with at least three years of experience in high-speed digital communication systems. A higher level of education may substitute for less experience.

Obviousness and Motivation to Combine

Motivations to combine with a reasonable expectation of success, as well as the general state of the art, may be found in a variety of places including in the references defined above and the specification of the ’252 Patent. For example, each piece of prior art relates to the design and/or structure and/or function of active cable devices. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine any one piece of identified prior art with any other identified piece of prior art with a reasonable expectation of success. For at least this reason, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein so as to practice the Asserted Claims and there was a motivation in the art to make such a combination.

Motivations to combine various prior art references with a reasonable expectation of success are present in the references themselves, the common knowledge of one of ordinary skill in the art, the prior art as a whole, or the nature of the problems allegedly addressed by the ’252 Patent. Further reasons to combine the references identified in these charts with a reasonable expectation of success include the nature of the problem being solved, the express, implied, and/or inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed towards methods and systems for the design and/or structure and/or function of active cable devices that such combinations would have yielded predictable results, and the fact that such combinations would have represented known alternatives to a person of ordinary skill in the art.

In *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." 550 U.S. 398, 416 (2007); *see also id.* at 401 ("[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions."). In particular, a patent is obvious where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill are not in material dispute, and the obviousness of the claim is apparent in light of these factors." *Id.* at 427. The Supreme Court explained that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 401.

Moreover, the Supreme Court recognized that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. *Id*. at 402 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp."). When a person of ordinary skill uses an identified, predictable solution to solve a problem, "it is likely the product not of innovation but of ordinary skill and common sense." *Id*. at 402-03.

In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. at 417. If a person of ordinary skill can implement a predictable variation, § 103 bars its patentability. *Id*. The rationale to combine or modify prior art references is significantly stronger when references

seek to solve similar problems, come from the same field, and correspond well with one another. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

The references share commonalities in terms of their general subject matter as well as the types of equipment, products, systems, and/or methods used. Further, the prior art references explicitly or implicitly reference other prior art references, share common authors or inventors, were published in the same journals, were compiled by a common author of a compilation or reference book, were presented at the same conferences, and/or were developed at common companies, schools, or organizations which would motivate one of skill in the art to combine them. Additionally, the references, and any products, devices, or processes described in the references, existed and/or were invented in the same time period providing further motivation for combination.

These disclosures are provided without prejudice to any arguments or objections concerning the relevance of motivation to combine in connection with any invalidity contentions. Respondents reserve the right to further specify the motivations to combine the prior art in response to positions that Complainants may take later in this Investigation and as discovery proceeds. Respondents may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. Moreover, Respondents reserve the right to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the ’252 Patent.

One or more combinations of the prior art references identified in Exhibits B-1 through B-11 would have been obvious because these references would have been combined with a reasonable expectation of success using a simple substitution of one known, equivalent element

for another to obtain predictable results and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Exhibits B-1 through B-11 would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

All the Asserted Claims are directed to active cables. Such technology was widely known before the alleged priority date of the ’252 Patent, as evidenced by the references in Exhibits B-1 through B-11. *See, e.g.*, Exs. B-1 (U.S. Patent No. 10,148,414 (“Lugthart ’414”)); B-2 (U.S. Patent App. Pub. No. 2013/0115803 (“Tang”)); B-3 (U.S. Patent App. Pub. No. 2017/0302431 (“Lugthart 431”)), B-4 (U.S. Patent No. 8,516,238 (“Cornelius”), B-5 (Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“TI DS110DF111”)), B-6 (Texas Instruments – DS125DF410 Low-Power Multi-Rate Quad Channel Retimer (“TI DS125DF410”)), B-7 (U.S. Patent No. 9,270,500 (“Vijayaraghavan”)), B-8 (U.S. Patent No. 8,499,103 (“Carter”)), B-9 (U.S. Patent Pub. US 2019-0028262A1 (“Kobayashi”)), B-10 (Amphenol SMP9 Active Electric Cable Product (“SMP9 Cable”), B-11 (collected secondary references).

The prior art references provide motivations to combine with a reasonable expectation of success because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield

predictable results. The substitution of one element in an active cable device could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the ’252 Patent.

Additional motivations to combine specific references are discussed below.

5.1.1.1. Exemplary Motivations to Combine for the ’252 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references described in Exhibits B-1 – B-11, or any reference disclosed above, with a reasonable expectation of success, to perform the teachings of an active electrical cable employing fixed, cable-independent, equalization parameters for the remodulation of outbound data streams and the clock and data recovery performed on inbound electrical signals. The ’252 patent recognizes that active electrical cables containing certain data processing functionality were well known in the art prior to the priority date of the ’252 patent. *See* ’252 patent at 1:5-22, 4:4-26, 6:44-54, 7:27-34.

For example, a person of ordinary skill in the art would have been motivated to combine U.S. Patent No. 10,148,414 (“Lugthart ’414”) with U.S. Patent No. 7,762,727 (“Aronson”) to render obvious claims 1–14 of the ’252 Patent.

Lugthart ’414 was filed on June 30, 2017, was published October 19, 2017, and claims domestic priority to at least U.S. Patent Application No. 14,581,979 filed on December 23, 2014. Lugthart ’414 qualifies as prior art under 35 U.S.C. § 102(a)(1)(AIA) and 35 U.S.C. § 102(a)(2)(AIA).

Lugthart ’414 discloses an “active cable” 110 comprising “transceiver assemblies 105a, 105b positioned at either end of … conductive lines 111.” *See* Lugthart ’414 at 14:32-56, Fig. 2A (below).

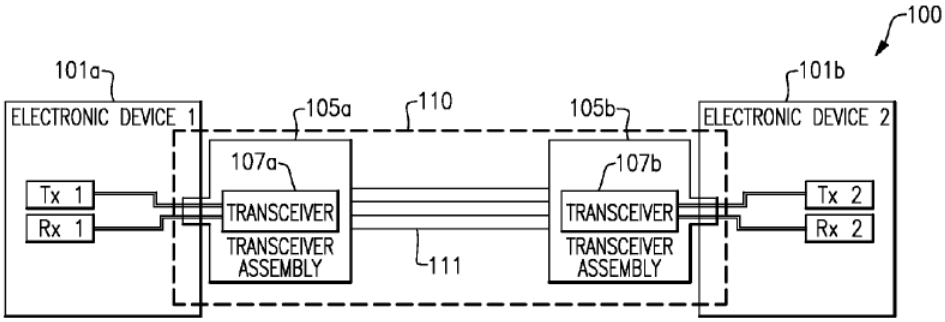


FIG.2A

Conductive lines 111 can be micro coaxial cable conductors. *See, e.g.*, Lugthart ’414 at 17:47-19:15, Figs. 3A-3B. Cable 110 interconnects electronic devices 101a/101b (“host devices”), with transceivers 107a/107b in transceiver assembly 105a/105b communicating signals on its “host side” and “line side.” *See, e.g.*, Lugthart ’414 at 14:15-45; Fig. 4A.

The transceiver 10 in Figure 1A of Lugthart ’414 processes data transmitted through “EGRESS/TRANSMIT” (from host to line/cable) and “INGRESS/RECEIVE” (from line/cable to host)[6] paths. *See, e.g.*, Lugthart ’414 at 8:3-36.

[6] The Lugthart ’414 labels INGRESS/EGRESS from the ***host’s*** perspective, whereas the ’252 Patent labels ***inbound/outbound*** paths from the ***cable’s*** perspective.

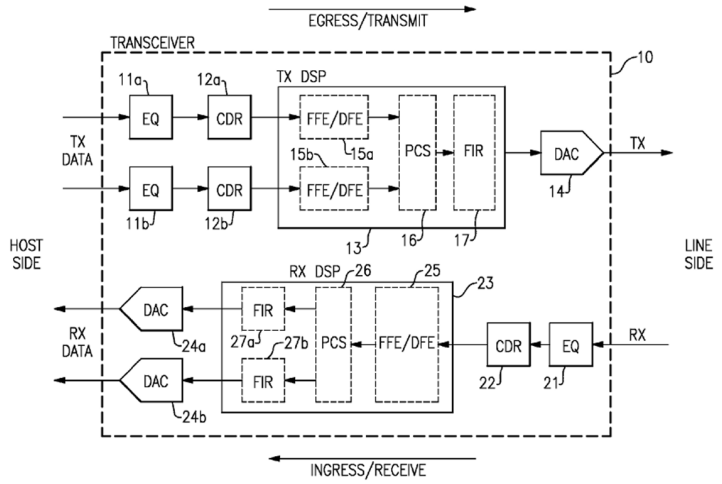


FIG.1A

In the EGRESS / TRANSMIT path, equalizers 11a/11b receive host-side transmit data (TX DATA) and perform "equalization to compensate for transmission line losses on the host side." *See* Lugthart '414 at 8:17-21, 9:14-29.

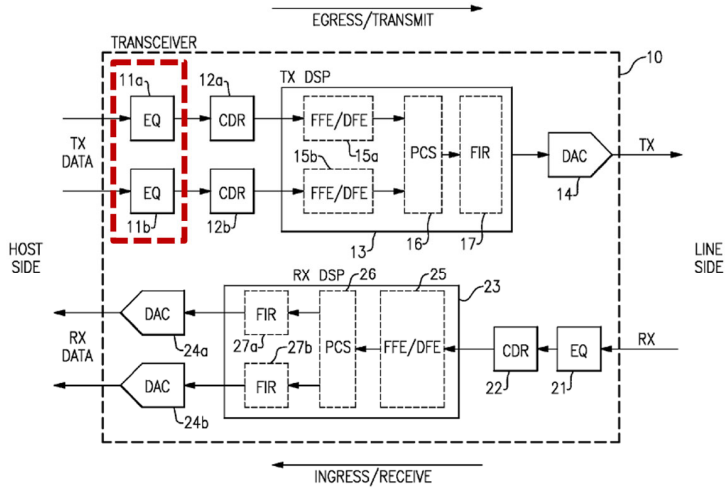


FIG.1A

CDR circuits 12a/12b "recover data in data streams generated by … transmit path equalizers [11a/11b]." *See* Lugthart '414 at 8:17-21, 9:38-41.

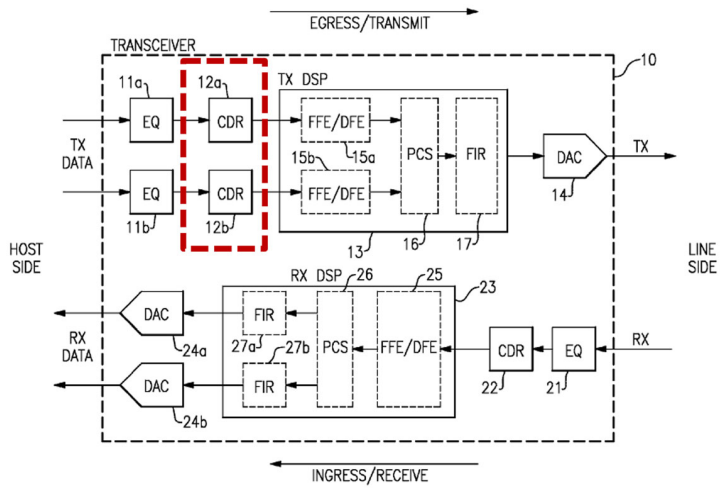


FIG.1A

Digital signal processor (DSP) 13 has feed-forward equalizer (FFE) and/or decision feedback equalizer (DFE) 15a/15b, physical coding sublayer (PCS) block 16, and finite impulse response (FIR) filter 17 ("FIR 17"). *See* Lugthart '414 at 8:21-23, 9:42-55.

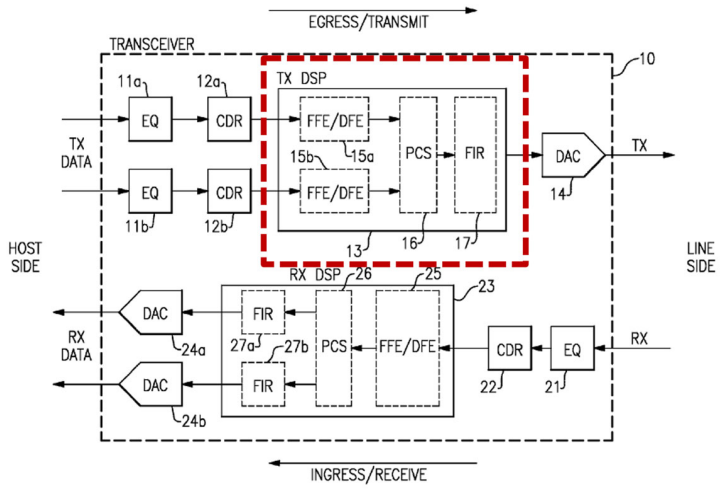


FIG.1A

PCS block 16 combines multiple parallel NRZ-encoded channels into a single PAM-4-encoded channel. *See, e.g.*, Lugthart '414 at 23:29-63. FIR 17 pre-equalizes the signal by pre-compensating for line-side channel distortion. *See, e.g., id*. at 22:19-23, 23:64-24:7.

Equalizer 21, CDR 22, and DSP 23 perform analogous functions on the INGRESS / RECEIVE path. *See, e.g.*, Lugthart '414 at 8:3-36, 9:14-29, 24:8-21. Equalizer 21 compensates for line-side transmission line losses. *See, e.g., id*. at 9:14-23.

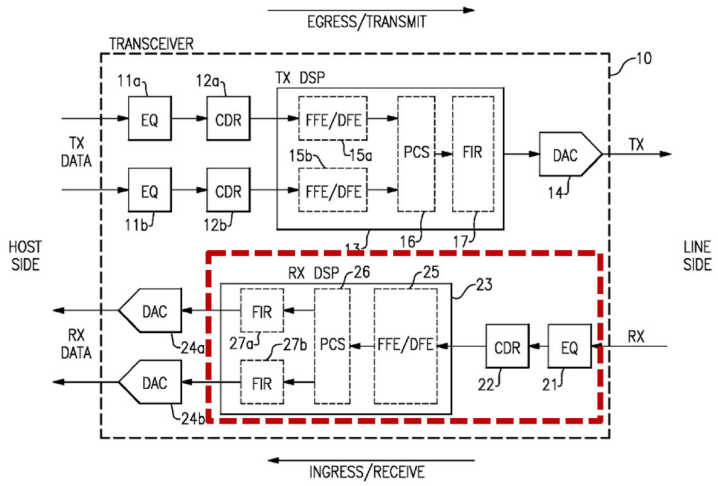


FIG.1A

Figure 10 (below) illustrates CDR system 500's CDR circuit 502 as used in the transceivers in, e.g., Figures 1A-2B. *See, e.g.*, Lugthart '414 at 35:16-32.

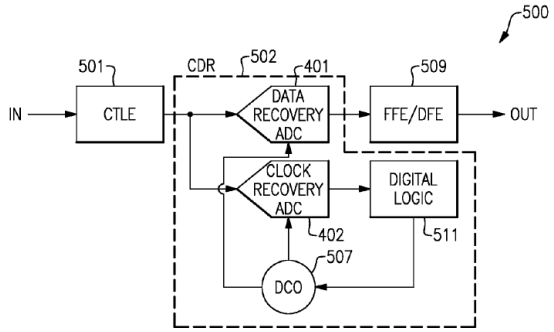


FIG.10

CTLE 501 equalizes analog input signal IN to mitigate distortions from the transmission side—*e.g.*, the host for EGRESS/TRANSMIT path, or the line for INGRESS/RECEIVE path—after which CDR circuit 502 recovers the clock and data by aligning sample clock signals from oscillator 507 to the input signal and generating a digital representation of the analog input signal.

See, e.g., Lugthart '414 at 35:40-36:19, 30:29-31. CDR circuit 502 provides the recovered data to FFE/DFE 509, which condition it as output signal OUT. *See, e.g., id*. at 36:14-19.

U.S. Patent No. 7,762,727 to Aronson ("Aronson")was filed on October 31, 2008, was issued on July 27, 2010, and claims domestic priority to U.S. Patent Application No. 11/401,803 filed on April 10, 2006. Aronson qualifies as prior art under 35 U.S.C. § 102(a)(1)(AIA) and 35 U.S.C. § 102(a)(2)(AIA).

Aronson discloses an active cable for high-speed transmissions between network nodes. *See, e.g.*, Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.

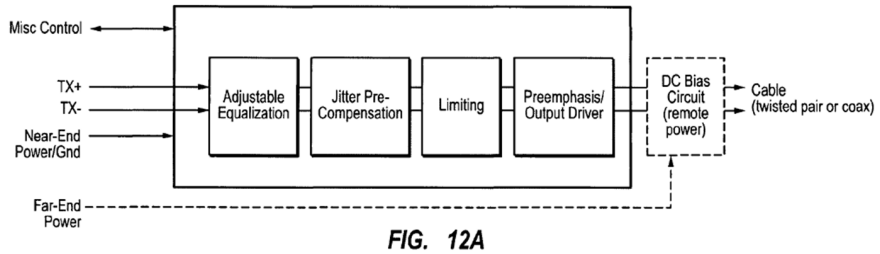


FIG. 12A

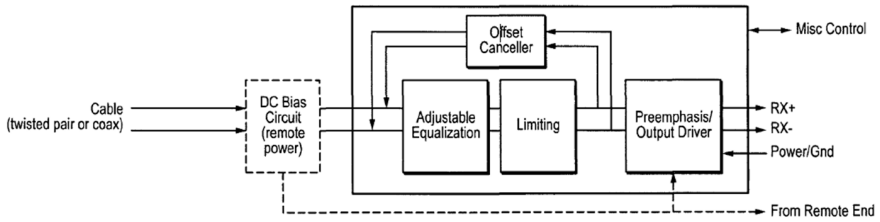


FIG. 12B

Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles

dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23.

Claims 1–14 of the '252 Patent recite well-known concepts that—with CDR circuits in an active cable transceiver—the link between hosts has three segments (two host interfaces and a cable) for which: (1) equalization in the cable segment uses cable-dependent parameters, while (2) equalization at the host interfaces uses cable-independent parameters. The claims also recite the well-known concepts that equalization parameters can be fixed or adaptive.

To the extent that Lugthart '414 is considered to not expressly disclose any such claimed requirements, Aronson—and other references corroborating an ordinarily skilled artisan's background knowledge—expressly disclose all these claimed requirements and would have given an ordinarily skilled artisan reasons to have implemented Lugthart '414 in view of Aronson in a manner meeting all claims of the '252 Patent.

On the EGRESS/TRANSMIT path, the transceivers of Lugthart '414 equalize the signals conveying inbound data stream TX, using equalizers 11a/11b, to "compensate for transmission line losses on the host side." *See, e.g.*, Lugthart '414 at 9:14-29, Fig. 1A (below).

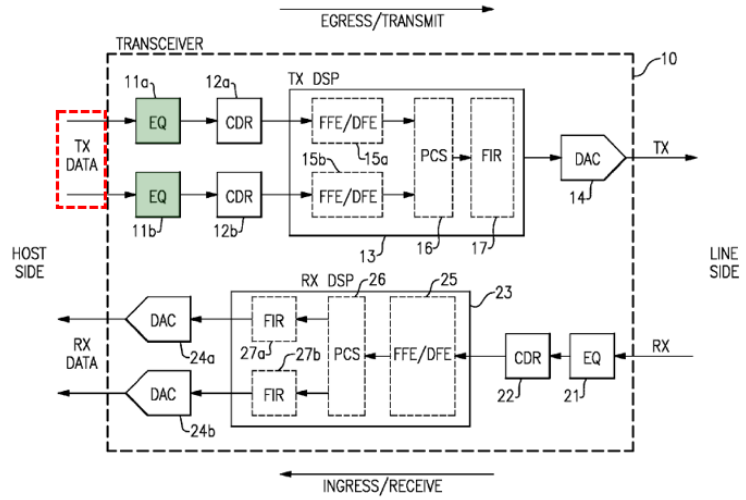


FIG.1A

On the INGRESS/RECEIVE side, the FIR filters 27a/27b ("FIRs 27a/27b") of the DSP 23 pre-equalize the signals conveying outbound data stream RX, thereby pre-compensating for host-side distortion/losses on a line-side data stream that was already equalized for line-side losses by equalizer 21. *See, e.g.*, Lugthart '414 at 9:14-18.

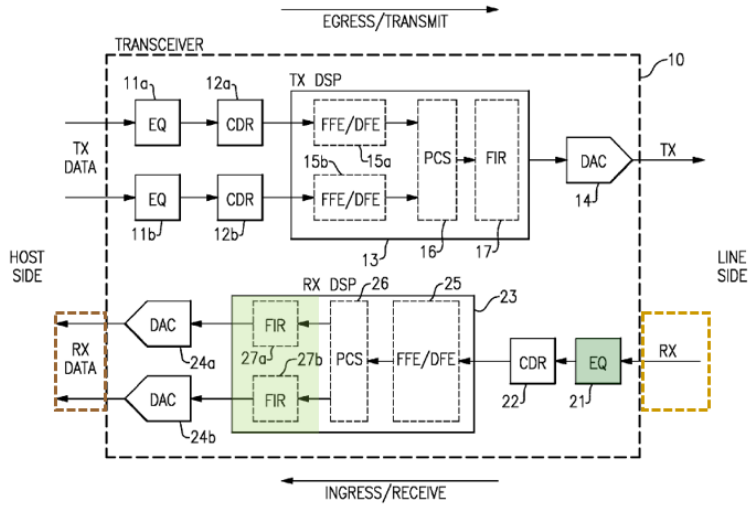


FIG.1A

Cable-Independent Parameters

Because the CDR functionality recovers signals before cable-side output via CDRs 12a/12b and FFE/DFEs 15a/15b on the EGRESS/TRANSMIT path, and via CDR 22 and FFE/DFE 25

(§VI.D.6 infra) after cable-side reception on the INGRESS/RECEIVE path, POSAs understood that for equalizers 11a/11b and FIRs 27a/27b to compensate for host-side distortion/losses each would employ equalization parameters based on the host interface characteristics and not a line-side cable's characteristics (from which they are separated by CDR processes), such that they would be "cable-independent" per the '252 Patent.

To the extent Lugthart '414 is considered to not expressly teach or suggest using cable-independent parameters for pre-equalizing and equalizing signals to and from the host, Aronson does disclose using cable-independent parameters for pre-equalization.

The cable's transmitter Integrated Circuit (IC) in Aronson Figure 12A (below) performs cable-independent equalization on inbound data stream TX+/TX- to "compensat[e] for high frequency loss in the host board traces." *See, e.g.*, Aronson at 14:16-23. Host board traces are independent of the cable, so parameters compensating for them are cable-independent.

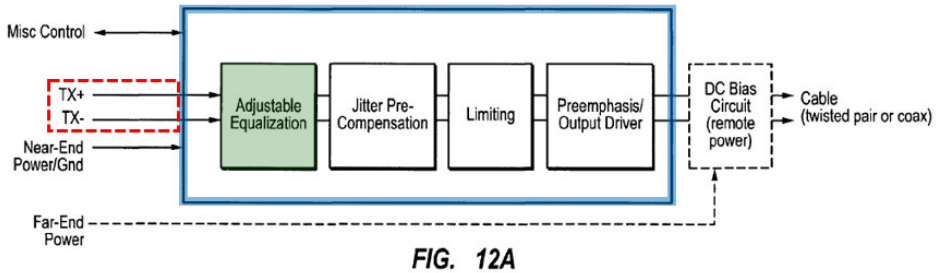


FIG. 12A

Aronson's PCB traces are on the host (*see, e.g.*, Aronson at 15:1-8 ("host PCB traces")) so pre-equalization parameters addressing them are cable-independent. Aronson's teachings to use cable-independent parameters to perform equalization compensating for host-side losses gave an ordinarily skilled artisan reason to implement Lugthart '414 in the same manner.

Fixed Parameters

Aronson also teaches that these cable-independent parameters are fixed. While Figure 12A shows "adjustable" equalization, "[s]uch equalization could be fixed." *See, e.g.*, Aronson at 14:20-23.

The cable's receiver IC generates outbound data stream RX+/RX- to the host by, *inter alia*, performing equalization in a pre-emphasis/output driver that drives "host PCB traces." *See, e.g.*, Aronson at 15:1-8, Fig. 12B (below). Pre-emphasis was another term for pre-equalization. *See, e.g.*, U.S. Patent No. 8,787,430 at 2:39-41. Pre-equalizing outbound stream RX+/RX- addresses "losses on long PCB traces" and "could be fixed." *See, e.g.*, Aronson at 15:17-24.

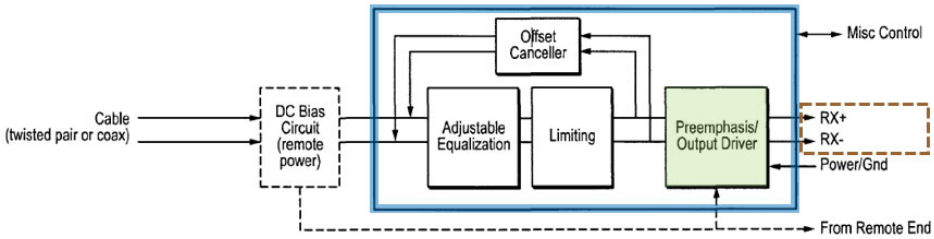


FIG. 12B

An ordinarily skilled artisan understood that the design choice between fixed or adaptive equalization involved tradeoffs between, e.g, accuracy, speed, manufacturing cost, and complexity when equalizing a communication channel like an active copper cable's host interface. *See, e.g.*, Aronson at 15:17-24. "Fixed" parameters reduced complexity and manufacturing costs. *See, e.g.*, U.S. Patent No. 7,239,665 at 1:7-18 (discussing slow convergence with adaptive equalization); U.S. Patent App. Pub. No. 2011/0228821 at [0009]-[0011] (discussing tradeoffs between fixed and adaptive equalization); U.S. Patent No. 6,621,862 at 1:52-55 (large gate count for adaptive equalization can cause "high chip costs"); U.S. Patent App. Pub. No. 2006/0045176 at [0034] ("The adaptive equalizer can be trapped in a failure state (i.e., incorrect state) and not able to recover from the failure state."); U.S. Patent App. Pub. No. 2017/0187463 at [0058]

("[E]qualization techniques … come with different engineering tradeoffs, including trade-offs in power consumption, performance, and/or cost.").

An ordinarily skilled artisan's background knowledge of these tradeoffs between fixed and adaptive parameters would have given POSAs additional reasons—beyond Aronson's specific teaching to use fixed parameters—to make the design choice to fix the cable-independent equalization parameters in Lugthart '414 's equalizers 11a/11b and DSP 23's FIRs 27a/27b.

The '252 Patent says the cable-independent parameters are fixed "[i]n at least some contemplated embodiments." *See, e.g.*, '252 Patent at 4:60-64. Thus, the cable-independent parameter need not be fixed in all embodiments. There is nothing critical or inventive about fixing the cable-independent parameters—the inventors claimed one of the known, obvious, design choices. *KSR Int'l v. Teleflex*, 550 U.S. 398, 421 (2007) (obvious to pursue finite number of identified predictable solutions).

Using fixed cable-independent parameters to perform Lugthart '414 's equalization (in equalizers 11a/11b and FIRs 27a/27b) that compensates for host-side losses also meets a rationales indicative of obviousness. *KSR*, 550 U.S., 417-418. This combines no more than prior art elements (Lugthart's host-side equalization; Aronson's teaching to use fixed cable-independent parameters for host-side equalization) according to known methods to yield predictable results (equalizing Lugthart's host-side signals using fixed cable-independent parameters).

The DSP 13 of Lugthart '414 uses FIR 17 to "perform [pre-]emphasis on the signal to compensate for channel losses" over the cable (e.g., on the transceiver's line-side). *See, e.g.*, Lugthart '414 at 23:49-24:7, Fig. 1A (below). The equalizer 21 of Lugthart '414 "provide[s] signal equalization to compensate for transmission line losses on the line side." *See id.* at 9:14-29; *see also* 22:49-54 (compensates for losses "over the cable"). An ordinarily skilled artisan understood

that FIR 17 and equalizer 21 use "cable-dependent" parameters because they compensate for degradation/distortion over the cable (e.g., "line side").

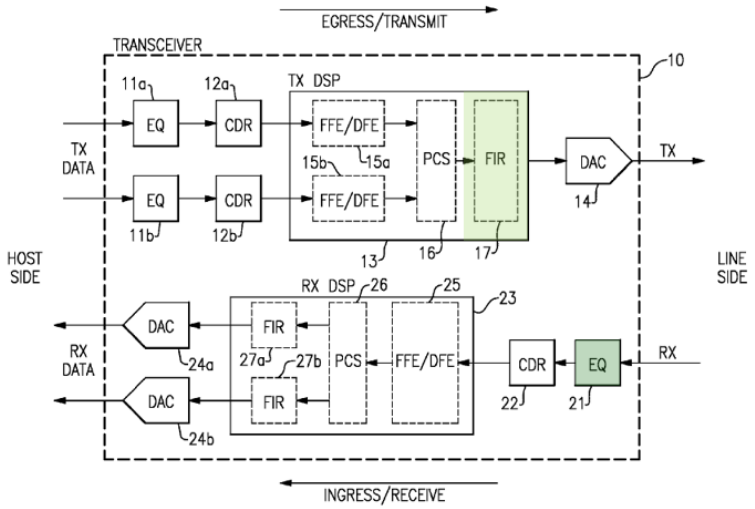


FIG.1A

To the extent Lugthart '414 is considered to not explicitly describe the equalization parameters used by FIR 17 and equalizer 21 as cable dependent, Aronson confirms that would have been the conventional and obvious way to implement equalization addressing cable-side losses in Lugthart '414. Aronson's transmitter IC's line-side pre-emphasis/output driver overcomes "loss on the cable" using cable-dependent parameters that "match the particular length [and/or] the characteristics of the copper cabling." *See, e.g.*, Aronson at 14:33-43, Fig. 12A (below). Similarly, Aronson's receiver IC equalizes received line-side signals to "compensat[e] for the cable" losses using cable-dependent parameters based on "cable length and characteristics." *See id*. at 15:1-8, Fig. 12B (below).

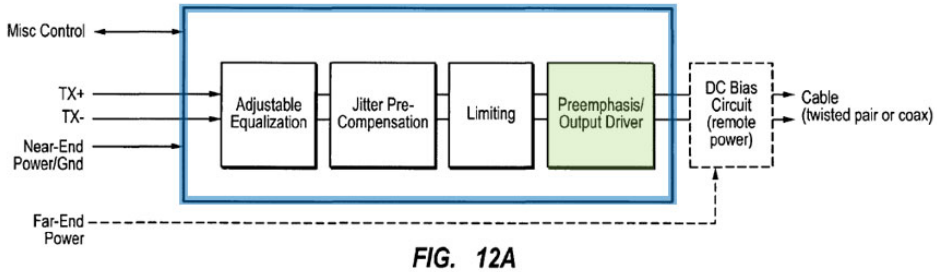


FIG. 12A

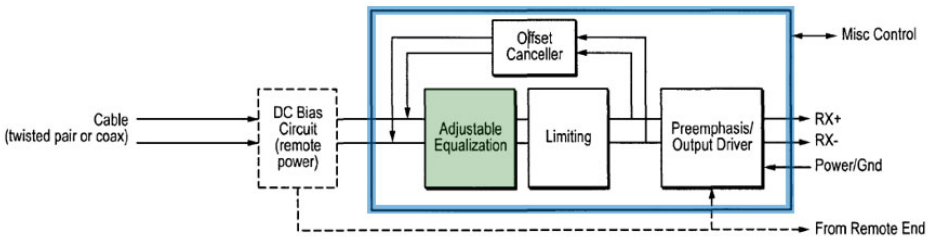


FIG. 12B

Aronson's express teachings to use cable-dependent parameters to equalize signals the cable transceiver transmits to, and receives from, the cable, gave an ordinarily skilled artisan reason to implement Lugthart '414 using cable-dependent equalization parameters in the same manner. Doing so was nothing more than combining prior art elements (Lugthart's line-side equalization; Aronson's teaching to use cable-dependent parameters for line-side equalization) according to known methods to yield predictable results (equalizing Lugthart's line-side signals using cable-dependent parameters). *KSR*, 550 U.S., 417-418.

Aronson describes a known design choice to set equalization parameters by fixing them or using an adaptive scheme. *See, e.g.*, Aronson at 15:1-6. As explained below, an ordinarily skilled artisan had reasons to use either alternative.

Adapting the Line-Side Cable-Dependent Parameters

An ordinarily skilled artisan knew that equalization parameters could be adapted by adjusting them based on distortions to known training signals transmitted over the cable. Lugthart '414 describes training phases during which the cable-dependent equalization parameters for DSP 13's FIR 17 and equalizer 21 are adapted as discussed. To the extent Lugthart '414 is considered to not teach expressly that the equalization coefficients for DSP 13 and equalizer 21 are among the parameters adapted during Lugthart '414 's training phases, an ordinarily skilled artisan had reasons to implement Lugthart '414 in this manner based on Aronson and an ordinarily skilled artisan's background knowledge of the benefits of adapting equalization parameters.

Aronson explains that "pre-emphasis and/or equalization can be fixed, adjustable, or adaptable." *See* Aronson at Abstract. While Aronson's Abstract refers to an optical cable embodiment, ordinarily skilled artisans understood that adaptation applies equally to Aronson's copper cable embodiments, as in Figs. 12A-12B. *See, e.g., id*. at 3:62-65; 14:16-15:24. Indeed, Aronson is explicit that adjustable equalization in Figure 12B (below) that "compensate[s] for the cable" losses can be "adaptive." *See, e.g., id*. at 15:1-7 (describing adjustable factory-set equalization as of "particular interest" because cable characteristics are established at manufacture but disclosing an "adaptive" equalization alternative).

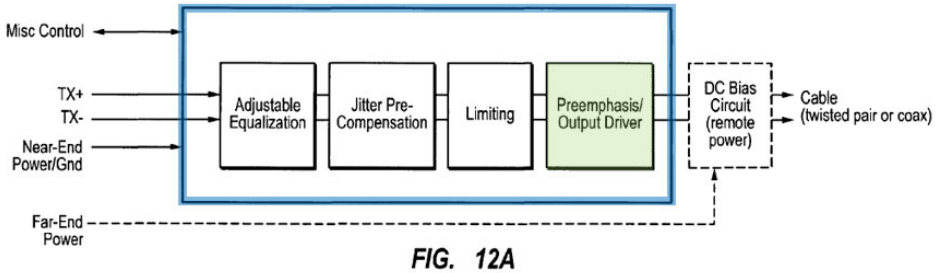


FIG. 12A

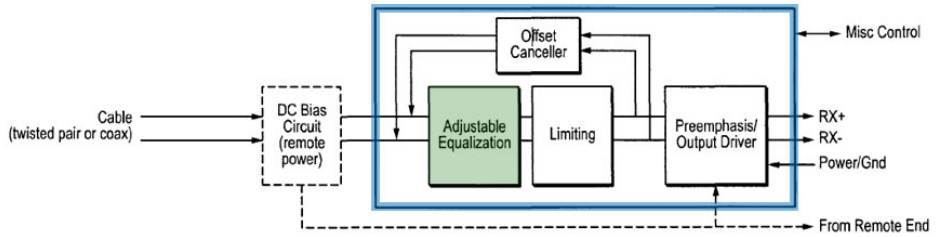


FIG. 12B

An ordinarily skilled artisan understood that pre-equalization by Figure 12A's pre-emphasis/output driver is "adaptive" given Aronson's teachings that "pre-emphasis … can be … adaptable" (Aronson at Abstract), and adaptive equalization can similarly be used for line-side losses (Aronson at 15:1-7). Aronson's teaching adapting cable-dependent equalization parameters gave an ordinarily skilled artisan reason to make the design choice to adapt the cable-dependent equalization parameters for the FIR 17 of DSP 13 and equalizer 21 during Lugthart '414's training phases.

An ordinarily skilled artisan's knowledge of the benefits of using adaptive cable-dependent parameters in active copper cables like Lugthart '414 's and Aronson's—including better distortion compensation yielding better signal quality and lower error rates—gave ordinarily skilled artisans additional reasons to make the design choice to make the cable-dependent parameters in the FIR 17 and equalizer 21 adaptive during Lugthart '414 's training phases. *See, e.g.*, Lugthart '414 at 48:64-49:37; U.S. Patent No. 6,621,862 at 1:39-51 (adaptive equalization yields "[b]etter signal quality and lower bit error rates" than "static equalization"); U.S. Patent App. Pub. No. 2010/0232492 at [0027] ("Adaptive transmit equalization enables enhanced performance compared to fixed equalization," can support "a broader range of cable lengths" and "tolerances," can "simplif[y] receiver design," and "may save [transmitter] power … by using power back-off," compared to fixed transmit equalization or receiver equalization).

It was known that environmental conditions like temperature, bending and vibration can impact signal transmission through a cable and that adaptive equalization compensated for such environmental conditions that may differ from a factory-testing environment. *See, e.g.*, U.S. Patent App. Pub. No. 2017/0187463 at [0057] (ISI changes over time based on environmental conditions like temperature, physical bending, vibrations); U.S. Patent No. 6,055,269 at 2:5-11, 3:16-17 (adaptive equalization can compensate variations in channel distortion from changes in humidity, temperature, and power); U.S. Patent No. 6,621,862 at 1:39-51 ("Conventional adaptive equalization … is … better able to compensate for unpredictable and time-dependent distortion [than static equalization]."). An ordinarily skilled artisan understood that these environmental conditions (e.g., bending) may have a greater impact on the cable than on host traces and thus lead an ordinarily skilled artisan to choose adaptive cable-dependent parameters while choosing fixed cable-independent parameters for host-side losses.

Using fixed (rather than adaptive) cable-dependent parameters was also a known obvious alternative. Demonstrating obviousness of either alternative does not require showing that one was a better option than the other—only that each was a known suitable option. *Intel v. Qualcomm*, 21 F.4th 784, 800 (Fed. Cir. 2021) ("It's not necessary to show that a combination is the best option, only that it be a suitable option.") (cleaned up). The inventors' claiming both known alternatives does not render either non-obvious. *See, e.g.*, claims 3 ("adapt") and 4 ("fixed"); *KSR*, 550 U.S., 421 (obvious to pursue finite number of identified predictable solutions).

Using adaptive cable-dependent parameters in the FIR 17 and equalizer 21 of Lugthart '414—trained during Lugthart's training phases—would have been nothing more than combining prior art elements using known methods to yield the predictable results of cable-dependent equalization parameters that better compensate for the cable's installed environment. *KSR*, 550 U.S., 417-418.

Line-Side Cable-Dependent Parameters Determined During Manufacturing-Testing and Fixed During Normal Usage

While Aronson teaches the design choice of adapting the cable-dependent line-side equalization parameters, Aronson is explicit that line-side pre-equalization by the pre-emphasis/output driver—and received line-side signal equalization—in Figures 12A-12B (below) can be determined during manufacturing-testing and then fixed. *See, e.g.*, Aronson at 14:33-39 (Fig. 12A's pre-equalization can be "adjusted at factory setup"), 15:1-7 (Fig. 12B's equalization may be "fixed;" "[a]djustable but factory set equalization" is of "particular interest").

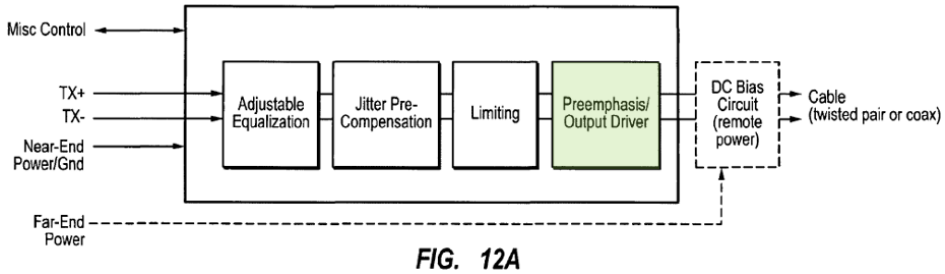


FIG. 12A

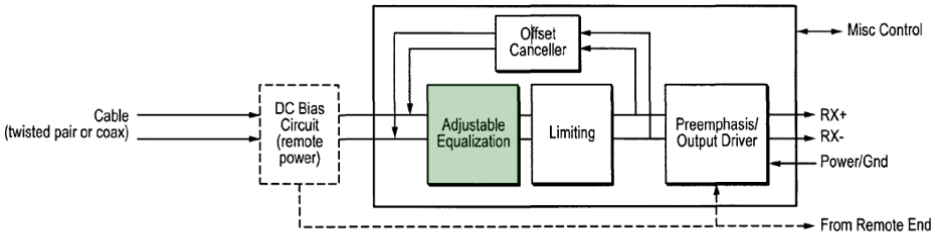


FIG. 12B

The known benefits from using fixed parameters—e.g., reducing complexity and manufacturing cost—for equalizing received and pre-equalizing transmitted signals for distortion from transmission over a copper cable, as in Lugthart '414 and Aronson, would have given ordinarily skilled artisans further reason to make the design choice to fix the cable-dependent parameters in DSP 13's FIR 17 and equalizer 21 of Lugthart '414. *KSR*, 550 U.S., 421 (obvious to pursue finite number of identified predictable solutions).

Indeed, ordinarily skilled artisans understood that factory-set fixed parameters for line-side equalizers are of "particular interest because the cable length and characteristics will be established at the time of the cable manufacture." *See, e.g.*, Aronson at 15:6-8; U.S. Patent App. Pub. No. 2006/0045176 at [0031]-[0032] (fixed parameters optimized for known cable length are simple and reliable).

Fixing the parameters for the FIR 17 and equalizer 21 of Lugthart '414 to values determined during manufacturing-testing would have been nothing more than combining prior art elements, using known methods, yielding the predictable results of fixed equalization parameters that require less complexity and cost to implement. *KSR*, 550 U.S., 417-418.

An ordinarily skilled artisan would have had a reasonable expectation of success in implementing Lugthart '414 's transceivers in any and all of the ways discussed previously. For example, Lugthart '414 already discloses cable-dependent and cable-independent parameters that ordinarily skilled artisans understood can be fixed or adaptive, and every above-discussed design

choice was well-known as demonstrated by Aronson and numerous other references corroborating an ordinarily skilled artisan's background knowledge. Implementing these techniques well-known for use in active copper cables like those disclosed in Lugthart '414 was well within an ordinarily skilled artisan's capabilities.

As another example, a person of ordinary skill in the art would have been motivated to combine U.S. Patent App. Pub. No. 2013/0115803 ("Tang") (B-2) with Texas Instruments DS125DF1610 9.8 to 12.5 Gbps 16-Channel Retimer ("DS125DF1610") (Ex. B-11) and U.S. Patent No. 7,762,727 ("Aronson") (Ex. B-11) to render obvious claims 1–4, 6–9, and 11–14.

Tang was filed on November 9, 2011, and was published on May 9, 2013. Tang qualifies as prior art under 35 U.S.C. § 102 (AIA).

Tang is directed to networking data cables supporting Ethernet communications between transceivers in host devices (e.g., servers, routers, switches). *See, e.g.*, Tang at [0001]-[0002], [0014]-[0017]. Cable 10 may include one QSFP+ end for plugging into a first transceiver 12 and across the cable four SFP+ ends for plugging into four transceivers 14a-14d. *See, e.g., id*. at [0017]-[0019], Fig. 1A (below).

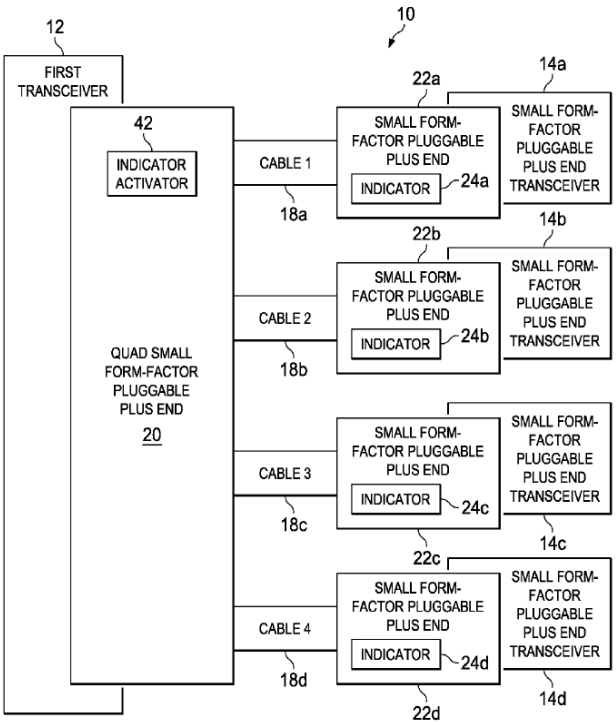


FIG. 1A

In one variation, cable 10 includes SFP+ ends 22k/22l on each side, connected by twinaxial copper cable 18a. *See, e.g.*, Tang at [0045]-[0047], Fig. 6 (below). Each SFP+ end 22k/22l has two "signal drivers 44 (e.g., CDR)": one to handle an inbound data stream that is received from a host and transmitted over the cable, and the other to handle an outbound data stream transmitted from the cable to the host. *See, e.g., id.* at [0037] (defining "CDR" as clock and data recovery), [0045].

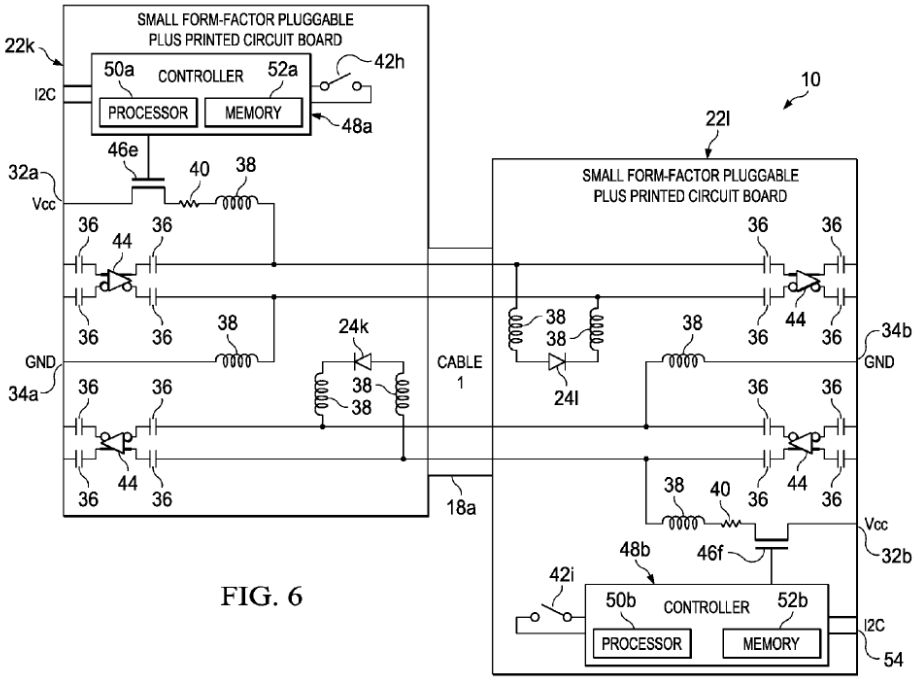


FIG. 6

In March 2017, Texas Instruments published a data sheet for its DS125DF1610 retimer chip. The DS125DF1610 publication qualifies as prior art under 35 U.S.C. § 102(a)(1)(AIA).

The DS125DF1610 is a 9.8 to 12.5 Gbps 16-Channel Retimer integrated circuit, and the retimer signal conditioning features include a continuous time linear equalizer (CTLE), CDR, and transmit FIR filter for each of its sixteen channels. *See, e.g.*, DS125DF1610 at Sections 3, 7. Each channel supports differential input and output signals. *See, e.g., id*. at 13-14, 19, Figs. 1-2 (differential input/output); *see also* Sections 7.3.2 (differential receiver input), 7.3.8 (differential driver output). Figure 2 (below) illustrates the data path for a single channel from received input signal IN, through the CTLE (labelled "EQ"), CDR, and FIR Filter, before being output as signal OUT.

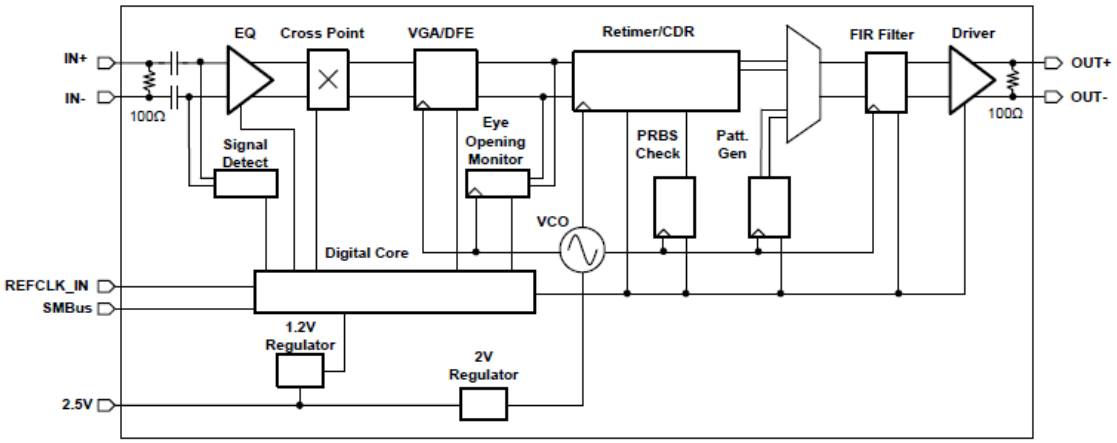


Figure 2. DS125DF1610 Simplified Data Path Diagram

The signal conditioning features "enhance… robustness over long, lossy, crosstalk impaired high speed serial links," such as "lossy copper interconnects and backplanes." *See, e.g.*, DS125DF1610 at Sections 3, 7.3.3 (CTLE is an "equalizer"), 7.3.6 ("equalized data is fed into the CDR for clock and data recovery" and "recovered data is then output to the FIR filter"), 7.3.8 (FIR filter "assist[s] with transmit equalization").

U.S. Patent No. 7,762,727 to Aronson ("Aronson")was filed on October 31, 2008, was issued on July 27, 2010, and claims domestic priority to U.S. Patent Application No. 11/401,803 filed on April 10, 2006. Aronson qualifies as prior art under 35 U.S.C. § 102(a)(1)(AIA) and 35 U.S.C. § 102(a)(2)(AIA).

Aronson discloses an active cable for high-speed transmissions between network nodes. *See, e.g.*, Aronson at Abstract, 1:12-21. While Aronson's title recites an optical cable, Aronson also discloses copper twisted-pair or coaxial cables like Lugthart '414. *See, e.g., id*. at 1:29-2:23, 7:17-20. Figures 12A-12B (below) illustrate features "incorporated into the ICs in a copper active cable design." *See, e.g., id*. at 14:16-15:24.

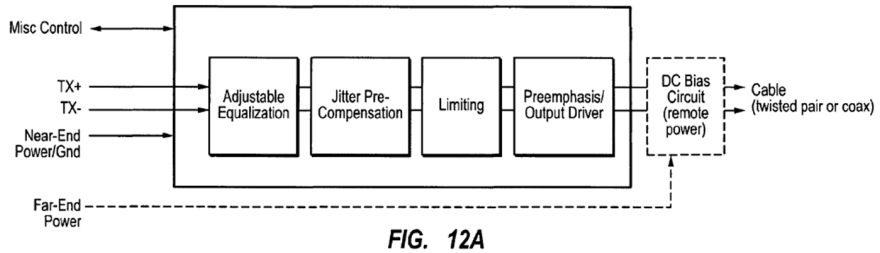


FIG. 12A

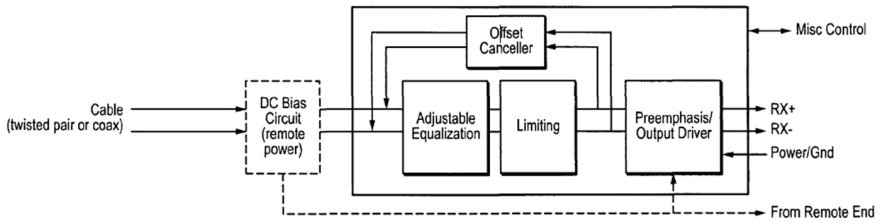


FIG. 12B

Figure 12A's circuit processes TX signals from the host and transmits signals over the cable, where equalization "compensat[es] for high frequency loss in the host board traces," and pre-equalization overcomes loss on the cable and "match[es]" loss from "the particular length [and] characteristics of the copper cabling." *See* Aronson at 14:16-43. Figure 12B's circuit handles dataflow in the other direction: it receives RX signals from the cable, performs equalization "to compensate for" cable losses, and—before transmitting to the host—performs pre-emphasis to "overcome high frequency losses on long [host-side] PCB traces." *See, e.g., id*. at 15:1-6, 15:17-24. Signal pre-emphasis and/or equalization can be "fixed, adjustable, or adaptable." *See, e.g., id*. at Abstract, 14:19-23, 14:33-34, 15:1-8, 15:17-23.

Tang's active Ethernet data cable has signal drivers 44 that include, e.g., CDR. *See, e.g.,* Tang at Abstract, [0014]-[0017], [0045]-[0047]. Tang does not describe in detail how to implement signal drivers 44 and other aspects of the cable, so a ordinarily skilled artisan implementing Tang's cable would have had reasons to implement Tang's signal drivers 44 using known components. *See id*. at [0052].

An ordinarily skilled artisan had reasons to use the DS125DF1610 chip to implement Tang's signal driving circuits 44. *See, e.g.* DS125DF1610 at 2-7 (use of DS125DF1610 chip in active copper cables). Tang describes "data cable 10" for 10 Gb "Ethernet connectivity" (Tang at [0016]), which the DS125DF1610 chip supports (*see, e.g.*, DS125DF1610 at 1, 10 (§6.6, input data rate)). The DS125DF1610 chip describes a signal driving circuit of the type used in Tang and was well-suited to use in Tang's active cable because DS125DF1610 chip has the CDR signal processing disclosed in Tang (*see* Tang at [0037]) and "enhance[s]… robustness over long, lossy, crosstalk impaired high speed serial links," such as "lossy copper interconnects and backplanes" (*see, e.g.*, DS125DF1610 at Section 3), which ordinarily skilled artisans understood describe the line-side and host-side connections for the transceivers in the connectors of Tang's active cable.

Additionally, ordinarily skilled artisans knew that standard-based connectors like Tang describes were customizable with various circuitry, including filters, amplifiers, transceivers, and other "active" components. See, e.g., U.S. Patent App. Pub. No. 2020/0194911 at [0065], [0099]. Thus, implementing Tang's signal driver 44 using the DS125DF1610 chip would have been nothing but a "simple substitution of one known element [DS125DF1610 chip] for another [Tang's signal driver 44]" to obtain predictable results [Tang's cable using the DS125DF1610 chip to implement signal driver 44]. *KSR*, 550 U.S. at 417-418. This combination is nothing more than an "application of a known technique [DS125DF1610 chip] to a piece of prior art ready for improvement [Tang's cable, relying on ordinarily skilled artisan's knowledge of how to implement signal driver 44]" to yield predictable results [Tang's cable using DS125DF1610 chip to implement signal driver 44]. *KSR*, 550 U.S. at 417-418; Min, ¶261.

In Figure 6 below, the Tang-DS125DF1610 chip combination uses a channel of the DS125DF1610 chip for each transmit or receive channel in Tang's connectors ("Form Factor

Pluggable), with one the DS125DF1610 chip channel handling the inbound data stream (highlighted yellow below) from the host and the other (shown upside down below) handling the outbound data stream (highlighted blue below) to the host.

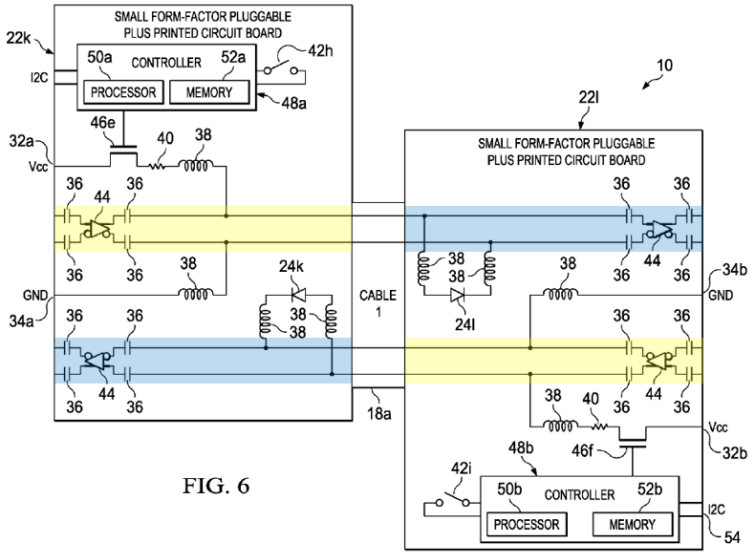


FIG. 6

While this analysis references Tang's Figure 6 for simplicity (showing two channels analogous to the '252 claims), ordinarily skilled artisans would have found the DS125DF1610 chip advantageous for single-chip implementation in any of Tang's embodiments (or variations thereof) with additional channels (*e.g.*, Tang Figure 1A-1B's "quad" ends process eight channels each). *See, e.g.*, Tang at [0017]-[0018].

Fixed Cable-Independent Parameters for Host-Side Equalization

In the Tang-DS125DF1610 combination figures shown above, the equalizer EQ in the channel handling the yellow-highlighted data stream performs equalization on inbound signals from the host, and the FIR filter in the channel handling the blue-highlighted data stream performs pre-equalization on outbound signals transmitted to the host.

For the same reasons discussed above, an ordinarily skilled artisan would have implemented the host-side equalization (via the yellow-highlighted EQ) and the host-side pre-

equalization (via the blue-highlighted FIR Filter) in the Tang-DS125DF1610 combination by using fixed cable-independent parameters to address host-side losses as taught by Aronson and numerous references corroborating an ordinarily skilled artisan's background knowledge.

Cable-Dependent Parameters for Line-Side Equalization

In the Tang-DS125DF1610 combination figures shown above, the equalizer EQ in the blue-highlighted signal processing channel equalizes line-side signals received from across the cable from the other connector, and the FIR filter in the yellow-highlighted signal processing channel pre-equalizes signals transmitted across the cable to the other connector.

For the same reasons discussed above, an ordinarily skilled artisan would have implemented the line-side equalization (via the blue-highlighted EQ) and the line-side pre-equalization (via the yellow FIR Filter) in the Tang-DS125DF1610 combination by using cable-dependent parameters to address cable-side losses as taught by Aronson and numerous references corroborating an ordinarily skilled artisan's background knowledge.

Adapting the Line-Side Cable-Dependent Parameters

For the same reasons discussed above, an ordinarily skilled artisan had reasons to use adaptive cable-dependent parameters for the line-side equalization (via the blue-highlighted EQ) and line-side pre-equalization (via the yellow FIR Filter) in the Tang-DS125DF1610 combination as taught by Aronson and numerous references corroborating an ordinarily skilled artisan's background knowledge of the desirable design choice option of using adaptive equalization parameters. This adaption would have been obvious to perform during the DS125DF1610 chip's CDR lock acquisition process—i.e., during an adjustment period. *See, e.g.*, DS125DF1610 at Section 7.3.3 (CTLE adaption).

Line-Side Cable-Dependent Parameters Determined During Manufacturing-Testing and Fixed During Normal Usage

For the same reasons discussed above, an ordinarily skilled artisan had reasons to determine the cable-dependent parameters for the line-side equalization (via the blue-highlighted EQ) and line-side pre-equalization (via the yellow FIR Filter) in the Tang-DS125DF1610 combination during manufacturing-testing and then fix those parameters during normal usage as taught by Aronson and numerous references corroborating an ordinarily skilled artisan's background knowledge of the desirable design choice option of using adaptive equalization parameters.

An ordinarily skilled artisan would have had a reasonable expectation of success in implementing the Tang-DS125DF1610 combination in all of the ways discussed above. Aronson and other references corroborating an ordinarily skilled artisan's background knowledge demonstrate that each above-discussed design choice was well-known. Implementing these well-known techniques for use in active cables like Tang's, using signal processing circuits similar to those disclosed in the DS125DF1610 chip, was well-within an ordinarily skilled artisan's capabilities.

An ordinarily skilled artisans understood that the DS125DF1610 chip worked with, or without, adaptation because it provides configurable settings for enabling/disabling adaptation. *See, e.g.*, DS125DF1610 at Section 7.5, Address 31 (describing a setting for "no adaption" of the CTLE). If every DS125DF1610 chip equalization component does not specifically implement selectable fixed and adaptive equalization, the known benefits of fixed and adaptive equalizers provided reasons to implement that functionality, as discussed above. The Tang-DS125DF1610-Aronson combination with compensation for the host, compensation for the cable, and fixed or

adaptive equalization would have required no more than a ordinarily skilled artisan's ordinary skill.

Similarly, a POSITA would have been motivated to combine Lugthart 431 in view of either TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Rianni, or Zheng, or a combination thereof; TI DS110DF111 in view of Lugthart 431, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or a combination thereof; TI DS125DF410 in view of Lugthart 431, or TI DS110DF111, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Cornelius, or Musah, or Riani, or Zheng, or a combination thereof; Vijayaraghavan in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Carter, or Cornelius, or Musah, or Rianni, or Zheng, or a combination thereof; or Carter in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Cornelius, or Musah, or Rianni, or Zheng, or a combination thereof; or Cornelius in view of Lugthart 431, or TI DS110DF111, or TI DS125DF410, or CMIS, or Chung, or Vijayaraghavan, or Carter, or Musah, or Rianni, or Zheng, or a combination thereof with a reasonable expectation of success.

To the extent that it is determined that any of these references do not disclose or render obvious "electrical conductors connected between a first connector and a second connector," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include electrical conductors connected between a first connector and a second connector in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI

DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, each of which teach electrical conductors connected between a first connector and a second connector. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 1[a]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose electrical conductors connected between a first connector and a second connector, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses "cable configurations" including "conducting lines 111" that "can include metal (e.g., copper) conductors," Carter discloses a "first device" coupled to "an electrical cable or optical cable," Cornelius discloses an "active cable" including "two active plugs 500 and 505, one on each end of cable 507," and Vijayaraghavan discloses a "bi-directional lane which is configured to communicate data between two communication devices" and "may use two pairs of differential lines to communicate data in both directions at the same time." Exs. B-3, B-8, B-4, B-7 (claim 1[a]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to use electrical conductors connected between a first connector and a second connector. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 1[a]);. Indeed, using electrical conductors connected between a first connector and a second connector is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such a device would thus require nothing more than the application of a known solution (electrical conductors), according to its established function (to connect a first connector and a second connector), yielding a predictable result (greater

data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so. To the extent that it is determined that any of these references do not disclose or render obvious "each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach that each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 1[b]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, and Vijayaraghavan, where they disclose each of the first and second connectors being adapted to fit into an Ethernet port of

a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable, with the embodiments of at least TI DS110DF111, TI DS125DF410, Cornelius, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111" as well as "the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111," Carter discloses a "converter device 10 that is configured to connect to a first device 12 and a second device 14" that "converts traffic data" and comprises a first connector that is configured to connect to (or to be coupled to) a connector 16 within the first device 12," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-8, B-7 (claim 1[b]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 1[b]). Indeed, each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal

conveying an outbound data stream from the cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. It would thus require nothing more than the application of a known solution (each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device), according to its established function (to receive from that host device an electrical input signal conveying an inbound data stream to the cable and to provide to that host device an electrical output signal conveying an outbound data stream from the cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream, in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter,

Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 1[c]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, and/or any combinations therein. *See* Exs. B-3 – B-9, B-11 (claim 1[c]). As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-8, B-7, B-4 (claim 1[b]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater

data processing capabilities and efficiency in cable applications. It was also already well-known in the art to use first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See, e.g.*, Exs. B-1 – B-9, B-11 (claim 1[c]). Indeed, using first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. It would thus require nothing more than the application of a known solution (each of the first and second connectors including a respective transceiver), according to its established function (for performing clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream), yielding a predictable result (the communication of electrical transit signals between a first device and a second device). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof,

with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 1[d]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a

plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 1[d]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 1[d]). Indeed, the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. It would thus require nothing more than the application of a known solution (the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal), according to its established function (to extract and re-modulate the transit data stream as the outbound data stream from the cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal," a person of ordinary skill

in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, Lusted, Yin, Yu, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, Lusted, Yin, Yu, each of which teach the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 1[e]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, CMIS, and TI DS110DF111 where they disclose the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal, with the embodiments of at least Lugthart 431, TI DS125DF410, Chung, Cornelius, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses that "the TX equalizer circuitry may be configured to compensate for channel loss" and "may perform pre-emphasis" and that "equalization-related settings are obtained," including "UC

TX preset coefficient data," TI DS110DF111 discloses "output de-emphasis compensates for the lossy transmission medium at the output" and that it "cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set of reach channel independently," CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-7, B-8, B-5, B-11 (claim 1[e]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 1[e]). Indeed, the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. It would thus require nothing more than the application of a known solution (the respective transceivers each employing fixed, cable-independent, equalization parameters), according to its established function (for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a

person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, Lusted, Ikeda, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, Lusted, Ikeda, each of which teach that the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 2). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, Cornelius, CMIS where they disclose a first controller that configures a first DRR device in response to a power-on event and retrieves the transmit filter coefficient values from the nonvolatile memories as part of said configuring, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any

combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-4, B-7, B-8, B-11 (claim 2). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 2). Indeed, that the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (employing cable-dependent equalization parameters), according to its established

function (for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters adapt during usage of the Ethernet cable," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, Lusted, Ikeda or a combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that said cable-dependent equalization parameters adapt during usage of the Ethernet cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, Lusted, Ikeda each of which teach that said cable-dependent equalization parameters adapt during usage of the Ethernet cable. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 3). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, Cornelius, CMIS where they disclose that said cable-dependent equalization parameters adapt during usage of the Ethernet cable, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the

signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-4, B-7, B-8, B-11 (claim 3). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters adapt during usage of the Ethernet cable. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 3). Indeed, that said cable-dependent equalization parameters adapt during usage of the Ethernet cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (adapting cable-dependent equalization parameters), according to its established function (during the usage of the Ethernet cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters are fixed during normal usage of the

Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, Lusted, Ikeda or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, Lusted, Ikeda, each of which teach that said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 4). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Vijayaraghavan, Cornelius, CMIS,Lusted, Ikeda where they disclose that said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable, with the embodiments of at least TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "start-up phase to determine the channel parameters such as, for example, loss, noise, dispersion, non-linearity, etc.," Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at

242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-3, B-4, B-7, B-8, B-11 (claim 4). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 4). Indeed, that said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (determining equalization parameters during manufacturing-testing of the Ethernet cable), according to its established function (to fix cable-dependent equalization parameters during normal usage of the Ethernet cable), yielding a predictable result (greater data processing capabilities and

efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, Norimatsu, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, Norimatsu each of which teach that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 5). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, TI DS125DF410, and Musah where they disclose that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd, with the embodiments of at least TI DS110DF111, CMIS, Chung, Vijayaraghavan, Cornelius, Rianni, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses "speeds of between about 480 Mbits/s/ and about 10Gbit/s," Carter discloses "speeds faster than 10 gigabits per second (G) and in particular 40 G and 100G," TI DS125DF410 discloses "Data Rates from 9.8 to 12.5 Gbps," and Musah discloses "data rate of up to 32 Gb/s per lane." Exs. B-

3, B-6, B-8, B-11 (claim 5). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 5). Indeed, that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of

which teach receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[a]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, and Vijayaraghavan, where they disclose receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device, with the embodiments of at TI DS110DF111, TI DS125DF410, Cornelius, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111" as well as "the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111," Carter discloses a "converter device 10 that is configured to connect to a first device 12 and a second device 14" that "converts traffic data" and comprises a first connector that is configured to connect to (or to be coupled to) a connector 16 within the first device 12," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-7, B-8 (claim 6[a]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[a]). Indeed, receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using

such techniques would thus require nothing more than the application of a known solution according to its established function (receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[b]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS,

Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 6[b]). A POSITA would have been motivated with a reasonable expectation of success to make such combinations to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[b]). Indeed, performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream), yielding a predictable result (greater data processing capabilities

and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[c]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit

12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 6[c]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[c]). Indeed, re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[d]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, and Vijayaraghavan, where they disclose receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device, with the embodiments of at least TI DS110DF111, TI DS125DF410, Cornelius, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111" as well as "the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111," Carter discloses a "converter device 10 that is configured to connect to a

first device 12 and a second device 14" that "converts traffic data" and comprises a first connector that is configured to connect to (or to be coupled to) a connector 16 within the first device 12," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-7, B-8 (claim 6[d]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to receive with the second connector a second electrical input signal conveying a second inbound data stream from a second host device. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[d]). Indeed, receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been

obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[e]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11 As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 6[e]). A POSITA would have been

motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to perform clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[e]). Indeed, performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs in view of the teachings of at least the knowledge

of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[f]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 6[f]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the second inbound data stream as a second transit data stream conveyed

by a second electrical transit signal over a second of the conductor pairs. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[f]). Indeed, re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream. *See, e.g.,* Exs. B-3

– B-9, B-11 (claim 6[g]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 6[g]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to perform clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[g]). Indeed, performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using

such techniques would thus require nothing more than the application of a known solution (performing clock and data recovery on the first electrical transit signal with the second transceiver), according to its established function (to extract the first transit data stream), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[h]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni,

Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 6[h]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[h]). Indeed, re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have

been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[i]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive

path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-4, B-3, B-7, B-8 (claim 6[i]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to perform clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[i]). Indeed, performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (performing clock and data recovery on the second electrical transit signal with the first transceiver), according to its established function (to extract the second transit data stream), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device," a person of ordinary skill in the art would

have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[j]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor (DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and

data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 6[j]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[j])]. Indeed, re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of

any of the above recited references to include wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 6[k]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, CMIS, and TI DS110DF111 where they disclose wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters, with the embodiments of at least Lugthart 431, TI DS125DF410, Chung, Cornelius, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11 As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses that "the TX equalizer circuitry may be configured to compensate for channel loss" and "may perform pre-emphasis" and that "equalization-related settings are obtained," including "UC TX preset coefficient data," TI DS110DF111 discloses "output de-emphasis compensates for the

lossy transmission medium at the output" and that it "cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set of reach channel independently," CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-7, B-8, B-5, B-11 (claim 6[k]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 6[k]). Indeed, wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters), yielding a predictable result (greater data processing

capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include cable-dependent equalization parameters employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters. *See, e.g.,* Exs. B-3 – B-9, B-11

(claim 7). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, Cornelius, CMIS where they disclose cable-dependent equalization parameters employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11 As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-8, B-7, B-4, B-11 (claim 7). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound

data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 7). Indeed, cable-dependent equalization parameters employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (cable-dependent equalization parameters are employed), according to its established function (for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters are adaptively updated," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include said cable-

dependent equalization parameters are adaptively updated in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach said cable-dependent equalization parameters are adaptively updated. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 8). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, Cornelius, CMIS where they disclose said cable-dependent equalization parameters are adaptively updated, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-4, B-7, B-8, B-11 (claim 8). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters are adaptively updated. *See, e.g.*, Exs.

B-3 – B-9, B-11 (claim 8). Indeed, that said cable-dependent equalization parameters are adaptively updated is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (said cable-dependent equalization parameters are adaptively updated), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable. *See, e.g.,* Exs. B-3 – B-

9, B-11 (claim 9). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Vijayaraghavan, Cornelius, CMIS where they disclose said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable, with the embodiments of at least TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "start-up phase to determine the channel parameters such as, for example, loss, noise, dispersion, non-linearity, etc.," Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-3, B-4, B-7, B-8, B-11 (claim 9). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining

said cable-dependent equalization parameters during manufacturer-testing of the network cable. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 9). Indeed, that said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first inbound data stream has a per-lane symbol rate in excess of 50 GBd," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 10). For example, a POSITA would have been motivated to

incorporate the embodiments of at least each of Lugthart 431, Carter, TI DS125DF410, and Musah where they disclose that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd, with the embodiments of at least TI DS110DF111, CMIS, Chung, Vijayaraghavan, Cornelius, Rianni, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses "speeds of between about 480 Mbits/s/ and about 10Gbit/s," Carter discloses "speeds faster than 10 gigabits per second (G) and in particular 40 G and 100G," TI DS125DF410 discloses "Data Rates from 9.8 to 12.5 Gbps," and Musah discloses "data rate of up to 32 Gb/s per lane." Exs. B-3, B-8, B-6, B-11 (claim 10). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 10). Indeed, that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first inbound data stream has a per-lane symbol rate in excess of 50 GBd), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second

transceiver to the first transceiver," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 11[a]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver, with the embodiments of at least TI DS110DF111, TI DS125DF410, CMIS, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses "cable configurations" including "conducting lines 111" that "can include metal (e.g., copper) conductors," Carter discloses a "first device" coupled to "an electrical cable or optical cable,"

Cornelius discloses an "active cable" including "two active plugs 500 and 505, one on each end of cable 507," and Vijayaraghavan discloses a "bi-directional lane which is configured to communicate data between two communication devices" and "may use two pairs of differential lines to communicate data in both directions at the same time." Exs. B-4, B-7, B-8 (claim 11[a]). Additionally, Lugthart 431 discloses a "first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111" as well as "the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111," Carter discloses a "converter device 10 that is configured to connect to a first device 12 and a second device 14" that "converts traffic data" and comprises a first connector that is configured to connect to (or to be coupled to) a connector 16 within the first device 12," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-7, B-8 (claim 11[a]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to connect a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 11[a]). Indeed, connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver is but one of a finite number of known, predictable solutions to achieve greater data

processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively), according to its established function (to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach packaging the first transceiver into a first connector configured

to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 11[b]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, and Vijayaraghavan, where they disclose packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device, with the embodiments of at least TI DS110DF111, TI DS125DF410, Cornelius, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111" as well as "the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111," Carter discloses a "converter device 10 that is configured to connect to a first device 12 and a second device 14" that "converts traffic data" and comprises a first connector that is configured to connect to (or to be coupled to) a connector 16 within the first device 12," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-7, B-8 (claim 11[b]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to package the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical

output signal from the first transceiver to the network interface port of the first host device. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 11[b]). Indeed, packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (packaging the first transceiver into a first connector), according to its established function (configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include packaging the second transceiver into a second connector

configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 11[c]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, and Vijayaraghavan, where they disclose packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device, with the embodiments of at least TI DS110DF111, TI DS125DF410, Cornelius, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "first transceiver assembly 105a includes a host side that is electrically connected to the first electronic device 101a and a line side that is electrically connected to a first end of the conductive lines 111" as well as "the second transceiver assembly 105b includes a host side that is electrically connected to the second electronic device 101b and a line side that is electrically connected to a second end of the conductive lines 111," Carter discloses a "converter device 10 that is configured to connect to a first device 12 and a second device 14" that "converts traffic data" and comprises a first connector that is configured to connect to (or to be coupled to) a connector 16 within the

first device 12," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-7, B-8 (claim 11[c]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to package the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 11[c]). Indeed, packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (packaging the second transceiver into a second connector), according to its established function (configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers being configured to perform clock and data recovery on

the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach that the first and second transceivers being configured to perform clock and data

recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 11[d]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, CMIS, TI DS110DF111, and Vijayaraghavan, where they disclose that the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals, with the embodiments of at least TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng, and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "the transceiver 10 includes a first transmit path equalizer 11a, a second transmit path equalizer 11b, a first transmit path clock and data recovery (CDR) circuit 12a, a second transmit path CDR circuit 12b, a transmit path digital signal processor

(DSP) 13, a transmit path DAC 14, a receive path equalizer 21, a receive path CDR circuit 22, a receive path DSP 23, a first receive path DAC 24a, and a second receive path DAC 24b," Carter discloses a "converter device 10 converts traffic data between the first form factor pluggable standard and the second form factor pluggable standard in a variety of data transport modes to enable connectivity between the first device and a plurality of different types of second devices," Cornelius discloses a device containing "clock and data recovery circuits," Vijayaraghavan discloses "two devices" with "transmitter (TX) circuit and a receiver (RX) circuit." Exs. B-3, B-4, B-5, B-7, B-8, B-11 (claim 11[d]). Additionally, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses that "the TX equalizer circuitry may be configured to compensate for channel loss" and "may perform pre-emphasis" and that "equalization-related settings are obtained," including "UC TX preset coefficient data," TI DS110DF111 discloses "output de-emphasis compensates for the lossy transmission medium at the output" and that it "cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set of reach channel independently," CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-11 (claim 11[d]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-

modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 11[d]). Indeed, that the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-

modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach that the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 12). For example,

a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, Cornelius, CMIS where they disclose that the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-4, B-7, B-8, B-11 (claim 12). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 12). Indeed, that

the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 13). For example,

a POSITA would have been motivated to incorporate the embodiments of at least each of Carter, Vijayaraghavan, Cornelius, CMIS where they disclose that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation, with the embodiments of at least Lugthart 431, TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-4, B-7, B-8, B-11 (claim 13). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation. *See, e.g.*, Exs. B-3 – B-9, B-11 (claim 13). Indeed, that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in

cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters," a person of ordinary skill in the art would have been motivated to combine Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Kobayashi, Zheng, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart 431, TI DS110DF111, TI DS125DF410, CMIS, Carter, Chung, Vijayaraghavan, Cornelius, Musah, Rianni, Zheng, each of which teach that the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters. *See, e.g.,* Exs. B-3 – B-9, B-11 (claim 14). For example, a POSITA would have been motivated to incorporate the embodiments

of at least each of Lugthart 431, Carter, Vijayaraghavan, Cornelius, CMIS where they disclose that the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters, with the embodiments of at least TI DS110DF111, TI DS125DF410, Chung, Musah, Rianni, Kobayashi, Zheng and/or any combinations therein. *See* Exs. B-3 – B-9, B-11. As specific examples, Lugthart 431 discloses a "start-up phase to determine the channel parameters such as, for example, loss, noise, dispersion, non-linearity, etc.," Carter discloses that "the controller 130 retrieves from non-volatile memory 144 (FIG. 3), specific transmit emphasis parameters, and at 242, supplies those transmit emphasis parameters to the signal processor," Vijayaraghavan discloses a TX equalizer circuitry "configured to compensate for channel loss" and "perform pre-emphasis" with "DC preset data" "obtained from firmware at the UC by the equalization controller," Cornelius discloses that "the clock and data recovery circuits may employ equalizer circuits, buffers, emphasis, and de-emphasis circuits" and that "operational parameters" "may be configured" to "allow cables to adapt to new hosts and devices as the cable is used in various system applications," and CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Exs. B-3, B-4, B-7, B-8, B-11 (claim 14). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-

dependent equalization parameters. *See, e.g.*, Exs. B-3 – B-9, B-11 – B-9, B-11 (claim 14). Indeed, that the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

Similarly, a POSITA would have been motivated to combine the SMP9 Cable in view of the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson.

To the extent that it is determined that any of these references do not disclose or render obvious "each of the first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that each of the first and

second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream, in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 1[c]). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Lugthart 431, Carter, Cornelius, and Vijayaraghavan, where they disclose first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream, with the embodiments of at least CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, and/or any combinations therein. *See* Ex. B-11 (claim 1[c]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to use first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream. *See, e.g.*, Exs. B-10 – B-11 (claim 1[c]). Indeed, using first and second connectors including a respective transceiver that performs clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. It would thus require nothing more than the application of a known solution (each of the first and second connectors including a respective transceiver), according to its

established function (for performing clock and data recovery on the electrical input signal to extract and re-modulate the inbound data stream for transit via the electrical conductors as a respective electrical transit signal conveying a transit data stream), yielding a predictable result (the communication of electrical transit signals between a first device and a second device). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 1[d]). For example, a POSITA would have been motivated to incorporate the embodiments of the SMP9 Cable, where it discloses the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable, with the embodiments of at least CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson and/or any combinations therein. *See* Exs. B-10 – B-11. A POSITA would have been motivated to make such combinations with a reasonable

expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable. *See, e.g.*, Exs. B-10 – B-11 (claim 1[d]). Indeed, the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. It would thus require nothing more than the application of a known solution (the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal), according to its established function (to extract and re-modulate the transit data stream as the outbound data stream from the cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references

to include the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 1[e]). For example, a POSITA would have been motivated to incorporate the embodiments of the SMP9 Cable where it discloses disclose the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal, with the embodiments of at least CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson and/or any combinations therein. *See* Exs. B-10 – B-11. As specific examples, CMIS discloses a "module control state" where "all memory map register locations shall be set to their power-on defaults" and control field such as "Tx Adaptive Input Eq Enable," "TX Adaptive Input Eq Recall," "Rx Output Eq control, pre-cursor," and "RX Output Eq control, post-cursor." Ex. B-11 (claim 1[e]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal. *See, e.g.*, Exs. B-10 – B-11 (claim 1[e]). Indeed, the respective transceivers each employing fixed, cable-independent, equalization parameters for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. It would thus require nothing more

than the application of a known solution (the respective transceivers each employing fixed, cable-independent, equalization parameters), according to its established function (for each of: the remodulation of the transit data stream as the outbound data stream, and the clock and data recovery performed on the electrical input signal), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 2). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the respective transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal. *See, e.g.*, Exs. B-10 – B-11 (claim 2). Indeed, that the respective

transceivers each employ cable-dependent equalization parameters for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (employing cable-dependent equalization parameters), according to its established function (for at least one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters adapt during usage of the Ethernet cable," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that said cable-dependent equalization parameters adapt during usage of the Ethernet cable in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 3). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters adapt during usage of the Ethernet cable. *See, e.g.*, Exs. B-10 – B-11 (claim 3). Indeed, that said cable-dependent equalization parameters adapt during

usage of the Ethernet cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (adapting cable-dependent equalization parameters), according to its established function (during the usage of the Ethernet cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 4). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable. *See, e.g.*, Exs. B-10 – B-11 (claim 4). Indeed, that said cable-

dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (determining equalization parameters during manufacturing-testing of the Ethernet cable), according to its established function (to fix cable-dependent equalization parameters during normal usage of the Ethernet cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 5). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd. *See, e.g.*, Exs. B-10 – B-11 (claim 5). Indeed, that the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of

50 GBd is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the inbound data stream and the outbound data stream each have a per-lane symbol rate in excess of 50 GBd), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device in view of the teachings of at least the knowledge of a POSITA *See, e.g.,* Exs. B-10 – B-11 (claim 6[a]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device. *See, e.g.*, Exs. B-10 – B-11 (claim 6[a]). Indeed, receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of

a known solution according to its established function (receiving with the first connector a first electrical input signal conveying a first inbound data stream from a first host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[b]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream. *See, e.g.*, Exs. B-10 – B-11 (claim 6[b]). Indeed, performing clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (performing

clock and data recovery on the first electrical input signal with a first transceiver in the first connector to extract the first inbound data stream), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[c]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs. *See, e.g.*, Exs. B-10 – B-11 (claim 6[c]). Indeed, re-modulating the first inbound data stream as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the first inbound data stream

as a first transit data stream conveyed by a first electrical transit signal over a first of the conductor pairs), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[d]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to receive with the second connector a second electrical input signal conveying a second inbound data stream from a second host device. *See, e.g.*, Exs. B-10 – B-11 (claim 6[d]). Indeed, receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (receiving with the second connector a second electrical input signal conveying a second inbound data stream from a second host device), yielding a predictable result (greater data processing

capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[e]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to perform clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream. *See, e.g.*, Exs. B-10 – B-11 (claim 6[e]). Indeed, performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the second inbound data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (performing clock and data recovery on the second electrical input signal with a second transceiver in the second connector to extract the

second inbound data stream), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[f]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs. *See, e.g.*, Exs. B-10 – B-11 (claim 6[f]). Indeed, re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical transit signal over a second of the conductor pairs is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the second inbound data stream as a second transit data stream conveyed by a second electrical

transit signal over a second of the conductor pairs), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[g]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to perform clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream. *See, e.g.*, Exs. B-10 – B-11 (claim 6[g]). Indeed, performing clock and data recovery on the first electrical transit signal with the second transceiver to extract the first transit data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (performing clock and data recovery on the first electrical transit signal with the second transceiver), according to its established function (to extract the first transit data stream), yielding a predictable result (greater

data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[h]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device. *See, e.g.*, Exs. B-10 – B-11 (claim 6[h]). Indeed, re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the first transit data stream as a second outbound data stream conveyed by a second electrical output signal to the second host device), yielding a predictable result (greater data processing capabilities and efficiency).

Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[i]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to perform clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream. *See, e.g.*, Exs. B-10 – B-11 (claim 6[i]). Indeed, performing clock and data recovery on the second electrical transit signal with the first transceiver to extract the second transit data stream is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (performing clock and data recovery on the second electrical transit signal with the first transceiver), according to its established function (to extract the second transit data stream), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art

would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[j]). A POSITA would have been motivated with a reasonable expectation of success to make such combinations to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to re-modulate the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device. *See, e.g.*, Exs. B-10 – B-11 (claim 6[j]). Indeed, re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (re-modulating the second transit data stream as a first outbound data stream conveyed by a first electrical output signal to the first host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of

ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 6[k]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters. *See, e.g.*, Exs. B-10 – B-11 (claim 6[k]). Indeed, wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said

performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (wherein said re-modulating the first transit data stream, said re-modulating the second transit data stream, said performing clock and data recovery on the first electrical input signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, eaualization [sic] parameters), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include cable-dependent equalization parameters employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed,

cable-independent, equalization parameters in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 7). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that cable-dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters. *See, e.g.*, Exs. B-10 – B-11 (claim 7). Indeed, cable-dependent equalization parameters employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (cable-dependent equalization parameters are employed), according to its established function (for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said peforming [sic] clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters are adaptively updated," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include said cable-dependent equalization parameters are adaptively updated in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 8). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters are adaptively updated. *See, e.g.*, Exs. B-10 – B-11 (claim 8). Indeed, that said cable-dependent equalization parameters are adaptively updated is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (said cable-dependent equalization parameters are adaptively updated), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable," a person of ordinary skill in the art would have

been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 9). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable. *See, e.g.*, Exs. B-10 – B-11 (claim 9). Indeed, that said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (said cable-dependent equalization parameters are fixed during normal usage, and wherein the method further comprises: determining said cable-dependent equalization parameters during manufacturer-testing of the network cable), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first inbound data stream has a per-lane symbol rate in excess of 50 GBd," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 10). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd. *See, e.g.*, Exs. B-10 – B-11 (claim 10). Indeed, that the first inbound data stream has a per-lane symbol rate in excess of 50 GBd is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first inbound data stream has a per-lane symbol rate in excess of 50 GBd), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second

transceiver to the first transceiver," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 11[a]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to connect a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver. *See, e.g.*, Exs. B-10 – B-11 (claim 11[a]). Indeed, connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively, to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second transceiver to the first transceiver is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (connecting a first end and a second end of a set of conductor pairs to a first transceiver and a second transceiver, respectively), according to its established function (to transport a first electrical transit signal from the first transceiver to the second transceiver and a second electrical transit signal from the second

transceiver to the first transceiver), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 11[b]). *See, e.g.*, Exs. B-10 – B-11 (claim 11[b]). Indeed, packaging the first transceiver into a first connector configured to couple a first electrical input signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (packaging the first transceiver into a first connector), according to its established function (configured to couple a first electrical input

signal from a network interface port of a first host device to the first transceiver and a first electrical output signal from the first transceiver to the network interface port of the first host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 11[c]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art to package the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device. *See, e.g.*, Exs. B-10

– B-11 (claim 11[c]). Indeed, packaging the second transceiver into a second connector configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution (packaging the second transceiver into a second connector), according to its established function (configured to couple a second electrical input signal from a network interface port of a second host device to the second transceiver and a second electrical output signal from the second transceiver to the network interface port of the second host device), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals," a person of ordinary skill in the art would have been motivated to

combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 11[d]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals. *See,*

e.g., Exs. B-10 – B-11 (claim 11[d]). Indeed, that the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re- modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers being configured to perform clock and data recovery on the first and second electrical input signal to extract and re-modulate the first and second inbound data streams respectively as the first and second electrical transit signals conveying first and second transit data streams, configured to perform clock and data recovery on the second and first electrical transit signals to extract and re-modulate the second and first transit data streams as first and second outbound data streams conveyed by the first and second electrical output signals from the cable, and each configured to employ fixed, cable-independent, equalization parameters for clock and data recovery on the respective electrical input signals and for generating the respective electrical output signals), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 12). *See, e.g.*, Exs. B-10 – B-11 (claim 12). Indeed, that the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers are each configured to employ cable-dependent equalization parameters for generating the first and second electrical transit signals and for clock and data recovery on the second and first electrical transit signals), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation in view of the teachings of at least the knowledge of a POSITA. *See, e.g.,* Exs. B-10 – B-11 (claim 13). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater data processing capabilities and efficiency in cable applications. It was also already well-known in the art that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation. *See, e.g.*, Exs. B-10 – B-11 (claim 13). Indeed, that the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers are each configured to adapt the cable-dependent equalization parameters during operation), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose or render obvious "the first and second transceivers are each configured to use preset cable-dependent

equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable with CMIS, Chung, Musah, Rianni, Kobayashi, Zheng, Aronson, or a combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include that the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exs. B-10 – B-11 (claim 14). Indeed, that the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters is but one of a finite number of known, predictable solutions to achieve greater data processing capabilities and efficiency in cable applications. Using such techniques would thus require nothing more than the application of a known solution according to its established function (the first and second transceivers are each configured to use preset cable-dependent equalization parameters during operation, and wherein the method further comprises: testing an assembled cable to determine the cable-dependent equalization parameters), yielding a predictable result (greater data processing capabilities and efficiency). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

Complainant has yet to indicate a belief that any of the prior art references do not supply any of the claim limitations. Respondents' motivations to combine the prior art to supply other

limitations may be amended or supplemented in view of Complainant's contentions regarding the missing limitations in the prior art references.

Secondary Considerations

Respondents are not aware of any secondary-considerations evidence demonstrating non-obviousness of the Asserted Claims of the '252 Patent. Complainants have not produced any documents related to secondary considerations, nor have Complainants identified any such secondary considerations, let alone demonstrated a nexus between any such considerations and the alleged inventions of the Asserted Claims of the '252 Patent.

As discussed in Appendix B, the prior art references confirm that the Asserted Claims of the '252 Patent would have been obvious to a POSITA before the earliest possible priority date. Respondents reserve the right to supplement or modify these factors to address any evidence or arguments later identified by Complainants.

Invalidity Grounds Under 35 U.S.C. § 112

. Subject to Respondents' reservation of rights above, Respondents identify their grounds of invalidity for the '252 Patent based on lack of enablement, written description, and indefiniteness pursuant to 35 U.S.C. §§ 112(a) and (b) below. The terms recited below are invalid based on lack of enablement, written description, and indefiniteness pursuant to 35 U.S.C. §§ 112(a) and (b) under any scope of the claim terms. If, however, an overbroad construction is applied, at least under the overbroad constructions that Complainants appear to be applying to the Asserted Claims of the '252 Patent, which go beyond (and are not adequately described or enabled by) the purported inventions allegedly disclosed in the '252 Patent, the claims are invalid for that additional reason. Specifically, to the extent that Complainants assert that the Asserted Claims of the '252 Patent are so broad as to cover the Respondents' respective Accused Products and alleged

domestic industry products, or to the extent that they may eventually be construed so broadly, such an interpretation or construction would render the Asserted Claims of the ’252 Patent invalid for failure to meet the requirements of 35 U.S.C. § 112. A more detailed discussion of Respondents’ written description, enablement, and indefiniteness defenses will be set forth in Respondents’ expert report(s) on invalidity.

Lack of Written Description and/or Enablement

The ’252 Patent does not provide sufficient written description to establish that the applicants were in possession of the alleged inventions recited in certain of the Asserted Claims at the time the ’252 Patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that “reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus.

The specification of the ’252 Patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the Asserted Claims without undue experimentation. To the extent the following limitations are definite, the application that became the ’252 Patent fails to sufficiently describe or enable them as required:

Term	Relevant Claim(s)	Basis
“fixed, cable-independent, equalization parameters”	1, 6, 11	The specification of the ’252 Patent provides that “the host-facing transmitter and receiver set 210 employ fixed equalization parameters that are cable-independent, i.e., they are not customized on a cable-by-cable basis.” The ’252 does not otherwise provide any detail regarding the “cable-independent equalization

Term	Relevant Claim(s)	Basis
		parameters" nor does it provide any examples of such parameters. Accordingly the '252 Patent does not contain sufficient written description to allow a person of ordinary skill in the art to recognize that the inventors were in possession of the claimed invention nor does it enable a person of ordinary skill in the art to make and use the invention without undue experimentation.
"wherein cable dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters"	7–10	The '252 Patent does disclose and does not provide sufficient information to allow a POSITA to make and use a device wherein both "cable dependent equalization parameters" and "fixed, cable-independent, equalization parameters" are employed for the same process. The '252 Patent does not disclose a device wherein both "cable dependent equalization parameters" and "fixed, cable-independent, equalization parameters." The disclosures in the d'252 Patent are thus insufficient to allow a POSITA to recognize that the inventors were in possession of the claimed invention.
"have a per-lane symbol rate in excess of 50 GBd."	5, 10	The '252 Patent does not disclose and does not provide sufficient information to allow a POSITA to make and use a device with "per-lane symbol rate in excess of 50 GBd." The specification discusses only "26.5625 GBd" per lane.

Term	Relevant Claim(s)	Basis
		The ’252 Patent does not disclose a per-lane symbol rate in excess of 50 GBd, and only describes 26.5625 GBd. This disclosure is insufficient to allow a POSITA to recognize that the inventors were in possession of the claimed invention.

Indefiniteness

Certain of the Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the Asserted Claims are indefinite in whole, in part or in combination:

Term	Relevant Claim(s)	Basis
“fixed, cable-independent, equalization parameters”	1, 6, 11	The specification of the ’252 Patent provides that “the host-facing transmitter and receiver set 210 employ fixed equalization parameters that are cable-independent, i.e., they are not customized on a cable-by-cable basis.” The ’252 does not otherwise provide any detail regarding the “cable-independent equalization parameters” nor does it provide any examples of such parameters. Accordingly the ’252 Patent fails to inform, with reasonable certainty, a person of ordinary skill in the art of the scope of the invention.

Term	Relevant Claim(s)	Basis
"re-modulating the first inbound data stream," "re-modulating the second inbound data stream," "re-modulating the first transit data stream," "re-modulating the second transit data stream"	6, 7	The claims, read in light of the specification and prosecution history, fail to inform, with reasonable certainty, what the term "re-modulating" means. The term "re-modulating" is used in the specification in multiple contexts. For example, the specification states that "receiver 400 receives an analog electrical signal (CH_IN) and supplies it to an optional low noise amplifier." *See* 252 Patent at 6:62-63. The Specification continues to state that, after passing through a CTLE and FFE, a "decision feedback equalizer (DFE) 404 operates on the filtered signal to correct for trailing ISI an detect each transmitted channel bit or symbol, thereby producing a demodulated digital data stream." *See* 252 Patent at 7:3-7. Thereafter, the specification further states that the "symbols or data blocks are placed on the digital receive bus (RXD) for remodulation and transmission by a transmitter to the remote end of the channel." 252 Patent at 7:14-16. In other contexts, however, the 252 Patent discusses modulation with respect to the type of modulation scheme employed (e.g., PAM4 or NRZ). *See* 252 Patent at 8:38-56. The 252 Patent specifically contemplates that the "[t]hough not explicitly shown here, the host-facing transmitter and receiver sets 910 may include "gearbox" functions that convert 1 lane of PAM4 symbols into 2

Term	Relevant Claim(s)	Basis
		lanes of NRZ symbols, and vice versa." 252 Patent at 8:64-67. Given the inconsistent use of the term in the specification and the lack of guidance in the claims, the claims of the 252 patent are indefinite, as they fail to provide reasonable certainty as to the meaning of the term "re-modulating."
"3. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters adapt during usage of the Ethernet cable."	3	Claim 3 is an apparatus claim that is directed to "The active Ethernet cable of claim 2." The additional limitations of this claim, however, require the steps of "said cable-dependent equalization parameters *adapt during usage* of the Ethernet cable." The inclusion of this step within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
"4. The active Ethernet cable of claim 2, wherein said cable-dependent equalization parameters are fixed during normal usage of the Ethernet cable, and wherein said cable-dependent equalization parameters are determined during manufacturing-testing of the Ethernet cable."	4	Claim 4 is an apparatus claim that is directed to "The active Ethernet cable of claim 2." The additional limitations of this claim, however, require the additional steps of "said cable-dependent equalization parameters are fixed during normal usage" and that the "cable-dependent equalization parameters [be] determined during manufacturing-testing." The inclusion of these steps within an apparatus claim renders the claim indefinite as it does not

Term	Relevant Claim(s)	Basis
		provide a POSITA with reasonable certainty as to when infringement would occur. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005).
"wherein cable dependent equalization parameters are employed for at least one of: re-modulating the first inbound data stream, re-modulating the second inbound data stream, said performing clock and data recovery on the first electrical transit signal, and said performing clock and data recovery on the second electrical input signal, each employ fixed, cable-independent, equalization parameters"	7–10	The claims, read in light of the specification and prosecution history, fail to inform, with reasonable certainty, how the cables can simultaneously use, for the same process, both cable dependent equalization parameters and cable-independent equalization parameters.
"each of the first and second connectors being adapted to fit into an Ethernet port of a corresponding host device"	1–5	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty as to what an "Ethernet port" is.
"a respective transceiver that performs clock and data recovery . conveying a transit data stream" "the respective transceiver for each of the first and second connectors performing clock and data recovery on the respective electrical transit signal to extract and re-modulate the transit data stream as the outbound data stream from the cable" "the respective transceivers each employing"	1	The claim recites structural components in combination with method steps (e.g., "performing clock and data recovery," "conveying a transit data stream," and "employing."). *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005). The inclusion of these steps within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur.
"wherein the respective transceivers each employ cable-dependent equalization parameters for at least	2	The claim recites structural components in combination with method steps (e.g., "employ").

Term	Relevant Claim(s)	Basis
one of: the remodulation of the inbound data stream for transit, and the clock and data recovery performed on the electrical transit signal."		*IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005). The inclusion of these steps within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur.
"wherein the *inbound data stream and the outbound data stream each have* a per-lane symbol rate in excess of 50 GBd."	5	The claim recites structural components in combination with method steps. *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005). The inclusion of these steps within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur.

Inequitable Conduct

Discovery is ongoing regarding the enforceability of the '252 Patent. To date, Complainants have refused to disclose any prior art known to Complainants, those involved in prosecution, or known to the inventors, outside of what is identified in the prosecution history and what was disclosed to it by third parties in litigation.

In view of Complainants' continued obstruction to relevant discovery, Respondents reserve the right to amend or supplement these contentions as discovery progresses including in response to, among other things, information learned in fact and/or expert discovery including identification of additional prior art, Complainants' positions on priority, infringement, claim construction, and/or invalidity, the Court's rulings, including on claim construction, changes in the Respondents'

respective Accused Products, and in the event Complainants are permitted to revise infringement or domestic industry theories.

Improper Inventorship

Complainants have yet to provide discovery concerning each named inventor's participation, involvement, and contribution to the conception and reduction to practice of the alleged invention, including the dates of such participation, involvement, and contribution to the conception and reduction to practice on an element-by-element basis. *See, e.g.*, Respondents' Common Interrogatory No. 27. Respondents reserve their rights to contend, based on further discovery, that the Asserted Claims of the '252 Patent are invalid and/or unenforceable due to misjoinder of one or more inventors, nonjoinder of one or more inventors, or derivation of the claimed inventions from another.

6. THE '111 PATENT

Priority Date

Complainants have yet to satisfy their burden of proving that any of the Asserted Claims of the '111 Patent are entitled to a priority date prior to the filing date of its application, August 27, 2019. Because Complainants have not shown that United States Provisional Patent Application No. 62/723,701 ("'701 Provisional Application") provides written description support for the Asserted Claims, Complainants are not entitled to the priority date of August 28, 2018, the filing date of that application. Additionally, because Complainants have not shown that any of the Asserted Claims of the '111 Patent were conceived or reduced to practice, actually or constructively, prior to the filing date of the '111 Patent, none of the Asserted Claims of the '111 Patent are entitled to a date of invention that is earlier than the filing date, August 27, 2019.

Respondents reserve the right to supplement and amend its Initial Contentions should Complainants subsequently identify alleged support for its claimed priority date.

Subject Matter Eligibility Grounds Under 35 U.S.C. § 101

As shown in Exhibits C-1 through C-12, each of the limitations of the Asserted Claims of the '111 Patent, individually and in combination with the other elements of each claim, were well understood, routine, and conventional in the industry at the time. Exhibits C-1 through C-12 cite a number of prior art references as evidence of the description of the industry at the relevant time and how the various claim elements were well understood, routine, and conventional (alone and in combination). The prior art references referred to are exemplary only.

The information provided in prior art references and cited herein and in Appendices should not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Respondents claim construction disclosures will be provided according to the procedural schedule. Nothing contained in these Initial Contentions should be understood or deemed to be an express or implied admission or contention with respect to the absence of factual disputes relating to patent ineligibility, the absence of a need for construction of any terms in an Asserted Claim, any proper construction of any terms in an Asserted Claim, or alleged infringement of that claim. There is no claim construction issue or factual issue that precludes the Administrative Law Judge finding that the claims of the Asserted Patents are patent-ineligible.

Respondents also reserve the right to rely upon expert testimony as evidence of the description of the industry at the relevant time and how the various claim elements were well understood, routine, and conventional (alone and in combination). Respondents also further

incorporate by reference the discussion below providing the exemplary legal and factual bases supporting its Section § 101 contentions. *See infra* at Section 6.2.2.

Furthermore, to the extent the listed prior art discloses and describes particular products that were publicly known and/or in public use, in addition to each publication itself serving to demonstrate that the Asserted Claims of the ’111 Patent were well understood, routine, and conventional at the time of filing, the various products described in the publications also serve to demonstrate that the Asserted Claims of the ’111 Patent were well understood, routine, and conventional at the time of filing.

Respondents also reserve the right to rely upon foreign counterparts of the references identified in these Initial Contentions, U.S. counterparts of foreign patents and foreign patent applications identified in these Initial Contentions, U.S. and foreign patents and patent applications corresponding to articles and publications identified in these Initial Contentions, issued patents corresponding to published patent applications identified in these Initial Contentions, published patent applications corresponding to issued patents identified in these Initial Contentions, and any systems, products, or prior inventions related to any of the references identified in these Initial Contentions.

As discussed below, the limitations of the Asserted Claims of the ’111 Patent recite cables comprised of generic and conventional hardware components, such as registers, transceivers, pluggable transceiver modules, and chip-to-module communications links, and the components therein are used in their known and expected manner. The transceivers can also comprise software-based functions implemented by firmware stored in the memory and/or the microcontrollers, and the software-based functions are generic and conventional as well (*e.g.*, storing data (e.g., coefficients) to/from memory).

Identification of Asserted Claims That Are Ineligible Under § 101

’111 Patent Claim	Exception to Eligibility	Factual and Legal Basis	Representative Claim[7]
1	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
2	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
3	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
4	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
5	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
6	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
7	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
8	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

7 Claims 8, 11 and 16 are substantially equivalent in scope to claim 1, therefore claim 1 can be used as representative of claims 8, 11, and 16 for purposes of these Contentions. Claims 2–7, 9–10, 12-14, and 17–19 have additional limitations that do nothing to make these claims valid under Section 101 and therefore claim 1 can be used as representative of all Asserted Claims for purposes of these Contentions. *See, e.g., Content Extraction,* 776 F.3d at 1349 (affirming that a specific claim is “representative, because all the claims are ‘substantially similar and linked to the same abstract idea’”). Moreover, as discussed below, each of the Asserted Claims of the ’111 Patent fails to satisfy Section 101 irrespective of whether claim 1 is representative.

9	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
10	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
11	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
12	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
13	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
14	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
15	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
16	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
17	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
18	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1
19	Abstract Idea	Respondents incorporate by reference the below discussion concerning 35 U.S.C. § 101.	1

Factual and Legal Basis for Subject Matter Ineligibility

***Alice* Step One: The Asserted Claims Are Directed to The Abstract Idea of Transferring and Converting Data**

Representative Independent Claim 1

Representative claim 1 of the'111 Patent recites as follows:

1. A SerDes communications method that comprises, in a transceiver:

[c] selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model;

[c] updating the initial pre-equalizer coefficient values during a training phase; and

[c] using the updated pre-equalizer coefficient values to convey a transmit data stream.

'111 Patent, claim 1.

The plain language of claim 1 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of retrieving data from a register, updating data during a training phase, and using the updated data. Claim 1 does not specify any non-conventional ways of retrieving data, updating data, using the data, or conveying data. In addition, claim 1 does not provide any new algorithms or methods or techniques for accomplishing these tasks. In effect, claim 1 claims a computer-implemented method of converting and conveying data, and the Federal Circuit has "consistently held that similar claims reciting the collection, transfer, and publishing of data are directed to an abstract idea." *Cellspin Soft, Inc. v. Fitbit, Inc.*, 927 F.3d 1306, 1315 (Fed. Cir. 2019) (citing *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016); *In re TLI Commc'ns. Patent Litig.*, 823 F.3d 607, 610–12 (Fed. Cir. 2016)). *See also Adaptive Streaming Inc. v. Netflix, Inc.*, 836 F.App'x 900, 903 (Fed. Cir. 2020) ("We have held that the ideas of encoding and decoding image data and of converting formats, including when data is received

from one medium and sent along through another, are by themselves abstract ideas, and accordingly conclude that claims focused on those general ideas governing basic communication practices, not on any more specific purported advance in implementation ,were directed to abstract ideas."); *Interval Licensing LLC v. AOL, Inc.*, 896 F.3d 1335, 1344 (Fed. Cir. 2019) ("We have recognized that 'information as such is an intangible' and that collecting, analyzing, and displaying that information, without more, is an abstract idea") (cleaned up).

Claim 1 appears to require the functional result of "convey[ing]," data, but fails to do so in a non-abstract way as it does not sufficiently describe how to achieve these results in a non-abstract way. *See, e.g.*, *Two-Way Media Ltd. v. Comcast Cable Commc'ns., LLC*, 847 F.3d 1329, 1338–39 (Fed. Cir. 2017) (holding that "claim 1 manipulates data but fails to do so in a non-abstract way," because "[t]he claim requires the functional result of 'converting,' 'routing,' 'controlling,' 'monitoring,' and 'accumulating records,' but does not sufficiently describe how to achieve these results in a non-abstract way."); *RecogniCorp LLC v. Nintendo Co., Ltd.*, 855 F.3d 1322, 1326–27 (Fed. Cir. 2017) ("standard encoding and decoding" is "an abstract concept long utilized to transmit information," and "[a] process that started with data, added an algorithm, and ended with a new form of data was directed to an abstract idea"); *Adaptive Stream Inc. v. Netflix, Inc.*, 836 F.App'x 900, 903 (Fed. Cir. 2020) ("We have held that the ideas of encoding and decoding image data and of converting formats, including when data is received from one medium and sent along through another, are by themselves abstract ideas."); *Entropic Commc'ns., LLC v. DISH Network Corp.*, 767 F.Supp.3d 1043, 1058 (C.D. Cal. 2025) ("Sending and receiving data, even in the context of a communication network, is abstract."). Claim 1 is only directed to the aspirational end-result that, somehow, conversion and pre-equalization occurs. *See also TriDim Innovations LLC v. Amazon.com, Inc.*, 207 F.Supp.3d 1073, 1080 (N.D. Cal. 2016) ("Much like the

unpatentable subject matter in TLI Communications, the claims in question here are defined only in terms of their functions . .") (citing *In re TLI*, 823 F.3d at 613); *Affinity Labs of Tex., LLC v. Amazon.com, Inc.*, 838 F.3d 1266, 1269–70 (Fed. Cir. 2016) ("The purely functional nature of the claim confirms that it is directed to an abstract idea . ."); *Elec. Power Grp.*, 830 F.3d at 1354 (ineligible claims provided no "particular . inventive technology for performing those functions").

Hardware for performing data retrieval, updating, and use was generic at least as of the '111 Patent's August 28, 2018 filing date, *see, e.g.*, C-1 – C-12, and no specific type of data retrieval and use hardware are recited in these elements. These elements are abstract because they describe a generic devices (a transceiver) configured to perform an abstract process (data retrieval and use) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations recited therein that improve technology or solve a technical problem in a novel way. As of the August 28, 2018 filing date of the '111 Patent, active cables were in common usage. *See, e.g.*, C-1 – C-12.

Although Respondents believe that independent claim 1 of the '111 Patent is representative of all Asserted Claims of the '111 patent (all asserted claims recite the same abstract idea with immaterial and conventional variations), out of an abundance of caution, Respondents will discuss the remaining asserted independent and dependent claims here.

Dependent Claim 2

Dependent claim 2 of the '111 Patent recites as follows:

> 2. The method of claim 1, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.

'111 Patent, claim 2.

The additional limitations recited in dependent claim 2 merely add the requirement that the channel models are for C2M channels with different insertion loss and package loss characteristics. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 2 only recites abstract ideas, as the additional limitations of claim 2 are neither in isolation nor combined render claim 2 patent eligible.

Dependent Claim 3

Dependent claim 3 of the ’111 Patent recites as follows:

> 3. The method of claim 1, wherein at least some of the different channel models presume different types of receiver equalization.

’111 Patent, claim 3.

The additional limitations recited in dependent claim 3 merely add the requirement that at least some of the different channel models presume different types of receiver equalization. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 3 only recites abstract ideas, as the additional limitations of claim 3 are neither in isolation nor combined render claim 3 patent eligible.

Dependent Claim 4

Dependent claim 4 of the ’111 Patent recites as follows:

> 4. The method of claim 1, wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.

’111 Patent, claim 4.

The additional limitations recited in dependent claim 4 merely adds the requirement that selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 4 only recites abstract ideas, as the additional limitations of claim 4 are neither in isolation nor combined render claim 4 patent eligible.

Dependent Claim 5

Dependent claim 5 of the ’111 Patent recites as follows:

5. The method of claim 4, wherein the performance characteristic is an error signal energy. ’111 Patent, claim 5.

The additional limitations recited in dependent claim 5 merely add the requirement that the performance characteristic is an error signal energy. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 5 only recites abstract ideas, as the additional limitations of claim 5 are neither in isolation nor combined render claim 5 patent eligible.

Dependent Claim 6

Dependent claim 6 of the ’111 Patent recites as follows:

The method of claim 4, wherein the performance characteristic is a bit error rate. ’111 Patent, claim 6.

The additional limitations recited in dependent claim 6 merely add the requirement that the performance characteristic is a bit error rate. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 6 only recites abstract ideas, as the additional limitations of claim 6 are neither in isolation nor combined render claim 6 patent eligible.

Dependent Claim 7

Dependent claim 7 of the ’111 Patent recites as follows:

> The method of claim 4, further comprising updating the selected register with the updated pre-equalizer coefficient values.

’111 Patent, claim 7.

The additional limitations recited in dependent claim 7 merely add updating the selected register with the updated pre-equalizer coefficient values. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 7 only recites abstract ideas, as the additional limitations of claim 7 are neither in isolation nor combined render claim 7 patent eligible.

Independent Claim 8

Independent claim 8 recites as follows:

> 8. A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
>
> [c] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and

[c] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,
[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.

'111 Patent, claim 8.

Like claim 1, the plain language of claim 8 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of abstract idea of storing data, retrieving data, and using the data.

Hardware for performing data storage, retrieval, and use was generic at least as of the '111 Patent's August 28, 2018 filing date, *see, e.g.*, C-1 – C-12, and no specific type of data retrieval and use hardware are recited in these elements. These elements are abstract because they describe a generic devices (a transceiver) configured to perform an abstract process (data retrieval and use) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations recited therein that improve technology or solve a technical problem in a novel way. As of the August 28, 2018 filing date of the '111 Patent, active cables were in common usage. *See, e.g.*, C-1 – C-12.

Dependent Claim 9

Dependent claim 9 of the '111 Patent recites as follows:

9. The communications link of claim 8, wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.

'111 Patent, claim 9.

The additional limitations recited in dependent claim 9 merely add the requirement that the channel models are for C2M channels with different insertion loss and package loss characteristics. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date

of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 9 only recites abstract ideas, as the additional limitations of claim 9 are neither in isolation nor combined render claim 9 patent eligible.

Dependent Claim 10

Dependent claim 10 of the ’111 Patent recites as follows:

> 10. The communications link of claim 8, wherein at least some of the different channel models presume different types of receiver equalization.

’111 Patent, claim 10.

The additional limitations recited in dependent claim 10 merely add the requirement that at least some of the different channel models presume different types of receiver equalization. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 10 only recites abstract ideas, as the additional limitations of claim 10 are neither in isolation nor combined render claim 10 patent eligible.

Independent Claim 11

Independent claim 11 recites as follows:

> 11. A chip-to-module communications link that comprises a port connector coupling a port transceiver to a pluggable module transceiver, the pluggable module transceiver including:
>
> [c] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver; and
> [c] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic,
> [c] the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters.

’111 Patent, claim 11.

Like claims 1 and 8, the plain language of claim 11 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of abstract idea of storing data, retrieving data, and using the data.

Hardware for performing data storage, retrieval, and use was generic at least as of the ’111 Patent’s August 28, 2018 filing date, *see, e.g.*, C-1 – C-12, and no specific type of data retrieval and use hardware are recited in these elements. These elements are abstract because they describe a generic devices (a transceiver) configured to perform an abstract process (data retrieval and use) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations recited therein that improve technology or solve a technical problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, active cables were in common usage. *See, e.g.*, C-1 – C-12.

Dependent Claim 12

Dependent claim 12 of the ’111 Patent recites as follows:

> 12. The communications link of claim 11, wherein the performance characteristic is an error signal energy.

’111 Patent, claim 12.

The additional limitations recited in dependent claim 12 merely add the requirement that the performance characteristic is an error signal energy. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 12 only recites abstract ideas, as the additional limitations of claim 12 are neither in isolation nor combined render claim 12 patent eligible.

Dependent Claim 13

Dependent claim 13 of the ’111 Patent recites as follows:

> 13. The communications link of claim 11, wherein the performance characteristic is a bit error rate.

’111 Patent, claim 13.

The additional limitations recited in dependent claim 13 merely add the requirement that the performance characteristic is a bit error rate. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 13 only recites abstract ideas, as the additional limitations of claim 13 are neither in isolation nor combined render claim 13 patent eligible.

Dependent Claim 14

Dependent claim 14 of the ’111 Patent recites as follows:

> 14. The communications link of claim 11, wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters.

’111 Patent, claim 14.

The additional limitations recited in dependent claim 14 merely add the requirement that the port transceiver generates updates for the coefficient values of the one or more transmit filters. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 14 only recites abstract ideas, as the additional limitations of claim 14 are neither in isolation nor combined render claim 14 patent eligible.

Dependent Claim 15

Dependent claim 15 of the ’111 Patent recites as follows:

15. The communications link of claim 14, wherein the controller saves updated coefficient values in one of the registers.

’111 Patent, claim 15.

The additional limitations recited in dependent claim 15 merely add the requirement that the controller saves updated coefficient values in one of the registers. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional and well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 15 only recites abstract ideas, as the additional limitations of claim 15 are neither in isolation nor combined render claim 15 patent eligible.

Independent Claim 16

Independent claim 16 of the ’111 Patent recites as follows:

16. A pluggable module transceiver including:

[c] one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to a port transceiver; and
[c] a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model,
[c] the controller using one of the registers to set initial coefficient values for the one or more transmit filters.

’111 Patent, claim 16.

Like claims 1, 8, and 11, the plain language of claim 16 establishes that it is directed to a patent-ineligible concept, namely the abstract idea of abstract idea of storing data, retrieving data, and using the data.

Hardware for performing data storage, retrieval, and use was generic at least as of the '111 Patent's August 28, 2018 filing date, *see, e.g.*, C-1 – C-12, and no specific type of data retrieval and use hardware are recited in these elements. These elements are abstract because they describe a generic devices (a transceiver) configured to perform an abstract process (data retrieval and use) without specifying sufficiently concrete or inventive technological improvements; and there are no specific, non-generic components or configurations recited therein that improve technology or solve a technical problem in a novel way. As of the August 28, 2018 filing date of the '111 Patent, active cables were in common usage. *See, e.g.*, C-1 – C-12.

Dependent Claim 17

Dependent claim 17 of the '111 Patent recites as follows:

> 17. The pluggable module transceiver of claim 16, wherein the port transceiver determines a performance characteristic for each register.

'111 Patent, claim 17.

The additional limitations recited in dependent claim 17 merely add the requirement that the port transceiver determine a performance characteristic for each register. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the '111 Patent, these were conventional well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 17 only recites abstract ideas, as the additional limitations of claim 17 are neither in isolation nor combined render claim 17 patent eligible.

Dependent Claim 18

Dependent claim 18 of the '111 Patent recites as follows:

> 18. The pluggable module transceiver of claim 17, wherein the performance characteristic is an error signal energy.

’111 Patent, claim 18.

The additional limitations recited in dependent claim 18 merely add the requirement that the performance characteristic is an error signal energy. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 18 only recites abstract ideas, as the additional limitations of claim 18 are neither in isolation nor combined render claim 18 patent eligible.

Dependent Claim 19

Dependent claim 19 of the ’111 Patent recites as follows:

> 19. The pluggable module transceiver of claim 17, wherein the performance characteristic is a bit error rate.

’111 Patent, claim 19.

The additional limitations recited in dependent claim 19 merely add the requirement that the performance characteristic is a bit error rate. These elements do not disclose any improved function of a computer or other technology, nor do they solve a specific technological problem in a novel way. As of the August 28, 2018 filing date of the ’111 Patent, these were conventional well-known techniques. *See, e.g.*, C-1 – C-12. In sum, claim 19 only recites abstract ideas, as the additional limitations of claim 19 are neither in isolation nor combined render claim 19 patent eligible.

Alice Step Two: The Asserted Claims Contain No “Inventive Concept” Sufficient to Render Them Patent Eligible

As noted above, the second step of a Section 101 analysis under *Alice* requires the consideration of each claim element “both individually and ‘as an ordered combination’ to

determine" whether there are additional elements present in the claim that 'transform the nature of the claim' into a patent-eligible application." *Alice*, 573 U.S. at 217 (quotation omitted).

The Asserted Claims of the '111 Patent merely invoke well-understood, routine, and conventional software methods and techniques to achieve the multiple abstract ideas interspersed throughout the Asserted Claims. The claims are directed to storing data in registers, retrieving the data from the registers, and using the data, which is well-known to one of ordinary skill in the art. *See, e.g.*, C-1 – C-12. As the Federal Circuit has held, "claims are not saved from abstraction merely because they recite components more specific than a generic computer." *BSG Tech LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1286 (Fed. Cir. 2018). As discussed in detail in the preceding Section, the Asserted Claims of the '111 Patent lack any of the inventive hallmarks found in other patents found to be patent eligible.

As noted earlier, the Asserted Claims of the '111 Patent provide no technological solution to the purported problems but instead simply disclose the abstract idea of storing, retrieving, and using data, which moreover would have been well-known to one of ordinary skill in the art. As noted at the beginning of this section, the second step of a Section 101 analysis under *Alice* requires the consideration of the claim elements "as an ordered combination" to determine whether there are additional elements present in the claim that "transform the nature of the claim" into a patent-eligible application." *Alice*, 134 S. Ct. at 2347 (quotation omitted). However, the method claims' order of claim elements transfer the claim into patent-eligible material. The order of the claim elements does not disclose any software and/or hardware technological advancement.

All of the Asserted Claims Are Substantially Similar—Represented by Claim 1—for Purposes of Section 101 Analysis

All the Asserted Claims of the ’111 Patent are directed to patent-ineligible abstract ideas. Where claims are “substantially similar and linked to the same abstract idea,” courts may look to representative claims in a Section 101 analysis. *Content Extraction and Trans. v. Wells Fargo Bank,* 776 F.3d 1343, 1349 (Fed. Cir. 2014). Here, claim 1 of the ’111 Patent is representative of all Asserted Claims of the ’111 Patent, as the remaining claims recite the same abstract idea with immaterial and conventional variations.

Asserted independent claims 1, 8, 11, and 16 recite nearly the same subject matter with only minor variations for purposes of Section 101 analysis. As discussed above, claim 1 is directed to the abstract idea of retrieving, updating, and using data. Claims 8, 11, and 16 recite the same subject matter written as apparatus claims.

The asserted dependent claims add additional limitations, but those additional limitations do not impart patent eligibility. Instead, the dependent claims add further variations on abstract ideas that are not technological advancements. *See, e.g.*, *Universal Secure Registry LLC v. Apple Inc.*, 10 F.4th 1342, 1357 (Fed. Cir. 2021).

As noted previously, dependent claims 2-7, 9-10, 12-15, and 17-19 recite conventional and well-known subject matter, (*see, e.g.*, C-1 – C-12) and do not contain an inventive concept that would suffice to transform the abstract subject matter into an eligible application of the abstract idea.

Notably, there are no specific instructions or limitations in the specification concerning how these claim limitations must be carried out, other than a description of the idea, non-specific examples of how the idea may be carried out, and the instructions to apply it to the conventional

technological environment. *See Alice*, 573 U.S. at 220–21. Thus, as with claim 1, none of the asserted dependent claims provide particular requirements as to how the claimed steps are to be performed, nor do they recite anything other than conventional components that are used in conventional ways.

Accordingly, claim 1 of the ’111 Patent is representative for purposes of the Section 101 analysis, and any differences amongst claims 2–19 are insubstantial with respect to eligibility, as each of the claims in the ’111 Patent are drawn to the same abstract idea of storing, updating, retrieving, and using data using generic components and configurations. *Alice*, 573 U.S. at 225; *see also Content Extraction*, 776 F.3d at 1348.

Invalidity Grounds Under 35 U.S.C. §§ 102 and 103

Respondents attach, as Appendix C to its Initial Contentions, claim charts showing examples of how the cited references anticipate and/or render obvious the Asserted Claims of the ’111 Patent under at least AIA 35 U.S.C. §§ 102 and 103 either expressly or inherently as understood by a person having ordinary skill in the art or based on Complainants’ apparent interpretation of the claims.

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
C-1	U.S. Patent No. 10,148,414 (“Lugthart ’414”)	October 19, 2017 (Published)	June 30, 2017
C-2	U.S. Patent Publication No. 2017/0302431 (Lugthart ’431)	Oct. 19, 2017 (Published)	Apr. 21, 2014
C-3	U.S. Patent No. 11,032,111 (Ran)	July 14, 2020 (Published)	Aug. 24, 2018
C-4	U.S. Patent Publication No. 2010/0158538 (Mazzini)	June 24, 2019 (Published)	Dec. 19, 2008
C-5	U.S. Patent Publication No. 2013/0073749 (Tremblay)	Mar. 21, 2013 (Published)	Feb. 22, 2011
C-6	U.S. Patent No. 6,466,626 (Cecchi)	Oct. 15, 2002 (Published)	Feb. 23, 1999
C-7, C-12	U.S. Patent No. 9,768,985 (Ciacci)	Sept. 19, 2017 (Published)	Jan. 1, 2016

Ex.	Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
C-8, C-12	U.S. Patent Publication No. 2003/0058959 (Rafie)	March 27, 2003 (Published)	Sept. 25, 2001
C-9	Amphenol SMP9 Active Electric Cable Product (SMP9 Cable)	N/A	N/A
C-10	Stratix V Product (Stratix)	Published no later than November 2012 and 2016	N/A
C-11	High Speed Serdes Devices and Applications (Stauffer)	Published no later than 2008	N/A
C-12	U.S. Patent No. 11,095,271 (Kang)	Dec. 12, 2019 (Published)	Dec. 19, 2018
C-12	InfiniBandTM Architecture Specification Volume 2 Release 1.4 (Infiniband)	Nov. 16, 2016 (Published)	N/A
C-12	U.S. Patent No. 8,516,238 (Cornelius)	Jan. 5, 2012 (Published)	June 30, 2011
C-12	U.S. Patent Publication No. 2005/0232336 (Balakrishnan)	Oct. 20, 2005 (Published)	Apr. 19, 2005
C-12	WIPO Patent No. 13155160 (Fox)	Oct. 17, 2013 (Published)	Apr. 10, 2013
C-12	U.S. Patent Publication No. 2014/0281067 (Das Sharma)	Sept. 18, 2014 (Published)	Mar. 15, 2013
C-12	U.S. Patent No. 7,239,665 (Mezer)	May 26, 2005 (Published)	Nov. 24, 2003
C-12	PCI Express Base Specification Revision 3.1a (PCIe 3,1a)	Nov. 7, 2015 (Published)	N/A
C-12	Texas Instruments – DS125DF410 Low-Power Multi-Rate Quad Channel Retimer (TI DS125DF410)	Published no later than February 2018	N/A
C-12	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (TI DS110DF111)	Published no later than June 2015	N/A

The attached claim charts identify specific examples of disclosures that teach or suggest a given claim limitation. These identifications should be understood to be exemplary; the charts do not necessarily indicate every location within a particular prior art reference where a claim

limitation may be disclosed or suggested. Respondents and their expert witnesses may rely on other portions of the prior art.

To the extent Complainants contend that any reference identified above does not anticipate the Asserted Claims, it would have been obvious over that primary reference alone or to combine or modify the primary references with concepts from other prior art, such as the other references identified and as explained herein and in Exhibits C-01 – C-12.

In particular, for each limitation of the Asserted Claims that Complainants contend is not met by a particular reference, Respondents contend that the limitation (and claim as a whole) is obvious based on a combination of that particular reference with (1) any other reference disclosing the limitation, (2) any admitted prior art, as explained in the background of each patent or discussed in the file history, (3) any other reference identified in Exhibits C-01 – C-12, as disclosing that limitation, and/or (4) the knowledge of a person of ordinary skill in the art and/or any of the references and concepts discussed herein regarding the relevant background and state of the art. Respondents' obviousness grounds for each dependent claim incorporate the obviousness grounds for the claims from which the dependent claim depends in addition to any obviousness grounds identified in the charts for the dependent claim. To the extent that individual Exhibits C-01 – C-12 include specific combination of prior art, Respondents' contentions are not limited only to those particular combinations, as such combinations are merely exemplary and are meant to be inclusive of the combinations expressed herein and in the other Appendices to these contentions.

The suggested obviousness combinations discussed herein are not to be construed to suggest that any reference included in the combinations is not anticipatory. Further, to the extent that Complainants contend that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, Defendants reserve the right to identify other prior art

references that, when combined with the anticipatory prior art, would render the claims obvious despite an allegedly missing limitation. Defendants will further specify the motivations to combine the prior art, including through reliance on expert testimony, at the appropriate later stage of this Investigation.

In addition to the combinations of Exhibits C-01 – C-12, at least the following exemplary combinations would have been obvious to a POSITA:

- Lugthart ’414, Das Sharma, & Mezer
- Lugthart ’431 in view of Tremblay, or Kang, or Ran, or Mazzini, or Infiniband, Cornelius, Fox, Mezer, Balakrishnan, or Das Sharma, or a combination thereof;
- Ran in view of Lugthart ’431, Tremblay, or Kang, or Infiniband, Cornelius, Fox, Mezer , Balakrishnan, or Das Sharma, or a combination thereof;
- Tremblay in view of Kang, or Ran, or Mazzini, or Infiniband, Cornelius, Fox, Mezer , Balakrishnan, or Das Sharma, or a combination thereof;
- Mazzini in view of Kang, or Tremblay, Ran, or a combination thereof;
- Cecchi in view of Tremblay, or Kang, or Ran, or Mazzini, or Infiniband, or a combination thereof;
- Stratix V Product in view of Lugthart ’414, Das Sharma, Mezer, or a combination thereof;
- Stauffer in view of Lugthart ’414, Das Sharma, Mezer, or a combination thereof;
- Rafie in view of Lugthart ’431/’414, or Tremblay, or Kang, or Infiniband, or Ran, or Cecchi, or Mazzini, or Tremblay, or Cornelius, or Fox, or Mezer, or Balakrishnan, or Das Sharma, or Ciacci, or a combination thereof;

- Ciacci in view of Lugthart ’431/’414, or Tremblay, or Kang, or Infiniband, or Ran, or Cecchi, or Mazzini, or Tremblay, or Cornelius, or Fox, or Mezer, or Balakrishnan, or Das Sharma, or Rafie, or a combination thereof.

For each specified combination, Respondents rely on the references herein, as well as the knowledge of a person of ordinary skill in the art, including that which will be discussed through expert discovery. Although Respondents provide exemplary disclosures and motivations to combine below, Respondents will present expert opinion in accordance with the procedural schedule. Respondents reserve the right to supplement or modify the anticipation and obviousness grounds in response to, for example, Complainants’ positions regarding the scope and meaning of the Asserted Claims taken in this Investigation, before the PTAB, or during prosecution of pending matters related to the Asserted Patents, claim construction determinations made in this Investigation or other proceedings involving the Asserted Patents, updates or changes to Complainants’ infringement and/or technical domestic industry positions, and materials later obtained during discovery, including from Complainants or in response to any third party subpoenas.

Respondents reserve the right to rely on the prior art references identified in connection with any of the other Asserted Patents in connection with the ’111 Patent. In addition, Respondents hereby cite the following additional references as being relevant to the subject matter claimed in the ’111 Patent. Respondents are producing concurrently herewith a number of such references that are relevant to the validity of the Asserted Patents, the state of the art, and as evidencing a motivation to combine various references. Respondents reserve the right to rely on one or more of the references produced concurrently herewith as anticipatory references under 35 U.S.C. § 102, as further evidence of obviousness under 35 U.S.C. § 103 (including as evidence of motivation to

combine or reasonable expectation of success), as background references demonstrating the state of the art, as a limitation upon the doctrine of equivalents, or for any other purpose. Based on further investigation and discovery, based on positions that Complainants may take regarding the scope of the Asserted Claims, and/or based on the Court's claim construction (once issued), Respondents reserve the right to revise these contentions and to rely on these references to prove the invalidity of the '111 Patent in a manner consistent with this ALJ's Ground Rules.

- United States Patent No. 5,854,921
- United States Patent No. 6,680,681
- United States Patent No. 7,308,058
- United States Patent No. 7,664,171
- United States Patent No. 8,477,835
- United States Patent No. 8,787,430
- United States Patent No. 9,088,336
- United States Patent No. 9,118,512
- United States Patent No. 9,137,063
- United States Patent No. 9,152,257
- United States Patent No. 9,495,245
- United States Patent No. 9,754,605
- United States Patent No. 9,806,812
- United States Patent No. 10,736,201
- United States Patent Publication No. 2010/0232493
- United States Patent Publication No. 2013/0223506
- United States Patent Publication No. 2015/0189092
- PCT Publication No. 2016/203205

- Optical Internetworking Forum, "OIF Next Generation Interconnect Framework," OIF-FD-Client-400G/1T-01.0 (2013)
- Optical Internetworking Forum Implementation Agreement, "Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps,25G+ bps I/O and 56G+ bps," OIF-CEI-04.0 (Dec. 29, 2017)
- Insertion loss, package, loss, dissipation, Oxford – A Dictionary of Electronics and Electrical Engineering (5th ed. 2018)
- Insertion loss, Newton's Telecom Dictionary (31st ed. 2018)
- IEEE Std. 802.3bs-2017 "IEEE Standard for Ethernet: Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation" (2017)
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section One
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Two
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Three
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Four
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Five
- IEEE Standard for Ethernet, IEEE 802.3 (2015) Section Six

Level of Ordinary Skill in the Art

To assess the level of ordinary skill of a POSITA, the following factors can be considered: (i) the type of problems encountered in the art; (ii) the prior solutions to those problems; (iii) the rapidity at which innovations are made; (iv) the sophistication of the technology; and (v) the level of education of active workers in the relevant field.

Based on the foregoing, Respondents contend that a POSITA for the '111 Patent as of August 27, 2019 (as well as August 28, 2019) would have had a Bachelor of Science in electrical or computer engineering with at least three years of experience in high-speed digital communication systems. A higher level of education may substitute for less experience.

Obviousness and Motivation to Combine

Motivations to combine with a reasonable expectation of success, as well as the general state of the art, may be found in a variety of places including in the references defined above, and the specification of the ’111 Patent. For example, each piece of prior art relates to the design and/or structure and/or function of active cable devices. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine any one piece of identified prior art with any other identified piece of prior art with a reasonable expectation of success. For at least this reason, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein so as to practice the Asserted Claims and there was a motivation in the art to make such a combination with a reasonable expectation of success.

Motivations to combine various prior art references with a reasonable expectation of success are present in the references themselves, the common knowledge of one of ordinary skill in the art, the prior art as a whole, or the nature of the problems allegedly addressed by the ’111 Patent. Further reasons to combine the references identified in these charts with a reasonable expectation of success include the nature of the problem being solved, the express, implied, and/or inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed towards methods and systems for the design and/or structure and/or function of active cable devices that such combinations would have yielded predictable results, and the fact that such combinations would have represented known alternatives to a person of ordinary skill in the art.

In *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, “[t]he combination of familiar elements according to known methods is likely

to be obvious when it does no more than yield predictable results." 550 U.S. 398, 416 (2007); *see also id.* at 401 ("[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions."). In particular, a patent is obvious where "the content of the prior art, the scope of the patent claim, and the level of ordinary skill are not in material dispute, and the obviousness of the claim is apparent in light of these factors." *Id.* at 427. The Supreme Court explained that "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill." *Id.* at 401.

Moreover, the Supreme Court recognized that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. *Id*. at 402 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp."). When a person of ordinary skill uses an identified, predictable solution to solve a problem, "it is likely the product not of innovation but of ordinary skill and common sense." *Id*. at 402-03.

In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id*. at 417. If a person of ordinary skill can implement a predictable variation, § 103 bars its patentability. *Id*. The rationale to combine or modify prior art references is significantly stronger when references seek to solve similar problems, come from the same field, and correspond well with one another. *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023).

The references share commonalities in terms of their general subject matter as well as the types of equipment, products, systems, and/or methods used. Further, the prior art references explicitly or implicitly reference other prior art references, share common authors or inventors, were published in the same journals, were compiled by a common author of a compilation or reference book, were presented at the same conferences, and/or were developed at common companies, schools, or organizations which would motivate one of skill in the art to combine them. Additionally, the references, and any products, devices, or processes described in the references, existed and/or were invented in the same time period providing further motivation for combination with a reasonable expectation of success.

These disclosures are provided without prejudice to any arguments or objections concerning the relevance of motivation to combine in connection with any invalidity contentions. Respondents reserve the right to further specify the motivations to combine the prior art in response to positions that Complainants may take later in this Investigation and as discovery proceeds. Respondents may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. Moreover, Respondents reserve the right to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the ’111 Patent.

One or more combinations of the prior art references identified in Exhibits C-1 through C-12 would have been obvious because these references would have been combined with a reasonable expectation of success using a simple substitution of one known, equivalent element for another to obtain predictable results and/or a teaching, suggestion, or motivation in the prior

art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Exhibits C-1 through C-12 would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

All of the Asserted Claims are directed to the use of registers storing equalization coefficients. Such technology was widely known before the alleged priority date of the '111 Patent, as evidenced by the references in Exhibits C-1 through C-12. *See, e.g.*, Exs. C-1 (Lugthart '414); C-2 (Lugthart '431); C-3 (Ran); C-4 (Mazzini); C-5 (Tremblay); C-6 (Cecchi); C-7 (Ciacci); C-8 (Rafie); C-9 (SMP9 Cable); C-10 (Stratix); C-11 (Stauffer); C-12 (Secondary References).

The prior art references provide motivations to combine with a reasonable expectation of success because they describe the field of the Asserted Patents, teach improvements, explain desired features, and even expressly state that one of skill in the art would be able to apply their teachings to related systems or methods.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in an active cable device could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including the structure and timing methodologies and techniques, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the '111 Patent.

Additional motivations to combine specific references are discussed below.

6.1.1.1. Exemplary Motivations to Combine for the ’111 Patent

A person of ordinary skill in the art would have been motivated to combine any of the references described in Exhibits C-01 – C-12, or any reference disclosed above, with a reasonable expectation of success to perform the teachings of using a controller to adjust registers containing equalizer coefficients. The ’111 patent recognizes that active cables containing certain data processing functionality were well known in the art prior to the priority date of the ’111 patent. *See* ’111 patent at 1:19-35.

For example, a person of ordinary skill in the art would have been motivated to combine U.S. Patent No. 10,148,414 B1 (“Lugthart ’414”) with U.S. Patent Publication No. 2014/0281067 (“Das Sharma”) and United States Patent No. 7,239,665 (“Mezer”) with a reasonable expectation of success to render obvious claims 1–19 of the ’111 Patent.

U.S. Patent No. Lugthart ’414 was filed on June 30, 2017, was published October 19, 2017, and claims domestic priority to at least U.S. Patent Application No. 14,581,979 filed on December 23, 2014. Lugthart ’414 qualifies as prior art under 35 U.S.C. § 102(a)(1)(AIA) and 35 U.S.C. § 102(a)(2)(AIA).

Lugthart ’414 discloses an “active cable” that “includes… first and second transceiver assemblies 105a, 105b positioned at either end of… conductive lines 111.” *See* Lugthart ’414 at 14:32-37, Fig. 2A (below).

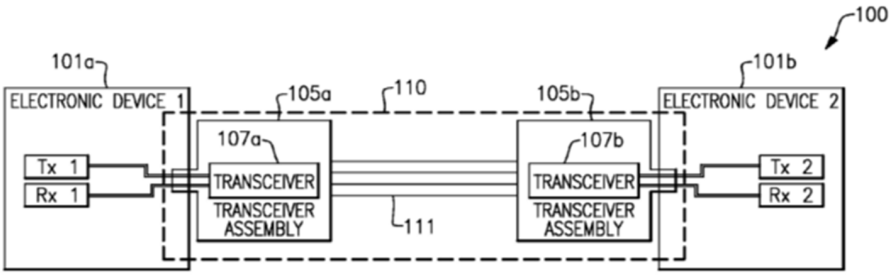
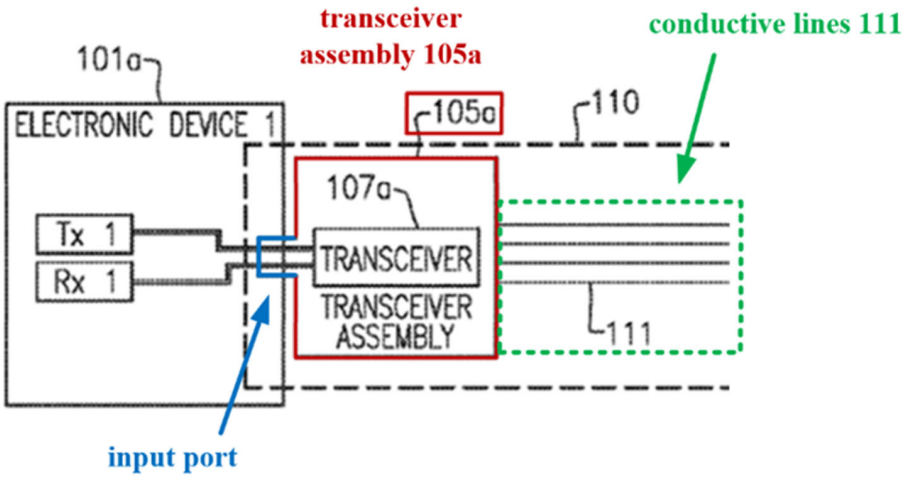


FIG.2A

The electronic components of an active cable improve signal quality. *See, e.g.*, Lugthart '414 at 14:32-34. The transceiver assemblies 105a, 105b include transceivers 107a, 107b, respectively. *See id*. at 14:50-56, Fig. 2A. Each transceiver assembly has a "host side" electrically connected to a host (termed an "electronic device") and a "line side" electrically connected to one end of the cable's conductive lines 111. *See id*. at 14:36-45, Fig. 2A (annotated detail below).



Each transceiver assembly's input port comprises a connector, such as an industry standard SFP or QSFP connector, that "is configured to mechanically and electrically connect, e.g., in a releasable fashion, to a corresponding port or other interface on the respective electronic device 101a, 101b, and an output port that is connected to the cable." *See id*. at 15:49-59, Figs. 2A, 17A, 17B, 18.

The transceivers 107a/107b of Lugthart '414 can perform pre-equalization (which Lugthart '414 calls pre-emphasis) on signals transmitted over the cable's conductive lines 111, as well as on signals transmitted to electronic devices 101a/101b. *See, e.g., id*. at 23:67-24:2, 29:25-30.

Figure 1A's transceiver 10 illustrates one embodiment of Figure 2A's pluggable module transceiver 107a/107b. *See, e.g., id*. at 14:50-56.

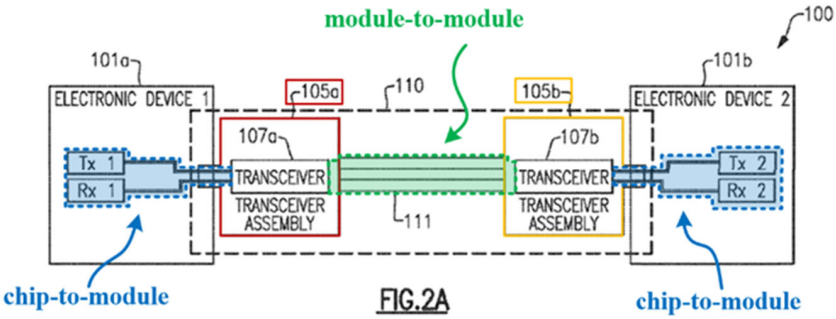


FIG.2A

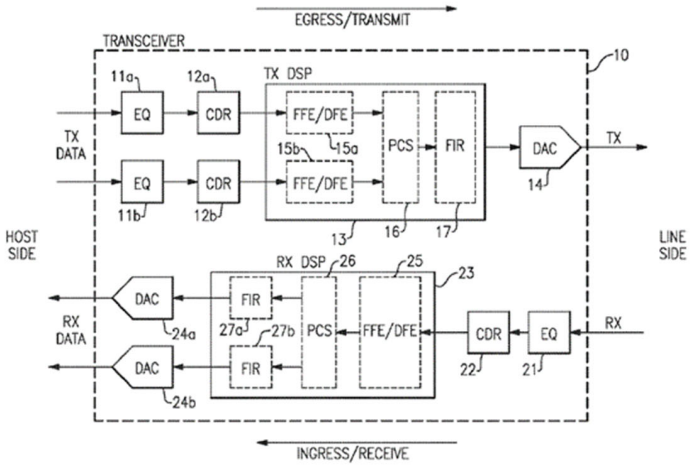


FIG.1A

Transceiver 10's "EGRESS/TRANSMIT" path through DSP 13 performs digital signal processing, including retiming, on the multi-lane TX DATA signal before transmitting the TX signal over conductive lines 111. *See, e.g., id*. at 16:4-10, 21:42-49, Figs. 1A, 2A. The finite impulse response (FIR) filter 17 is a transmit filter that performs pre-emphasis on the re-timed TX signal transmitted over conductive lines 111. *See, e.g., id*. at 16:17-22, 29:25-30.

Lugthart '414 configures FIR filters using "tap coefficients," and the filters "perform emphasis on the signal to compensate for channel losses." *See id*. at 22:19-23, 23:64-24:7. "Pre-emphasis" and "pre-equalization" were used interchangeably in the art. *See, e.g.*, U.S. Patent No. 8,787,430 at 2:39-41 (describing a "technique for combating ISI [inter-symbol interference]… known as 'pre-emphasis', or pre-equalization"); *see also* U.S. Patent No. 9,806,812 at 7:54-55; U.S. Patent No. 9,137,063 at 3:24-27; U.S. Patent No. 9,152,257 at 5:4-8. The purpose of pre-equalization is to compensate for anticipated channel distortion on a transmitted signal.

On the "INGRESS/RECEIVE" path, the DSP 23 performs digital signal processing on signal RX received from the cable before that signal is transmitted to the host (electronic device 101a/101b in Figure 2A). *See, e.g.*, Lugthart '414 at 8:30-36, 9:42-55, Fig. 1A. The DSP 23 includes FIR filters 27a/27b. *See, e.g.*, *id*. at 9:42-50. The DSP 23 uses these FIR filters for "adaptive and configurable signal conditioning features such as… output pre-emphasis" on the signal transmitted to the host. *See, e.g.*, *id*. at 9:56-59, 29:25-30. In one exemplary embodiment, Lugthart '414 describes a five-tap FIR 17 and 27a/27b. *See, e.g.*, *id*. at 22:19-23.

U.S. Patent Publication No. 2014/0281067 ("Das Sharma") was filed on March 15, 2013, and published on September 18, 2014. Das Sharma qualifies as prior art under at least 35 U.S.C. § 102(a)(1)(AIA) and 35 U.S.C. § 102(a)(2)(AIA).

Das Sharma discloses adaptive pre-equalization to fine-tune pre-equalization coefficients. *See, e.g.*, Das Sharma at [0075], [0080]. Das Sharma stores pre-equalization coefficients in registers on the transmitter side. *See id*. at [0078], [0106]. Das Sharma uses these adaptive pre-equalization techniques for PCI Express applications, a widely practiced SerDes method and one of the protocols that Lugthart '414 explicitly supports. *See id*. at [0038], [0069]; *see also* Lugthart '414 at 16:38-43.

More specifically, Das Sharma describes "a link training and equalization procedure" in which "a set of coefficients" is "applied to [the] transmission logic" of the transceiver. Das Sharma at [0066]. The set of coefficients is "applied to a finite impulse response (FIR) filter" in transmission logic of the transceiver to apply pre-emphasis before signal transmission. Das Sharma at [0079]. Das Sharma explains that "a lower bit error rate may be achieved in a channel of a communications link… when an optimized set of coefficients are applied to" the transceiver's "transmission logic." *See id*. at [0089].

Das Sharma stores "a set of default coefficients located within registers of the transmitter" that "may be applied to the transmission… logic." *See, e.g.*, Das Sharma at [0078], [0106]. Das Sharma refers to each register storing coefficient data as a "coefficient register table." *See id*. at [0078]. During operation, the default coefficients (also referred to as "pre-sets") "are requested from the configuration registers" and applied to the transmitter's pre-emphasis filter. *See id*. at [0086]-[0088], [0136], [0155].

United States Patent No. 7,239,665 ("Mezer") was filed on November 24, 2003, and published on May 26, 2005. Mezer qualifies as prior art under at least 35 U.S.C. § 102(a)(1)(AIA) and 35 U.S.C. § 102(a)(2)(AIA).

Mezer discloses an equalization process that uses "a set of coefficients" that Mezer calls "equalizer characteristic[s]." *See, e.g.*, Mezer at 3:64-4:7, 7:4-15 ("'equalizer characteristic' shall be understood to include a set of coefficients such as a set of filter coefficients"). "[V]arious types of channels may be tested in advance to determine suitable FFE [Feed-Forward Equalizer] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected." *See id.* at 6:53-57; *see also* 3:33-4:42 (describing the process for pre-computing the various sets of

coefficients). An ordinarily skilled artisan would have understood that Mezer teaches that different initial "set[s] of coefficients" can be "pre-computed" for different types of channels and those different sets of coefficients can be "stored in [a] storage unit." *See id.* at 4:4-15.

"Selection of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to virtually any communication channel that has an impulse response that varies with a physical characteristic," including a C2M channel. *See id.* at 6:62-7:3.

Lugthart '414 describes training phases. *See, e.g.*, Lugthart '414 at 47:55-60. During training, signals are transmitted over the communication channel and "parameters" are "adjusted," including "operating parameters for the equalizers." *See, e.g.*, Lugthart '414 at 48:65-49:12. An ordinarily skilled artisan understood that this describes adaptive equalization. While Lugthart '414 is not explicit about which of the equalizers has its parameters "adjusted" during training, an ordinarily skilled artisan understood that Lugthart '414 describes adjusting the equalization parameters for any, or all, of Lugthart '414's equalizers, including FIR filters 27a/27b of RX DSP 23 in Lugthart '414's transceiver assembly that performs pre-equalization on signals transmitted to the host transceiver as discussed *supra* §VI.A. *See, e.g.*, Lugthart '414 at 23:26-28, 23:64-24:2, 48:65-49:12.

To the extent Lugthart '414 is read to not expressly disclose using adaptive pre-equalization to adjust pre-equalization coefficients for FIR filters 27a/27b of RX DSP 23 in Lugthart '414's transceiver assembly, Das Sharma would have motivated an ordinarily skilled artisan to have implemented Lugthart '414 in that manner. Das Sharma teaches adaptive pre-equalization used in the same type of PCI Express protocol that Lugthart '414 describes. *See, e.g.*, Das Sharma at [0038], [0069]; *see also* Lugthart '414 at 16:40-43. Das Sharma stores an initial set of pre-equalization coefficients in registers of the transceiver on the transmitter side (Das Sharma at

[0078], [0106]) and performs an adaptive pre-equalization process that optimizes the pre-equalization coefficients during a training process to "achieve communication… with minimal data loss." *See, e.g.*, Das Sharma at [0075].

Lugthart '414 Figure 2A shows that Lugthart '414 specifically contemplates the using conductive lines 111 to connect transceiver assemblies 107a and 107b. An ordinarily skilled artisan would have known that Lugthart '414's cable assembly 110 in Figure 2A would be assembled during the manufacturing process. As such, the characteristics of the channel formed by conductive lines 111 connecting transceiver assemblies 107a and 107b would be largely determined during the manufacturing process, while surrounding factors such as the interference from other proximate conductors, transceiver electrical noise, or changes in cable electrical conductivity from, e.g., temperature or humidity variations, would perturb the channel characteristics.

An ordinarily skilled artisan knew that storing default pre-equalization parameter values determined during the manufacturing process was convenient and even essential for certain operating environments that made adaptation impractical. Storing default values also improves the cable assembly's boot-up speed as the pre-equalization adjusts incrementally from the default values, e.g., the training sequence, and need only account for deviations incurred during actual cable assembly use. *Id*.

If Lugthart '414 is not understood as describing an adaptive pre-equalization process, then an ordinarily skilled artisan had multiple reasons to modify Lugthart '414 to make Lugthart '414's pre-equalization process adaptive and to store the initial set of pre-equalization coefficients in a set of registers with a reasonable expectation of success.

First, Das Sharma expressly teaches the benefits of using an adaptive pre-equalization process that optimizes the pre-equalization coefficients to the particular channel, thereby achieving

communication "with minimal data loss." *See, e.g.*, Das Sharma at [0075]. An ordinarily skilled artisan understood that an adaptive pre-equalization process, like Das Sharma's, enables optimizing coefficients for the current characteristics of a particular channel, thereby compensating for changes in the operating environment (*e.g.*, temperature) that may alter the channel impairments (*e.g.*, distortion) affecting transmitted signals. United States Patent No. 8,477,835 at 3:51-64 (pre-equalization coefficients "can be adapted periodically during system operation to account for changes in the system environment that may impact performance"). Das Sharma also expressly teaches storing initial pre-equalization coefficients in a set of registers. *See, e.g.*, Das Sharma at [0078], [0106]. An ordinarily skilled artisan would have used Das Sharma's teachings to make Lugthart '414's pre-equalization process adaptive and to store an initial set of pre-equalization coefficients in a set of registers, which are specific memory locations that the processor(s) performing the pre-equalization can access quickly and conveniently.

Second, adaptive pre-equalization's benefits for improving data transmission performance were well-known. *See, e.g.*, Das Sharma at [0075], [0089] (optimizing the initial pre-equalizer coefficients based on channel conditions yields "a lower bit error rate" and thus "increase[d] data transmission performance within [the] communication system[]"); United States Patent No. 9,806,812 at 10:40-11:2; United States Patent No. 8,477,835 at 5:34-39; United States Patent No. 6,680,681 at 2:20-28.

Similarly, on-chip registers were a well-known storage medium that an ordinarily skilled artisan understood were desirable for storing coefficients in a digital signal processor (DSP) because values can be retrieved from registers more quickly than from other types of storage, which may require the specific address locations for access (as opposed to the names typically associated with the registers, to which the software programs can point), thereby increasing the

speed and flexibility of DSP operations. *See, e.g.*, United States Patent No. 9,495,245 at 5:13-22 (registers permit "parallel and… immediate[]" access and allow "data to be accessed, processed, and transferred more efficiently"); United States Patent No. 5,854,921 at 1:41-52, 2:8-34 (operations by a processor on data stored in "registers… within the microprocessor" requires fewer clock cycles than operations on data stored in off-chip memory like DRAM).

An ordinarily skilled artisan would have been motivated to store Mezer's pre-computed sets of coefficients in a coefficient register table as taught by Das Sharma, to reduce the size, cost, and complexity of implementing Mezer's "lookup table." *See, e.g.*, United States Patent No. 6,680,681 at 1:38-41 (the "size, cost and complexity" of storing equalizer coefficients in a "lookup table" in memory may be "unacceptable"), 2:46-49 (addressing these concerns by storing equalizer coefficients in a "register array"); *see also* Mezer at 5:13-18; Das Sharma at [0075], [0078], [0106].

These well-known benefits of an adaptive pre-equalization process and storing coefficients in registers would have motivated an ordinarily skilled artisan to make Lugthart '414's pre-equalization process adaptive and to store an initial set of pre-equalization coefficients in registers with a reasonable expectation of success.

Third, making Lugthart '414's pre-equalization process adaptive and storing an initial set of pre-equalization coefficients in a set of registers meets multiple rationales that are indicative of obviousness. *KSR v. Teleflex*, 550 U.S. 398, 417-421 (2007). This combination is a "mere application of a known technique [adaptive pre-equalization using initial coefficients stored in registers as taught by Das Sharma] to a piece of prior art [Lugthart '414] ready for the improvement" because Lugthart '414's system was ready for the improved error rate reduction achieved by Das Sharma's adaptive pre-equalization. *Id*., 417.

This also combines known elements (Lugthart '414's pluggable module transceiver that performs pre-equalization and Das Sharma's adaptive pre-equalization that uses initial coefficients stored in registers) to perform their same known functions to yield predictable results. *KSR*, 550 U.S. at 417 ("When a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious.") (cleaned up); *see also Intel v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-1381 (Fed. Cir. 2023) ("There is a motivation to combine when a known technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the prior art elements according to their established functions.") (cleaned up); *Intel v. Qualcomm*, 21 F.4th 784, 799–800 (Fed. Cir. 2021) (applying "known-technique" rationale).

An ordinarily skilled artisan would have reasonably expected success in making Lugthart '414's pre-equalization process adaptive and storing an initial set of pre-equalization coefficients in a set of registers as taught by Das Sharma. Adaptive pre-equalization was well-known. *See, e.g.,* Das Sharma at [0081]; *see also* United States Patent No. 7,664,171 at 1:62-2:40. Based on these teachings in the art, an ordinarily skilled artisan understood how to use training signals to perform adaptive pre-equalization and to update an initial set of pre-equalization coefficients. *See, e.g.*, Das Sharma at [0081]; *see also* United States Patent No. 7,664,171 at 1:62-2:40. An ordinarily skilled artisan further knew how to store initial and updated pre-equalization coefficients in registers because Das Sharma taught this (Das Sharma at [0075]-[0078]) and registers were a well-known storage medium for storing data in a digital signal processor like Lugthart '414's RX DSP 23. *See, e.g.*, United States Patent No. 9,495,245 at 5:13-22; United States Patent No. 5,854,921 at 2:8-34.

As another example, claims 1-19 are invalid under 35 U.S.C. § 103 (AIA) over the combination of Lugthart '414 in view of Das Sharma, and in further view of Mezer.

To the extent Lugthart '414 and Das Sharma do not disclose storing different initial pre-equalization coefficient values for different channel models, that was taught by Mezer.

Mezer's equalization process uses "coefficients" that Mezer also calls "equalizer characteristics." *See, e.g.*, Mezer at 3:64-4:7, 7:11-15. Mezer teaches that "various types of channels may be tested in advance to determine suitable FFE [Feed-Forward ***Equalizer***] characteristics therefor, and when it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected." *See, e.g.*, Mezer at 6:53-57; *see also id.* 3:33-4:42 (describing process for pre-computing the various sets of coefficients). An ordinarily skilled artisan understood that a "feed-forward equalizer" was a type of equalizer that, like pre-equalization, improved communication by compensating for channel distortion, and thus the "equalizer characteristics" (coefficients) in Mezer are analogous to coefficients used in an adaptive pre-equalization process. *See, e.g.*, United States Patent No. 8,787,430 at 17:4-14. Thus, Mezer teaches that different initial "set[s] of coefficients" can be "pre-computed" for different channel types and "stored in [a] storage unit." *See, e.g.*, Mezer at 4:4-7.

An ordinarily skilled artisan understood that Mezer's teachings were applicable to the pre-equalization process performed by Lugthart '414 (as modified by Das Sharma in the manner described above). Mezer teaches that "[s]election of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to virtually any communication channel that has an impulse response that varies with a physical characteristic" and is explicit that this includes Ethernet channels. *See, e.g.*, Mezer at 6:62-7:3. An ordinarily skilled artisan understood that Lugthart '414's *chip-to-module communications link* between the pluggable module

transceiver and the host transceiver is a "communication channel that has an impulse response that varies with a physical characteristic" as described by Mezer, because Lugthart '414's C2M link distorts transmitted signals in ways that vary with the physical characteristics of the channel as discussed above.

Mezer's equalizer is on the receiver side of the communication channel rather than the transmitter side as in Lugthart '414 and Das Sharma, so Mezer's equalization is not pre-equalization as in Lugthart '414 and Das Sharma. *See, e.g.*, Mezer at 5:25-28; *see also* Lugthart '414 at 23:26-28, 23:64-02, 48:65-49:19; Das Sharma at [0078], [0081], FIG. 5. However, an ordinarily skilled artisan understood that the below-discussed benefits Mezer describes of storing different initial equalization coefficients for different channel types (improved efficiency and/or using less hardware) apply equally to pre-equalization performed on the transmitter side. *See, e.g.*, Mezer at 5:40-55. Indeed, applying the same type of "lookup table" approach for initial pre-equalizer coefficients on the transmitter side was known. United States Patent No. 9,118,512 at 12:34-55, 13:56-59 ("a measurement of a channel condition… may be used to index a lookup table and obtain… coefficient[s]" for a transmitter-side pre-equalizer); United States Patent No. 10,736,201 at 10:13-52 (initial pre-equalizer coefficients "can be pre-determined and stored in a memory of the driving circuitry," for example "in a look-up table"); United States Patent No. 8,477,835 at 9:67-10:2 ("a simple mapping table, which can be realized through a table-lookup ROM, RAM, or through firmware, can provide the means to set TX equalizer coefficients"); Das Sharma at [0078], [0106].

Thus, an ordinarily skilled artisan understood that Mezer's teachings apply directly to Lugthart '414's pre-equalization process (as modified by Das Sharma as described *above*).

An ordinarily skilled artisan had multiple reasons to modify the above-discussed combination based on Lugthart '414 and Das Sharma to store, in Das Sharma's registers, different pre-computed pre-equalization coefficients for different channel models with a reasonable expectation of success.

First, Mezer expressly teaches the benefits of using different pre-stored pre-computed pre-equalization coefficients for different channel types with different channel characteristics. *See, e.g.*, Mezer at Abstract, 5:40-56. If the adaptive equalizer does not customize the initial coefficients to the channel type, "convergence of the adaptive equalizer may be slower than desirable." *See, e.g.*, Mezer T 1:16-18. Mezer explains that its use of different pre-computed coefficients for different channel types can be used in an adaptive equalization process that uses "conventional principles" like in Lugthart '414 and Das Sharma, but "because of the relatively high degree of equalization provided by the pre-computed FFE block 48, the adaptive FFE 52 may converge more rapidly, and/or may require less hardware (e.g., fewer gates) than would be the case" if initial equalization coefficients were used that were not pre-computed for the specific channel type. *See, e.g.*, Mezer at 5:40-55; *id.*, 2:21-23 (FFE means "feed forward equalizer").

Thus, Mezer expressly teaches that using different sets of stored coefficients for different channel types can advantageously provide a more efficient adaptive training process that "converges more rapidly" to coefficients that yield an acceptable error rate and/or can use less hardware. *See, e.g.*, Mezer at 5:40-55. One exemplary Mezer channel characteristic is the length of a cable used in the channel, because different cable lengths can distort the signal transmitted through the channel differently. *See, e.g.*, Mezer at 3:32-4:22. An ordinarily skilled artisan understood that Mezer's techniques are applicable to other variable channel characteristics, such as different PCB trace lengths between the host transceiver and the pluggable module connector.

See, e.g., Mezer at 6:50-53 ("selection of one of a number of stored pre-computed equalizer characteristics may be performed on the basis of a channel characteristic other than cable length"), 6:62-7:3 (Mezer's techniques "may be performed with respect to virtually any communication channel that has an impulse response that varies with a physical characteristic").

Thus, an ordinarily skilled artisan understood that channel characteristics can vary widely, so that the designers of the chips with SerDes typically characterize multiple different channel models and store the corresponding pre-equalization parameters as potential initial values for the adaptation process. Mezer's express teachings would have motivated an ordinarily skilled artisan to modify Lugthart '414 and Das Sharma to store different pre-computed pre-equalization coefficients for different channel models as initial coefficients for use in the adaptive pre-equalization process used by Lugthart '414 as modified by Das Sharma with a reasonable expectation of success. An ordinarily skilled artisan would have stored the pre-computed initial pre-equalization coefficients in a set of registers in the same way Das Sharma describes for storing initial pre-equalization coefficients. Das Sharma at [0078].

Second, it was well-known that using initial pre-equalization coefficients that accurately estimate the impact of the channel "shorten[s] the training time" for the pre-equalizer, leading to less costly down time for training. *See, e.g.*, Mezer at 5:40-55 (the adaptive training process converges more rapidly); *see also* United States Patent No. 7,664,171 at 10:30-33, 2:33-40 ("if the initial coefficient value of equalizer is estimated accurately enough, the equalizer will nearly enter into the convergence state before training"), 2:33-40 (describing a "pre-loading technique of equalizer coefficient[s], which first writes a group of initial coefficient value pre-calculated (estimated) into the coefficient register of equalizer before the equalizer starts training process"), 10:47-11:7 ("the effect of equalizer coefficient pre-load of the present invention is much better

than the prior art."); United States Patent No. 9,118,512 at 12:34-55, 13:56-59; United States Patent No. 10,736,201 at 10:13-52; United States Patent No. 8,477,835 at 9:67-10:3; Das Sharma at [0078], [0082], [0106]; Mezer at 6:27-42.

It was also well-known that active cable systems like Lugthart '414's could be plugged into different types of electronic devices 101a/101b with different types of communication links between the pluggable module connector and the host transceiver (Lugthart '414 Fig. 2A) and that the C2M link between the pluggable module's transceiver and the host device's transceiver could vary for different electronic devices and distort the signal differently. *See, e.g.*, Lugthart '414 at 6:25-48.

Thus, an ordinarily skilled artisan would have understood that storing different initial equalization coefficients, for different types of electronic devices that might be used with the cable, would increase the likelihood of selecting, for a particular device, initial coefficients that accurately estimated the C2M channel's impact on the signal, thus desirably yielding an efficient training process.

Third, modifying the pluggable module transceiver of Lugthart '414 in view of Das Sharma discussed above to store different initial sets of pre-equalization coefficients for different channel models meets multiple rationales indicative of obviousness. *KSR*, 550 U.S. at 417-421. Modifying the pluggable module transceiver of Lugthart '414 in view of Das Sharma to use different pre-equalization coefficients for different C2M channel models is a "mere application of a known technique [using different initial coefficients for different channel types as taught by Mezer] to a piece of prior art [Lugthart '414 as modified by Das Sharma] ready for the improvement" because the pluggable module transceiver of Lugthart '414 in view of Das Sharma was ready for the

improvement of a more efficient pre-equalization training process that results from having different initial coefficients for different channel types. *Id*., 417.

This combination is also nothing more than combining known elements (Lugthart '414's pluggable module transceiver that performs pre-equalization, Das Sharma's adaptive pre-equalization that uses initial coefficients stored in registers, and Mezer's different initial equalization coefficients for different channel types) to perform their same known functions to yield predictable results. *KSR*, 550 U.S. at 417*; PACT XPP,* 61 F.4th at 1380-81 (discussing known technique improving similar devices in same way).

An ordinarily skilled artisan also would have reasonably expected success in further modifying Lugthart '414 and Das Sharma to store different initial pre-equalization coefficients for different channel types as taught by Mezer. *See, e.g.*, Mezer at Abstract, 5:40-56. Mezer teaches that initial equalization coefficients for different channel types can be computed and stored in advance. *See, e.g.*, Mezer at 3:34-4:22.

At least two techniques were known for how the transceiver of the combination based on Lugthart, Das Sharma, and Mezer would determine which set of initial coefficients to use when the cable is plugged into a new host device.

First, Mezer teaches that the pre-computed equalizer characteristics may be selected based on cable length or "on the basis of a channel characteristic other than cable length." *See, e.g.*, Mezer at 6:27-28, 6:50-57. "Selection of a pre-computed equalizer characteristic based on a channel characteristic may be performed with respect to virtually any communication channel that has an impulse response that varies with a physical characteristic." *See, e.g.*, Mezer at 6:62-7:3. "[W]hen it is determined to which one of the channel types the computer system is coupled, the suitable FFE characteristic for that type of channel may be selected." *See, e.g.*, Mezer at 6:50-57.

Lugthart ’414 teaches a “startup-phase” when its active cable is installed between two electronic devices. *See, e.g.*, Lugthart ’414 at 47:65-48:7, Fig. 2A. In the start-up phase, a “basic channel test may be performed… to determine the channel parameters such as, for example, loss, noise, dispersion, non-linearity, etc.” *See, e.g.*, Lugthart ’414 at 48:20-23. To the extent Lugthart ’414 suggests that this “channel test” tests the channel between the host transceivers in the electronic devices 101a/101b, an ordinarily skilled artisan understood that pluggable module transceivers 107a/107b could have been easily adapted to each perform a channel test for the channel shown in red below between the pluggable module transceiver and its respective host transceiver in the electronic device 101a/101b into which the pluggable module transceiver’s assembly is releasably plugged. This would have been well-within the POSA’s capabilities as it would have simply involved implementing Lugthart ’414’s known “basic channel test” capability in the pluggable module transceiver because Lugthart ’414’s host transceiver already had this “basic channel test” functionality. *See, e.g.*, Lugthart ’414 at 48:20-23.

An ordinarily skilled artisan understood that Lugthart ’414’s “basic channel test” that “determine[s] the channel parameters” like “loss, noise, dispersion, non-linearity, etc.” was a desirable way to select among Mezer’s different sets of initial pre-equalization coefficients for different channel types. *See, e.g.*, Lugthart ’414 at 48:20-23; Mezer at 6:50-7:3. During Das Sharma’s adaptive equalization process, equalization coefficients are adjusted to compensate for these types of “channel parameters” like loss and noise. *See, e.g.*, Das Sharma at [0066], [0075]-[0077], [0087]-[0089]. An ordinarily skilled artisan understood that these same channel parameters used to adapt pre-equalization coefficients to yield suitably low error in the received signal were desirable parameters to use to select an initial set of pre-equalization coefficients that best compensates for the channel’s impact on the signal to make the training process “converge more

rapidly, and/or… require less hardware." *See, e.g.*, Mezer at 5:40-55, 6:27-33, 6:50-57; Das Sharma at [0081] (describing generating new coefficient values during the adaptive equalization process based on a measured bit error rate for the channel).

Second, an alternative way to select from among the sets of pre-computed pre-equalization coefficients in the combination based on Lugthart, Das Sharma, and Mezer was to send a known test signal using each set, determine which set produced a received signal that most closely matched the known test signal, and select the set of coefficients that produced that closest matching signal. *See, e.g.*, Mezer at 6:53-57 (selecting set of coefficients when channel type is determined); Das Sharma at [0081] (iteratively cycling through multiple sets of coefficients during the adaptive equalization process and determining a bit error rate for each one). This was well-within the ordinarily skilled artisan's capabilities. It simply involves the pluggable module transceiver sending a known test signal using each set of coefficients, the port transceiver determining which received test signal most closely matches the known test signal using the same error evaluation techniques known for use in adaptive equalization (Das Sharma at [0081]), selecting the register with the coefficients that yielded the test signal with lowest error, and the pluggable module transceiver using the set of coefficients selected by the port transceiver.

Whether the pluggable module transceiver or the port transceiver selects the register with the best performing coefficients was an ordinarily skilled artisan's design choice, as backchannel communication between the transceivers meant either transceiver could make the selection. *KSR*, 550 U.S. at 421 ("When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp.").

It was well-known to use backchannel communication between transceivers on opposite ends of a communications channel to implement equalization. *E.g.*, United States Patent Publication No. 2004/0071203 at [0070]; IEEE Std. 802.3-2015, "IEEE Standard for Ethernet: Section 5" at 473 (802.3-215, Clause 72, "§72.6.10.2.3 Coefficient update field: The coefficient update field carries correction information from the local receiver to the link partner transmit equalizer."). The receiving host transceiver could use a backchannel communication technique to provide error information on each test signal to the transmitting pluggable module transceiver, which could use that error information to select the register with the coefficients that produced the lowest error. Alternatively, the receiving port transceiver could evaluate the error data and select the register with the coefficients that produced the lowest error and communicate that selection to the pluggable module transceiver using backchannel communication.

Thus, an ordinarily skilled artisan would have had a reasonable expectation of success in implementing Lugthart '414's active cable to perform adaptive pre-equalization, store in Das Sharma's registers different initial pre-equalization coefficients for different channel types as taught by Mezer, and select from among those different coefficients the set best suited to the channel in which the cable is installed because this involved simply using known techniques and was well within an ordinarily skilled artisan's skill.

Similarly, a POSITA would have been motivated to combine Ran in view of either Lugthart '431, or Tremblay, or Kang, or Infiniband, or a combination thereof; Tremblay in view of either Kang, or Ran, or Mazzini, or Infiniband, or a combination thereof; Mazzini in view of either Kang, or Tremblay, Ran, or a combination thereof; or Cecchi in view of Tremblay, or Kang, or Ran, or Mazzini, or Infiniband, or a combination thereof.

To the extent that it is determined that any of these references do not disclose "selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Rafie, Ciacci, Balakrishnan, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such selection of registers to specify pre-equalization coefficient values in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, TI DS125DF410, or TIDS110DF111, each of which teach selecting registers to specify pre-equalization coefficient values. *See, e.g.*, Exhibits C-2–C-6, C-12 (claim 1[a]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Kang, Cornelius, Infiniband, Ran, Balakrishnan, and Cecchi where they disclose the use of multiple registers with equalization coefficients corresponding to different channel models, with the embodiments of at least Lugthart '431, Tremblay, Mazzini, Rafie, Ciacci, Balakrishnan, TI DS125DF410, TIDS110DF111, and/or any combinations therein. *See* Exs. C-3, C-6, C-12. As specific examples, Kang discloses "a plurality of registers," Cornelius discloses configuring "operational parameters, modes, and other aspects," Ran discloses multiple registers for a "Chip-to-Module (C2M) device," and Cecchi discloses different registers that correspond to different length cables with different pre-emphasis coefficients to compensate for various factors, each of which a POSITA would have had reason to implement in at least Lugthart '431, Tremblay, and /or Mazzini. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. Balakrishnan discloses

storing "gain coefficients of the digital pre-equalizer" in a register. Balakrishnan ¶ 27. It was also well-known in the art to store coefficients in registers and that using multiple registers was an option. *See, e.g.*, Exhibits C-3, C-6, C-12 (claim 1[a]). Indeed, using multiple registers with coefficient values is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of selecting from multiple registers corresponding to different channel models would thus require nothing more than the application of a known solution (incorporating multiple registers that correspond to different channel models), according to its established function (selecting between the multiple registers), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "updating the initial pre-equalizer coefficient values during a training phase," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such updating via a training phase in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, TI DS125DF410, or TIDS110DF111, each of which teach updating coefficient values. *See, e.g.*, Exhibits C-2–C-6, C-12 (claim 1[b]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Ran, Mazzini, and Tremblay where they disclose the use of updating via training with the embodiments of at least Lugthart '431, Kang, Cecchi, Infiniband, Cornelius and/or any combinations therein. *See* Exs. C-3 – C-5.

As specific examples, Mazzini describes a training phase with respect to at least Figure 4, Ran discloses a training phase with respect to at least Figures 3A, 3B, and 3D, and Tremblay describes an adaptive process. *Id.* A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that you could use a training phase to update coefficients in the manner considered. *See, e.g.*, *id.* (claim 1[b]). Indeed, using a training phase to update coefficients is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of training would thus require nothing more than the application of a known solution (incorporating a training phase), according to its established function (updating coefficient values), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "using the updated pre-equalizer coefficient values to convey a transmit data stream," (claim 1[c]) a person of ordinary skill in the art would have been motivated to combine any of these references with a reasonable expectation of success for the same reasons discussed related to the prior limitations related to Claim 1 of the '111 patent. A POSITA would have understood that any selection of multiple registers or updating that occurs would ultimately be used to transmit the updated coefficient values to convey a data stream.

To the extent that it is determined that any of these references do not disclose that "the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics," a person of ordinary skill in the art would have been motivated to

combine Lugthart ’431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Balakrishnan, Das Sharma, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models with different insertion loss and package loss characteristics in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart ’431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Balakrishnan, Das Sharma, TI DS125DF410, orTIDS110DF111 each of which teach models with differing channel characteristics. *See, e.g.*, Exhibits C-2–C-6, C-12 (claims 2, 9). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Cecchi, Kang, Cornelius, Balakrishnan, Das Sharma, TI DS125DF410, or TIDS110DF111 where they disclose the varying models having variations in channel characteristics with the embodiments of at least Lugthart ’431, Tremblay, Ran, Mazzini, or Infiniband. *See* Exs. C-6, C-12. As a specific example, Cecchi discloses a plurality of registers with differing characteristics, Balakrishnan discloses frequency shaping, and Das Sharma discloses channel losses. *Id.* A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that variations in channel models would account for variations of insertion loss and package loss characteristics. *See, e.g.*, *id.* (claim 1[a]). Indeed, using different models to account for different characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these different models would thus require nothing more than the application of a known solution (using multiple models), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art

would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "at least some of the different channel models presume different types of receiver equalization," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Ciacci, Rafie, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, or Infiniband, each of which teach models with differing channel characteristics. *See, e.g.*, Exhibits C-2–C-6, C-12 (claims 3, 10). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Cecchi, Kang, Cornelius, and Infiniband where they disclose the varying models having different types of receiver equalization with the embodiments of at least Lugthart '431, Tremblay, Ran, Mazzini, Ciacci, Rafie, TI DS125DF410, or TIDS110DF111. *See* Exs. C-6, C-12. As a specific example, Cecchi discloses different registers that correspond to different length cables with different pre-emphasis coefficients to compensate for various factors. Ex. C-6. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that variations in channel models would account for variations in different types of receiver equalization. *See, e.g.*, Exhibits C-6, C-12 (claims 3, 10). Indeed, using different models to account for different characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization

using these different models would thus require nothing more than the application of a known solution (using multiple models), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Rafie, Ciacci, Fox, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Fox, TI DS125DF410, or TIDS110DF111, each of which teach determining a performance characteristic. *See, e.g.*, Exhibits C-2–C-6, C-12 (claim 4). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Mazzini, Tremblay, Ran, Cecchi, Kang, Cornelius, and Ran where they disclose the varying models having different types of receiver equalization with the embodiments of at least Lugthart '431, Tremblay, Ran, Mazzini, or Infiniband. *See* Exs. C-3–C-5. As specific examples, Mazzini describes a training phase with respect to at least Figure 4, Ran discloses a training phase with respect to at least Figures 3A, 3B, and 3D, and Tremblay describes an adaptive process, each of which includes using initial pre-equalizer coefficients. *See id*. Fox teaches "utilize ongoing CMTS receiver measurements, such as bit error rates, modulation

error rates, and power measurements, to continually recalculate and optimize various CMTS receiver parameters in each channel's profile." Fox at 11:26-31, *see also id.* at 10:6-8. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that the initial pre-equalize coefficients could be used to determine characteristics of registers. *See, e.g.*, *id.* (claim 4). Indeed, using the initial coefficients to determine register characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these initial coefficient values to determine varying register characteristics would thus require nothing more than the application of a known solution (using initial values), according to its established function (measuring different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "the performance characteristic is an error signal energy," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Fox, Mezer, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include a performance characteristic that is an error signal energy in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Fox, Mezer, TI DS125DF410, or TIDS110DF111, each of which teaches the performance characteristic relating to errors. *See, e.g.*, Exhibits C-2–C-6, C-12 (claims 5, 12, 18). For example, a POSITA would have

been motivated to incorporate the embodiments of at least each of Cecchi, Cornelius, Fox, Mezer, TI DS125DF410, or TIDS110DF111, where they disclose the varying models having a performance characteristic that is an error signal energy with the embodiments of at least Lugthart '431, Tremblay, Ran, Mazzini, or Infiniband *See* Exs. C-6, C-12 (claims 5, 12, 18). As a specific example, Cecchi discloses measuring error rate, Cornelius discloses measuring transmission errors, Fox discloses bit error rates, and Mezer discloses error signals. *Id*. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that error signal energy could be used as a performance characteristic. *See, e.g.*, *id.* (claims 5, 12, 18). Indeed, using an error signal energy as a performance characteristics but one of a finite number of known, predictable solutions to measuring performance. Implementing pre-equalization using an error signal energy as a performance characteristic thus requires nothing more than the application of a known solution (using an error signal energy as a performance characteristic), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "a performance characteristic is a bit error rate," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Fox, Mezer, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include a performance characteristic that is a bit error rate in view

of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, Fox, Mezer, TI DS125DF410, or TIDS110DF111, each of which teaches the performance characteristic relating to errors. *See, e.g.*, Exhibits C-2–C-6, C-12 (claims 6, 13, 19). For example, a POSITA would have been motivated to incorporate the embodiments of at least each of Cecchi, Cornelius, Fox, Mezer, TI DS125DF410, and TIDS110DF111 where they disclose the varying models having a performance characteristic that is a bit error rate with the embodiments of at least Lugthart '431, Tremblay, Ran, Mazzini, or Infiniband. *See* Exs. C-6, C-12 (claims 6, 13, 19). As a specific example, Cecchi discloses measuring error rate, Cornelius discloses measuring transmission errors, Fox discloses bit error rates, and Mezer discloses error signals. *Id.* A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that bit error rates could be used as a performance characteristic. *See, e.g.*, *id.* (claims 6, 13, 19). Indeed, using a bit error rate as a performance characteristics but one of a finite number of known, predictable solutions to measuring performance. Implementing pre-equalization using a bit error rate as a performance characteristic thus requires nothing more than the application of a known solution (using a bit error rate as a performance characteristic), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "updating the selected register with the updated pre-equalizer coefficient values," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini,

Cecchi, Infiniband, Cornelius, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, TI DS125DF410, and TIDS110DF111, each of which teach determining a performance characteristic. *See, e.g.*, Exhibits C-2–C-6, C-12 (claims 7, 14, 15). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Mazzini, Tremblay, Ran, Cecchi, Kang, Cornelius, Ran, TI DS125DF410, and TIDS110DF111 where they disclose the varying models updating the selected register with updated pre-equalizer coefficients with the embodiments of at least Lugthart '431, Tremblay, Ran, Mazzini, or Infiniband. *See* Exs. C-3–C-5 (claims 7, 14, 15). As specific examples, Mazzini describes a training phase with respect to at least Figure 4, Ran discloses a training phase with respect to at least Figures 3A, 3B, and 3D, and Tremblay describes an adaptive process, each of which includes using initial pre-equalizer coefficients. *See id.* A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that training would require updating the coefficient values. *See, e.g.*, *id.* (claims 7, 14, 15). Indeed, updating coefficient values is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using this updating would thus require nothing more than the application of a known solution (updating coefficient values), according to its established function (a training sequence), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the

art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such transmit filters to pre-equalize streams being transmitted in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, TI DS125DF410, or TIDS110DF111, each of which teach transmit filters. *See, e.g.*, Exhibits C-2–C-6, C-12 (claims 8[a], 11[a], 16[a]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Kang, Cornelius, Infiniband, Ran, Cecchi, TI DS125DF410, and TIDS110DF111 where they disclose the use of multiple registers with equalization coefficients corresponding to different channel models, with the embodiments of at least Lugthart '431, Tremblay, Mazzini, and/or any combinations therein. *See* Exs. C-6, C-12. As specific examples, Kang discloses "a plurality of registers," Cornelius discloses configuring "operational parameters, modes, and other aspects," Ran discloses multiple registers for a "Chip-to-Module (C2M) device," and Cecchi discloses different registers that correspond to different length cables with different pre-emphasis coefficients to compensate for various factors, each of which a POSITA would have had reason to implement in at least Lugthart '431, Tremblay, and /or Mazzini. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known

in the art to use transmit filters on a data stream. *See, e.g.*, Exhibits C-6, C-12 (claims 8[a], 11[a], 16[a]). Indeed, using a transmit filters on a data stream is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of transmit filters on a data stream would thus require nothing more than the application of a known solution (transmit filters on a data stream), according to its established function (apply the transmit filters), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.," a person of ordinary skill in the art would have been motivated to combine Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, TI DS125DF410, TIDS110DF111, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such multiple registers each of which contain initial coefficient values corresponding to different channel models in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lugthart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, TI DS125DF410, or TIDS110DF111, each of which teach transmit filters. *See, e.g.*, Exhibits C-2–C-6, C-12 (claims 8[b], 11[b], 11[c], 16[b]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Kang, Cornelius, Infiniband, Ran, Cecchi, TI DS125DF410, and TIDS110DF111 where they disclose the use of multiple registers with equalization coefficients corresponding to different channel models, with the

embodiments of at least Lugthart ’431, Tremblay, Mazzini, and/or any combinations therein. *See* Exs. C-6, C-12. As specific examples, Kang discloses “a plurality of registers,” Cornelius discloses configuring “operational parameters, modes, and other aspects,” Ran discloses multiple registers for a “Chip-to-Module (C2M) device,” and Cecchi discloses different registers that correspond to different length cables with different pre-emphasis coefficients to compensate for various factors, each of which a POSITA would have had reason to implement in at least Lugthart ’431, Tremblay, and /or Mazzini. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art to use multiple registers each of which contain initial coefficient values corresponding to different channel models. *See, e.g.*, Exhibits C-6, C-12 (claims 8[b], 11[b], 11[c], 16[b]). Indeed, using multiple registers each of which contain initial coefficient values corresponding to different channel models is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of multiple registers each of which contain initial coefficient values corresponding to different channel models would thus require nothing more than the application of a known solution (multiple registers each of which contain initial coefficient values corresponding to different channel models), according to its established function (selecting on of the multiple registers), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

Similarly, a POSITA would have been motivated to combine the Stratix V Product in view of either Lugthart ’414, Das Sharma, Mezer, or a combination thereof, and Stauffer in view of

Lugthart ’414, Das Sharma, Mezer, or a combination thereof, with a reasonable expectation of success.

To the extent that it is determined that any of these references do not disclose “selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model,” a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart ’414, Das Sharma, or Mezer, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such selection of registers to specify pre-equalization coefficient values in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart ’414, Das Sharma, or Mezer, each of which teach selecting registers to specify pre-equalization coefficient values. *See, e.g.*, Exhibits C-10-C-11, C-12 (claim 1[a]). A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art to store coefficients in registers and that using multiple registers was an option. *See, e.g.*, Exhibits C-10, C-11, C-12 (claim 1[a])‥ Indeed, using multiple registers with coefficient values is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of selecting from multiple registers corresponding to different channel models would thus require nothing more than the application of a known solution (incorporating multiple registers that correspond to different channel models), according to its established function (selecting between the multiple registers), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "updating the initial pre-equalizer coefficient values during a training phase," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such updating via a training phase in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, each of which teach updating coefficient values. *See, e.g.*, Exhibits C-10-C-11, C-12 (claim 1[b]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that you could use a training phase to update coefficients in the manner considered. *See, e.g.*, *id.* (claim 1[b]). Indeed, using a training phase to update coefficients is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of training would thus require nothing more than the application of a known solution (incorporating a training phase), according to its established function (updating coefficient values), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "using the updated pre-equalizer coefficient values to convey a transmit data stream," (claim 1[c]) a person of ordinary skill in the art would have been motivated to combine any of these references for the same reasons discussed related to the prior limitations related to Claim 1 of the '111 patent. A

POSITA would have understood that any selection of multiple registers or updating that occurs would ultimately be used to transmit the updated coefficient values to convey a data stream.

To the extent that it is determined that any of these references do not disclose that "the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Meze or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models with different insertion loss and package loss characteristics in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, each of which teach models with differing channel characteristics. *See, e.g.*, Exhibits C-10-C-11, C-12 (claims 2, 9). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that variations in channel models would account for variations of insertion loss and package loss characteristics. *See, e.g.*, *id.* (claim 1[a]). Indeed, using different models to account for different characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these different models would thus require nothing more than the application of a known solution (using multiple models), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "at least some of the different channel models presume different types of receiver equalization," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, each of which teach models with differing channel characteristics. *See, e.g.*, Exhibits C-10-C-11, C-12 (claims 3, 10). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that variations in channel models would account for variations in different types of receiver equalization. *See, e.g.*, Exhibits C-6, C-12 (claims 3, 10). Indeed, using different models to account for different characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these different models would thus require nothing more than the application of a known solution (using multiple models), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers," a person of ordinary skill in the art would have been motivated

to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, each of which teach determining a performance characteristic. *See, e.g.*, Exhibits C-10-C-11, C-12 (claim 4). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that the initial pre-equalize coefficients could be used to determine characteristics of registers. *See, e.g.*, *id.* (claim 4). Indeed, using the initial coefficients to determine register characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these initial coefficient values to determine varying register characteristics would thus require nothing more than the application of a known solution (using initial values), according to its established function (measuring different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "the performance characteristic is an error signal energy," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include a performance

characteristic that is an error signal energy in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer each of which teaches the performance characteristic relating to errors. *See, e.g.*, Exhibits C-10-C-11, C-12 (claims 5, 12, 18). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that error signal energy could be used as a performance characteristic. *See, e.g.*, *id.* (claims 5, 12, 18). Indeed, using an error signal energy as a performance characteristics but one of a finite number of known, predictable solutions to measuring performance. Implementing pre-equalization using an error signal energy as a performance characteristic thus requires nothing more than the application of a known solution (using an error signal energy as a performance characteristic), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "a performance characteristic is a bit error rate," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include a performance characteristic that is a bit error rate in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer each of which teaches the performance characteristic relating to errors. *See, e.g.*, Exhibits C-10-C-11, C-12

(claims 6, 13, 19). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that bit error rates could be used as a performance characteristic. *See, e.g.*, *id.* (claims 6, 13, 19). Indeed, using a bit error rate as a performance characteristics but one of a finite number of known, predictable solutions to measuring performance. Implementing pre-equalization using a bit error rate as a performance characteristic thus requires nothing more than the application of a known solution (using a bit error rate as a performance characteristic), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "updating the selected register with the updated pre-equalizer coefficient values," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, each of which teach determining a performance characteristic. *See, e.g.*, Exhibits C-10-C-11, C-12 (claims 7, 14, 15). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that training would require updating the coefficient values. *See, e.g.*, *id.* (claims 7, 14, 15). Indeed, updating coefficient values

is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using this updating would thus require nothing more than the application of a known solution (updating coefficient values), according to its established function (a training sequence), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such transmit filters to pre-equalize streams being transmitted in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, each of which teach transmit filters. *See, e.g.*, Exhibits C-10-C-11, C-12 (claims 8[a], 11[a], 16[a]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art to use transmit filters on a data stream. *See, e.g.*, Exhibits C-6, C-12 (claims 8[a], 11[a], 16[a]). Indeed, using a transmit filters on a data stream is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of transmit filters on a data stream would thus require nothing more than the application of a known solution (transmit filters on a data stream), according to its established function (apply the transmit filters), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the

art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters," a person of ordinary skill in the art would have been motivated to combine the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, or any combination thereof with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such multiple registers each of which contain initial coefficient values corresponding to different channel models in view of the teachings of at least the knowledge of a POSITA and/or one or more of the Stratix V Product, Stauffer, Lugthart '414, Das Sharma, or Mezer, each of which teach transmit filters. *See, e.g.*, Exhibits C-10-C-11, C-12 (claims 8[b], 11[b], 11[c], 16[b]). A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art to use multiple registers each of which contain initial coefficient values corresponding to different channel models. *See, e.g.*, Exhibits C-6, C-12 (claims 8[b], 11[b], 11[c], 16[b]). Indeed, using multiple registers each of which contain initial coefficient values corresponding to different channel models is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of multiple registers each of which contain initial coefficient values corresponding to different channel models would thus require nothing more than the application of a known solution (multiple registers each of which contain initial coefficient values corresponding to different channel models), according to its established function (selecting

on of the multiple registers), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so. Similarly, a POSITA would have been motivated to combine Rafie or Ciacci in view of either Balakrishnan or Fox or a combination thereof, and, for any claim that Credo asserts requires a cable, a pluggable module, or SerDes communications or similar feature, in further view of Lugthart (any of 414/434/993), Ran, Cecchi, or Mazzini. These references are in the same field of invention and have compatible and complementary teachings.

It would have been obvious to apply the adaptive pre-equalization techniques taught by Rafie or Ciacci (Exs. C-6 and C-7) to wireline communication in a cable, such as those taught by Lugthart (Exs. C-1, C-2, C-12), Ran (Ex. C-3), Cecchi (Ex. C-6), Mazzini (Ex. C-4). Both wireless and wireline systems suffer from channel impairments that degrade signal quality. Wireless systems are susceptible to multipath fading, interference, and frequency-selective attenuation. Wireline systems (e.g., coaxial or twisted pair cables) suffer from inter-symbol interference (ISI), attenuation, and reflections, particularly at higher frequencies or over longer distances. A POSITA would recognize that pre-equalization—where the transmitter compensates for expected channel impairments—can mitigate these effects in both domains. Given the known limitations of cable infrastructure—such as frequency-dependent loss, reflections due to impedance mismatches, and signal degradation over long distances—a POSITA would be motivated to implement any known solution that improves signal integrity and throughput, including those used in wireless communication. Implementing pre-equalization techniques in active cables would thus require nothing more than the application of a known solution (pre-equalization), according to its established function (improving transmission performance), yielding a predictable result (pre-

equalization in a wired cable). It is also the of known technique (pre-equalization) to improve similar devices (wireless and active cables) in the same way. It is also applying a known technique to a known device (active cables) ready for improvement to yield predictable results. Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that Rafie or Ciacci do not disclose that "the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics," a person of ordinary skill in the art would have been motivated to combine Rafie or Ciacci with Balakrishnan, Cecchi, or Kang with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models with different insertion loss and package loss characteristics in view of the teachings of at least the knowledge of a POSITA and/or one or more of Lutghart '431, Tremblay, Kang, Ran, Mazzini, Cecchi, Infiniband, Cornelius, or Balakrishnan, each of which teach updating coefficient values. See, e.g., Exhibits C-1, C-2, C-3, C-4, C-6, C-12] (claims 2, 9). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Balakrishnan, Cecchi, or Kang where they disclose the varying models having variations in channel characteristics with the embodiments of at least Rafie or Ciacci. See Exs. C-12. A POSITA would have been motivated to make such combinations with a reasonable expectation of success to achieve greater adaptability in cable applications. It was also well-known in the art that variations in channel models would account for variations of insertion loss and package loss characteristics. See Exs. C-12 (claim 1[a]). Indeed, using different models to account for different characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these different models

would thus require nothing more than the application of a known solution (using multiple models), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that Rafie does not disclose "updating the selected register with the updated pre-equalizer coefficient values," a person of ordinary skill in the art would have been motivated to combine Rafie in further view of Ciacci or Balakrishnan with a reasonable expectation of success. Ciacci discloses "For instance, the transmitter device can be configured to select a first path to adaptively initialize the coefficients before data is transmitted and a second path to continuously adjust the coefficients while data is being transmitted. More particularly, the processing control logic 102 can be configured to select the presence transition equalization path 114 when there are presence change events for the RF carrier signal (e.g., events corresponding to when the RF carrier signal transitions between being present and being absent on the antenna 106). Once data is being transmitted, with pre-equalization using the coefficients generated by path 114, the processing control logic 102 can select the adaptive feedback equalization path 112, which can include logic circuitry that is configured to continuously adjust the coefficients based upon feedback received from the antenna relative to the updated coefficients." Ciacci at 4:39-54. Balakrishnan discloses "Once frequency response of front-end components has been characterized, this information can be stored in the digital base band on a configuration register (CFR), and thereby used to specify gain coefficients of the digital pre-equalizer. Balakrishnan, ¶ 27. A POSITA would have understood it was beneficial to store the

updated coefficients in the proper register, which is the purpose of said register, especially in light of the teachings of Ciacci and Balakrishnan.

To the extent that it is determined that Ciacci does not disclose bi-directional communication, a person of ordinary skill in the art would have found it obvious to modify Ciacci to allow communications in two directions.

Similarly, a POSITA would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or a combination thereof, with a reasonable expectation of success.

To the extent that it is determined that any of these references do not disclose "selecting one of multiple registers to specify initial pre-equalizer coefficient values, each of the multiple registers corresponding to a different channel model," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such selection of registers to specify pre-equalization coefficient values in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claim 1[a]). For example, a POSITA would have been motivated to incorporate the embodiments at least each of Kang, Cornelius, Ran, Balakrishnan, and Cecchi where they disclose the use of multiple registers with equalization coefficients corresponding to different channel models. *See* Exs. C-3, C-9, C-12. As specific examples, Kang discloses "a plurality of registers," Cornelius discloses configuring "operational parameters, modes, and other aspects," Ran discloses multiple registers for a "Chip-to-Module (C2M) device," and Cecchi discloses different registers that correspond to different length cables with different pre-emphasis coefficients to compensate

for various factors. A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. Balakrishnan discloses storing "gain coefficients of the digital pre-equalizer" in a register. Balakrishnan ¶ 27. It was also well-known in the art to store coefficients in registers and that using multiple registers was an option. *See, e.g.*, Exhibit C-12 (claim 1[a]). Indeed, using multiple registers with coefficient values is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of selecting from multiple registers corresponding to different channel models would thus require nothing more than the application of a known solution (incorporating multiple registers that correspond to different channel models), according to its established function (selecting between the multiple registers), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "updating the initial pre-equalizer coefficient values during a training phase," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such updating via a training phase in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claim 1[b]). A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art that you could use a training phase to update coefficients in the manner considered. *See, e.g.*, *id.* (claim 1[b]). Indeed, using a training phase to

update coefficients is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of training would thus require nothing more than the application of a known solution (incorporating a training phase), according to its established function (updating coefficient values), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "using the updated pre-equalizer coefficient values to convey a transmit data stream," (claim 1[c]) a person of ordinary skill in the art would have been motivated to combine any of these references for the same reasons discussed related to the prior limitations related to Claim 1 of the '111 patent. A POSITA would have understood that any selection of multiple registers or updating that occurs would ultimately be used to transmit the updated coefficient values to convey a data stream.

To the extent that it is determined that any of these references do not disclose that "the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models with different insertion loss and package loss characteristics in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claims 2, 9). A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art that variations in channel

models would account for variations of insertion loss and package loss characteristics. *See, e.g.*, *id.* (claim 1[a]). Indeed, using different models to account for different characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these different models would thus require nothing more than the application of a known solution (using multiple models), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "at least some of the different channel models presume different types of receiver equalization," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claims 3, 10). A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art that variations in channel models would account for variations in different types of receiver equalization. *See, e.g.*, Exhibits C-3, C-9, C-12 (claims 3, 10). Indeed, using different models to account for different characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these different models would thus require nothing more than the application of a known solution (using

multiple models), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claim 4). A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art that the initial pre-equalize coefficients could be used to determine characteristics of registers. *See, e.g.*, *id.* (claim 4). Indeed, using the initial coefficients to determine register characteristics is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using these initial coefficient values to determine varying register characteristics would thus require nothing more than the application of a known solution (using initial values), according to its established function (measuring different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "the performance characteristic is an error signal energy," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include a performance characteristic that is an error signal energy in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claims 5, 12, 18). F. As a specific example, Cecchi discloses measuring error rate, Cornelius discloses measuring transmission errors, and Mezer discloses error signals. *Id*. A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art that error signal energy could be used as a performance characteristic. *See, e.g.*, *id.* (claims 5, 12, 18). Indeed, using an error signal energy as a performance characteristics but one of a finite number of known, predictable solutions to measuring performance. Implementing pre-equalization using an error signal energy as a performance characteristic thus requires nothing more than the application of a known solution (using an error signal energy as a performance characteristic), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "a performance characteristic is a bit error rate," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson,

Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include a performance characteristic that is a bit error rate in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claims 6, 13, 19). As a specific example, Cecchi discloses measuring error rate, Cornelius discloses measuring transmission errors, and Mezer discloses error signals. *Id.* A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art that bit error rates could be used as a performance characteristic. *See, e.g.*, *id.* (claims 6, 13, 19). Indeed, using a bit error rate as a performance characteristics but one of a finite number of known, predictable solutions to measuring performance. Implementing pre-equalization using a bit error rate as a performance characteristic thus requires nothing more than the application of a known solution (using a bit error rate as a performance characteristic), according to its established function (accounting for different channel characteristics), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose that "updating the selected register with the updated pre-equalizer coefficient values," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include the use of differing channel models that presume different types of receiver equalization in view of the teachings of at least the knowledge of a POSITA. *See,*

e.g., Exhibits C-3, C-9, C-12 (claims 7, 14, 15). A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art that training would require updating the coefficient values. *See, e.g.*, *id.* (claims 7, 14, 15). Indeed, updating coefficient values is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization using this updating would thus require nothing more than the application of a known solution (updating coefficient values), according to its established function (a training sequence), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "one or more transmit filters to each pre-equalize a corresponding serial symbol stream being transmitted to the port transceiver," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such transmit filters to pre-equalize streams being transmitted in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claims 8[a], 11[a], 16[a]). As specific examples, Kang discloses "a plurality of registers," Cornelius discloses configuring "operational parameters, modes, and other aspects," Ran discloses multiple registers for a "Chip-to-Module (C2M) device," and Cecchi discloses different registers that correspond to different length cables with different pre-emphasis coefficients to compensate for various factors. A POSITA would have been motivated to make such combinations to achieve greater adaptability in cable applications. It

was also well-known in the art to use transmit filters on a data stream. *See, e.g.*, Exhibits C-3, C-12 (claims 8[a], 11[a], 16[a]). Indeed, using a transmit filters on a data stream is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of transmit filters on a data stream would thus require nothing more than the application of a known solution (transmit filters on a data stream), according to its established function (apply the transmit filters), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent that it is determined that any of these references do not disclose "a controller having multiple registers, each of the multiple registers containing a set of initial coefficient values corresponding to a different channel model, the controller using one of the registers to set initial coefficient values for the one or more transmit filters.," a person of ordinary skill in the art would have been motivated to combine the SMP9 Cable in view of Ran, Kang, Das Sharma, Mezer, Aronson, Cecchi, Cornelius, Balakrishnan, or any combination thereof, with a reasonable expectation of success. It would have been obvious to modify the teachings of any of the above recited references to include such multiple registers each of which contain initial coefficient values corresponding to different channel models in view of the teachings of at least the knowledge of a POSITA. *See, e.g.*, Exhibits C-3, C-9, C-12 (claims 8[b], 11[b], 11[c], 16[b]). As specific examples, Kang discloses "a plurality of registers," Cornelius discloses configuring "operational parameters, modes, and other aspects," Ran discloses multiple registers for a "Chip-to-Module (C2M) device," and Cecchi discloses different registers that correspond to different length cables with different pre-emphasis coefficients to compensate for various factors. A POSITA would have

been motivated to make such combinations to achieve greater adaptability in cable applications. It was also well-known in the art to use multiple registers each of which contain initial coefficient values corresponding to different channel models. *See, e.g.*, Exhibits C-3, C-12 (claims 8[b], 11[b], 11[c], 16[b]). Indeed, using multiple registers each of which contain initial coefficient values corresponding to different channel models is but one of a finite number of known, predictable solutions to implement adaptability in pre-equalization. Implementing pre-equalization making use of multiple registers each of which contain initial coefficient values corresponding to different channel models would thus require nothing more than the application of a known solution (multiple registers each of which contain initial coefficient values corresponding to different channel models), according to its established function (selecting on of the multiple registers), yielding a predictable result (adaptability in pre-equalization). Therefore, a person of ordinary skill in the art would have been motivated to make such contemplated combinations and would have had a reasonable expectation of success in doing so.

To the extent any of the preambles are deemed to be limiting, a POSITA would have likewise been motivated to combine any of the above references for the above-mentioned reasons.

Complainant has yet to indicate a belief that any of the prior art references do not supply any of the claim limitations. Respondents' motivations to combine the prior art to supply other limitations may be amended or supplemented in view of Complainant's contentions regarding the missing limitations in the prior art references.

Secondary Considerations

Respondents are not aware of any secondary-considerations evidence demonstrating non-obviousness of the Asserted Claims of the '111 Patent. Complainants have not produced any documents related to secondary considerations, nor have Complainants identified any such

secondary considerations, let alone demonstrated a nexus between any such considerations and the alleged inventions of the Asserted Claims of the ’111 Patent.

As discussed in Appendix C, the prior art references confirm that the Asserted Claims of the ’111 Patent would have been obvious to a POSITA before the earliest possible priority date. Respondents reserve the right to supplement or modify these factors to address any evidence or arguments later identified by Complainants.

Invalidity Grounds Under 35 U.S.C. § 112

. Subject to Respondents’ reservation of rights above, Respondents identify their grounds of invalidity for the ’111 Patent based on lack of enablement, written description, and indefiniteness pursuant to 35 U.S.C. §§ 112(a) and (b) below. The terms recited below are invalid based on lack of enablement, written description, and indefiniteness pursuant to 35 U.S.C. §§ 112(a) and (b) under any scope of the claim terms. If, however, an overbroad construction is applied, at least under the overbroad constructions that Complainants appear to be applying to the Asserted Claims of the ’111 Patent, which go beyond (and are not adequately described or enabled by) the purported inventions allegedly disclosed in the ’252 Patent, the claims are invalid for that additional reason. Specifically, to the extent that Complainants assert that the Asserted Claims of the ’111 Patent are so broad as to cover the Respondents’ respective Accused Products and alleged domestic industry products, or to the extent that they may eventually be construed so broadly, such an interpretation or construction would render the Asserted Claims of the ’111 Patent invalid for failure to meet the requirements of 35 U.S.C. § 112. A more detailed discussion of Respondents’ written description, enablement, and indefiniteness defenses will be set forth in Respondents’ expert report(s) on invalidity.

Lack of Written Description and/or Enablement

The ’111 Patent does not provide sufficient written description to establish that the applicants were in possession of the alleged inventions recited in certain of the Asserted Claims at the time the ’111 Patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that “reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus.

The specification of the ’111 Patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the Asserted Claims without undue experimentation. To the extent the following limitations are definite, the application that became the ’111 Patent fails to sufficiently describe or enable them as required:

Term	Relevant Claim(s)	Basis
“wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics”	2, 9	The patent does not disclose and has insufficient disclosure to allow a POSITA to make and use a device “wherein at least some of the different channel models are for chip-to-module (C2M) channels with different insertion loss and package loss characteristics.”
“wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers”	4–7	The patent does not disclose and has insufficient disclosure to allow a POSITA to make and use a device “wherein said selecting includes using the initial pre-equalizer coefficient values to determine a performance characteristic for each of the multiple registers.”
“wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters”	14–15	The patent does not disclose and has insufficient disclosure to allow a POSITA to make and use a device “wherein the port transceiver

Term	Relevant Claim(s)	Basis
		generates updates for the coefficient values of the one or more transmit filters."
"wherein the port transceiver determines a performance characteristic for each register"	17–19	The patent does not disclose and has insufficient disclosure to allow a POSITA to make and use a device "wherein the port transceiver determines a performance characteristic for each register."
"a set of initial coefficient values for which the port transceiver determines a performance characteristic"	4, 11, 16	The patent does not disclose and has insufficient disclosure to allow a POSITA to make and use a device with "multiple registers containing a set of initial coefficient values for which the port transceiver determines a performance characteristic"
"wherein the performance characteristic is an error signal energy"	5, 12, 18	The patent does not disclose and has insufficient disclosure to allow a POSITA to make and use a device "wherein the performance characteristic is an error signal energy"

Indefiniteness

Certain of the Asserted Claims are invalid because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite for failing to particularly point out and distinctly claim the subject matter the applicants regard as their invention.

The following limitations recited in the Asserted Claims are indefinite in whole, in part or in combination:

Term	Relevant Claim(s)	Basis
"wherein at least some of the different channel models are for chip-to-module (C2M) channels	2, 9	The meaning of this term—read in light of the specification and prosecution history—cannot be

Term	Relevant Claim(s)	Basis
with different insertion loss and package loss characteristics”		determined with reasonable certainty because it is not clear what insertion loss and package loss characteristics are.
“wherein at least some of the different channel models presume different types of receiver equalization”	3, 10	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty because it is not clear what it means to “presume different types of receiver equalization.”
“using the initial pre-equalizer coefficient values to determine a performance characteristic” / “a set of initial coefficient values for which the port transceiver determines a performance characteristic” / “ determines a performance characteristic for each register”	4, 11, 16	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty because it is not clear what a “performance characteristic” of a “coefficient value” or “register” means or what using “initial pre-equalizer coefficient values to determine a performance characteristic” means.
“different channel model”	1, 8, 16	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty with regard to the scope of “different channel model.”
“updating the initial pre-equalizer coefficient values during a training phase” / “wherein the port transceiver generates updates for the coefficient values of the one or more transmit filters”	1, 14	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty what it means to “update” “initial pre-equalizer coefficient values.”
“training phase”	1	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty as to the distinction

Term	Relevant Claim(s)	Basis
		between a training phase and a non-training phase.
"wherein the performance characteristic is an error signal energy"	5, 12, 18	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty as to the meaning of an error signal energy.
"convey a data stream"	1	The meaning of this term—read in light of the specification and prosecution history—cannot be determined with reasonable certainty because it is not clear what it means to "convey" a data stream.
"the controller using one of the registers to set initial coefficient values for the one or more transmit filters" "the controller using one of the registers selected by the port transceiver to specify the initial coefficient values for the one or more transmit filters"	8, 11, 16	The claim recites structural components in combination with method steps (e.g., "using one of the registers to set"). *IPXL Holdings, L.L.C. v. Amazon.com*, Inc., 05-1009 (Fed. Cir. Nov. 21, 2005). The inclusion of these steps within an apparatus claim renders the claim indefinite as it does not provide a POSITA with reasonable certainty as to when infringement would occur.

Inequitable Conduct

Discovery is ongoing regarding the enforceability of the '111 Patent. To date, Complainants have refused to disclose any prior art known to Complainants, those involved in prosecution, or known to the inventors, outside of what is identified in the prosecution history and what was disclosed to it by third parties in litigation.

In view of Complainants' continued obstruction to relevant discovery, Respondents reserve the right to amend or supplement these contentions as discovery progresses including in response to, among other things, information learned in fact and/or expert discovery including identification of additional prior art, Complainants' positions on priority, infringement, claim construction, and/or invalidity, the Court's rulings, including on claim construction, changes in the Respondents' respective Accused Products, and in the event Complainants are permitted to revise infringement or domestic industry theories.

Improper Inventorship

Complainants have yet to provide discovery concerning each named inventor's participation, involvement, and contribution to the conception and reduction to practice of the alleged invention, including the dates of such participation, involvement, and contribution to the conception and reduction to practice on an element-by-element basis. *See, e.g.*, Respondents' Common Interrogatory No. 27. Respondents reserve their rights to contend, based on further discovery, that the Asserted Claims of the '111 Patent are invalid and/or unenforceable due to misjoinder of one or more inventors, nonjoinder of one or more inventors, or derivation of the claimed inventions from another.

* * *

7. CONCLUSION

For the reasons discussed above, and those revealed through further discovery, the Asserted Claims of the Asserted Patents are invalid.

Respondents expect to have experts provide relevant analysis. Respondents' contentions are without prejudice to Respondents' experts' analysis and opinions, which will be disclosed in accordance with the deadlines set forth in the Procedural Schedule in this Investigation (Order No. 7). Once those reports are served, they shall be deemed incorporated by reference herein.

Respondents reserve the right to supplement, amend, and/or revise its contentions in accordance with the Ground Rules (Order No. 2), the Procedural Schedule in this Investigation (Order No. 6), pursuant to 19 C.F.R. § 210.27(f), in response to any supplements, amendments, modifications, or clarifications of Complainants' validity contentions, in response to a decision on claim construction, based on Respondents' further investigation, or as may be warranted in light of ongoing discovery.

Date: June 26, 2025

Respectfully submitted,

/s/ Adam D. Swain

Adam D. Swain
ALSTON & BIRD LLP
950 F Street NW
Washington, DC 20004
Telephone: (202) 239-3300
Facsimile: (202) 239-3333
Adam.Swain@alston.com

Joshua M. Weeks
ALSTON & BIRD LLP
1201 West Peachtree Street, Suite 4900
Atlanta, GA 30309
Telephone: (404) 881-7000
Facsimile: (404) 881-7777
Joshua.Weeks@alston.com

Natalie C. Clayton
ALSTON & BIRD LLP
90 Park Ave.
New York, NY 10016
Telephone: (212) 210-9400
Facsimile: (212) 210-9444
Natalie.Clayton@alston.com

Dana Zottola
ALSTON & BIRD LLP
55 Second Street
Suite 2100
San Francisco, CA 94105
Telephone: (415) 243-1000
Facsimile: (415) 243-1001
Dana.Zottola@alston.com

Nicholas C. Marais
Mary I. Riolo
ALSTON & BIRD LLP
Vantage South End
1120 South Tryon Street
Suite 300
Charlotte, NC 29203
Telephone: (704) 444-1000
Facsimile: (704) 444-1001
Nic.Marais@alston.com
Mary.Riolo@alston.com

Counsel for Respondent Molex, LLC

/s/ Michael A. Pearson, Jr.
Paul F. Brinkman, P.C.
Michael A. Pearson, Jr.
John R. Rhine
Azaad Zimmermann
KIRKLAND & ELLIS LLP
1301 Pennsylvania Avenue, N.W.
Washington, DC 20004
Telephone: (202) 389-5000
Facsimile: (202) 389-5200

Russell E. Levine, P.C.
KIRKLAND & ELLIS LLP
333 West Wolf Point Plaza
Chicago, IL 60654
Telephone: (312) 862-2000
Facsimile: (312) 862-2200

Brandon H. Brown, P.C.
Eric Provost
KIRKLAND & ELLIS LLP
555 California Street
San Francisco, CA 94104
Telephone: (415) 439-1400
Facsimile: (415) 439-1500

Email: KE-TE-ITC@kirkland.com

Counsel for Respondent TE Connectivity Corp.

/s/ Thomas E. Garten
Brian R. Nester
Indranil Mukerji
R. Jason Fowler
Paul J. Wilson
Neal A. Hoopes
Scott C. Burger
COVINGTON & BURLING LLP
One CityCenter, 850 Tenth Street, NW
Washington, DC 20001-4956
Telephone: (202) 662-6000
Amphenol-COV-337@cov.com

Thomas E. Garten
COVINGTON & BURLING LLP
Salesforce Tower
415 Mission Street, Suite 5400
San Francisco, CA 94105-2533
Telephone: (415) 591-6000
Amphenol-COV-337@cov.com

Counsel for Respondent Amphenol Corporation

CERTAIN ACTIVE ELECTRICAL CABLES AND COMPONENTS THEREOF **Inv. No. 337-TA-1446**

CERTIFICATE OF SERVICE

I hereby certify that on June 26, 2025, copies of the foregoing served upon the following as indicated:

Steve Shahida, Esq. Office of Unfair Import Investigations **U.S. INTERNATIONAL TRADE COMMISSION** 500 E Street, S.W. Washington, D.C. 20436 Khashayar.Shahida@usitc.gov	☐ Via First Class Mail ☐ Via Courier (UPS) ☐ Via Hand Delivery ☒ Via Email
COUNSEL FOR COMPLAINANTS CREDO SEMICONDUCTOR INC., AND CREDO TECHNOLOGY GROUP LTD. Richard A. Sterba **FISH & RICHARDSON P.C.** 1000 Maine Ave., SW Washington, DC 20024 FRServiceCredoITCOffense@fr.com	☐ Via First Class Mail ☐ Via Courier (UPS) ☐ Via Hand Delivery ☒ Via Email
COUNSEL FOR RESPONDENT AMPHENOL CORPORATION Thomas E. Garten **COVINGTON & BURLING LLP** One City Center 850 Tenth Street, NW Washington, DC 20001 Amphenol-COV-337@cov.com	☐ Via First Class Mail ☐ Via Courier (UPS) ☐ Via Hand Delivery ☒ Via Email
COUNSEL FOR RESPONDENT TE CONNECTIVITY CORPORATION Paul F. Brinkman **KIRKLAND & ELLIS LLP** 1301 Pennsylvania Avenue, NW Washington, DC 20004 KE-TE-ITC@kirkland.com	☐ Via First Class Mail ☐ Via Courier (UPS) ☐ Via Hand Delivery ☒ Via Email

/s/ Bilal Iddinn
Bilal Iddinn
ITC Litigation Paralegal
ALSTON & BIRD
950 F Street, NW
Washington, DC 20004
Telephone: 202-239-3098
E-Mail: bilal.iddinn@alston.com